

Compal confidential

Schematics Document

Mobile AMD S1G2 CPU with ATI
RX781(NB) & SB700(SB) core logic

2008-11-07

REV:0.1



Security Classification	Compal Secret Data			Title Compal Electronics, Inc.		
Issued Date	2007/10/11	Deciphered Date	200810/11	Cover Sheet		
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Voltage Rails **O MEANS ON** **X MEANS OFF**

power plane	+B	+5VALW	+1.8V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +VGA_CORE +1.2V_HT +CPU_CORE_0 +CPU_CORE_1 +CPU_CORE_NB
State	+5VL	+1.2VALW		
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

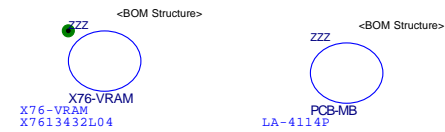
Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

DEBUG@ : means just reserve for debug.



I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0
ACCELEROMETER	3A	0 0 1 1 1 1 0 1 0

EC SM Bus1 address EC SM Bus2 address

Device	HEX	Address	Device	HEX	Address
Smart Battery	16H	0001 011X b	AD1032-2 CPU	9AH	1001 101X b
24C16	A0H	1010 000X b	AD1032-1 VGA	98H	1001 100X b
CPU SIC interface	98H	1001 100X b			

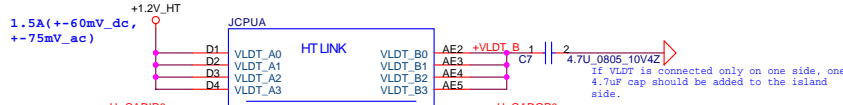
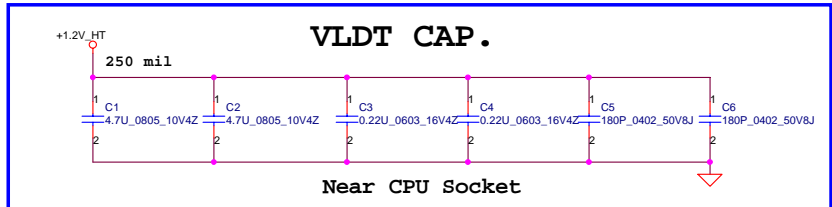
SMBUS Control Table

	SOURCE	THERMAL SENSOR VGA M82-SE ADM1032	BATT	SERIAL EEPROM	THERMAL SENSOR CPU & ADM1032	SODIMM I / II	CLK CHIP	WL MINI CARD Slot 1	LCD	HDMI	CRT	Temp Sensor
SMB_EC_CK1	KB926	X	V	X	X	X	X	X	X	X	X	X
SMB_EC_DA1	KB926	V	X	X	V	X	X	X	X	X	X	X
SMB_EC_CK2	KB926	V	X	X	V	X	X	X	X	X	X	X
SMB_EC_DA2	KB926	V	X	X	V	X	X	X	X	X	X	X
SCL	VGA M82-SE	X	X	X	X	X	X	X	V	X	X	X
SDA	VGA M82-SE	X	X	X	X	X	X	X	V	X	X	X
DDC4CLK	VGA M82-SE	X	X	X	X	X	X	X	X	V	X	X
DDC4DATA	VGA M82-SE	X	X	X	X	X	X	X	X	V	X	X
DDC3CLK	VGA M82-SE	X	X	X	X	X	X	X	X	X	V	X
DDC3DATA	VGA M82-SE	X	X	X	X	X	X	X	X	X	V	X
SCL0	SB700	X	X	X	X	V	V	X	X	X	X	V
SDA0	SB700	X	X	X	X	V	V	X	X	X	X	V
SCL1	SB700	X	X	X	X	X	X	V	X	X	X	X
SDA1	SB700	X	X	X	X	X	X	V	X	X	X	X
SCL2	SB700	X	X	X	X	X	X	X	X	X	X	X
SDA2	SB700	X	X	X	X	X	X	X	X	X	X	X
SCL3	SB700	X	X	X	X	X	X	X	X	X	X	X
SDA3	SB700	X	X	X	X	X	X	X	X	X	X	X

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				Size Custom	Document Number
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<10> H_CADIP[0..15] H_CADIP[0..15]
 <10> H_CADIN[0..15] H_CADIN[0..15]

H_CADOP[0..15] H_CADOP[0..15] <10>
 H_CADON[0..15] H_CADON[0..15] <10>



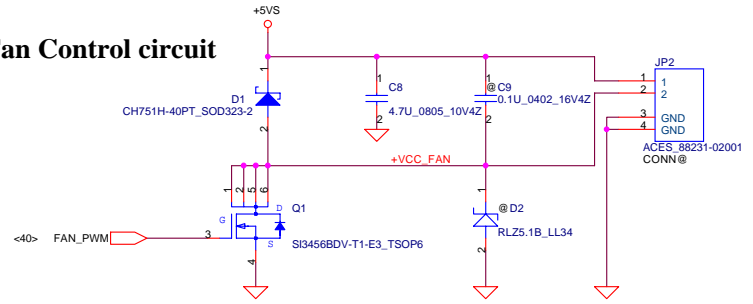
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H_CADIN0	E2	L0_CADIN_L0	L0_CADOUT_L0	AC1	H_CADON0
H_CADIP1	E1	L0_CADIN_H1	L0_CADOUT_H1	AC2	H_CADOP1
H_CADIN1	E1	L0_CADIN_L1	L0_CADOUT_L1	AC3	H_CADON1
H_CADIP2	G3	L0_CADIN_H2	L0_CADOUT_H2	AB1	H_CADOP2
H_CADIN2	G2	L0_CADIN_L2	L0_CADOUT_L2	AA1	H_CADON2
H_CADIP3	G1	L0_CADIN_H3	L0_CADOUT_H3	AA2	H_CADOP3
H_CADIN3	H1	L0_CADIN_L3	L0_CADOUT_L3	AA3	H_CADON3
H_CADIP4	J1	L0_CADIN_H4	L0_CADOUT_H4	W2	H_CADOP4
H_CADIN4	I3	L0_CADIN_L4	L0_CADOUT_L4	W3	H_CADON4
H_CADIP5	K1	L0_CADIN_H5	L0_CADOUT_H5	W1	H_CADOP5
H_CADIN5	L2	L0_CADIN_L5	L0_CADOUT_L5	U1	H_CADON5
H_CADIP6	L1	L0_CADIN_H6	L0_CADOUT_H6	U2	H_CADOP6
H_CADIN6	L3	L0_CADIN_L6	L0_CADOUT_L6	U3	H_CADON6
H_CADIP7	M1	L0_CADIN_H7	L0_CADOUT_H7	T1	H_CADOP7
H_CADIN7	N2	L0_CADIN_L7	L0_CADOUT_L7	R1	H_CADON7
H_CADIP8	E5	L0_CADIN_H8	L0_CADOUT_H8	AD4	H_CADOP8
H_CADIN8	F5	L0_CADIN_L8	L0_CADOUT_L8	AD3	H_CADON8
H_CADIP9	F3	L0_CADIN_H9	L0_CADOUT_H9	AD5	H_CADOP9
H_CADIN9	F4	L0_CADIN_L9	L0_CADOUT_L9	AC5	H_CADON9
H_CADIP10	G5	L0_CADIN_H10	L0_CADOUT_H10	AB4	H_CADOP10
H_CADIN10	H5	L0_CADIN_L10	L0_CADOUT_L10	AB3	H_CADON10
H_CADIP11	H3	L0_CADIN_H11	L0_CADOUT_H11	AB5	H_CADOP11
H_CADIN11	H4	L0_CADIN_L11	L0_CADOUT_L11	AA5	H_CADON11
H_CADIP12	K3	L0_CADIN_H12	L0_CADOUT_H12	Y5	H_CADOP12
H_CADIN12	K4	L0_CADIN_L12	L0_CADOUT_L12	W5	H_CADON12
H_CADIP13	L5	L0_CADIN_H13	L0_CADOUT_H13	V4	H_CADOP13
H_CADIN13	M5	L0_CADIN_L13	L0_CADOUT_L13	V3	H_CADON13
H_CADIP14	M3	L0_CADIN_H14	L0_CADOUT_H14	V5	H_CADOP14
H_CADIN14	M4	L0_CADIN_L14	L0_CADOUT_L14	U5	H_CADON14
H_CADIP15	N5	L0_CADIN_H15	L0_CADOUT_H15	T4	H_CADOP15
H_CADIN15	P5	L0_CADIN_L15	L0_CADOUT_L15	T3	H_CADON15

<10> H_CLKIP0 J3 L0_CLKIN_H0 L0_CLKOUT_H0 Y1 H_CLKOP0 <10>
 <10> H_CLKIN0 J2 L0_CLKIN_L0 L0_CLKOUT_L0 W4 H_CLKON0 <10>
 <10> H_CLKIP1 K5 L0_CLKIN_H1 L0_CLKOUT_H1 Y3 H_CLKOP1 <10>
 <10> H_CLKIN1 K6 L0_CLKIN_L1 L0_CLKOUT_L1 Y4 H_CLKON1 <10>

<10> H_CTLIP0 N1 L0_CTLIN_H0 L0_CTLOUT_H0 R2 H_CTLOP0 <10>
 <10> H_CTLIN0 P1 L0_CTLIN_L0 L0_CTLOUT_L0 T5 H_CTLON0 <10>
 <10> H_CTLIP1 P3 L0_CTLIN_H1 L0_CTLOUT_H1 T6 H_CTLOP1 <10>
 <10> H_CTLIN1 P4 L0_CTLIN_L1 L0_CTLOUT_L1 R5 H_CTLON1 <10>

FOX_PZ6382A-284S-41F_GRIFFIN
 CONN @
 Athlon 64 S1
 Processor Socket

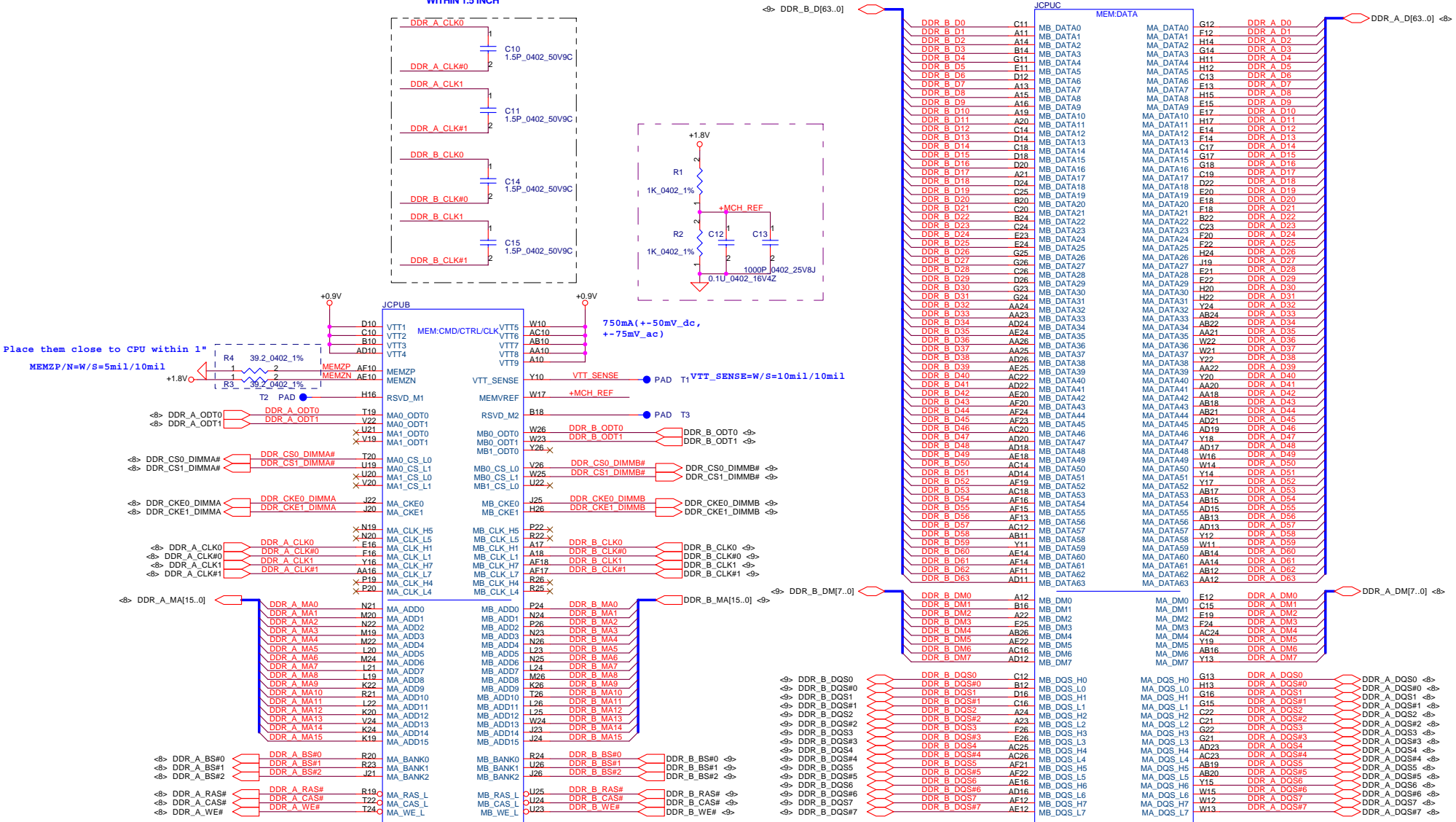
PWM Fan Control circuit



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Processor DDR2 Memory Interface

PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH



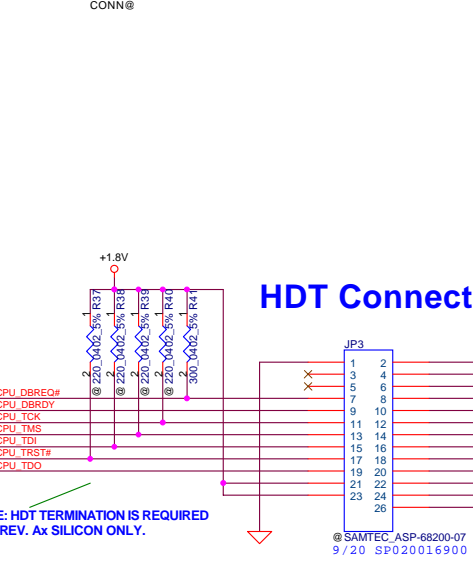
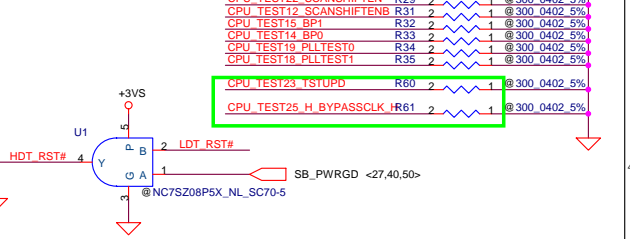
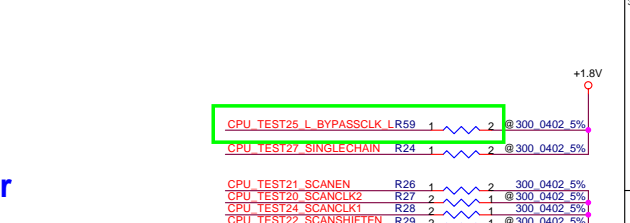
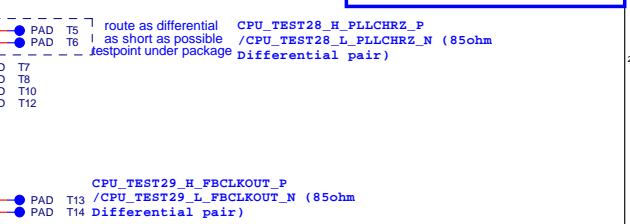
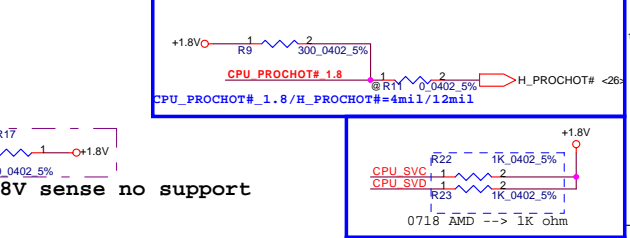
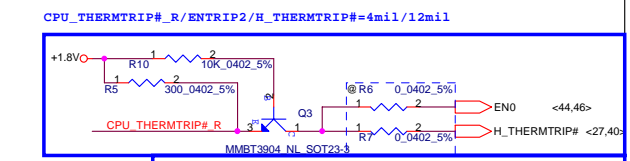
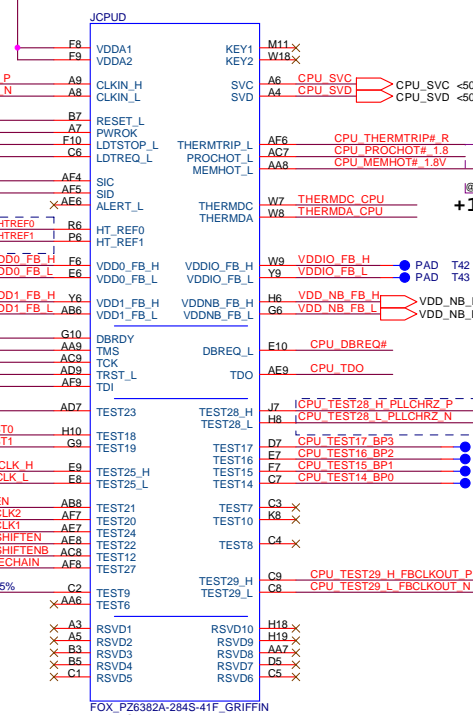
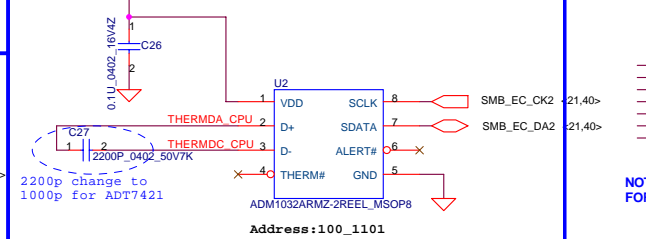
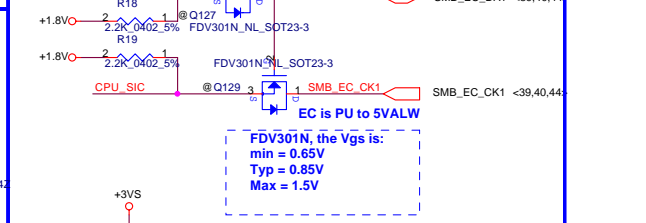
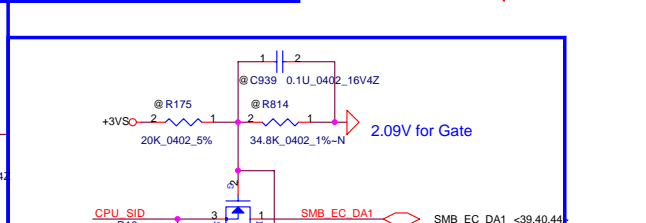
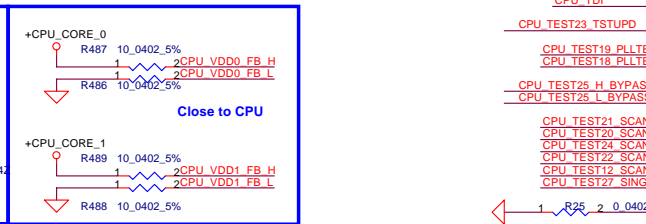
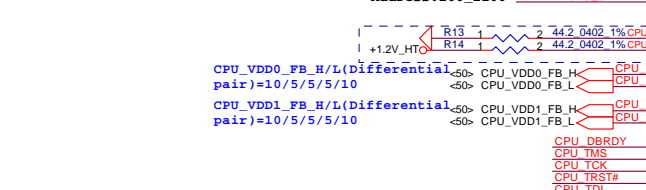
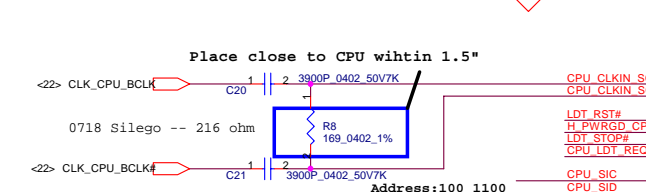
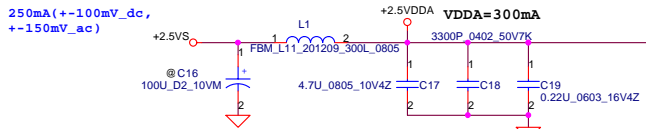
Place them close to CPU within 1"

FOX P26382A-284S-41F_GRIFFIN
Athlon 64 S1
Processor
Socket

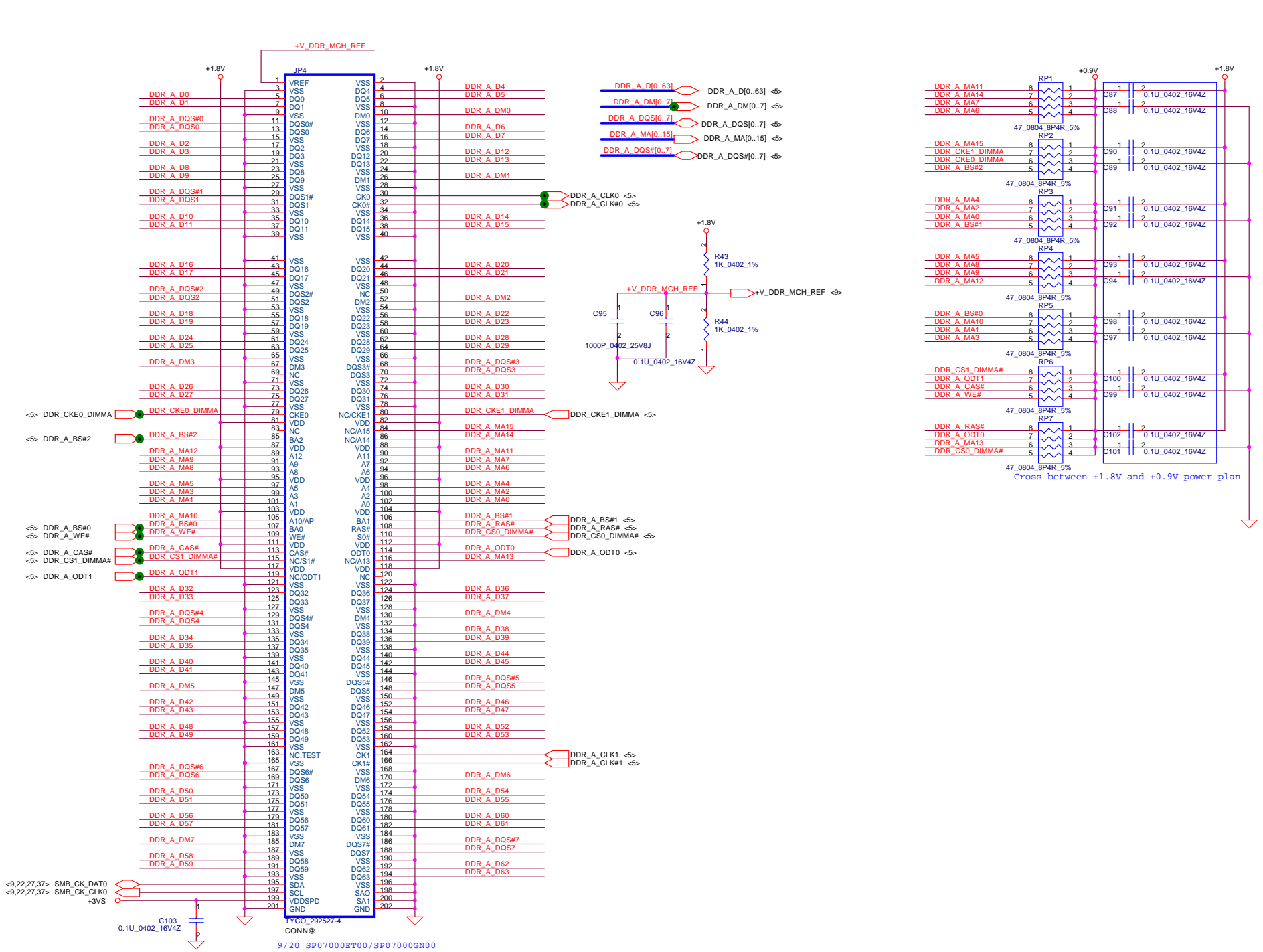
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Athlon 64 S1
Processor Socket
CONN@

CONN@

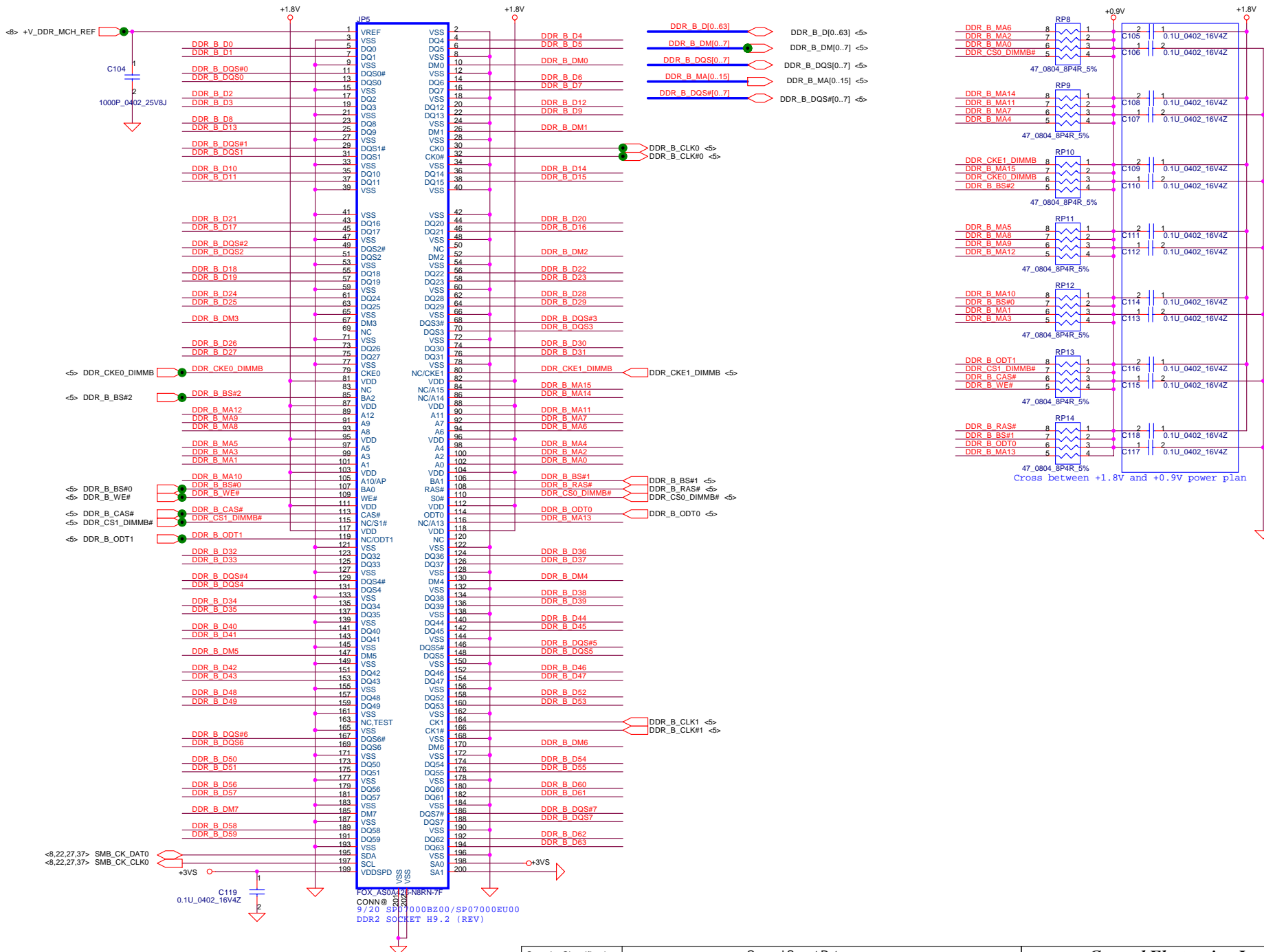
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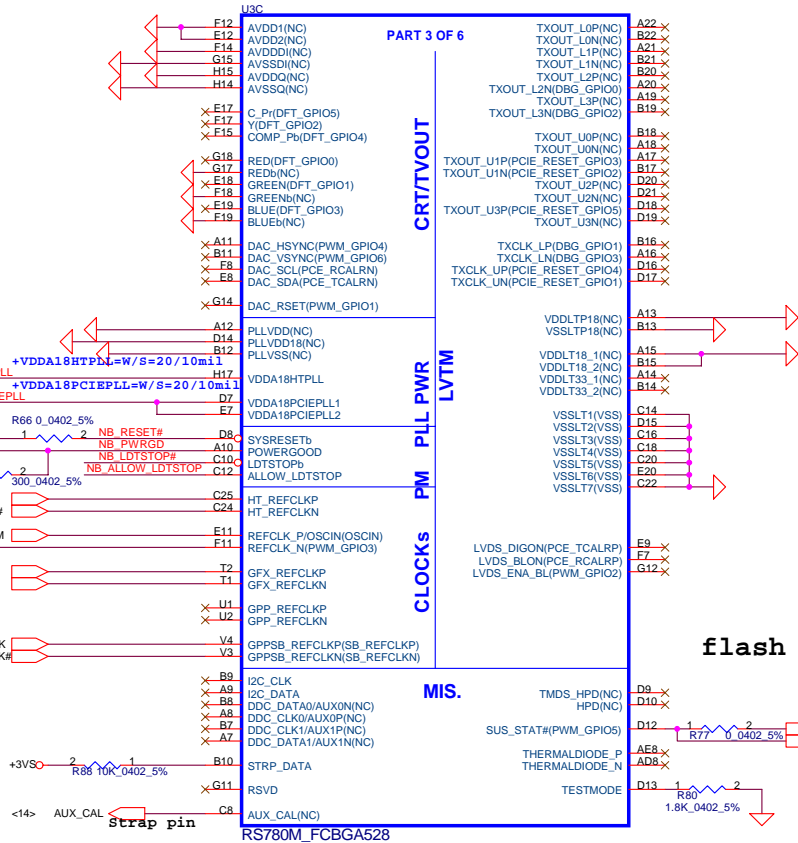
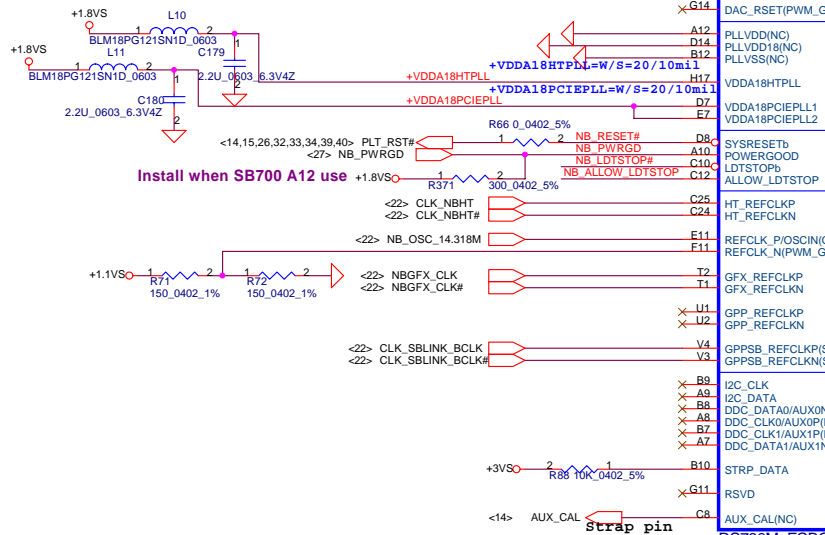
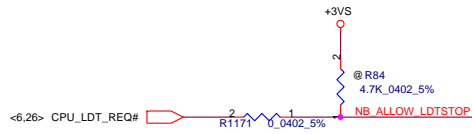
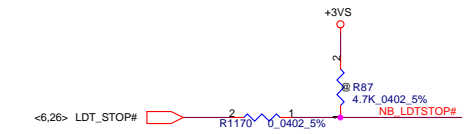
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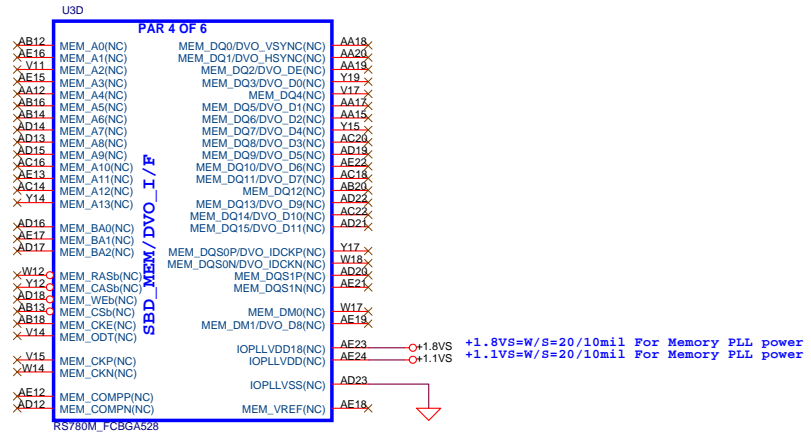
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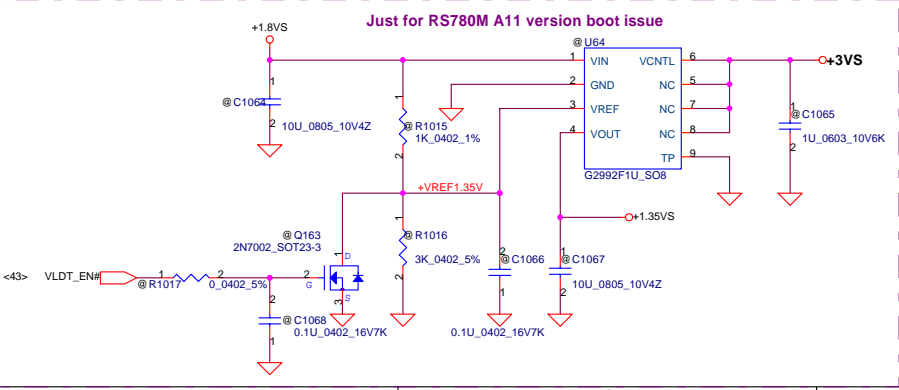
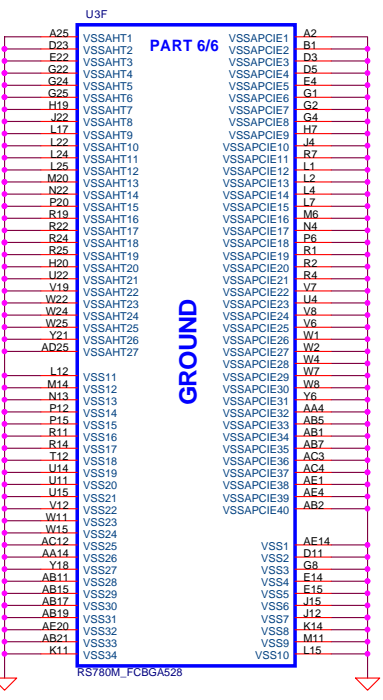
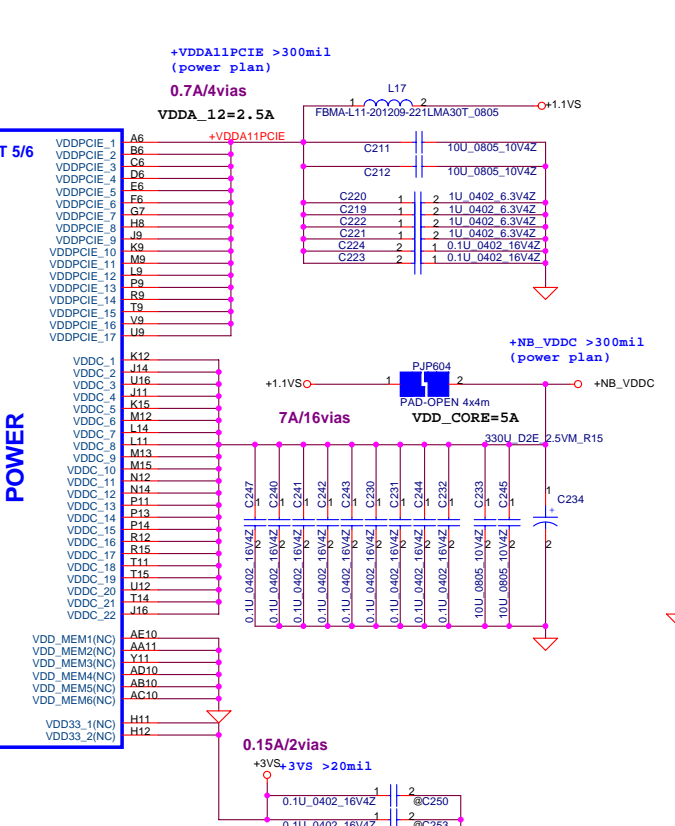
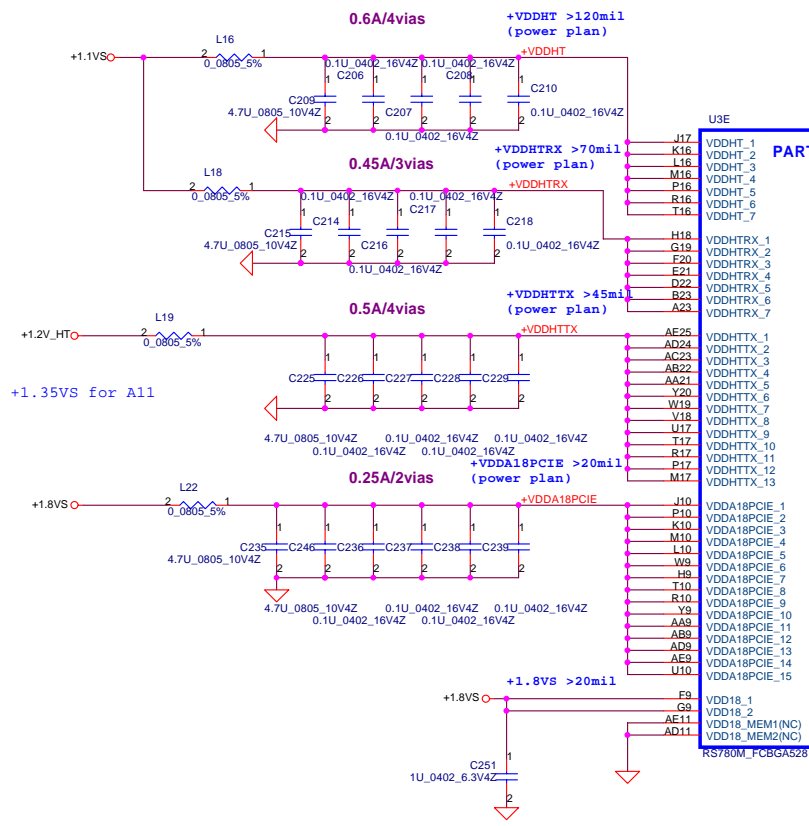
flash issue check IALAA

SUS_STAT# <27>
SUS_STAT_R# <14> Strap pin
NB temp to SB

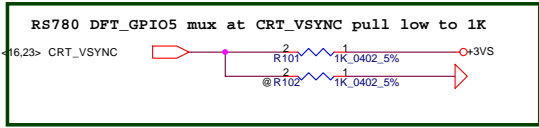
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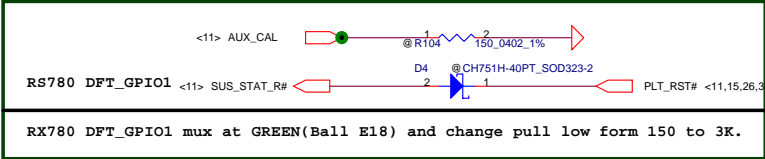


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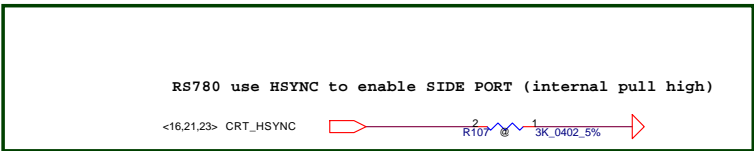
DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.
 1 : Disable (RS740) Enable (RX780, RS780)
 0 : Enable (RS740) Disable (RX780, RS780)
 PIN: RS740-->RS780_AUX_CAL; RX780-->NB_TV_C; RS780--> VSYNC#



DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
 1 : Bypass the loading of EEPROM straps and use Hardware Default Values
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
 RS740/RX780: DFT_GPIO1 RS780:SUS_STAT



DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

RX780: Enables the Test Debug Bus using PCIE bus
 1 : Disable (Can still be enabled using nbcfg register access)
 0 : Enable

RS740/RS780: Enables Side port memory (RS780 use HSYNC#)
 1. Disable (RS740/RS780)
 0 : Enable (RS740/RS780)

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				Custom	LA-4114P
Date: Thursday, November 06, 2008				Sheet	14 of 54

<10> PCIE_GTX_C_MRX_P[0..15] ← PCIE GTX C MRX P[0..15]
 <10> PCIE_GTX_C_MRX_N[0..15] ← PCIE GTX C MRX N[0..15]
 <10> PCIE_MTX_C_GRX_P[0..15] ← PCIE MTX C GRX P[0..15]
 <10> PCIE_MTX_C_GRX_N[0..15] ← PCIE MTX C GRX N[0..15]

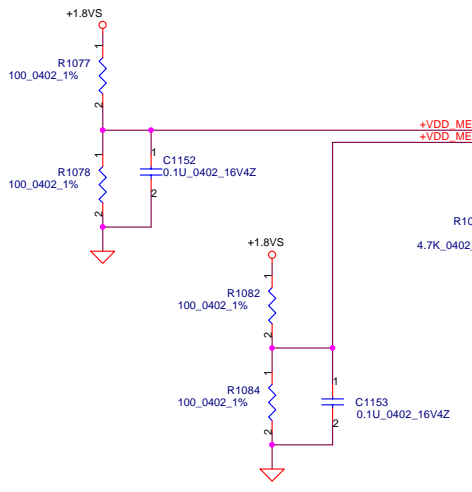
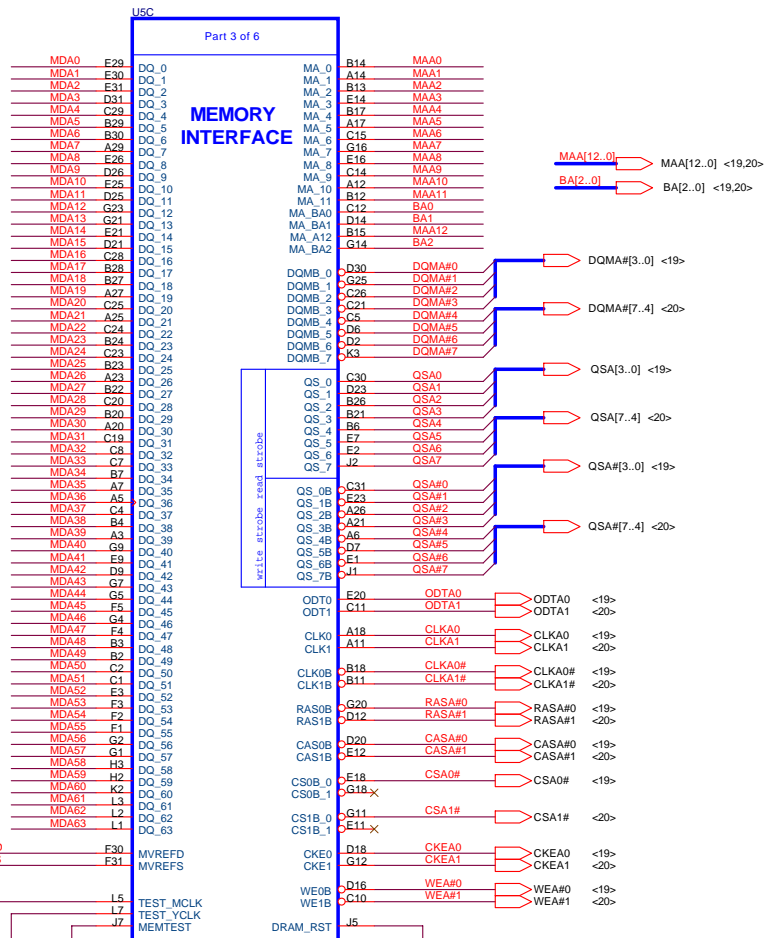
PCIE LANE REVERSAL

PCIE LANE REVERSAL

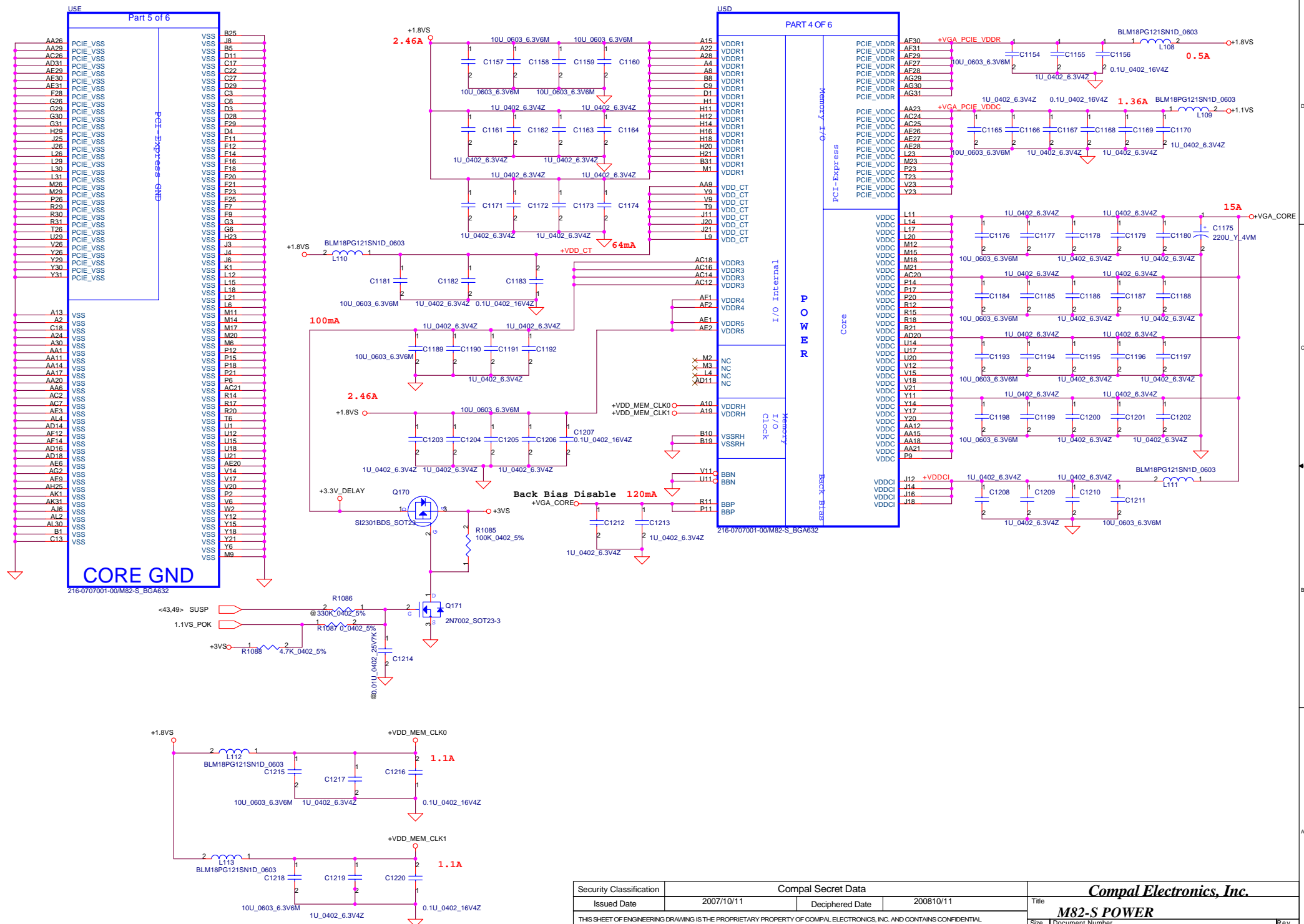


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			Date:	Thursday, November 06, 2008	Sheet 15 of 54

<20> MDA[63..32] ← MDA[63..32]
 <19> MDA[31..0] ← MDA[31..0]



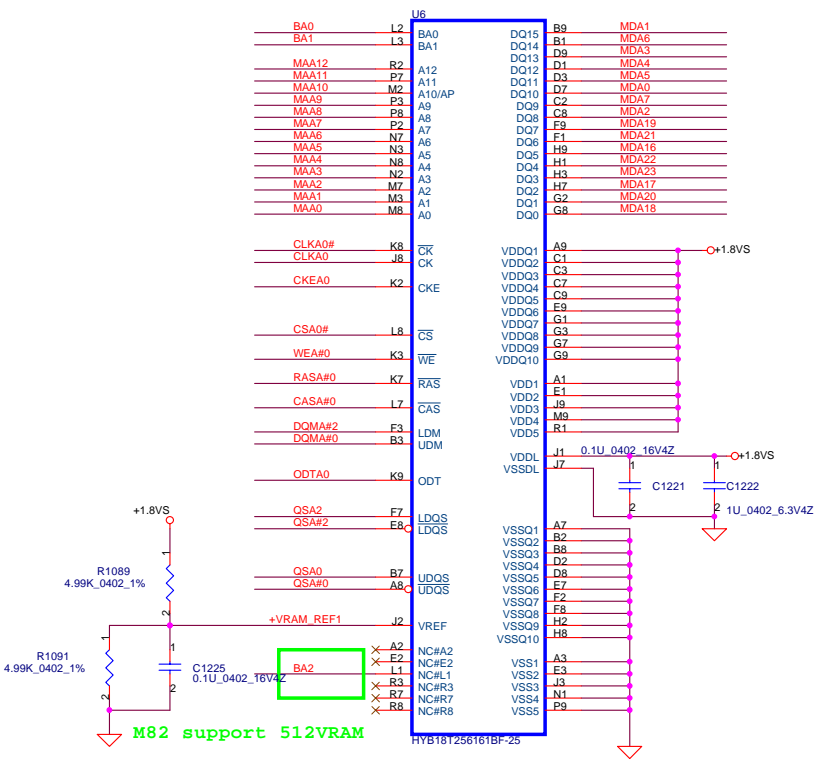
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Issued Date	2007/10/11	Deciphered Date	2008/10/11	Compal Electronics, Inc.	
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				LA-4114P	Rev 0.1
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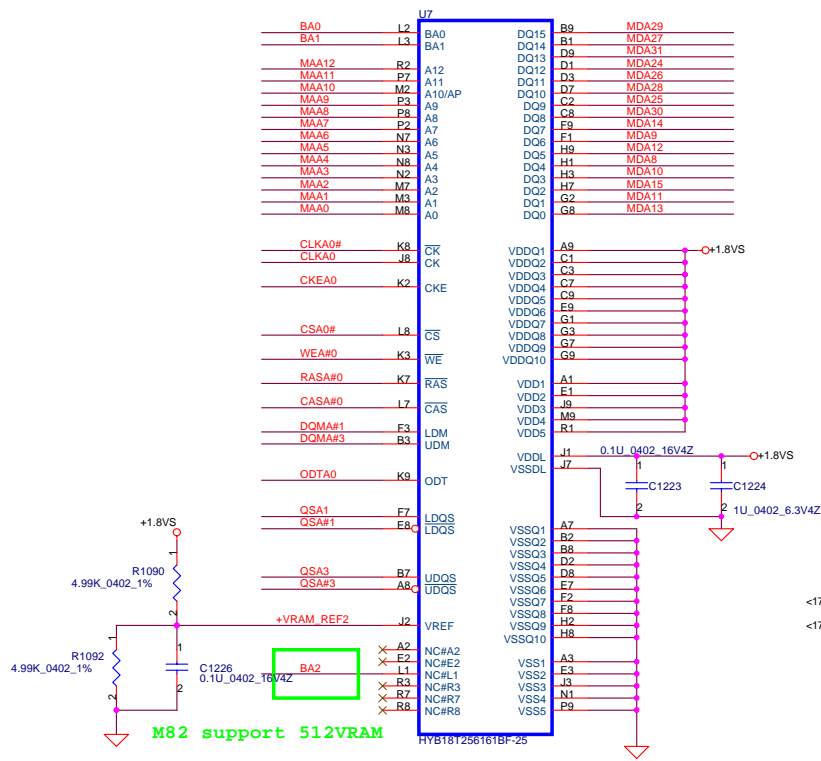
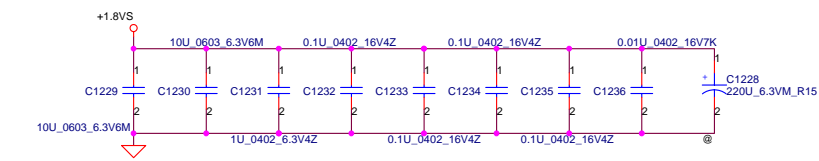
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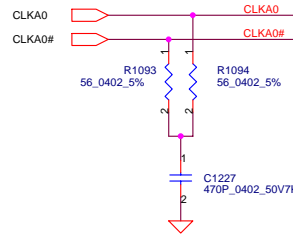
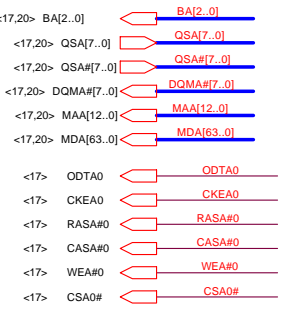
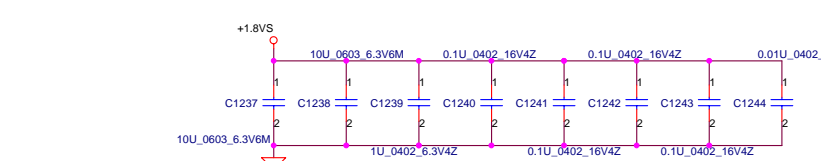
Compal Electronics, Inc.		
Title M82-S POWER		
Size	Document Number LA-4114P	Rev 0.1
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SA00002A600(QIMONDA) S IC D2 32M16/500 HYB18T512161B2F-20 84P
 SA00002AJ10(SAMSUNG) IC D2 32M16/500 K4N51163QG-HC20 FBGA84

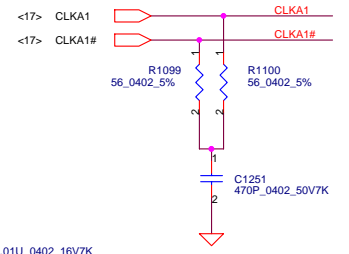
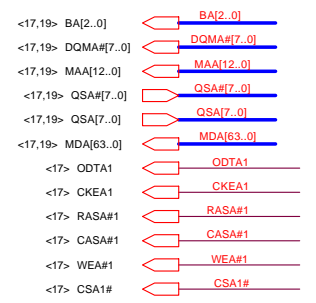
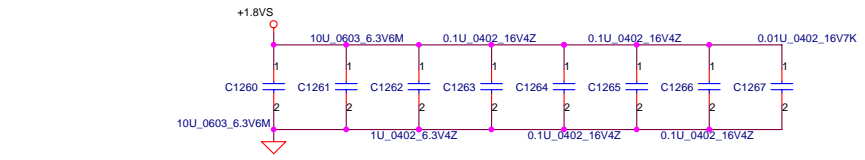
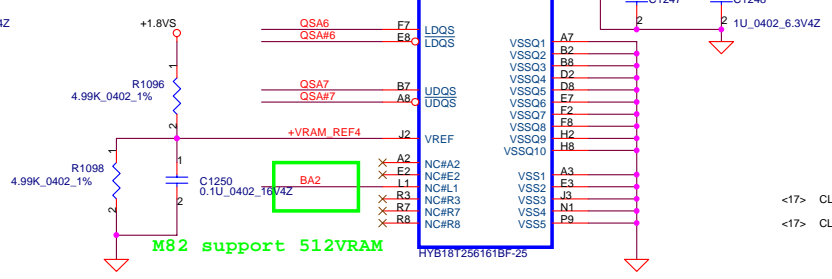
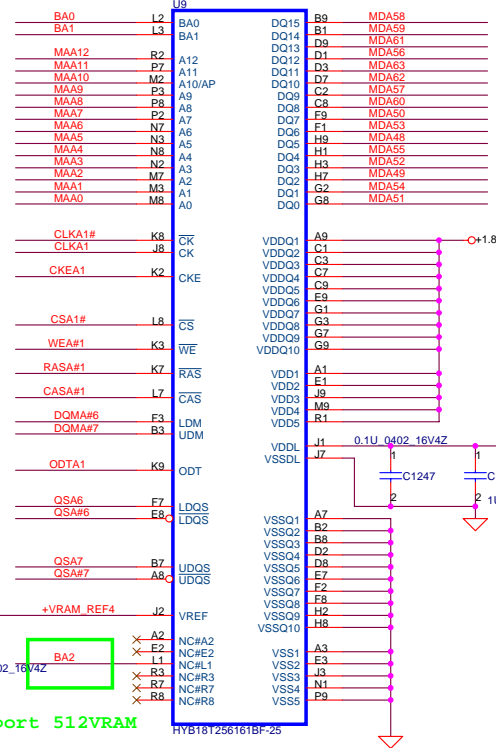
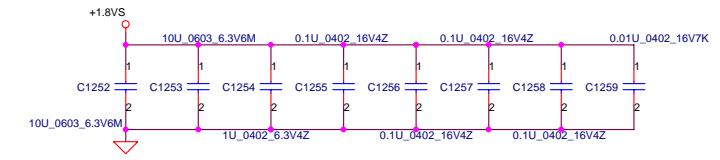
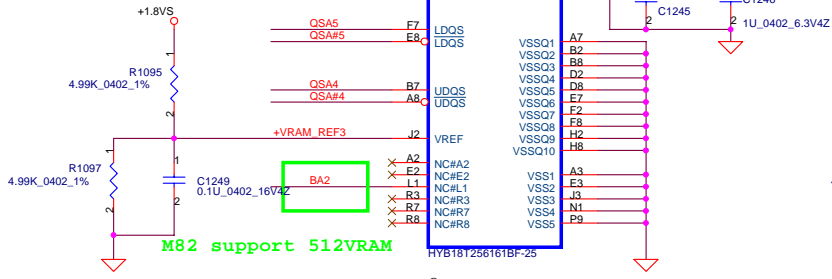
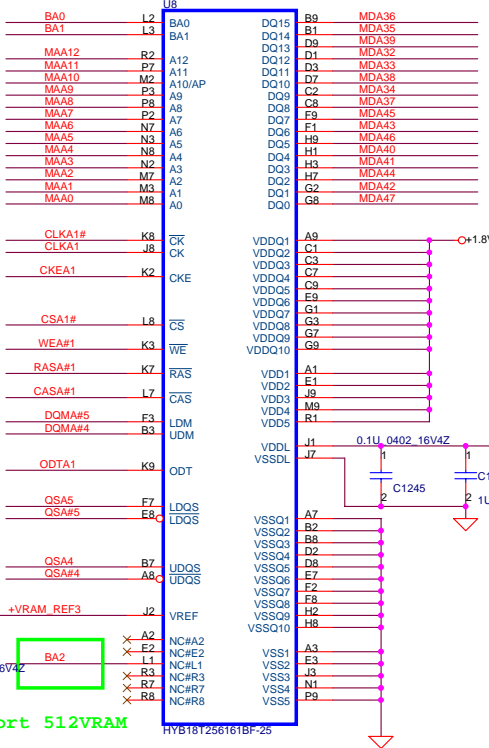


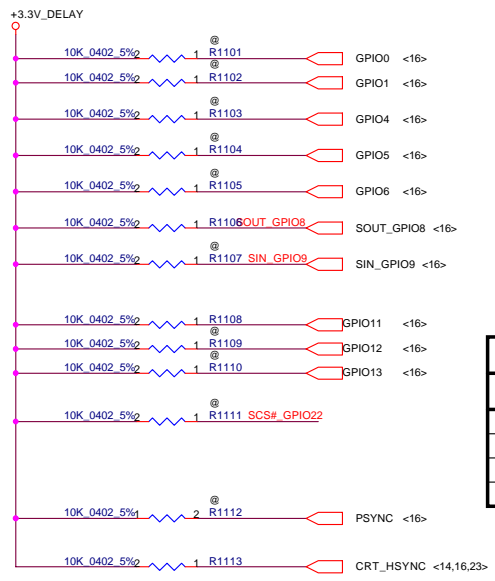
SA00002A600(QIMONDA) S IC D2 32M16/500 HYB18T512161B2F-20 84P
 SA00002AJ10(SAMSUNG) IC D2 32M16/500 K4N51163QG-HC20 FBGA84



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			M82-S VRAM	
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ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESE

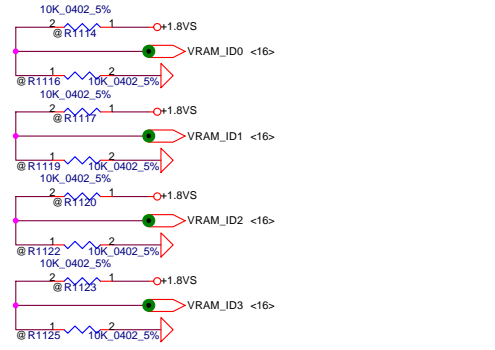
GPIO2 GPIO3 GPIO5 GPIO6 DVALID H2SYNC V2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

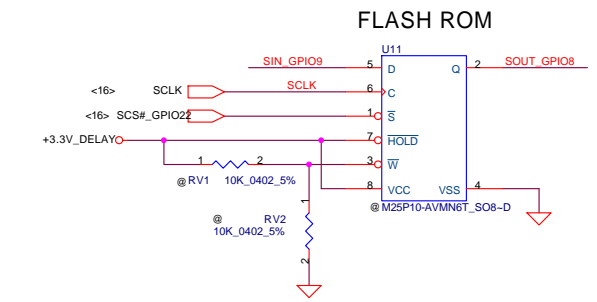
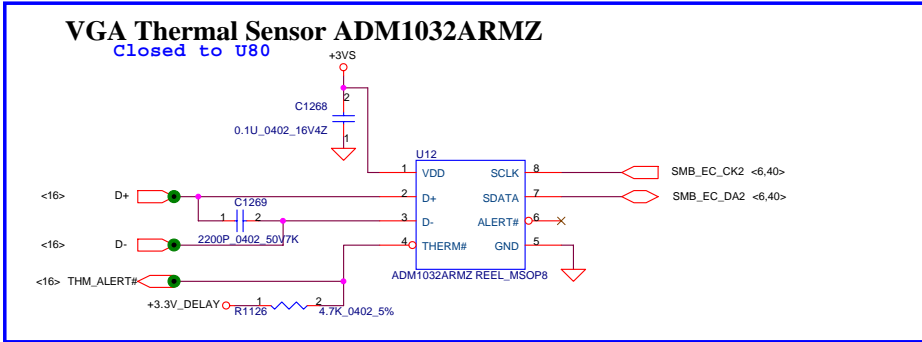
GENERICC GPIO21_BB_EN GPIO_28_TDO

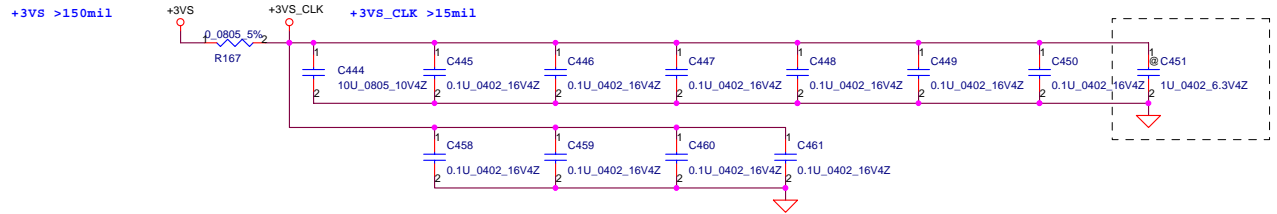
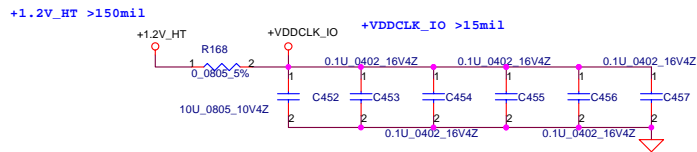
GPIO9 = 0 (BIOS_ROM_EN = 0)	
GPIO[13:11]	MEMORY SIZE
0 0 0	128MB
0 0 1	256MB
0 1 0	64MB
1 0 0	512MB

STRAPS	FN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED MBX
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLES	0
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0
BIF_GEN2_EN_A	GPIO5	PCI-E 5.0GT/s or 2.5 GT/s select	0
DEBUG_I2C_ENABLE	GPIO6	Internal use only	0
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO(M8X)	1
ROMIDCFG[3:0]	GPIO [9,13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 1 0 1
BIOS_ROM_EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	0
BIF_VGA_DIS	PSYNC	VGA ENABLED==0 is enable	0
BIF_HDMI_EN	HSYNC	HDMI ENABLE	1

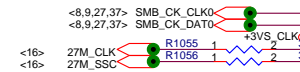
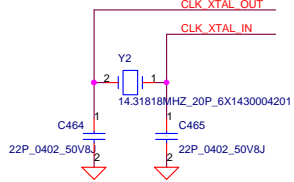


STRAPS	PIN	GPU	Project	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 3,2,1,0
VRAM_ID[3:0]	DVPDATA (23,22,21,20)	M82M-XT	Rachman 1.2	512M(x4)	Samsung 64Mx16 1.8V	SA00002MD00	0 0 0 0
			Rachman 1.2	256M(X4)	Samsung 32Mx16 1.8V	SA00002AJ10	0 0 0 1
				512M(x4)	Hynix 64Mx16 1.8V		0 0 1 0
			Rachman 1.1	256M(X4)	Hynix 32Mx16 1.8V	SA00002DL00	0 0 1 1
			Rachman 1.1	256M(X4)	Qimonda 32Mx16 1.8V	SA00002A600	0 1 0 0
			Rachman 1.2	512M(x4)	Qimonda 64Mx16 1.8V	SA00002MF00	0 1 0 1

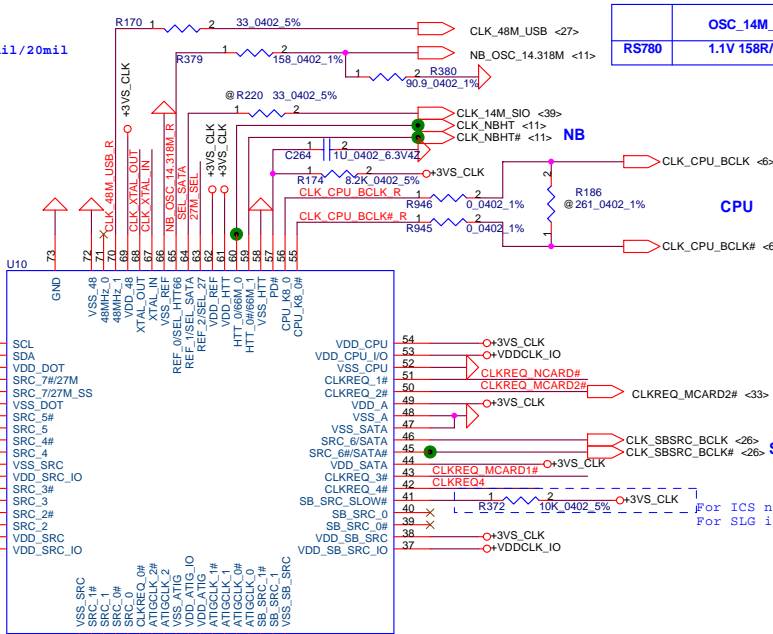
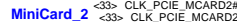




CLK_XTAL_IN/OUT=width
/spacing/Others=10mil/10mil/20mil

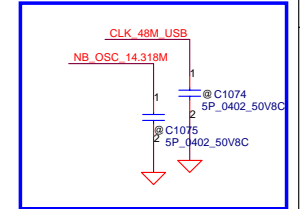


MiniCard_1(delete)



	OSC_14M_NB
RS780	1.1V 158R/90.0R

EMI Caps for single end clock.

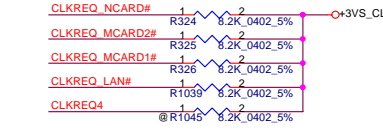


CPU

SB SRC

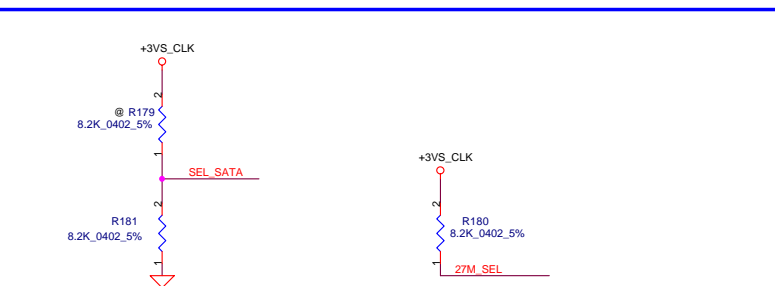
For ICS need to pull high.
For SLG is NC

CLKREQ_NCARD#, CLKREQ_LAN#, CLKREQ4,
CLKREQ_MCARD2#=width
/spacing/Others=8mil/8mil/12mil



NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P		vref
REFCLK_N	14M SE (1.8V)	14M SE (1.1V)
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)



SEL_SATA	1	configure as SATA output
	0	configure as normal SRC(SRC_6) output
	*	default

Use voltage divider resistor R379 & R380 to pull low

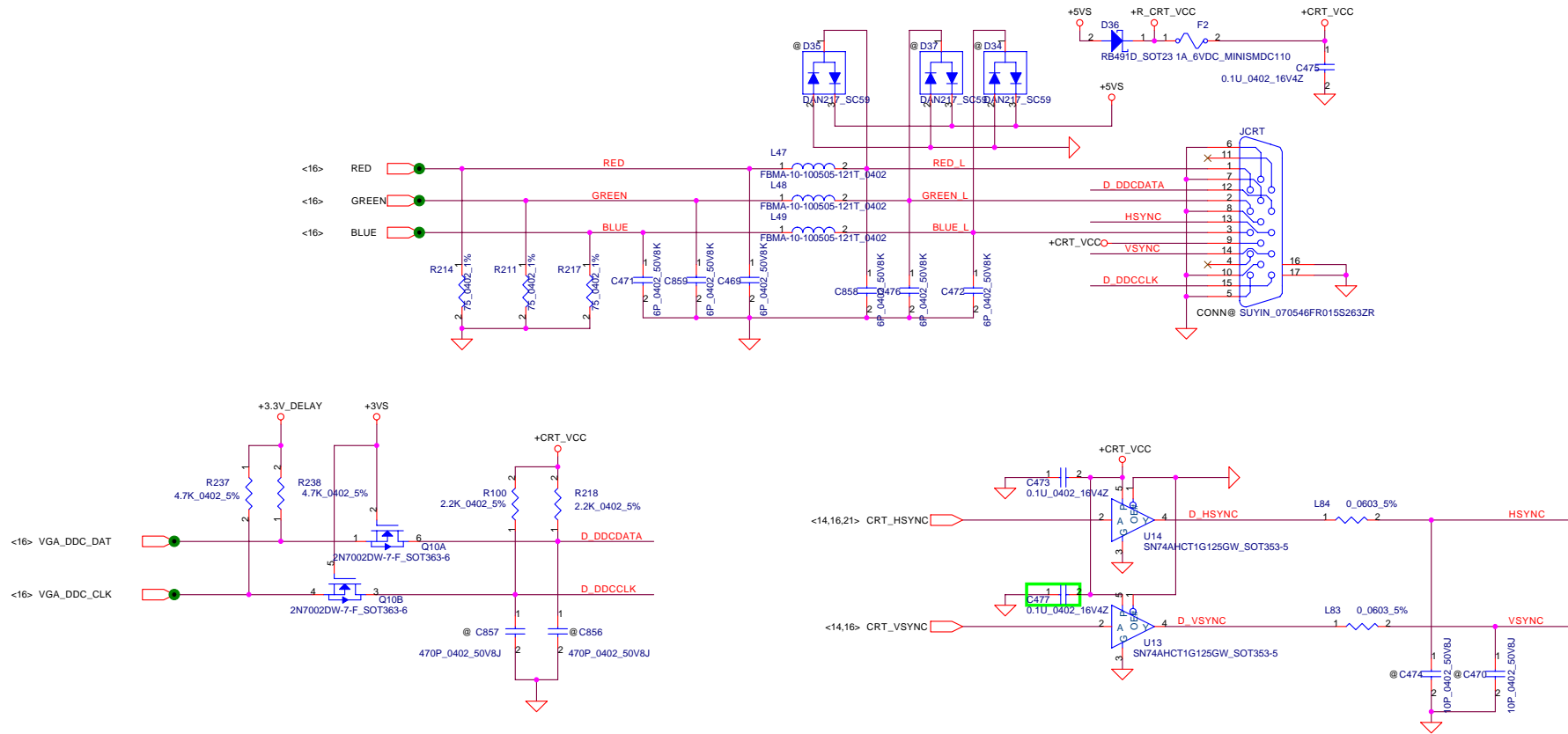
NB_OSC_14.318M	1	configure as single-ended 66MHz output
	0	configure as differential 100MHz output
	*	default

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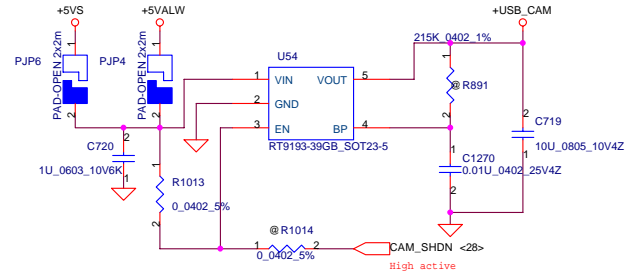
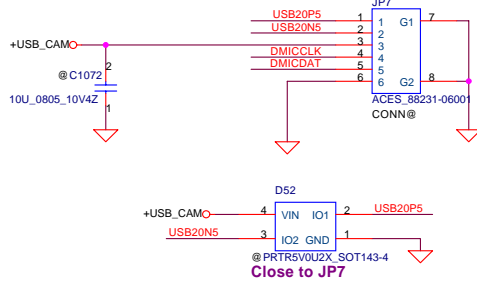
Title			Compal Electronics, Inc.		
			Clock generator		
Size	Document Number		Rev		
Custom	LA-4114P		0.1		
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CRT CONNECTOR

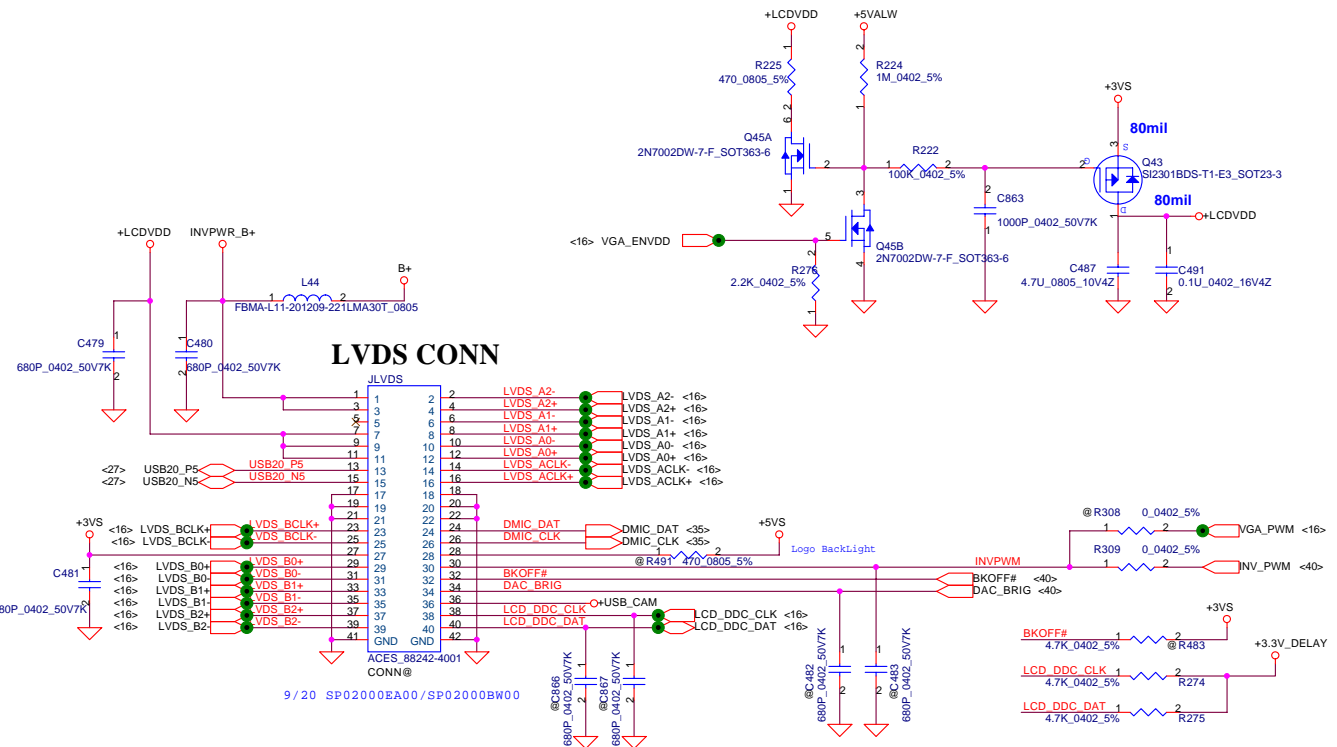
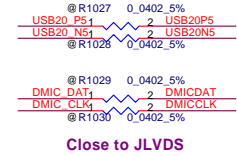
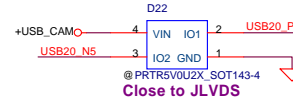


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Size	Document Number	Rev		
Custom	LA-4114P	0.1		
Date:	Thursday, November 06, 2008	Sheet	23	of 54

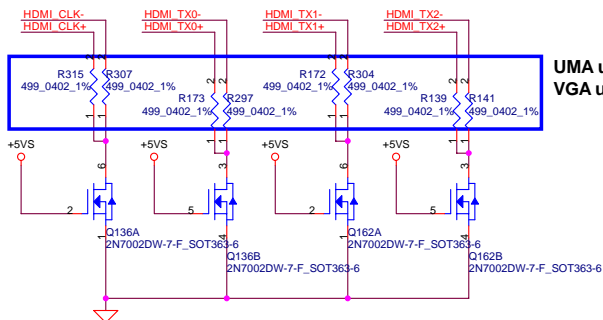
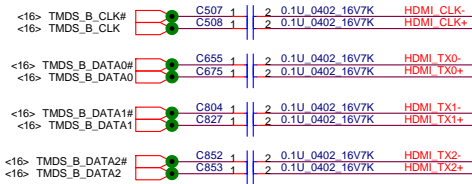
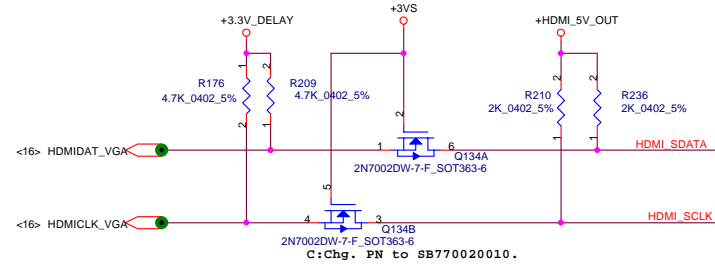
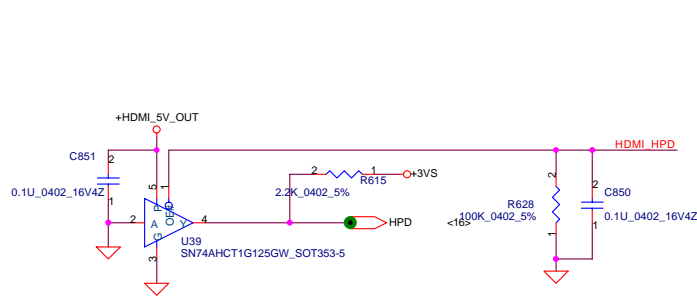
WebCam+Digital Mic



USB_VCCA is +3.9V, R892:100K; R891:215K Kohm
G916 Vref=1.25V

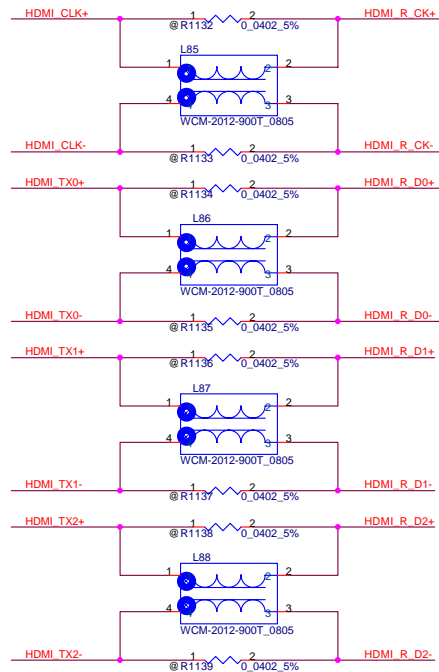


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Custom	LA-4114P	0.1			

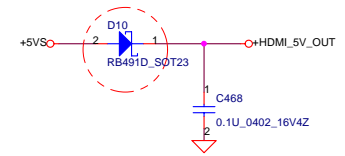


UMA use 750 ohm
VGA use 499 ohm

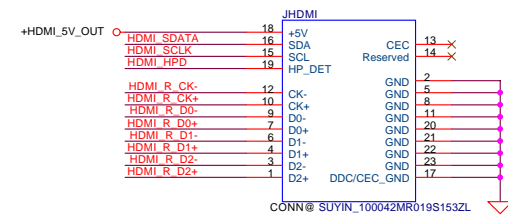
COMMON MODE CHOCK is SM07000K00 KING_WCM-2012-900T_4P



MP:Update D10 to meet HDMI.



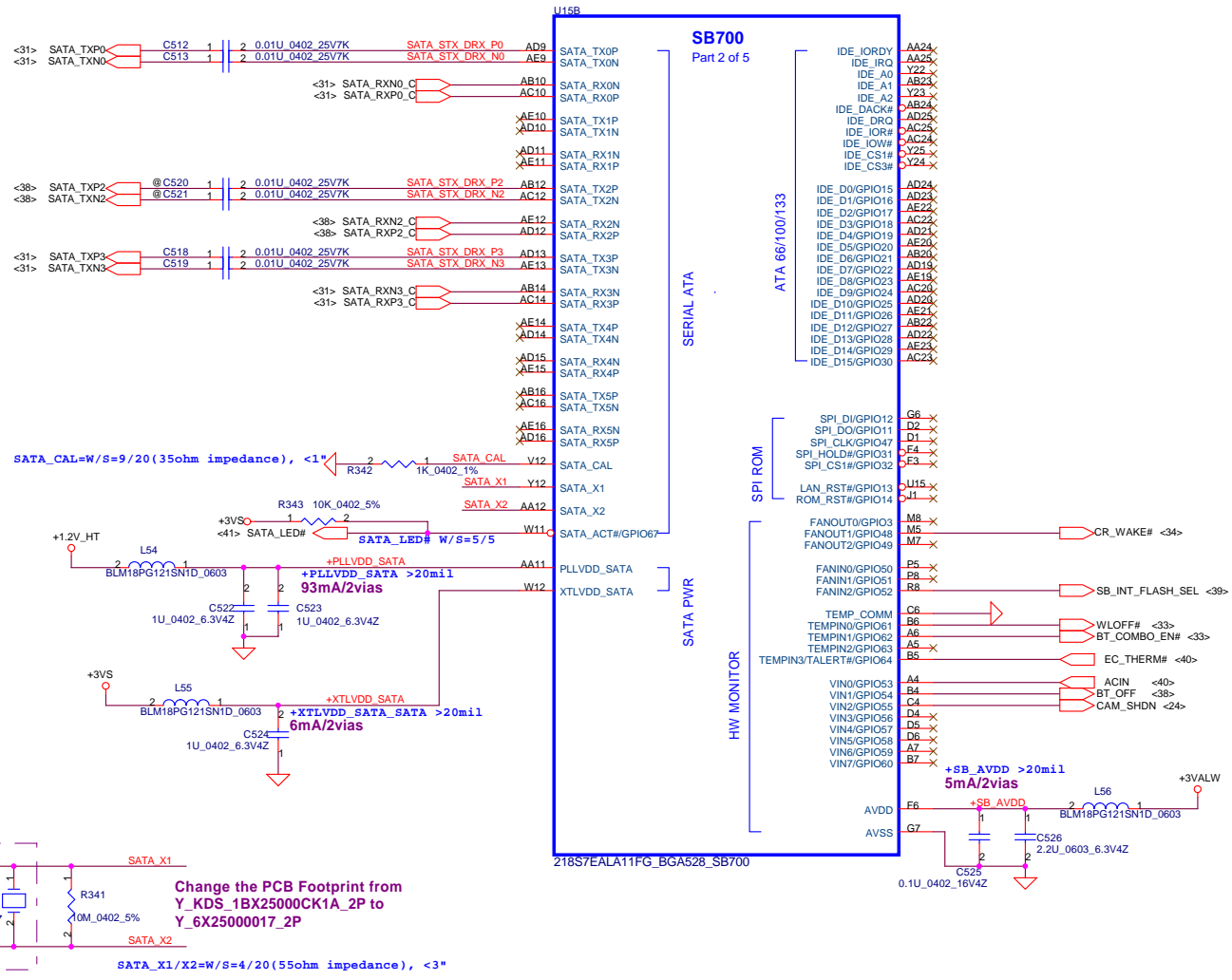
HDMI Connector



CONN@ SUYIN_100042MR019S153ZL

9/20 DC020709040

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				Date		Thursday, November 06, 2008



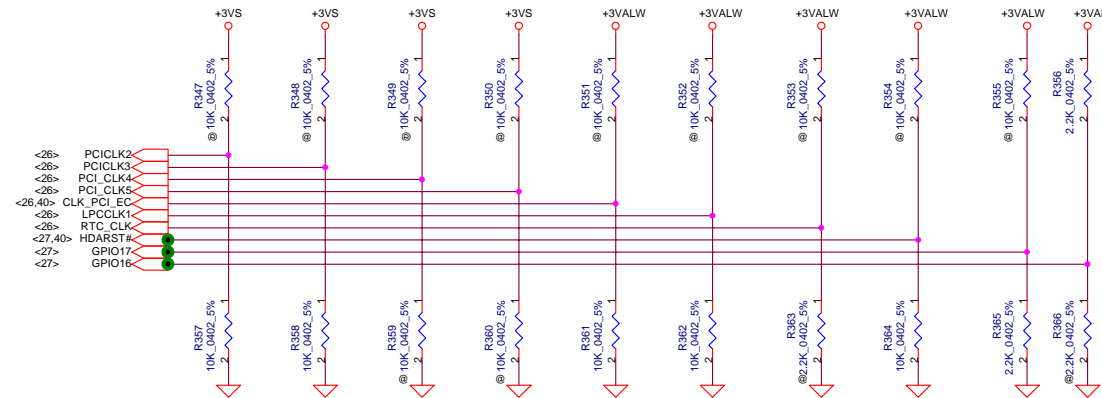
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Title			Compal Electronics, Inc.	
			SB700 SATA/IDE/SPI	
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REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

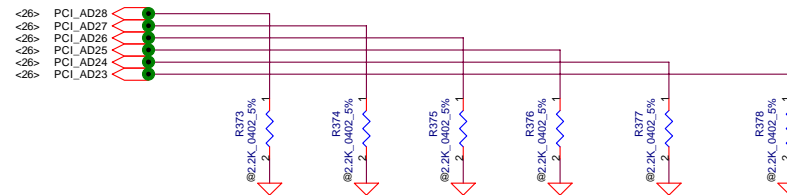
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	AZ_RST_CD#	LPC_CLK1	RTC_CLK	LPC_CLK0	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED		Internal pull up H,H = Reserved H,L = SPI ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		L,H = LPC ROM (Default) L,L = FW ROM



DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



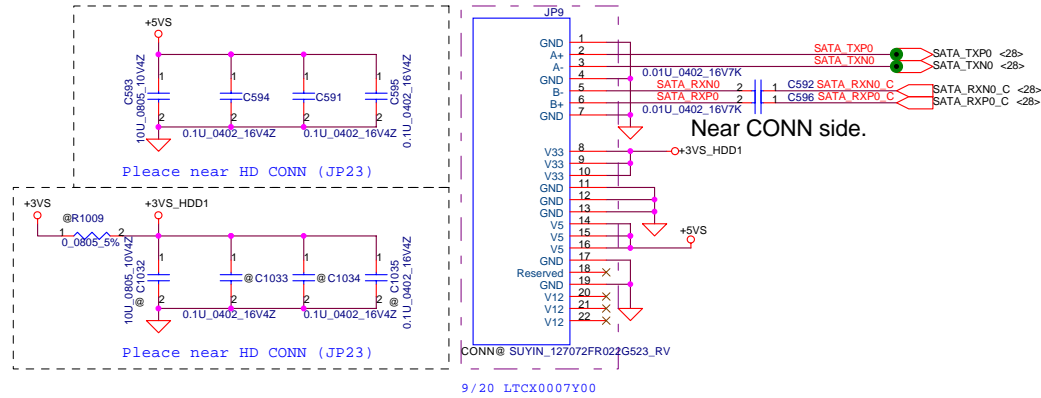
Security Classification	Compal Secret Data			Title	
Issued Date	2007/10/11	Deciphered Date	2008/10/11	SB700 STRAPS	
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				Date:	Thursday, November 06, 2008
				Sheet	30 of 54
				Rev	0.1

Compal Electronics, Inc.

SB700 STRAPS

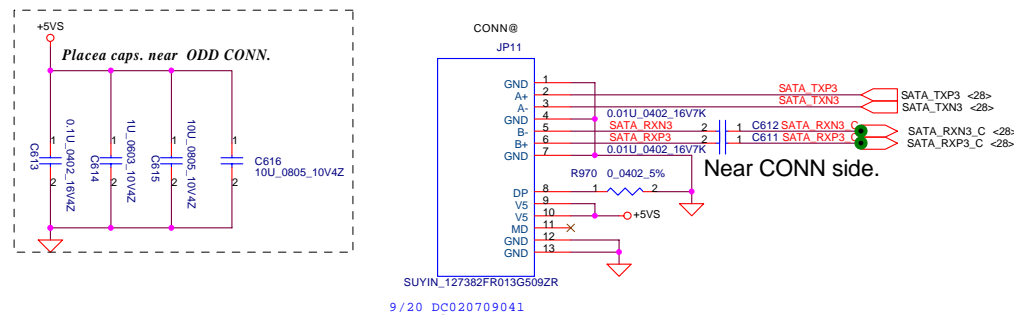
Size: Custom, Document Number: LA-4114P, Rev: 0.1, Date: Thursday, November 06, 2008, Sheet: 30 of 54

HDD Connector



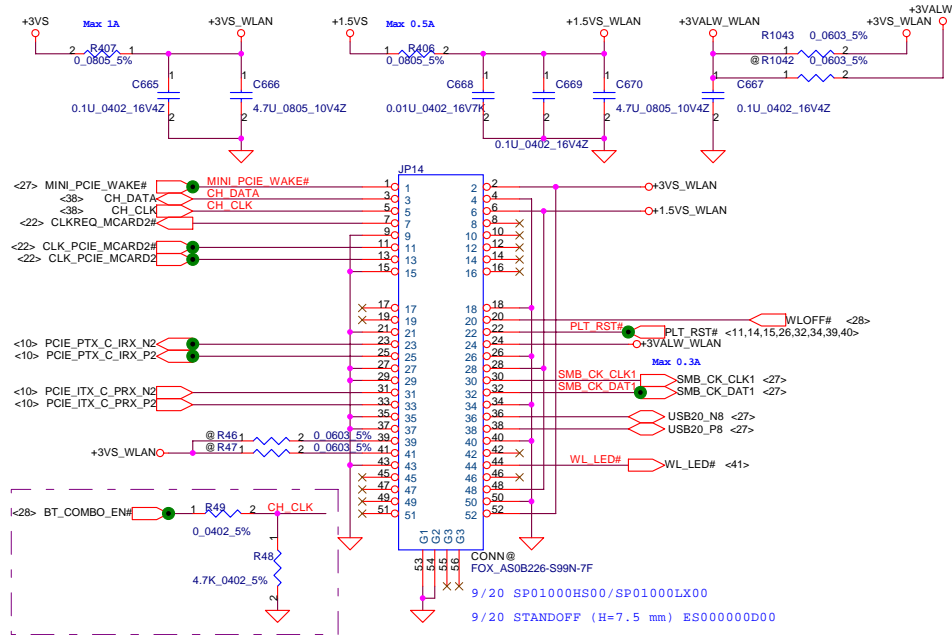
Multi-Bay Connector-option(deltet)

CD-ROM Connector

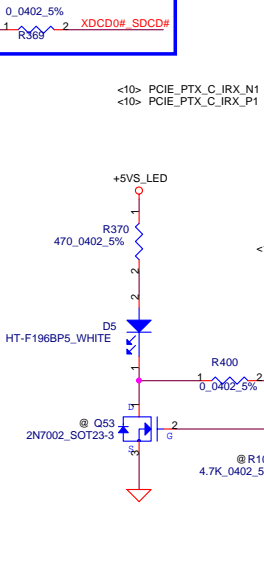
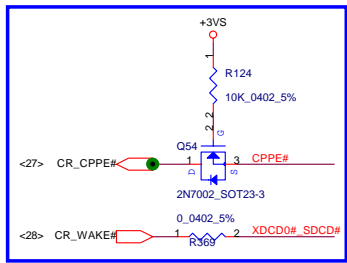
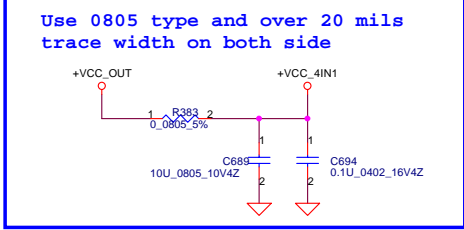
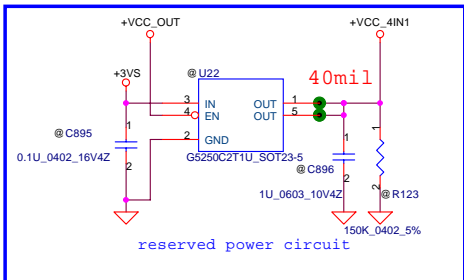


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				Date:	Thursday, November 06, 2008
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				Rev	0.1

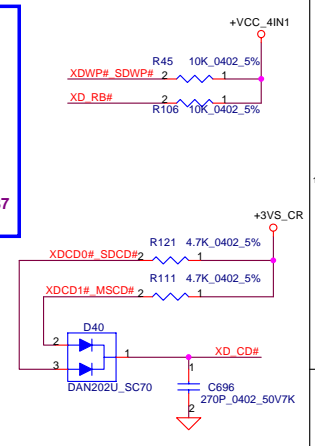
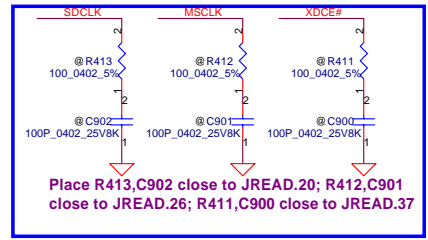
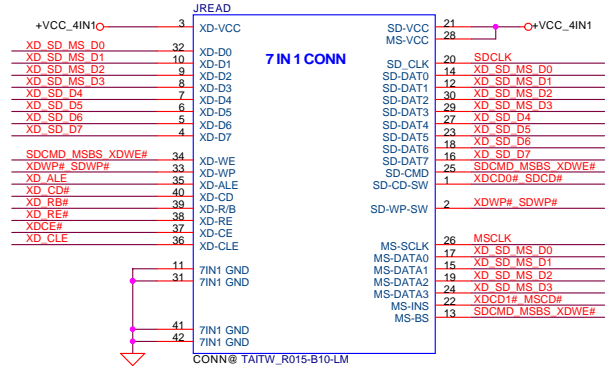
Mini Card Slot 1---WLAN



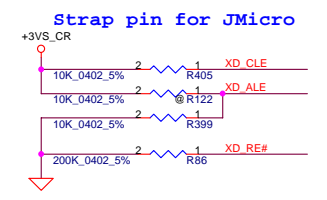
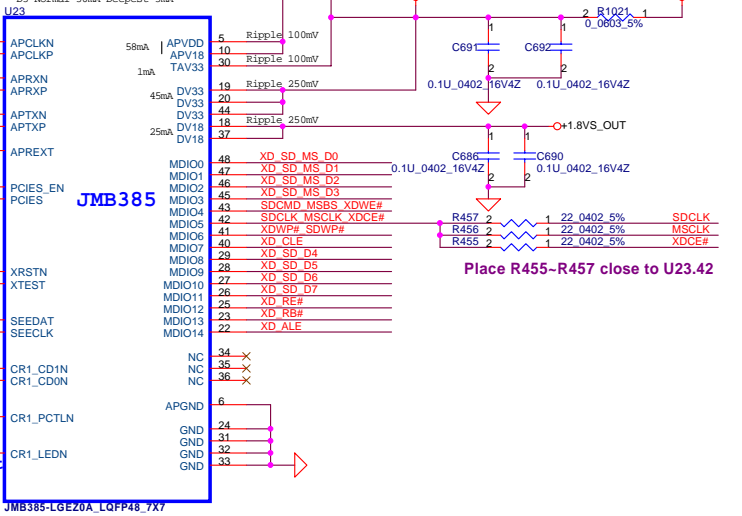
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Issued Date	2007/10/11	Deciphered Date	2008/10/11	Title WLAN	
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Card Reader Connector

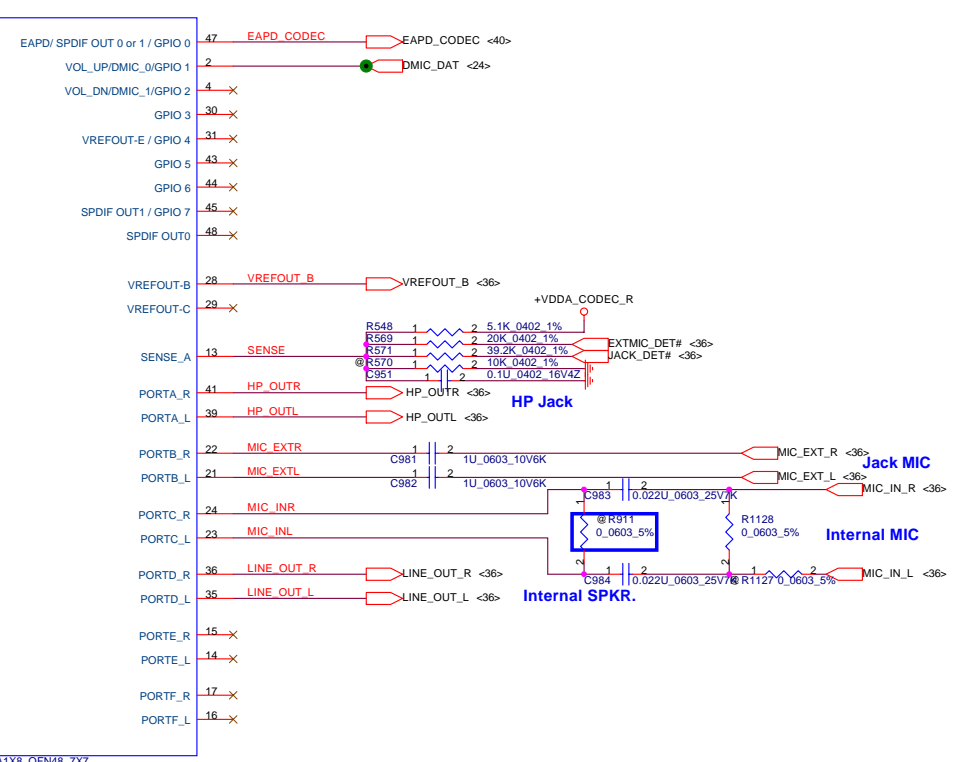
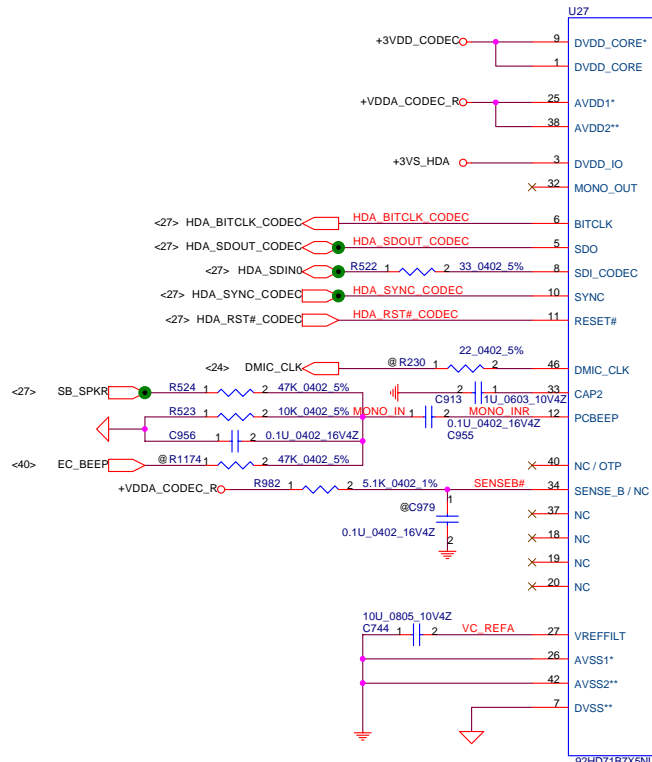
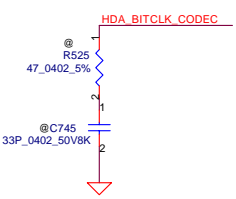
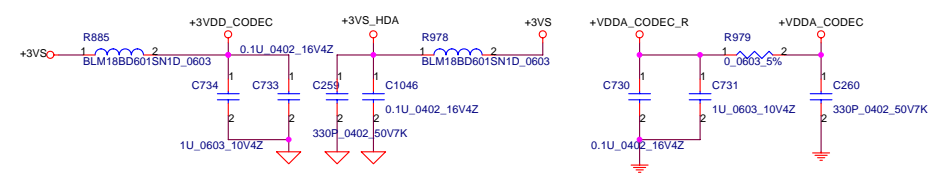
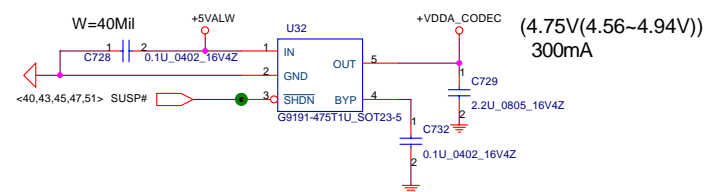


Power Circuit

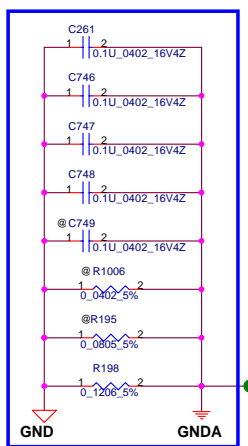


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CODEC POWER



SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K

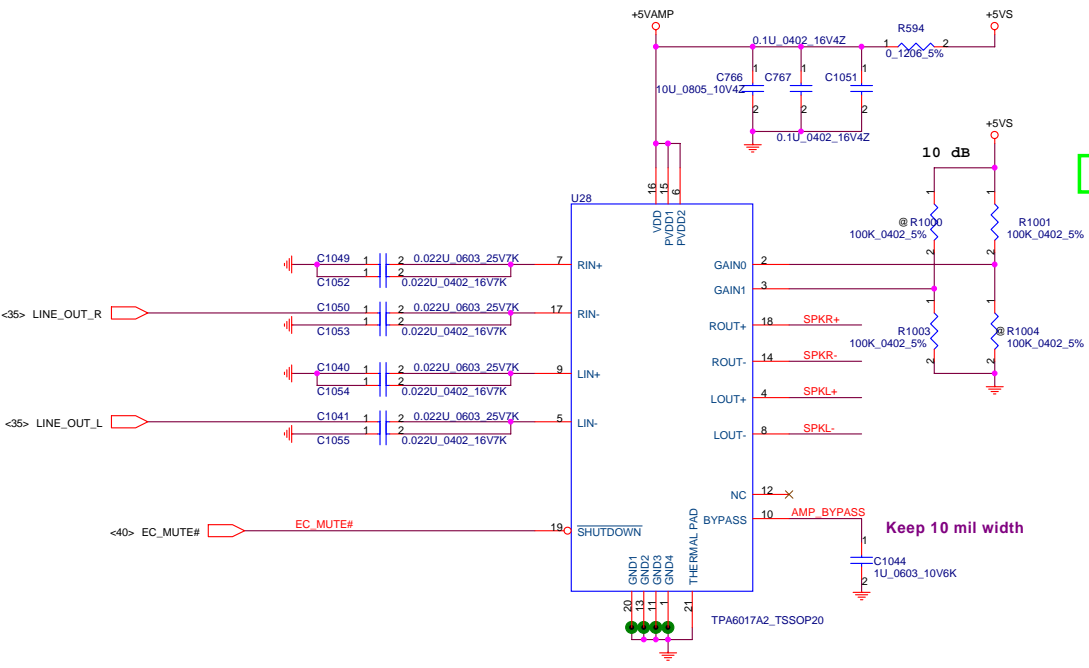


Use an 80mil to connection or place a 1206 resistor under CODEC with double vias.

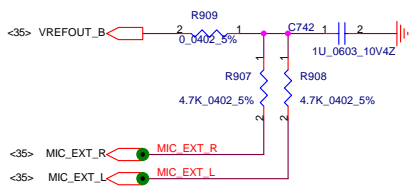
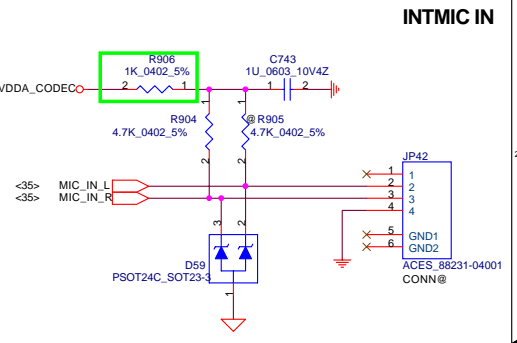
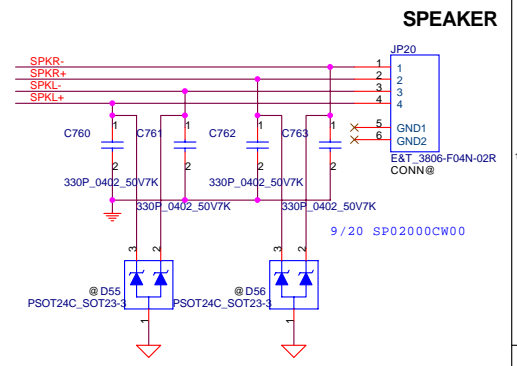
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Issued Date	2007/10/11	Deciphered Date
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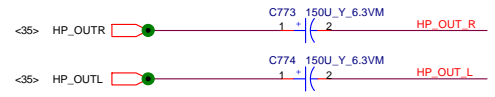
Compal Electronics, Inc.		
Title		
Audio Codec-IDT9271B7		
Size	Document Number	Rev
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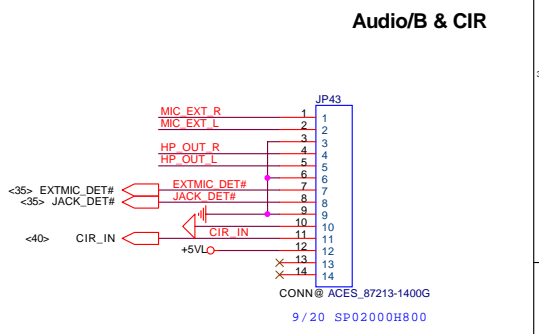
GAIN0	GAIN1	Av (inv)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



EXTMIC IN

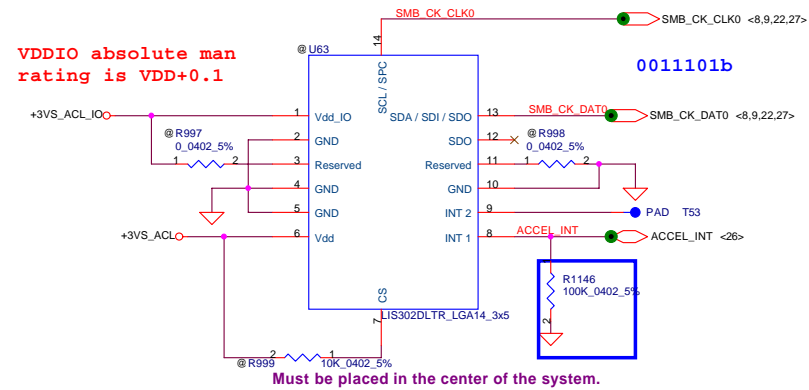
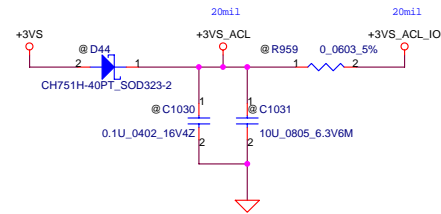


HP OUT For M/B



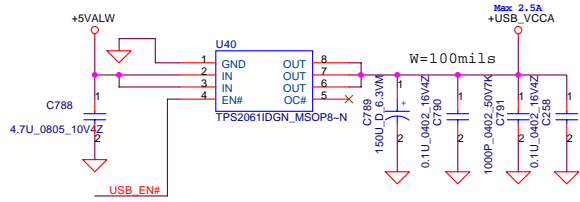
Audio/B & CIR

ACCELEROMETER

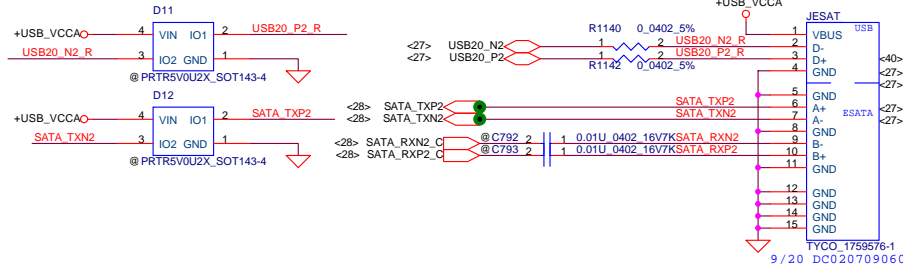


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Issued Date	2007/10/11	Deciphered Date	2008/10/11	Accelerometer		
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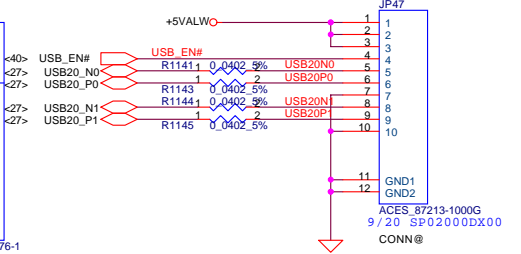
Left side USB CONNECTOR



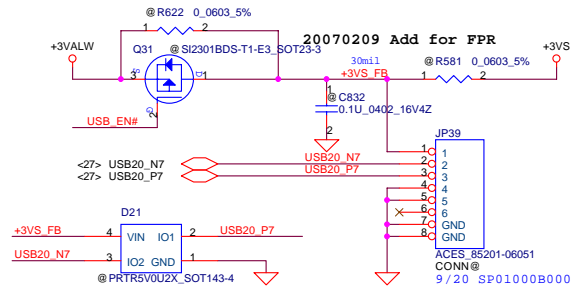
Left side ESATA5/USB2 combination Connector



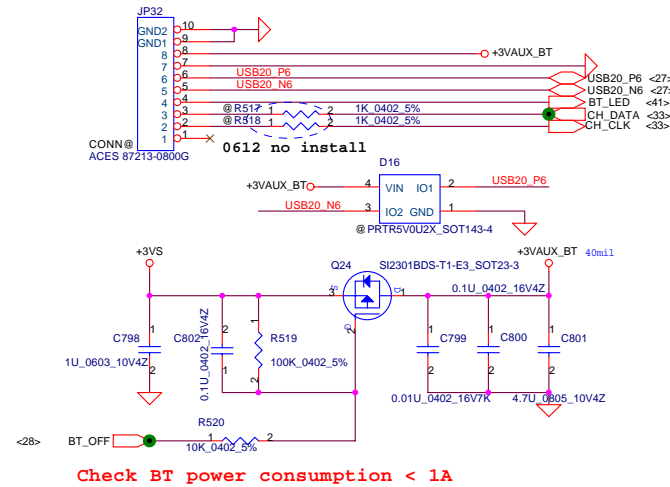
Right side USB 0&1 Board Conn



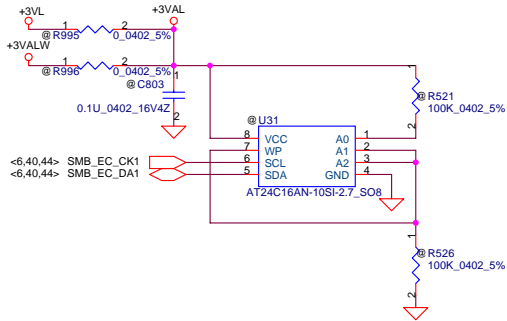
Finger printer



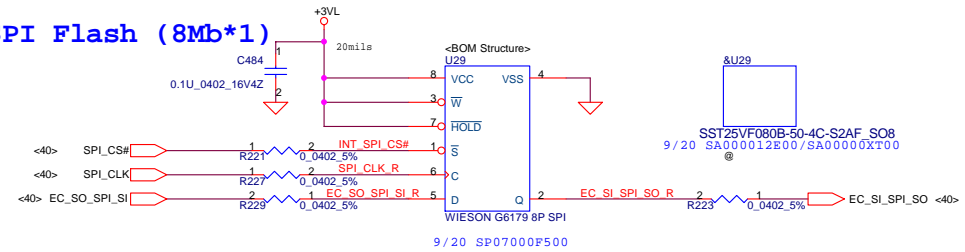
BT Connector



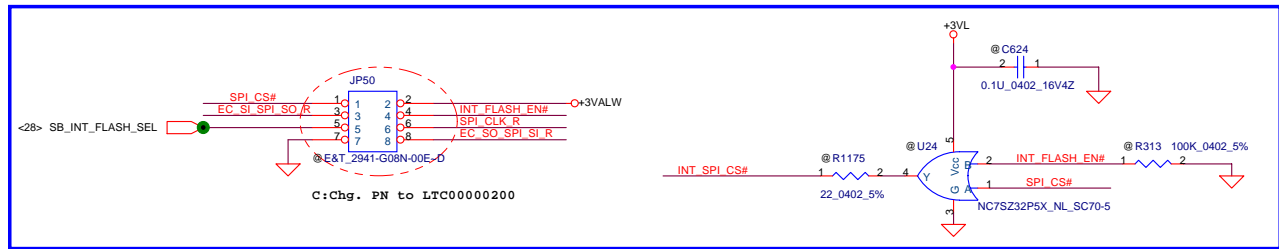
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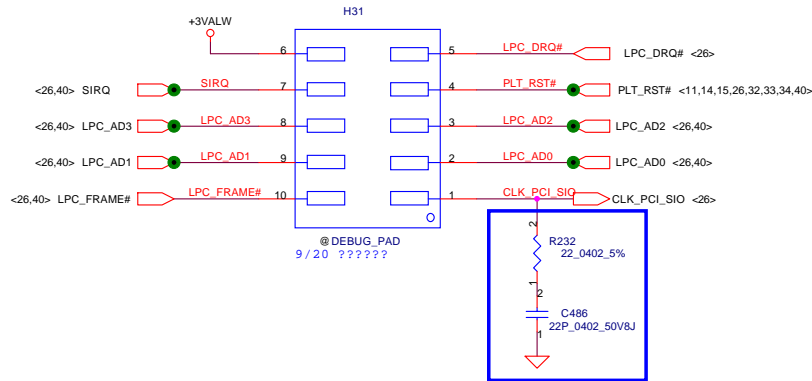
SPI Flash (8Mb*1)



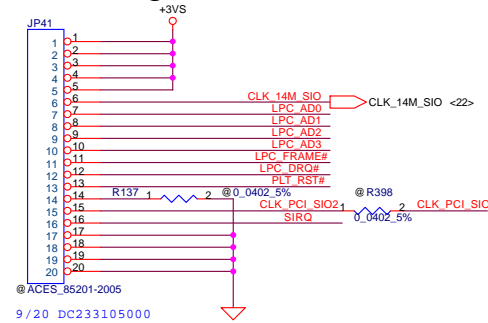
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9/20 SA000012E00/SA00000XT00



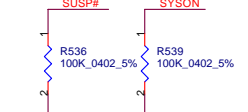
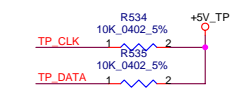
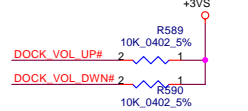
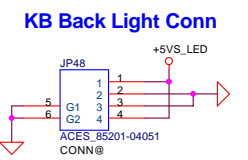
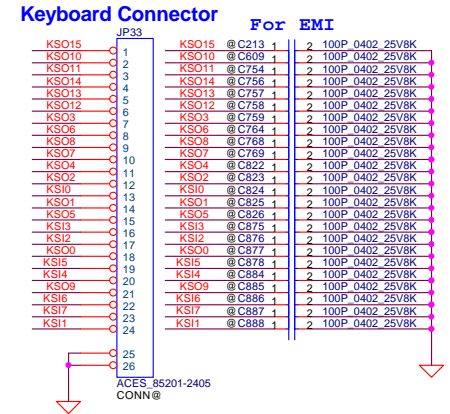
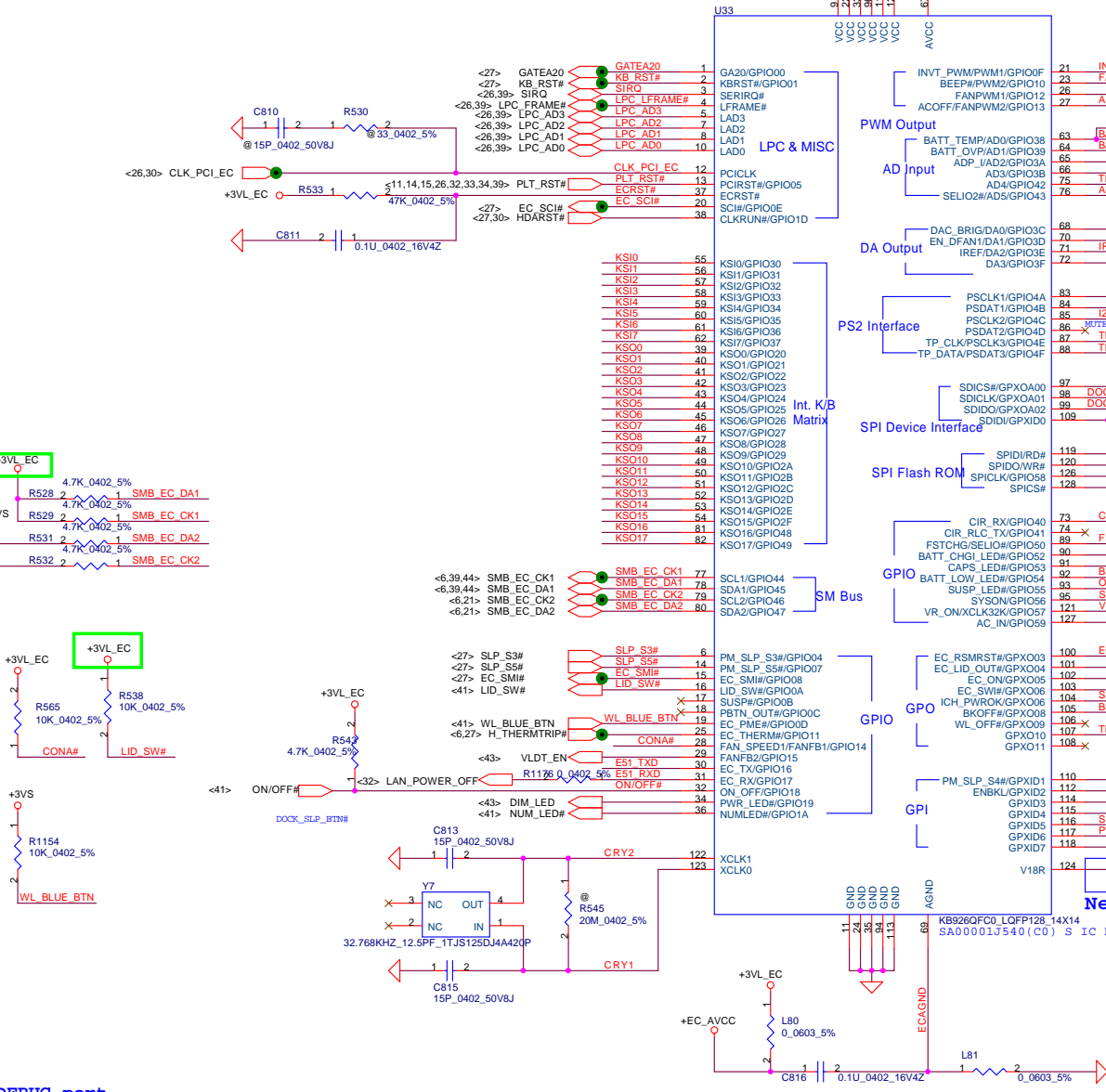
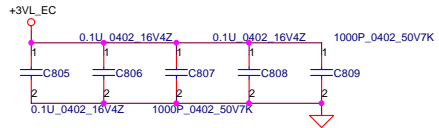
LPC Debug Port



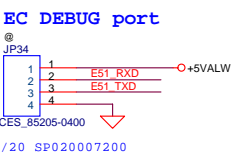
LPC Debug Port



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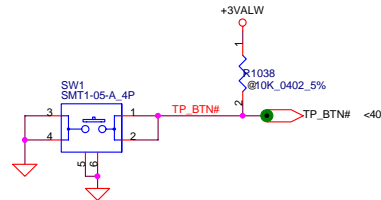
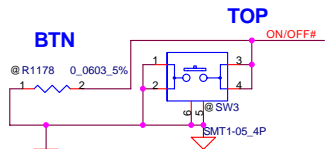
Need luf for 926 C version



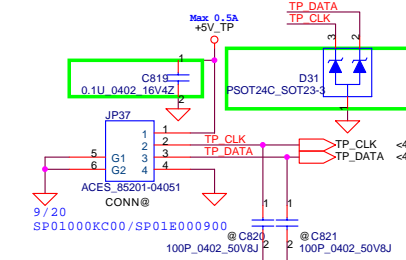
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for debug only

ON/OFF Button Connector(delete) TP ON/OFF

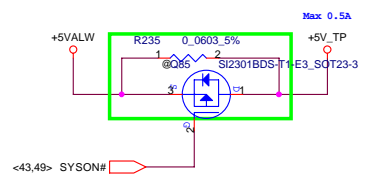
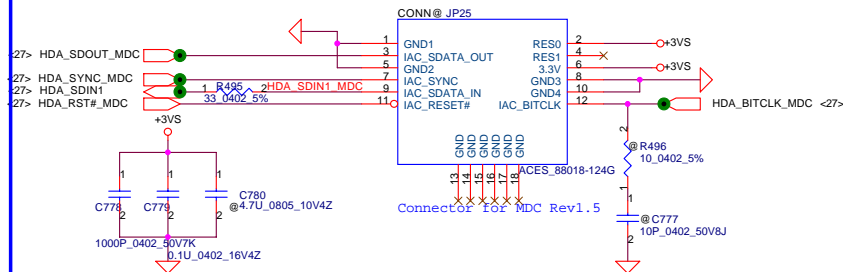


M/B TO TP/B

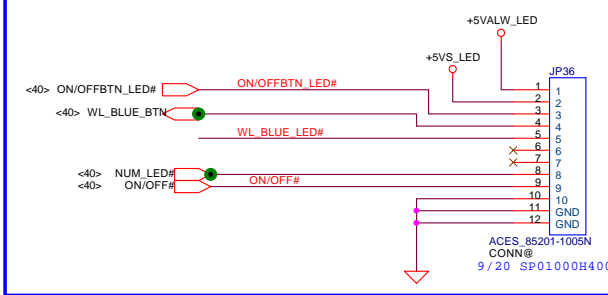


MDC 1.5 Conn.

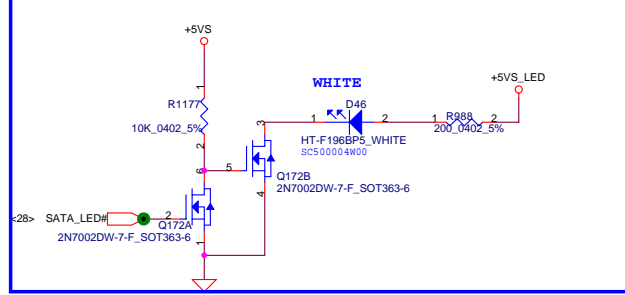
9/20 SP01000J100
9/20 STANDOFF (H= 5.0 mm) ES000000800



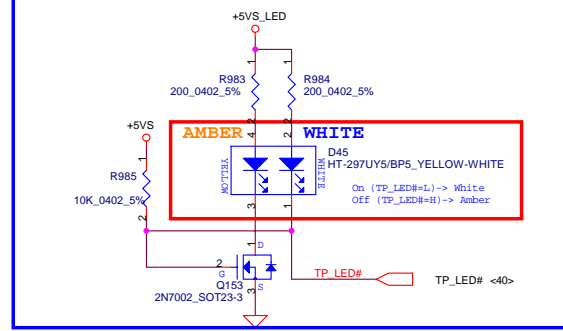
SWITCH BOARD.



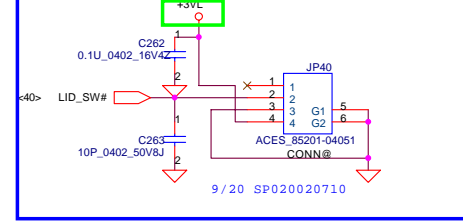
HDD LED



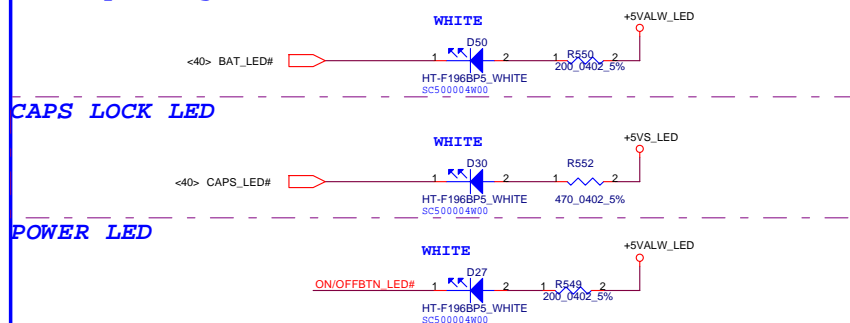
TouchPAD ON/OFF LED



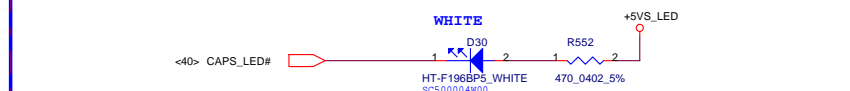
Reed switch BOARD.



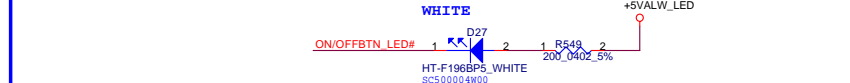
Battery Charge LED



CAPS LOCK LED

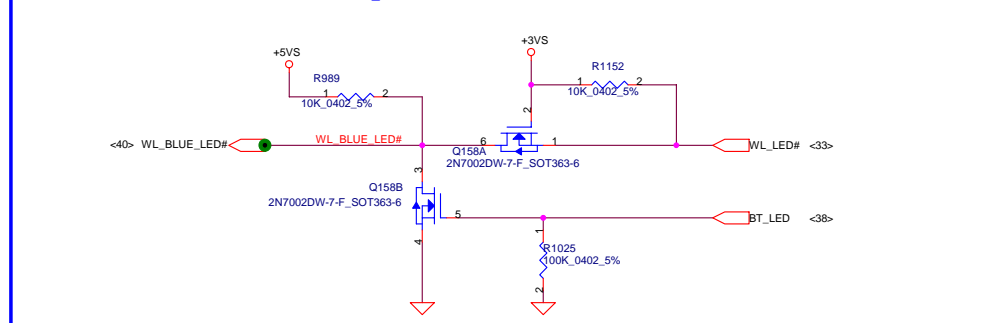


POWER LED



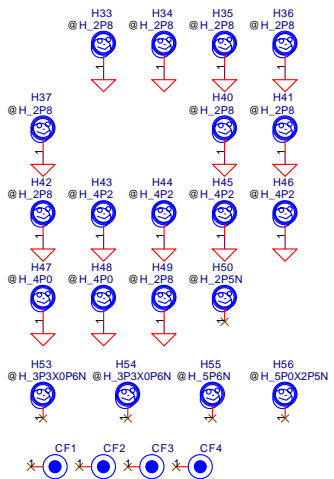
White LED: VF=3V, IF = 10mA, Res = 200 ohm
Amber LED: VF=1.8V, IF = 8mA, Res = 390 ohm

WLAN and BT LED inform pin to KBC



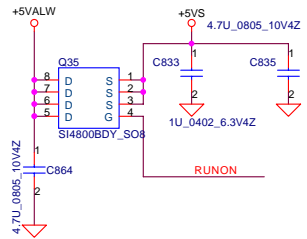
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H47, H48 -Stand off of MODEM on BOT Side

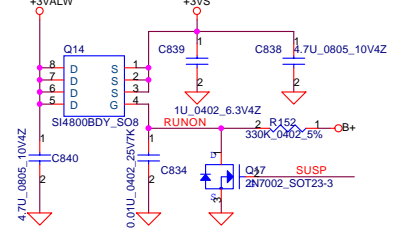


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				Date:	Thursday, November 06, 2008	Sheet 42 of 54

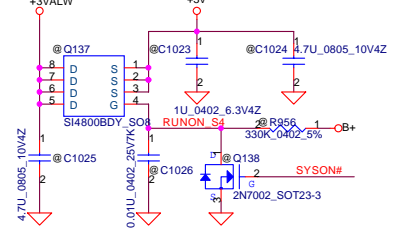
+5VALW TO +5VS



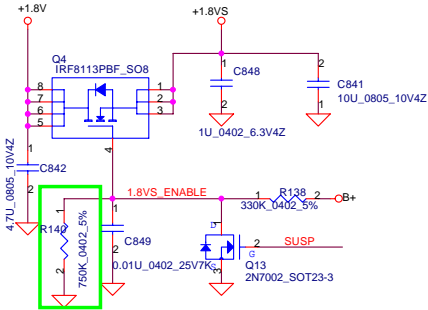
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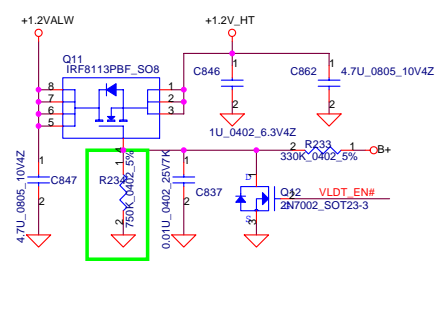
+3VALW TO +3V



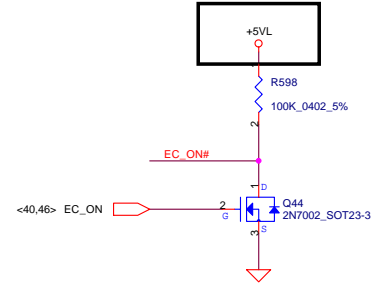
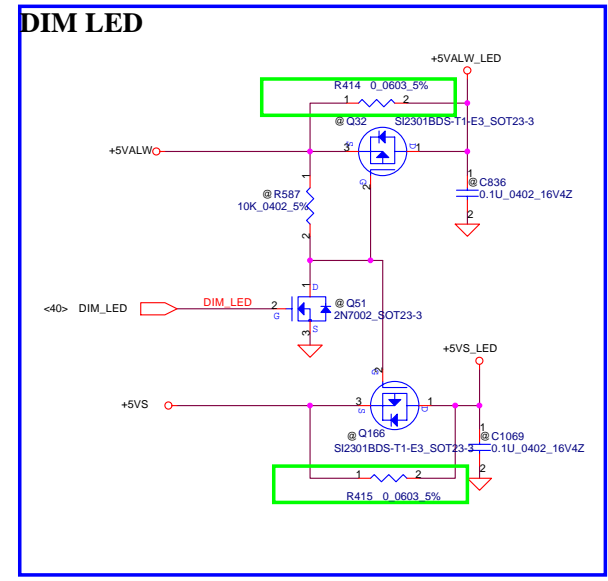
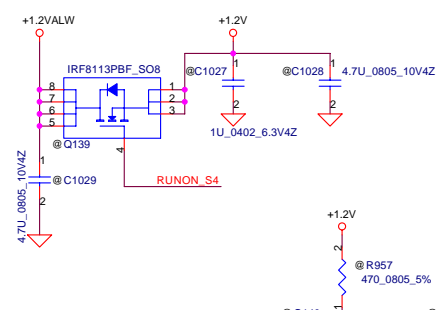
+1.8V TO +1.8VS



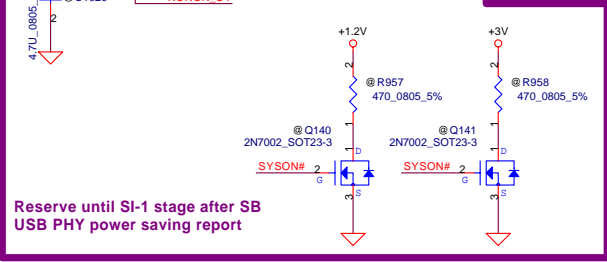
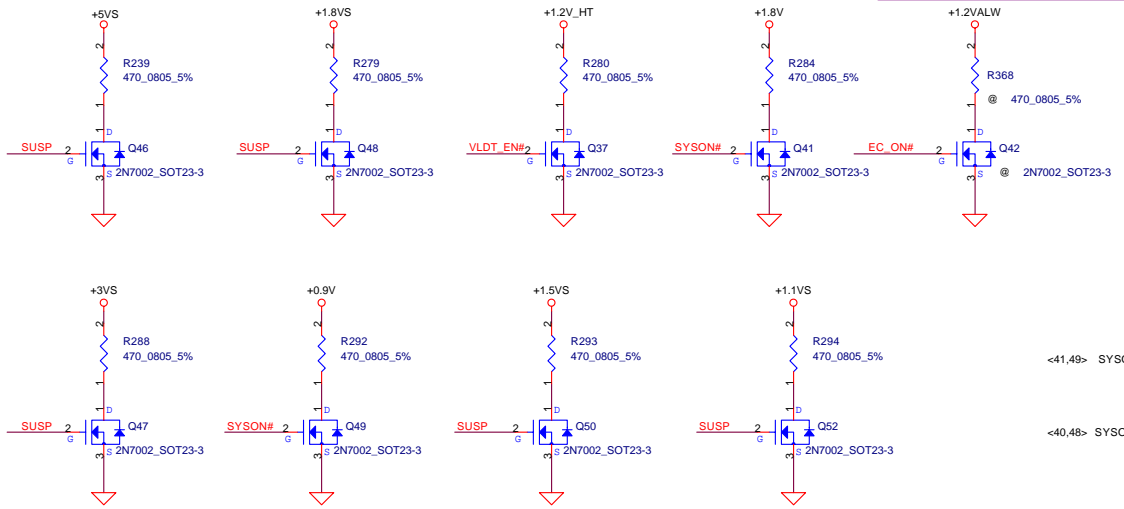
+1.2VALW TO +1.2V_HT



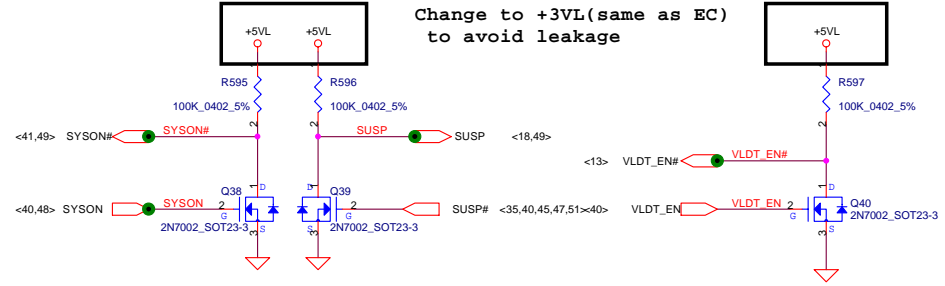
+1.2VALW TO +1.2V



Discharge circuit

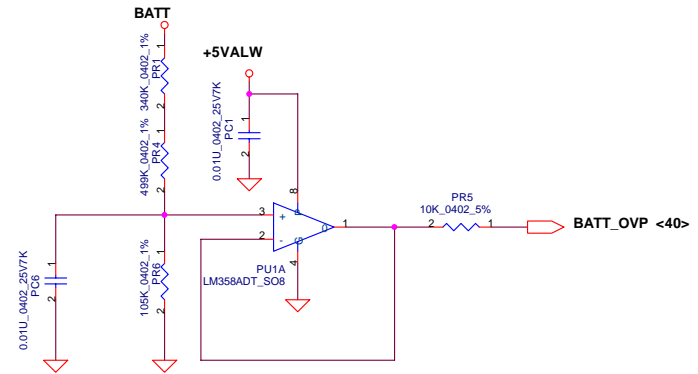
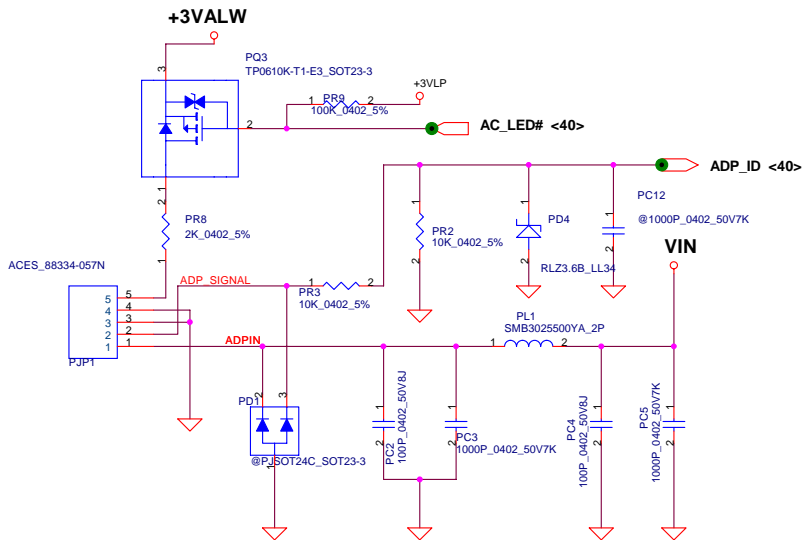


Change to +3VL (same as EC) to avoid leakage

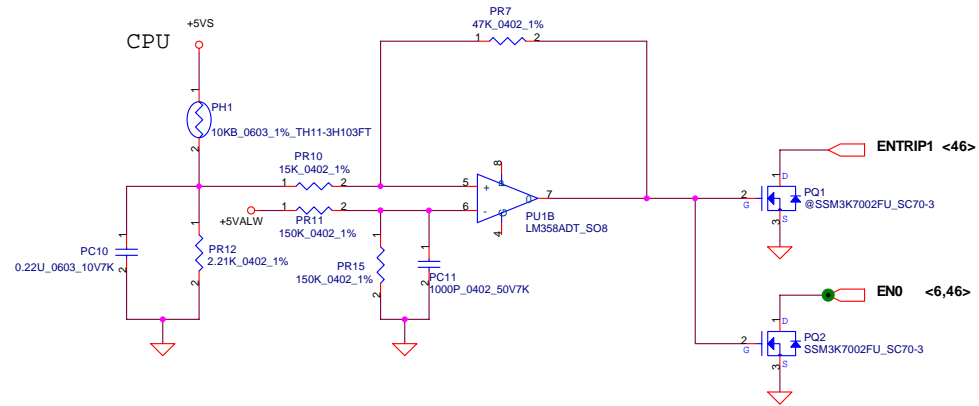
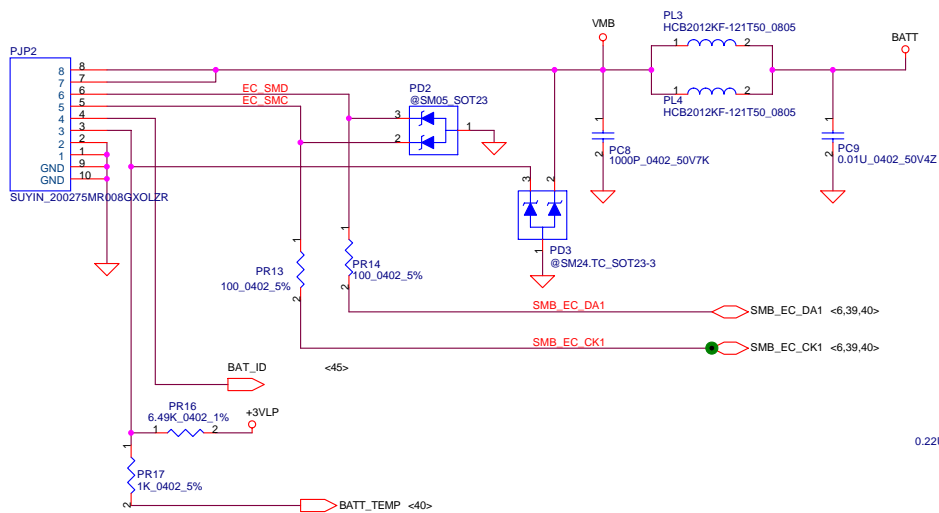


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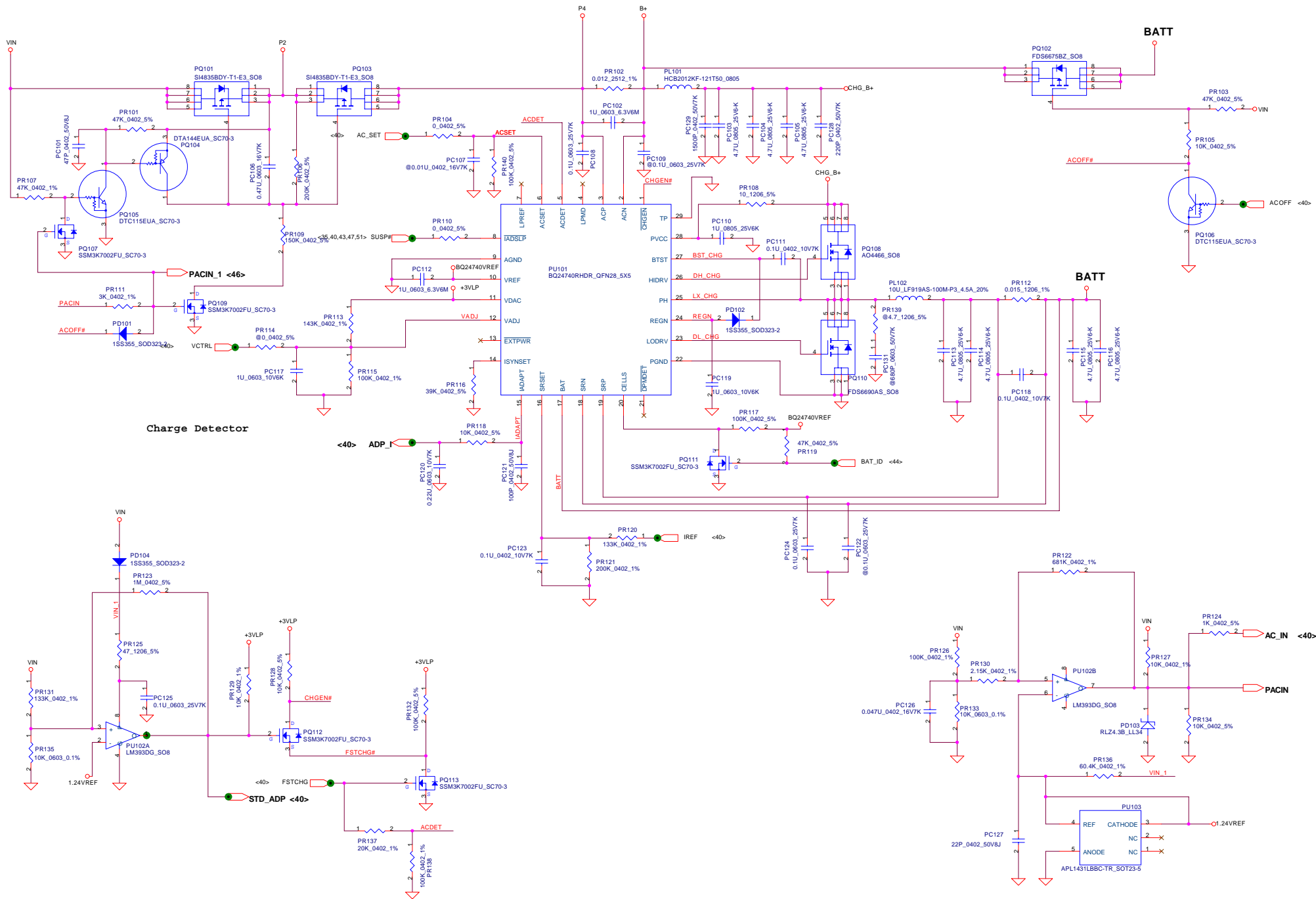
BATT1
45@CR2032 RTC BATTERY



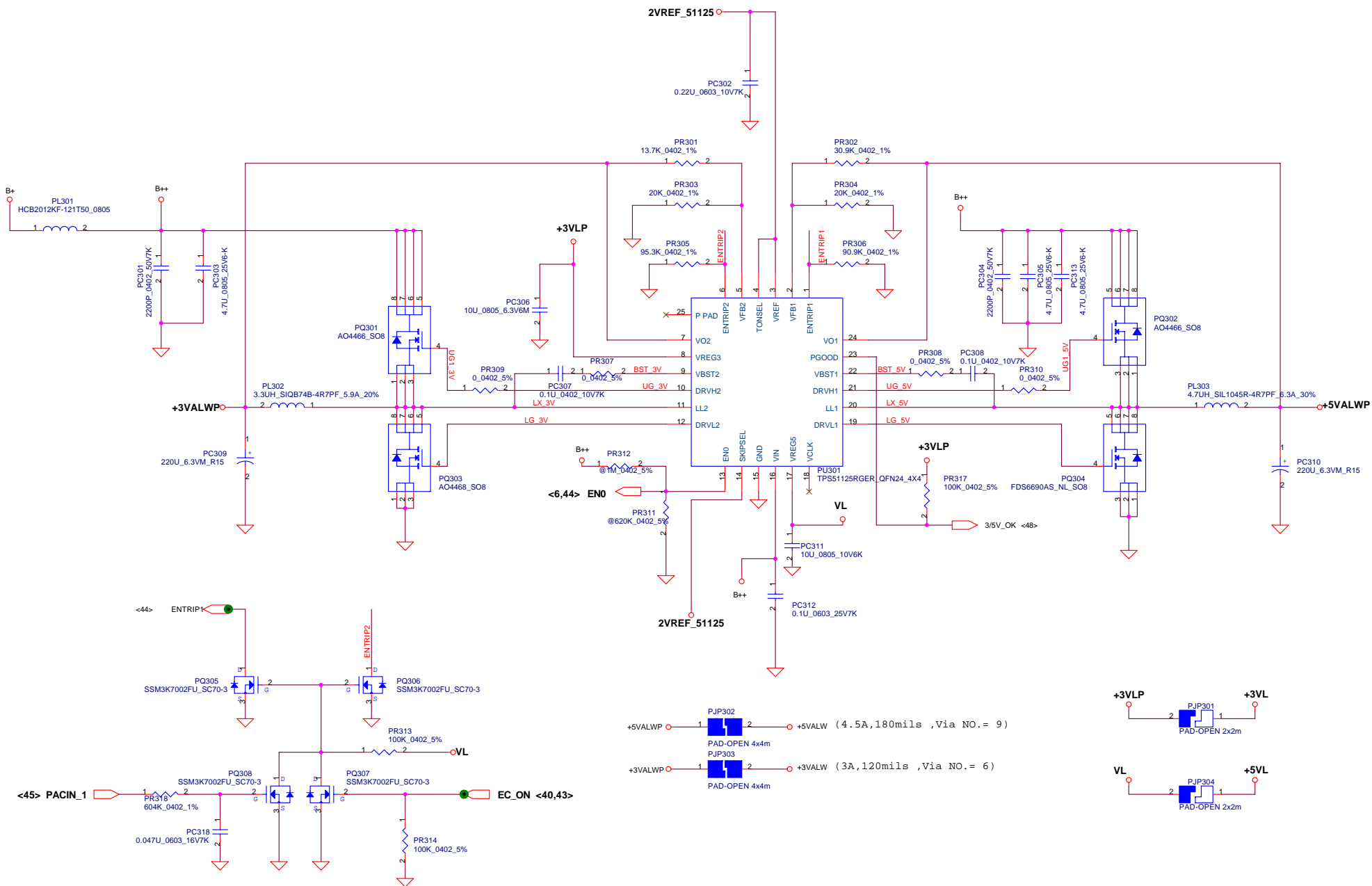
PH1 under CPU bottom side :
CPU thermal protection at 95 +/-3 degree C
Recovery at 47 +/-3 degree C



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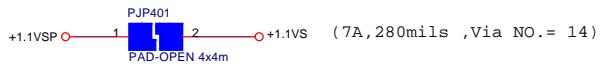
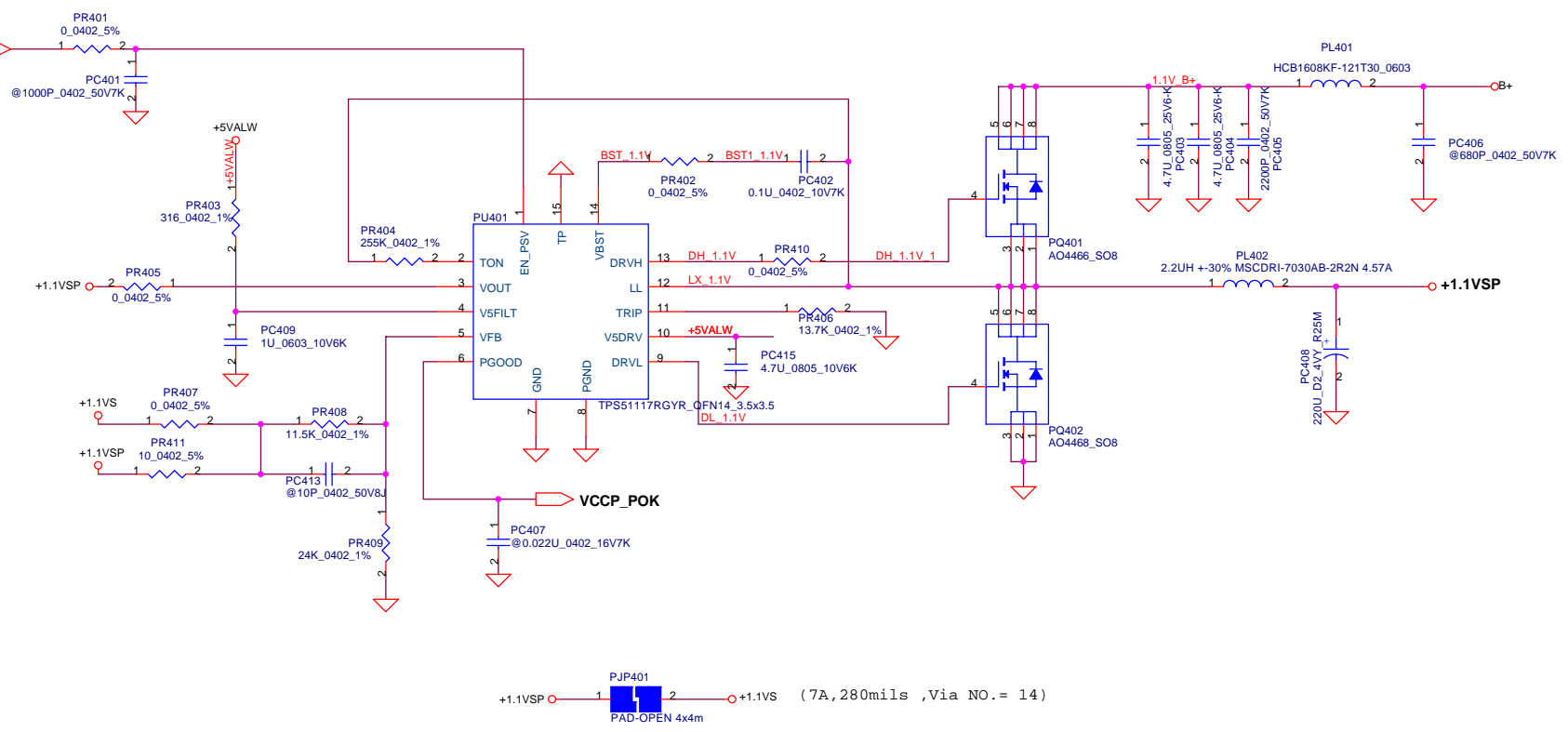
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Size	Document Number	Rev		Date	
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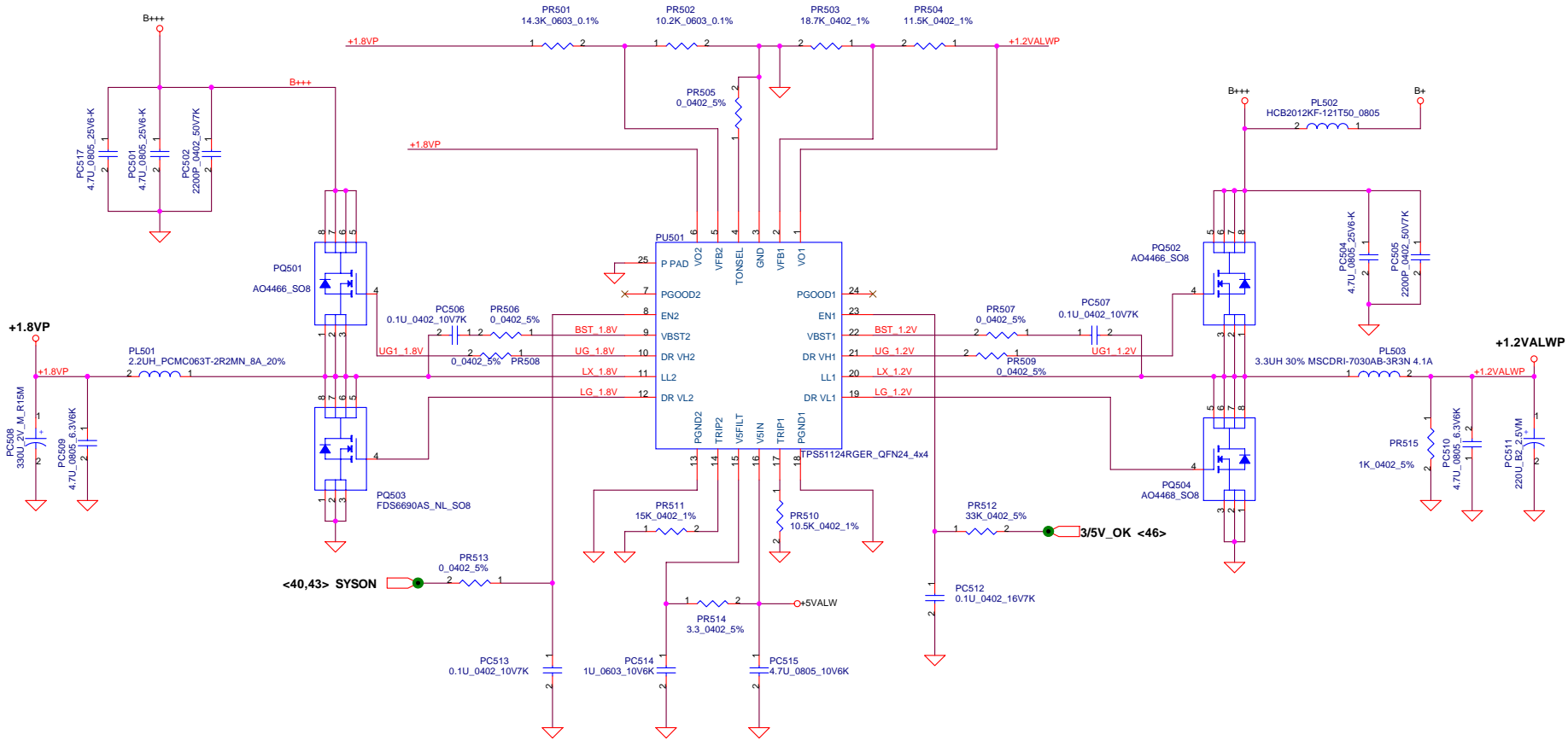
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Title		
Compal Electronics, Inc.		
3.3VALWP/5VALWP		
Size	Document Number	Rev
Custom	LA-4114P	0.1
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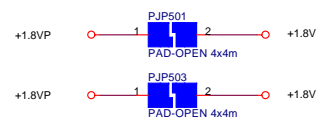
5,40,43,45,51> SUSP#



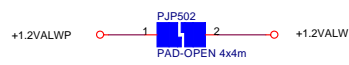
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Issued Date	2007/05/29	Deciphered Date	200810/11			Title
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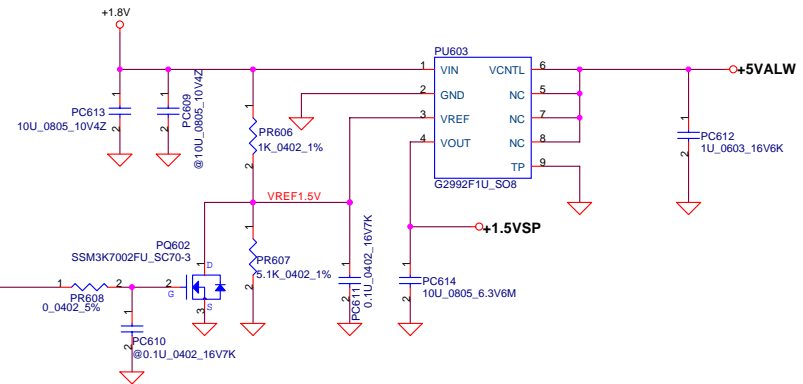
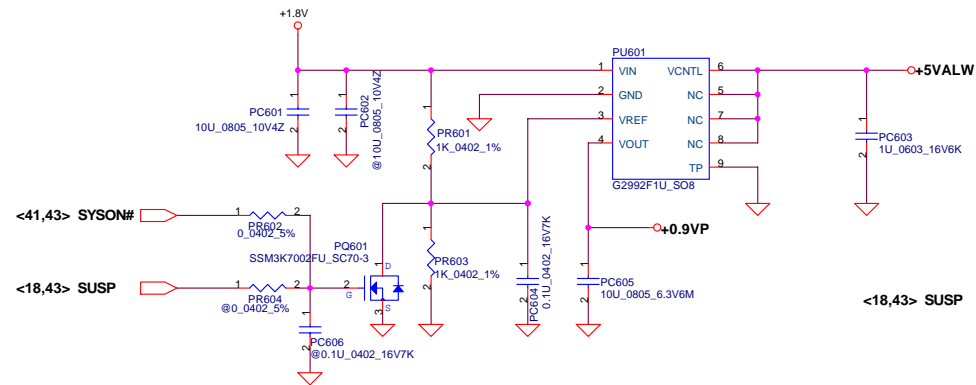
(8A,320mils ,Via NO.=16)



(4A,160mils ,Via NO.=8)



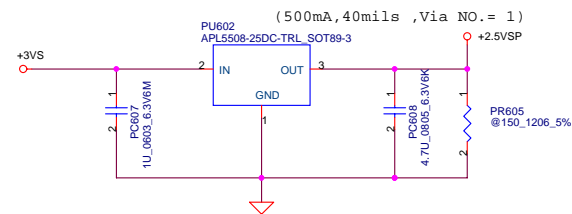
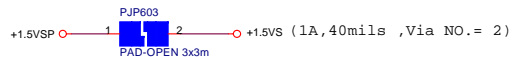
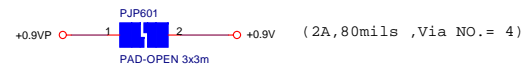
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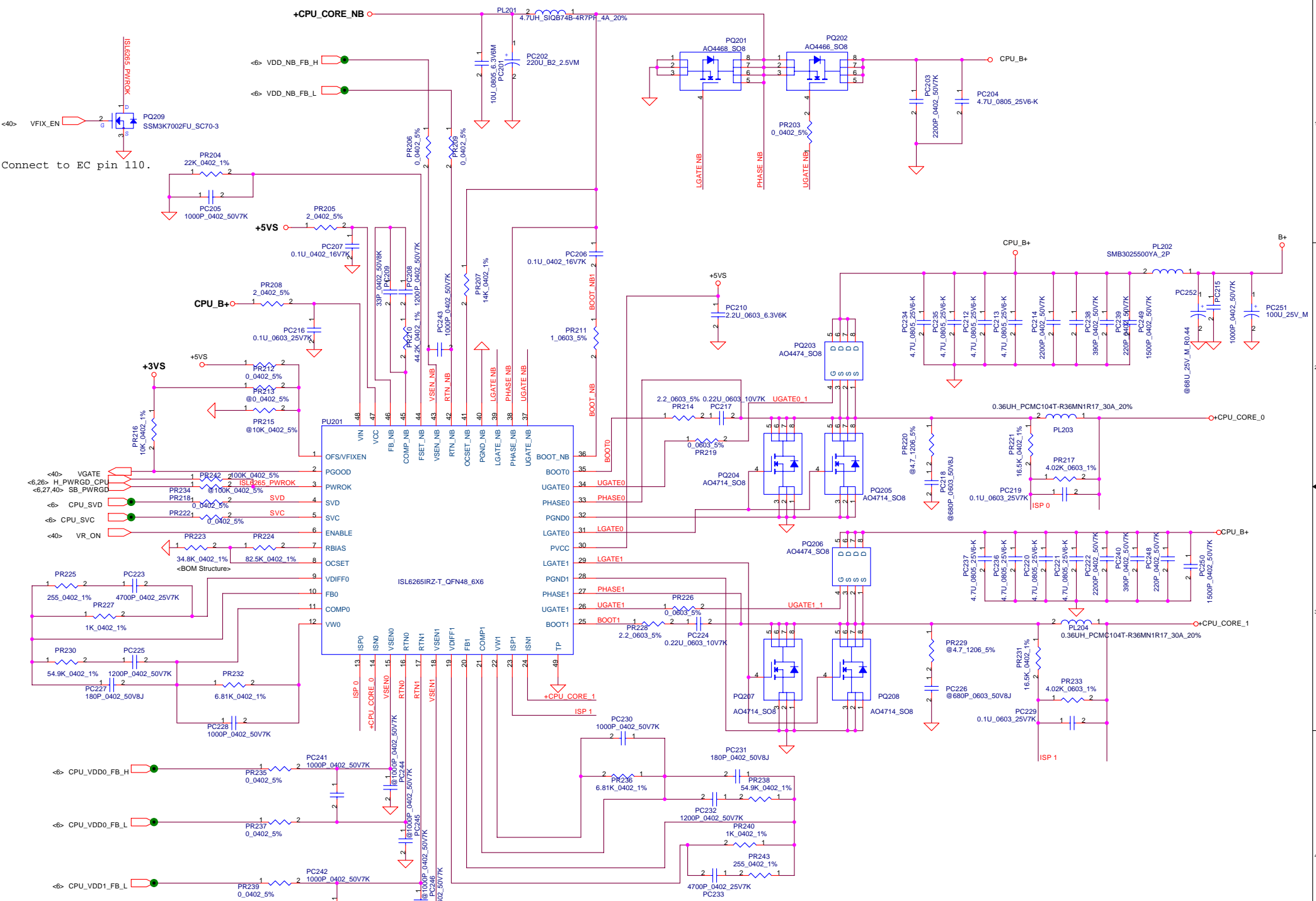
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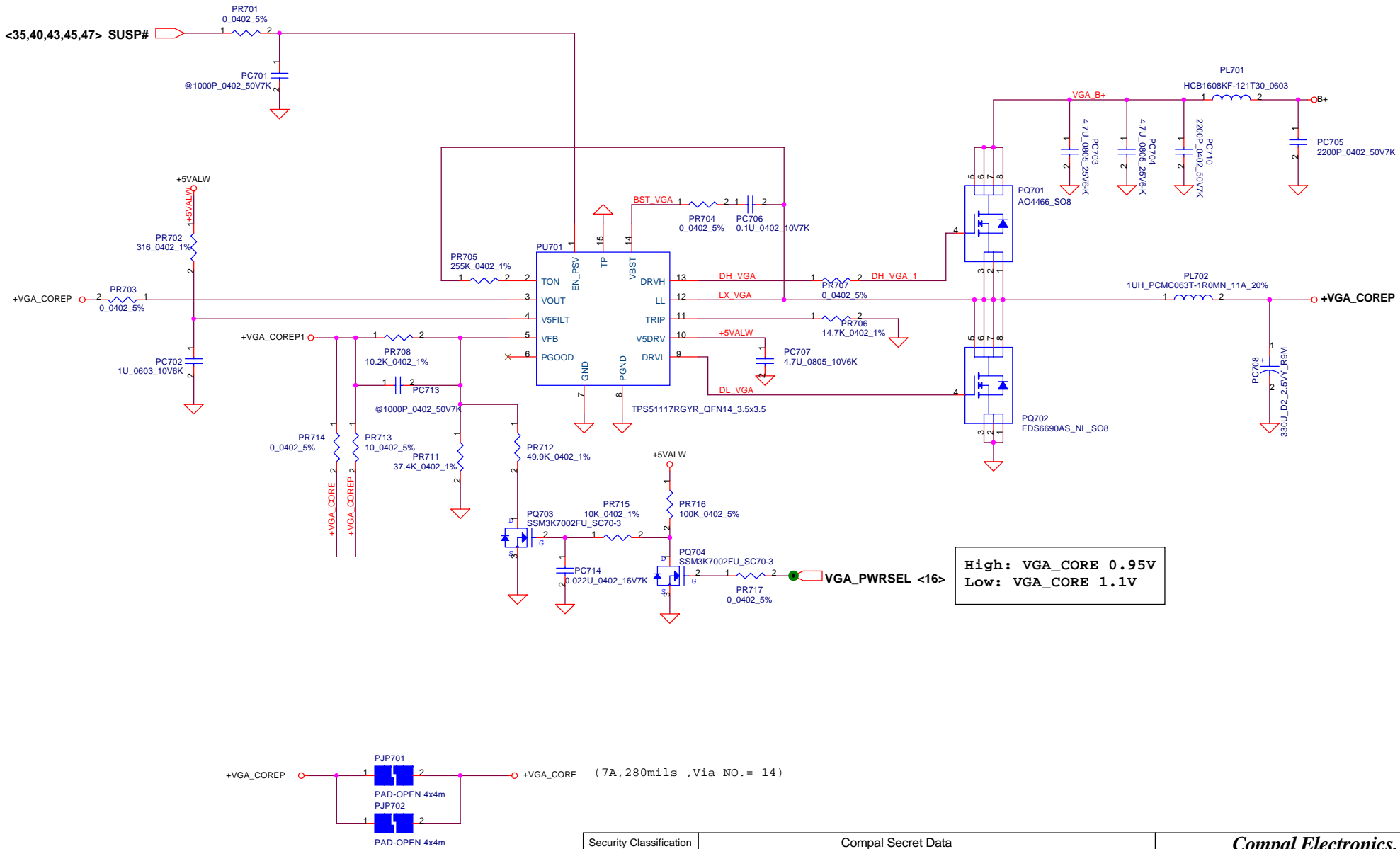


Connect to EC pin 110.

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Title		
Compal Electronics, Inc.		
CPU CORE		
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High: VGA_CORE 0.95V
Low: VGA_CORE 1.1V

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Compal Electronics, Inc.

VGA CORE

LA-4114P

Rev 0.1

Date: Thursday, November 06, 2008 | Sheet 51 of 53

LA-4112P Rev0.1 -> 0.2 Product Improvement Record (P.I.R.)

BOM change list:

1. Stuff R41(220 Ohm), R26(300 Ohm), R28(300 Ohm). (Page 6)-* AMD recommand.
2. Stuff R1101(10K Ohm). (Page 21)-* Strengthen PCI-E swing to meet PCI-E spec.
3. Un-stuff R1061,R1062,R1064/Change R214,R211,R217 from 150 -> 75 Ohm/C858,C476,C472 from 22p -> 6pF/Chagne L47,L48,L49 type (Page 16/25)-* Tune CRT(R/G/B) rising & falling skew time to meet SPEC.
4. Change C863 1000p -> 0.047uF. (Page 24)-* For LED Panel power up timing >0.5mSec.
5. Change C643,C652 18p -> 12pF. (Page 26)-* Tune RTC 32K Caps to meet HP SVTP spec.
6. Change R323 11.8K -> 11K Ohm. (Page 27)-* Tune the value to meet USB EE spec.
7. Change R356 10K -> 2.2K Ohm. (Page 30)-* ATI recommand.
8. Change C1040 10U -> 1UF. (Page 36)-* Reduce Power up "BOBO" noise.
9. Change Keyboard connector type. (Page 40)-* For ME request.
10. Change Reed Switch Board connector type. (Page 41)-* For ME request.
11. Un-stuff C9. (Page 4)-* Fixed Caps issue noise.
12. Change R371 10K -> 300 Ohm. (Page 10)-* ATI recommand.
13. Un-stuff L2,L4,L6,L9,L7/Stuff C170,C172,C175,C178,C176 0 Ohm. (Page 11)-* ATI RX781 changed recommand.
14. Un-stuff R1054/Stuff C252 0 Ohm. (Page 13)-* ATI RX781 changed recommand.
15. Un-stuff C250,C253. (Page 13)-* Follow 17" AMD circuit change.
16. Change C101,C102 1K->3K Ohm. (Page 14)-* ATI recommand.
17. Un-stuff R1067. (Page 16)-* Follow 17" AMD circuit circuit change.
18. Un-stuff R1155,R1157,R1159. (Page 28)-* Dont need to reserve it for UMA side port buffer strapping.

Circuit change list:

1. Del Q6, Q5 (Page 10)-* Dont need to reserve it.
2. Divide DPA_PDD & DPB_PVDD power.(Page 16)-* ATI recommand.
3. Del Q155 (Page 26)-* Dont need to reserve it.
4. Chagne PCICLK output source to LPCCLK1 output. (Page 26)-* Follow 17" AMD circuit change.
5. Add SSC circuit for AZ bus BIT CLK. (Page 27)-* EMI request.
6. Delete R1002,R1005. (Page 36)-* Dont need to reserve it for line out serial resistor from CODEC to AMP.
7. Modify JP20 speaker signals define. (Page 36)-* DB stage define error fix.
8. Chagne C802 position to +3VALW. (Page 38)-* DB stage +3VAUX_BT leakage fix.
9. Chagne U24 power source from +3VALW -> +3VL. (Page 39)-* Power souce need to be the same power source of SPI ROM.
10. Delete LPC debug port circuit. (Page 39)-* With BIOS discuss and delete it.
11. Add power requesting net "VFIX_EN". (Page 40)-* Power request.
12. Change JP36 pin7 GND -> NC. (Page 41)-* Follow Riply pin define.
13. Swap D45 T/P LED. (Page 41)-* DB Stage LED behavior error fix.
14. Add a signal AC_LED# of EC pin97 & VFIX_EN of EC pin110.. (Page 40)-* Power request.
15. Change AC_IN pull high from +3VALW to +3VL_EC. (Page 40)-* Power request.

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Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	46	3.3VALWP/5VALWP	12/31	Compal	PWR request	Add PU302, control signal changed to ACOFF	
2	51	VGA_COREP	12/31	Compal	PWR request	Connect the PR715 and PC714 to PQ703 pin1	
3	51	VGA_COREP	12/31	Compal	EMI request	Change PC705 to 2220pF	
4	50	CPU_CORE	12/31	Compal	EMI request	Add PC238, PC239, PC240, PC248	
5	50	CPU_CORE	12/31	Compal	Vendor request	Change PR221 and PR231 to 16.6K_ohm Change PR217 and PR233 to 4.02K_ohm Change PR223 to 17.8K_ohm Change PR224 to 100K_ohm	
6	45	Charger	12/31	Compal	EMI request	add PC128	
7	45	Charger	01/04	Compal	PWR request	Change PQ102 to FDS6675BZ	
8	50	CPU_CORE	01/04	Compal	PWR request	Change PQ204, PQ205, PQ207, PQ208 to FDS6676AS Add PQ209 and PQ234 to fix CPU core voltage.	
9	44	DC Connector /CPU_OTP	01/09	Compal	AC LED change to KBC control	AC_LED connect to KBC pin 97	
10	51	VGA_COREP	02/27	Compal	Change VGA low voltage to 0.95V	Change PR712 to 49.9K_ohm and PR711 to 37.4K_ohm	
11	46	3.3VALWP/5VALWP	02/27	Compal	Change OTC shun down pin.	Change OTC shun down pin to PU301 pin13.	
12	50	CPU_CORE	03/03	Compal	EMI request	Add PC249, PC250	
13	45	Charger	03/03	Compal	EMI request	Add PC129	
14	50	CPU_CORE	03/03	Compal	HW request	Add H_PWRGD	
15	44	DC Connector /CPU_OTP	04/02	Compal	AC LED issue	Change AC_LED# pull high to +3VLP	
16	50	CPU_CORE	04/24	Compal	acoustic noise	Add PC251	
17	44	DC Connector /CPU_OTP	04/24	Compal	HW CPU thermal protection change to 95 +-3 degree C	Change PR12 to 2.21K_ohm	

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LA-4112P Rev0.2 -> 0.3 Product Improvement Record (P.I.R.)

Circuit change list:

1. Un-Stuff C18, Q127, Q129, R175, R814, C939 and change SMBus 2 -> SMBus 1. (Page 6)-* Follow 17" AMD circuit change.
2. Add signal H_PWRGD_CPU to option CPU core chip`s PWR OK. (Page 6)-* Follow AMD recommand power up sequence change.
3. Change signal name ENTRIP2 to EN0. (Page 6)-* For power team chagne request.
4. Un-Stuff C54. (Page 7)-* Follow 17" AMD circuit change.
5. AVDD1, AVDD2, AVDDI, AVDDQ, .PLVDD, PLVDD18, VDDLTP18, VDDLTP18_1, VDDLTP18_2 directly conecct to GND.
(Page11)-* For RX781 change recommand.
6. VDD18_MEM1, VDD18_MEM_2 directly conecct to GND. (Page 13)-* For RX781 change recommand.
7. Change Bead L16, L22 to 0 ohm and Delete L20, L21 than use jumper to link the power. (Page 13)-* Follow 17" AMD circuit change.
8. Change R101, R102 3K -> 1K ohm. (Page 14)-* ATI recommand.
9. Add VGA_PWN to Panel. (Page 16/24)-* For panel power saving request.
10. Un-stuff R1101. (Page 21)-* For PCI-E EA request.
11. Add signal CLK_14M_SIO. (Page 22)-* For debug port request.
12. Stuff C447. (Page 23)-* EMI/ESD recommand.
13. Add +5VS power for webcam`s LDO power option. (Page 24)-* Follow 17" AMD circuit change.
14. Change C863 0.047U -> 1000p. (Page 24)-* Fix panel power down waveform bounce.
15. Change Bead L61, L61 to 0 ohm. (Page 29)-* Follow 17" AMD circuit change.
16. Un-stuff R1148, C1271. (Page 32)-* Follow 17" AMD circuit change.
17. Modify JRJ45 layout footprint. (Page 32)-* For DFX request.
18. Add D58 ESD diode. (Page 32)-* EMI/ESD recommand.
19. Stuff R1043, Un-stuff R1042 (Page 33)-* Follow 17" AMD circuit change.
20. Add R399, R400 and un-stuff R122, R1051, Q53.(Page 34)-* Follow project common design.
21. Add C259, C260, C261 and stuff C746, C747,C748 and change C760, C761, C762, C763 100p -> 330p. (Page 35/36)-* EMI/ESD recommand.
22. Signal INTMIC_DET directly connect to AGND and Delete Q160, Q151, R951. (Page 35/36)-* OPP dont need the detect circuit.
23. Add C258. (Page 38)-* EMI/ESD recommand.
24. ME change JP32 and change Q24`s power +3VALW -> +3VS. (Page 38)-* Follow 17" AMD circuit change.
25. Add LPC debug port. (Page 39)-* For debug request.
26. Add D57, R397. (Page 40)-* Fix AC-IN chip power rail different issue.
27. Delete Q34, R645. (Page 41)-* Follow 17" AMD circuit change.
28. Add C262, C263. (Page 41)-* For Small/B design change.
29. Chagne C1175 type B2 ->Y. (Page 18)-* For fixed ME issue.
30. Add C264. (Page 22)-* For IDT request.
31. Add L85, L86, L87, L88. (Page 22)-* For EMI/ESD recommand.

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LA-4112P Rev0.3 -> 1.0 Product Improvement Record (P.I.R.)

Circuit change list:

1. Reserve R59, R60, R61. (Page 6)-* AMD suggest to reserve the pull high/down resistor of these test pin.
2. Add C477 0.1UF. (Page 23)-* For EMI recommand.
3. Change R906 from 0 ohm to 1k ohm. (Page 36)-* For reduce MIC background noise issue.
4. Change SMB DA1/CK1 pull high power rail from +3VALW to +3VL. (Page 40)-* EC recommand & follow Riply change list.
5. Add C819 0.1UF & D31 ESD diode. (Page 41)-* For EMI recommand.
6. Add R414 & R415 0 ohm. (Page 43)-* no support DIM function.
8. Add R140 & R234 750k ohm. (Page 43)-* Solve Rds on issue.

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