

S-SERIES 2009

INVICTA (Intel-Discrete)

MV Build (A03) - Final

2009.03.18

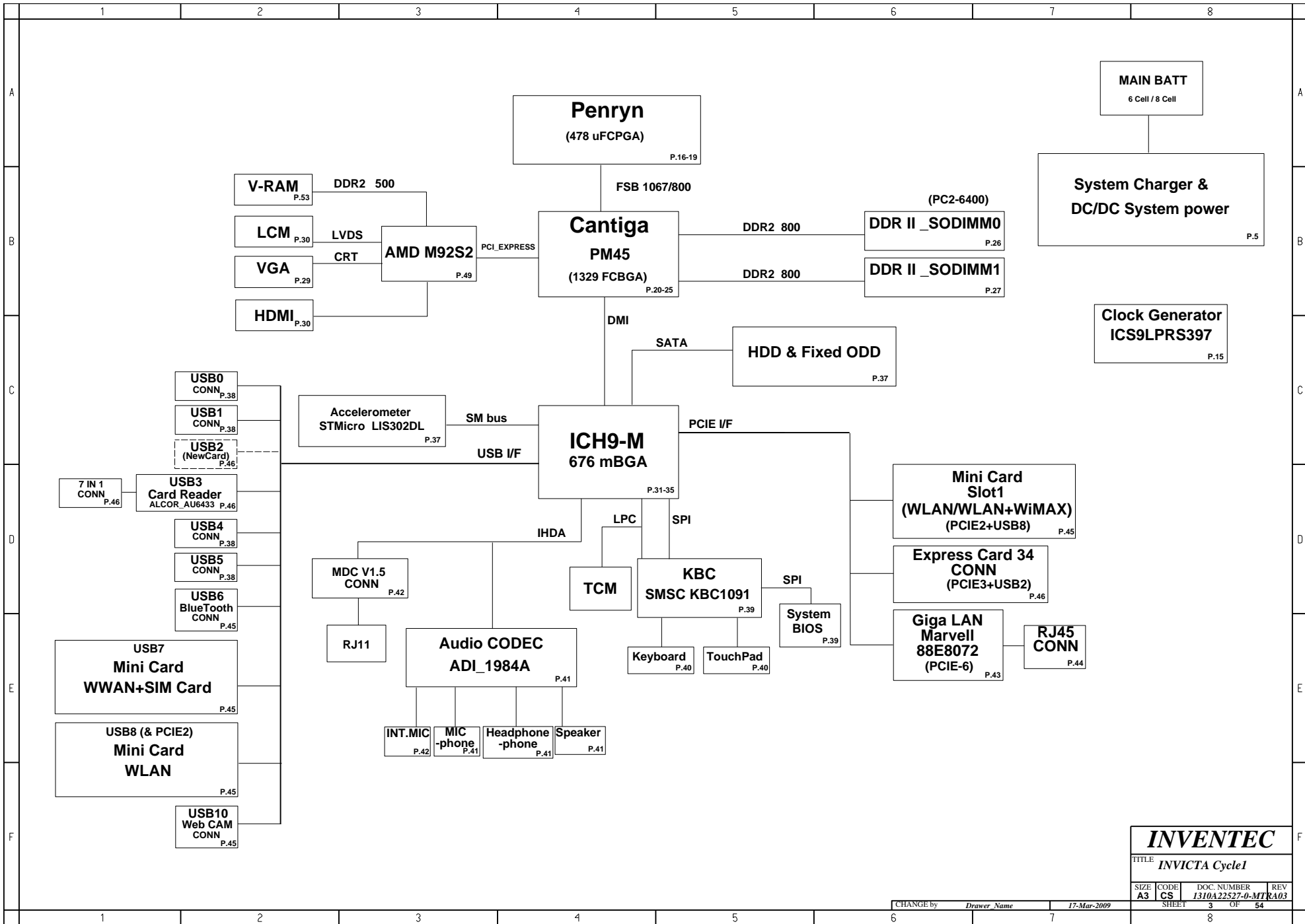
DATE	CHANGE NO.	REV

DRAWER	EE	DATE	POWER	DATE	INVENTEC		
DESIGN							
CHECK							
RESPONSIBLE							
TITLE					<i>INVICTA Cycle1</i>		
SIZE =	3	VER :					
FILE NAME :	XXXX-XXXXXX-XX			SIZE	CODE	DOC. NUMBER	REV
P/N	XXXXXXXXXXXX			A3	CS	J310A22527-0-MTR	A03
					SHEET	1	OF 54

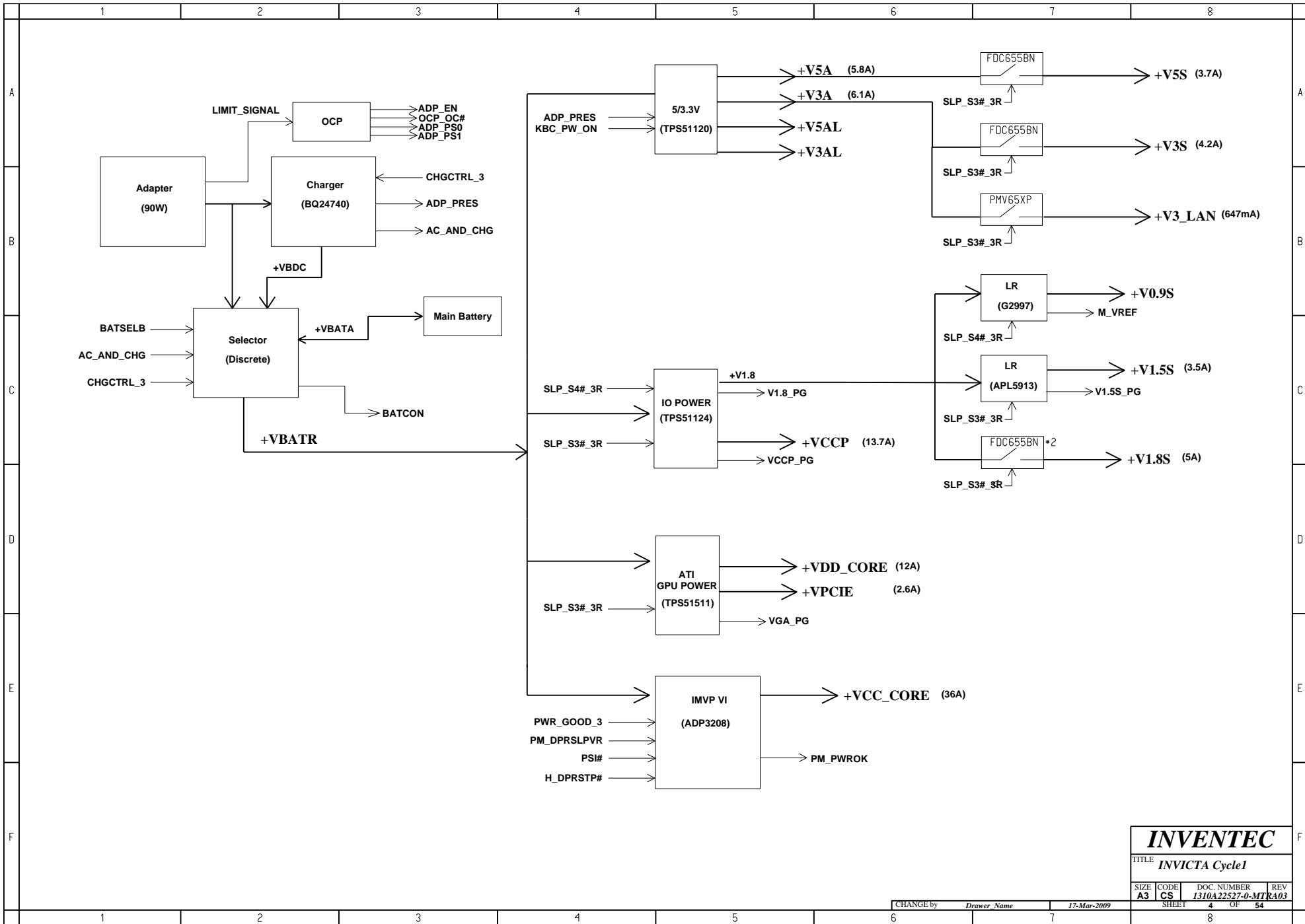
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7- System Power (+V3A/+V5A).	17- CPU Penryn-2.	38- USB CONN.
8- System Power (+V1.8/+VCCP) .	18- CPU Penryn-3.	39- KBC, BIOS ROM, Debug Port.
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INVENTEC			
TITLE <i>INVICTA Cycle1</i>			
Contents			
SIZE A3	CODE CS	DOC NUMBER <i>1310A22527-0-MTR</i>	REV A03
CHANGE by <i>Drawer Name</i>		<i>17-Mar-2009</i>	
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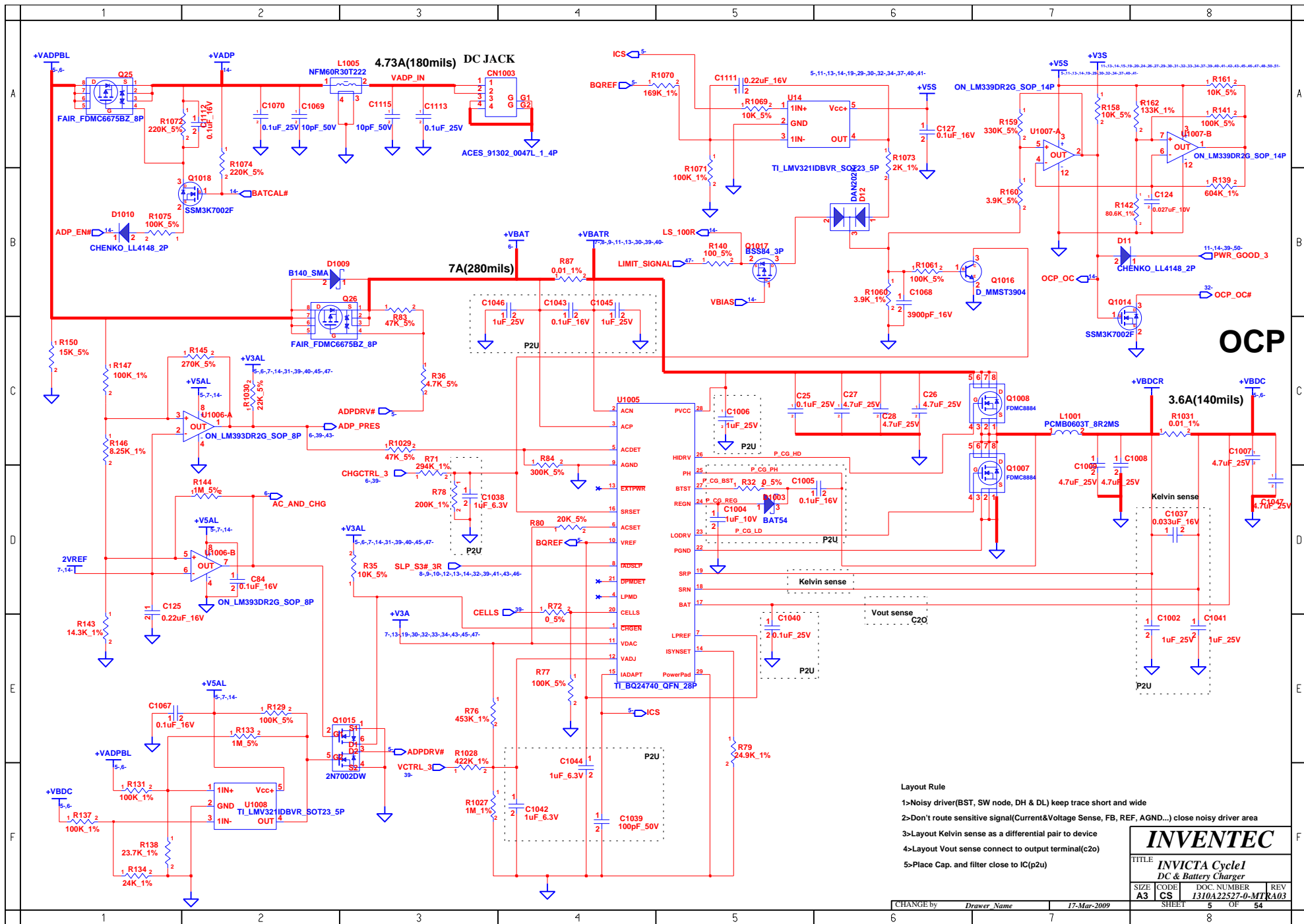
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SIZE A3	CODE CS	DOC. NUMBER 1310A22527-0-MTR	REV A03
CHANGE by Drawer Name		17-Mar-2009	SHEET 3 OF 54



INVENTEC

TITLE *INVICTA Cycle 1*

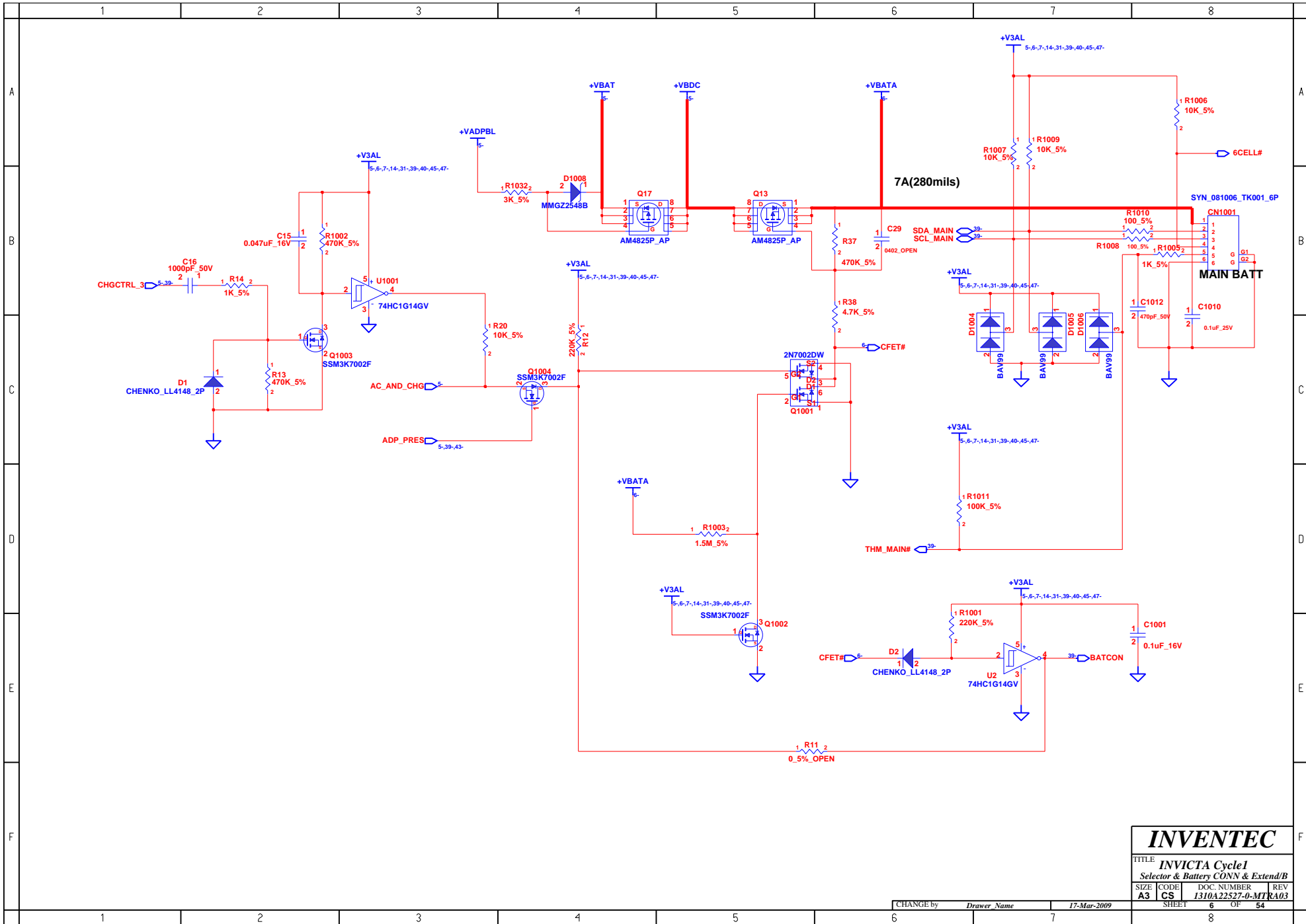
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A3	CS	1310A22527-0-MTR	A03



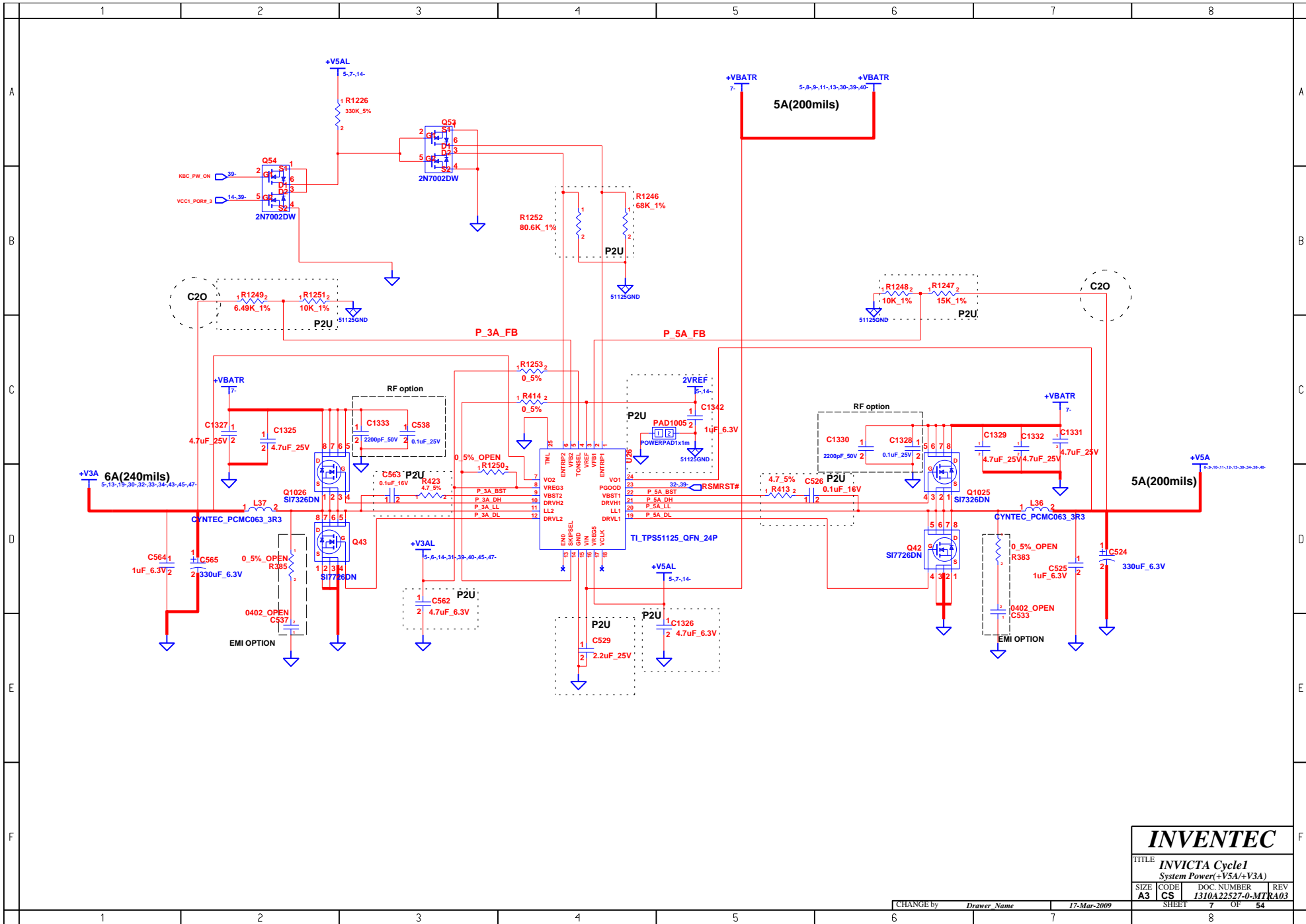
OCP

- Layout Rule**
- 1>Noisy driver(BST, SW node, DH & DL) keep trace short and wide
 - 2>Don't route sensitive signal(Current&Voltage Sense, FB, REF, AGND...) close noisy driver area
 - 3>Layout Kelvin sense as a differential pair to device
 - 4>Layout Vout sense connect to output terminal(c2o)
 - 5>Place Cap. and filter close to IC(p2u)

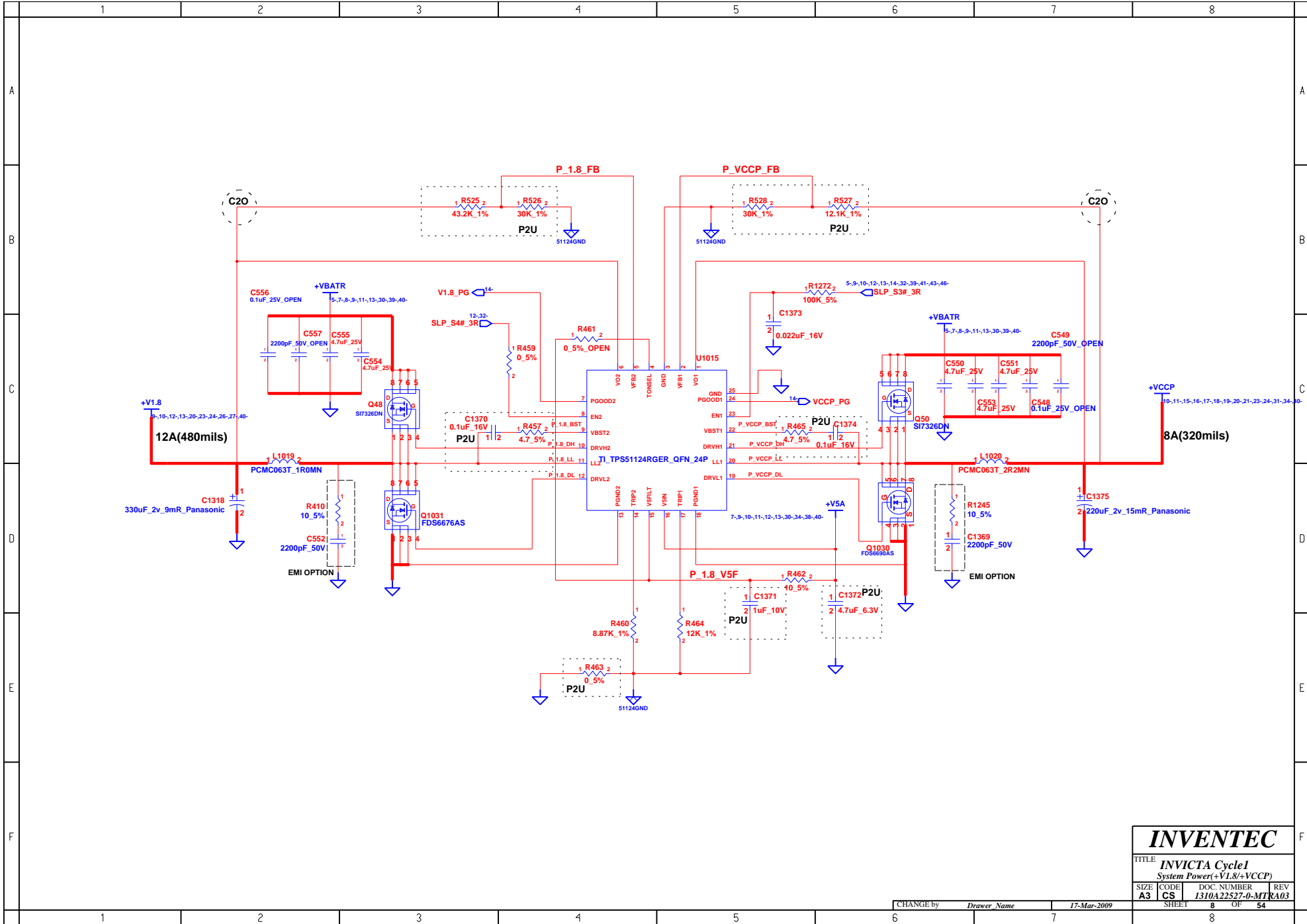
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SIZE: A3	CODE: CS	DOC NUMBER: I310A22527-0-MTR	REV: R403
CHANGE by: <i>Drawer Name</i>		17-Mar-2009	
SHEET: 5		OF: 54	



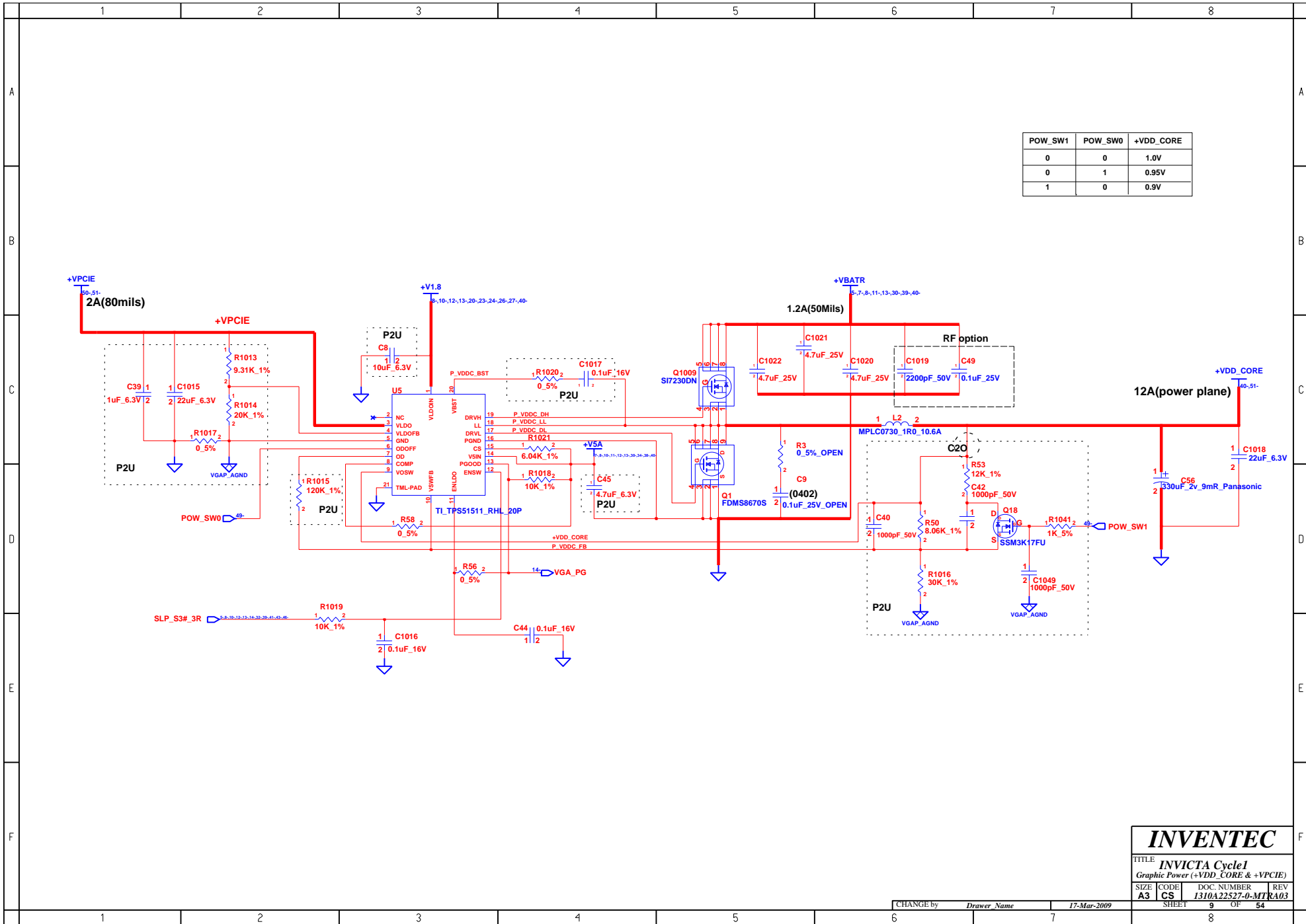
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TITLE INVICTA Cycle1			
Selector & Battery CONN & Extend/B			
SIZE A3	CODE CS	DOC NUMBER 1310A22527-0-MT	REV A03
CHANGE by <i>Drawer Name</i>		17-Mar-2009	
SHEET 6		OF 54	



INVENTEC			
TITLE: INVICTA Cycle1			
System Power(+V5A/+V3A)			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MT	R403



INVENTEC			
TITLE <i>INVICTA Cycle 1</i>			
System Power(+V1.8/+VCCP)			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310A22527-0-MT	R403
CHANGE by		Drawer Name	17-Mar-2009
SHEET		8	OF 54

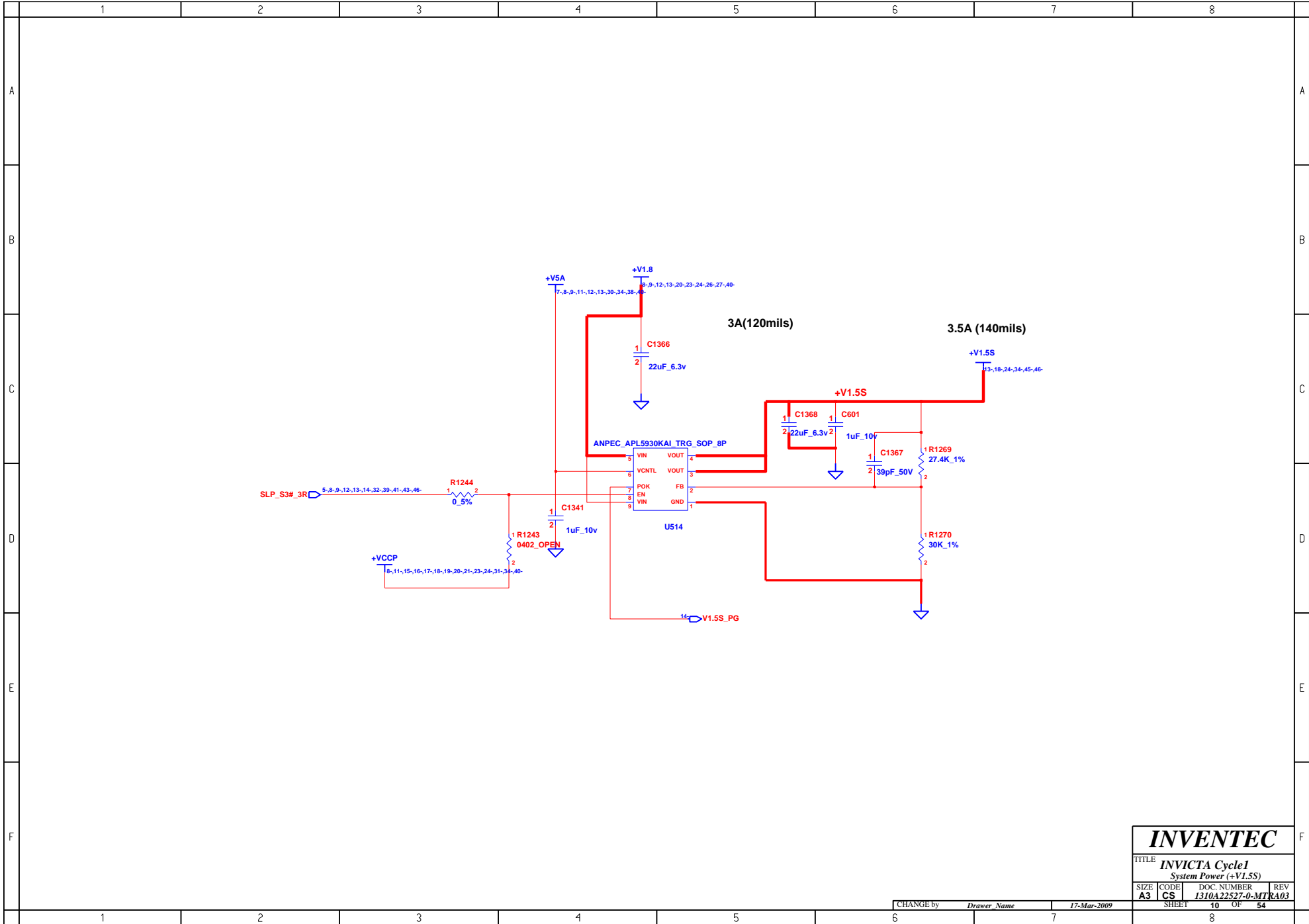


INVENTEC

TITLE: **INVICTA Cycle1**
 Graphic Power (+VDD_CORE & +VPCIE)

SIZE	CODE	DOC. NUMBER	REV
A3	CS	I310A22527-0-MTR	A03

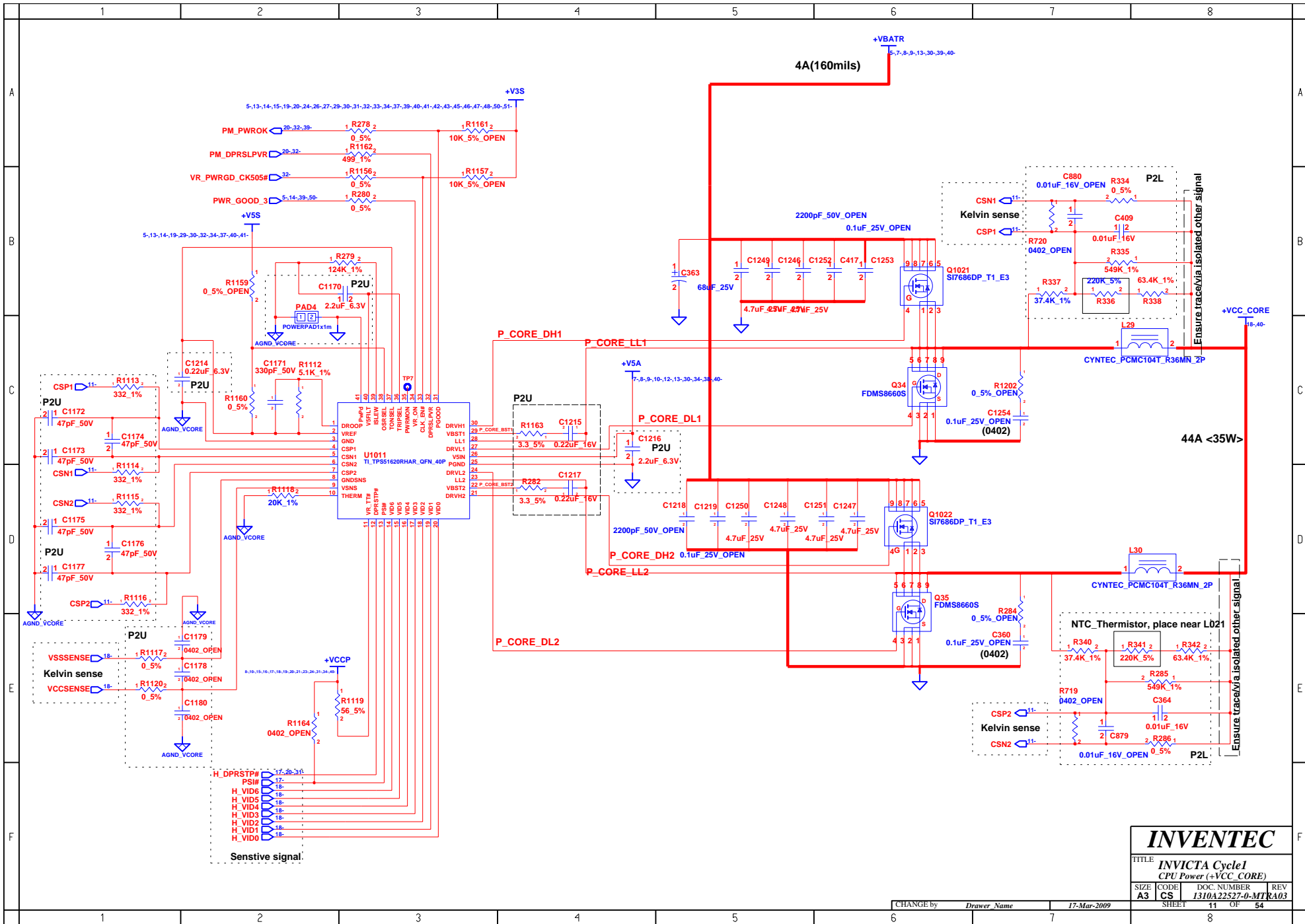
CHANGE by: *Drawer Name* 17-Mar-2009 SHEET 9 OF 54



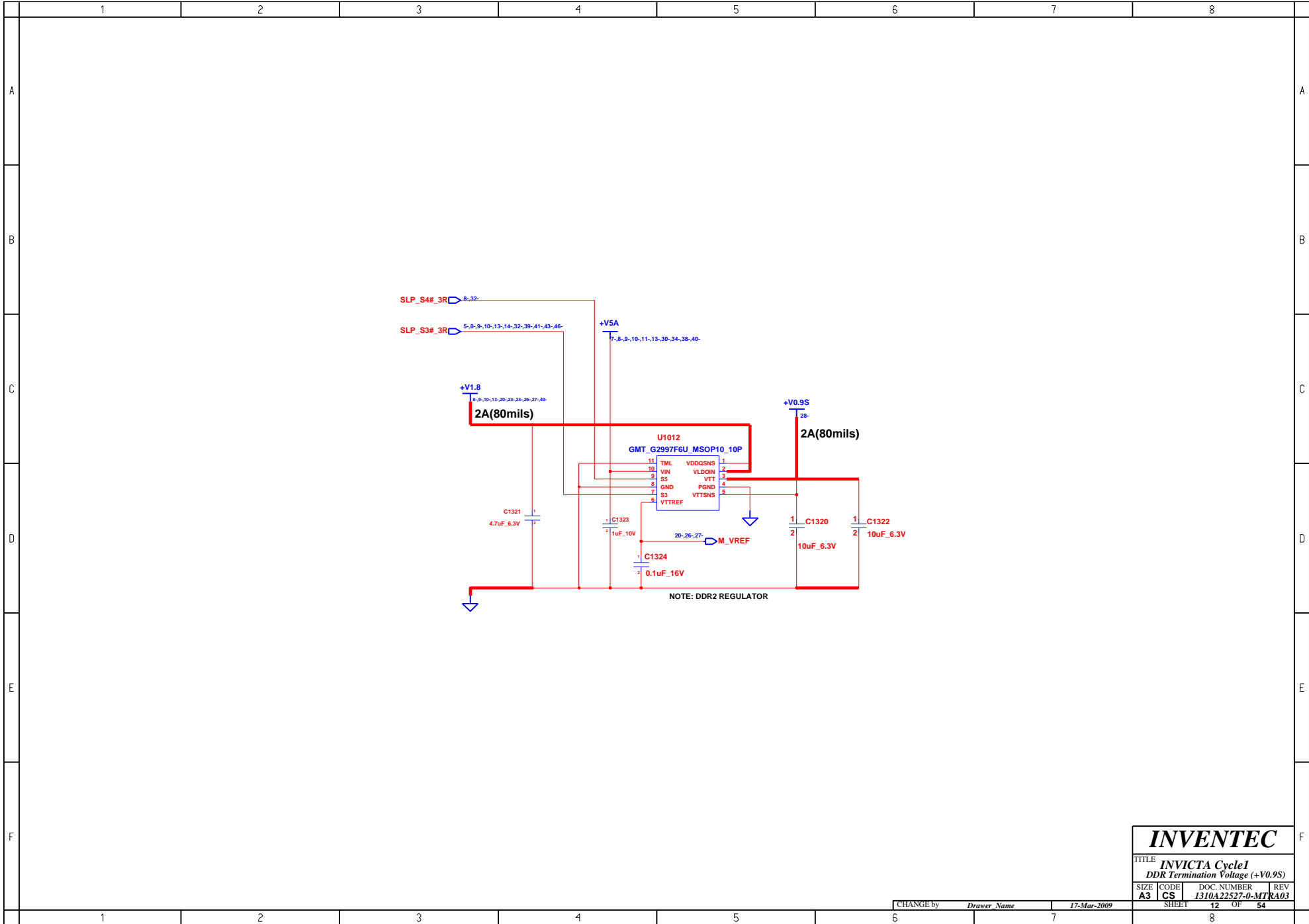
INVENTEC

TITLE **INVICTA Cycle 1**
System Power (+V1.5S)

SIZE A3	CODE CS	DOC. NUMBER I310A22527-0-MTR	REV A03
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INVENTEC			
TITLE: INVICTA Cycle1 CPU Power (+VCC_CORE)			
SIZE: A3	CODE: CS	DOC. NUMBER: I310A22527-0-MTR	REV: R03
CHANGE by: Drawer Name		17-Mar-2009	
SHEET: 11		OF: 54	



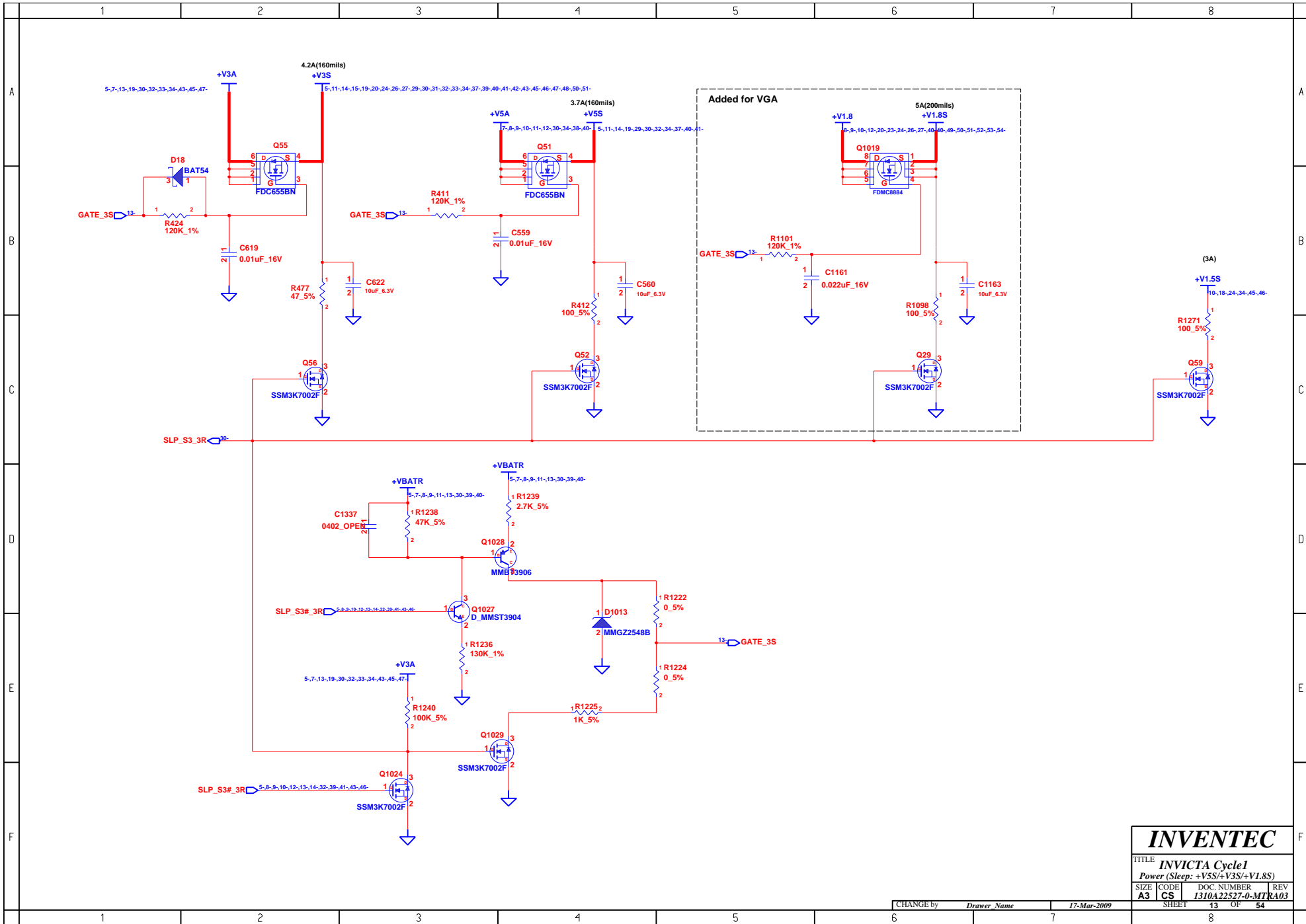
INVENTEC

TITLE **INVICTA Cycle1
DDR Termination Voltage (+V0.9S)**

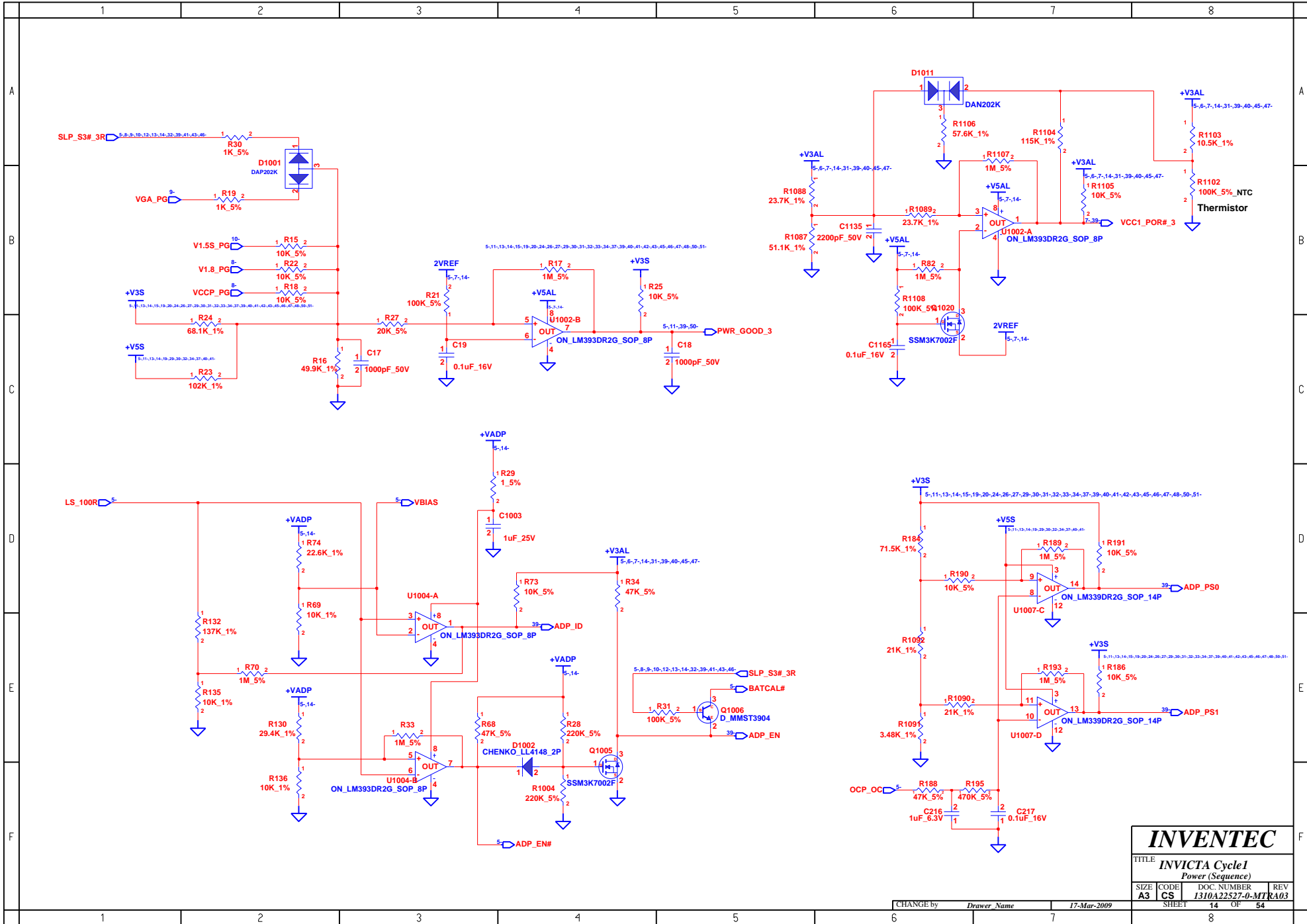
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CHANGE by *Drawer Name* 17-Mar-2009

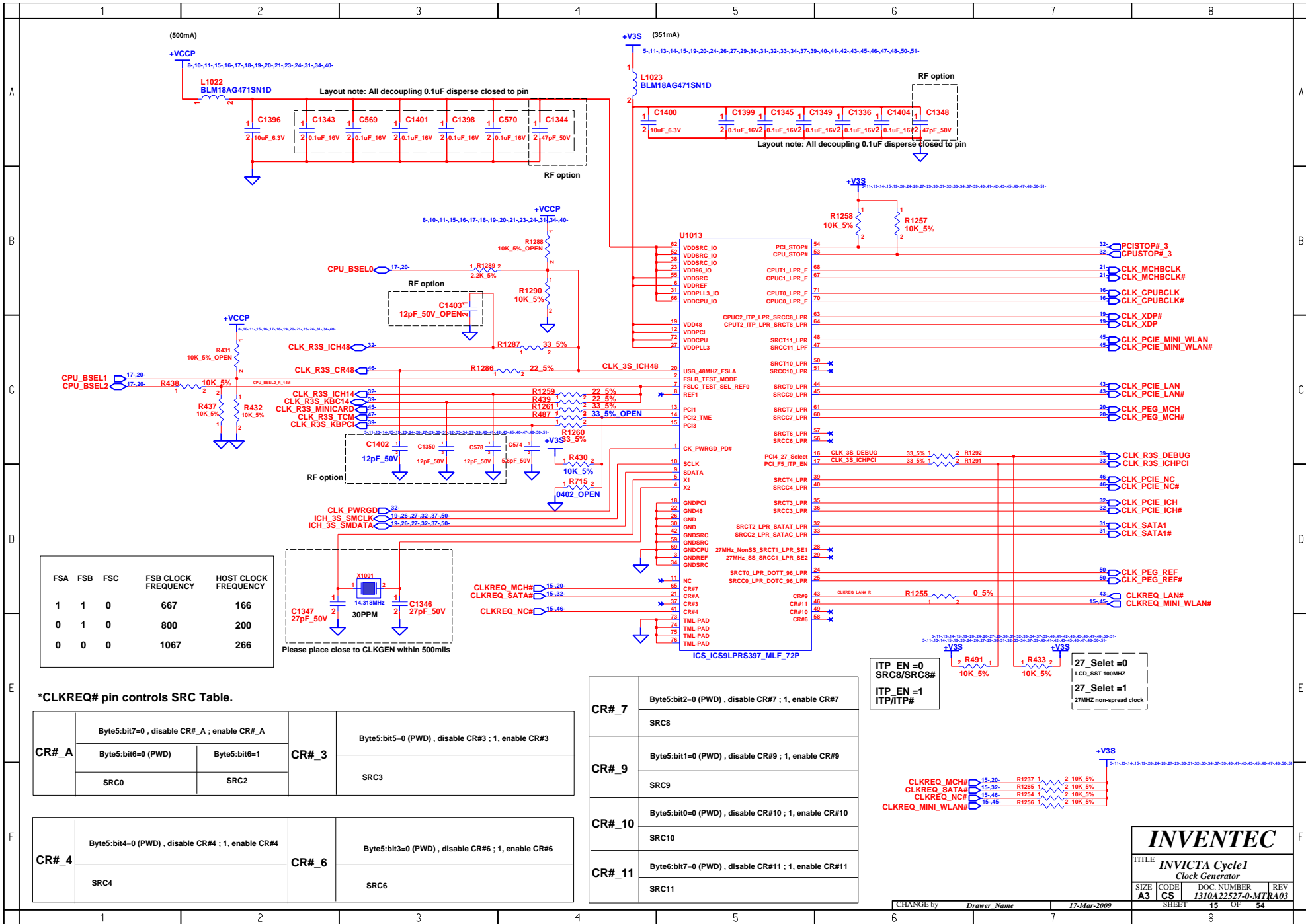
SHEET 12 OF 54



INVENTEC			
TITLE <i>INVICTA Cycle 1</i>			
Power (Sleep: +VSS/+V3S/+V1.8S)			
SIZE	CODE	DOC NUMBER	REV
A3	CS	I310A22527-0-MT	R403
CHANGE by		Drawer Name	17-Mar-2009
SHEET		13	OF 54



INVENTEC			
TITLE INVICTA Cycle1 Power (Sequence)			
SIZE A3	CODE CS	DOC NUMBER 1310A22527-0-MTR	REV A03
CHANGE by Drawer Name		17-Mar-2009	SHEET 14 OF 54



FSA	FSB	FSC	FSB CLOCK FREQUENCY	HOST CLOCK FREQUENCY
1	1	0	667	166
0	1	0	800	200
0	0	0	1067	266

*CLKREQ# pin controls SRC Table.

CR#_A	Byte5:bit7=0 (PWD), disable CR#_A ; enable CR#_A		CR#_3	Byte5:bit5=0 (PWD), disable CR#3 ; 1, enable CR#3	
	Byte5:bit6=0 (PWD)	Byte5:bit6=1		SRC0	SRC2
CR#_4	Byte5:bit4=0 (PWD), disable CR#4 ; 1, enable CR#4		CR#_6	Byte5:bit3=0 (PWD), disable CR#6 ; 1, enable CR#6	
	SRC4			SRC6	

CR#_7	Byte5:bit2=0 (PWD), disable CR#7 ; 1, enable CR#7
	SRC8
CR#_9	Byte5:bit1=0 (PWD), disable CR#9 ; 1, enable CR#9
	SRC9
CR#_10	Byte5:bit0=0 (PWD), disable CR#10 ; 1, enable CR#10
	SRC10
CR#_11	Byte6:bit7=0 (PWD), disable CR#11 ; 1, enable CR#11
	SRC11

ITP_EN=0
SRC8/SRC8#
ITP_EN=1
ITP/ITP#

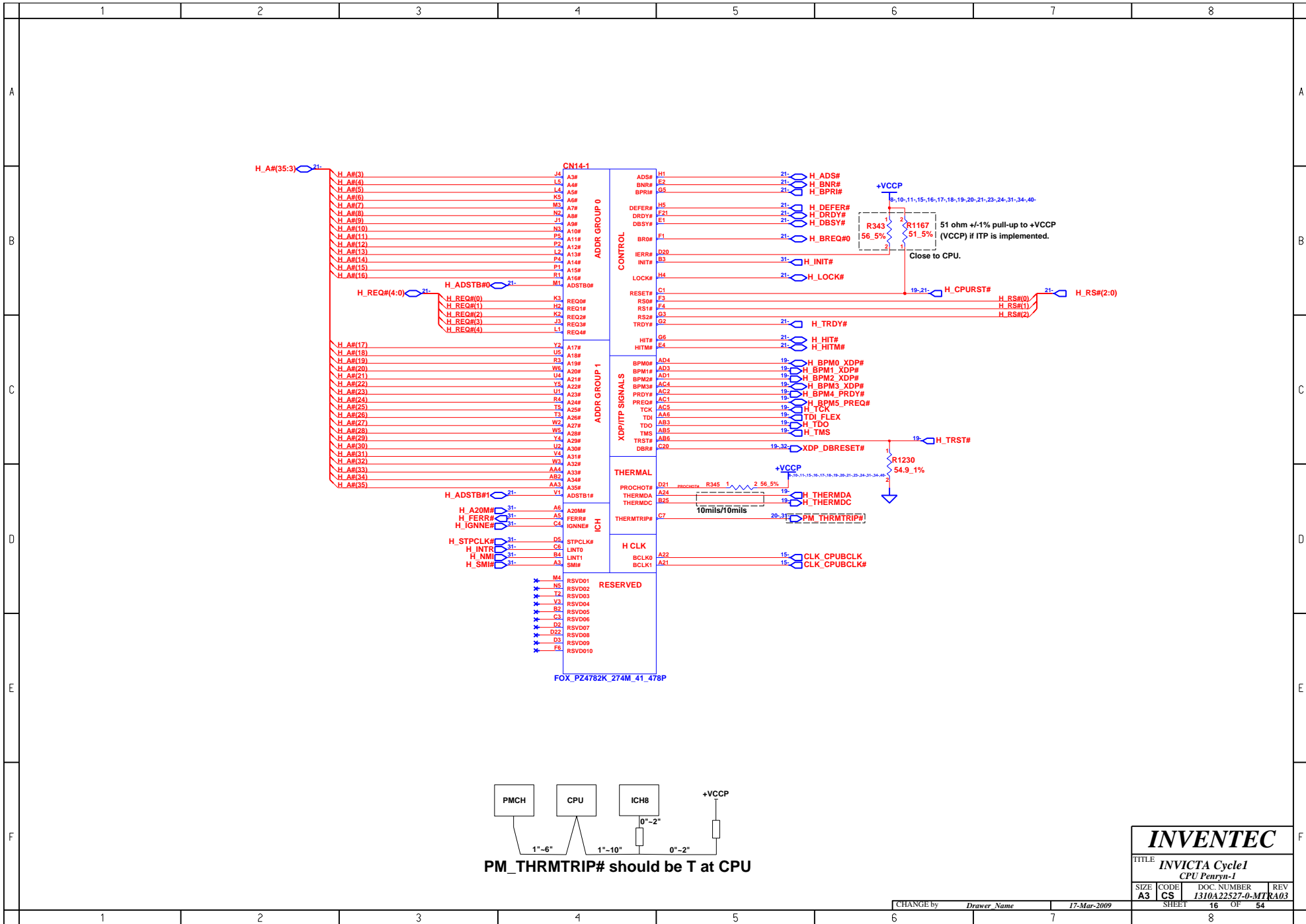
27_Select=0
LCD_SST 100MHz
27_Select=1
27MHz non-spread clock

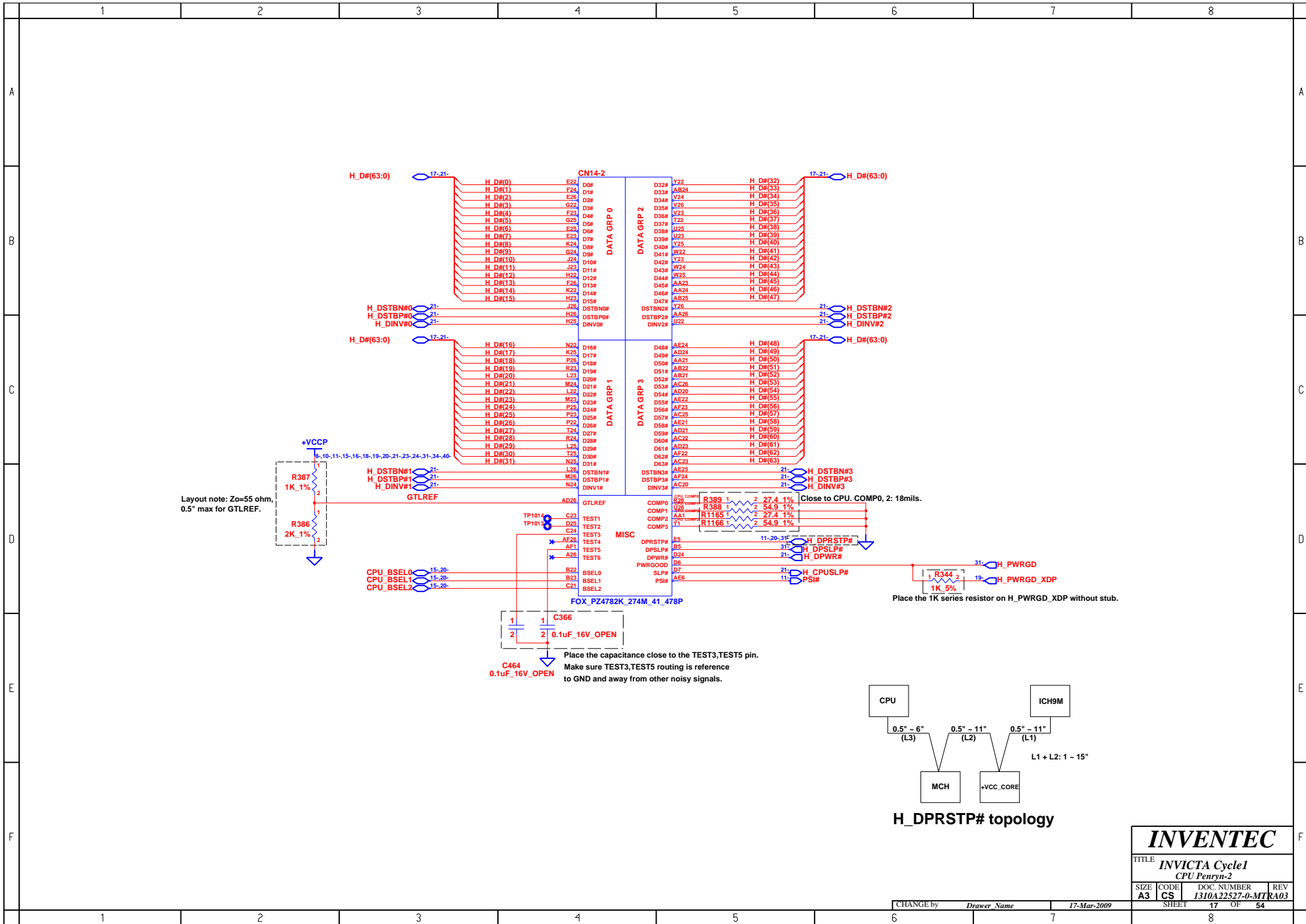
INVENTEC

TITLE
INVICTA Cycle1
Clock Generator

SIZE CODE DOC NUMBER REV
A3 CS 1310A22527-0-MTR A03

CHANGE by Drawer Name 17-Mar-2009 SHEET 15 OF 54

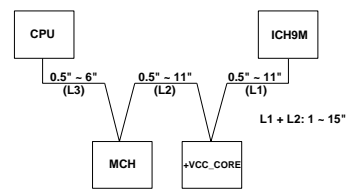




Layout note: Zo=55 ohm,
0.5" max for GTLREF.

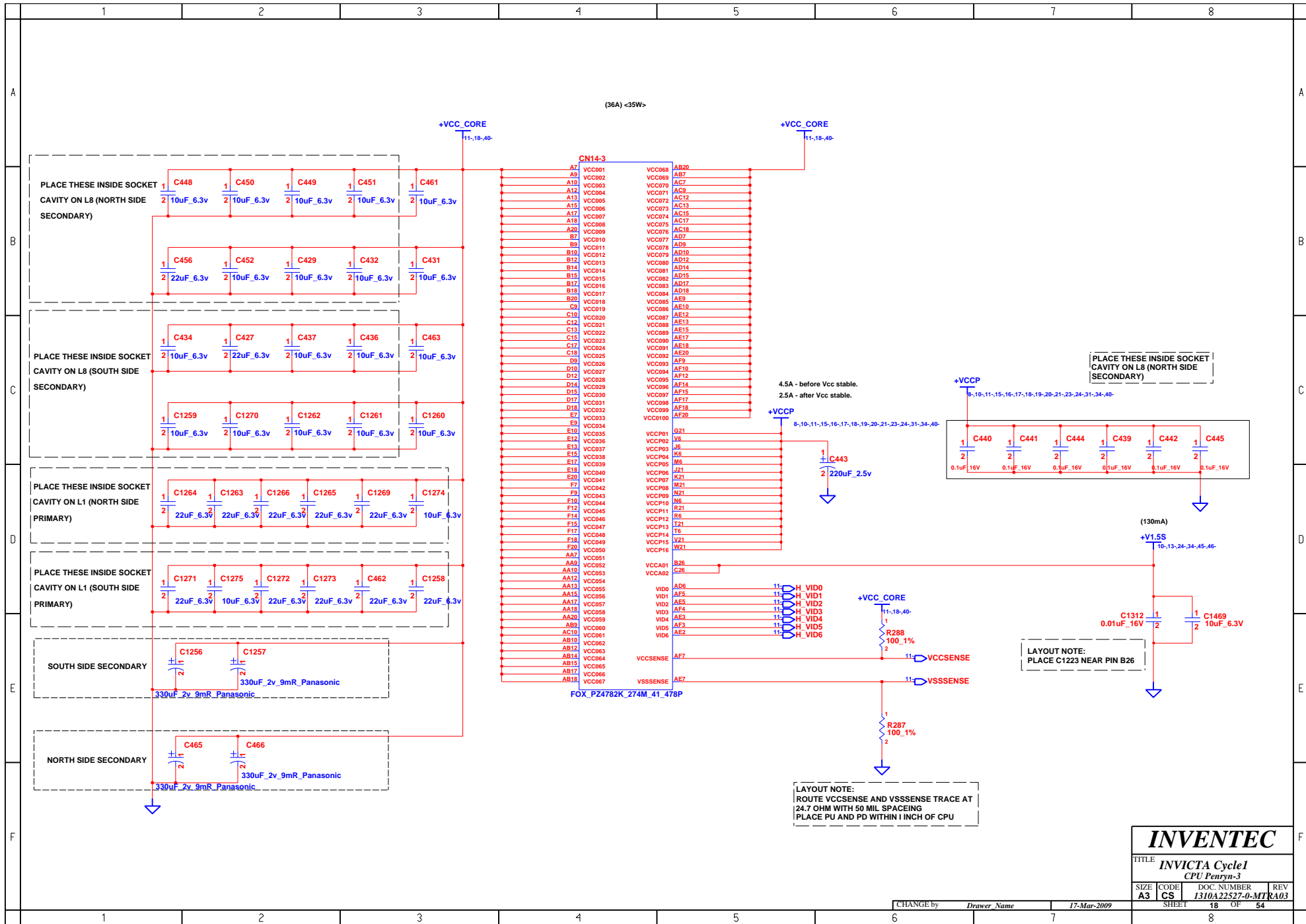
Place the capacitance close to the TEST3, TEST5 pin.
Make sure TEST3, TEST5 routing is reference
to GND and away from other noisy signals.

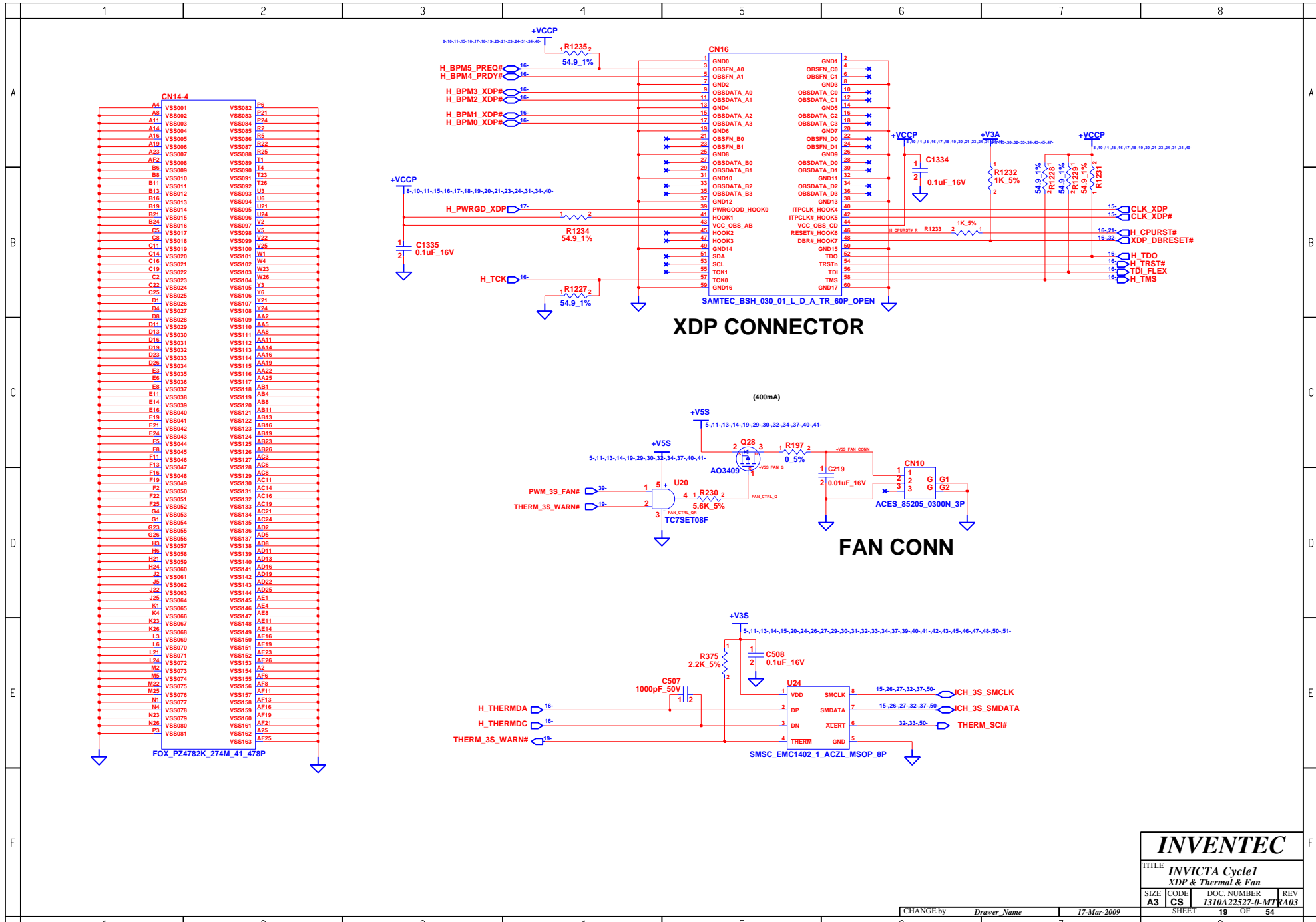
Close to CPU_COMP0, 2: 18mils.
Place the 1K series resistor on H_PWRGD_XDP without stub.



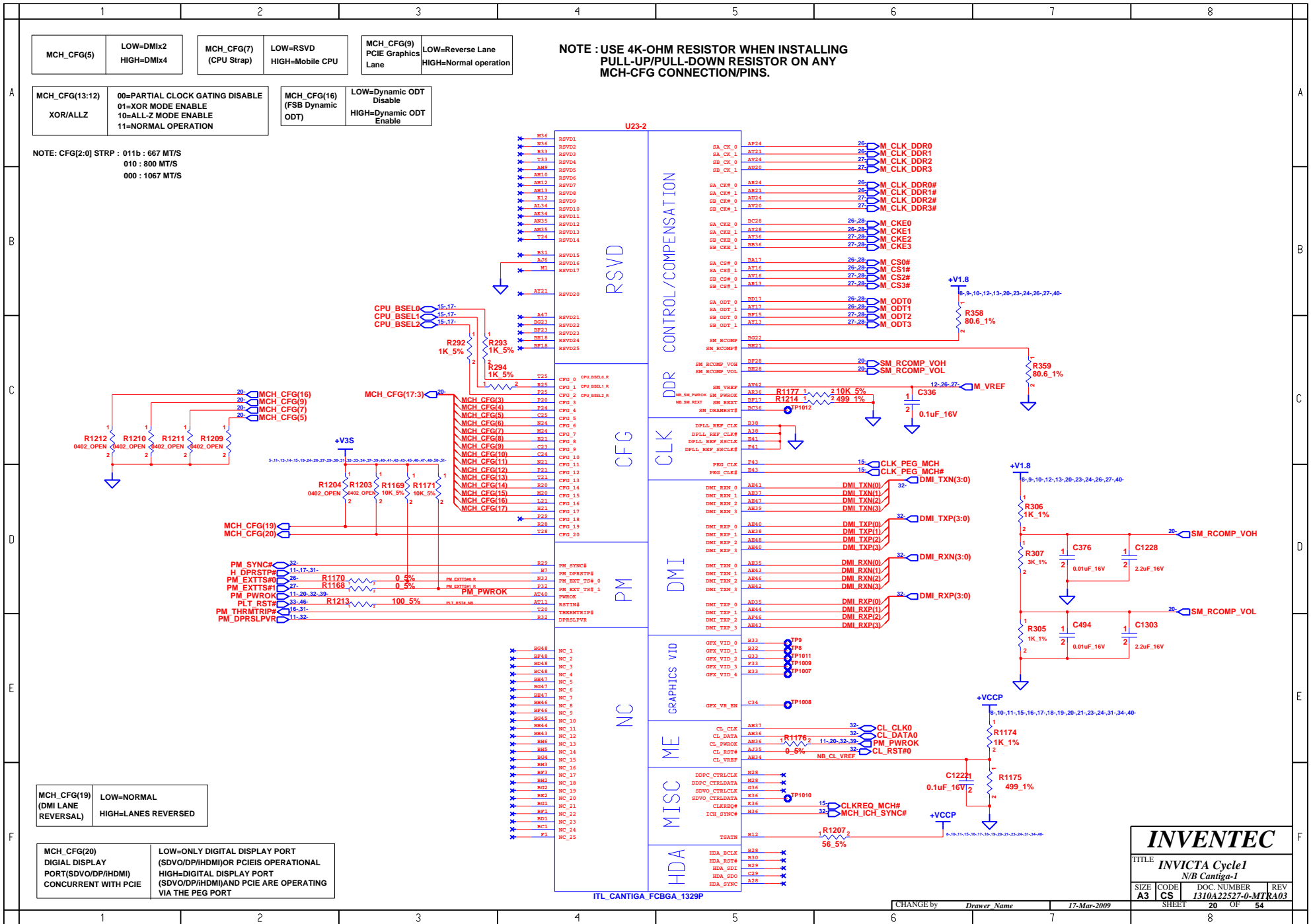
H_DPRSTP# topology

INVENTEC			
TITLE INVICTA Cycle1			
CPU Penryn-2			
SIZE A3	CODE CS	DOC NUMBER 1310A22527-0-MIT	REV A03
CHANGE by Drawer Name		17-Mar-2009	SHEET 17 OF 54





INVENTEC			
TITLE: INVICTA Cycle1 XDP & Thermal & Fan			
SIZE: A3	CODE: CS	DOC. NUMBER: I310A22527-0-MTR	REV: RA03
CHANGE by: Drawer Name		17-Mar-2009	
SHEET: 19		OF: 54	



NOTE : USE 4K-OHM RESISTOR WHEN INSTALLING PULL-UP/PULL-DOWN RESISTOR ON ANY MCH-CFG CONNECTION/PINS.

MCH_CFG(5)	LOW=DMiX2 HIGH=DMiX4	MCH_CFG(7) (CPU Strap)	LOW=RSVD HIGH=Mobile CPU	MCH_CFG(9) PCIE Graphics Lane	LOW=Reverse Lane HIGH=Normal operation
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MCH_CFG(13:12) XOR/ALLZ	00=PARTIAL CLOCK GATING DISABLE 01=XOR MODE ENABLE 10=ALL-Z MODE ENABLE 11=NORMAL OPERATION	MCH_CFG(16) (FSB Dynamic ODT)	LOW=Dynamic ODT HIGH=Dynamic ODT Enable
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NOTE: CFG[2:0] STRP : 011b : 667 MT/S
010 : 800 MT/S
000 : 1067 MT/S

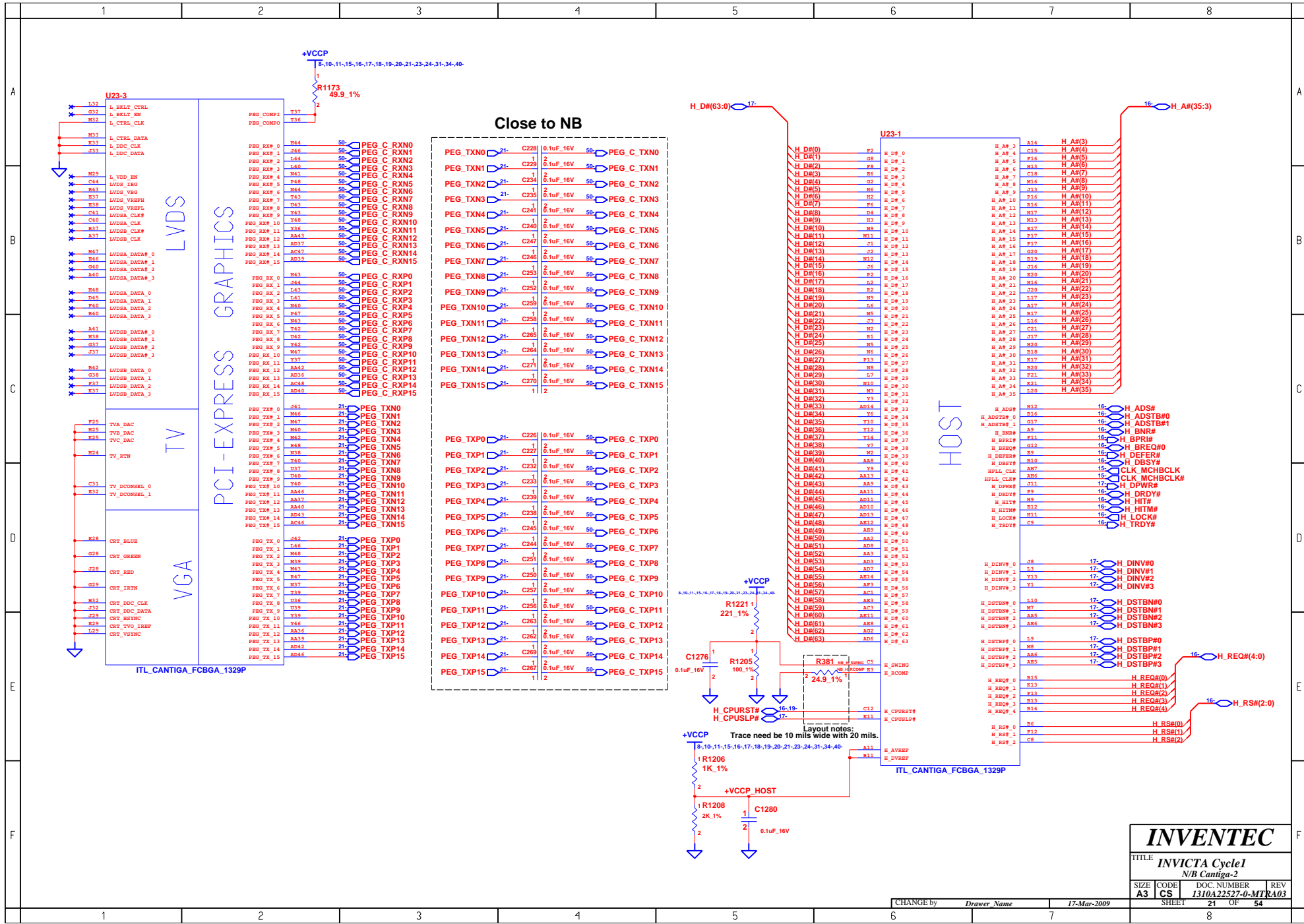
MCH_CFG(19) (DMI LANE REVERSAL)	LOW=NORMAL HIGH=LANES REVERSED
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MCH_CFG(20) DIGIAL DISPLAY PORT(SDVO(DP/HDMI)OR PCIEIS OPERATIONAL PORT(SDVO(DP/HDMI) CONCURRENT WITH PCIE	LOW=ONLY DIGITAL DISPLAY PORT HIGH=DIGITAL DISPLAY PORT (SDVO(DP/HDMI)AND PCIE ARE OPERATING VIA THE PEG PORT
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INVENTEC

TITLE: **INVICTA Cycle1**
/N/B Cantiga-1

SIZE A3	CODE CS	DOC. NUMBER 1310A22527-0-1	REV A03
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Close to NB

PEG_TXN0	21-	C228	0.1uF_16V	50-	PEG_C_TXN0
PEG_TXN1	21-	C229	0.1uF_16V	50-	PEG_C_TXN1
PEG_TXN2	21-	C230	0.1uF_16V	50-	PEG_C_TXN2
PEG_TXN3	21-	C235	0.1uF_16V	50-	PEG_C_TXN3
PEG_TXN4	21-	C241	0.1uF_16V	50-	PEG_C_TXN4
PEG_TXN5	21-	C240	0.1uF_16V	50-	PEG_C_TXN5
PEG_TXN6	21-	C247	0.1uF_16V	50-	PEG_C_TXN6
PEG_TXN7	21-	C246	0.1uF_16V	50-	PEG_C_TXN7
PEG_TXN8	21-	C253	0.1uF_16V	50-	PEG_C_TXN8
PEG_TXN9	21-	C252	0.1uF_16V	50-	PEG_C_TXN9
PEG_TXN10	21-	C259	0.1uF_16V	50-	PEG_C_TXN10
PEG_TXN11	21-	C258	0.1uF_16V	50-	PEG_C_TXN11
PEG_TXN12	21-	C265	0.1uF_16V	50-	PEG_C_TXN12
PEG_TXN13	21-	C264	0.1uF_16V	50-	PEG_C_TXN13
PEG_TXN14	21-	C271	0.1uF_16V	50-	PEG_C_TXN14
PEG_TXN15	21-	C270	0.1uF_16V	50-	PEG_C_TXN15

PEG_TXP0	21-	C226	0.1uF_16V	50-	PEG_C_TXP0
PEG_TXP1	21-	C227	0.1uF_16V	50-	PEG_C_TXP1
PEG_TXP2	21-	C232	0.1uF_16V	50-	PEG_C_TXP2
PEG_TXP3	21-	C233	0.1uF_16V	50-	PEG_C_TXP3
PEG_TXP4	21-	C239	0.1uF_16V	50-	PEG_C_TXP4
PEG_TXP5	21-	C238	0.1uF_16V	50-	PEG_C_TXP5
PEG_TXP6	21-	C245	0.1uF_16V	50-	PEG_C_TXP6
PEG_TXP7	21-	C244	0.1uF_16V	50-	PEG_C_TXP7
PEG_TXP8	21-	C251	0.1uF_16V	50-	PEG_C_TXP8
PEG_TXP9	21-	C250	0.1uF_16V	50-	PEG_C_TXP9
PEG_TXP10	21-	C257	0.1uF_16V	50-	PEG_C_TXP10
PEG_TXP11	21-	C256	0.1uF_16V	50-	PEG_C_TXP11
PEG_TXP12	21-	C263	0.1uF_16V	50-	PEG_C_TXP12
PEG_TXP13	21-	C262	0.1uF_16V	50-	PEG_C_TXP13
PEG_TXP14	21-	C269	0.1uF_16V	50-	PEG_C_TXP14
PEG_TXP15	21-	C267	0.1uF_16V	50-	PEG_C_TXP15

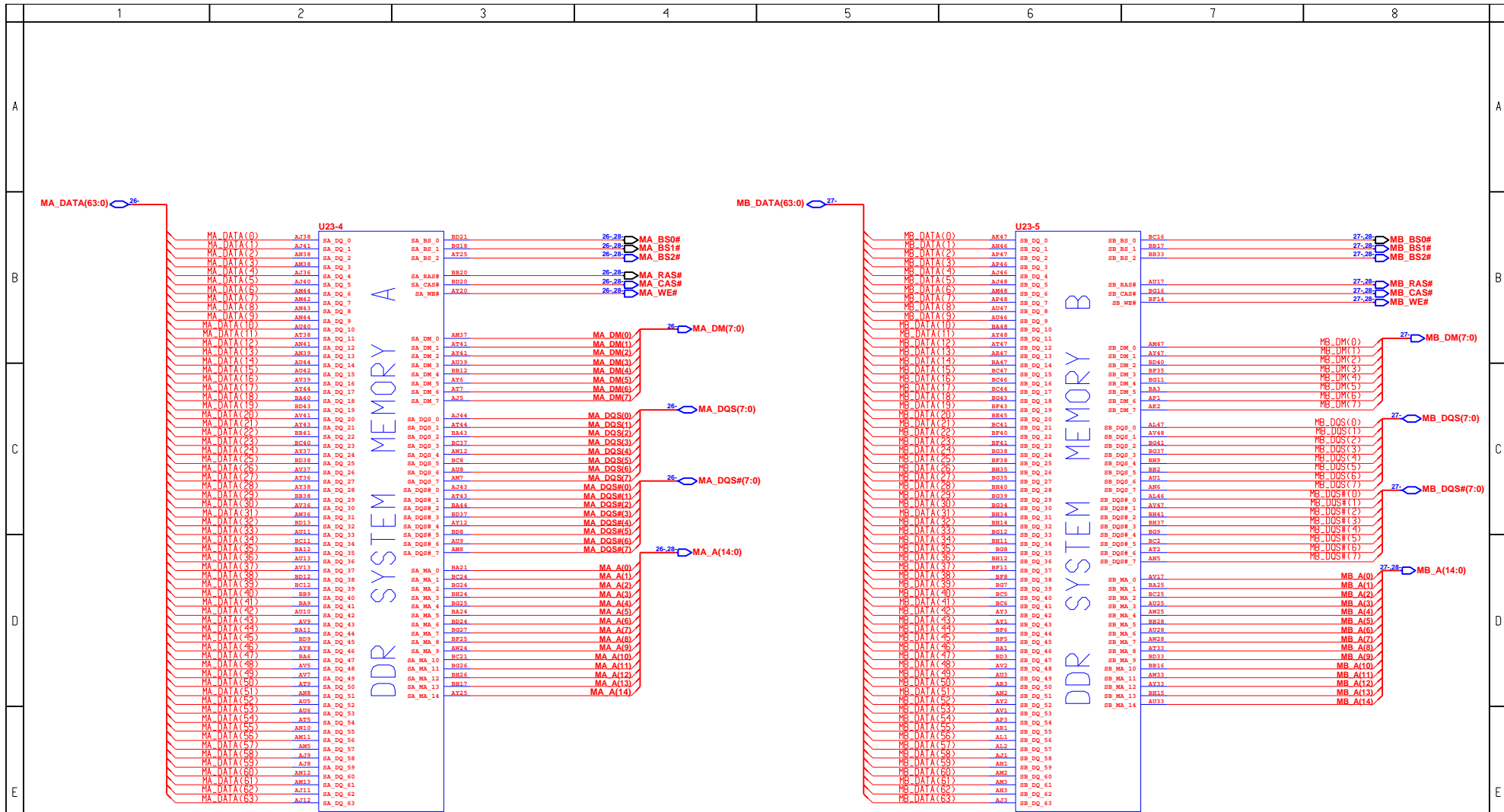
INVENTEC

TITLE: INVICTA Cycle1
N/B Cantiga-2

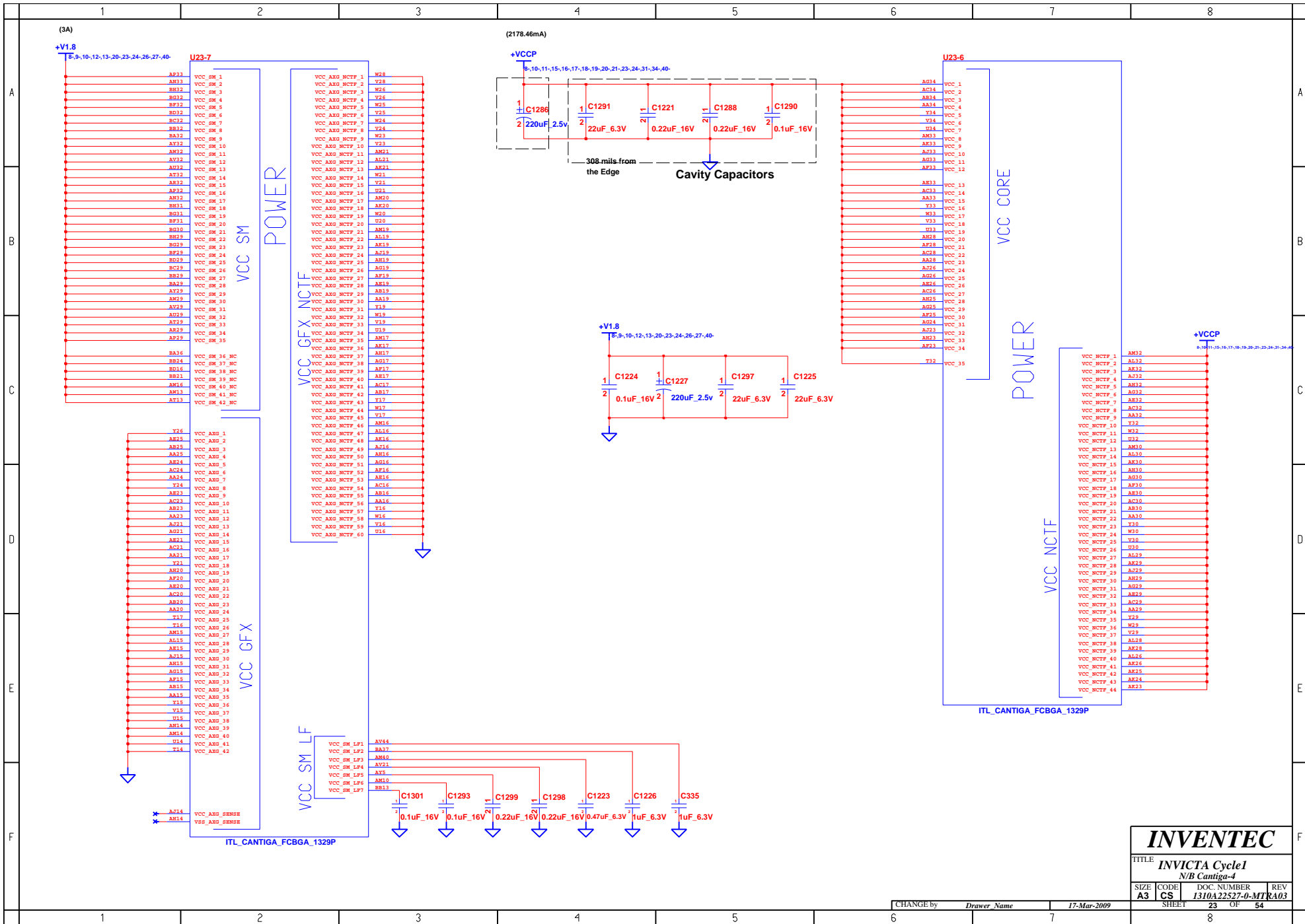
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTR	A03

CHANGE by: Drawer Name 17-Mar-2009

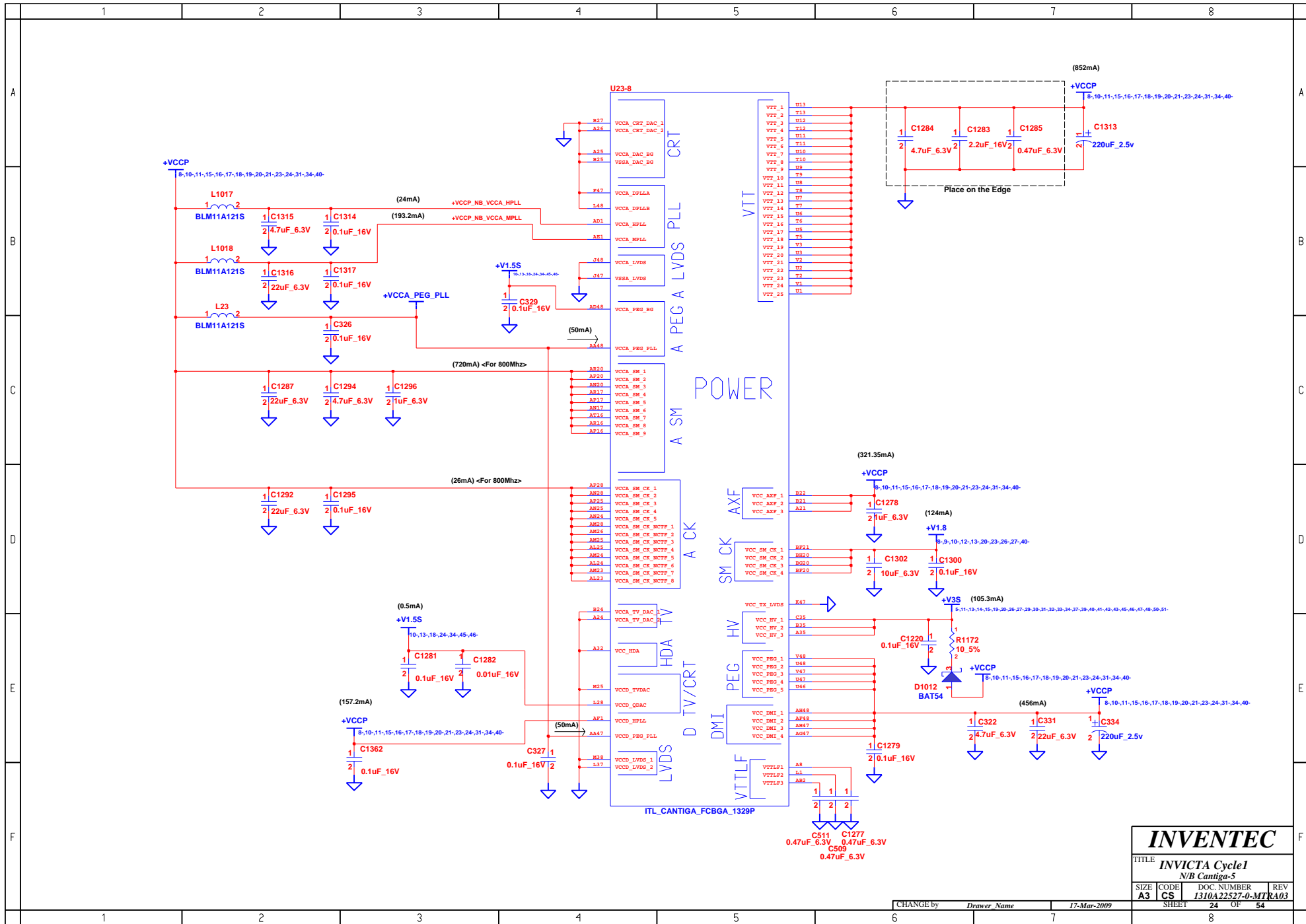
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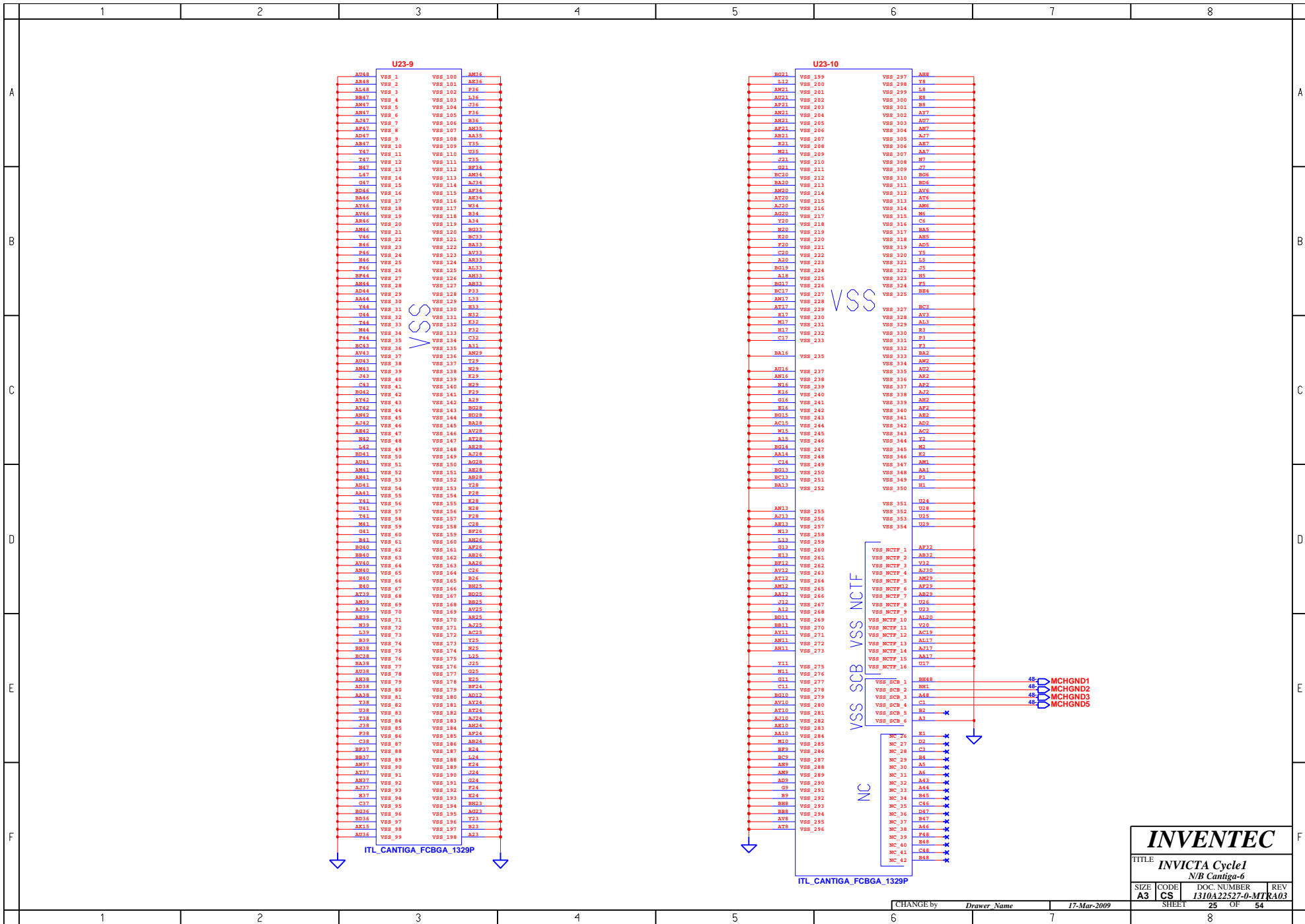
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N/B Cantiga-3			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTR	A03
CHANGE by		Drawer Name	17-Mar-2009
		SHEET	22 OF 54



INVENTEC			
TITLE <i>INVICTA Cycle1</i> <i>N/B Cantiga-4</i>			
SIZE A3	CODE CS	DOC NUMBER <i>1310A22527-0-MTR</i>	REV A03
CHANGE by <i>Drawer Name</i>		17-Mar-2009	
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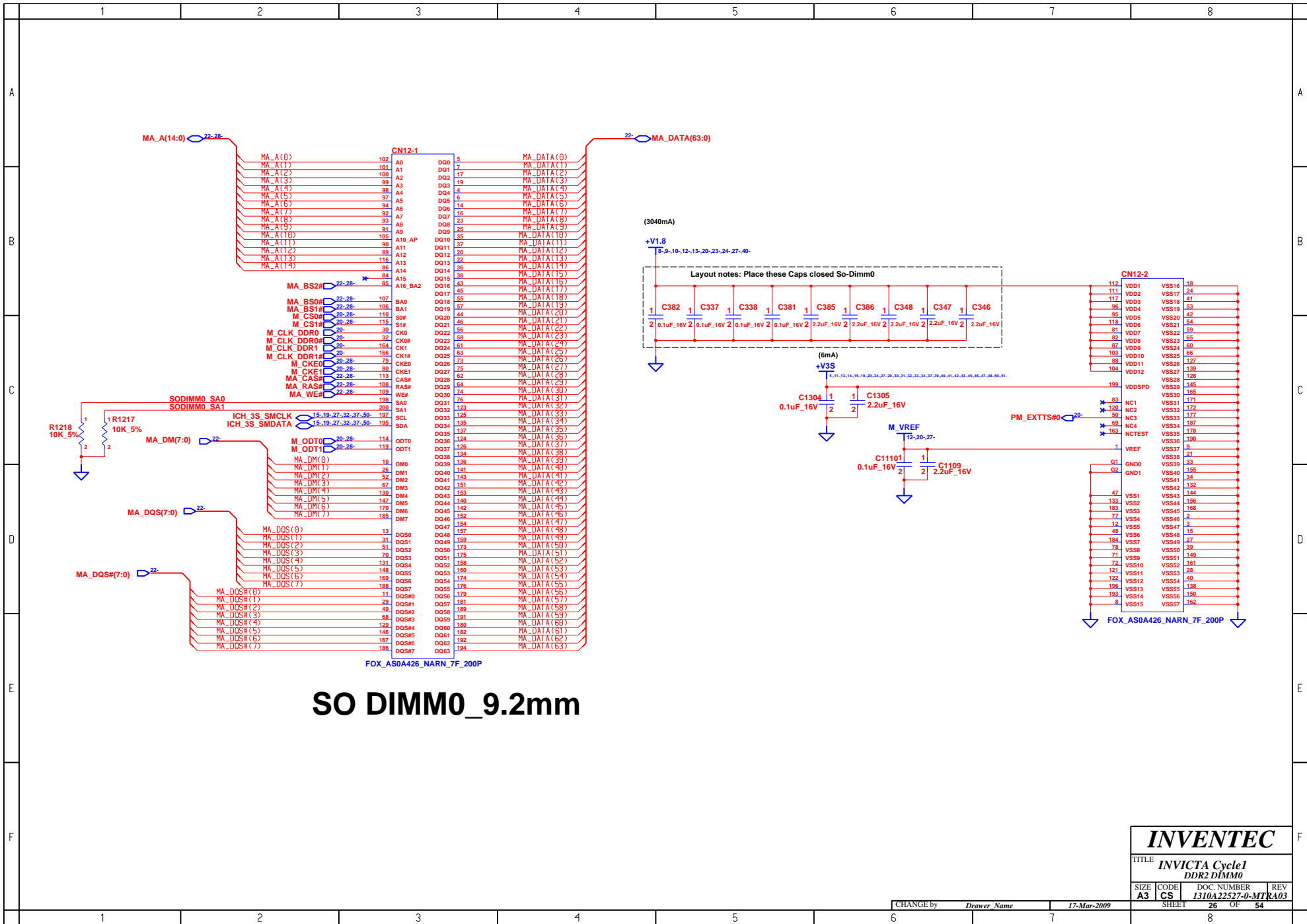


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TITLE INVICTA Cycle1 <i>N/B Cantiga-5</i>			
SIZE A3	CODE CS	DOC NUMBER 1310A22527-0-MTR	REV A03
CHANGE by <i>Drawer Name</i>		17-Mar-2009	
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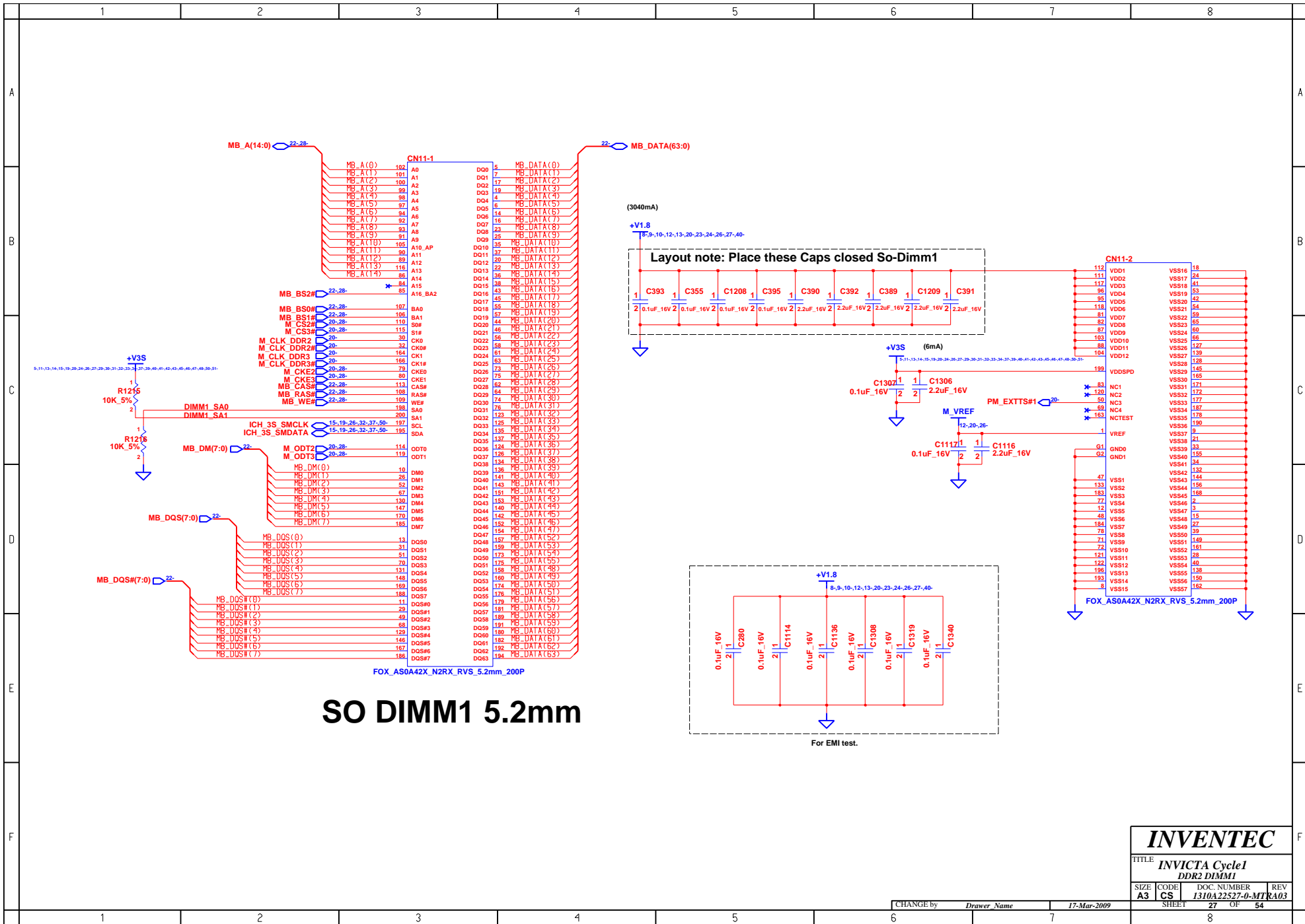
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TITLE INVICTA Cycle1 N/B Cantiga-6			
SIZE A3	CODE CS	DOC. NUMBER 1310A22527-0-MTR	REV A03
SHEET 25		OF 54	

CHANGE by *Drawer Name* 17-Mar-2009



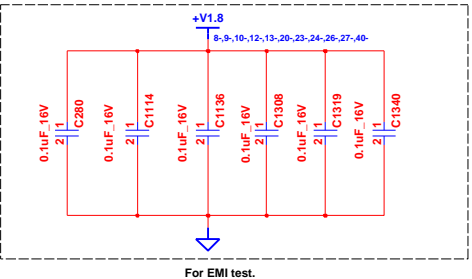
SO DIMM0_9.2mm

INVENTEC			
TITLE: INVICTA Cycle1 DDR2 DIMM0			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MIT	A03
CHANGE by		Drawer Name	17-Mar-2009
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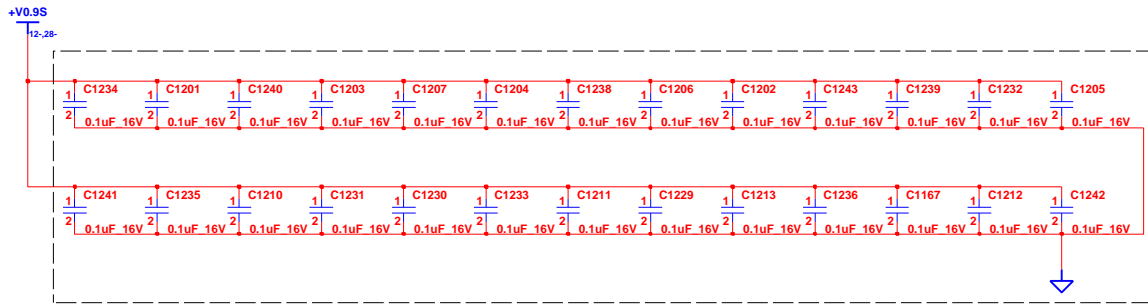


SO DIMM1 5.2mm

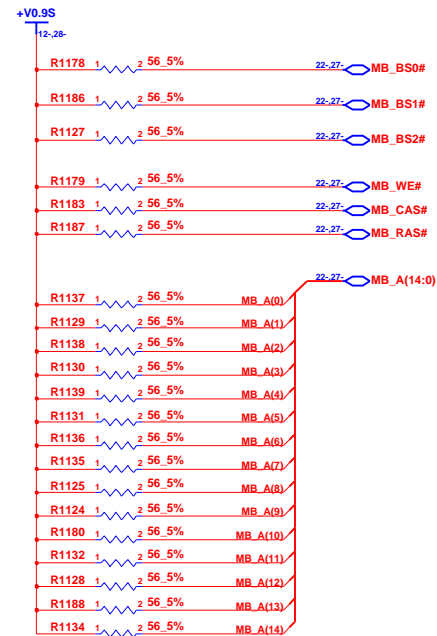
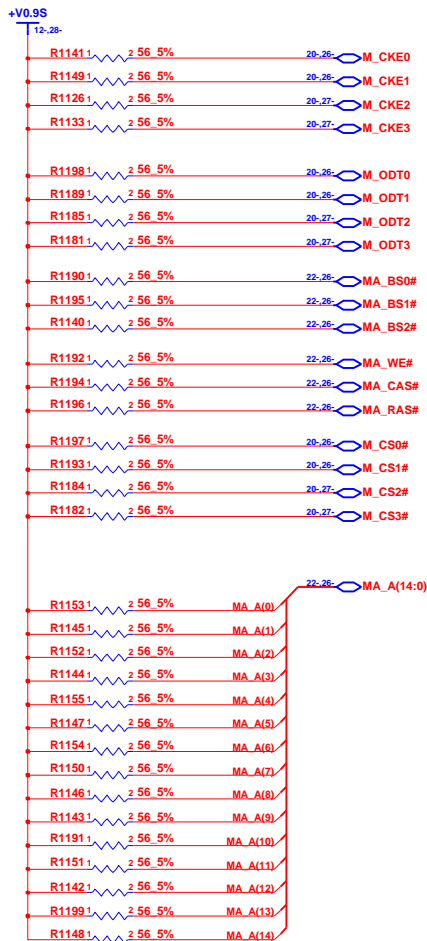
Layout note: Place these Caps closed So-Dimm1



INVENTEC			
TITLE INVICTA Cycle1 DDR2 DIMM1			
SIZE A3	CODE CS	DOC. NUMBER 1310A22527-0-MT	REV A03
CHANGE by <i>Drawer Name</i>		17-Mar-2009	
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Layout notes : Place one Cap close to every 2 pull up resistor terminated to +V0.9S.

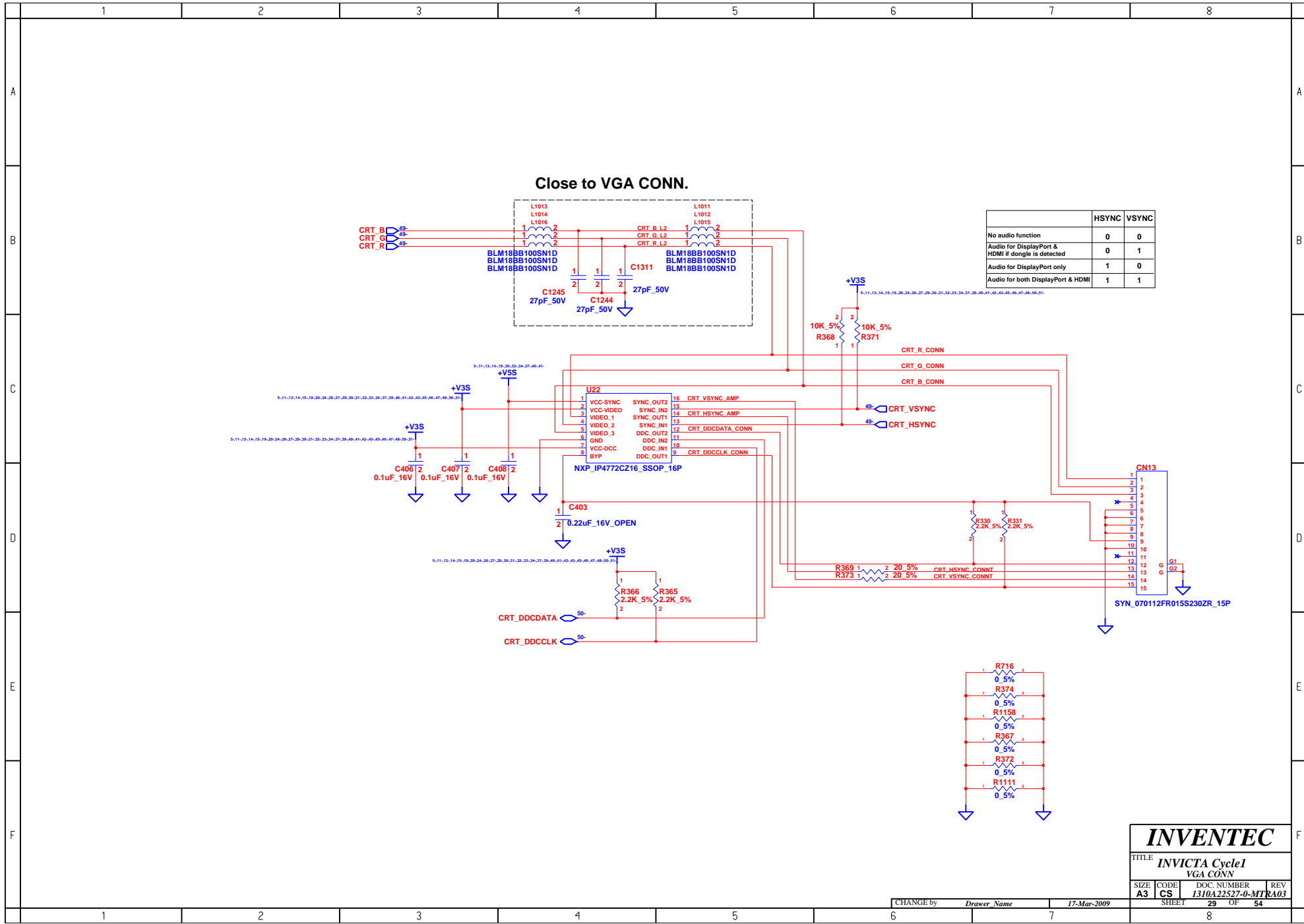


INVENTEC

TITLE
INVICTA Cycle1
DDR2 termination

SIZE A3	CODE CS	DOC. NUMBER I310A22527-0-MTR	REV A03
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CHANGE by *Drawer Name* 27-Sep-2003



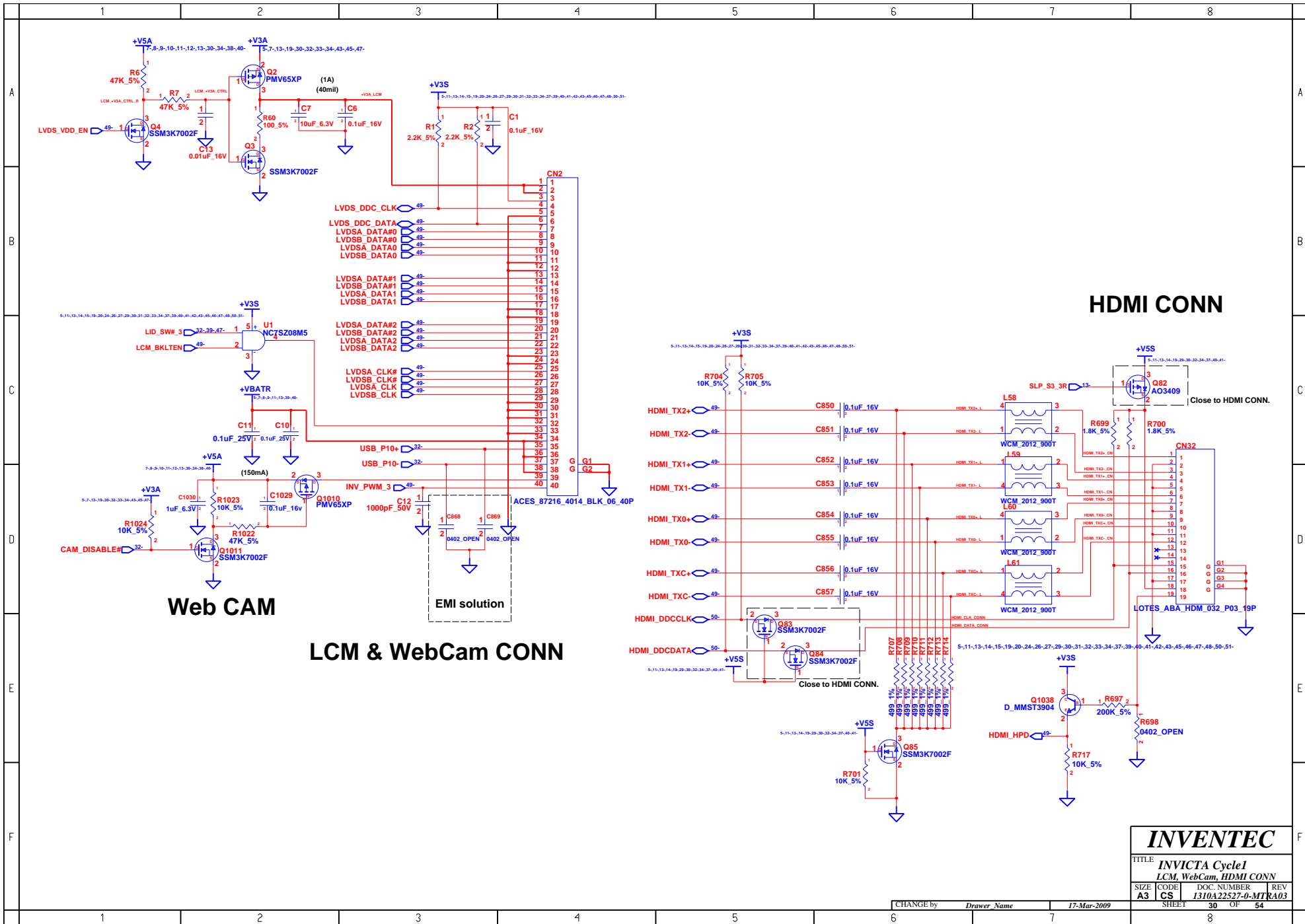
	HSYNC	VSYNC
No audio function	0	0
Audio for DisplayPort & HDMI if dongle is detected	0	1
Audio for DisplayPort only	1	0
Audio for both DisplayPort & HDMI	1	1

INVENTEC

TITLE: **INVICTA Cycle1
VGA CONN**

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTR	A03

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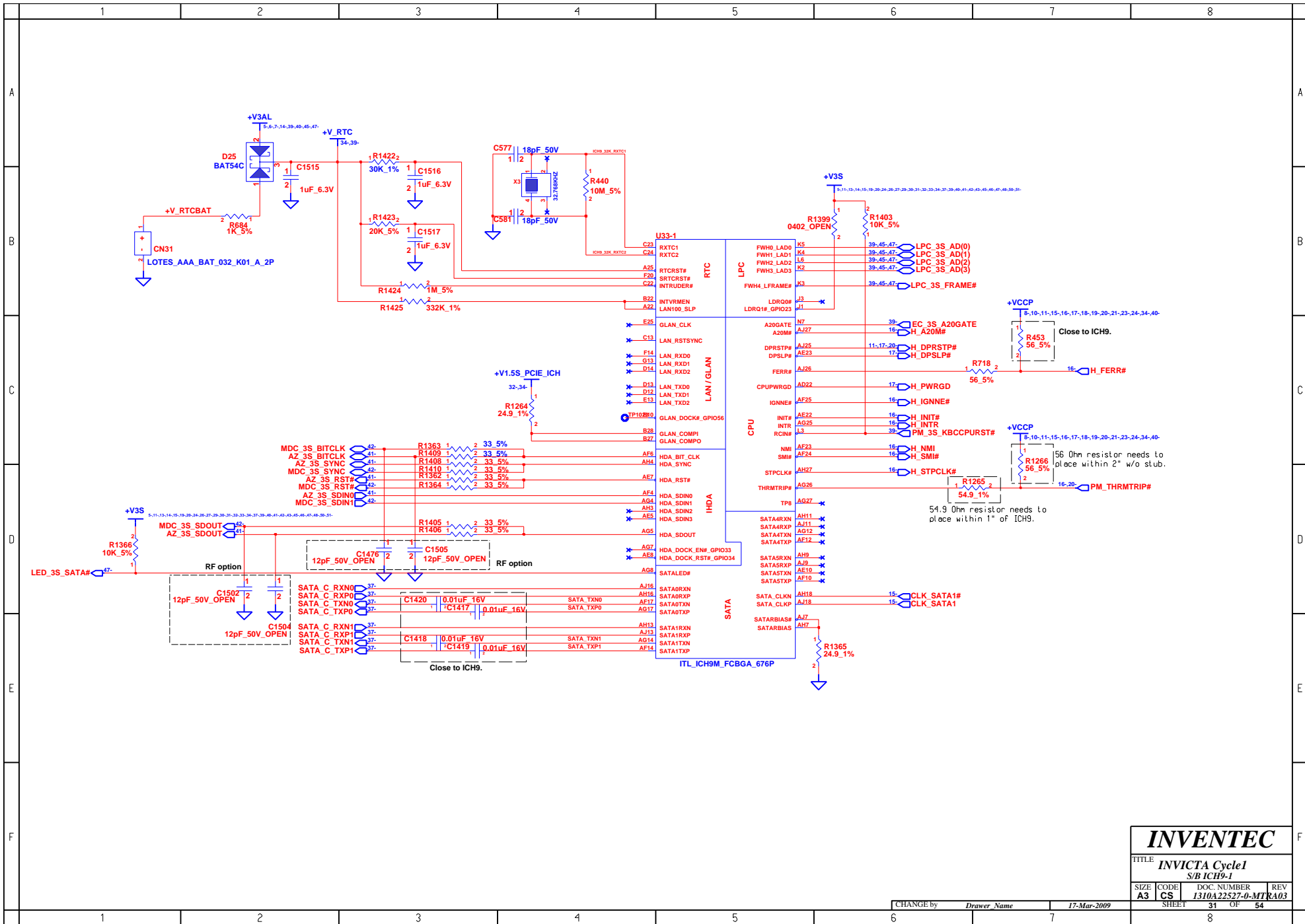


HDMI CONN

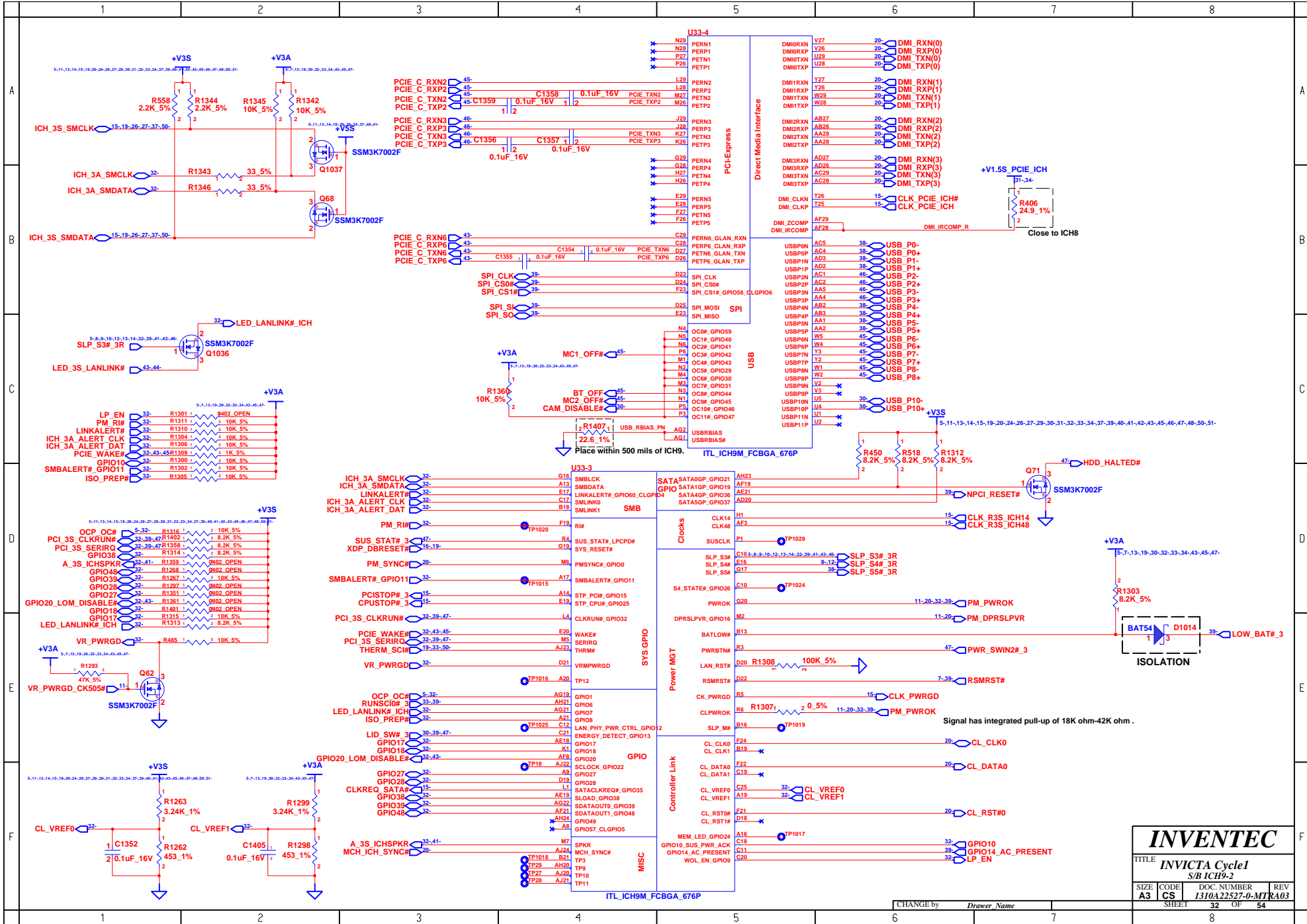
Web CAM

LCM & WebCam CONN

INVENTEC			
TITLE <i>INVICTA Cycle1</i>			
LCM, WebCam, HDMI CONN			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	I310A22527-0-MTR	A03
CHANGE by		Drawer Name	17-Mar-2009
SHEET		30	OF 54

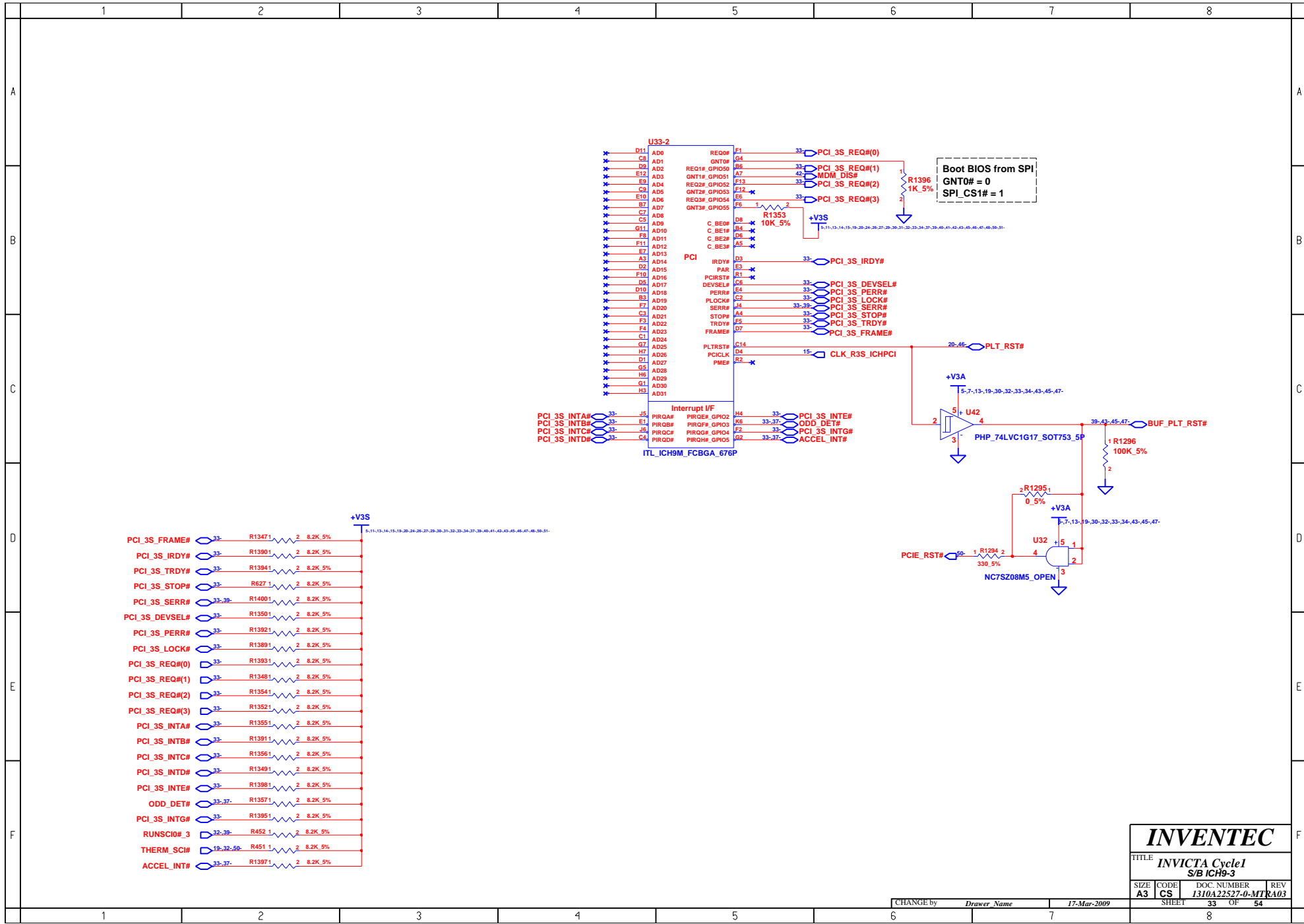


INVENTEC			
TITLE INVICTA Cycle1			
S/B ICH9-1			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MT	RA03
CHANGE by		Drawer Name	17-Mar-2009
		SHEET	31 OF 54



INVENTEC			
TITLE: INVICTA Cycle1 S/B ICH9-2			
SIZE: A3	CODE: CS	DOC. NUMBER: I310A22527-0-MTR	REV: R403
SHEET: 32		OF: 54	

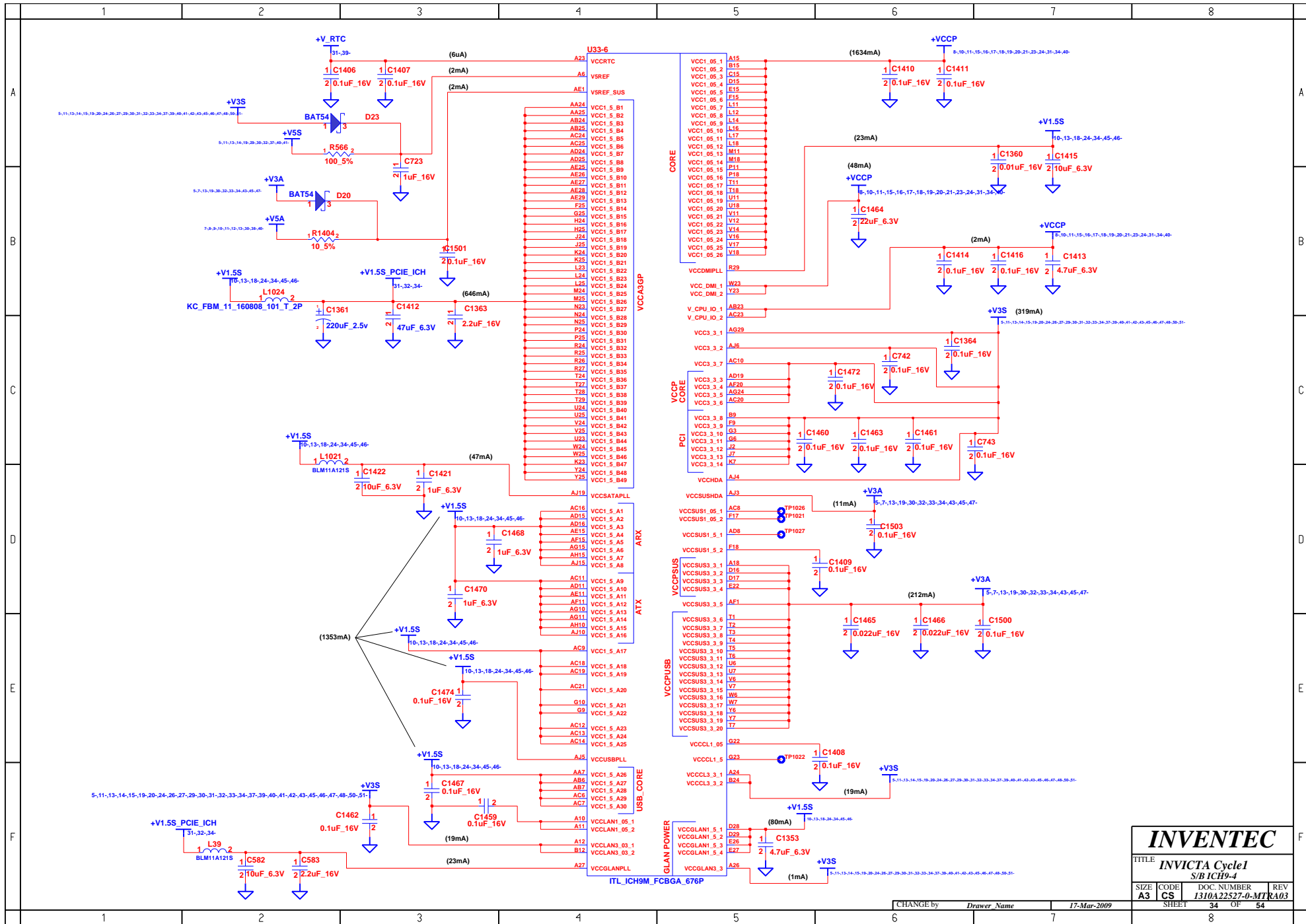
CHANGE by *Drawer Name* 8



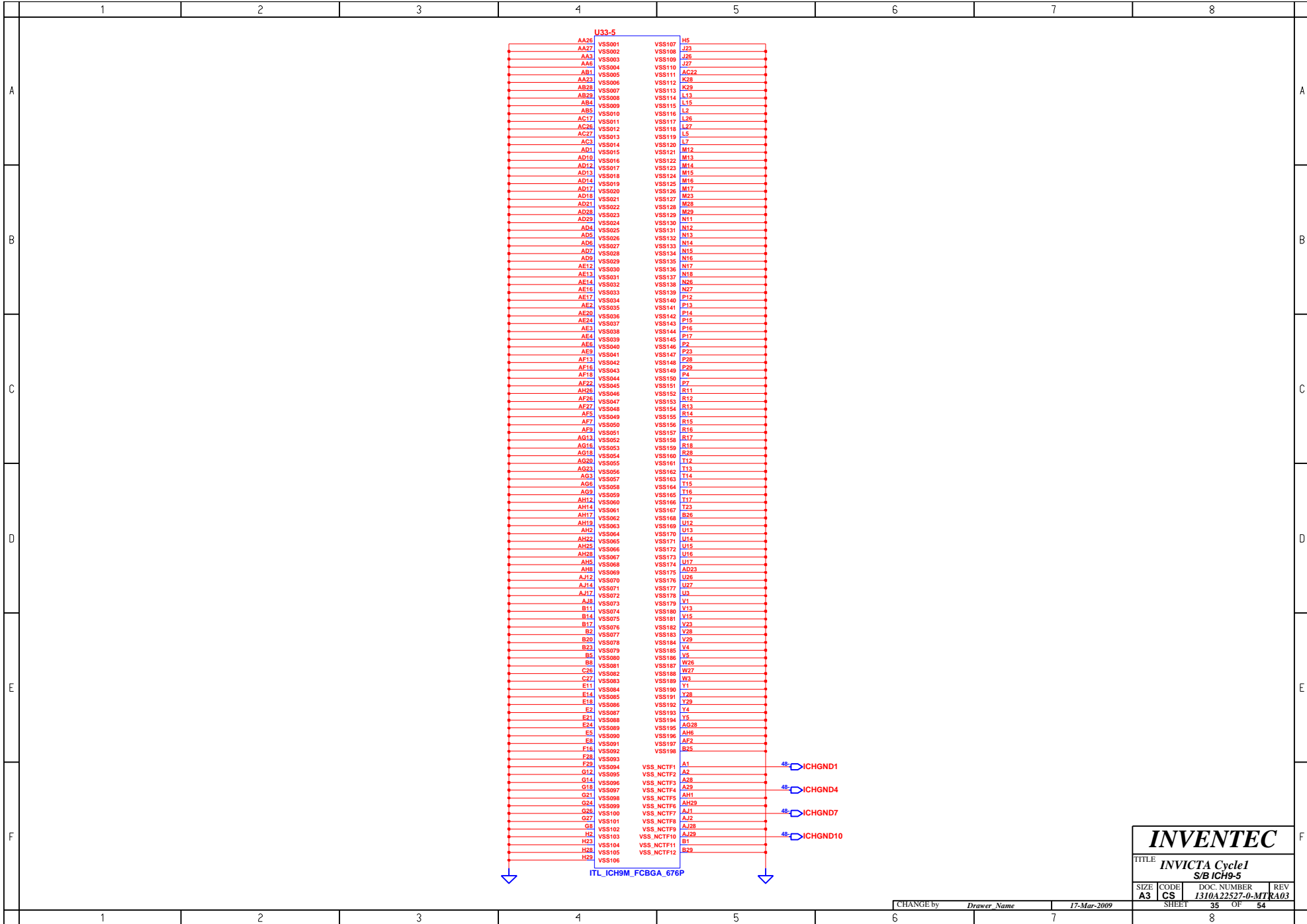
Boot BIOS from SPI
 GNT0# = 0
 SPI_CS1# = 1

- +V3S**
 5-11,13,14,15,19,20,24,26,27,29,30,31,32,33,34,37,39,40,41,42,43,45,46,47,48,50,51
- PCI_3S_FRAME# 33- R1347 2 8.2K 5%
 - PCI_3S_IRDY# 33- R1390 2 8.2K 5%
 - PCI_3S_TRDY# 33- R1394 2 8.2K 5%
 - PCI_3S_STOP# 33- R627 2 8.2K 5%
 - PCI_3S_SERR# 33-39- R1400 2 8.2K 5%
 - PCI_3S_DEVSEL# 33- R1350 2 8.2K 5%
 - PCI_3S_PERR# 33- R1392 2 8.2K 5%
 - PCI_3S_LOCK# 33- R1389 2 8.2K 5%
 - PCI_3S_REQ#(0) 33- R1393 2 8.2K 5%
 - PCI_3S_REQ#(1) 33- R1348 2 8.2K 5%
 - PCI_3S_REQ#(2) 33- R1354 2 8.2K 5%
 - PCI_3S_REQ#(3) 33- R1352 2 8.2K 5%
 - PCI_3S_INTA# 33- R1355 2 8.2K 5%
 - PCI_3S_INTB# 33- R1391 2 8.2K 5%
 - PCI_3S_INTC# 33- R1356 2 8.2K 5%
 - PCI_3S_INTD# 33- R1349 2 8.2K 5%
 - PCI_3S_INTE# 33- R1398 2 8.2K 5%
 - ODD_DET# 33-37- R1357 2 8.2K 5%
 - PCI_3S_INTG# 33- R1395 2 8.2K 5%
 - RUNSCIO#_3 32-39- R452 2 8.2K 5%
 - THERM_SCI# 19-32-50- R451 2 8.2K 5%
 - ACCEL_INT# 33-37- R1397 2 8.2K 5%

INVENTEC			
TITLE INVICTA Cycle1 S/B ICH9-3			
SIZE A3	CODE CS	DOC NUMBER I310A22527-0-MT	REV RA03
CHANGE by Drawer Name		17-Mar-2009	
SHEET 33		OF 54	



INVENTEC			
TITLE INVICTA Cycle1 S/B ICH9-4			
SIZE A3	CODE CS	DOC. NUMBER I310A22527-0-MTR	REV A03
CHANGE by <i>Drawer Name</i>		17-Mar-2009	
SHEET 34		OF 54	



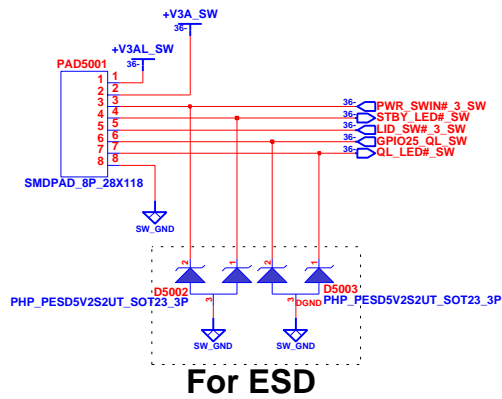
INVENTEC

TITLE *INVICTA Cycle 1*
S/B ICH9-5

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTR	A03

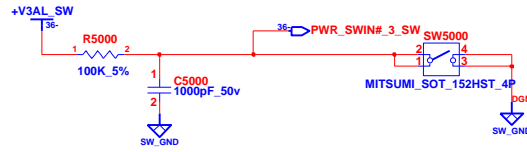
CHANGE by *Drawer Name* 17-Mar-2009 SHEET 35 OF 54

PWR SW B/B CONN

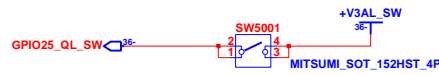


For ESD

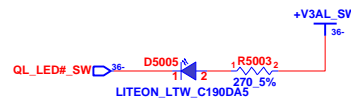
Power Button



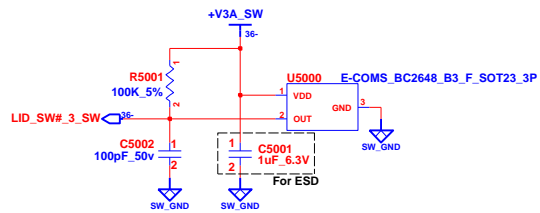
Quick Look Button



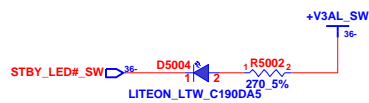
Quick Look LED



LID Switch



Power / Standby LED

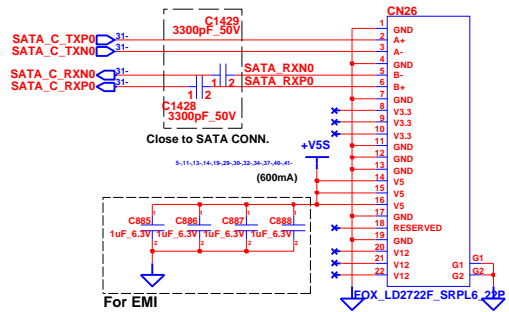


- FIX5000
- FIX_MASK
- FIX5001
- FIX_MASK
- FIX5002
- FIX_MASK
- FIX5003
- FIX_MASK
- FIX5004
- FIX_MASK
- FIX5005
- FIX_MASK

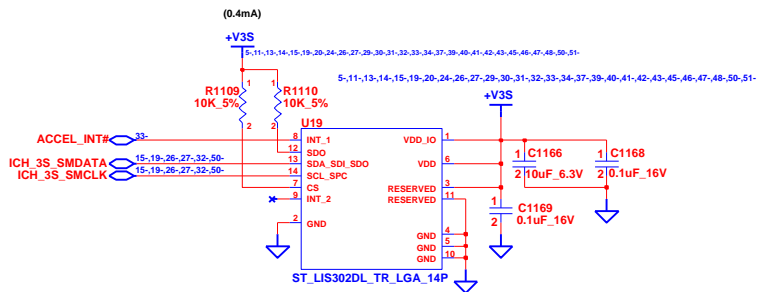
Power & LID Switch Board

INVENTEC

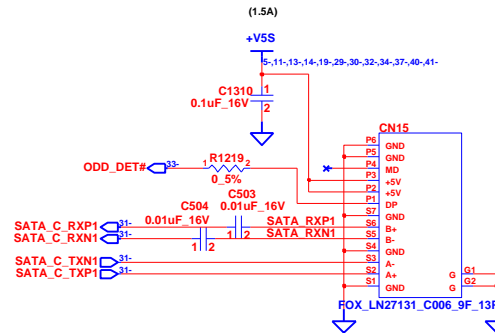
TITLE INVICTA Cycle1			
PWR, LID, APP SW/Bs			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310A22527-0-MTR	A03
CHANGE by		Drawer Name	17-Mar-2009
SHEET		36	OF 54



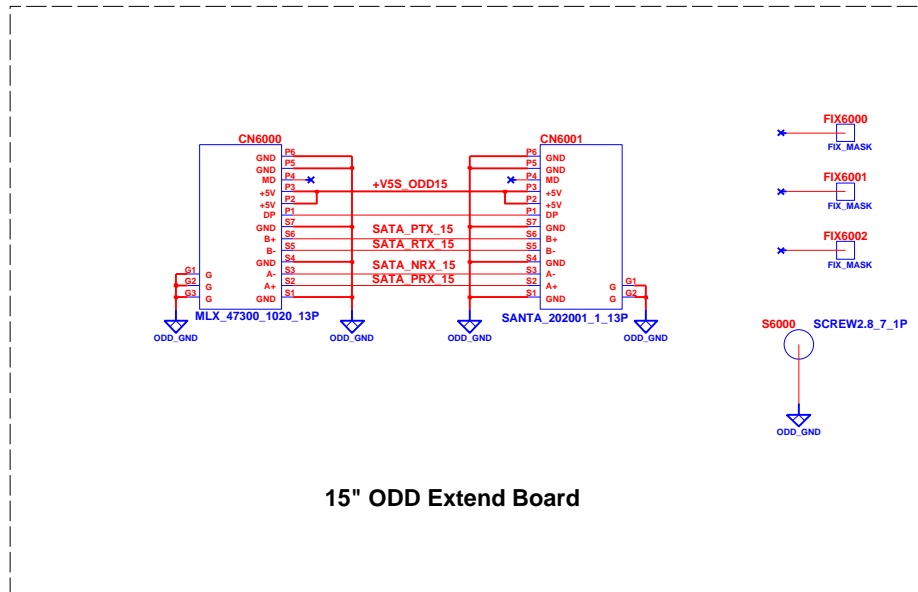
SATA HDD



Accelerometer



SATA ODD



15" ODD Extend Board

INVENTEC

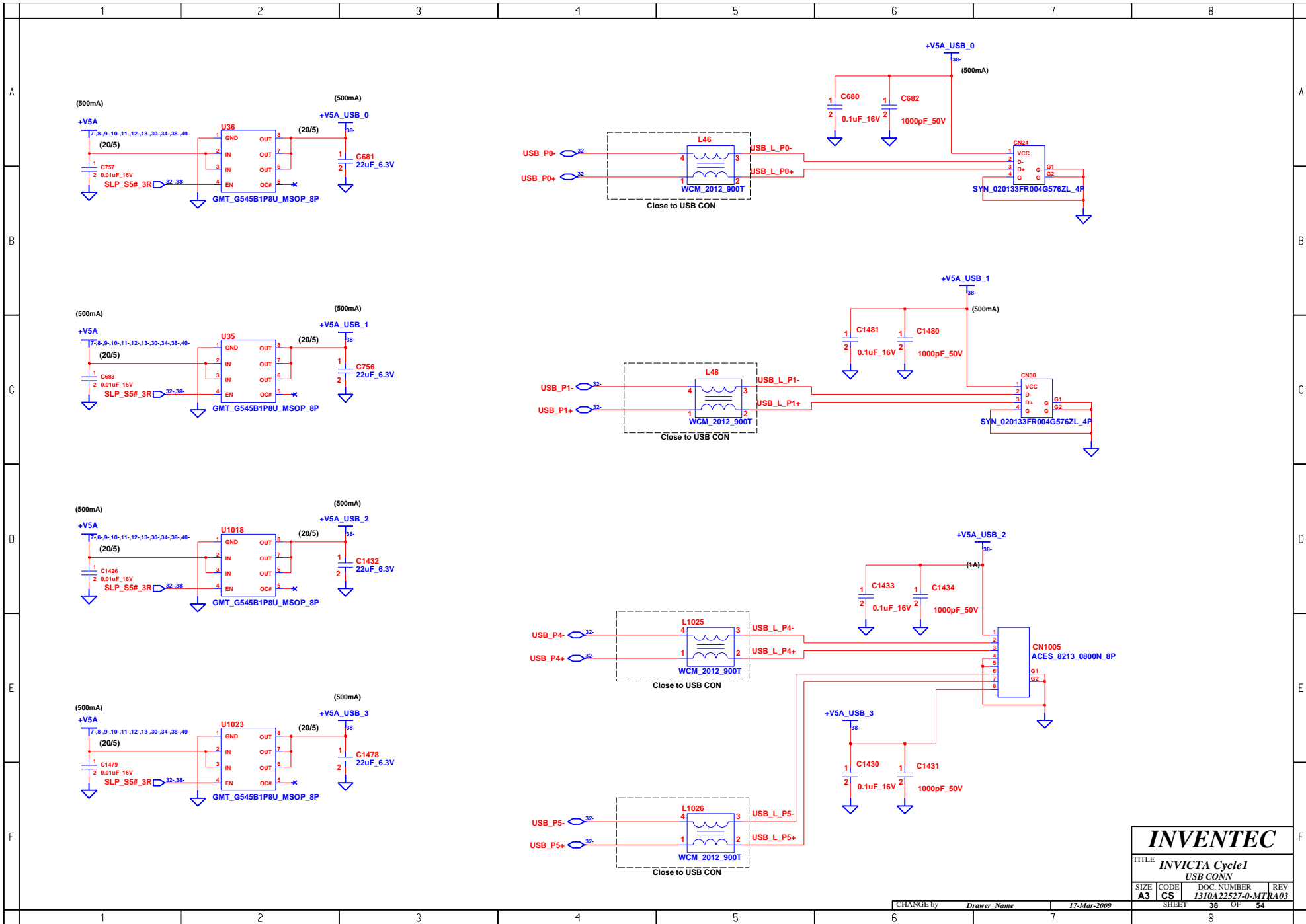
TITLE **INVICTA Cycle1**

HDD & ODD CONN & Accelerometer & 15" ODD EXT B

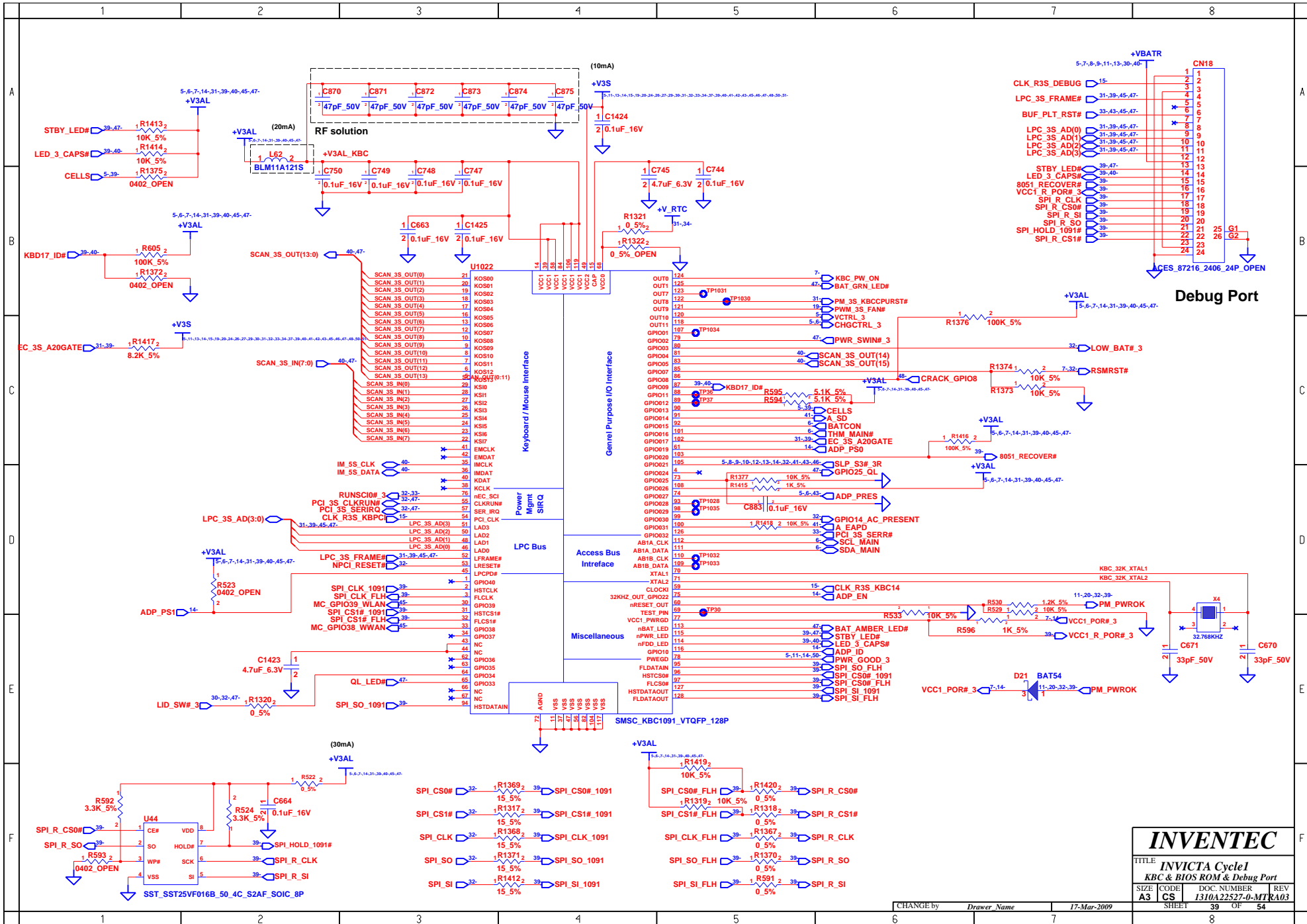
SIZE **A3** CODE **CS** DOC NUMBER **1310A22527-0-MTR** REV **A03**

SHEET **37** OF **54**

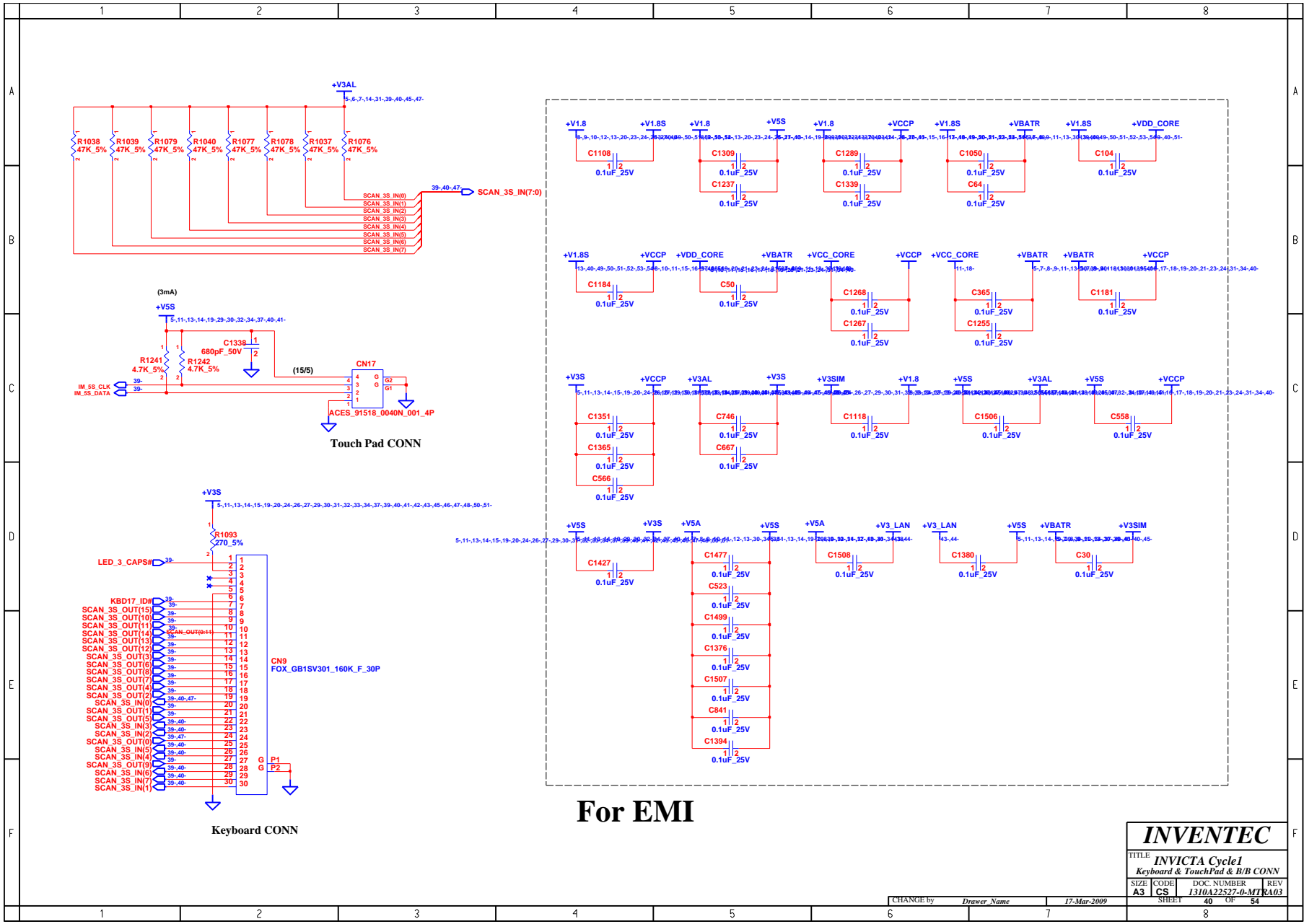
CHANGE by *Drawer Name* 17-Mar-2009



INVENTEC			
TITLE <i>INVICTA Cycle1</i> USB CONN			
SIZE A3	CODE CS	DOC NUMBER <i>1310A22527-0-MTR</i>	REV A03
CHANGE by <i>Drawer Name</i>		17-Mar-2009	
SHEET 38		OF 54	



INVENTEC			
TITLE: <i>INVICTA Cycle1</i>			
KBC & BIOS ROM & Debug Port			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310A22527-0-MTR	A03
CHANGE by		Drawer Name	17-Mar-2009
SHEET		39	OF 54



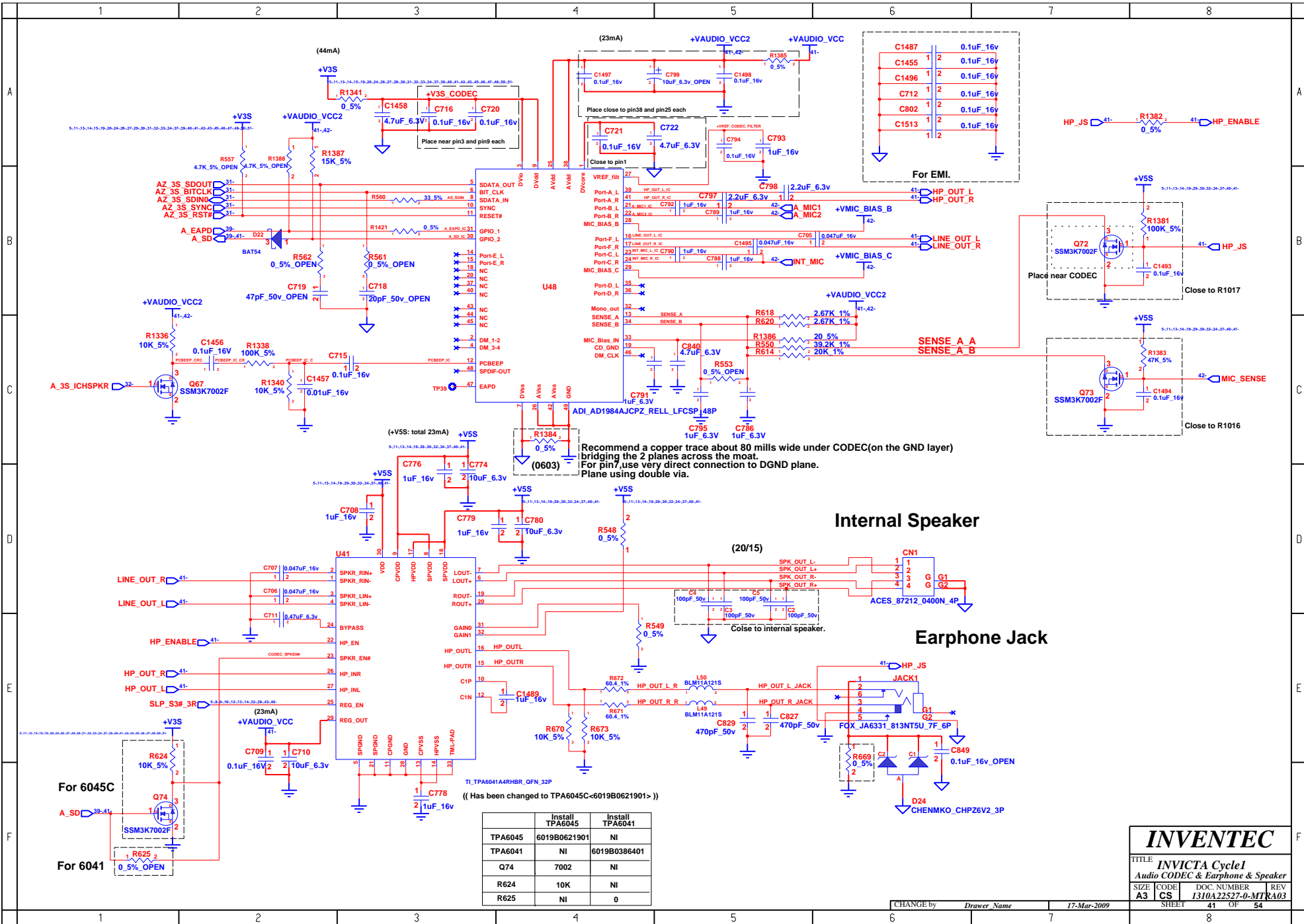
For EMI

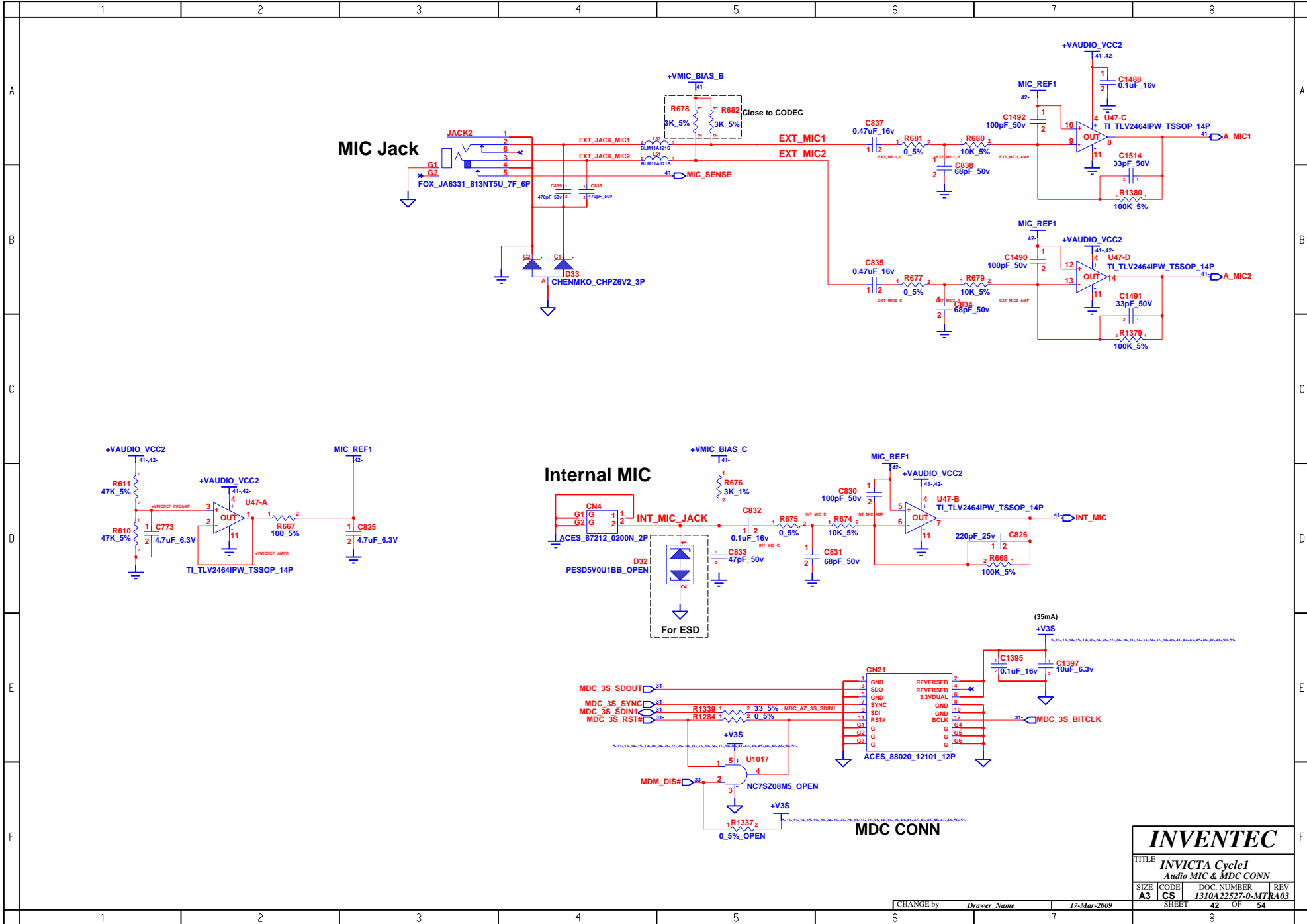
INVENTEC

TITLE: **INVICTA Cycle1**
Keyboard & TouchPad & B/B CONN

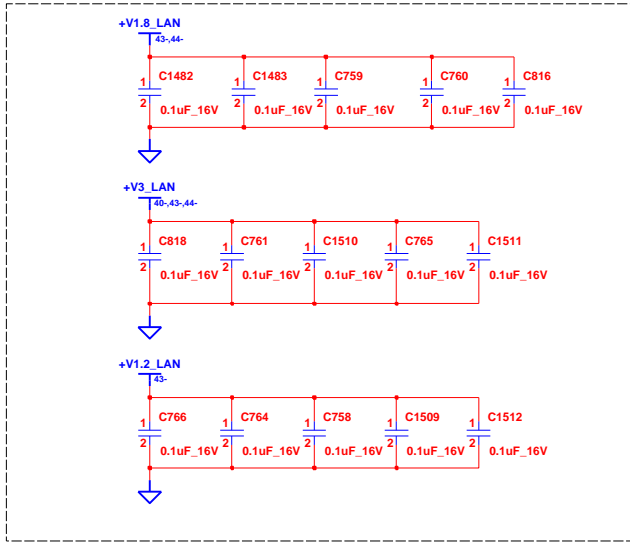
SIZE	CODE	DOC NUMBER	REV
A3	CS	I310A22527-0-MTKA03	

CHANGE by: *Drawer Name* 17-Mar-2009 SHEET 40 OF 54

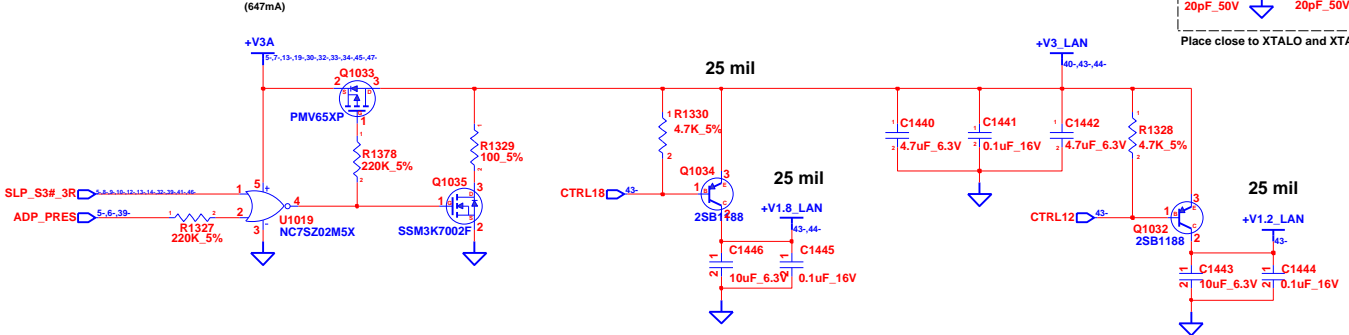
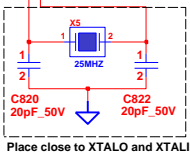
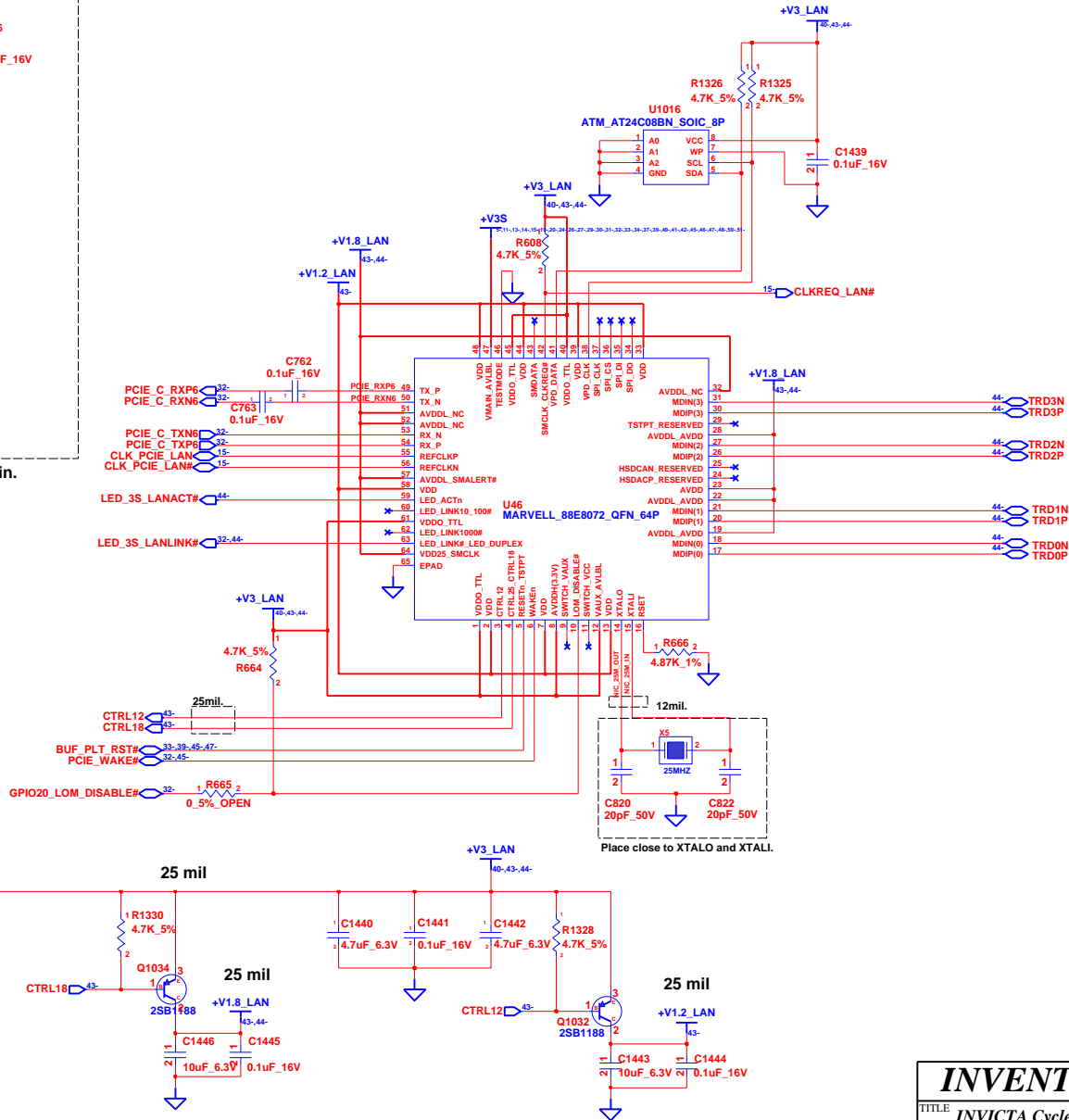




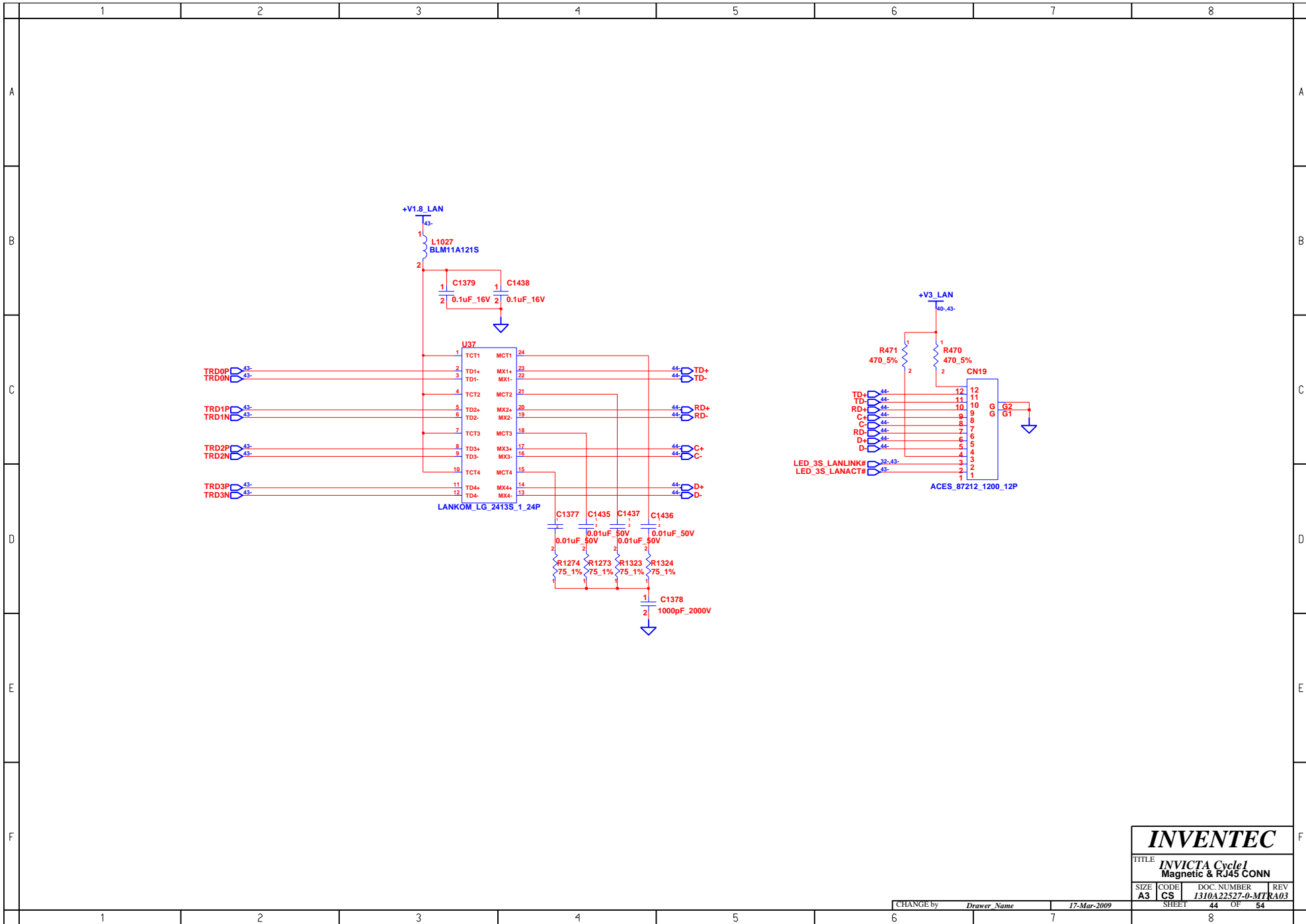
INVENTEC			
TITLE INVICTA Cycle1			
Audio MIC & MDC CONN			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTR	A03
CHANGE by		Drawer Name	17-Mar-2009
SHEET		42	OF 54



Place bypass cap as close as possible with every power pin.



INVENTEC			
TITLE: INVICTA Cycle1			
Giga LAN Controller			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22527-0-MTR	A03
CHANGE by		Drawer Name	17-Mar-2009
SHEET		43	OF 54



INVENTEC

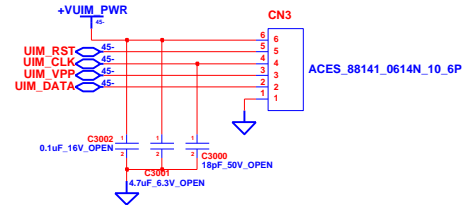
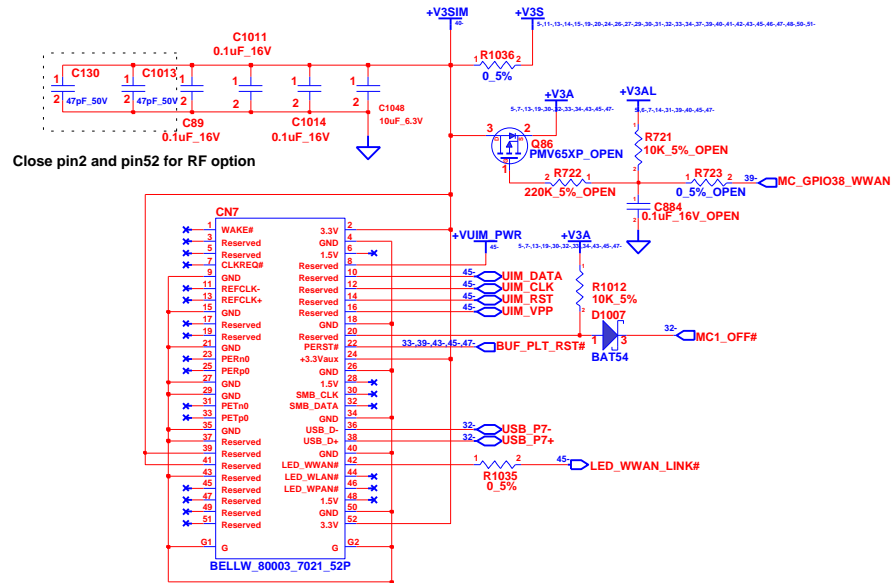
TITLE **INVICTA Cycle1
Magnetic & RJ45 CONN**

SIZE A3	CODE CS	DOC. NUMBER 1310A22527-0-MTR	REV A03
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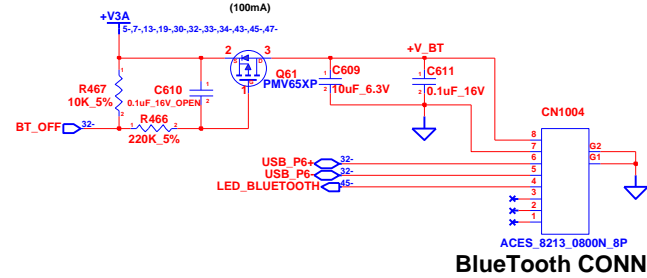
CHANGE by *Drawer Name* 17-Mar-2009

SHEET 44 OF 54

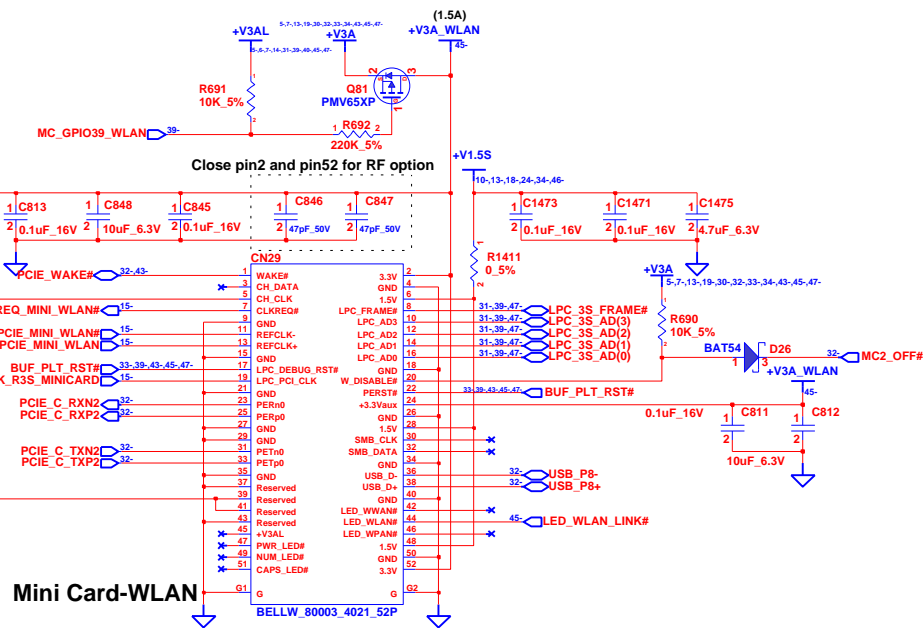
MINI Card-WWAN



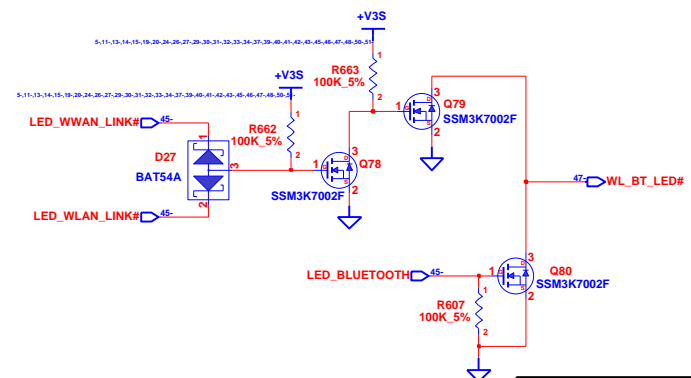
SIM Card B2B MB side CONN



BlueTooth CONN



Mini Card-WLAN



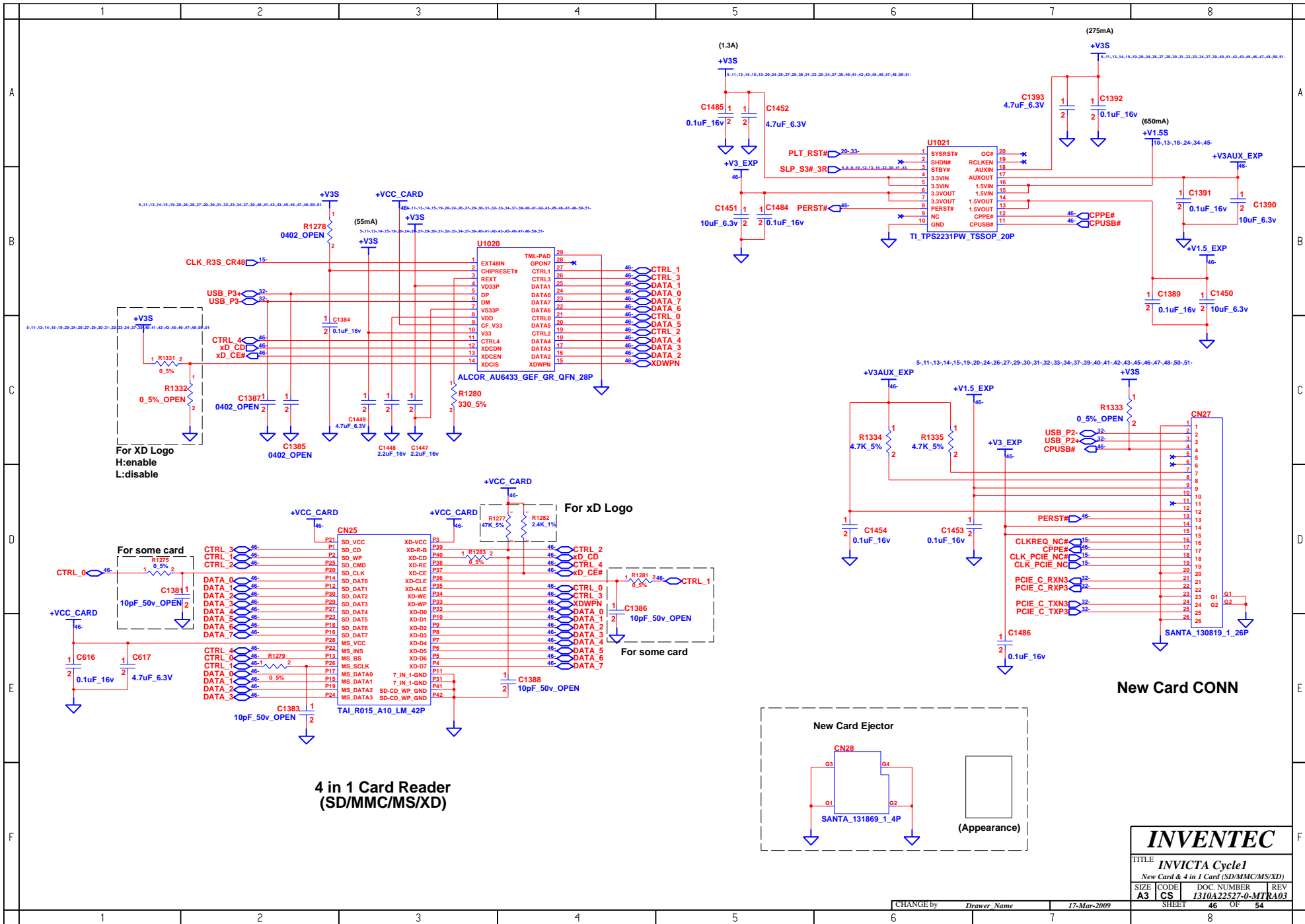
INVENTEC

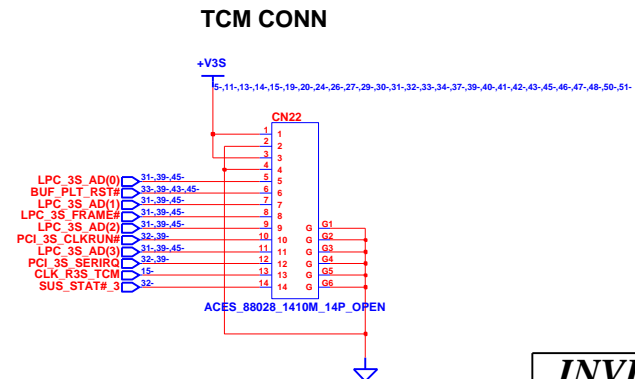
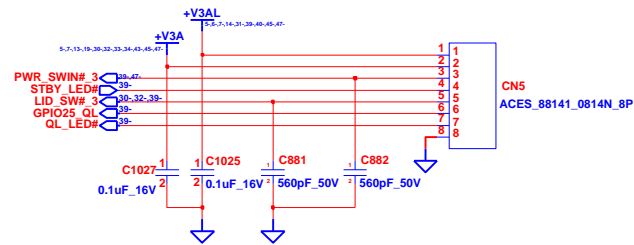
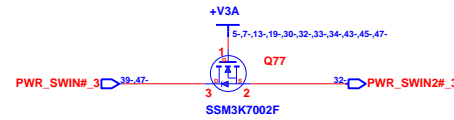
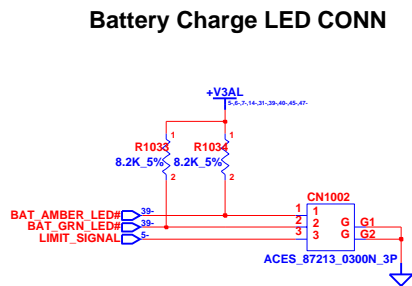
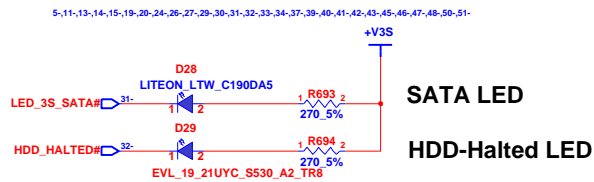
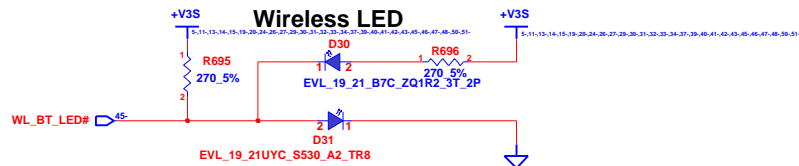
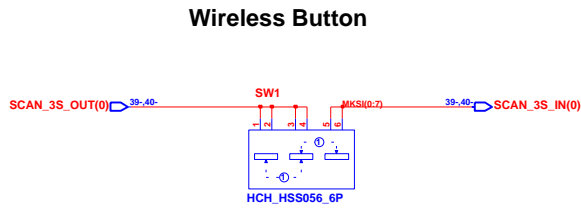
TITLE: **INVICTA Cycle1**
Mini Card (WLAN/WWAN) / BT

SIZE CODE DOC NUMBER REV
A3 CS 1310A22527-0-MTR A03

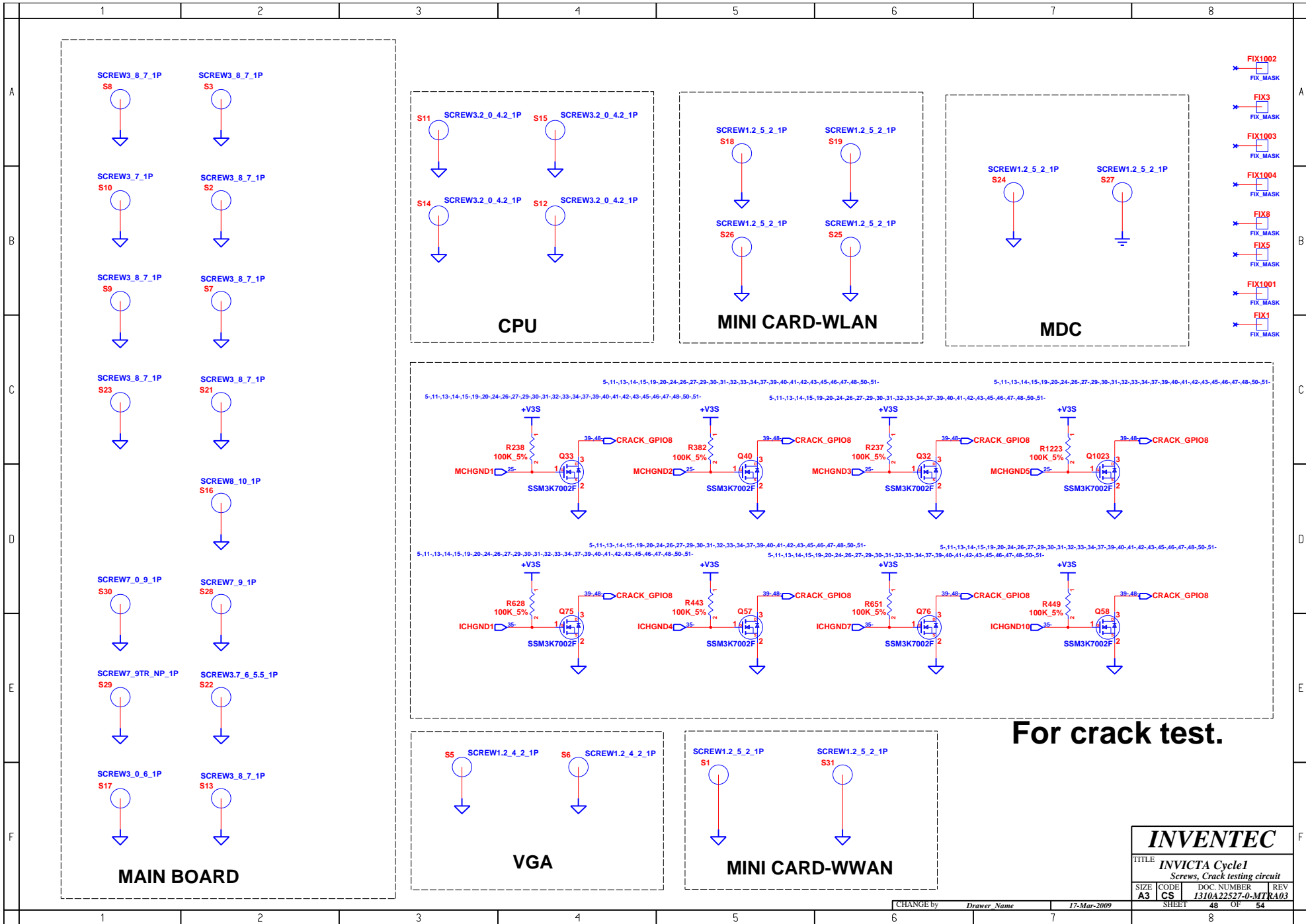
CHANGE by *Drawer Name* 17-Mar-2009

SHEET 45 OF 54





INVENTEC			
TITLE: INVICTA Cycle1			
LEDs & TCM CONN			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310A22527-0-MTR	A03
CHANGE by		Drawer Name	17-Mar-2009
SHEET		47	OF 54



For crack test.

INVENTEC			
TITLE: <i>INVICTA Cycle1</i>			
Screws, Crack testing circuit			
SIZE A3	CODE CS	DOC NUMBER 1310A22527-0-MTR	REV A03
CHANGE by Drawer Name		17-Mar-2009	
SHEET		48 OF 54	

STRAPS	PIN	Description of default settings	
TX_PWRS_ENB	GPIO0	PCIE full TX output swing.	1
TX_DEEMPH_EN	GPIO1	PCIE transmitter de-emphasis enabled.	1
BIF_DEBUG_ACCESS	GPIO4	Debug signals muxed out.	0
ROMIDCFG(0:3)	GPIO[11:13,9]	Memory aperture type	X X X X

X = DESIGN DEPENDANT
0 = DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR

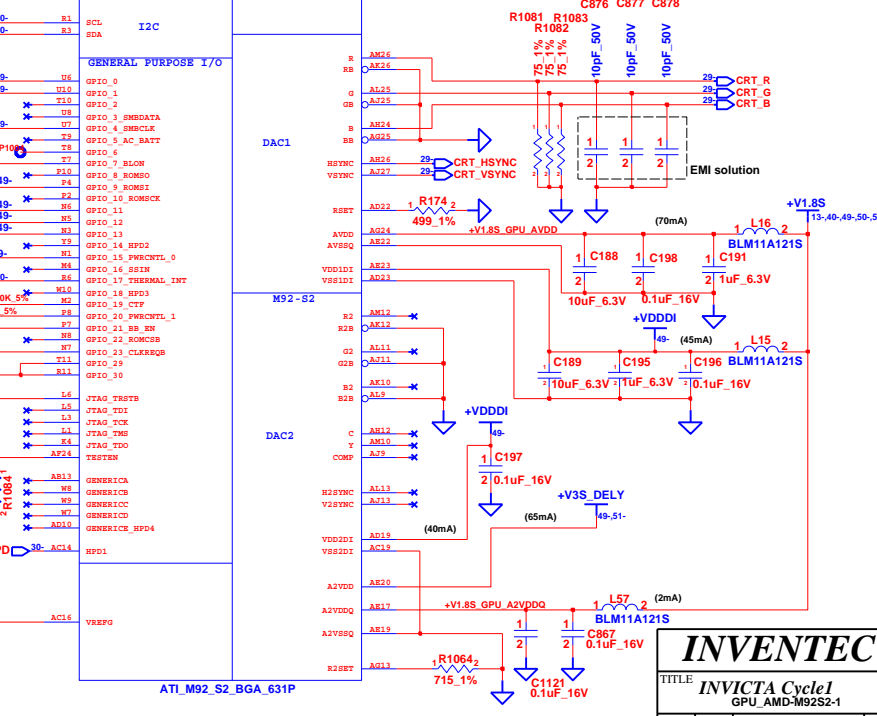
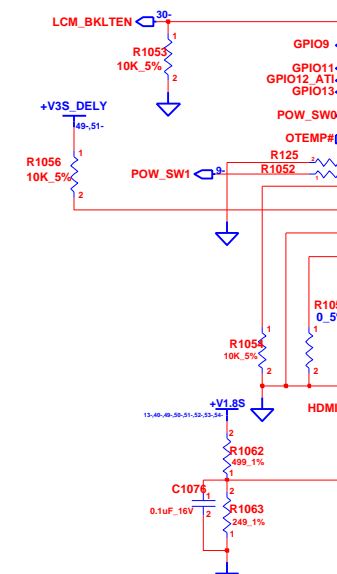
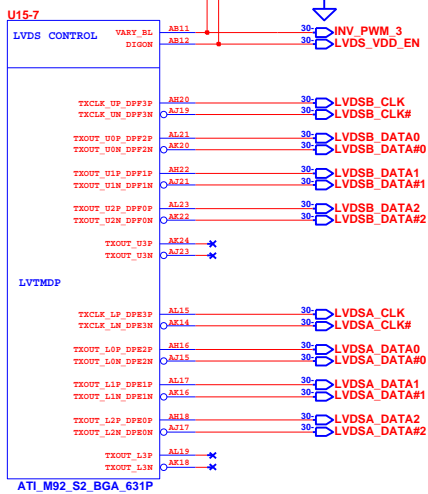
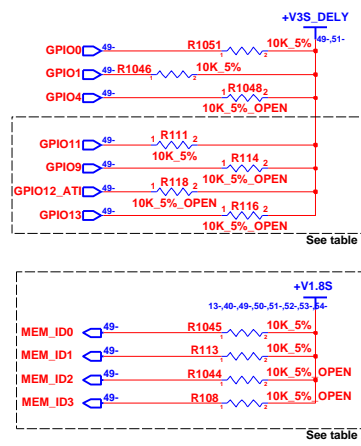
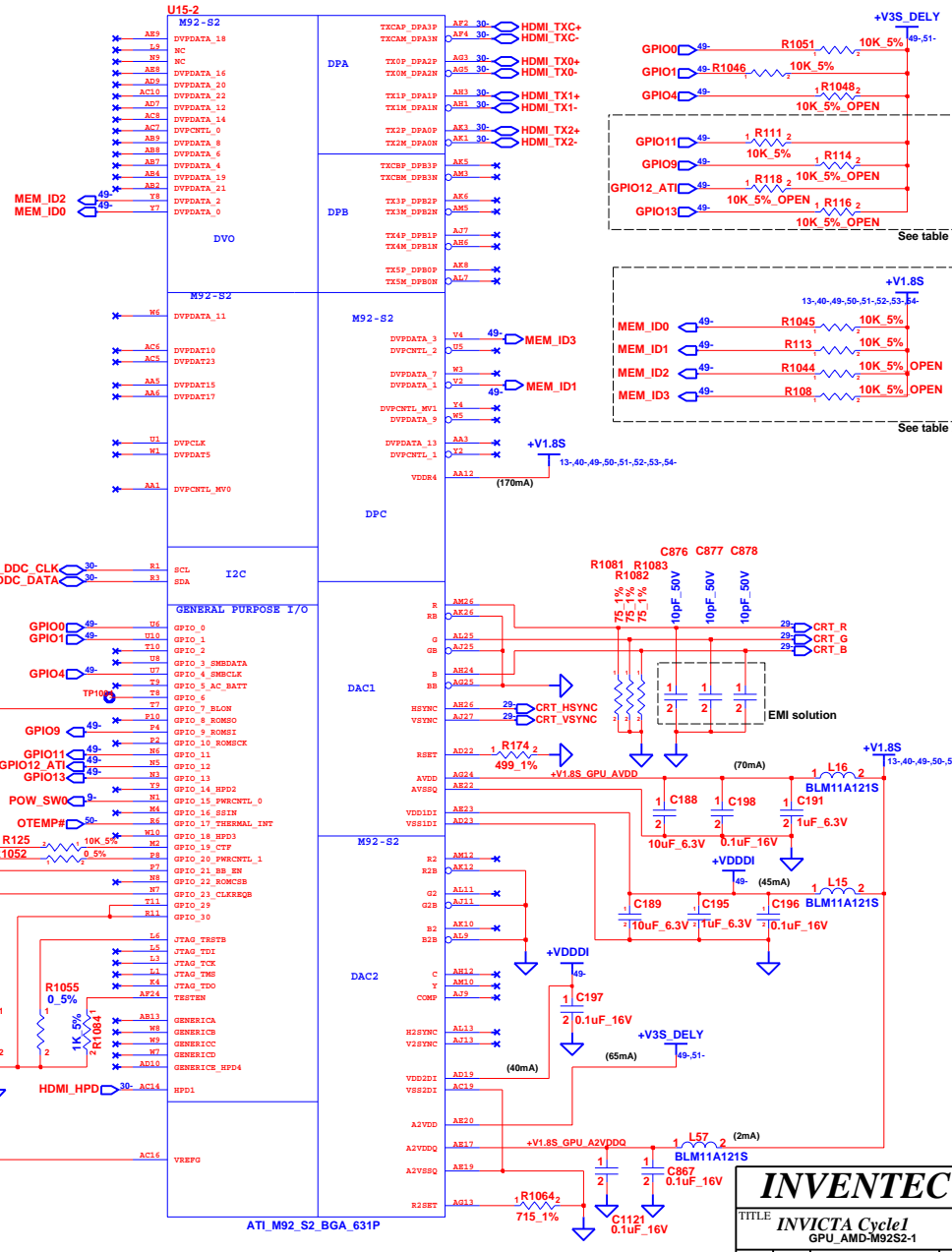
Table 1

GPIO_13	GPIO_12	GPIO_11	For DIS-GDDR2
0	0	1	512MB/256MB memory aperture (Default)
1	1	0	reserved

POW_SW1	POW_SW0	+VDD_CORE
0	0	1.0V
0	1	0.95V
1	0	0.9V

Table 2

For DIS-VRAM DDR2				
MEM_ID3	MEM_ID2	MEM_ID1	MEM_ID0	vendor
0	0	0	1	Samsung (512MB)
0	0	1	0	Qimonda (512MB)
0	0	1	1	Hynix (512MB) (Default)

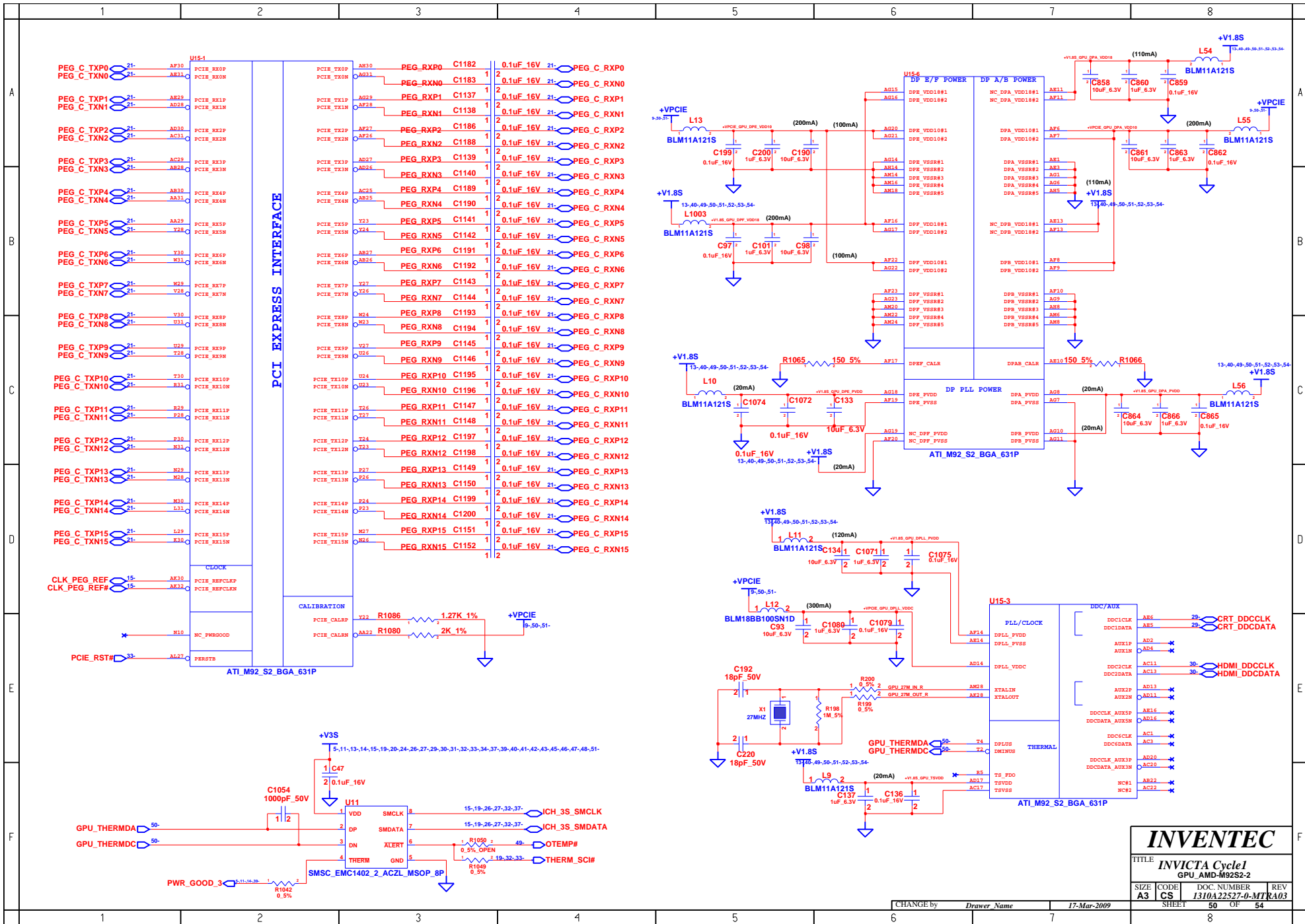


INVENTEC

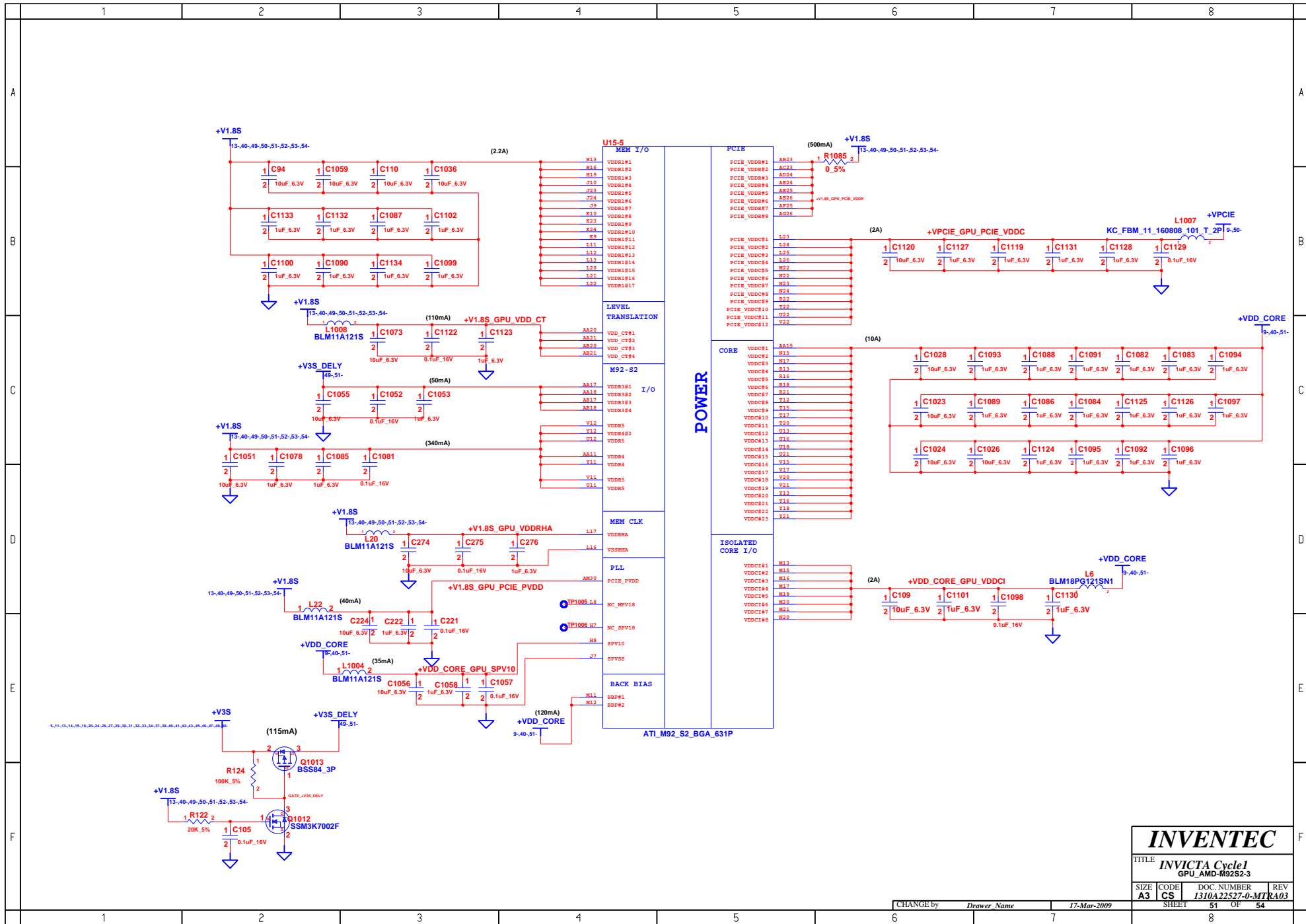
TITLE: INVICTA Cycle1 GPU_AMD-M92S2-1

SIZE	CODE	DOC. NUMBER	REV
A3	CS	I310A22527-0-MTR	A03

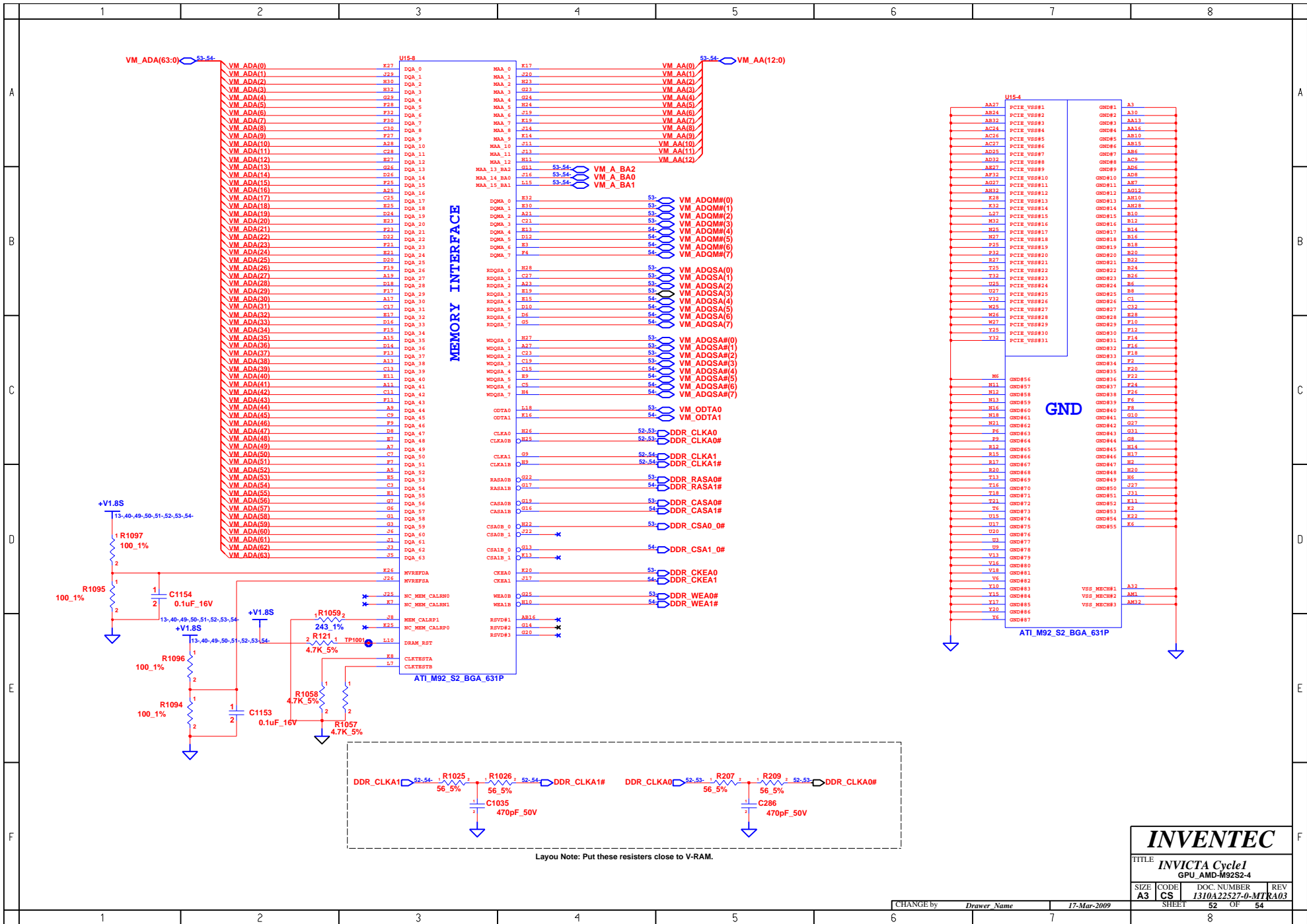
SHEET 49 OF 54



INVENTEC			
TITLE INVICTA Cycle1 GPU_AMD-M92S2-2			
SIZE A3	CODE CS	DOC NUMBER I310A22527-0-MTR	REV A03
CHANGE by <i>Drawer Name</i>		17-Mar-2009	
SHEET 50		OF 54	



INVENTEC			
TITLE: INVICTA Cycle1 GPU_AMD-M92S2-3			
SIZE: A3	CODE: CS	DOC. NUMBER: I310A22527-0-MTR	REV: A03
CHANGE by: Drawer Name		17-Mar-2009	
SHEET: 51		OF: 54	



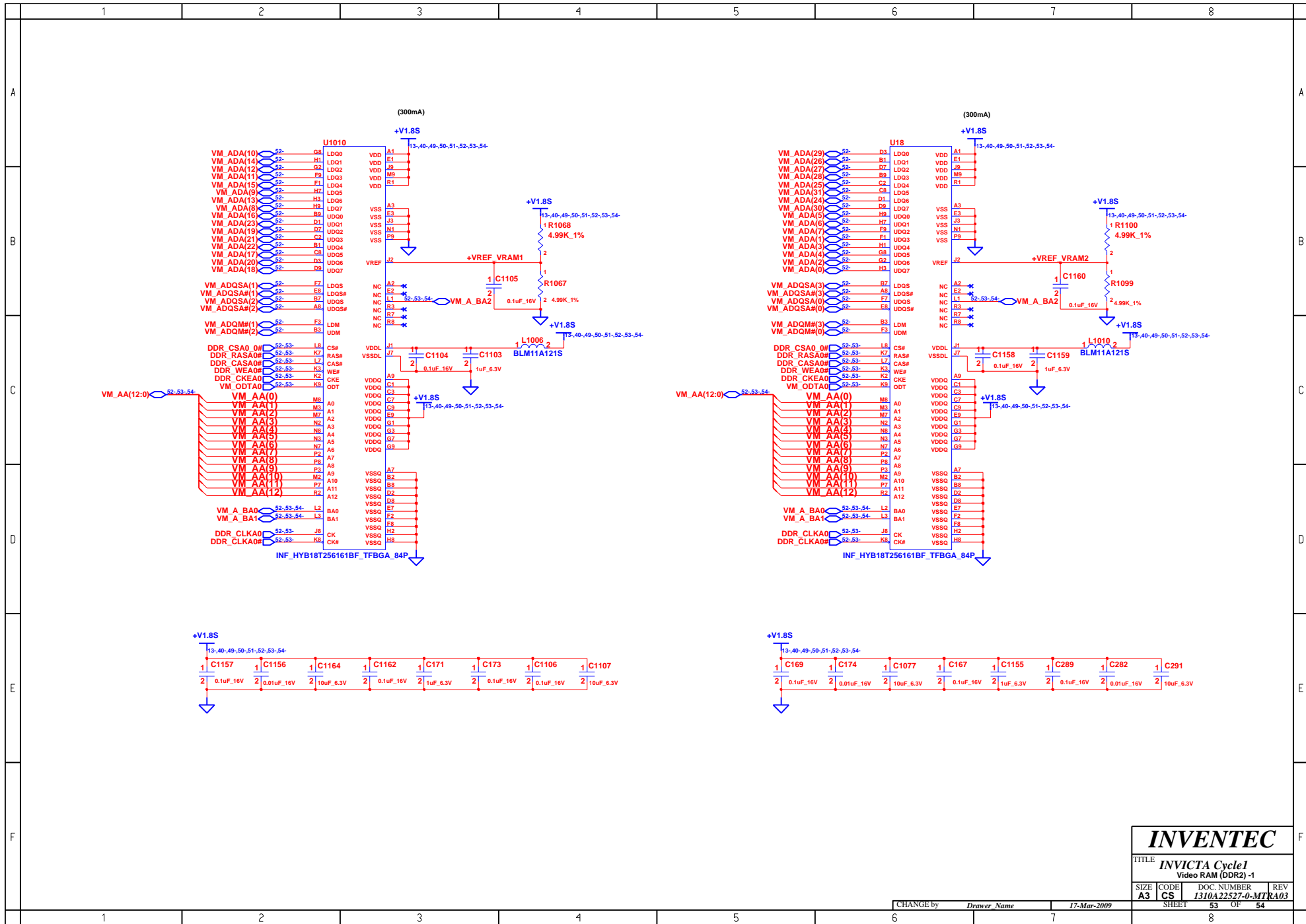
GND

ATI_M92_S2_BGA_631P

MEMORY INTERFACE

Layout Note: Put these resistors close to V-RAM.

INVENTEC	
TITLE: INVICTA Cycle1 GPU_AMD-M92S2-4	
SIZE: A3	CODE: CS
DOC NUMBER: 1310A22527-0-MTR	
REV: A03	
SHEET: 52 OF 54	



INVENTEC

TITLE: INVICTA Cycle1
Video RAM (DDR2) -1

SIZE	CODE	DOC. NUMBER	REV
A3	CS	I310A22527-0-MTR	A03

CHANGE by	Drawer Name	17-Mar-2009	SHEET	53	OF	54
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