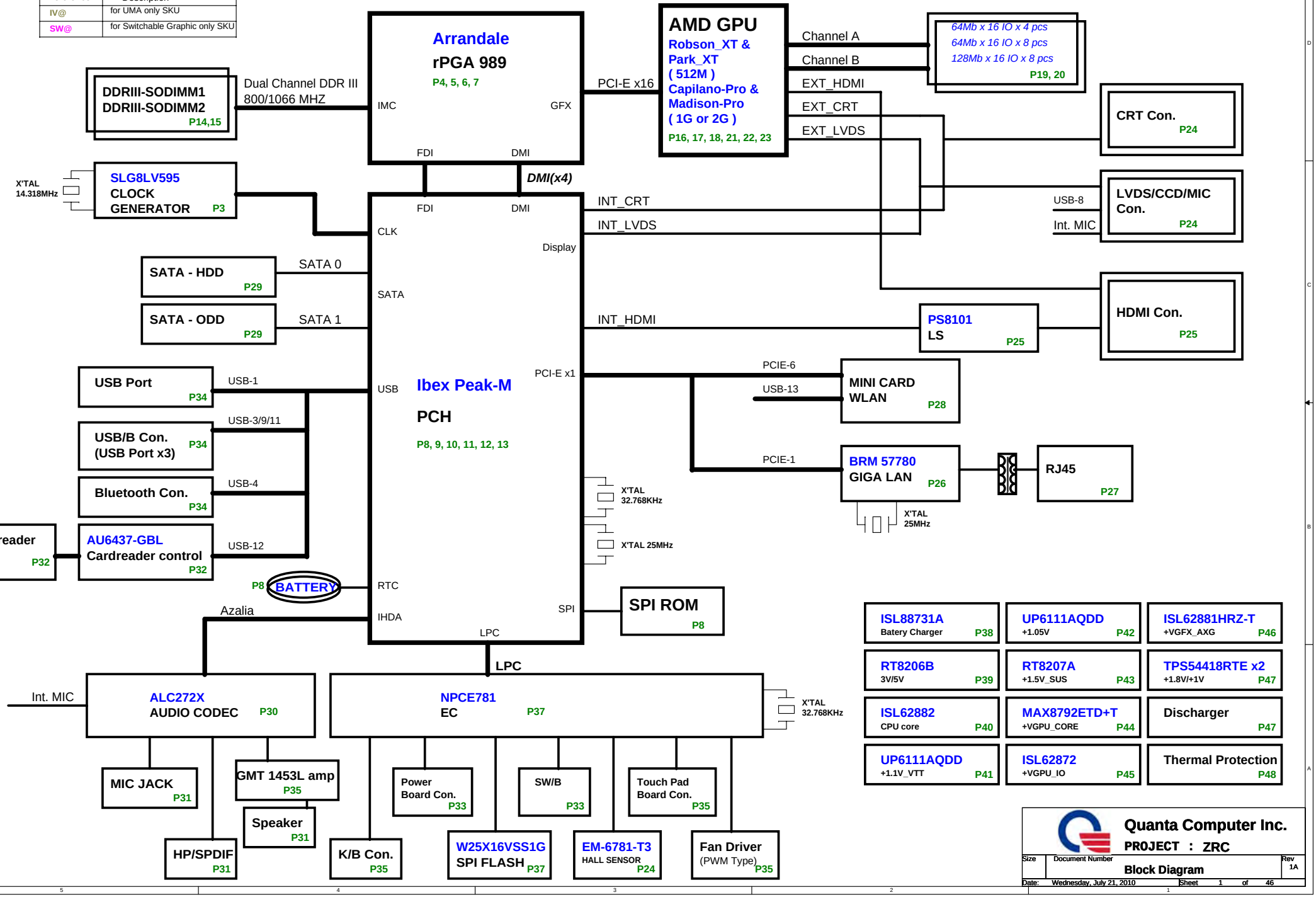
ZRC SYSTEM BLOCK DIAGRAM

BOM Option Table

Reference	Description
IV@	for UMA only SKU
SW@	for Switchable Graphic only SKU



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	Block Diagram	1A

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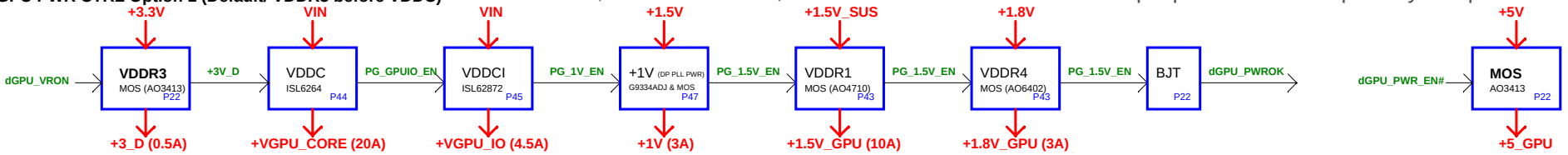
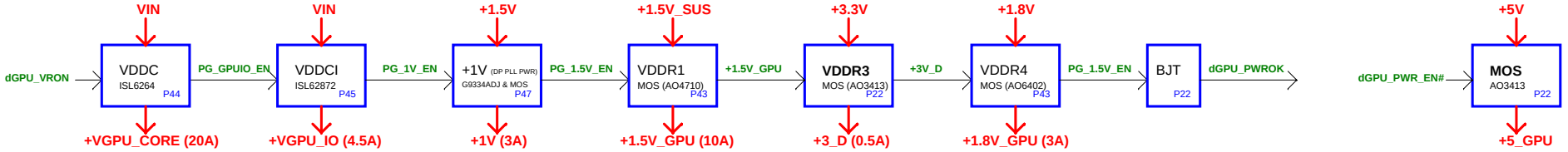
GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



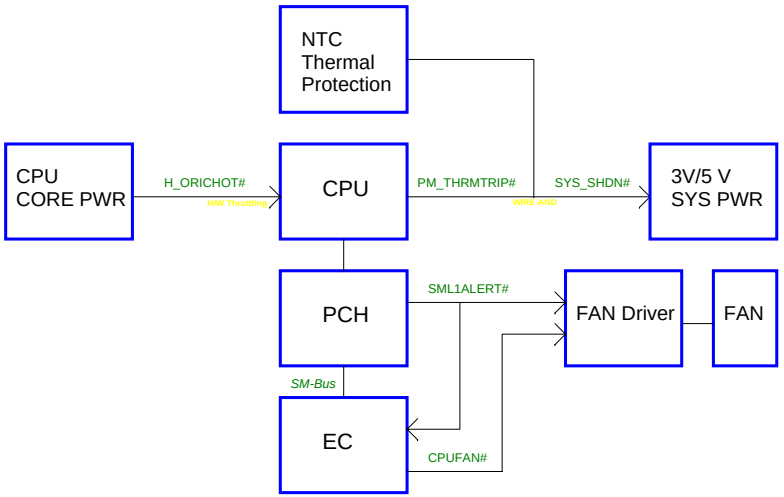
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart



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	PWR Status & GPU PWR CRL & THRM	1A

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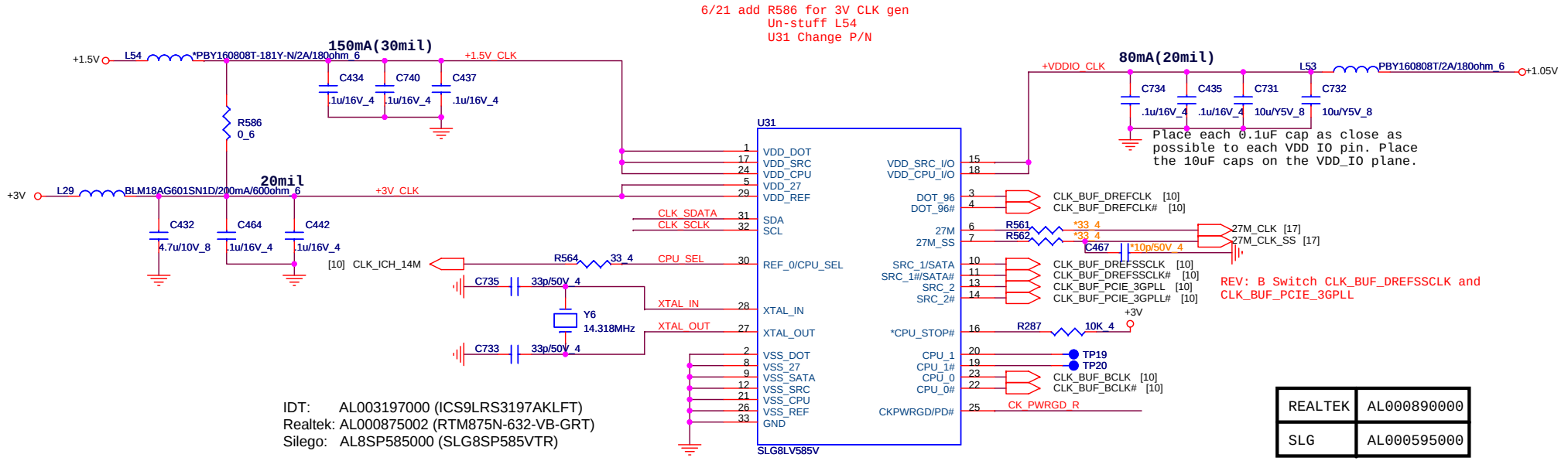
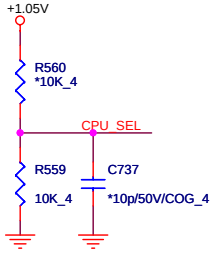


IDT: AL003197000 (ICS9LRS3197AKLFT)
Realtek: AL000875002 (RTM875N-632-VB-GRT)
Silego: AL8SP585000 (SLG8SP585VTR)

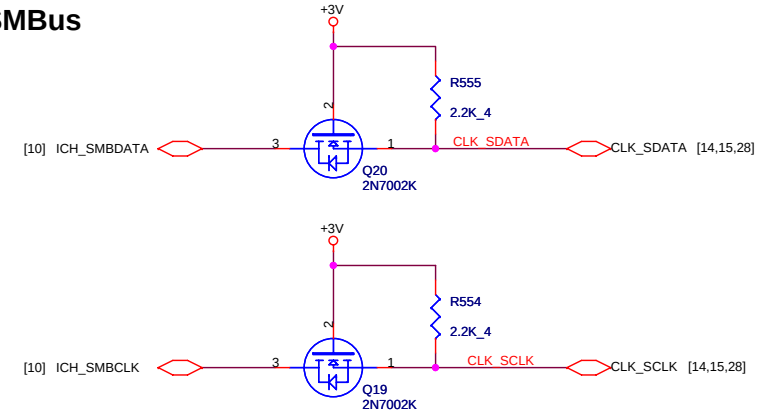
REALTEK	AL000890000
SLG	AL000595000

CPU_CLK select

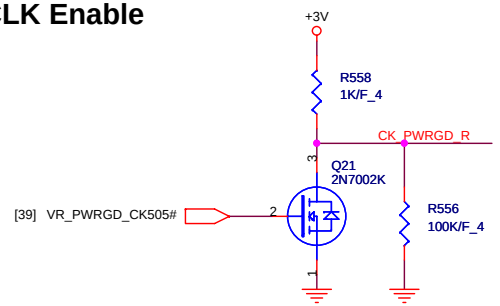


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus



CLK Enable



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	Clock Generator	1A

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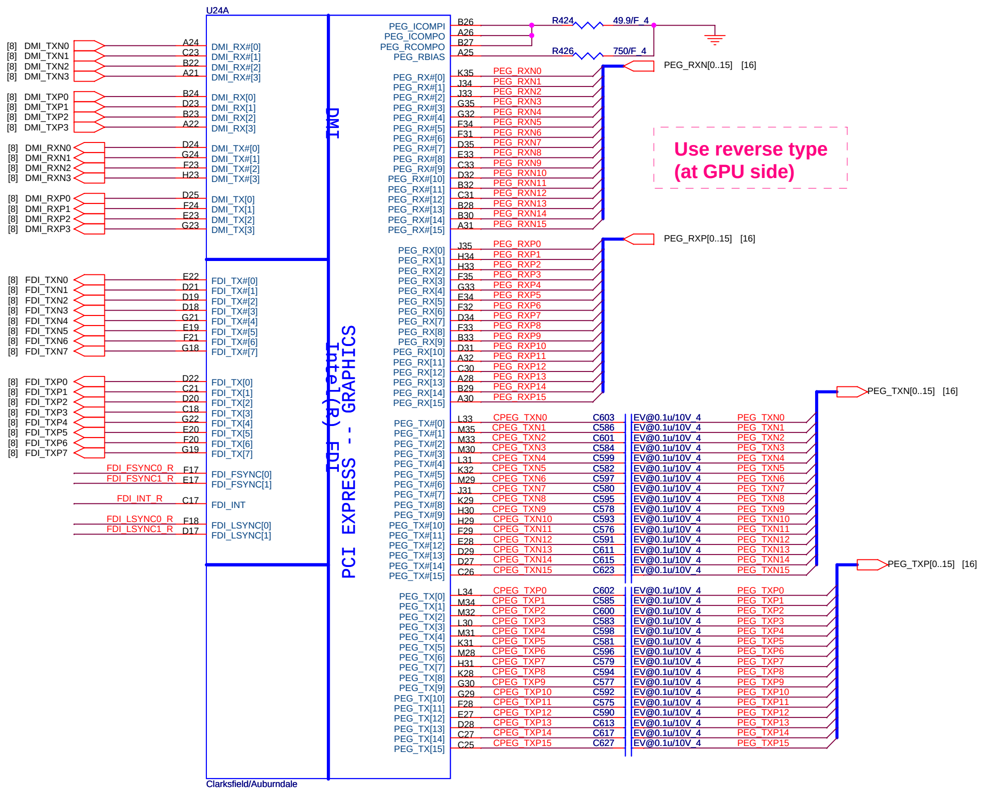
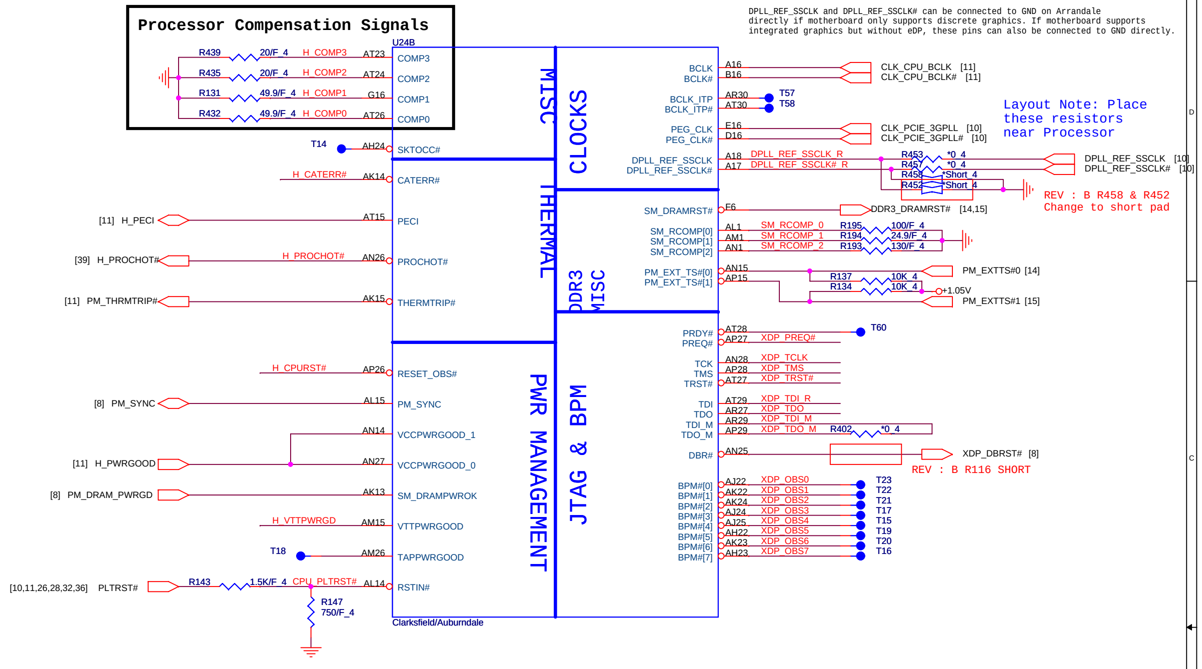
AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)

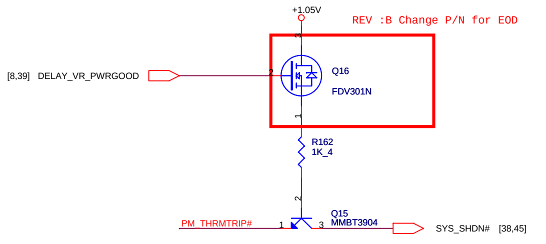


AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)

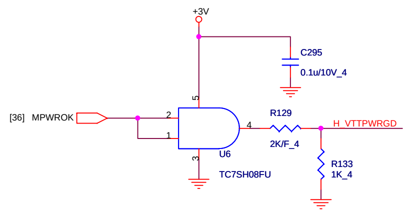


LTS	DGG^9000005
SUY	DGG^9000016
FOX	DGG^9000023

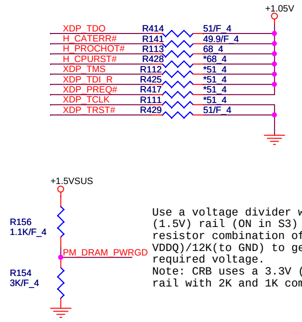
Thermaltrip protect



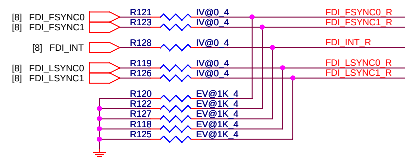
VTT PWR_Good



Processor pull-up



Use a voltage divider with VDDQ (1.5V) rail (ON in S3) and resistor combination of 4.75K (to VDDQ)/12K(to GND) to generate the required voltage.
Note: CRB uses a 3.3V (always ON) rail with 2K and 1K combination.



<The GFX_IMON, FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT>Note that if these signals are left as no connect, there are no functional impacts, but a small amount of power (~15 mW) maybe wasted.

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	AUBURNDA 1/4	1A
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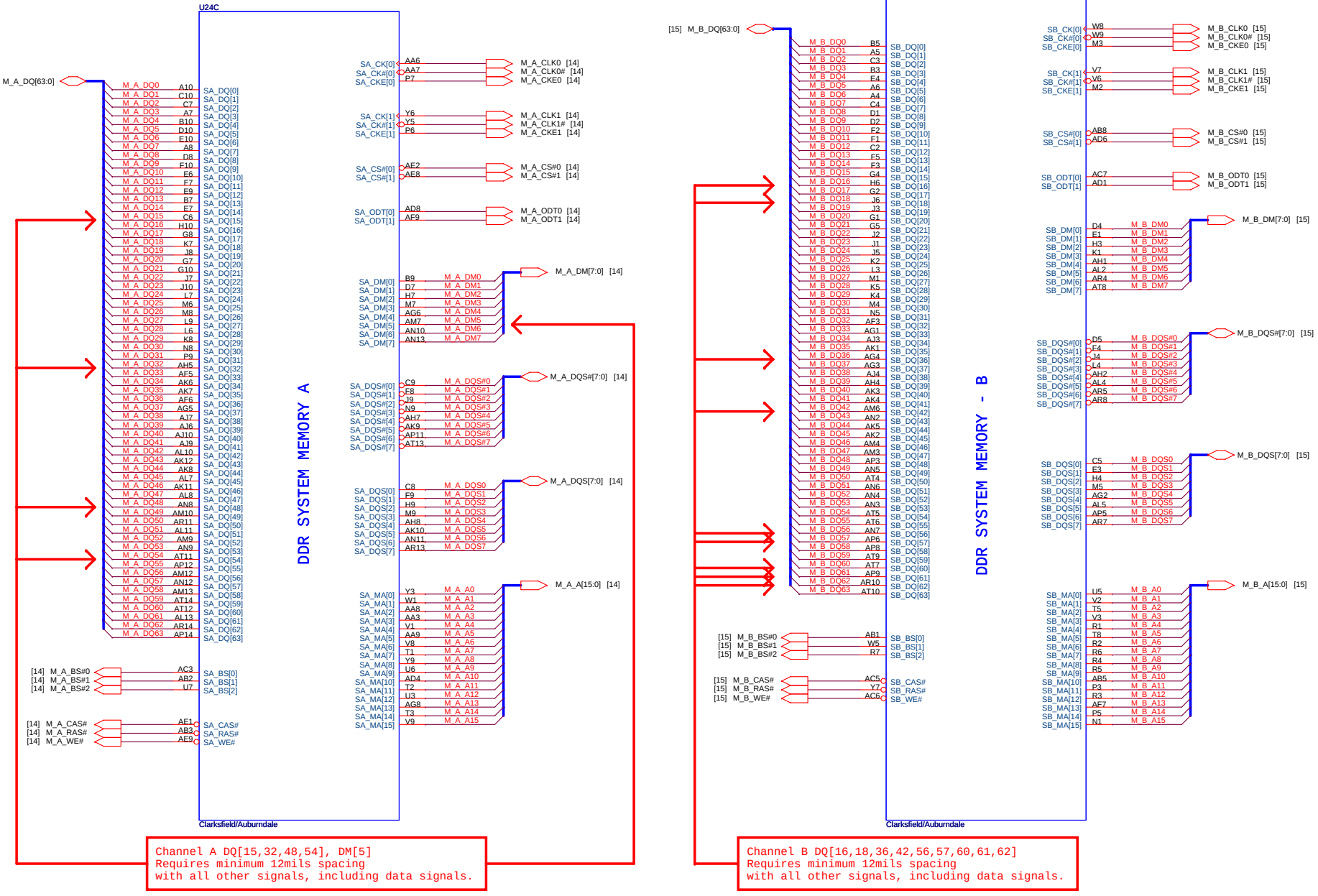
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Quanta Computer Inc.		
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AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

CPU Core Power

ARD:48A
CFD:52A

+VCC_CORE

C604 10U/6.3V_8
C653 22U/6.3V_8
C249 10U/6.3V_8
C607 22U/6.3V_8
C650 22U/6.3V_8
C673 10U/6.3V_8
C672 10U/6.3V_8
C196 22U/6.3V_8
C606 22U/6.3V_8
C670 10U/6.3V_8
C217 10U/6.3V_8
C181 22U/6.3V_8
C250 10U/6.3V_8
C195 10U/6.3V_8
C288 10U/6.3V_8
C651 10U/6.3V_8
C648 10U/6.3V_8
C669 10U/6.3V_8
C652 10U/6.3V_8
C605 10U/6.3V_8
C649 10U/6.3V_8
C274 10U/6.3V_8
C273 10U/6.3V_8
C251 10U/6.3V_8
C671 10U/6.3V_8
C286 10U/6.3V_8
C248 10U/6.3V_8
C662 10U/6.3V_8
C280 0.1u/10V_4
C276 0.1u/10V_4
C284 + 330u/2V_7343
C285 + 330u/2V_7343

U24F

AG35 VCC1
AG34 VCC2
AG33 VCC3
AG32 VCC4
AG31 VCC5
AG30 VCC6
AG29 VCC7
AG28 VCC8
AG27 VCC9
AG26 VCC10
AF35 VCC11
AF34 VCC12
AF33 VCC13
AF32 VCC14
AF31 VCC15
AF30 VCC16
AF29 VCC17
AF28 VCC18
AF27 VCC19
AF26 VCC20
AD35 VCC21
AD34 VCC22
AD33 VCC23
AD32 VCC24
AD31 VCC25
AD30 VCC26
AD29 VCC27
AD28 VCC28
AD27 VCC29
AD26 VCC30
AC35 VCC31
AC34 VCC32
AC33 VCC33
AC32 VCC34
AC31 VCC35
AC30 VCC36
AC29 VCC37
AC28 VCC38
AC27 VCC39
AC26 VCC40
AA35 VCC41
AA34 VCC42
AA33 VCC43
AA32 VCC44
AA31 VCC45
AA30 VCC46
AA29 VCC47
AA28 VCC48
AA27 VCC49
AA26 VCC50
Y35 VCC51
Y34 VCC52
Y33 VCC53
Y32 VCC54
Y31 VCC55
Y30 VCC56
Y29 VCC57
Y28 VCC58
Y27 VCC59
Y26 VCC60
V35 VCC61
V34 VCC62
V33 VCC63
V32 VCC64
V31 VCC65
V30 VCC66
V29 VCC67
V28 VCC68
V27 VCC69
V26 VCC70
U35 VCC71
U34 VCC72
U33 VCC73
U32 VCC74
U31 VCC75
U30 VCC76
U29 VCC77
U28 VCC78
U27 VCC79
U26 VCC80
R35 VCC81
R34 VCC82
R33 VCC83
R32 VCC84
R31 VCC85
R30 VCC86
R29 VCC87
R28 VCC88
R27 VCC89
R26 VCC90
P35 VCC91
P34 VCC92
P33 VCC93
P32 VCC94
P31 VCC95
P30 VCC96
P29 VCC97
P28 VCC98
P27 VCC99
P26 VCC100

Clarksfield/Auburndale

VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V

18A

1.1V RAIL POWER

VTT0_1 AH14
VTT0_2 AH12
VTT0_3 AH11
VTT0_4 AH10
VTT0_5 J14
VTT0_6 J13
VTT0_7 H14
VTT0_8 H12
VTT0_9 G14
VTT0_10 G13
VTT0_11 G12
VTT0_12 G11
VTT0_13 F14
VTT0_14 F13
VTT0_15 F12
VTT0_16 F11
VTT0_17 E14
VTT0_18 E12
VTT0_19 D14
VTT0_20 D13
VTT0_21 D12
VTT0_22 D11
VTT0_23 C14
VTT0_24 C13
VTT0_25 C12
VTT0_26 C11
VTT0_27 B14
VTT0_28 B12
VTT0_29 A14
VTT0_30 A13
VTT0_31 A12
VTT0_32 A11

+1.05V

C694 10U/6.3V_8
C693 10U/6.3V_8
C664 10U/6.3V_8
C306 10U/6.3V_8
C678 10U/6.3V_8
C685 10U/6.3V_8
C675 10U/6.3V_8
C695 10U/6.3V_8
C696 10U/6.3V_8
C308 10U/6.3V_8
C301 + 330u/2V_7343

CPU CORE SUPPLY

VTT0_33 AF10
VTT0_34 AE10
VTT0_35 AC10
VTT0_36 AB10
VTT0_37 Y10
VTT0_38 W10
VTT0_39 U10
VTT0_40 T10
VTT0_41 J12
VTT0_42 J11
VTT0_43 J16
VTT0_44 J15

+1.05V

C298 22U/6.3V_8
C305 22U/6.3V_8

POWER

CPU VIDS

PSI# AN33 H_PSI# → H_PSI# [39]

VID[0] AK35 H_VID0 → H_VID0 [39]
VID[1] AK33 H_VID1 → H_VID1 [39]
VID[2] AK34 H_VID2 → H_VID2 [39]
VID[3] AL35 H_VID3 → H_VID3 [39]
VID[4] AL33 H_VID4 → H_VID4 [39]
VID[5] AM33 H_VID5 → H_VID5 [39]
VID[6] AM35 H_VID6 → H_VID6 [39]
PROC_DPRSLPVR AM34 H_DPRSLPVR → H_DPRSLPVR [39]

VTT_SELECT G15

H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V

SENSE LINES

ISENSE AN35 → I_MON [39]

VCC_SENSE A34 — R71 100/F_4 — +VCC_CORE → VCCSENSE [39]
VSS_SENSE A35 — R70 100/F_4 → VSSSENSE [39]

VTT_SENSE B15 VTT_SENSE → T64
VSS_SENSE_VTT A15 VSS_SENSE_VTT → T63

AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)

+VGFX_AXG

22A

+ C665 *330U/2V_7343
C283 1V@22u/6.3V_8
C282 1V@22u/6.3V_8
+ C686 *330U/2V_7343
C289 1V@10u/6.3V_8
C290 1V@10u/6.3V_8

U24G

AT21 VAXG1
AT19 VAXG2
AT18 VAXG3
AT16 VAXG4
AR21 VAXG5
AR19 VAXG6
AR18 VAXG7
AR16 VAXG8
AP21 VAXG9
AP19 VAXG10
AP18 VAXG11
AP16 VAXG12
AN21 VAXG13
AN19 VAXG14
AN18 VAXG15
AN16 VAXG16
AM21 VAXG17
AM19 VAXG18
AM18 VAXG19
AM16 VAXG20
AL21 VAXG21
AL19 VAXG22
AL18 VAXG23
AL16 VAXG24
AK21 VAXG25
AK19 VAXG26
AK18 VAXG27
AK16 VAXG28
AJ21 VAXG29
AJ19 VAXG30
AJ18 VAXG31
AJ16 VAXG32
AH21 VAXG33
AH19 VAXG34
AH18 VAXG35
AH16 VAXG36

R117 EV@1K_4

GRAPHICS

SENSE LINES

VAXG_SENSE AR22 → VCC_AXG_SENSE [42]
VSSAXG_SENSE AT22 → VSS_AXG_SENSE [42]

GRAPHICS VIDs

GFX_VID[0] AM22 → GFX_VID0 [42]
GFX_VID[1] AP22 → GFX_VID1 [42]
GFX_VID[2] AN22 → GFX_VID2 [42]
GFX_VID[3] AP23 → GFX_VID3 [42]
GFX_VID[4] AM23 → GFX_VID4 [42]
GFX_VID[5] AP24 → GFX_VID5 [42]
GFX_VID[6] AN24 → GFX_VID6 [42]

GFX_VR_EN AR25 → GFX_ON [42]
GFX_DPRSLPVR AT25 → GFX_DPRSLPVR [42]
GFX_IMON AM24 → GFX_IMON [42]

R115 EV@1K_4

ARD:3A
CFD:6A

DDR3 - 1.5V RAILS

VDDQ1 AJ1
VDDQ2 AF1
VDDQ3 AE7
VDDQ4 AE4
VDDQ5 AC1
VDDQ6 AB7
VDDQ7 AB4
VDDQ8 Y1
VDDQ9 W7
VDDQ10 W4
VDDQ11 U1
VDDQ12 T7
VDDQ13 T4
VDDQ14 P1
VDDQ15 N7
VDDQ16 N4
VDDQ17 L1
VDDQ18 H1

+1.5VSUS

C347 1U/6.3V_4
C342 1U/6.3V_4
C341 1U/6.3V_4
C338 1U/6.3V_4
C415 1U/6.3V_4
C352 22U/6.3V_8
C343 22U/6.3V_8
+ C358 *330U/2V_7343

+1.05V

C296 10U/6.3V_8
C691 22U/6.3V_8

J24 VTT1_45
J23 VTT1_46
H25 VTT1_47

POWER

FDI

PEG & DMI

C309 10U/6.3V_8
C692 10U/6.3V_8
C297 22U/6.3V_8
C307 22U/6.3V_8

K26 VTT1_48
J27 VTT1_49
J26 VTT1_50
J25 VTT1_51
H27 VTT1_52
G28 VTT1_53
G27 VTT1_54
G26 VTT1_55
F26 VTT1_56
E26 VTT1_57
E25 VTT1_58

1.1V

VTT0_59 P10
VTT0_60 N10
VTT0_61 L10
VTT0_62 K10

+1.05V

C697 10U/6.3V_8
C690 10U/6.3V_8

VTT1_63 J22
VTT1_64 J20
VTT1_65 J18
VTT1_66 H21
VTT1_67 H20
VTT1_68 H19

C644 10U/6.3V_8
C658 10U/6.3V_8

1.8V

0.6A

VCCPLL1 L26
VCCPLL2 L27
VCCPLL3 M26

+1.8V

C271 22U/6.3V_8
C278 4.7U/6.3V_6
C223 2.2U/6.3V_6
C225 1U/6.3V_4
C226 1U/6.3V_4

Clarksfield/Auburndale

H_VID0 1 R381 1K_4 R386 *1K/F_4
H_VID1 1 R380 1K_4 R385 *1K/F_4
H_VID2 1 R382 1K_4 R387 *1K/F_4
H_VID3 0 R389 *1K/F_4 R395 1K_4
H_VID4 0 R390 *1K/F_4 R396 1K_4
H_VID5 1 R393 1K_4 R399 *1K/F_4
H_VID6 0 R391 *1K/F_4 R397 1K_4
H_DPRSLPVR 1 R392 1K_4 R398 *1K/F_4
H_PSI# 0 R407 *1K/F_4 R401 1K_4

→ +1.05V

Note:
For Validating IMVP VR R6451 should be STUFF and R2N1 NO_STUFF

HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

Quanta Computer Inc.
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	AUBURNDA 3/4 (PWR)	1A

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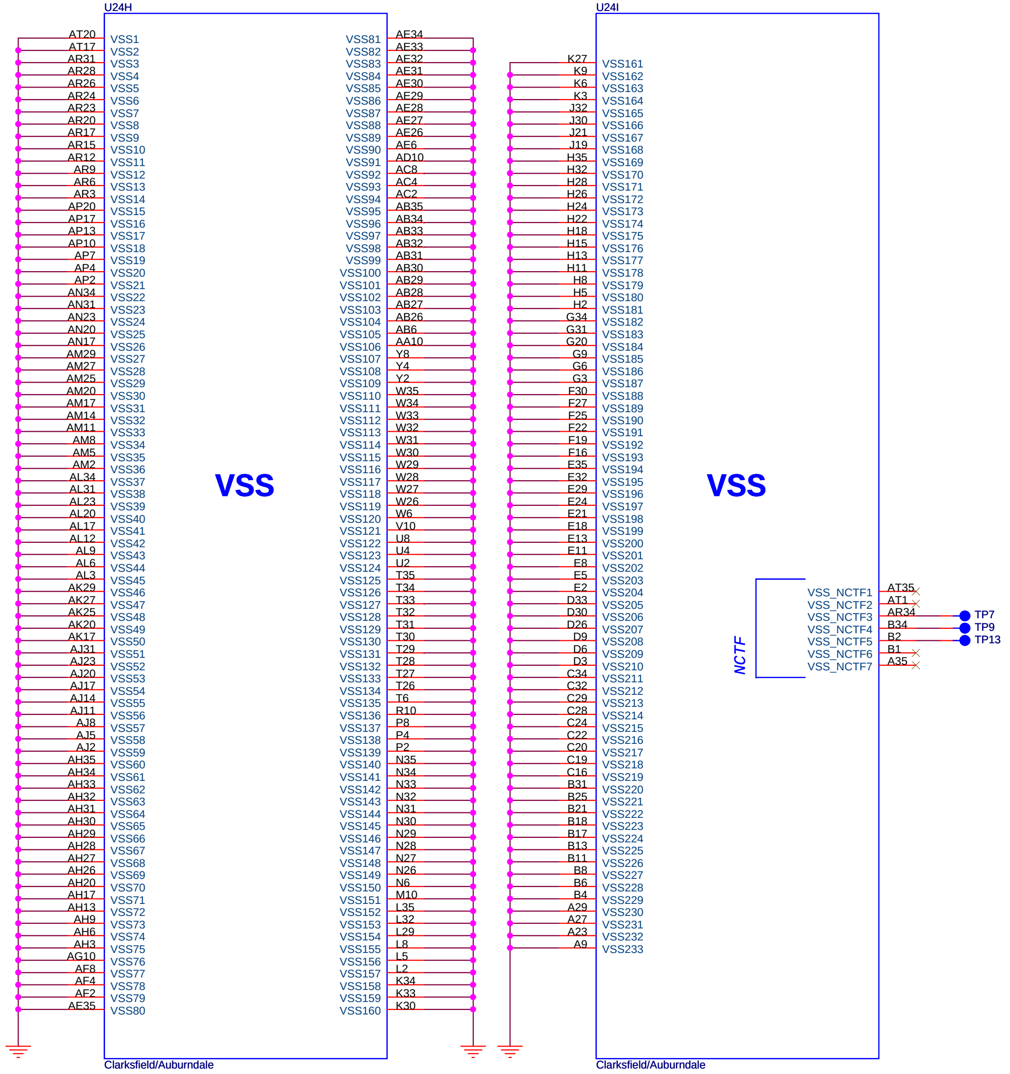
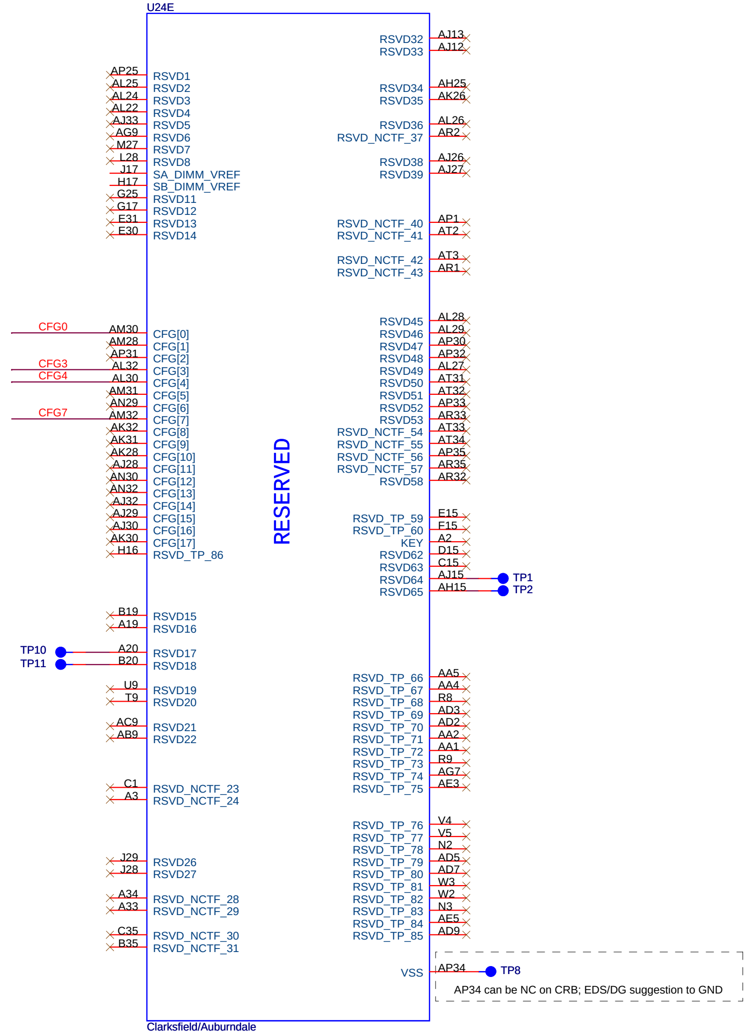
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)





Processor Strapping

	1	0	DEFAULT	
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1	CFG0 R110 *3.01K_NC
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1	CFG3 R102 3.01K/F_4
CFG4 (Embedded Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port	1	CFG4 R109 *3.01K
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA ~~components. This pull down resistor should be removed when this issue is fixed.~~				CFG7 R103 *3.01K/F_4

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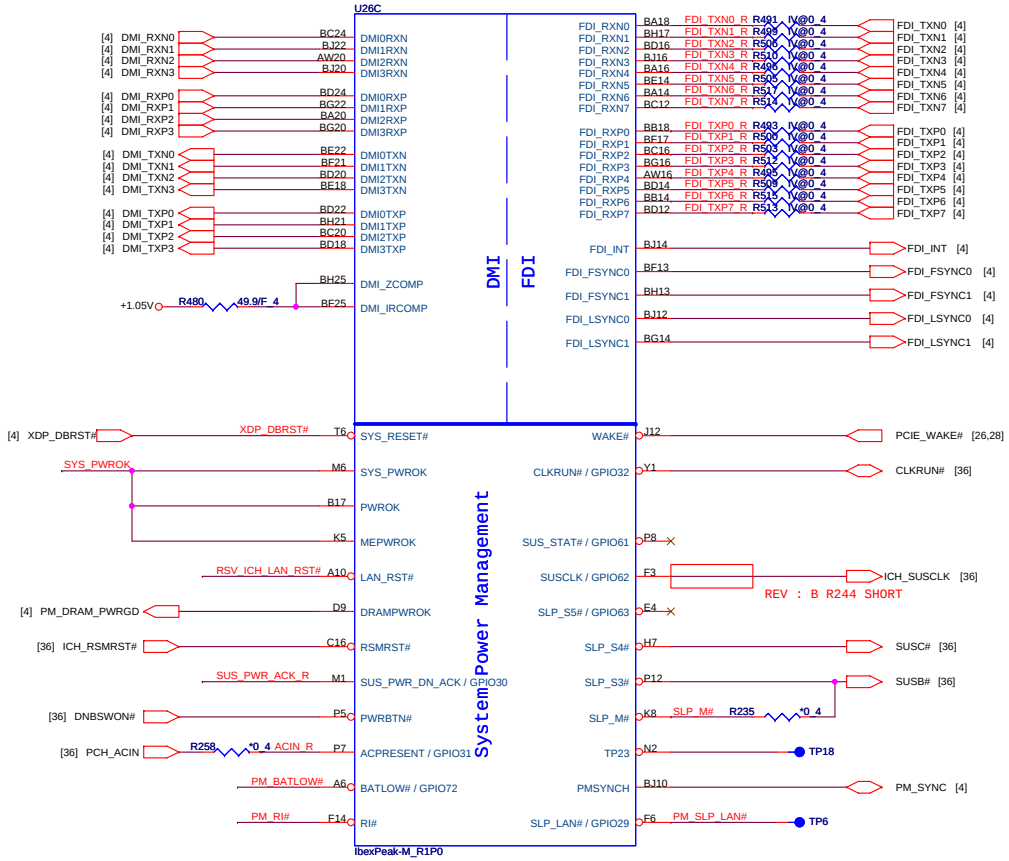
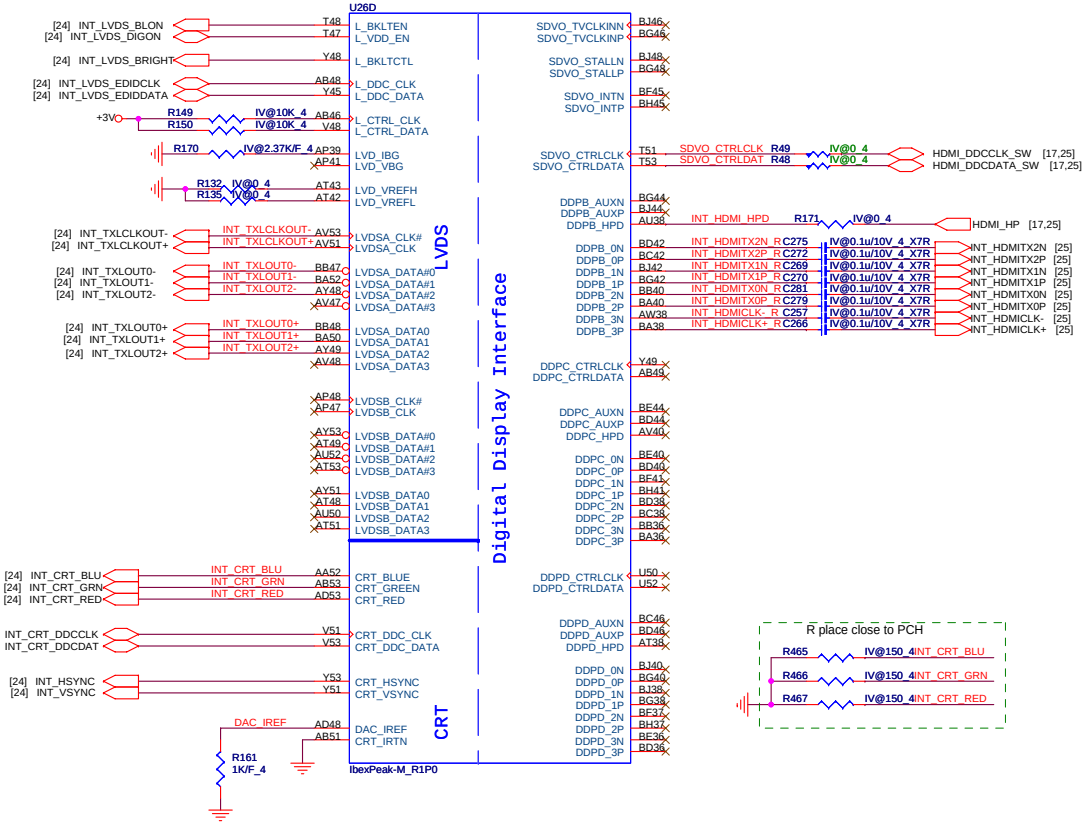
IBEX PEAK-M (DMI,FDI,GPIO)

0-ohm resistor place close to PCH

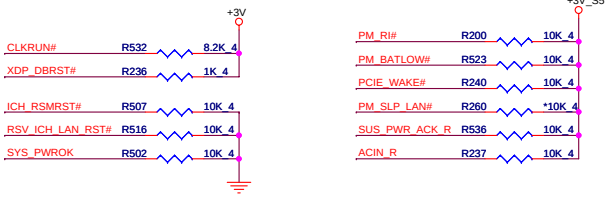


AC-coupling CAP place close to PCH

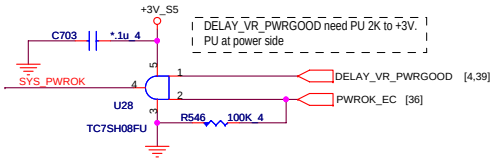
IBEX PEAK-M (LVDS,DDI)



PCH Pull-high/low



System PWR_OK



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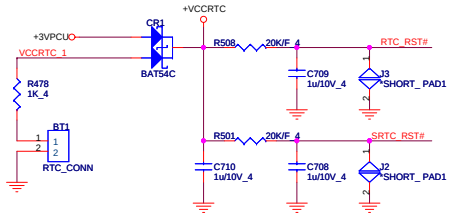
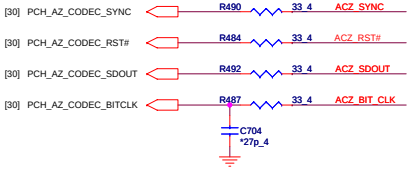
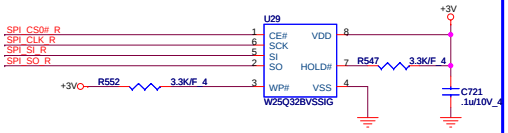
RTC Circuitry



HDA Bus

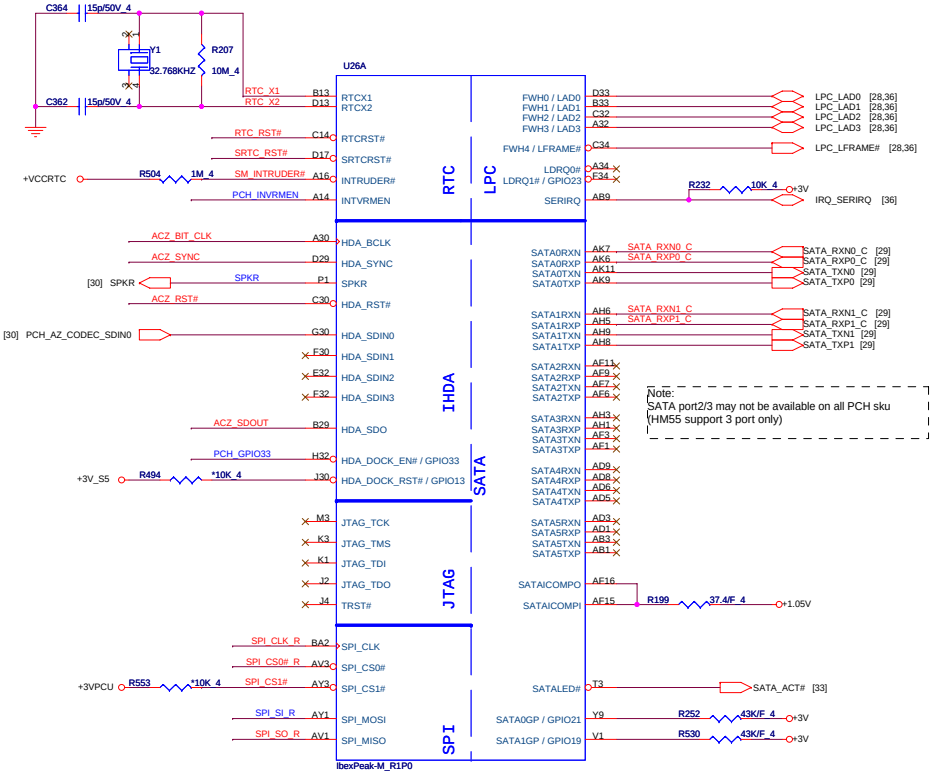


PCH SPI



HDA_SYNC (PCH strap pin)

Internal weak pull-down
VCCVRM=>+1.8V (default)
external pull-up
VCCVRM=>+1.5V



Note:
SATA port2/3 may not be available on all PCH sku (HM55 support 3 port only)

PCH Strap Pin Configuration Table-1

INTVRMEN	Integrated 1.05V VRM Enable / Disable	1 = Integrated VRM is enabled 0 = Integrated VRM is disabled	+VCCRTC R511 330K_6 PCH_INVRMEN
SPI_MOSI	TPM Functionality Disable	1 = Enabled 0 = Disable	+3V R551 *1K_4 SPI_SI_R
SPKR	Reboot option at power-up	0 = Default Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled	+3V R538 *1K/F_4 SPKR
HDA_DOCK_EN #/GPIO33	Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled.	PCH_GPIO33 J1 *SHORT_PAD1
GNT0#, GNT1#	Boot BIOS Strap	(0,0) = LPC (0,1) = Reserved NAND (1,0) = PCI (1,1) = SPI	[10] PCI_GNT0# R158 1K_4 [10] PCI_GNT1# R152 1K_4 R153 *1K_4 R159 *1K_4 +3V
GNT2#/ GPIO53	ESI Strap (Server Only)	ESI compatible mode is for server platforms only	[10] PWM_SELECT# R182 *1K/F_4
GNT3#/ GPIO55	Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (Internal pull-up)	[10] PCI_GNT3# R462 *10K/F_4
NV_ALE	IntelR Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable	1 = Enabled 0 = Disabled (Default)	[10] NV_ALE R213 *1K/F_4 +1.8V
NV_CLE	DMI Termination Voltage	DMI termination voltage. Weak internal pull-up. Do not pull low.	[10] NV_CLE R216 *1K/F_4 +1.8V

GPIO8	Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low	[11] RSV_GPIO8 R215 10K_4 +3V_S5 R214 *1K_4
GPIO15	Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality	[11] CR_WAKE# R256 1K_4 +3V_S5
GPIO27	On-Die PLL Voltage Regulator <internal weak pull-up>	0 = Disables the VccVRM. 1 = Enables the internal VccVRM to have a clean supply for analog rails.	[11] PCH_GPIO27 R231 *10K_4

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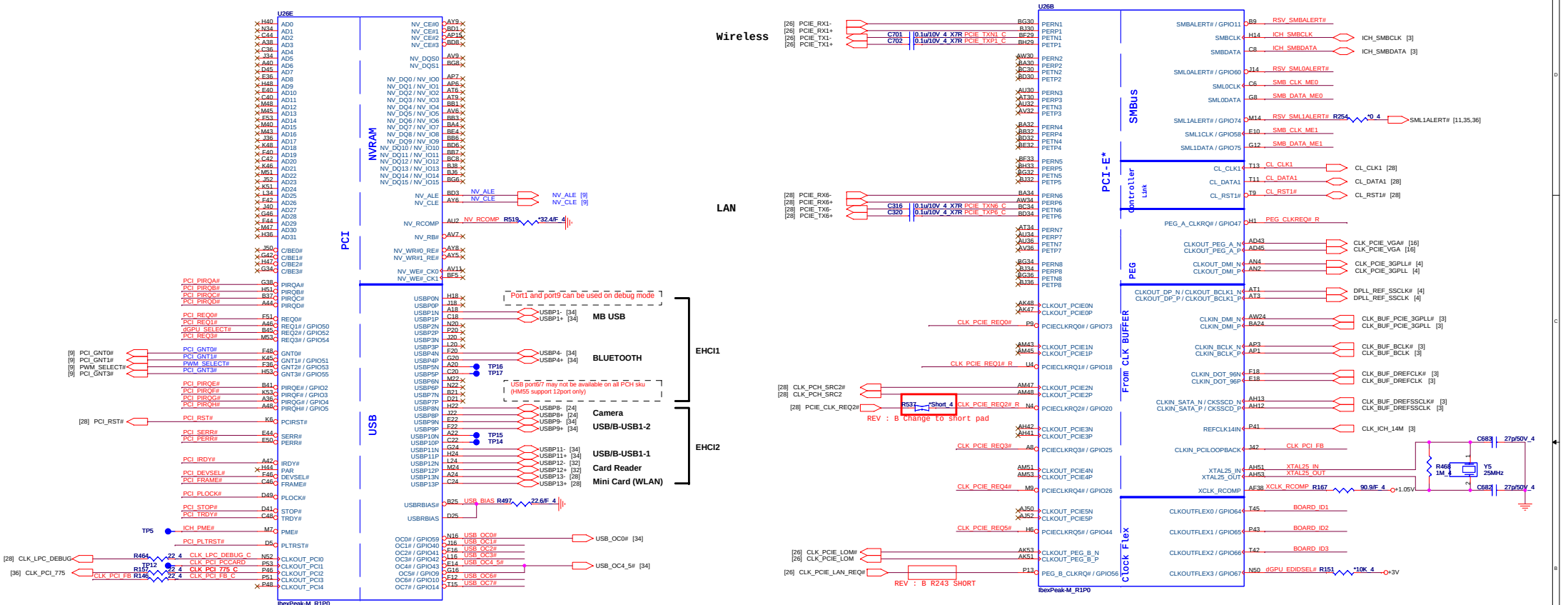
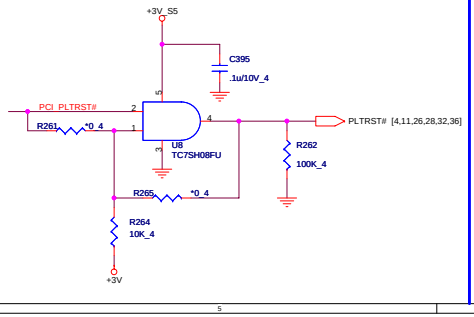
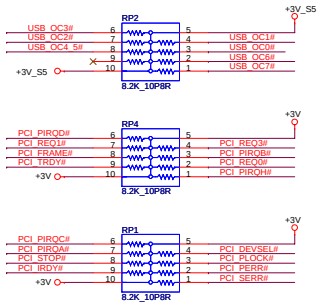
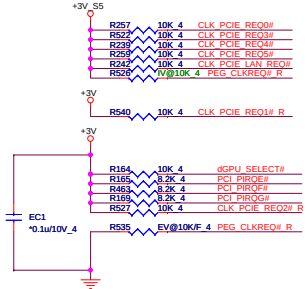


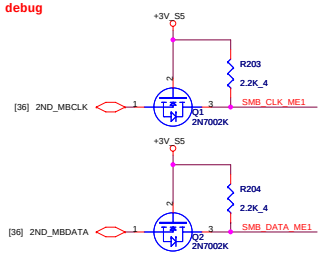






R163 stuff/R442 non stuff for SMT debug

BOARD_ID1	High = Capitano Low = Madsion or other GPUs
BOARD_ID2	High = 80port output to LPC Low = 80port output to PCI
BOARD_ID3	High = Reserved Low = Reserved (Default)



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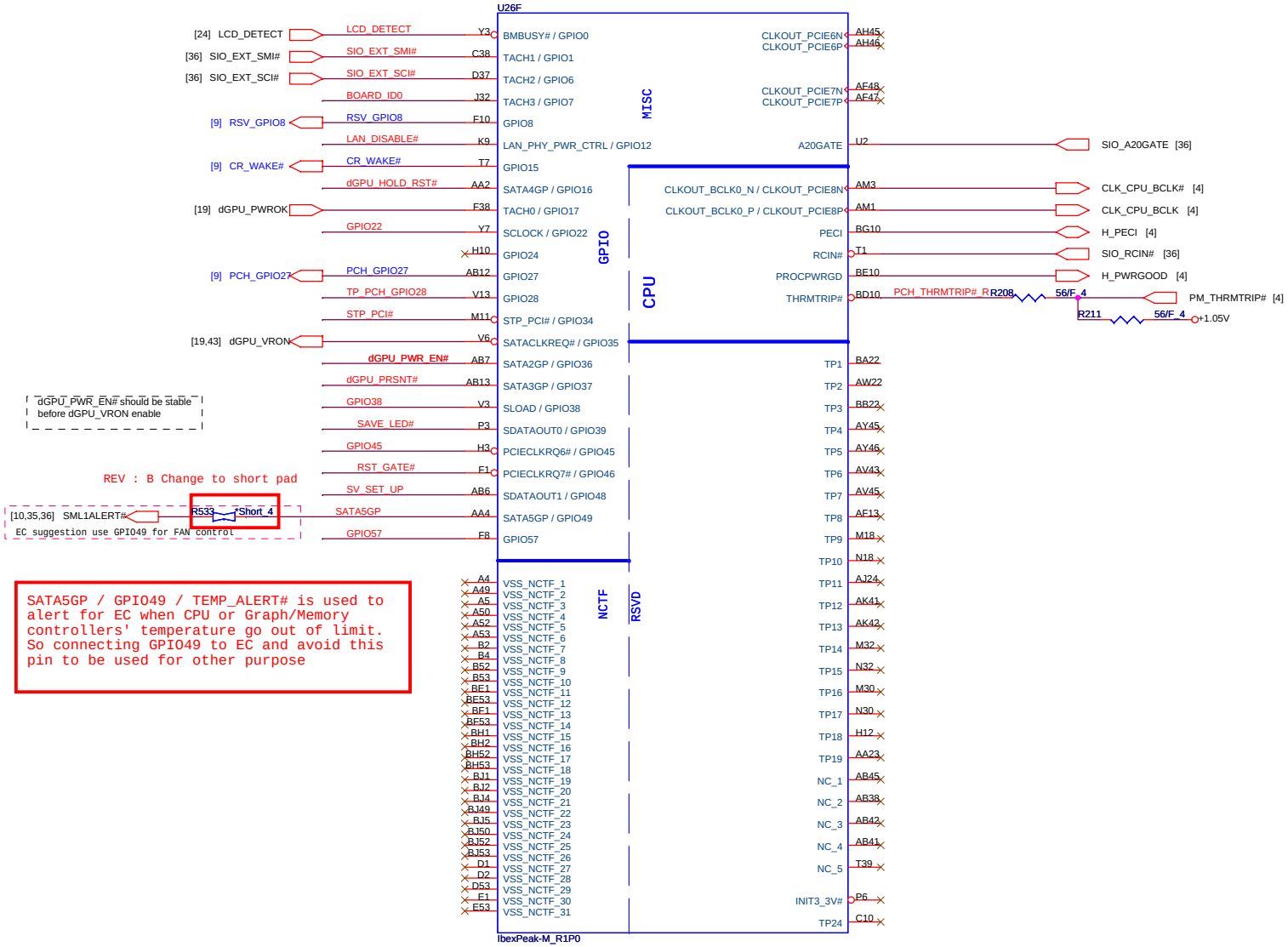
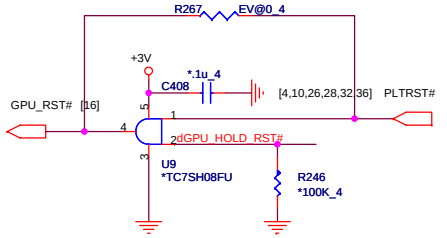
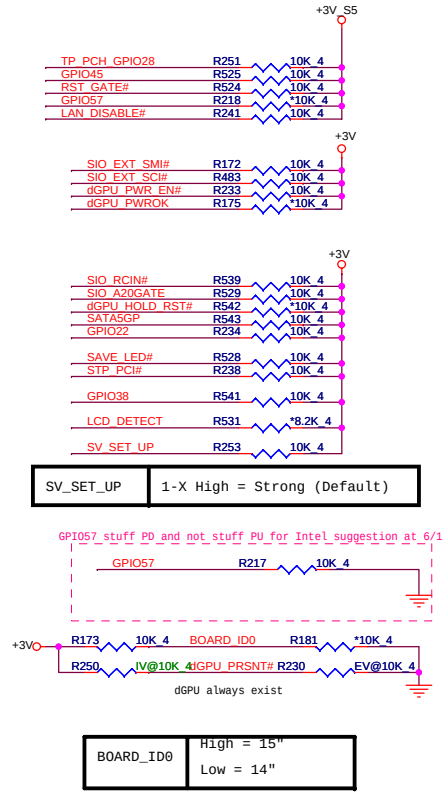
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



GPU RST#



GPIO Pull-up/Pull-down



SV_SET_UP	1-X High = Strong (Default)

BOARD_ID0	High = 15" Low = 14"

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IBEX PEAK-M (POWER)

VRM enable by strap pin GPIO27
which supply clean 1.05V for
[VCCACLK,VCCAPLLEXP,VCCFDIPLL,VCCSATAPLL]

HDA_SYNC (PCH strap pin)
Internal weak pull-down
VCCVRM=>+1.8V (default)
external pull-up
VCCVRM=>+1.5V

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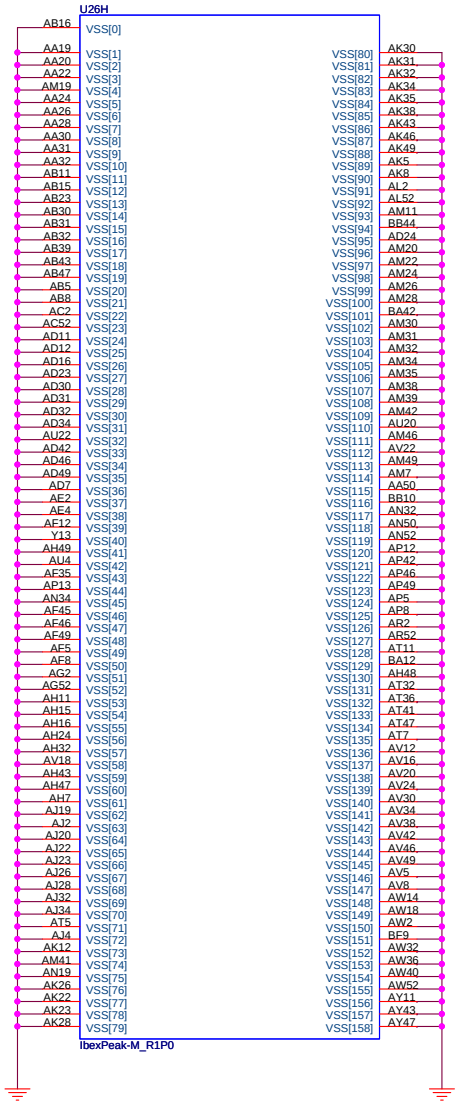
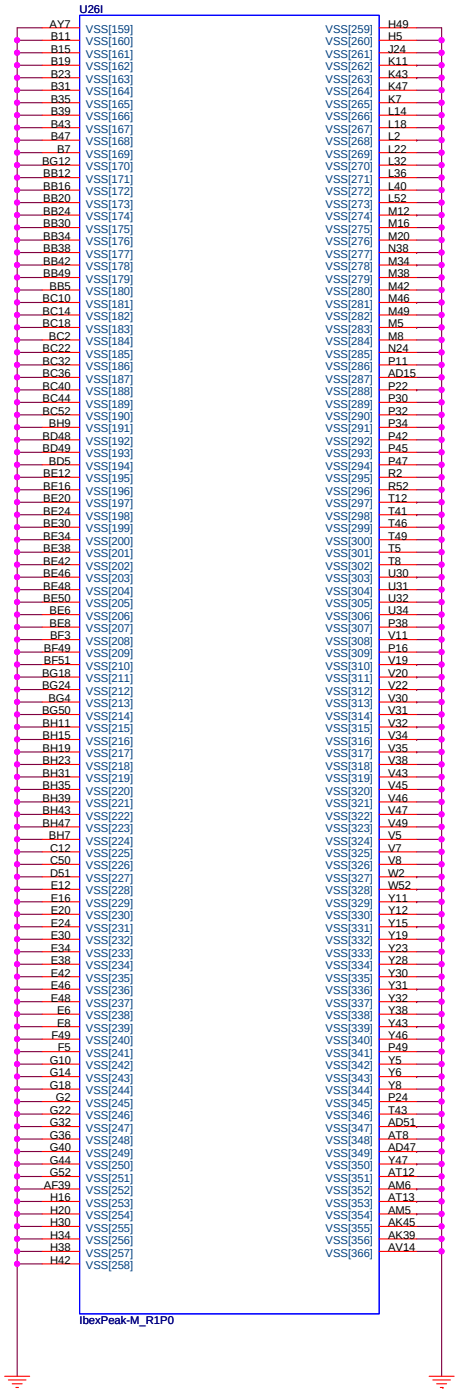
IBEX PEAK-M (GND)





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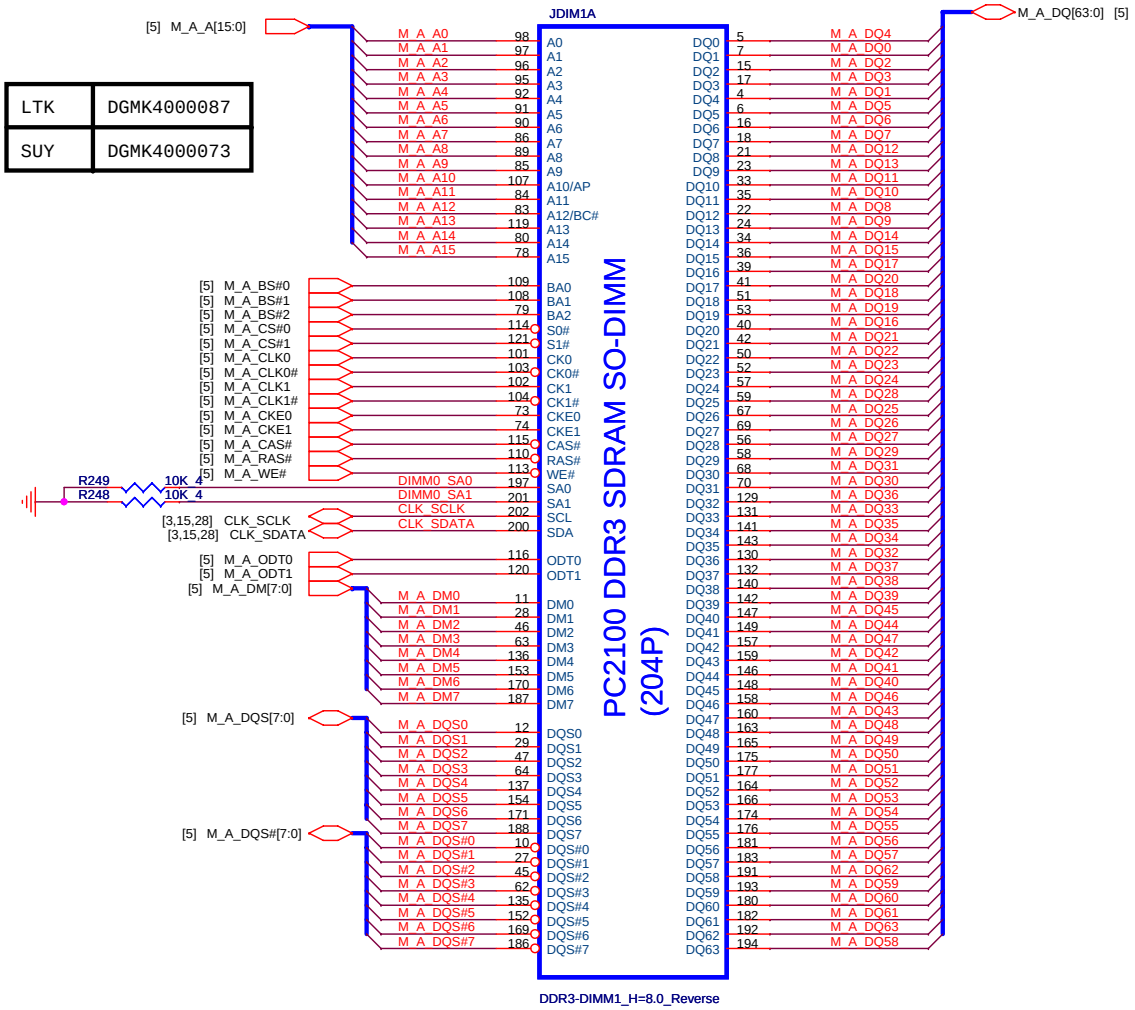
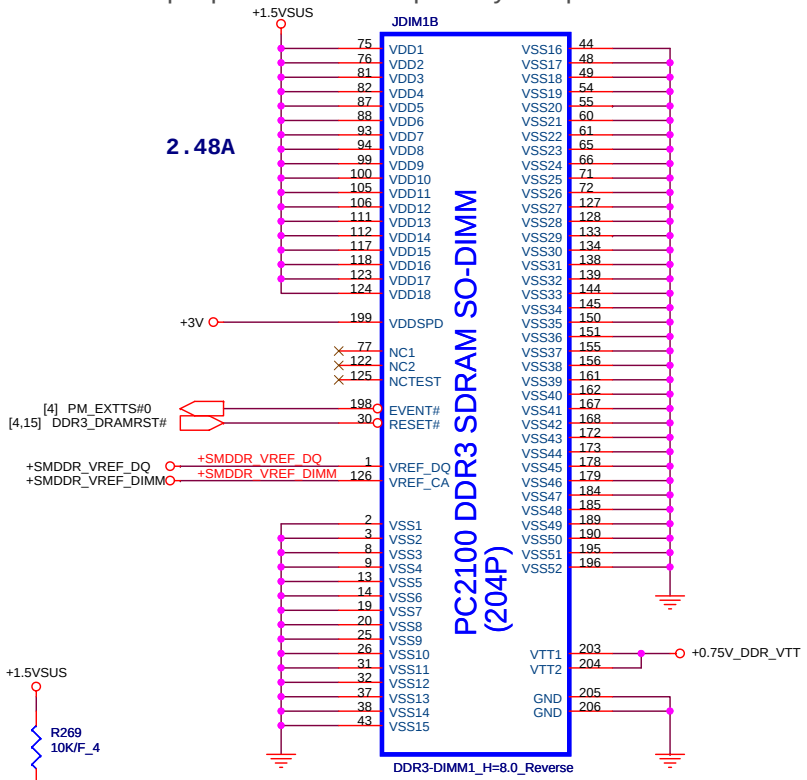
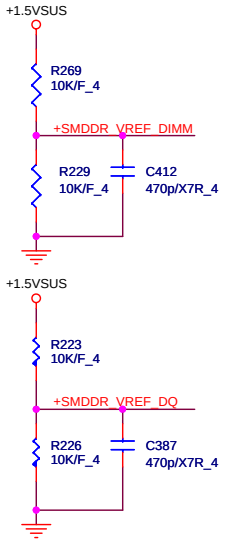
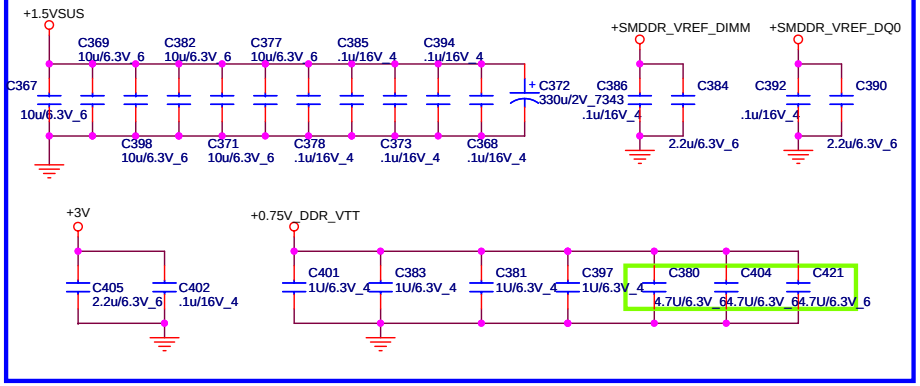
LTK	DGMK4000087
SUY	DGMK4000073







Place these Caps near So-Dimm0.



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	DDRIII SO-DIMM-0	1A
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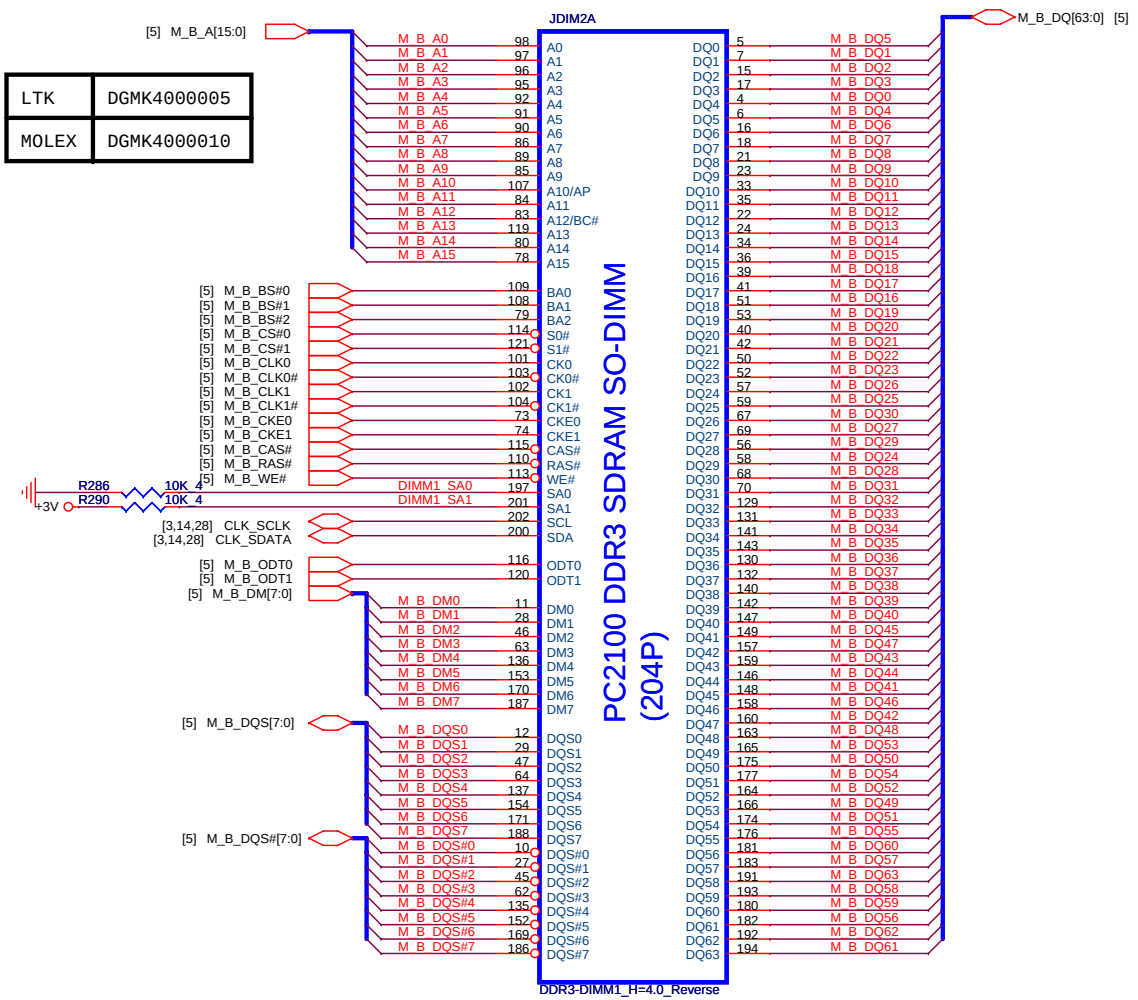
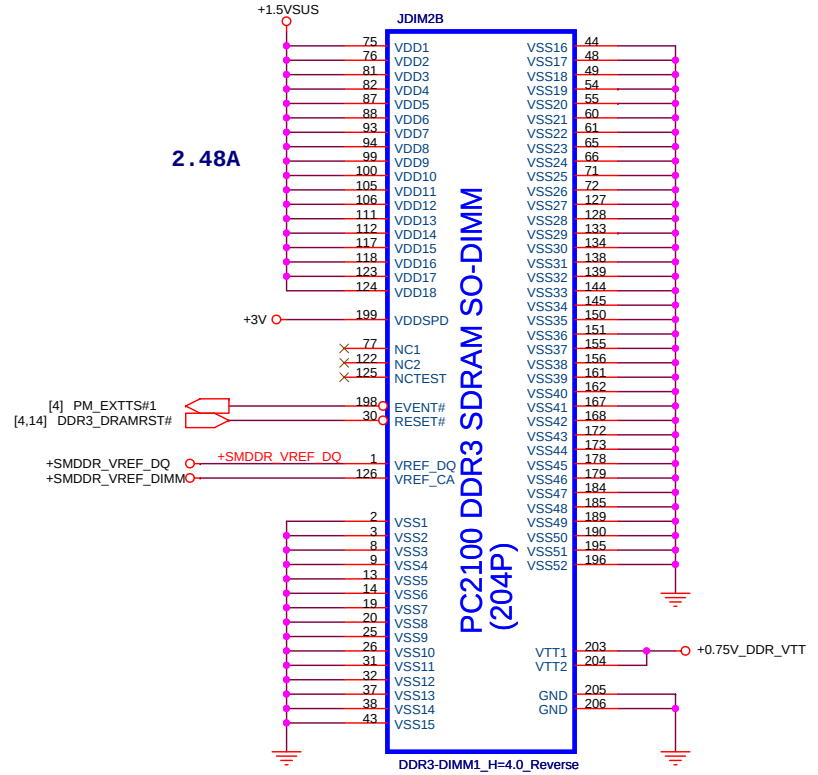
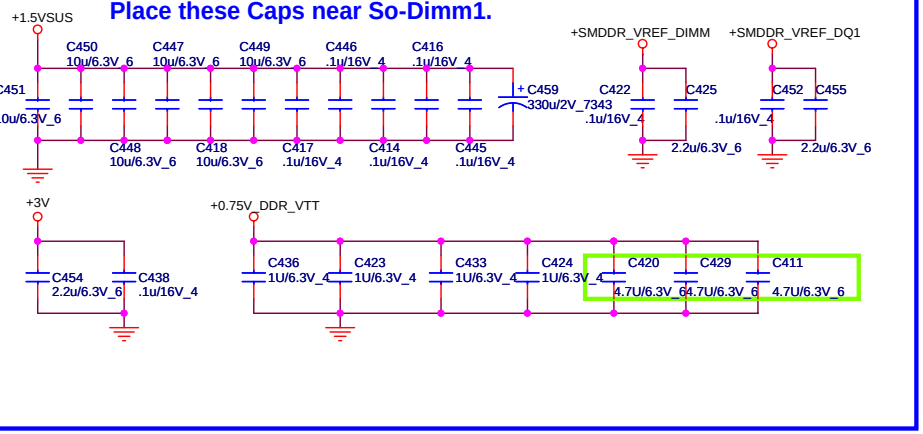
LTK	DGMK4000005
MOLEX	DGMK4000010







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GPU_1(VGA)

[4] PEG_TXP[0..15] — PEG_TXP[0..15]
[4] PEG_TXN[0..15] — PEG_TXN[0..15]
[4] PEG_RXP[0..15] — PEG_RXP[0..15]
[4] PEG_RXN[0..15] — PEG_RXN[0..15]

U21A

0518 SWAP PCIE for VGA side

[4] PEG_TXP15 / [4] PEG_TXN15	PEG_TXP15 / PEG_TXN15	AA38 / Y37	PCIE_RX0P / PCIE_RX0N	PCIE_TX0P / PCIE_TX0N	Y33 / Y32	CPEG_RXP15 / CPEG_RXN15	C155 / C164	EV@0.1u/10V_4	PEG_RXP15 [4] / PEG_RXN15 [4]
[4] PEG_TXP14 / [4] PEG_TXN14	PEG_TXP14 / PEG_TXN14	Y35 / W36	PCIE_RX1P / PCIE_RX1N	PCIE_TX1P / PCIE_TX1N	W33 / W32	CPEG_RXP14 / CPEG_RXN14	C147 / C154	EV@0.1u/10V_4	PEG_RXP14 [4] / PEG_RXN14 [4]
[4] PEG_TXP13 / [4] PEG_TXN13	PEG_TXP13 / PEG_TXN13	W38 / V37	PCIE_RX2P / PCIE_RX2N	PCIE_TX2P / PCIE_TX2N	U33 / U32	CPEG_RXP13 / CPEG_RXN13	C141 / C146	EV@0.1u/10V_4	PEG_RXP13 [4] / PEG_RXN13 [4]
[4] PEG_TXP12 / [4] PEG_TXN12	PEG_TXP12 / PEG_TXN12	V35 / U36	PCIE_RX3P / PCIE_RX3N	PCIE_TX3P / PCIE_TX3N	U30 / U29	CPEG_RXP12 / CPEG_RXN12	C136 / C131	EV@0.1u/10V_4	PEG_RXP12 [4] / PEG_RXN12 [4]
[4] PEG_TXP11 / [4] PEG_TXN11	PEG_TXP11 / PEG_TXN11	U38 / T37	PCIE_RX4P / PCIE_RX4N	PCIE_TX4P / PCIE_TX4N	T33 / T32	CPEG_RXP11 / CPEG_RXN11	C130 / C116	EV@0.1u/10V_4	PEG_RXP11 [4] / PEG_RXN11 [4]
[4] PEG_TXP10 / [4] PEG_TXN10	PEG_TXP10 / PEG_TXN10	T35 / R36	PCIE_RX5P / PCIE_RX5N	PCIE_TX5P / PCIE_TX5N	T30 / T29	CPEG_RXP10 / CPEG_RXN10	C109 / C106	EV@0.1u/10V_4	PEG_RXP10 [4] / PEG_RXN10 [4]
[4] PEG_TXP9 / [4] PEG_TXN9	PEG_TXP9 / PEG_TXN9	R38 / P37	PCIE_RX6P / PCIE_RX6N	PCIE_TX6P / PCIE_TX6N	P33 / P32	CPEG_RXP9 / CPEG_RXN9	C105 / C92	EV@0.1u/10V_4	PEG_RXP9 [4] / PEG_RXN9 [4]
[4] PEG_TXP8 / [4] PEG_TXN8	PEG_TXP8 / PEG_TXN8	P35 / N36	PCIE_RX7P / PCIE_RX7N	PCIE_TX7P / PCIE_TX7N	P30 / P29	CPEG_RXP8 / CPEG_RXN8	C91 / C87	EV@0.1u/10V_4	PEG_RXP8 [4] / PEG_RXN8 [4]
[4] PEG_TXP7 / [4] PEG_TXN7	PEG_TXP7 / PEG_TXN7	N38 / M37	PCIE_RX8P / PCIE_RX8N	PCIE_TX8P / PCIE_TX8N	N33 / N32	CPEG_RXP7 / CPEG_RXN7	C86 / C80	EV@0.1u/10V_4	PEG_RXP7 [4] / PEG_RXN7 [4]
[4] PEG_TXP6 / [4] PEG_TXN6	PEG_TXP6 / PEG_TXN6	M35 / L36	PCIE_RX9P / PCIE_RX9N	PCIE_TX9P / PCIE_TX9N	N30 / N29	CPEG_RXP6 / CPEG_RXN6	C79 / C75	EV@0.1u/10V_4	PEG_RXP6 [4] / PEG_RXN6 [4]
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[4] PEG_TXP4 / [4] PEG_TXN4	PEG_TXP4 / PEG_TXN4	K35 / J36	PCIE_RX11P / PCIE_RX11N	PCIE_TX11P / PCIE_TX11N	L30 / L29	CPEG_RXP4 / CPEG_RXN4	C67 / C63	EV@0.1u/10V_4	PEG_RXP4 [4] / PEG_RXN4 [4]
[4] PEG_TXP3 / [4] PEG_TXN3	PEG_TXP3 / PEG_TXN3	J38 / H37	PCIE_RX12P / PCIE_RX12N	PCIE_TX12P / PCIE_TX12N	K33 / K32	CPEG_RXP3 / CPEG_RXN3	C59 / C61	EV@0.1u/10V_4	PEG_RXP3 [4] / PEG_RXN3 [4]
[4] PEG_TXP2 / [4] PEG_TXN2	PEG_TXP2 / PEG_TXN2	H35 / G36	PCIE_RX13P / PCIE_RX13N	PCIE_TX13P / PCIE_TX13N	J33 / J32	CPEG_RXP2 / CPEG_RXN2	C56 / C58	EV@0.1u/10V_4	PEG_RXP2 [4] / PEG_RXN2 [4]
[4] PEG_TXP1 / [4] PEG_TXN1	PEG_TXP1 / PEG_TXN1	G38 / F37	PCIE_RX14P / PCIE_RX14N	PCIE_TX14P / PCIE_TX14N	K30 / K29	CPEG_RXP1 / CPEG_RXN1	C50 / C48	EV@0.1u/10V_4	PEG_RXP1 [4] / PEG_RXN1 [4]
[4] PEG_TXP0 / [4] PEG_TXN0	PEG_TXP0 / PEG_TXN0	F35 / E37	PCIE_RX15P / PCIE_RX15N	PCIE_TX15P / PCIE_TX15N	H33 / H32	CPEG_RXP0 / CPEG_RXN0	C55 / C52	EV@0.1u/10V_4	PEG_RXP0 [4] / PEG_RXN0 [4]

PCI EXPRESS INTERFACE

0518 SWAP PCIE for VGA side

CLOCK

[10] CLK_PCIE_VGA — AB35 — PCIE_REFCLKP
[10] CLK_PCIE_VGA# — AA36 — PCIE_REFCLKN

For Broadway, Madison and Park
the PWRGOOD ball must be connecctet to ground

R67 EV@10K_4

AJ21 NC#1
AK21 NC#2
AH16 PWRGOOD

[11] GPU_RST# — AA30 — PERSTB

CALIBRATION

PCIE_CALRP — Y30 — R47 EV@1.27K/F_4
PCIE_CALRN — Y29 — R46 EV@2K/F_4 — +1V

+1.0V

For M97, Broadway, Madison and Park PCIE_VDDC is 1.0V

SP@Capilano/Robson

Madison	AJ007720T02
Park	AJ077400T08

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GPU_2(VGA)

GPU Power-on sequence

1 => +VGPU_CORE
2 => +VGPU_IO
3 => +1V
4 => +1.5V_GPU
5 => +3V_D
6 => +1.8V_GPU
7 => dGPU_PWROK

1.8V GPIO

3.3V GPIO

NC on Park

NC on Park

Channel D N.C for Park-M2

DAC2 will be NC on future ASIC

REV C: C188 change footprint from 0603 to 0805

HDMI

DDC AUX4 NC for Park_M2

LVDS

CRT

DDC AUX7 NC for Park_M2

SP@Capilano/Robson

SP@Capilano/Robson

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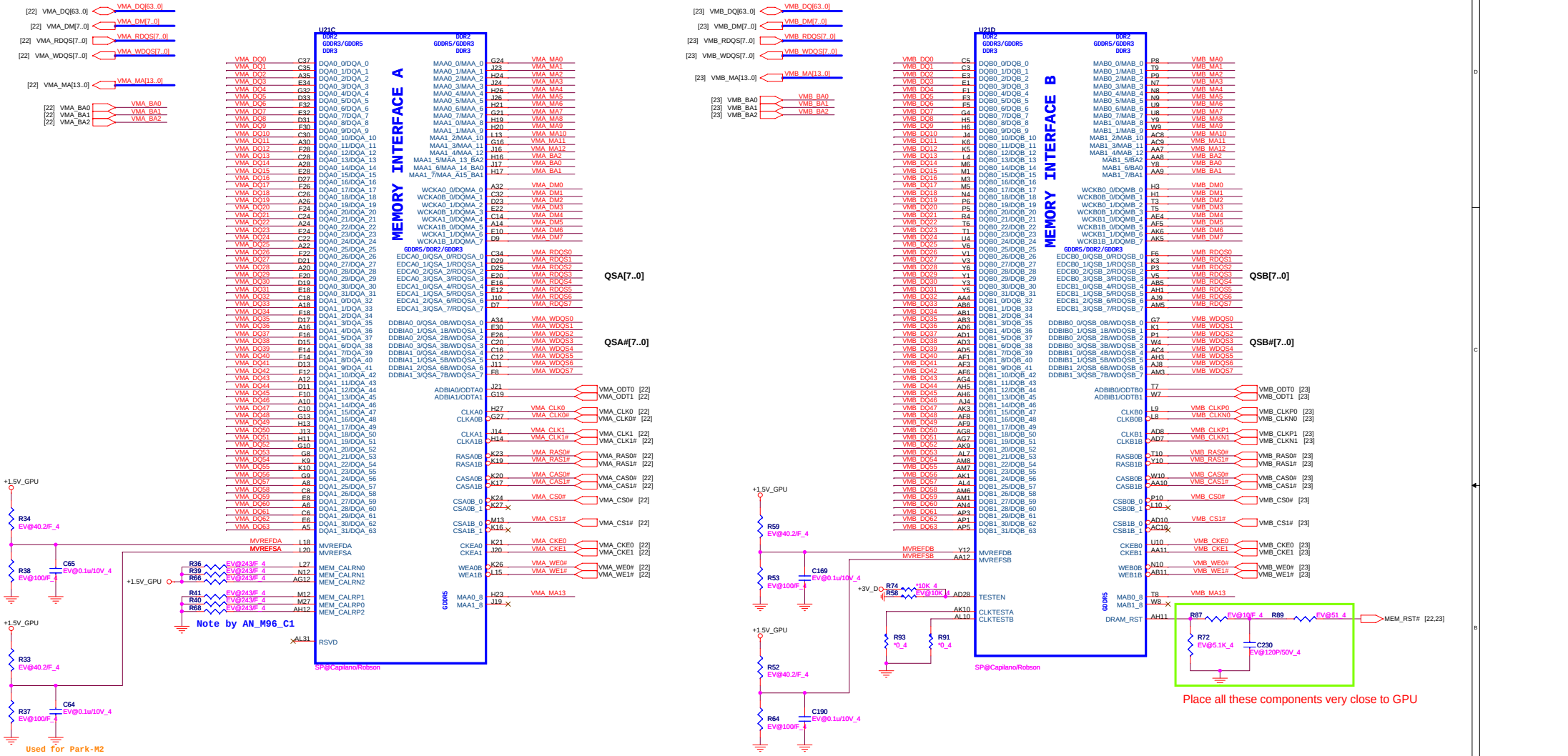
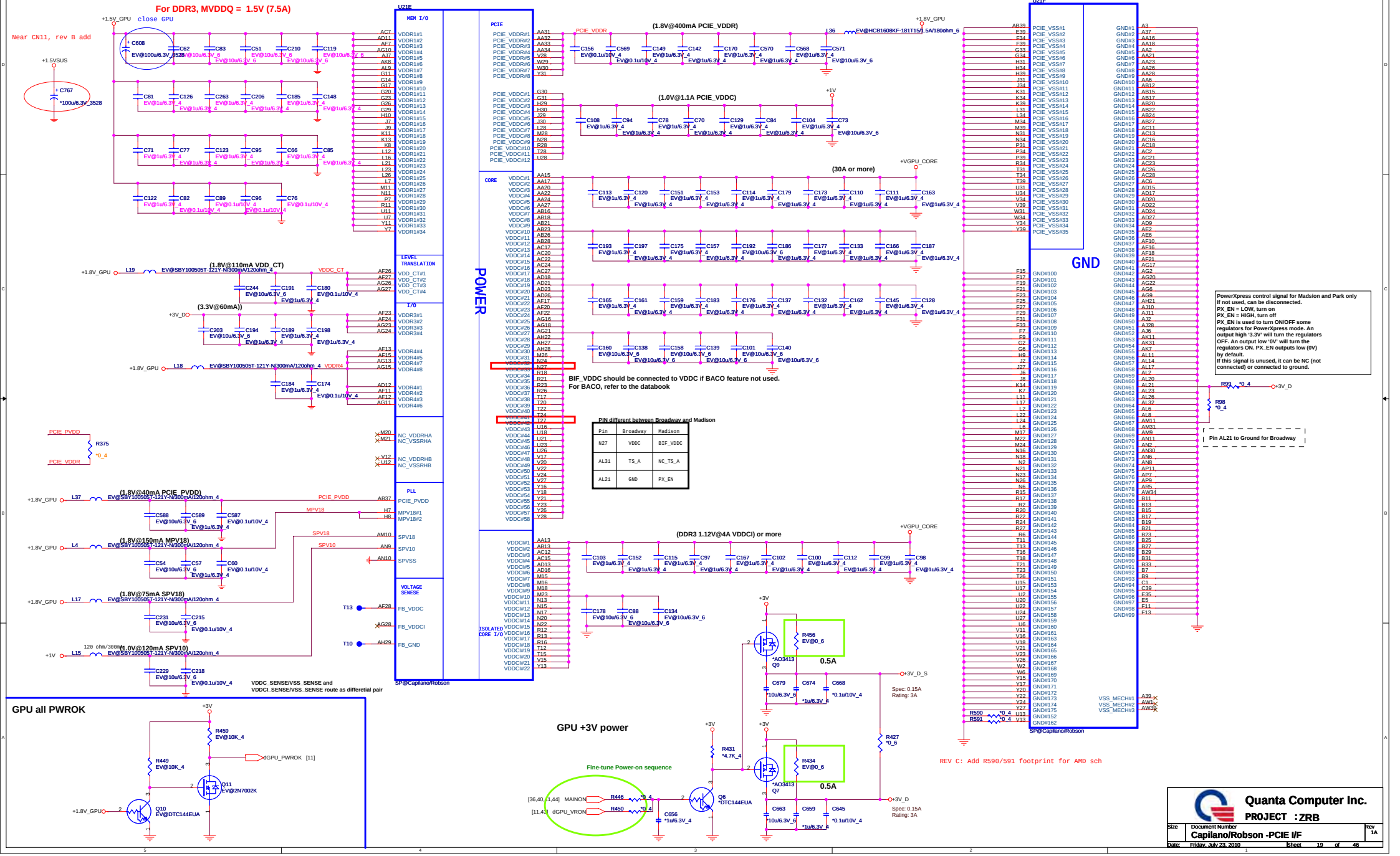
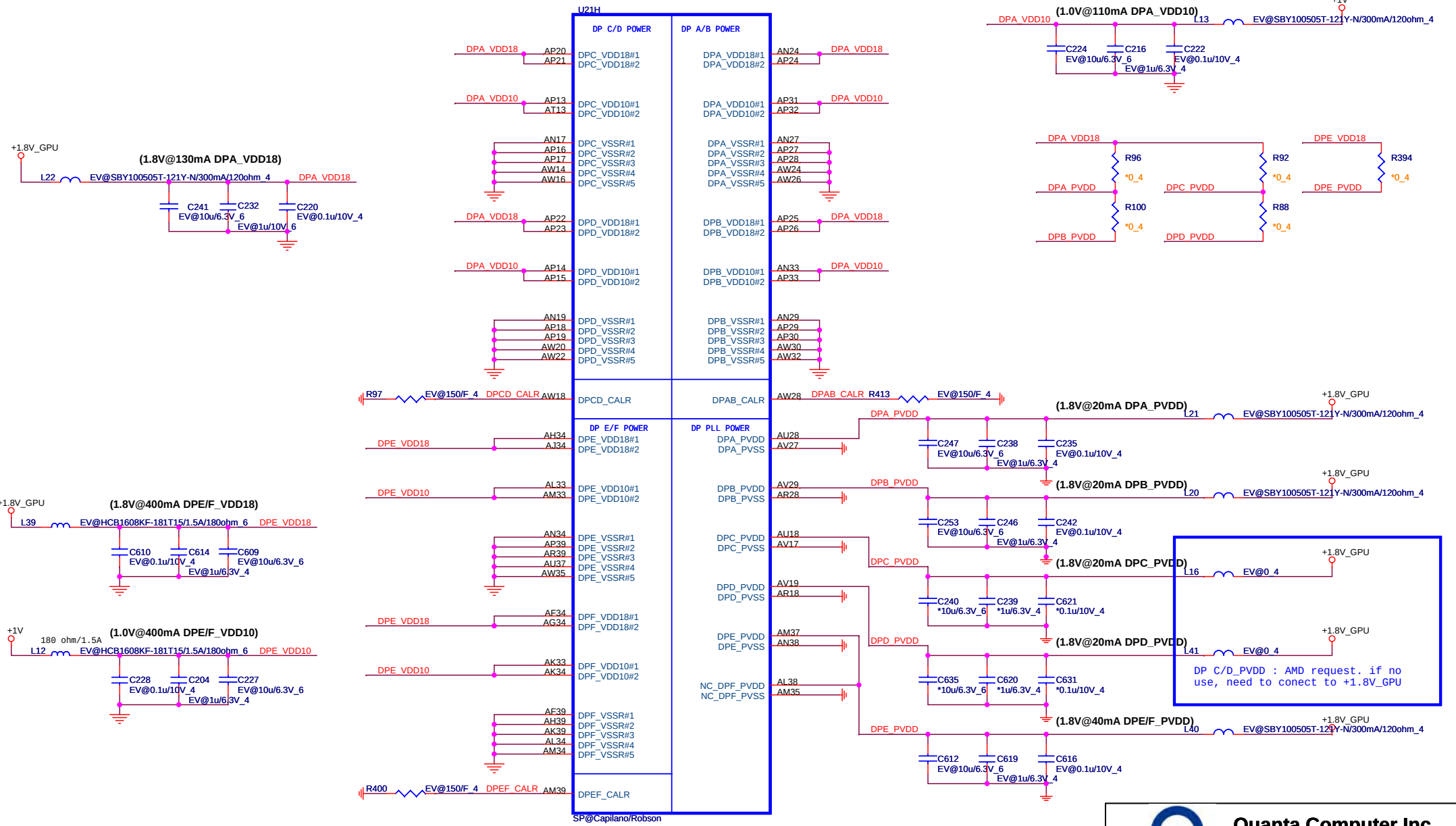
Park M2-channel B used(S3 package use Channel A)



GPU_4(VGA)



GPU_5(VGA)



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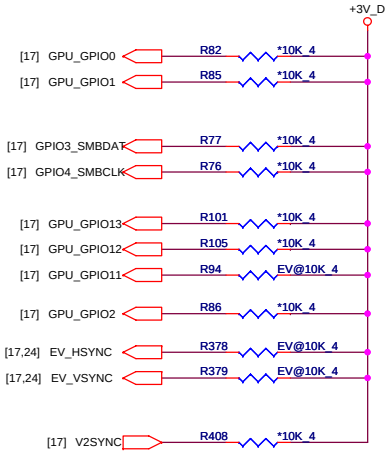
PIN STRAPS(VGA)



Size of the primary memory apertures	GPIO[13:11]
128 MB	000
256MB	001
64 MB	010
32 MB	011
More than 512 MB	Not Supported

CONFIGURATION STRAPS

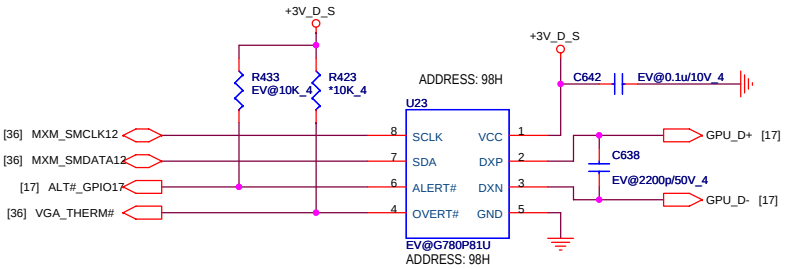
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0	
ROMIDCFG[2:0]	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	001	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

Thermal Sensor(VGA)

Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

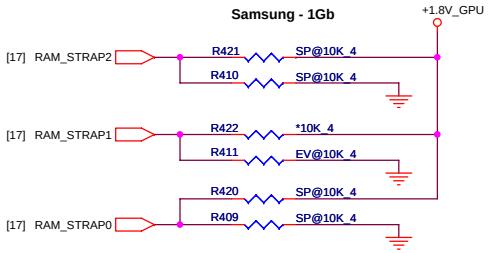
USD0.16



DDR3 Memory Aperture size(GPU)

DDR3 Memory size

Vendor	Vendor P/N	STN B/S P/N	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix			1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1	0	0
	H5TQ2G63BFR-12C	AKD5MGGTW03 (128M*16)	1	0	1
Samsung					
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500 (128m*16)	0	0	1
AMD	23EY2387MA12-SZ	AKD5LGGT700	0	1	0

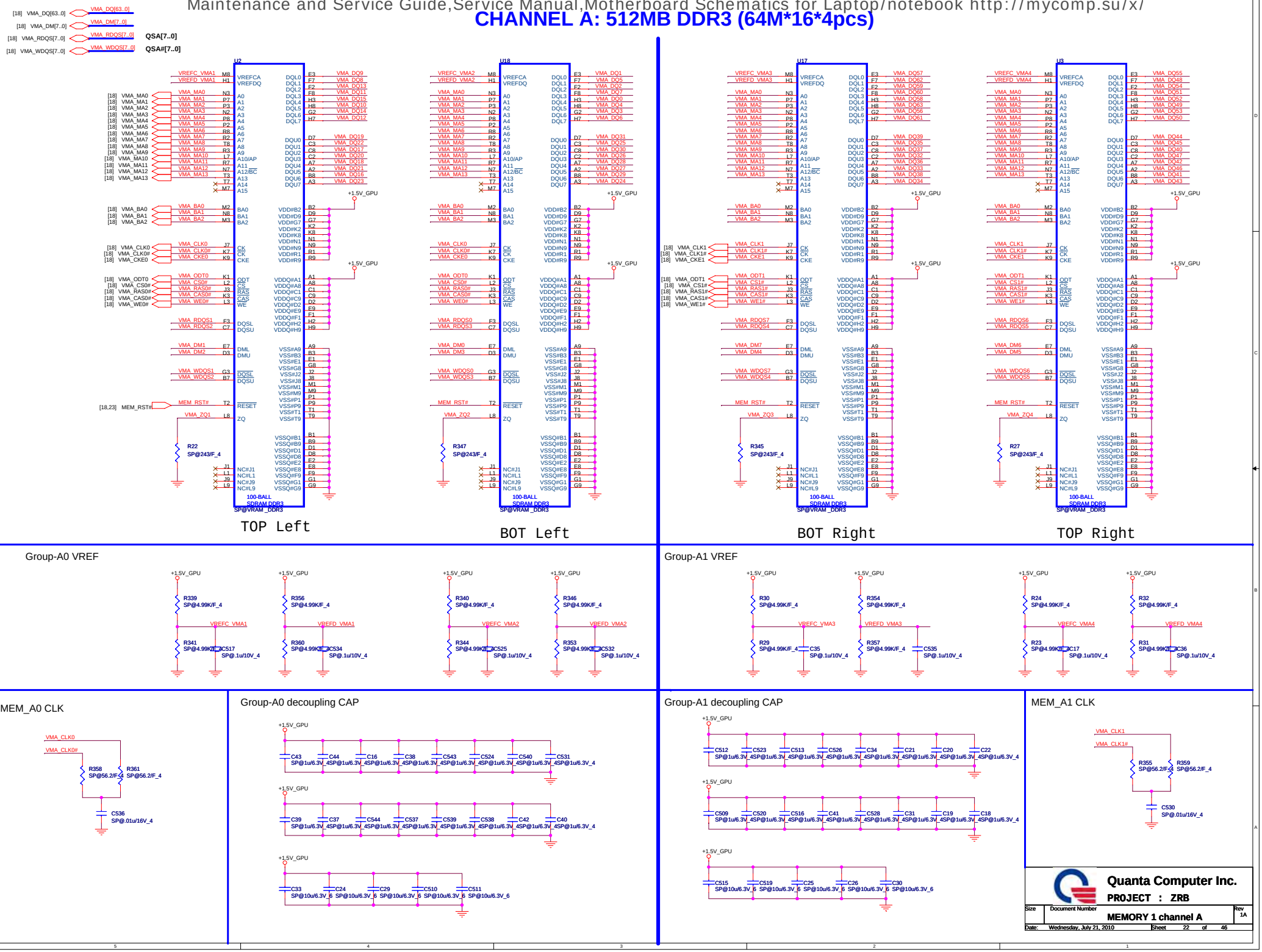


RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

Quanta Computer Inc.
PROJECT : ZRB

Size	Document Number	Rev
	Strip/Thermal	1A
Date: Wednesday, July 21, 2010	Sheet 21 of 46	

CHANNEL A: 512MB DDR3 (64M*16*4pcs)



CHANNEL B: 512MB DDR3 (16*64M*4pcs)

Park, M92M Use Channel B Memory Interface Only

[18] VMB_DQ[63..0] — VMB_DQ[63..0]
[18] VMB_DM[7..0] — VMB_DM[7..0]
[18] VMB_RDQS[7..0] — VMB_RDQS[7..0] — QSA[7..0]
[18] VMB_WDQS[7..0] — VMB_WDQS[7..0] — QSA#[7..0]

BOT Down

TOP Down

TOP Up

BOT Up

Group-B0 VREF

+1.5V_GPU
R368 EV@4.99K/F_4 — VREFC_VMB1 — R363 EV@4.99K/F_4 — C547 EV@0.1u/10V_4
R42 EV@4.99K/F_4 — VREFD_VMB1 — R43 EV@4.99K/F_4 — C127 EV@0.1u/10V_4
R372 EV@4.99K/F_4 — VREFC_VMB2 — R371 EV@4.99K/F_4 — C554 EV@0.1u/10V_4
R367 EV@4.99K/F_4 — VREFD_VMB2 — R364 EV@4.99K/F_4 — C549 EV@0.1u/10V_4

Group-B1 VREF

+1.5V_GPU
R107 EV@4.99K/F_4 — VREFC_VMB3 — R108 EV@4.99K/F_4 — C260 EV@0.1u/10V_4
R377 EV@4.99K/F_4 — VREFD_VMB3 — R376 EV@4.99K/F_4 — C572 EV@0.1u/10V_4
R80 EV@4.99K/F_4 — VREFC_VMB4 — R79 EV@4.99K/F_4 — C207 EV@0.1u/10V_4
R106 EV@4.99K/F_4 — VREFD_VMB4 — R104 EV@4.99K/F_4 — C259 EV@0.1u/10V_4

MEM_B0 CLK

VMB_CLKP0
VMB_CLKN0
R365 EV@56.2/F_4 — R366 EV@56.2/F_4
C545 EV@0.01u/16V_4

Group-B0 decoupling CAP

+1.5V_GPU
C557 C565 C550 C556 C558 C49 C261 C559 — EV@1u/6.3V_4
C555 C264 C46 C121 C566 C125 C45 C262 — EV@1u/6.3V_4
C564 C90 C551 C552 C561 — EV@10u/6.3V_6

Group-B1 decoupling CAP

+1.5V_GPU
C265 C47 C53 C258 C574 C124 C236 C630 — EV@1u/6.3V_4
C548 C252 C629 C243 C573 C560 C233 C546 — EV@1u/6.3V_4
C632 C118 C219 C634 C633 — EV@10u/6.3V_6

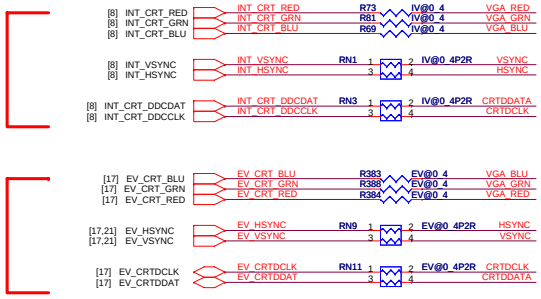
MEM_B1 CLK

VMB_CLKP1
VMB_CLKN1
R415 EV@56.2/F_4 — R416 EV@56.2/F_4
C637 EV@0.01u/16V_4

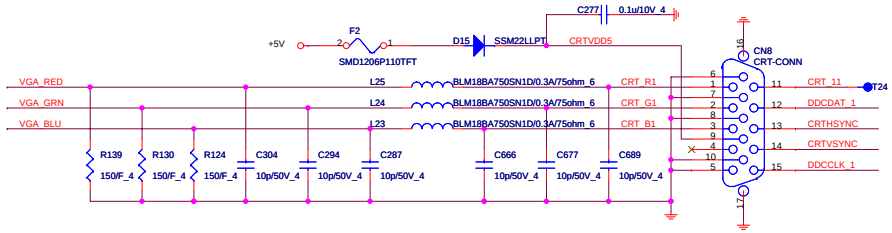
Quanta Computer Inc.
PROJECT : ZRB
Size | Document Number: MEMORY 2 channel B | Rev 1A
Date: Wednesday, July 21, 2010 | Sheet 23 of 46

CRT Switch

0_ohm Resistor place close to Joint-Point

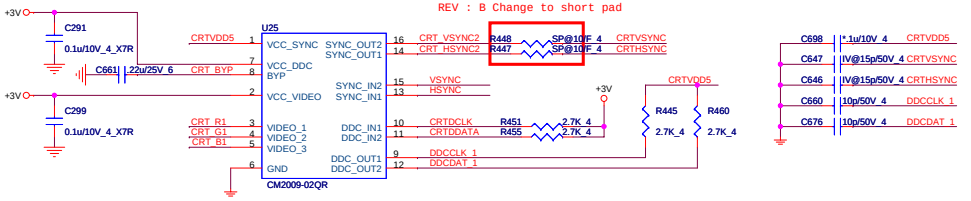


CRT



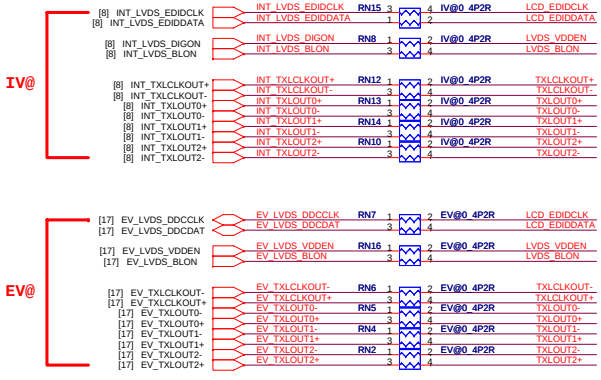
REV : C Change to 0402 R

REV : B Change to short pad



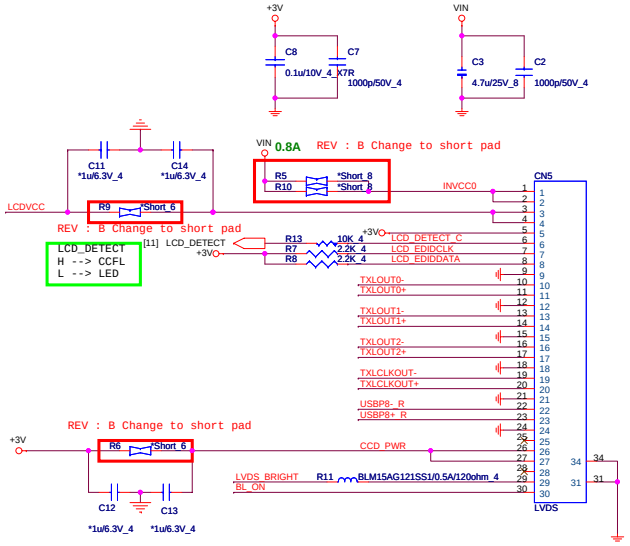
LVDS

0_ohm Resistor place close to Joint-Point

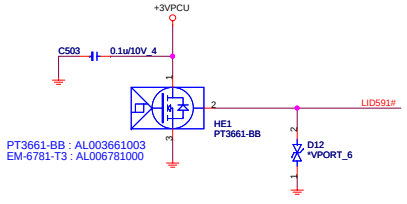


CCD +3V-current budget 0.2A

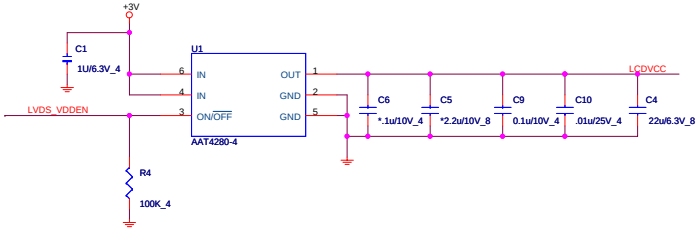
LVDS



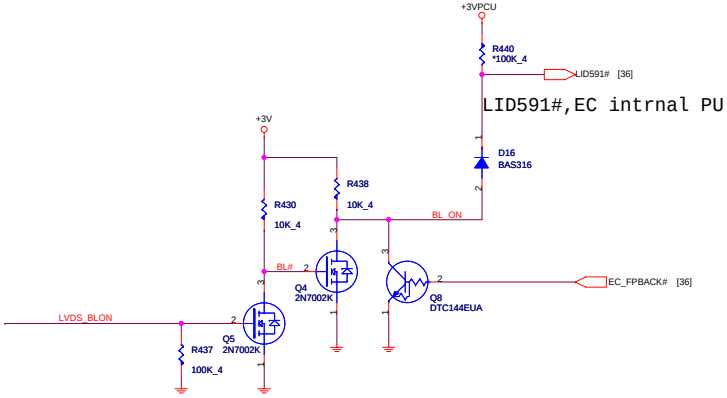
Lid Switch (Hall sensor)



LCD Power



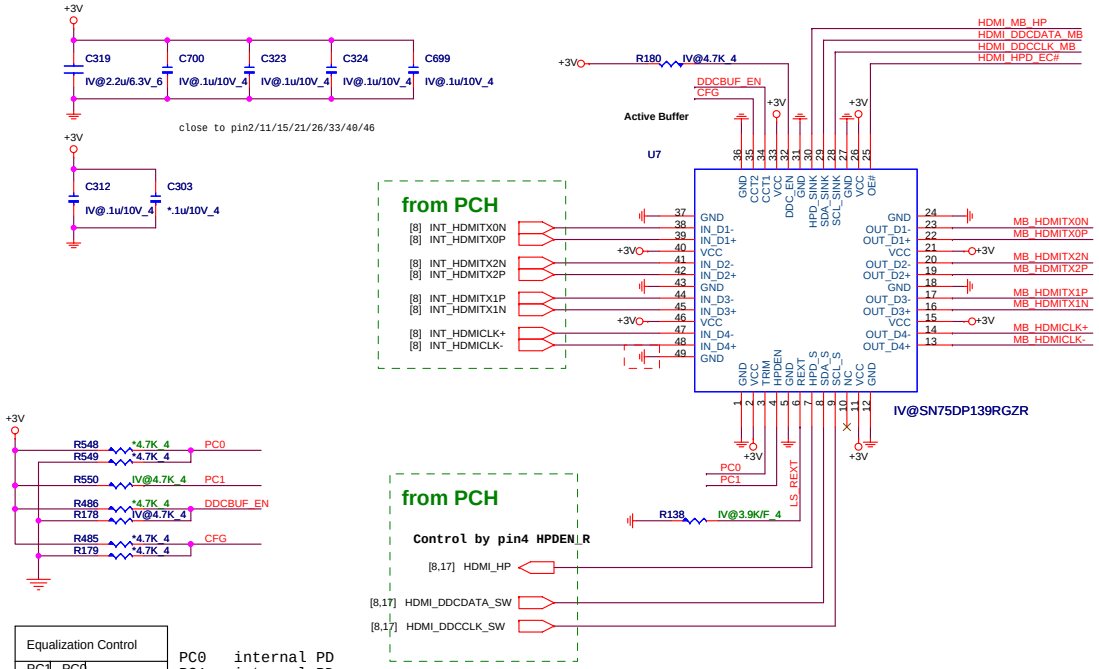
Backlight Control



Quanta Computer Inc. PROJECT : ZRB			
Size	Document Number	CRT/LVDS/CAMERA/LID	Rev 1A
Date: Friday, July 23, 2010		Sheet 24 of 46	

HDMI LEVEL SHIFTER

IV@



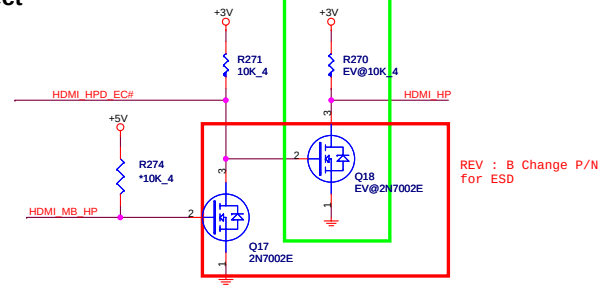
Equalization Control		
PC1 PIN4	PC0 PIN3	EQ Control
L	L	8dB
L	H	4dB
H	L	12dB
H	H	0dB

PC0 internal PD
PC1 internal PD
DDCBUF_EN internal PD
CFG internal PD
DDC_EN internal PU

HDMI-detect

EV@

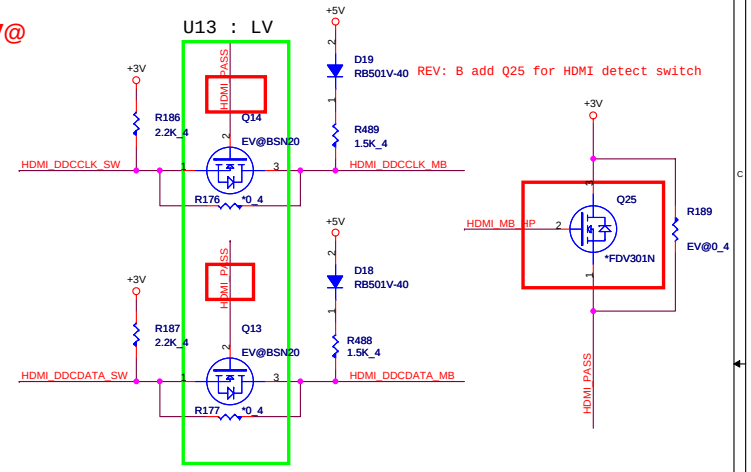
U13 : LV



I2C

EV@

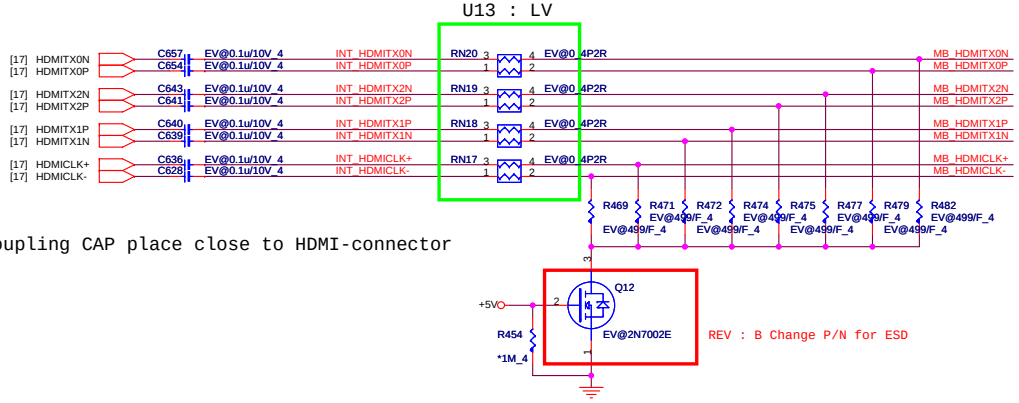
U13 : LV



Switchable Graphic HDMI source

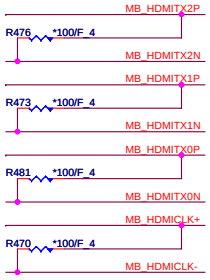
EV@

U13 : LV



AC-coupling CAP place close to HDMI-connector

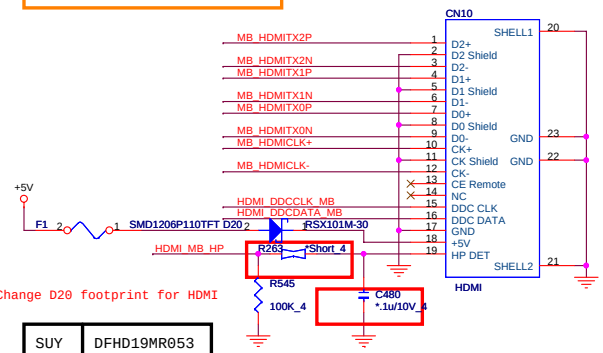
EMI



REV C: Change D20 footprint for HDMI

HDMI connector

REV : C Location :D20 Change Footprint & P/N



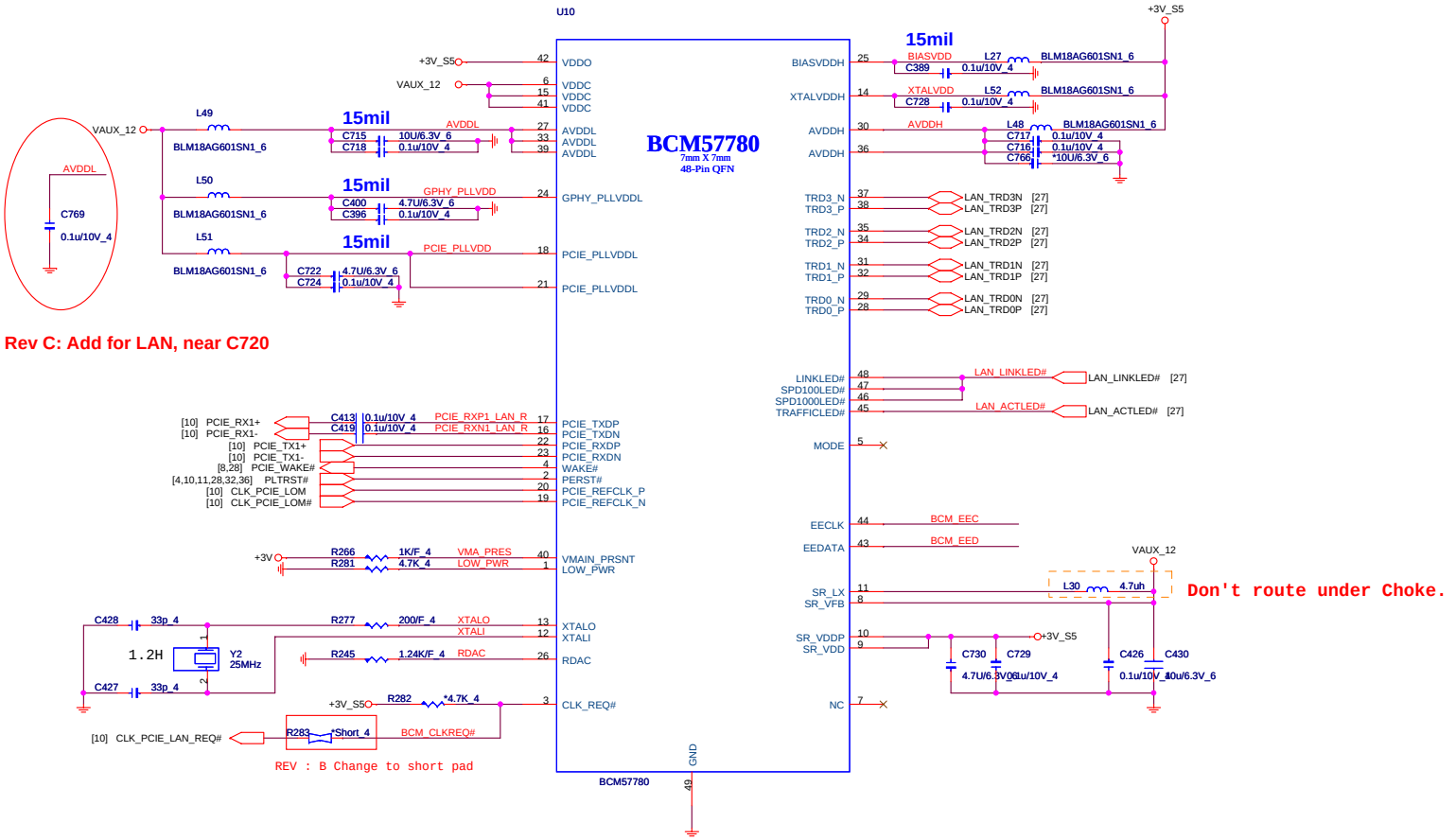
REV : B Change to short pad and add C480

SUY	DFHD19MR053
LTS	DFHD19MR085

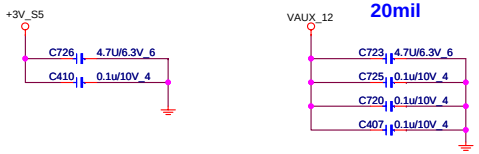
Quanta Computer Inc.
PROJECT : ZRB

Size	Document Number	Rev
	HDMI (PS8101)	1A
Date: Friday, July 23, 2010	Sheet 25 of 46	

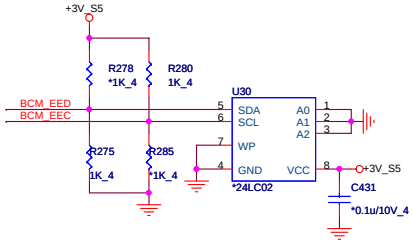
Giga-LAN BCM57780



LAN POWER



EEPROM



EEPROM Strapping

EEPROM Type	EECLK	EEDATA
24LC02	1	1
Internal	1	0

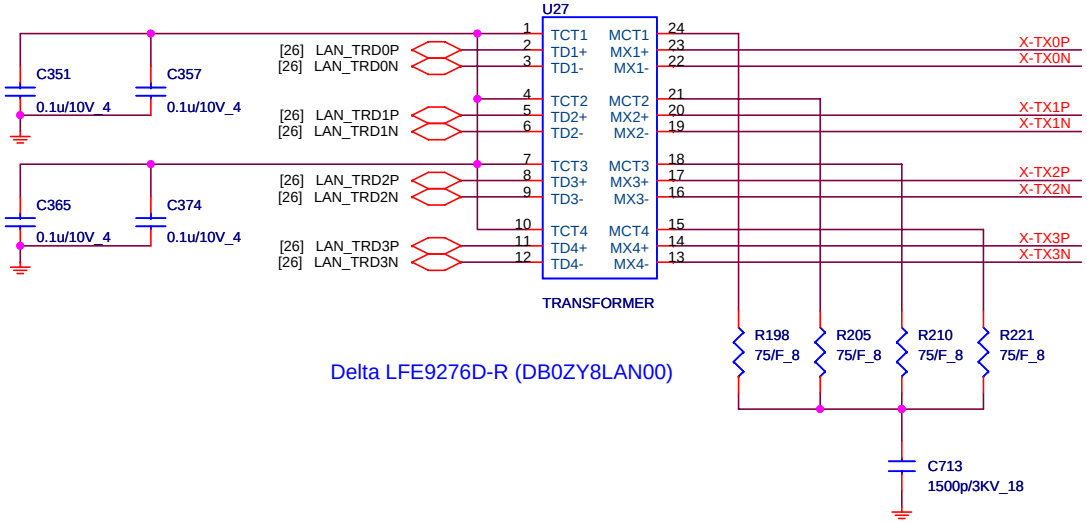
Quanta Computer Inc.
PROJECT : ZRB

Size	Document Number	Rev
	GLAN BCM57780	1A

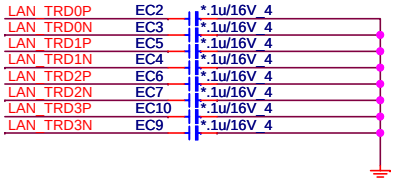
Date: Friday, July 23, 2010 Sheet 26 of 46

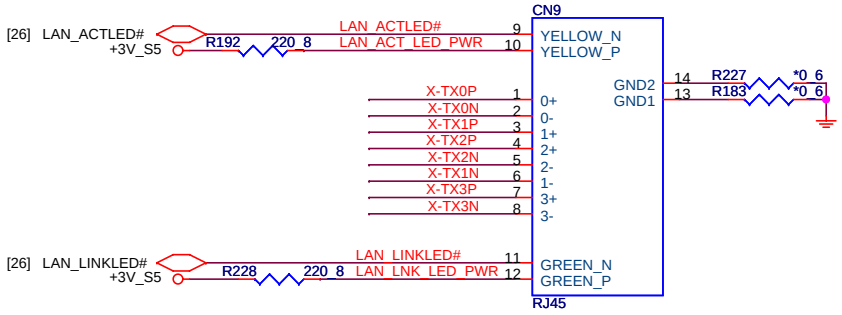
TRANSFORMER

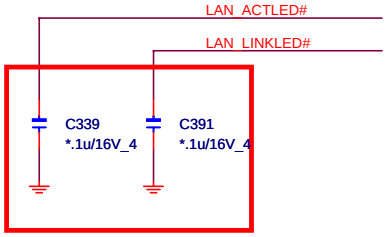
SUY	DFTJ12FR109
AEC	DFTJ12FR135



Delta LFE9276D-R (DB0ZY8LAN00)







REV : B Change to 0402 for ESD

Quanta Computer Inc.

PROJECT : ZRB

Size	Document Number	Rev
	LAN Transformer and RJ45	1A

Date: Thursday, July 22, 2010 Sheet 27 of 46

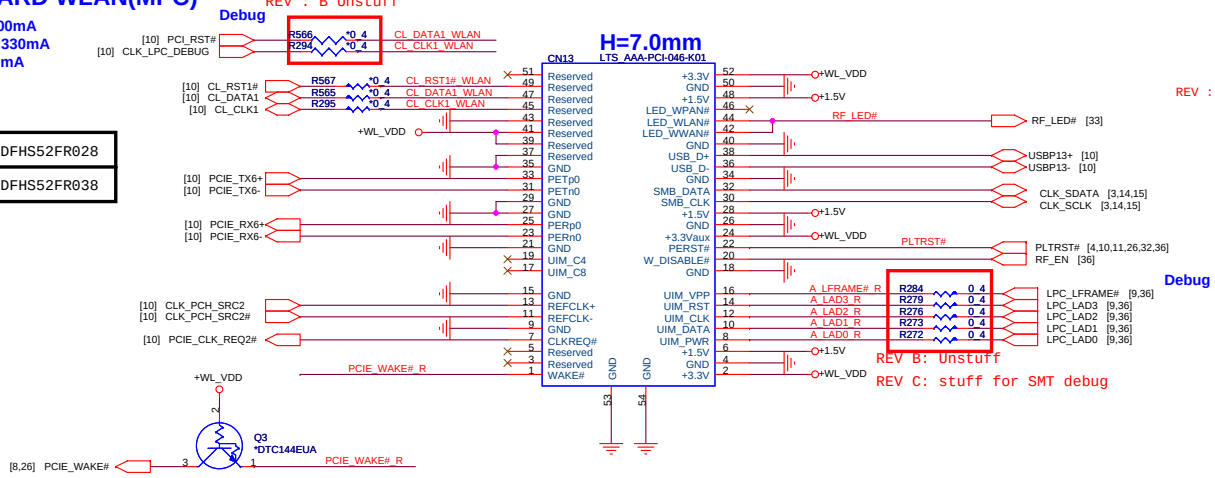
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

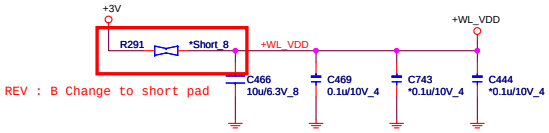
REV : B Unstuff

Debug

PTI	DFHS52FR028
LTS	DFHS52FR038

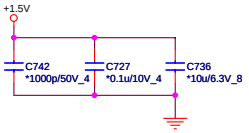


REV B: Unstuff
REV C: stuff for SMT debug



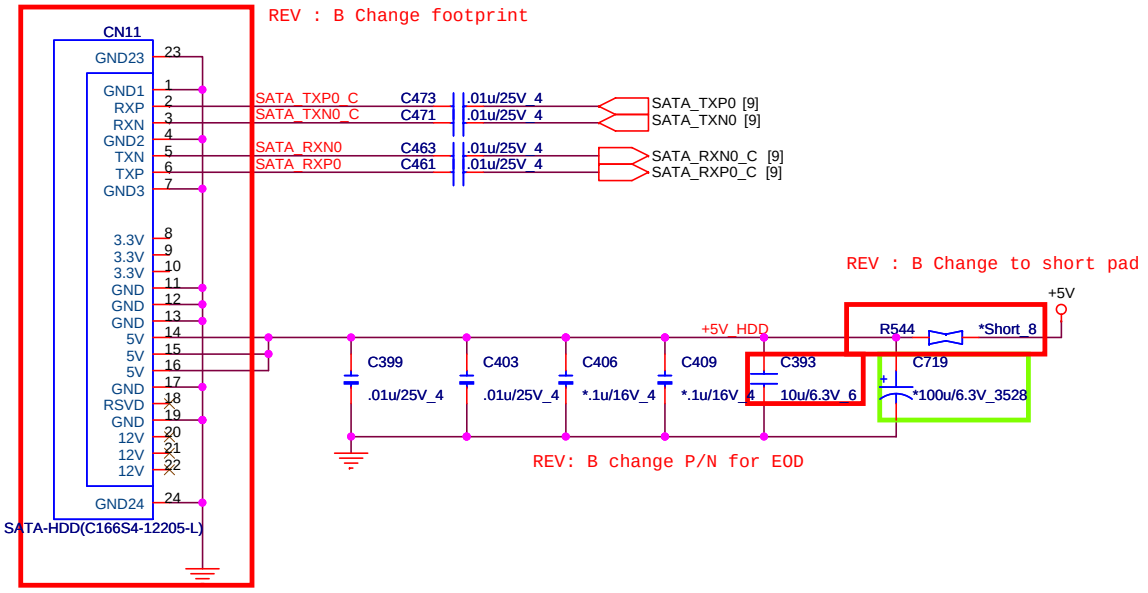
REV : B Change to short pad

Debug

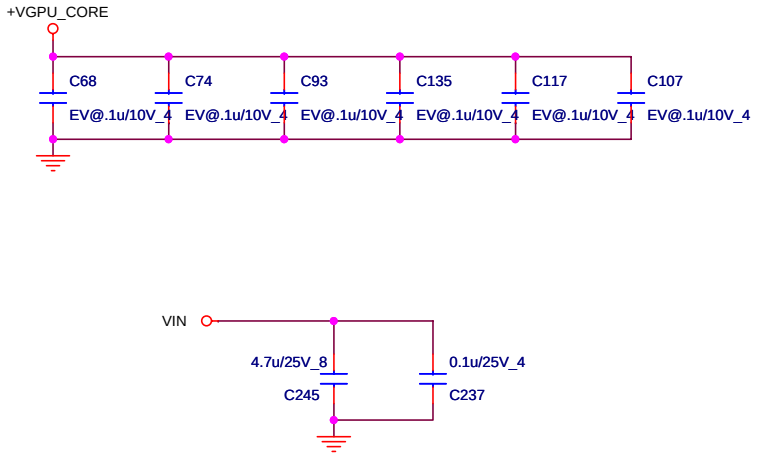


Quanta Computer Inc.			
PROJECT : ZRB			
Size	Document Number	MINI PCI-E card/TV	Rev 1A
Date: Friday, July 23, 2010		Sheet 28 of 46	

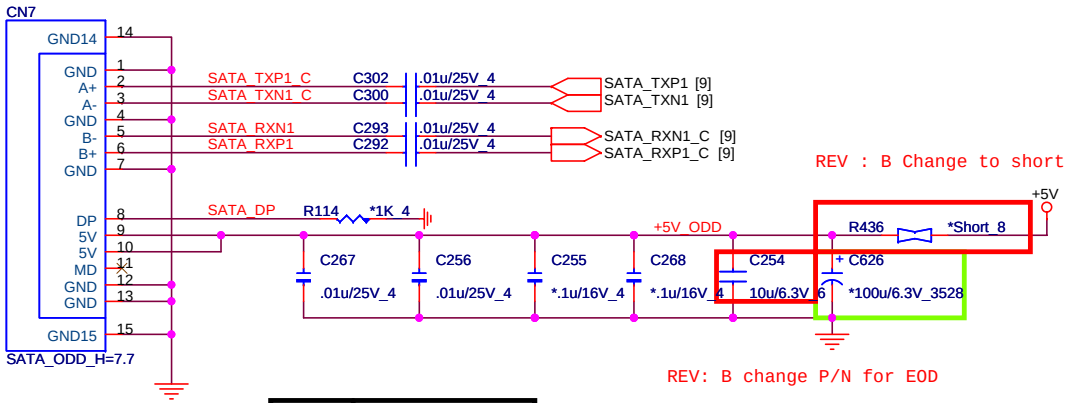
MAIN SATA HDD



EE RETURN-PATH CAPACITORS



ODD (SATA)



SUY	DFHS22FR214
AOP	DFHS22FR232
AEC	DFHS22FR216

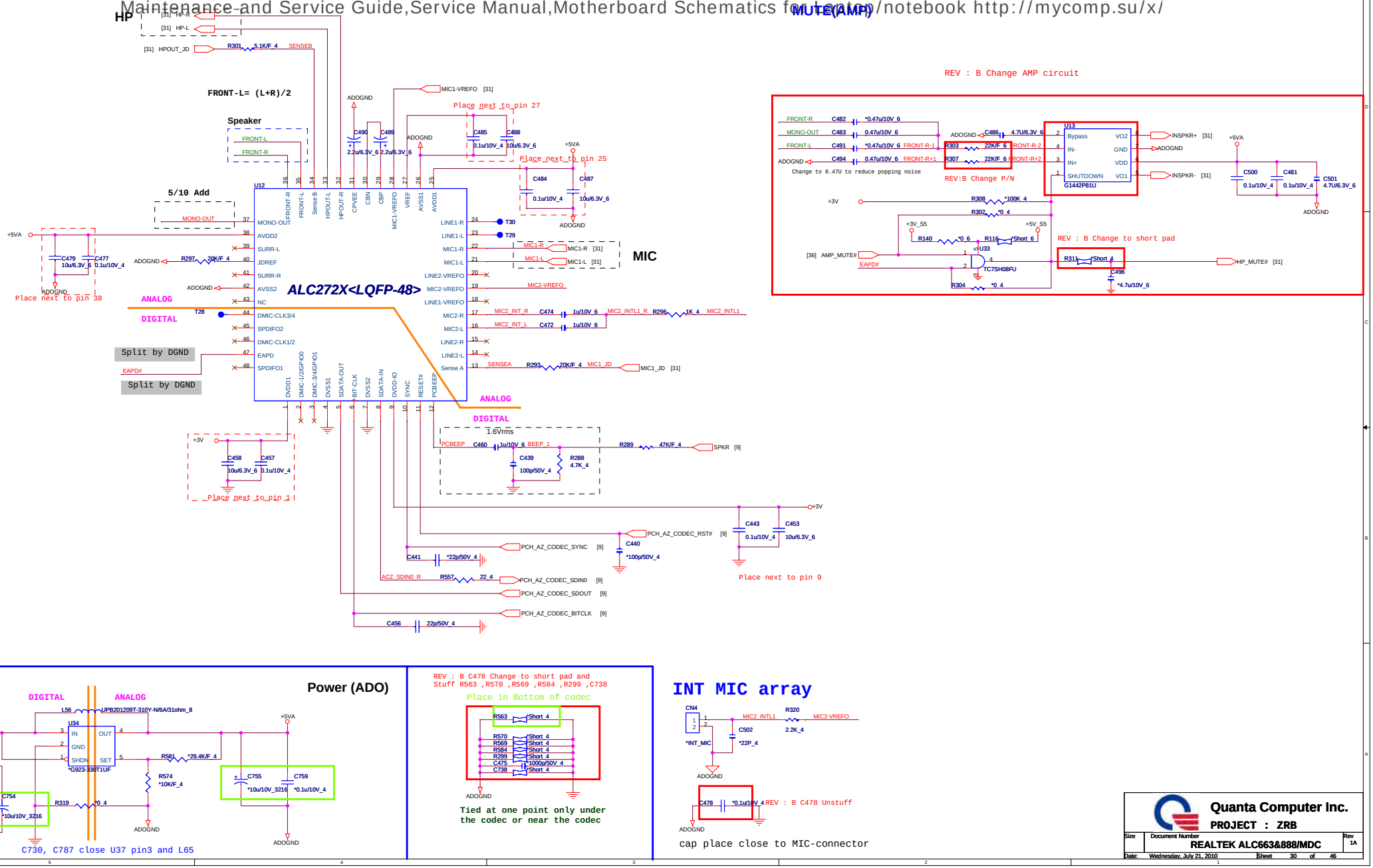
AOP	DFHS13FR011
OTK	DFHS13FR010

Quanta Computer Inc.

PROJECT : ZRB

Size	Document Number	Rev
	SATA-HDD/ODD/RETURN-PATH	1A
Date: Wednesday, July 21, 2010	Sheet 29 of 46	

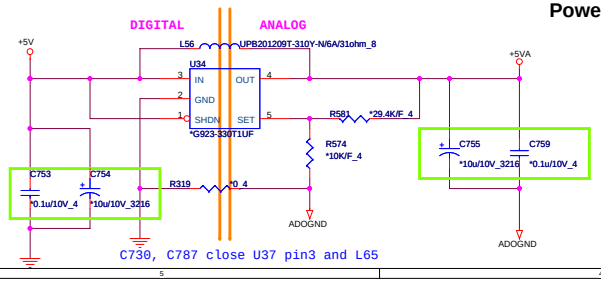
Codec(ADO)



MUTE(AMP)

REV : B Change AMP circuit

Power (ADO)



REV : B C478 Change to short pad and Stuff R563 ,R570 ,R569 ,R584 ,R299 ,C738

Place in Bottom of codec

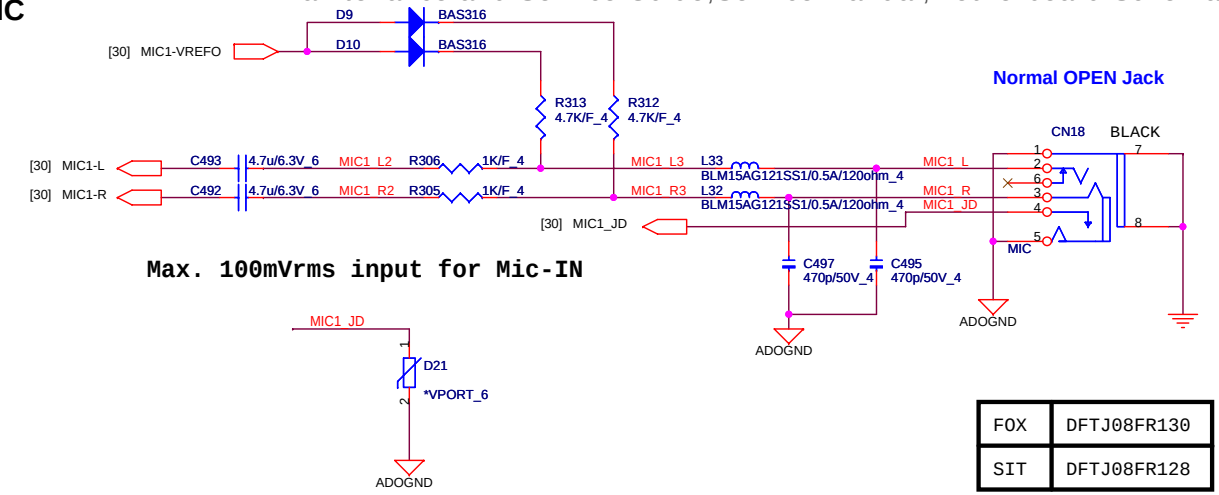
Tied at one point only under the codec or near the codec

INT MIC array

cap place close to MIC-connector

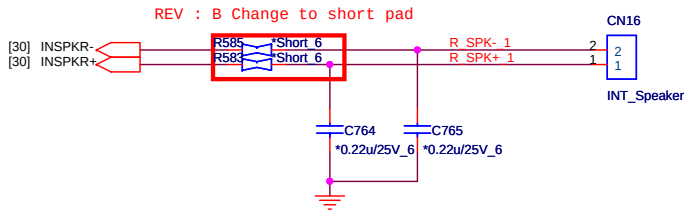
Quanta Computer Inc.		
PROJECT : ZRB		
Size	Document Number: REALTEK ALC663&888/MDC	Rev: 1A
Date: Wednesday, July 21, 2010	Sheet 30 of 46	

MIC



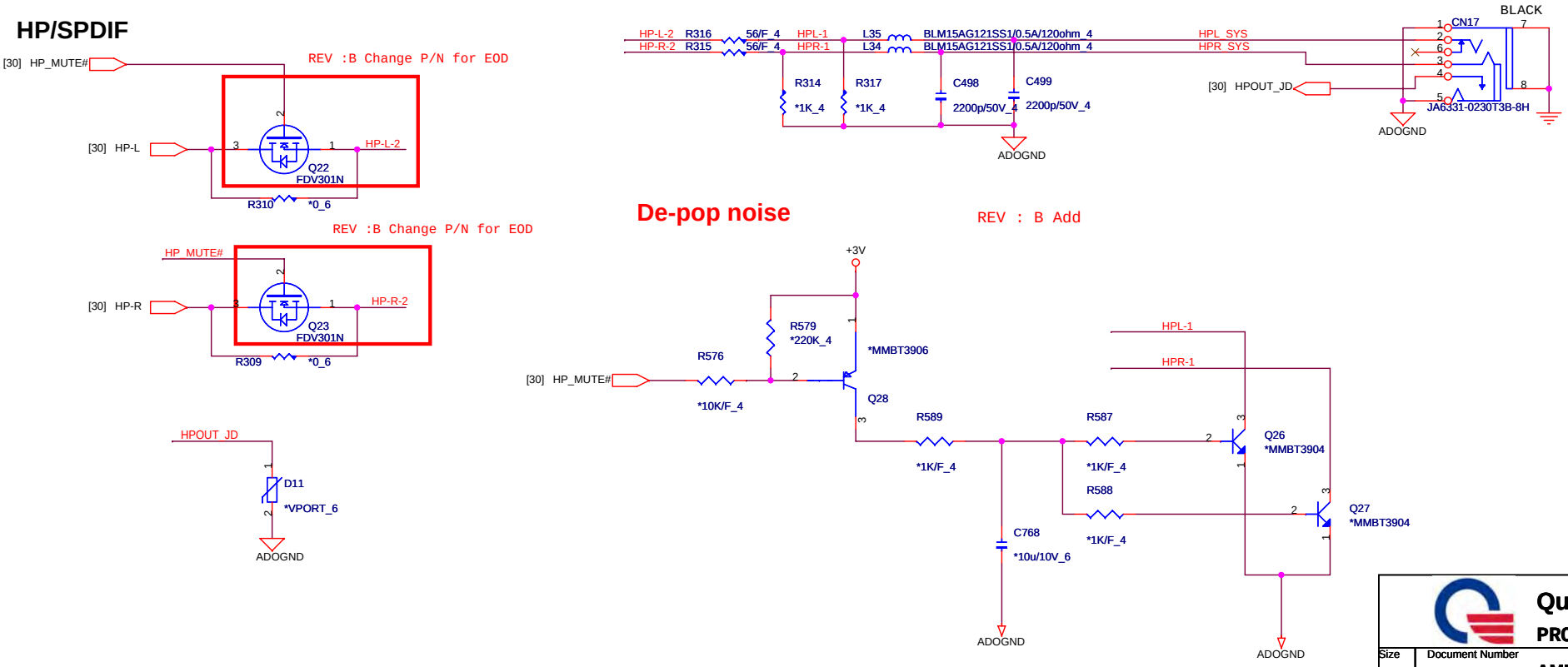
FOX	DFTJ08FR130
SIT	DFTJ08FR128

Internal Speaker



ACS	DFHD02MR311
PTI	DFHD02MR508

HP/SPDIF



Quanta Computer Inc.

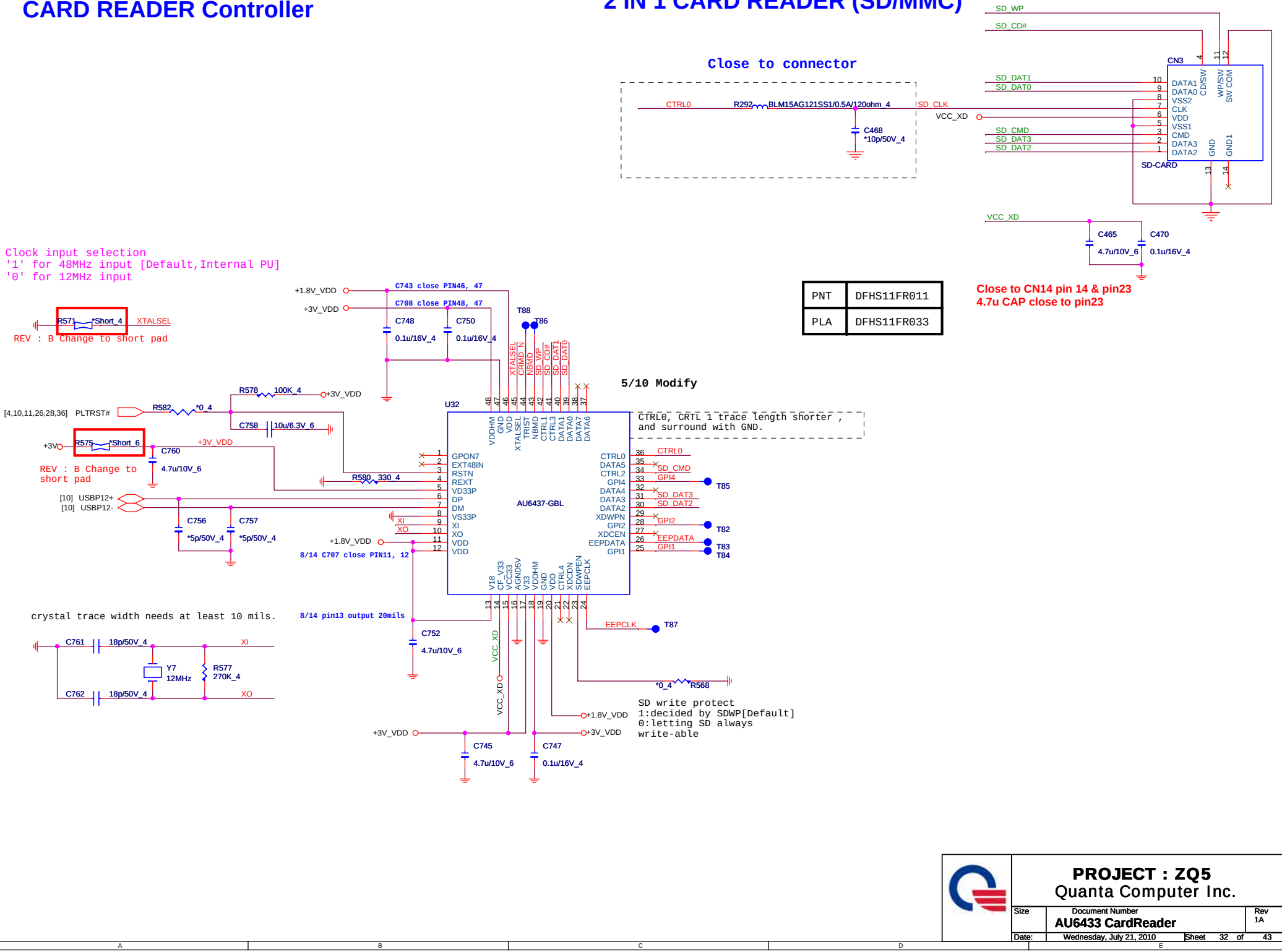
PROJECT : ZRB

Size	Document Number	Rev
	AMP /AUDIO JACK CONN	1A

Date: Wednesday, July 21, 2010 Sheet 31 of 46

CARD READER Controller

2 IN 1 CARD READER (SD/MMC)

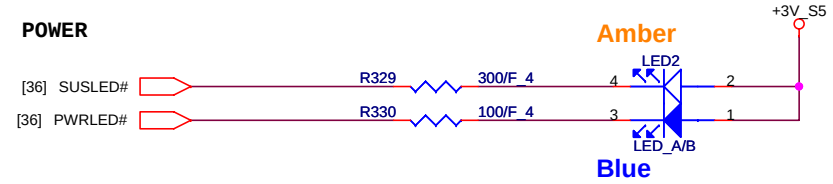


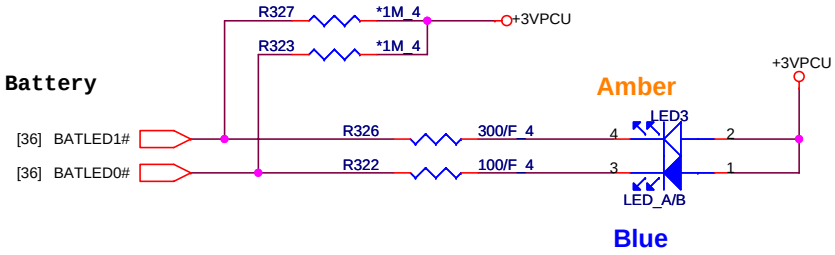
PNT	DFHS11FR011
PLA	DFHS11FR033

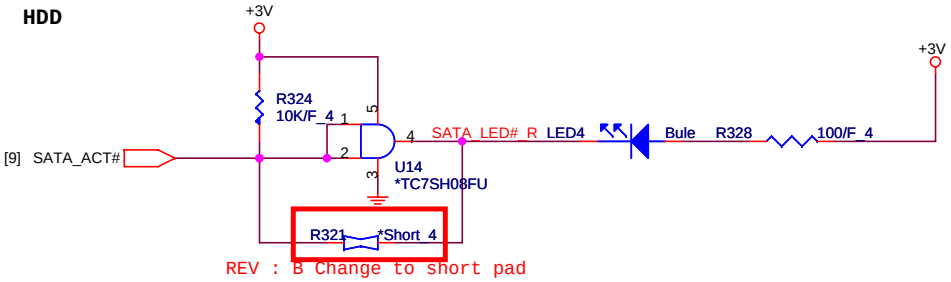
PROJECT : ZQ5
Quanta Computer Inc.

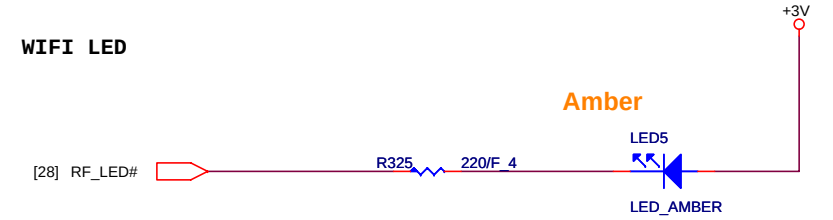
Size	Document Number	Rev
	AU6433 CardReader	1A
Date:	Wednesday, July 21, 2010	Sheet 32 of 43

LED



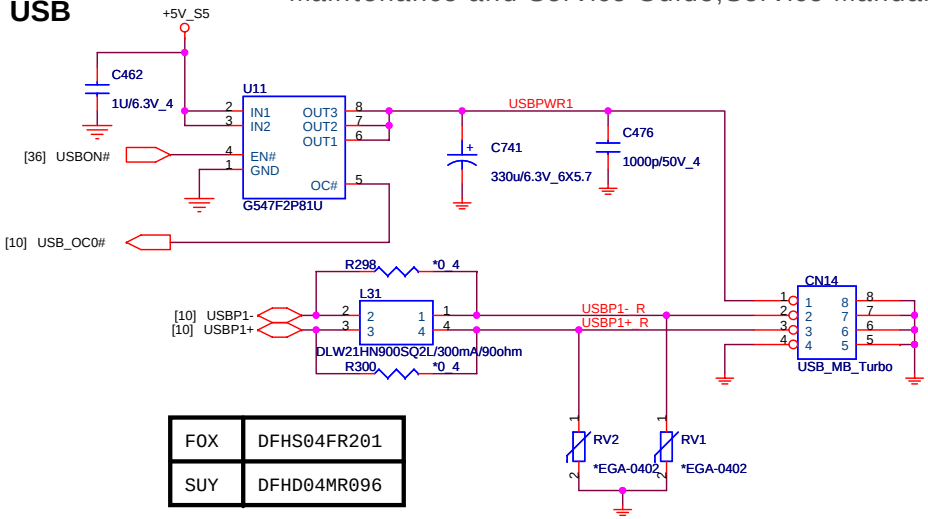






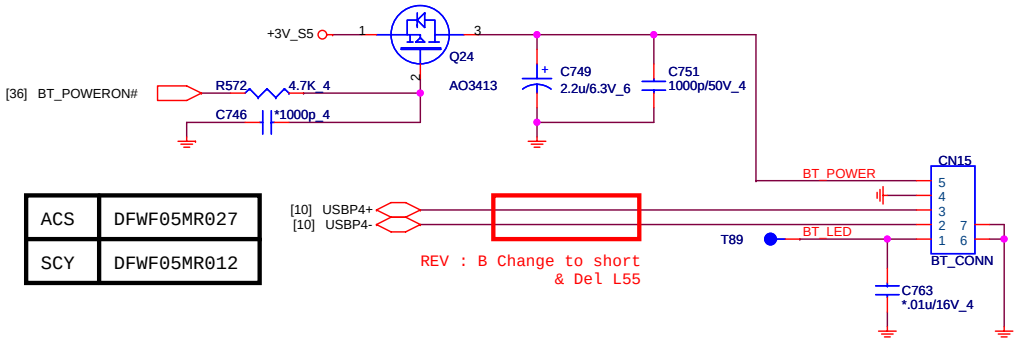
Quanta Computer Inc.		
PROJECT : ZRB		
Size	Document Number: POWER/MMB/LAUNCH/LED	Rev: 1A
Date: Monday, July 26, 2010	Sheet 33 of 46	

USB



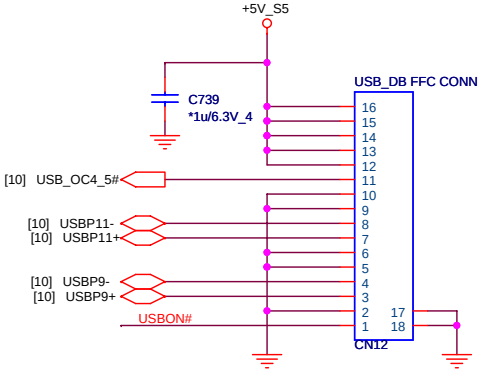
FOX	DFHS04FR201
SUY	DFHD04MR096

BLUETOOTH CONNECTOR



ACS	DFWF05MR027
SCY	DFWF05MR012

USB/B



Quanta Computer Inc.

PROJECT : ZRC

Size	Document Number	Rev
	USB/ BT	1A

Date: Friday, July 23, 2010 Sheet 34 of 46

K/B

PTI	DFFC26FR155
ACS	DFFC26FR014

CP1 CP2 CP6 CP5 CP4 CP3 *100p/50Vx4
C541 *100p/50V_4
C542 *100p/50V_4

CN1 KB

RP3 10K_10P8R

+3VPCU

CPU FAN

ACS	DFWF03MS091
SCY	DFWF03MS000

U20 G995
C567 2.2U_6
C562 2.2U_6
C563 .01U_4
C553 *.01U_4
R369 10K_4
CN6 FAN_CONN
TH_FAN_POWER
[36] FANSIG
[10,11,36] SML1ALERT#
[36] CPUFAN#

FANPWR = 1.6*VSET

TOUCHPAD & Switch CONN.

ACS	DFFC12FR017
SCY	DFFC12FR015
PTI	DFFC12FR234

REV : B Change to short pad

R44 10K_4
R45 10K_4
L5 *Short_6
L6 *Short_6
L7 *Short_6
C150 0.1u/10V_4
C143 *.01u/25V_4
C144 *.01u/25V_4
CN2 Aces 88501-120N
[36] TPDATA
[36] TPCLK
TPDATA_R
TPCLK_R
RIGHT#
LEFT#
SW3 SWITCH_1.5
SW2 SWITCH_1.5

HOLE4 H-C315i154D154P2
HOLE10 H-TC197BC122D122P2
HOLE24 *h-c315in158d118p2
HOLE5 *h-c315d118p2
HOLE7 *h-c315d118p2
HOLE31 *h-c315d118p2
HOLE26 *h-c315d118p2
HOLE30 *h-c315d118p2
HOLE11 H-TC197BC122D122P2
HOLE17 H-TC197BC122D122P2
HOLE13 *h-c315d118p2
HOLE32 *h-c315d118p2
HOLE3 *h-c315d118p2
HOLE16 *h-c315d118p2
HOLE29 *h-c315d118p2
HOLE22 *h-c315d118p2
HOLE18 h-c315d146p2
HOLE25 H-TC315BC146D146P2
HOLE14 *H-TC165BC256D165P2
HOLE21 *H-TC165BC256D165P2
HOLE20 *H-TC165BC256D165P2
HOLE27 h-c197d87p2
HOLE1 h-tc197bc79d79p2
HOLE2 h-tc197bc102d102p2
HOLE9 *h-o315x354d315x354n
HOLE19 *H-TC91BC197D91P2
HOLE15 *H-TC91BC197D91P2
HOLE23 *H-TC91BC197D91P2
HOLE28 *H-TC91BC197D91P2
+1.05V *SPAD1 PAD1
+1.05V *SPAD3 PAD3
HOLE12 *h-c315d118p2
HOLE6 *h-c94d94n
HOLE8 *h-c1417d1417na1457

Quanta Computer Inc.
PROJECT : ZRB

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	KB/FAN/TP+FP	1A
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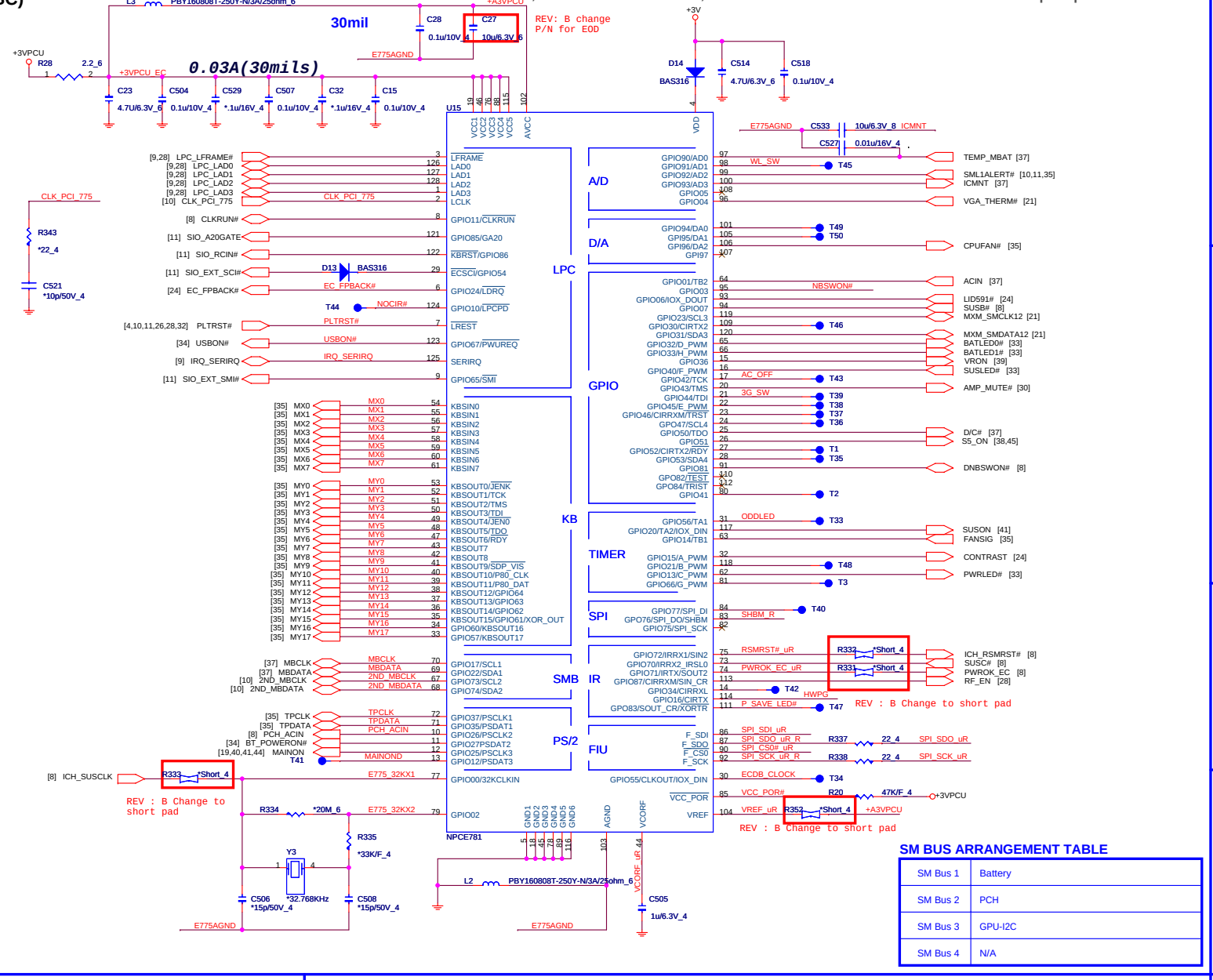
EC(KBC)



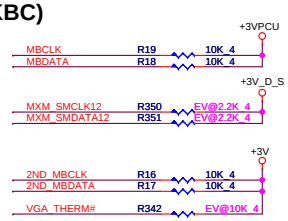
I/O ADDRESS SETTING(KBC)

SHBM=0: Enable shared memory with host BIOS

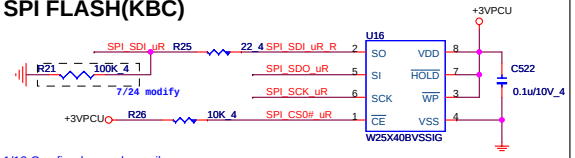
SHBM R336 *10K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU(KBC)

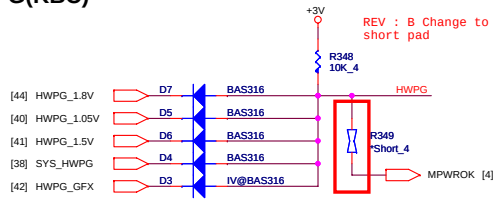


SPI FLASH(KBC)



1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

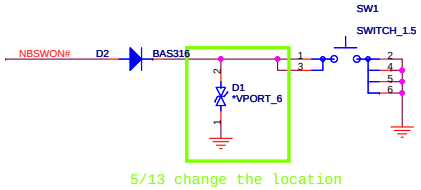
HWPG(KBC)



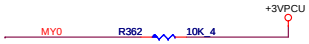
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	GPU-I2C
SM Bus 4	N/A

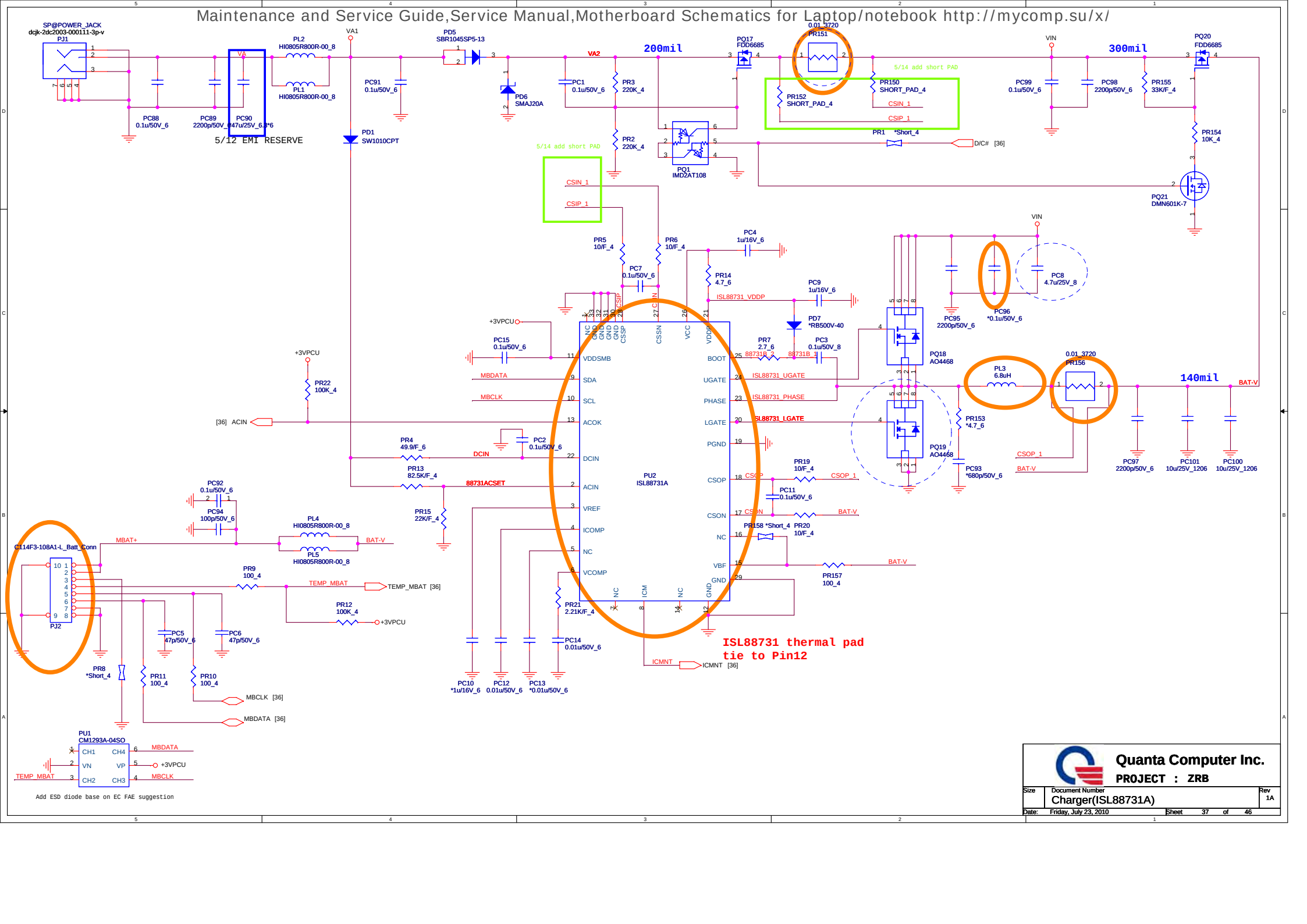
POWER-ON Switch(KBC)

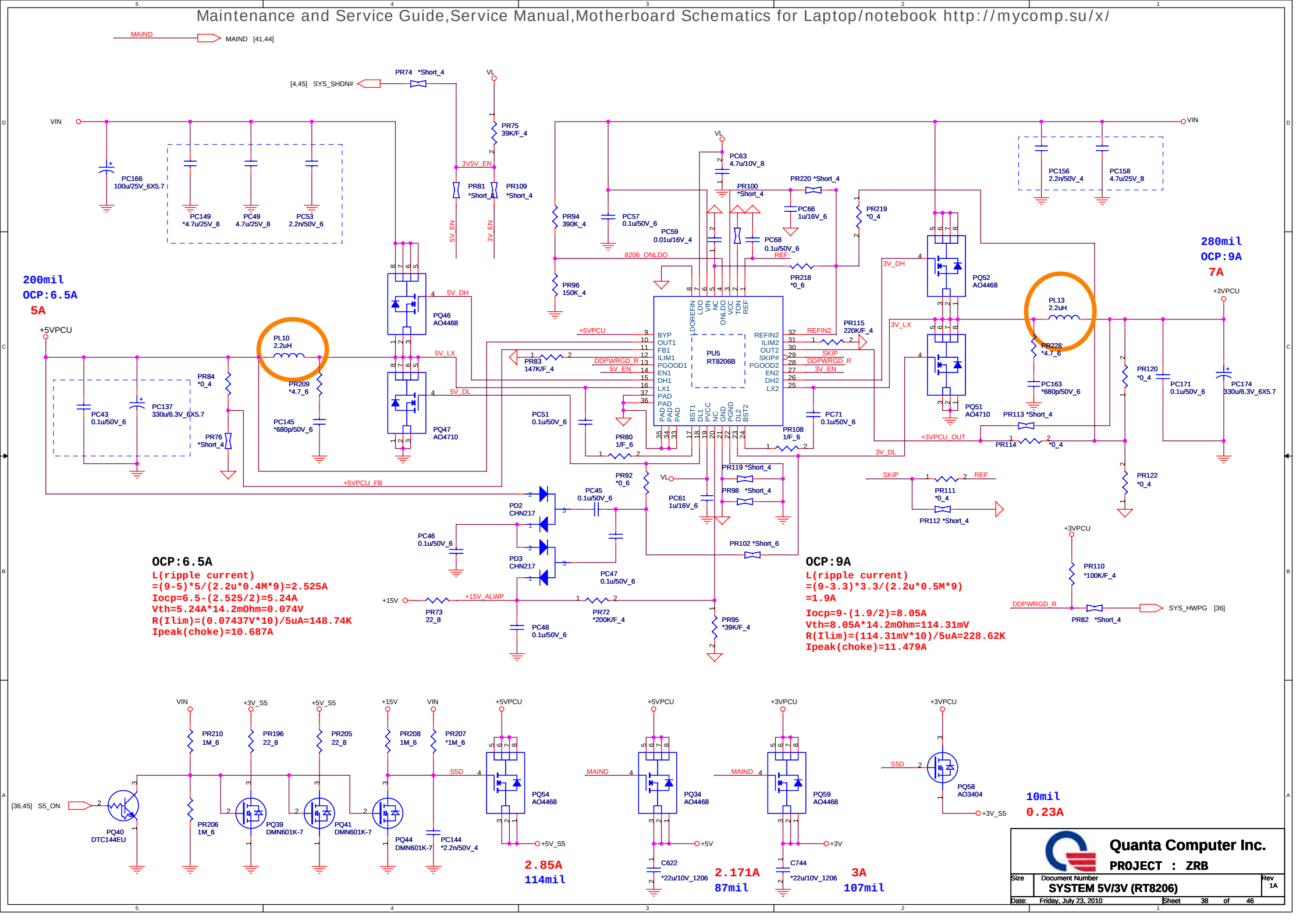


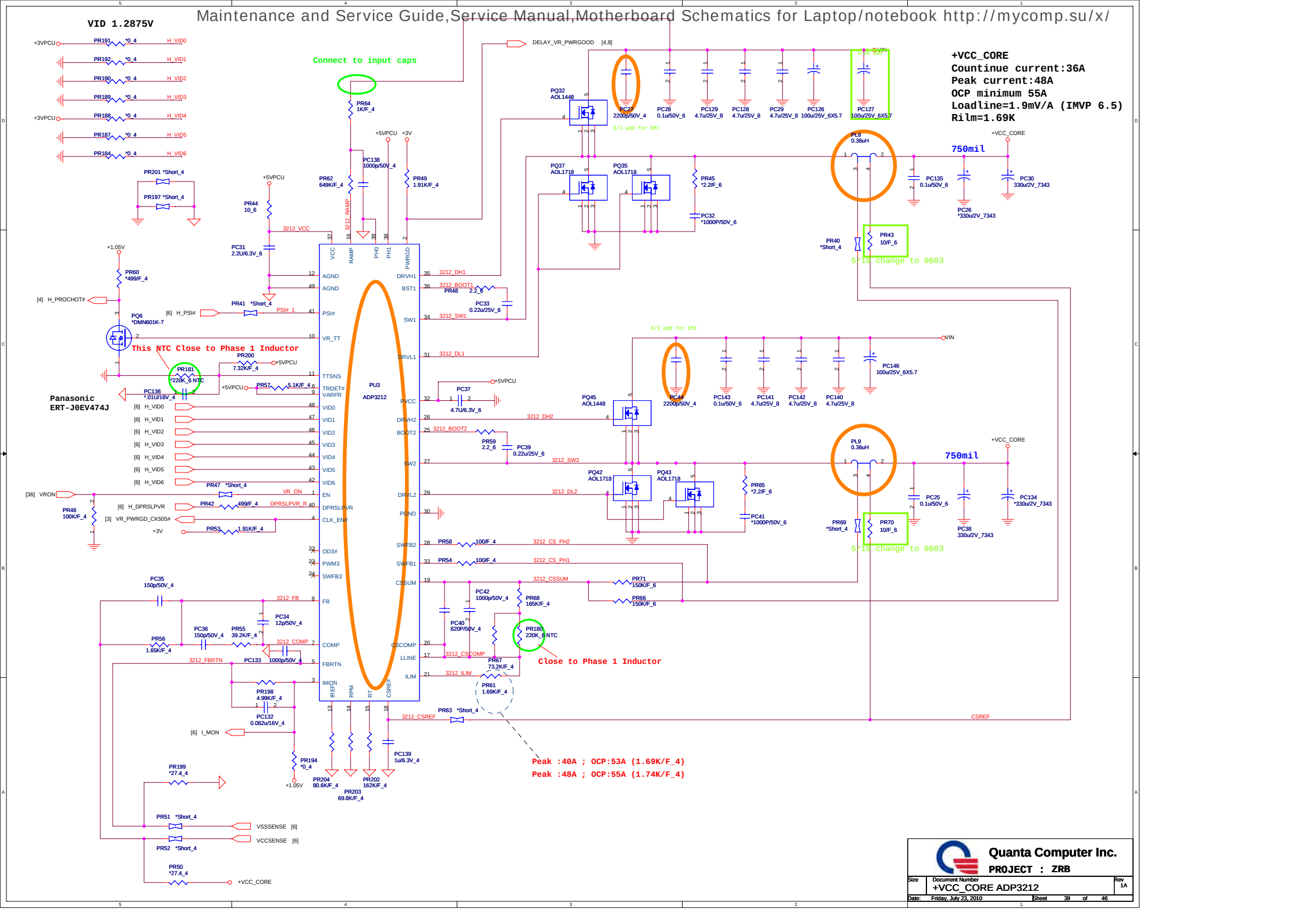
INTERNAL KEYBOARD STRIP SET(KBC)



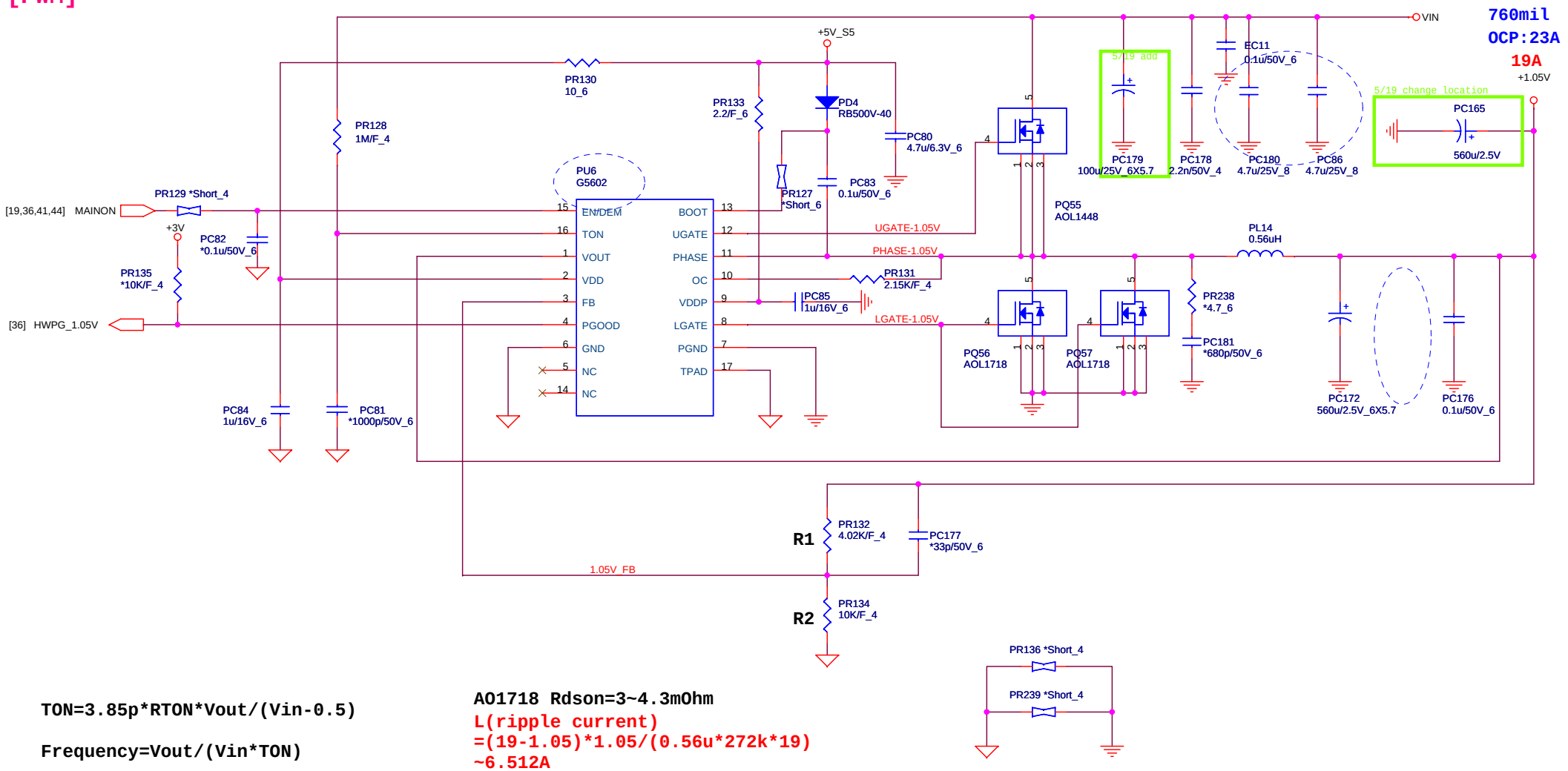
Quanta Computer Inc.			
PROJECT : ZRB			
Size	Document Number		Rev
	WPCE781 & FLASH		1A
Date: Wednesday, July 21, 2010		Sheet 36 of 46	







[PWM]



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO1718 Rdson=3~4.3mOhm

L(ripple current)
=(19-1.05)*1.05/(0.56u*272k*19)
~6.512A

RILIM=2.15mohm*23-3.256/20uA=2.122Kohm

I(choke)peak=29.512A

Quanta Computer Inc.		
PROJECT : ZRB		
Size	Document Number: +VTT (UP6111A)	Rev: 1A
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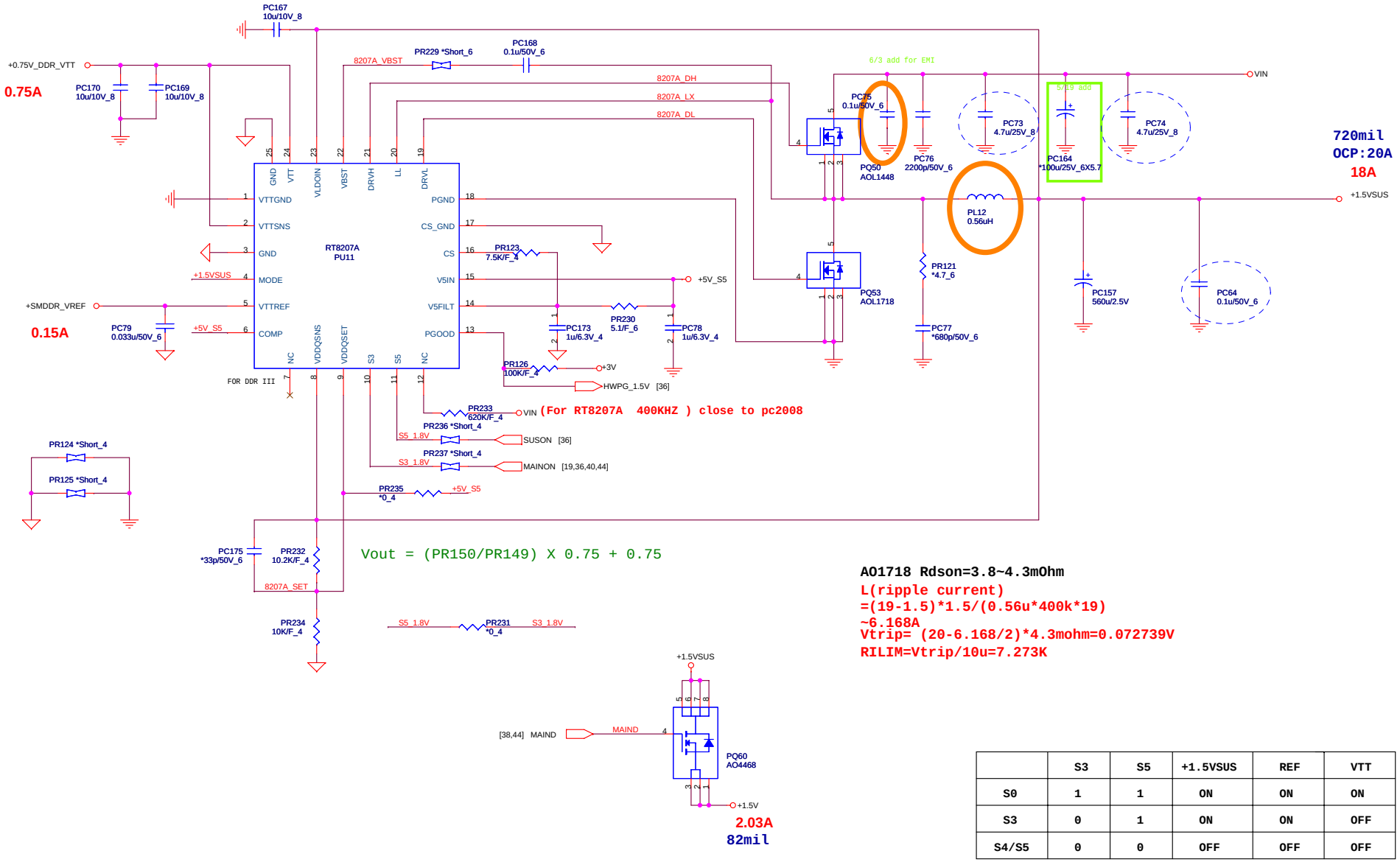
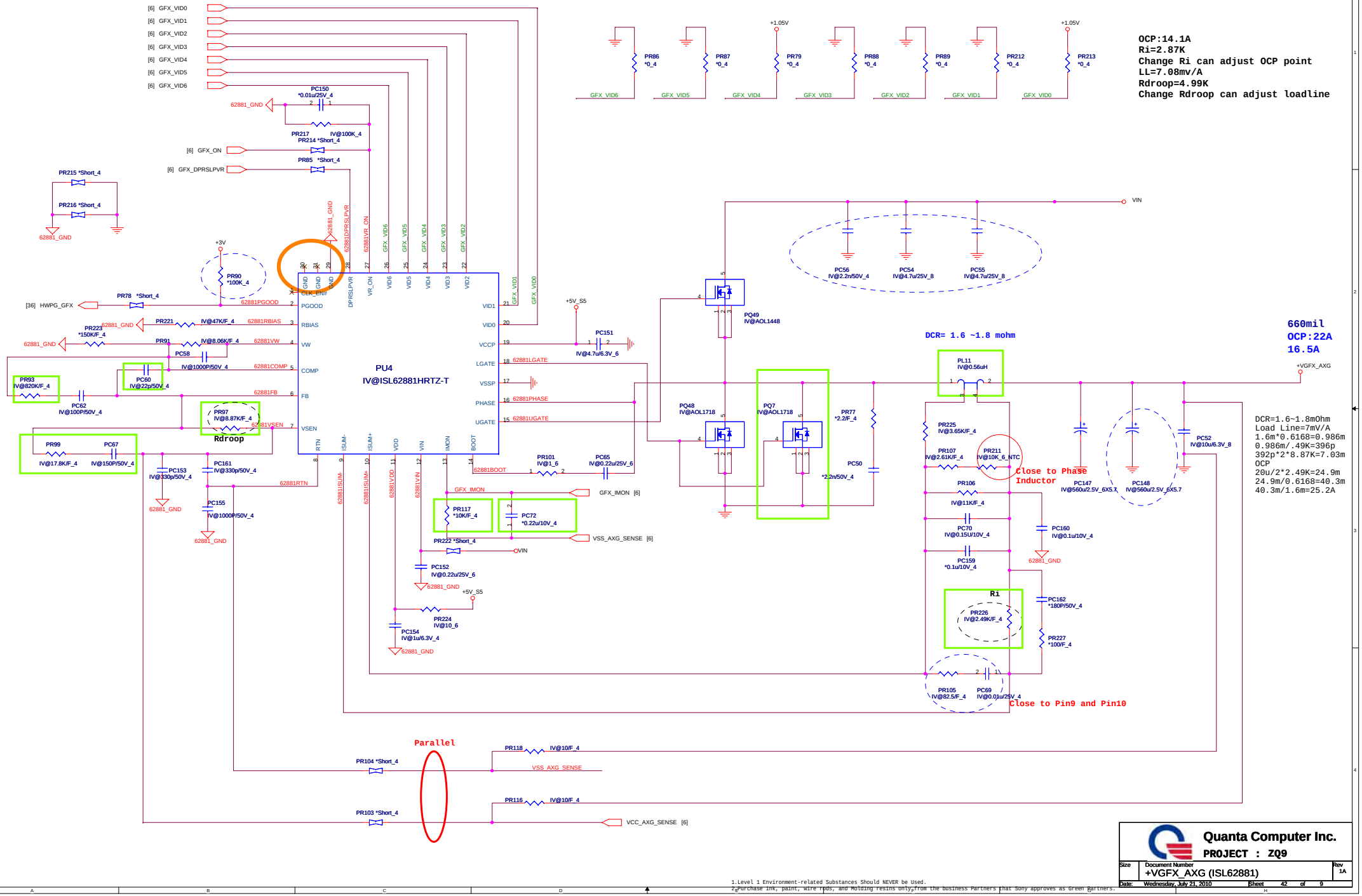


	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT : ZRB

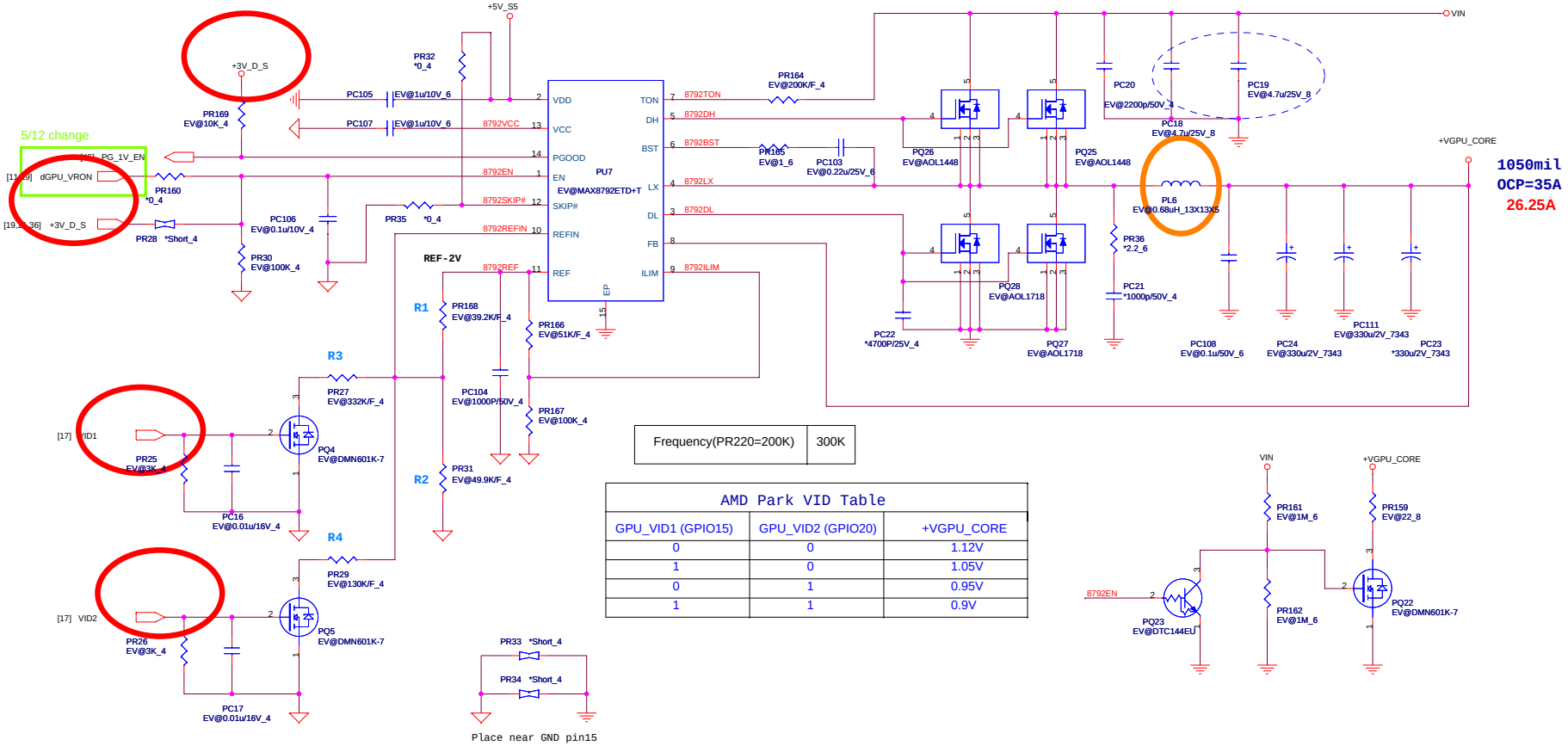
Size	Document Number	Rev
	DDR 1.5V(RT8207A)	1A

Date: Wednesday, July 21, 2010 Sheet 41 of 46



Quanta Computer Inc. PROJECT : ZQ9			
Size	Document Number +VGFX_AXG (ISL62881)		Rev 1A
Date: Wednesday, July 21, 2010	Sheet 42 of 9		

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



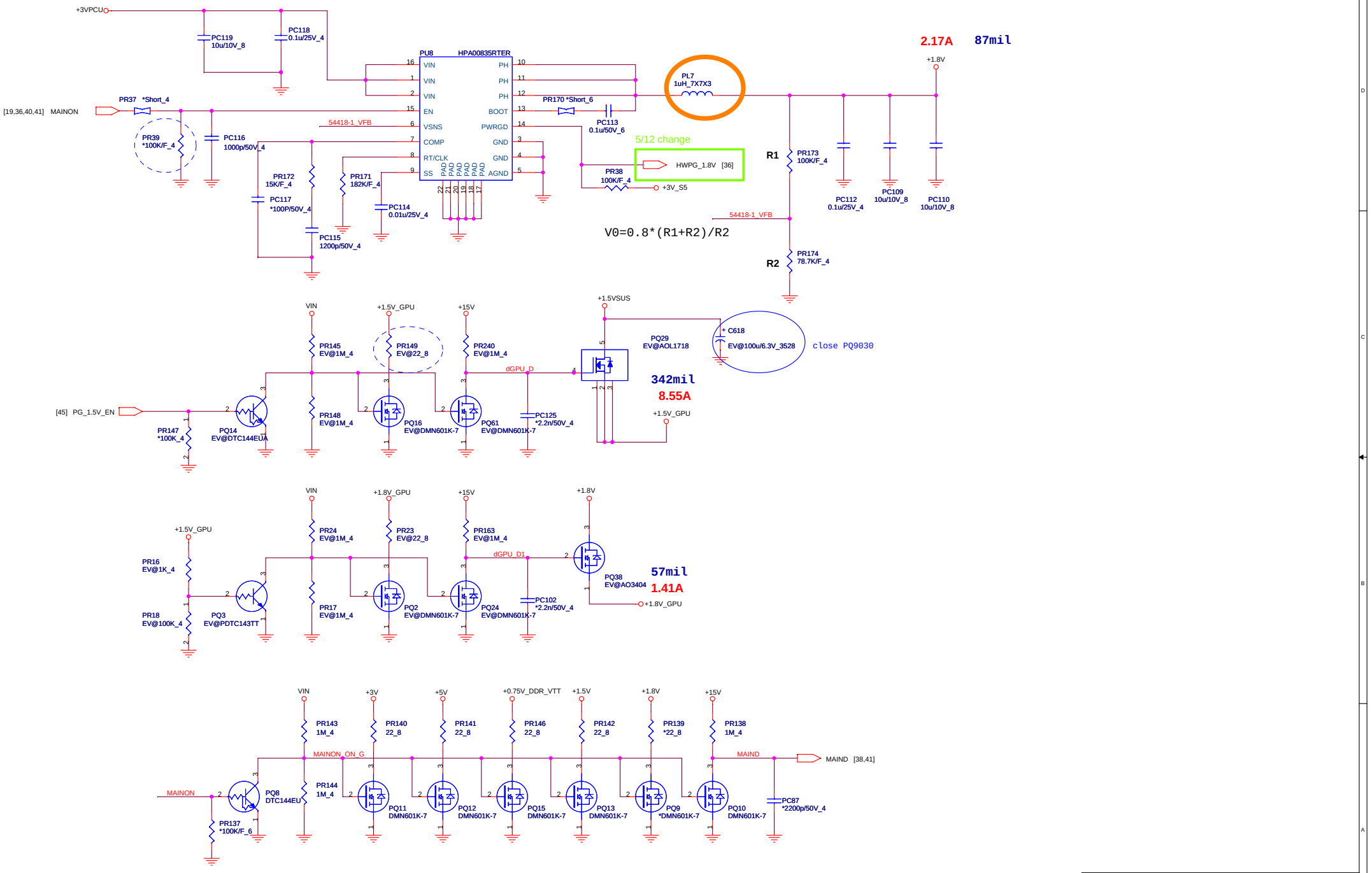
Frequency(PR220=200K)	300K

AMD Park VID Table

GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	1.12V
1	0	1.05V
0	1	0.95V
1	1	0.9V

Quanta Computer Inc.
PROJECT : ZQ9

Size	Document Number	Rev
	GPU CORE(MAX8792)	1A
Date: Wednesday, July 21, 2010	Sheet 43 of 9	



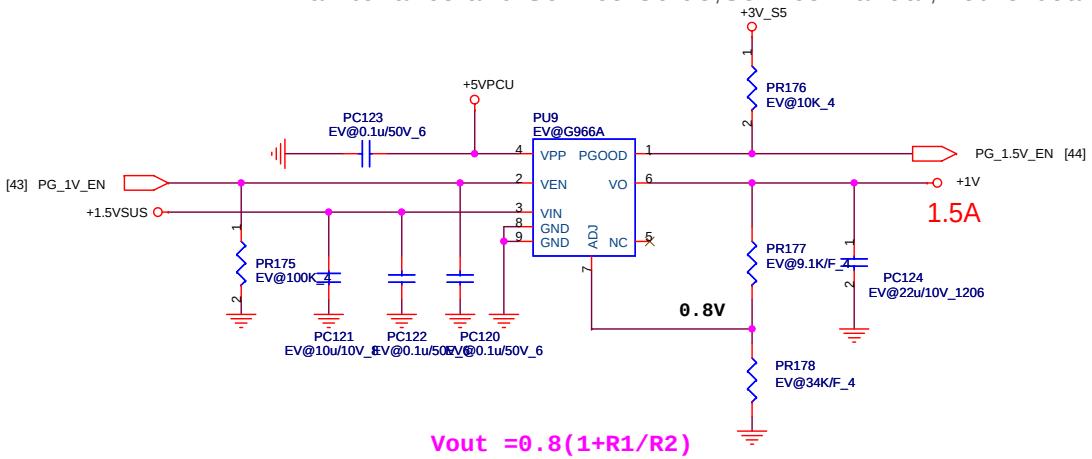
7/7 modify

Quanta Computer Inc.

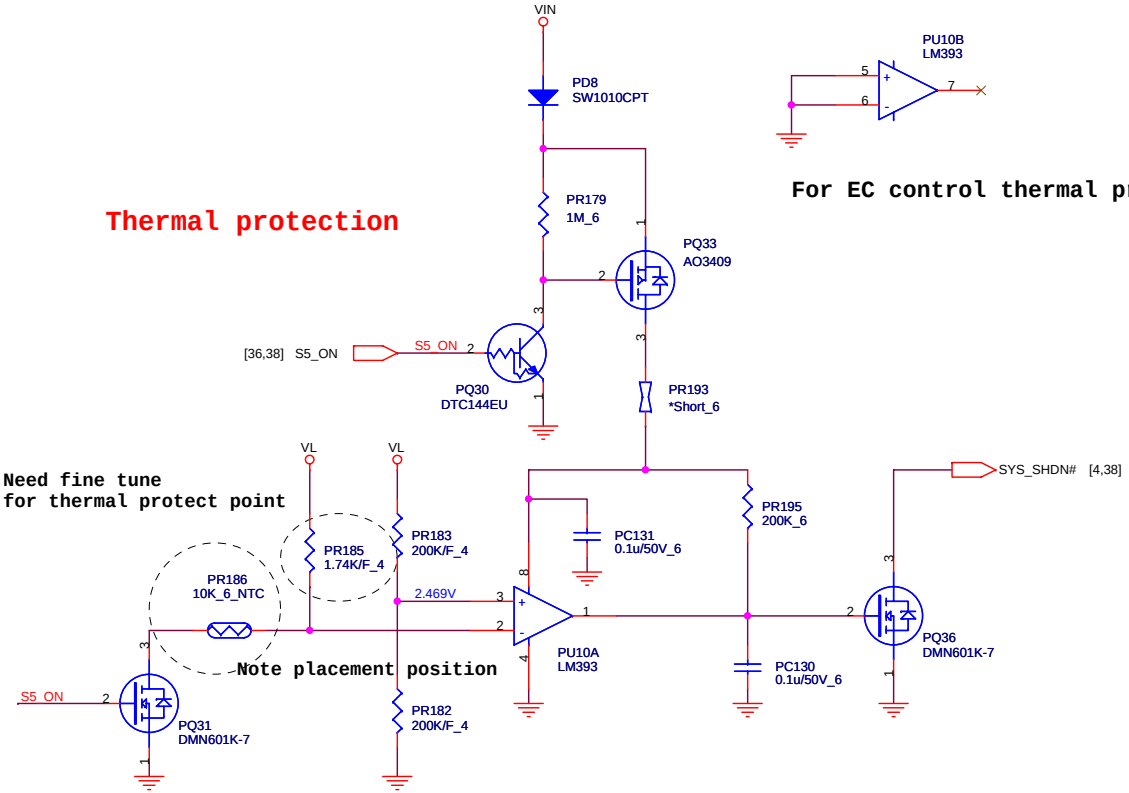
PROJECT : ZRB

Size	Document Number	Rev
	Discharge/1.8V)	1A

Date: Friday, July 23, 2010 Sheet 44 of 46



Vout =0.8(1+R1/R2)
=1V



Thermal protection

For EC control thermal protection (output 3.3V)

Need fine tune
for thermal protect point

Note placement position

Quanta Computer Inc.			
PROJECT : ZRB			
Size	Document Number		Rev 1A
Date: Wednesday, July 21, 2010		Sheet 45 of 46	

CHANGE LIST

Model	REV	CHANGE LIST
ZY9B MB	1A	FIRST RELEASED
	2A	Page 3 : Unstuff L54 & stuff R586 & change U31 P/N for 3V CLK gen and Switch CLK_BUF_DREFSSCLK and CLK_BUF_PCIE_3GPLL Page 4 : Q16 Change P/N for EOD part & short R116 (Del.) for 0 ohm Page 8 : Short R244 (Del.) for 0 ohm Page 10 :Short R243 (Del.) for 0 ohm Page 12 :Short R189 ,R190 & R534 (Del.) for 0 ohm & C655 change P/N for EOD part Page 14 :Del. R268 & R247 for M3 solution & stuff R269 ,R229 ,R223 & R226 for M1 solution,Stuff C372 for +1.5VSUS leakage Page 15 :Stuff C459 for +1.5VSUS leakage Page 25 :Q12 ,Q17 & Q18 Change P/N for ESD , CN10 Change P/N ,Q14.2 & Q13.2 Change from +5V to +3V Page 27 :C339 & C391 of footprint Change from 0805 to 0402 for ESD Page 28 :Unstuff R566 ,R294 ,R284 ,R279 ,R276 ,R273 ,R272 for disable debug card function Page 29 :C393 & C254 Change P/N for EOD , CN11 Change footprint for ME design request. Page 30 :U13 Change AMP circuit Page 31 :Q22 & Q23 Change P/N for EOD part. Page 34 :Del. L55 , CN12 Change P/N Page 36 :C27 Change P/N for EOD part Page All : Change to short pad : Location : R458 ,R452 ,R537 ,R533 ,R144 ,R155 ,R191 ,R140 ,R201 ,R224 ,R461 ,R136 ,R197 ,R206 ,R219 ,R212 ,R166 ,R174 ,R188 ,R202 ,R209 ,R184 ,R168 ,R185 ,R448 ,R447 ,R5 ,R10 ,R9 ,R6 ,R263 ,R288 ,R544 ,R436 ,R563 ,R570 ,R569 ,R584 ,R299 ,C738 ,R311 ,R585 ,R583 ,R571 ,R582 ,R575 ,R576 ,R579 ,R333 ,R352 ,R331 ,R332 & R349
	3A	
	3C	

MODEL: ZY9B

FROM	To
X	1A
X	1A
1A	2A
1A	2A
1A	2A
1A	2A
1A	2A
1A	2A
1A	2A
1A	2A
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3A	3B

DOC NO.	PROJECT MODEL :	ZY9B	APPROVED BY:	DATE:	2009/05/??
	PART NUMBER:		DRAWING BY:	REVISON:	1A