

LC22 Schematic

Pentium-M
RS400MD+SB400

DATE: May. 5th Revision: 0.1

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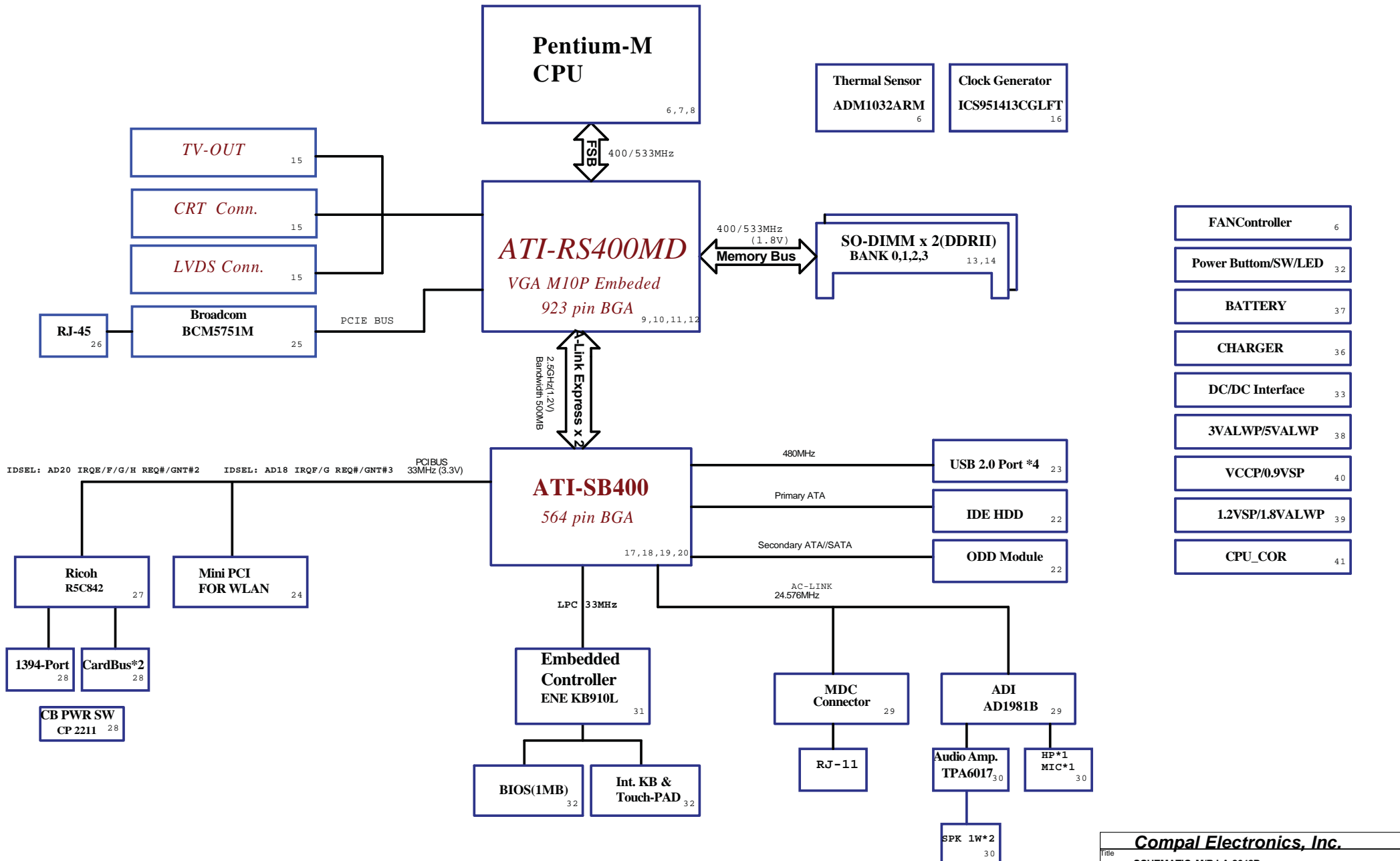
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BLOCK DIAGRAM



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+1.2VS	1.2VS for PCI-Express	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail	ON	ON	OFF
+0.9VS	0.9V power rail	ON	OFF	OFF
+3.3V	3.3V switched power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(R5C842)	AD20	2	PIRQE/PIRQF/PIRQG/PIRQH
Mini-PCI(WLAN)	AD18	3	PIRQF/PIRQG

EC SM Bus1 address

Device	Address	Device	Address
Main Battery	0001 011X b	ADM1032	1001 110X b
EEPROM(24C16/02)	1010 000X b		
Second Battery			

SB400 SM Bus address

Device	Address
Clock Generator (1CS951413CYGLFF)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM2	1010 001Xb

Dip SW function

KBSELO/1#	11:JP K/B 01:US K/B 10:UK K/B 00: Reserve
PASSWORD#	0:Override 1:Avaliable
FINGERPRINT#	0:Existence 1:Non-Existence

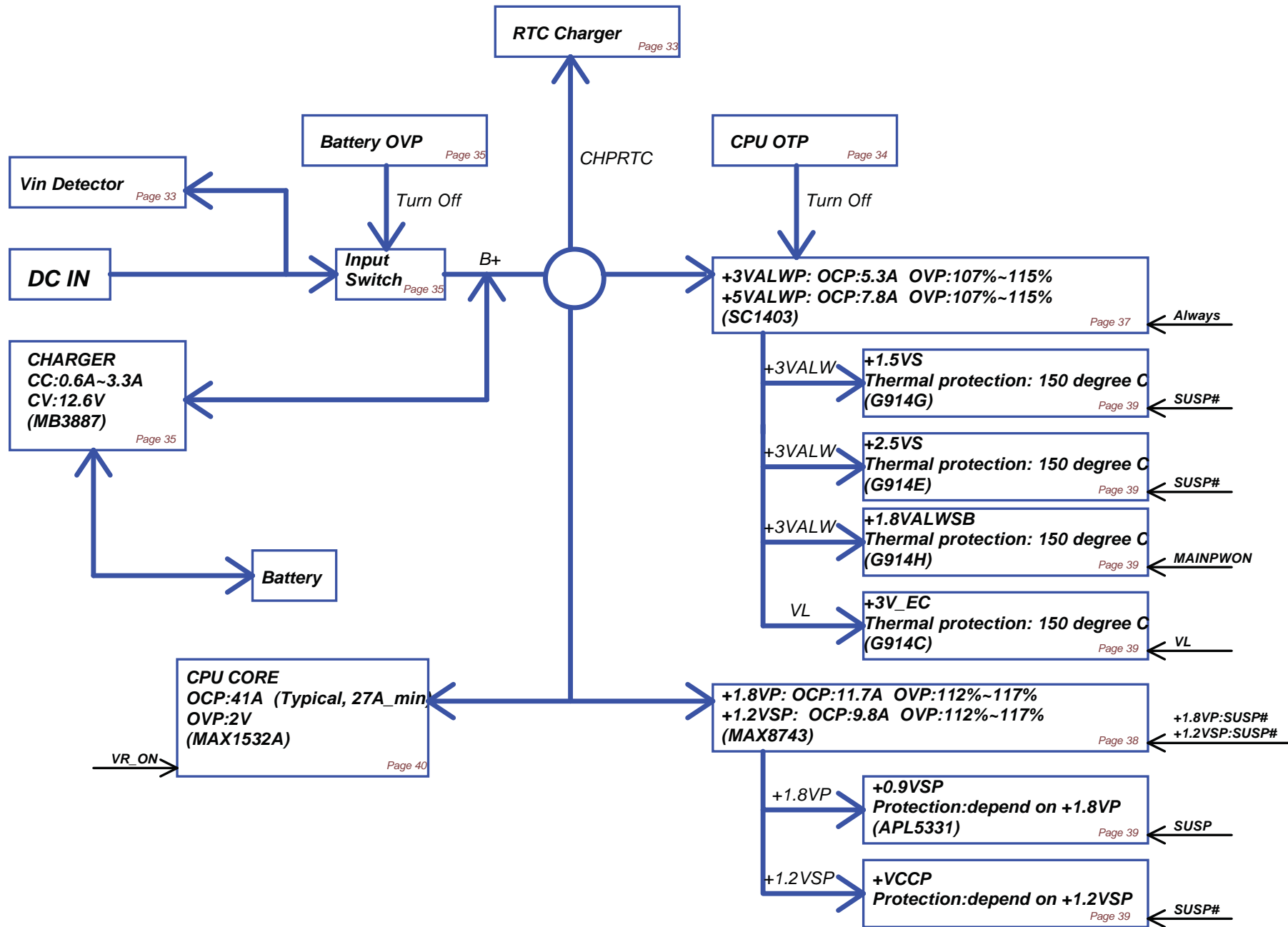
Function Table

Function	Japan			HK/CHINA	Comment
	Commercial	Consumer			
		LaVie	NEC Direct (Internet Retailing)		
TV-OUT	Yes	<-	<-	<-	
Bluetooth	No	Yes	<-	<-	Need BTO
PWR LED (Odekake)	No	<-	<-	<-	Not need Odekake
S/W	I/II Key	<-	<-	<-	all same
4 in 1 Card Adapter	No	Yes	<-	<-	
Finger Print	Yes (BTO)	No	Yes (BTO)	No	Need BTO
TPM	Yes	No	<-	<-	Need BTO
W-LAN	JP	JP	JP	Oversea	

Chip Reversion

Chip	Phase	ES Phase	PP Phase	MP1 Phae	DR2
RS400MD		A12	A21-LF	A21-LF	
SB400		A31	A31-LF	A32-LF	
Clk Gen		B	C	C	
KB910L		A0	A1	A1	
AD1981B		A	A	A	

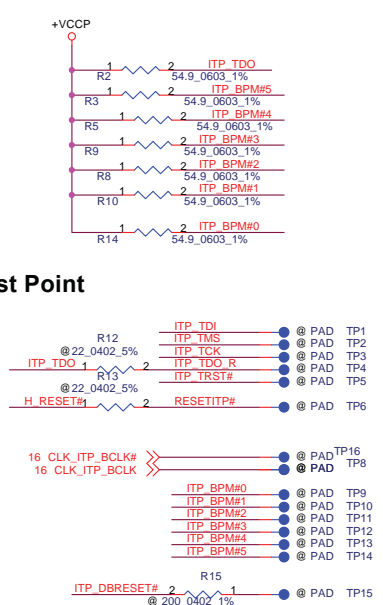
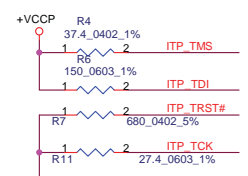
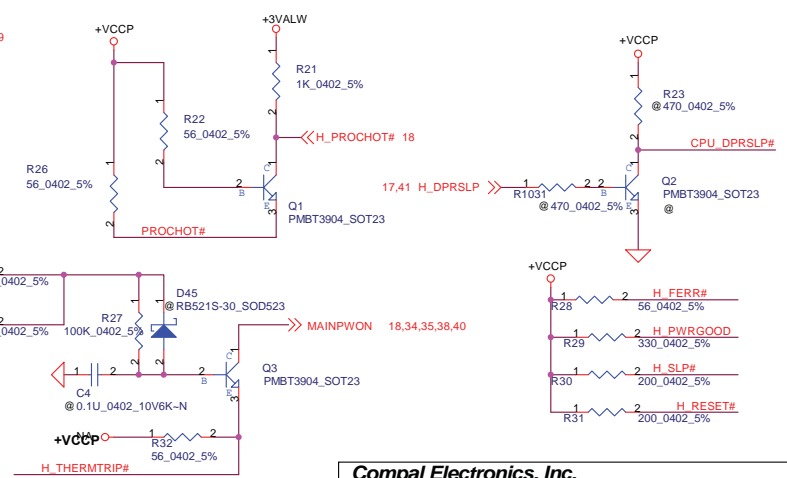
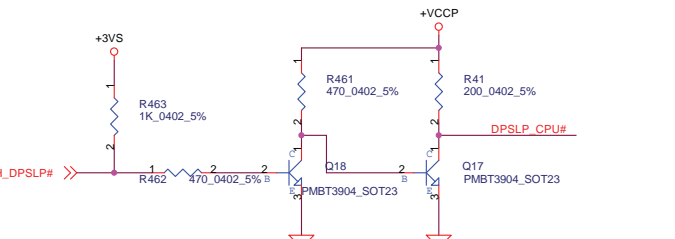
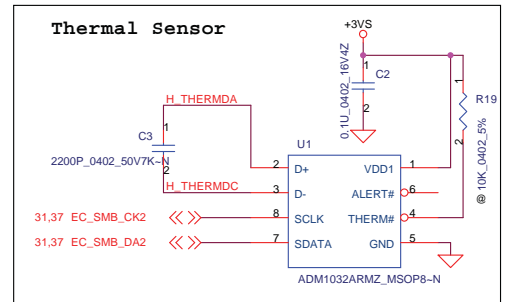
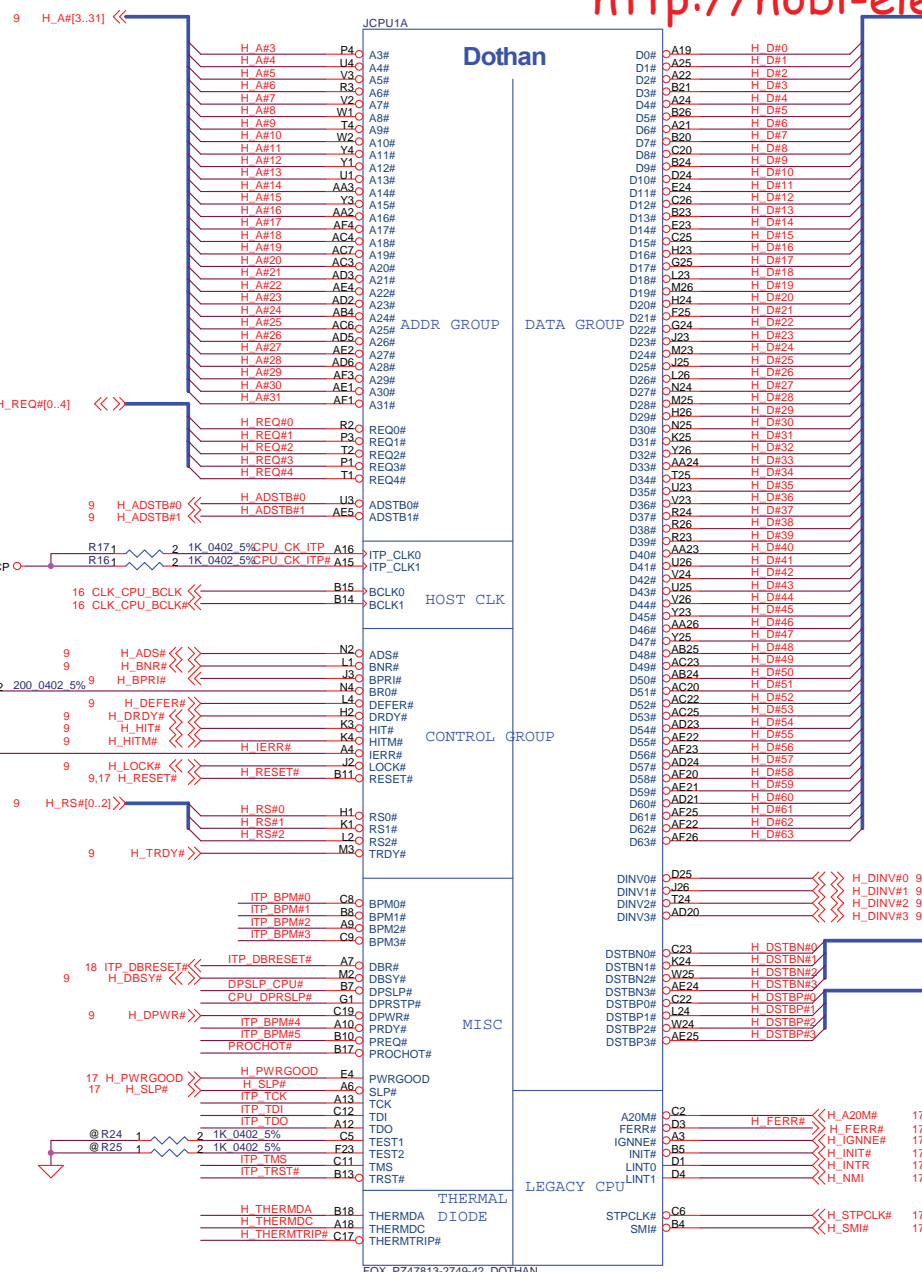
LC2 Power block



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ITP Test Point

Thermal Sensor

DPSLP CPU#

PROCHOT#

CPU DPRSLP#

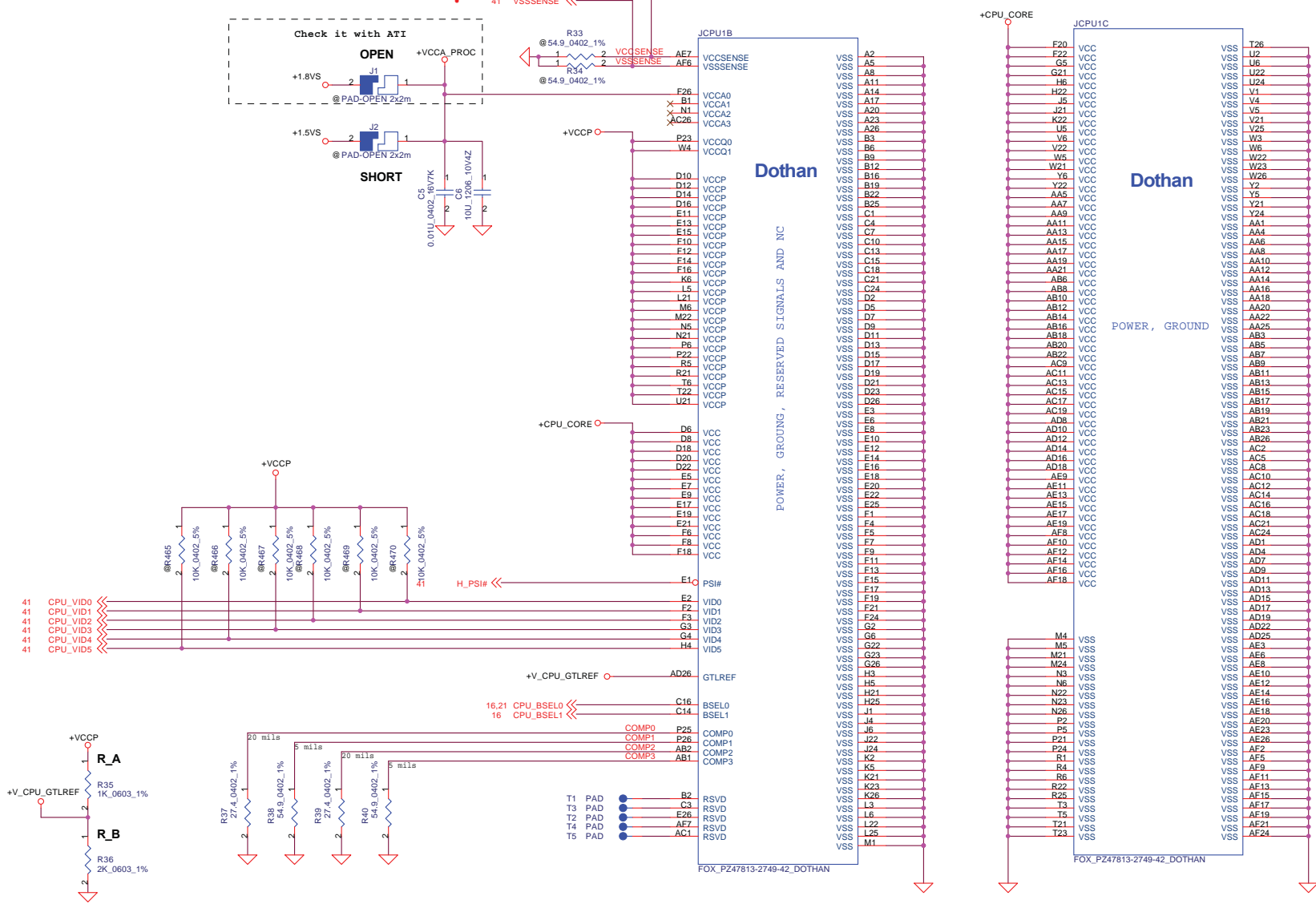
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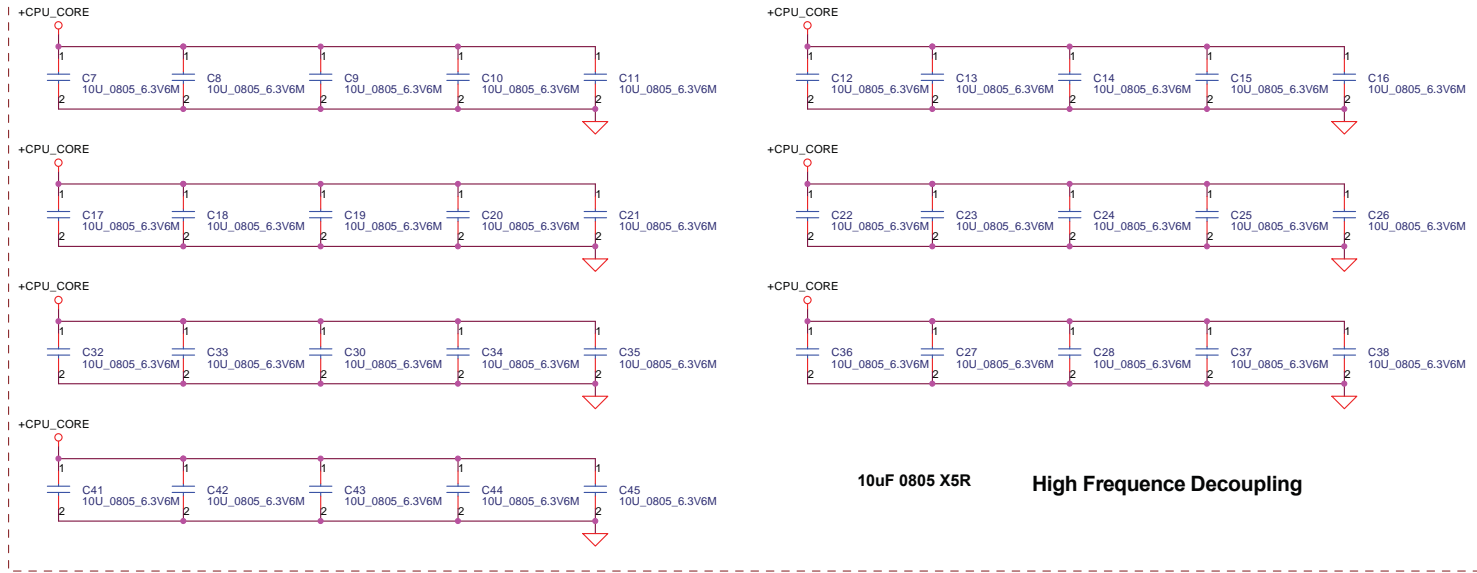
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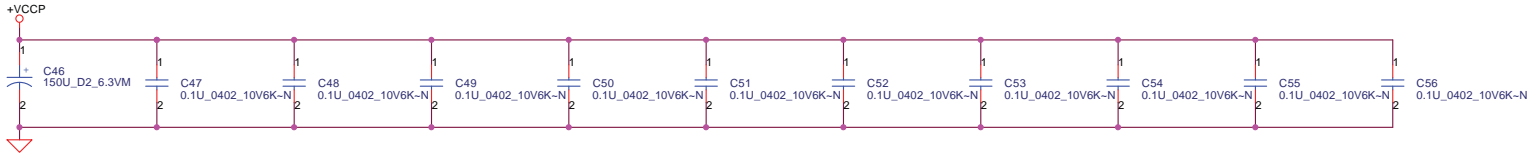
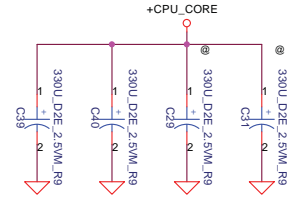


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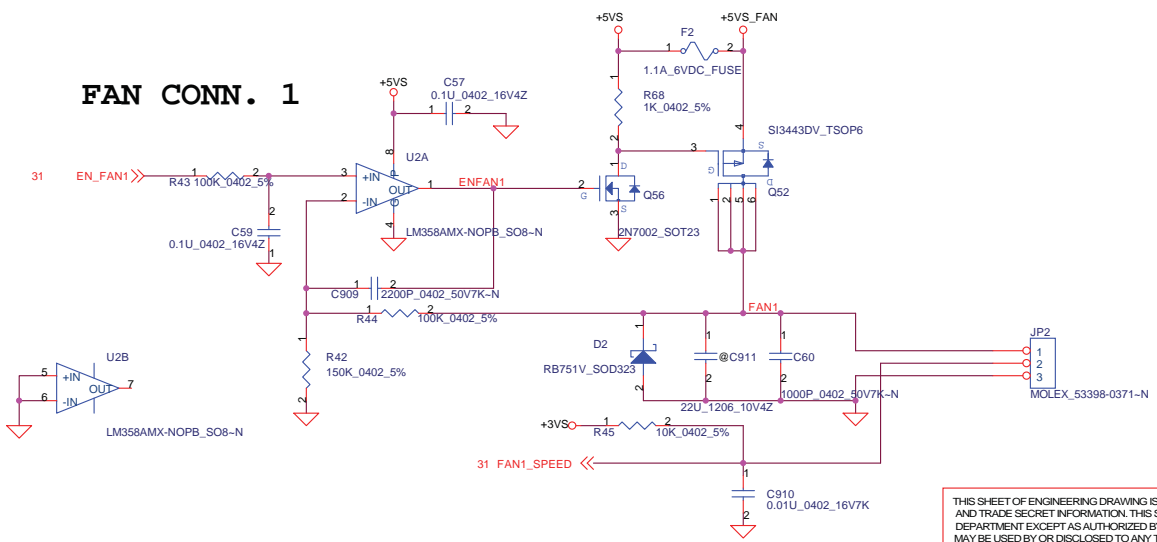


ESR <= 3m ohm
Capacitor > 880 uF

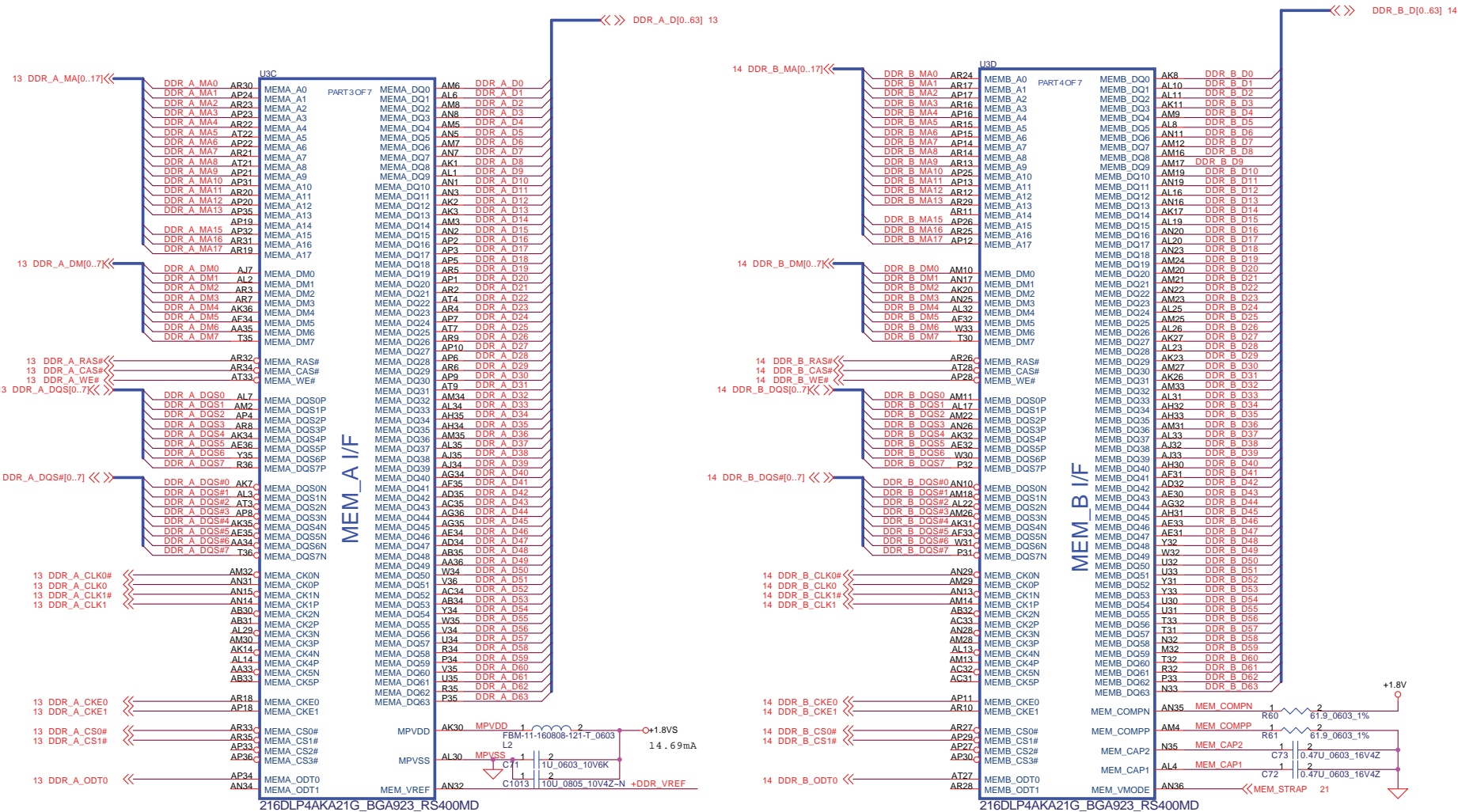
Near VCORE regulator.



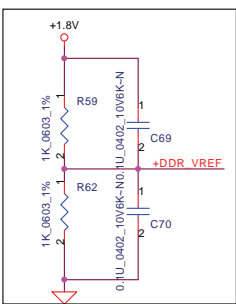
FAN CONN. 1



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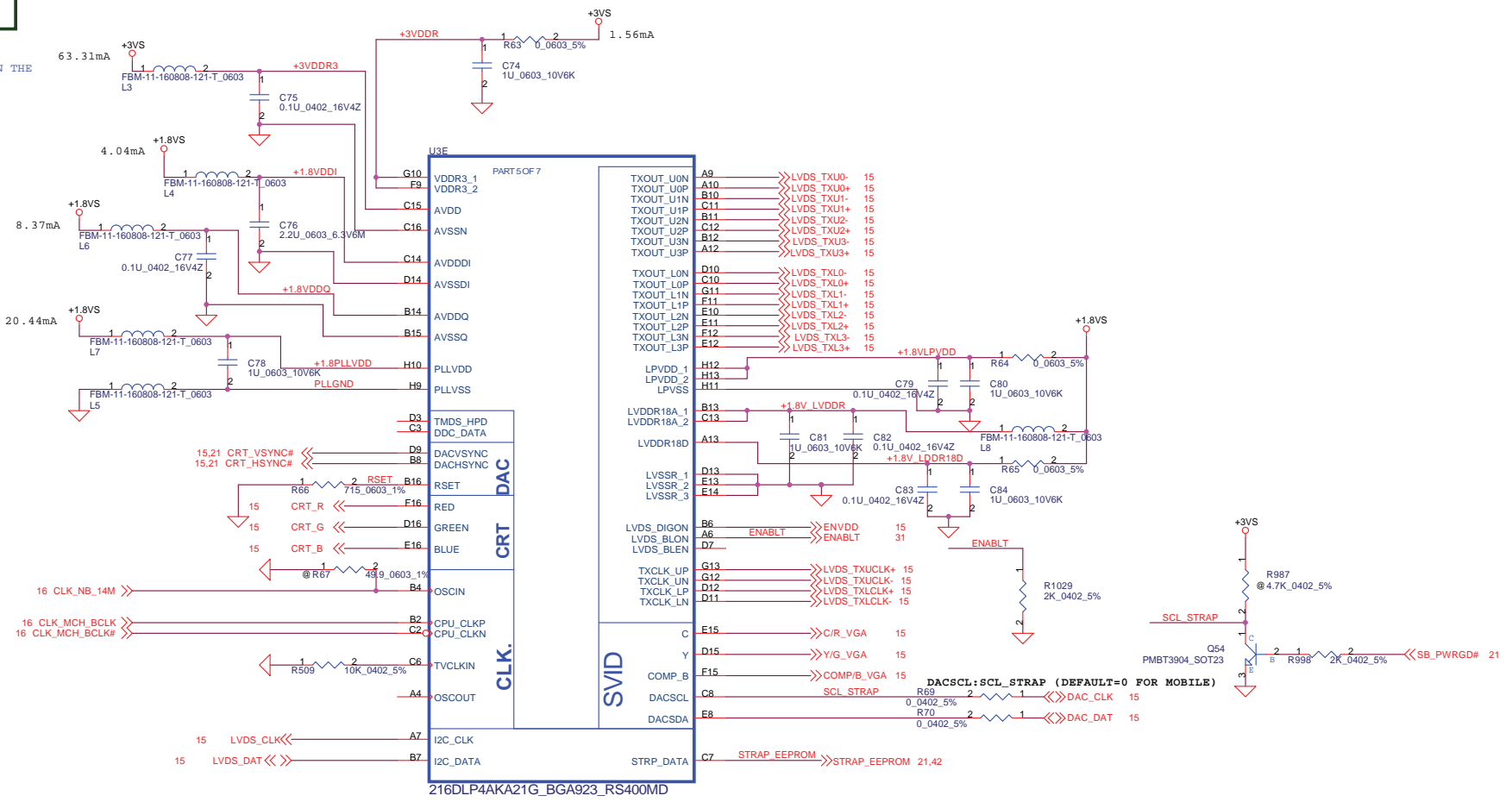


Place these R and C close to relative Ball.



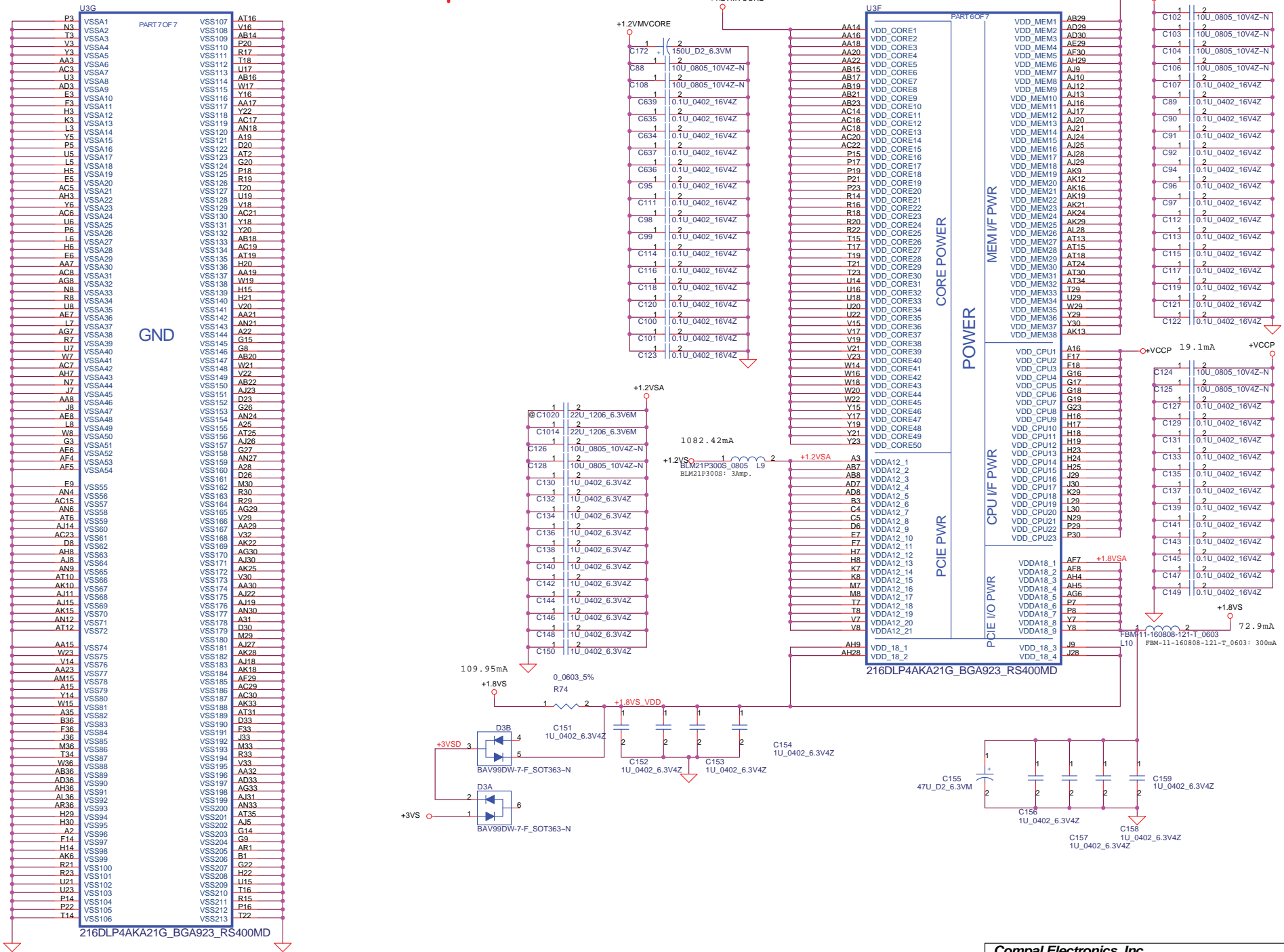
VDD	DAC VDD (2.5V/3.3V)
AVDDDI	DIGITAL VDD (1.8V)
AVDDQ	DAC2 BANDGAP REF (1.8V)
PLLVD	PLL VDD (1.8V)

PUT AVDD, AVDDDI, AVDDQ, PLLVD DECOUPLING CAPS ON THE BOTTOM, CLOSE TO BALLS



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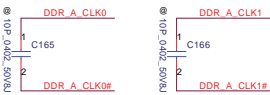
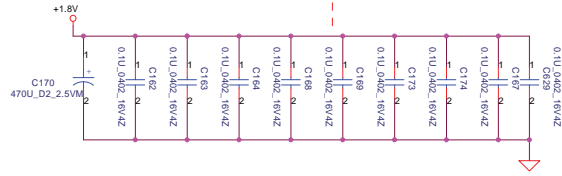
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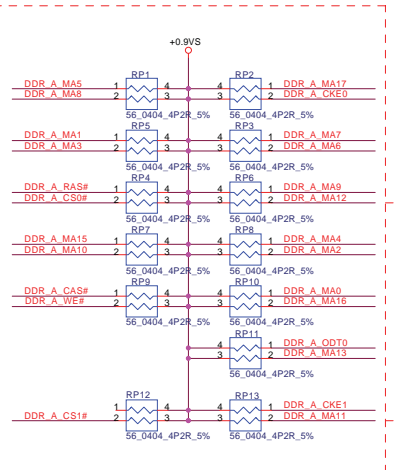
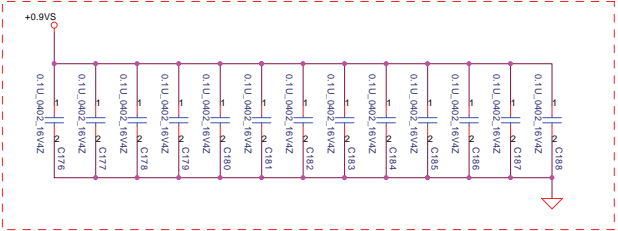
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10 DDR_A_DQS# [0..7] <<>>
10 DDR_A_D [0..63] <<>>
10 DDR_A_DM [0..7] <<>>
10 DDR_A_MA [0..13] <<>>
10 DDR_A_DQS [0..7] <<>>

Layout Note:
Place near JDIM1

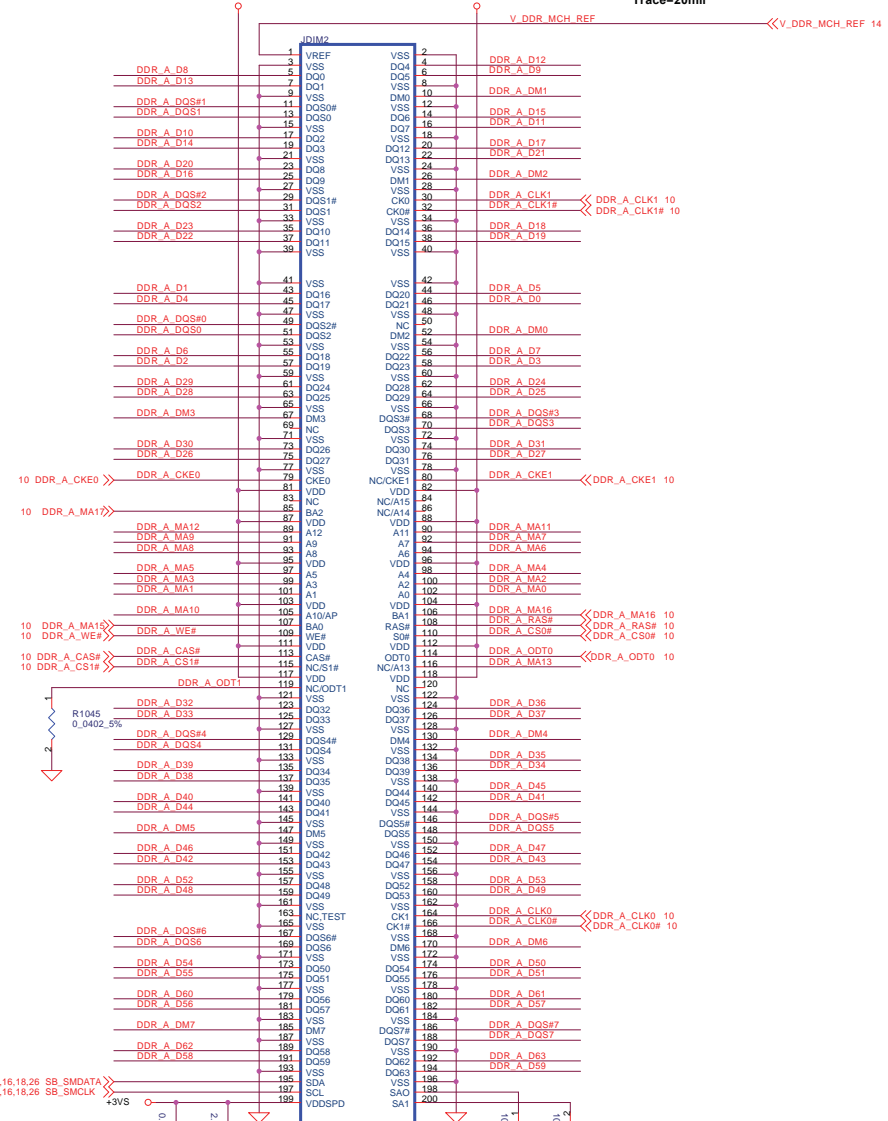


Layout Note:
Place one cap close to every 2 pullup resistors terminated to V_DDR_MCH_REF



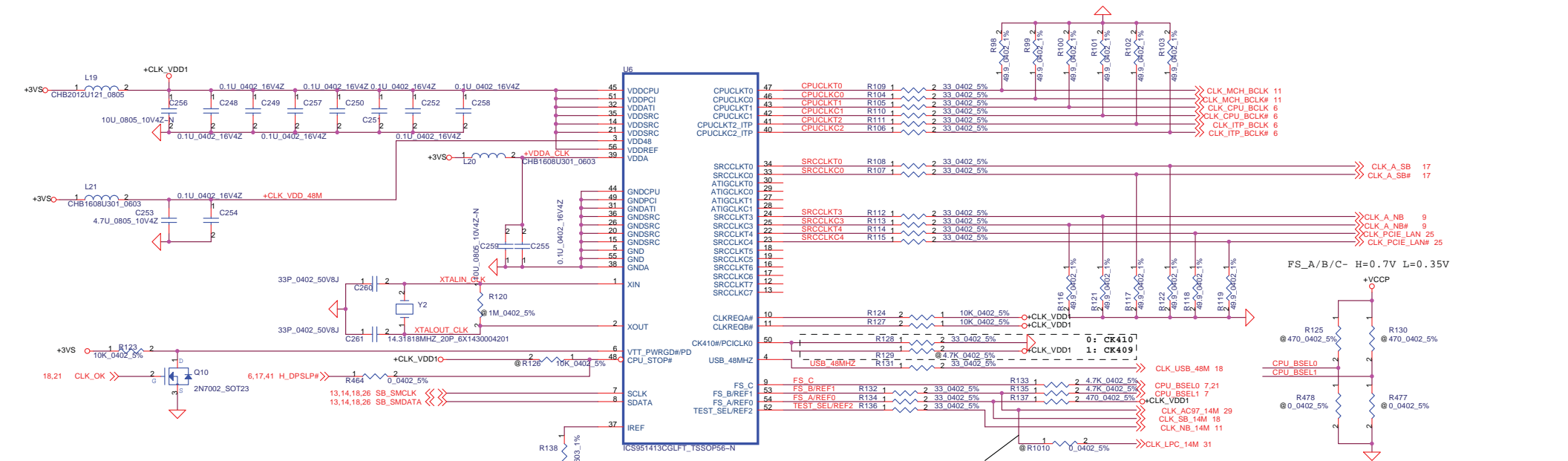
Layout Note:
Place these resistor closely JDIM2, all trace length < 750 mil

Layout Note:
Place these resistor closely JDIM2, all trace length Max = 1.3"



DIMM2 Reverse

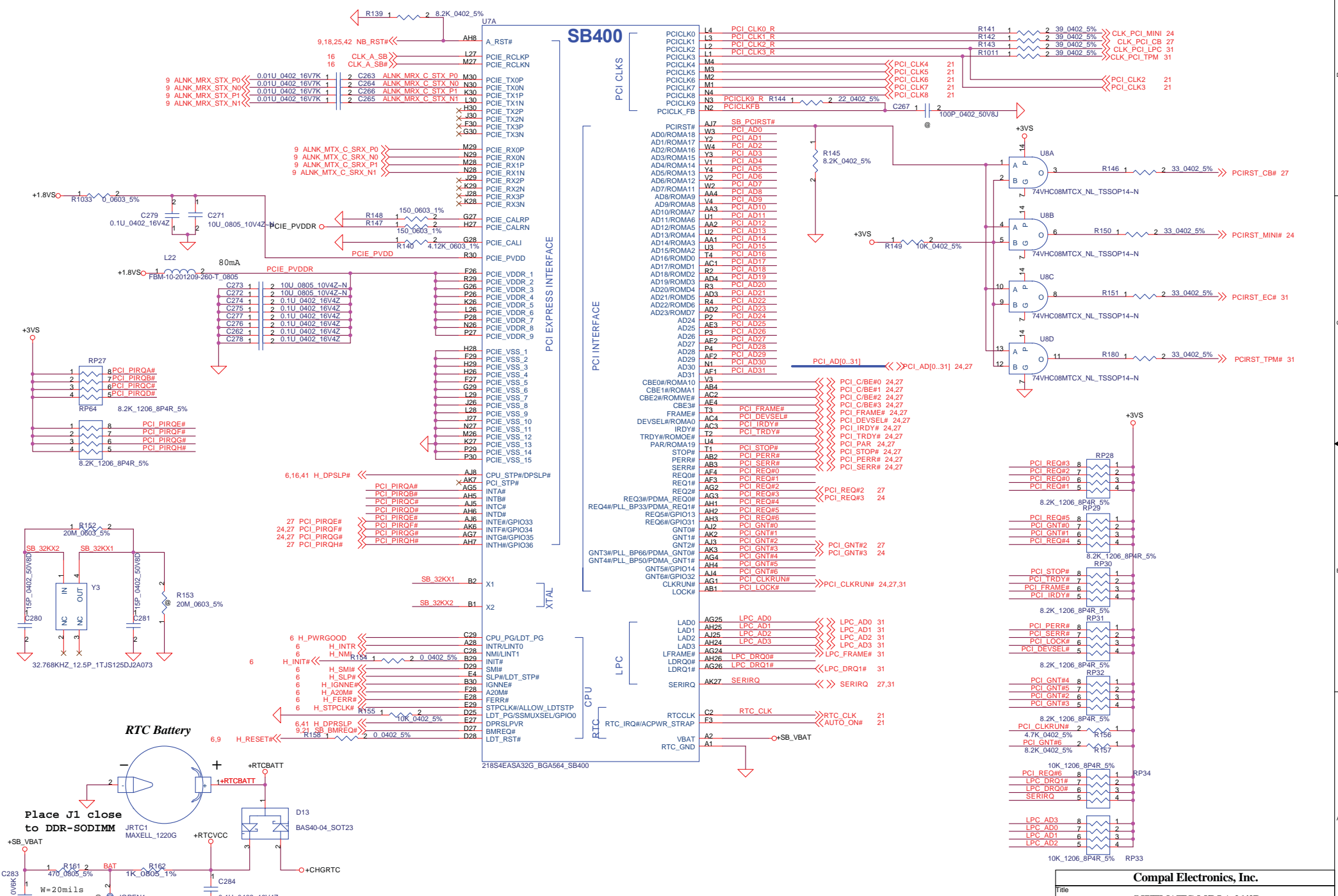
Clock Generator



ICS95141 and CY28RS400 ARE FULLY PIN COMPATIBLE AND CAN BE INTERCHANGED WITHOUT ANY HARDWARE MODIFICATION.
 Internal Pull-low 120k: pin48
 Internal Pull-up 120k: pin 52, 53 and 54.

Keep the trace as short as possible.

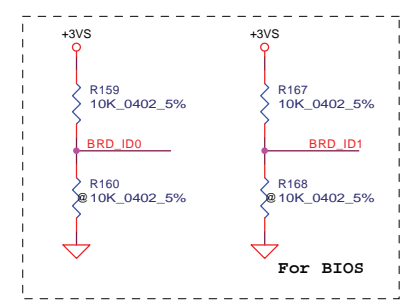
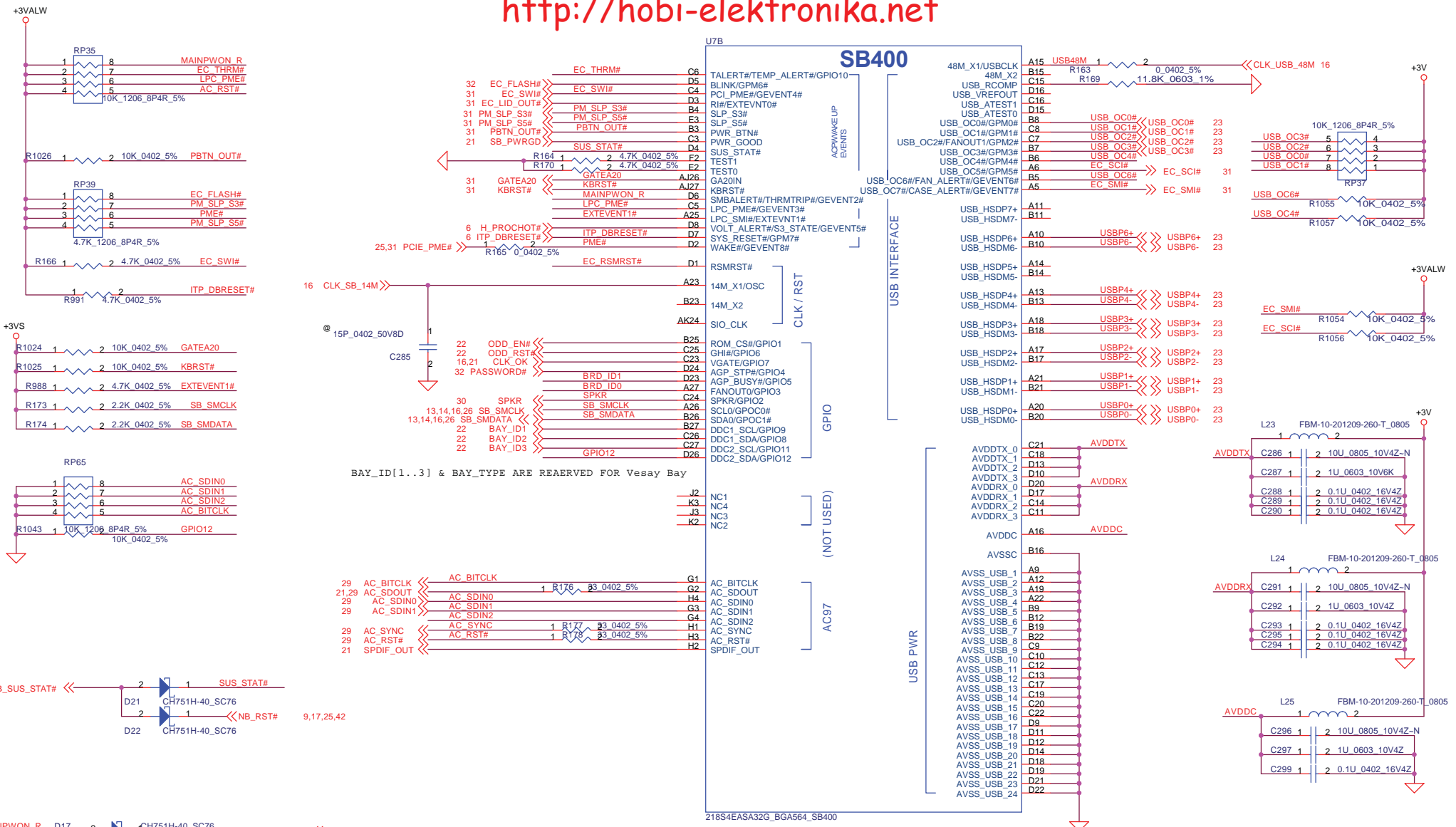
FS_C	FS_B	FS_A	CPU	SRC	PCI	REF	USB
0	0	0	266.66	100.00	33.33	14.318	48.000
	1	1	133.33	100.00	33.33	14.318	48.000
1	0	1	166.66	100.00	33.33	14.318	48.000
	1	1	100.00	100.00	33.33	14.318	48.000
						RESERVED	14.318



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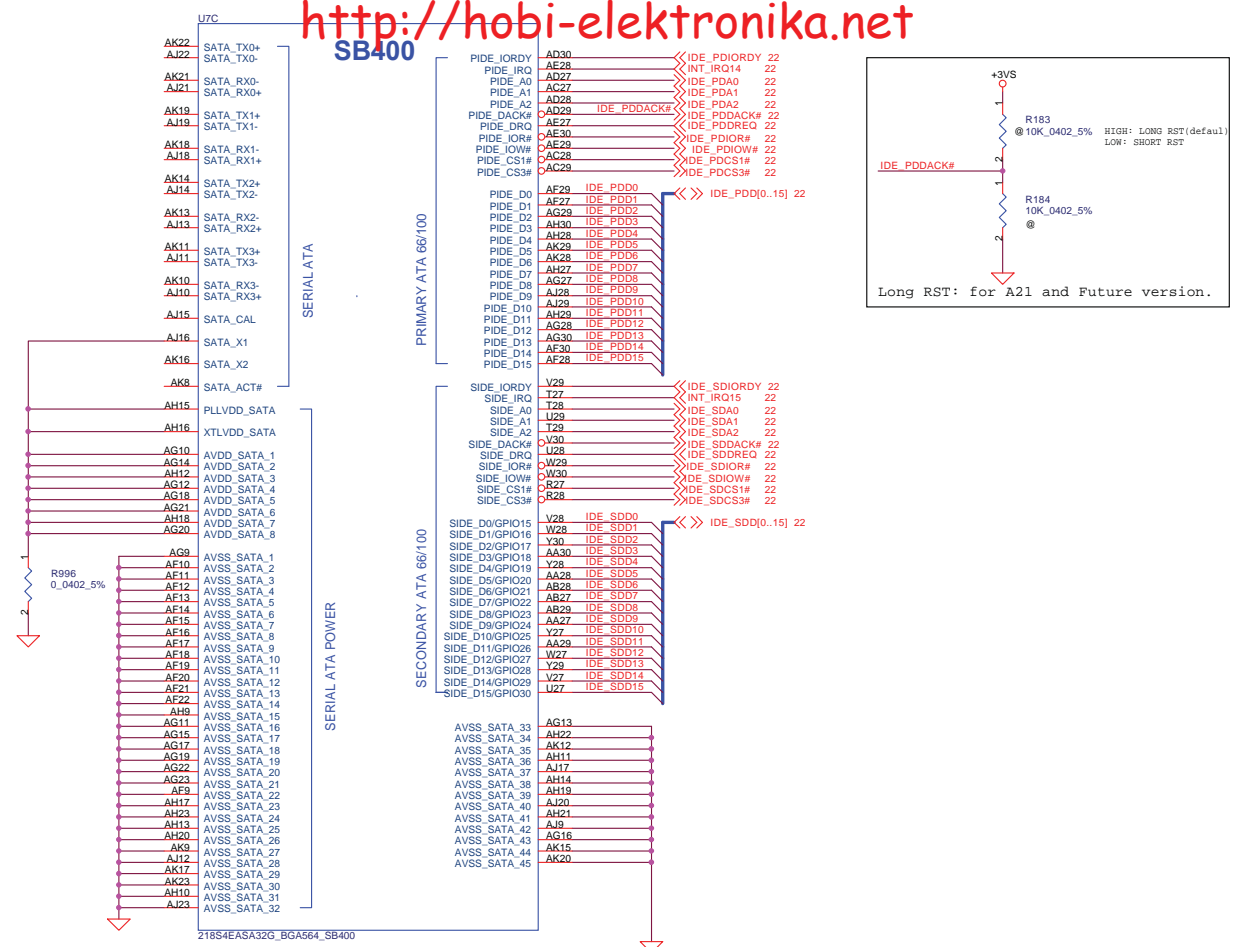
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PUT JOPEN1 NEAR TO RAM DOOR

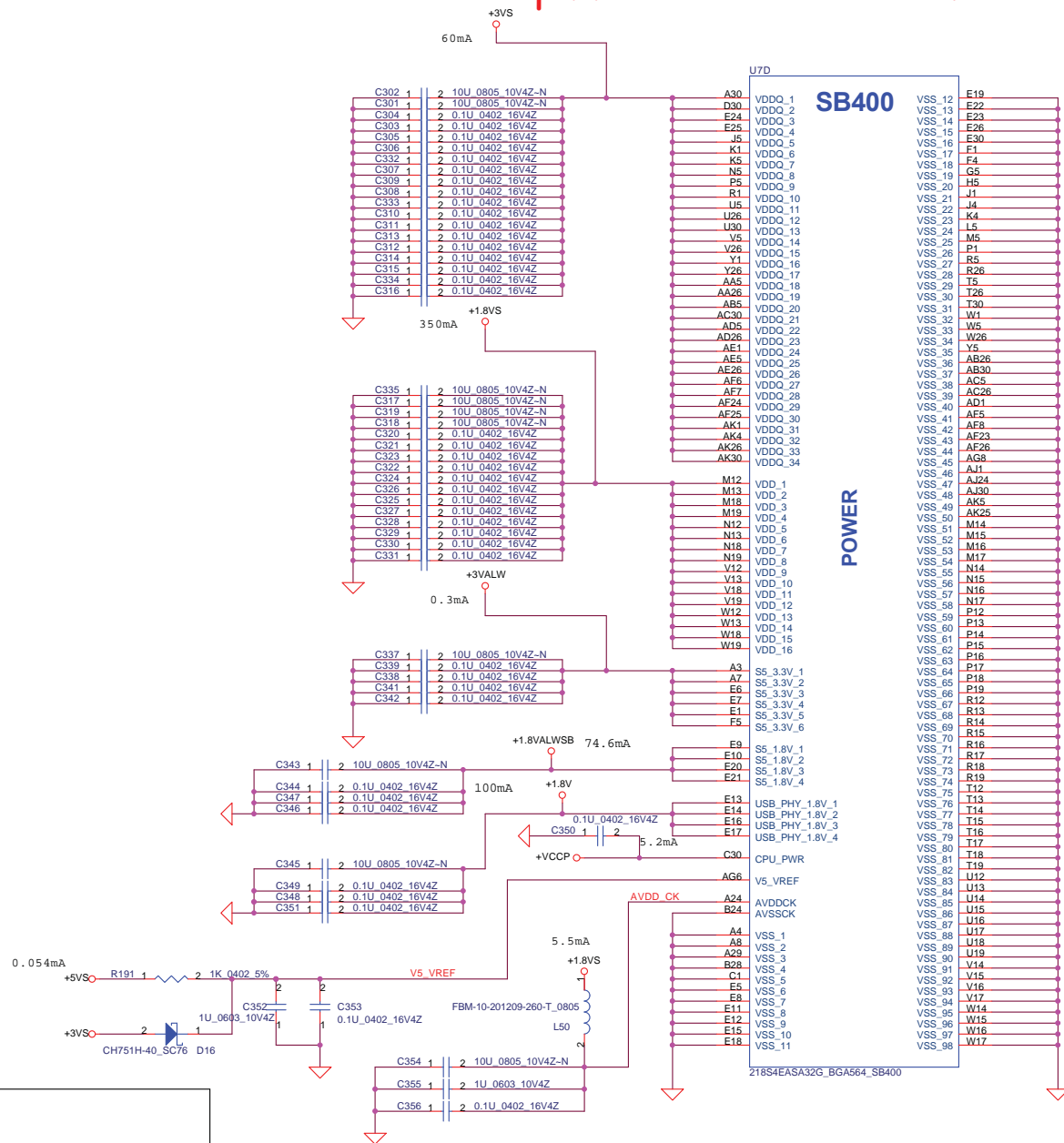


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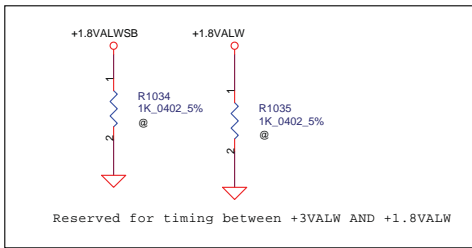
21854EAS432G_BGA564_SB400



SB400

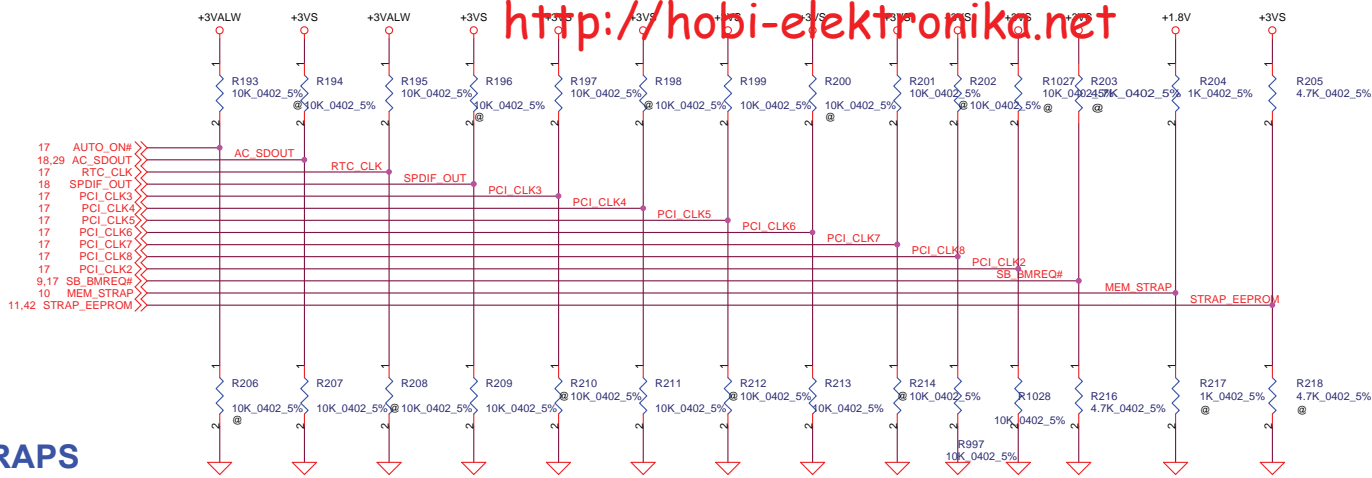
POWER

VDD0_1	E19
VDD0_2	E22
VDD0_3	E23
VDD0_4	E26
VDD0_5	E30
VDD0_6	F1
VDD0_7	F4
VDD0_8	G5
VDD0_9	H5
VDD0_10	J1
VDD0_11	J4
VDD0_12	K4
VDD0_13	L5
VDD0_14	M5
VDD0_15	P1
VDD0_16	R5
VDD0_17	R26
VDD0_18	T5
VDD0_19	T26
VDD0_20	T30
VDD0_21	W1
VDD0_22	W5
VDD0_23	W26
VDD0_24	Y5
VDD0_25	AB26
VDD0_26	AB30
VDD0_27	AC5
VDD0_28	AC26
VDD0_29	AD1
VDD0_30	AF5
VDD0_31	AF8
VDD0_32	AF23
VDD0_33	AF26
VDD0_34	AG8
VDD_1	AJ1
VDD_2	AJ2
VDD_3	AJ30
VDD_4	AK5
VDD_5	AK25
VDD_6	M14
VDD_7	M15
VDD_8	M16
VDD_9	M17
VDD_10	N14
VDD_11	N15
VDD_12	N16
VDD_13	N17
VDD_14	P12
VDD_15	P13
VDD_16	P14
VDD_17	P15
VDD_18	P16
VDD_19	P17
VDD_20	P18
VDD_21	P19
VDD_22	R12
VDD_23	R13
VDD_24	R14
VDD_25	R15
VDD_26	R16
VDD_27	R17
VDD_28	R18
VDD_29	R19
VDD_30	T12
VDD_31	T13
VDD_32	T14
VDD_33	T15
VDD_34	T16
VDD_35	T17
VDD_36	T18
VDD_37	U12
VDD_38	U13
VDD_39	U14
VDD_40	U15
VDD_41	U16
VDD_42	U17
VDD_43	U18
VDD_44	U19
VDD_45	V14
VDD_46	V15
VDD_47	V16
VDD_48	V17
VDD_49	W14
VDD_50	W15
VDD_51	W16
VDD_52	W17



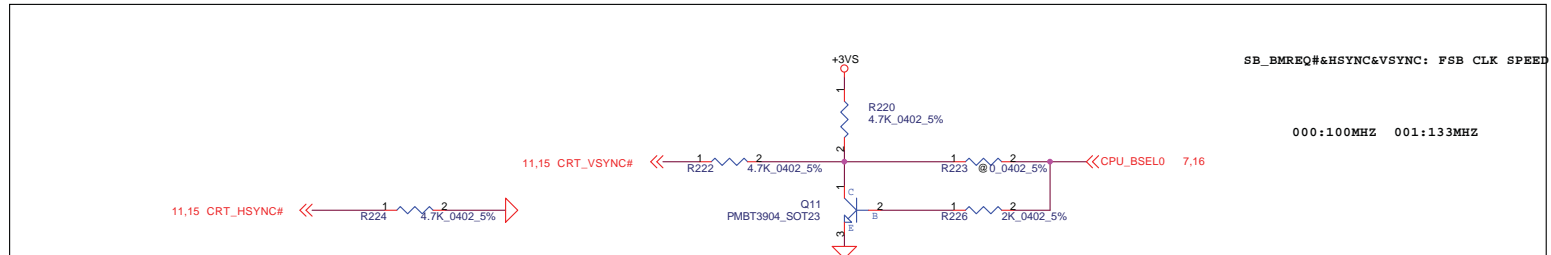
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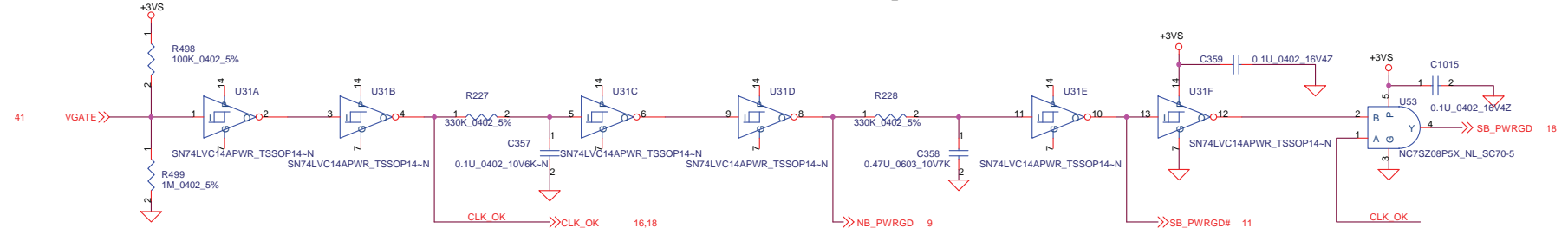


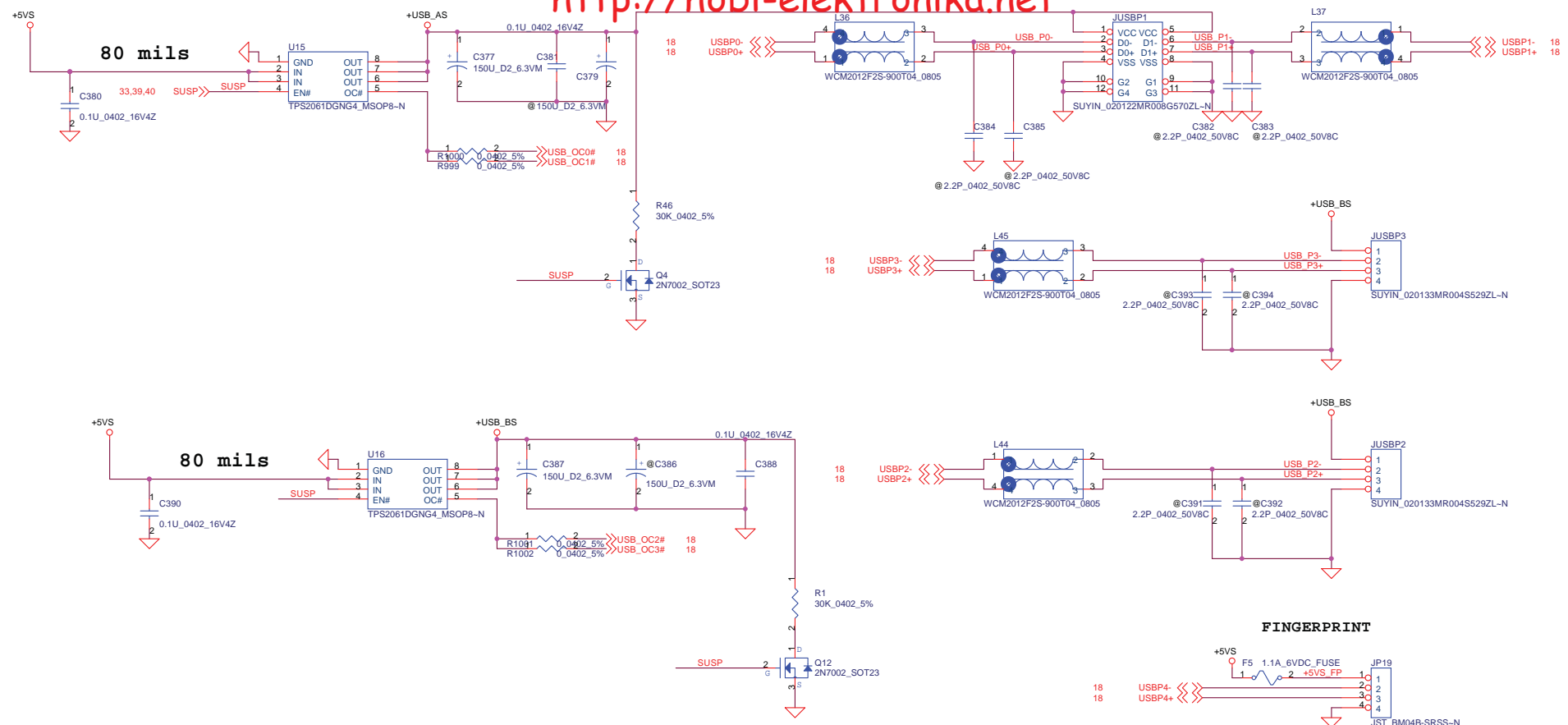
REQUIRED STRAPS

	AUTO_ON#	AC97_SDOOUT	RTC_CLK	SPDIF_OUT	PCI_CLK3	PCI_CLK4	PCI_CLK5	PCI_CLK6	PCI_CLK7	PCI_CLK8	SB_BMREQ#	MEM_STRAP	STRAP_EEPROM
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	USB PHY PWRDOWN DISABLE	Use internal PLL for 48MHZ	PCIE_CM SET LOW	CPU I/F = AMD	ROM TYPE H,H = PCI ROM H,L = PMC LPC ROM DEFAULT			1.8V DDR	EEPROM STRAP
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz DEFAULT	USB PHY PWRDOWN ENABLE DEFAULT	48MHz XTAL MODE DEFAULT	PCIE_CM SET HIGH DEFAULT	CPU I/F = INTEL DEFAULT	L,H = NORMAL LPC ROM L,L = FWH ROM		0 = NORMAL (Default)	2.5V DDR	MEM CHANNEL

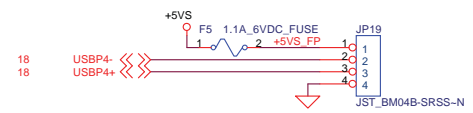


U32-->please close to SB400(U16)

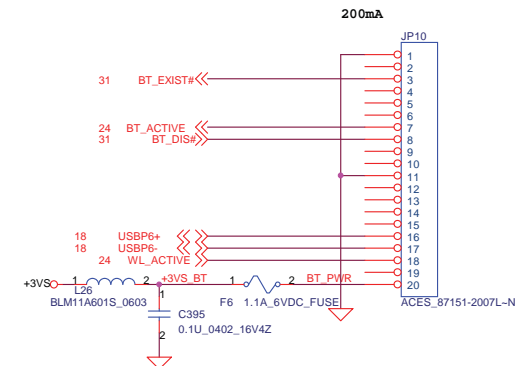




FINGERPRINT



BLUETOOTH



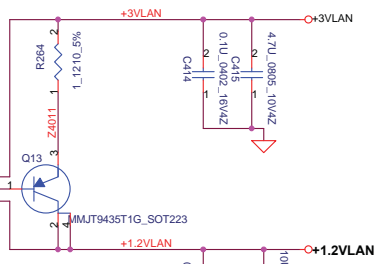
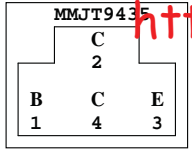
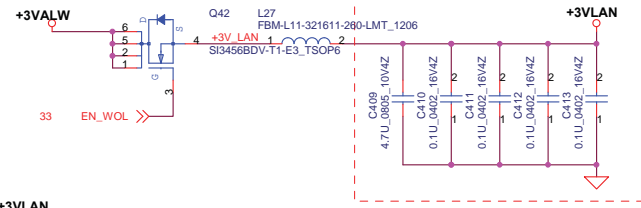
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file: **SCHEMATIC, M/B LA-2642P**

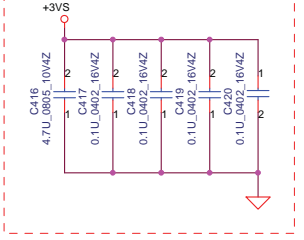
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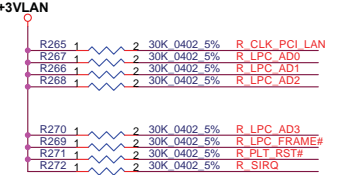
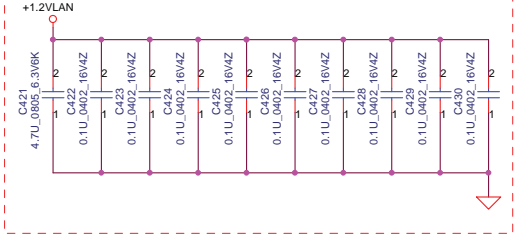
Layout Notice : Place as close chip as possible.



Layout Notice : 3.3V filter. Place as close chip as possible.

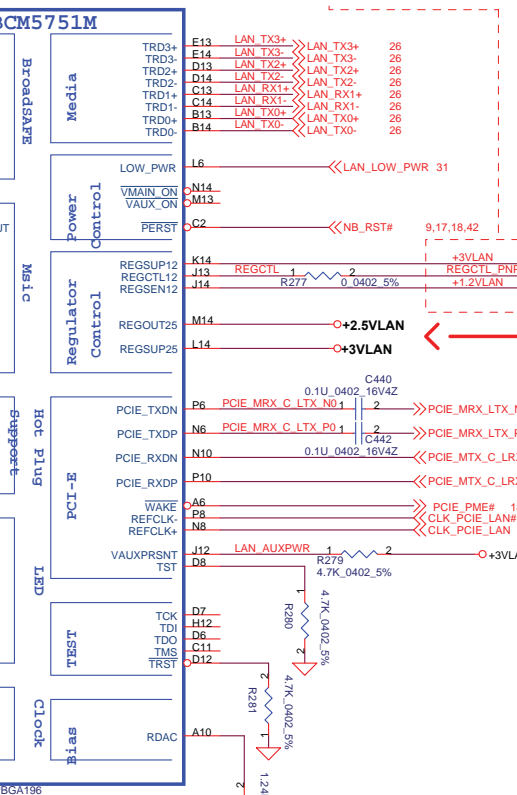
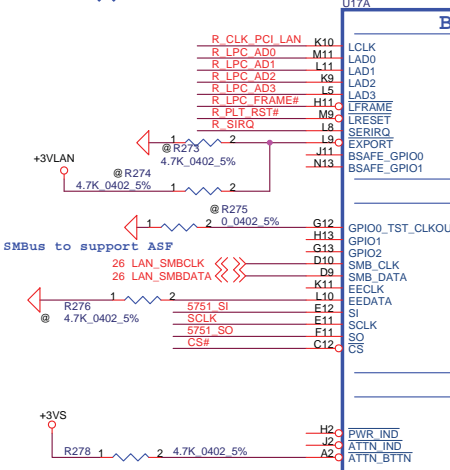


Layout Notice : 1.2V filter. Place as close chip as possible.

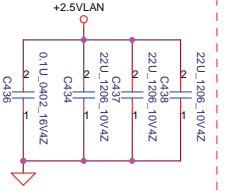


Pin L9, if TPM supported, Pull down via 4.7K resistor. L09 floating to disable TPM function.

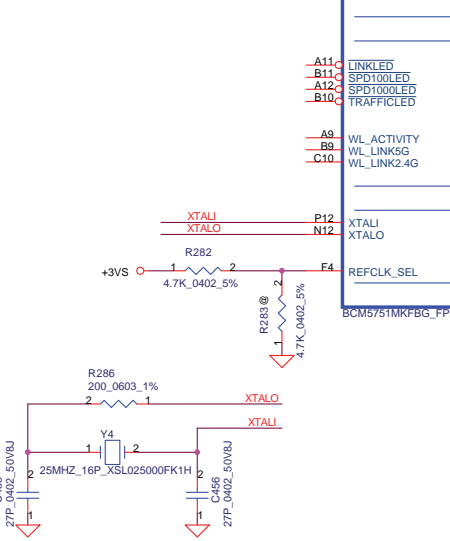
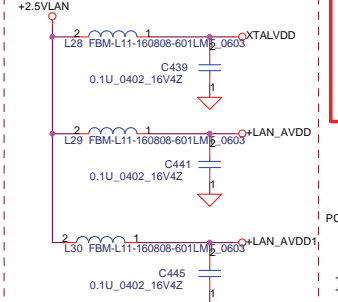
Pin L06:Low Power Mode Driven High-IDDD Mode(less than 20mA) Driven Low-Normal Mode



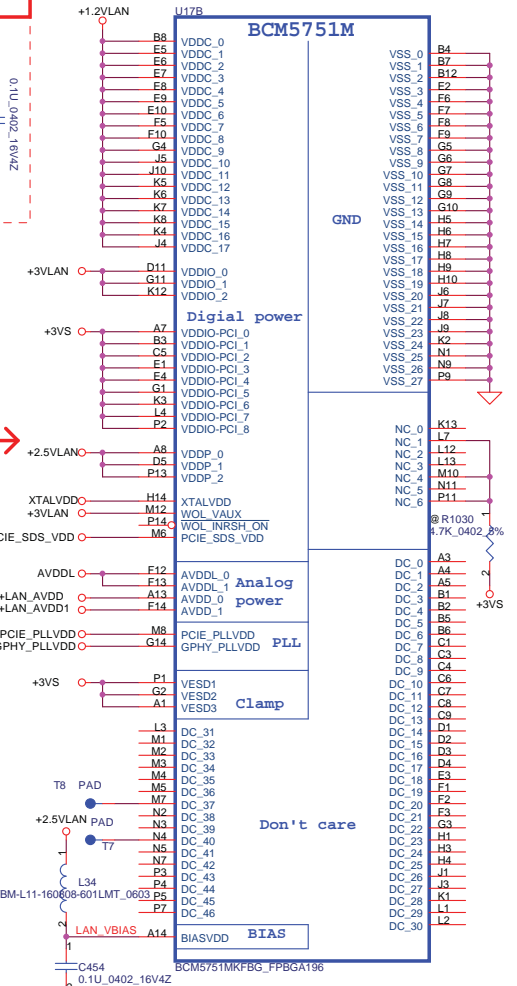
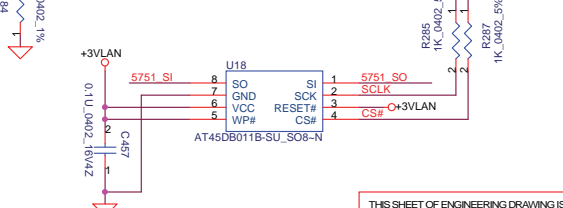
Layout Notice : Place as close chip as possible.



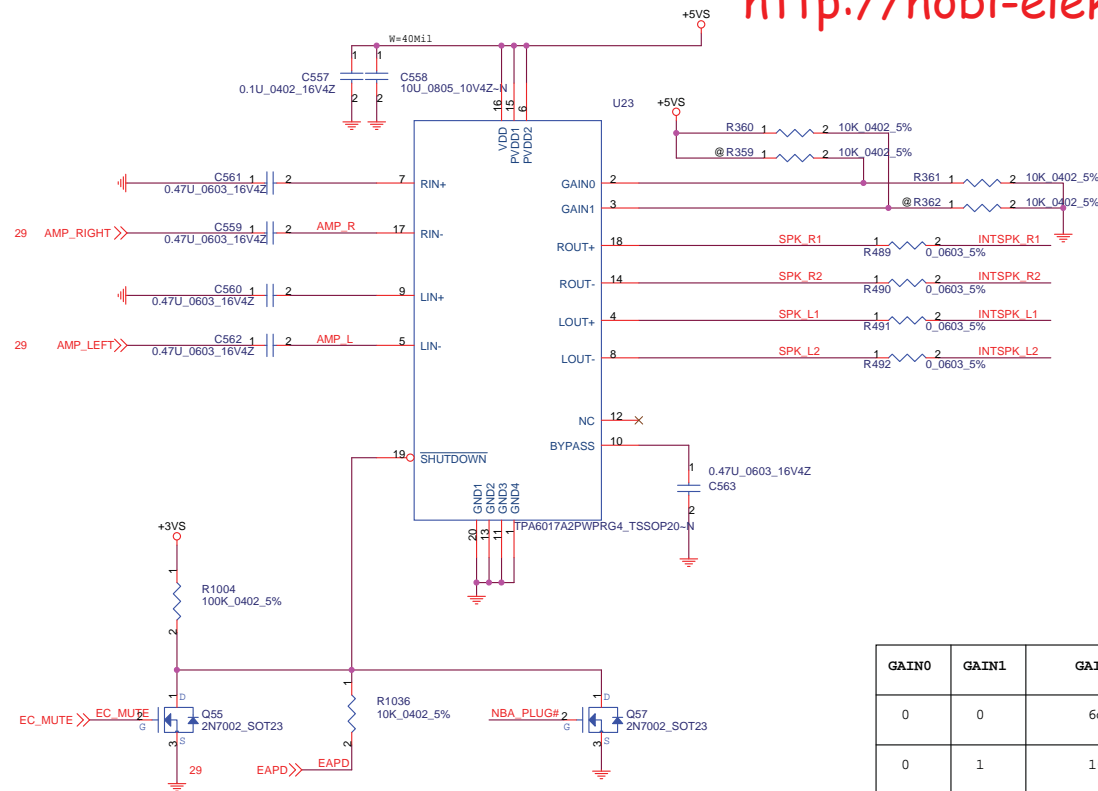
Layout Notice : Filter place as close chip as possible.



Layout Notice : No high speed signal should be routed near RDAC or on adjacent layer to RDAC

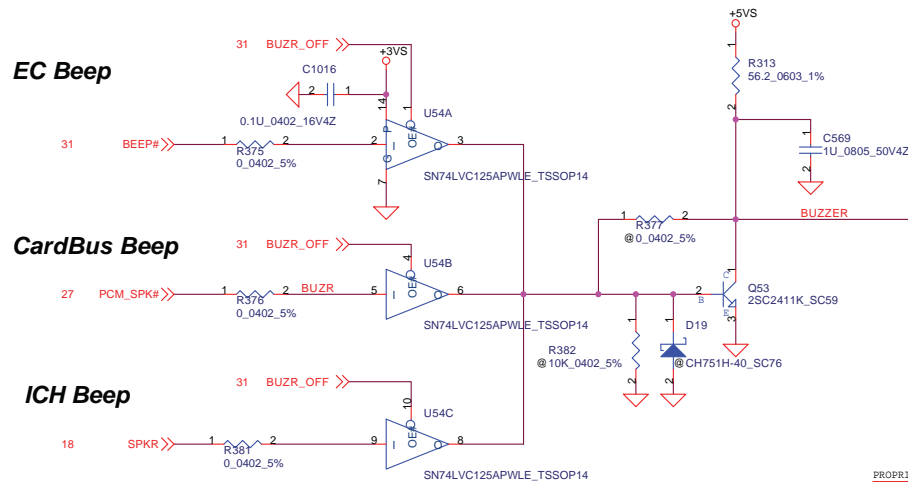


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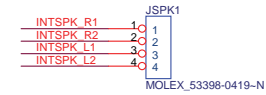


GAIN0	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

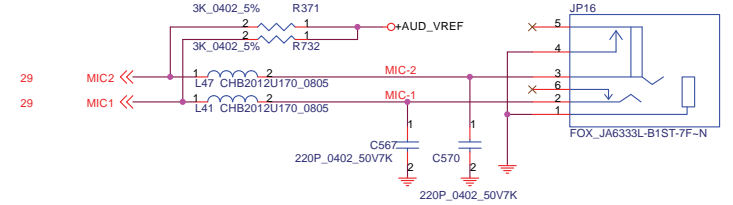
Buzzer need to support ICH/PCM_SPK/Battery_low and WL_on/off



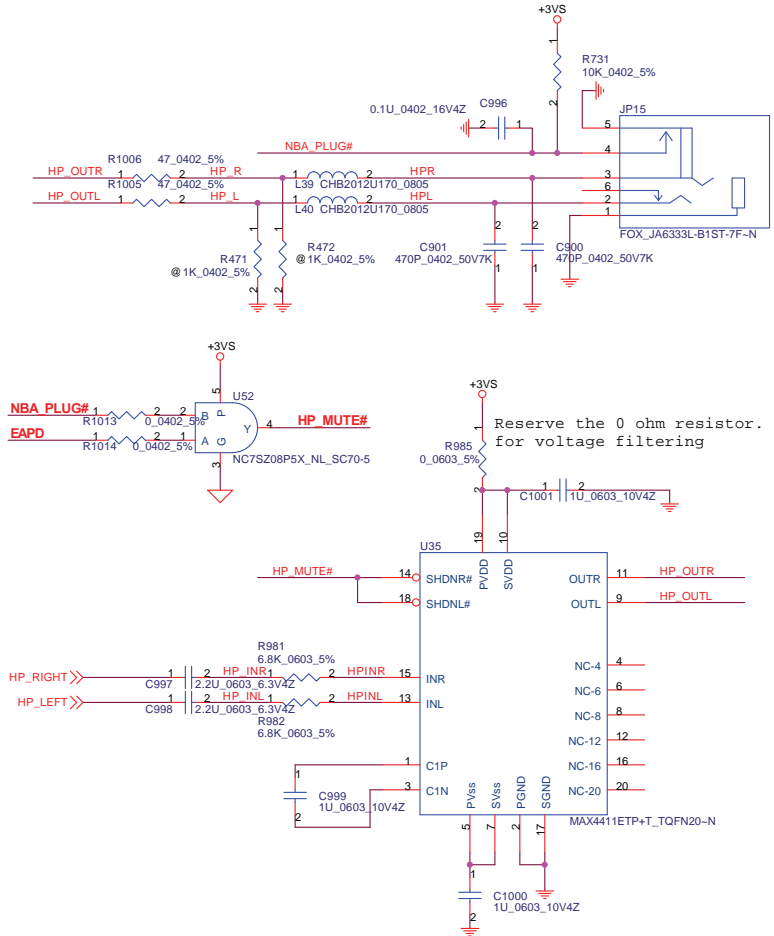
Speaker Connector



MICROPHONE IN JACK



HEADPHONE OUT JACK



PROPRIETARY NOTE

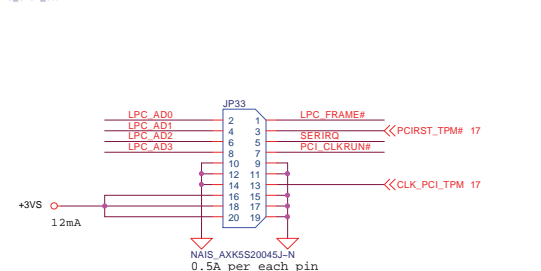
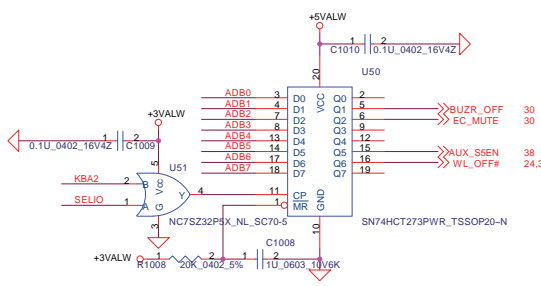
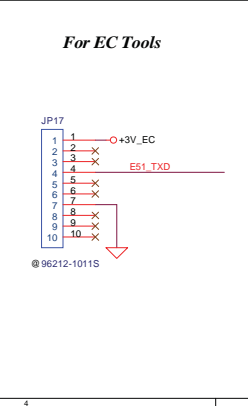
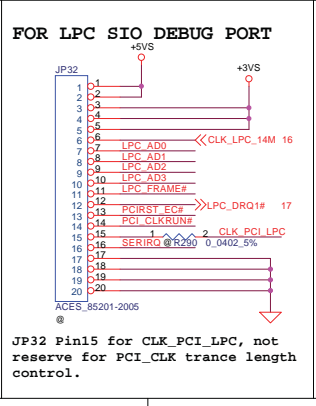
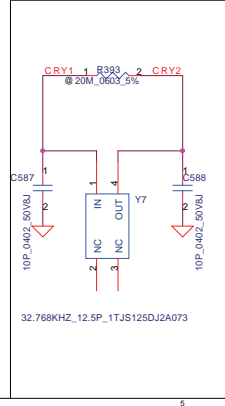
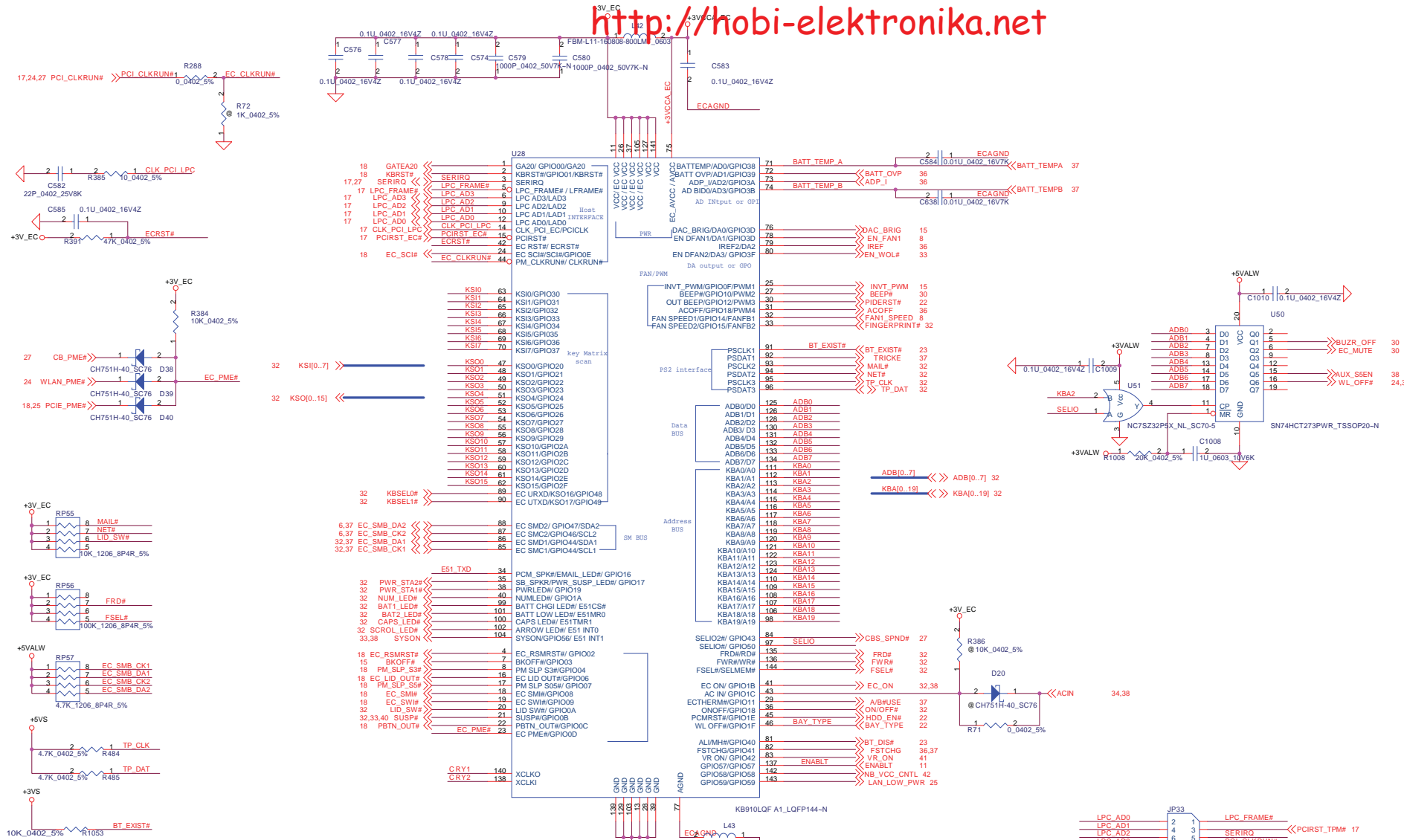
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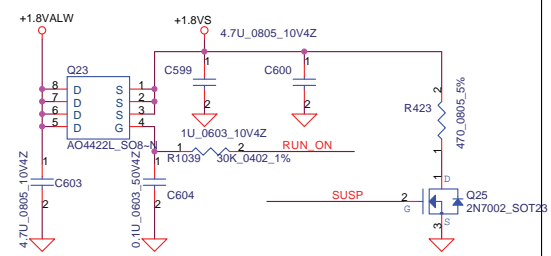
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Size 401380

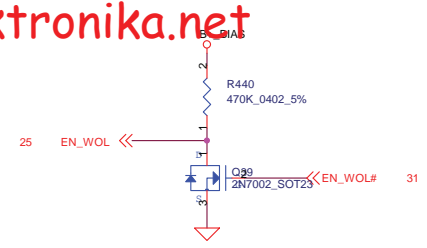
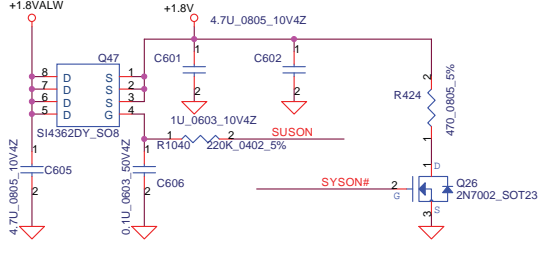
Rev B



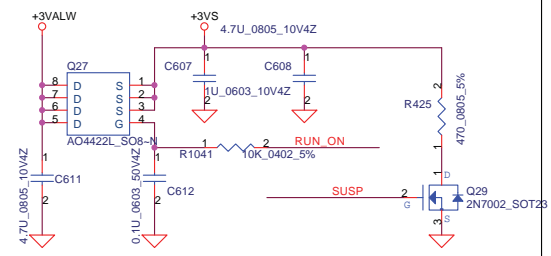
+1.8VALW TO +1.8VS



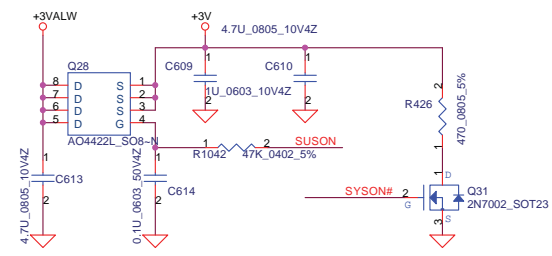
+1.8VALW TO +1.8V



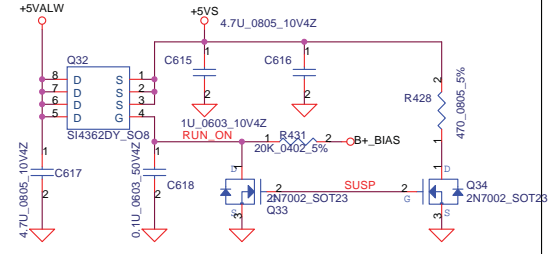
+3VALW TO +3VS



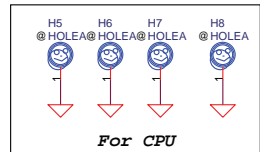
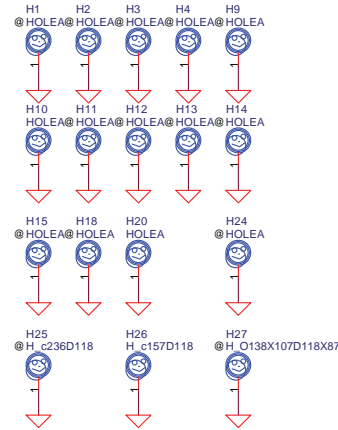
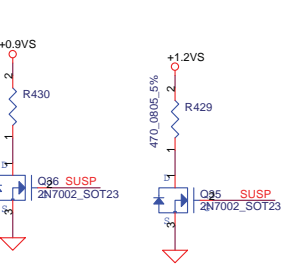
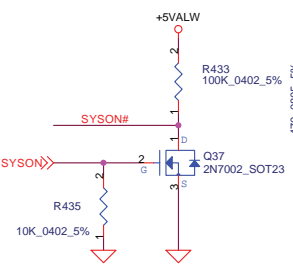
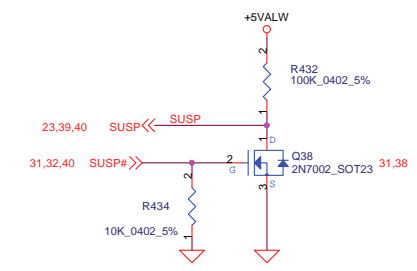
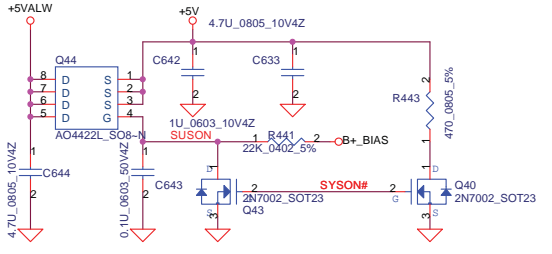
+3VALW TO +3V



+5VALW TO +5VS



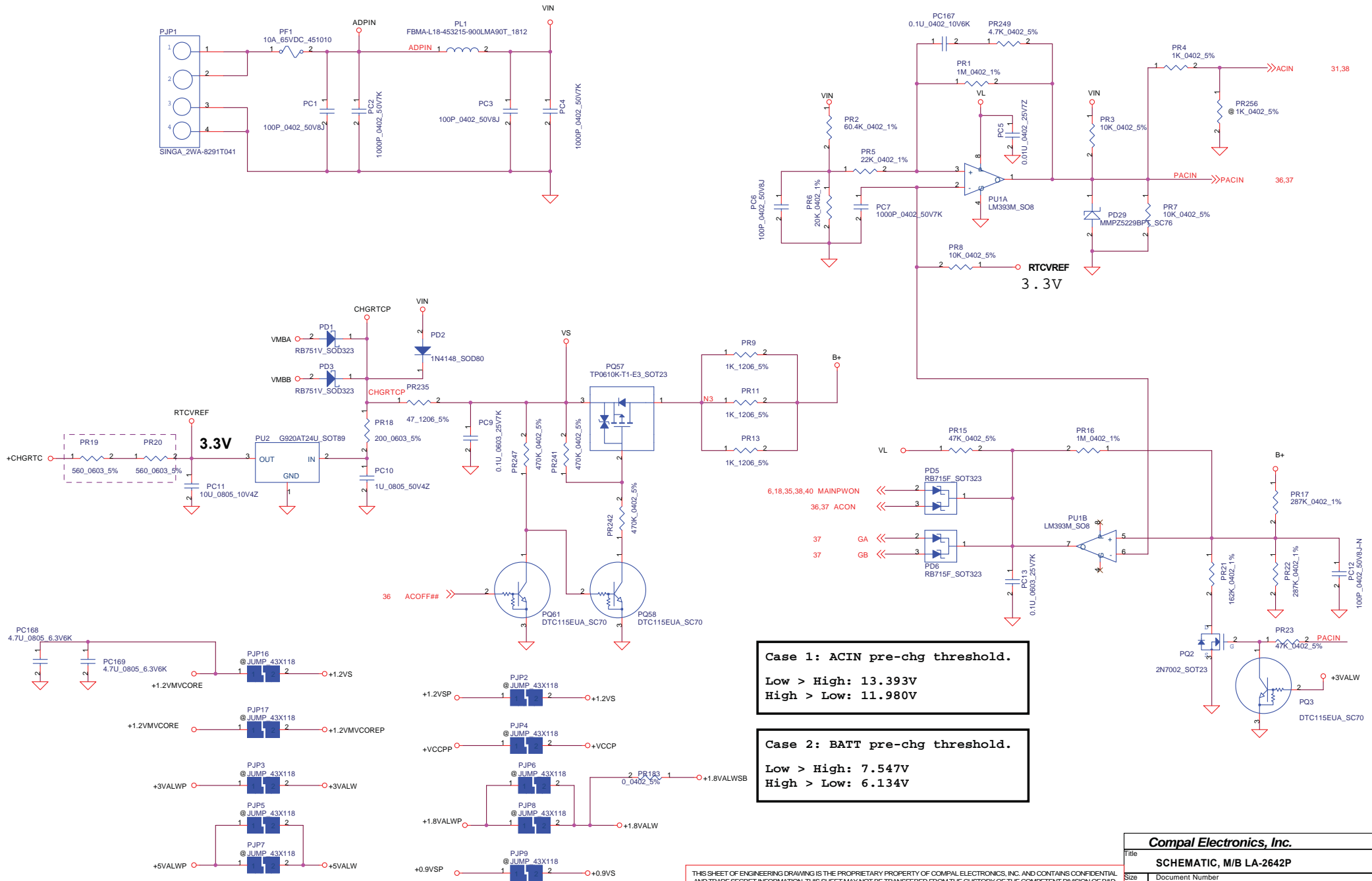
+5VALW TO +5V



Vin Detector Threshold:

Low > High: 13.757V

High > Low: 13.160V



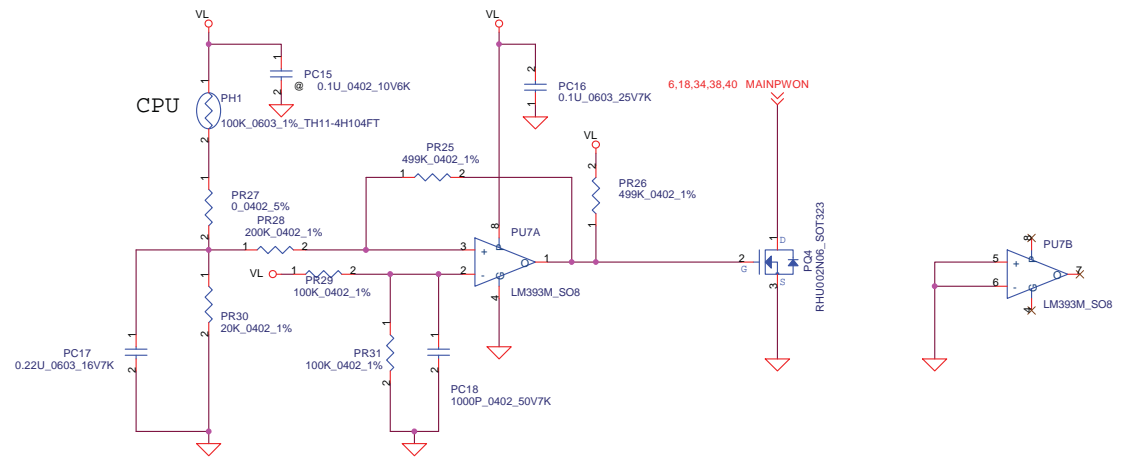
Case 1: ACIN pre-chg threshold.
 Low > High: 13.393V
 High > Low: 11.980V

Case 2: BATT pre-chg threshold.
 Low > High: 7.547V
 High > Low: 6.134V

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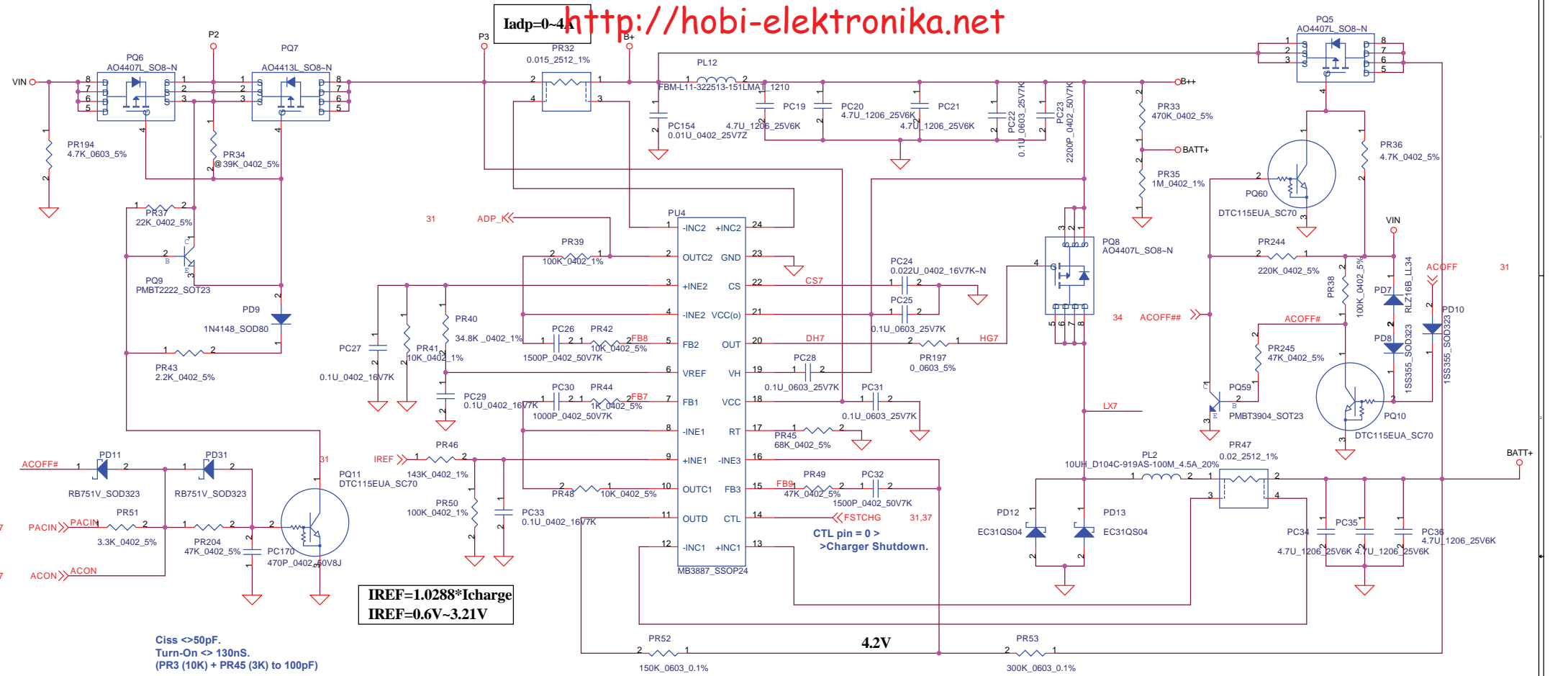
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PH1 under CPU botten side :
 CPU thermal protection at 86 +-3 degree C
 Recovery at 51 +-3 degree C



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IREF=1.0288*Icharge
IREF=0.6V~3.21V

Ciss < 50pF.
 Turn-On < 130nS.
 (PR3 (10K) + PR45 (3K) to 100pF)

Vadp=15V

I limit: 3.72A

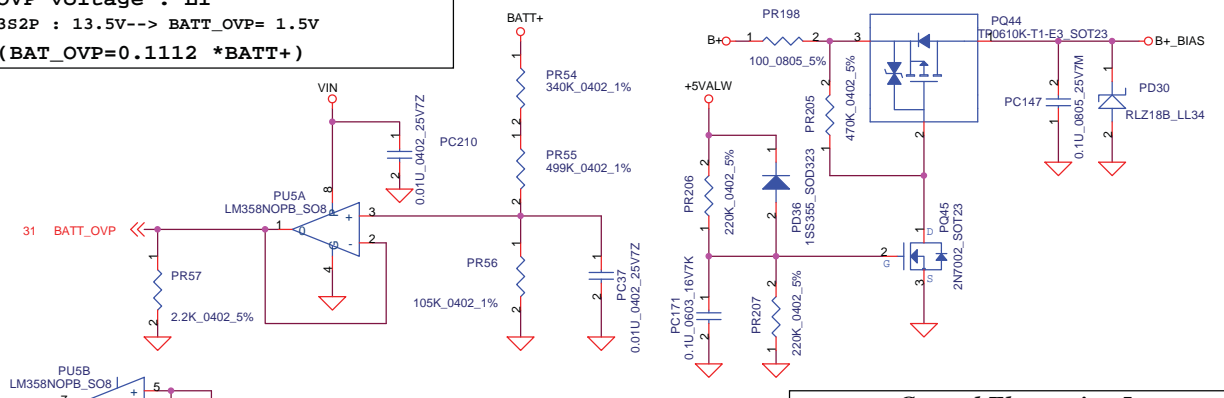
D.A.C.A. (C.P.) on 60W adaptor: Take PR41= 10K
 $4A * 0.015 * 20 = 5 * PR41 / (PR41 + PR40) \Leftrightarrow PR40 < 34.8K$

Fast charge current < 3.3A,
 $3.3A * 0.02 * 20 / [(3.21V - 3.3A * 0.02 * 20) / PR46] \Leftrightarrow PR50$
 PR46 < 143K

Trickle charge current < 0.6A,
 $0.6A * 0.02 * 20 / [(0.6V - 0.6A * 0.02 * 20) / PR46] \Leftrightarrow PR50$
 PR46 < 143K

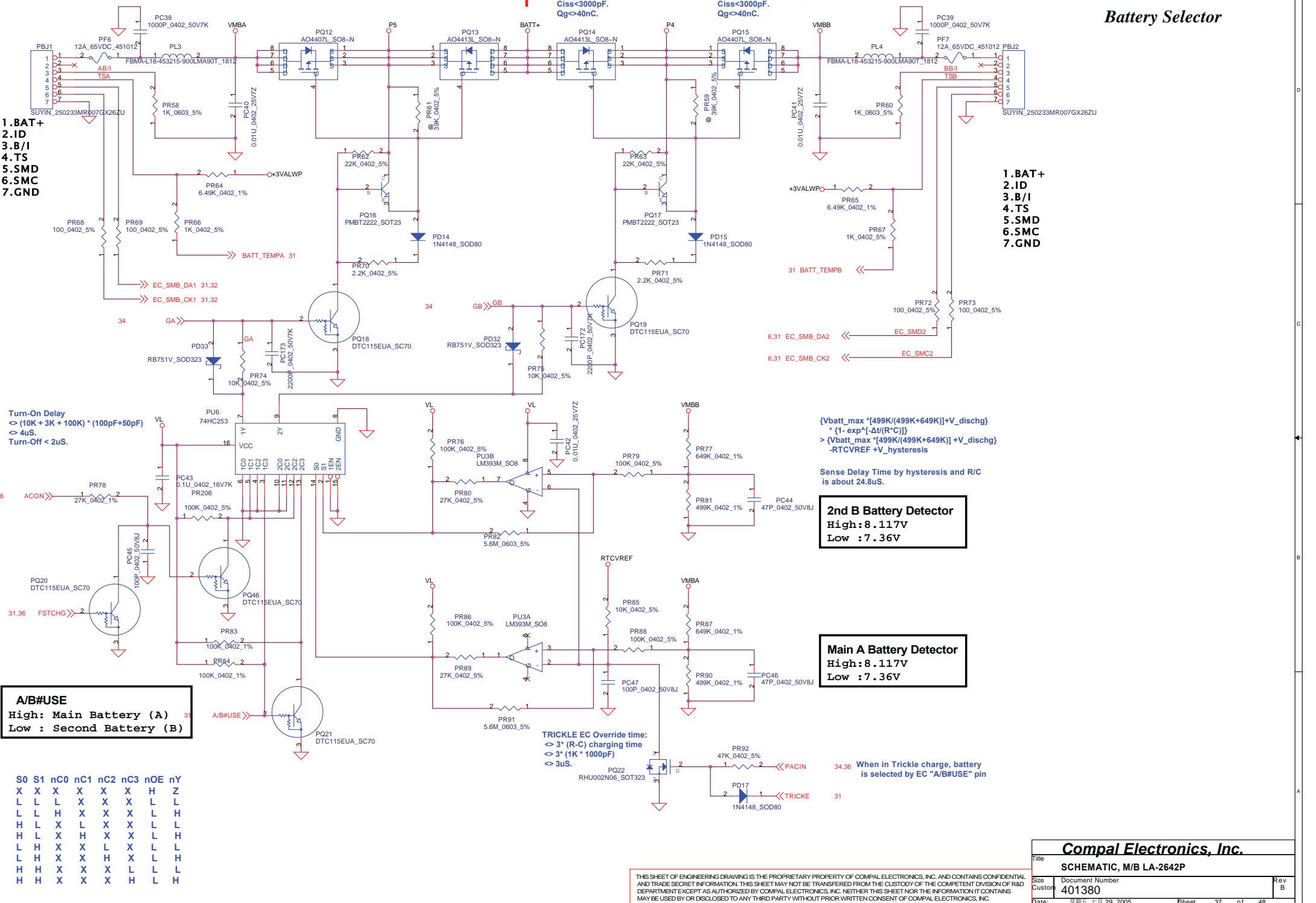
OVP voltage : LI
3S2P : 13.5V--> BATT_OVP= 1.5V
(BAT_OVP=0.1112 *BATT+)

CC=0.6-3.3A
CV=12.6V(6 CELLS LI-ION)



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- 1. BAT+
- 2. ID
- 3. B/I
- 4. TS
- 5. SMD
- 6. SMC
- 7. GND

- 1. BAT+
- 2. ID
- 3. B/I
- 4. TS
- 5. SMD
- 6. SMC
- 7. GND

Turn-On Delay
 $\approx (10K + 3K + 100K) \cdot (100pF + 50pF)$
 $\approx 4\mu S$
 Turn-Off < 2 μS .

$$\{V_{batt_max} \cdot [499K / (499K + 649K)] + V_{dischg}\} \cdot \{1 - \exp^{-\Delta t / (R \cdot C)}\}$$

$$> \{V_{batt_max} \cdot [499K / (499K + 649K)] + V_{dischg}\} - RTCVREF + V_{hysteresis}$$

Sense Delay Time by hysteresis and R/C is about 24.8 μS .

2nd B Battery Detector
 High : 8.117V
 Low : 7.36V

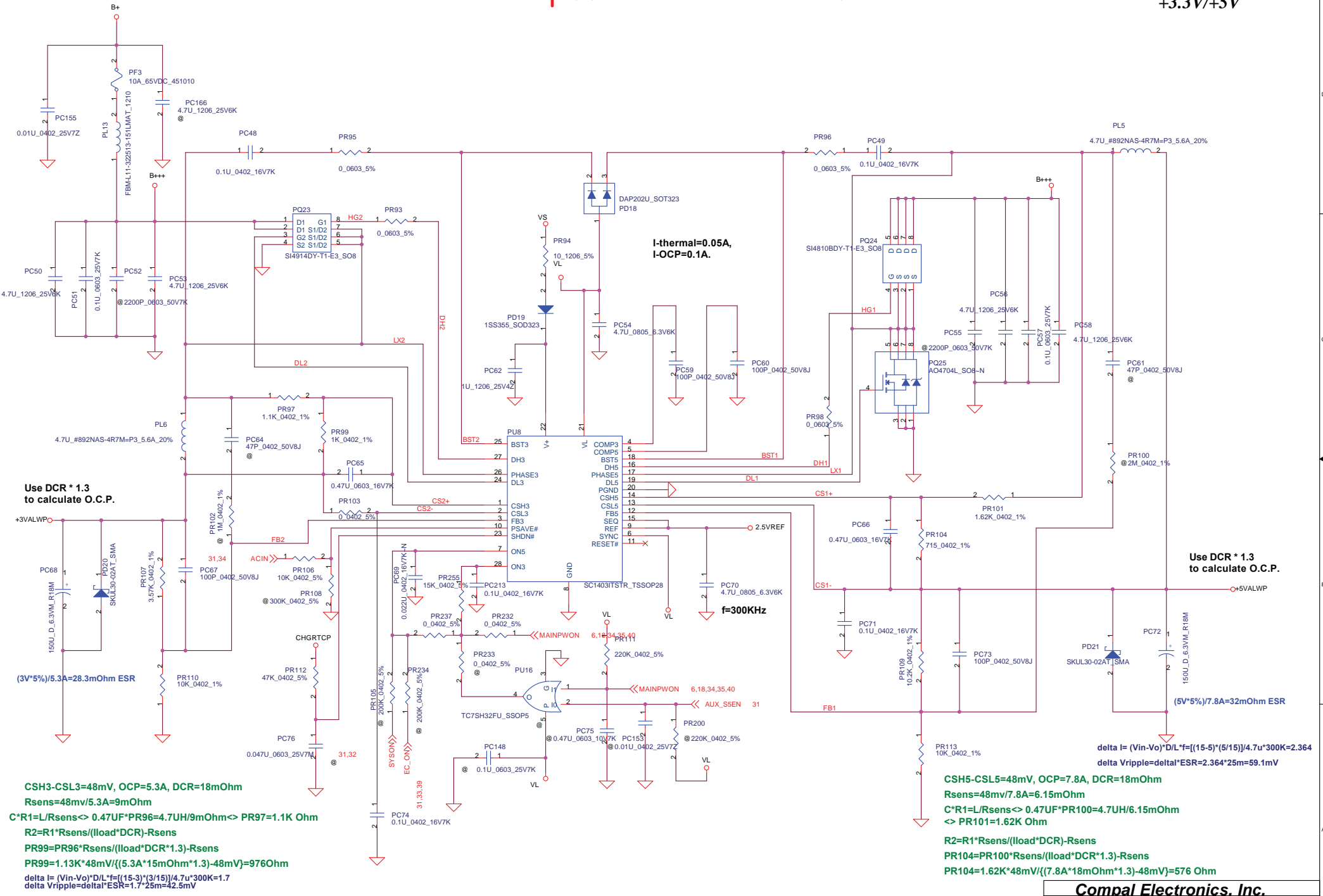
Main A Battery Detector
 High : 8.117V
 Low : 7.36V

A/B#USE
 High: Main Battery (A) 31
 Low : Second Battery (B)

S0	S1	nC0	nC1	nC2	nC3	nOE	nY
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	L	L	H

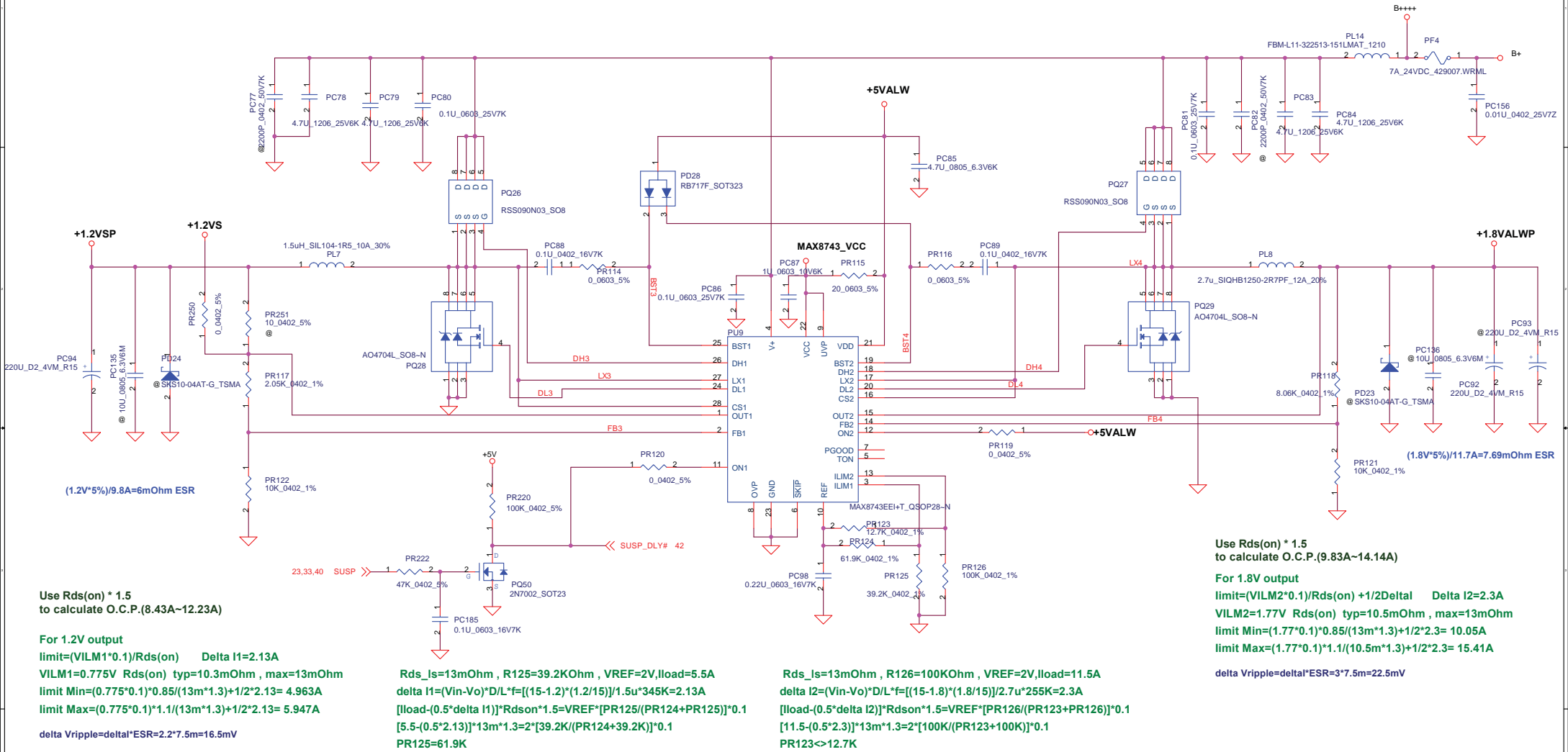
TRICKLE EC Override time:
 $\approx 3 \cdot (R \cdot C)$ charging time
 $\approx 3 \cdot (1K \cdot 1000pF)$
 $\approx 3\mu S$.

34,36 When in Trickle charge, battery is selected by EC "A/B#USE" pin



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Use $R_{ds(on)} * 1.5$ to calculate O.C.P. (8.43A~12.23A)

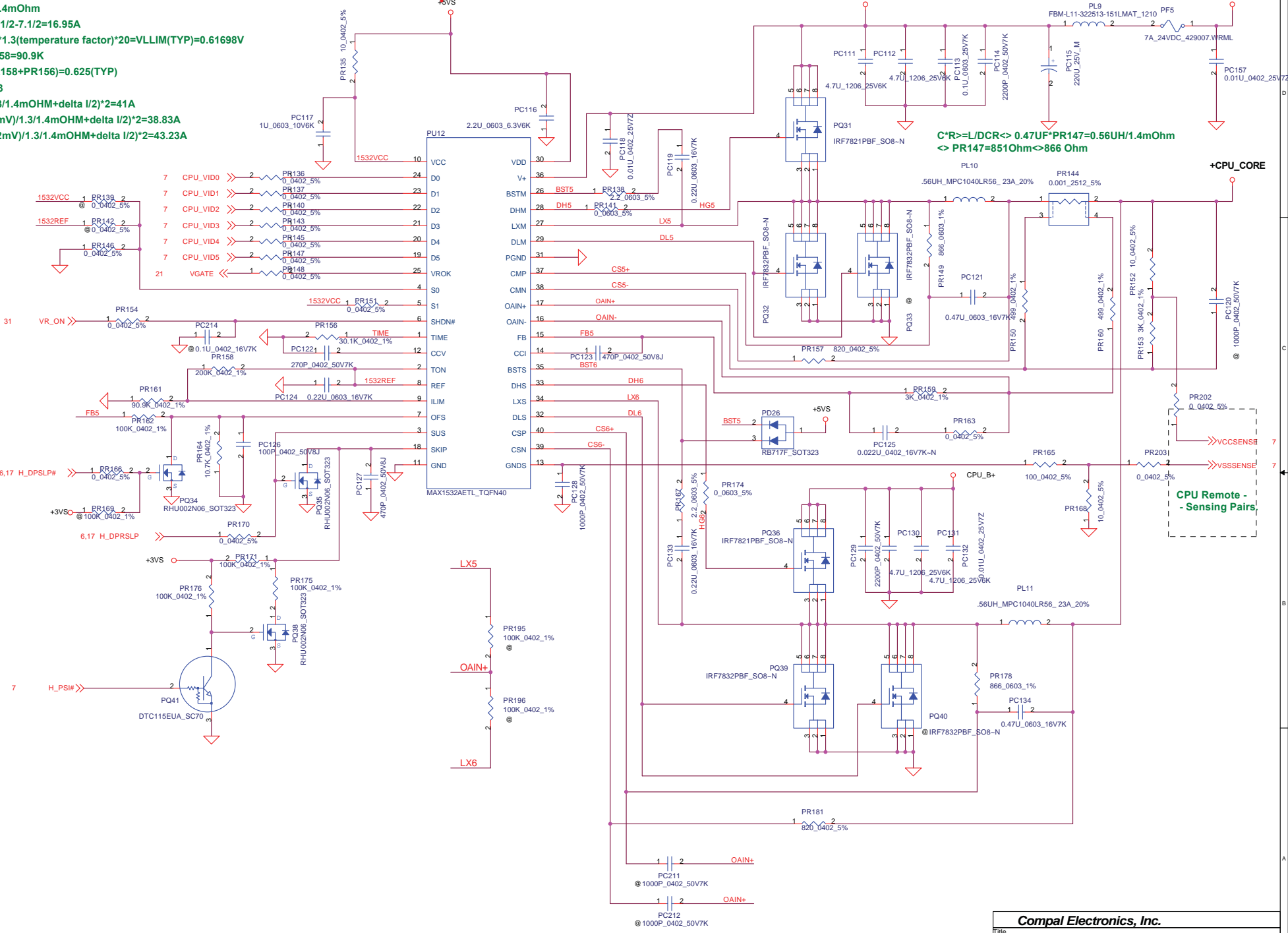
For 1.2V output
 $limit = (V_{ILM1} * 0.1) / R_{ds(on)}$ $\Delta I_1 = 2.13A$
 $V_{ILM1} = 0.775V$ $R_{ds(on)} \text{ typ} = 10.3m\Omega$, $\text{max} = 13m\Omega$
 $limit \text{ Min} = (0.775 * 0.1) * 0.85 / (13m * 1.3) + 1/2 * 2.13 = 4.963A$
 $limit \text{ Max} = (0.775 * 0.1) * 1.1 / (13m * 1.3) + 1/2 * 2.13 = 5.947A$
 $\Delta I_{\text{Ripple}} = \Delta I_1 * ESR = 2.2 * 7.5m = 16.5mV$

$R_{ds_{is}} = 13m\Omega$, $R_{125} = 39.2K\Omega$, $V_{REF} = 2V$, $I_{load} = 5.5A$
 $\Delta I_1 = (V_{in} - V_o) * D / L * f = [(15 - 1.2) * (1.2 / 15)] / 1.5u * 345K = 2.13A$
 $[I_{load} - (0.5 * \Delta I_1)] * R_{ds(on)} * 1.5 = V_{REF} * [PR_{125} / (PR_{124} + PR_{125})] * 0.1$
 $[5.5 - (0.5 * 2.13)] * 13m * 1.3 = 2 * [39.2K / (PR_{124} + 39.2K)] * 0.1$
 $PR_{125} = 61.9K$

$R_{ds_{is}} = 13m\Omega$, $R_{126} = 100K\Omega$, $V_{REF} = 2V$, $I_{load} = 11.5A$
 $\Delta I_2 = (V_{in} - V_o) * D / L * f = [(15 - 1.8) * (1.8 / 15)] / 2.7u * 255K = 2.3A$
 $[I_{load} - (0.5 * \Delta I_2)] * R_{ds(on)} * 1.5 = V_{REF} * [PR_{126} / (PR_{123} + PR_{126})] * 0.1$
 $[11.5 - (0.5 * 2.3)] * 13m * 1.3 = 2 * [100K / (PR_{123} + 100K)] * 0.1$
 $PR_{123} < 12.7K$

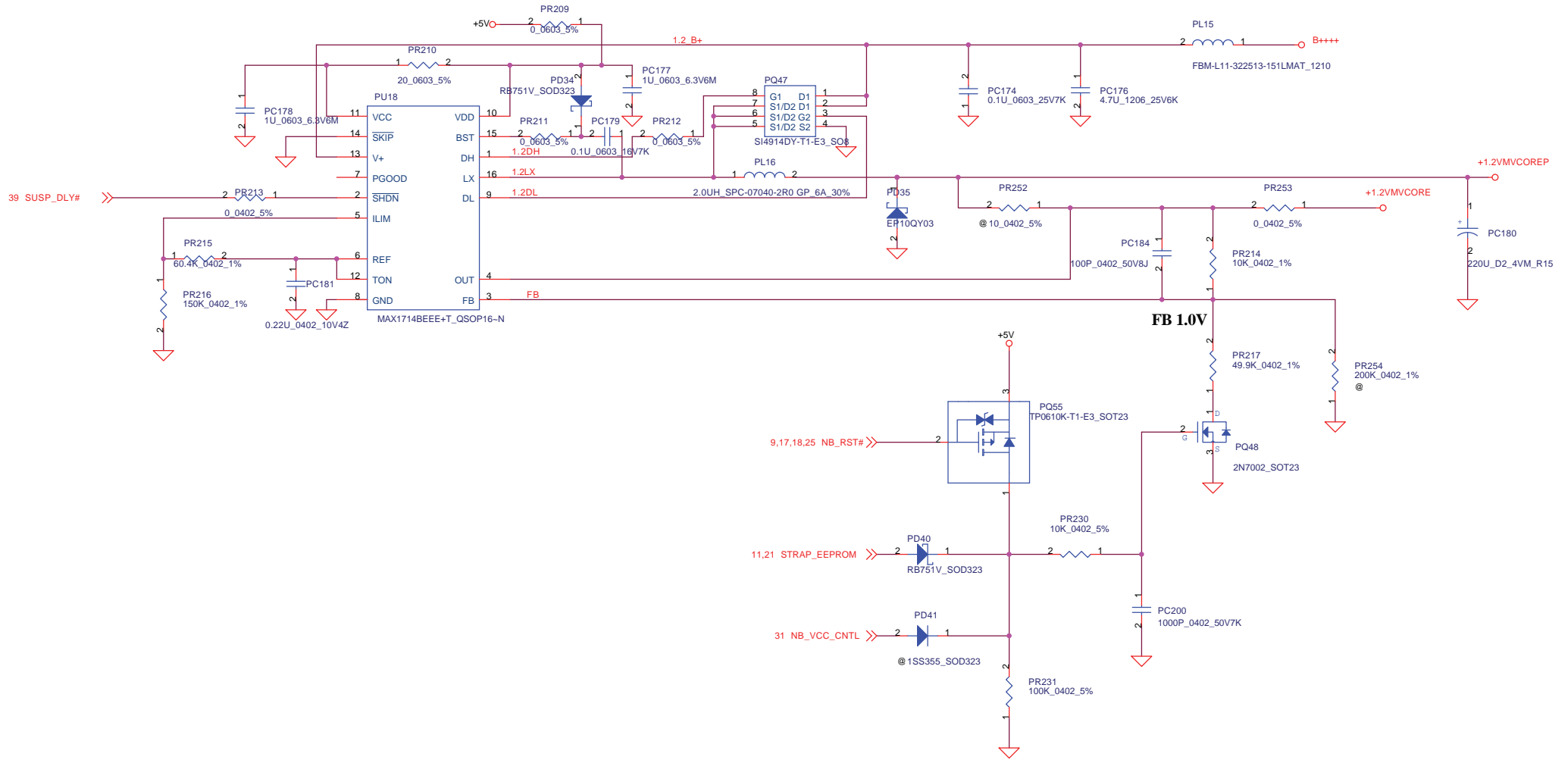
Use $R_{ds(on)} * 1.5$ to calculate O.C.P. (9.83A~14.14A)
 For 1.8V output
 $limit = (V_{ILM2} * 0.1) / R_{ds(on)}$ $\Delta I_2 = 2.3A$
 $V_{ILM2} = 1.77V$ $R_{ds(on)} \text{ typ} = 10.5m\Omega$, $\text{max} = 13m\Omega$
 $limit \text{ Min} = (1.77 * 0.1) * 0.85 / (13m * 1.3) + 1/2 * 2.3 = 10.05A$
 $limit \text{ Max} = (1.77 * 0.1) * 1.1 / (13m * 1.3) + 1/2 * 2.3 = 15.41A$
 $\Delta I_{\text{Ripple}} = \Delta I_2 * ESR = 3 * 7.5m = 22.5mV$

$\Delta I = (V_{in}-V_o) \cdot D/L \cdot f = [(15-1.308)/(1.308/15)] / (.56 \mu \cdot 300K) = 7.1A$
OCP=41A(TYP), DCR=1.4mOhm
Ilimit(min) per phase=41/2-7.1/2=16.95A
16.95A*1.4mOHM(DCR)*1.3(temperature factor)*20=VLLIM(TYP)=0.61698V
Take PR156=200K, PR158=90.9K
VILIM=VREF*PR158/(PR158+PR156)=0.625(TYP)
VILIM/20=Ilimit*DCR*1.3
OCP(TYP)=(0.625/20/1.3/1.4mOHM+delta I/2)*2=41A
OCP(min)=(0.625/20-2mV)/1.3/1.4mOHM+delta I/2)*2=38.83A
OCP(max)=(0.625/20+2mV)/1.3/1.4mOHM+delta I/2)*2=43.23A



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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	6	Pentium-M(1/3)	Nov. 19th	Compal	Correct circuit.	Add R1031	0.2
2	9, 17, 25	RS400MD-FSB/A-PCIE(1/4) SB400-PCIE/PCI/LPC/RTC(1/4) BCM5751M-GLAN	Nov. 19th	Compal	Correct net name	Easy to identify net connection between RS400MD and SB400/BCM5751M	0.2
3	8	CPU Decoupling/FAN(3/3)	Nov. 19th	Compal	U2.1 and U2.3 is short together.	Correct net name of U2.3	0.2
4	21	Hardware Trap	Nov. 19th	Compal	Fix it to follow SB400 A31 request	Change the status of PCI_CLK2 to low	0.2
5	24	MINI_PCI SLOT-WLAN	Nov. 19th	Compal	Follow Compal standard design	Change the IRQ routing to IRQF# and IRQG#	0.2
6	18	P18-SB400-USB/AC97/MISC.(2/4)	Nov. 19th	Compal	Different power plane maybe cause some leakage.	Correct Power plane from +3valv to +3v to match USB_PHY_1.8v plane	0.2
7	25	BCM5751M-GLAN	Nov. 19th	Compal	For Debug	Reserve Pull-up R1030.	0.2
8	31	ENE-KB910L/TPM	Nov. 19th	Compal	Fix S5 boot function and sequence	Correct AUXS5_EN# and VGATE and VGATE_EC control type	0.2
9	32	BIOS/EE-Prom/TP/KB/SW	Nov. 19th	Compal	Re-assign K/B ESD cap	Deleted C592.	0.2
10	33	DC TO DC	Nov. 22th	Compal	Follow M/E requirement	Deleted H16, H17, H23	0.2
11	11	RS400MD-DISPLAY(3/4)	Nov. 22th	Compal	LCD Backlight can't function.	Change the control signal from BLEN* U3.D7* to BLON* U3.A6.	0.2
12	22	IDE/CD_ROM Conn.	Nov. 22th	Compal	correct the Poly-fuse spec for HDD requirement.	Change the Poly-fuse from 1.1A to 1.8A	0.2
13	25 31	BCM5751M-GLAN ENE-KB910L/TPM	Nov. 22th	Compal	Reserved GPIO of KB910L for other function	Change the GLAN reset timing by A_RST# signal.	0.2
14	29	AC97 Codec AD1981B/MDC	Nov. 24th	Compal	MDC be changed.	Correct pin definition	0.2
15	16	ClockGen ICS951413	Nov. 24th	Compal	ICS951411 will function fail with CPU Speedstep	Change Clock Gen from ICS951411 to ICS951413	0.2
16		RS400MD & SB400	Nov. 24th	Compal	For Lead-free process	Change RS400MD & SB400 to Lead-Free part.	0.2
17	30	AMP./Audio Jack	Nov. 24th	Compal	To smooth the Cable routing	Swap Left and Right sound signals.---JSPK1	0.2
18	31	ENE-KB910L/TPM	Nov. 24th	Compal	Separate TPM to Module type	Removed TPM Chip and add JP23	0.2
19	23	USB/BlueTooth/FP	Nov. 25th	Compal	Bluetooth be changed	Correct connector" JP10" pin define and type.	0.2
20	32	BIOS/EE-Prom/TP/KB/SW	Nov. 25th	Compal	For M/E Requirement	Change the connecotr type" JPALM1" from Cable to FFC.	0.2
21	11	RS400MD-DISPLAY(3/4)	Nov. 25th	Compal	Reserved EEPROM" U49" debugging	Delete reserved circuit for PP phase	0.2
22	11	RS400MD-DISPLAY(3/4)	Nov. 25th	Compal	Reserved R508 for debugging	Delete R508 for PP phase	0.2
23	15	TV-OUT/LVDS/CRT	Nov. 25th	Compal	Reservd Resistors for LCD EDID	Update the R87, R88, R506, R507, R504 and R505 status for PP phase. Delete R1032 and R1049 at page 11	0.2
24			Nov. 25th	Compal	Reserved for PWR consumption measurement.	Delete R63, R189, JOPEN2, JOPEN3 and JOPEN4.	0.2
25	30	AMP./Audio Jack	Nov. 25th	Compal	Beep function fail	Correct Beep circuit	0.2
26	15	TV-OUT/LVDS/CRT	Nov. 25th	Compal	Lack of this part in vendor side	Change C907 from 0.1U_0402_25V4K to 0.1U_0805_50V.	0.2

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
27	22	IDE/CD_ROM Conn.	Nov. 30th	NEC	For safety	Add F4* Fuse* for ODD	0.2
28	15	TV-OUT/LVDS/CRT	Dec. 1st	Compal	CRT Function abnormal	Change the D12 to correct library	0.2
29	23	USB/BlueTooth/FP	Dec. 6th	NEC	For Safety.	Add Poly-Fuse for B/T and F/P.	0.2
30	30	AMP./Audio Jack	Dec. 6th	Compal	Correct Buzzer drive circuit	Remove serial Resistor, Capacitor and Transistor. Change to Buffer to separate the signals and improve the driving capacity.	0.2
31	6	Pentium-M(1/3)	Dec. 7th	Compal	Correct Thermal trip timing	Change R27 from 47k to 100k and fine-tune pwr sequense between +1.5vs and VCCP.	0.2
32			Dec. 8th	EMI	PCI Clock will cause EMI issue.	Add AC-termination 10-ohm and 22pf for PCI Clocks.	0.2
33	30	AMP./Audio Jack	Dec. 8th	Compal	1. Follow Buzzer voltage range 2V ~ 4V requirement 2. Follow NEC Audio team test result for HP signals.	1. Change the pull-up power to +3VS. 2. Change R1005 & R1006 from 0-ohm to 47-ohm	0.2
34	31	ENE-KB910L/TPM	Dec. 8th	Compal	Correct Extension IO control signal.	Change the control signal of U51A from KBA1 to KBA2	0.2
35	29	AC97 Codec AD1981B/MDC	Dec. 8th	EMI	EAPD will cause EMI issue with 197MHz	Change Resistor' R494' to Bead' L56'	0.2
36	23	USB/BlueTooth/FP	Dec. 9th	EMI	USB EMI problem	Add Common Choke for USB port	0.2
37	22	IDE/CD_ROM Conn.	Dec. 9th	EMI	Pin A24 ~ A26 will over 10dB for EMI	Add bypass capacitors' 1000p.	0.2
38	15	TV-OUT/LVDS/CRT	Dec. 10th	EMI	Reserved R to measure pwr consumption	Delete R488.	0.2
39	22	IDE/CD_ROM Conn.	Dec. 13th	NEC	For ODD Module Safety	Correct the Fuse with 3A for ODD	0.2
40	31	ENE-KB910L/TPM	Dec. 13th	Compal	For Power Play function	Reserved NB_VCC_CNIL for Power Play circuit.	0.2
41	22 33	IDE/CD_ROM Conn. DC TO DC	Dec. 13th	Compal	Correct cap power rating for B+BIAS	Change cap from 0.1u_0402_16V to 0.1u_0805_50V.	0.2
42	18	P18-SB400-USB/AC97/MISC.(2/4)	Dec. 13th	Compal	Prevent leakage current for EC_SI# and EC_SCI# signals.	Change these signals pull-up from +3V to +3VLAW.	0.2
43	32	BIOS/EE-Prom/TP/KB/SW	Dec. 30th	Compal	Update the Battery mode power-on circuit.	Un-pop. R422, R421, Q22, Q21, D33, D43, D44 and C598.	0.3
45	6	Pentium-M(1/3)	Jan. 11th	Compal	Improve thermal trip timing.	Change R32 from 75 to 10-ohm.	0.3
46	31	ENE-KB910L/TPM	Jan. 11th	Compal	Correct Extension buffer function	Swap AUX_S5EN and TRICKE signal. Move HDD_EN# from extension buffer, U50, to KB910L. Move A/B#USE signal to KB910L and deleted EC_THERM.	0.3
47	31	ENE-KB910L/TPM	Jan. 12th	Compal	To save space and cost.	Change U51 from SN74LVC32APWR TSSOP14 to NC7SZ32P5X_NL SC70-5.	0.3
48	30	AMP./Audio Jack	Jan. 13th	Compal	To solve Int. Speaker GAIN issue.	Change the POWER source of R360 & R359 from +5VAMP to +5VS. +5VAMP is single Power plane.	0.3
49	24	MINI_PCI SLOT-WLAN	Jan. 13th	Compal	Correct net name for WL_OFF# signal.	Change the pull-up R, R1021, from D18.1 to D18.2. Correct the net name for WL_OFF# to prevent confuse.	0.3
50	32	BIOS/EE-Prom/TP/KB/SW	Jan. 14th	Compal	Follow NEC DPD R02 for DIP SW function	Remove USBSEL and CONFIG signals.	0.3
51	30	AMP./Audio Jack	Jan. 14th	NEC	To improve Audio Dolby quality.	Change the C997 & C998 to 2.2U.	0.3
52	08 22 33	CPU Decoupling/FAN(3/3) IDE/CD_ROM Conn. DC TO DC	Jan. 18th	POWER	To save cost for CPU Decoupling Caps. To Save Power consumption for Battery life. To Save Power consumption for Battery life.	Depopulated C29 Change R480 & R481 from 100k to 470k. Change R440 from 100K to 470K	0.3
53	27	R5C942-PCI/CARD BUS/OHCI	Jan. 19th	Compal	For Sn-Zn-Bi process.	Change Y5 from SJ124P5M500 to SJ124P5MF00 for Sn-Zn-Bi process.	0.3
54	23	USB/BlueTooth/FP	Jan. 20th	Compal	Solve USB leakage voltage problem.	Add Dis-charge circuit R46, R1, Q4 and Q12.	0.3

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27	23	USB/BlueTooth/FP	Jan. 21th	Compal	For EMI	Add Common Chock to solve the issue.	0.3
28	30	AMP./Audio Jack	Jan. 24th	Vendor	To prevent leakage from +AUD_VREF	Float JP16 pin6.	0.3
30	12	RS400MD-PWR/GND(4/4)	Jan. 26th	Compal	improve the +1.2VSA and +1.2VMCOORE be stability.	Add C1020 & C172 to solve +1.2VSA and +1.2VMCOORE voltage drop issue.	0.3
31	08	CPU Decoupling/FAN(3/3)	Jan. 26th	Compal	To improve Battery Life when S4/S5 status.	Add Q56' SB570020000' and R68' SD028100100,Change Q52 to SB934430000.	0.3
32	18	SB400-USB/AC97/MISC.(2/4)	Jan. 26th	ATI	Work around for CKE# Glitch.	Add D21 & D22 with SC1H751H000.	0.3
33	8	RS400MD-FSB/A-PCIE(1/4)	Jan. 27th	NEC	Work around for CKE# Glitch.	Change R52 Value to 27K.	0.3
34	17	SB400-PCIE/PCI/LPC/RTC(1/4)	Feb. 16th	ATI	To solve SB400-A32 boot fail with PCIE I/P.	Change C263, C264, C265 and C266 from 0.1uf to 0.01uf.	1.0
35	31	ENE-KB910L/TPM	Feb. 23th	Compal	To by pass the ACIN to the EC	Add R71 and change D20 & R386 to @.	0.4
36	17	SB400-PCIE/PCI/LPC/RTC(1/4)	Feb. 23th	Compal	To improve Battery Life when S4/S5 status.	Change power source of U8.pin14 and R149.1 from +3VALW to +3VS	0.4
37	21	Hardware Trap	Feb. 23th	Compal	To improve Battery Life when S4/S5 status.	Change power source of U31F.pin14 and U53.pin5 from +3VALW to +3VS	0.4
38	31	ENE-KB910L/TPM	Feb. 23th	Compal	To improve Battery Life when S4/S5 status.	Change power source of R1053 from +3V_EC to +3VS	0.4
39	32	BIOS/EE-Prom/TP/KB/SW	Feb. 23th	Compal	To improve Battery Life when S4/S5 status.	Change power source of RP6 from +3V_EC to +3VS	0.4
40	9	RS400MD-FSB/A-PCIE(1/4)	Feb. 24th	ATI	To improve LAN performance.	Change LAN port from GPP0 to GPP2	0.4
41	18	SB400-USB/AC97/MISC.(2/4)	Feb. 24th	ATI	To improve LAN performance(For BIOS).	Add pull H & L to U7.A27(GPIO).	0.4
42	21	Hardware Trap	Feb. 25th	ATI	Strap on PCICLK5 has beed redefined	Pop R212 to pull low and unpop R199	0.4
43	18	SB400-USB/AC97/MISC.(2/4)	Feb. 25th	NEC	To improve LAN performance(For BIOS).	Add pull H & L to U7.D23(GPIO).	0.4
44	18	SB400-USB/AC97/MISC.(2/4)	Mar. 8th	NEC	To improve LAN performance(For BIOS-IRT).	Pop R160 & R167, unpop R159 & R168	0.5
45	8	RS400MD-FSB/A-PCIE(1/4)	Mar. 8th	Compal	Solve Fan noise	Deleted C911	0.5
46	21	Hardware Trap	Mar. 8th	ATI	Strap on PCICLK5 has beed redefined	Pop R199 to pull low and unpop R212	0.5
47	12	RS400MD-PWR/GND(4/4)	Mar. 8th	Compal	For voltage stable	Add C172	0.5
48	06	Pentium-M(1/3)	Apr. 7th	Compal	To solve S3 shut-down issue.	Add Diode D40, RB521S-30, to discharge Base voltage when shut-down.	2.0
49	22	IDE/CD_ROM Conn.	Apr. 28th	NEC	To solve ODDLED abnormal light.	Change the R236 power source from +5VODD to +5VS.	2.0
1	18	SB400-USB/AC97/MISC.(2/4)	May. 5th	NEC	To improve LAN performance(For BIOS).	Change pull H R159	0.1
2	17	SB400-PCIE/PCI/LPC/RTC(1/4)	May. 5th	Compal	Change PCI_CLK trace for EMI	Change R141, 142, 143, 1011 size from 0603 to 0402	0.1
3	31	ENE-KB910L/TPM	May. 5th	Compal	Add CLKRUN	Reserve 1K resistance pull down	0.1
4	22	IDE/CD_ROM Conn.	May. 5th	Compal	To solve ODDLED abnormal light.	Change R236 from 100K to 8.2K	0.1
5	6	Pentium-M(1/3)	Jun. 16th	Compal	To solve can't boot after high loading test..	Change R227 power source from VCCP to CPUCORE	0.2
6	18	SB400-USB/AC97/MISC.(2/4)	Jun. 16th	NEC	To meet ATI spec(USB_RCOMP)	Change R169 from 10K to 11.8K	0.2
7	27	R5C842-PCI/CARD BUS/OHCI	Jul. 21th	Compal	RICOH recommend	Change R452 from 0 to 10K	1.0
8	9	RS400MD-FSB/A-PCIE(1/4)	Jul. 21th	ATI	ATI recommend	1.Change R51 from 10K_0402_5% to 10K_0402_1% 2.Change R53 from 100_0402_1% to 82.5_0402_1% 3.Change R54 from 8.2K_0402_1% to 8.25K_0402_1% 5.Change C130,C132,C134,C136,C138,C140,C142,C144,C146,C148,C150,C151,C152,C153,C154,C156,C157,C158,C159 from 0.1U_0402_16V4Z to 1U_0402_6.3V4Z	1.0

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1	42	Optional VGA MVCORE Power	Dec. 07th	Compal	In order to use ATI's new power saving feature of Power Play, the VGA chip core Voltage has to be adjusted down to 1.0V. A new power regulator circuit is added using MAX1714 to have high efficiency at light load to make this feature able to prolong battery life.	Add optional PC174, PC176, PC177, PC178, PC179, PC180, PC181, PC184, PD34, PD35, PL15, PL16, PQ47, PQ48, PQ49, PR209, PR210, PR211, PR212, PR213, PR214, PR215, PR216, PR217, PR218, PR219, PU18. Add PC168 , PC169 to replace PC143 (deleted). Add PJP16, PJP17.	0.2
2	34	PWR DCIN / Precharge	Dec. 07th	Compal	To prevent adaptor plug in or plug out glitches.	Added PC167 (1000P_0402_50V7K).	0.2
3	34	PWR DCIN / Precharge	Dec. 07th	Compal	To adjust adaptor input precharge Voltage and Battery input precharge Voltage thresholds.	Change PR17 to 127K 1%, PR21 to 340K 1%, PC14 to 0.1uF.	0.2
4	36	Charger	Dec. 07th	Compal	Change adaptor isolation MOSFET turn-on turn-off delay time for proper multiple power source hot swap.	Change PQ11 to DTC115EUA. Add PD31, PR214, PC170.	0.2
5	36	Charger	Dec. 07th	Compal	To prevent power on single time short duration LED flashing by introducing delay in V_BIAS.	Add in PR205, PR206, PR207, PC171, PD36, PQ45, PQ44.	0.2
6	37	Battery Select	Dec. 07th	Compal	To provide proper multiple power source hot swap (main and second battery), component values are changed and extra components are added for extra delay to do "Break" before "Make" function.	Added PD33, PD32, PC173, PC172, PQ46, PC208. Change PC44, PC46 to 47pF. Change PR79, PR88 to 100K 5%.	0.2
7	39	+1.2VSP & +1.8VALWP	Dec. 07th	Compal	Correct wrong pin connection.	Change PQ28 pin 4 and pin 1,2,3 connection.	0.2
8	40	0.9VSP/VCCPP	Dec. 07th	Compal	Correct wrong pin connection.	Swap PQ42 pin 1 and pin 3 connection.	0.2
9	41	CPU_CORE	Dec. 07th	Compal	Correct CPU Vcore load line.	Change PR159 and PR153 from 3K to 2K 1%.	0.2
10	34	PWR DCIN / Precharge	Dec. 10th	Compal	Change to horizontal intertition type on-board adaptor connector jack.	Change PJP1 to use "SINGA_2WA-8291T041".	0.2
11	38	3.3V/5V	Dec. 10th	Compal	Change to use lower height Inductor to fit into low height area (5.5A rating is still > 4A requirement).	Change PL8 to use TOKO part: "4.7UH_D104C-919AS-47M_5A_20%".	0.2
12	35, 36, 37	CPU OTP Page, Charger Page, and Battery Select Page.	Dec. 13th	Compal	To save power in S4, change PU3, PU5, and PU7 power to be powered from +5VL (not Vs).	Change PU3, PU5, and PU7 pin 8 to VL net. Add PC210 to VL net close to PU5 pin 8.	0.2
13	42	Optional VGA MVCORE Power	Dec. 13th	Compal	To change Voltage control pin active polarity on ATI Power Play.	Add PR230, PR231, PQ50, PC200, PD40, and PD41. uninstall PD41. Delete PQ49, PR218, PR219.	0.2
14	38	3.3V/5V	Dec. 14th	Compal	Add option ckt to let +3VALW always on when batteries are in bay. Add option ckt to let +5VALW to be independantly controlled by ECON signal.	Add PR232, PR233, PR234. Uninstall PC148, PR105, pr233, and PU16.	0.2
15	34	PWR DCIN / Precharge	Dec. 14th	Compal	Add option ckt to let +3VALW always on when batteries are in bay.	Add PR235. Delete PC8, PR12, PR14, and PQ1.	0.2
16	34	PWR DCIN / Precharge	Dec. 14th	Compal	Change pre-charge time to be shorter by use smaller value.	Change PR9, PR11, PR13 to 1K.	0.2
17	40	0.9VSP/VCCPP	Dec. 14th	Compal	With option ckt to let +3VALW always on when batteries are in bay, old circuit components should be uninstalled.	Uninstall PC152, PR201, PQ43, PQ42, PR199, PC149, PC15, PU17, PC150. Add PJP20. Add PR236, but uninstall it.	0.2
18	39	+1.2VSP & +1.8VALWP	Dec. 22th	Compal	Add delay circuit requested by HW to form SUSP_DLY# signal for 1.2V and 1.0/1.2V regulators enable control.	Add PR220, PR222, PC185, PQ50.	0.2
19	36	Charger	Dec. 22th	Compal	Add control signal to prevent Voltage droop when adaptor is inserted. Change resistor value to slow down in-rush current.	Add PD43. Change PR43=33K 5%, and unpopulate PR34.	0.3
20	34	PWR DCIN / Precharge	Dec. 22th	Compal	Add control signal to prevent Voltage droop problem when adaptor is inserted.	Added PR249=4.7k. Changed PC13=1000pF, PC167 = 0.1uF.	0.3

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21	34	PWR DCIN / Precharge	Dec. 30th	Compal	To provide full protection in wrong adaptor over-voltage or Battery charger over-voltage conditions, A switch is inserted into Pre-charge path to stop pre-charge during over-voltage.	Deleted PR10 , and added in PR241, PR242, PR247, PQ57, PQ58, and PQ61.	0.3
22	36	Charger	Dec. 30th	Compal	To provide better protection for wrong adaptor over-voltage, a threshold protection circuit is added on ACOFF# control signal and PQ5 control signal.	Added PQ59, PQ60, PR244, PR245, and PR246. Changed PR36, and PR38. Changed PU5A pin8 to "VIN" net.	0.3
23	35	CPU OTP	Dec. 30th	Compal	To improve shutdown mode quiescent current, change CPU OVP circuit resistors to have higher value.	Changed PH1 to 100K (TH11-4H104FT), PR30, OR28, PR29, PR31, PR25, and PR26 value to larger values to reduce shutdown mode current. Changed PQ4 to RHU002N06 and PC18 to 1000pF.	0.3
24	39	+1.2VSP & +1.8VALWP	Dec. 30th	Compal	To correct the polarity of control signal for 1.0V/1.2V regulator for VGA.	Deleted PR221, PQ51. Changed "SUSP_DLY" connection to PQ50 pin1.	0.3
25	36	Charger	Jan. 04th	Compal	To save more power in S3, S4, S5 modes and increase switching speed during power source hot swapping.	Depopulated PR34, PR59, and PR61. Changed PR43, PR70, and PR71 to 2.2K.	0.3
26	41	CPU_CORE	Jan. 13th	Compal	Changed back CPU load line resistor value.	Change PR159 and PR153 from 2K to 3K 1%.	0.3
27	40	0.9VSP/VCCPP	Jan. 14th	Compal	De-populate paralleled polymer capacitor on 1.05V rail (H/W has one already).	De-populate PC101.	0.3
28	42	Optional VGA MVCORE Power	Jan. 20th	Compal	North Bridge Chip Core Voltage on the lower band change to higher band.	Changed PR217 to 44.2K 1%.	0.3
29	34	PWR DCIN / Precharge	Jan. 20th	Compal	To save S4 mode current, Change PUL pin8 power to VL.	Changed PR22=330K 1%, PR21=169K 1%, PR17=287K 1%, PR16=820K 1%, PR15 to 47K 5%. PUL pin6 to pin2. PUL pin8 to VL, Deleted PR24, and PC14.	0.3
30	39	+1.2VSP & +1.8VALWP	Jan. 24th	Compal	Add remote sense resistors.	Added PR250, PR251.	0.3
31	42	Optional VGA MVCORE Power	Jan. 24th	Compal	Add remote sense resistors.	Added PR252, PR253.	0.3
32	41	CPU_CORE	Jan. 24th	Compal	To prevent in-phase operation due to un-predicted noise problems.	Added/reserved PC211, PC212, but not install them.	0.3
33	38	3.3V/5V	Jan. 24th	Compal	To reduce temperature rise on NB skin.	Changed PL5, PL6 to use TOKO inductors.	0.3
34	34 38 39 41 36	PWR DCIN / Precharge 3.3V/5V +1.2VSP & +1.8VALWP CPU_CORE Charger	Jan. 24th	NEC	Add fuse at input trace for each DC/DC circuit and charger output trace.	Changed PF1 to 12A and add PF2 for charger output trace, PF3 for 3V/5V, PF4 for 1.2VSP/1.8VALWP/1.2VMVCOREP, PF5forCPU_CORE.	0.3
35	36	Charger	Jan. 28th	NEC	Add fuse at battery input trace.	Del PF2 and add PF6 and PF7 at PBJ1 pin 1 and PBJ2 pin 1.	0.3
36	39 42	+1.2VSP & +1.8VALWP Optional VGA MVCORE Power	Jan. 28th	Compal	System hang up at running 3DMark, change +1.2VSP and +1.2VMVCOREP to remote sense.	De-populate PR251 and in series with PR250 to +1.2VS . De-populate PR252 and in series with PR253 to +1.2VMVCORE .	0.3
37	34	PWR DCIN / Precharge	Fab. 24th	Compal	To reduce power consumption at S4 mode.	Reserve PR256 to as a volatagr divider with PR4.	0.4
38	38	3.3V/5V	Fab. 24th	Compal	To change +3VALWP and +5VALWP sequence, let +3VALWP turns on after +5VALWP.	Add PR255 and PC213 to delay the turn on sequence of +3VALWP.	0.4

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
39	34	PWR DCIN / Precharge	Mar. 8th	Compal	To change RTC battery charger current to meet RTC battery spec.	Change PR19 and PR20 to 560 Ohm.	0.4
40	34	PWR DCIN / Precharge	Mar. 8th	Compal	To change 1.2VMVCORE nomial voltage level and add output capacitor to meet spec.	Populate PC169 with 4.7U and change PR217 to 49.9K Ohm.	0.4
	42	Optional VGA MVCORE Power					
41	35	PWR CPU OTP	Mar. 8th	Compal	To change OTP triggle point at 86 degree C for thermal team request.	Change PR28 to 200K Ohm.	0.4
42	36	PWR-CHARGER	Mar. 8th	Compal	To faster the CP protection.	Change PC26 to 1500PF.	0.4
43	38	PWR-+1.2VSP & +1.8VALWP	Mar. 8th	Compal	To decrease +1.2VSP OCP point.	Change PR124 to 61.9K Ohm and PR125 to 39.2K Ohm.	0.4
44	42	Optional VGA MVCORE Power	Mar. 8th	Compal	To increase +1.2VMVCORE OCP point.	Change PR126 to 150K Ohm.	0.4
45	42	Optional VGA MVCORE Power	Mar. 11th	Compal	To increase +1.2VMVCORE 1.2V and 1.0V switch design margine.	Change PD40 to RB751V and PR231 to 100K Ohm.	0.4
46	38	3.3V/5V	Mar. 16th	Compal	To change +3VALWP and +5VALWP sequence, let +3VALWP turns on after +5VALWP.	Change PR255 to 15K Ohm and PC213 to 0.1u F.	0.5
47	34	PWR DCIN / Precharge	Mar. 29th	Compal	To solve can't power on when remove the AC outlet without battery	Change PR16 to 1M Ohm , PR21 to 162K Ohm ,PR22 to 287K Ohm , PC13 to 0.1UF , PC12 to 100PF and PD21 to SKUL30-02AT.	0.5
	38	3.3V/5V					
48	37	Battery Select	Mar. 29th	Compal	To solve can't power on when discharge battery to shut down mode	Change PR81 to 499K Ohm , PR90 to 499K Ohm and PQ22 to RHU002N06.	0.5
49	37	Battery Select	Mar. 29th	Compal	To solve can't charge when discharge battery to shut down mode	Change PR80 to 27K Ohm and PR89 to 27K Ohm.	0.5
50	41	CPU_CORE	Apr. 28th	Compal	To reserve VR_ON control signal for +VCCPP and change CPU_CORE enable signal pull down resistor to capacitor.	Add PR257 and change PR155 to PC214	2.0
	40	0.9VSP/VCCPP					
51	38	3.3V/5V	May. 10th	Compal	To solve no Power issue on Lavie and VersaPro MP status.	Change PC68 and PC72 to 150U 6.3V 18mOhm UD type and change Q24 to SI481-DY-T1-E3	2.0

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