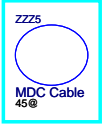


02/24 Change LA-4821P from mount to DA2@



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KFT00 Schematics Document

Intel Penryn Processor with SiSM672FX + DDRII + SiS968 + SiS307ELV

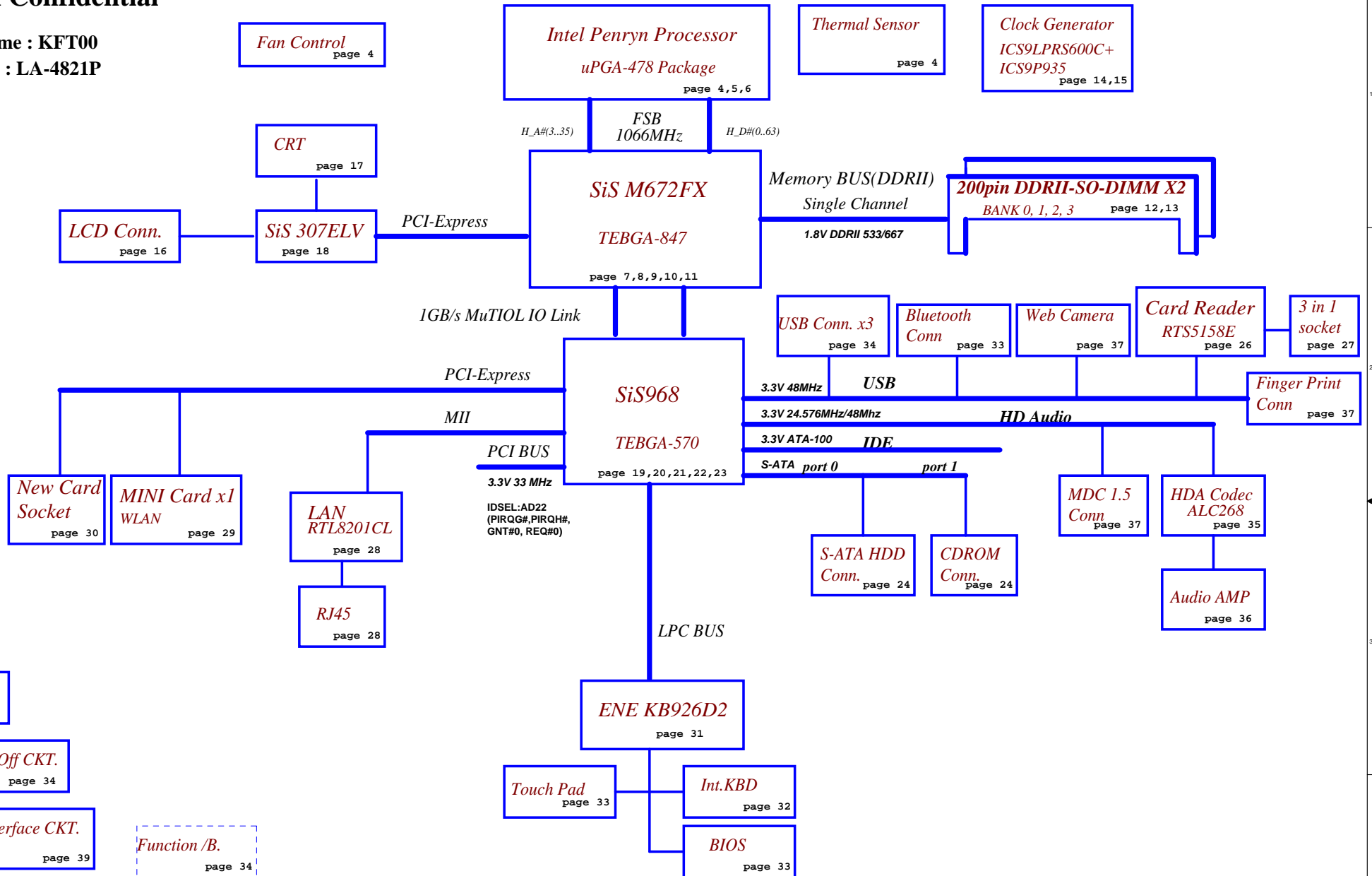
2009-03-10

REV:1.0

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<small> Size: E Document Number: KFT00-M/B LA-4821P Schematic Date: Tuesday, March 10, 2009 Sheet: 1 of 2 </small>				<small> Rev: 1.0 Scale: 1:1 </small>	

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Model Name : KFT00
File Name : LA-4821P



RTC CKT.
page 20

Power On/Off CKT.
page 34

DC/DC Interface CKT.
page 39

Power Circuit DC/DC
page 40, 41, 43, 44, 45, 46

CHARGER
page 42

Function /B.
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS (Actual +0.9V)	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.2VS	1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PROJECT ID Table

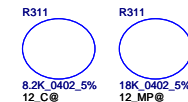
	PROJECT_ID1 GPIO5	PROJECT_ID0 GPIO0
KFT00	0	0
KSW01	1	0
KSW91	1	1

SKU ID Table

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Ra~ R312

Rb~ R311



Board ID	Rb	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	Rb BOM Structure
0	0	0 V	0 V	0 V	12_A@
1	8.2K +/- 5%	0.217 V	0.250 V	0.288 V	12_C@
2	18K +/- 5%	0.439 V	0.503 V	0.575 V	12_MP@

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
Smart Battery	0001 011X b		
EEPROM(24C16/02)	1010 000X b		

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b

EC SM Bus2 address

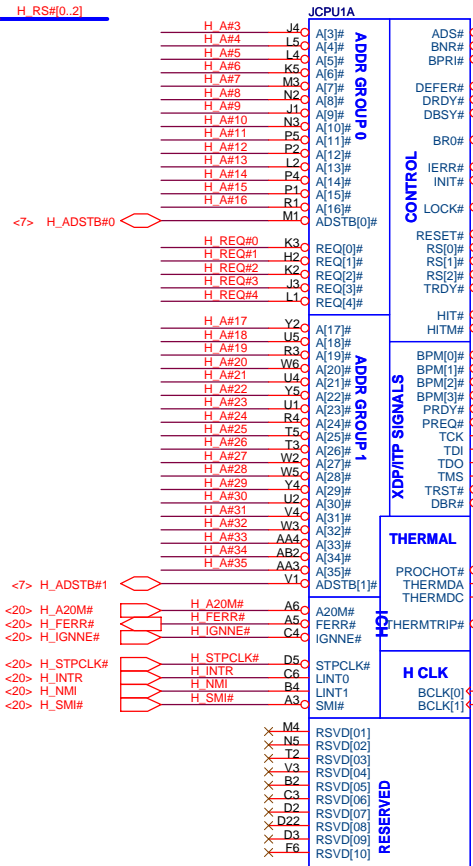
Device	Address
ADI ADM1032	1001 100X b
SMC EMC1402-1	

M672 SM Bus address

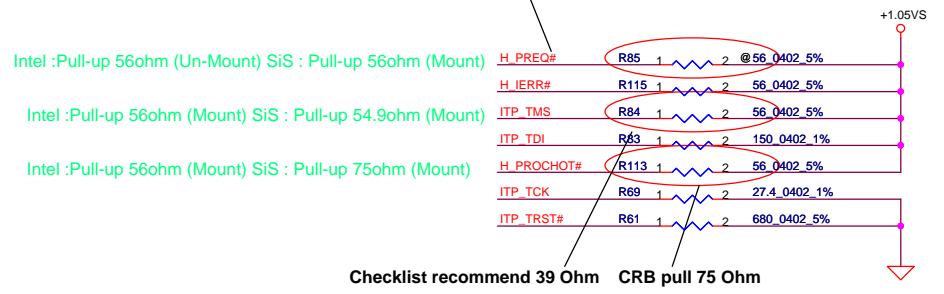
Device	Address
Clock Generator	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 001Xb

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Document Number: KFT00-MWB LA-4821P Schematic Date: Tuesday, March 10, 2009 Sheet: 3 of 4				

- <7> H_A# [3..35] H_A# [3..35]
- <7> H_REQ# [0..4] H_REQ# [0..4]
- <7> H_RS# [0..2] H_RS# [0..2]

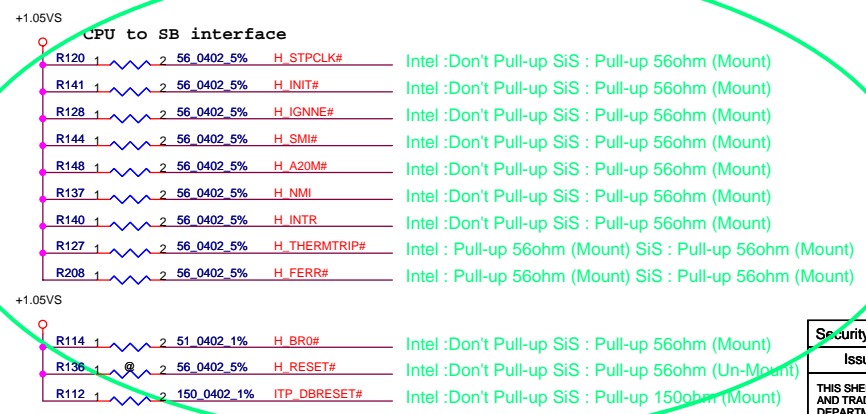
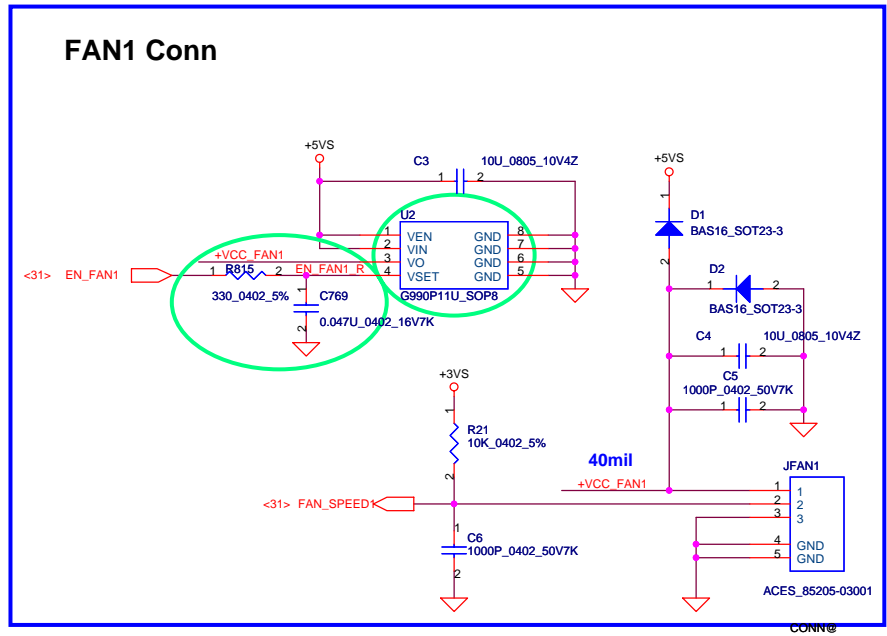
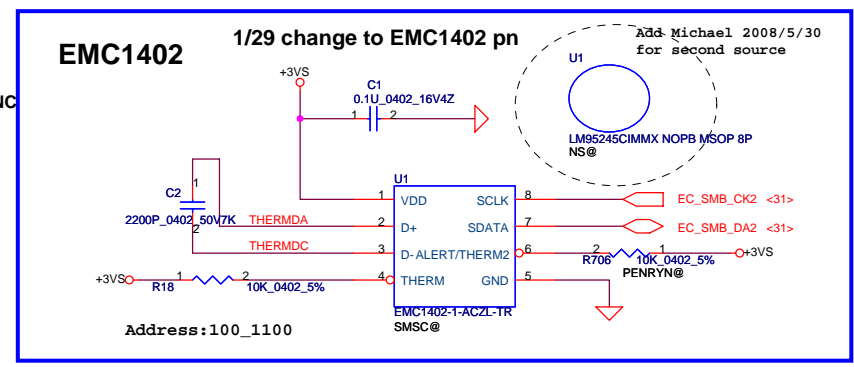


Trace length must short Place close to CPU within 500mil

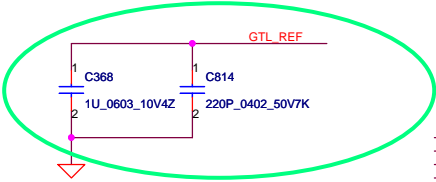


Connect SB SYS_RESET# or just left NC

H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil

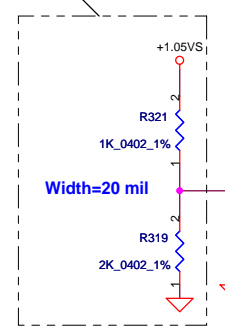


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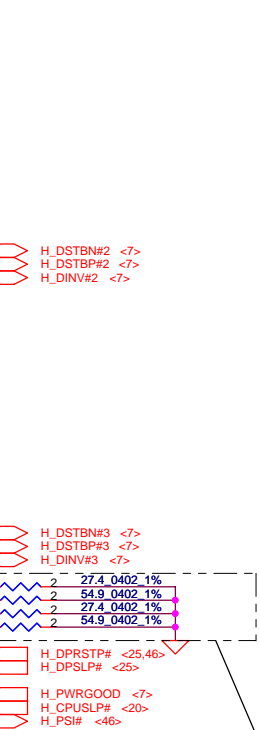
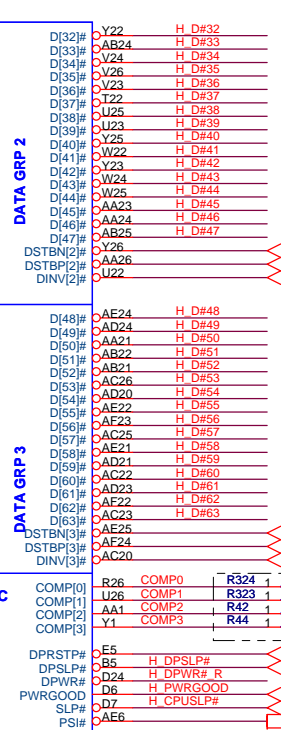
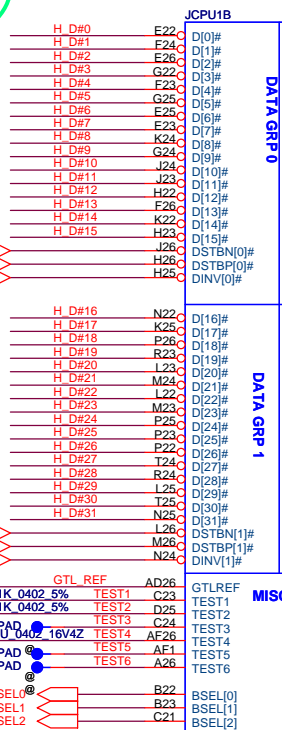
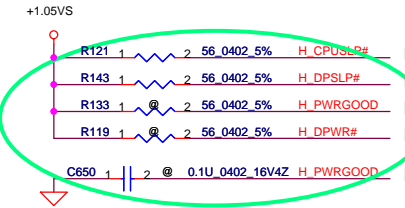
SiS Recommend

Close to CPU pin AD26 within 500mils.

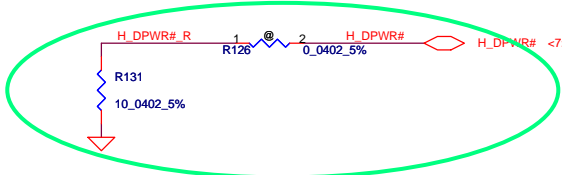


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1
200	0	1	0

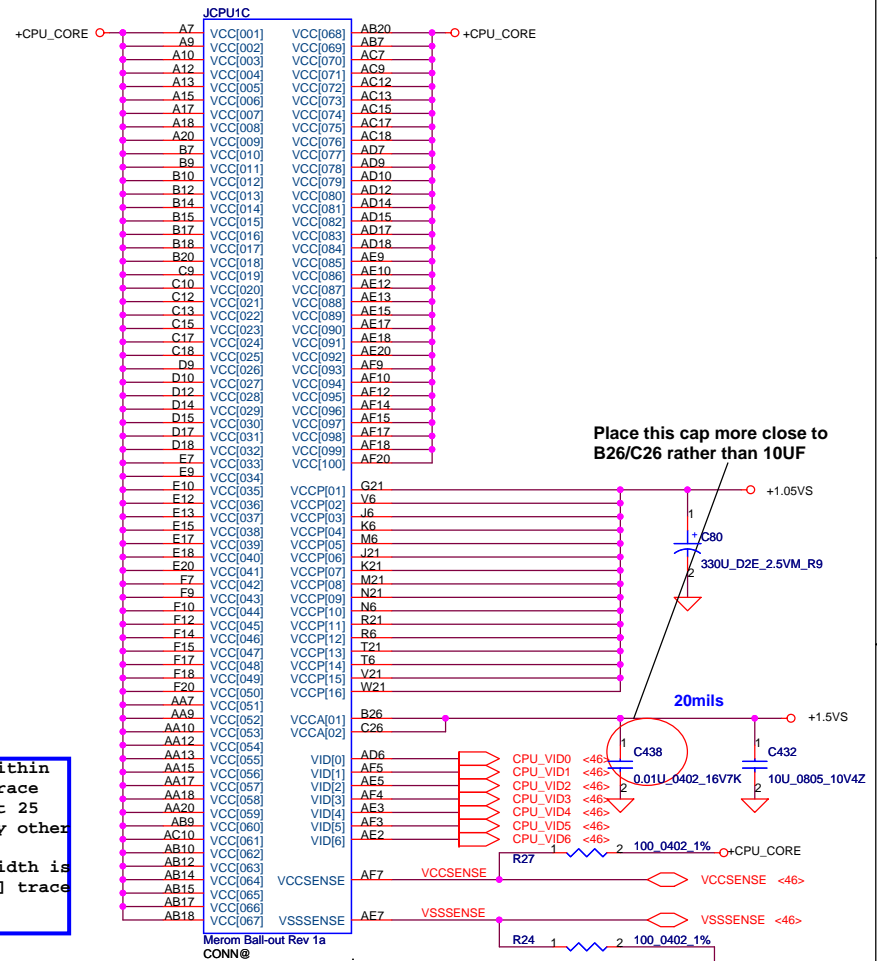


Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



Length match within 25 mils. The trace width/space/other is 20/7/25.

Close to CPU pin within 500mils.



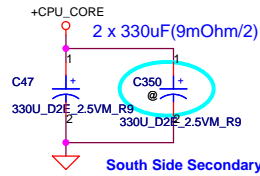
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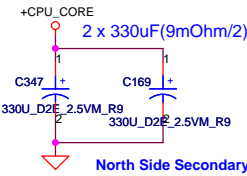
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Title		
Merom (2/3)		
Size	Document Number	Rev
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JCPU1D			
A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P24
A11	VSS[003]	VSS[084]	R2
A14	VSS[004]	VSS[085]	R5
A16	VSS[005]	VSS[086]	R22
A19	VSS[006]	VSS[087]	R25
A23	VSS[007]	VSS[088]	T1
AF2	VSS[008]	VSS[089]	T4
B6	VSS[009]	VSS[090]	T23
B8	VSS[010]	VSS[091]	T26
B11	VSS[011]	VSS[092]	U3
B13	VSS[012]	VSS[093]	U6
B16	VSS[013]	VSS[094]	U21
B19	VSS[014]	VSS[095]	U24
B21	VSS[015]	VSS[096]	V2
B24	VSS[016]	VSS[097]	V5
C5	VSS[017]	VSS[098]	V22
C8	VSS[018]	VSS[099]	V25
C11	VSS[019]	VSS[100]	W1
C14	VSS[020]	VSS[101]	W4
C16	VSS[021]	VSS[102]	W23
C19	VSS[022]	VSS[103]	W26
C22	VSS[023]	VSS[104]	Y3
C25	VSS[024]	VSS[105]	Y6
D1	VSS[025]	VSS[106]	Y21
D4	VSS[026]	VSS[107]	Y24
D8	VSS[027]	VSS[108]	AA2
D11	VSS[028]	VSS[109]	AA5
D13	VSS[029]	VSS[110]	AA8
D16	VSS[030]	VSS[111]	AA11
D19	VSS[031]	VSS[112]	AA14
D23	VSS[032]	VSS[113]	AA16
D26	VSS[033]	VSS[114]	AA19
E3	VSS[034]	VSS[115]	AA22
E6	VSS[035]	VSS[116]	AA25
E8	VSS[036]	VSS[117]	AB1
E11	VSS[037]	VSS[118]	AB4
E14	VSS[038]	VSS[119]	AB8
E16	VSS[040]	VSS[121]	AB11
E19	VSS[041]	VSS[122]	AB13
E21	VSS[042]	VSS[123]	AB16
F24	VSS[043]	VSS[124]	AB19
F5	VSS[044]	VSS[125]	AB23
F8	VSS[045]	VSS[126]	AB26
F11	VSS[046]	VSS[127]	AC3
F13	VSS[047]	VSS[128]	AC6
F16	VSS[048]	VSS[129]	AC8
F19	VSS[049]	VSS[130]	AC11
F2	VSS[050]	VSS[131]	AC14
F22	VSS[051]	VSS[132]	AC16
F25	VSS[052]	VSS[133]	AC19
G4	VSS[053]	VSS[134]	AC21
G1	VSS[054]	VSS[135]	AC24
G23	VSS[055]	VSS[136]	AD2
G26	VSS[056]	VSS[137]	AD5
H3	VSS[057]	VSS[138]	AD8
H6	VSS[058]	VSS[139]	AD11
H21	VSS[059]	VSS[140]	AD13
H24	VSS[060]	VSS[141]	AD16
J2	VSS[061]	VSS[142]	AD19
J5	VSS[062]	VSS[143]	AD22
J22	VSS[063]	VSS[144]	AD25
J25	VSS[064]	VSS[145]	AE1
K1	VSS[065]	VSS[146]	AE4
K4	VSS[066]	VSS[147]	AE8
K23	VSS[067]	VSS[148]	AE11
K26	VSS[068]	VSS[149]	AE14
L3	VSS[069]	VSS[150]	AE16
L6	VSS[070]	VSS[151]	AE19
L21	VSS[071]	VSS[152]	AE23
L24	VSS[072]	VSS[153]	AE26
M2	VSS[073]	VSS[154]	A2
M5	VSS[074]	VSS[155]	A5
M22	VSS[075]	VSS[156]	A8
M25	VSS[076]	VSS[157]	A11
N1	VSS[077]	VSS[158]	A13
N4	VSS[078]	VSS[159]	A16
N23	VSS[079]	VSS[160]	A19
N26	VSS[080]	VSS[161]	A21
P3	VSS[081]	VSS[162]	A25
		VSS[163]	AE25

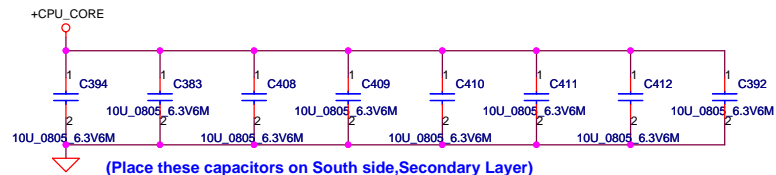
Merom Ball-out Rev 1a



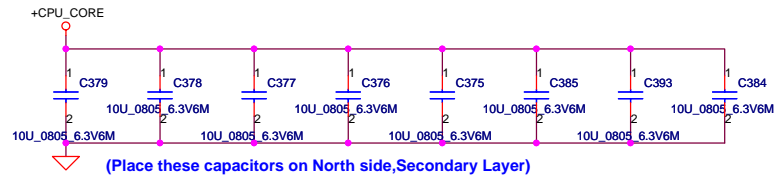
South Side Secondary



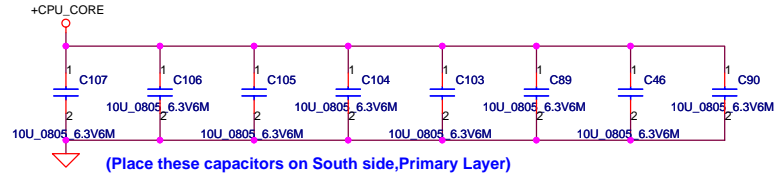
North Side Secondary



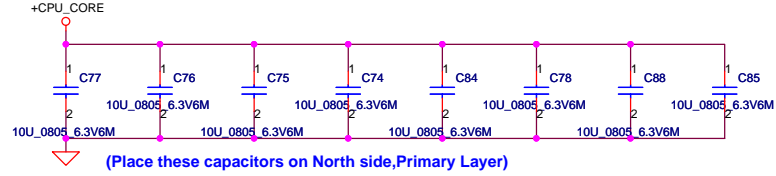
(Place these capacitors on South side, Secondary Layer)



(Place these capacitors on North side, Secondary Layer)

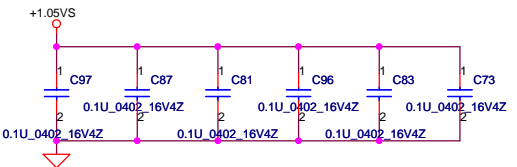


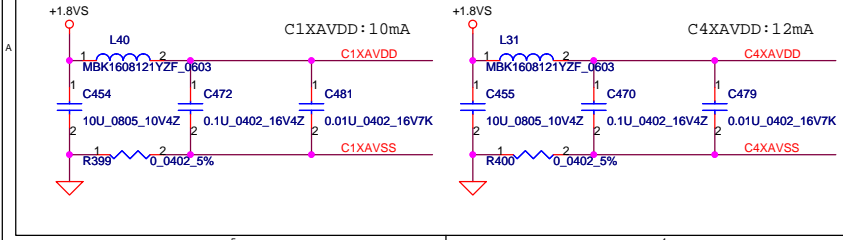
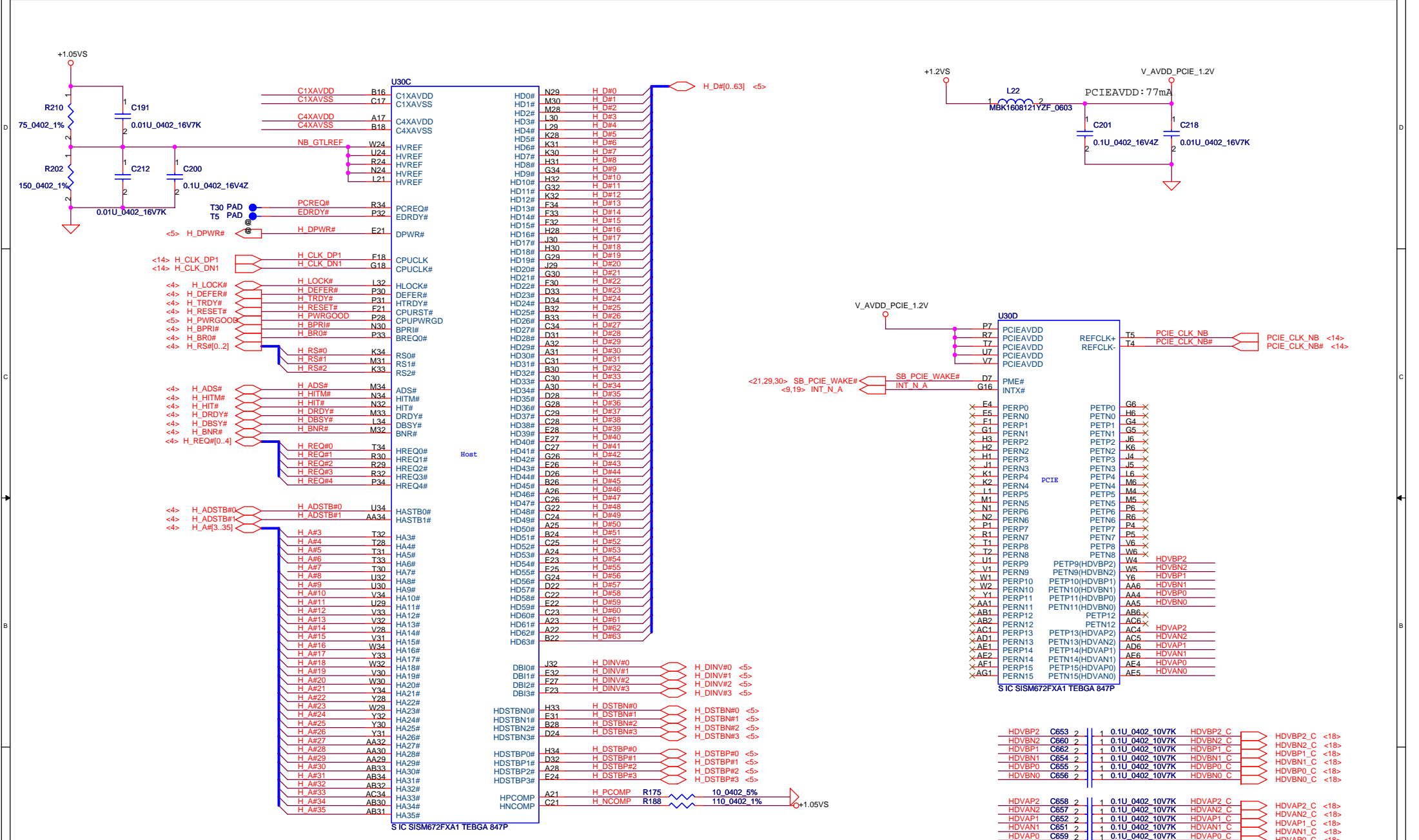
(Place these capacitors on South side, Primary Layer)



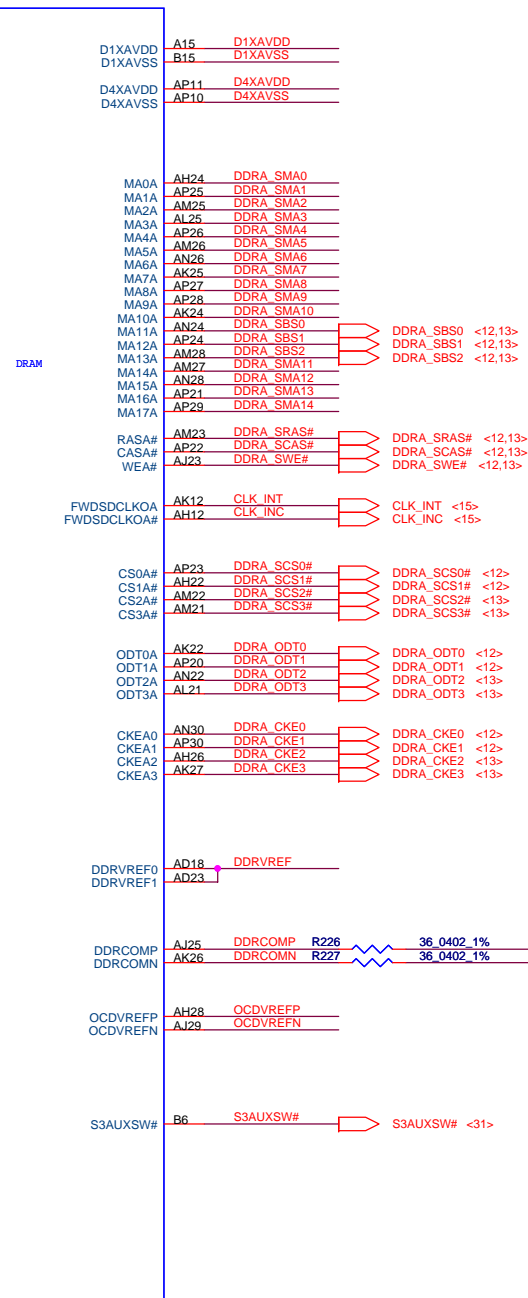
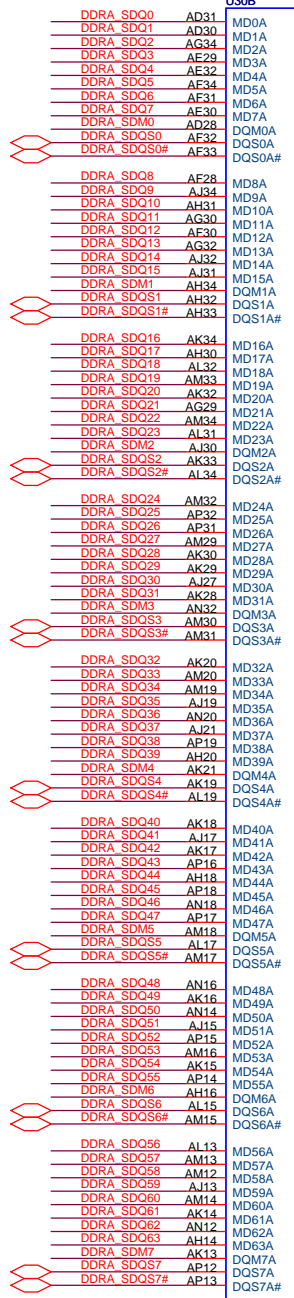
(Place these capacitors on North side, Primary Layer)

+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32

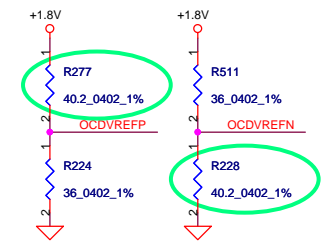
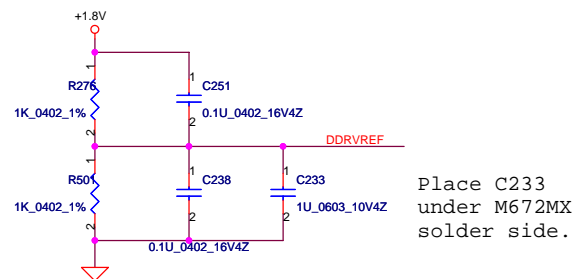
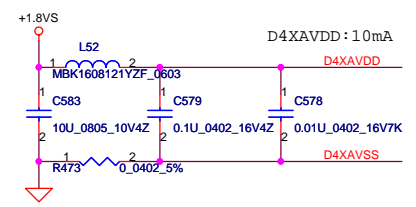
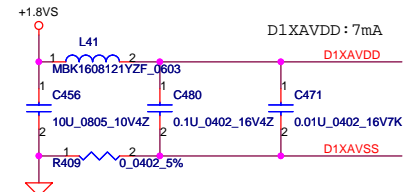




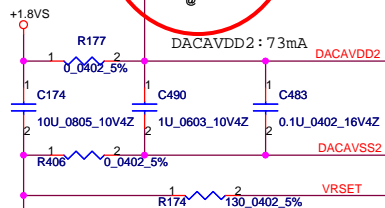
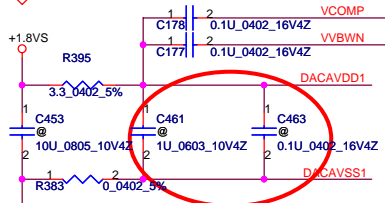
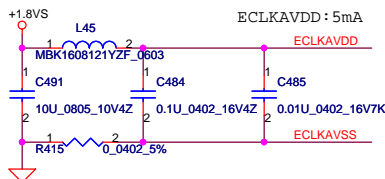
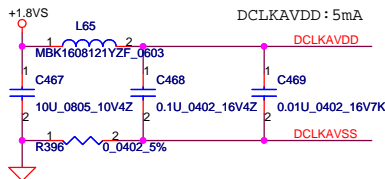
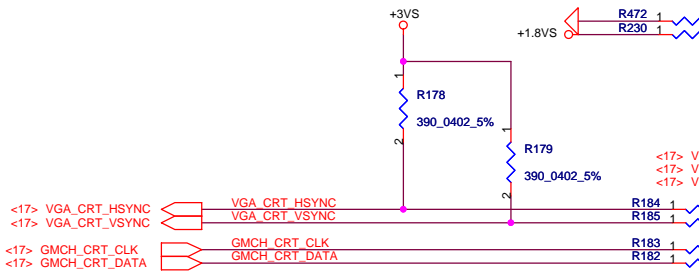
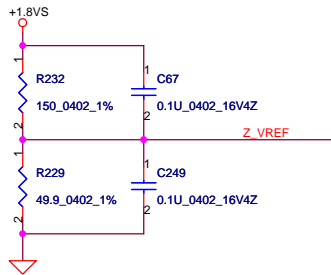
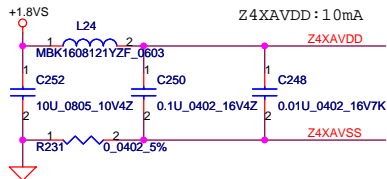
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Date: 11/20/09 5P:47					



S IC SISM672FXA1 TEBGA 847P

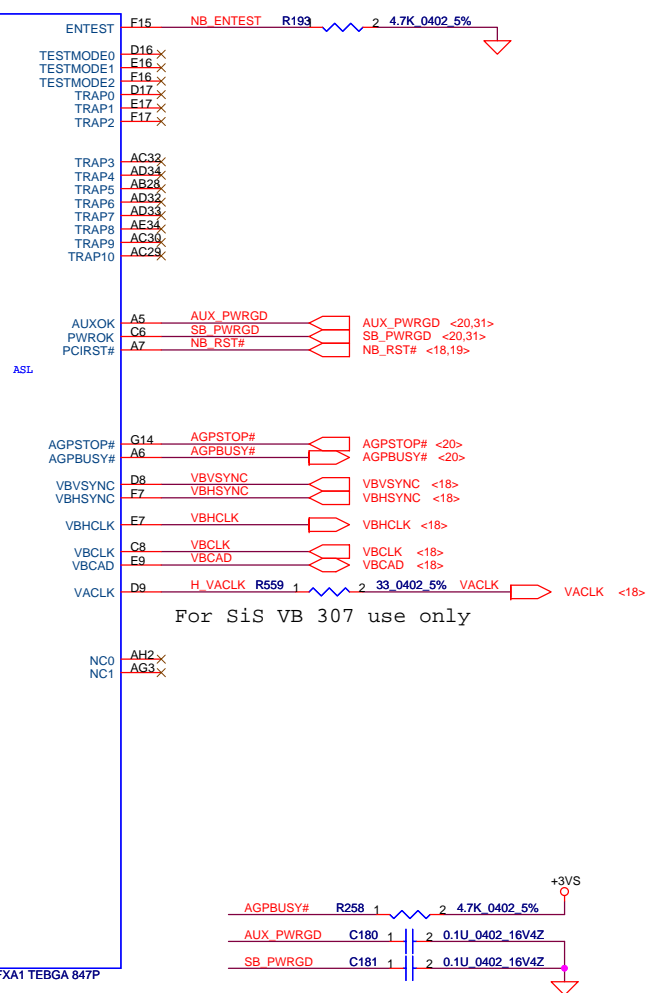
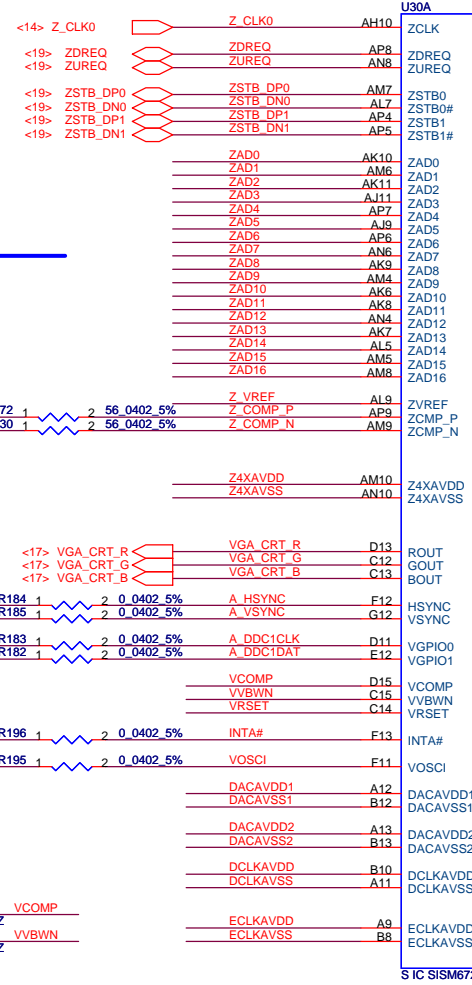


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Size	Document Number	Date		Rev	1.0
Custom	KFT00 M/B LA-4821P Schematic	Tuesday, March 10, 2009		Sheet	8 of 47



DACAVDD1 Spec.
Voltage : 1.5V +/- 5%
Current : 100mA

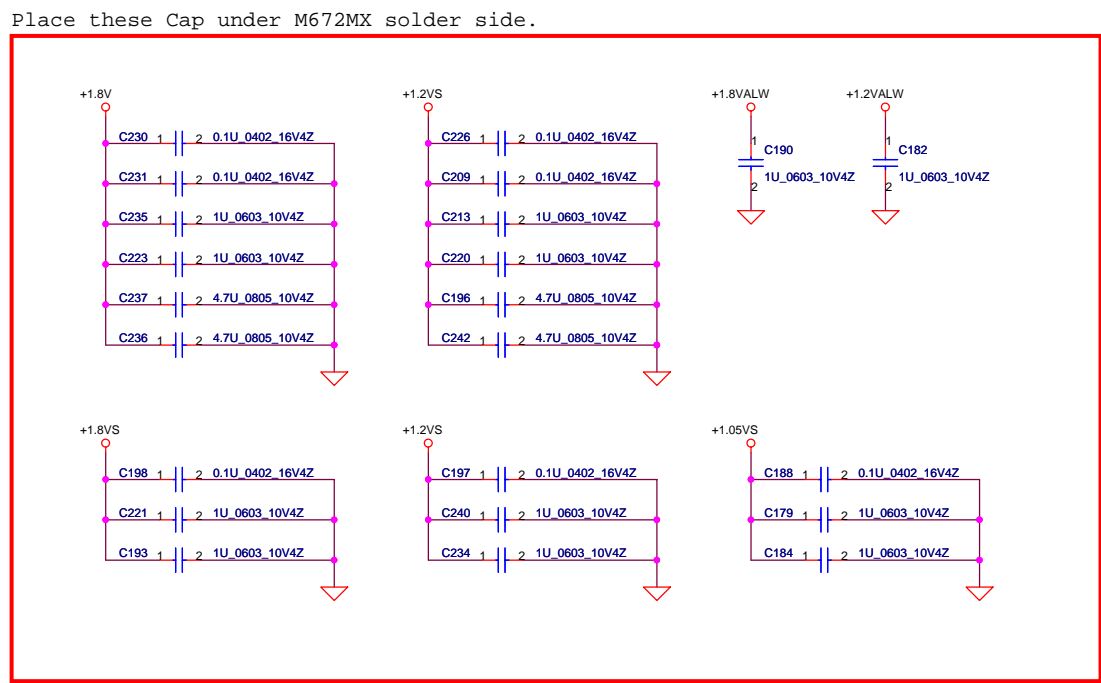
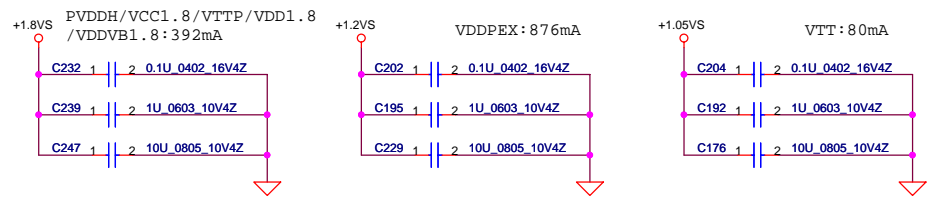
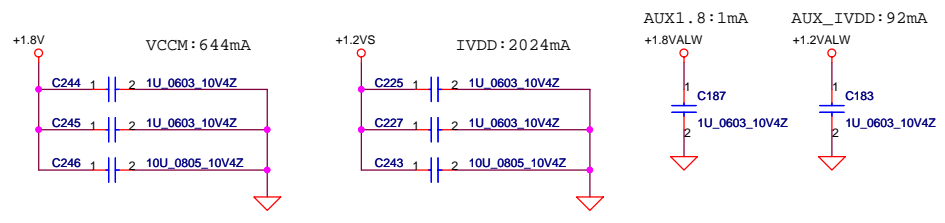
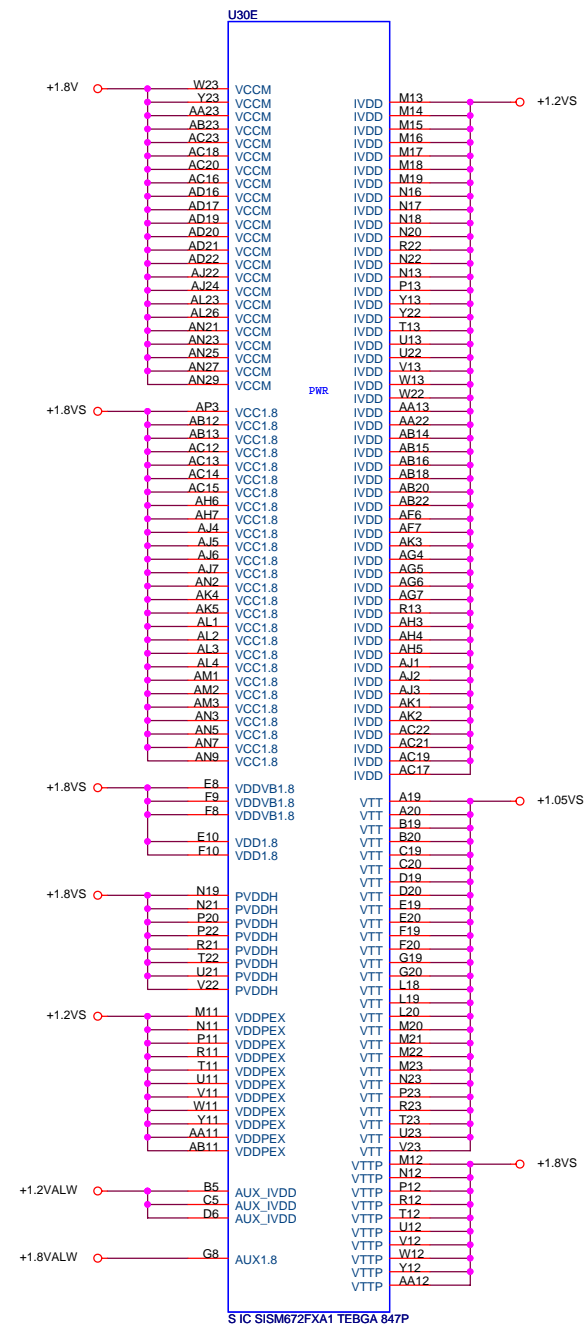
7/30 modified to @



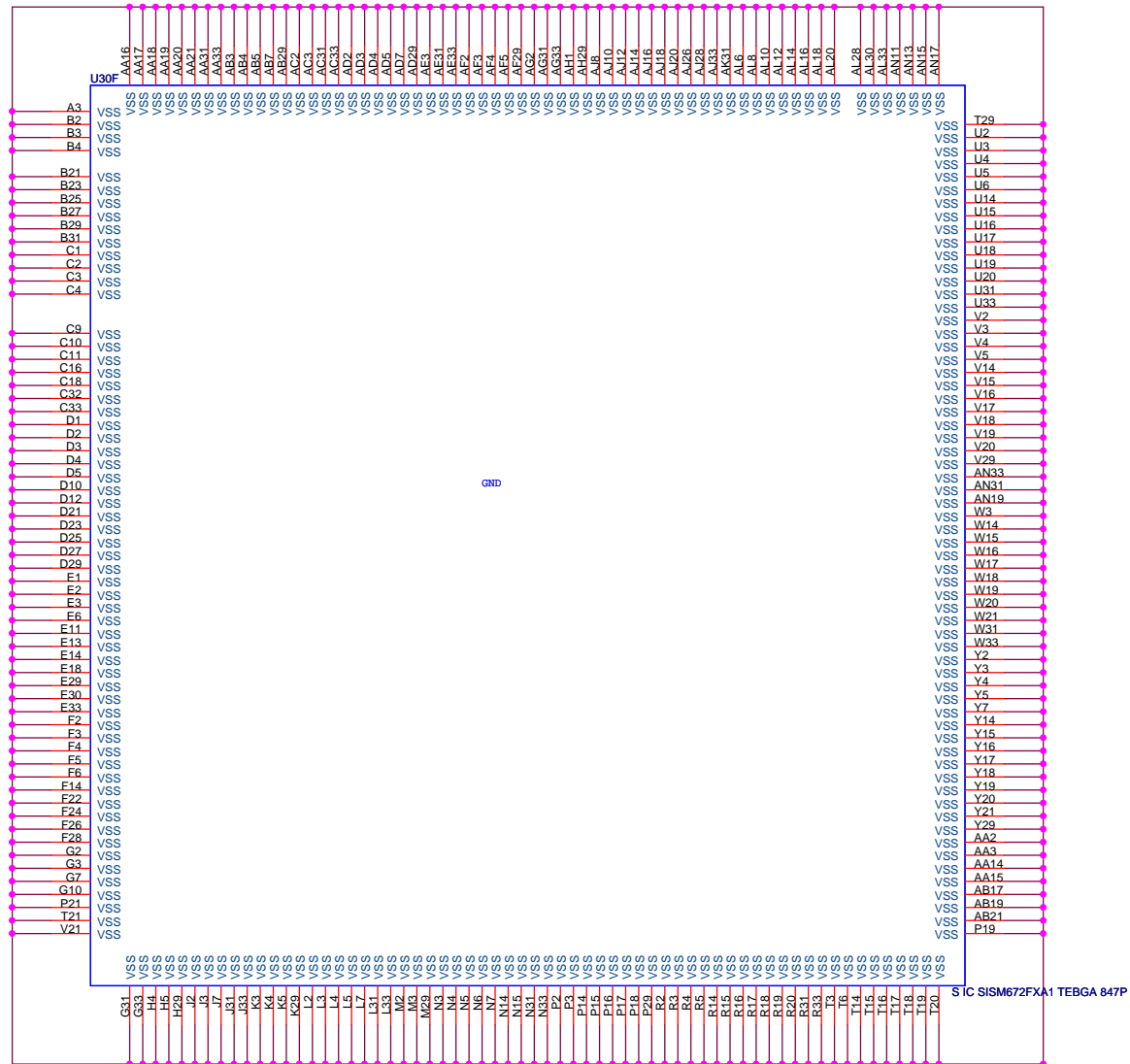
For SiS VB 307 use only

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Size	Custom	Document Number	M672MX (3/5)-ASL Schematic	Rev 1.0
Date:	Monday, March 10, 2008	Sheet	3	4

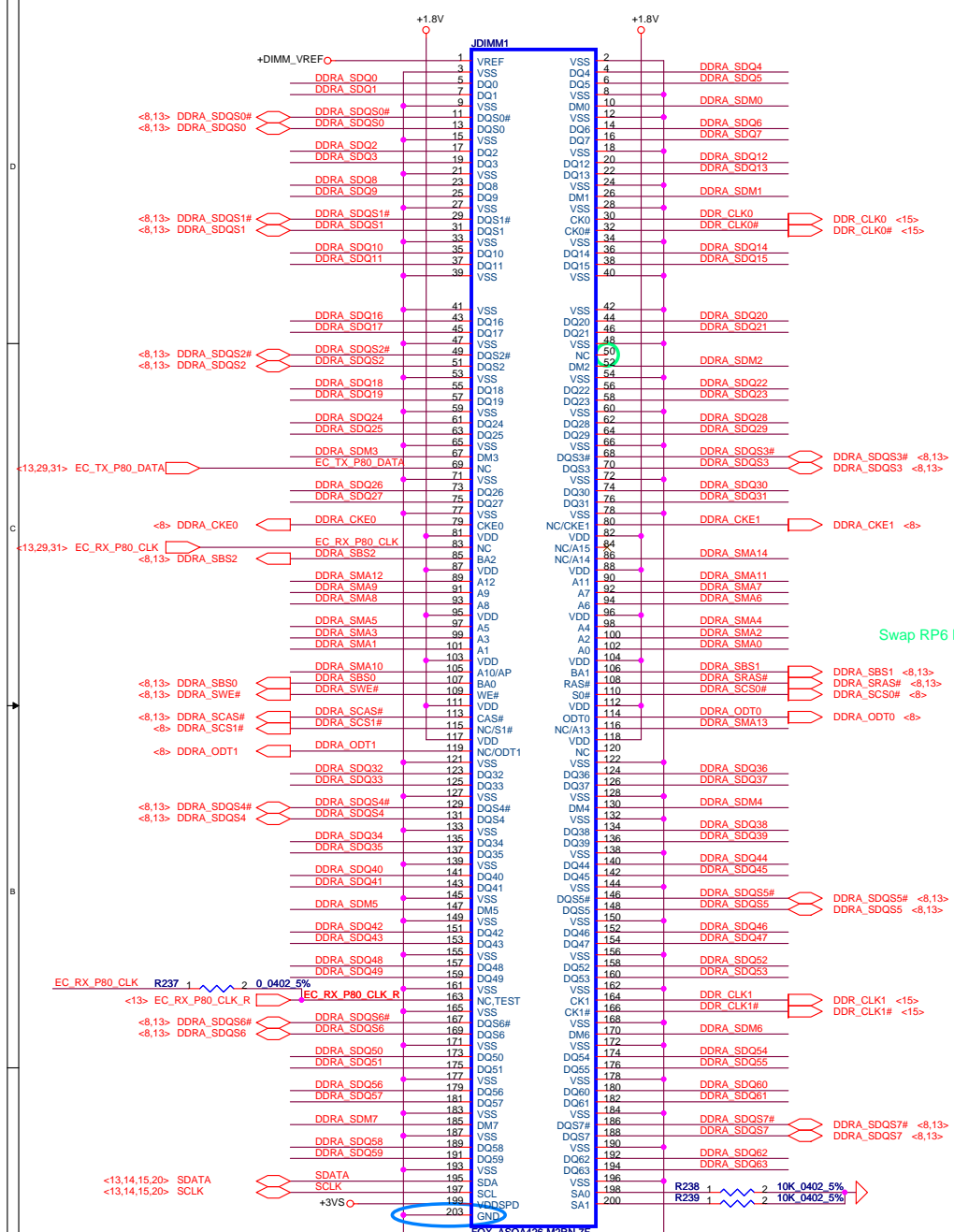


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				Custom	1.0
				Date:	Tuesday, February 10, 2009
				Sheet	10 of 47

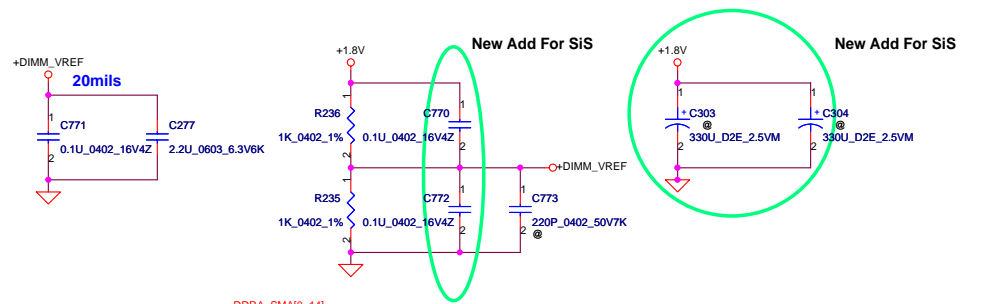


STC SISM672FXA1 TEBGA 847P

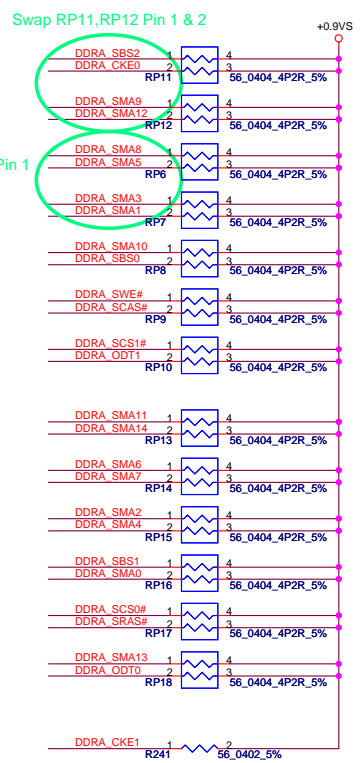
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Issued Date	2008/10/18	Deciphered Date	2009/10/18	M672MX (5/5)-GND	
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				Cus	m-KFT00 M/B LA-4821P Schematic
				Date:	February 10, 2009
				Sheet	11 of 47
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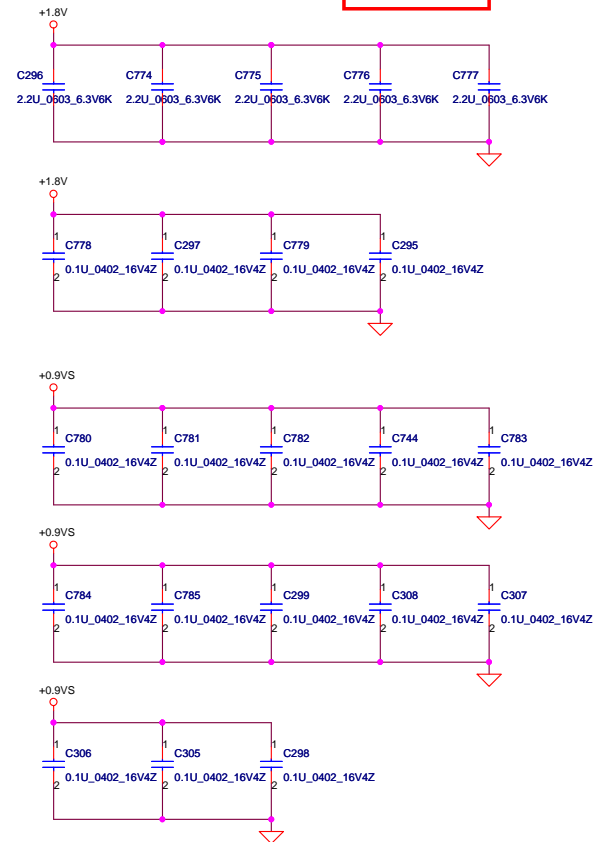
DDIMM0 STD H:5.2mm (BOT)



Layout Note:
Place near JP35

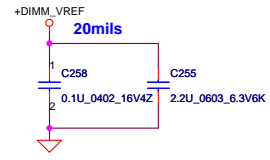
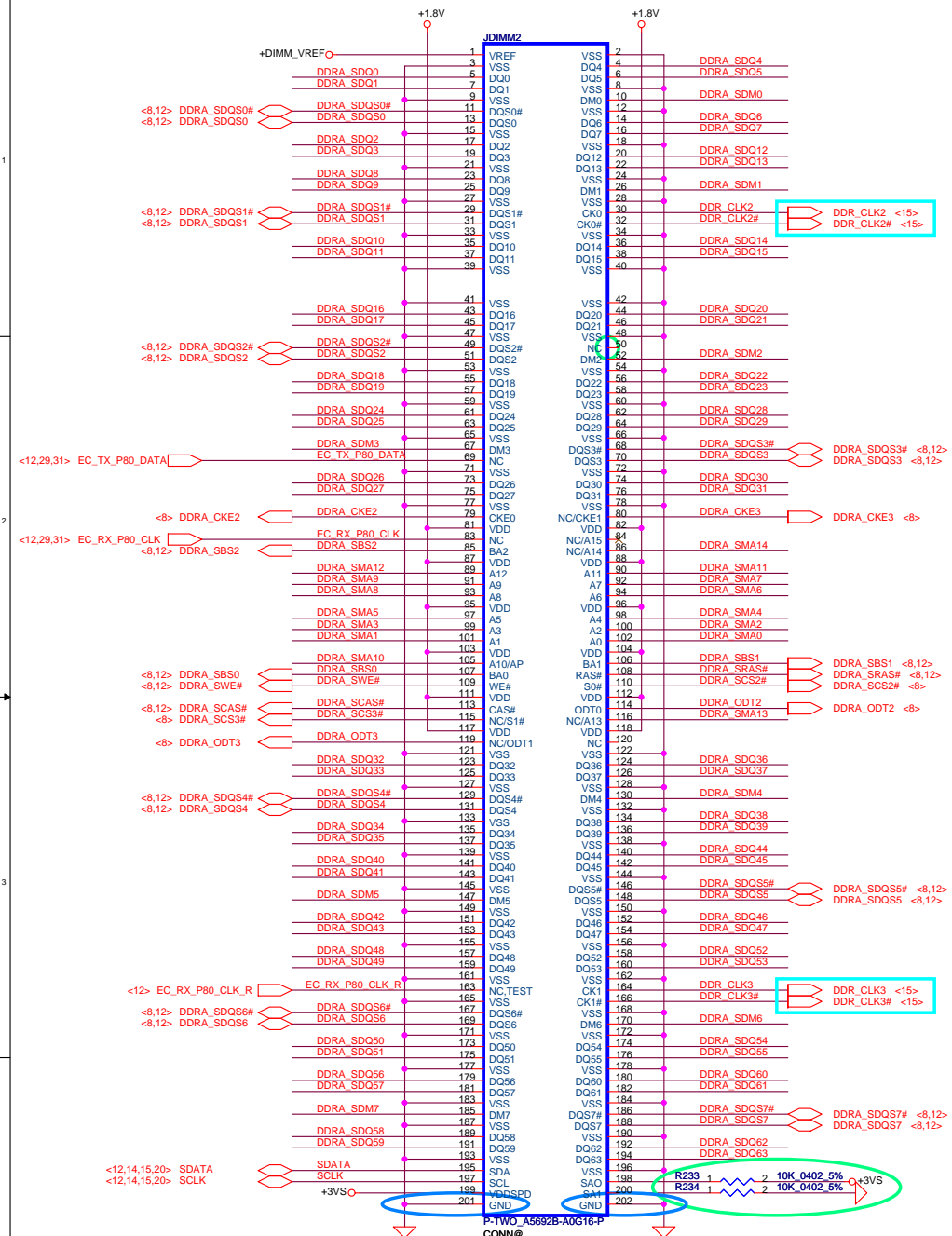


Layout Note:
Place these resistor closely JP35, all trace length Max=1.5"

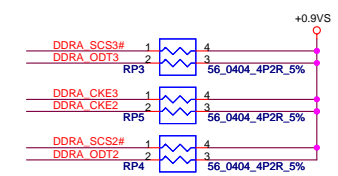
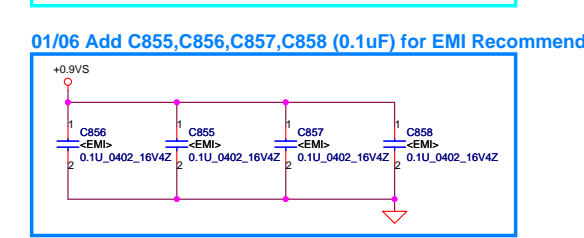
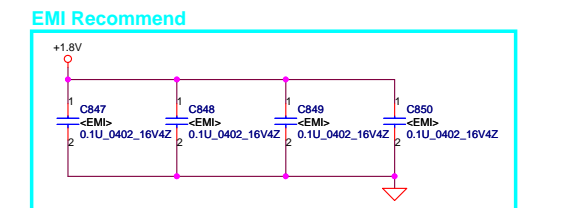
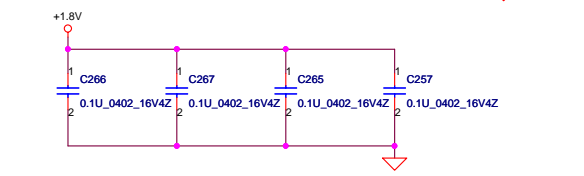
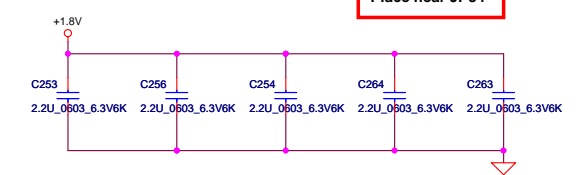


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

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Size	Document Number	Date:	Tuesday, March 10, 2009	Sheet	12 of 47
B	KFT00 M/B LA-4821P Schematic				
					Rev 1.0



Layout Note:
Place near JP34

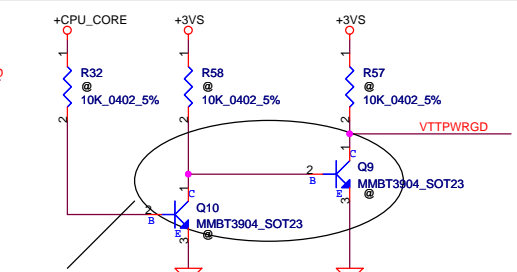
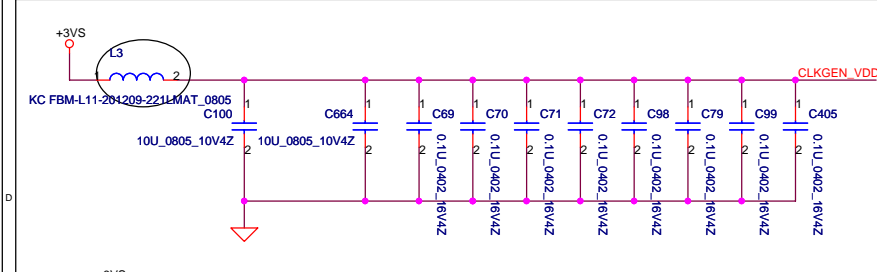


Layout Note:
Place these resistor closely JP34, all trace length Max=1.5"

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

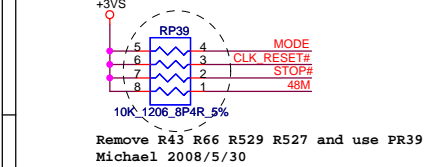
DIMM1 STD H:9.2mm (BOT)

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Sheet No.	1	Document Number	KFT00-M/B LA-4821-P Schematic	
Date	Monday, March 10, 2008	Sheet	13	of 27

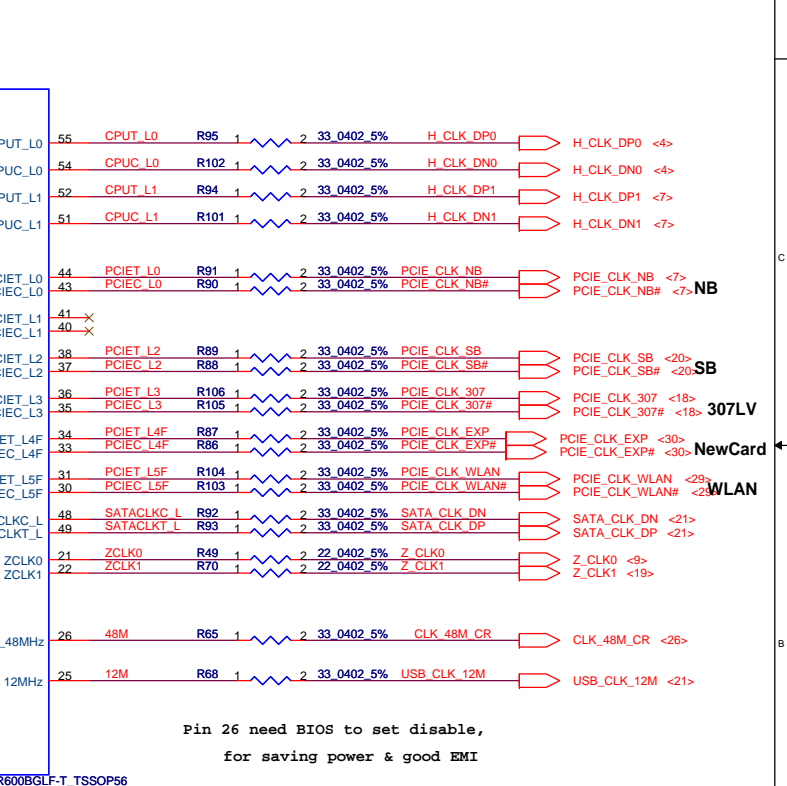
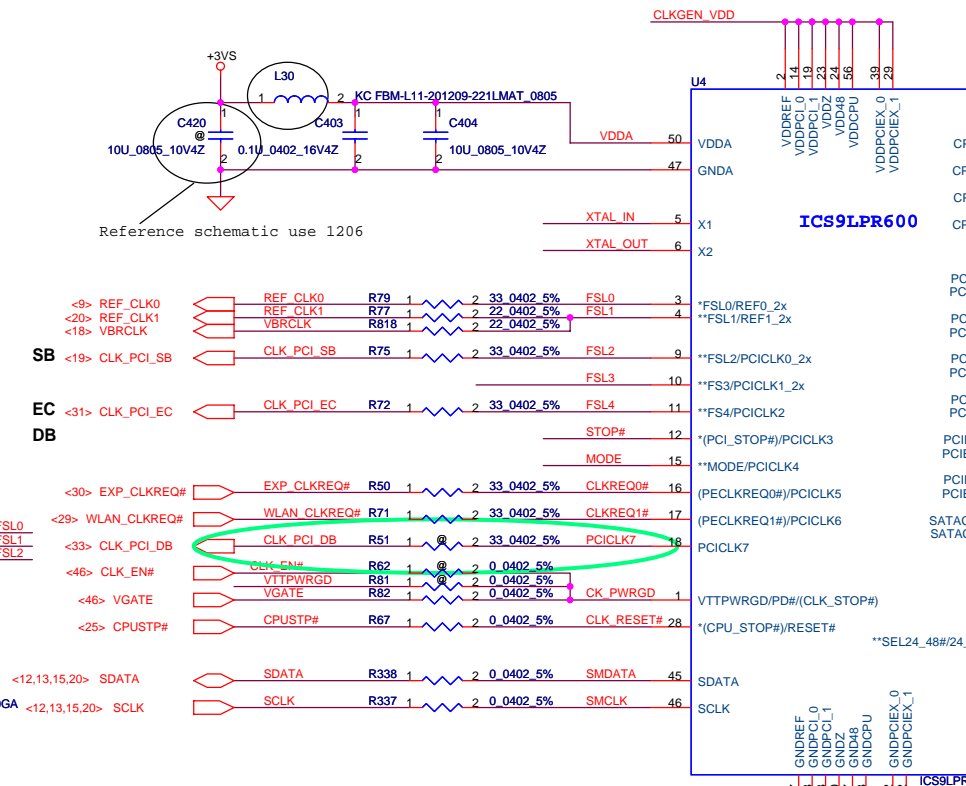
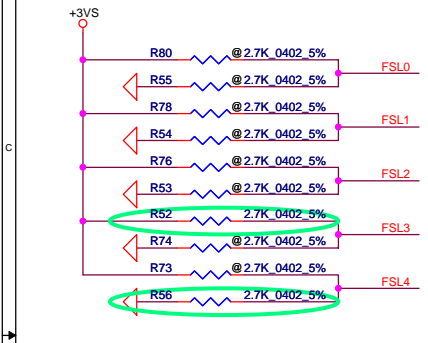


FSL4	FSL3	FSL2	FSL1	FSL0	CPU MHz	PCIE MHz	PCI MHz	ZCLK MHz
0	1	0	0	1	133	100	33.3	133
0	1	0	1	1	166	100	33.3	133
0	1	0	1	0	200	100	33.3	133

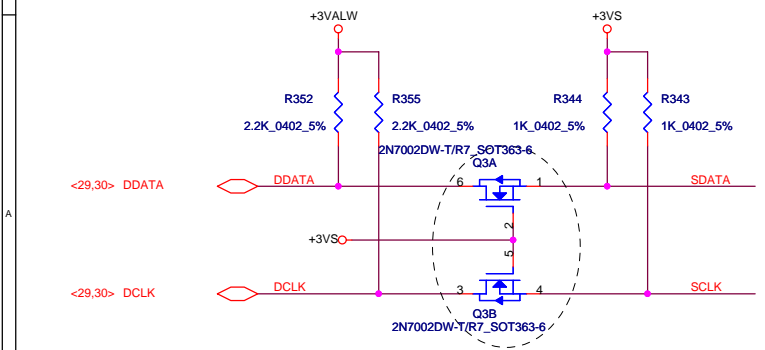
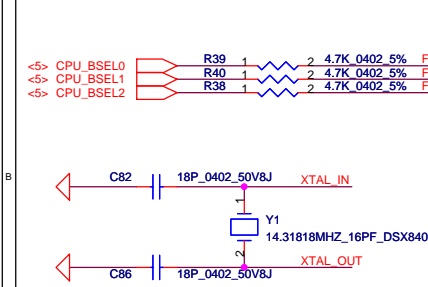
Use SB03904008L & SB000006A00 FootPrint



Remove R43 R66 R529 R527 and use PR39
Michael 2008/5/30



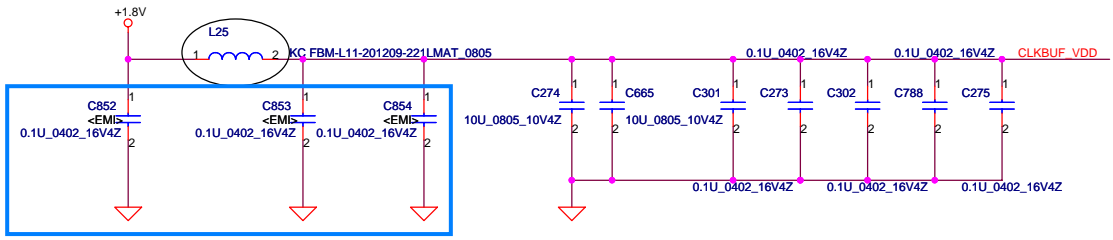
Pin 26 need BIOS to set disable,
for saving power & good EMI



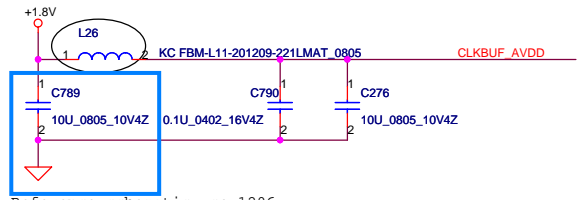
Replace Package from SOT23 to SOT363-6
Michael 2008/5/30

Z CLK0	C62	1	2	@ 10P_0402_50V8J
Z CLK1	C61	1	2	@ 10P_0402_50V8J
CLK_PCI_SB	C63	1	2	@ 10P_0402_50V8J
CLK_PCI_EC	C66	1	2	@ 10P_0402_50V8J
CLK_PCI_DB	C59	1	2	@ 10P_0402_50V8J
REF_CLK1	C65	1	2	@ 10P_0402_50V8J
REF_CLK1	C64	1	2	@ 10P_0402_50V8J

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Title: Clock Generator ICS9LPR600C Size: Document Number Custom: KFT00 M/B LA-4821P Schematic Rev: 1.0			

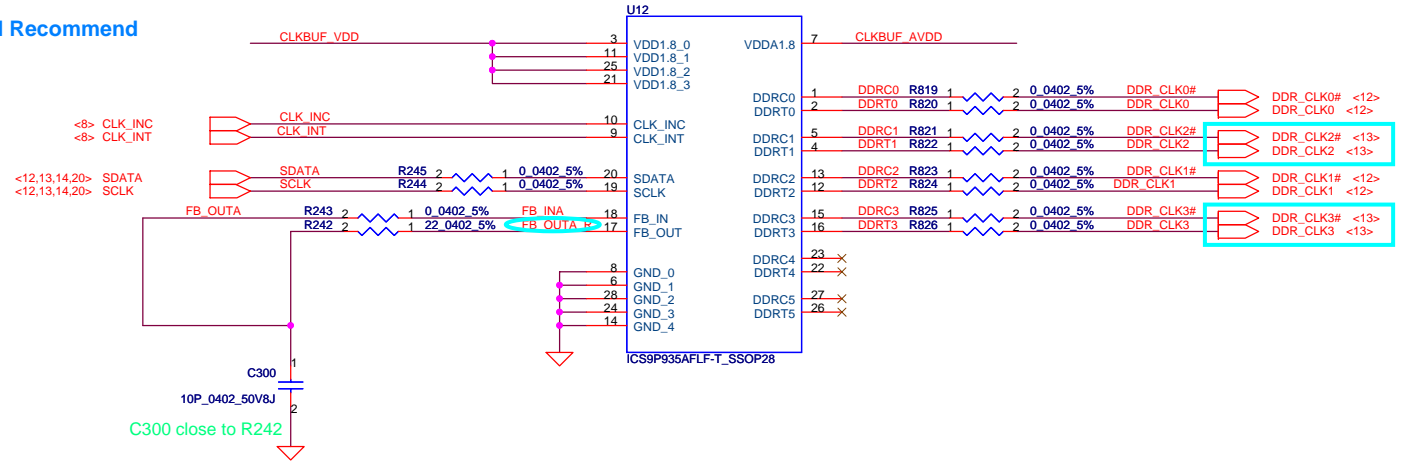


01/06 Add C852,C853,C854(0.1uF) for EMI Recommend



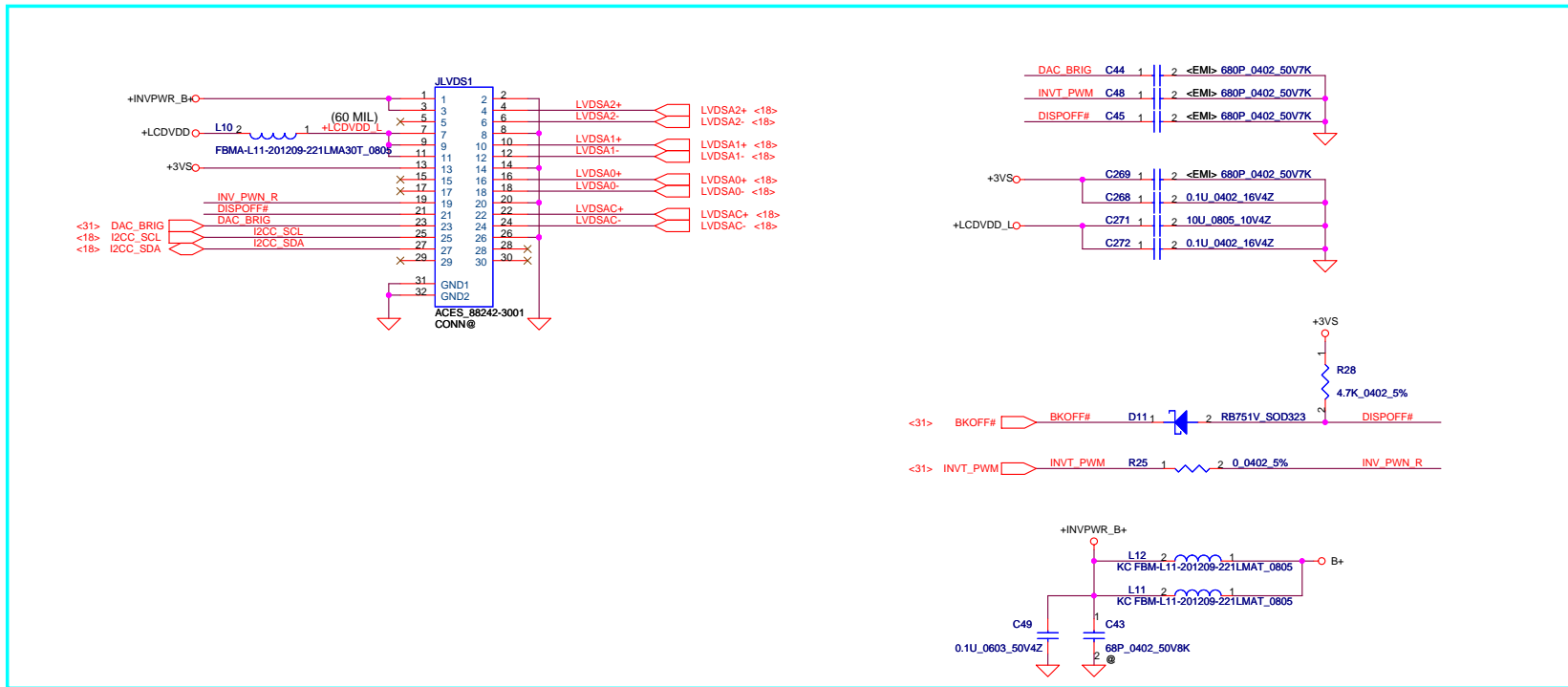
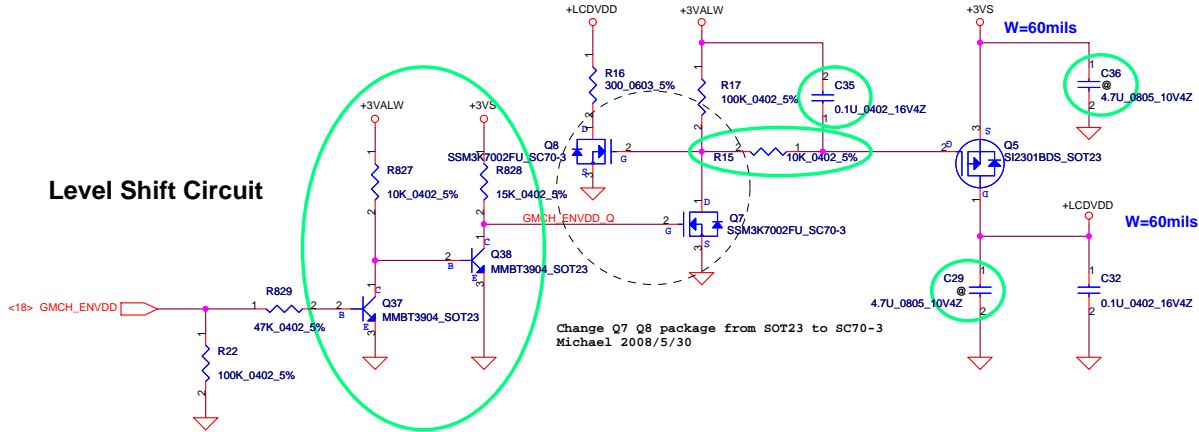
Reference schematic use 1206
01/10 Change C789 from @ to mount for EMI Recommend

Horizontal rotate



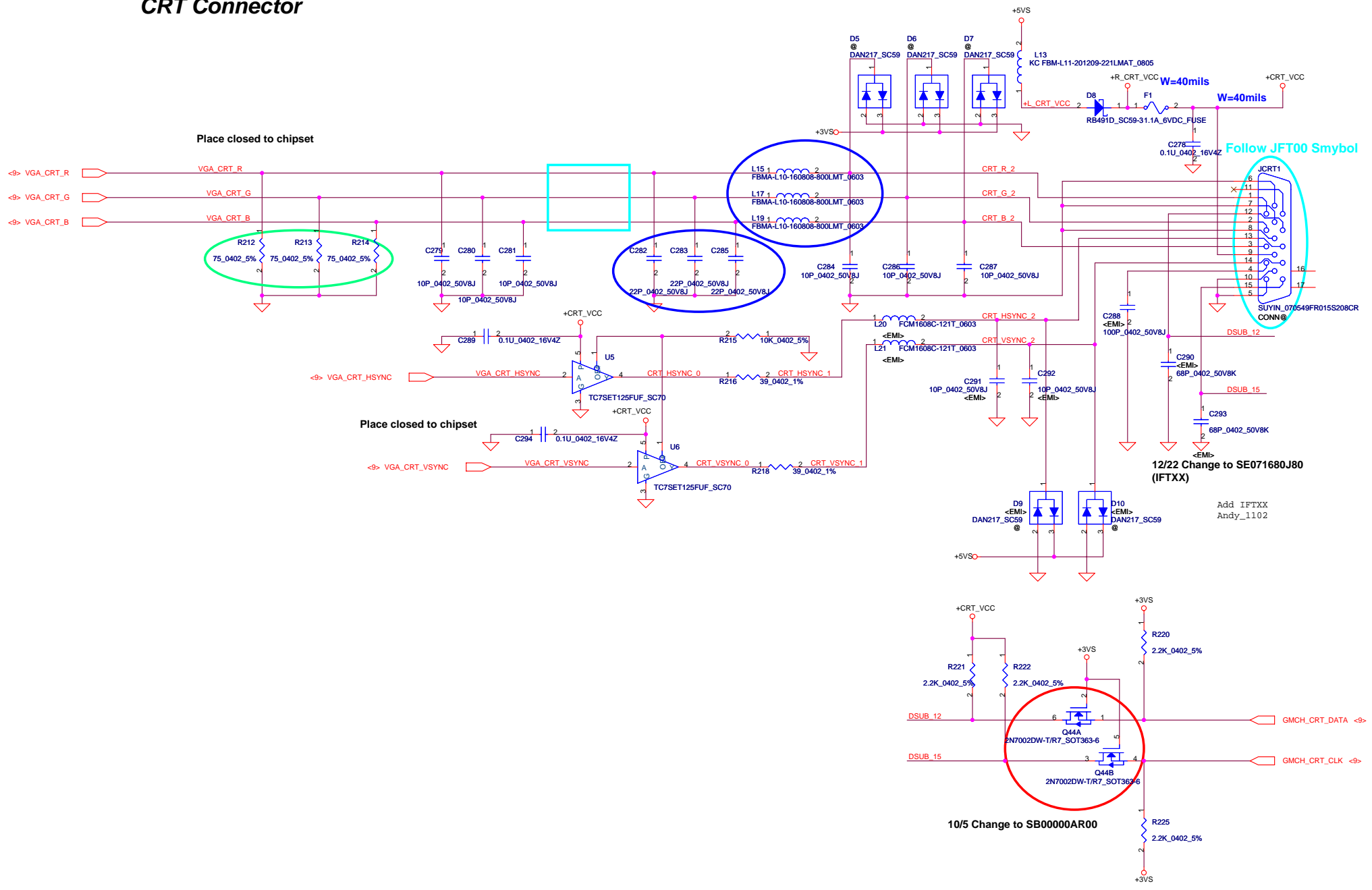
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Issued Date	2008/10/18	Deciphered Date	2009/10/18
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LCD POWER CIRCUIT

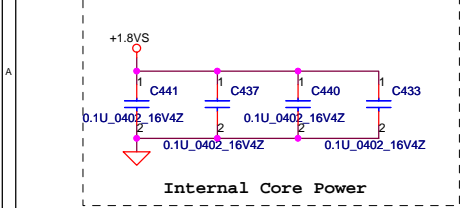
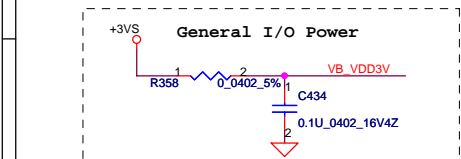
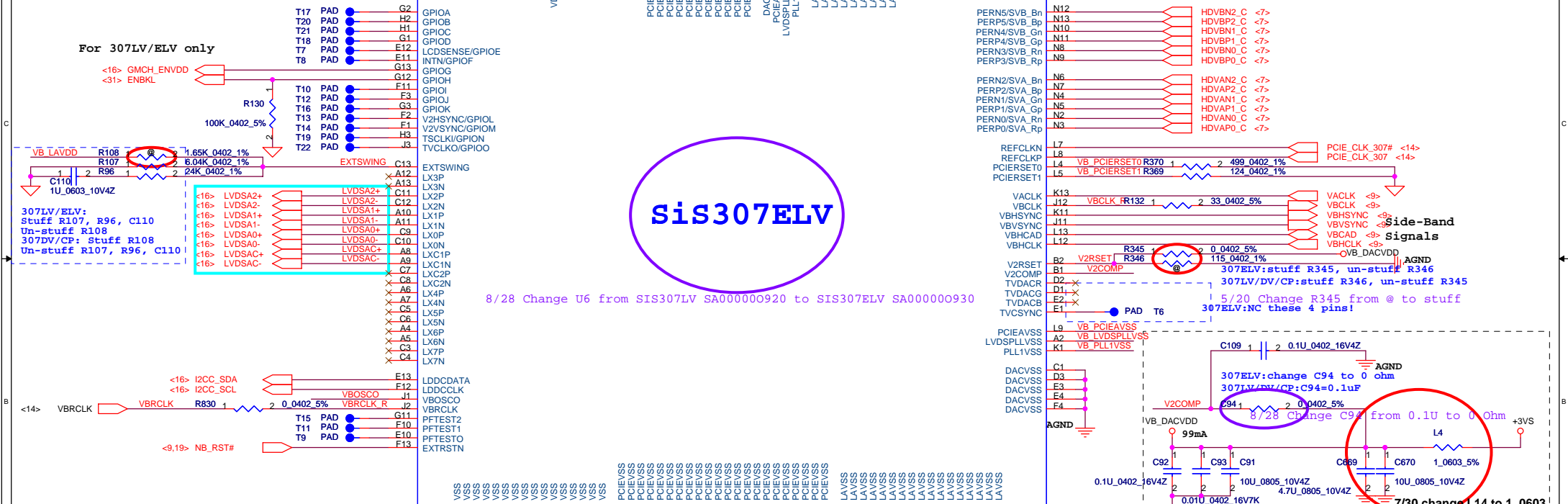
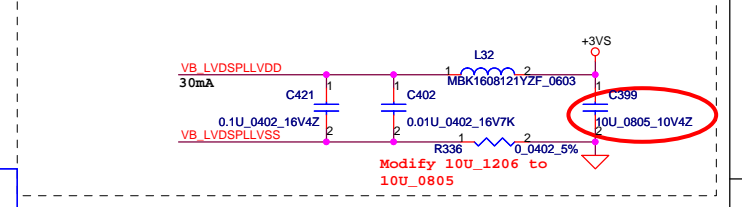
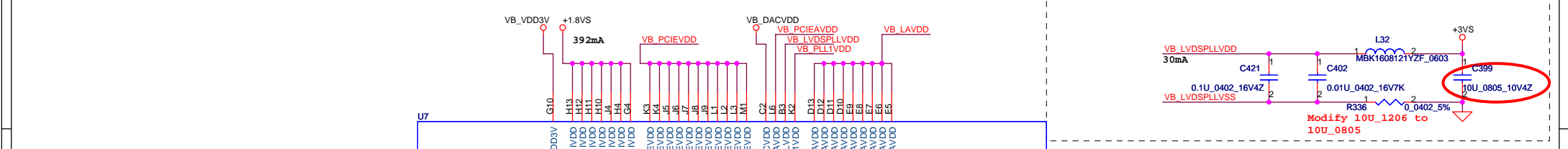
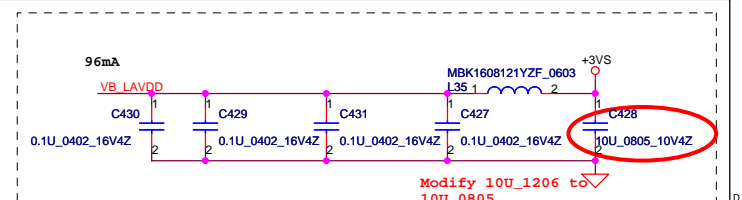
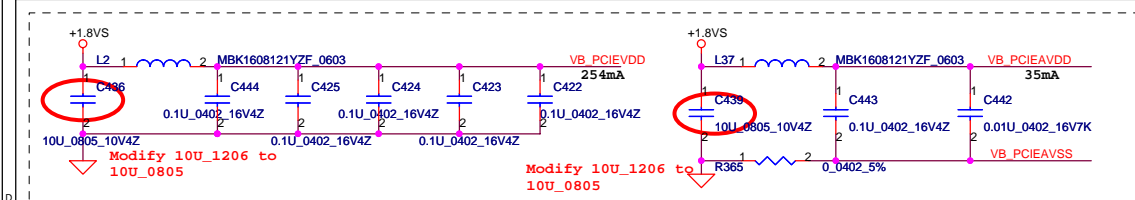


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				B	1.0
				Date:	Tuesday, March 10, 2009
				Sheet	16 of 47

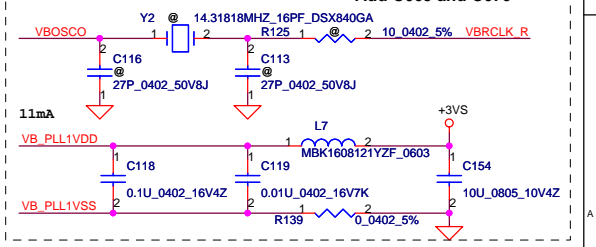
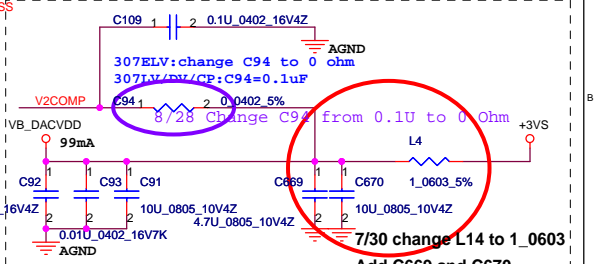
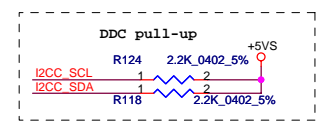
CRT Connector



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KFT00 M/B LA-4821P Schematic				Doc No.	17

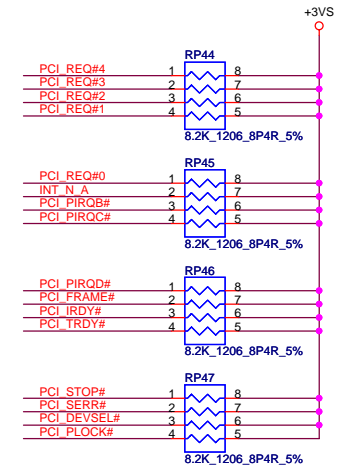
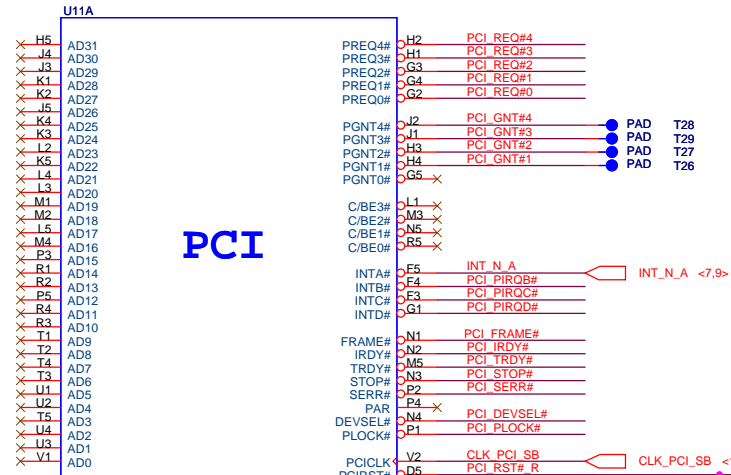


NOTE: all stuffed(default)
Modify before using!

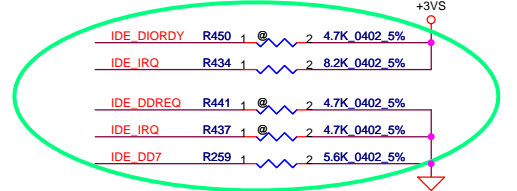
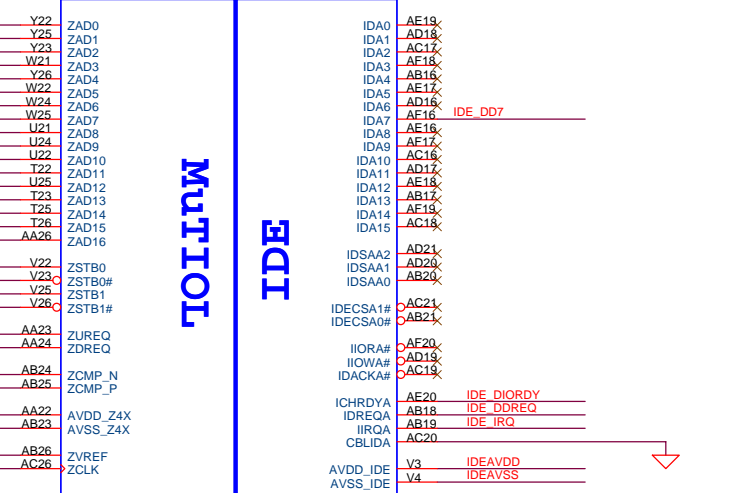


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Date:	Tuesday, March 10, 2009	Sheet	18	of	47

PCI

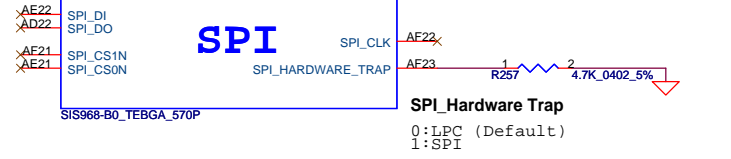


MULTI IDE

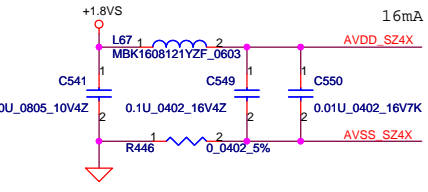
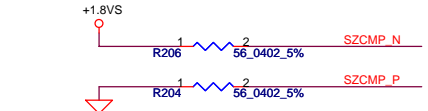
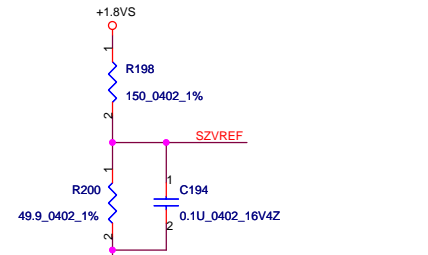
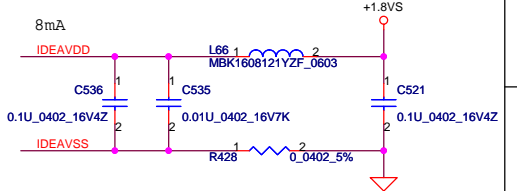


R450 => Intel :Pull-up 4.7K ohm (Mount) SIS : Pull-up ? ohm (Un-Mount)
 R434 => Intel :Pull-up 8.2K ohm (Mount) SIS :Not Pull-up
 R441 => Intel :Don't Pull-down SIS : Pull-down ? ohm (Un-Mount)
 R437 => Intel :Don't Pull-down SIS : Pull-down ? ohm (Un-Mount)
 R259 => Intel :Don't Pull-down SIS : Pull-down 5.6K ohm (Mount)

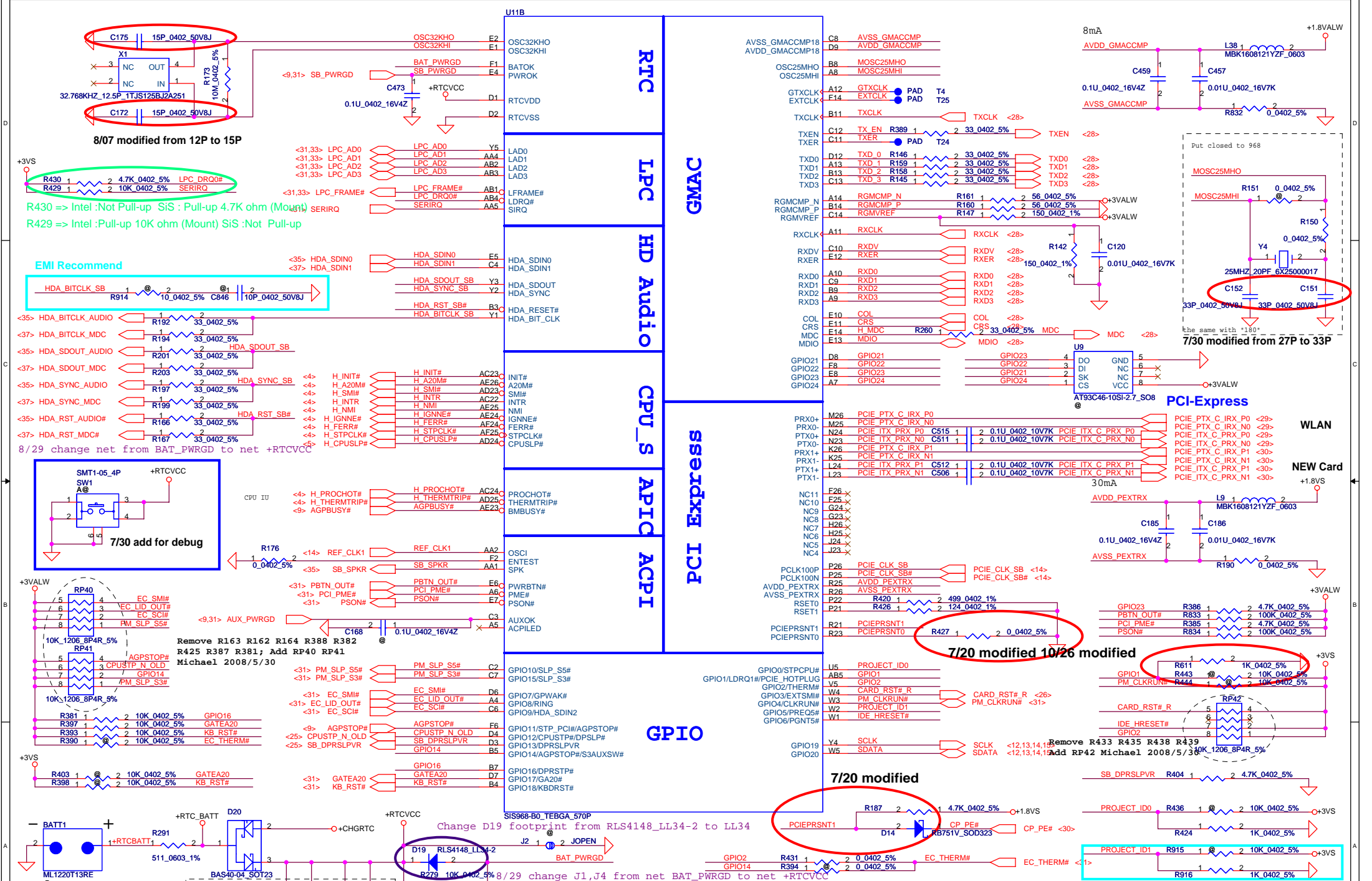
SPI



SPI Hardware Trap
 0:LPC (Default)
 1:SPI

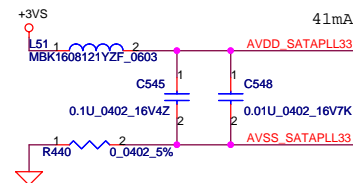
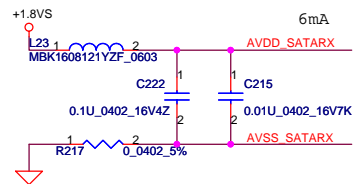
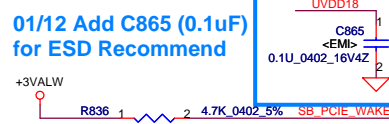
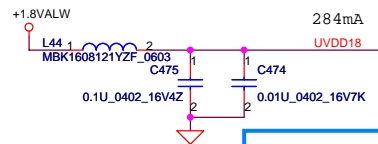
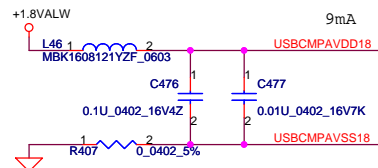
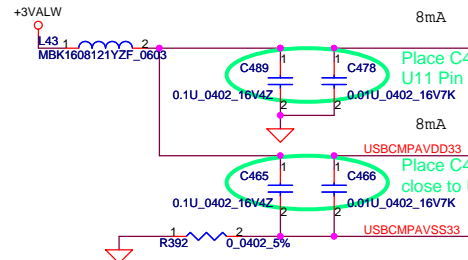
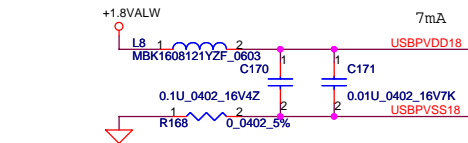


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Issued Date	2008/10/18	Deciphered Date	2009/10/18	Title	SIS968(1/5)-PCI_IDE_MuTIOL
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				Custbr	KFT00 M/B LA-4821P Schematic
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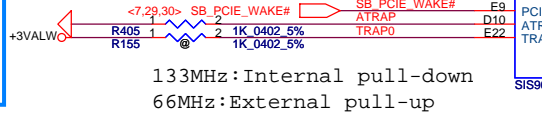
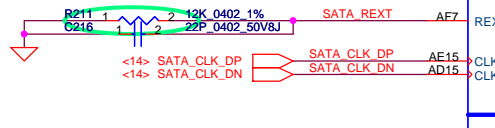
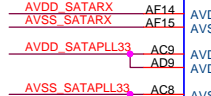
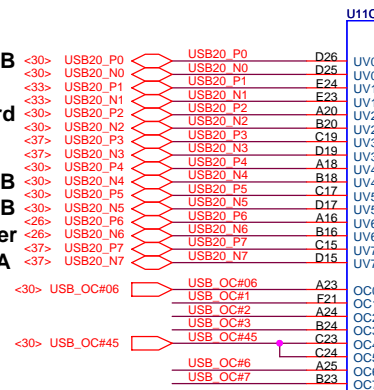
Compal Electronics, Inc.			
SIS968(2/5)-PCIE_LAN_RTC			
Size	Document Number		Rev
Custom	KFT00 M/B LA-4821P Schematic		1.0
Date:	Tuesday, March 10, 2009	Sheet	20 of 47



**USB
BT
New Card
FP
USB
USB
Card Reader
CAMERA**

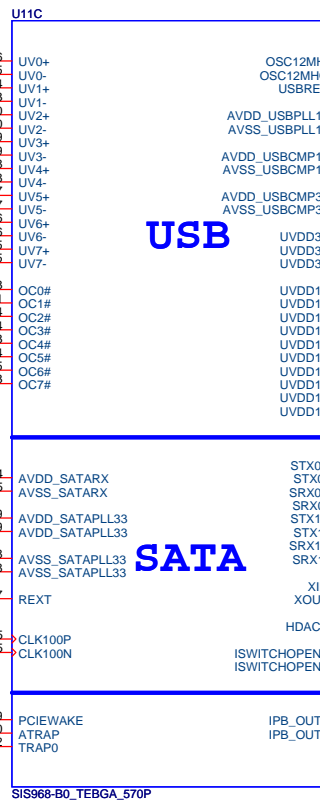
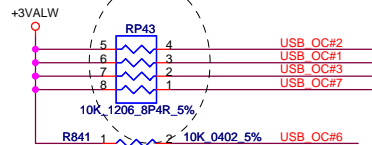
Place C478,C489 close to U11 Pin F17,F19,F22

Place C465,C466 close to U11 Pin D21



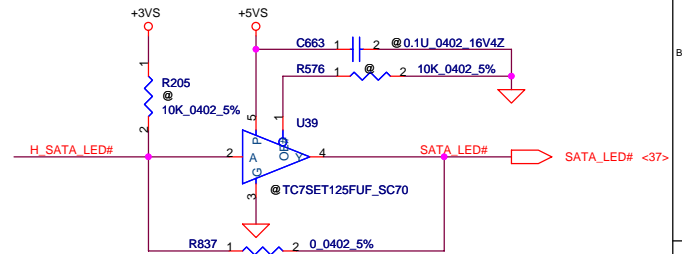
133MHz: Internal pull-down
66MHz: External pull-up

Remove R838 R839 R840 R552
Add RP43 Michael 2008/5/30



USB

SATA

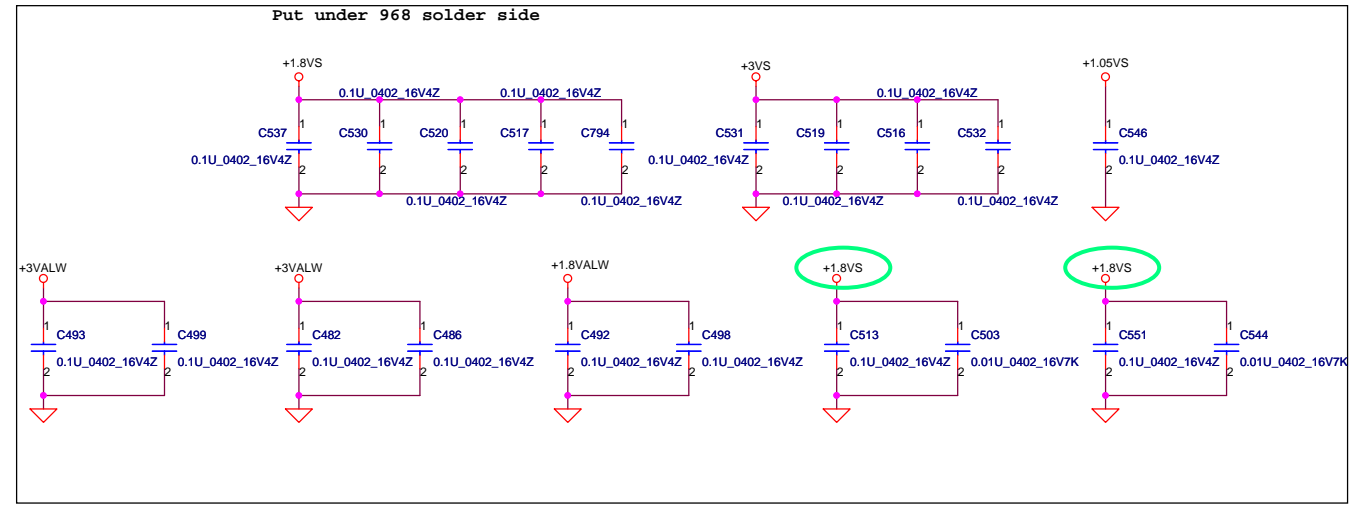
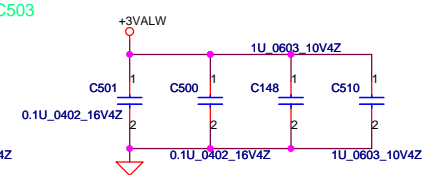
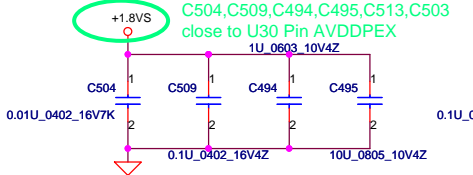
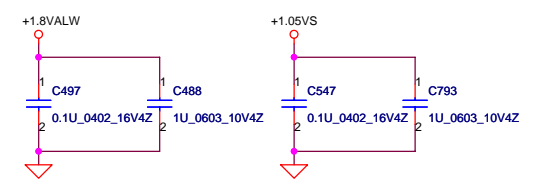
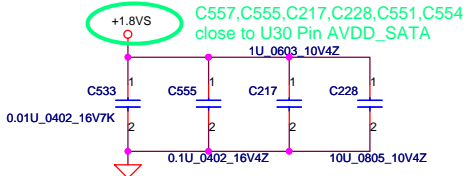
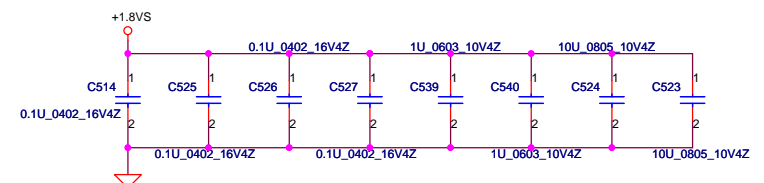
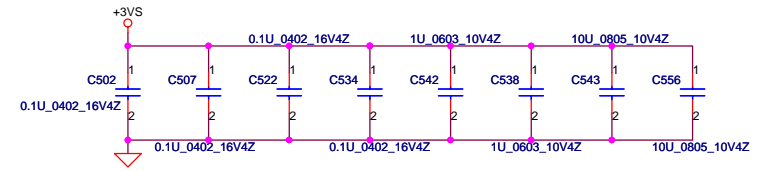
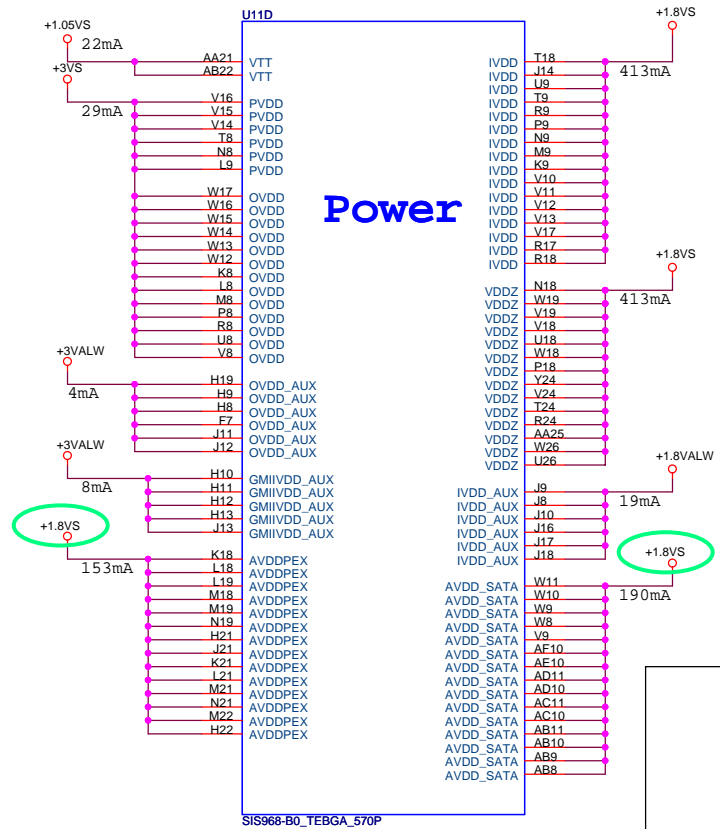


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Size	Document Number	Date		Rev	
Custom	KFT00 M/B LA-4821P-Schematic	Wednesday, March 10, 2009		1.0	

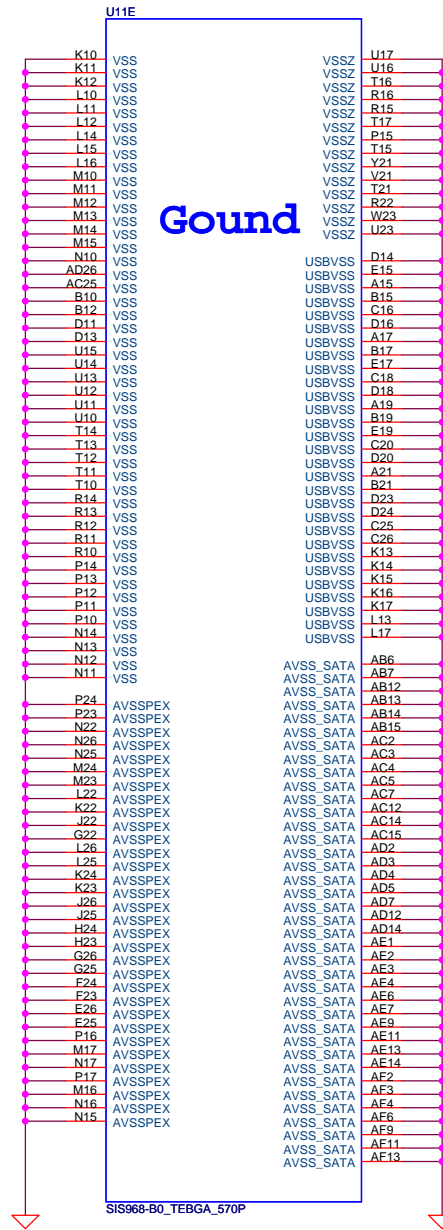
Compal Electronics, Inc.

SIS968(3/5)-USB_SATA

Size: Custom
Date: Wednesday, March 10, 2009
Rev: 1.0

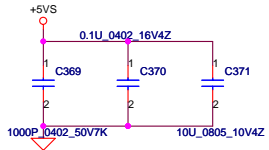


Security Classification		Compal Secret Data		Title	
Issued Date	2008/10/18	Deciphered Date	2009/10/18	SIS968(4/5)-POWER	
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				Custom	KFT00 M/B LA-4821P Schematic
				Date:	Tuesday, February 10, 2009
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				Rev	1.0

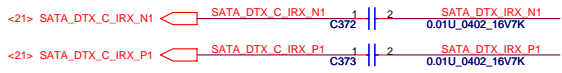
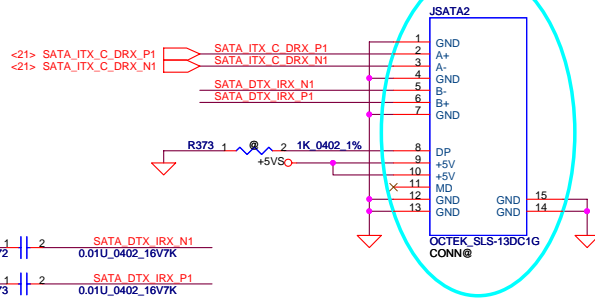


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Issued Date	2008/10/18	Deciphered Date	2009/10/18	Title	SIS968(5/5)-GND
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				Custom	KFT00 M/B LA-4821P Schematic
				Date:	Thursday, March 10, 2009 11:23 AM
				Rev	1.0

SATA ODD Conn.

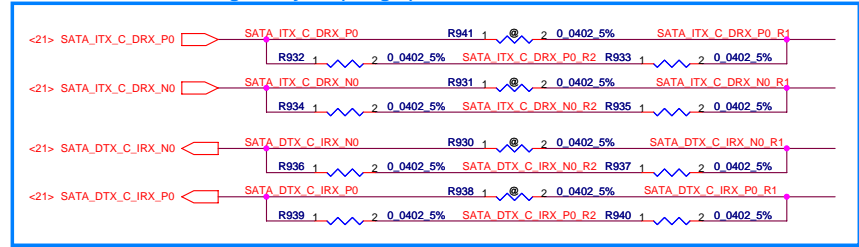


Follow JAT10 Smybol

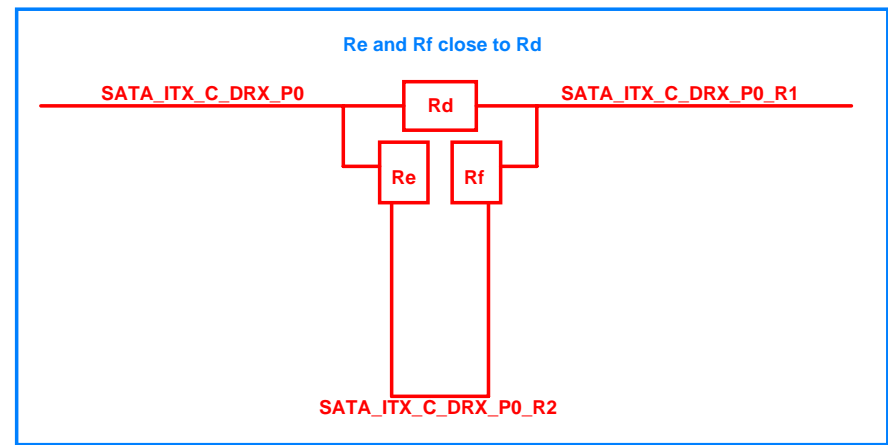
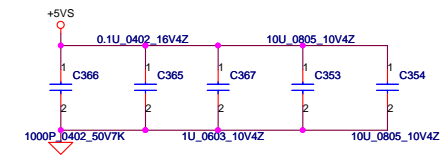
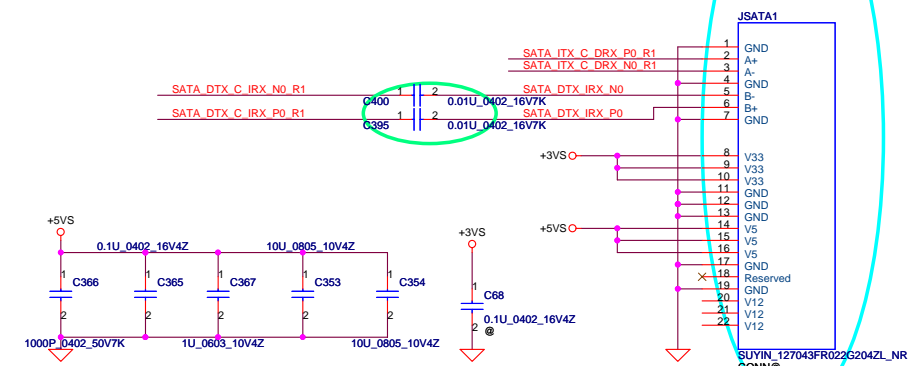


SATA HDD Conn.

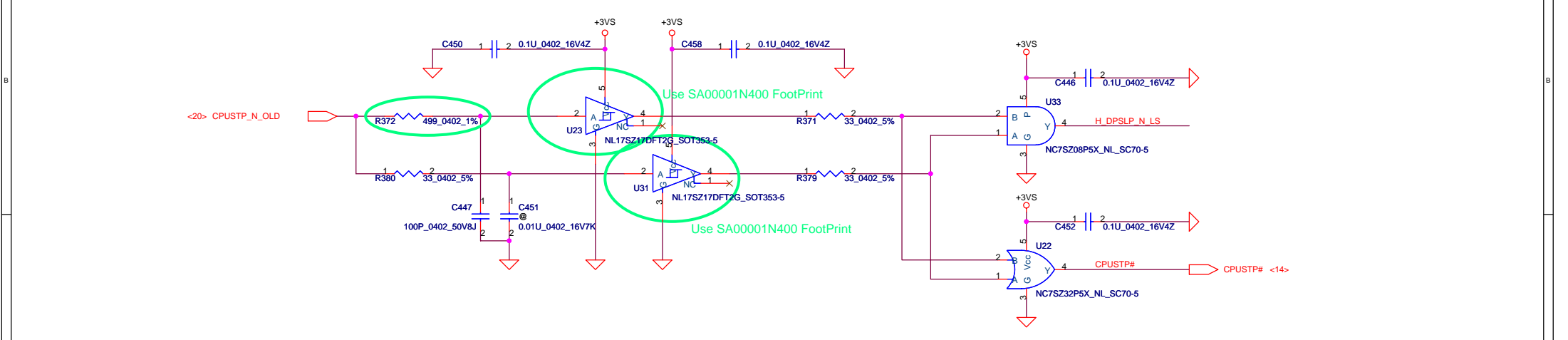
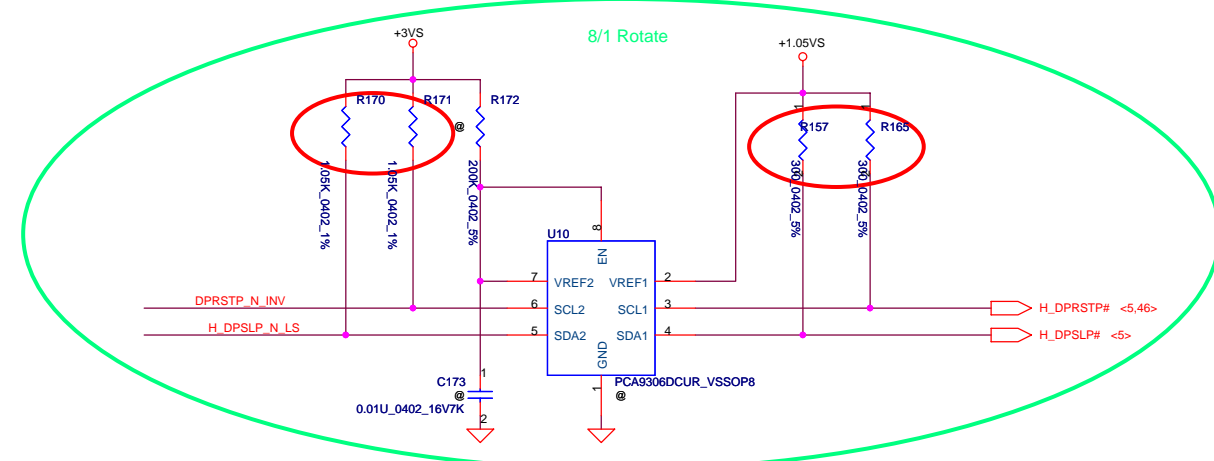
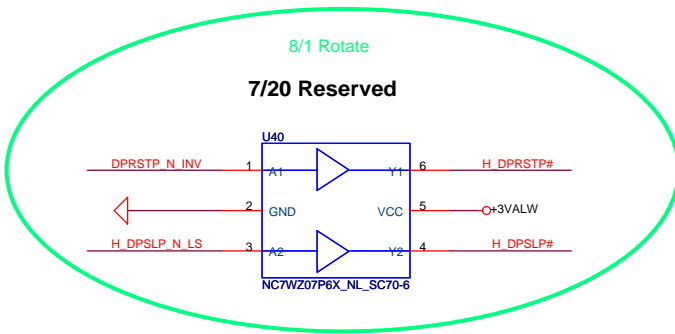
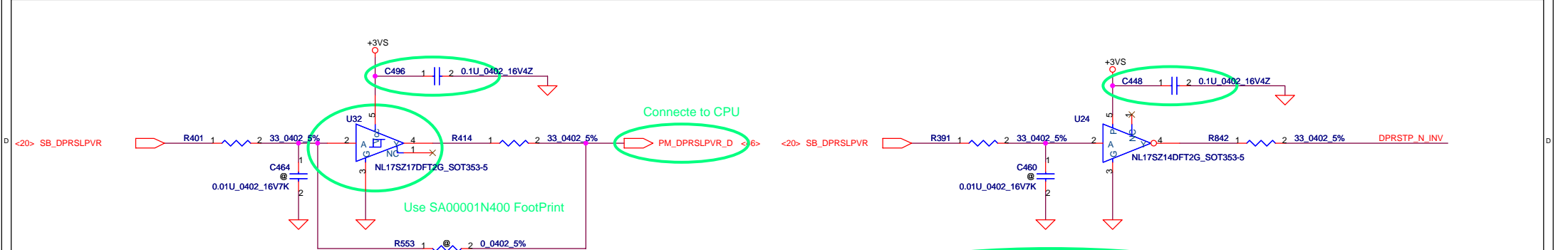
12/29 SATA trace routing for layout (Length)



Follow JFT00 Smybol

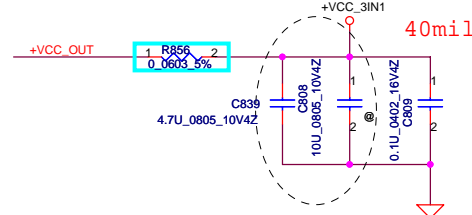
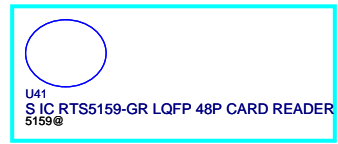
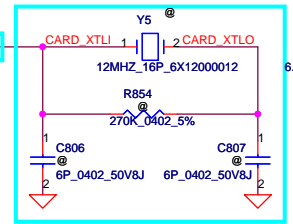
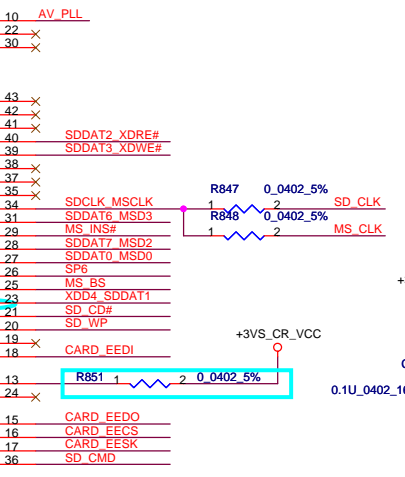
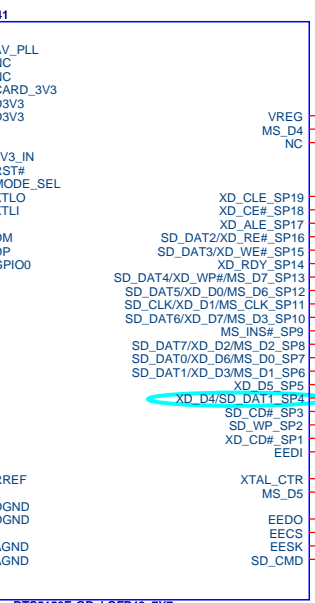
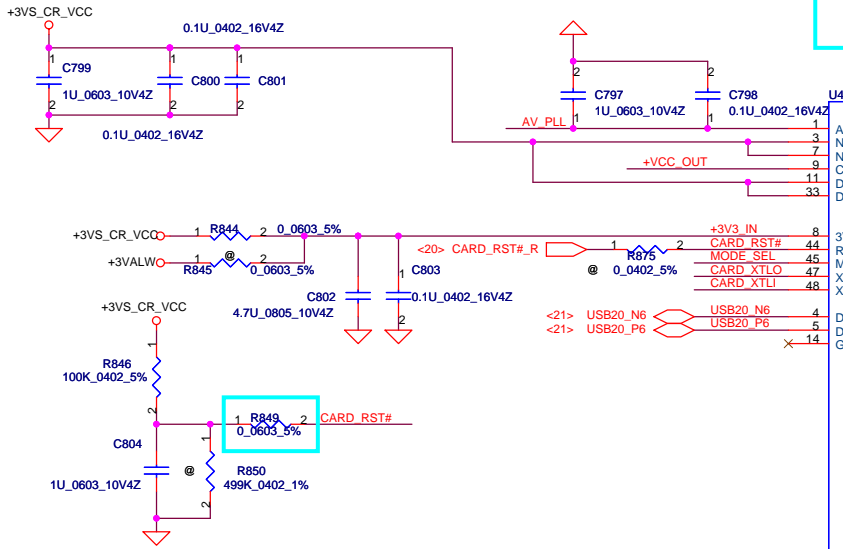
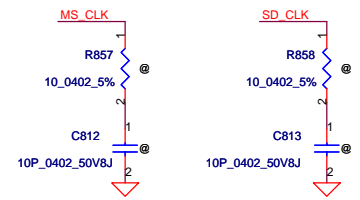
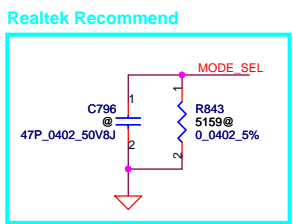


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				KFT00 M/B LA-4821P Schematic	
				Date:	Tuesday, March 10, 2009
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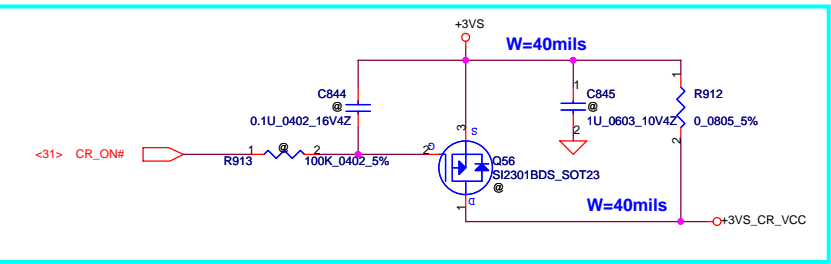


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Issued Date	2008/10/18	Deciphered Date	2009/10/18	Other	
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Change BOM control C796 R843 for 5158 and 5158E co-layout Michael 2008/6/18

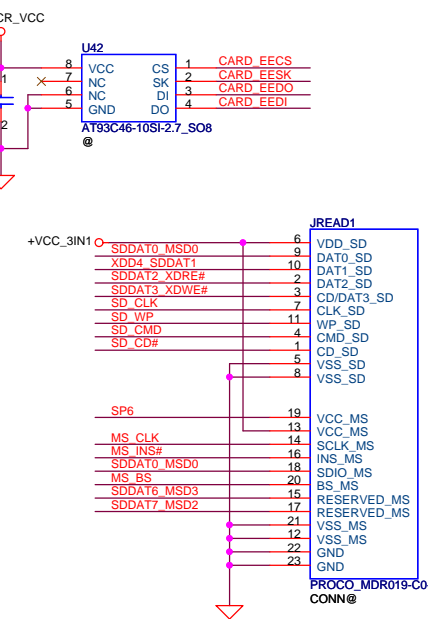


Add C822 4.7u and reserve C808 10u for cost down Michael 2008/5/30



SD,MMC,MS multi-function pin define

MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name
SP1			
SP2	SDWP#		
SP3	SDCD#		
SP4	SDCDAT1		MSWR
SP5			MSBS
SP6			MSCDAT1
SP7	SDCDAT0		MSCDAT0
SP8	SDCDAT7		MSCDAT2
SP9			MS_INS#
SP10	SDCDAT6		MSCDAT3
SP11	SDCLK		MSCCLK
SP12	SDCDAT5		MSCDAT6
SP13	SDCDAT4		MSCDAT7
SP14			
SP15	SDCDAT3		
SP16	SDCDAT2		
SP17			
SP18			
SP19			



5

4

3

2

1

D

D

C

C

B

B

A

A

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Issued Date	2008/10/18	Deciphered Date	2009/10/18	None	
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<p>DATE: Tuesday, February 10, 2009 18:58:27</p>				<p>Sheet 27 of 47</p>	

5

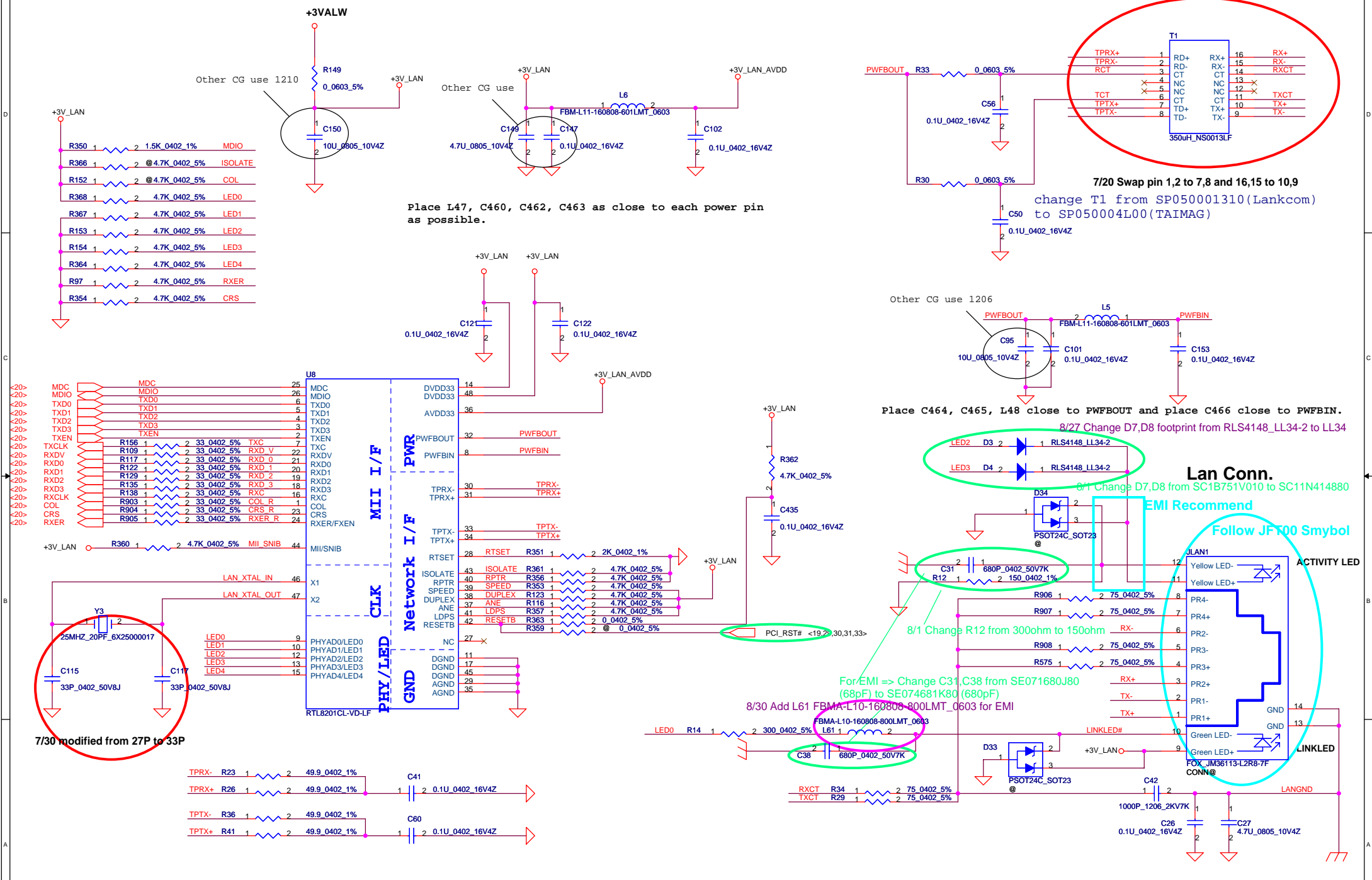
4

3

2

1





Place L47, C460, C462, C463 as close to each power pin as possible.

7/20 Swap pin 1,2 to 7,8 and 16,15 to 10,9 change T1 from SP050001310(Lankcom) to SP050004L00(TAIMAG)

Place C464, C465, L48 close to PWFBOU and place C466 close to PWFBIN.

8/27 Change D7,D8 footprint from RLS4148_LL34-2 to LL34

Lan Conn. 8/1 Change D7,D8 from SC1B751V010 to SC11N414880

EMI Recommend Follow JF-500 Symbol

7/30 modified from 27P to 33P

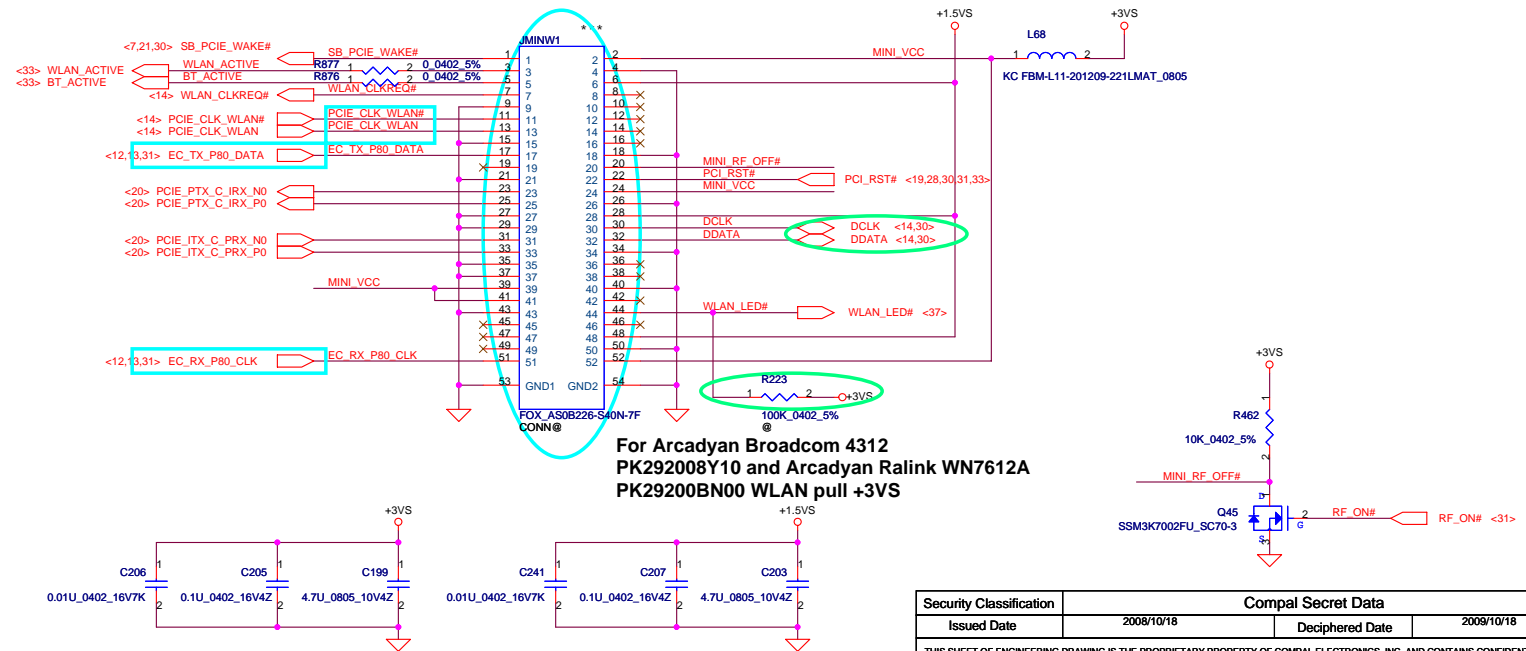
For EMI => Change C31, C38 from SE071680J80 (68pF) to SE074681K80 (680pF)

8/30 Add L61 FBMA-L10-160808-800LMT_0603 for EMI

LED0	LED1	LED2	LED3	LED4
Link	Dupx	10Act	100Act	COL

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Custom	KFT00 M/B LA-4821P Schematic	Tuesday, March 10, 2009	Sheet	28 of 47	1.0	

Mini-Express Card for WLAN Follow JFT00 Smybol

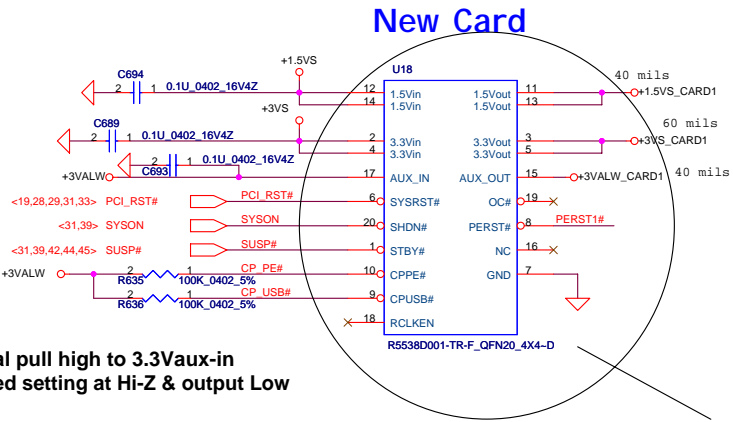


**For Arcadyan Broadcom 4312
PK292008Y10 and Arcadyan Ralink WN7612A
PK29200BN00 WLAN pull +3VS**

Please place these caps between JMIN1 and JMIN2

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Doc #	Document Number	Sheet	23	Rev	1.0

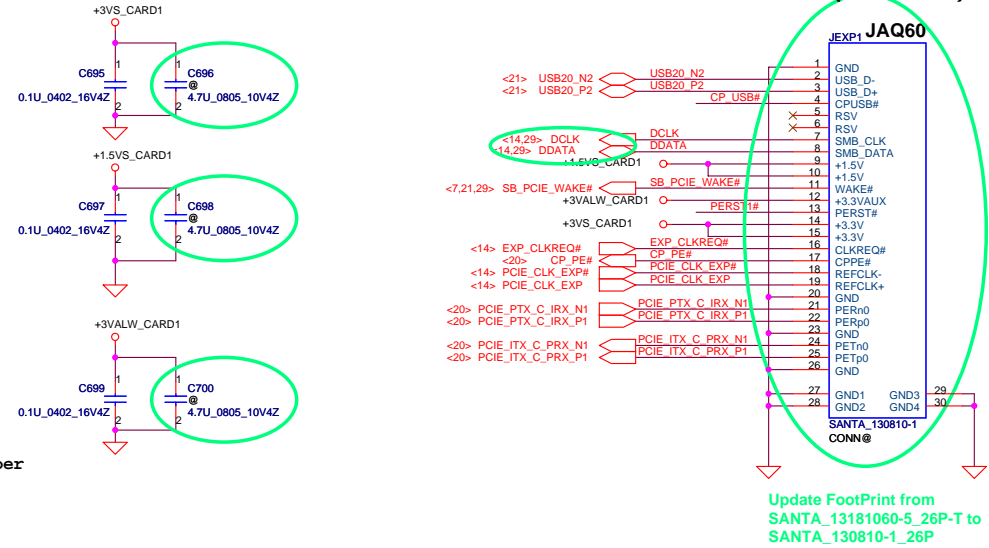
New Card Power Switch



internal pull high to 3.3Vaux-in
EC need setting at Hi-Z & output Low

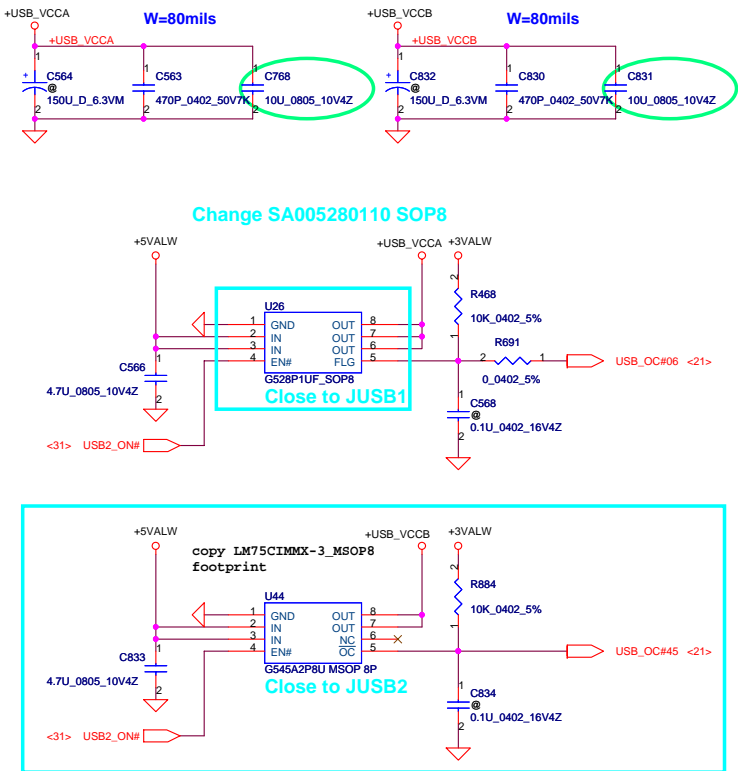
Change to GMT PartNumber

New Card Socket (Left/TOP)



Update FootPrint from
SANTA_13181060-5_26P-T to
SANTA_130810-1_26P

USB Connector

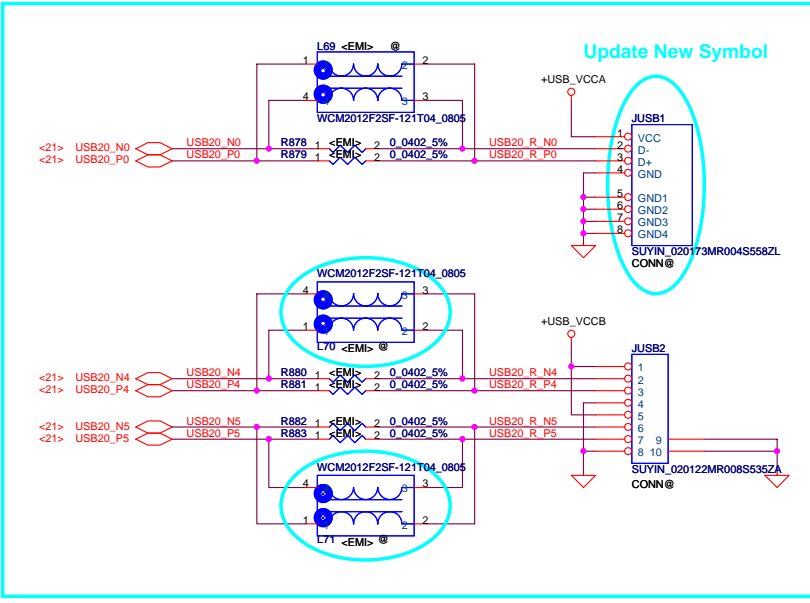


Change SA005280110 SOP8

Close to JUSB1

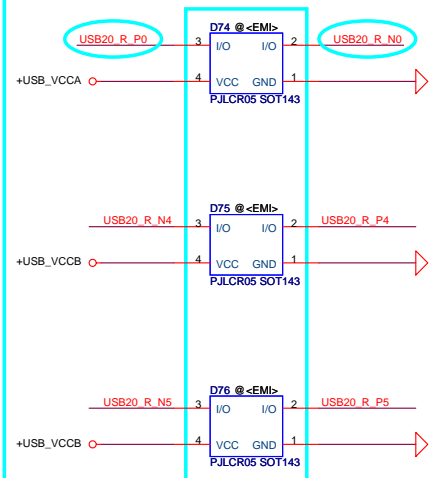
Close to JUSB2

11/29 change this symbol's footprint as
ADT7421ARMZ-REEL_MSOP8



Update New Symbol

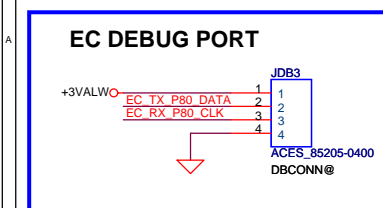
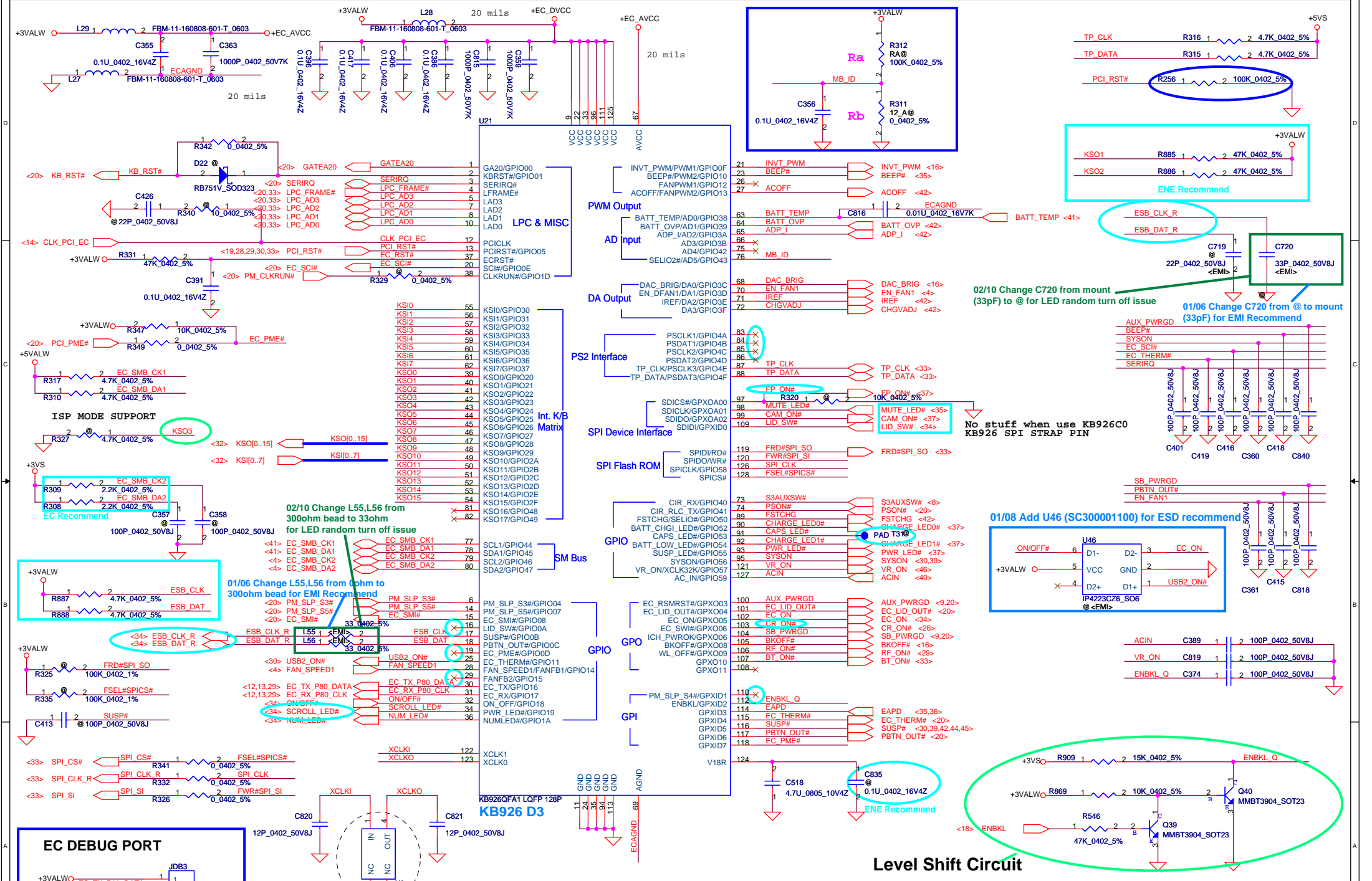
01/06 Add C860 for ESD Recommend



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Issued Date	2008/10/18
Deciphered Date	2009/10/18

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Compal Electronics, Inc.		
New Card & USB Connector		
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Date:	Tuesday, March 10, 2009	Sheet 30 of 47



Modify X2 part number from SJ132P7KW10 to SJ132P7K220 for cost down; Michael 2008/5/30

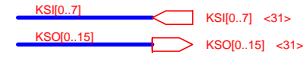
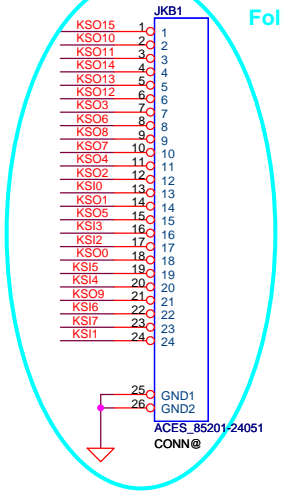
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Issued Date	2008/10/18	Deciphered Date	2009/10/18

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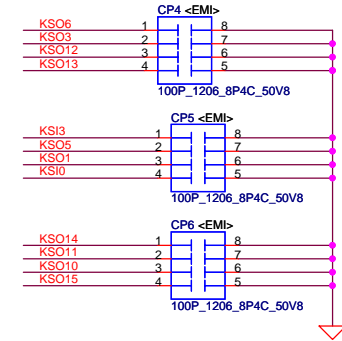
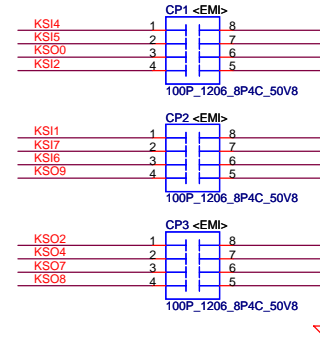
Compal Electronics, Inc.			
Title		EC_KB926	
Size	Document Number	Rev	
Custom	KFT00 M/B LA-4821P Schematic	1.0	
Date:	Thursday, March 10, 2009	Sheet	31 of 47

INT_KBD Conn.

Follow JFT00 Symbol

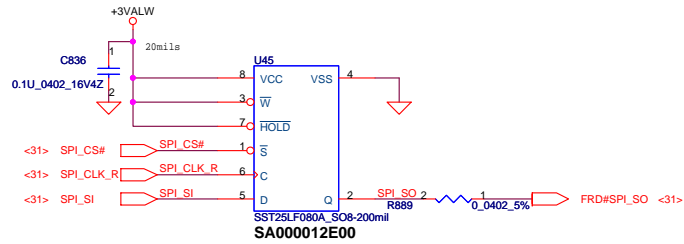


Delete C525~C548 SE071101J80 (100pF)
 Add SI102101K80 (CP : 100pF)
 (EMI Recommend)



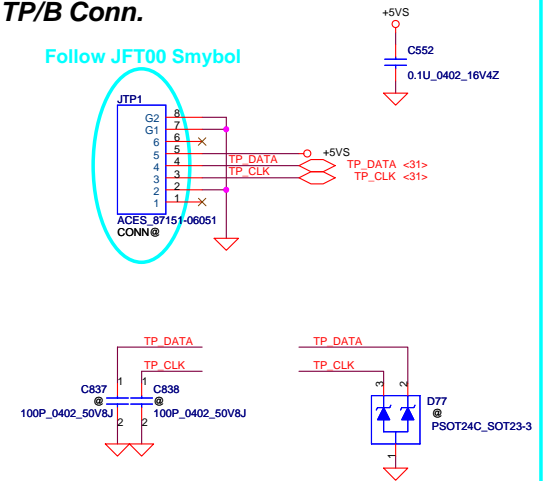
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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				Date: Tuesday, March 10, 2009	Rev 1.0
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8M SPI ROM For EC+BIOS



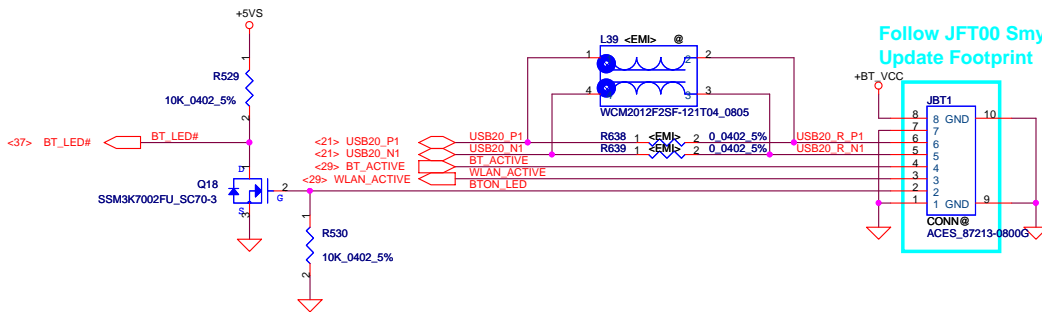
To TP/B Conn.

Follow JFT00 Symbol

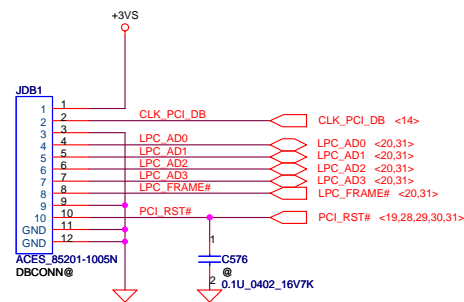
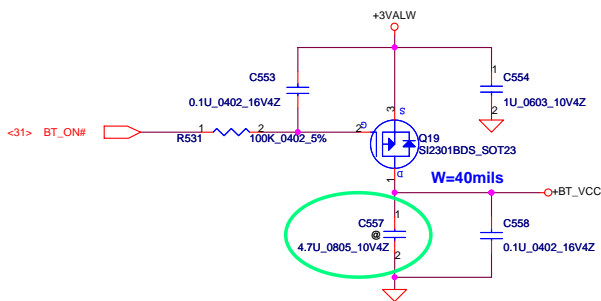


Bluetooth Conn.

Follow JFT00 Symbol
Update Footprint

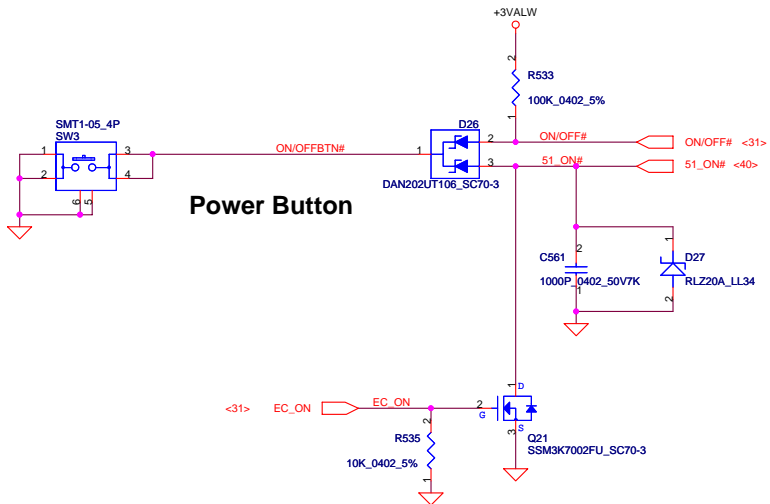


FOR LPC DEBUG PORT

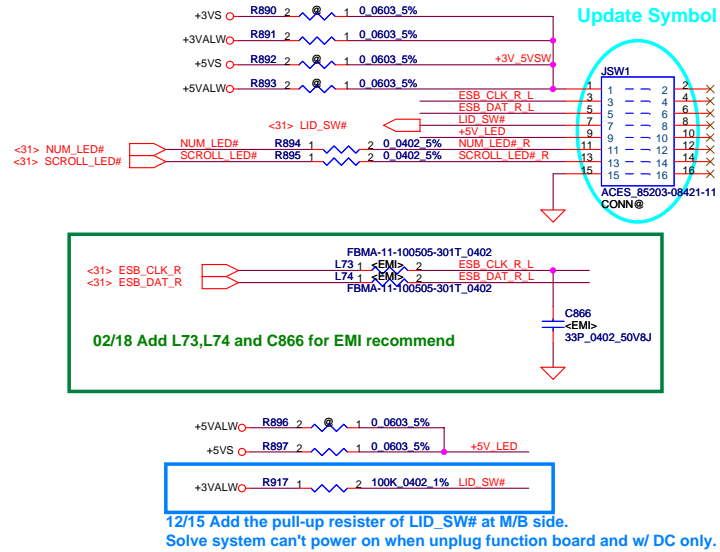


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Size	B				1.0
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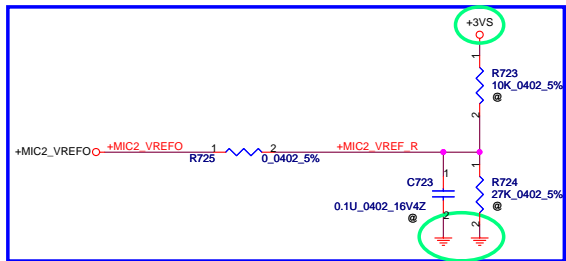
ON/OFF switch



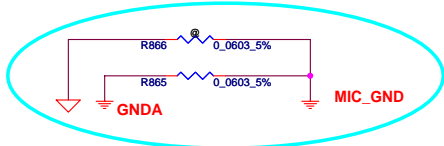
Conductive Board Conn.



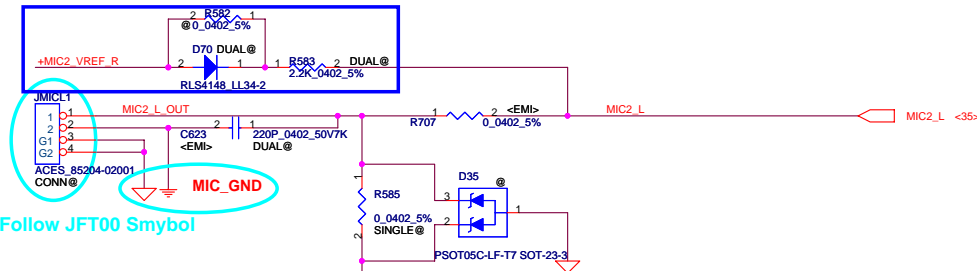
SINGLE INT MIC/DUAL INT MIC



Internal MIC component close to U27

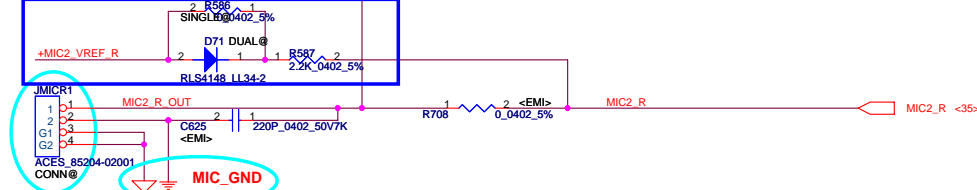


Internal MIC component close to U27



Follow JFT00 Symbol

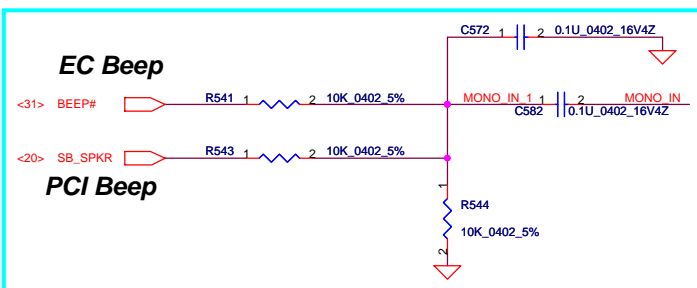
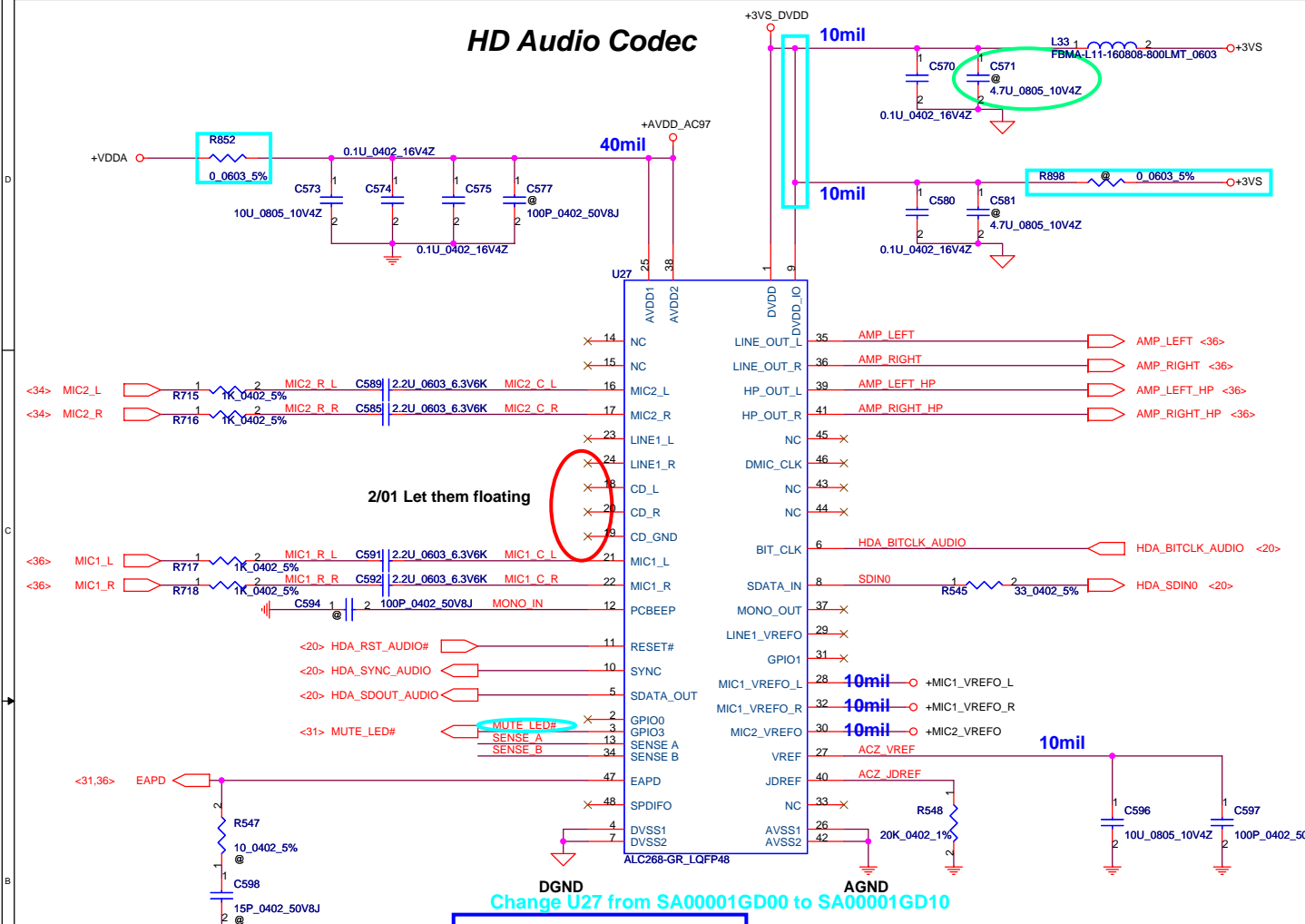
Internal MIC component close to U27



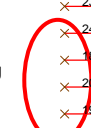
Follow JFT00 Symbol

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				KFT00 M/B LA-4821P Schematic	
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HD Audio Codec

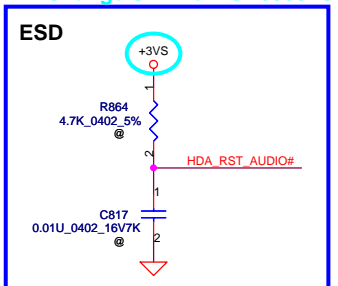


2/01 Let them floating

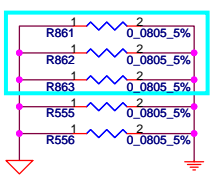


Sense Pin	Impedance	Codec Signals	Function
SENSE A / B	39.2K	PORT-A (PIN 39, 41)	HP
	20K	PORT-B (PIN 21, 22)	MIC
	10K	PORT-C (PIN 23, 24)	LINE IN
SENSE B	5.1K	PORT-D (PIN 35, 36)	LINE OUT
	39.2K	PORT-E (PIN 14, 15)	HP
	20K	PORT-F (PIN 16, 17)	MIC
	10K	PORT-G (PIN 43, 44)	LINE IN
	5.1K	PORT-H (PIN 45, 46)	LINE OUT

Change U27 from SA00001GD00 to SA00001GD10



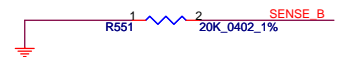
Moat Bridge



SENSE FOR Ext. Mic.



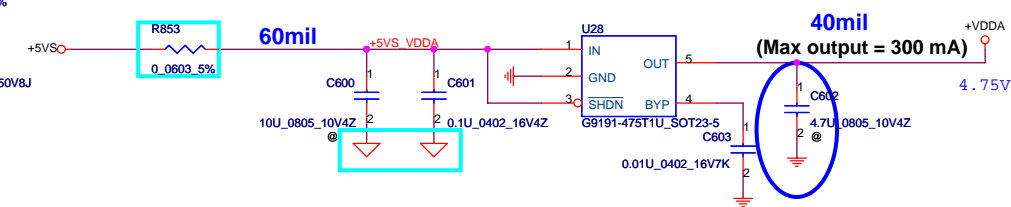
SENSE FOR Solo Int. Mic.



SENSE FOR HP



Regulator for CODEC



10/2 change circuit

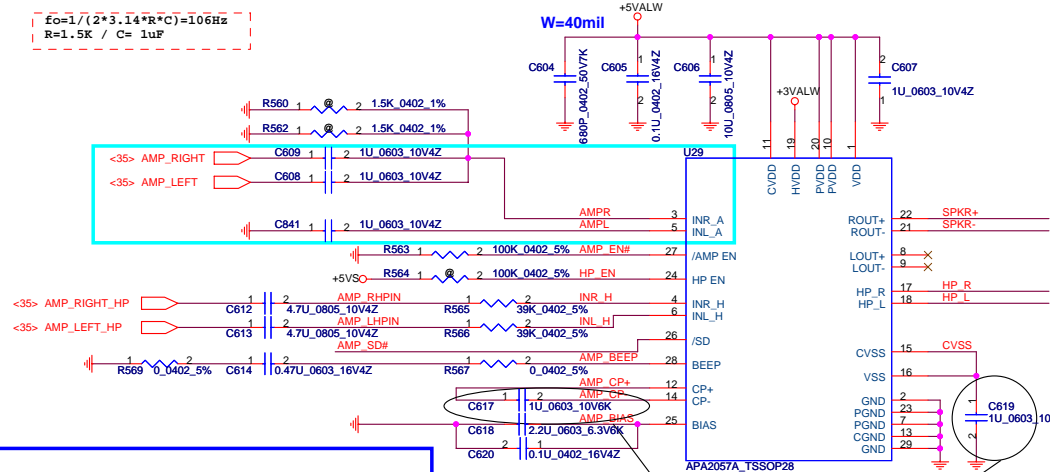
U8 change footprint

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Size	Document Number	Date	Friday, March 10, 2009	Sheet	35 of 47

APA2057 SPK/HP Amplifier

$$f_o = 1 / (2 * 3.14 * R * C) = 106\text{Hz}$$

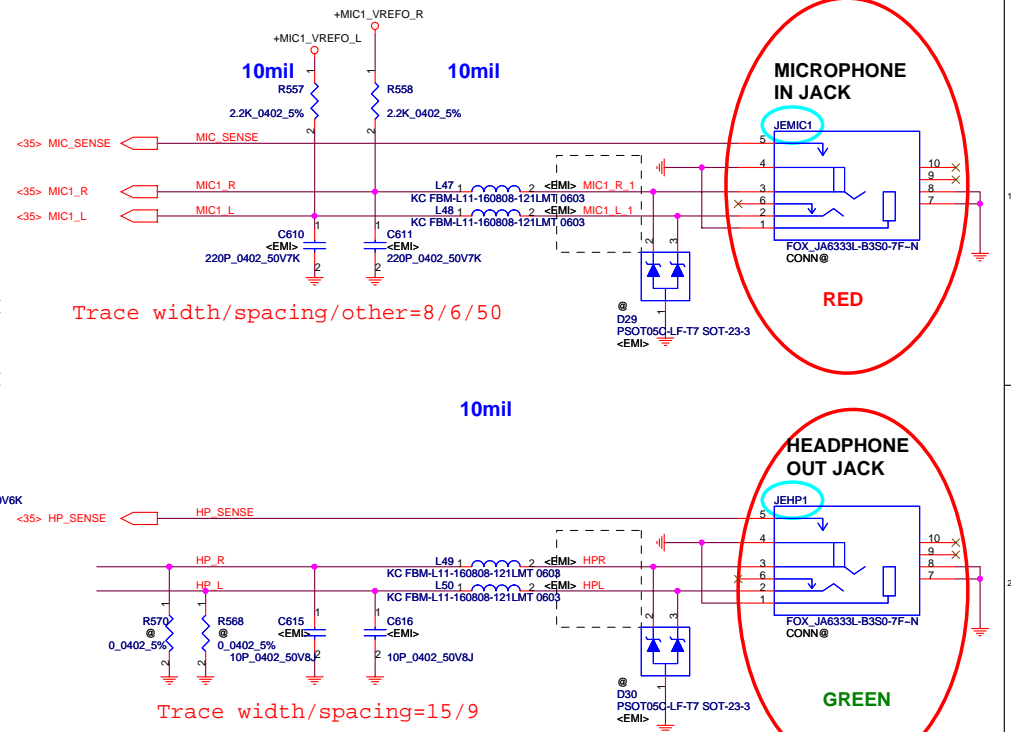
$$R = 1.5\text{K} / C = 1\mu\text{F}$$



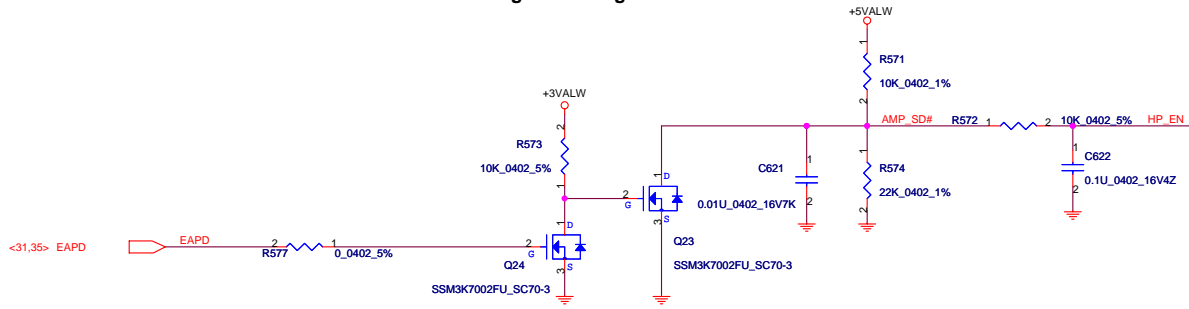
9/5 If implement AMP BEEP, Swap C641 and R524, R524 change from 0 Ohm to 47K

IN_A Gain = 10dB (Internal Speaker)
IN_H Gain = 0dB (Headphone)

11/28 Modified to X5R
11/28 Change to SE080105K80



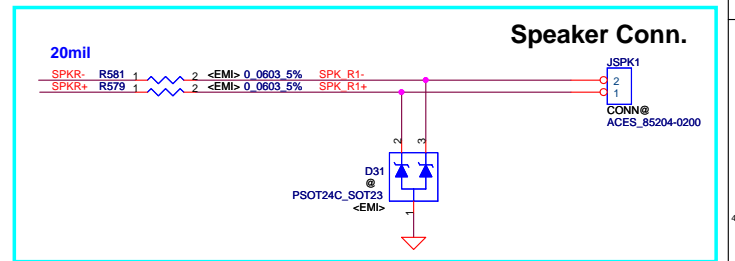
Add below circuit for APA2057 gain tuning use



Gain= 10dB

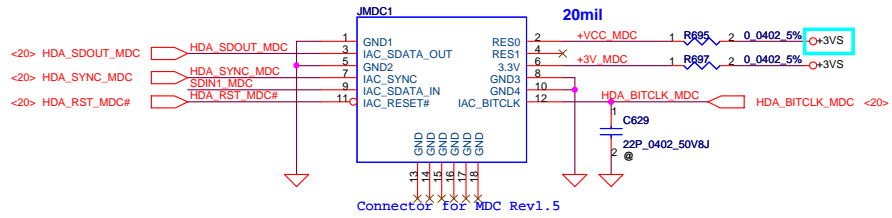
Gain (dB)	Low (V)	High (V)	Recommended (V)
10	3.45	3.51	3.48
11	3.56	3.62	3.59
12	3.68	3.73	3.70
13	3.80	3.85	3.82

+5VALW assume equal 5.1V
10 dB ----> 5.1 x 220 / 320 = 3.5



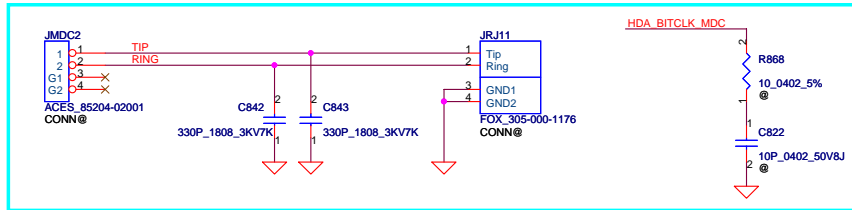
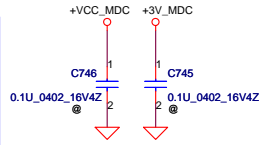
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Issued Date	Deciphered Date	AMP/VR/Audio Jack	
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		Document Number	1.0
		Customer	KFT00 M/B LA-4821P Schematic
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MDC Conn.

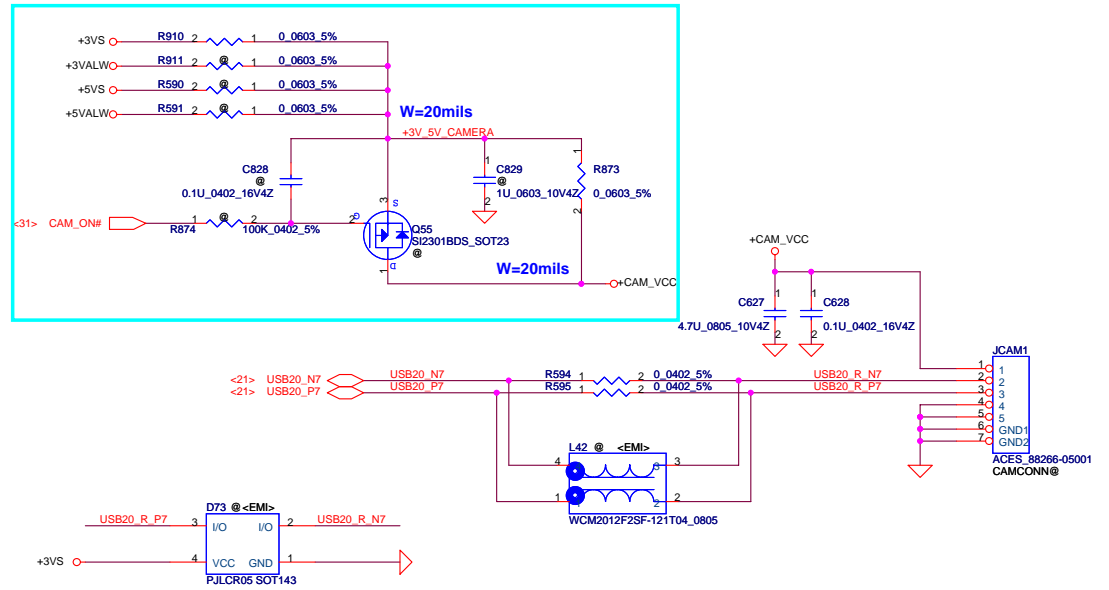


Please add these caps close to JMD1 as close as possible,

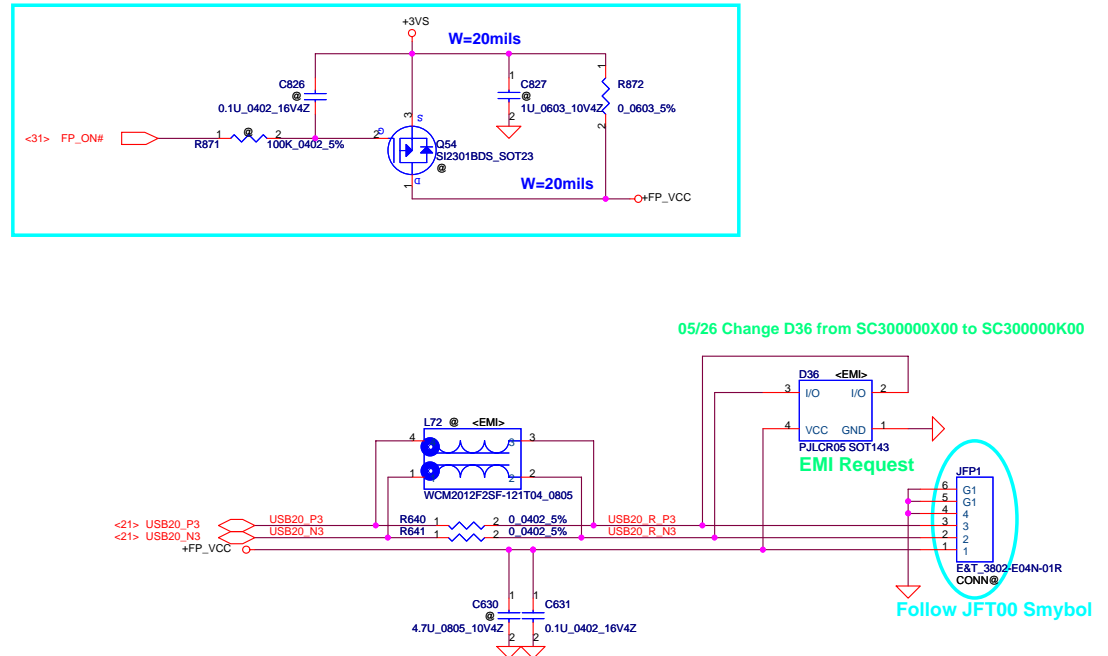
HDA_SDOUT_MDC	C752	1	2	@ 100P_0402_50V8J
HDA_SYNC_MDC	C753	1	2	@ 100P_0402_50V8J
HDA_RST_MDC#	C754	1	2	@ 100P_0402_50V8J
HDA_SDIN1	C756	1	2	@ 100P_0402_50V8J



Camera Conn



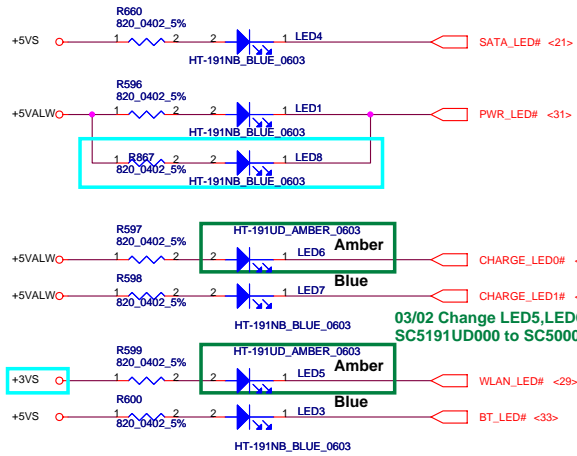
Finger Print board



05/26 Change D36 from SC30000X00 to SC30000K00

03/02 Change LED5,LED6 from SC5191UD000 to SC500005T00

LED

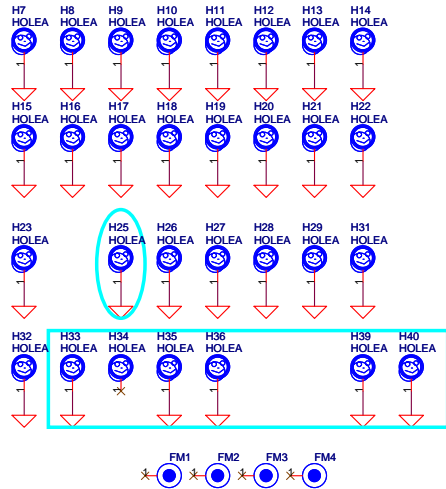


12/7 Modified LED footprint to LED_HT-297UD-CB_4P
 12/15 Modified to correct LED symbol!

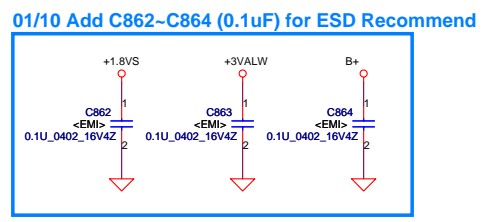
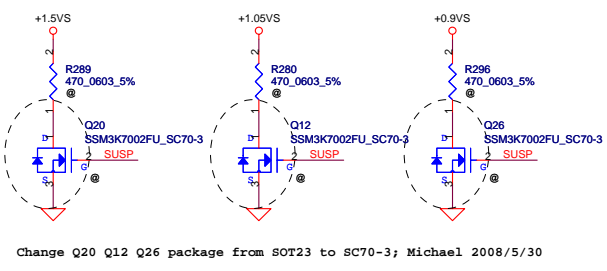
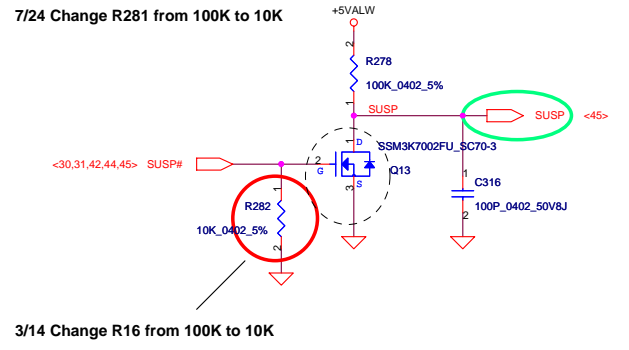
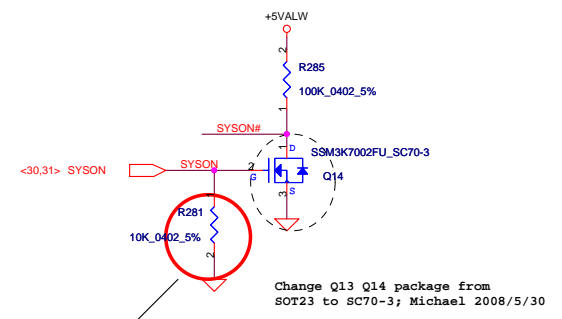
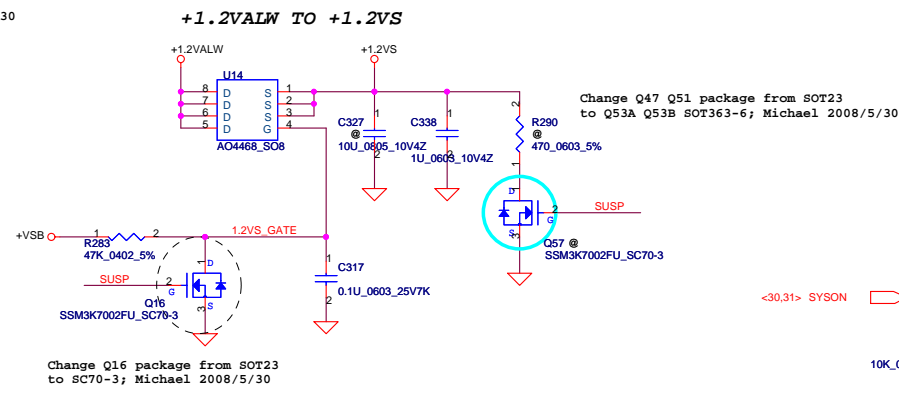
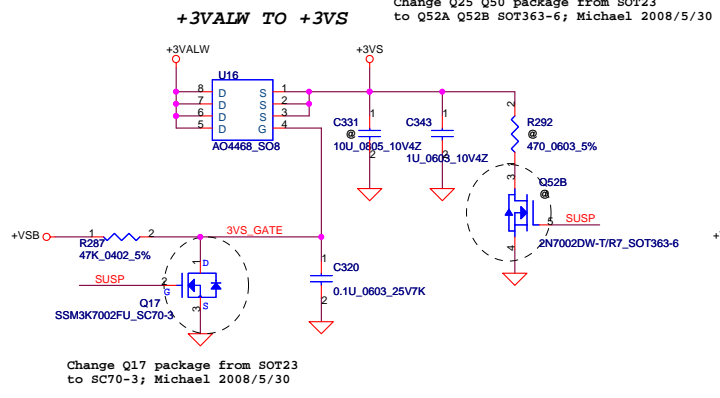
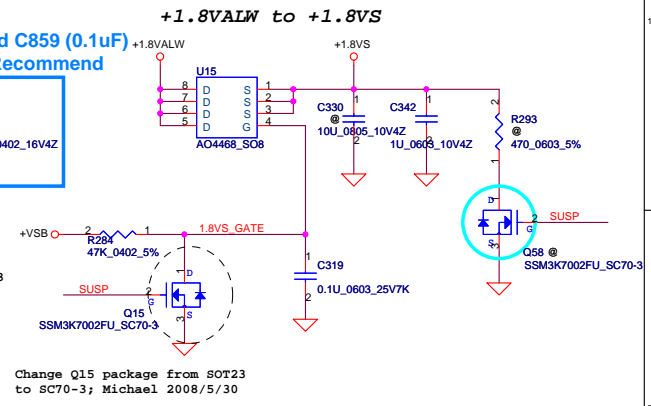
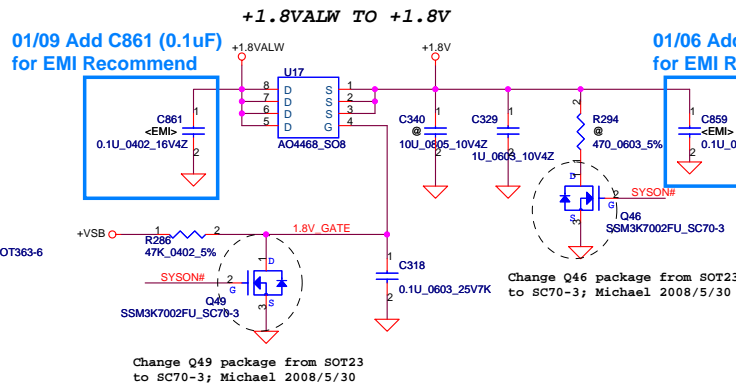
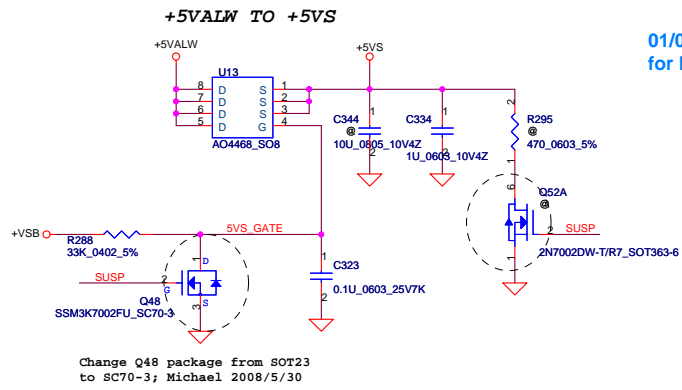
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				MDC/LED/Camera/FP
				Document Number
				KF-T00 M/B LA-4821P Schematic
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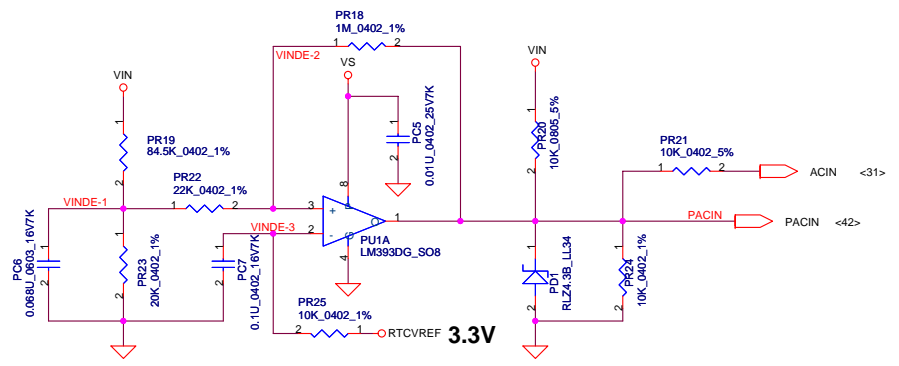
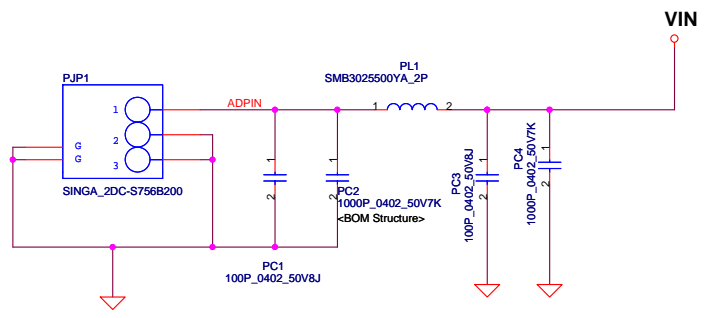


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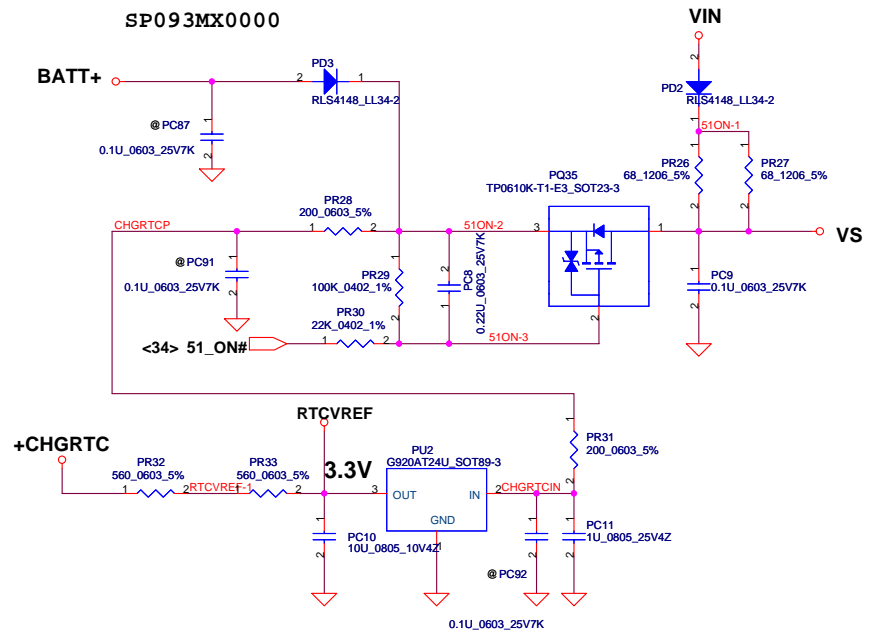
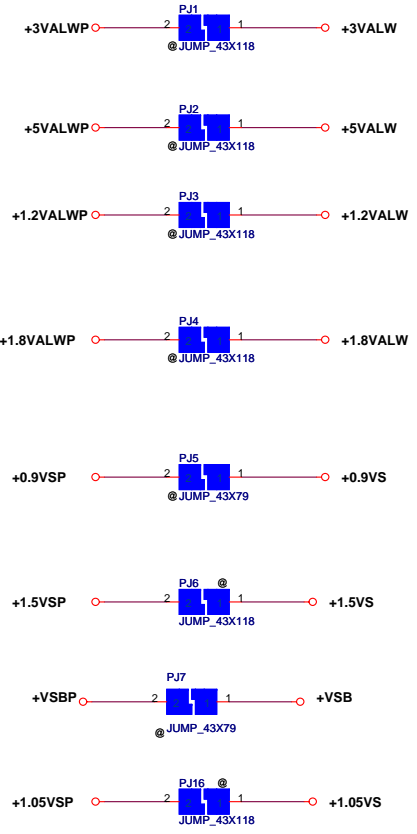


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PACIN PC271 1 2 @ 470P_0402_50V7K

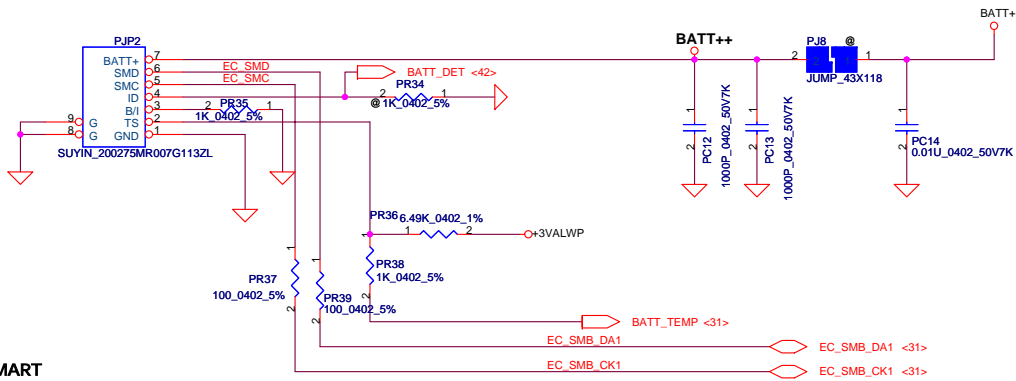


Vin Detector
 High 18.384 17.901 17.430
 Low 17.728 17.257 16.976



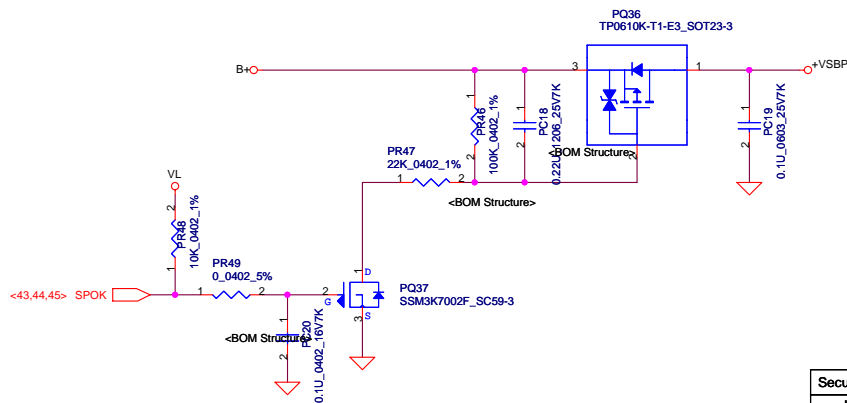
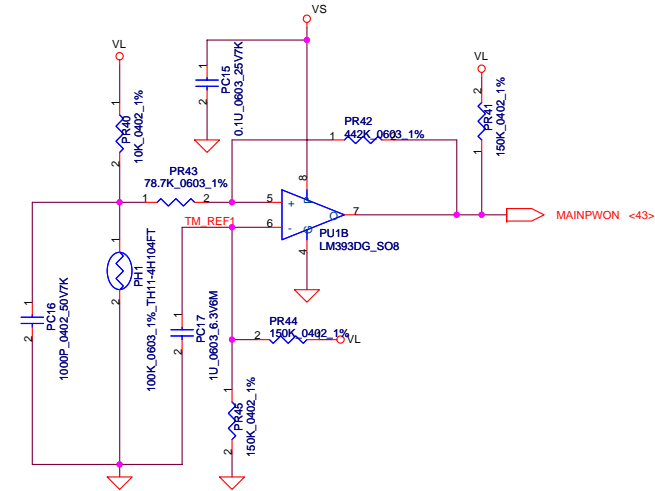
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Size	Document Number	Rev		0.2
Custom	KFT00 MB Schematic			
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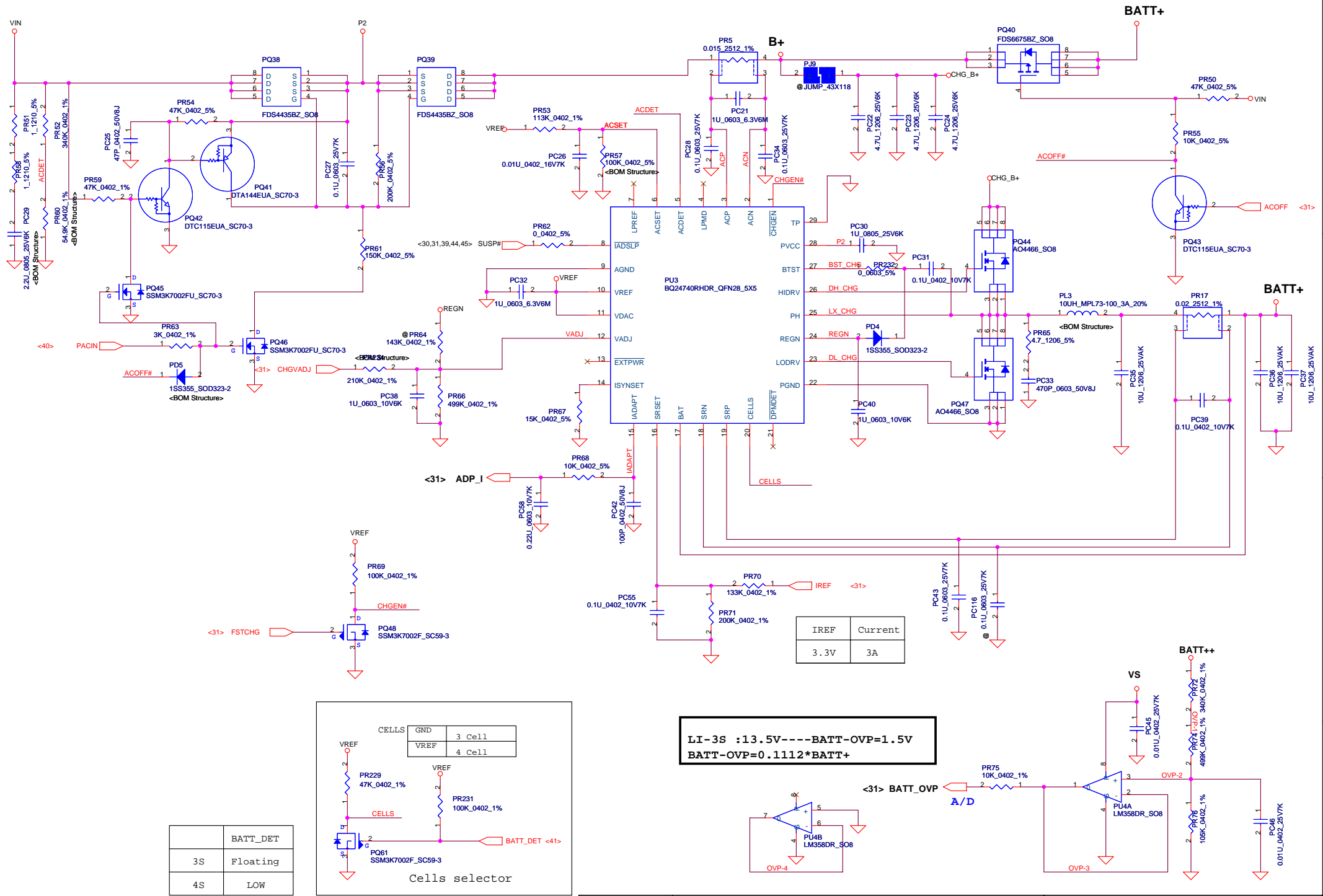
SMART Battery:
 7.BATT+
 6.SMD
 5.SMC
 4.ID
 3.B/I
 2.TS
 1.GND



	BATT_DET
3S	Floating
4S	LOW

PH1 under CPU bottom side :
 CPU thermal protection at 89 degree C
 Recovery at 70 degree C

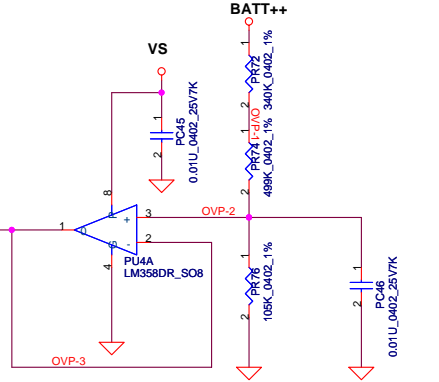
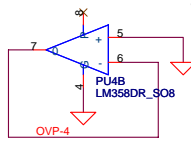
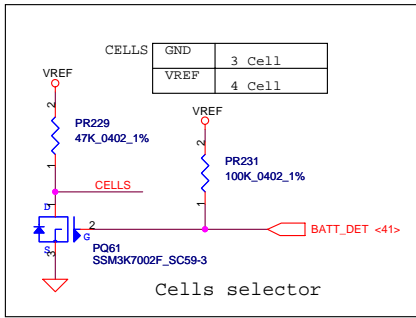


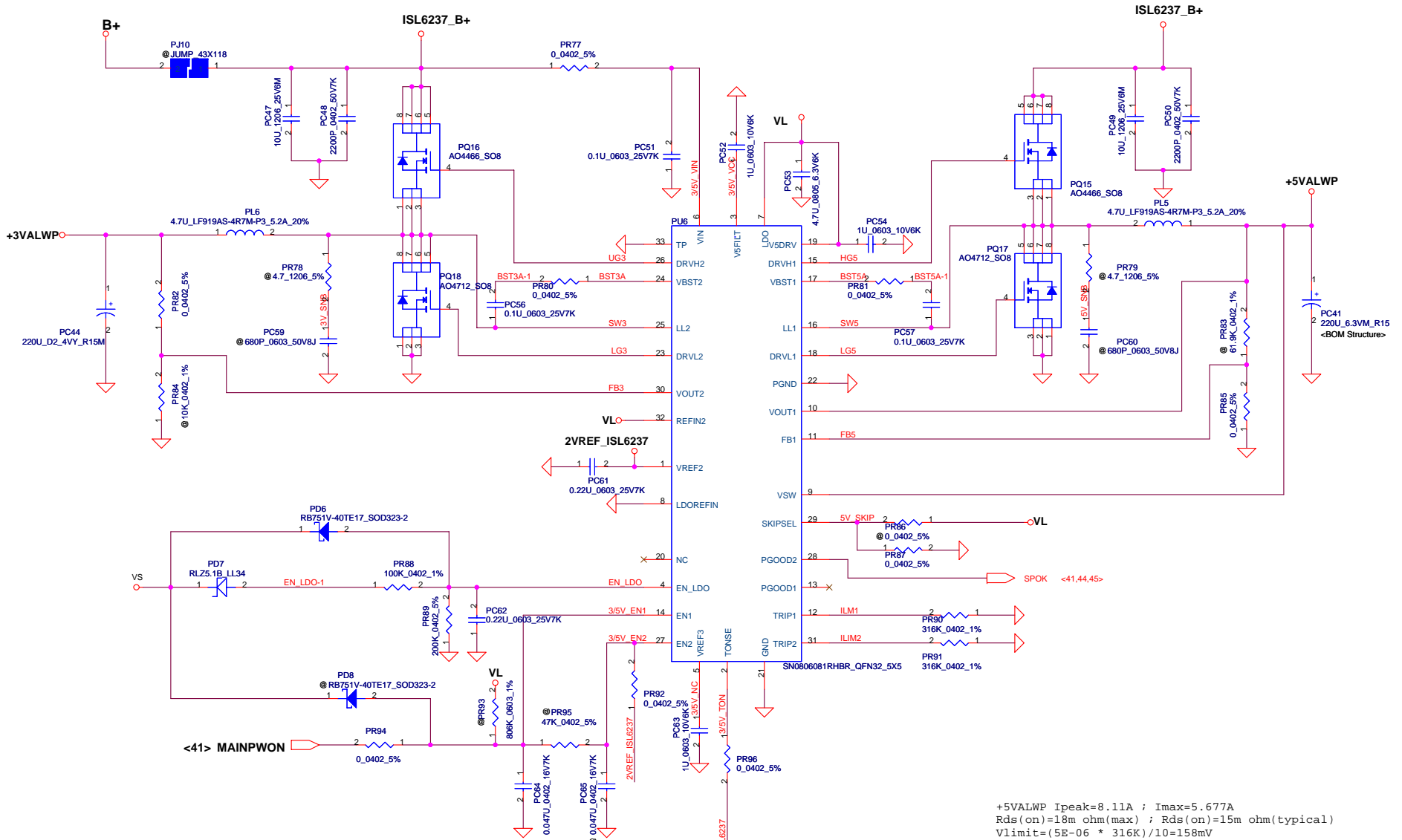


IREF	Current
3.3V	3A

LI-3S :13.5V----BATT-OVP=1.5V
BATT-OVP=0.1112*BATT+

	BATT_DET
3S	Floating
4S	LOW

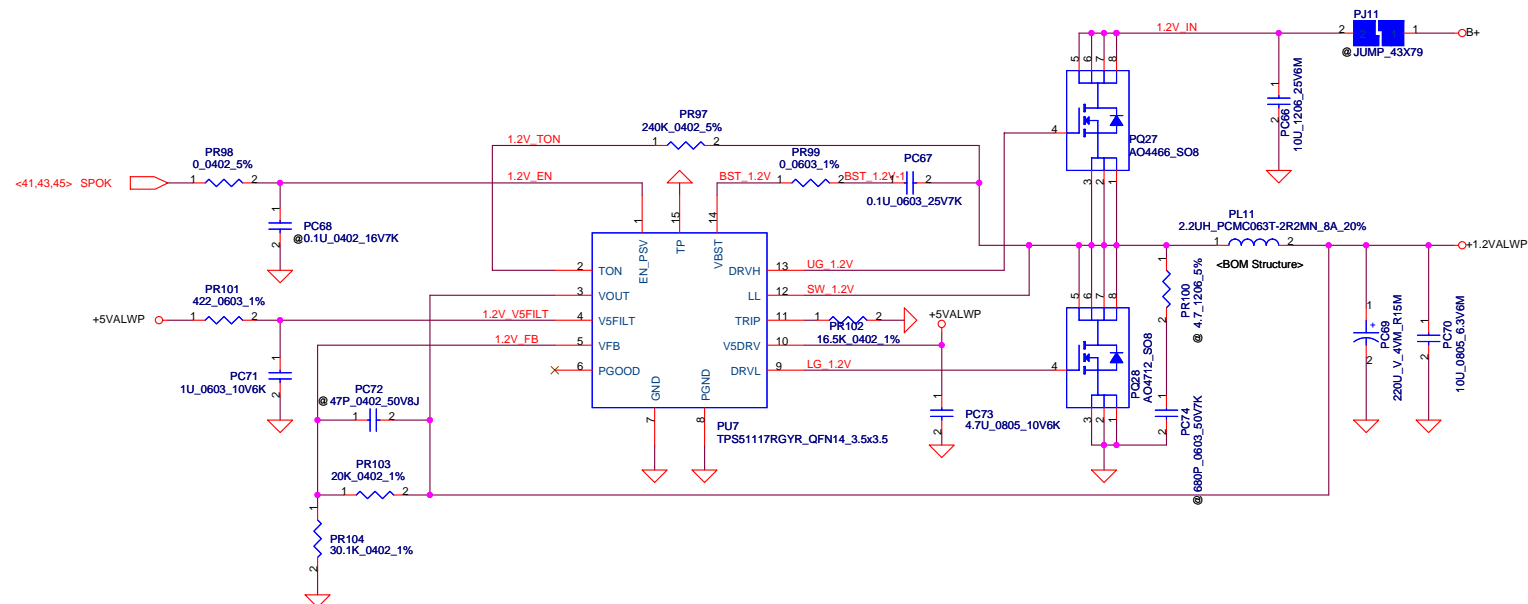




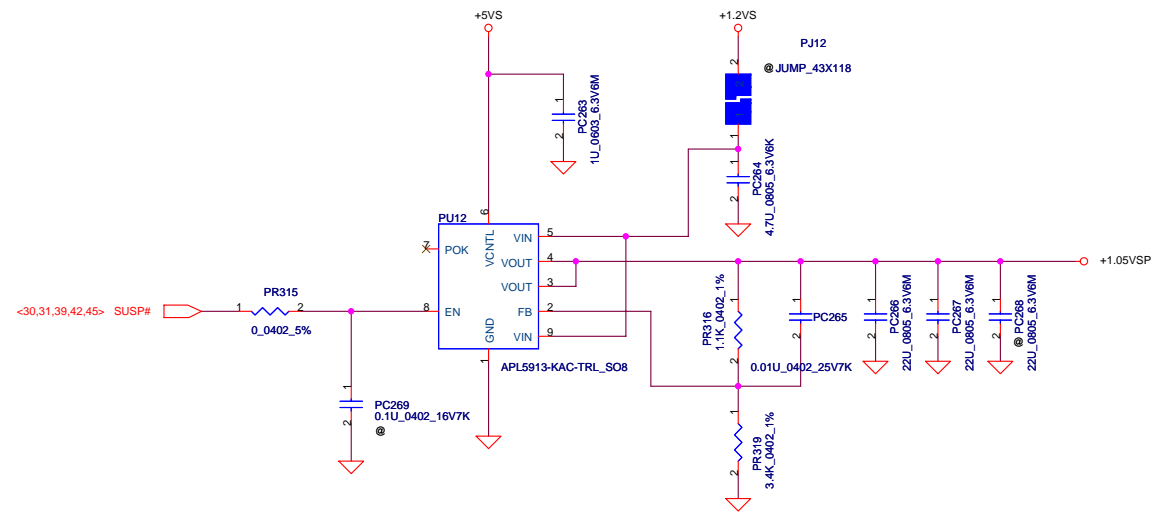
+3VALWP Ipeak=4.85A ; Imax=3.395A
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Vlimit=(5E-06 * 180K)/10=90mV
 Ilimit=90mV/(18m ~ 15m)
 =5A ~ 6A
 Iocp=Ilimit+Delta I/2
 =5.967A ~ 6.967A
 Delta I=1.934A (Freq=300KHz)

+5VALWP Ipeak=8.11A ; Imax=5.677A
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Vlimit=(5E-06 * 316K)/10=158mV
 Ilimit=158mV/(18m ~ 15m)
 =8.77A ~ 10.53A
 Iocp=Ilimit+Delta I/2
 =9.75A ~ 11.51 A
 Delta I=1.956A (Freq=400KHz)

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Issued Date	2008/07/15	Deciphered Date		
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			3	3VALW/5VALW
			1	Rev 02
			1	Sheet 42 of 47

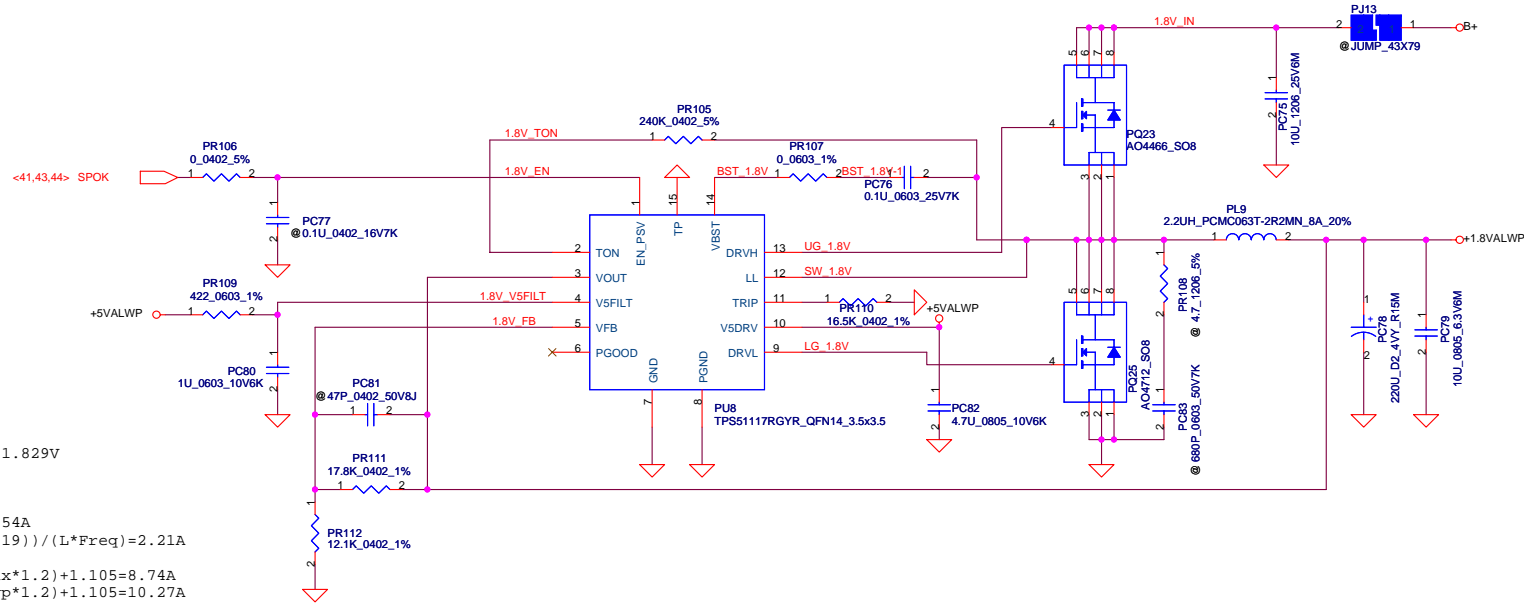


$V_{FB} = 0.75V$
 $V_o = V_{FB} * (1 + PR103 / PR104) = 1.203V$
 $T_{on} = 187.68ns$
 $Freq = 337KHz$
 $C_{esr} = 15m\ ohm$
 $I_{peak} = 7.82A$ $I_{max} = 5.474A$
 $\Delta I = ((19 - 1.2) * (1.2 / 19)) / (L * Freq) = 1.516A$
 $V_{trip} = R_{trip} * 10uA = 165mV$
 $I_{ocp-min} = V_{trip} / (R_{ds(on)max} * 1.2) + 0.758 = 8.4A$
 $I_{ocp-max} = V_{trip} / (R_{ds(on)typ} * 1.2) + 0.758 = 9.92A$
 $I_{ocp} = 8.4A \sim 9.92A$

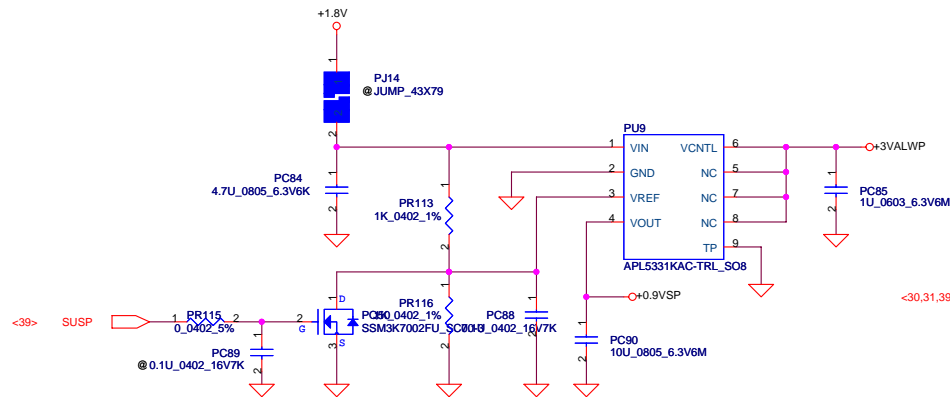


$FB = 0.8V$
 $V_{out} = 0.8v * (1 + R316 / R319)$
 $I_{max} = 3.22A$ $I_{peak} = 4.6A$

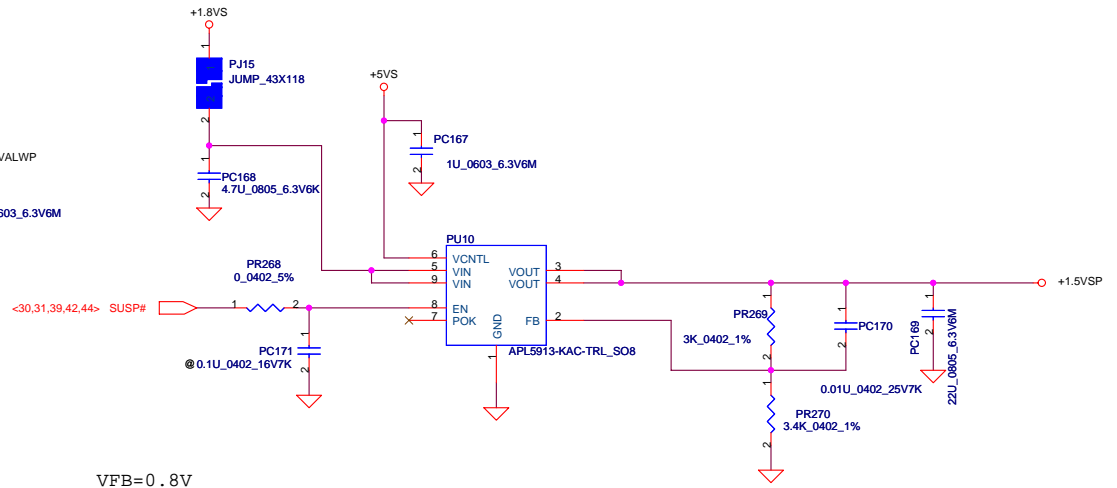
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Issued Date	2008/07/15	Deciphered Date	2009/07/15	Title	
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$V_{FB} = 0.75V$
 $V_o = V_{FB} * (1 + PR111 / PR112) = 1.829V$
 $Freq = 334KHz$
 $Cesr = \text{ohm}$
 $I_{peak} = 12.22 A$ $I_{max} = 8.554A$
 $\Delta I = ((19 - 1.8) * (1.8 / 19)) / (L * Freq) = 2.21A$
 $V_{trip} = R_{trip} * I_{max} = 165mV$
 $I_{ocp-min} = V_{trip} / (R_{dsonmax} * 1.2) + 1.105 = 8.74A$
 $I_{ocp-max} = V_{trip} / (R_{dson typ} * 1.2) + 1.105 = 10.27A$
 $I_{ocp} = 8.74A - 10.27A$



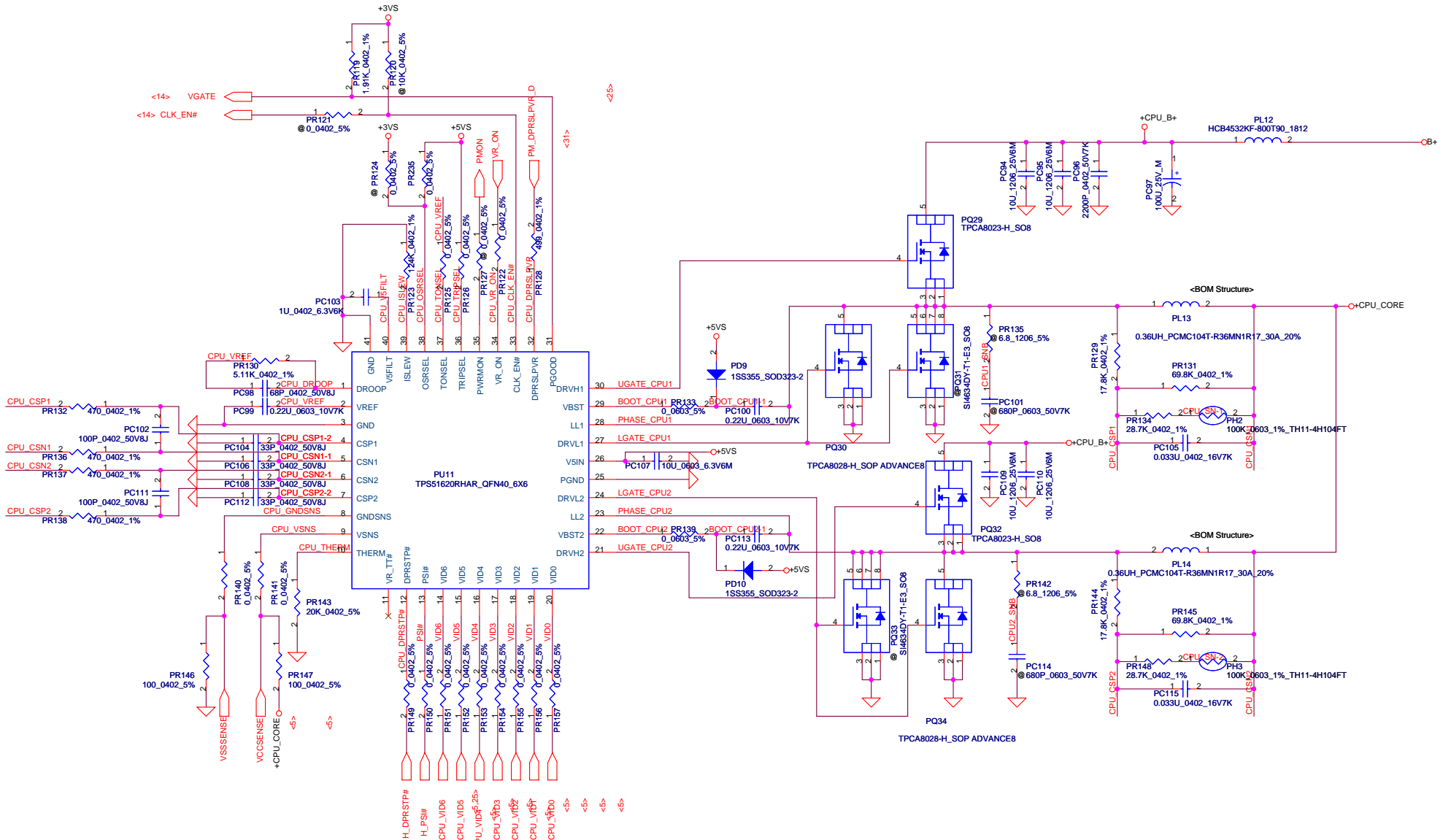
$V_{out} = V_{in} * R116 / (R113 + R116) = 0.925$
 $I_{max} = 1.4A$ $I_{peak} = 2A$



$V_{FB} = 0.8V$
 $I_{max} = 0.966A$ $I_{peak} = 1.38A$

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H_DPRSTP# PC270 1 2 470P_0402_50V7K



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Custom	Document Number	KFT00 MB Schematic		0.2	
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Change charge current to 3.36A at Iref=3.3V	A	3	change PR70 from 133K to 97.6K		
2		change charger current sense size and value	A	3	change PR17 from 15m to 20m ohm		
3		Set charger voltage	A	3	Delet PR64		
4		change PQ38 ,PQ39 for EOL	A	3	Change to FDS4435BZ		
5		change PR90 ,PR91 for 3V,5V ocp set	A	4	Change from 301K to 315K and 174K		
6		change PR102 for 1.2V OCP set	A	5	Change from 14.7K to 16.5K		
7		change 1.2v from 1.225V to 1.2V follow KSWXX	A	5	Change PR103 and PR104 to 18.2K and 30.1K		
8		change PR110 for 1.8V OCP set	A	6	Change from 14.7K to 16.5K		
9		change 1.8v from 1.851V to 1.829V follow KSWXX	A	6	Change PR111 and PR112 to 17.4K and 12.1K		
10		change chgvadj risister match ec parameter	A	3	Change PR66 100K to 499K		
11		change PL13,PL14 for cost	A	7	Change PL13 PL14 to Toho		
12		modify CP point to 3.13A	A	3	change PR53 from 0 to 113K ohm		
13		change charger current to 3A	C		change PR70 from 97.6K to 133K ohm		
14		change 3V OCP	C		change PR91 from 180K to 316K ohm		
15		adjust cpu load line	C		change PR130 from 4.02K to 5.49 K ohm		
16		change cpu choke footprint	C		change choke footprint from toho to cyntec		
17		change PR229 from 100k to 47k			adjust cell pin voltage		
18		adjust back to back mos turn off time			change PC27 from 0.47U to 0.1U		
19		Adjust 1.2v voltage from 1.2035V to 1.2483V for hw request			change PR103 from 18.2k to 20k		
20		Adjust 1.8v voltage from 1.8285V to 1.8533V for hw request			change PR111 from 17.4k to 17.8k		
21		adjust cpu load line			change PR130 from 5.49k to 5.11k		
22		NPO must use J tolerance			change PC104 PC106 PC108 PC112 from K to J tolerance		
23							