

ZQ2B SOLE UMA SYSTEM DIAGRAM



BOM P/N	Description	Model	SidePort	ODD
31ZQ2MB00A0	ZQ2B 6L JM MB (W/GRN,SAM,W/O CPU)ASSY	JM	Samsung	Slim
31ZQ2MB00E0	ZQ2B 6L JM MB (W/GRN,HYU,W/O CPU)ASSY	JM	Hynix	Slim
31ZQ2MB00H0	ZQ2B 6L JV MB (W/GRN,W/O CPU,VRAM)ASSY	JV	No Support	Standard

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

IV@ ----> iGPU
 SP@ ----> Option Notice
 SIDE@ ----> SidePort VRAM
 GA@ ----> Green Adapter (Default stuff)

Sideport-L75,L76,R583,R392,C832,R455,R550,R502
 NB A11-R105,R108
 SB A12-R267,R271
 JV/JM-CN16,R450,R456
 EC-D8,D27
 UMA-R461
 VRAM-R358,R359,R360,R363,R365,R72

CHARGER (ISL88731A) PAGE 26

AMD CPU CORE (ISL6265) PAGE 28 *CPU*

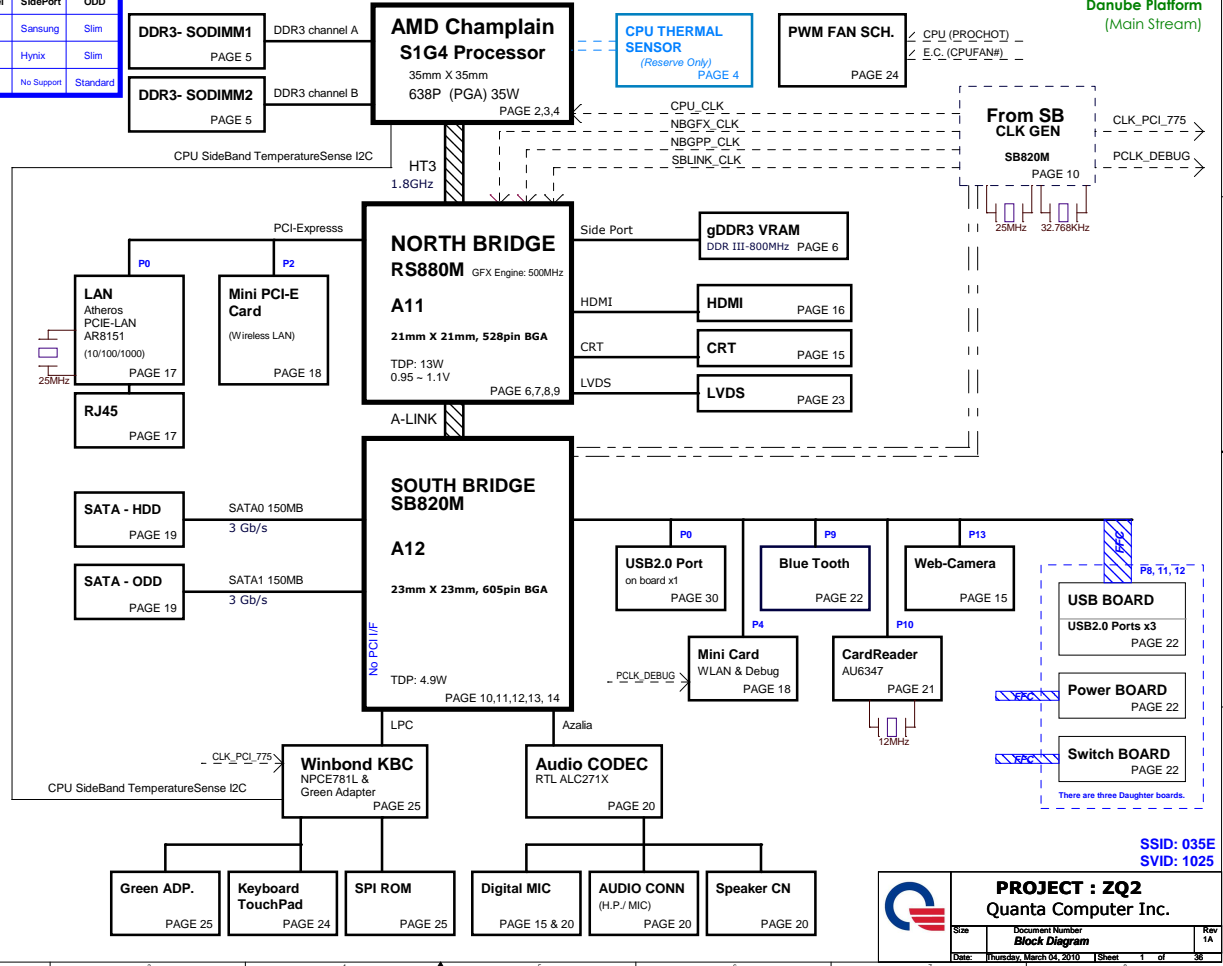
NB_CORE (UP6111AQDD) PAGE 30 *NB*

0.9V/DDR 1.5V (RT8207) PAGE 31

SYSTEM 5V/3V (RT8206) PAGE 27

1.1V (UP6111AQDD) PAGE 29

Discharge /Thermal protec PAGE 32



From SB CLK GEN PAGE 10

CLK_PCL_775
 PCLK_DEBUG

25MHz
 32.768KHz

USB BOARD PAGE 22

USB2.0 Ports x3

Power BOARD PAGE 22

Switch BOARD PAGE 22

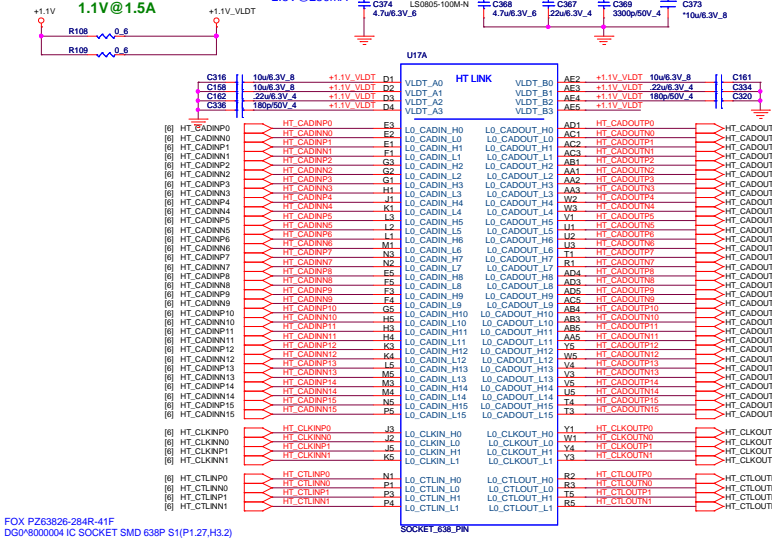
There are three Daughter boards.

SSID: 035E
 SVID: 1025

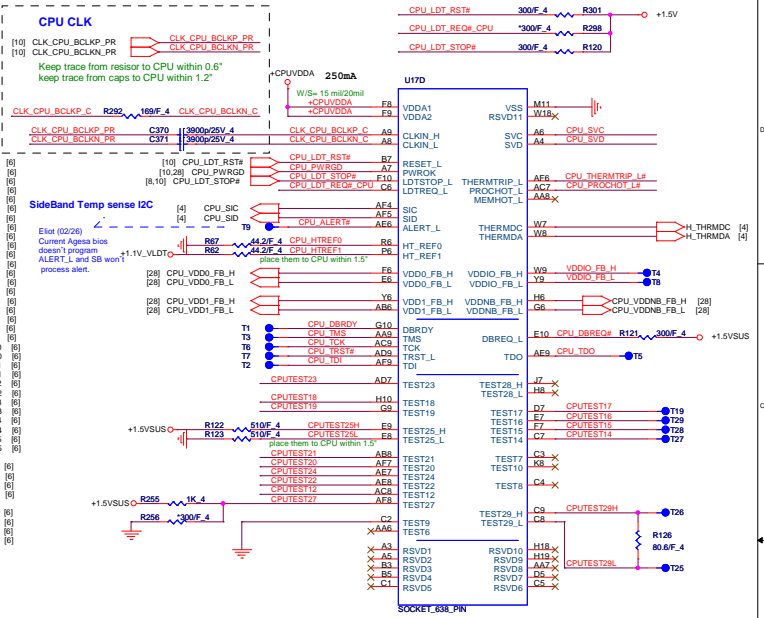
PROJECT : ZQ2
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Documet Number: Block Diagram
 Date: Thursday, March 04, 2010 | Sheet 1 of 86

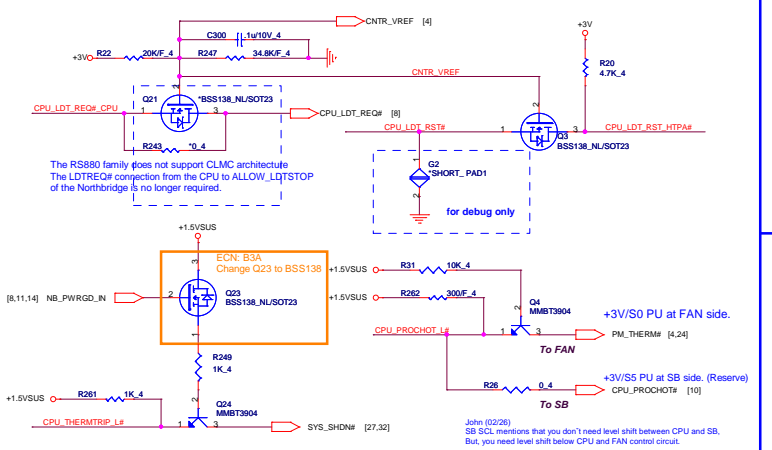
S1G4 (CPU)



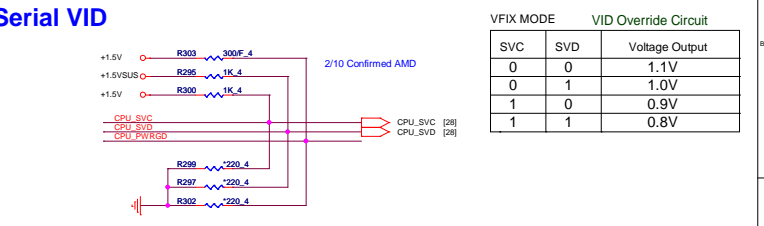
FOX PZ63826-284R-41F
 DGP#8000004 IC SOCKET SMD 638P S1(P1,27,H3,2)
 MLX 47296-4131
 DGP#8000003 IC SOCKET SMD 638P S1(P1,27,H3,2)
 TVC 4-11903491-2
 DGP#8000005 IC SOCKET SMD 638P S1(P1,27,H3,2)



SOCKET_638_P1N

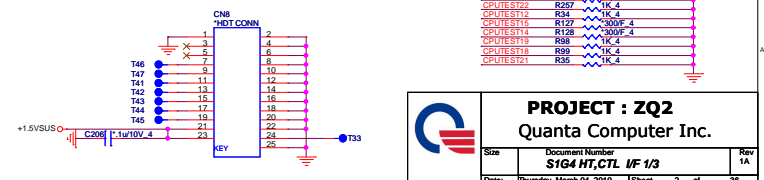


John (02/26)
 SB SCL mentions that you don't need level shift between CPU and SB.
 But you need level shift below CPU and FAN control circuit.



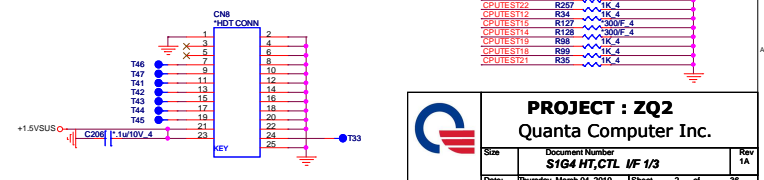
SOCKET_638_P1N

Serial VID



VFX MODE		VID Override Circuit	
SVC	SVD	Voltage Output	
0	0	1.1V	
0	1	1.0V	
1	0	0.9V	
1	1	0.8V	

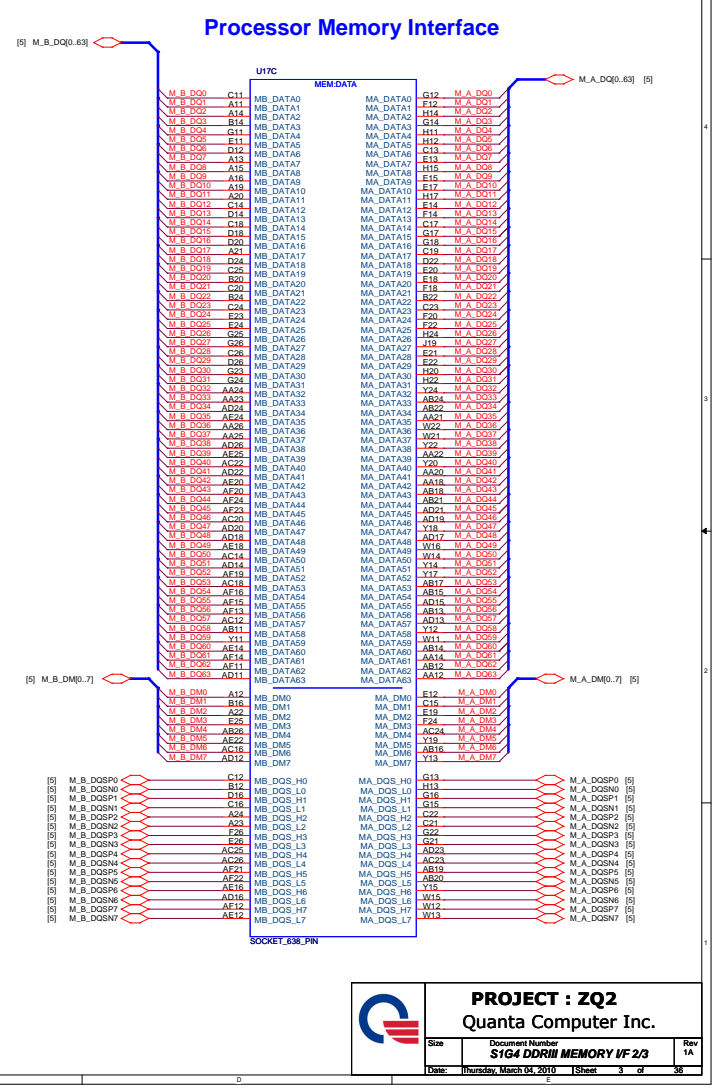
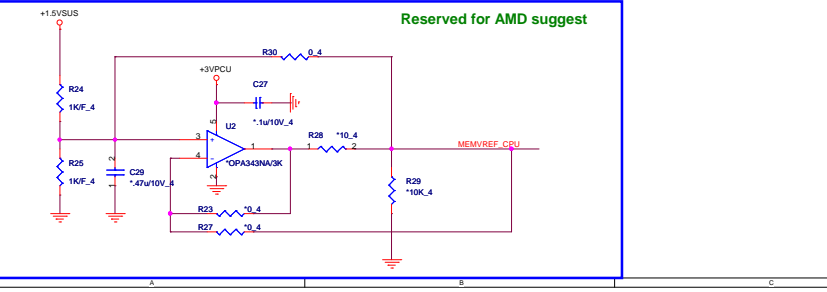
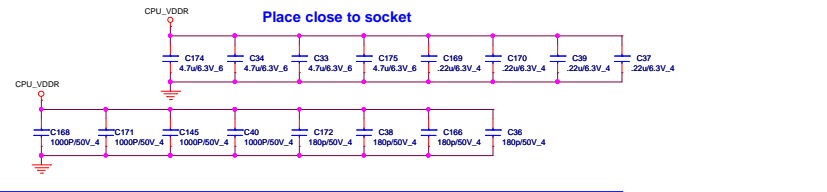
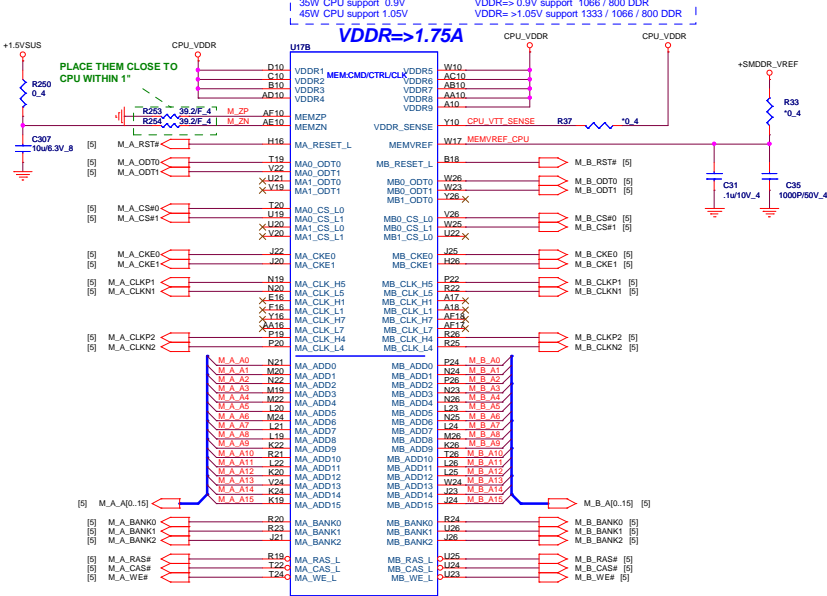
HDT Connector



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Size: _____ Document Number: **S1G4 HT_CTL IF 1/3** Rev: 1A

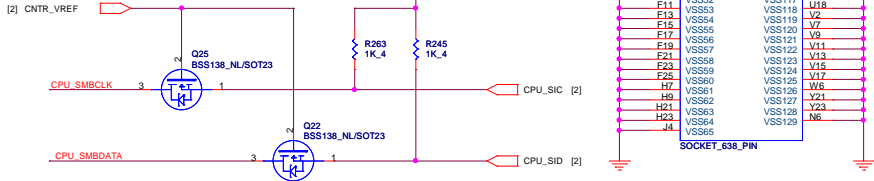
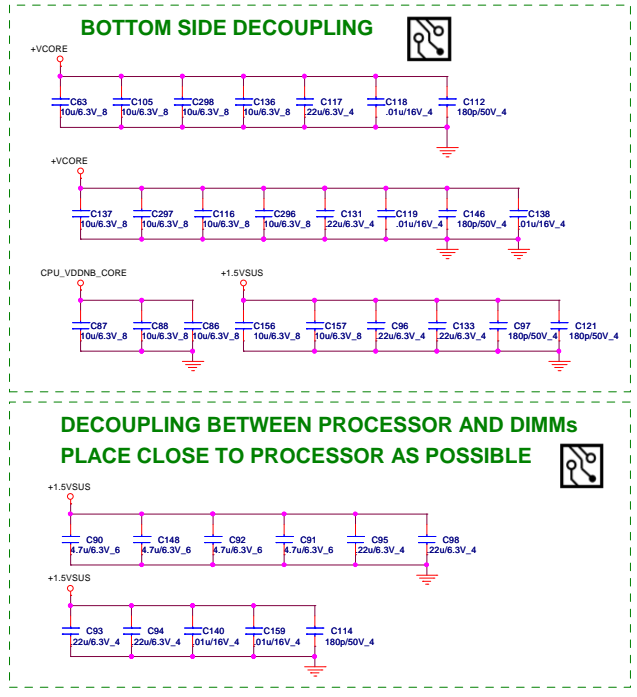
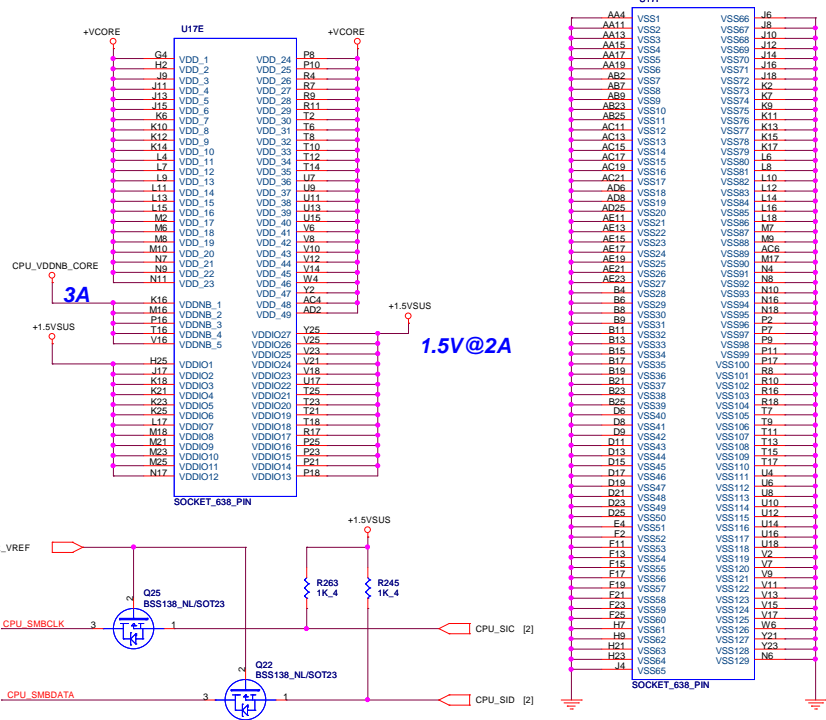
Date: Thursday, March 04, 2010 Sheet: 2 of 38



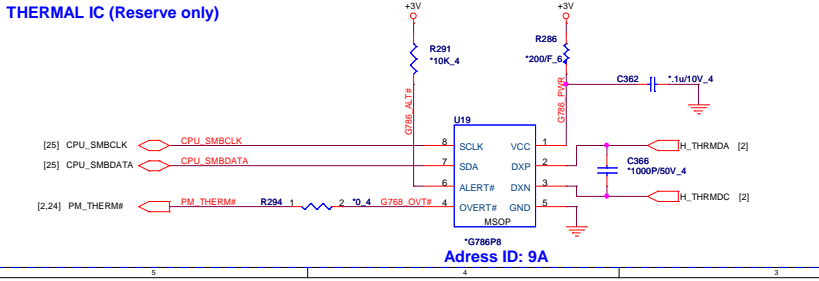
PROJECT : ZQ2
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Size Document Number **31G4 DDR4M MEMORY I/F 2/3** Rev **1A**

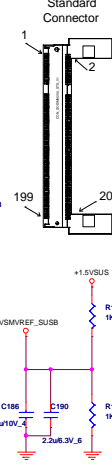
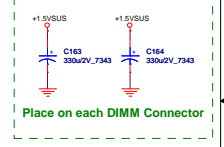
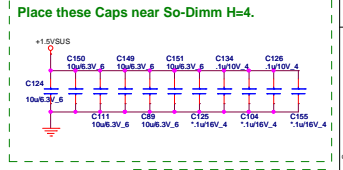
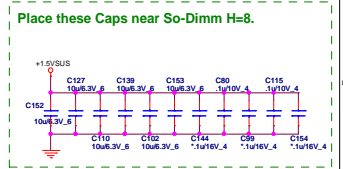
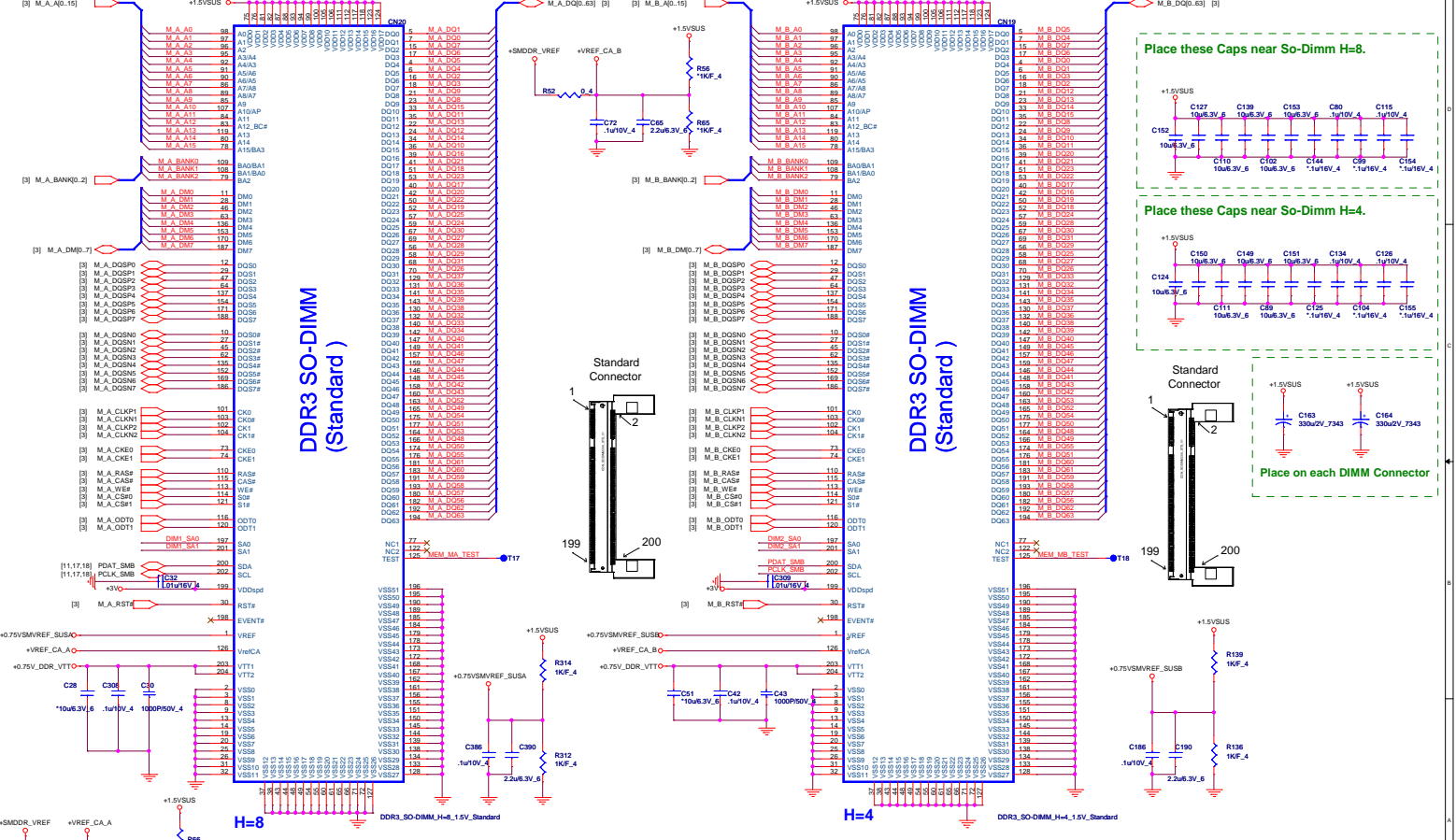
Date: Thursday, March 04, 2010 13:00 Sheet **3** of **36**



PROCESSOR POWER AND GROUND



PROJECT : ZQ2		
Quanta Computer Inc.		
Size	Document Number	Rev
	S1G4 PWR & GND 3/3	1A
Date:	Thursday, March 04, 2010	Sheet 4 of 36

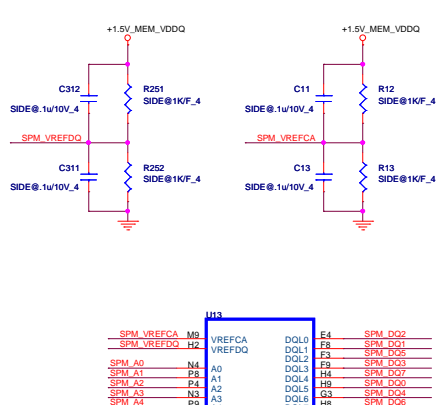


PROJECT : ZQ2
Quanta Computer Inc.

Doc: _____ Document Number: **DDR2 SODIMMS: A/B CHANNEL** Rev: **1A**

Date: **Thursday, March 04, 2010 13:58:54** of **38**

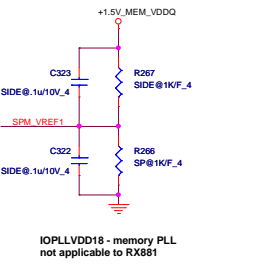
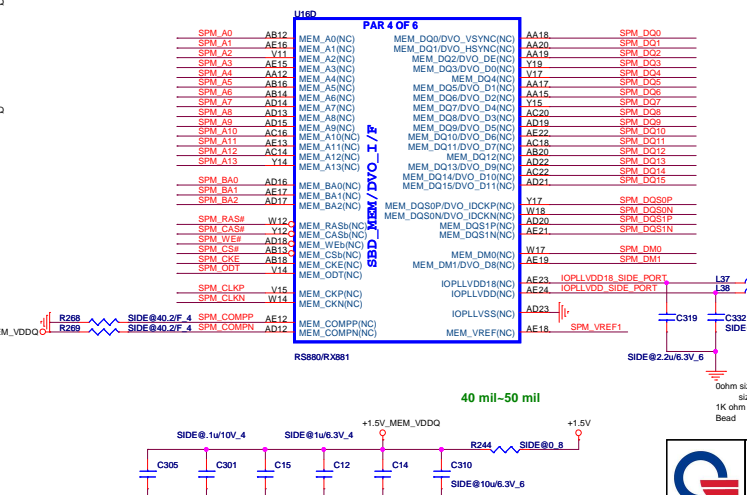
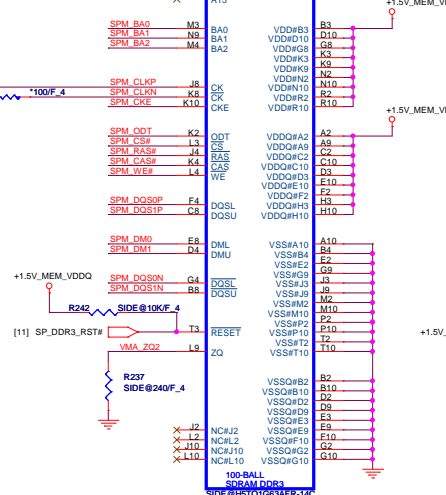
SIDE PORT



Signals	RS880	RX880
HT_TXCALP	Ra 301 ohm 1%	Ra 1.21k ohm 1%
HT_RXCALP	Rb 301 ohm 1%	Rb 1.21k ohm 1%

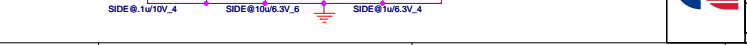
RES CHIP 1.21K 1/16W +1%(0402)
P/N : CS21212FB18

This block is for Side-Port only



IOPLLVD18 - memory PLL
not applicable to RX881

	W/I SP	W/O SP
R266	1K	0
L37	Bead	0
L38	Bead	0

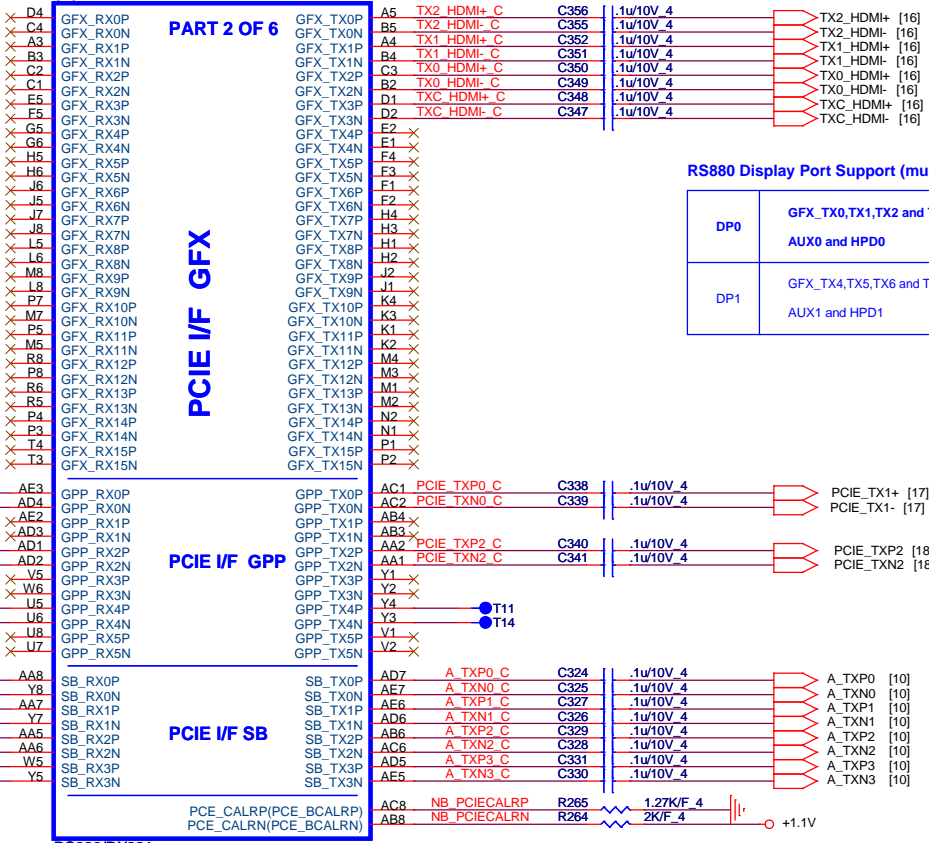


PROJECT : ZQ2
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Size	Document Number	Rev
	RS880-HT LINK I/F-1/4	1A
Date:	Thursday, March 04, 2010	Sheet 6 of 36

U16B

PART 2 OF 6



PCIE I/F GFX

PCIE I/F GPP

PCIE I/F SB

RS880 Display Port Support (muxed on GFX)

DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1

LAN
WLAN

SB

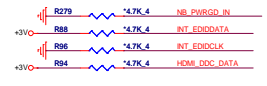


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Size	Document Number	Rev
	RS880M-PCIE I/F 2/4	1A
Date:	Thursday, March 04, 2010	Sheet 7 of 36

All RS880 variants do not support analog TV-out functionality. As such, Y, C, Pr, and COMP_Pb

For Check list JTAG



For A11 version

(02/10) Don't need 49.9 ohm PD.



STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.



RS880M: Enables Side port memory

RS880M:INT_CRT_HSYNCP

Selects if Memory SIDE PORT is available or not

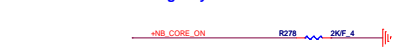
1 = Memory Side port Not available

0 = Memory Side port available

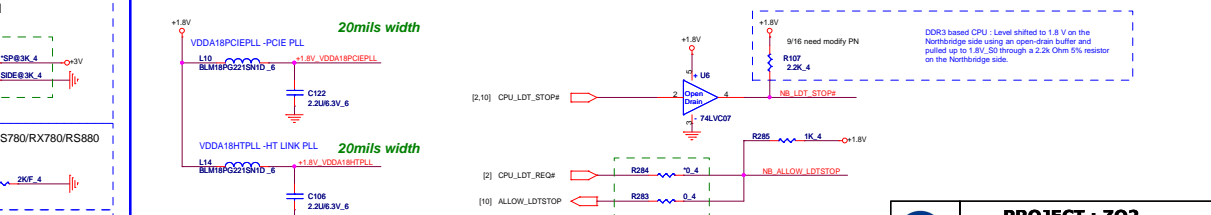
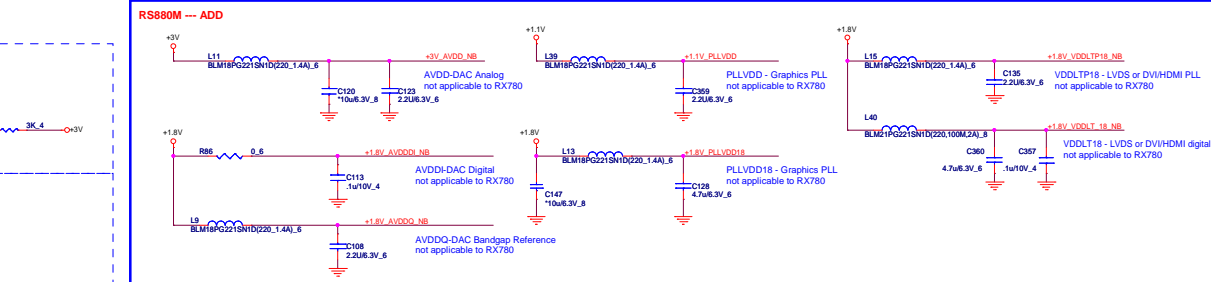
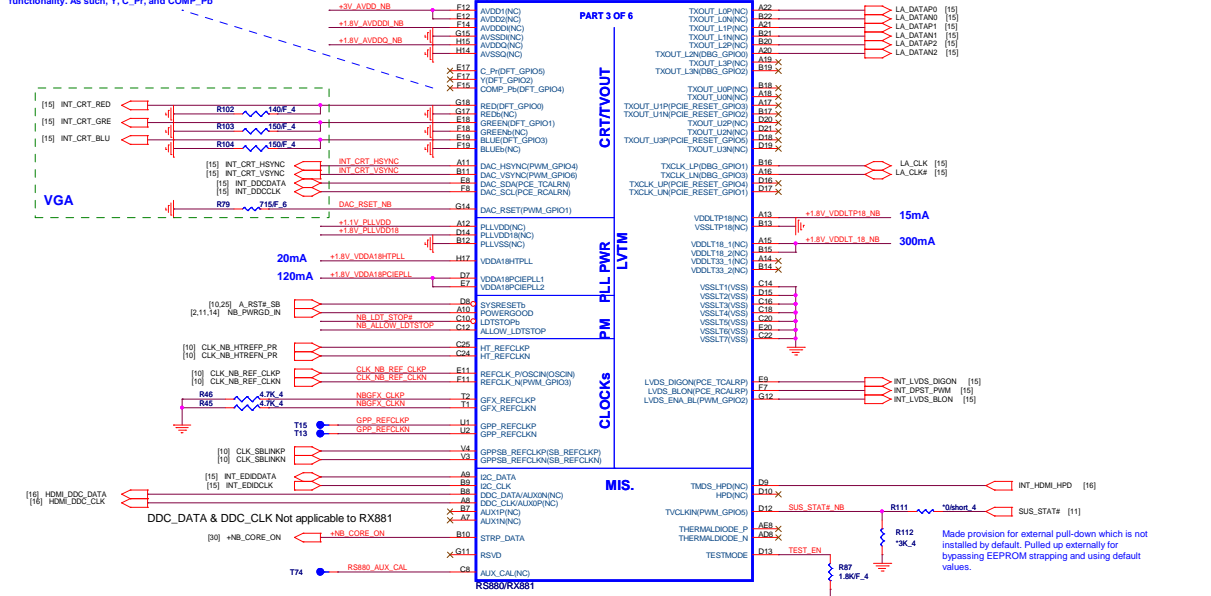
Register Readback of strap: NB_CLKCFG.CLK_TOP_SPARE_D[1]



For extrnal EEPROM Debug only



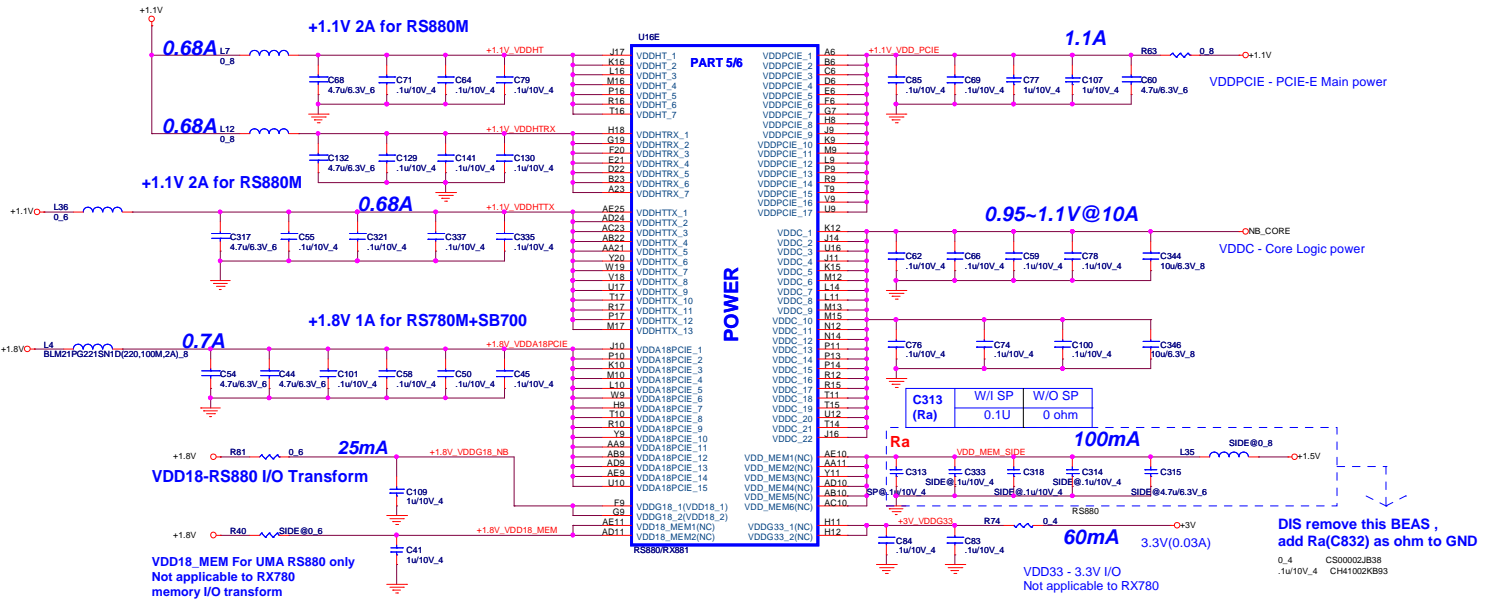
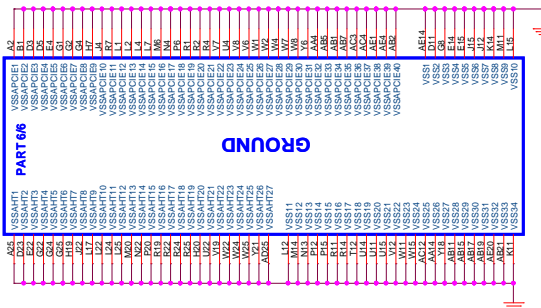
Display Port interface from PCIeGraphics (RS880/rs880M only)



The RS880 family does not support CLMC architecture. The LDTREQ# connection from the CPU to ALLOW_LDTSTOP of the Northbridge is no longer required.

PROJECT : ZQ2
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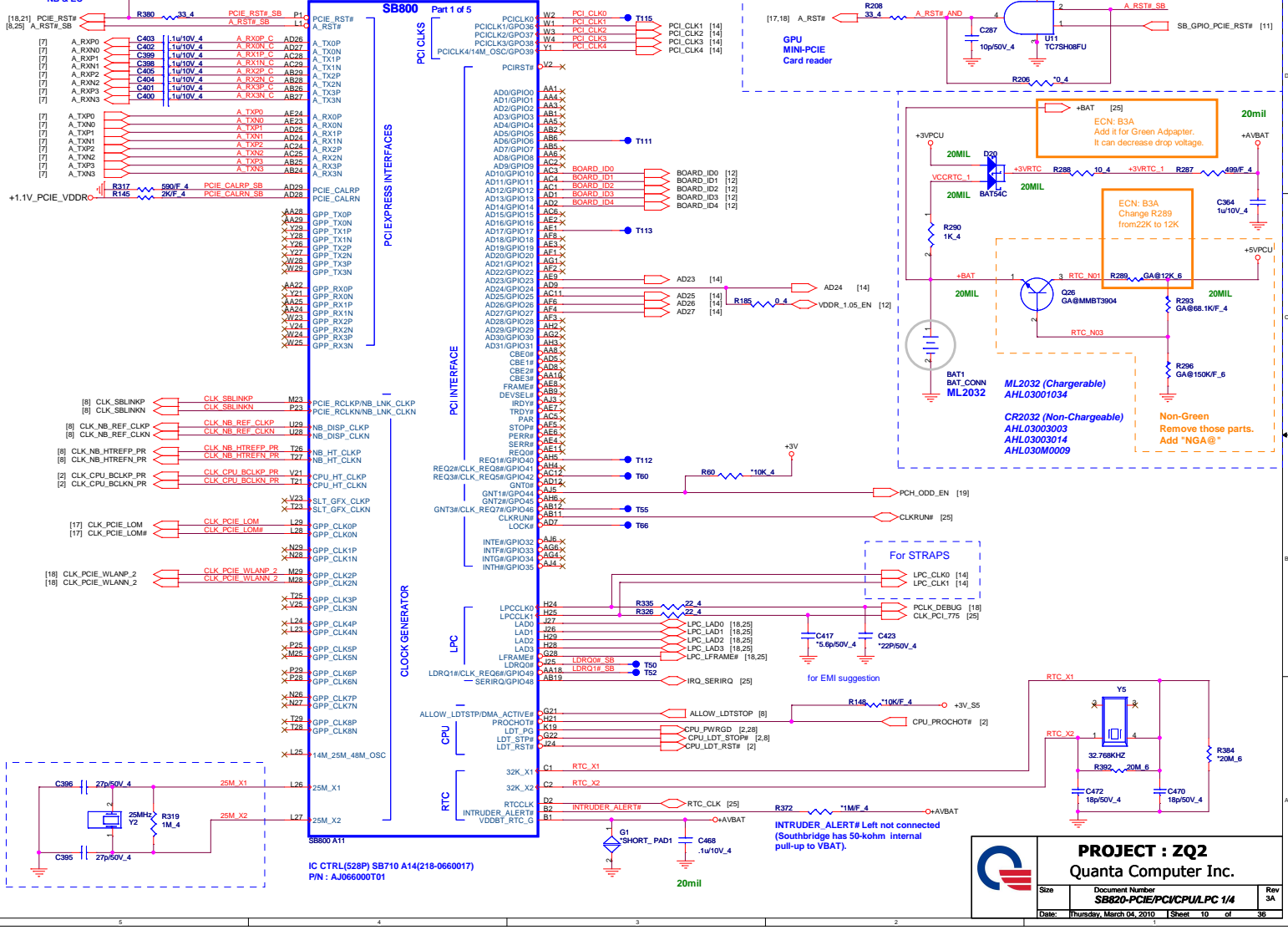
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PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number RS880M-POWER4/4	Rev 1A
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PLACE CAPS VERY CLOSE TO BALL OF SB800M



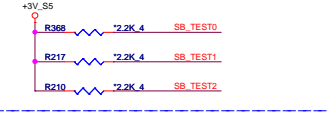
For AMD RST

For STRAPS

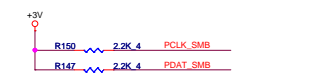
INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).

PROJECT : ZQ2 Quanta Computer Inc.		
Size	Document Number	Rev
	SB820-PCIE/PC/CPU/LPC 1/4	3A
Date:	Thursday, March 04, 2010	Sheet 10 of 36

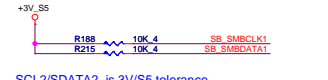
NC only ,Can't be install



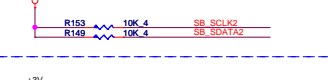
SCL0/SDATA0 is 3V tolerance. AMD datasheet define it
Clk Gen/ Robson/TV tuner/ DDR2/ Thermal/ Accelerometer



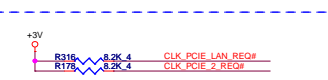
SCL1/SDATA1 is 3V/S5 tolerance. AMD datasheet define it



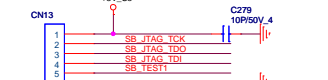
SCL2/SDATA2 is 3V/S5 tolerance. AMD datasheet define it



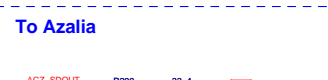
SUS_STAT#



Current Agessa bios doesn't program ALERT_L and SB won't process alert.



JTAG DEBUG

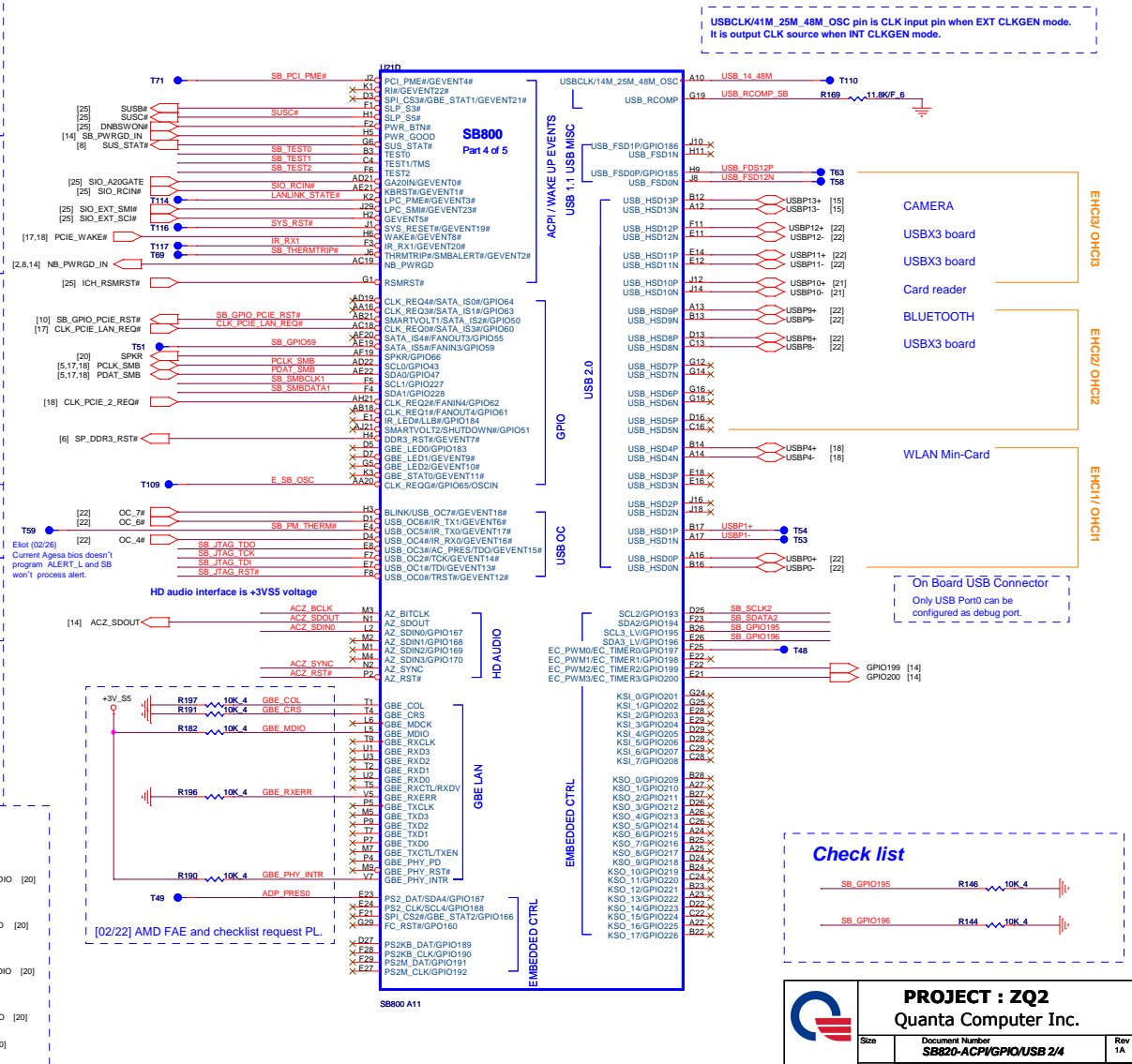


*SW JTAG DEBUG

To Azalia

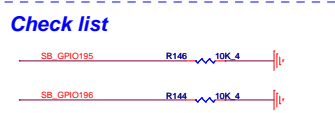


USBCLK14M_25M_48M_OSC pin is CLK input pin when EXT_CLKGEN mode. It is output CLK source when INT_CLKGEN mode.



- CAMERA
- USBX3 board
- USBX3 board
- Card reader
- BLUETOOTH
- USBX3 board
- WLAN Min-Card

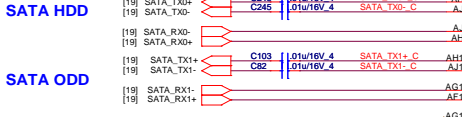
On Board USB Connector
Only USB Port0 can be configured as debug port.



PROJECT : ZQ2
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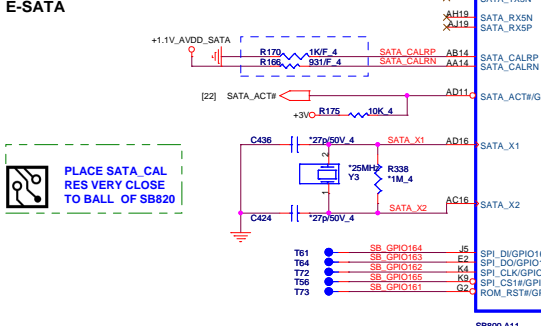
Size	Document Number	Rev
	SB820-ACP/GPIO/USB 2/4	1A
Date:	Thursday, March 04, 2010	Sheet 11 of 36

Max trace length: 6"

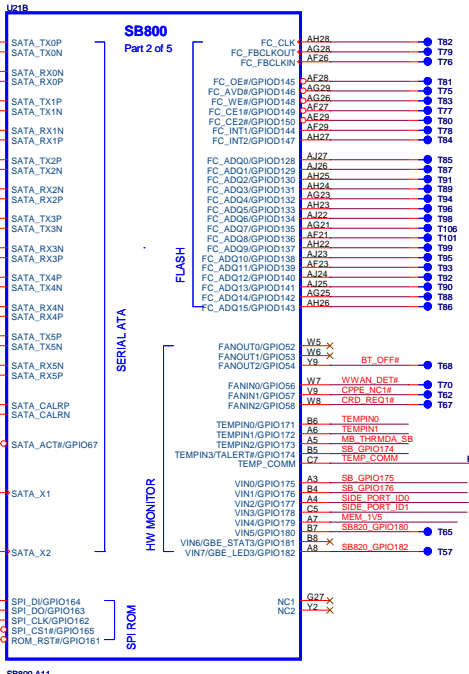


SATA PORT 0,1,2,3 can support AHCI mode

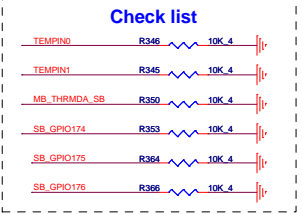
Signal Name	Explanation
SATA_CALRP	SB800 A11: 800 ohm 1% resistor to GND. SB800 A12: 1K ohm 1% resistor to GND.
SATA_CALRN	SB800 A11: 931 ohm 1% resistor to VDDAN_11 SATA. SB800 A12: 931 ohm 1% resistor to VDDAN_11 SATA.



PLACE SATA CAL RES VERY CLOSE TO BALL OF SB820

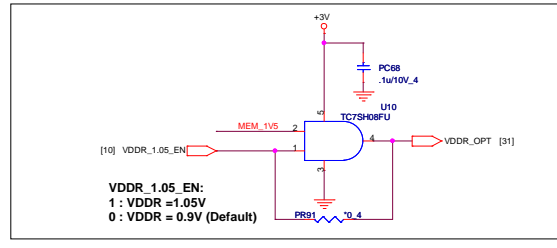
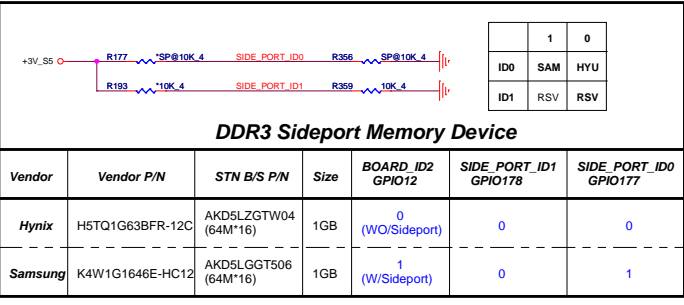
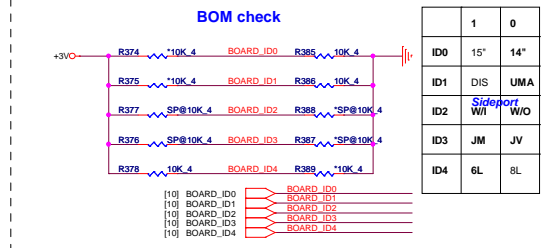


IF THERE IS NO IDE TEST POINTS FOR DEBUG BUS IS MANDATORY



IF THERE IS NO IDE TEST POINTS FOR DEBUG BUS IS MANDATORY

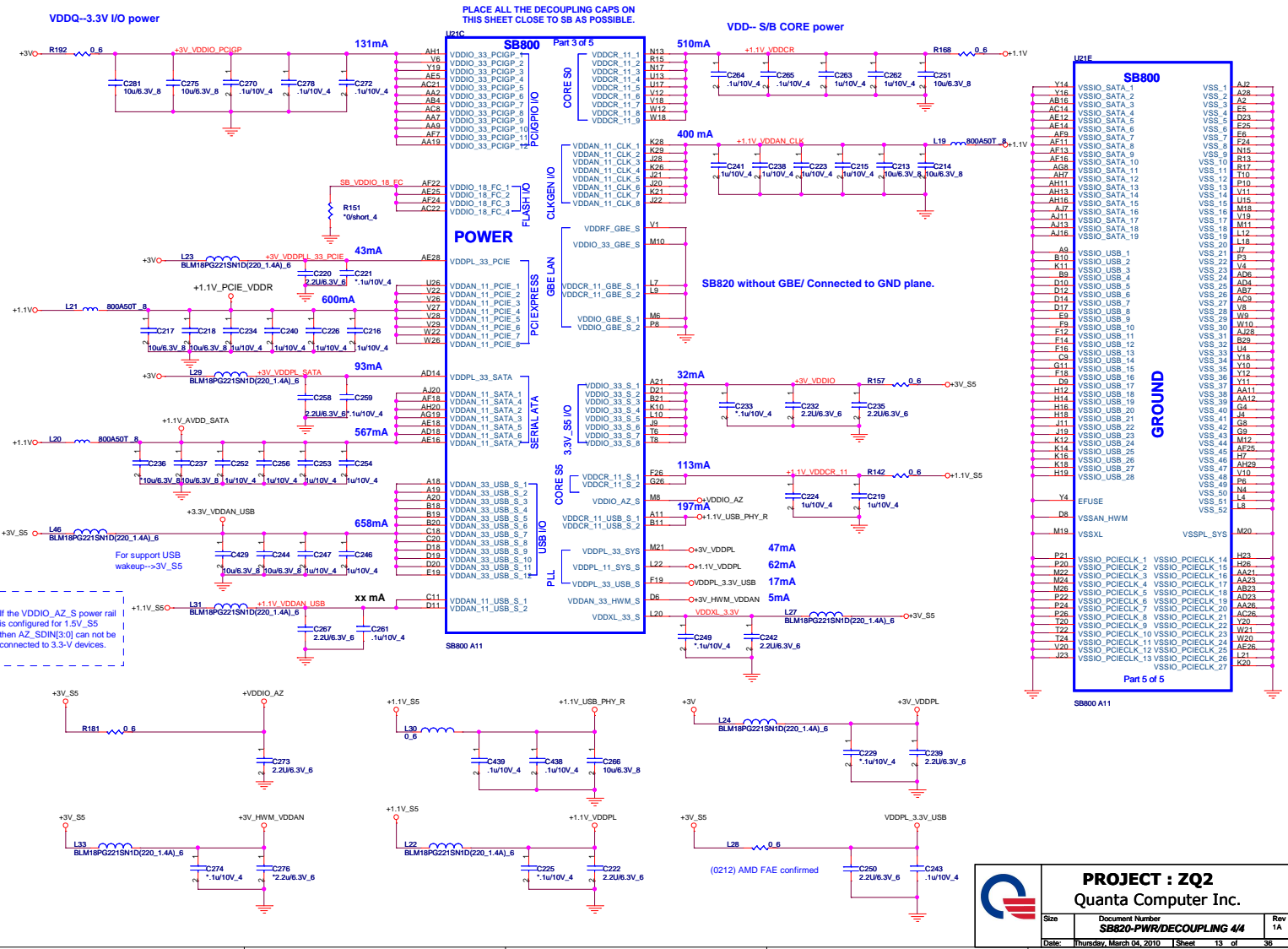
R178 *0short_4



PROJECT : ZQ2
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Size	Document Number	Rev
	SB820-SATA/IDE/SPI 3/4	1A

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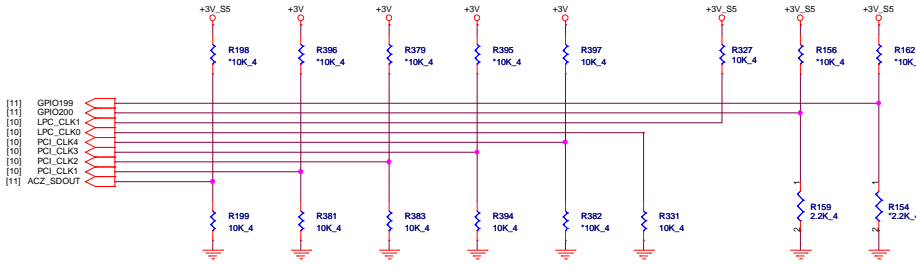
REQUIRED STRAPS



OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

SB820M is supported Gen.1 mode only.

For internal clock GEN.

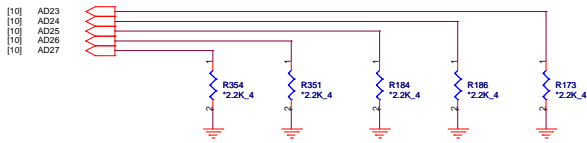


	AZ_SDOOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED	H, H=Reserved H, L=SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1 DEFAULT	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L, H=LPC ROM L, L=FWH ROM	DEFAULT

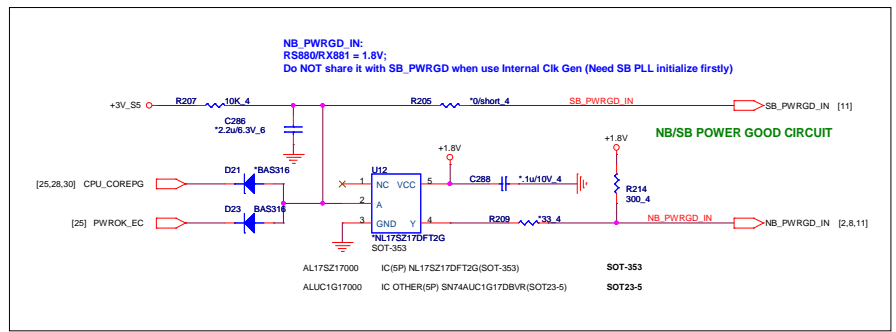
internal have pull H1 10K

DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



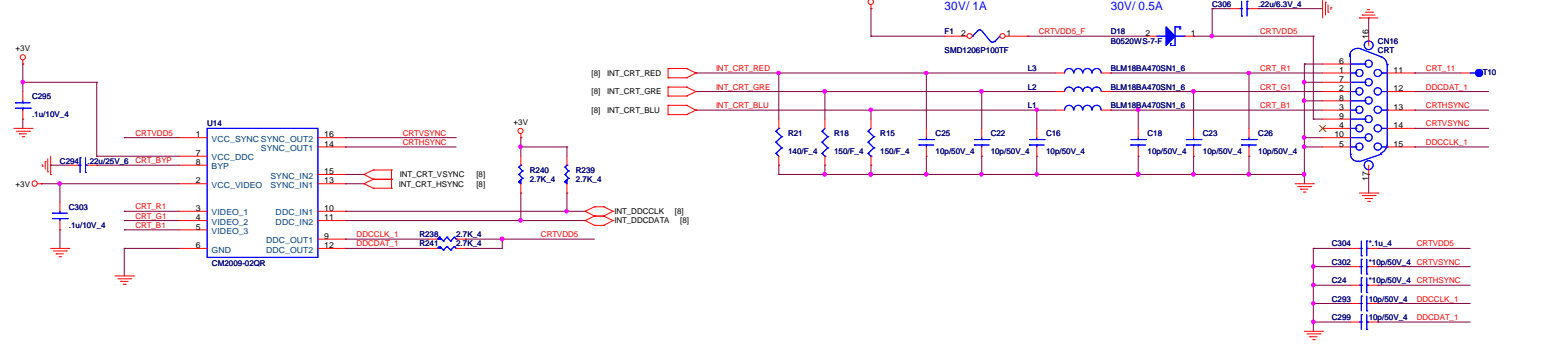
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	USE DEFAULT PCIE STRAPS	DISABLE PCI MEM BOOT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



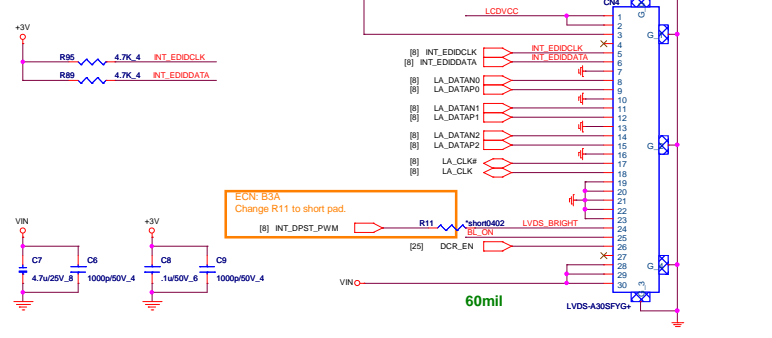
PROJECT : ZQ2
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Size	Document Number	Rev
	SB820-STRAPS	1A
Date:	Thursday, March 04, 2010	Sheet 14 of 36

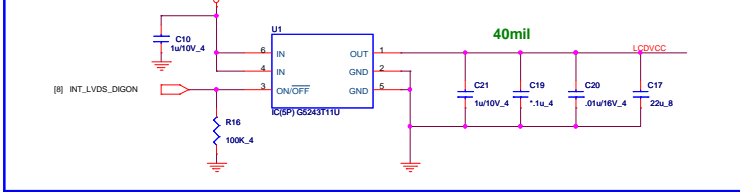
CRT



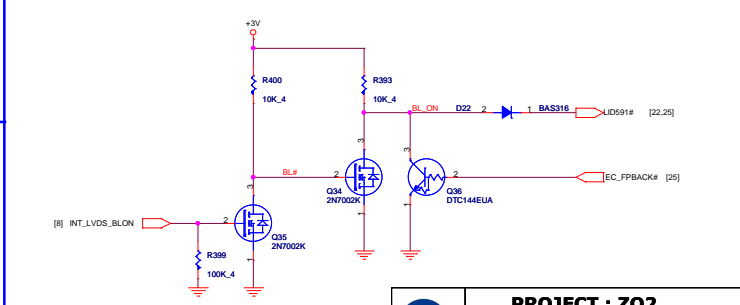
LVDS(LDS)



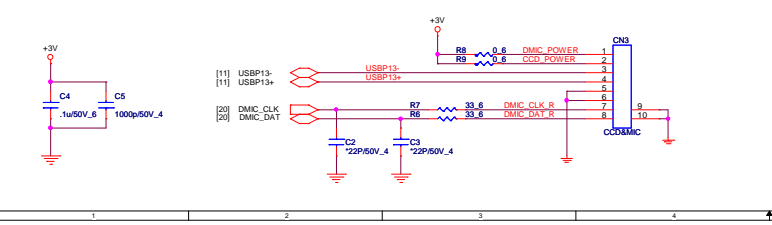
LCD PW(LDS)



Backlight Control(LDS)



CAMERA Module(CCD)

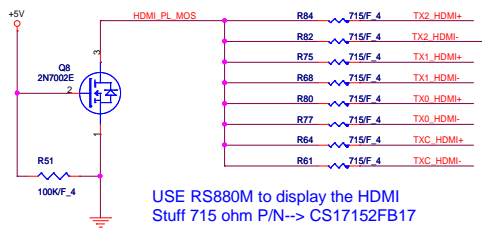


PROJECT : ZQ2
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Size	Document Number	Rev
	CRT/LVDS/LID	3A
Date	Thursday, March 04, 2010	Sheet 15 of 56

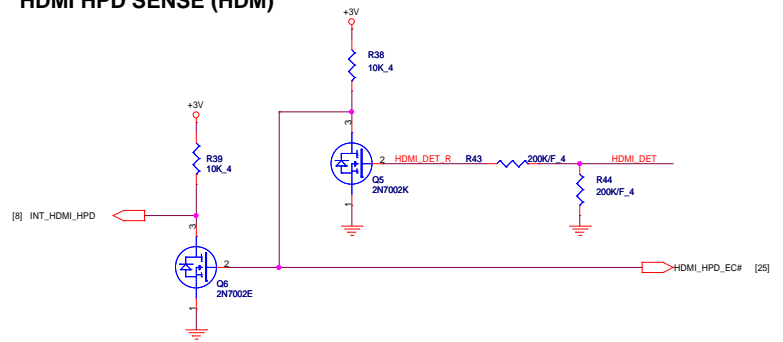
HDMI (HDM)

Close to HDMI Connector



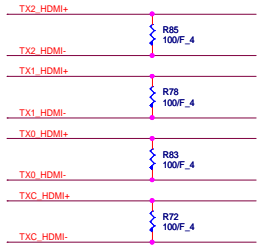
USE RS880M to display the HDMI Stuff 715 ohm P/N--> CS17152FB17

HDMI HPD SENSE (HDM)



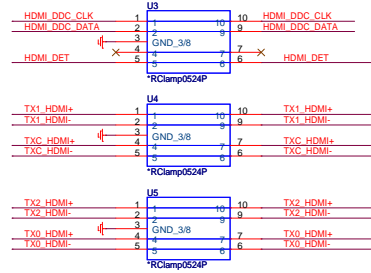
EMI reserve for HDMI(EMC)

Close connector

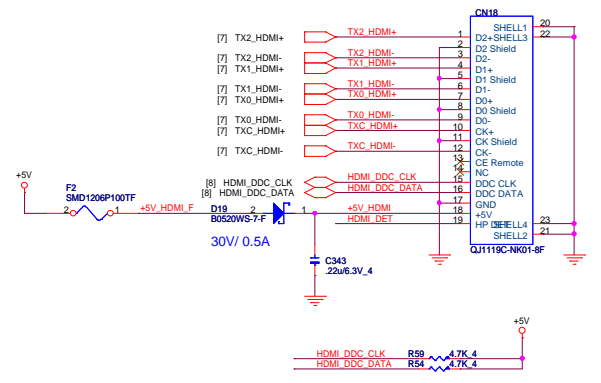


ESD Protect (EMC)

close to HDMI connector



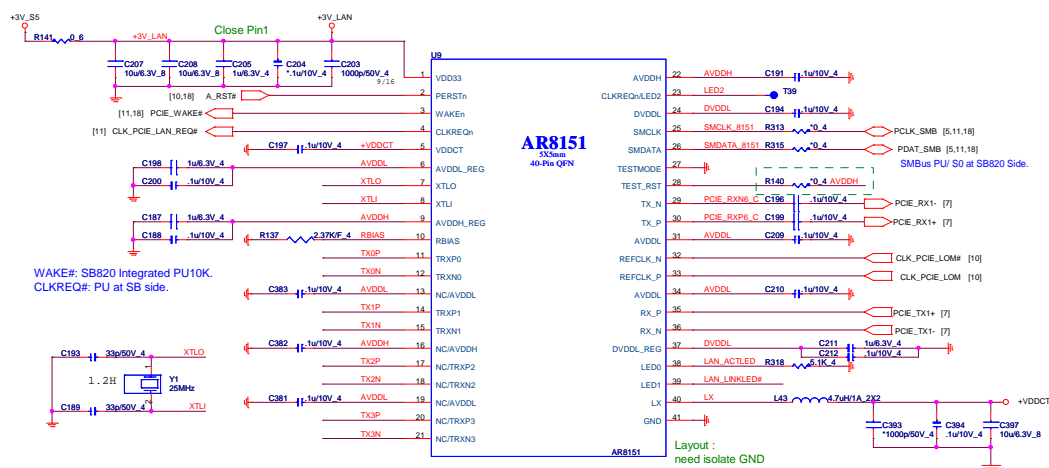
HDMI PORT (HDM)



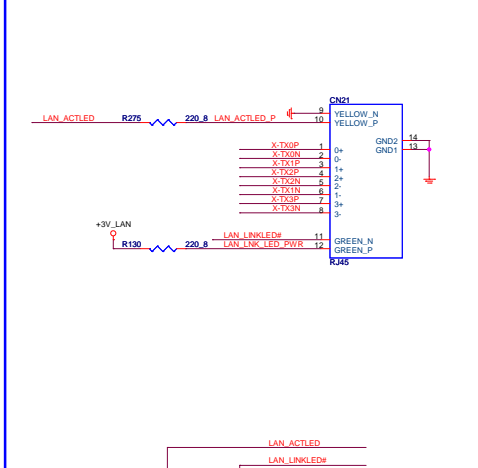
PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	HDMI	1A
Date:	Thursday, March 04, 2010	Sheet 16 of 36

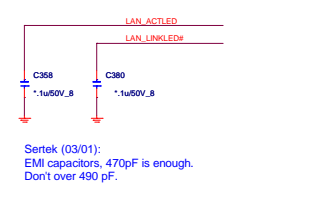
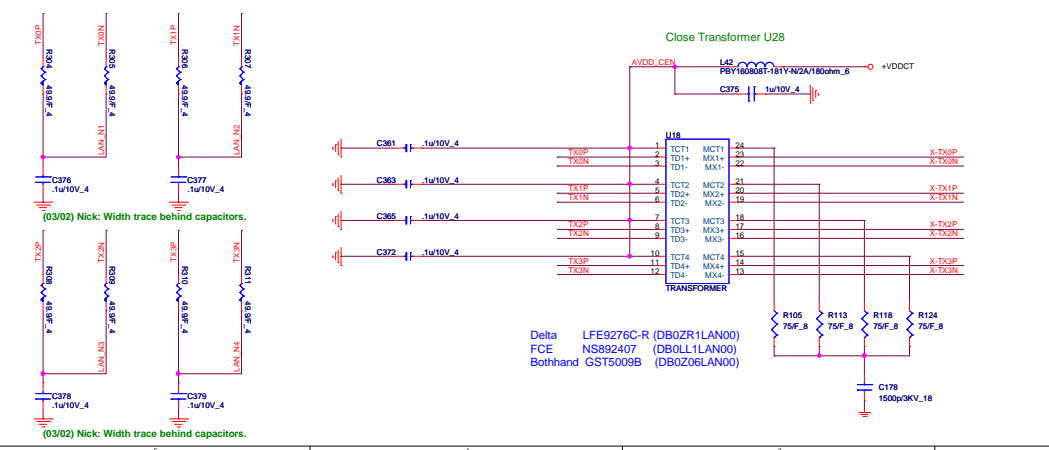
Giga-LAN AR8151



RJ45(LAN)



TRANSFORMER(LAN)



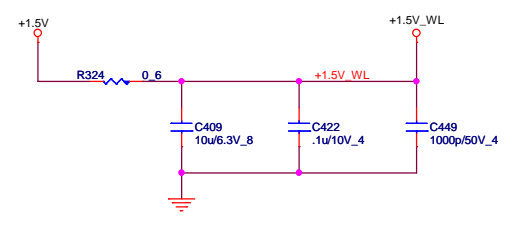
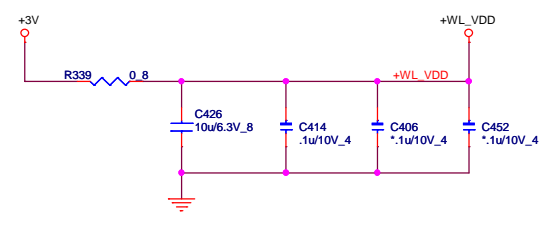
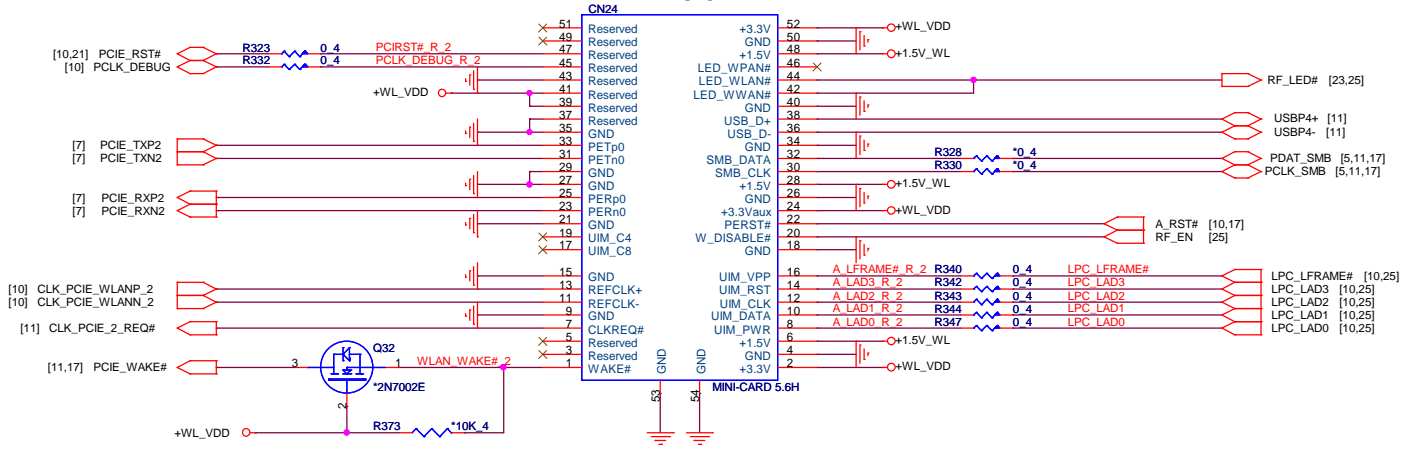
(03/02) Nick: Width trace behind capacitors.


(03/02) Nick: Width trace behind capacitors.

	PROJECT : ZQ2	
	Quanta Computer Inc.	
Size	Document Number	Rev
	LAN (AR8151)	1A
Date:	Thursday, March 04, 2010	Sheet 1Y of 85

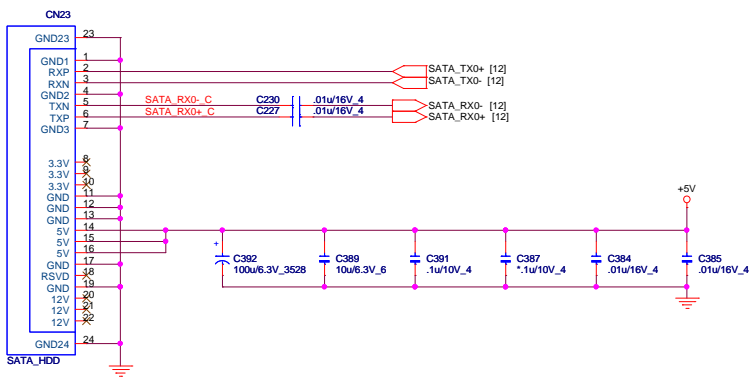
MINI-CARD WLAN(MNC)

H=5.6mm

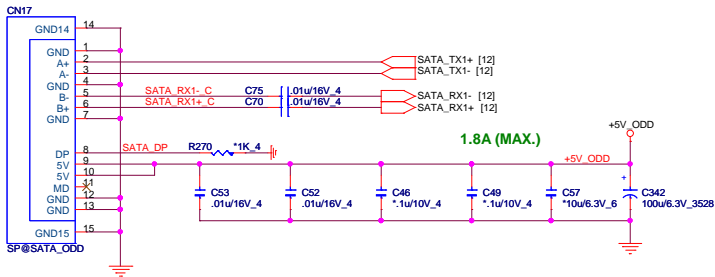


		PROJECT : ZQ2	
		Quanta Computer Inc.	
Size	Document Number		Rev
	Mini-Card/WL		1A
Date:	Thursday, March 04, 2010	Sheet	18 of 36

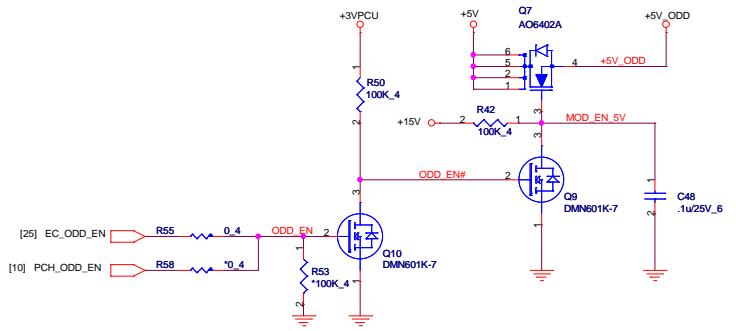
SATA HDD(HDD)



SATA ODD (ODD)



ODD POWER(ODD)



JM-9.5mm (H=2.4mm)/ Slim

Main	DFHS13FR078, DFHS13FR077
Second	DFHS13FR075

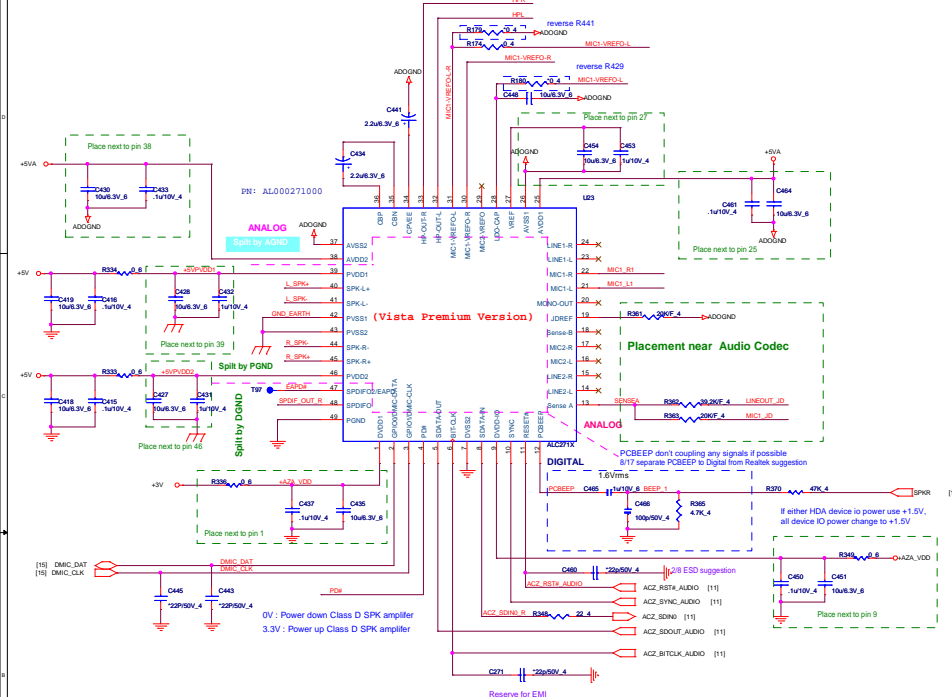
JV-12.7mm(H=5.5mm)/ Standard

Main	DFHS13FR017
Second	DFHS13FR006, DFHS13FR005

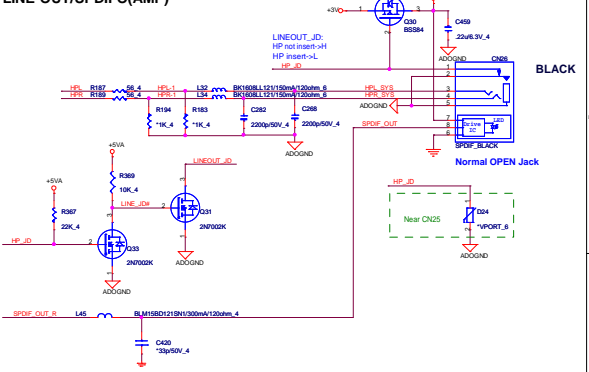
PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	SATA-HDD/ODD/HOLE	1A
Date:	Thursday, March 04, 2010	Sheet 19 of 36

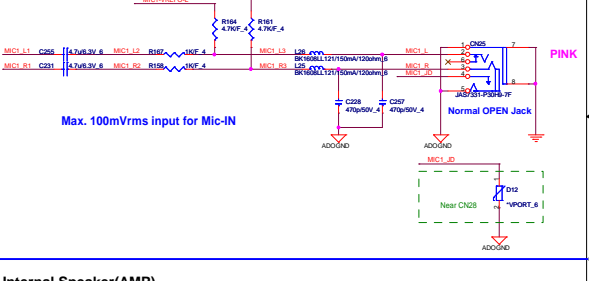
Codec(ADO)



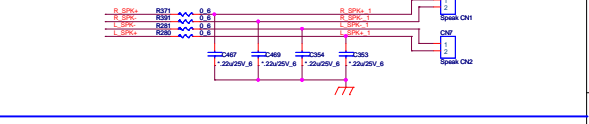
LINE-OUT/SPDIFO(AMP)



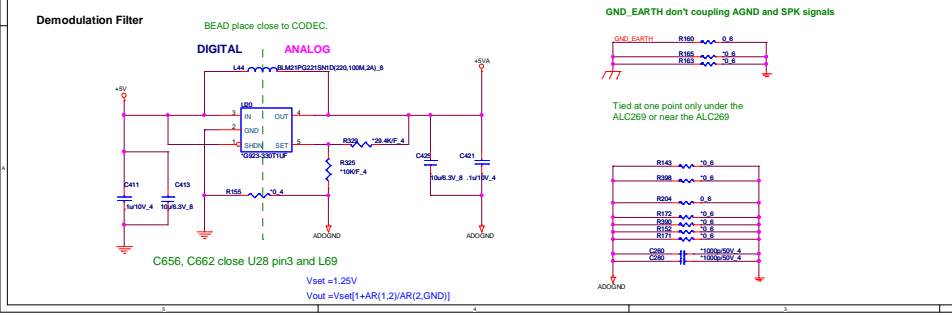
MIC(AMP)



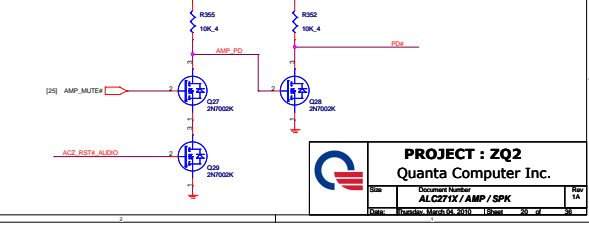
Internal Speaker(AMP)



Power (ADO)

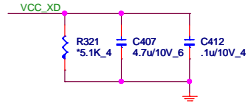
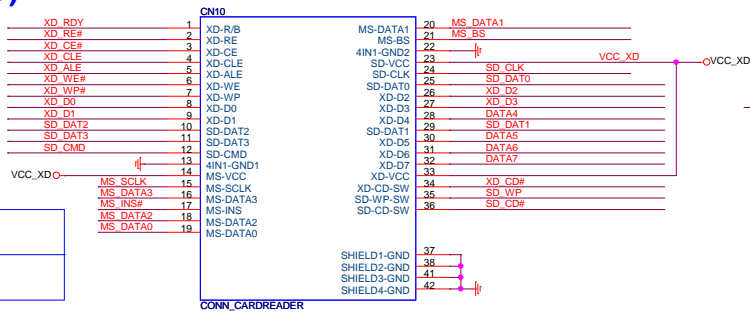


Mute(ADO)

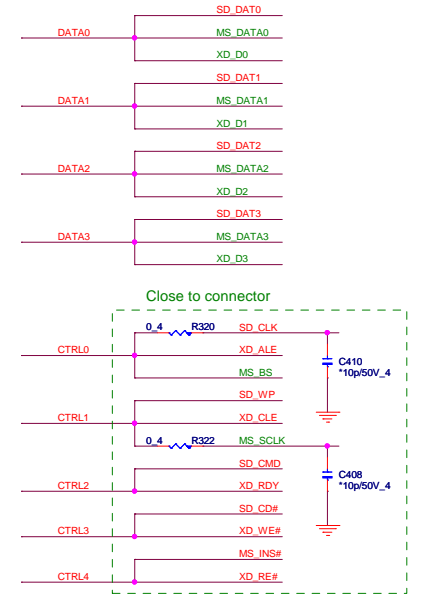
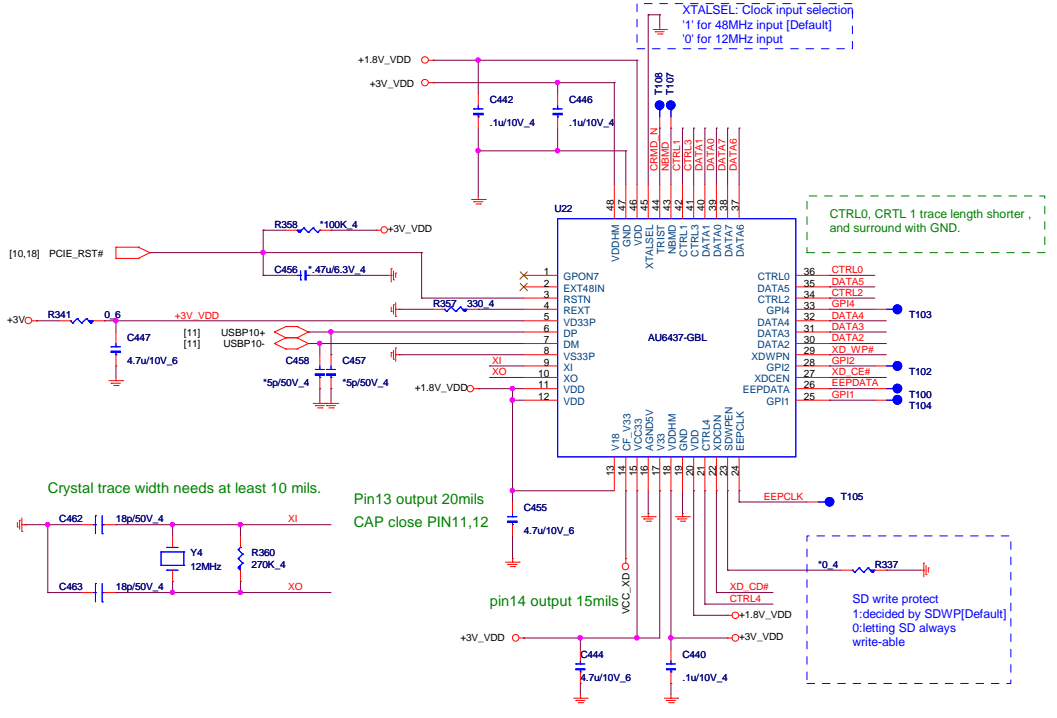


4 IN 1 CARD READER (MMC)

Main	??
Second	??



Close to CN10 pin 14 & pin23
4.7u CAP close to pin23



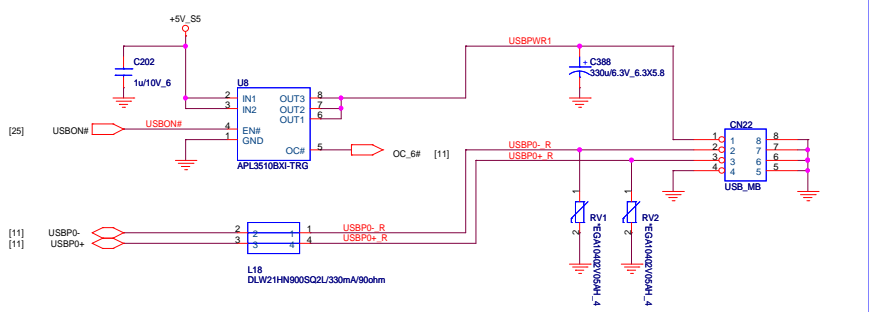
PROJECT : ZQ2

Quanta Computer Inc.

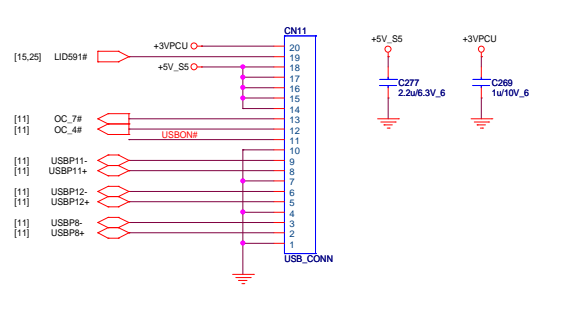
Size	Document Number	Rev
	AU6437 CardReader	1A
Date:	Thursday, March 04, 2010	Sheet 21 of 36

SD write protect
1:decided by SDWP[Default]
0:letting SD always write-able

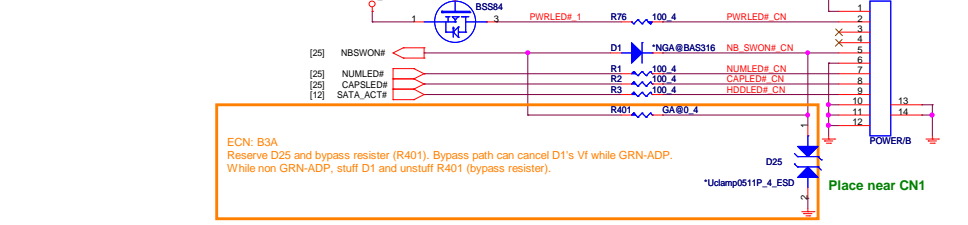
USB PORT(USB/MB)



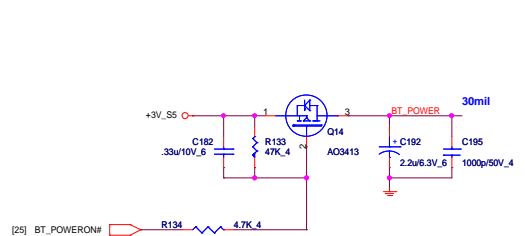
USB BOARD CONN(USB/SB)



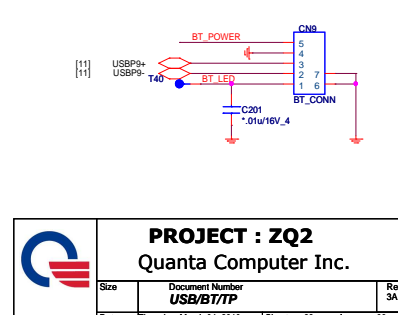
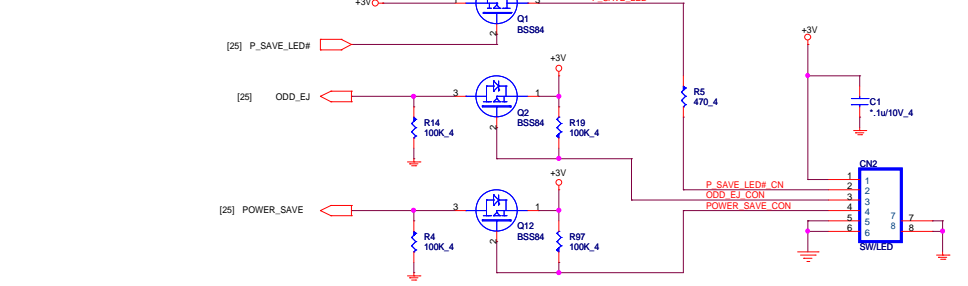
POWER BOARD CONN(UIF)



BLUETOOTH CONN(BTM)



LED BOARD CONNECTOR(UIF)

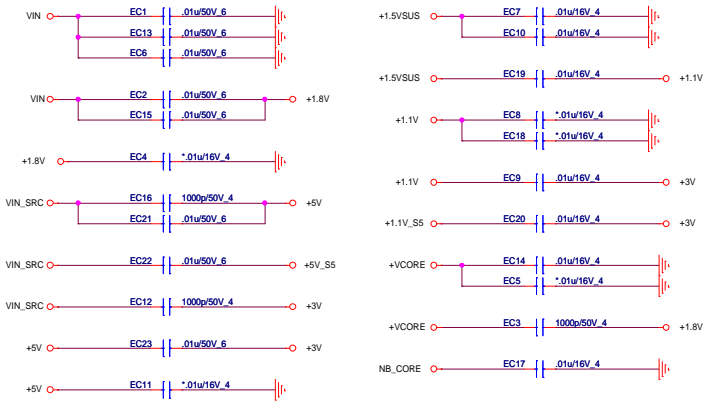


PROJECT : ZQ2
Quanta Computer Inc.

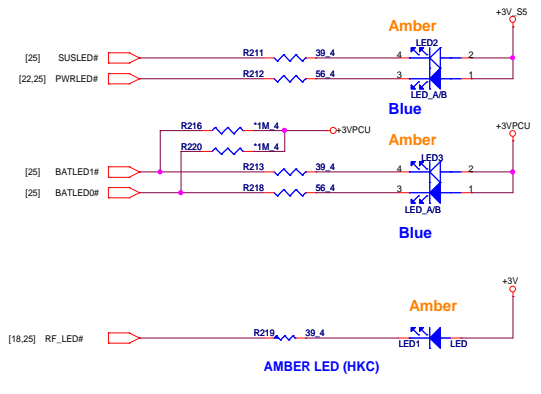
Rev 3A

Size	Document Number	Rev
	USB/BT/TP	3A
Date:	Thursday, March 04, 2010	Sheet 22 of 36

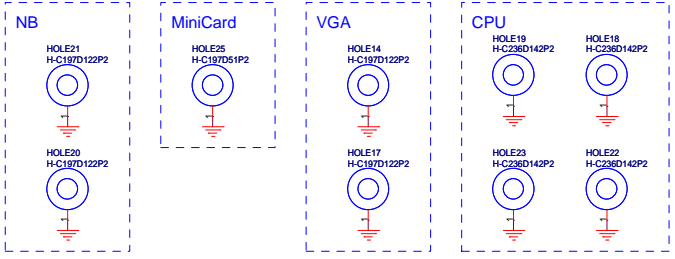
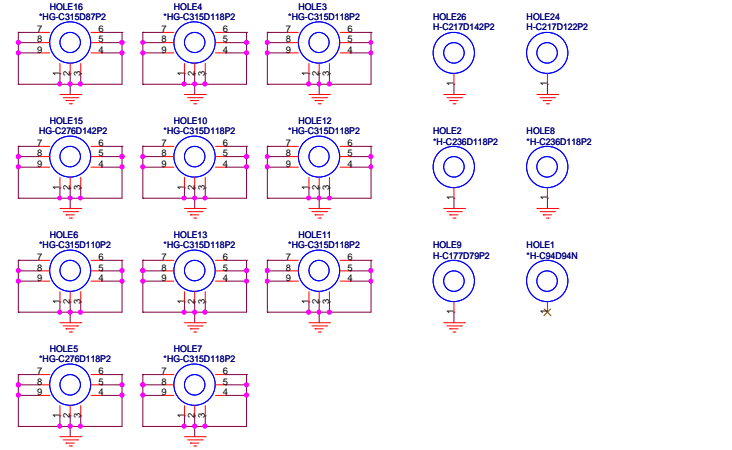
EE RETURN-PATH CAPACITORS(EMC)



LED(UIF)

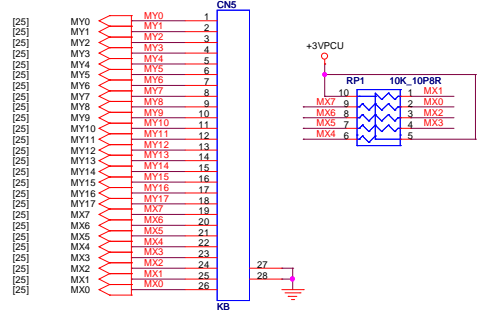


HOLE(OTH)

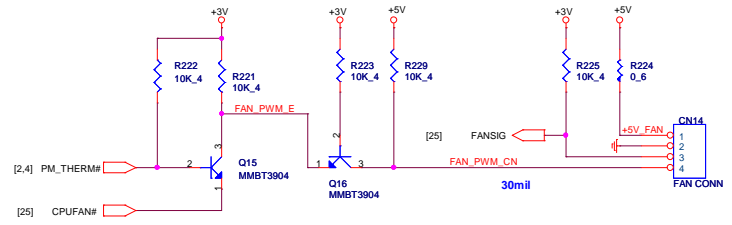


	PROJECT : ZQ2		
	Quanta Computer Inc.		
Size	Document Number	Rev	
	POWER/USB/BT/TPMDC	1A	
Date:	Thursday, March 04, 2010	Sheet	23 of 36

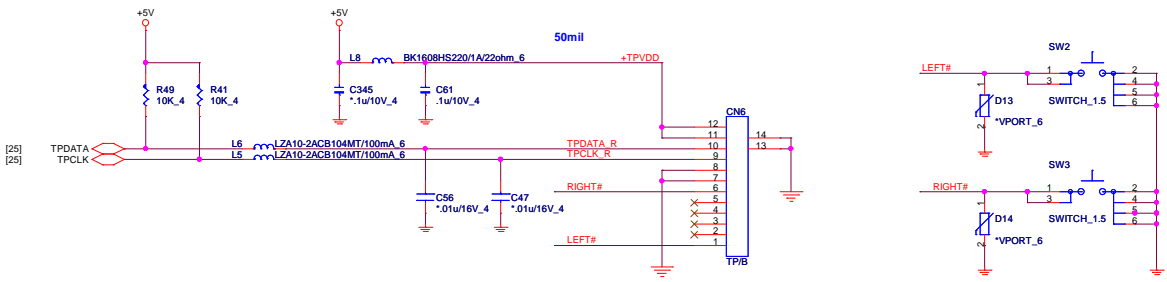
K/B(KBC)



CPU FAN(THM)



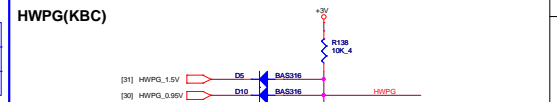
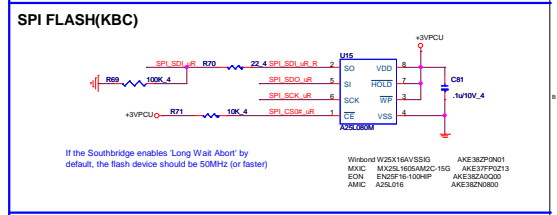
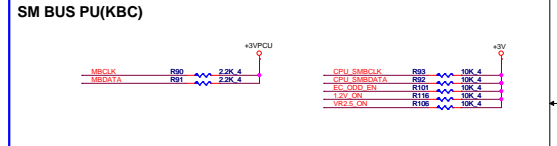
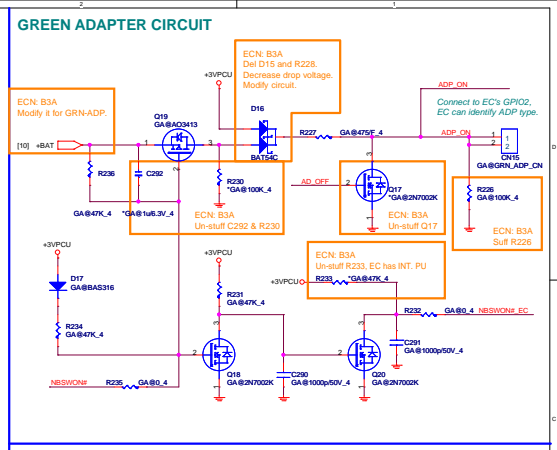
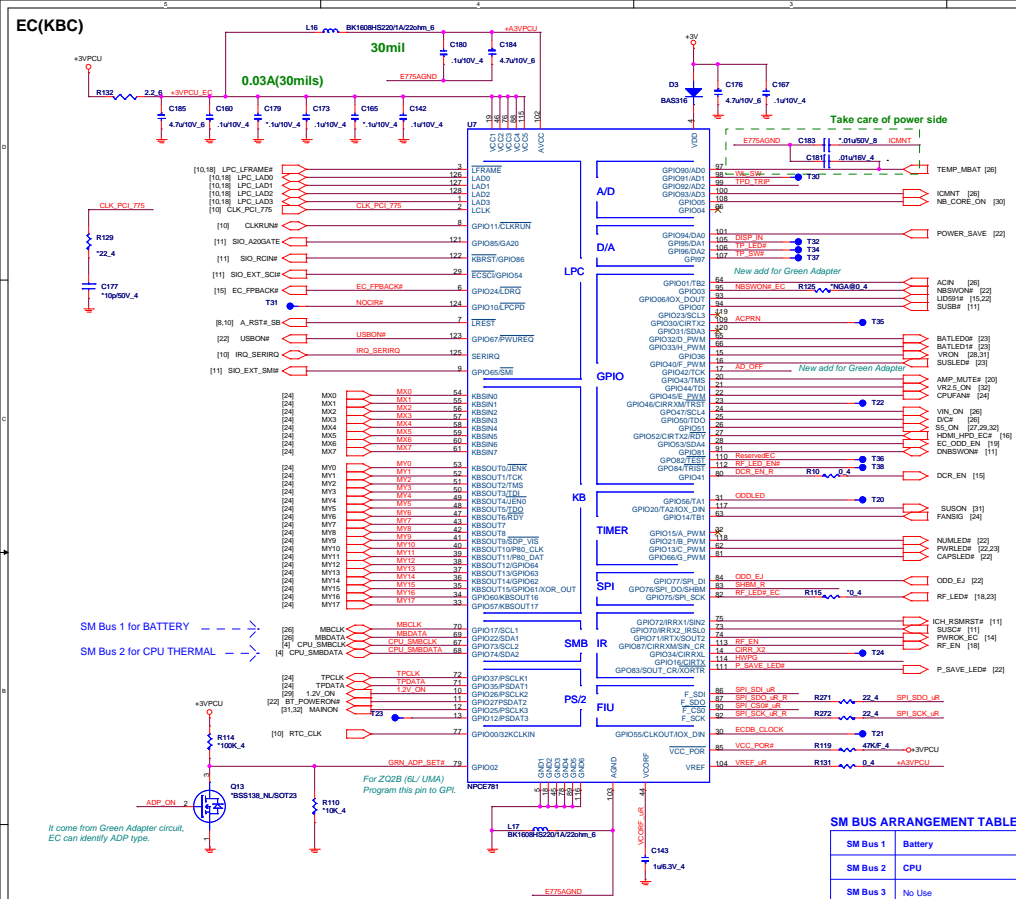
TOUCHPAD BOARD CONN(TPD)



PROJECT : ZQ2

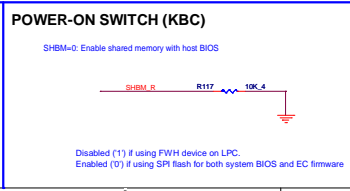
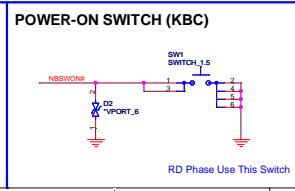
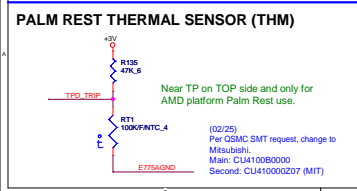
Quanta Computer Inc.

Size	Document Number	Rev
	KB/FAN/EE RETURN CAP	1A
	Date: Thursday, March 04, 2010	Sheet 24 of 36



SM BUS ARRANGEMENT TABLE

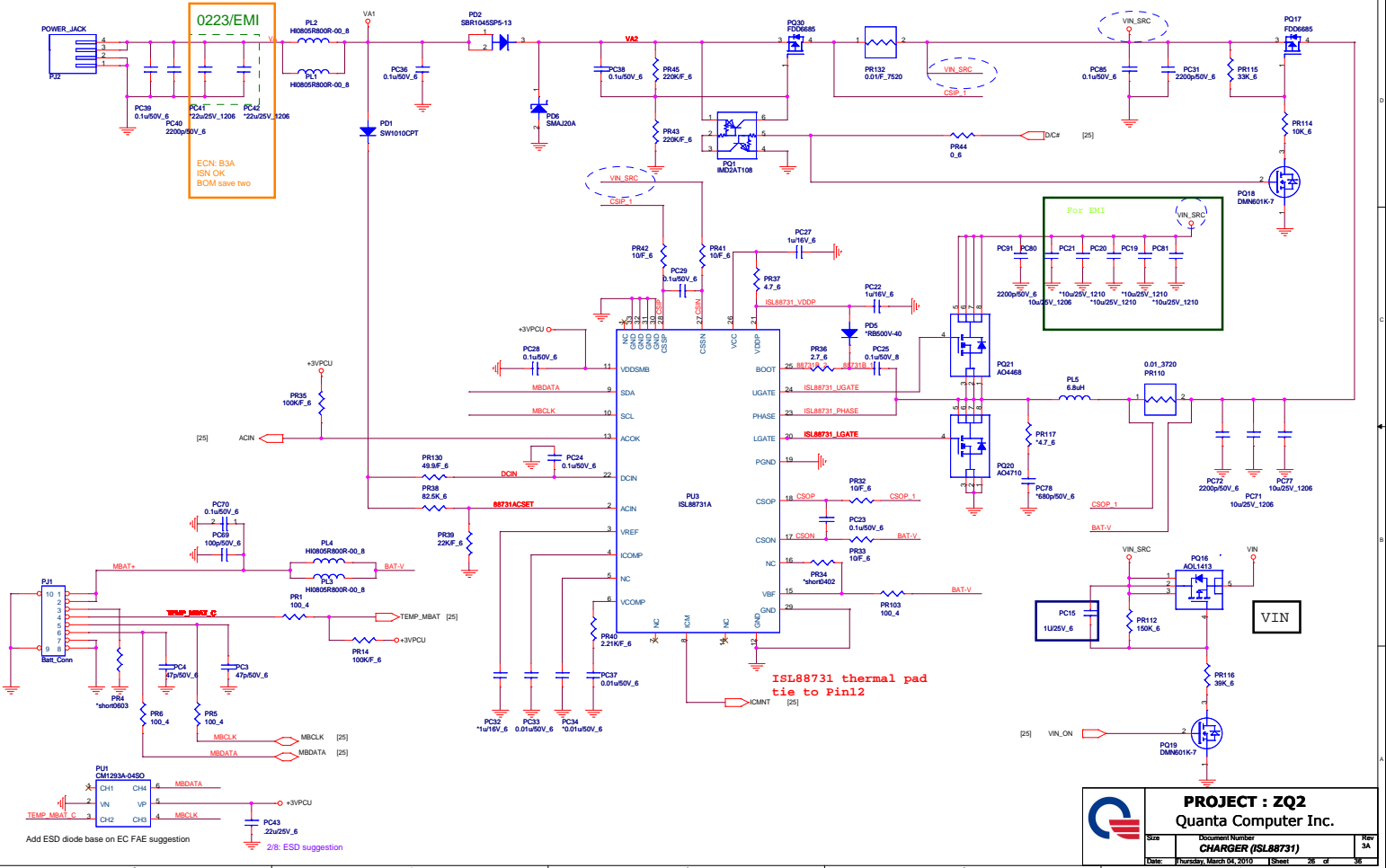
SM Bus 1	Battery
SM Bus 2	CPU
SM Bus 3	No Use



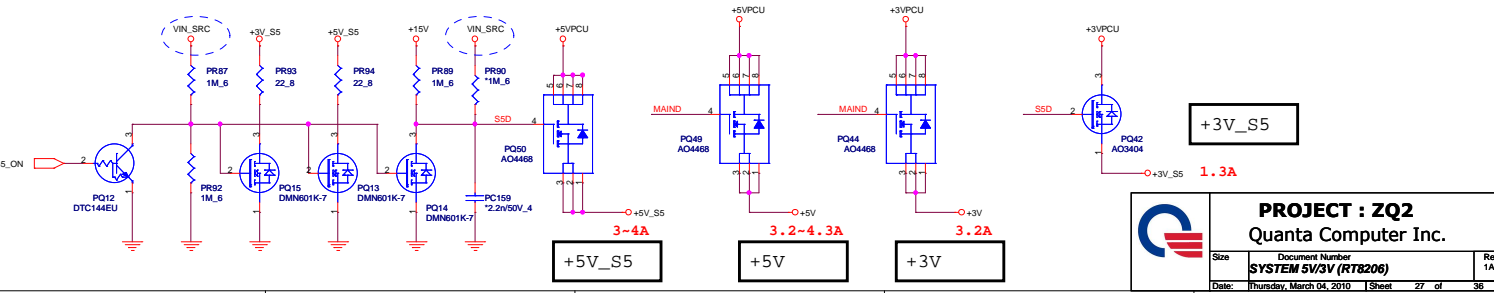
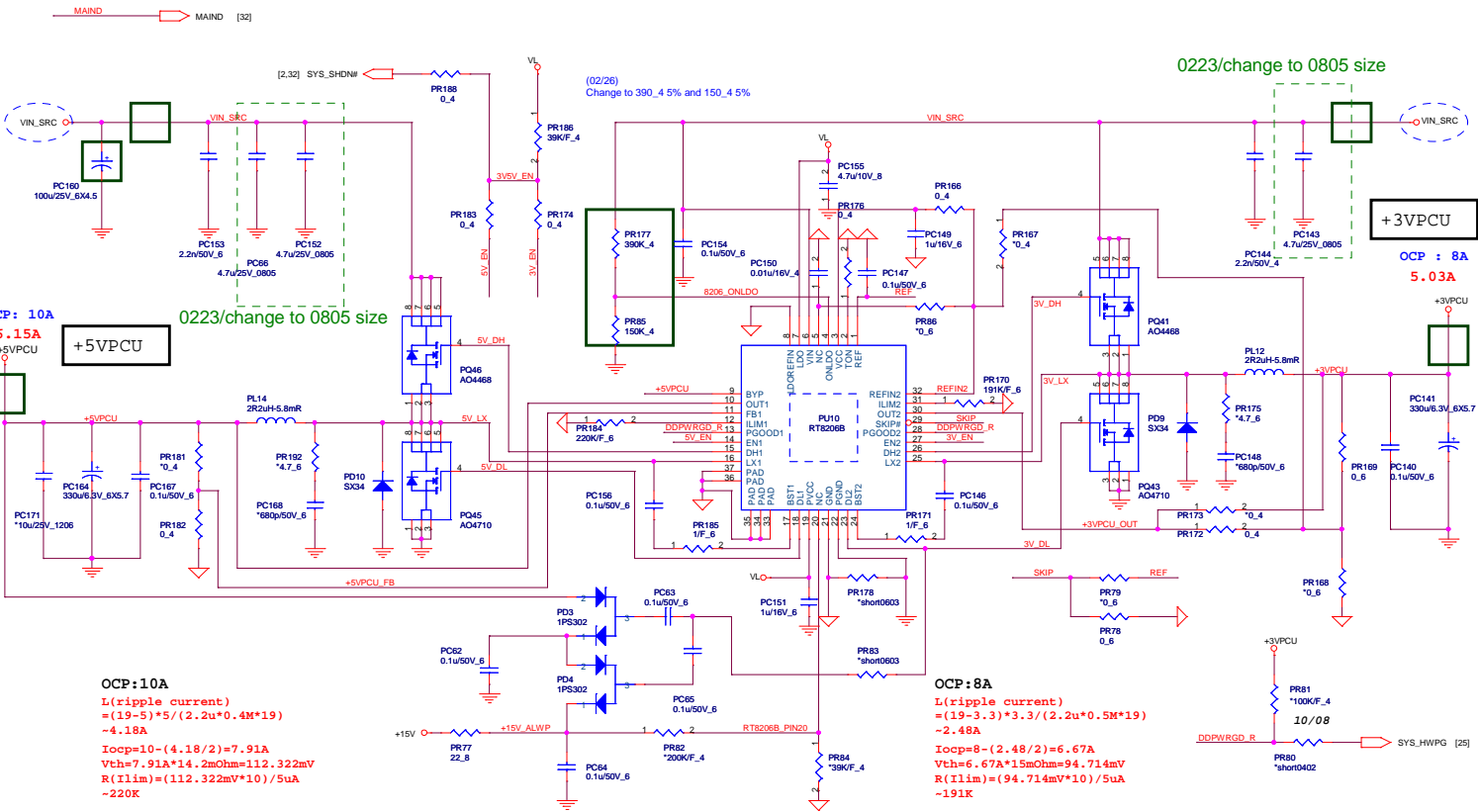
PROJECT : ZQ2

Quanta Computer Inc.

Size	Document Number	Rev
	WPCE75C_ODG & FLASH	3A
Date	Friday, March 04, 2010	Sheet
		25 of 35



PROJECT : ZQ2		
Quanta Computer Inc.		
Size	Document Number	R67
	CHARGER (ISL88731)	3A
Date:	Thursday, March 08, 2018	Sheet 26 of 36



PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	SYSTEM 5V/3V (RT8206)	1A
Date:	Thursday, March 04, 2010	Sheet 27 of 36

14) CPU_VDDNB_CORE CPU_VDDNB_CORE 3A

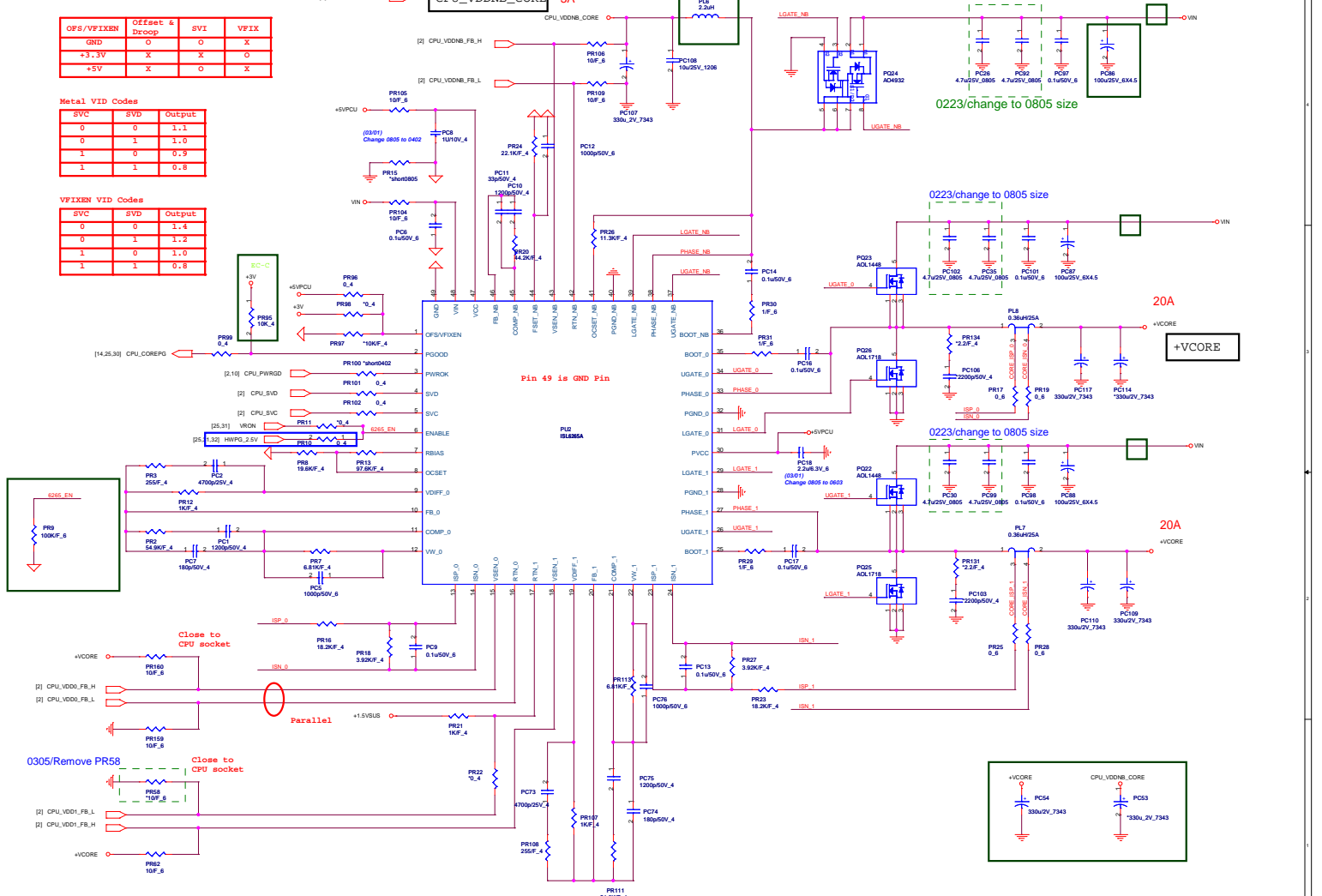
OPS/VFIXEN	Offset & Droop	SVID	VFIX
GND	0	0	X
+3.3V	X	X	0
+5V	X	0	X

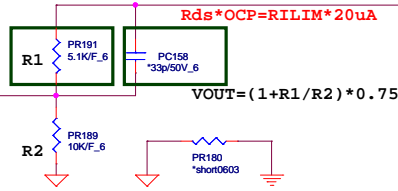
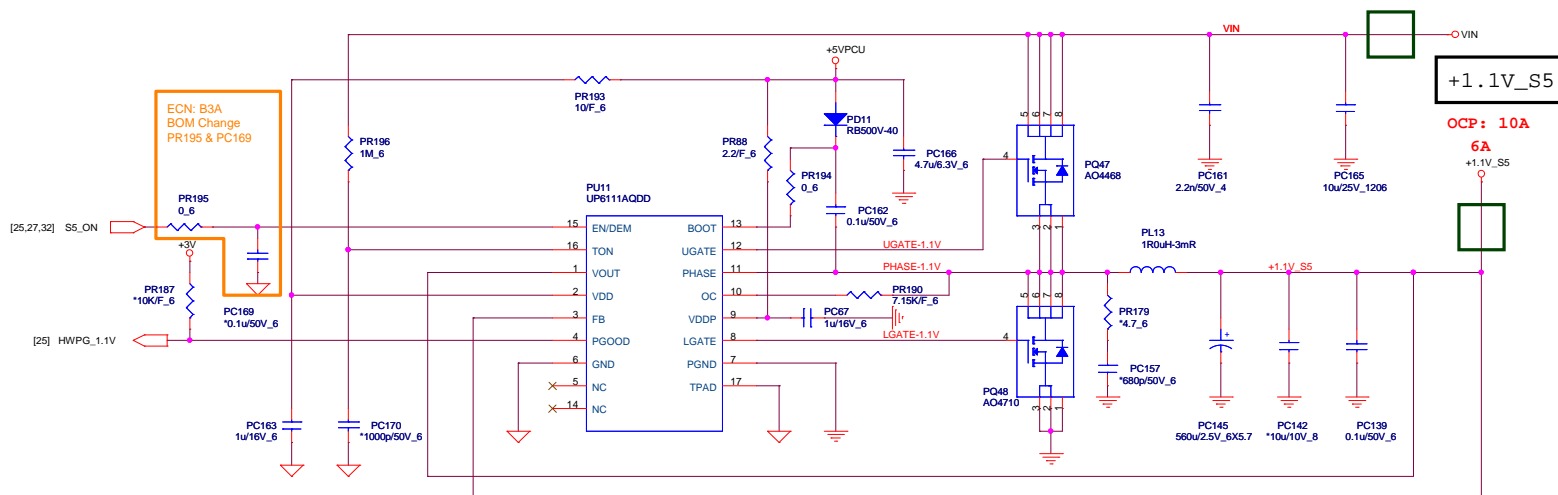
Metal VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VFIXEN VID Codes

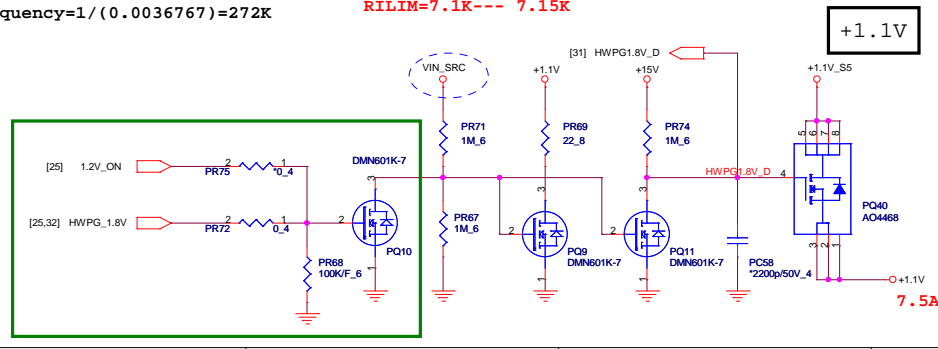
SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8





$TON = 3.85p * RTON * Vout / (Vin - 0.5)$
 $Frequency = Vout / (Vin * TON)$
 $TON = 3.85p * 1M * 1 / (Vin - 0.5)$
 $Frequency = 1 / (0.0036767) = 272K$

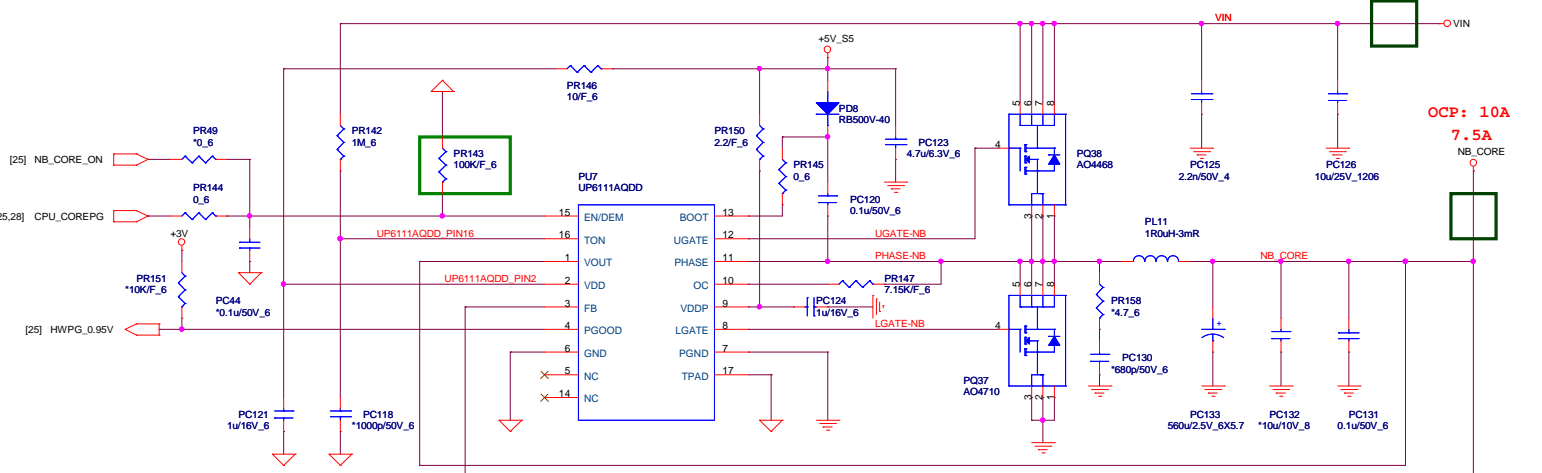
AO4710 $R_{dson} = 11.7 \sim 14.2m\Omega$
 I (ripple current)
 $= (19 - 1.1) * 1.1 / (1u * 272k * 19)$
 $\sim 3.81A$
 $14.2m * 10 = RILIM * 20uA$
 $RILIM = 7.1K \sim 7.15K$



PROJECT : ZQ2

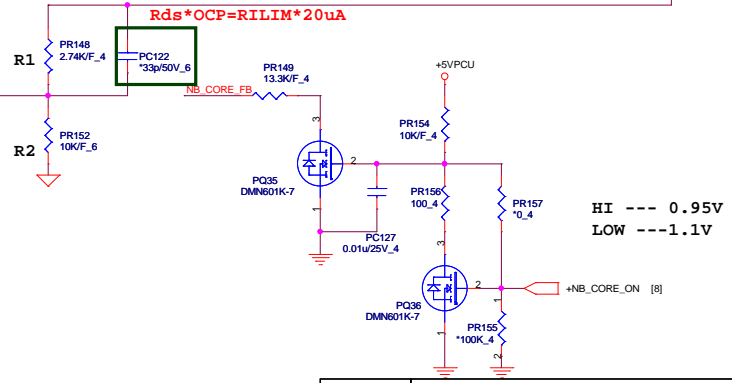
Quanta Computer Inc.

Size	Document Number	Rev
	VCCP 1.1V(UP6111A)	3A
Date:	Thursday, March 04, 2010	Sheet 29 of 36



$$V_{OUT} = (1 + R1/R2) * 0.75$$

$$R_{ds} * OCP = RILIM * 20\mu A$$



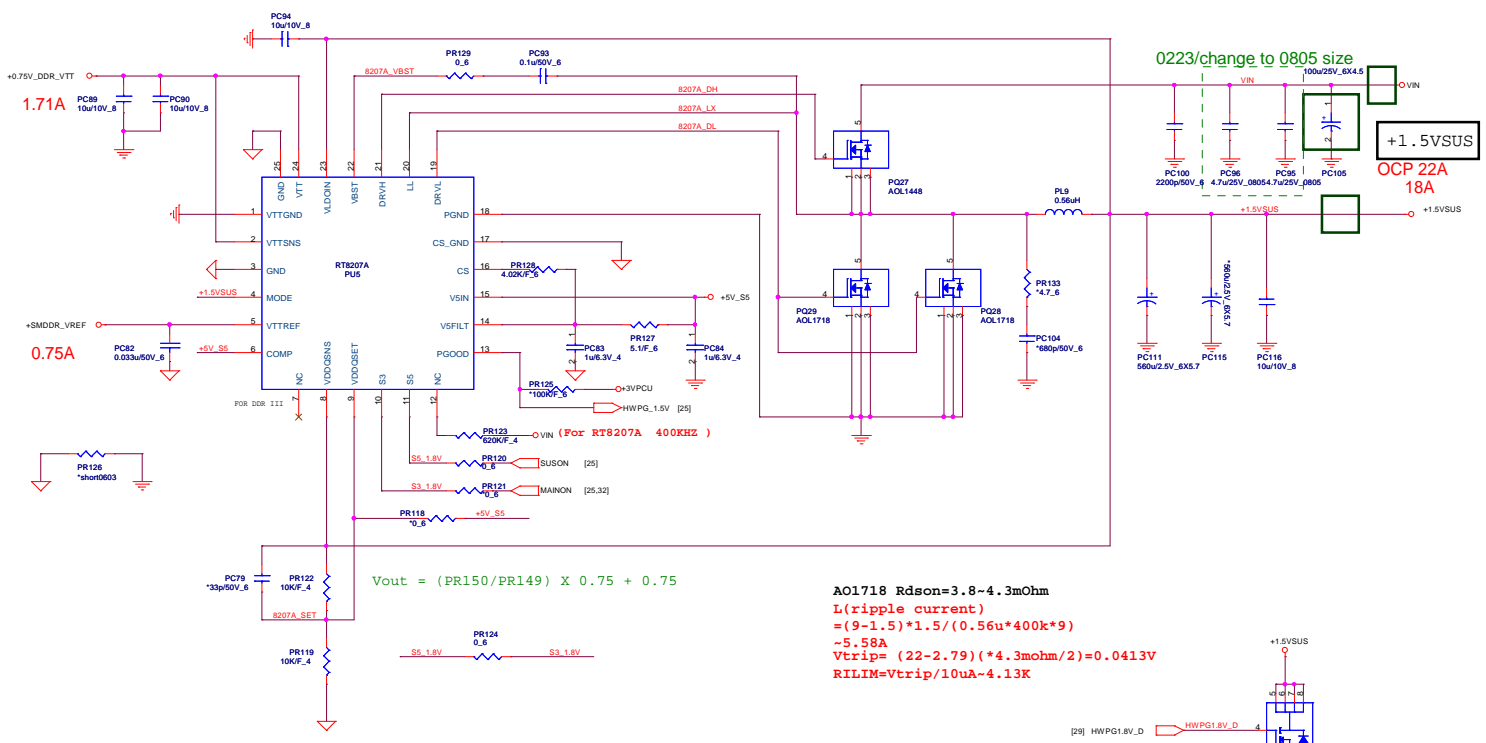
HI --- 0.95V
LOW --- 1.1V

$TON = 3.85p * RTON * Vout / (Vin - 0.5)$
 $Frequency = Vout / (Vin * TON)$
 $TON = 3.85p * 1M * 1 / (Vin - 0.5)$
 $Frequency = 1 / (0.0036767) = 272K$

AO4710 $R_{ds(on)} = 11.7 \sim 14.2m\Omega$
 $L(\text{ripple current}) = (1.9 - 1.05) * 1.05 / (1u * 272k * 19) \sim 3.646A$
 $14.2m * 10 = RILIM * 20\mu A$
 $RILIM = 7.1K \sim 7.15K$

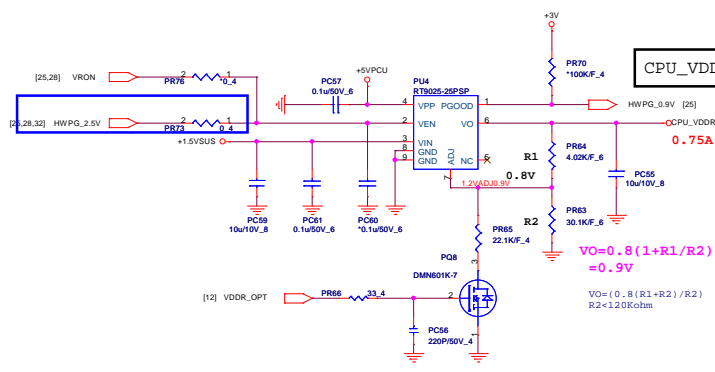
PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
Date	NB_CORE(UP6111A)	1A
Thursday, March 04, 2010	Sheet 30 of 36	

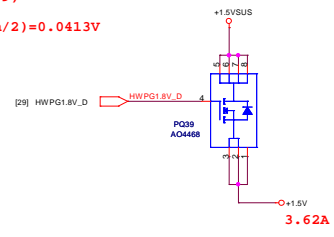


$V_{out} = (PR150/PR149) \times 0.75 + 0.75$

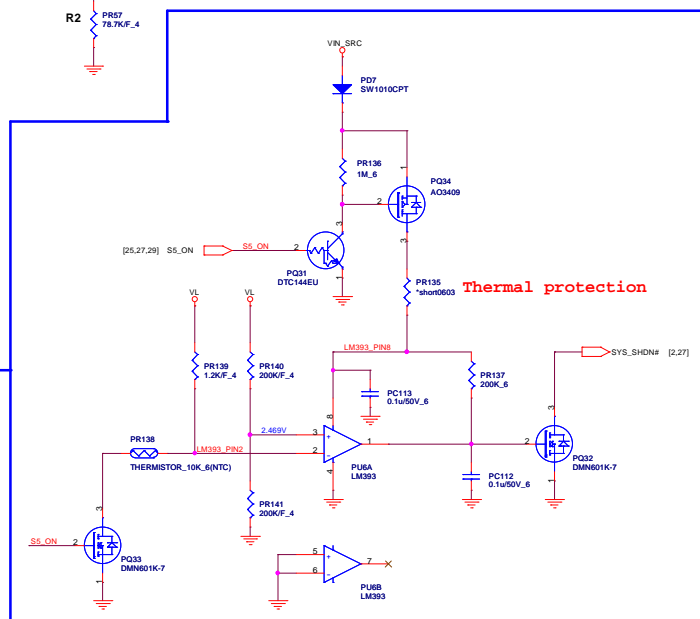
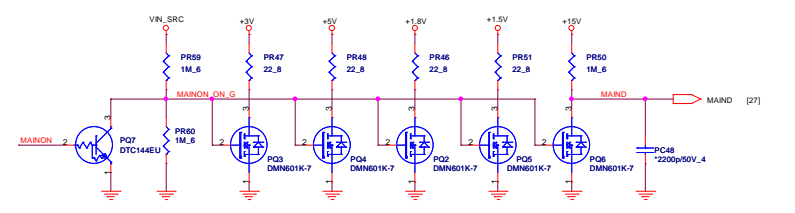
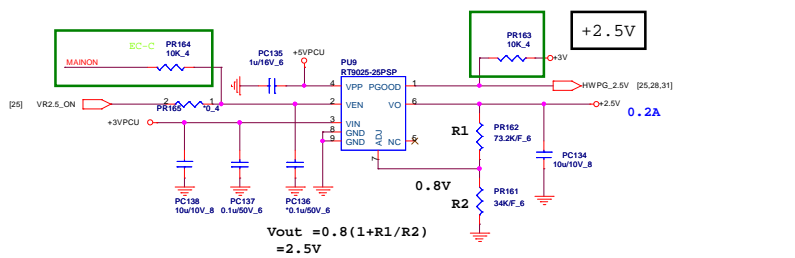
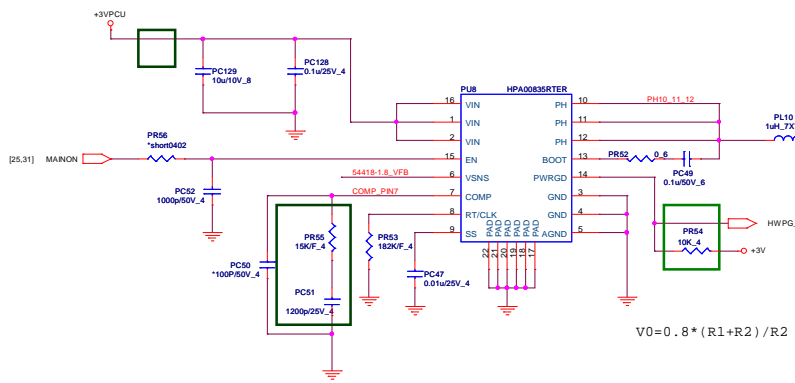
AO1718 $R_{dson} = 3.8 - 4.3 m\Omega$
 I (ripple current) $= (9 - 1.5) \times 1.5 / (0.56 \mu s \times 400k \times 9) \approx 5.58 A$
 $V_{trip} = (22 - 2.79) \times (4.3 m\Omega / 2) = 0.0413 V$
 $RILIM = V_{trip} / 10 \mu A = 4.13 k\Omega$



$V_O = 0.8 \times (1 + R1/R2) = 0.9V$
 $V_O = (0.8 \times (R1 + R2) / R2)$
 $R2 < 120 k\Omega$

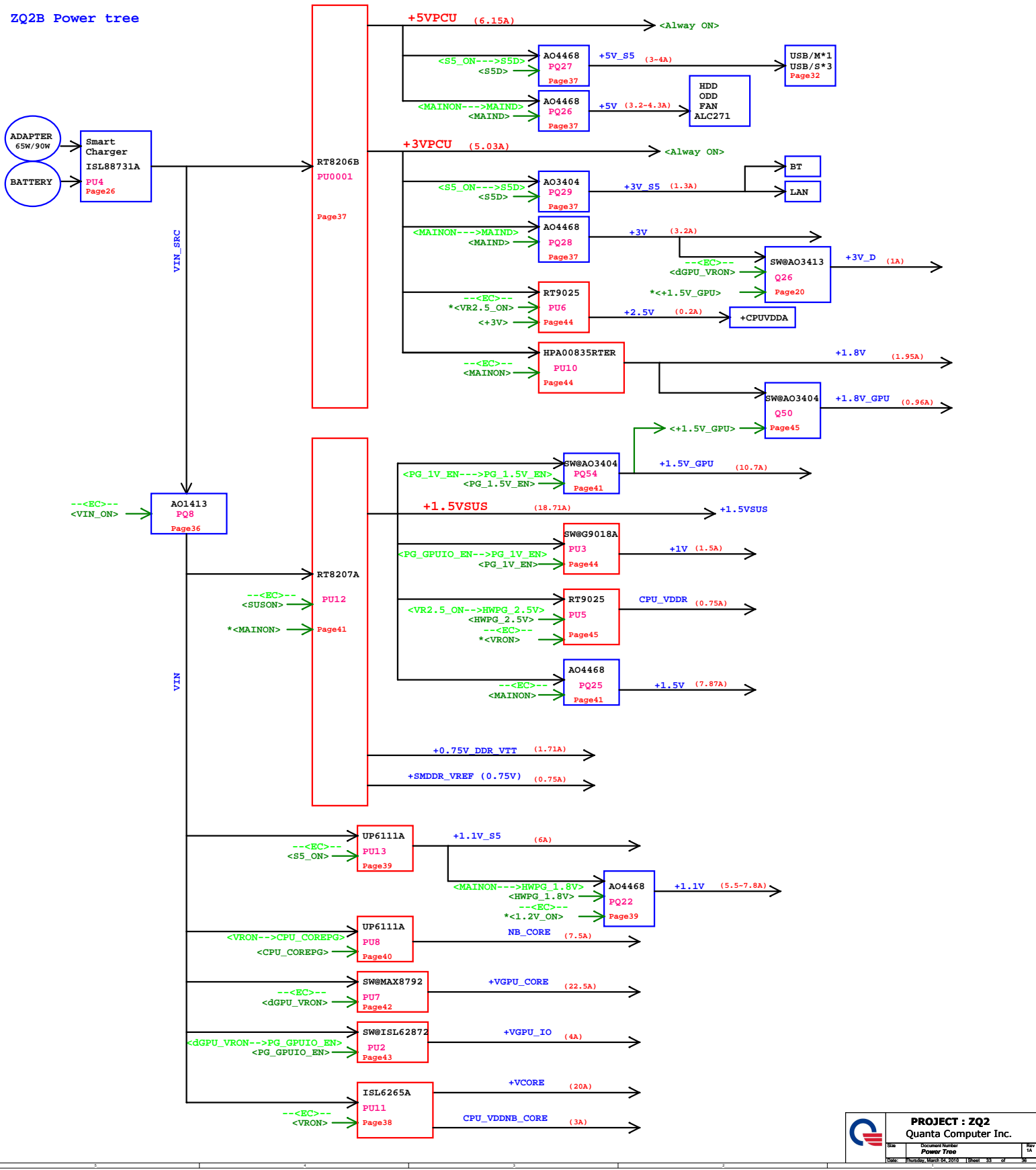


PROJECT : ZQ2		
Quanta Computer Inc.		
Size	Document Number	Rev
	DDR 1.5V(TPS3116)	1A
Date	Thursday, March 04, 2010	Sheet 31 of 36



		PROJECT : ZQ2	
		Quanta Computer Inc.	
Size	Document Number	Rev	
	Discharge / Thermal protection	1A	
Date	Thursday, March 04, 2010	Sheet	32 of 36

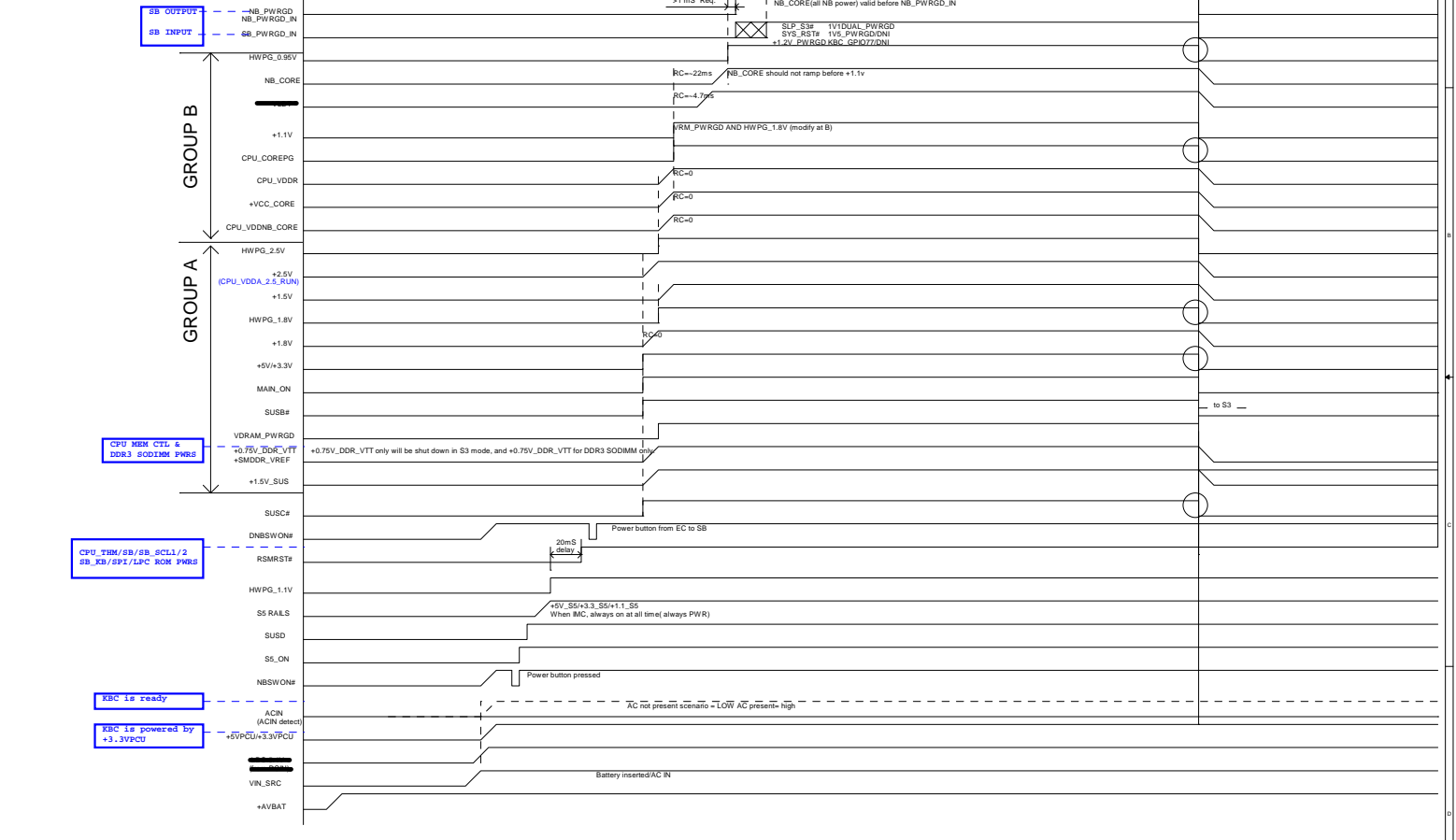
ZQ2B Power tree



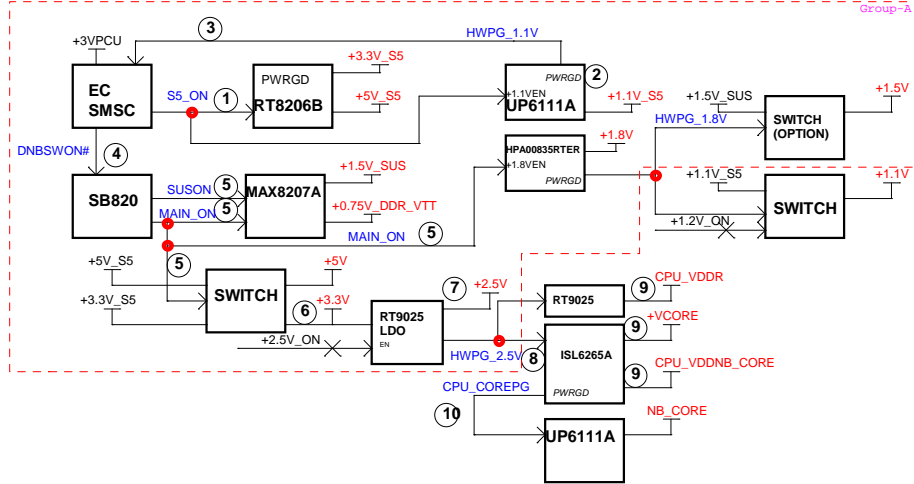
Power on Sequence required:

- SB800:**
 1, +3.3VDUAL ramp before +1.1VDUAL
 2, +3.3V ramp before +1.8V
 3, +1.8V ramp before +1.1V
 4, +3.3V ramp before +1.1V
 5, +3.3VALW_R ramping down time > 300us
 6, 50uS <= All power rails except +3.3VALW_R <= 40mS
 7, 100uS <= +3.3VALW_R <= 40mS

- RS800:**
 1, 0 <= (+3.3V) - (+1.8V) < 2.1
 2, +1.8V ramp before +1.1V
 3, +1.1V ramp before VCC_NB



	PROJECT : ZQ2		Rev 1A
	Quanta Computer Inc.		
Doc#	Document Number	Power Sequence Chart	Rev
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Power on Sequence required:

SB800:
 1, +3.3V_S5 ramp before +1.1_S5
 2, +3.3V ramp before +1.8v
 3, +1.8V ramp before +1.1v
 4, +3.3V ramp before +1.1v
 5, +3.3VALW_R ramping down time > 300us
 6, 50uS <= All power rails except +3.3VALW_R <= 40mS
 7, 100uS <= +3.3VALW_R <= 40mS

RS880:
 1, 0 <(+3.3V) - (+1.8v) < 2.1
 2, +1.8V ramp before +1.1v
 3, +1.1V ramp before VCC_NB

POWER RAILS Sequencing

1	S5_ON	13	+1.8V
2	+3.3V_S5	14	HWPG_1.8V
3	+5V_S5	15	+1.5V
4	+1.1V_S5	16	+2.5V
5	HWPG_1.1V	17	HWPG_2.5V
6	DNBSWON#	18	CPU_VDDNB_CORE
7	SUSON	19	+VCC_CORE
8	+1.5V_SUS	20	CPU_VDDR
9	+SMDDR_VTERM	21	CPU_COREPG
10	MAIN_ON	22	+1.1V
11	+5V	23	NB_CORE
12	+3.3V	24	

SB820 Sequencing

1	+3.3V_S5
2	ICH_RSMRST#
3	S0 POWER
4	PCIE_RCLKP/N
5	PCICLK[4:0]
6	SB_PWRGD_IN
7	NB_PWRGD_IN
8	LDT_PG
9	KBRST#
10	A_RST#
11	PCIRST#
12	LDT_RST#

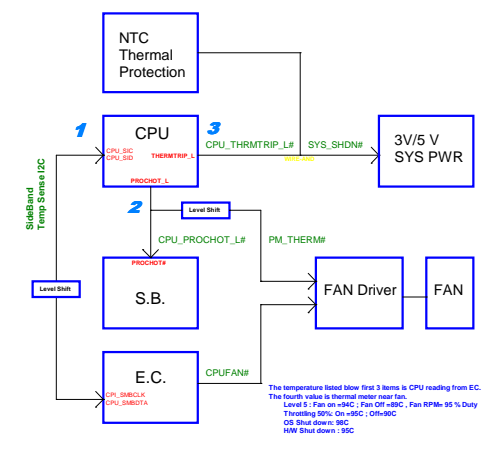
RS880 Sequencing

1	+3.3V
2	NB POWER RAILS
3	ATX PS_PWRGD
4	NB INPUT CLOCKS
5	CPUCLK
6	NB_PWRGD
7	SB_PWRGD
8	LDT_PG/CPU_PWRGD
9	PCIRST#_NB_RST#
10	LDT_RST#
11	
12	

EC Sequencing

1	3VPCU
2	NBSWON#
3	VIN_ON
4	S5_ON
5	ICH_RSMRST#
6	-DNBSWON#
7	SUSB#/SUSC#
8	SUSON/USB_ON#
9	MAIN_ON/HWPG
10	VRON
11	PWROK
12	

H/W Thermal Follow Chart



PROJECT : ZQ2
Quanta Computer Inc.

Document Number: **PWR ON SEQ and THERM POLICY**
 Date: **Friday, March 05, 2010** Page: **35** of **36**

Model

REV

CHANGE LIST

MODEL

ZQ2B

FROM To
X 1A

ZQ2B MB

1A

A1A The First Release.

3A

B3A Page 02 Q23 cahnge from FDV301V to BSS138. Becasue FDV301V EOL.

B3A Page 10 Add off-page net of +BAT for Green Adpapter. It can decrease drop voltage. R289 change value to 12K beucase charge current.

B3A Page 15 Change R11's footprint to short pad. BOM cancel R11.

B3A Page 22 Reserve D25 and add R401. It can cancel D1's Vf while GRN-ADP.

B3A Page 25 Del D15 and R228. And change PWR source of ADP_ON. All for decrease drop voltage. And un-stuff Q17 in oredr to EC suggestion.

B3A Page 25 BOM change for fine-tune. Stuff R226 and BOM unstuff C292, R230 and R233.

B3A Page 26 BOM save PC41 and PC42.

B3A Page 29 BOM change for Pr195 and PC169 in order to AMD power up timing requirement.

1A 3A

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DOC NO.

PROJECT MODEL :

ZQ2B

APPROVED BY:

DATE:

2010/03/05

PART NUMBER:

DRAWING BY:

REVISION:

1A



PROJECT : ZQ2

Quanta Computer Inc.

Size

Document Number

Change list

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Thursday, March 04, 2010

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Rev

1A

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