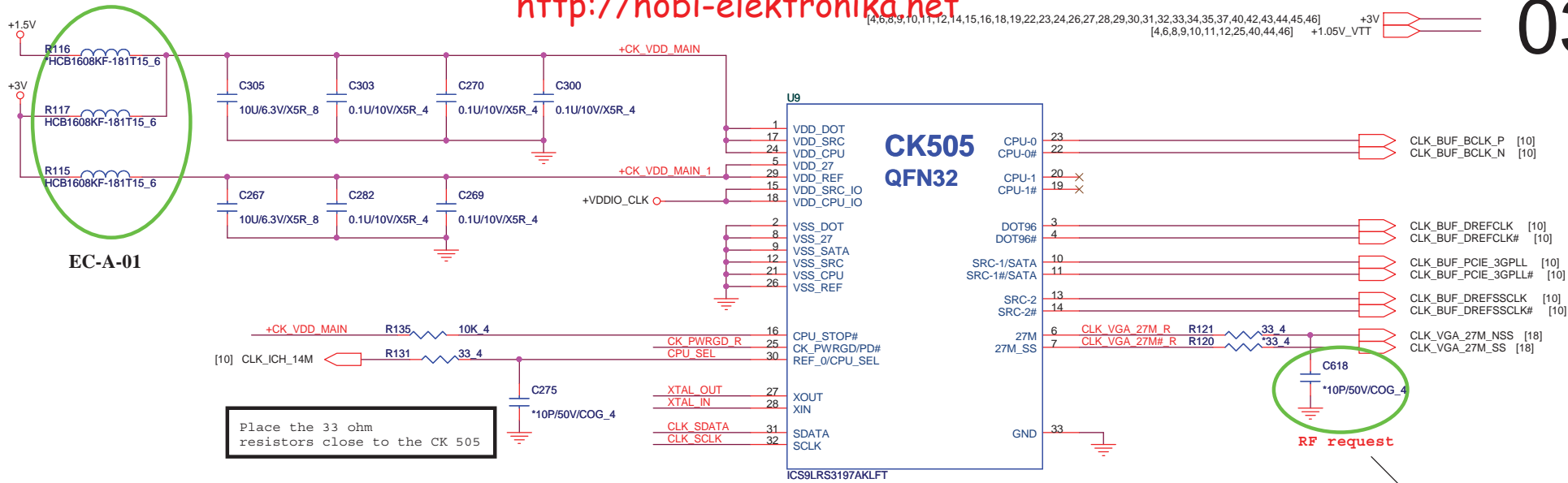


Table of Contents

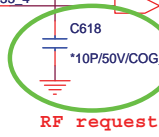
PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3	CLOCK GENERATOR
4-7	Auburndale CPU
8-13	Ibex Peak-M
14-15	DDRIII SO-DIMM
16-22	Discreate VGA (M92-XT)
23	LCD + Camera Conn.
24	HDMI Conn.
25	CRT Conn.
26	Audio Codec ALC269
27	RTL8111DL
28	SATA HDD & ODD
29	USB x 2 & ESATA
30	USB X2/SIM_CARD/LEDs/RF
31	MINI-Card (UWB & WWAN)
32	MINI-Card (WLAN)
33	ONFI
34	Express Card
35	K/B & T/P
36	BLUETOOTH
37	FAN & Thermal
38	G-Sensor
39	B To B Conn.
40	iTPM & RFID EEPROM
41	KBC IT8502E
42	HOLD & SKEW
43	Discharge
44	Charger
45	DDR3 (TPS5116REGR)
46	1.05V_VTT & 1.05_PCH (RT8204)
47	3V/5V (MAX17101)
48	CPU (MAX17082)
49	DIS_GFX_VCC (MAX8792)
50	DIS_1.8V_RUN (OZ8116LN)
51	Power Block Dianram
52	XDP
53	Revision & Schematic Value Description
54	BOM Matrix Table

Power States

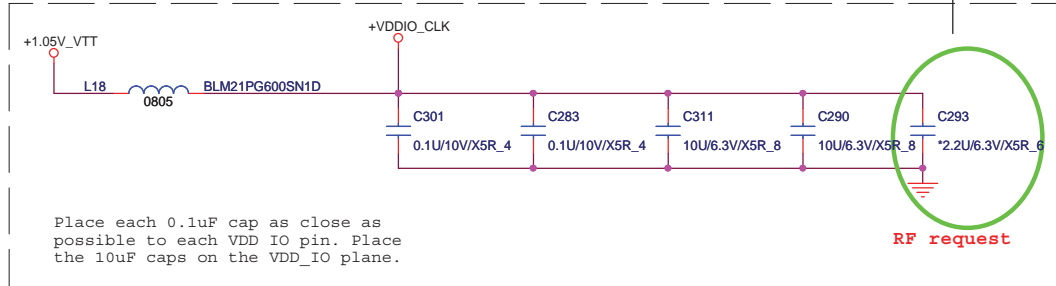
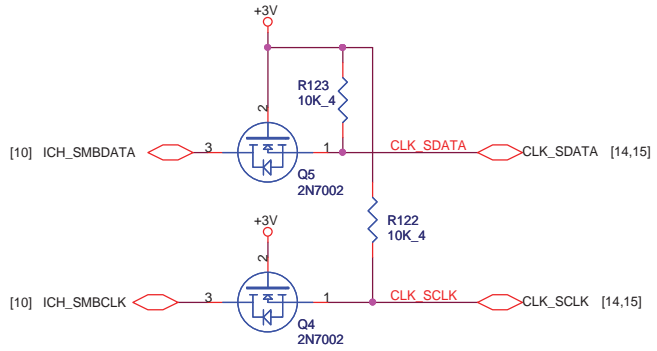
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	23,32,43,44,45,46,47,48,49,50	MAIN POWER		S0-S5
+3VRTC	+3.0V~+3.3V	9,12,41	RTC		S0-S5
3VPCU	+3.3V	9,23,27,30,32,35,39,41,43,44,47	ITE8052 POWER	3V5V_EN	S0-S5
5VPCU	+5V	14,43,44,45,46,47,49,50	DC/DC POWER IC SOURCE	3V5V_EN	S0-S5
+15V	+15V	23,38,43,45,46,47	LARGE POWER	3V5V_EN	S0-S5
LANVCC	+3.3V	27,43	LAN POWER	LAN_ON	
5V_S5	+5V	12,29,30,43	PCH SUS POWER	S5_ON	S0-S3
3V_S5	+3.3V	8,9,10,11,12,43,52	Sys Management,PCH Resume Well,Intel HD Audio,USB,WLAN WiMAX POWER	S5_ON	S0-S3
5VSUS	+5V	23,39,43,48	SLP_S4# CTRLD POWER	SUSON	S0-S3
3VSUS	+3.3V	14,15,30,34,41,43,49	SLP_S4# CTRLD POWER	SUSON	S0-S3
1.5VSUS	+1.5V	4,6,14,15,43,45,46,49,50	SODIMM POWER	SUSON	S0-S3
0.75VSMDDR_VTERM	+0.75V	14,15,43,45	DDR3 SODIMM REFERENCE POWER	MAIN_ON	S0
+5V	+5V	12,18,23,24,25,26,28,35,37,41,43,44	SLP_S3# CTRLD POWER	MAIN_ON	S0
+3V	+3.3V	3,4,8,9,10,11,12,14,15,17,23,25,26,27,28,29,30,31,32,33,34,36,37,38,39,40,41,43,44,45,46,47,48,50,52	SLP_S3# CTRLD POWER	MAIN_ON	S0
+1.8V	+1.8V	6,12,17,18,21,22,33,43,50	LVDS,NVM POWER	MAIN_ON	S0
+1.5V	+1.5V	12,18,19,20,31,32,34,45,46	Mini PCIe,Express Card POWER	MAIN_ON	S0
+1.05V_VTT	+1.05V	4,6,11,12,43,46,48,52	AuBurndale VTT POWER	MAIN_ON	S0
+1.05V_PCH	+1.05V	3,10,12,43,46,52	PCH CORE POWER	1.05V_RUN_ON	S0
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,43,49	VGA CORE POWER	GFXVR_EN	S0
VCC_CORE		6,43,48	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	23	LCD Power	ENVDD	S0
+5V_ODD	+5V	28	ODD Power	MAIN_ON	S0
+5V_HDD	+5V	28	HDD Power	MAIN_ON	S0
BAT-V	+10V~+17V	44	MAIN BATTERY	CHG_PBATT	S0-S5



Place the 33 ohm resistors close to the CK 505

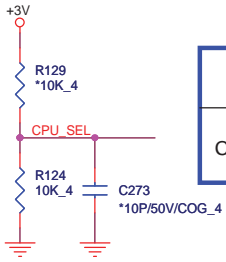


EC-A-02

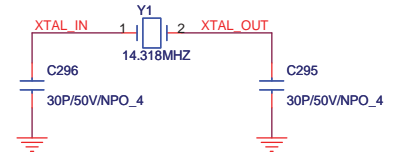
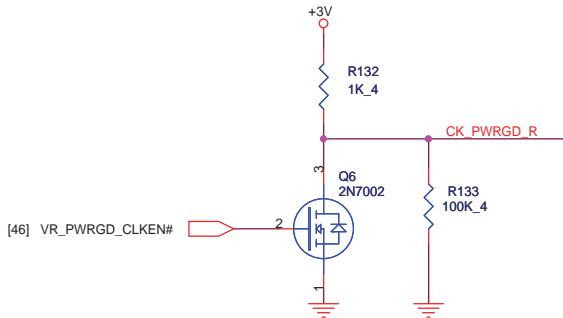


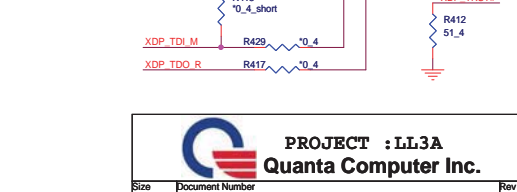
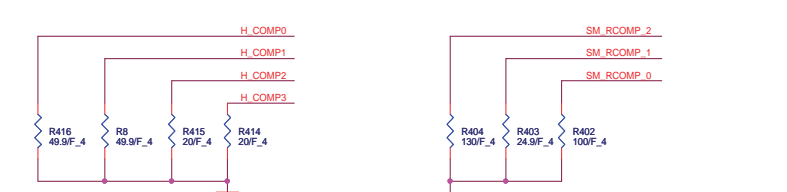
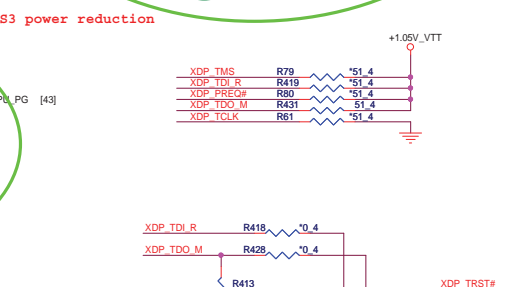
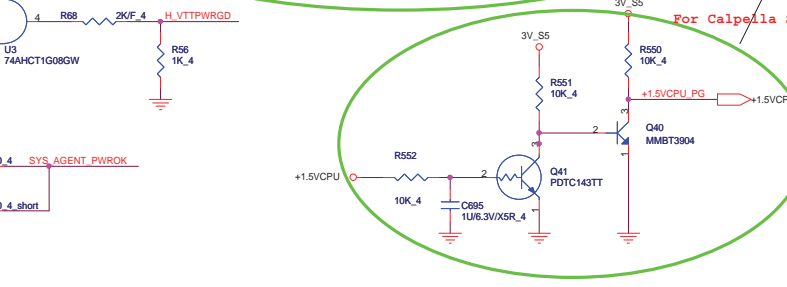
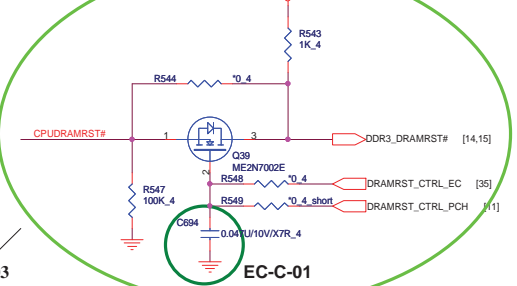
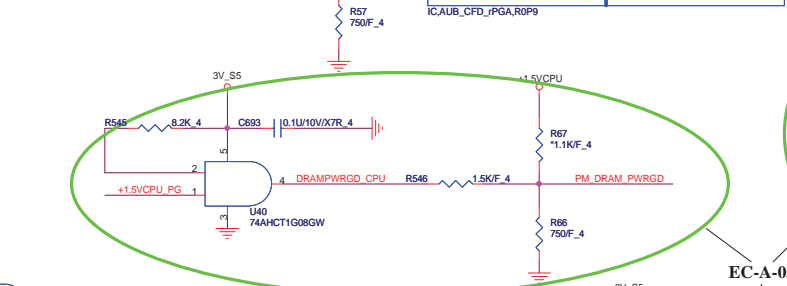
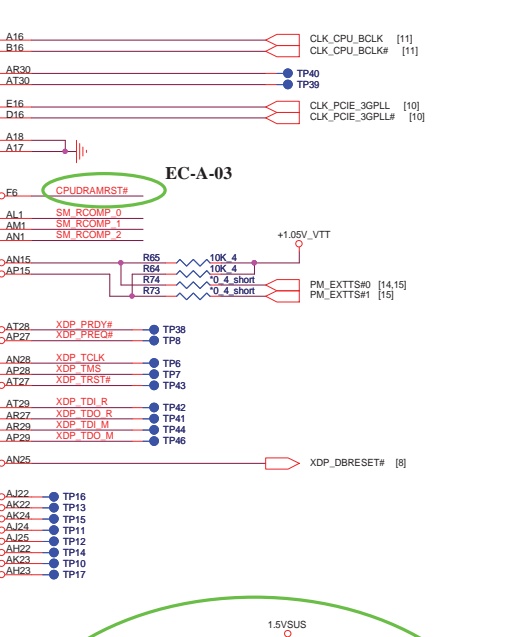
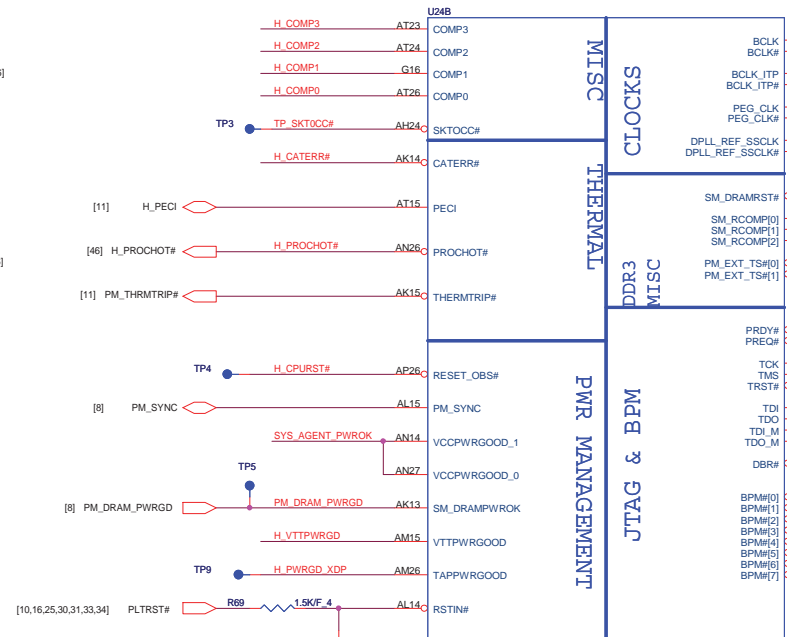
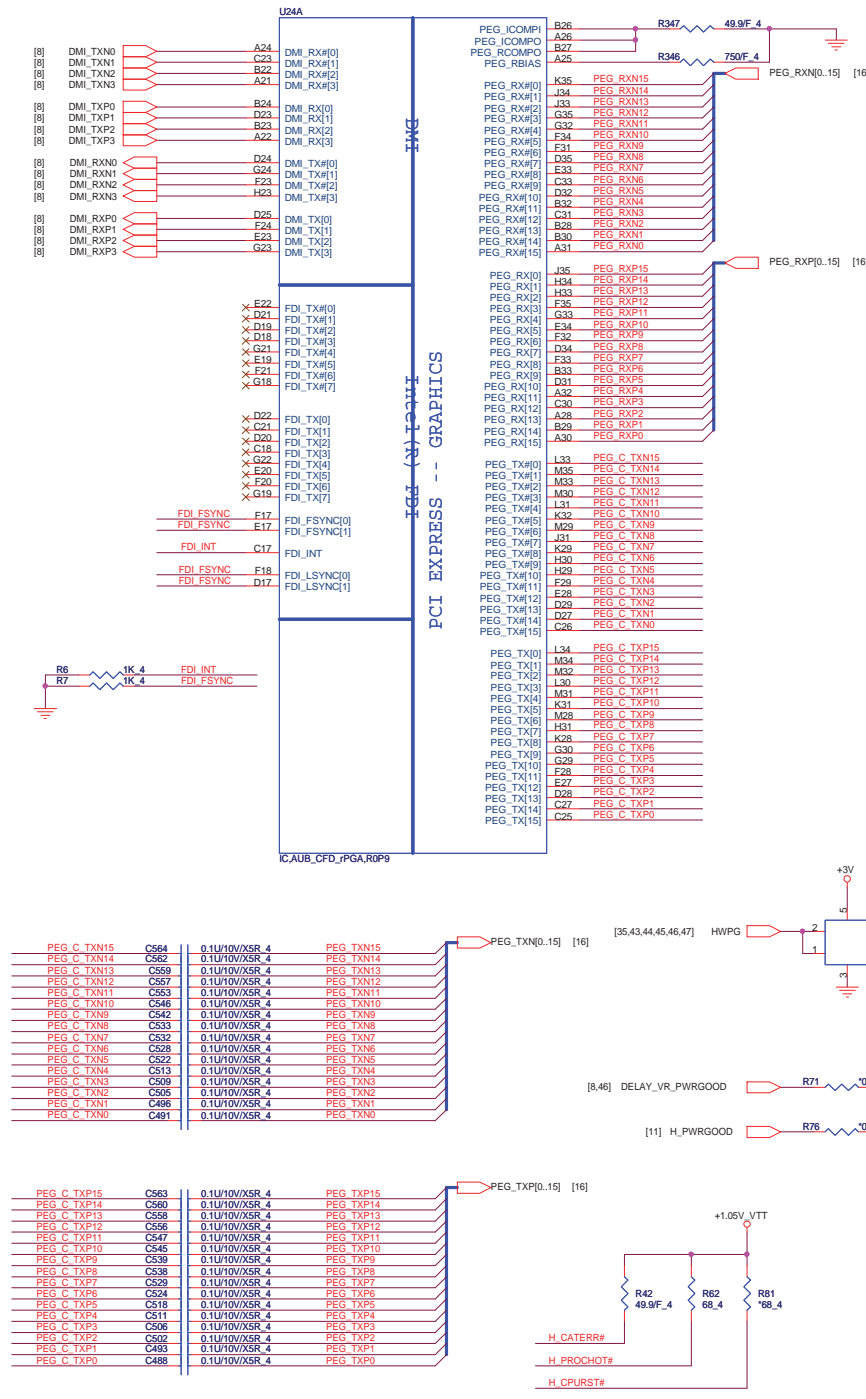
Place each 0.1uF cap as close as possible to each VDD IO pin. Place the 10uF caps on the VDD_IO plane.

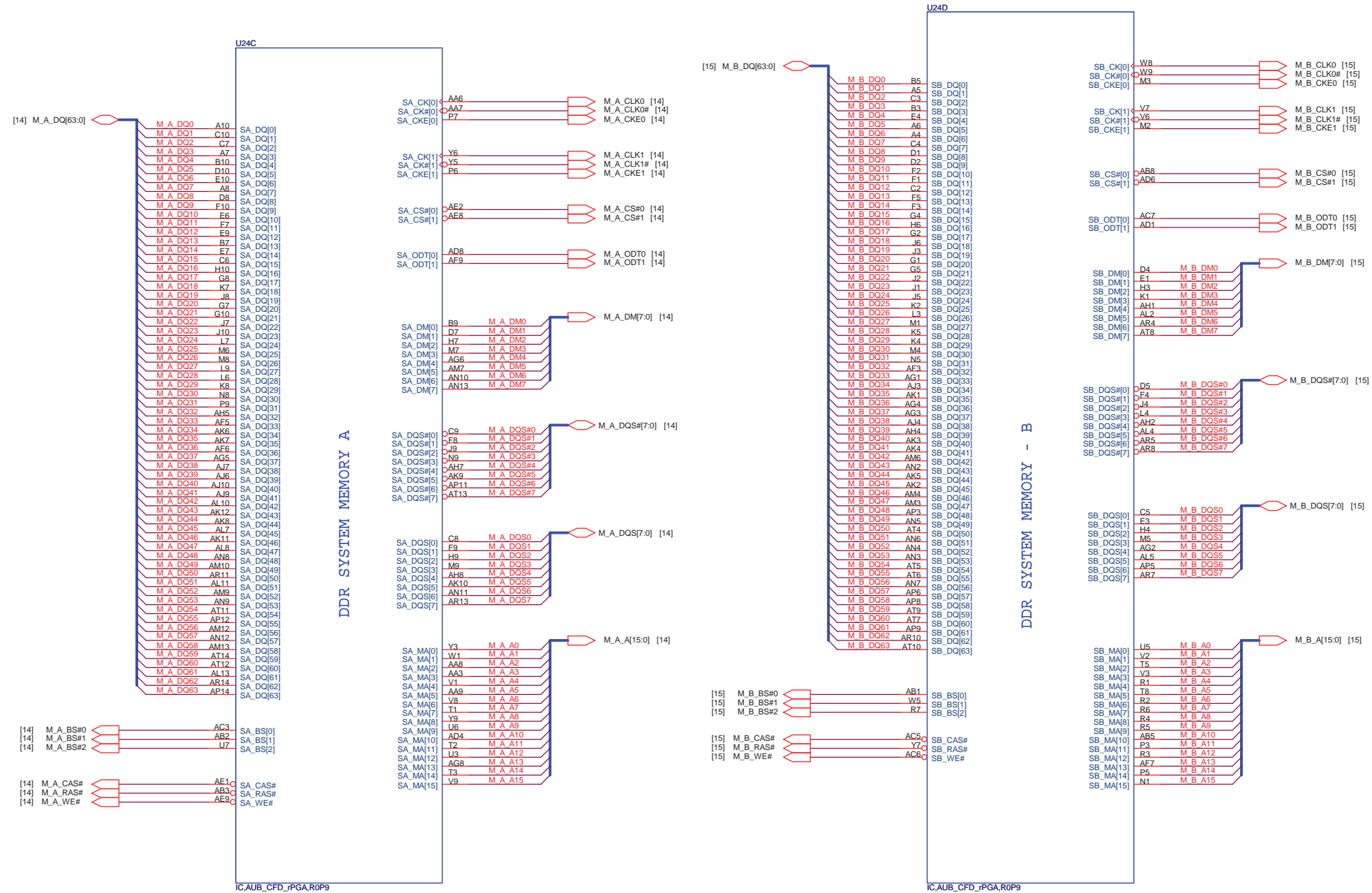
RF request



	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

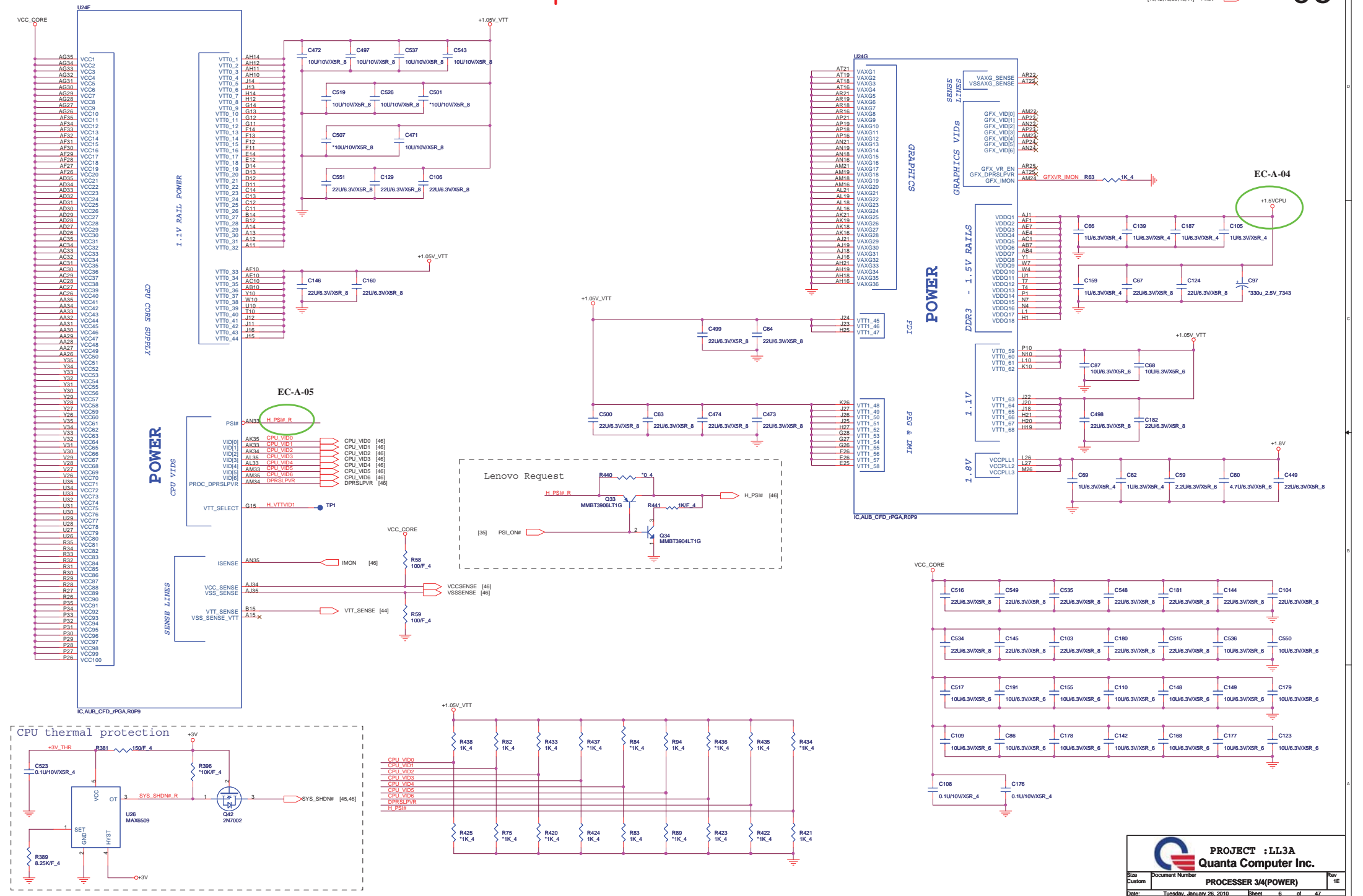


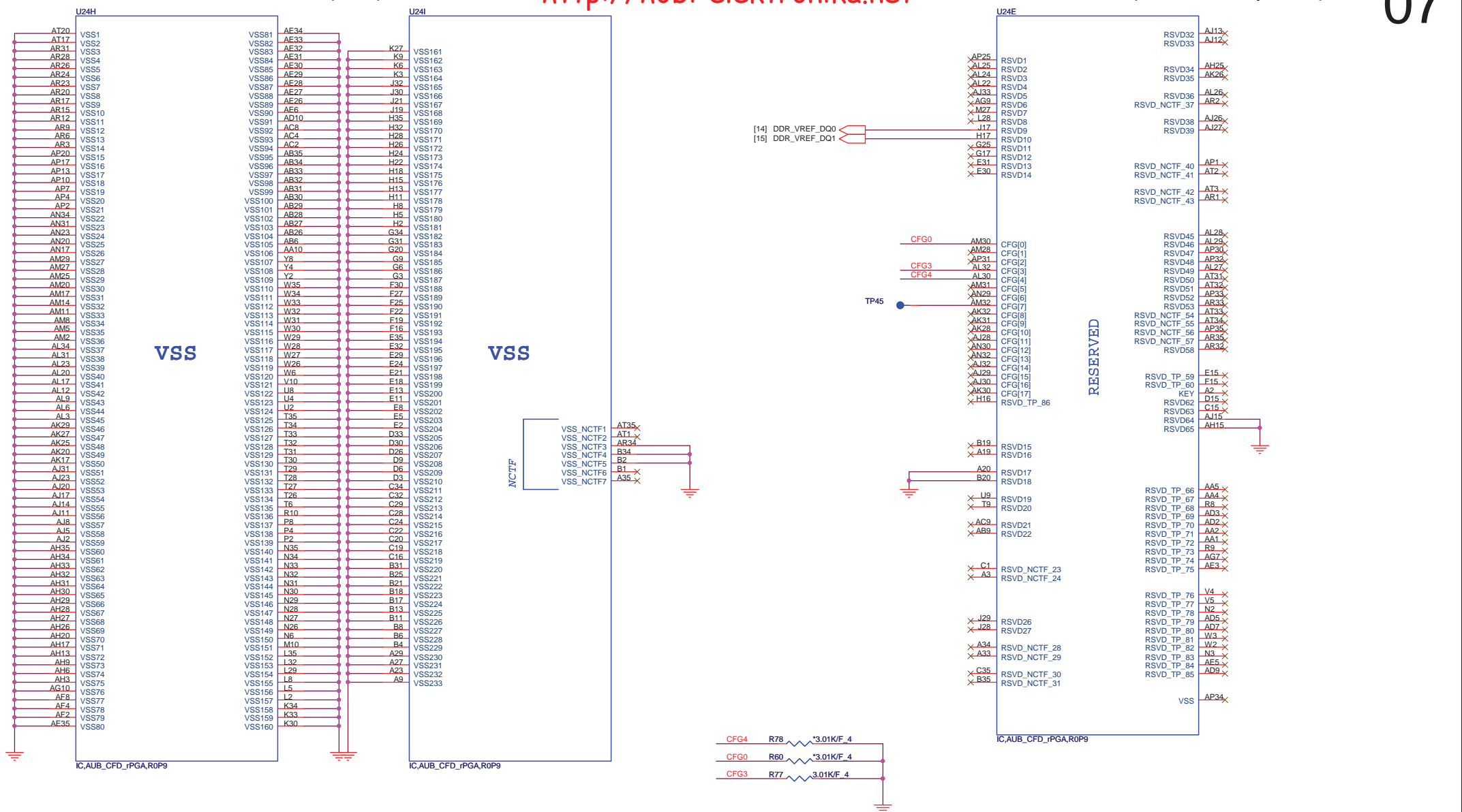




PROJECT : LL3A
Quanta Computer Inc.

Size Custom	Document Number PROCESSOR 2/4(DDR)	Rev 1E
Date:	Tuesday, January 26, 2010	Sheet 5 of 47



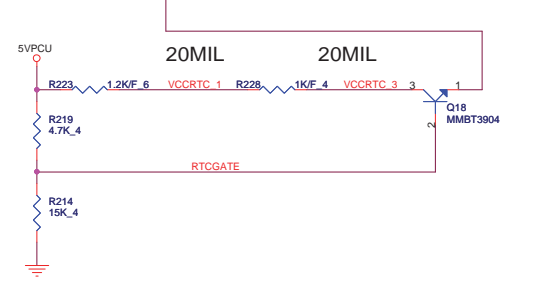
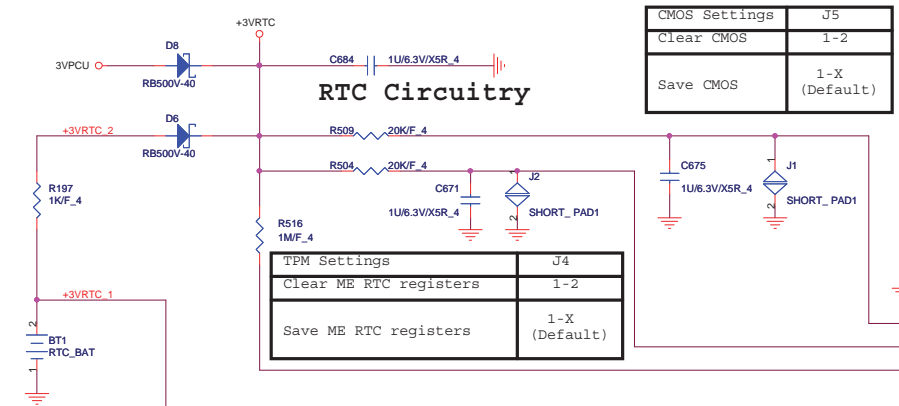


	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

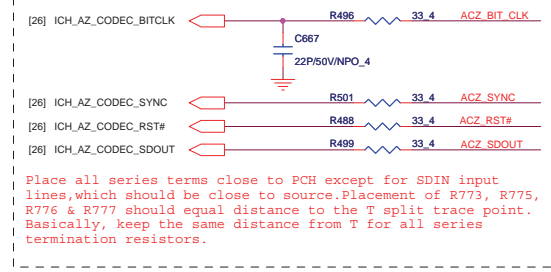
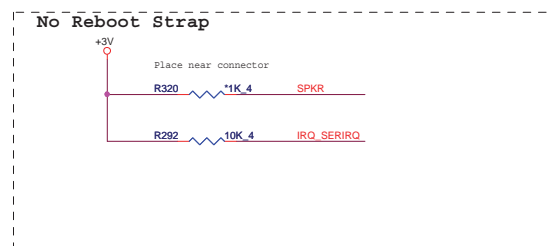
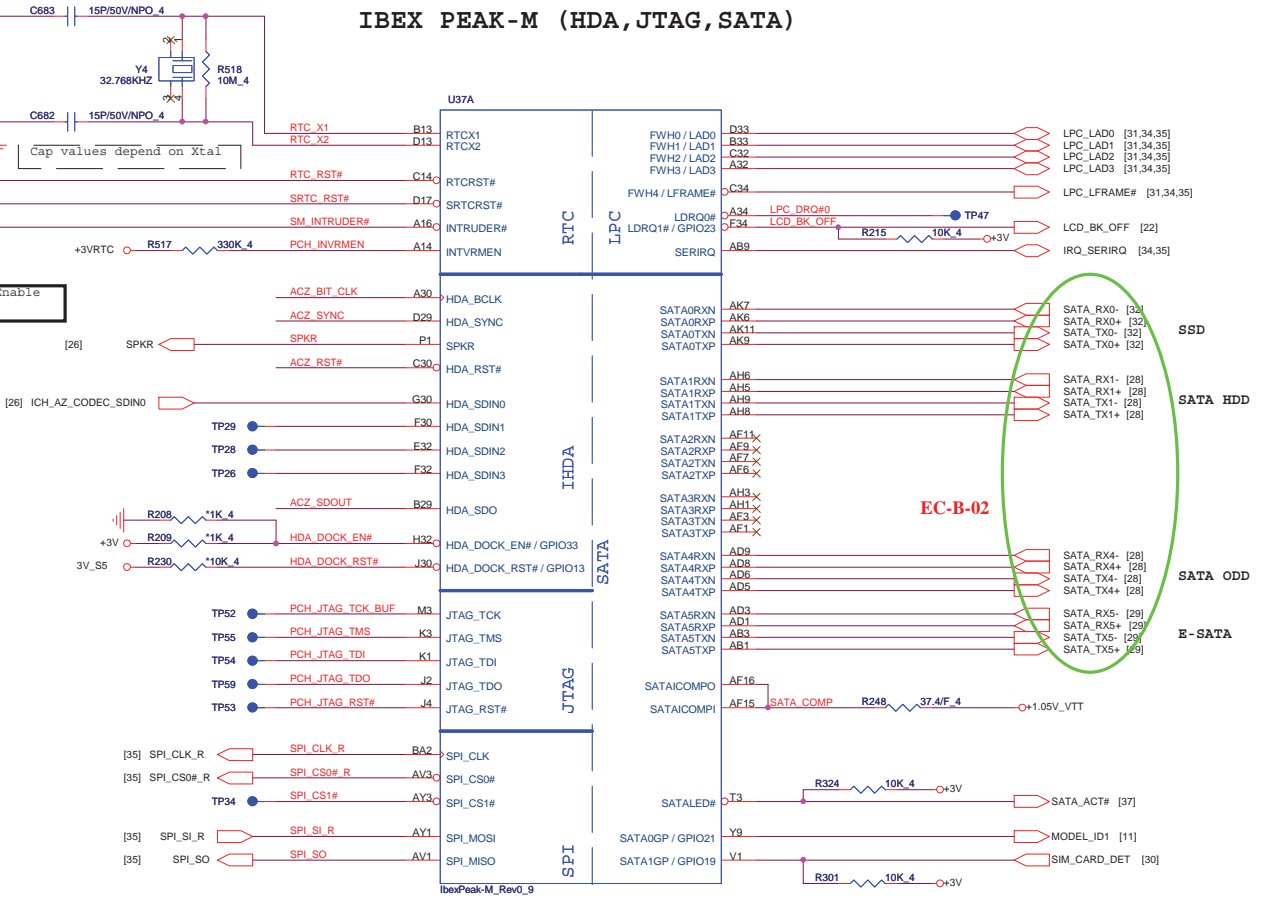
PROJECT :LL3A
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Size Custom Document Number **PROCESSOR 4/4(GND)** Rev 1E

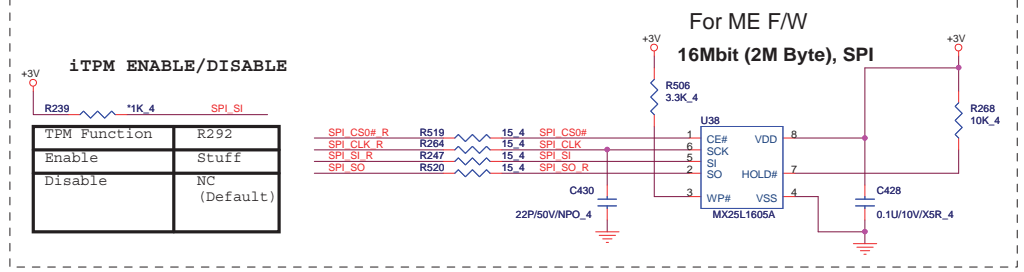
Date: Tuesday, January 26, 2010 Sheet 7 of 47

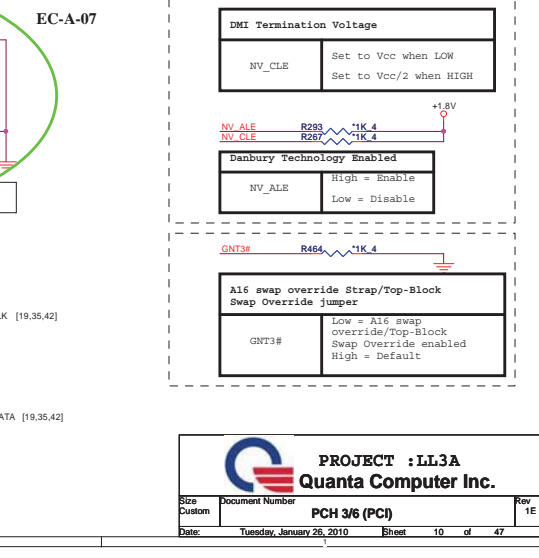
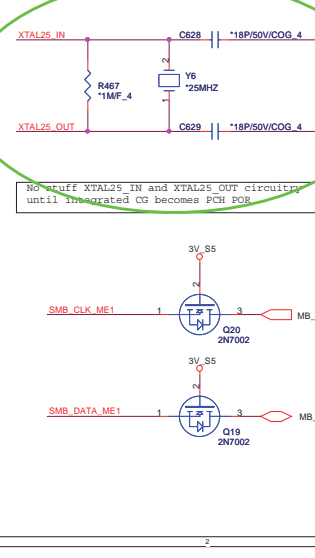
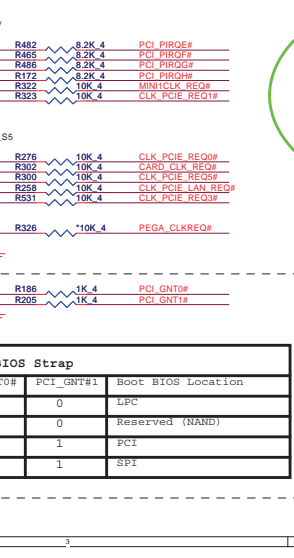
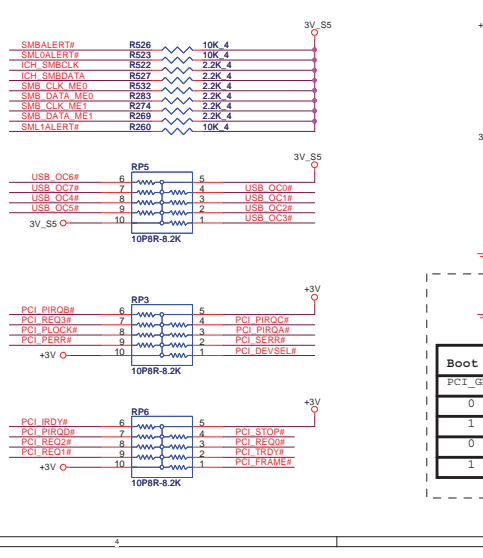
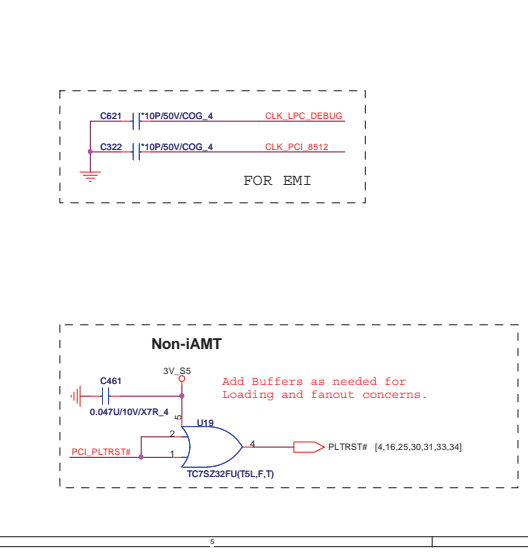
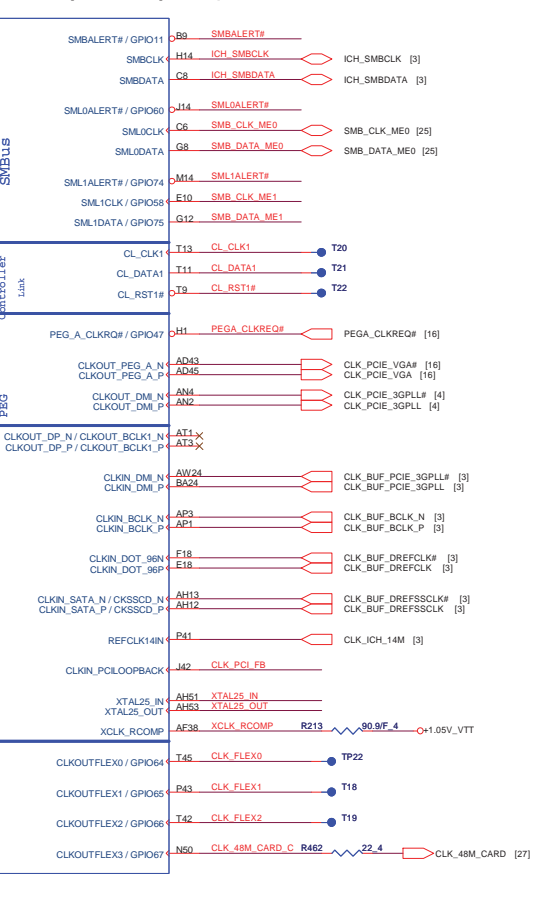
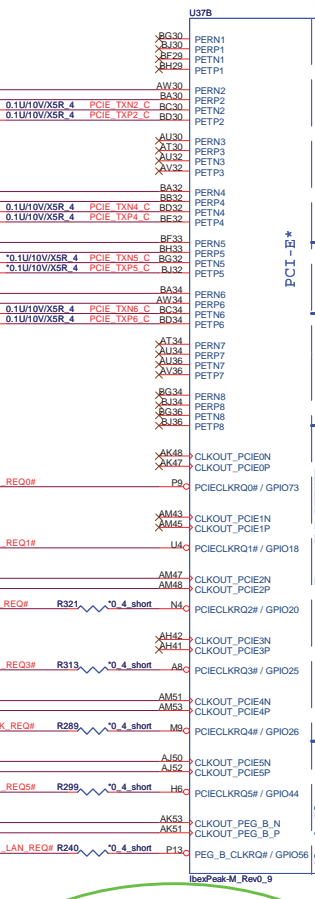
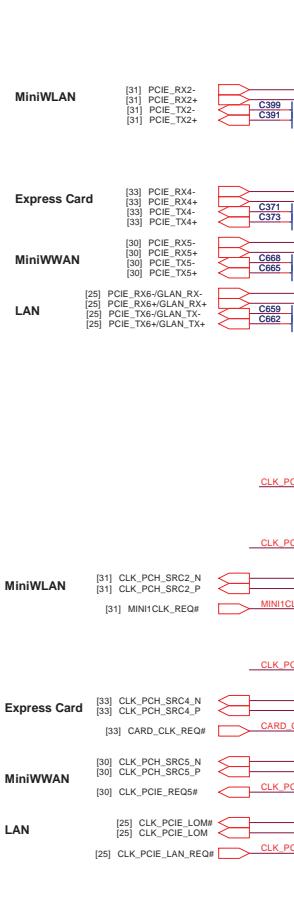
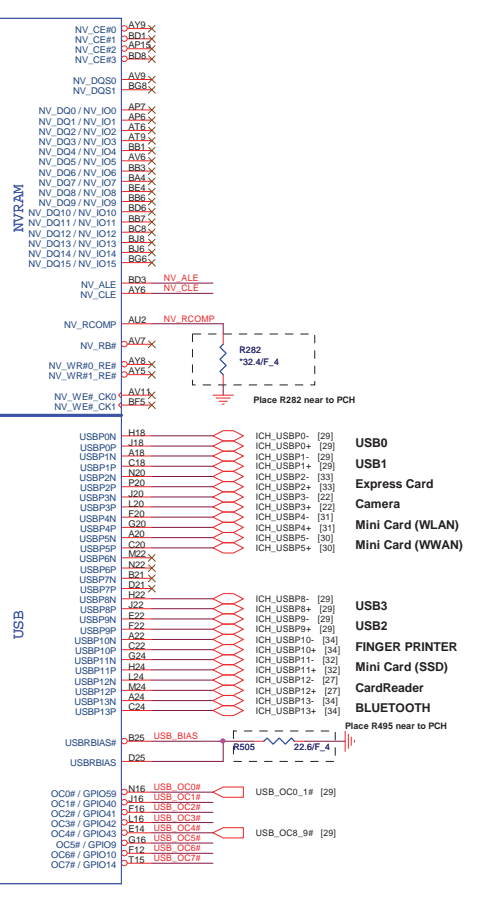
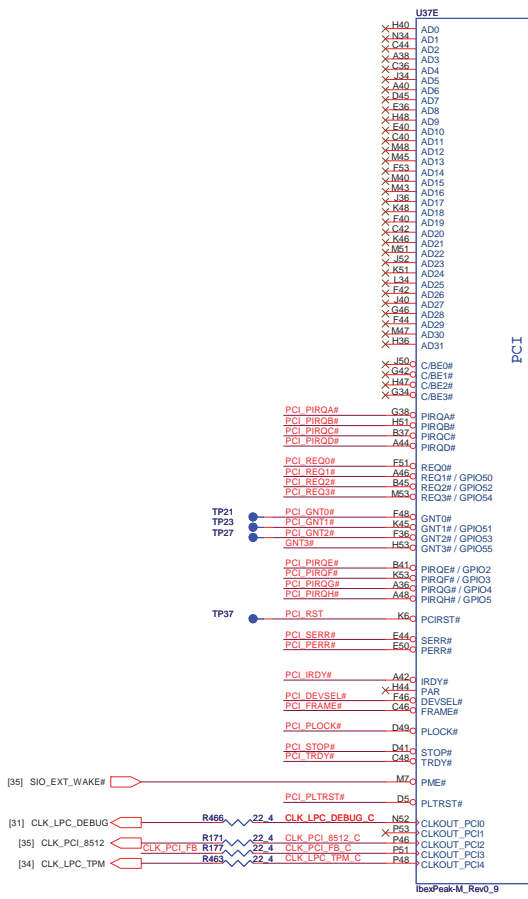


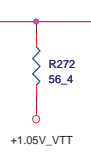
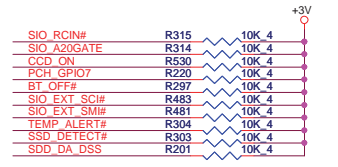
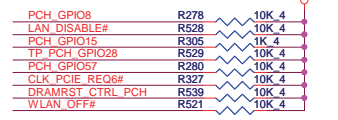
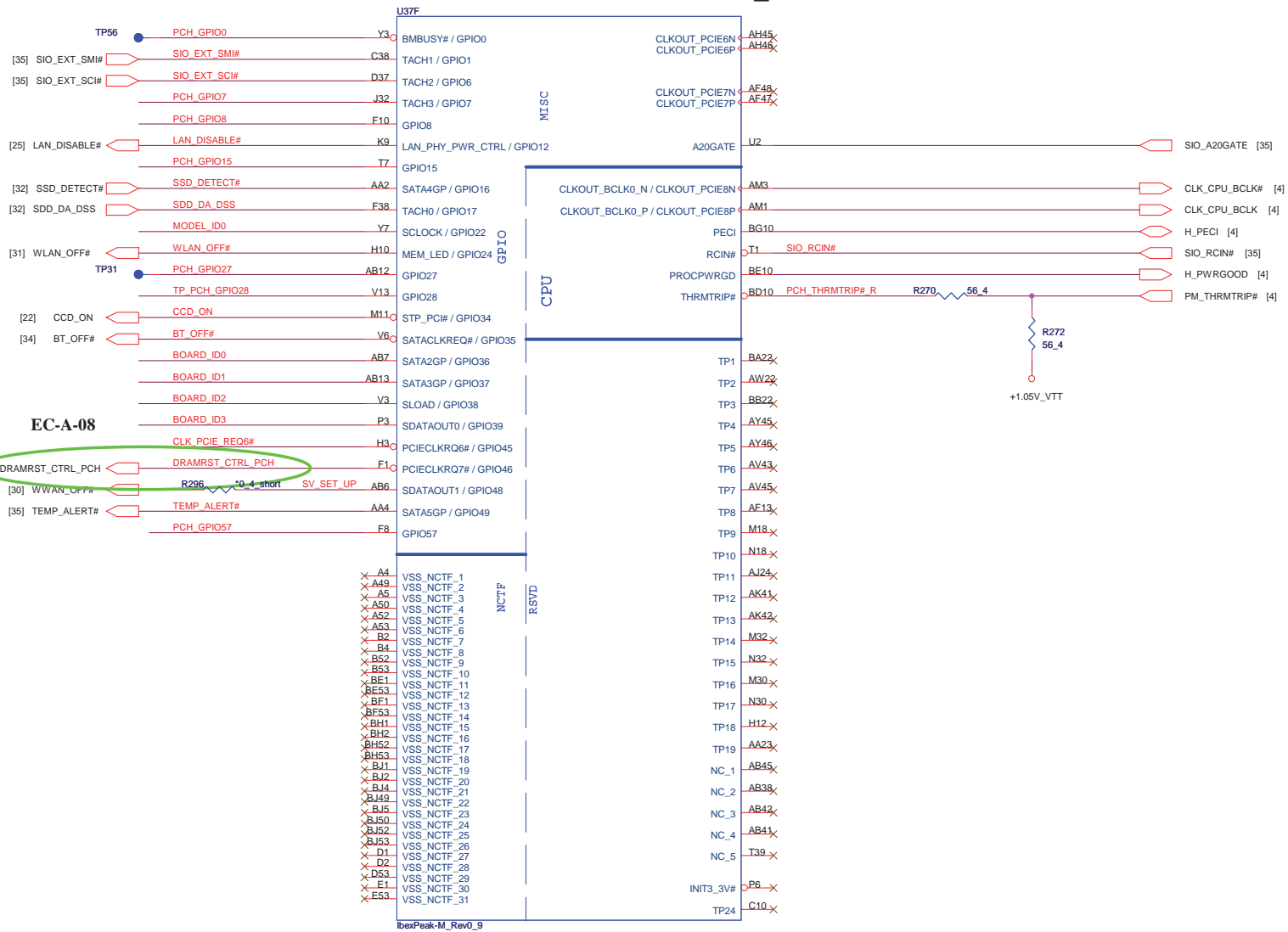
INTVRMEN - Integrated SUS 1.1V VRM Enable
 High - Enable Internal VRs



Place all series terms close to PCH except for SDIN input lines, which should be close to source. Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

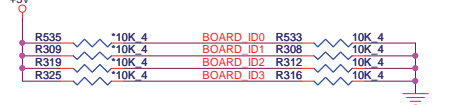






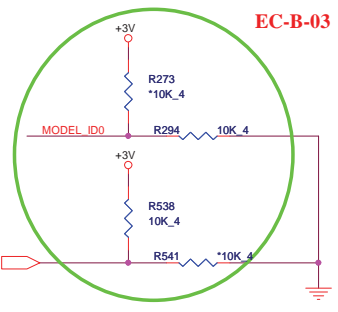
Board ID

Board ID For Function	ID3 GPIO39	ID2 GPIO38	ID1 GPIO37	ID0 GPIO36
SDV	0	0	0	0
SIV	0	0	0	1
SIT	0	0	1	0
SVT	0	0	1	1
SOVP	0	1	0	0



Model ID

Model ID	MODEL_ID0	MODEL_ID1
Default	0	0
LL3/LL3A	0	1
LL5/LL5A	1	0
	1	1

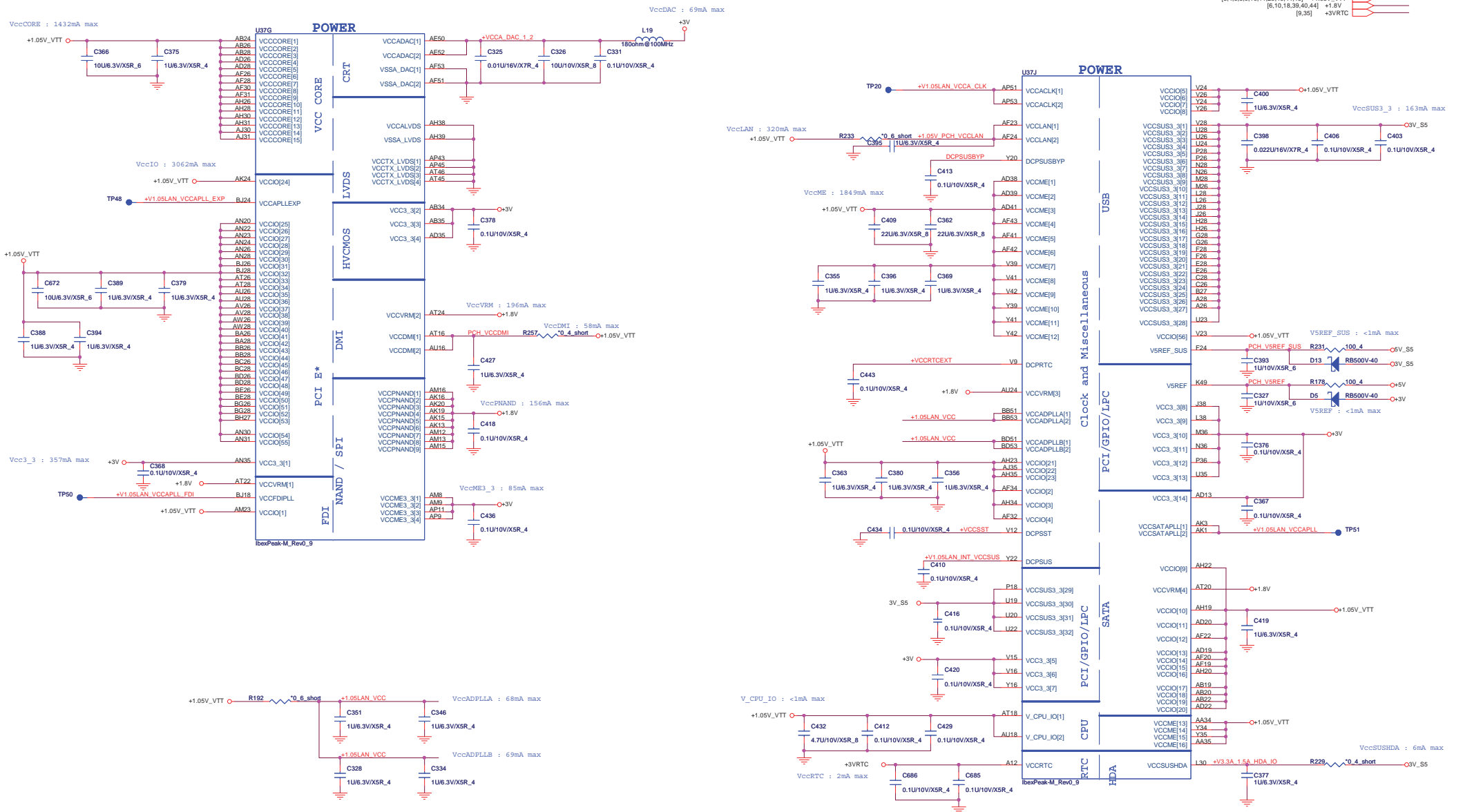


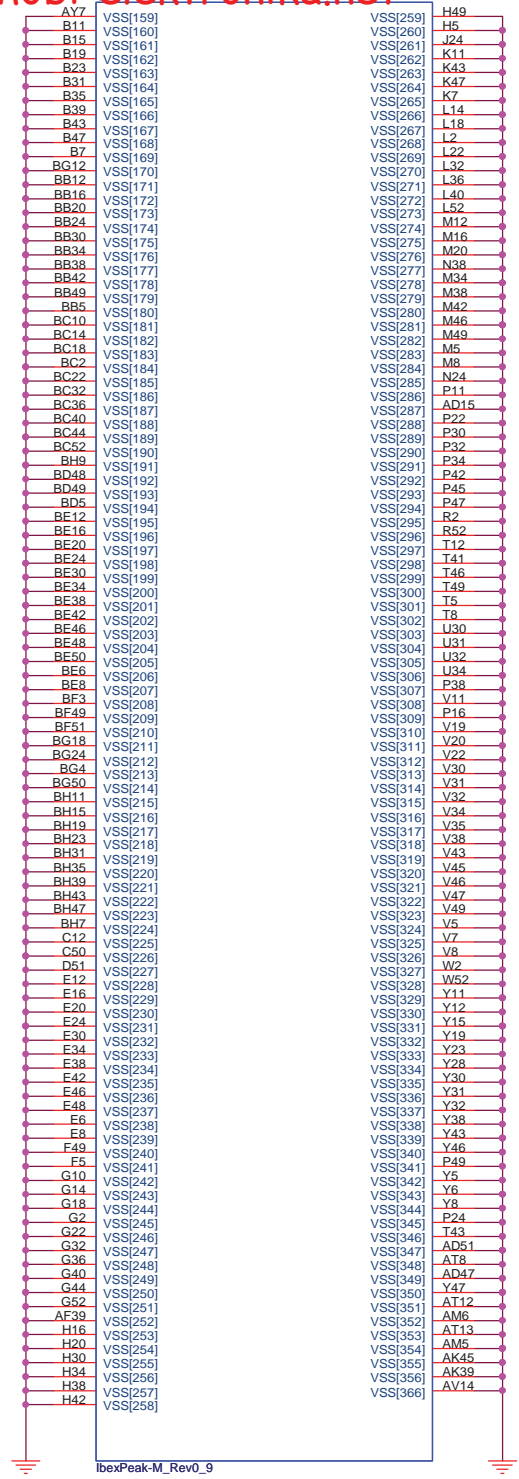
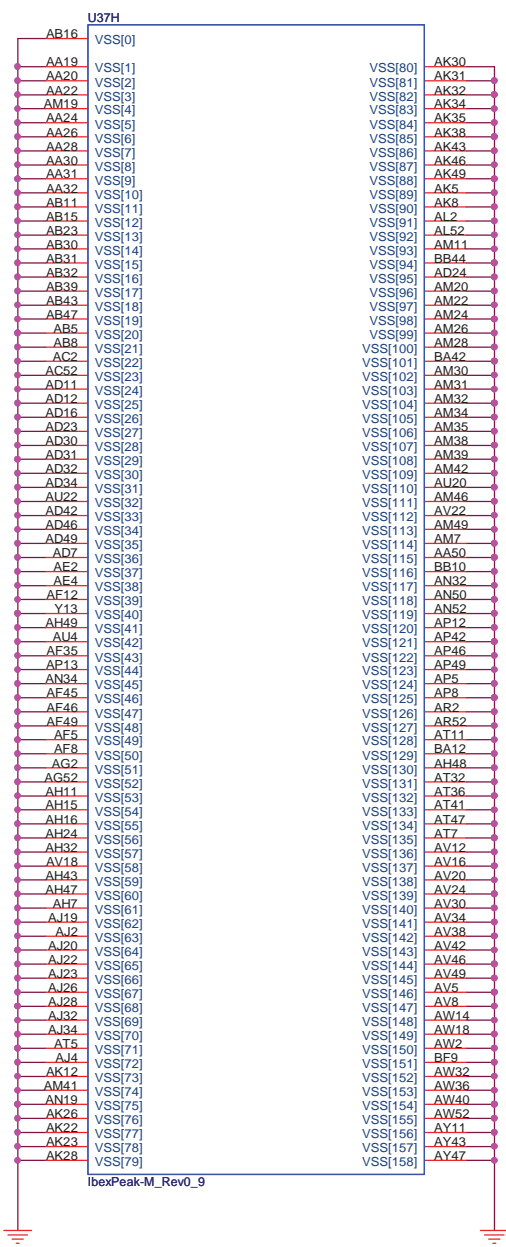
SV_SET_UP 1-X High = Strong (Default)

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Size Custom Document Number PCH 4/6 (GPIO) Rev 1E

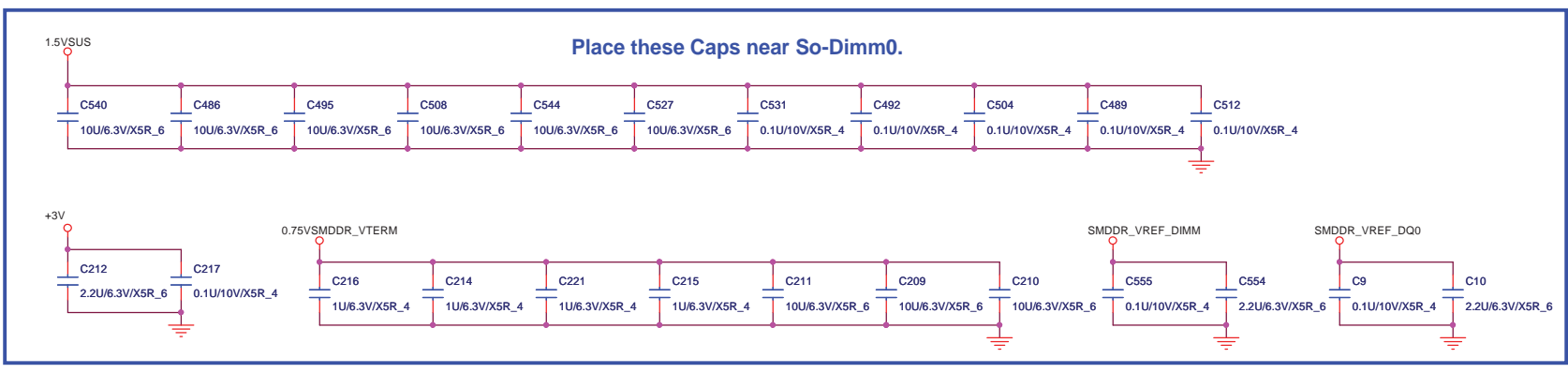
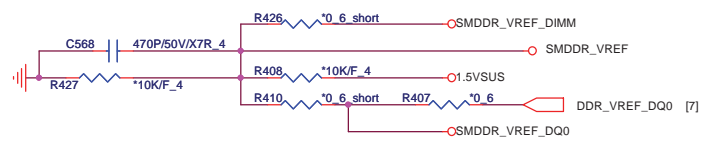
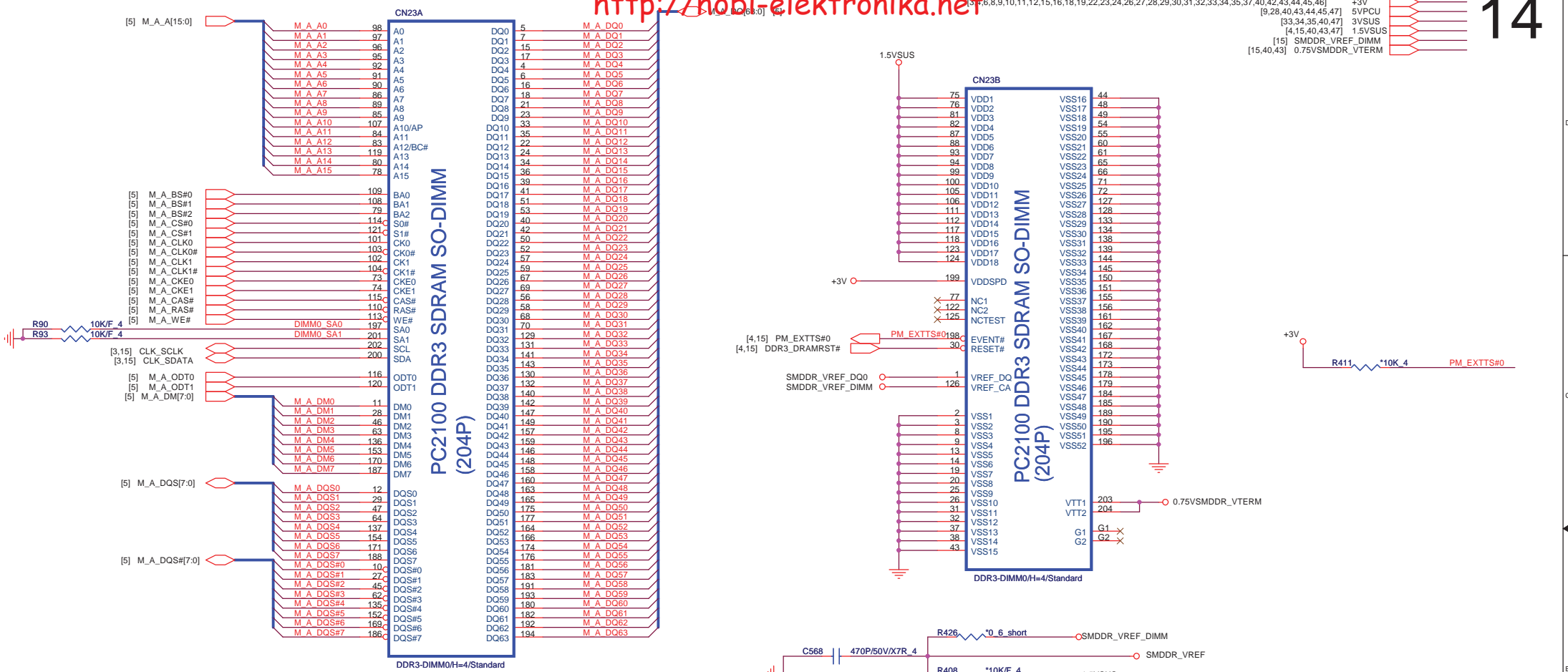
Date: Tuesday, January 26, 2010 Sheet 11 of 47





PROJECT : LL3A
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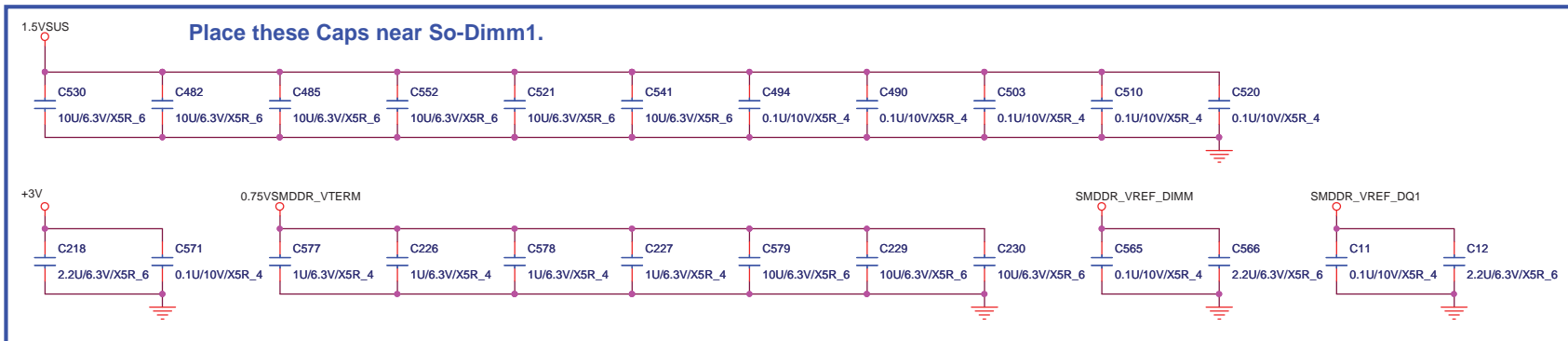
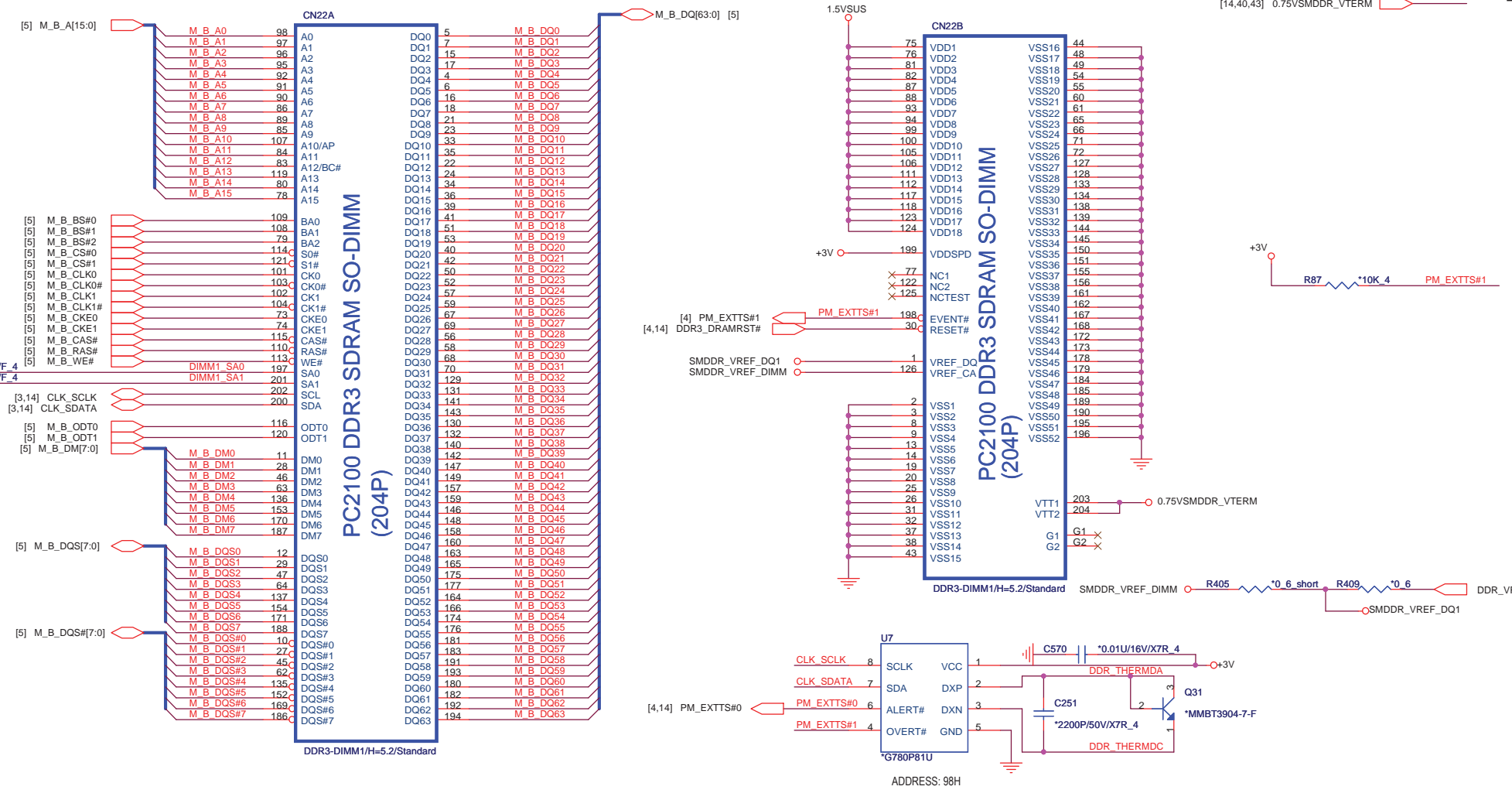
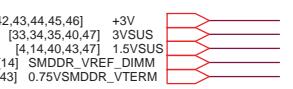
Size Custom	Document Number	PCH 6/6 (GND)	Rev 1E
Date:	Tuesday, January 26, 2010	Sheet 13 of 47	



PROJECT : LL3A
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Size Custom Document Number **DDR3 DIMM-0(H=5.2)** Rev 1E

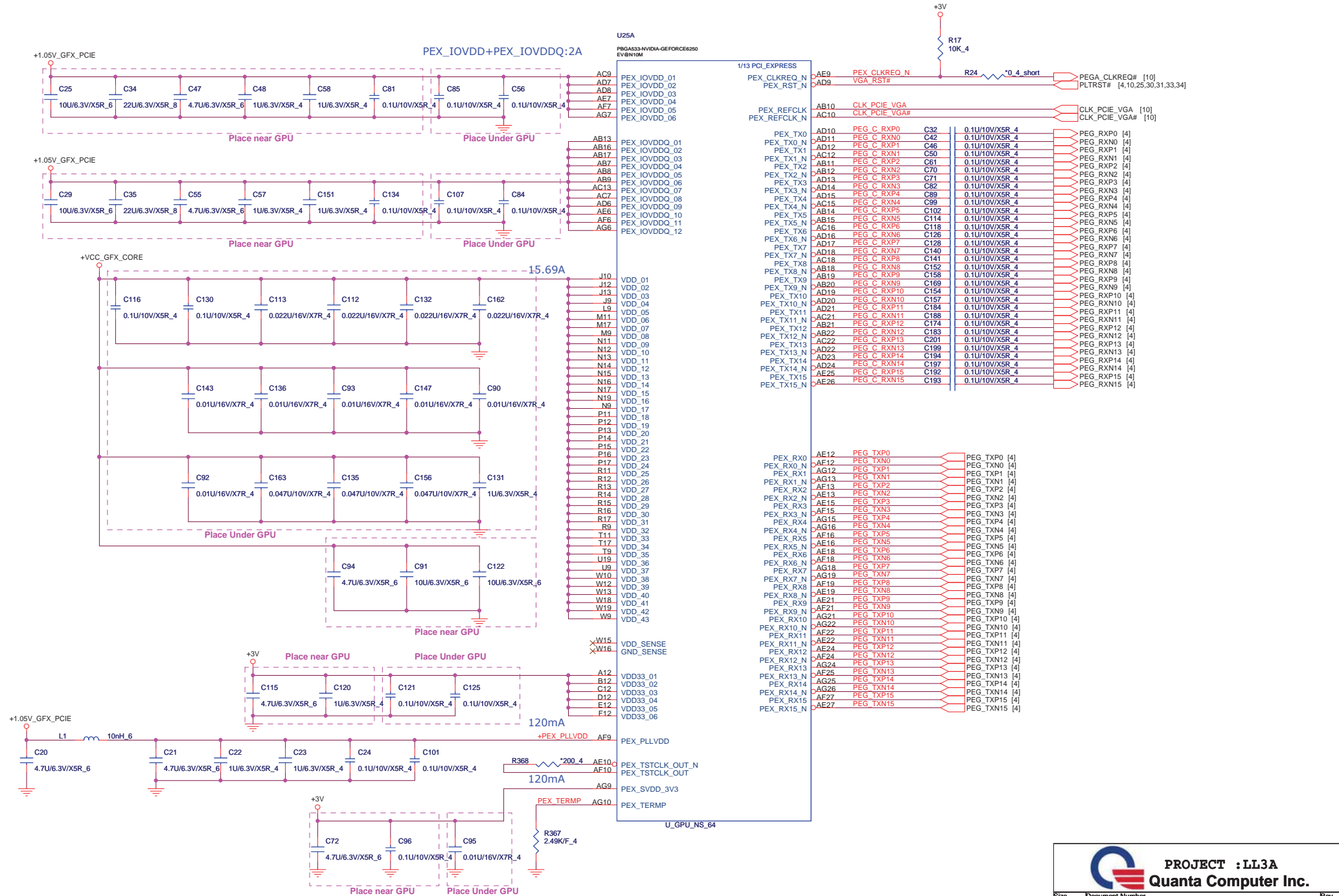
Date: Tuesday, January 26, 2010 Sheet 14 of 47



PROJECT : LL3A
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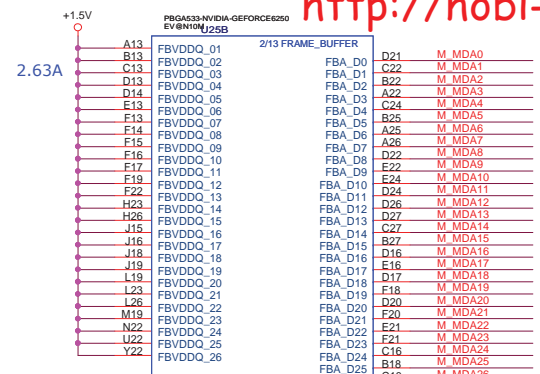
Size Custom | Document Number | **DDR3 DIMM-1(H=9.2)** | Rev 1E

Date: Tuesday, January 26, 2010 | Sheet 15 of 47

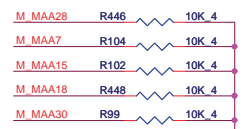
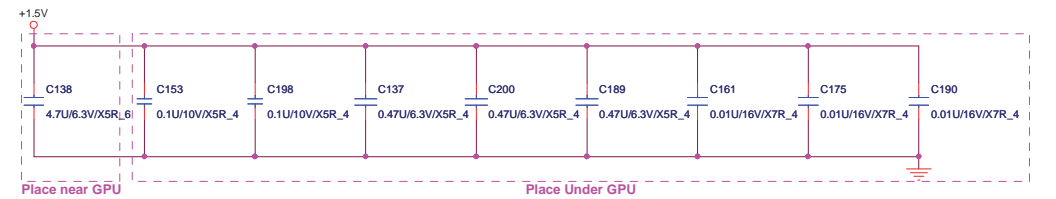
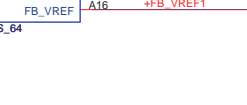
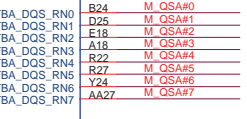
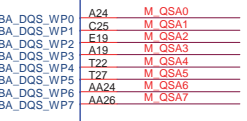
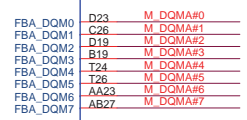
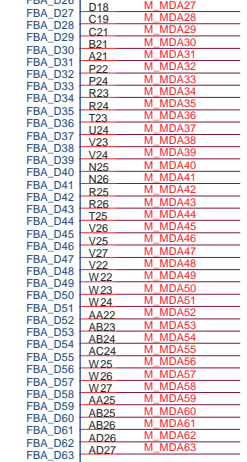
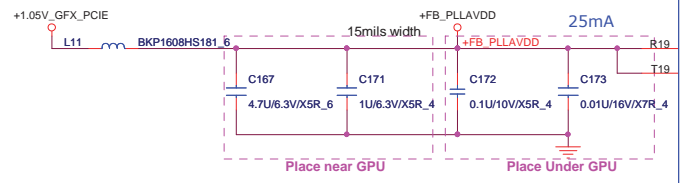
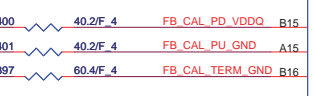
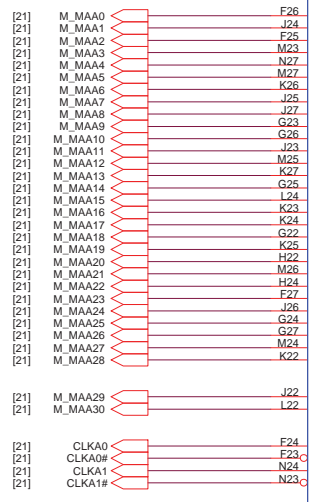


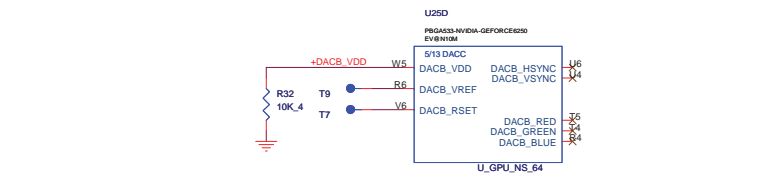
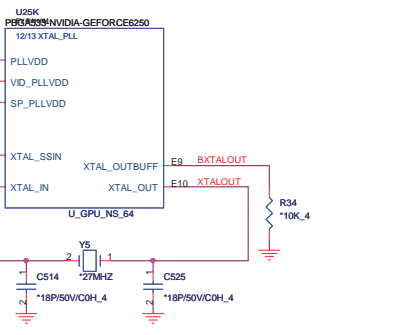
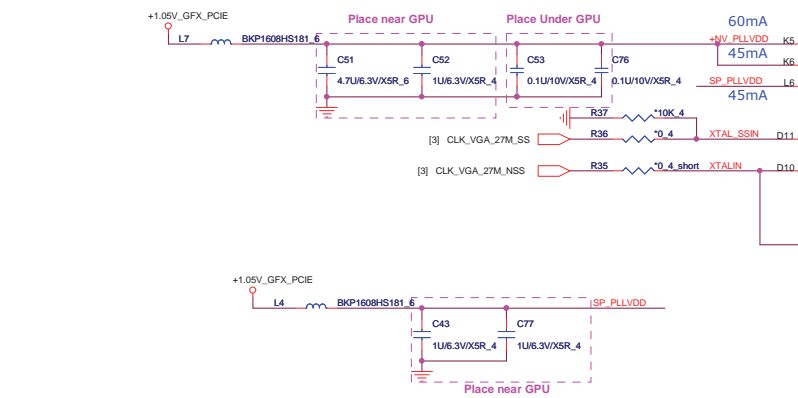
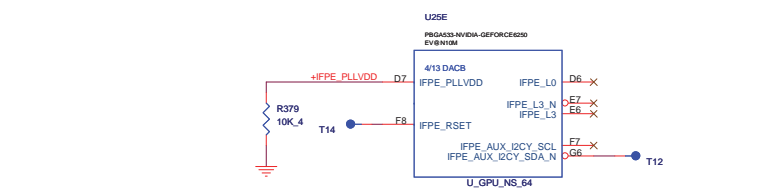
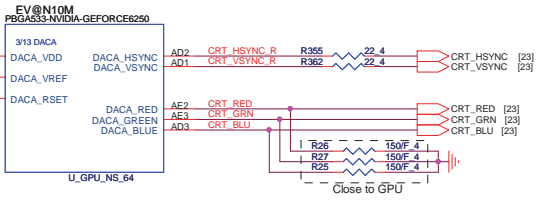
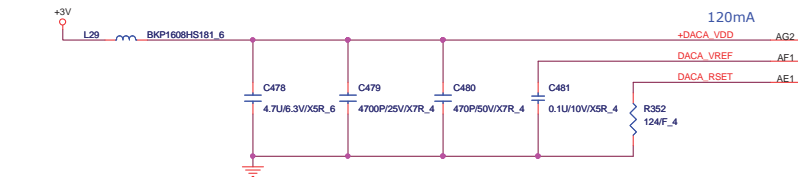
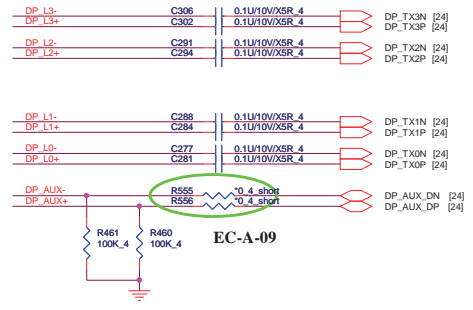
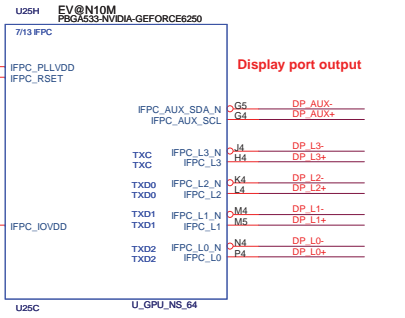
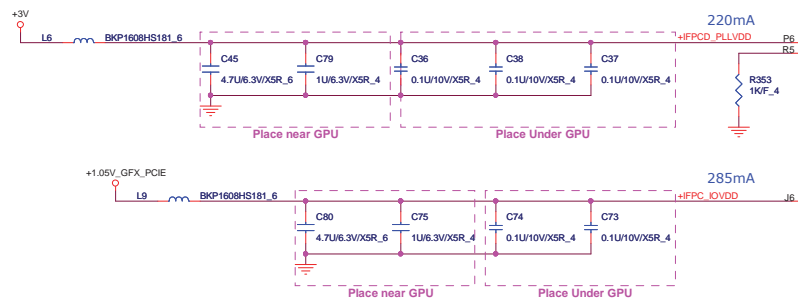
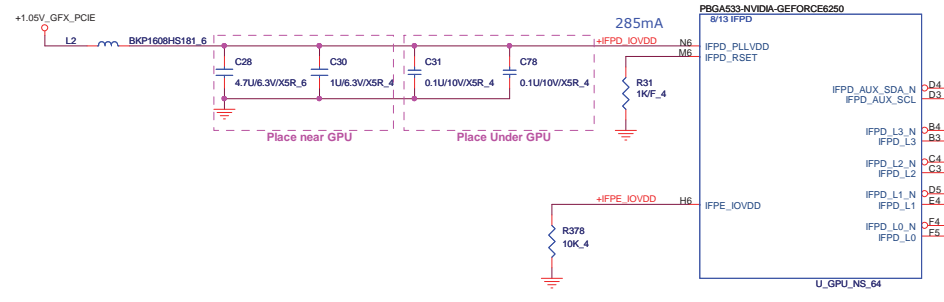
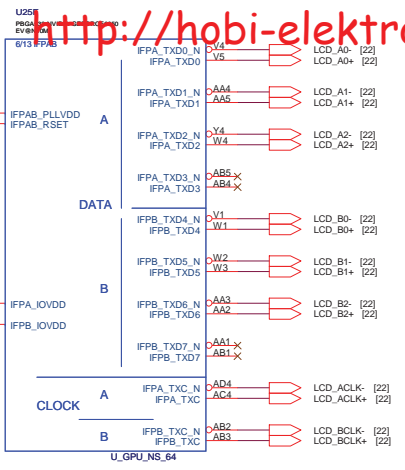
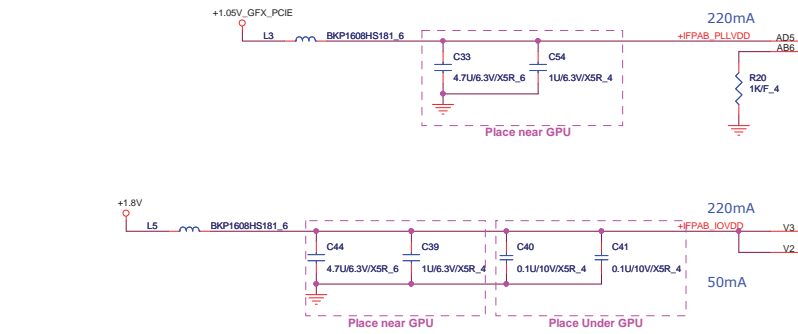
PROJECT : LL3A
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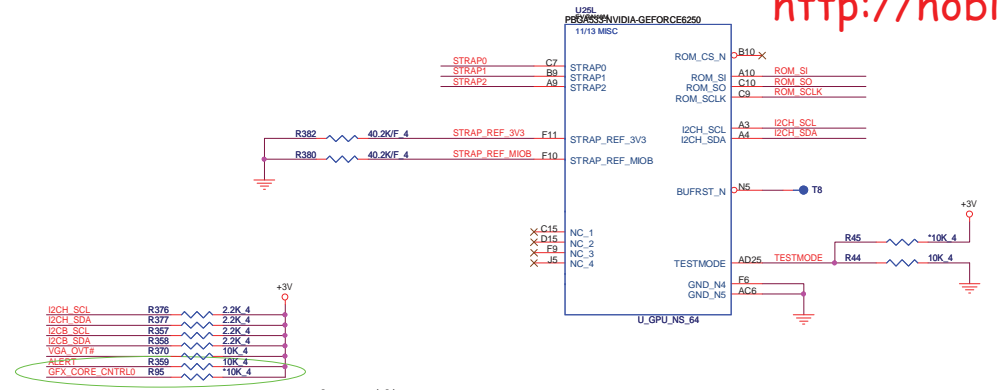
Size	Document Number	Rev
Custom	NV10N(PCIE I/F) 1/5	1E
Date:	Tuesday, January 26, 2010	Sheet 16 of 47



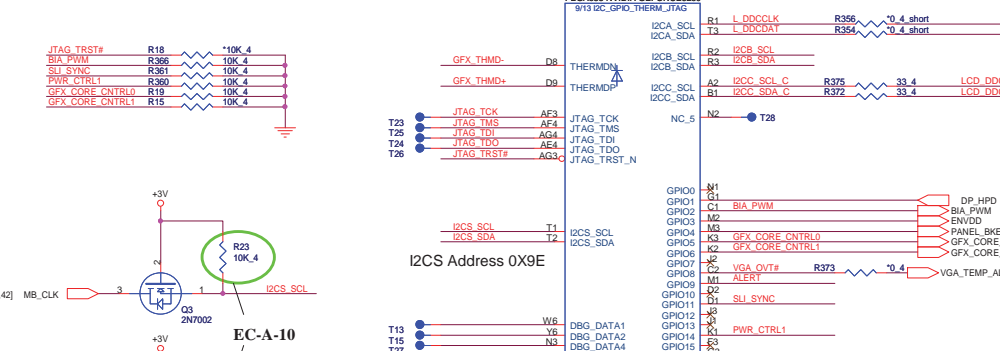
- [21] M_MDA[63..0] M_MDA[63..0]
- [21] M_QSA[7..0] M_QSA[7..0]
- [21] M_QSA#[7..0] M_QSA#[7..0]
- [21] M_DQMA#[7..0] M_DQMA#[7..0]



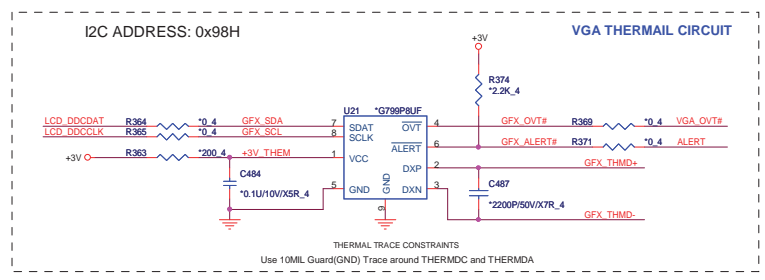
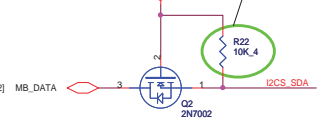




Reservverd as nVidia request



I2CS Address 0X9E



THERMAL TRACE CONSTRAINTS
Use 10MIL Guard(GND) Trace around THERMOC and THERMDA

LL3A STRAP FUNCTION MAPPING

USER[3:0]:	1111	EDID is used
3GIO_PADCFG[3:0]:	0001	NoteBook
PCI_DEVID[3:0]:	0001	
SUB_VENDOR:	0	No Vedio BIOS ROM
SLOT_CLK_CLG:	1	GPU AND MCH USE COMMON REF CLOCK
PEX_PLL_EN_TERM:	0	DISABLE PEX_PLL TERMINATION
RAMCFG[3:0]:	0010 AND 0011	
XCLK_417:	0	277MHz (Default)
FB_0_BAR_SIZE:	0	256MB (Default)
SMB_ALT_ADDR:	0	0x9E (Default)
VGA_DEVICE:	1	VGA device (Default)

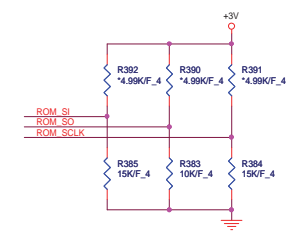
ROM_SI	RAMCFG LSIT:	
PD R385:20K/F	0011	SAMSUNG K4W1G1646E-HC12 64M16b * 4PCS
PD R385:15K/F	0010	HYNIX H5TQ1G63BFR-12C 64M16b * 4PCS

GPIO ASSIGNMENTS

GPIO	NB9X	N10X	I/O	ACTIVE	Function Description
0	General Purpose	General Purpose	I/O	N/A	
1	HPD-C	HPD-C	I	N/A	Hot Plug Detect for IFP Link C
2	LCD0_BL_PWM	LCD0_BL_PWM	O	H	Panel Backlight Brightness Control (PWM Capable)
3	LCD0_VDD	LCD0_VDD	O	H	Panel Power Enable
4	LCD0_BL_PWM	LCD0_BL_PWM	O	H	Panel Backlight ON/OFF
5	GPU_VID0	GPU_VID0	O	N/A	GPU_VID0
6	GPU_VID1	GPU_VID1	O	N/A	GPU_VID1
7	GPU_VID2/MEM_VID	GPU_VID2	O	N/A	GPU_VID2
8	OVERT	OVERT	I/O	L	Thermal Over Temperature
9	FAN_PWM/ALERT	ALERT	I/O	L	Thermal Alert (PWM Capable)
10	MEM_VREF	MEM_VREF	O	N/A	Memory VREF Switch
11	SLI_SYNC	SLI_SYNC	I/O	L	SLI_SYNC0
12	AC_DET	PWR_LEVEL (in)	I	N/A	Power Level Detect
13	PWR_CTRL0	MEM_VID (out)	O	L	MEM_VID0
14	PWR_CTRL1	PWR_CTRL1	O	N/A	Power Supply Control
15	HPD-E	HPD-E	I	N/A	Hot Plug Detect for IFP Link E
16	DVL_MODE1	FAN_PWM(out)	O		Fan PWM Control
17	HDMI_DETECT0	Reserved	N/A		
18	DVL_MODE1	Reserved	N/A		
19	HDMI_DETECT1	HPD-D	I	N/A	Hot Plug Detect for IFP Link D

Straps	NB9X	N10X	Function Description
ROM_SO	XCLK_277 TVMODE(2) TVMODE(1) TVMODE(0)	XCLK_277 TVMODE(2) TVMODE(1) TVMODE(0)	55nm PU 5K/F ohm 40nm PD 10K/F ohm
ROM_SCLK	PCI_DEVID_EXT SUB_VENDOR SLOT_CLK_CFG PEX_PLL_EN_TERM	PCI_DEVID_EXT SUB_VENDOR SLOT_CLK_CFG PEX_PLL_EN_TERM	55nm/40nm PD 15K/F ohm
ROM_SI	RAMCFG(3) RAMCFG(2) RAMCFG(1) RAMCFG(0)	RAMCFG(3) RAMCFG(2) RAMCFG(1) RAMCFG(0)	Hynix PD 15K/F ohm Samsung PD 20K/F ohm
Strap 2	PCI_DEVID(3) PCI_DEVID(2) PCI_DEVID(1) PCI_DEVID(0)	PCI_DEVID(3) PCI_DEVID(2) PCI_DEVID(1) PCI_DEVID(0)	55nm PU 25K/F ohm 40nm/GS PU 10K/F ohm 40nm/GE PU 5K/F ohm 40nm/NS PU 25K/F ohm
Strap 1	3GIO_PADCFG(3) 3GIO_PADCFG(2) 3GIO_PADCFG(1) 3GIO_PADCFG(0)	3GIO_PADCFG(3) 3GIO_PADCFG(2) 3GIO_PADCFG(1) 3GIO_PADCFG(0)	40nm/NS PU 34.9K/F ohm
Strap 0	USER(3) USER(2) USER(1) USER(0)	USER(3) USER(2) USER(1) USER(0)	

PCI_DEVID[4] / SUBVENDOR



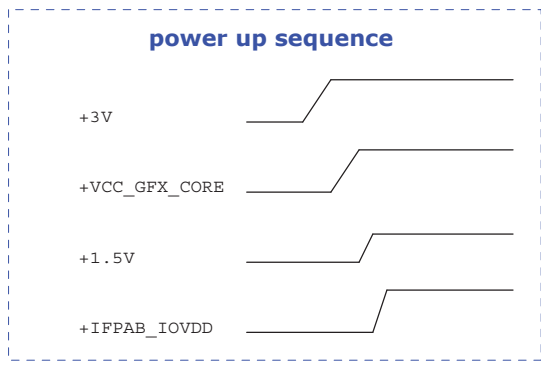
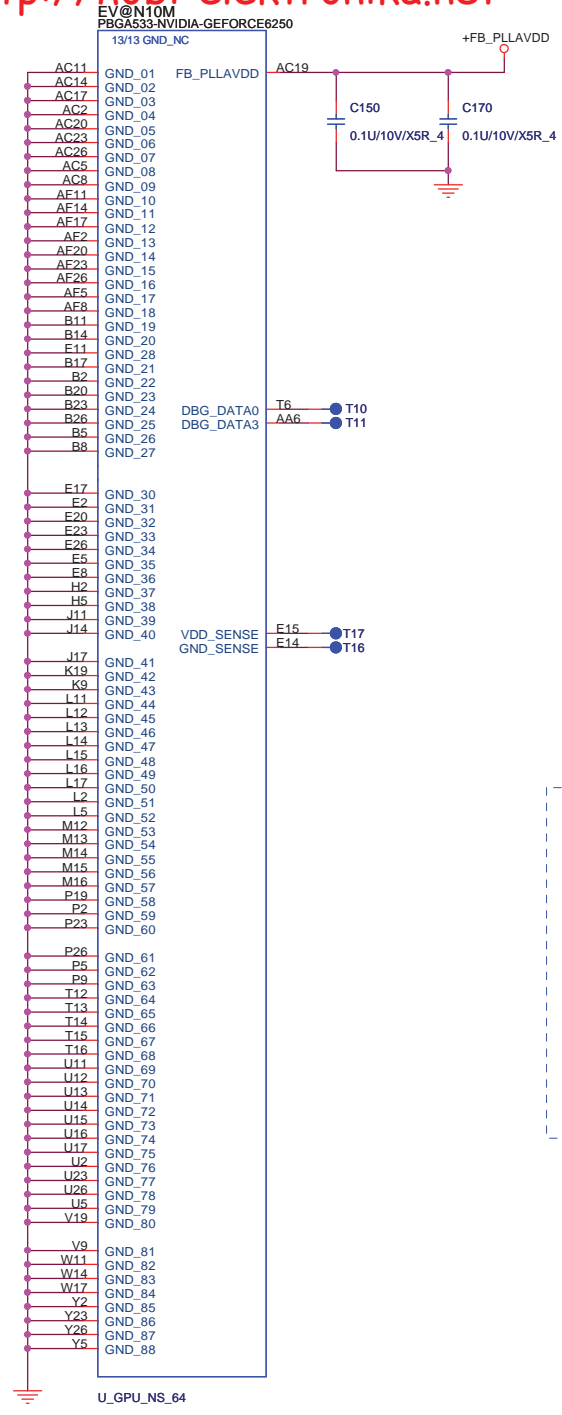
Logical Strap Bit Mapping


Straps	PU	PD
	5K	1000
	10K	1001
	15K	1010
	20K	1011
	25K	1100
	30K	1101
	35K	1110
	45K	1111

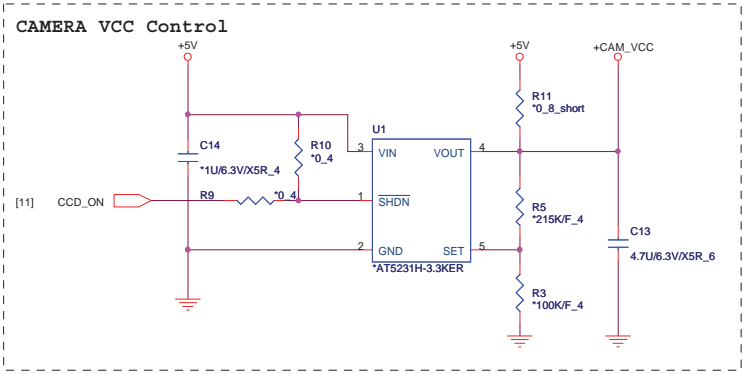
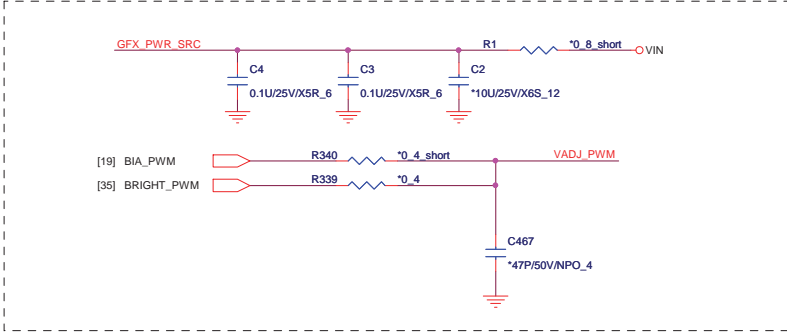
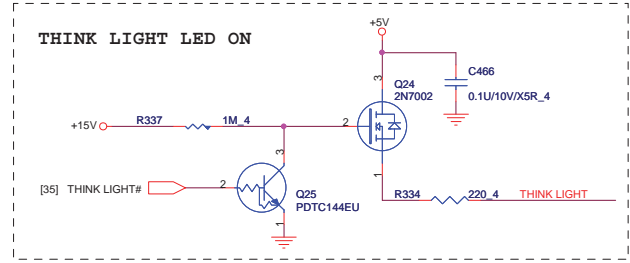
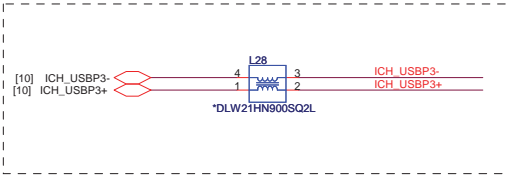
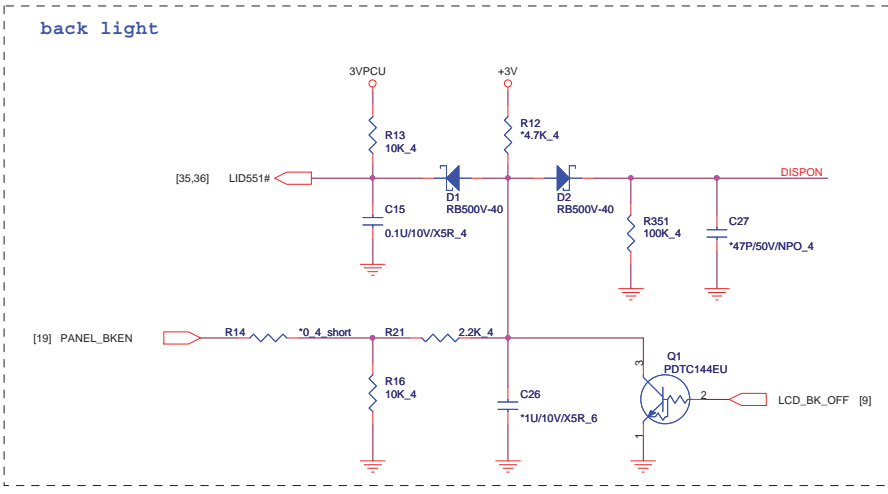
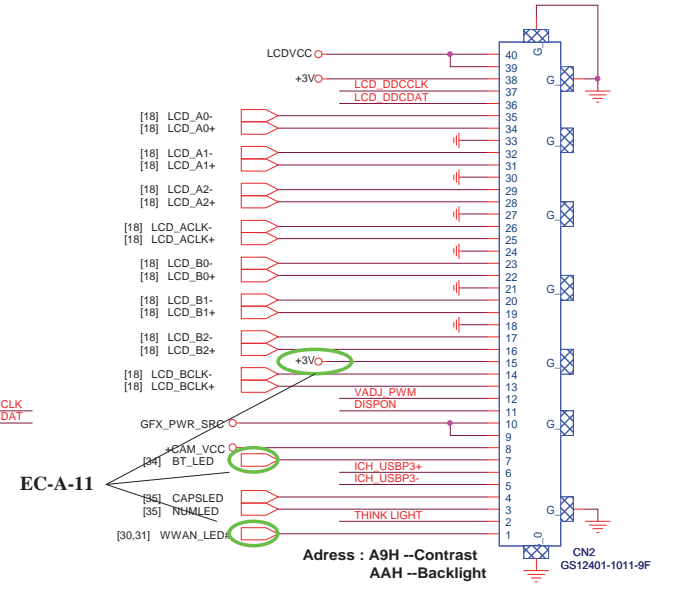
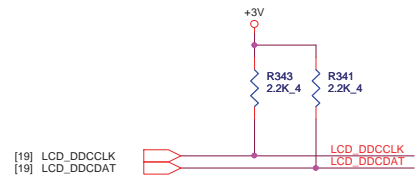
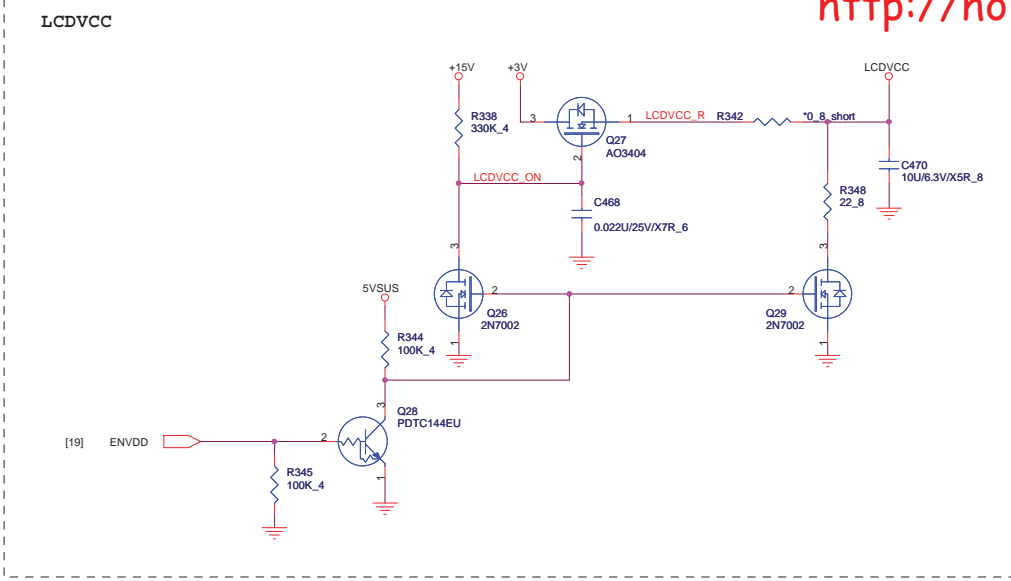
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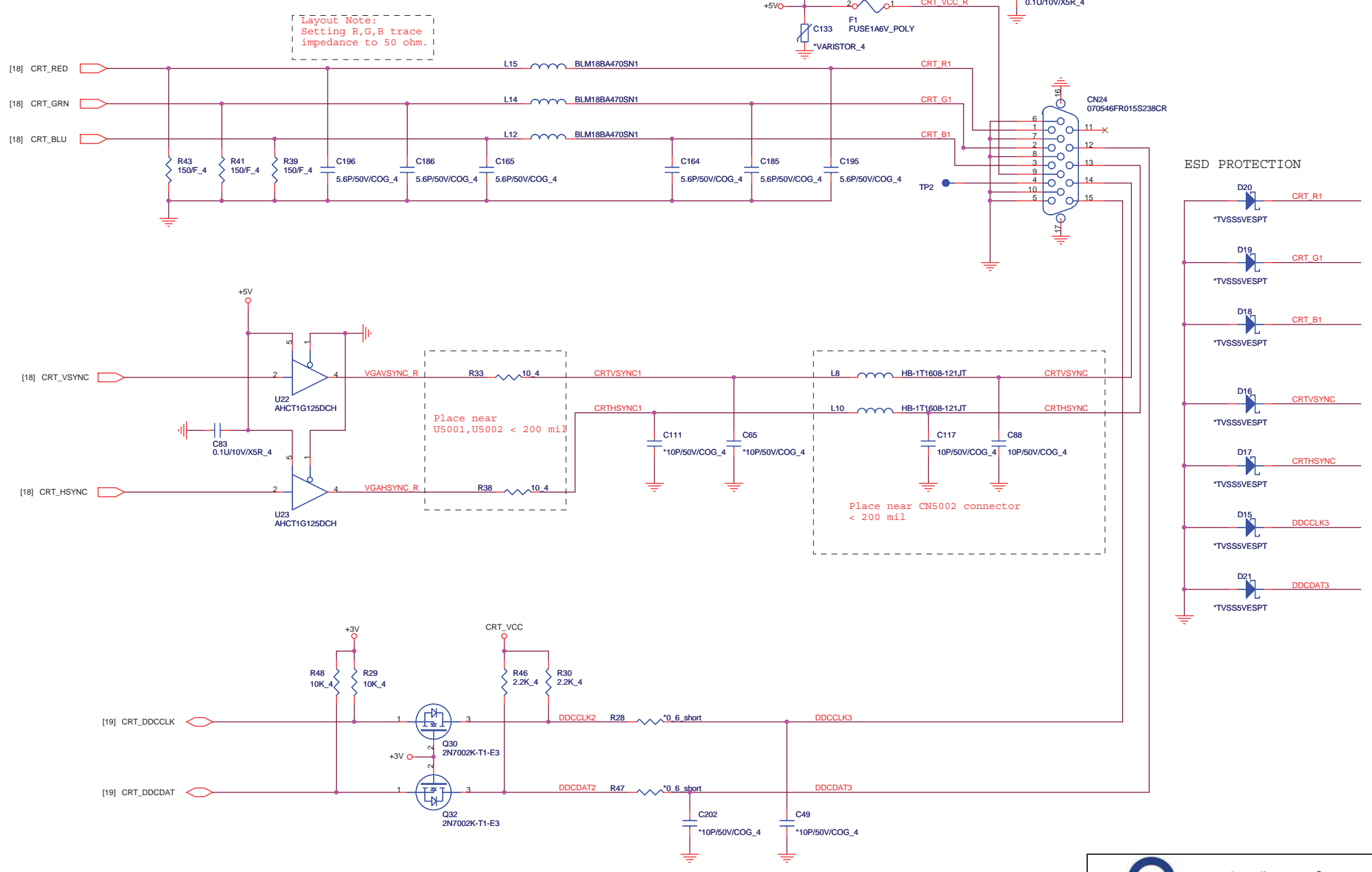
Size C Document Number **N10M (GPIO & STRAPS) 4/5** Rev 1E

Date: Tuesday, January 26, 2010 Sheet 19 of 47



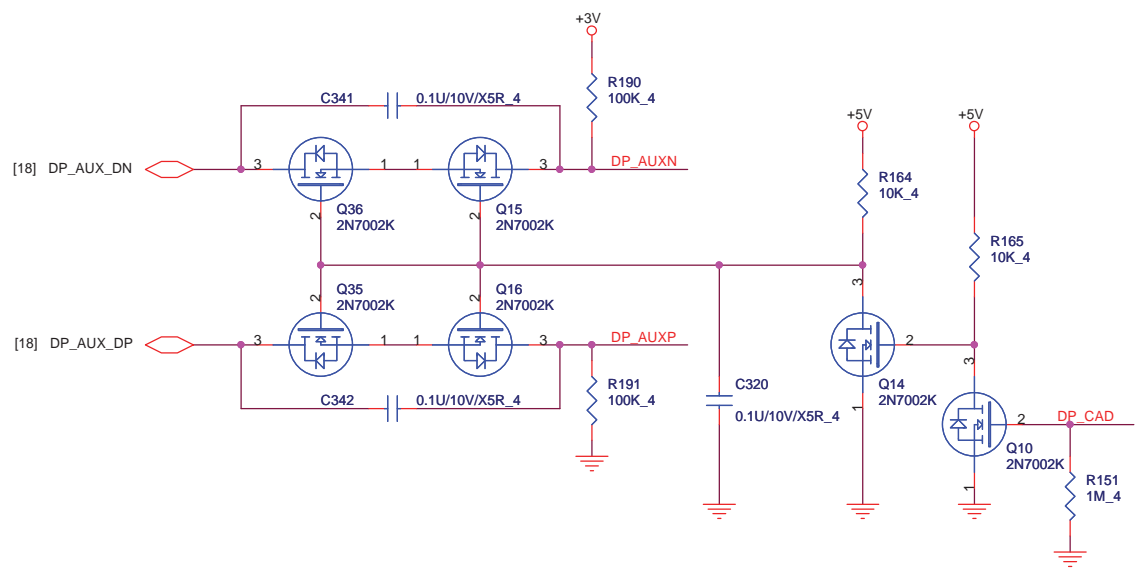
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		Quanta Computer Inc.	
Size Custom	Document Number N10M (GND) 5/5	Rev 1E	
Date:	Tuesday, January 26, 2010	Sheet	20 of 47





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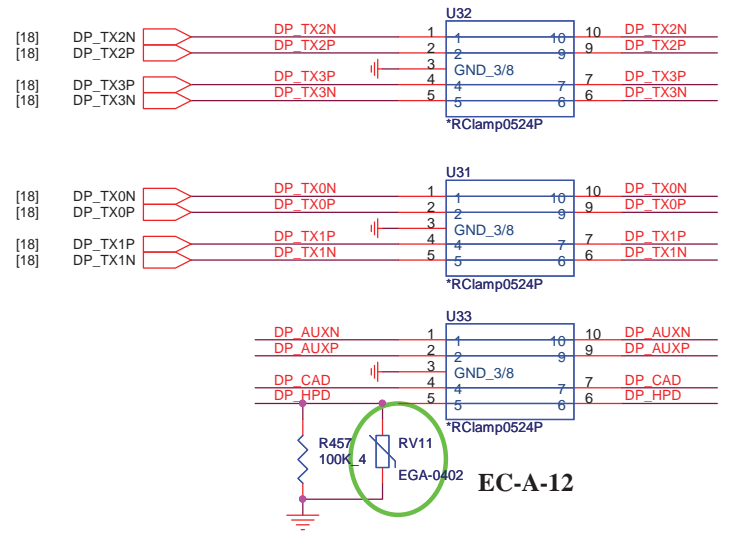
Size Custom	Document Number CRT CONN	Rev 1E
Date: Tuesday, January 26, 2010	Sheet 23	of 47



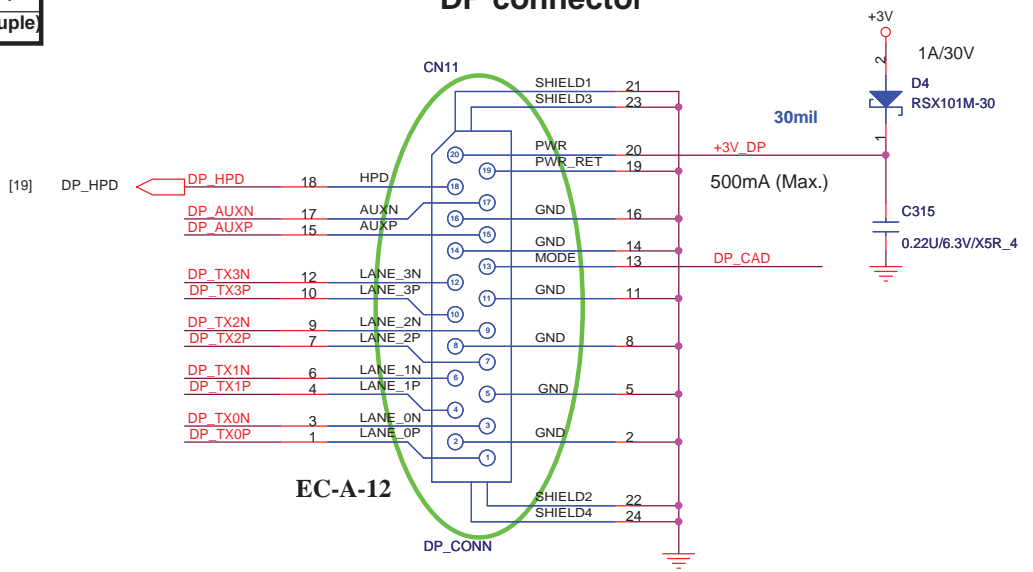
DP_CAD	Behavior
Low	DP signal (AC couple)
High	TMDS signal (DC couple)

ESD Protect

close to DP connector



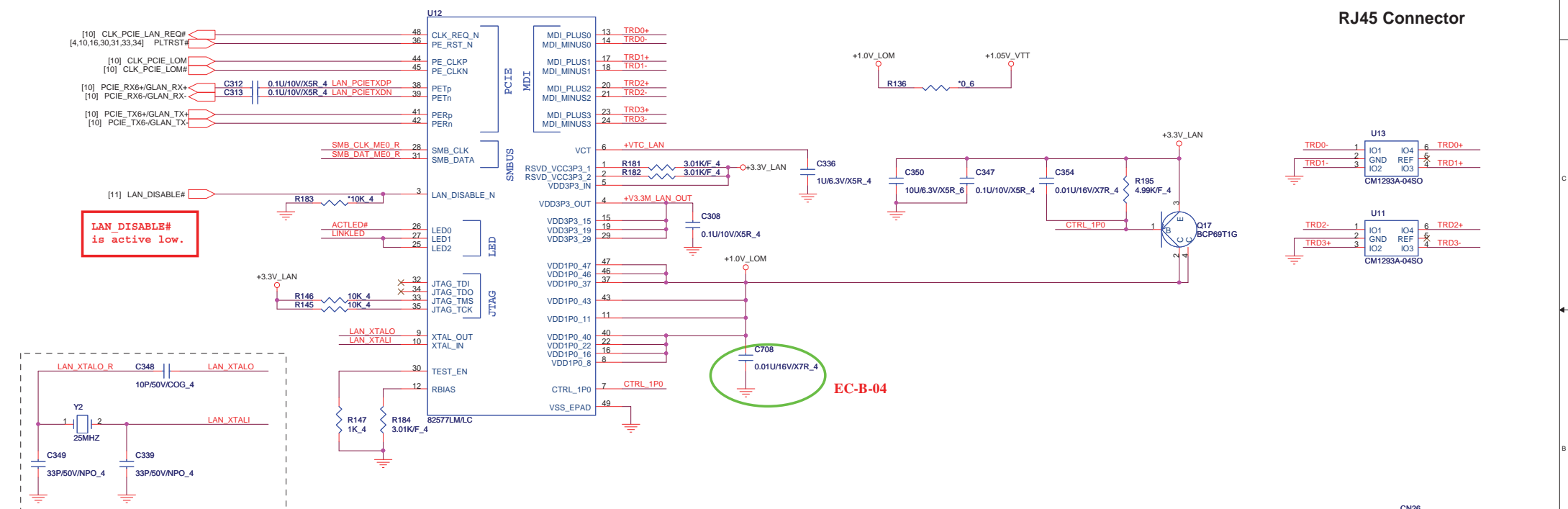
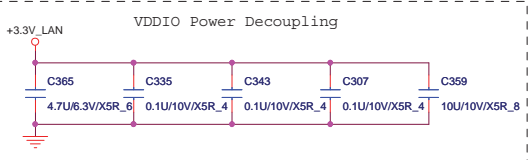
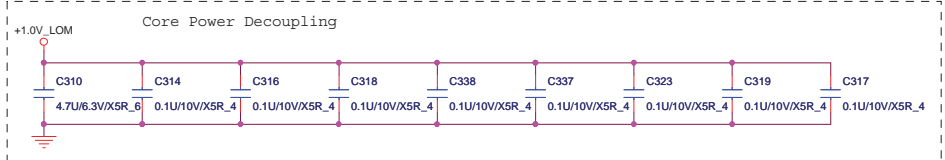
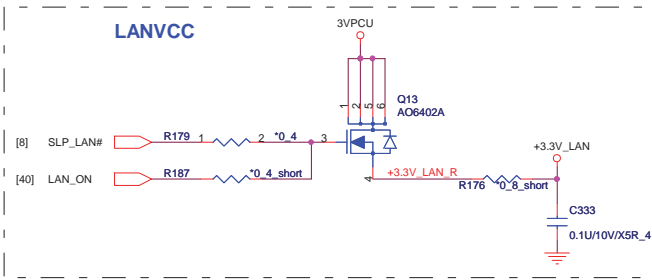
DP connector



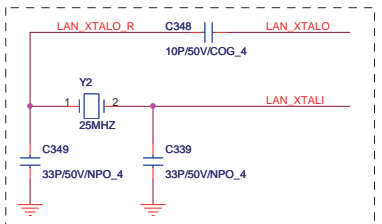
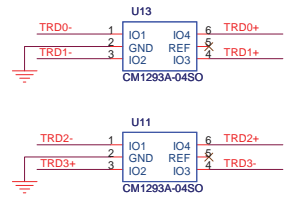
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Size: Custom | Document Number: DISPLAYPORT CONN | Rev: 1E

Date: Tuesday, January 26, 2010 | Sheet: 24 of 47

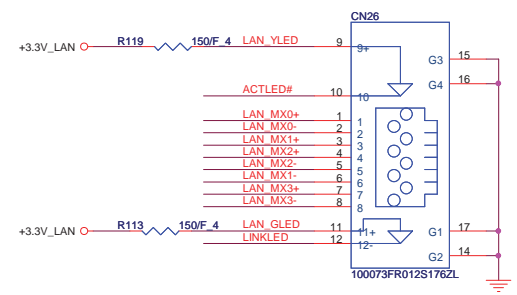
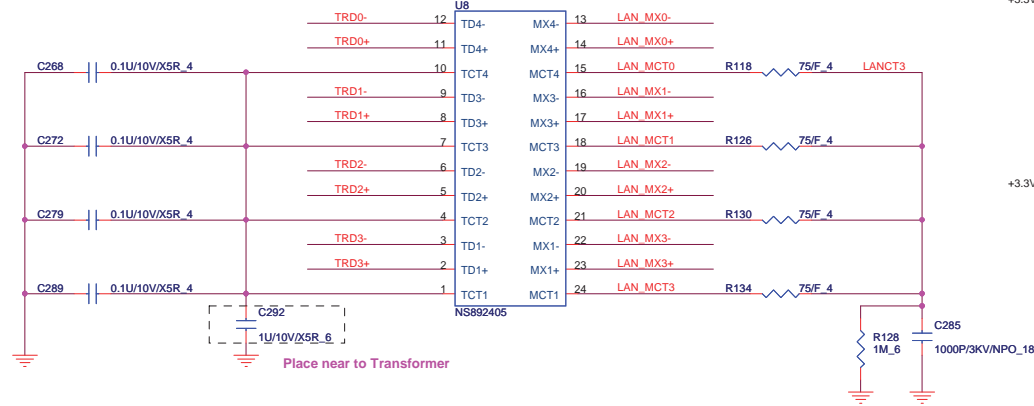
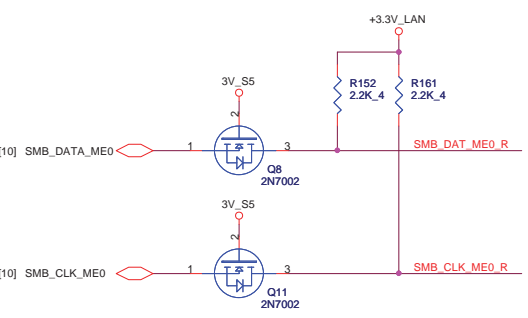


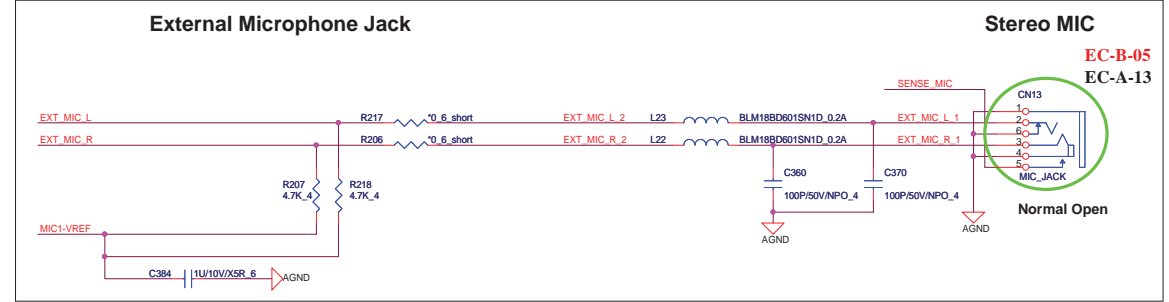
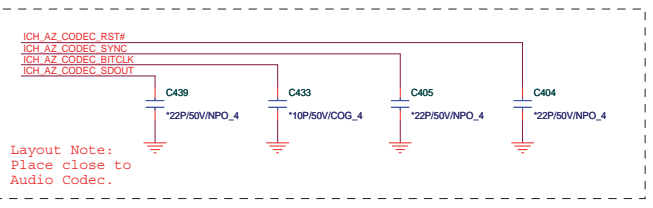
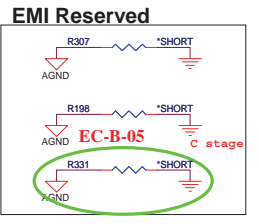
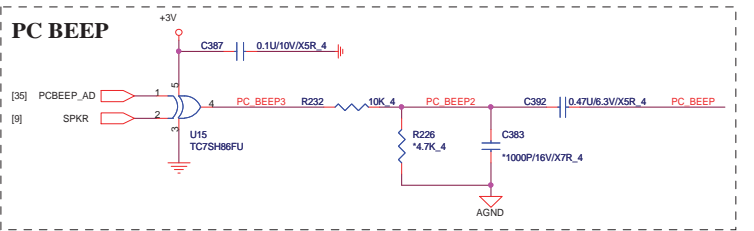
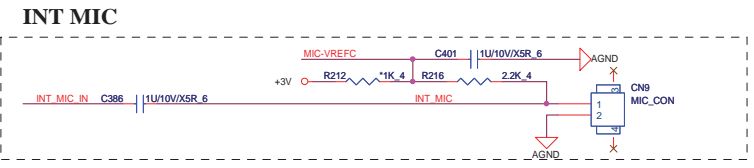
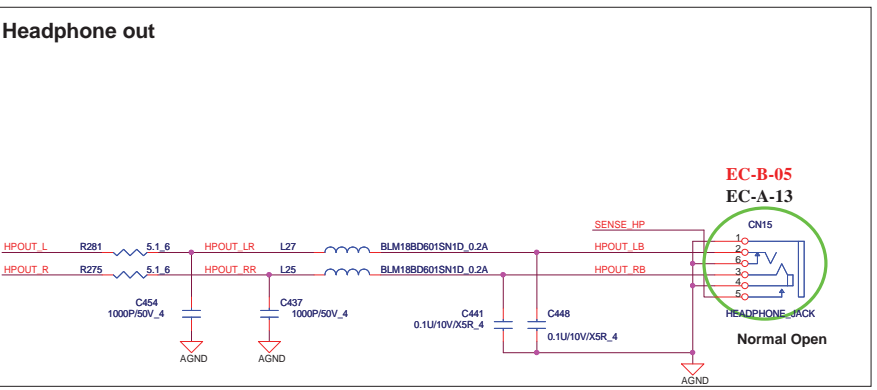
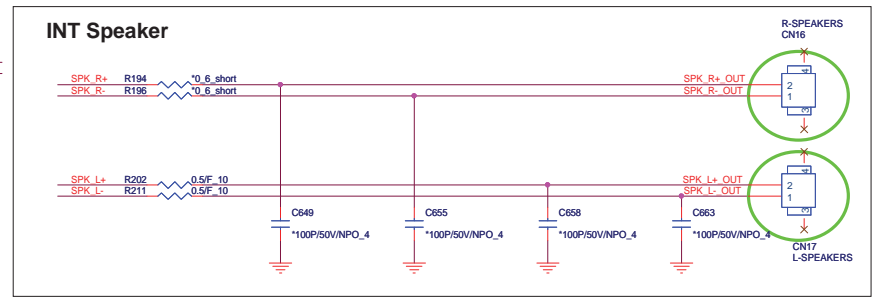
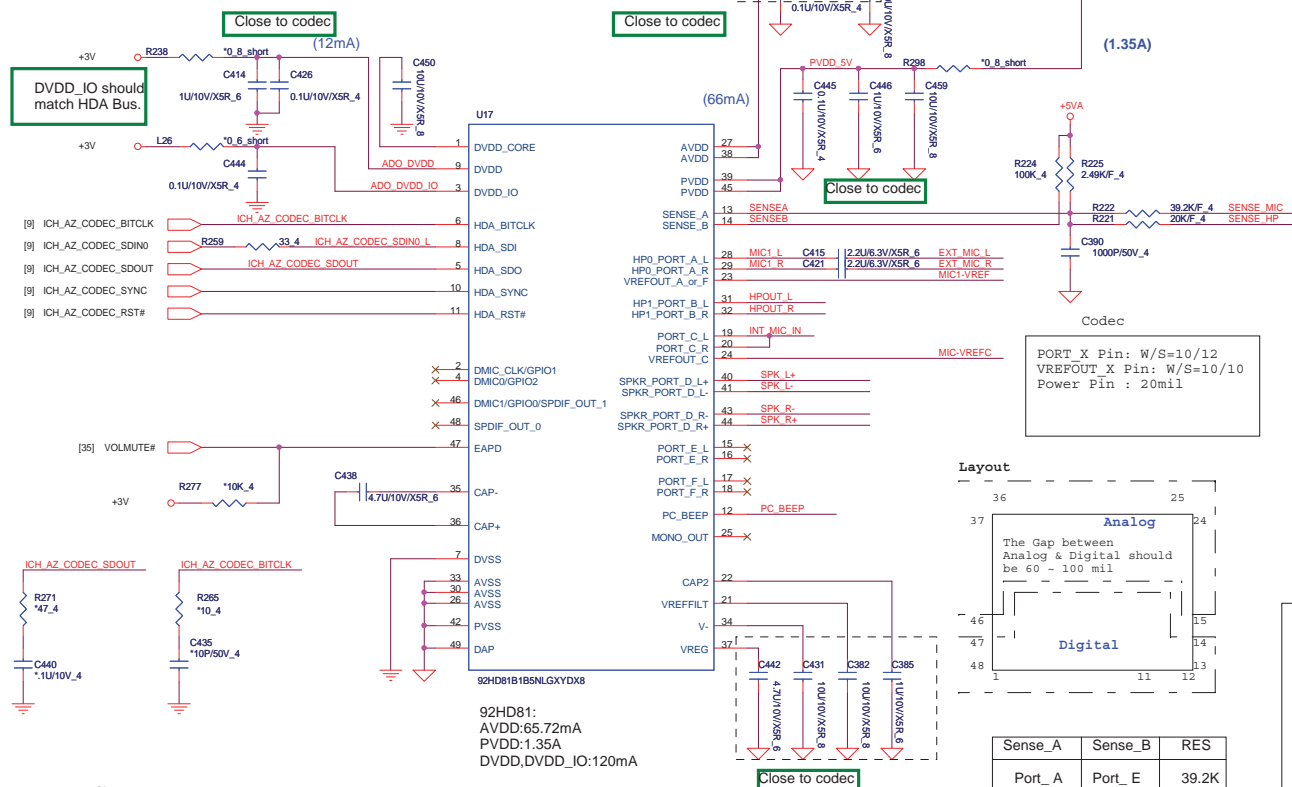
RJ45 Connector

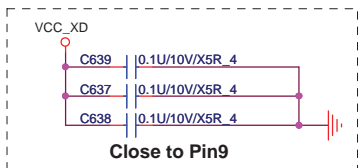
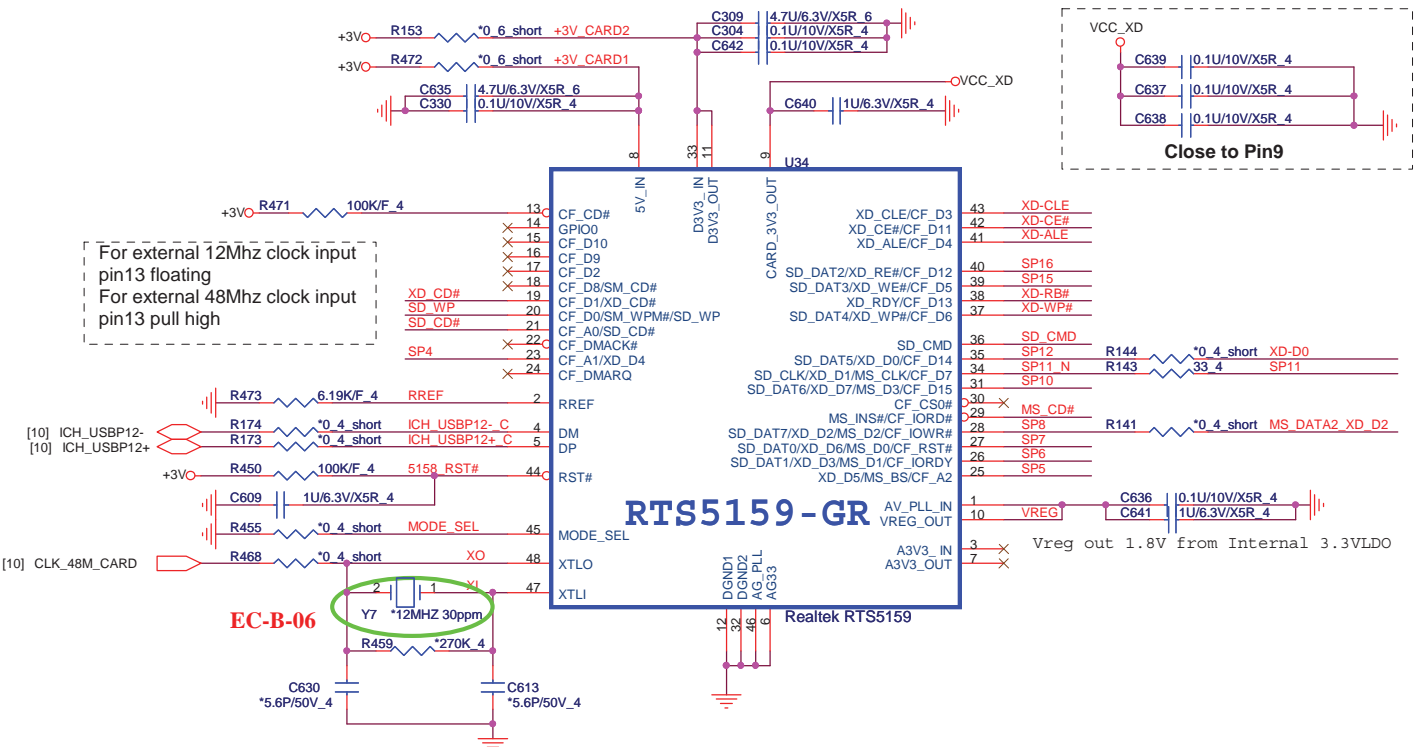


EC-B-04

Transformer

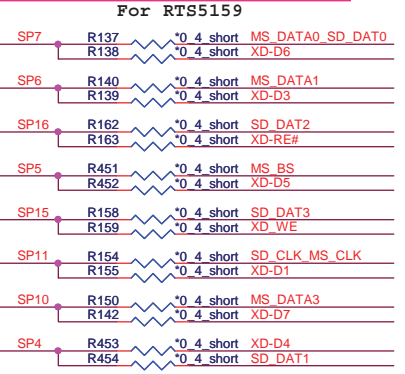




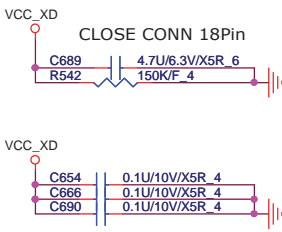
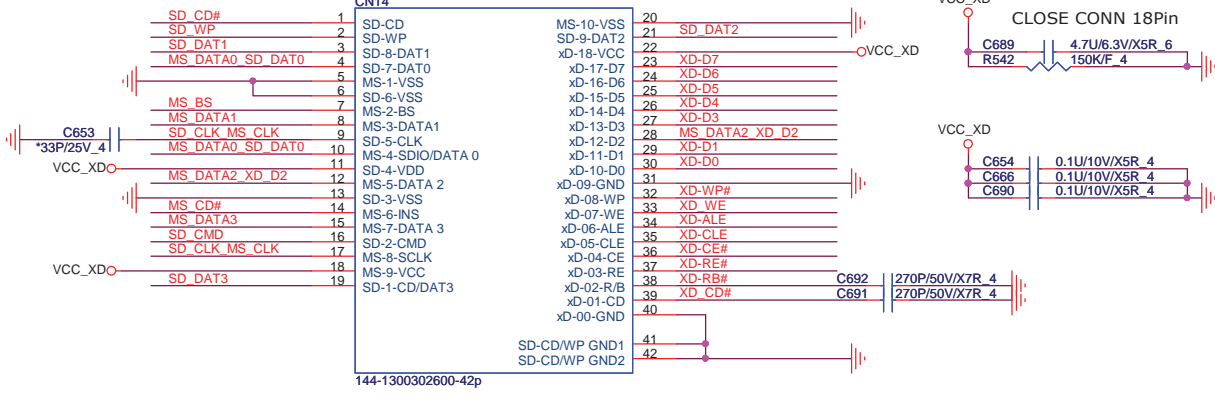


Note:

SP0	SD/MMC	MS	XD
SP1			XD_CD#
SP2	SD_WP		
SP3	SD_CD#		
SP4	SD_DAT1		XD_D4
SP5		MS_BS	XD_D5
SP6		MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_IN#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14			XD_R/#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE



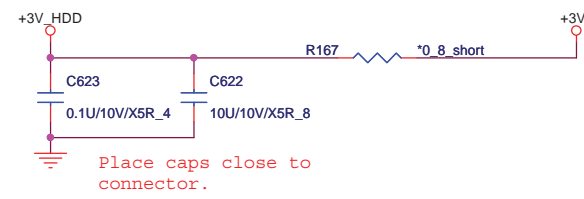
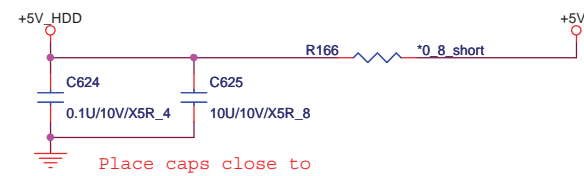
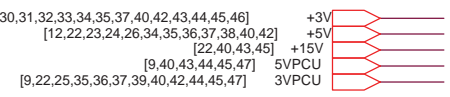
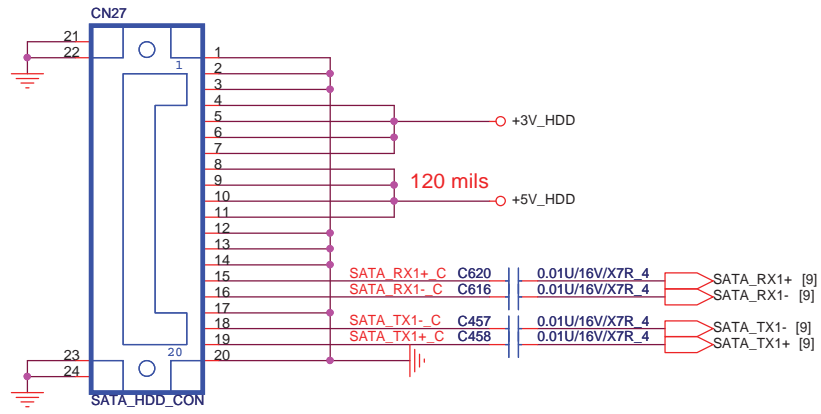
**5 IN1 CARD READER
XD, MMC/SD, MS/MSP**



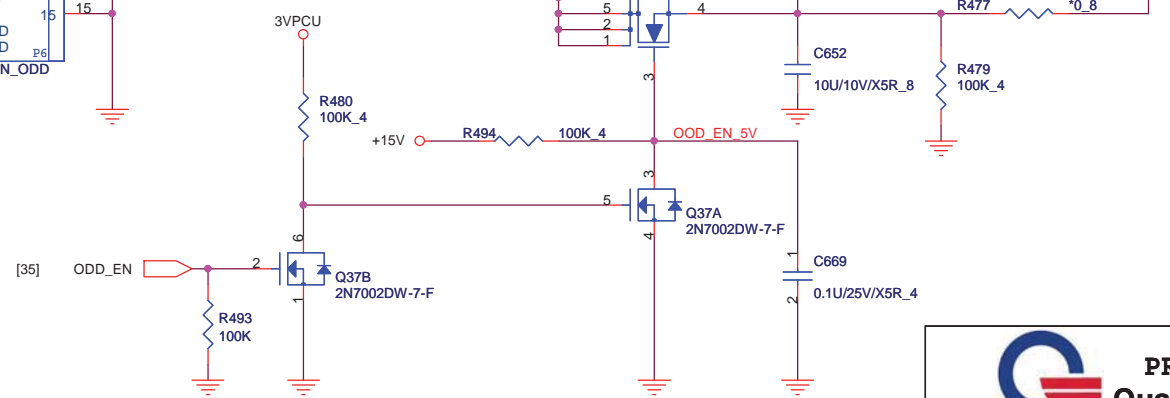
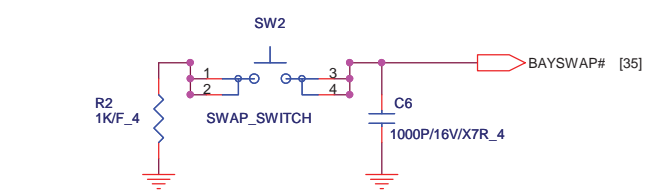
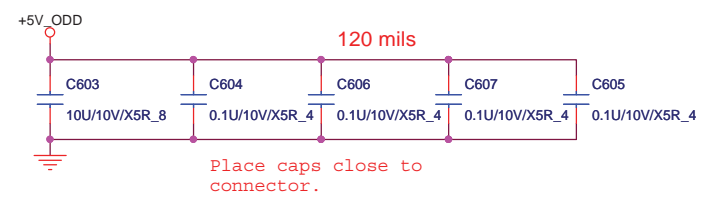
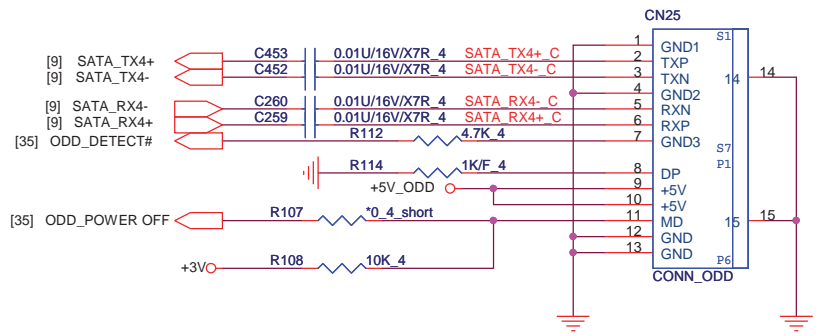
PROJECT : LL3A
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Size B	Document Number	Rev 1E
	Card Reader (RTS5159)	
Date:	Tuesday, January 26, 2010	Sheet 27 of 47

SATA-HDD CONNECTOR



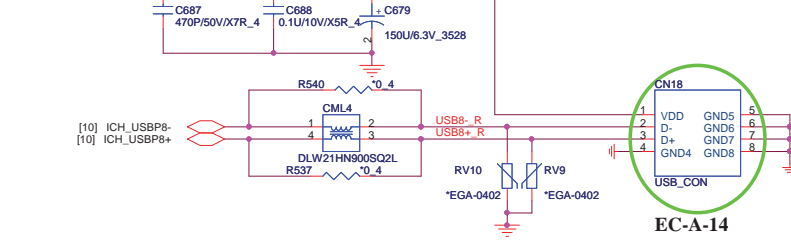
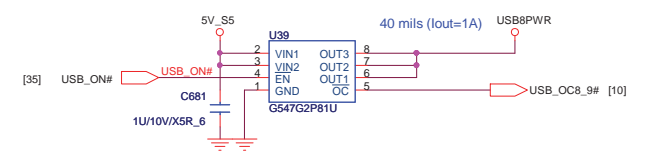
SATA CD-ROM



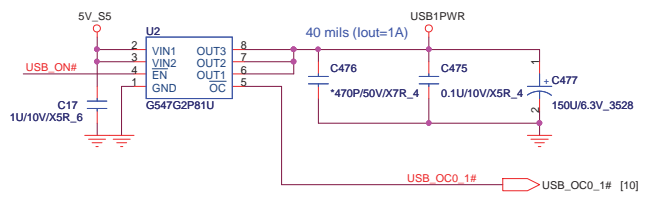


PROJECT : LL3A
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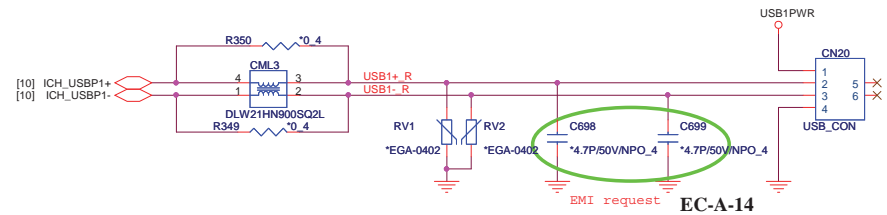
Size Custom	Document Number HDD/ODD	Rev 1E
Date:	Tuesday, January 26, 2010	Sheet 28 of 47



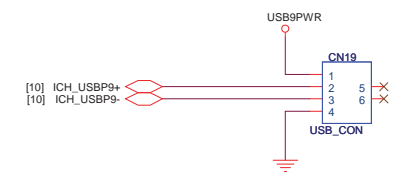
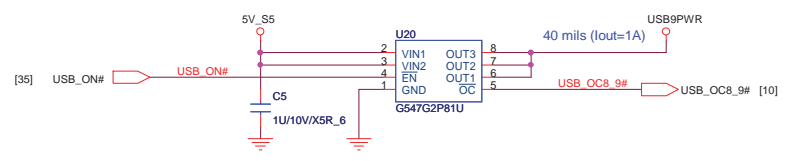
EC-A-14



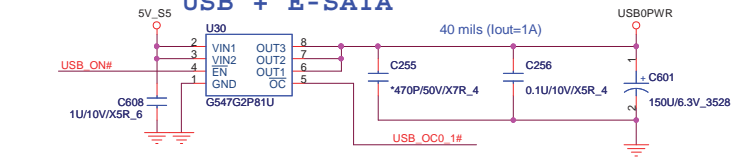
USB X1---> Wire to board conn



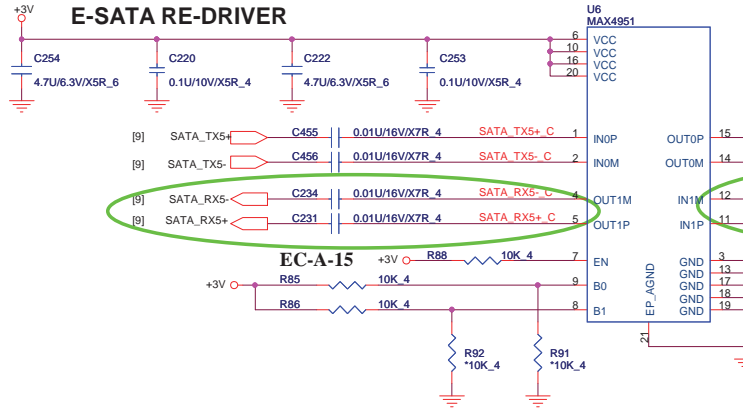
EC-A-14



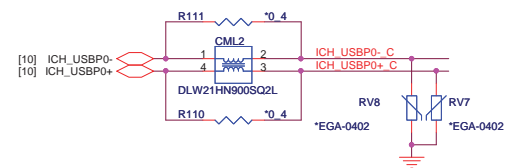
USB + E-SATA



E-SATA RE-DRIVER

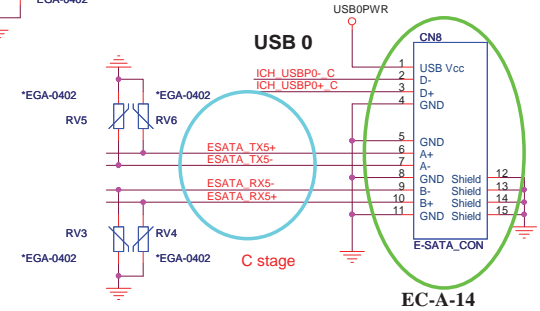


EC-A-15



EC-A-15

USB 0



EC-A-14

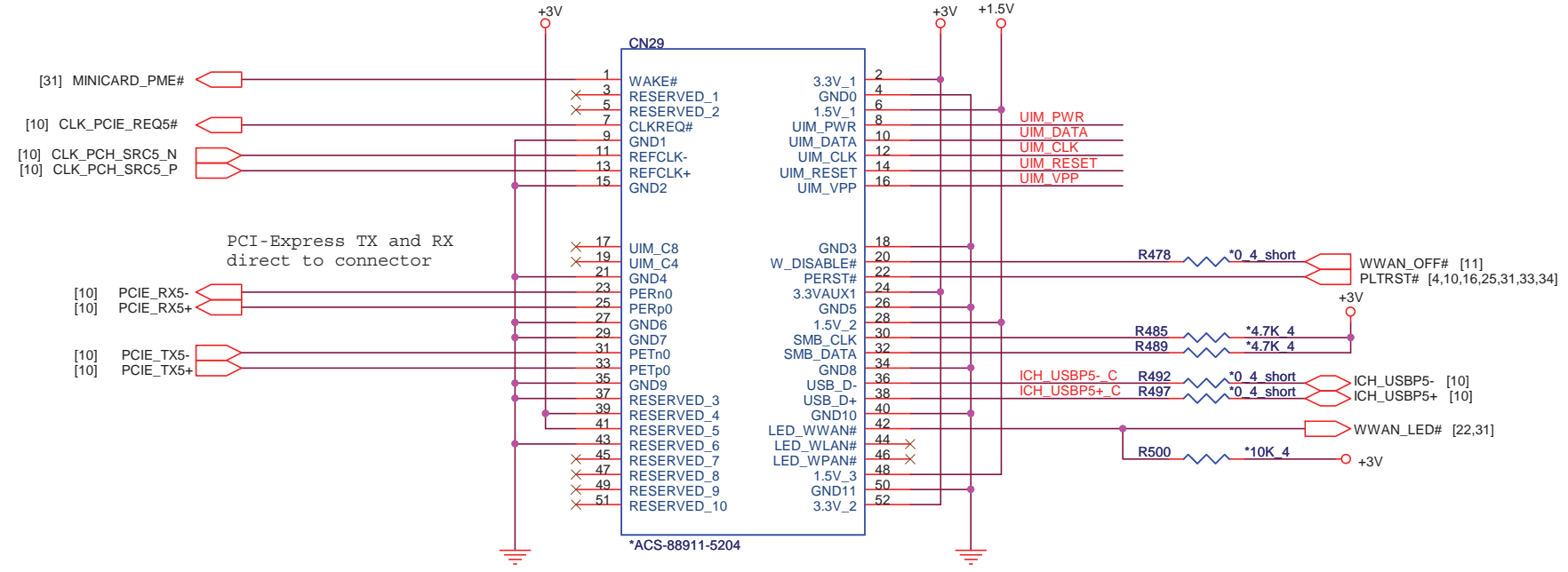
EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output

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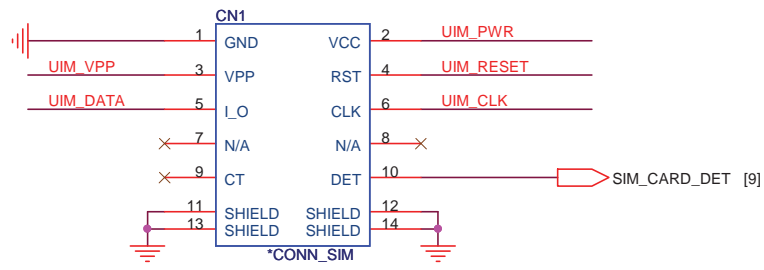
Size: Custom | Document Number: **USB X3/USB+ESATA** | Rev: 1E

Date: Tuesday, January 26, 2010 | Sheet: 29 of 47

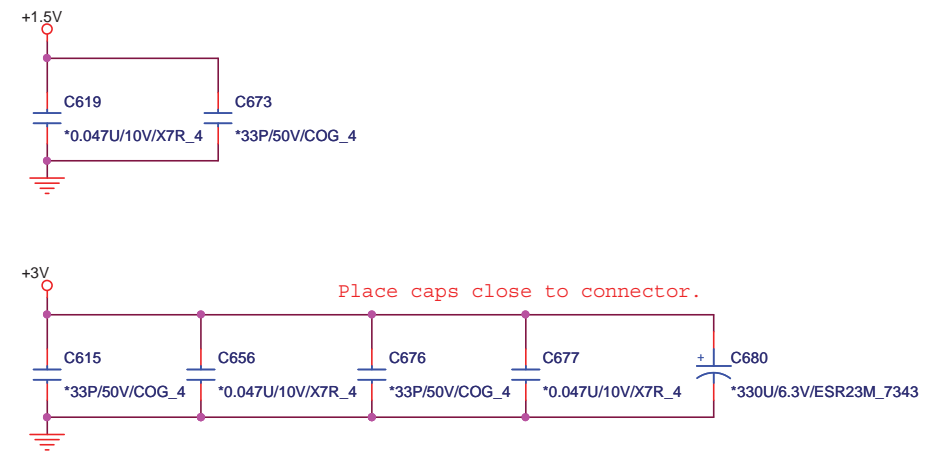
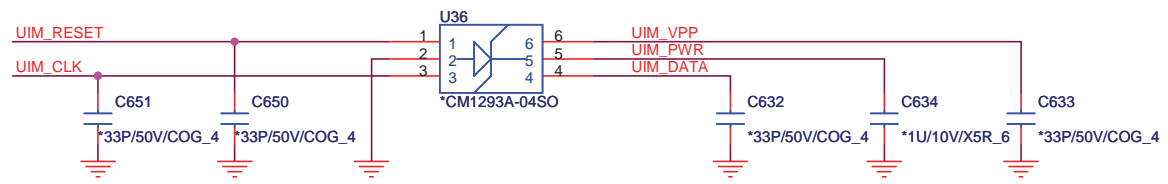
MiniCard WWAN connector




SIM Card CONN



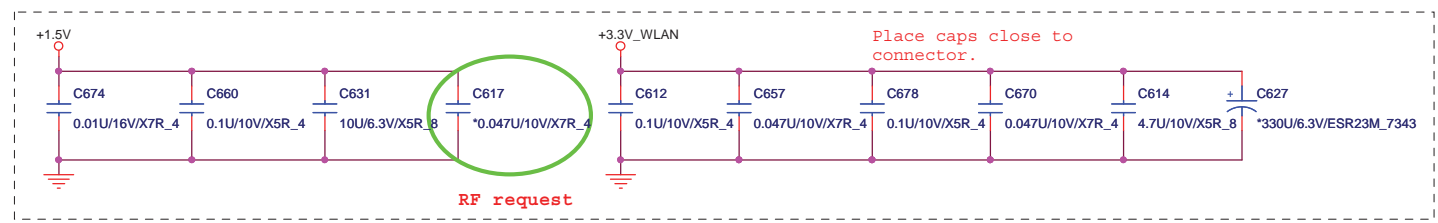
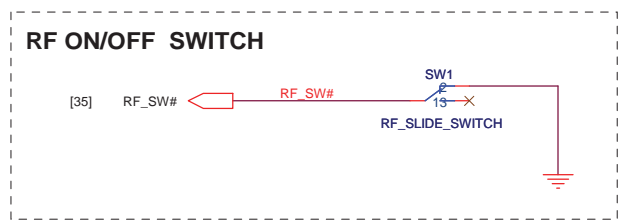
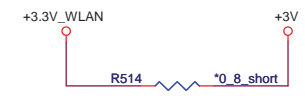
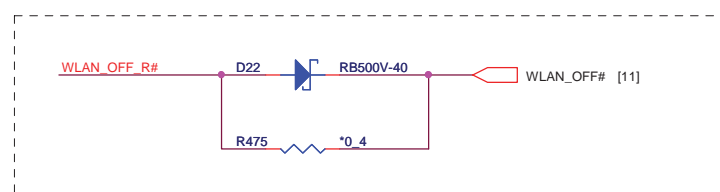
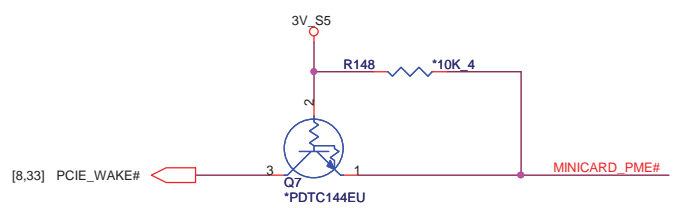
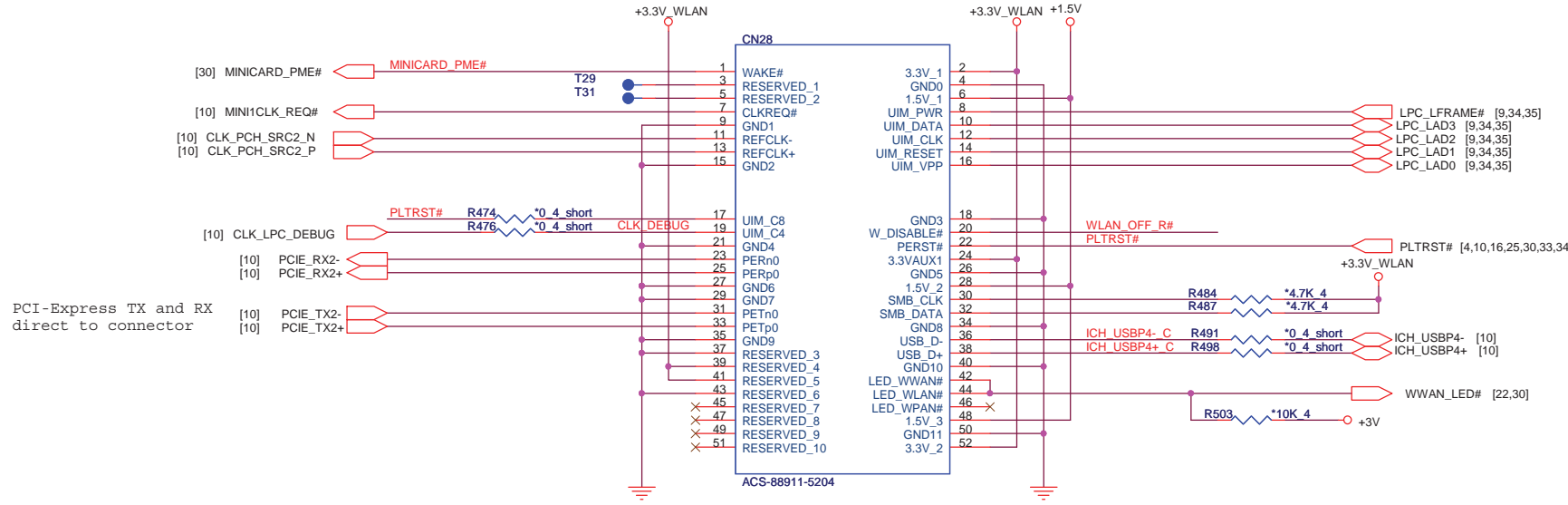
Layout Note:
UIM_RESET, UIM_CLK, UIM_DATA routing as short as possible





PROJECT : LL3A
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Size Custom	Document Number	Rev 1E
MINI-Card (WWAN)		
Date:	Tuesday, January 26, 2010	Sheet 30 of 47



EC-A-16

Mini PCI-E Card 3 SSD

<http://hobi-elektronika.net>

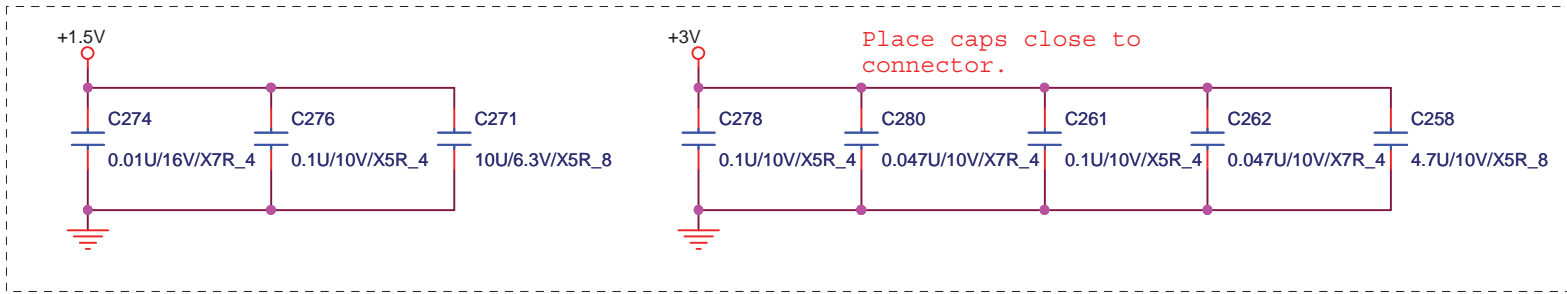
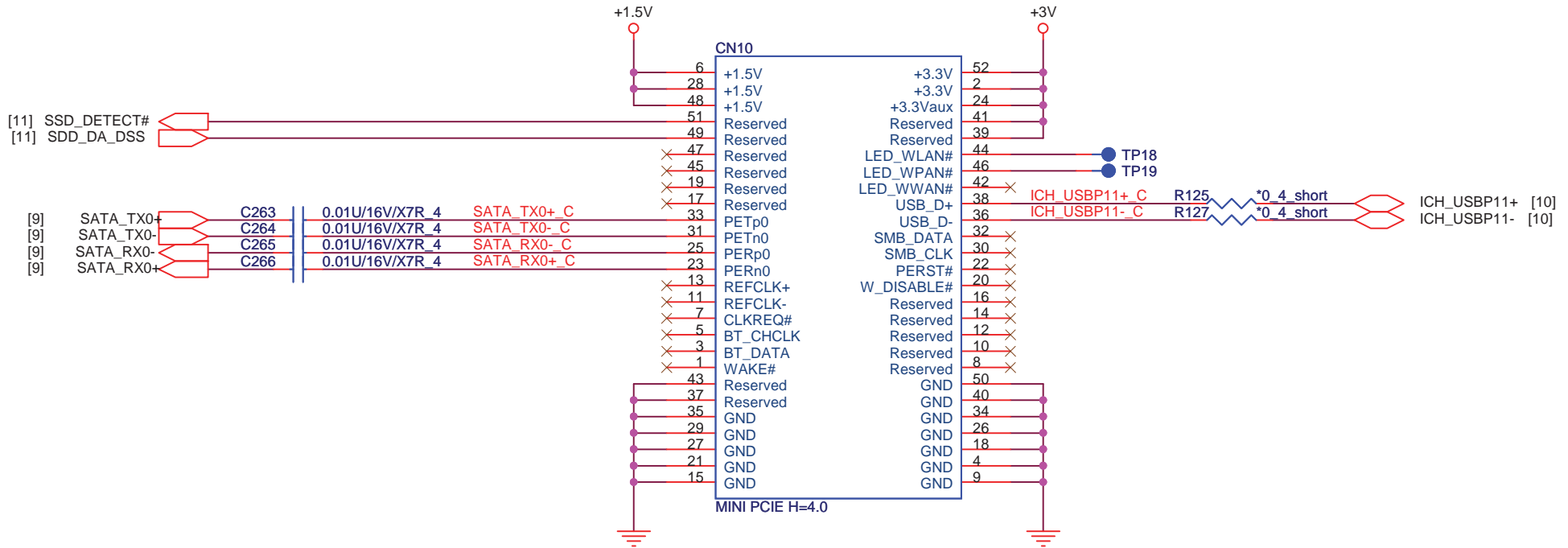
[3,17,21,30,31,33,39,43]

[3,4,6,8,9,10,11,12,14,15,16,18,19,22,23,24,26,27,28,29,30,31,33,34,35,37,40,42,43,44,45,46]

+1.5V

+3V

32

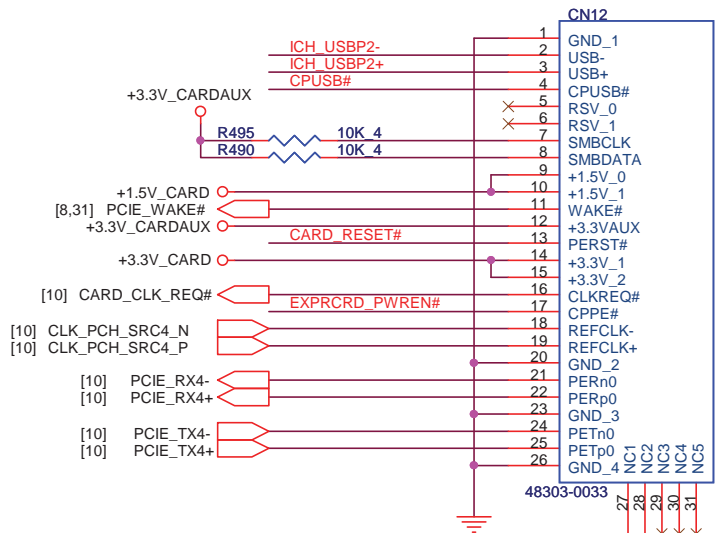
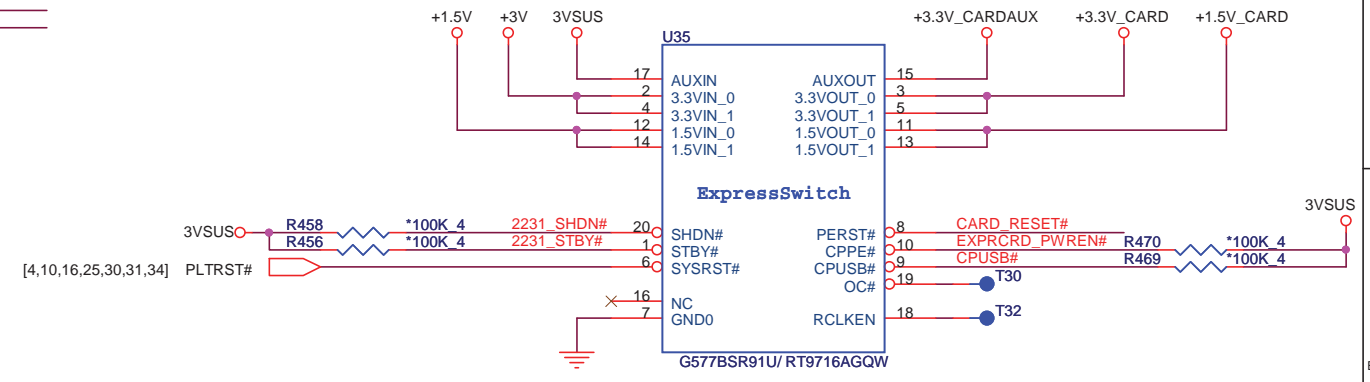
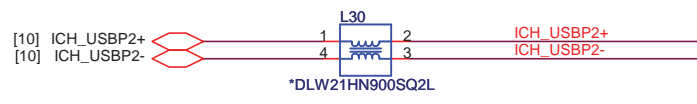


PROJECT : LL3A
Quanta Computer Inc.

Size Custom	Document Number MINI Card (SSD)	Rev 1E
Date:	Tuesday, January 26, 2010	Sheet 32 of 47

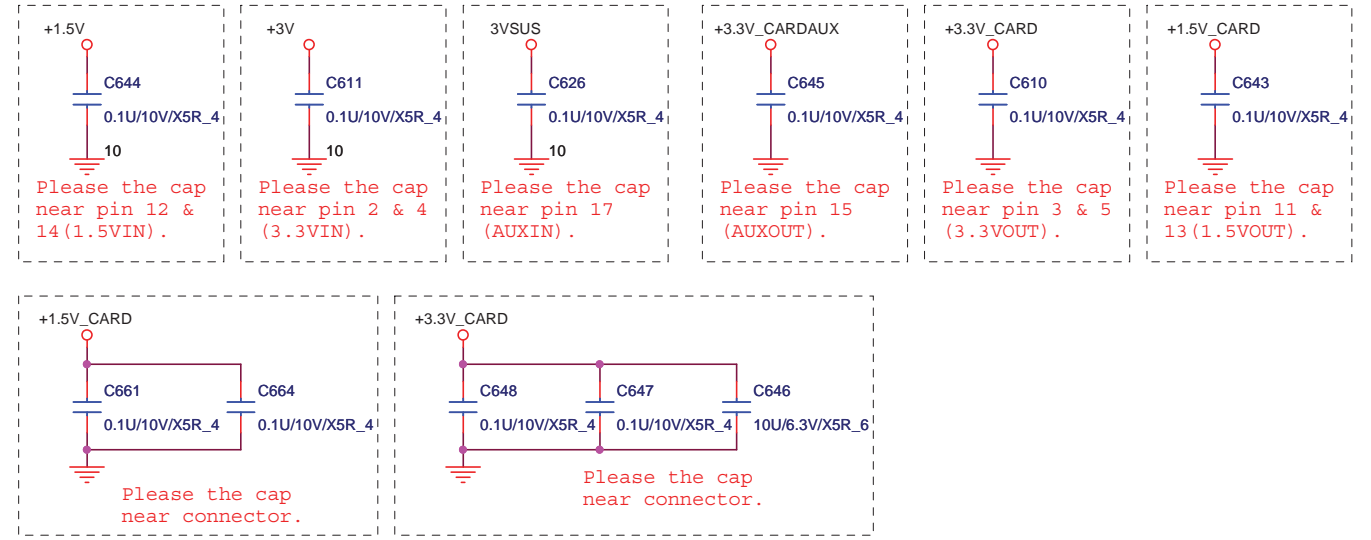
Express Card


+1.5V_CARD Max. 650mA, Average 500mA.
 +3.3V_CARD Max. 1300mA, Average 1000mA.



PCI-Express TX and RX direct to connector.

JAE PX10FS16PH-26P

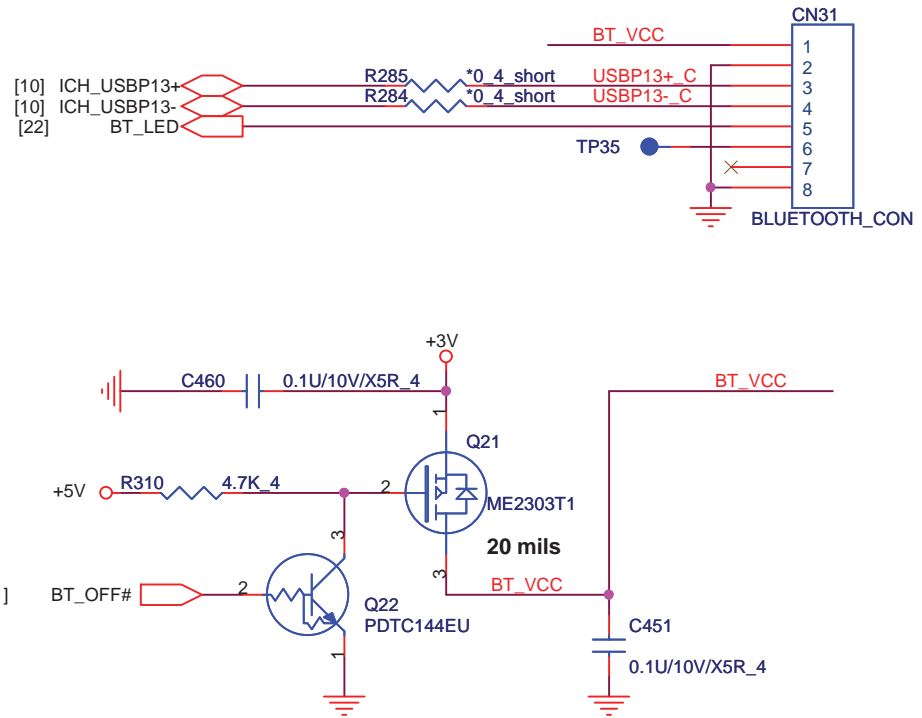




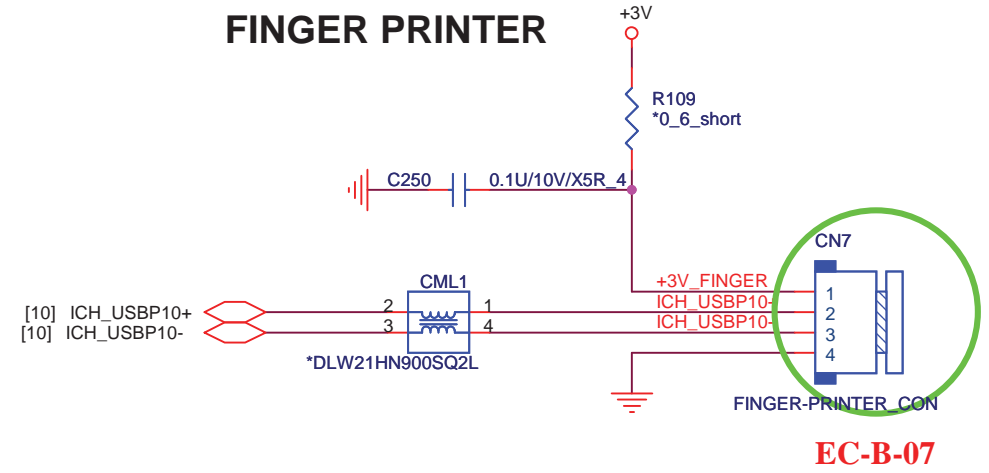
PROJECT : LL3A
Quanta Computer Inc.

Size Custom	Document Number	Rev 1E
Express Card		
Date: Tuesday, January 26, 2010	Sheet 33 of 47	

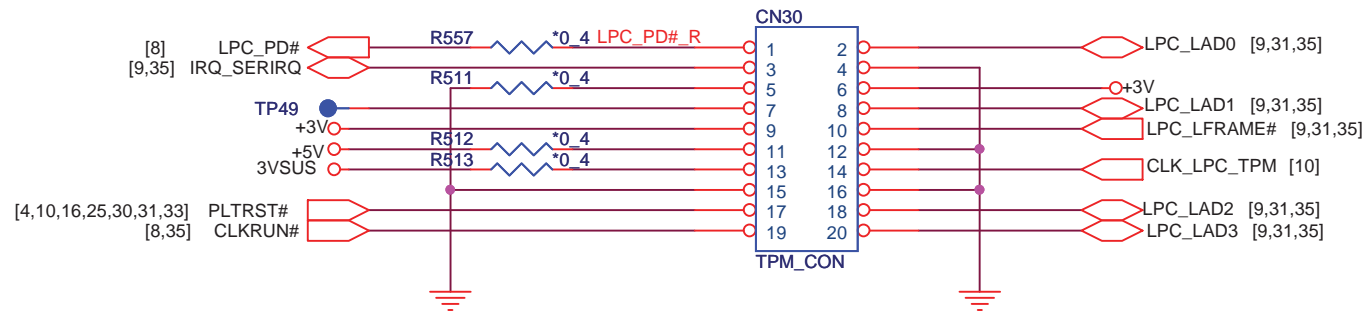
BLUETOOTH




FINGER PRINTER



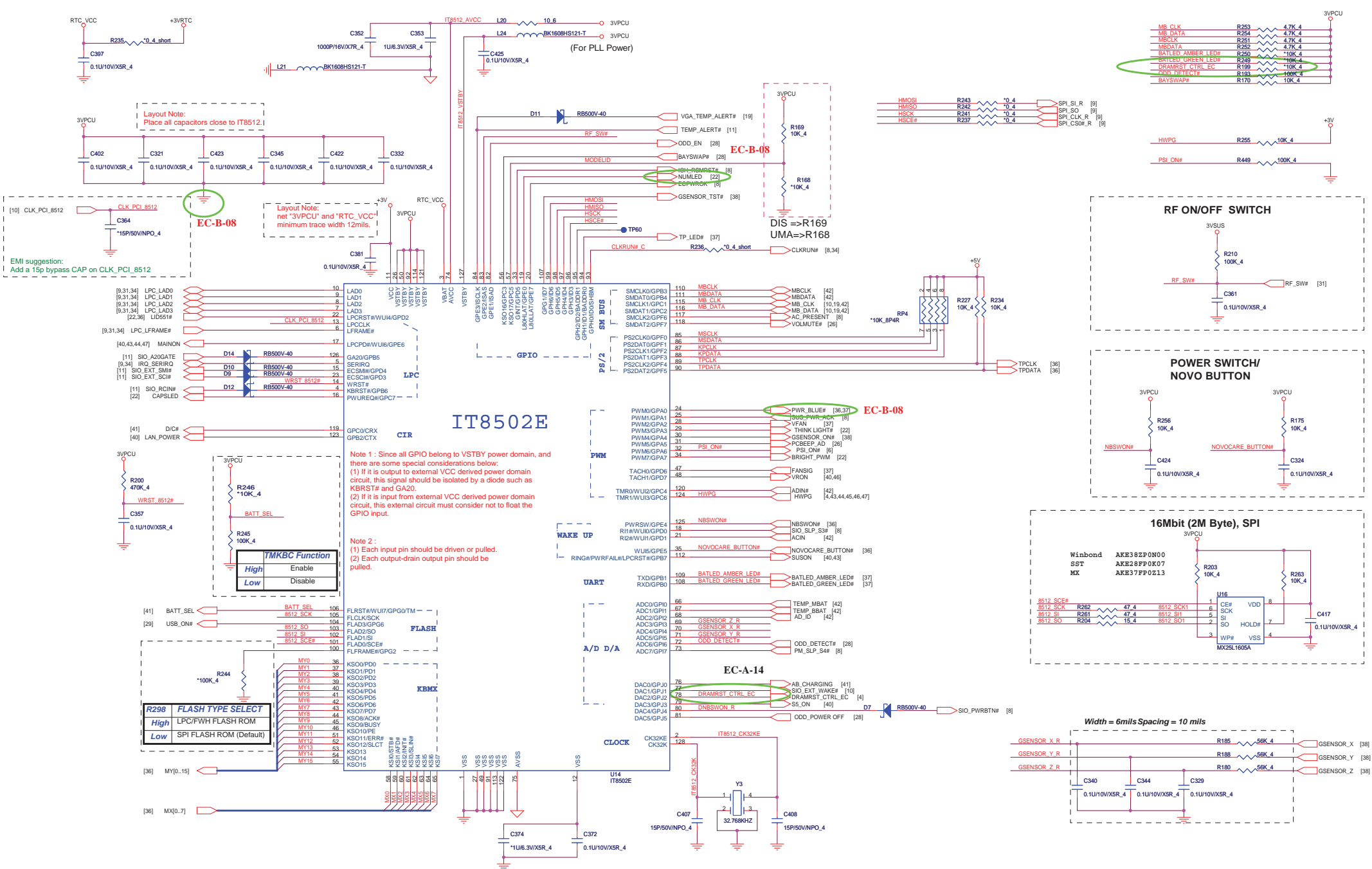
TPM





PROJECT : LL3A
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Size Custom	Document Number BT/FP/TPM	Rev 1E
Date: Tuesday, January 26, 2010		Sheet 34 of 47



Layout Note: Place all capacitors close to IT8512.

Layout Note: net "3VPCU" and "RTC_VCC" minimum trace width 12mils.

EMI suggestion: Add a 15p bypass CAP on CLK_PCI_8512

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below: (1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20. (2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 : (1) Each input pin should be driven or pulled. (2) Each output-drain output pin should be pulled.

TMKBC Function table with columns for High/Low and Enable/Disable.

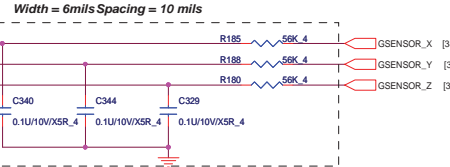
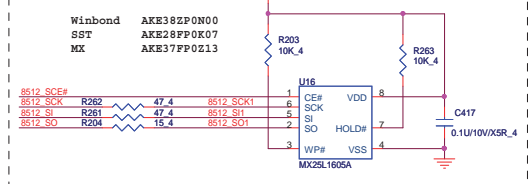
FLASH TYPE SELECT table with columns for High/Low and LPC/FWH FLASH ROM/SPI FLASH ROM (Default).

IT8502E

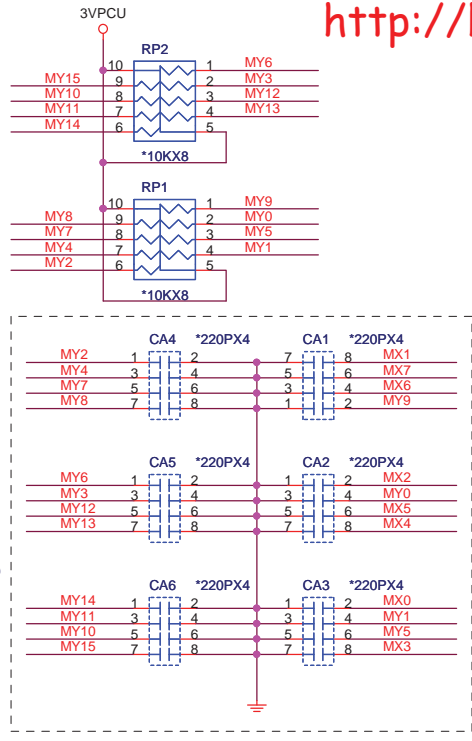
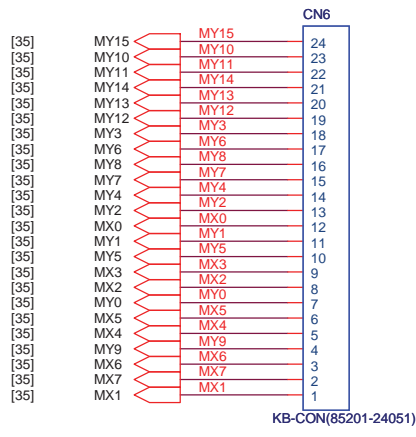
RF ON/OFF SWITCH

POWER SWITCH/ NOVO BUTTON

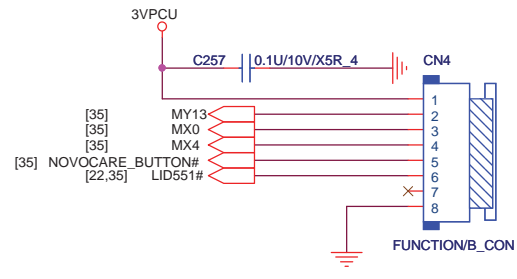
16Mbit (2M Byte), SPI



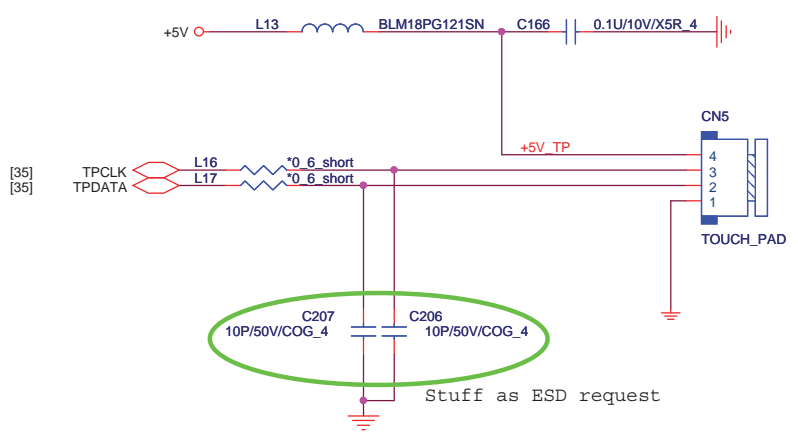
KEYBOARD



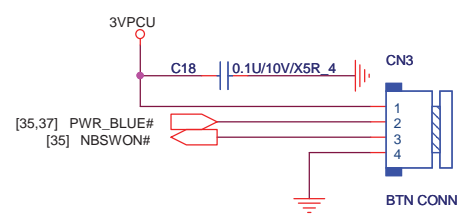
FUNCTION BUTTON BOARD



TOUCH PAD



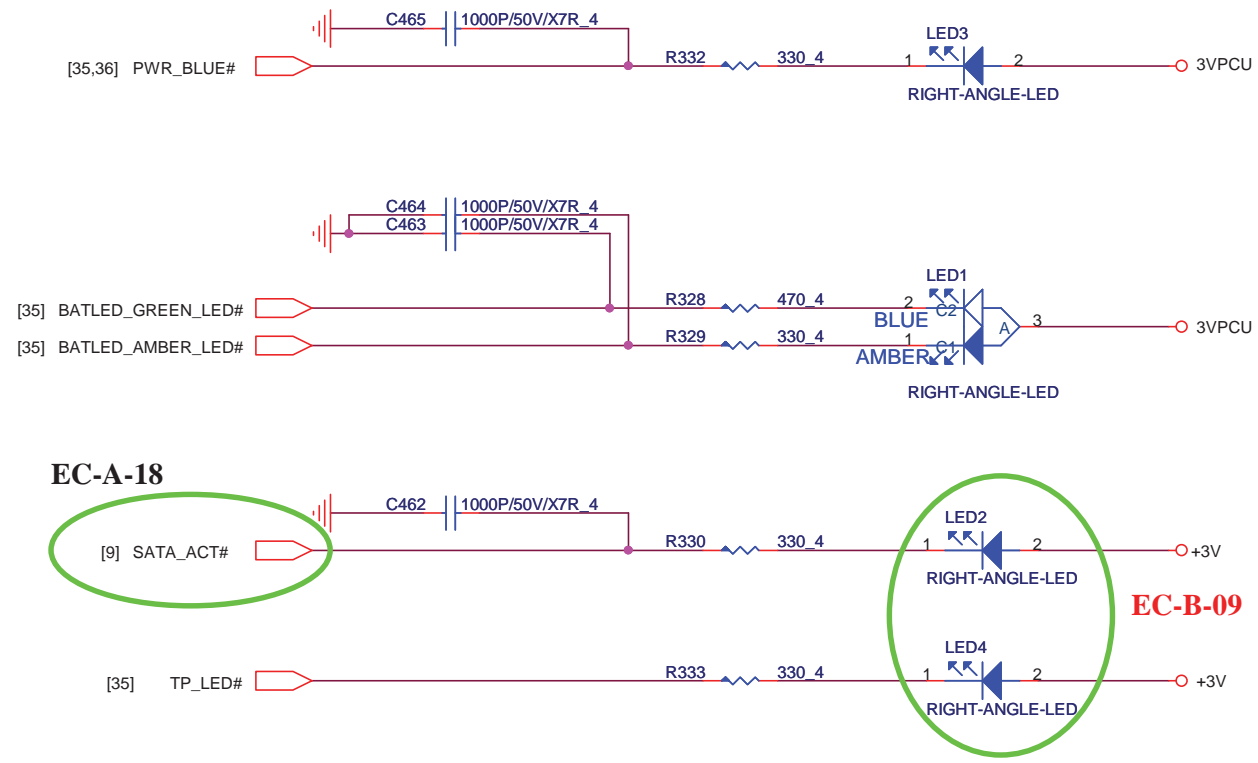
POWER BUTTON BOARD



PROJECT :LL3A
Quanta Computer Inc.

Size Custom	Document Number	Rev 1E
KB/TP/PW-B/FN-B		
Date: Tuesday, January 26, 2010	Sheet 36 of 47	

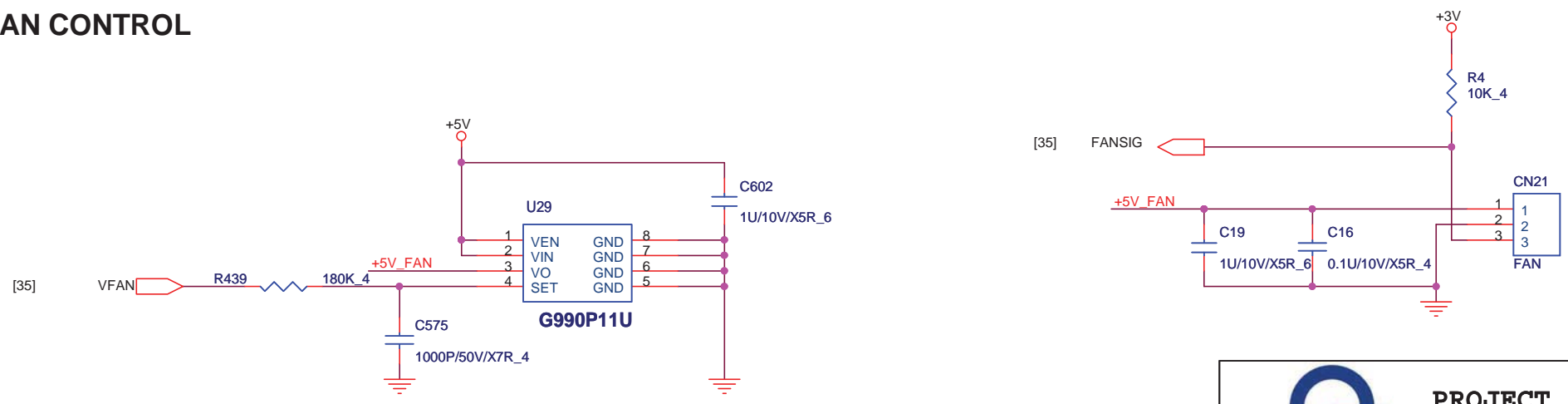
LED




EC-A-18

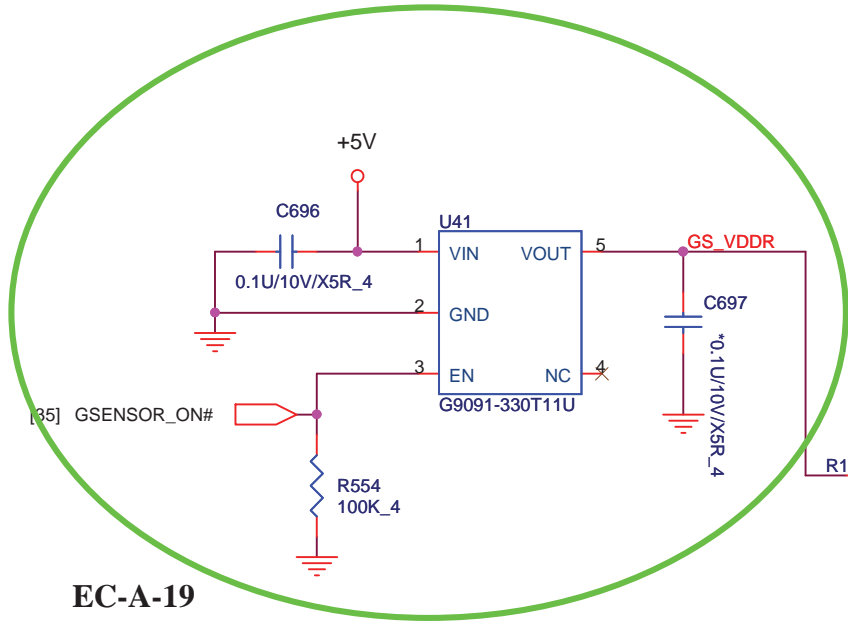
EC-B-09

FAN CONTROL



 PROJECT : LL3A Quanta Computer Inc.		
LED/FAN		
Date:	Tuesday, January 26, 2010	Sheet 37 of 47

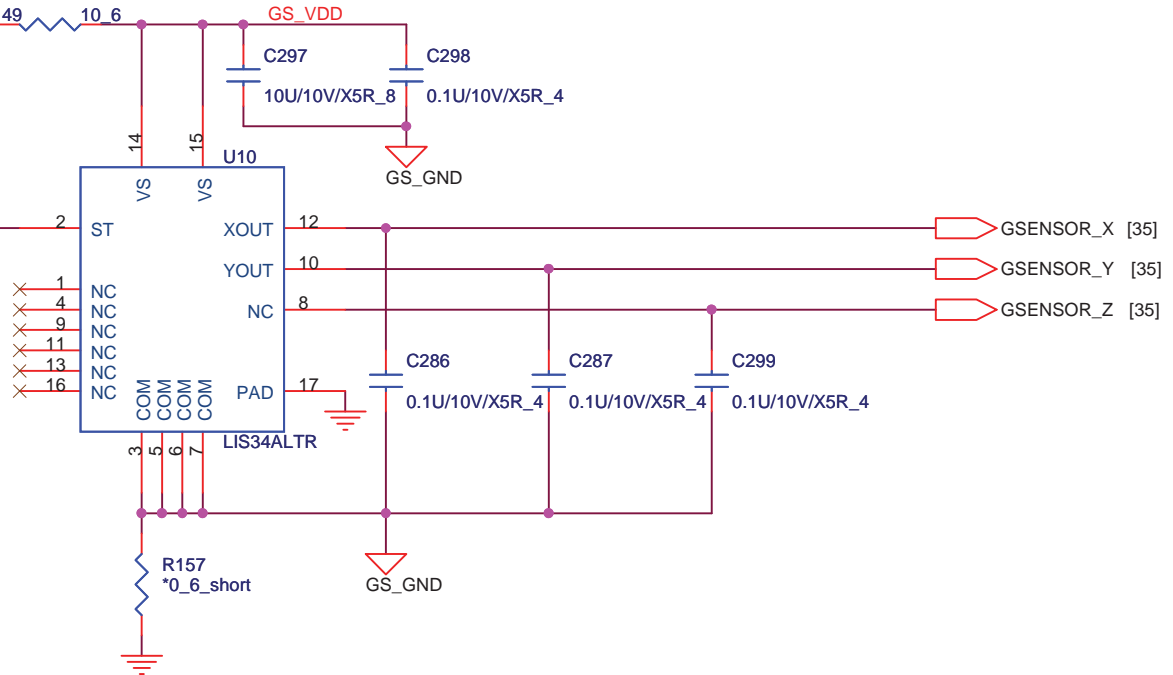
G-SENSOR (3-Axial)




EC-A-19

[35] GSENSOR_ON#

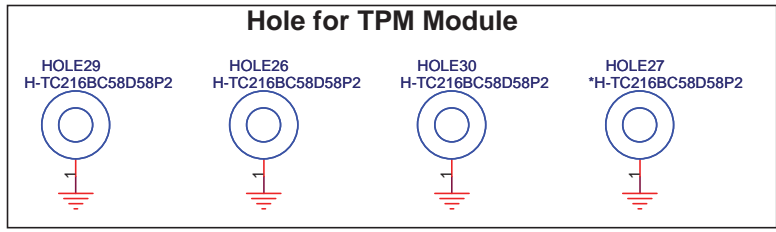
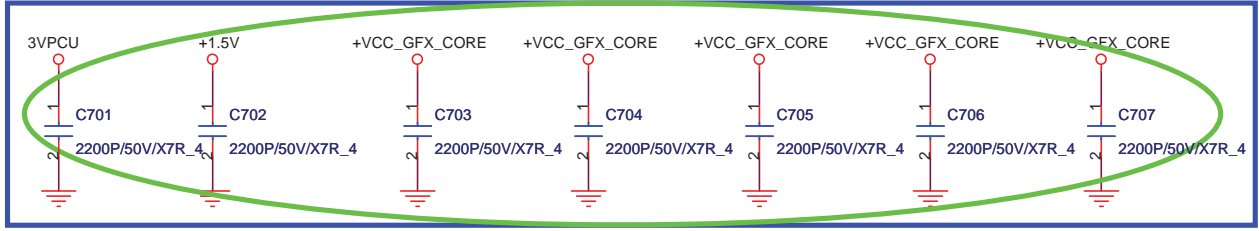
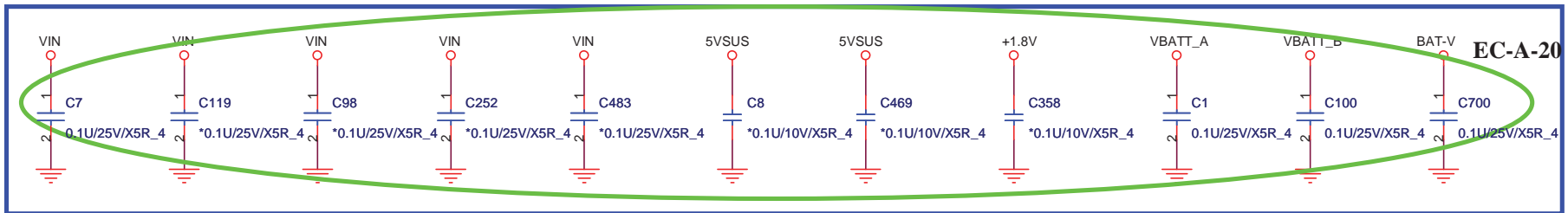
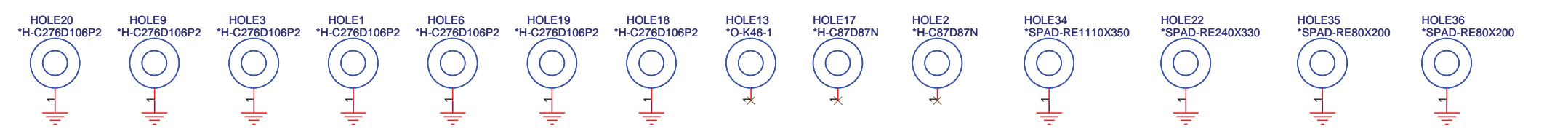
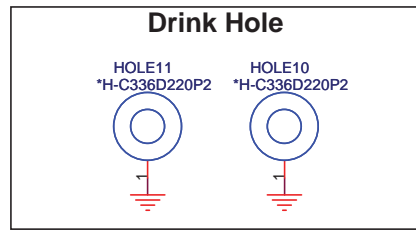
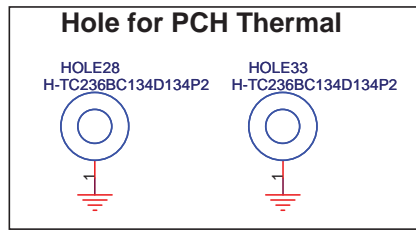
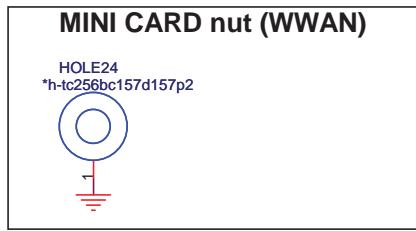
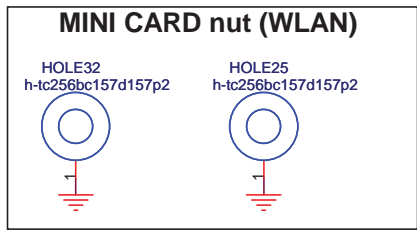
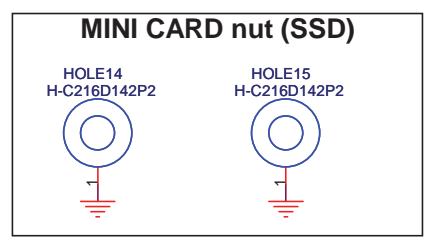
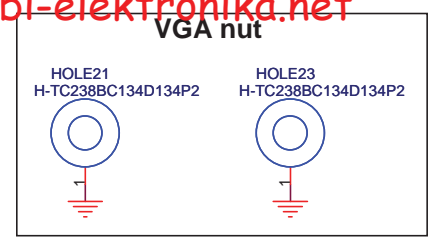
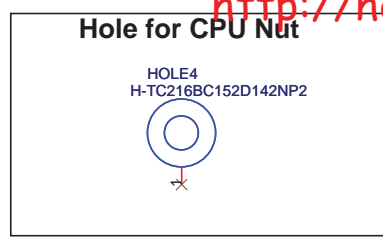
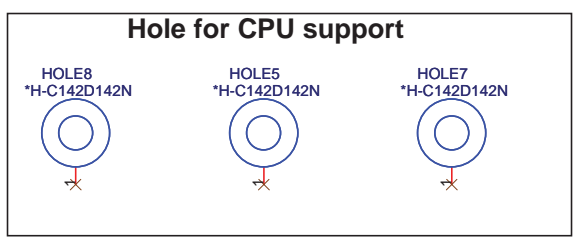
[35] GSENSOR_TST#



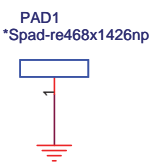


PROJECT : LL3A
Quanta Computer Inc.

Size Custom	Document Number G-SENSOR	Rev 1E
Date:	Tuesday, January 26, 2010	Sheet 38 of 47

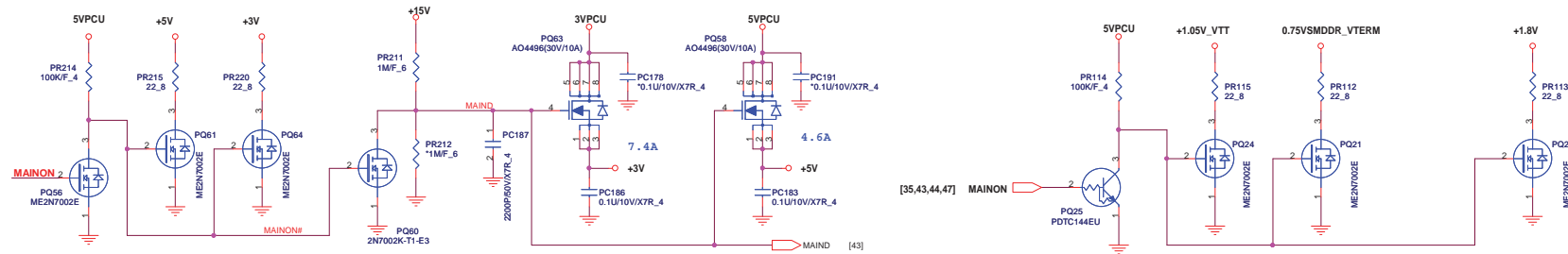


EC-B-10

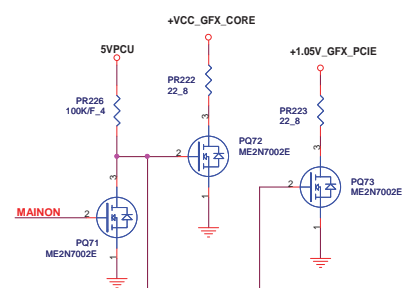
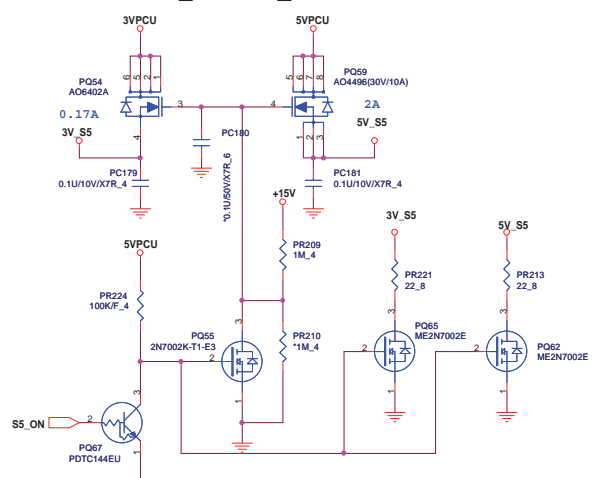


PROJECT : LL3A
Quanta Computer Inc.

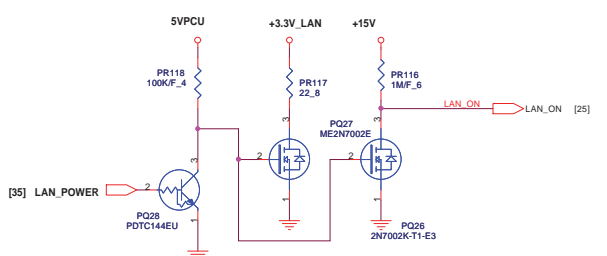
Size Custom	Document Number	Rev 1E
HOLD & SKEW		
Date: Tuesday, January 26, 2010	Sheet 39 of 47	



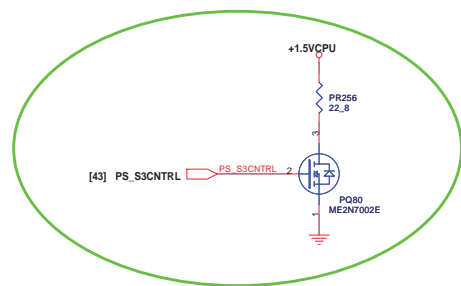
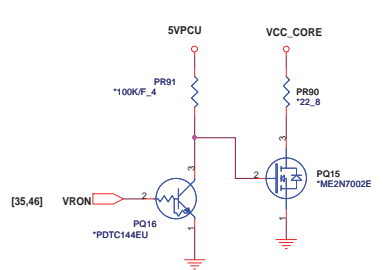
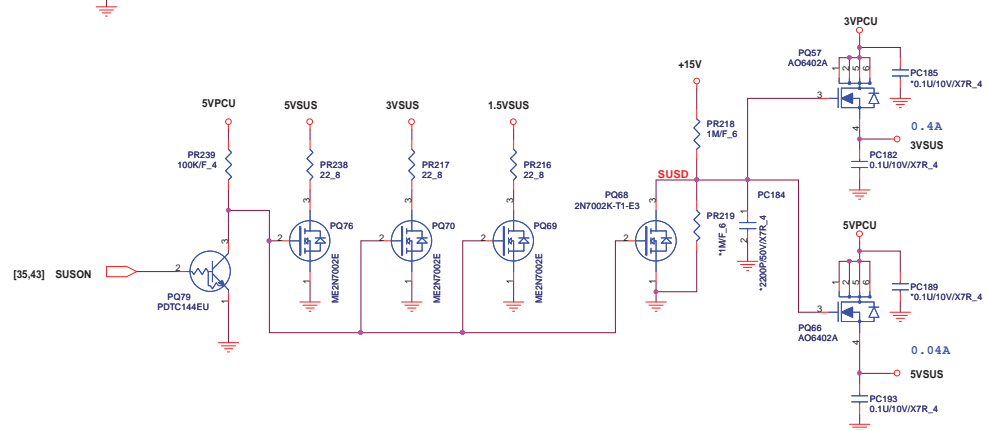
3V_S5, 5V_S5

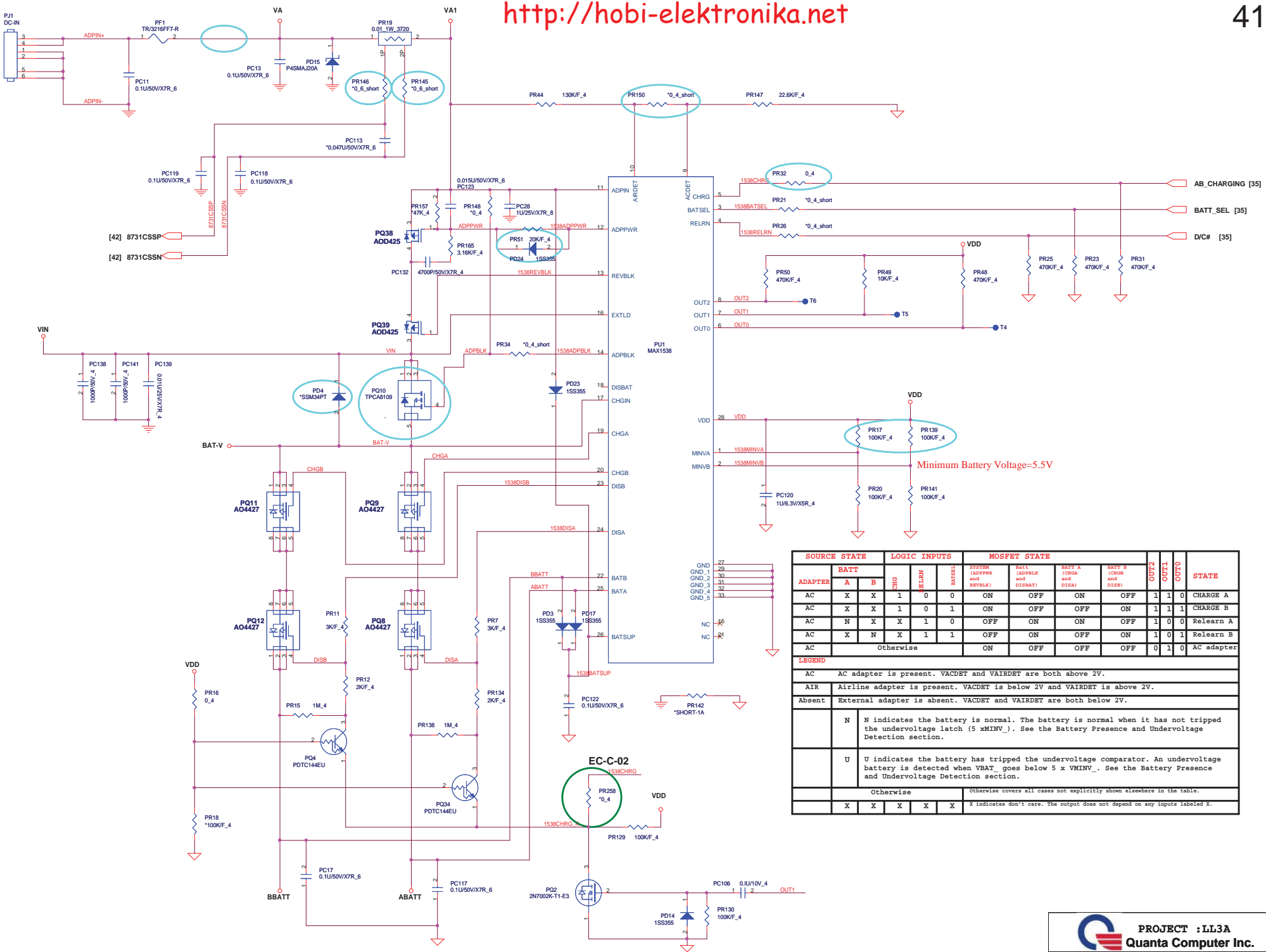


LANVCC



3VSUS, 5VSUS





ADAPTER	BATT		LOGIC INPUTS				MOSFET STATE					STATE
	A	B	CHG	RELEA	BATSEL	SYSTEM (ADPPWR AND REVBLK)	BATT (ADPBLK AND DISBAT)	BATT A (CHGA AND DISA)	BATT B (CHGB AND DISB)	OUT2	OUT1	
AC	X	X	1	0	0	ON	OFF	ON	OFF	1	1	CHARGE A
AC	X	X	1	0	1	ON	OFF	OFF	ON	1	1	CHARGE B
AC	N	X	X	1	0	OFF	ON	ON	OFF	1	0	Relearn A
AC	X	N	X	1	1	OFF	ON	OFF	ON	1	0	Relearn B
AC	Otherwise					ON	OFF	OFF	OFF	0	1	AC adapter

LEGEND

AC AC adapter is present. VACDET and VAIRDET are both above 2V.

AIR Airline adapter is present. VACDET is below 2V and VAIRDET is above 2V.

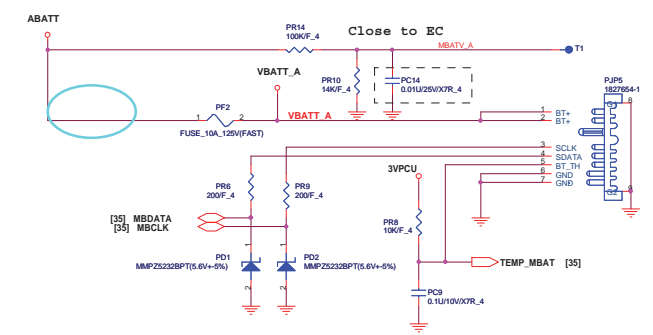
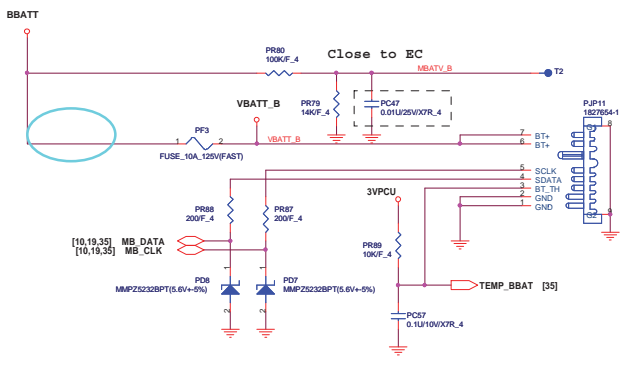
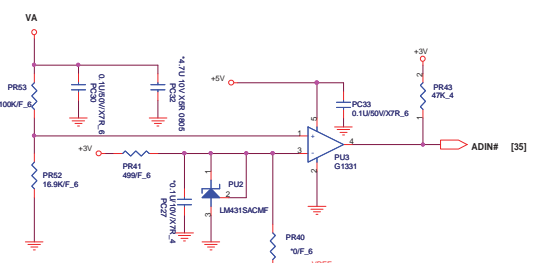
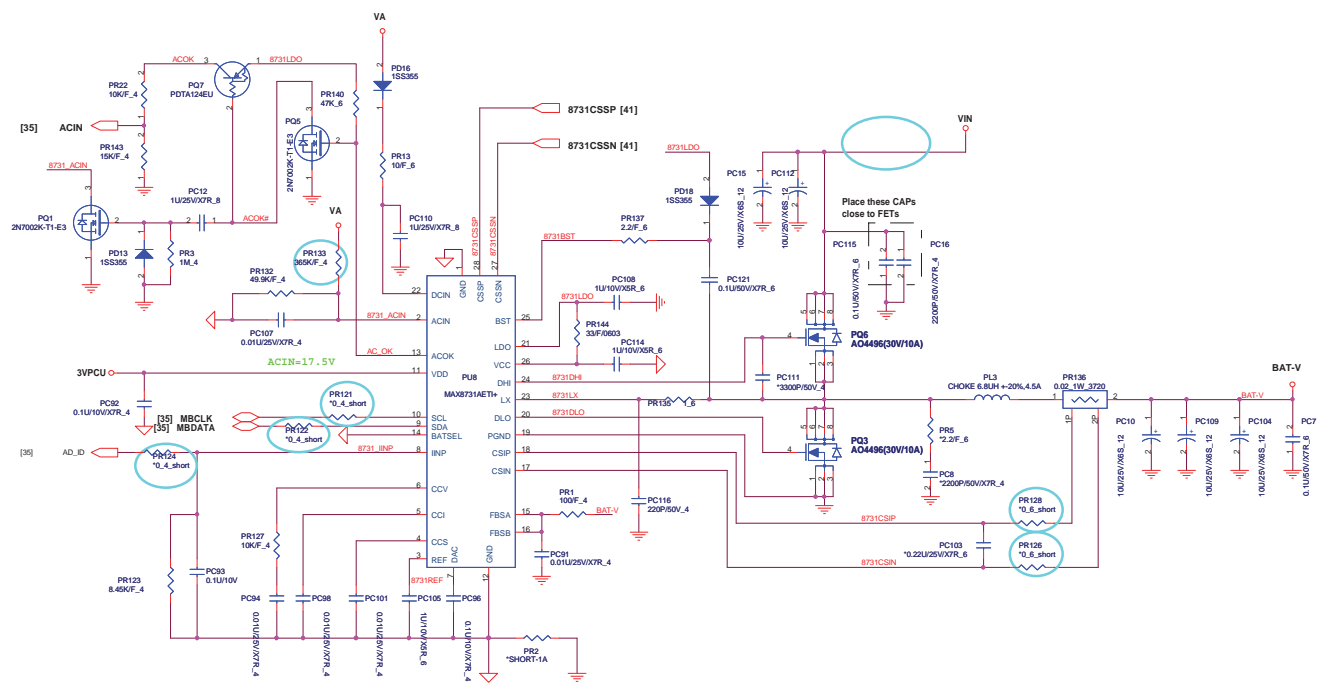
Absent External adapter is absent. VACDET and VAIRDET are both below 2V.

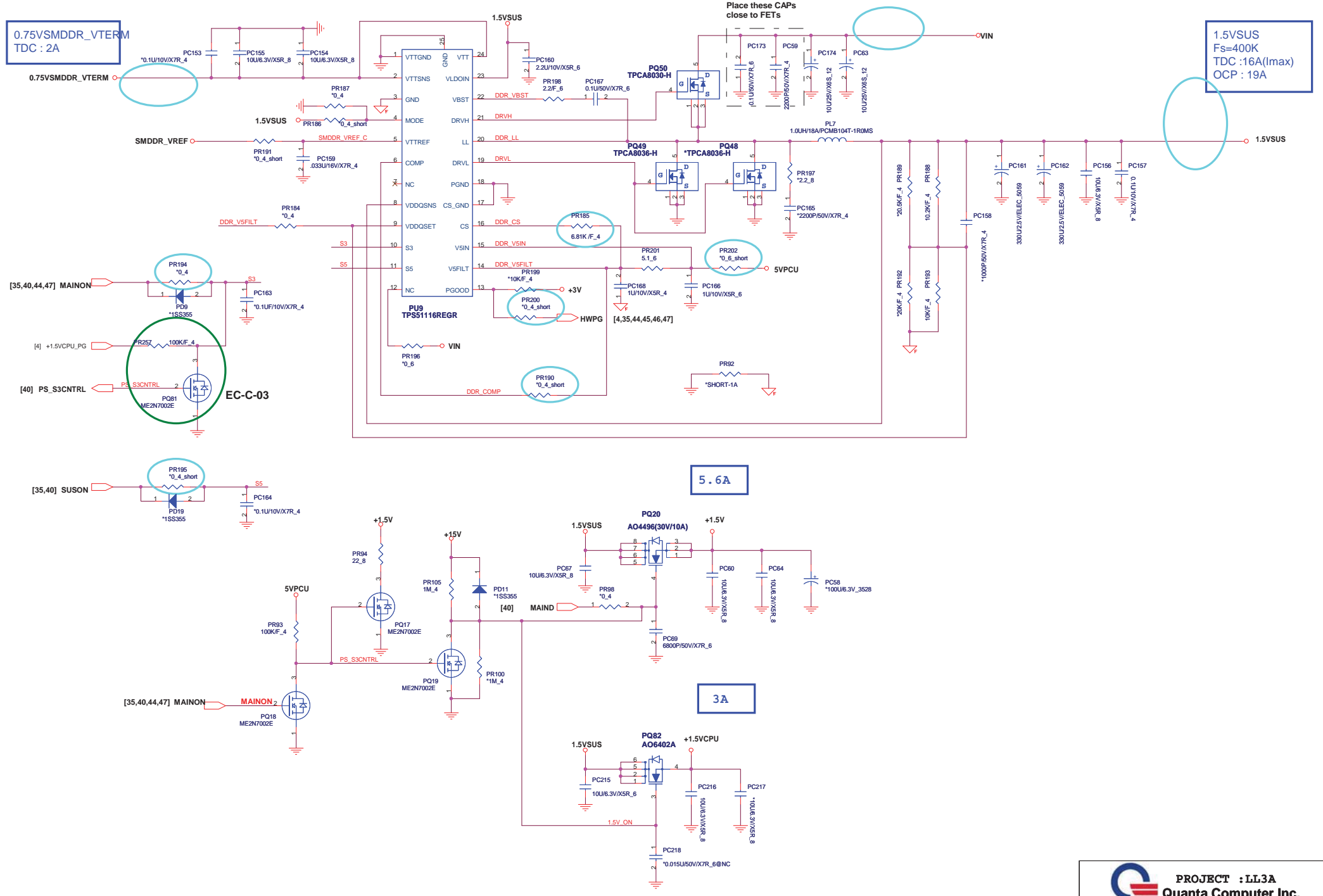
N N indicates the battery is normal. The battery is normal when it has not tripped the undervoltage latch (5 xMINV_). See the Battery Presence and Undervoltage Detection section.

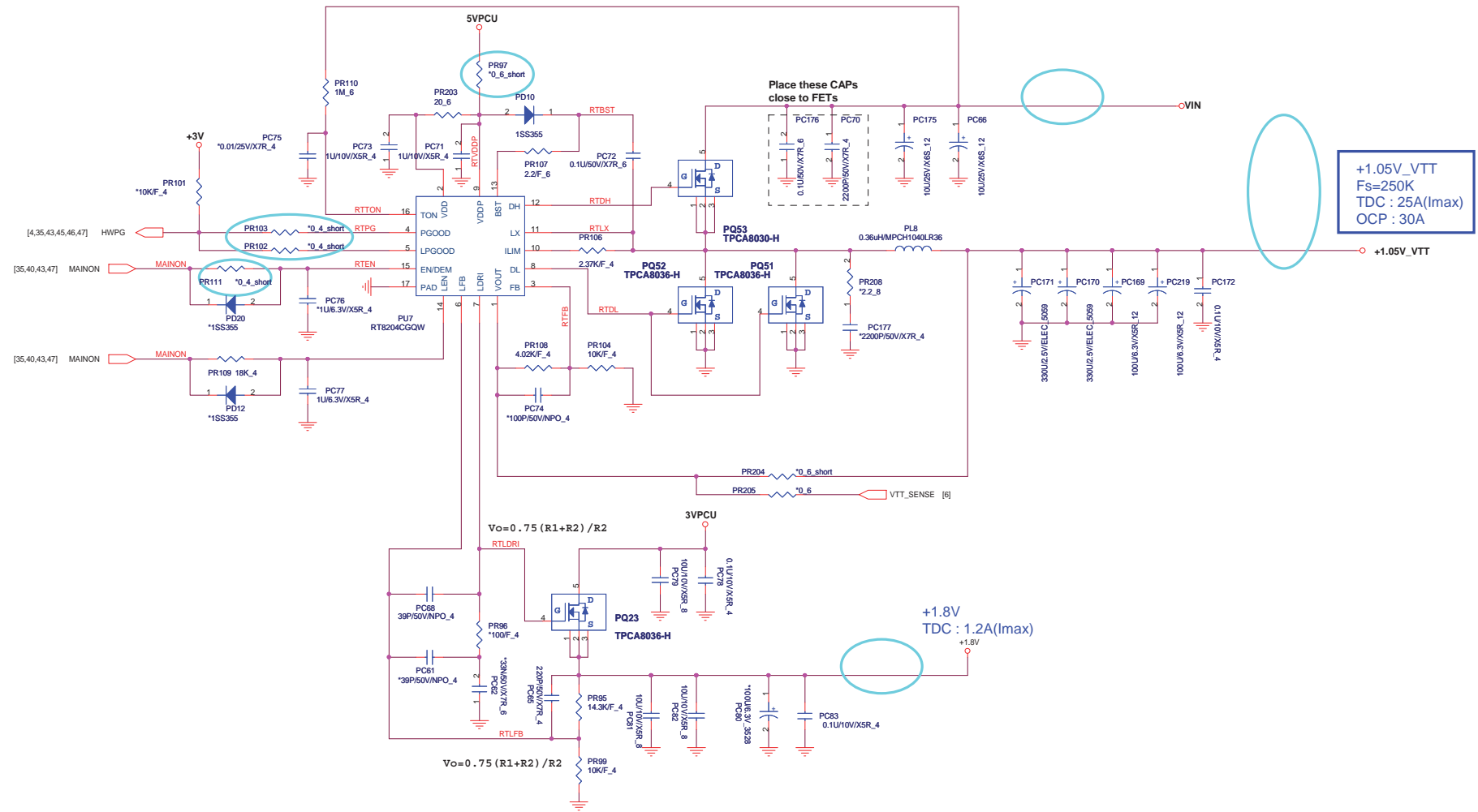
U U indicates the battery has tripped the undervoltage comparator. An undervoltage battery is detected when VBAT goes below 5 xMINV_. See the Battery Presence and Undervoltage Detection section.

Otherwise Otherwise covers all cases not explicitly shown elsewhere in the table.

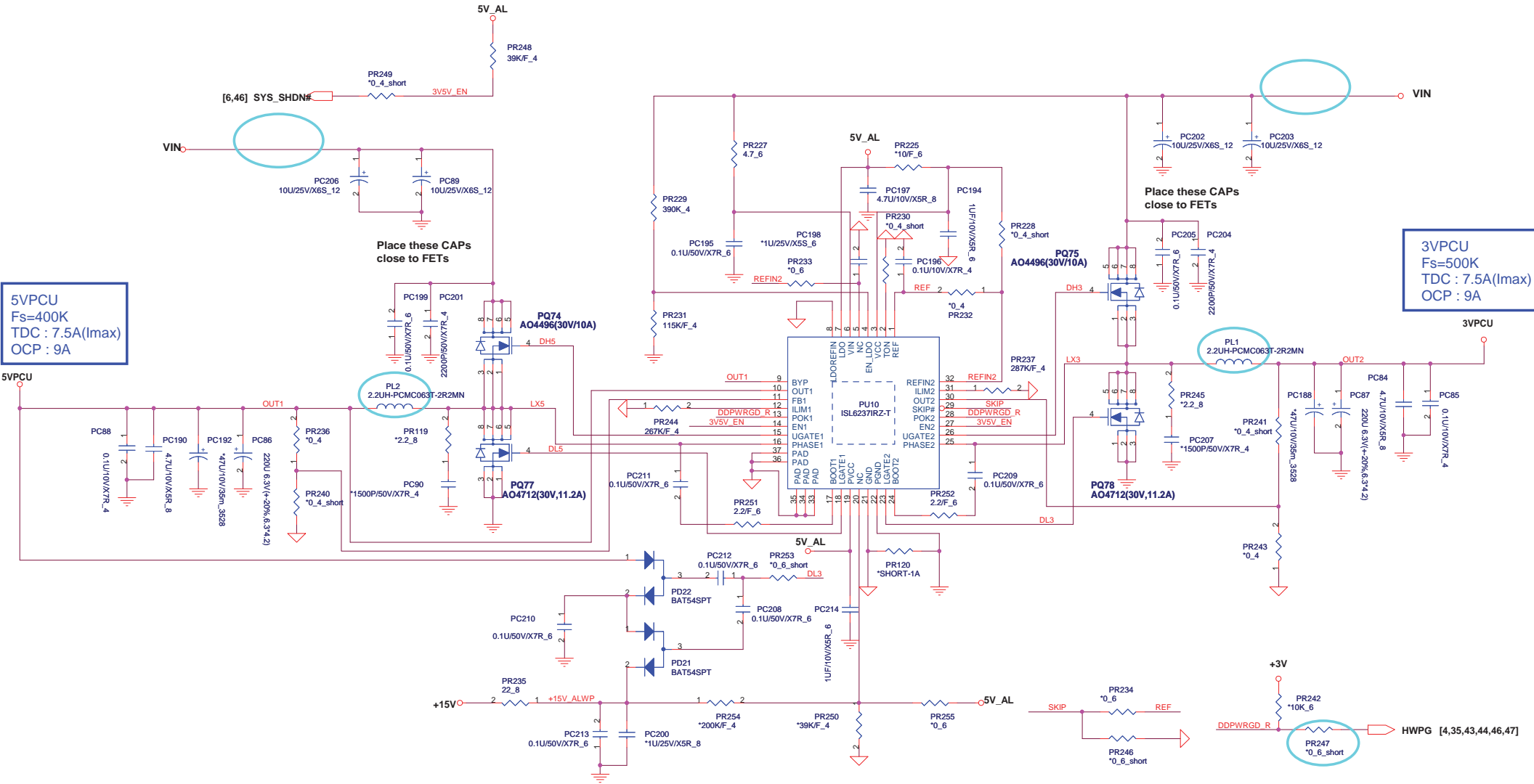
X X indicates don't care. The output does not depend on any inputs labeled X.







[9,22,25,28,35,36,37,39,40,42,44,47] 3VPCU
[9,28,40,43,44,47] 5VPCU
[22,28,40,43] +15V
[22,39,41,42,43,44,46,47] VIN



5VPCU
Fs=400K
TDC : 7.5A(I_{max})
OCP : 9A

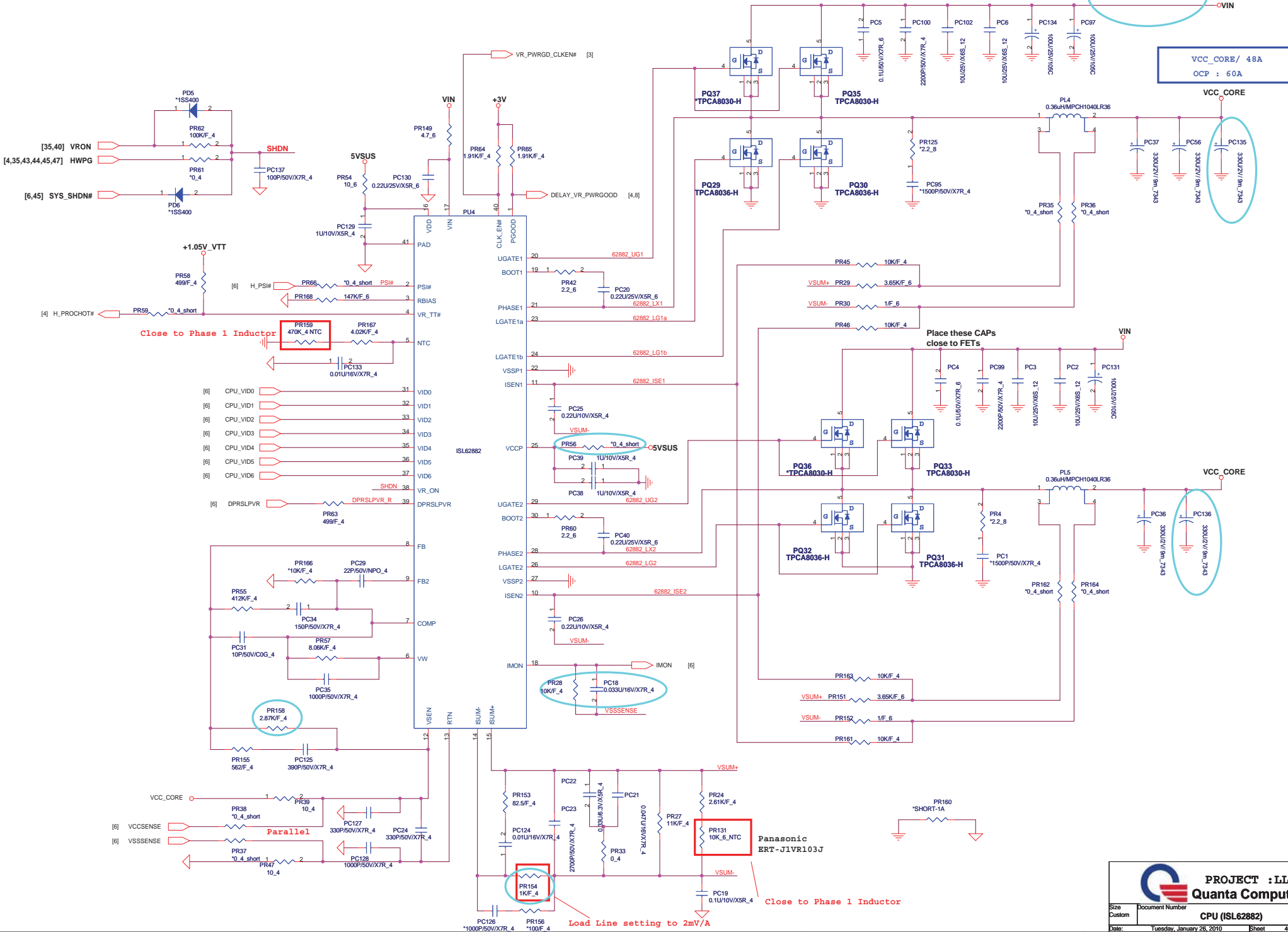
3VPCU
Fs=500K
TDC : 7.5A(I_{max})
OCP : 9A

Place these CAPs close to FETs

Place these CAPs close to FETs

PROJECT : LL3A
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Size Custom	Document Number 3V/5V (ISL6237IRZ-T)	Rev 1E
Date: Tuesday, January 26, 2010	Sheet 45	of 47

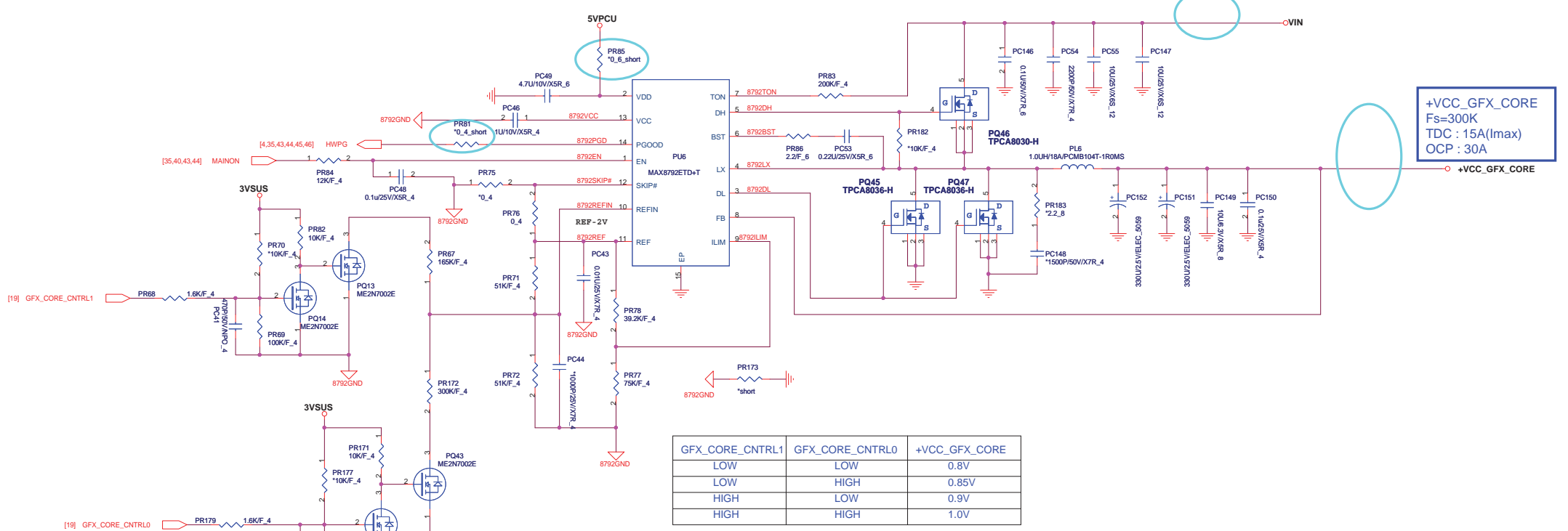


PROJECT : LL3A
Quanta Computer Inc.

Size: Custom Document Number: **CPU (ISL6282)** Rev: IE

Date: Tuesday, January 26, 2010 Sheet: 46 of 47

For Descrete N10M VGA Only



+VCC_GFX_CORE
 Fs=300K
 TDC : 15A(I_{max})
 OCP : 30A

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+VCC_GFX_CORE
LOW	LOW	0.8V
LOW	HIGH	0.85V
HIGH	LOW	0.9V
HIGH	HIGH	1.0V

