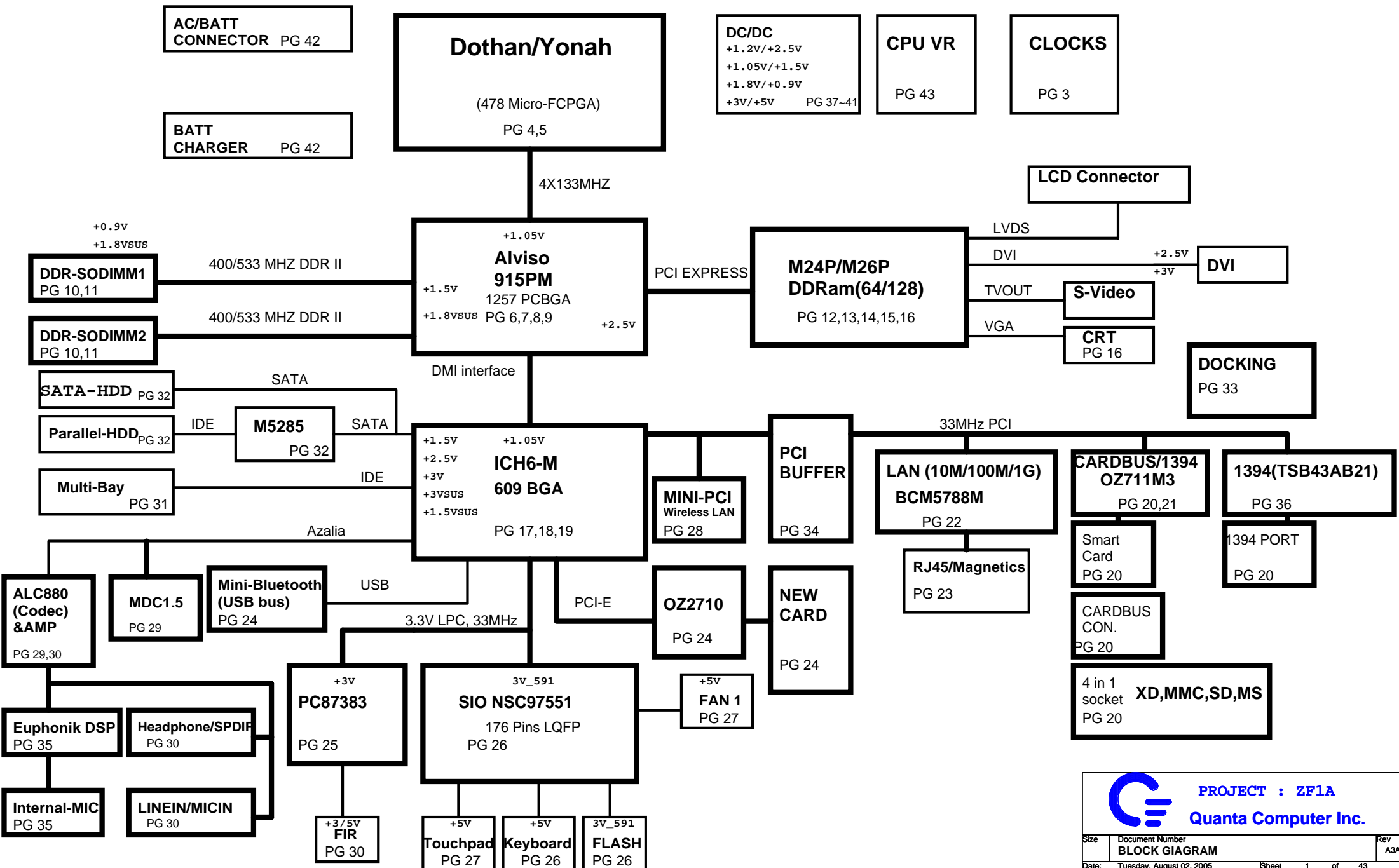


ZF1A



Check again

Change History

Voltage Rails	ON S0-S1	ON S3	ON S4	ON S5	Control signal
12VOUT	X	X	X	X	
3V_591	X	X	X	X	
5VPCU	X	X	X	X	
+3V_S5	X	X	X	X	S5_ON
3V_LAN	X	X	X	X	
+1.5V_S5	X	X	X	X	S5_ON
+1.8VSUS	X	X			SUS_ON
+3VSUS	X	X			SUSD
+5VSUS	X	X			SUSD
SMDDDR_VTERM DDR Termination voltage	X	X			MAINON
SMDDDR_VREF	X				MAINON
VGA_PCIE_1.2V	X				MAINON
VCC_CORE Core voltage for Processor	X				VR_ON
+VCCP 1.05V rail for Processor I/O	X				MAINON
+1.5V	X				MAINON
+1.8V	X				MAIND
+2.5V	X				MAIND
+3V	X				MAIND
+5V					MAIND
+12V	X				MAINON
+3VRUN	X				PCI_Switch_Power_ON
+5VRUN	X				PCI_Switch_Power_ON

- 5/28
- System DVI DET function move in EZ port . So,Del Q47,R557
 - Addition AND gate for DOCKING Power Good AND DockingIN Singal combine Circuit
 - Addition Power led circuit for system
 - Change D34 AND D35 + -
 - Addition LID Switch and LID connector
 - Addition RC Delay for PCIE1.2V
 - Change EC Three GPIO port same to ZL2
- 5/31
- Change C145 PCB Footprint to 3528
 - Combine USB and bluetooth connector to 19pin connector 87212-1900
 - Change PCBFootprint 88216-1200 to 88213-1200
 - Change USB connector bypass C to D805 10u
 - Adjulst 80pin connector 3 singal
- 6/1
- Update power all circuit for GND name
 - Addition OR to PRST
 - Change IDE RST
- 6/2
- Change ICH-6 USB Port
 - Del CDR,CDL,CDGND Singal and DEL prevent CDR,CDL,CDGND noise circuit.
- 6/4
- U49,U50 Form 3VRUN change to +3V AND CHANGE MINPCI connector to PCI BUS,And addition PCI_SWRST # AND PCI_SWRST1#
 - Change BT_POWER NAME
 - Change VOIP AGND
- 6/7
- Change VOIP AGND TO AGND2 for Layout

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus+Smart Card	AD25	1	PIRQC/B
Mini-PCI	AD19	2	PIRQB/D
LAN	AD22	0	PIRQA
1394	AD23	3	PIRQD

EC SM Bus1 address


Device

- Smart Battery
- THERMAL SENSOR
- LIGHT SENER
- VOIP FLASH ROM

ICH6-M SM Bus address

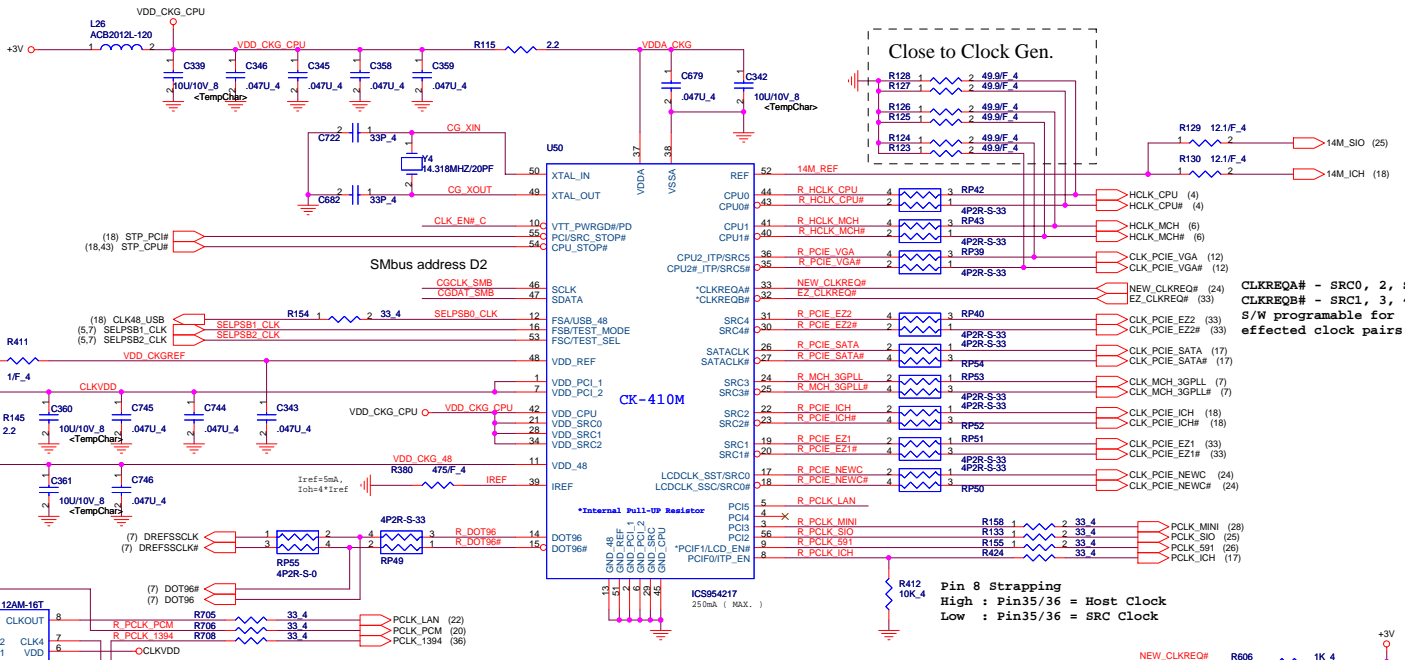
Device

- SODIMM 1010 000X b
- Clock Gen 1101 001x b



PROJECT : ZF1A
Quanta Computer Inc.

Size	Document Number	Rev
SYSTEM INFO		A3A
Date:	Tuesday, August 02, 2005	Sheet 2 of 43



Close to Clock Gen.

Pin 8 Strapping
High : Pin35/36 = Host Clock
Low : Pin35/36 = SRC Clock

Resistor Stuff Table

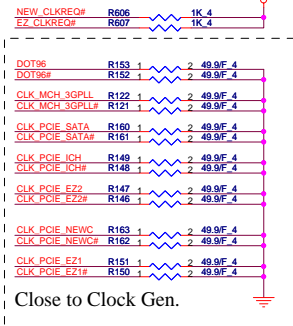
	RA	RB	RC	RD
Dothan A 400	V	X	X	V
Dothan A 533	X	V	X	V
Dothan B	X	X	X	X

Clock Gen. Frequency Selection Table

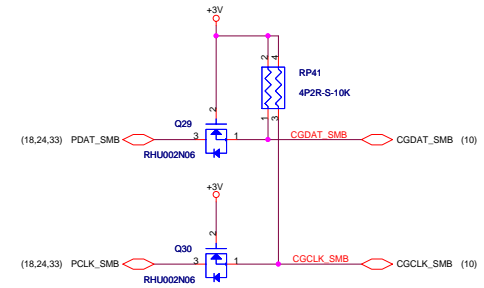
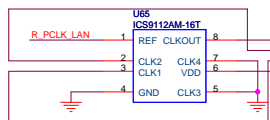
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

DOTHAN BSEL Output Value

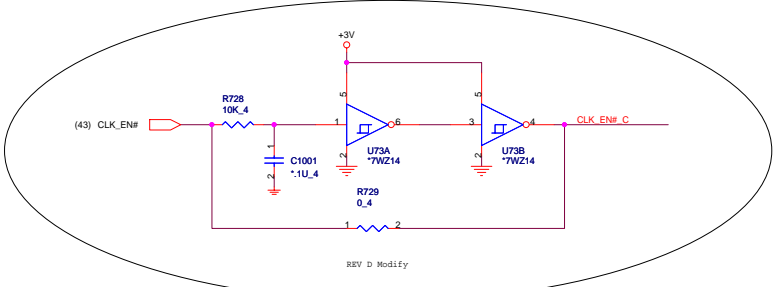
FSB Frequency	DOTHAN A-Step		DOTHAN B-Step	
	BSEL1	BSEL0	BSEL1	BSEL0
400 MHz	0	0	0	1
533 MHz	0	1	0	0



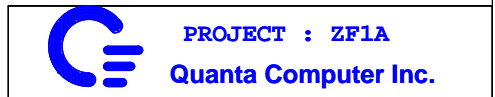
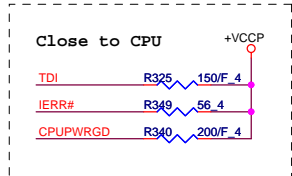
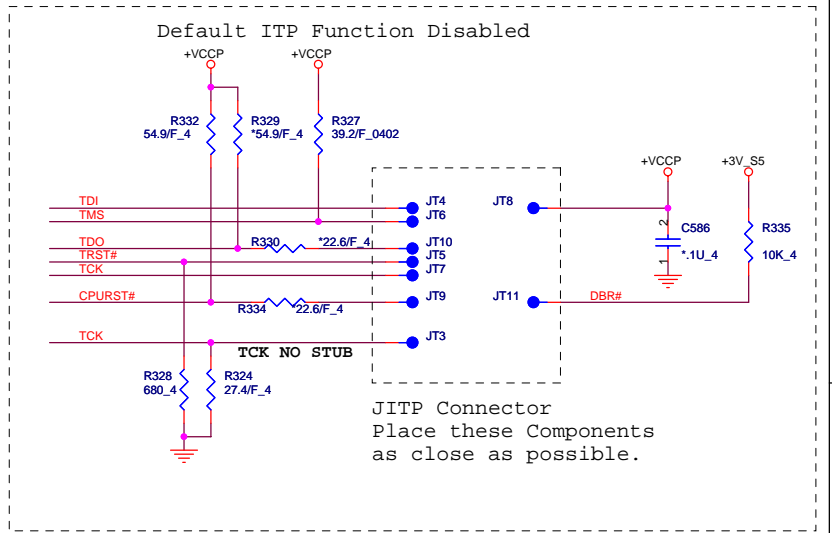
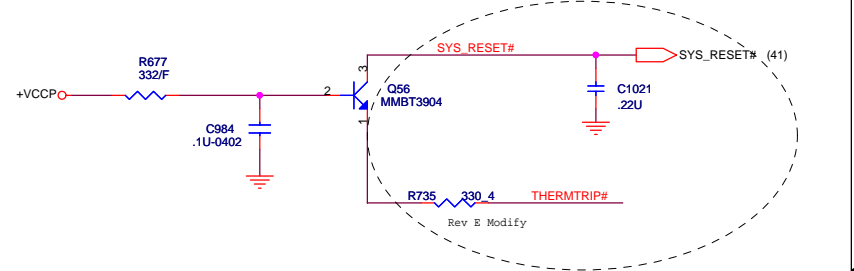
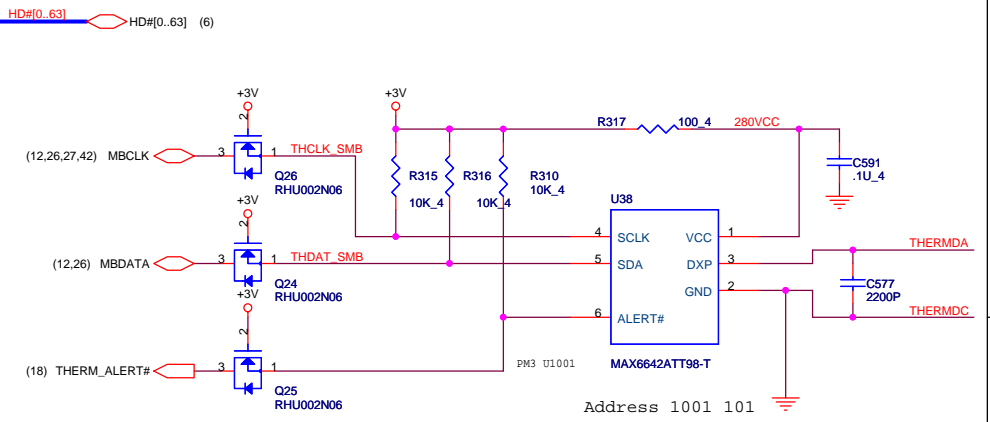
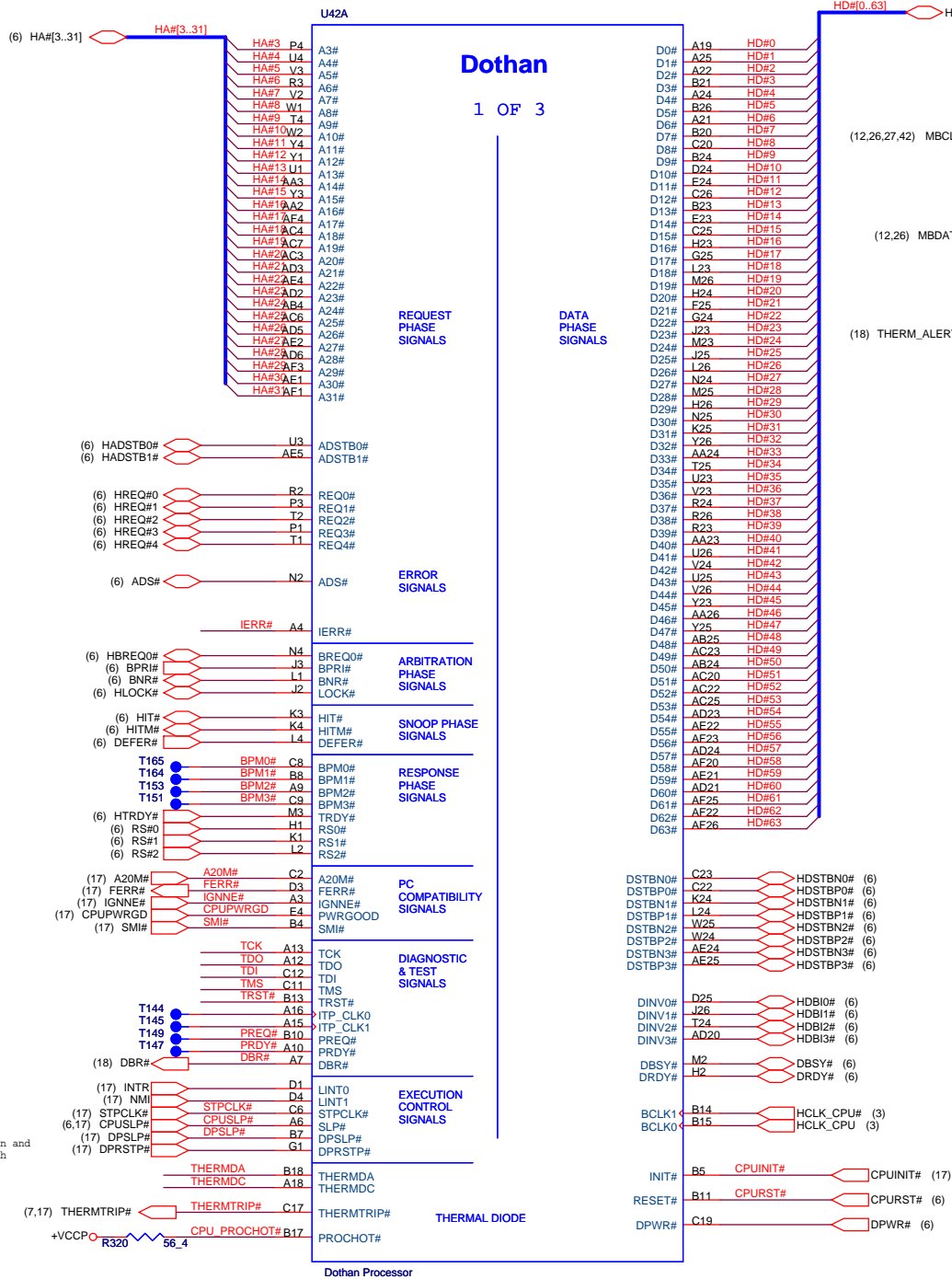
Close to Clock Gen.

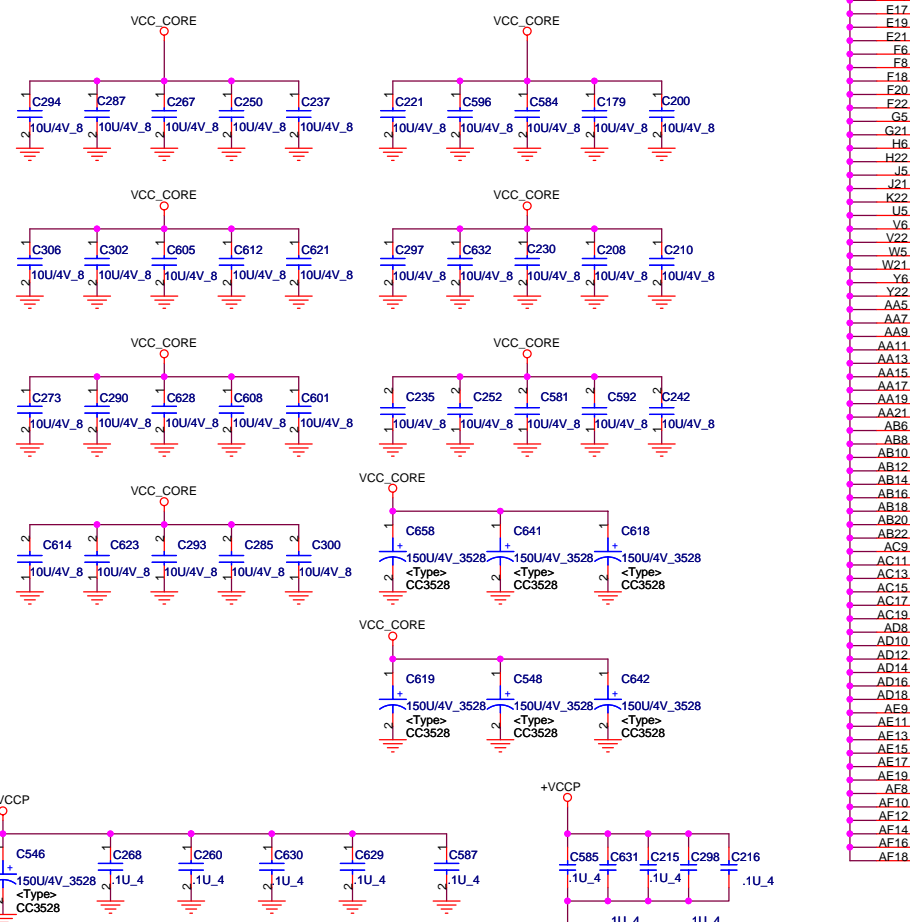
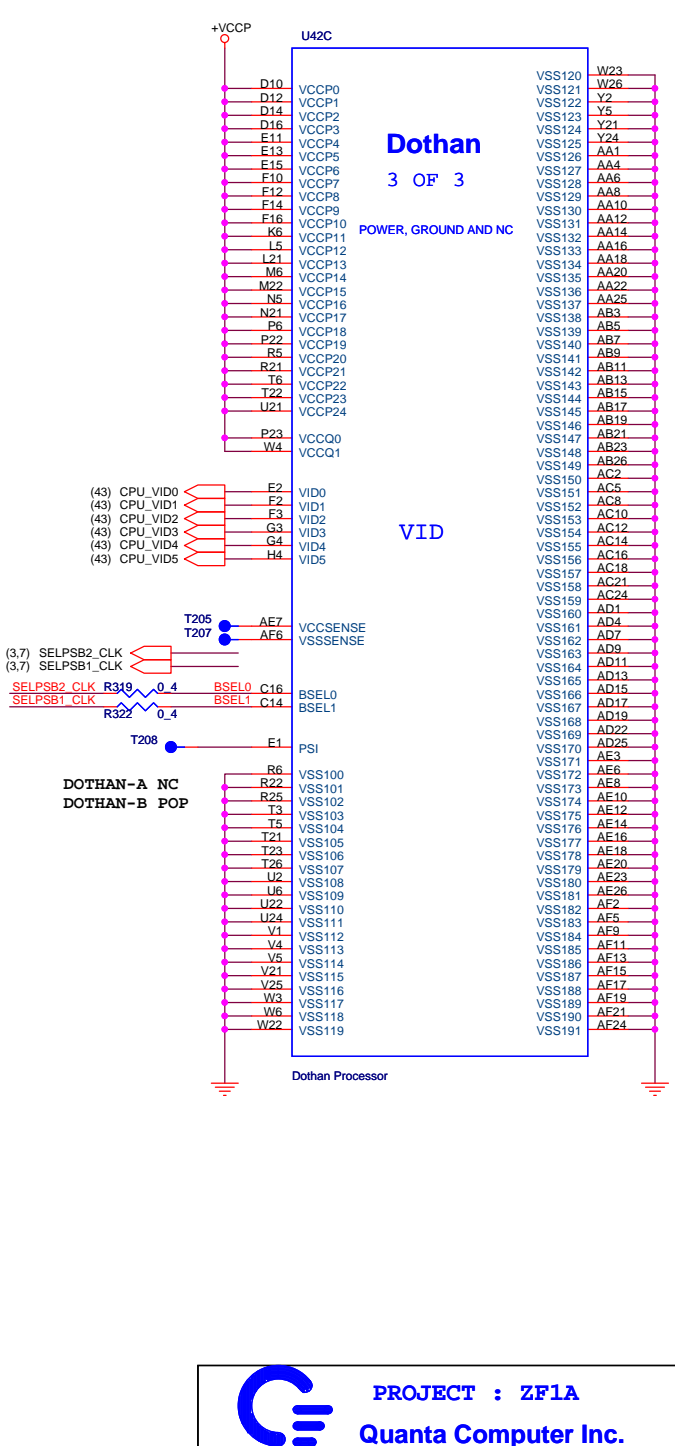
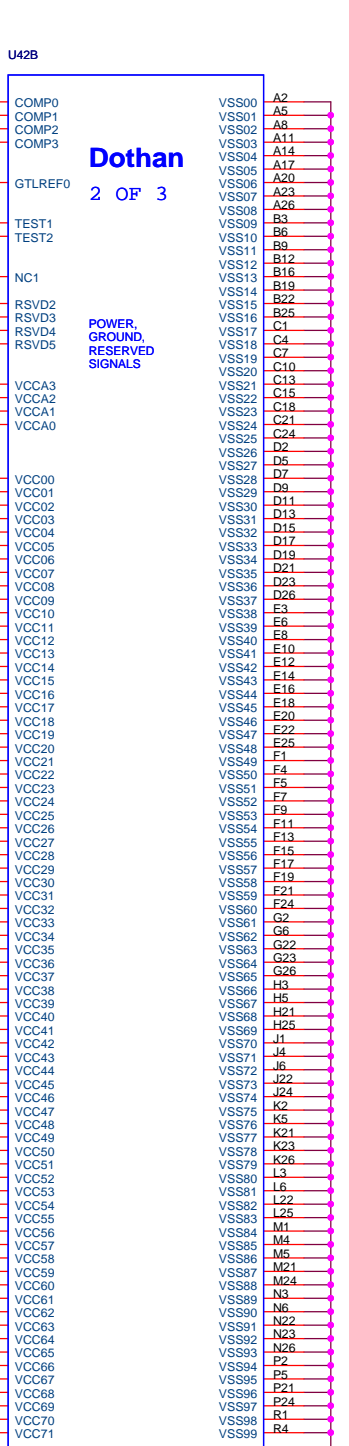
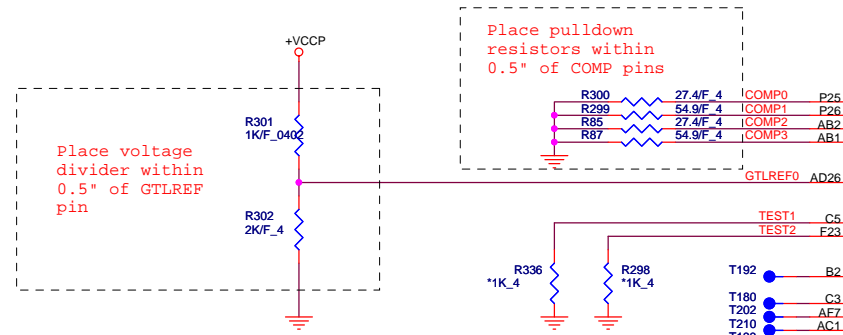


These are for backdrive issue



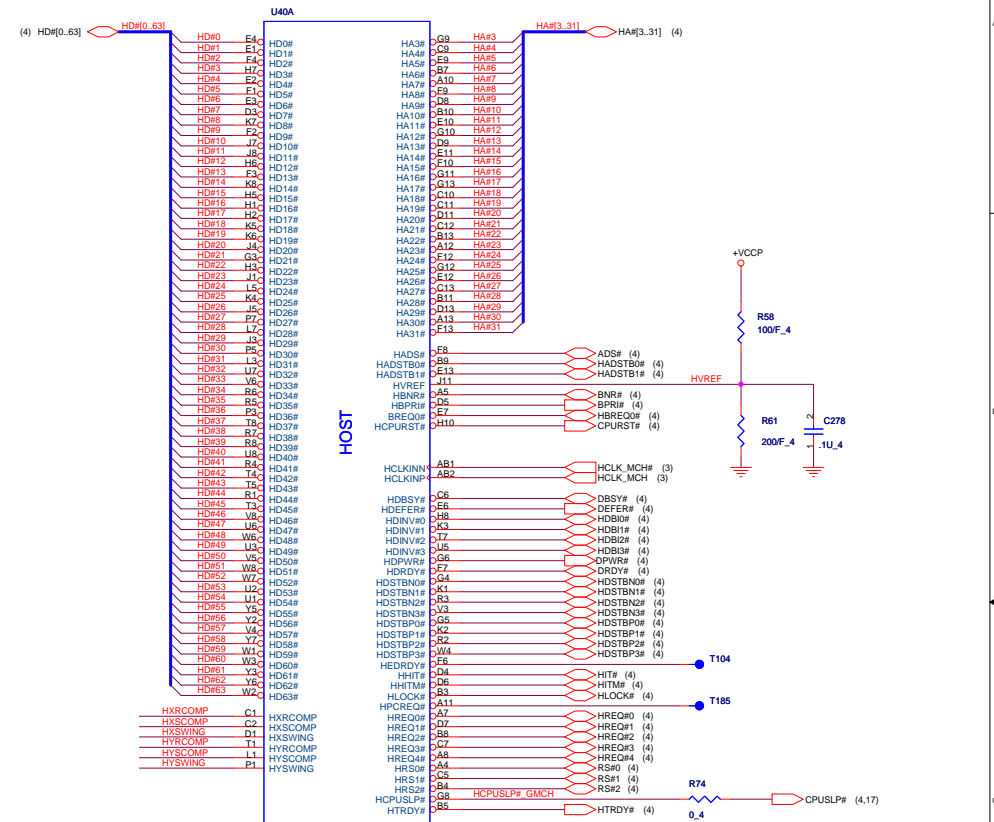
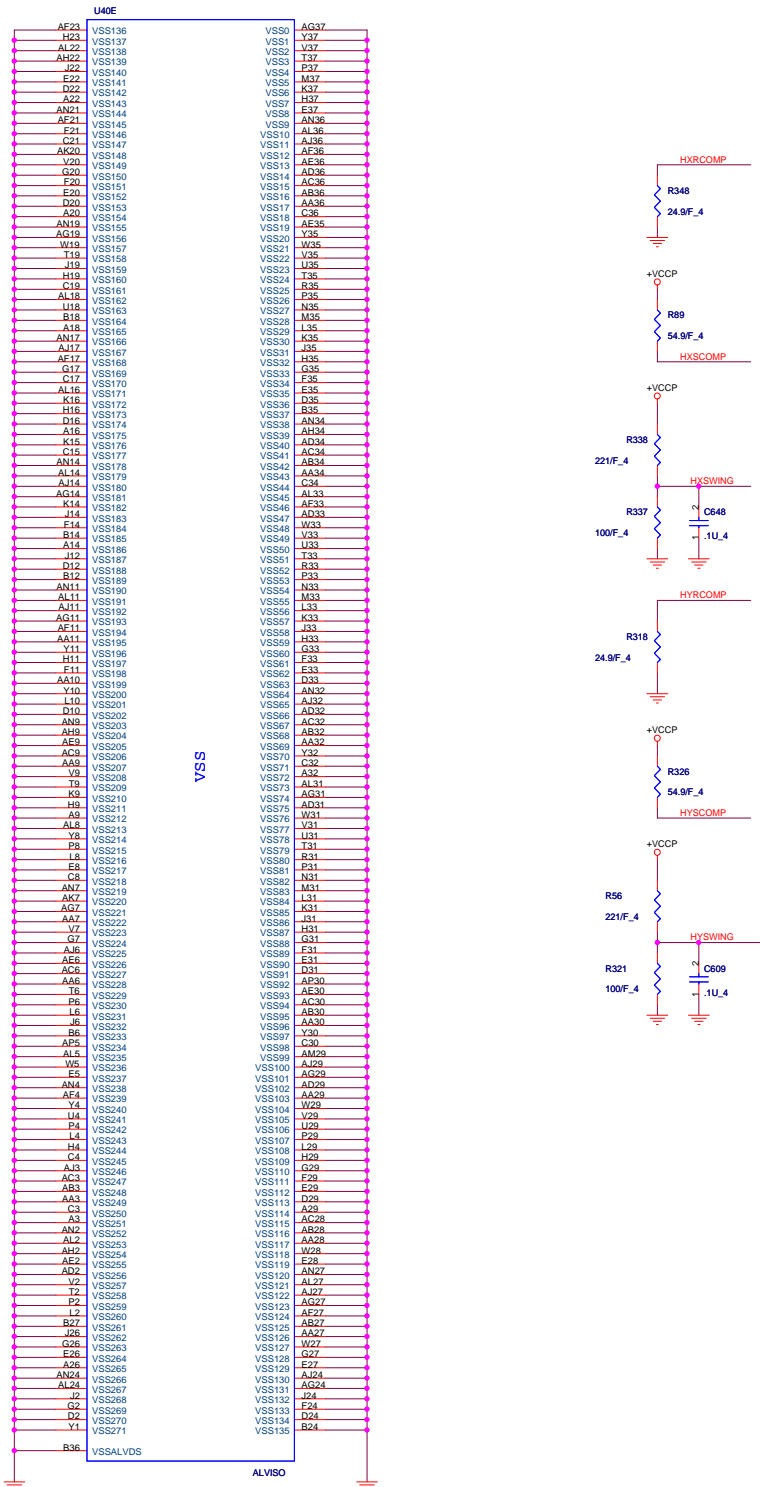
REV D Modify





PROJECT : ZF1A
Quanta Computer Inc.

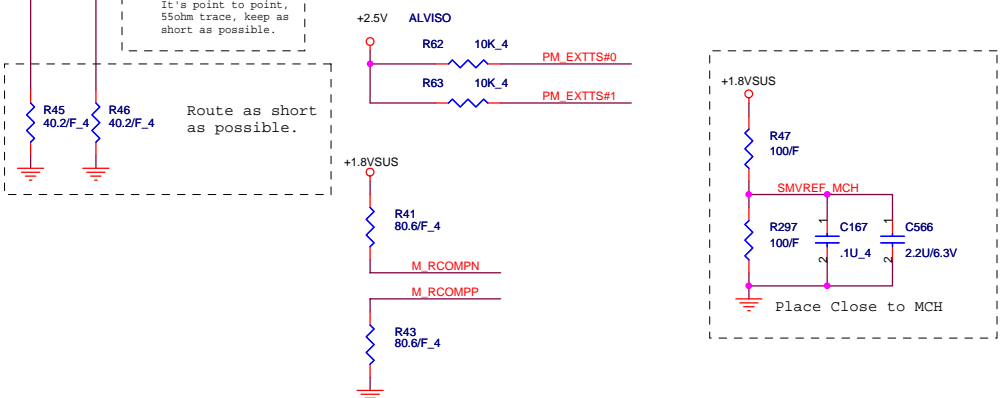
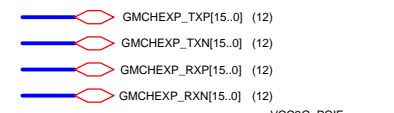
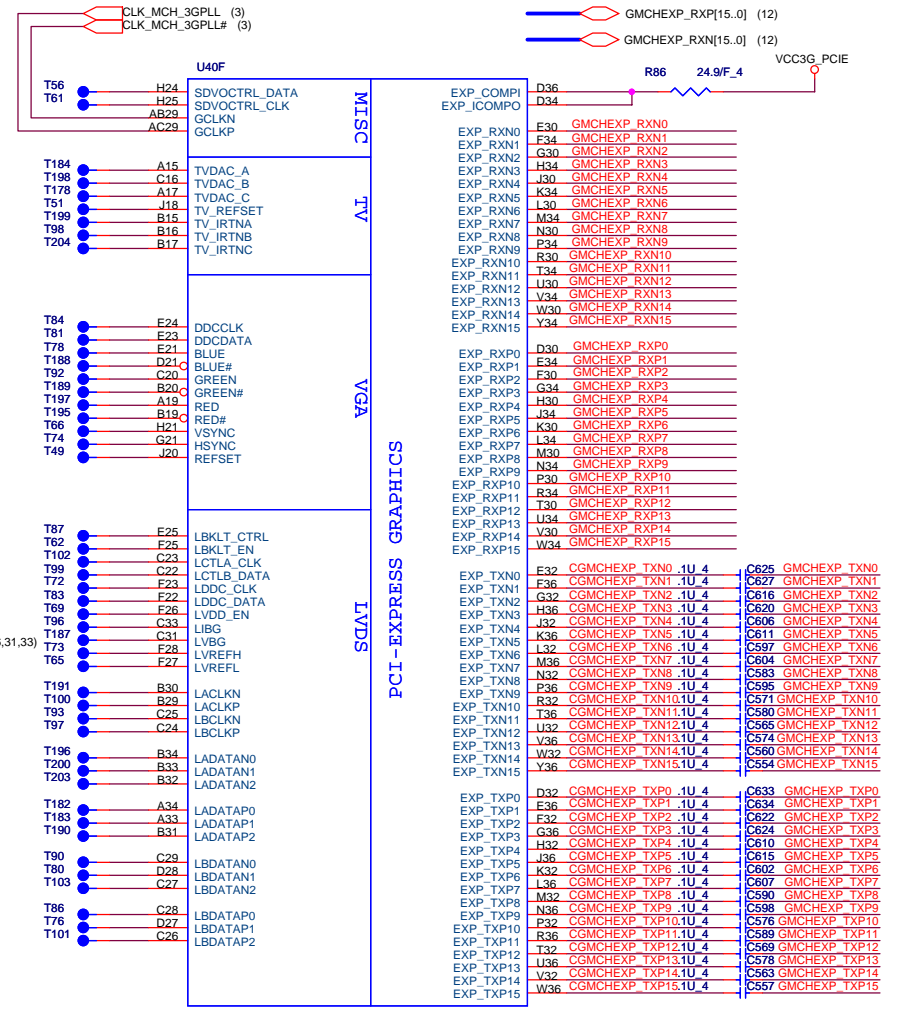
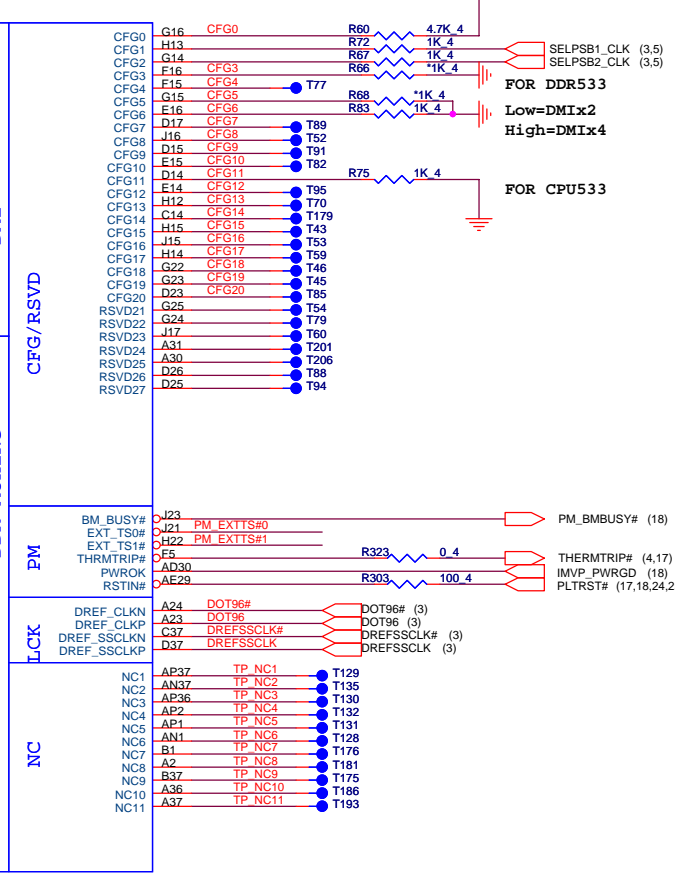
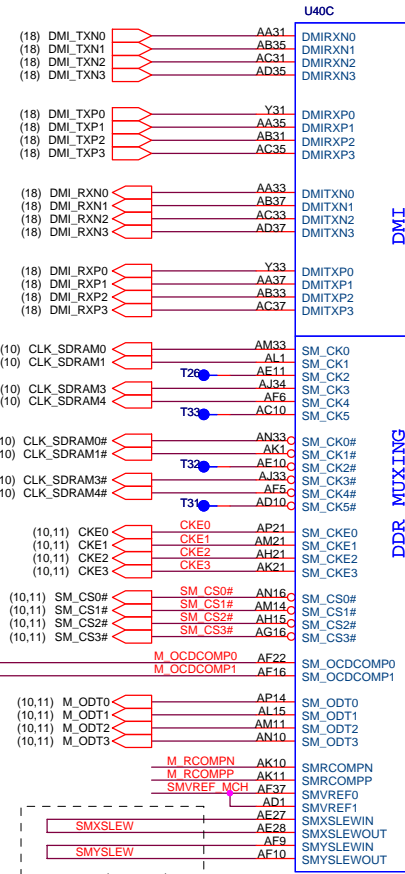
Size	Document Number	Rev
	Dothan Power & NC	A3A
Date:	Tuesday, August 02, 2005	Sheet 5 of 43



PROJECT : ZF1A
Quanta Computer Inc.

Size	Document Number	Rev
	Alviso Host	A3A
Date:	Tuesday, August 02, 2005	Sheet 6 of 43

CFG[0:2]=100 FOR FSB 533
 CFG[0:2]=101 FOR FSB 400



PROJECT : ZFLA
Quanta Computer Inc.

Size Document Number Rev
 Alviso DMI & PCIE ASA

Date: Tuesday, August 02, 2005 Sheet 7 of 43

(10) R_A_MD[0..63]

R A MD0	AG35	SADO0
R A MD1	AH35	SADO1
R A MD2	AL35	SADO2
R A MD3	AL37	SADO3
R A MD4	AH36	SADO4
R A MD5	AJ35	SADO5
R A MD6	AK37	SADO6
R A MD7	AL34	SADO7
R A MD8	AM36	SADO8
R A MD9	AN35	SADO9
R A MD10	AP32	SADO10
R A MD11	AM31	SADO11
R A MD12	AM34	SADO12
R A MD13	AM35	SADO13
R A MD14	AL32	SADO14
R A MD15	AM32	SADO15
R A MD16	AN31	SADO16
R A MD17	AP31	SADO17
R A MD18	AN28	SADO18
R A MD19	AP28	SADO19
R A MD20	AL30	SADO20
R A MD21	AM30	SADO21
R A MD22	AM28	SADO22
R A MD23	AL28	SADO23
R A MD24	AP27	SADO24
R A MD25	AM27	SADO25
R A MD26	AM23	SADO26
R A MD27	AM22	SADO27
R A MD28	AL23	SADO28
R A MD29	AM24	SADO29
R A MD30	AN22	SADO30
R A MD31	AP22	SADO31
R A MD32	AM19	SADO32
R A MD33	AL9	SADO33
R A MD34	AL6	SADO34
R A MD35	AP7	SADO35
R A MD36	AP11	SADO36
R A MD37	AP10	SADO37
R A MD38	AL7	SADO38
R A MD39	AM7	SADO39
R A MD40	AN5	SADO40
R A MD41	AN6	SADO41
R A MD42	AN3	SADO42
R A MD43	AP3	SADO43
R A MD44	AP6	SADO44
R A MD45	AM6	SADO45
R A MD46	AL4	SADO46
R A MD47	AM3	SADO47
R A MD48	AK2	SADO48
R A MD49	AK3	SADO49
R A MD50	AG2	SADO50
R A MD51	AG1	SADO51
R A MD52	AL3	SADO52
R A MD53	AM2	SADO53
R A MD54	AH3	SADO54
R A MD55	AG3	SADO55
R A MD56	AF3	SADO56
R A MD57	AE3	SADO57
R A MD58	AD6	SADO58
R A MD59	AC4	SADO59
R A MD60	AF2	SADO60
R A MD61	AF1	SADO61
R A MD62	AD4	SADO62
R A MD63	AD5	SADO63

DDR SYSTEM MEMORY A

SA_BS0#	AK15	R A BS0#	R_A_BS0# (10,11)
SA_BS1#	AK16	R A BS1#	R_A_BS1# (10,11)
SA_BS2#	AL21	R A BS2#	R_A_BS2# (10,11)
SA_DM0	AJ37	R A DM0	R_A_DM[0..7] (10)
SA_DM1	AP35	R A DM1	
SA_DM2	AL29	R A DM2	
SA_DM3	AP24	R A DM3	
SA_DM4	AP9	R A DM4	
SA_DM5	AP4	R A DM5	
SA_DM6	AJ2	R A DM6	
SA_DM7	AD3	R A DM7	
SA_DQS0	AK36	R A DQS0	R_A_DQS[0..7] (10)
SA_DQS1	AP33	R A DQS1	
SA_DQS2	AN29	R A DQS2	
SA_DQS3	AP23	R A DQS3	
SA_DQS4	AM8	R A DQS4	
SA_DQS5	AM4	R A DQS5	
SA_DQS6	AJ1	R A DQS6	
SA_DQS7	AE5	R A DQS7	
SA_DQS0#	AK35	R A DQS#0	R_A_DQS#[0..7] (10)
SA_DQS1#	AP34	R A DQS#1	
SA_DQS2#	AN30	R A DQS#2	
SA_DQS3#	AN23	R A DQS#3	
SA_DQS4#	AM8	R A DQS#4	
SA_DQS5#	AM5	R A DQS#5	
SA_DQS6#	AH1	R A DQS#6	
SA_DQS7#	AE4	R A DQS#7	
SA_MA0	AL17	R A MA0	R_A_MA[0..13] (10,11)
SA_MA1	AP17	R A MA1	
SA_MA2	AP18	R A MA2	
SA_MA3	AM17	R A MA3	
SA_MA4	AN18	R A MA4	
SA_MA5	AM18	R A MA5	
SA_MA6	AL19	R A MA6	
SA_MA7	AP20	R A MA7	
SA_MA8	AM19	R A MA8	
SA_MA9	AL20	R A MA9	
SA_MA10	AM16	R A MA10	
SA_MA11	AN20	R A MA11	
SA_MA12	AM20	R A MA12	
SA_MA13	AM15	R A MA13	
SA_CAS#	AN15	R A SCASA#	R_A_SCASA# (10,11)
SA_RAS#	AP16	R A SRASA#	R_A_SRASA# (10,11)
SA_RCVENIN#	AE29	SA RCVENIN#	
SA_RCVENOUT#	AE28	SA RCVENOUT#	
SA_WE#	AP15	R A BMWEA#	R_A_BMWEA# (10,11)

ALVISO

(10) R_B_MD[0..63]

R B MD0	AE31	SBDQ0
R B MD1	AE32	SBDQ1
R B MD2	AG32	SBDQ2
R B MD3	AG36	SBDQ3
R B MD4	AE34	SBDQ4
R B MD5	AE33	SBDQ5
R B MD6	AF31	SBDQ6
R B MD7	AF30	SBDQ7
R B MD8	AH33	SBDQ8
R B MD9	AH32	SBDQ9
R B MD10	AK31	SBDQ10
R B MD11	AG30	SBDQ11
R B MD12	AG33	SBDQ12
R B MD13	AG33	SBDQ13
R B MD14	AH31	SBDQ14
R B MD15	AJ31	SBDQ15
R B MD16	AK30	SBDQ16
R B MD17	AJ30	SBDQ17
R B MD18	AH28	SBDQ18
R B MD19	AH28	SBDQ19
R B MD20	AK29	SBDQ20
R B MD21	AH30	SBDQ21
R B MD22	AH27	SBDQ22
R B MD23	AG28	SBDQ23
R B MD24	AF24	SBDQ24
R B MD25	AG23	SBDQ25
R B MD26	AJ22	SBDQ26
R B MD27	AK22	SBDQ27
R B MD28	AH24	SBDQ28
R B MD29	AH23	SBDQ29
R B MD30	AG22	SBDQ30
R B MD31	AJ21	SBDQ31
R B MD32	AG10	SBDQ32
R B MD33	AG9	SBDQ33
R B MD34	AG8	SBDQ34
R B MD35	AH8	SBDQ35
R B MD36	AH11	SBDQ36
R B MD37	AH10	SBDQ37
R B MD38	AJ8	SBDQ38
R B MD39	AK9	SBDQ39
R B MD40	AJ7	SBDQ40
R B MD41	AK6	SBDQ41
R B MD42	AJ4	SBDQ42
R B MD43	AH6	SBDQ43
R B MD44	AK8	SBDQ44
R B MD45	AJ8	SBDQ45
R B MD46	AJ5	SBDQ46
R B MD47	AK4	SBDQ47
R B MD48	AG5	SBDQ48
R B MD49	AG4	SBDQ49
R B MD50	AD8	SBDQ50
R B MD51	AH4	SBDQ51
R B MD52	AD9	SBDQ52
R B MD53	AG6	SBDQ53
R B MD54	AE8	SBDQ54
R B MD55	AD7	SBDQ55
R B MD56	AC5	SBDQ56
R B MD57	AB8	SBDQ57
R B MD58	AB6	SBDQ58
R B MD59	AC8	SBDQ59
R B MD60	AC8	SBDQ60
R B MD61	AC7	SBDQ61
R B MD62	AA4	SBDQ62
R B MD63	AA5	SBDQ63

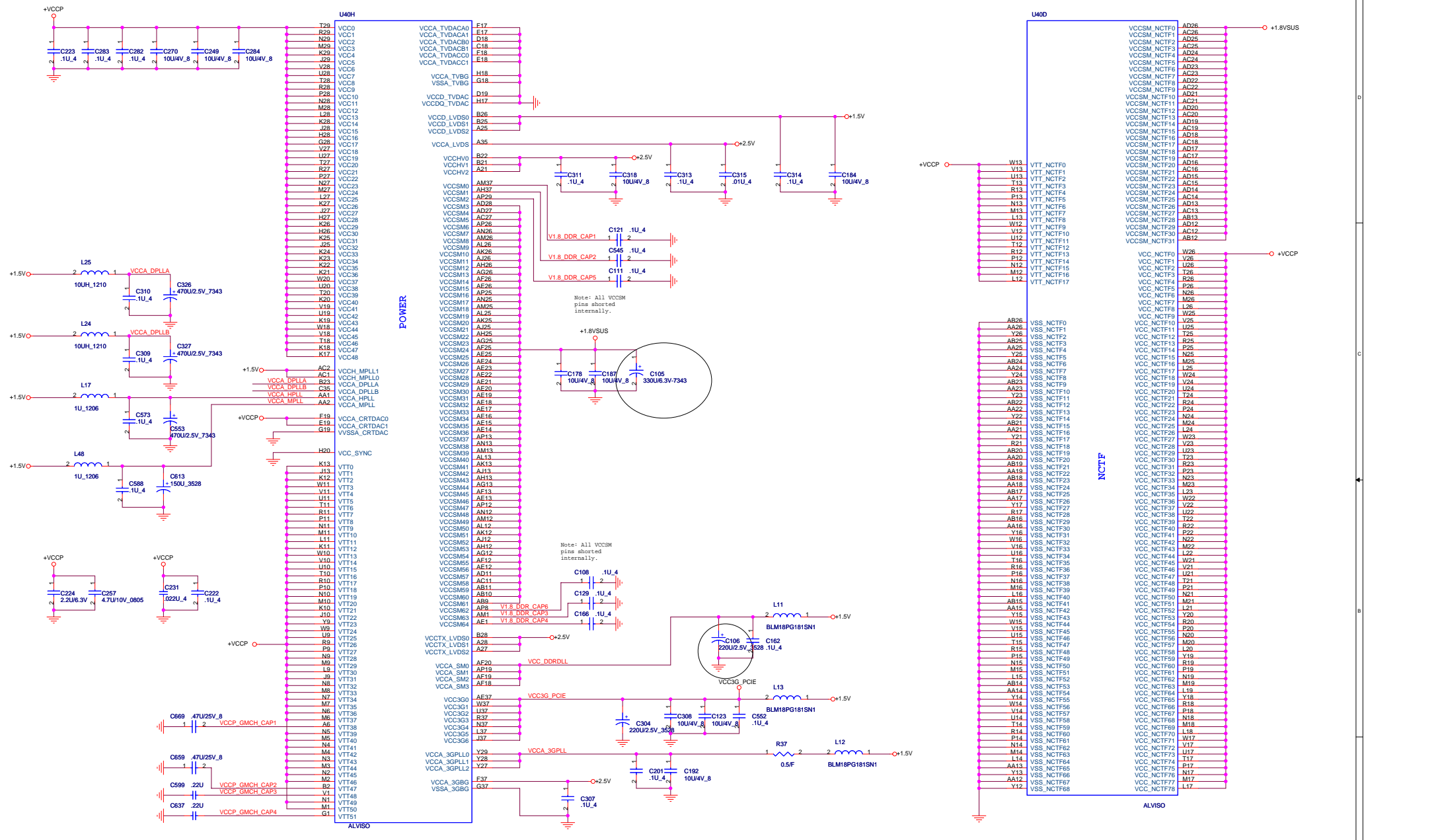
DDR SYSTEM MEMORY B

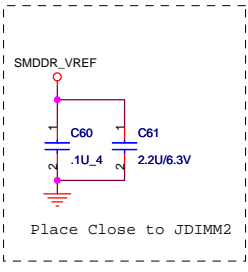
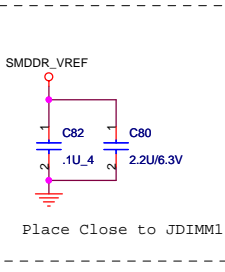
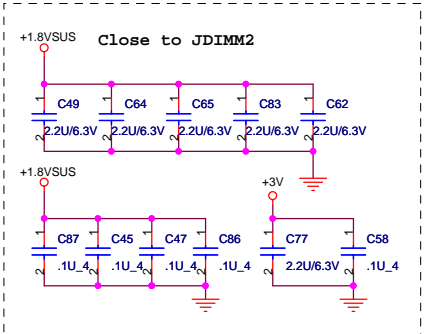
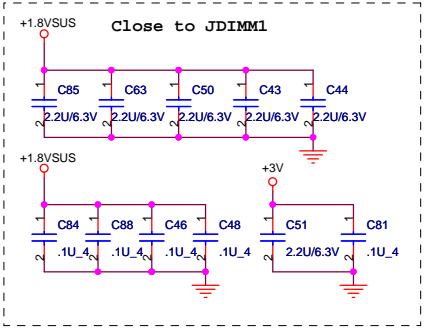
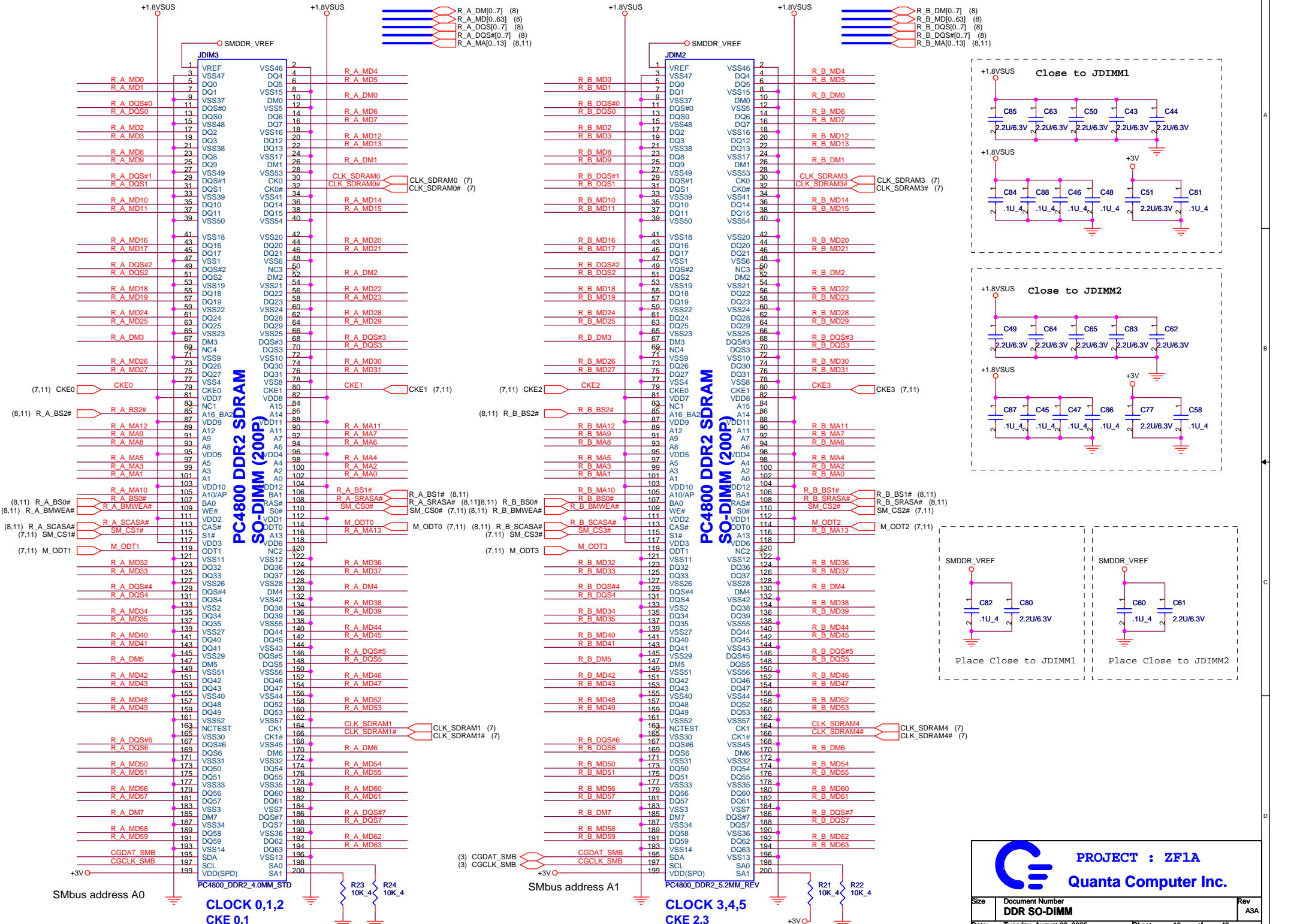
SB_BS0#	AJ15	R B BS0#	R_B_BS0# (10,11)
SB_BS1#	AG17	R B BS1#	R_B_BS1# (10,11)
SB_BS2#	AG21	R B BS2#	R_B_BS2# (10,11)
SB_DM0	AF32	R B DM0	R_B_DM[0..7] (10)
SB_DM1	AK34	R B DM1	
SB_DM2	AK27	R B DM2	
SB_DM3	AK24	R B DM3	
SB_DM4	AJ10	R B DM4	
SB_DM5	AK5	R B DM5	
SB_DM6	AE7	R B DM6	
SB_DM7	AB7	R B DM7	
SB_DQS0	AF34	R B DQS0	R_B_DQS[0..7] (10)
SB_DQS1	AK32	R B DQS1	
SB_DQS2	AJ28	R B DQS2	
SB_DQS3	AK23	R B DQS3	
SB_DQS4	AM10	R B DQS4	
SB_DQS5	AH6	R B DQS5	
SB_DQS6	AF8	R B DQS6	
SB_DQS7	AB4	R B DQS7	
SB_DQS0#	AF35	R B DQS#0	R_B_DQS#[0..7] (10)
SB_DQS1#	AK33	R B DQS#1	
SB_DQS2#	AK28	R B DQS#2	
SB_DQS3#	AJ23	R B DQS#3	
SB_DQS4#	AL10	R B DQS#4	
SB_DQS5#	AH7	R B DQS#5	
SB_DQS6#	AF7	R B DQS#6	
SB_DQS7#	AB5	R B DQS#7	
SB_MA0	AH17	R B MA0	R_B_MA[0..13] (10,11)
SB_MA1	AK17	R B MA1	
SB_MA2	AH18	R B MA2	
SB_MA3	AJ18	R B MA3	
SB_MA4	AK18	R B MA4	
SB_MA5	AJ19	R B MA5	
SB_MA6	AK19	R B MA6	
SB_MA7	AH19	R B MA7	
SB_MA8	AJ20	R B MA8	
SB_MA9	AH20	R B MA9	
SB_MA10	AJ16	R B MA10	
SB_MA11	AG18	R B MA11	
SB_MA12	AG20	R B MA12	
SB_MA13	AG15	R B MA13	
SB_CAS#	AH14	R B SCASA#	R_B_SCASA# (10,11)
SB_RAS#	AK14	R B SRASA#	R_B_SRASA# (10,11)
SB_RCVENIN#	AF15	SB RCVENIN#	
SB_RCVENOUT#	AF14	SB RCVENOUT#	
SB_WE#	AH16	R B BMWEA#	R_B_BMWEA# (10,11)

ALVISO

PROJECT : ZFLA
Quanta Computer Inc.

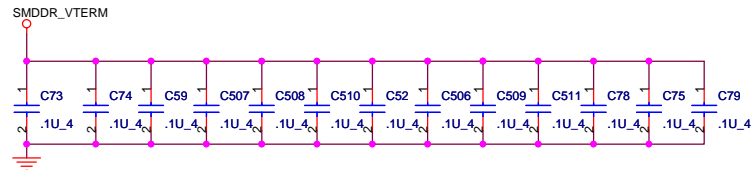
Size	Document Number	Rev
	Alviso DDR	A3A
Date:	Tuesday, August 02, 2005	Sheet 8 of 43



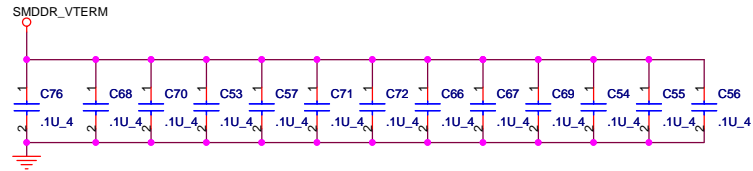


PROJECT : ZF1A
Quanta Computer Inc.

Size	Document Number	Rev	
	DDR SO-DIMM	A3A	
Date:	Tuesday, August 02, 2005	Sheet	10 of 43



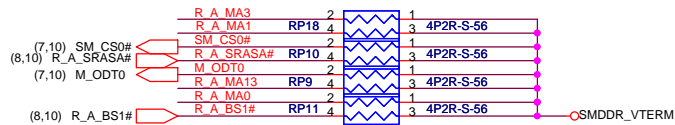
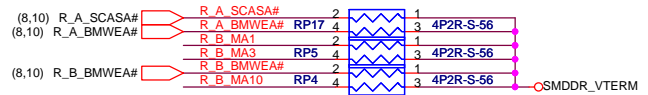
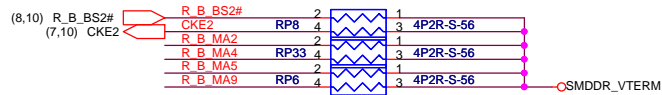
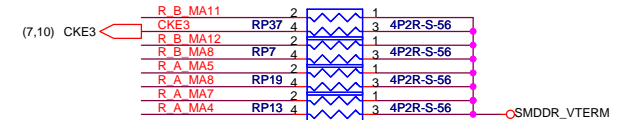
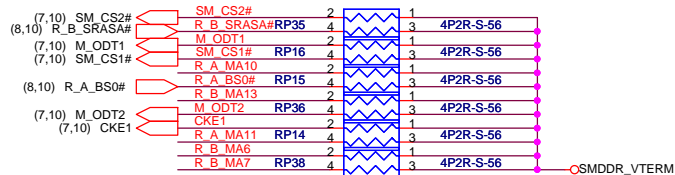
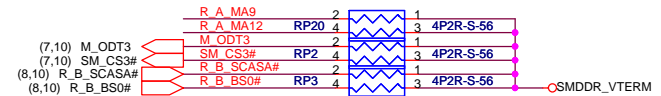
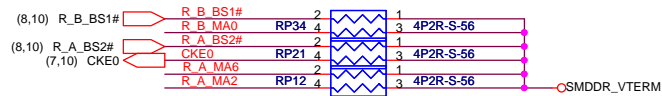
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

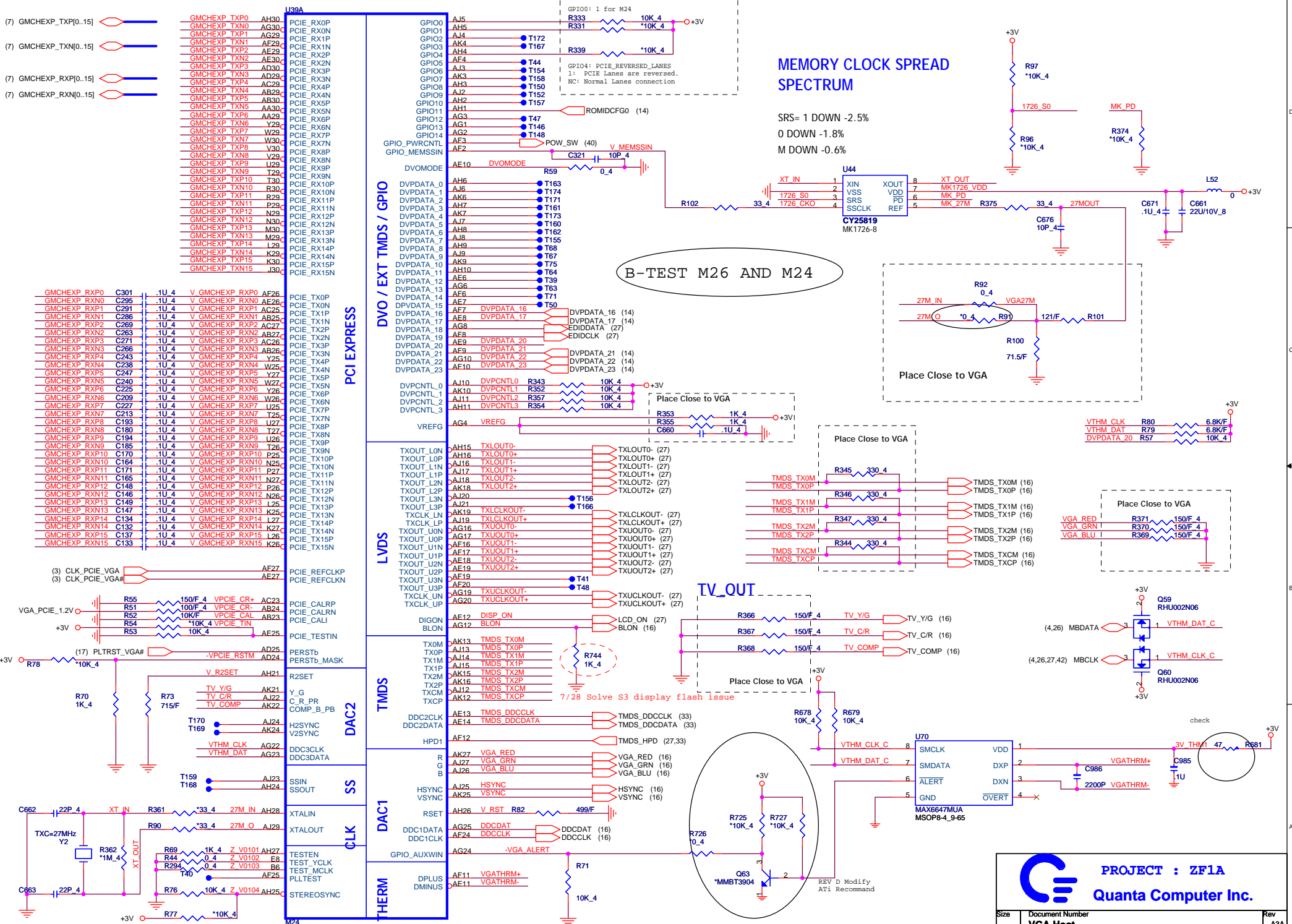
R_A_MA[0..13] (8,10)

R_B_MA[0..13] (8,10)



PROJECT : ZF1A
Quanta Computer Inc.

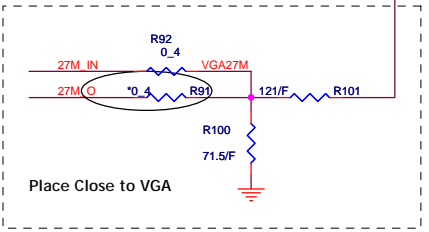
Size	Document Number	Rev
	DDR Res. ARRAY	A3A
Date:	Tuesday, August 02, 2005	Sheet 11 of 43



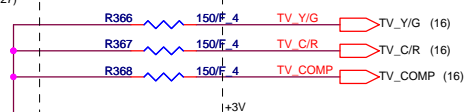
MEMORY CLOCK SPREAD SPECTRUM

SRS= 1 DOWN -2.5%
 0 DOWN -1.8%
 M DOWN -0.6%

B-TEST M26 AND M24

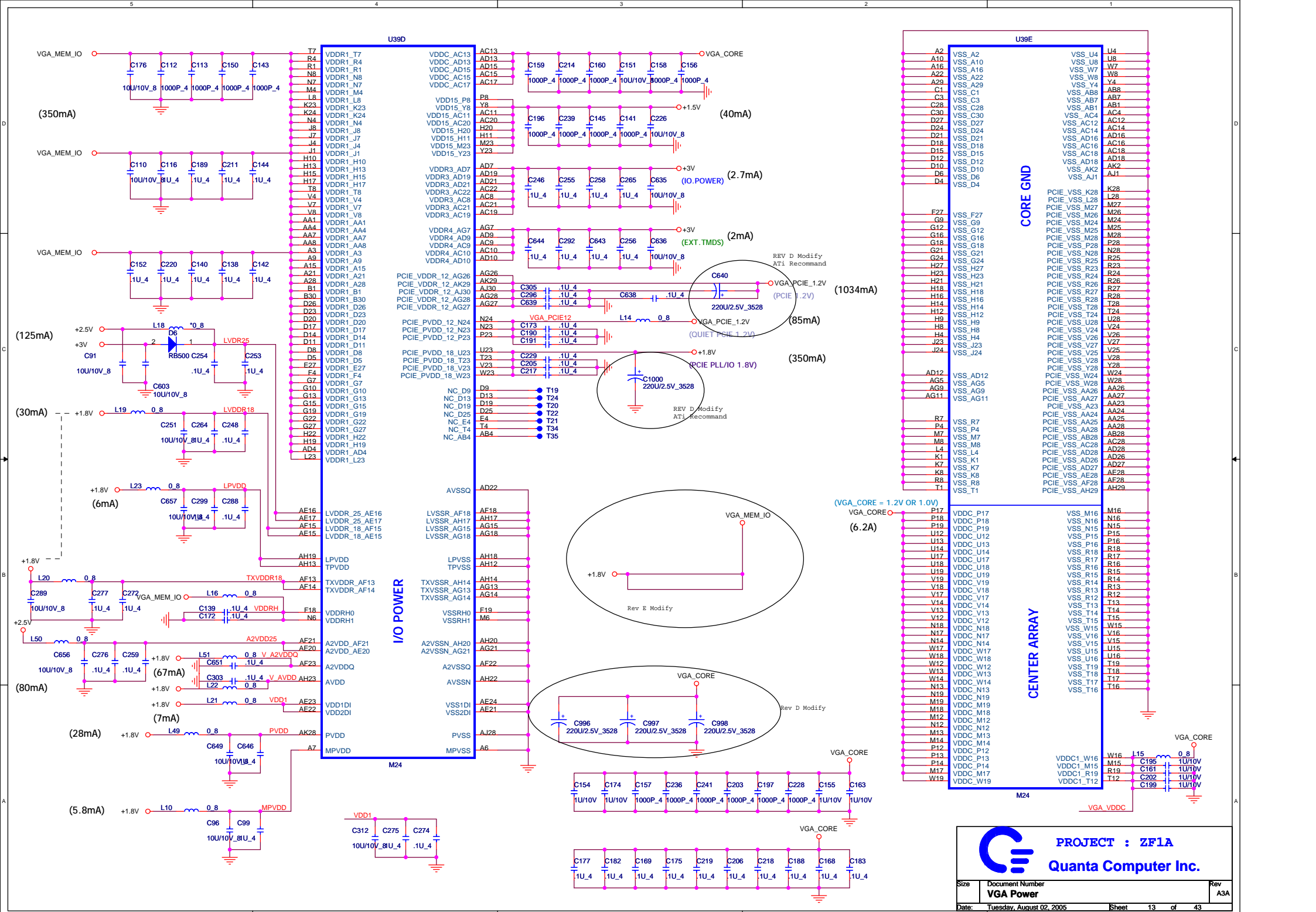



TV_OUT



PROJECT : ZF1A
Quanta Computer Inc.

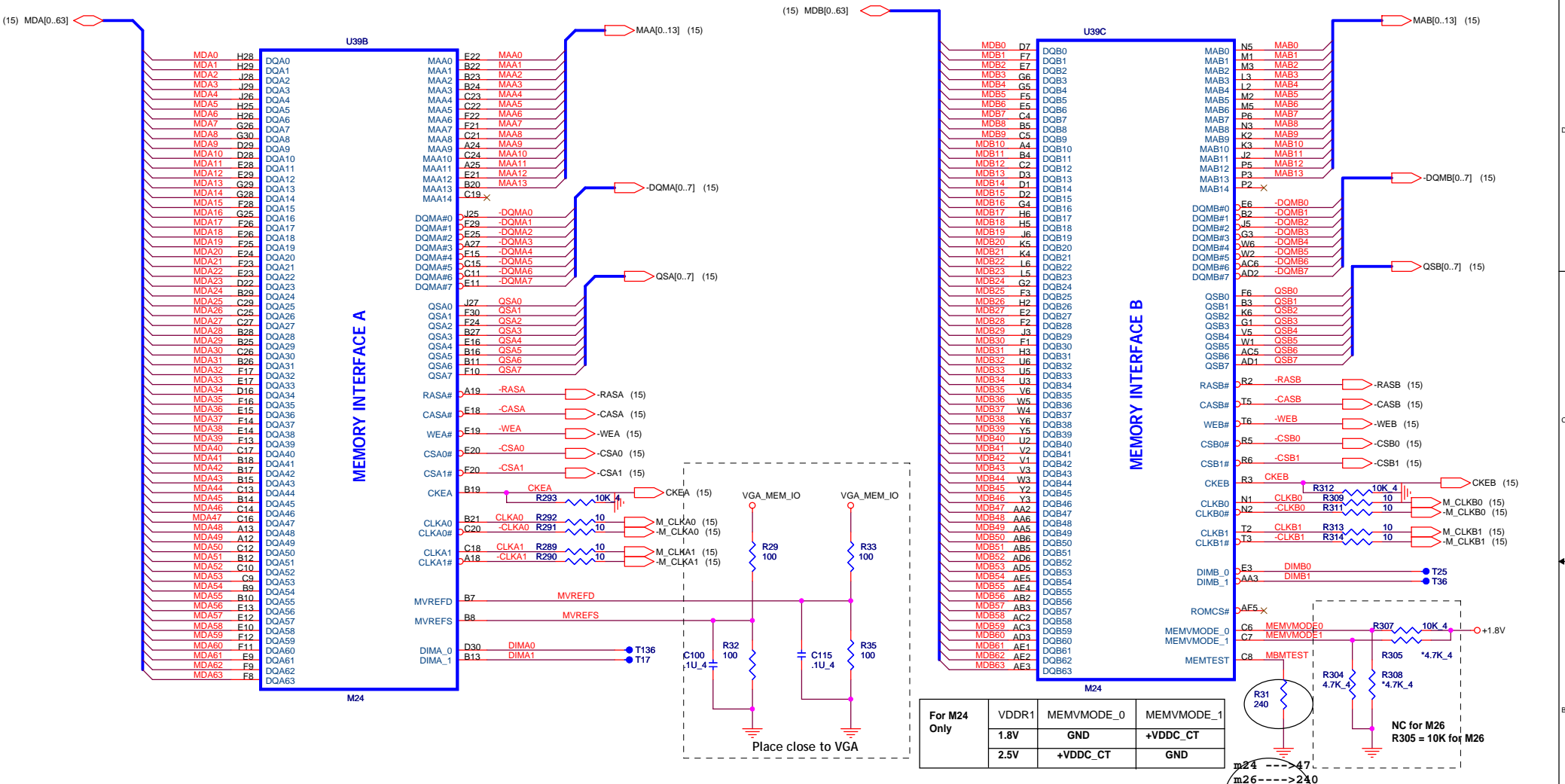
Size	Document Number	Rev
	VGA Host	A3A
Date:	Tuesday, August 02, 2005	Sheet 12 of 43





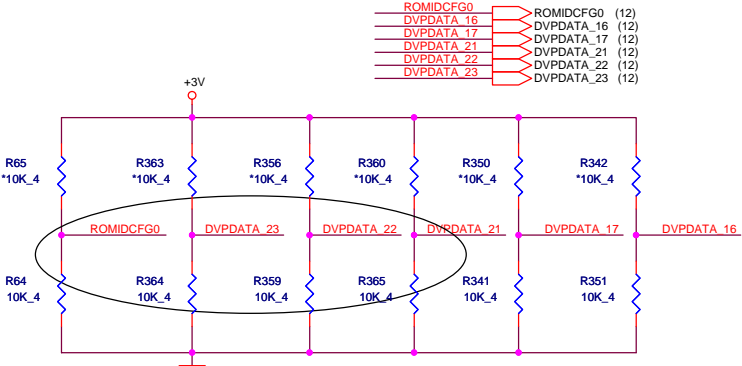
PROJECT : ZF1A
Quanta Computer Inc.

Size	Document Number	Rev
	VGA Power	A3A
Date:	Tuesday, August 02, 2005	Sheet 13 of 43




STRAPS PIN

GPIO(9,13:11) INT P/D	ROMIDCFG
	0x0x: No ROM, CHG_ID=0 0x1x: No Rom, CHG_ID=1 1000: Parallel ROM, Chip ID'S from ROM 1000: Parallel ROM, Chip ID'S from ROM
DVPDATA_21-23 MEM TYPE	DVPDATA_21: 0=4Mx32 1=8Mx32
	DVPDATA_22: 0=128M 1=64M
	DVPDATA_23: 0=Hynix 1=Samsung

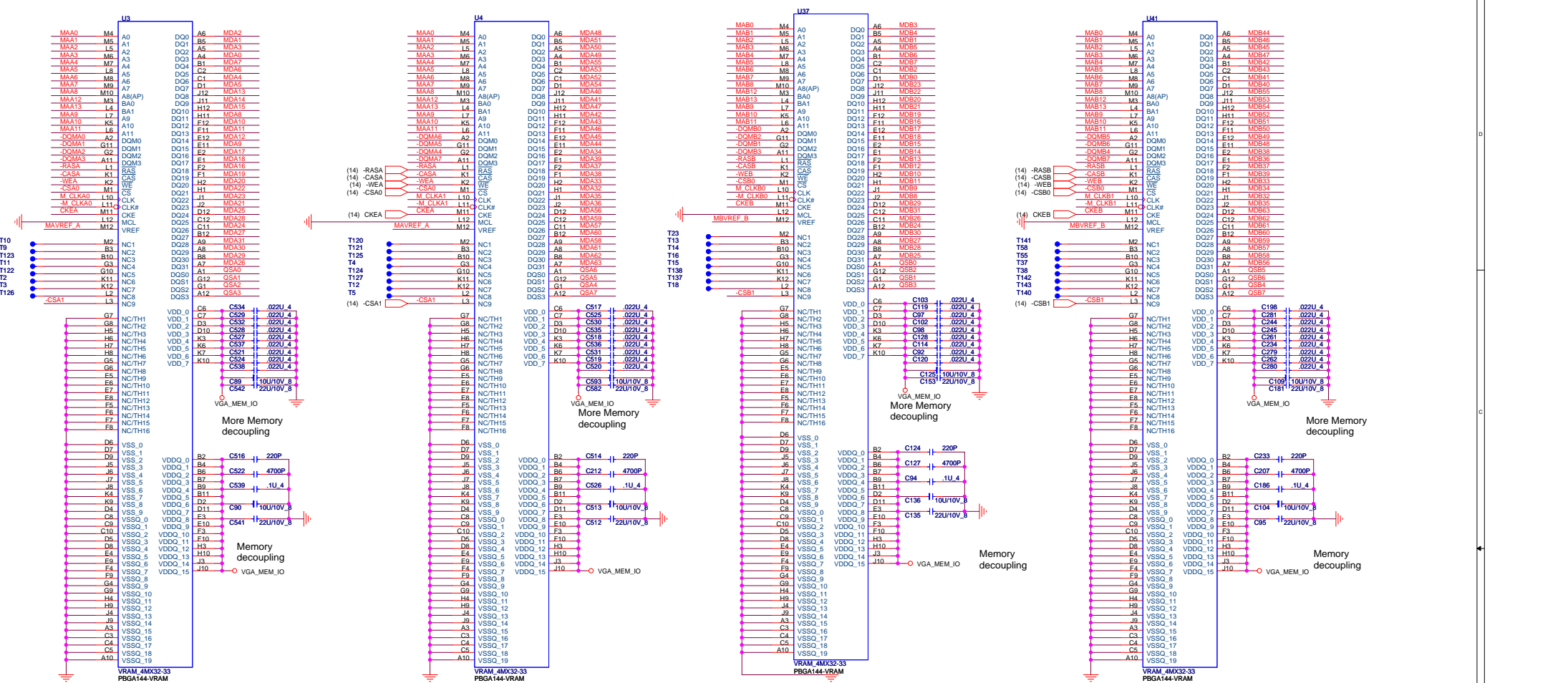


FOR M26P ONLY
0 : 128M
1 : 256M



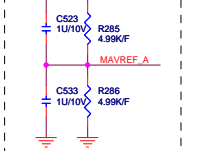
PROJECT : ZF1A
Quanta Computer Inc.

Size	Document Number	Rev
	VGA MEM & Strapping	A3A
Date:	Tuesday, August 02, 2005	Sheet 14 of 43



VGA DDR MEMORY A
 @64/128MBytes DDR 128Mbit 1MX32X4 uBGA

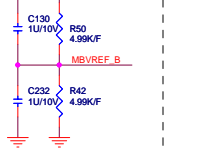
- MAA[0..13] (14)
- MDA[0..63] (14)
- DOMA[0..7] (14)
- QSA[0..7] (14)



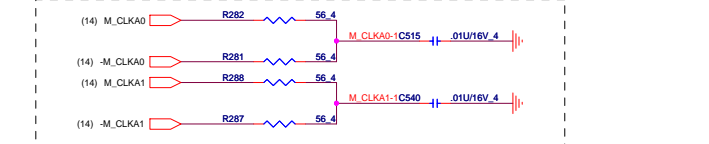
Place close to VRAM

VGA DDR MEMORY B
 @64/128MBytes DDR 128Mbit 1MX32X4 uBGA

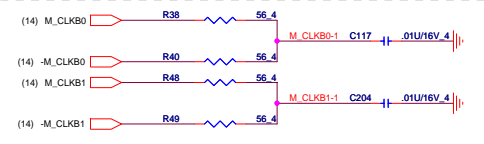
- MAB[0..13] (14)
- MDB[0..63] (14)
- DOMB[0..7] (14)
- OSB[0..7] (14)



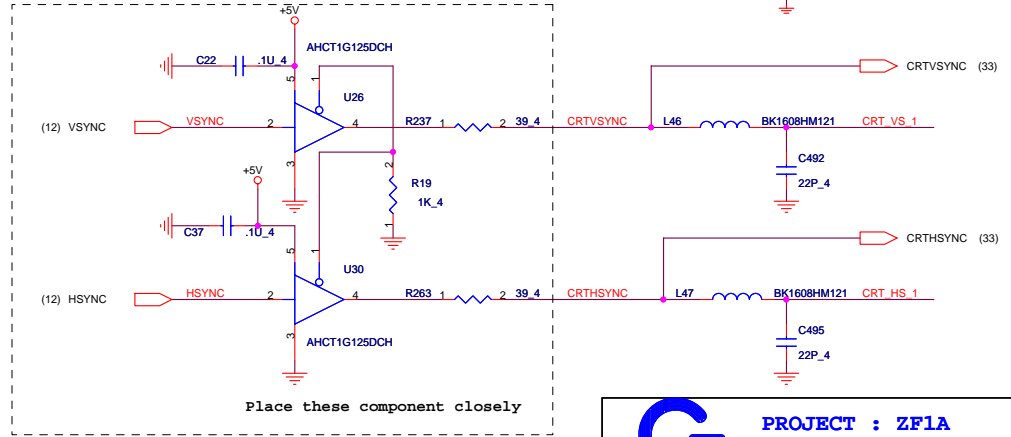
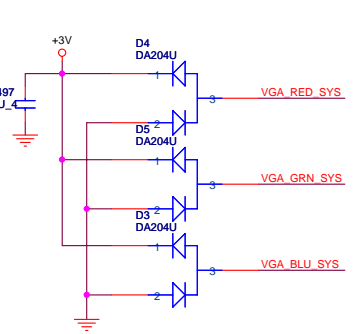
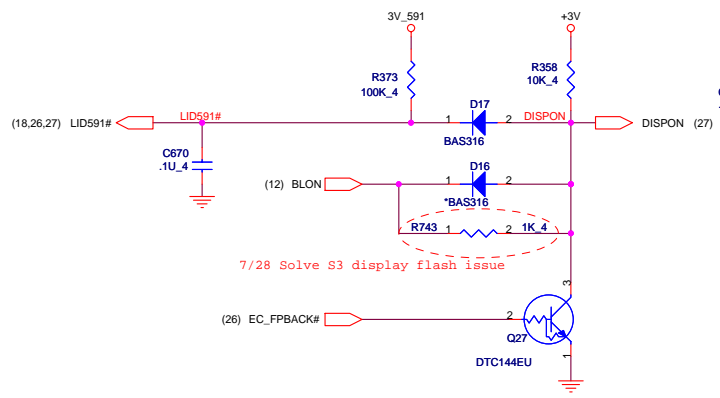
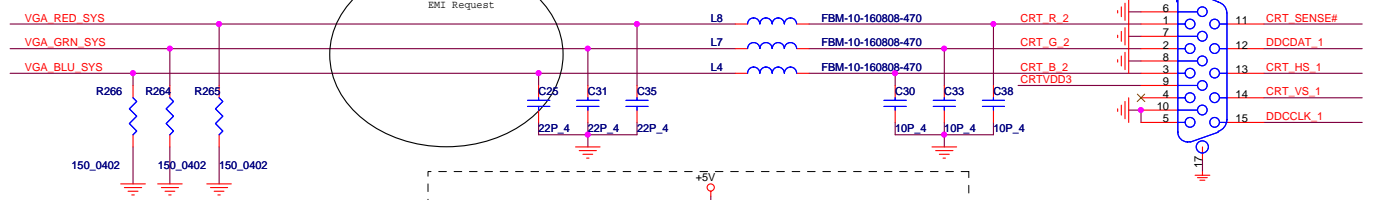
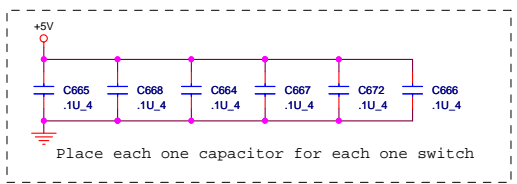
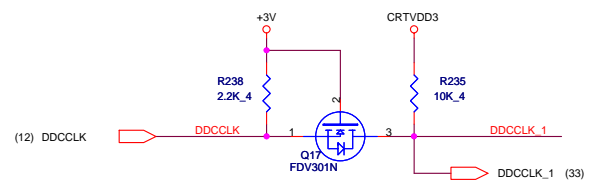
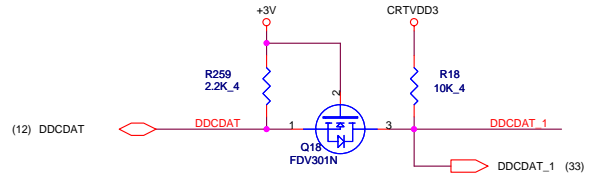
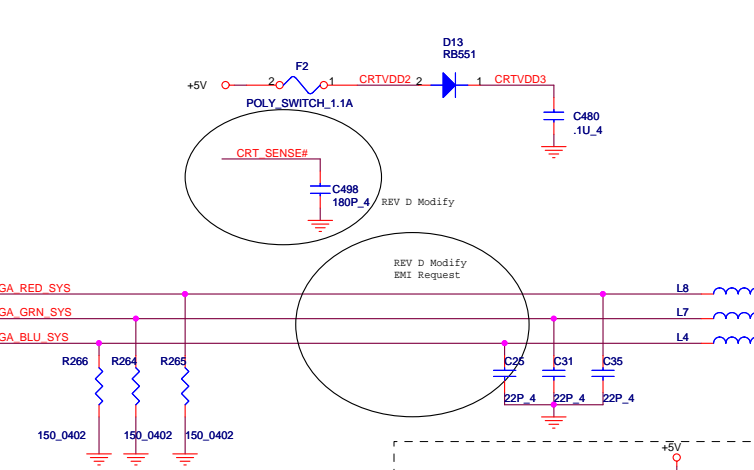
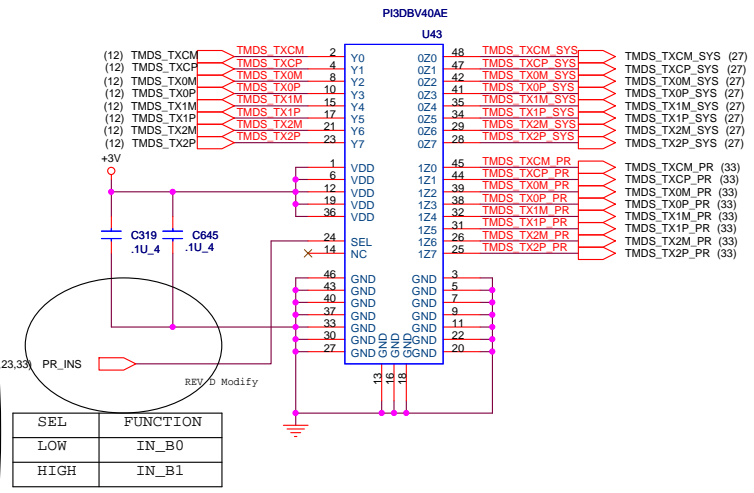
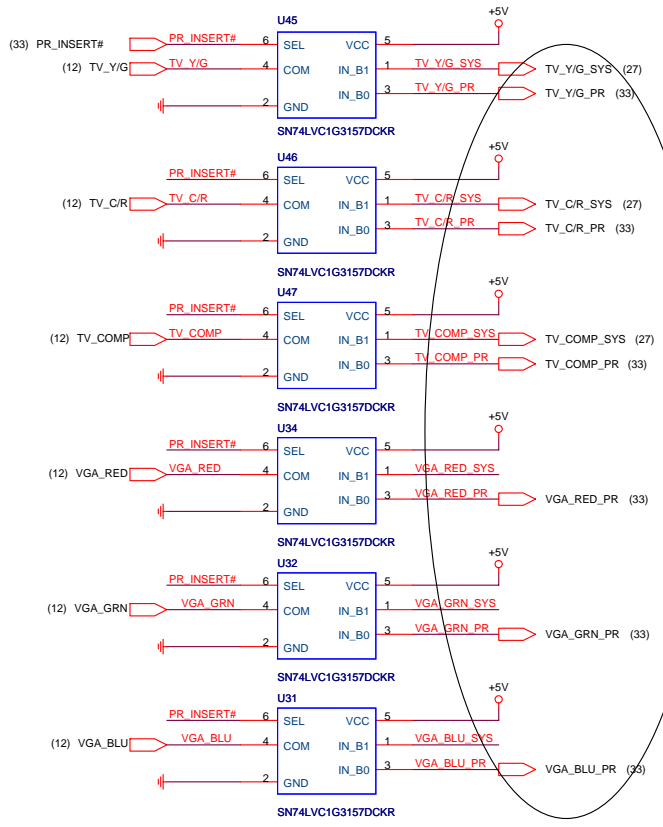
Place close to VRAM



At least a 2.5:1 spacing between the pair
 These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory

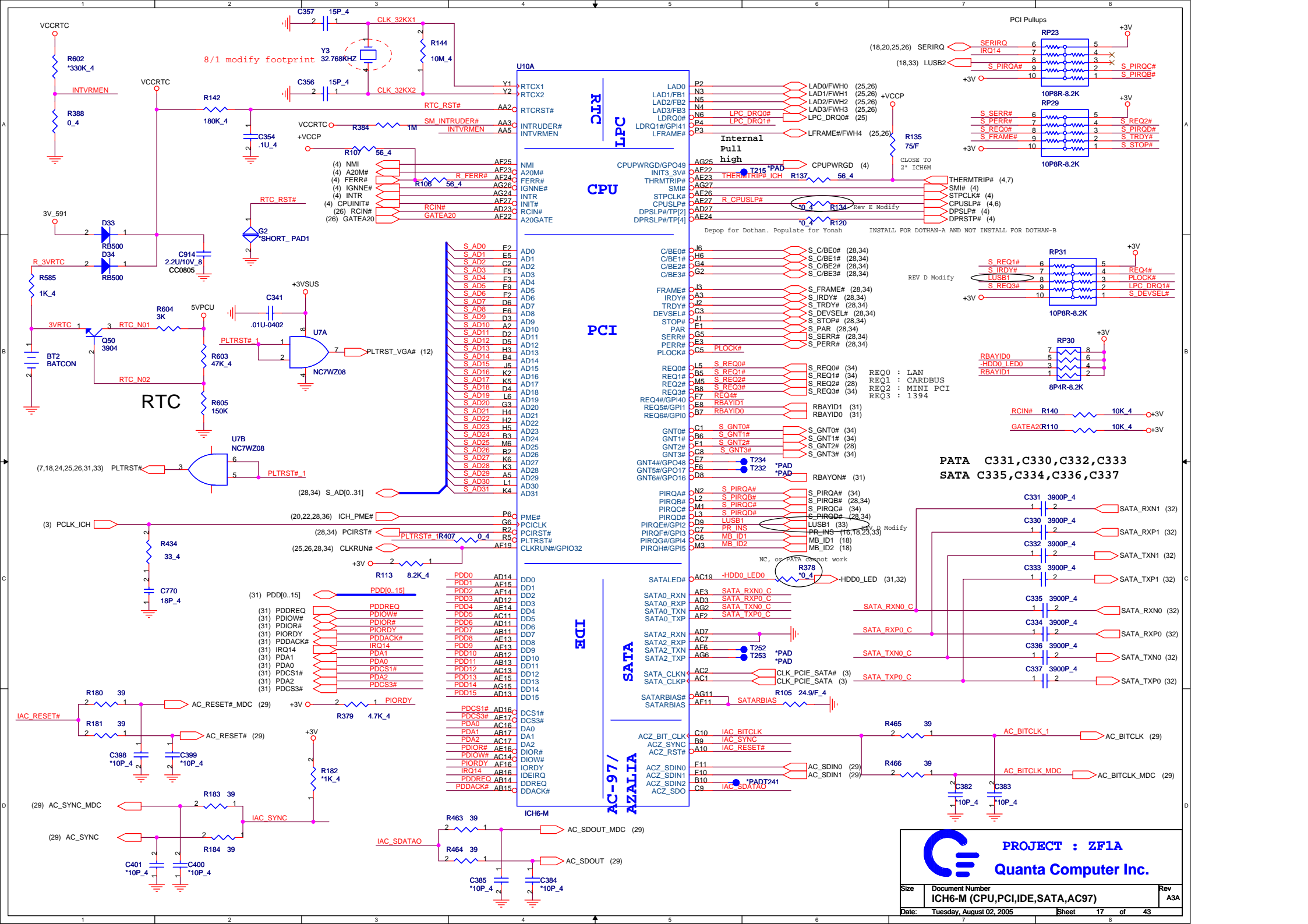


At least a 2.5:1 spacing between the pair
 These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory



PROJECT : ZF1A
Quanta Computer Inc.

Size	Document Number	Rev
	VGA Output	A3A
Date:	Tuesday, August 02, 2005	Sheet 16 of 43



8/1 modify footprint

RTC

CPU

PCI

IDE

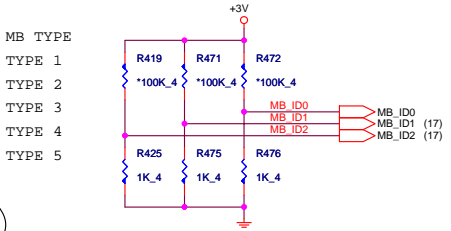
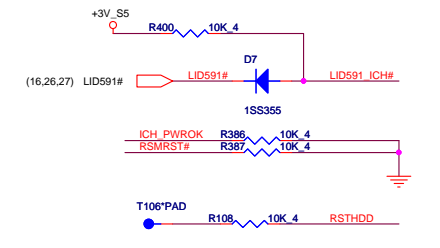
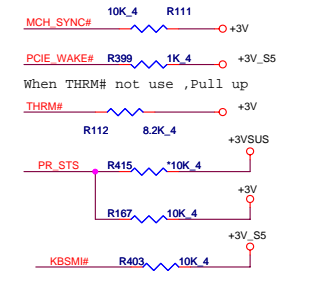
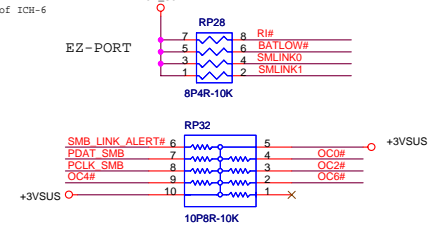
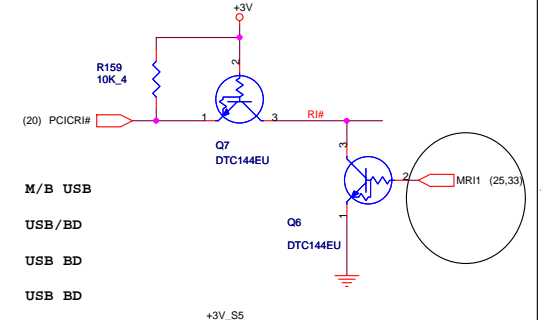
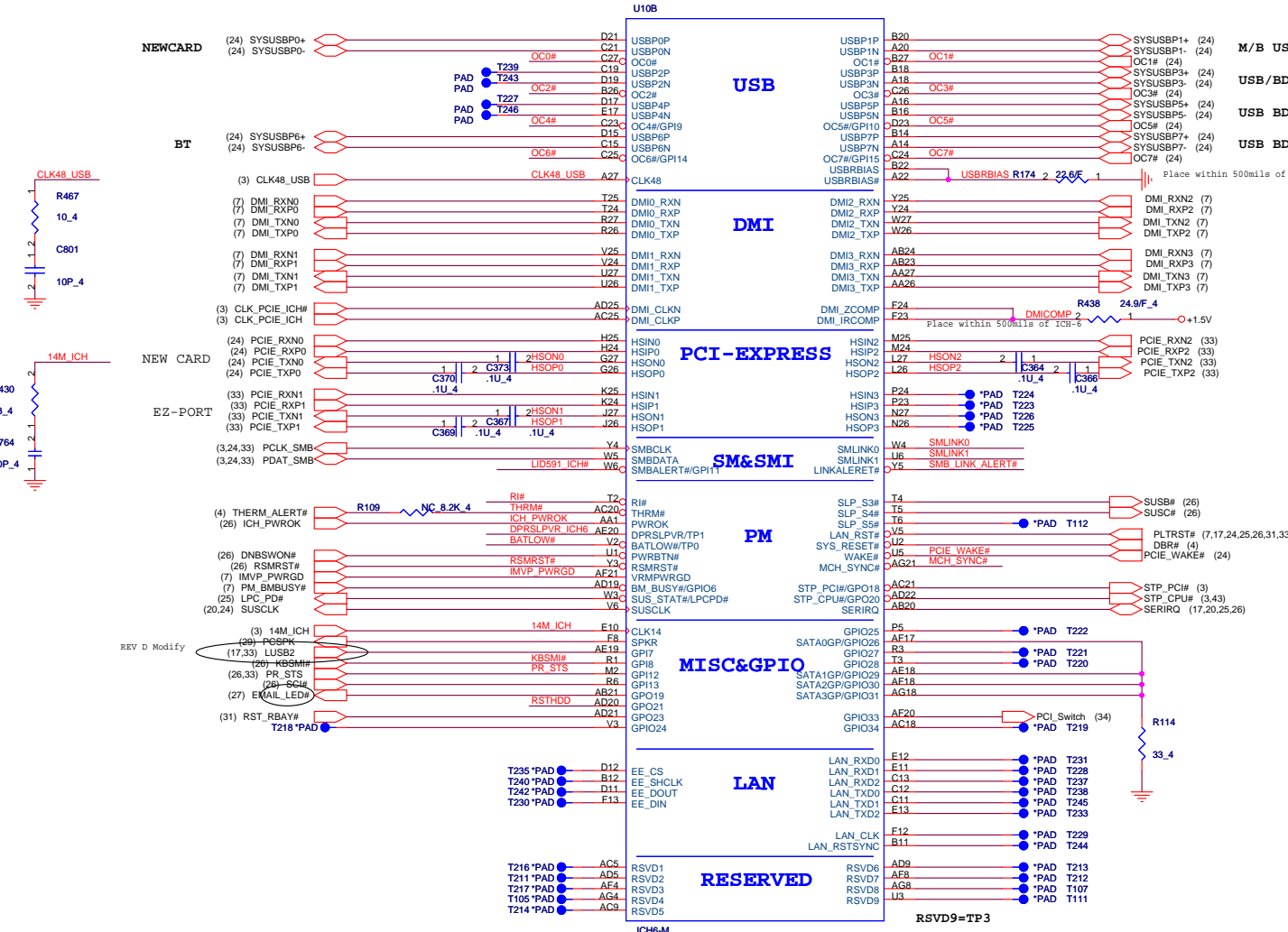
SATA

AC-97/AZALIA

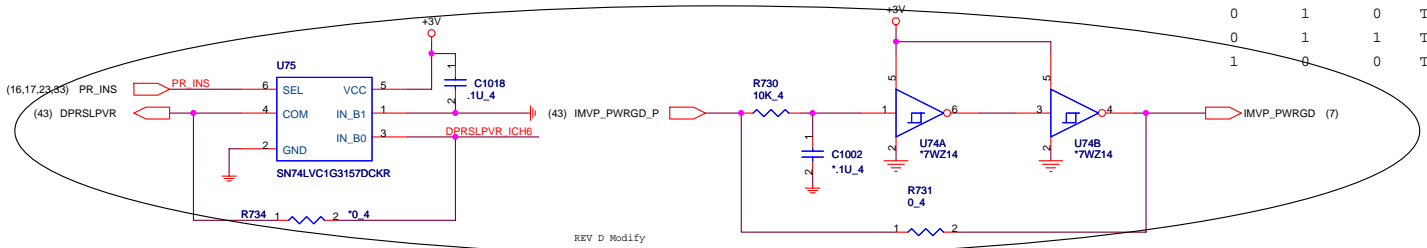
PATA C331, C330, C332, C333
SATA C335, C334, C336, C337



PROJECT : ZF1A
Quanta Computer Inc.

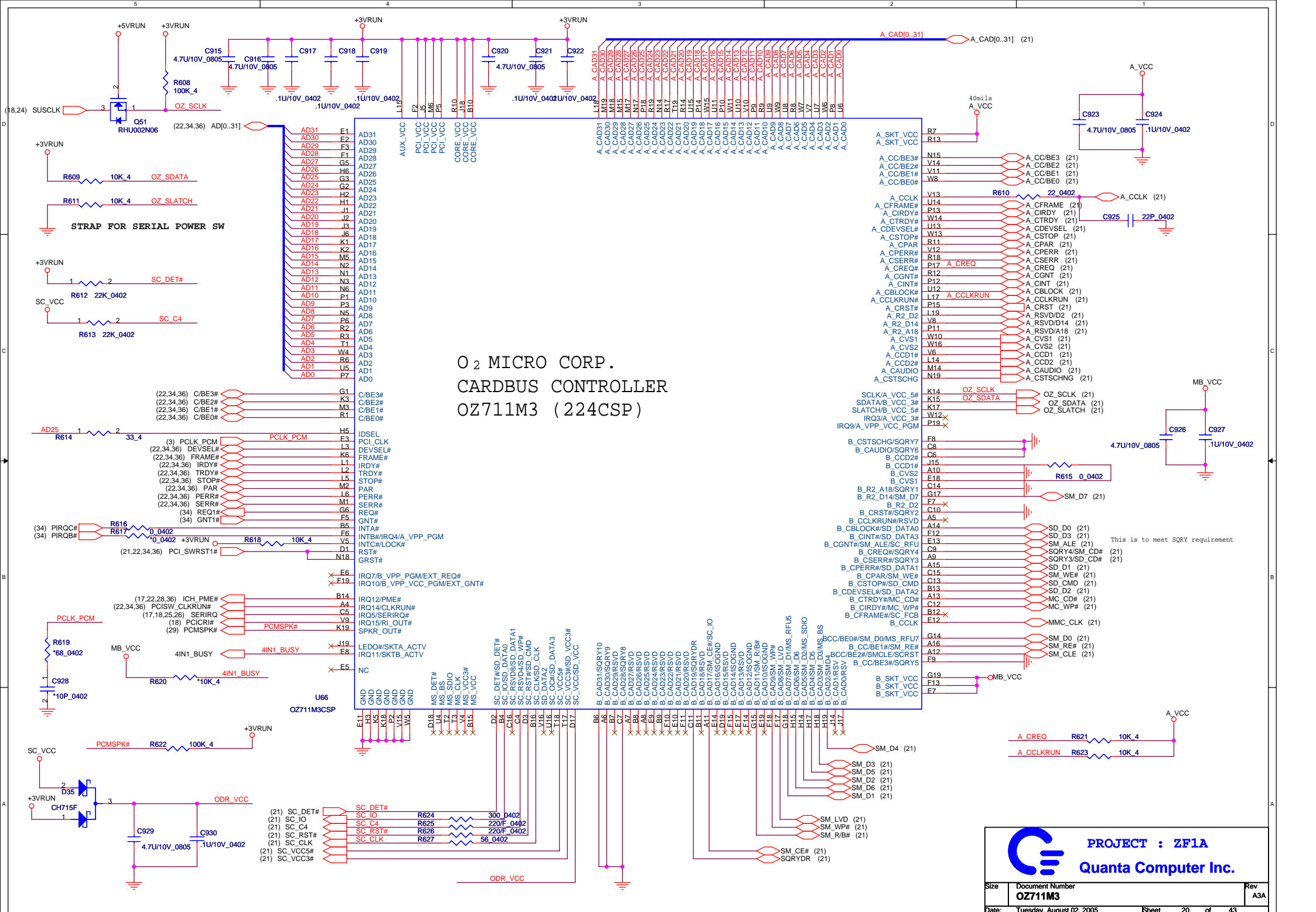


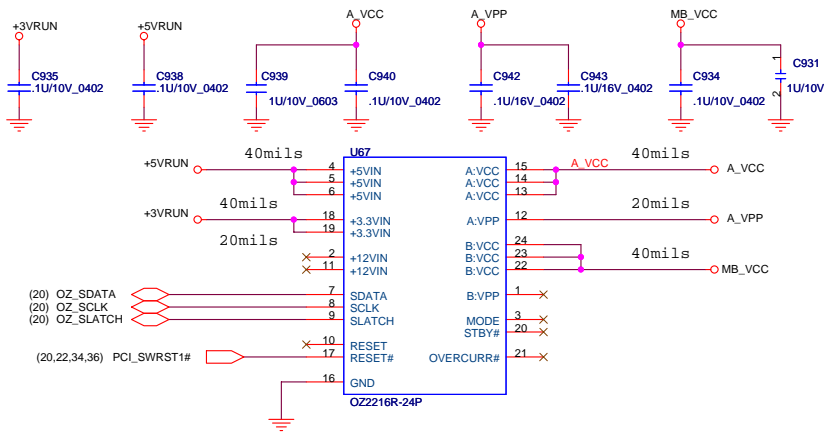
MB_ID2	MB_ID1	MB_ID0	MB TYPE
0	0	0	TYPE 1
0	0	1	TYPE 2
0	1	0	TYPE 3
0	1	1	TYPE 4
1	0	0	TYPE 5



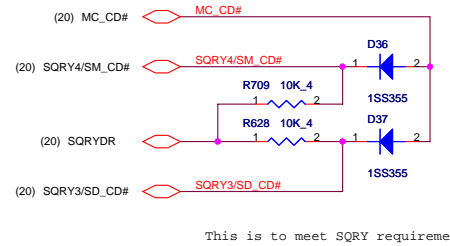
PROJECT : ZF1A
Quanta Computer Inc.

Size	Document Number	Rev
	ICH6-M(USB/HUB)	A3A
Date:	Tuesday, August 02, 2005	Sheet 18 of 43



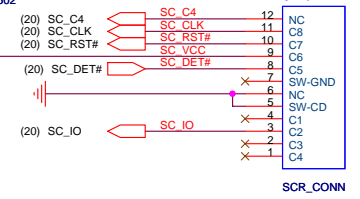
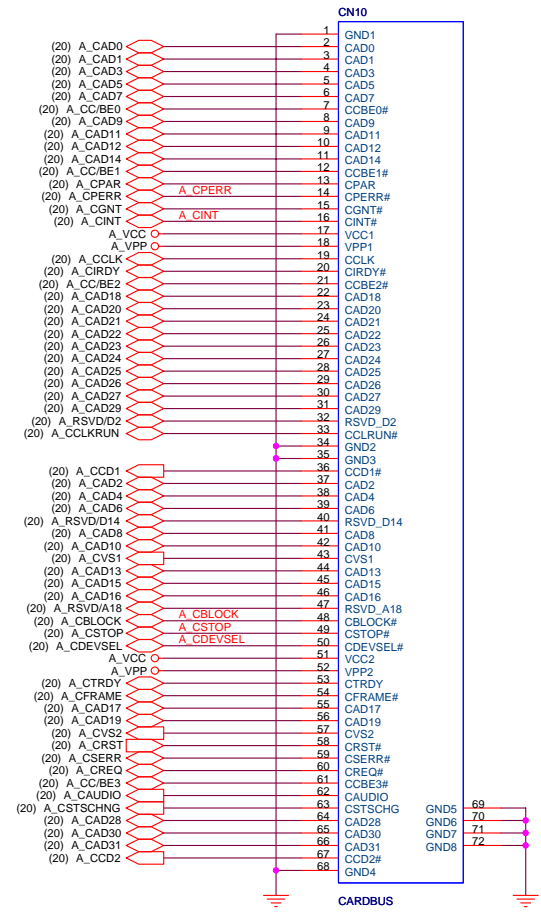
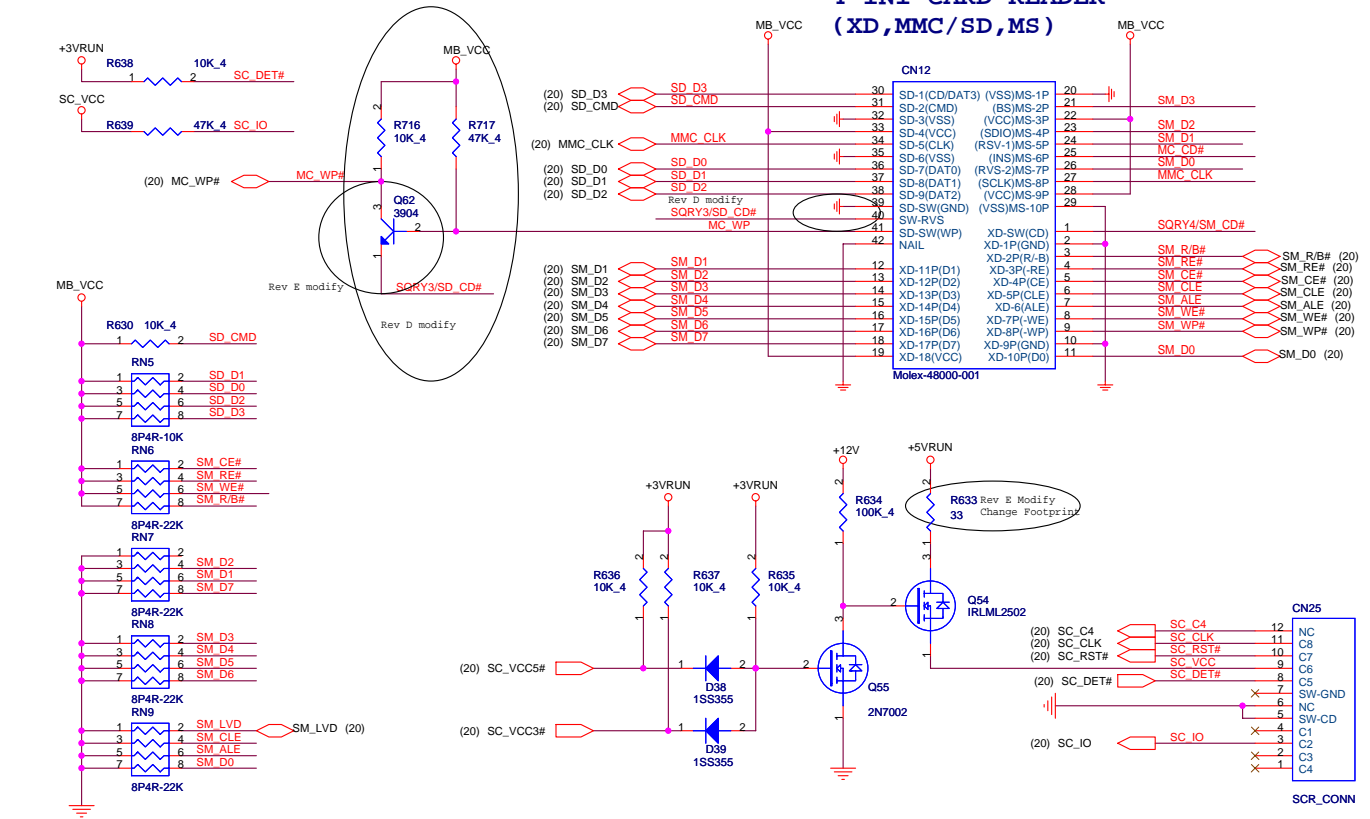


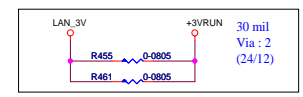
Card	XD	MMC/SD	MS
SQRY3	1	0	1
SQRY4	0	1	1
MC_CD#	0	0	0



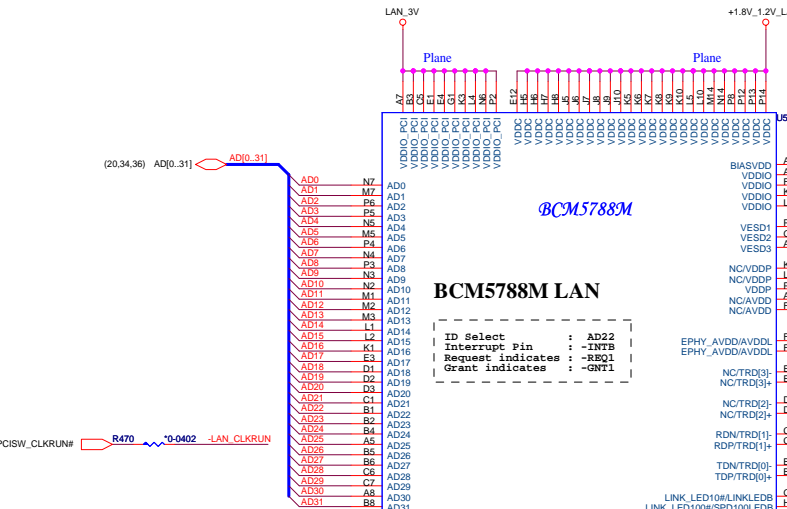
This is to meet SQRY requirement

4 IN1 CARD READER (XD, MMC/SD, MS)





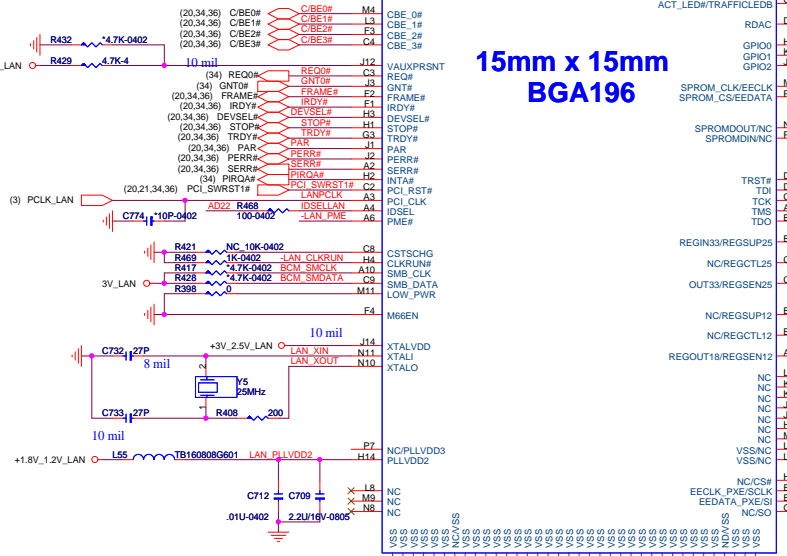
FOR 5788M(GIGA) USE



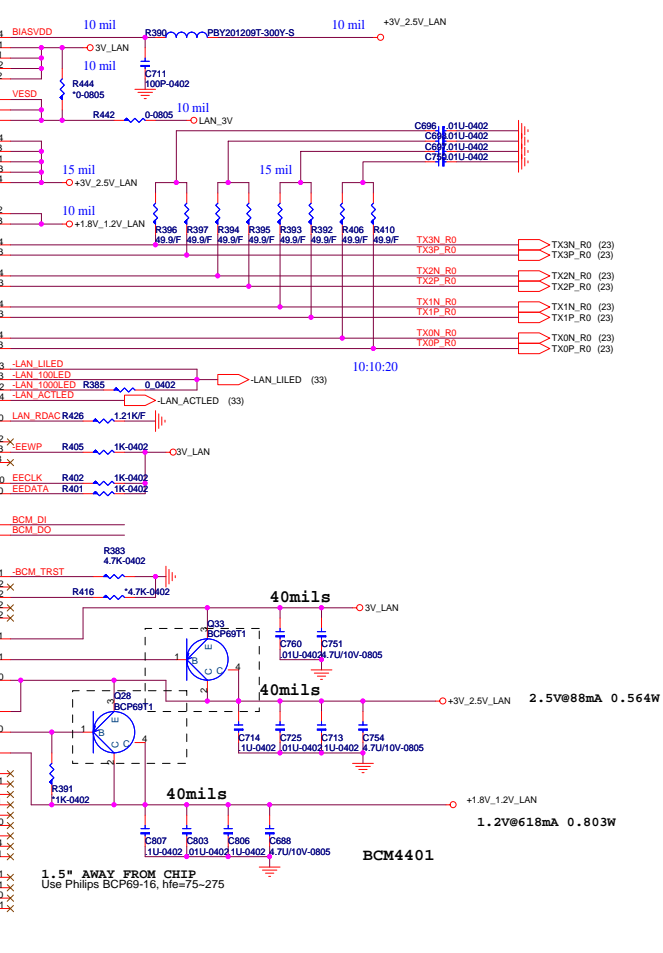
BCM5788M

BCM5788M LAN

ID Select : AD22
 Interrupt Pin : -INTB
 Request indicates : -REQ0
 Grant indicates : -GNT1

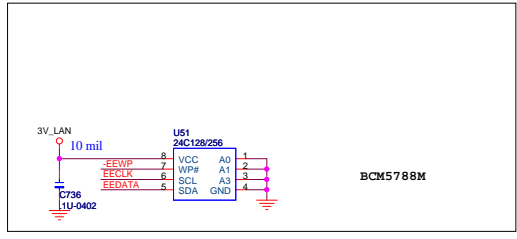
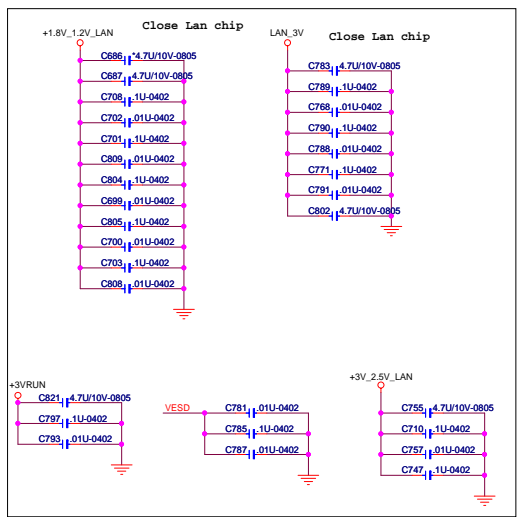


15mm x 15mm
BGA196

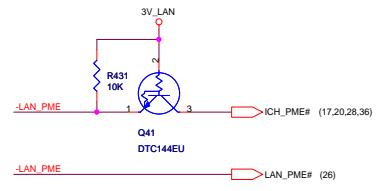


BCM4401

1.5" AWAY FROM CHIP
Use Philips BCP69-16, hfe=75-275



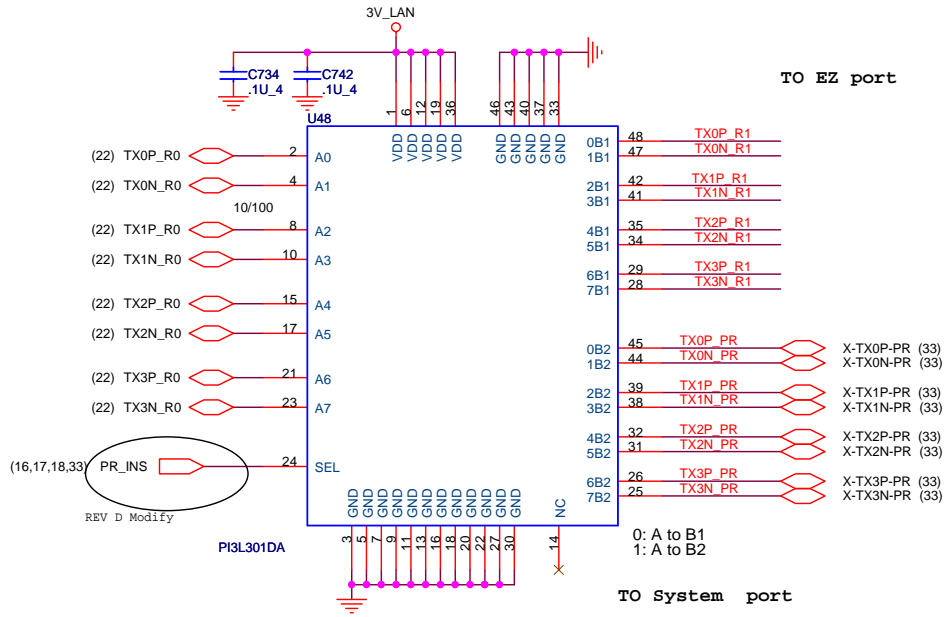
BCM5788M



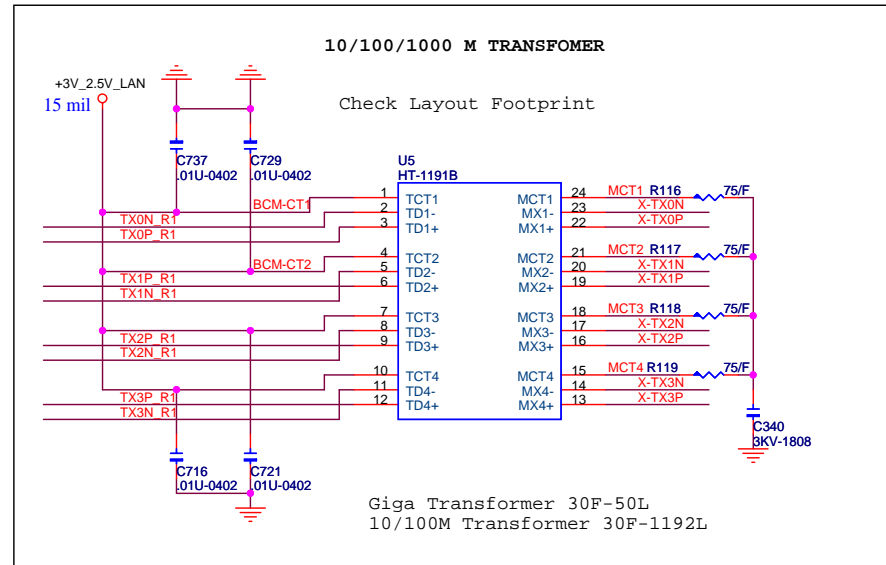
Voltage Rail	4401	5702	5705M
VDDIO_PCI	3V_S5	+3V	+3V
+3V_2.5V_LAN	3.3V	2.5V	2.5V
+1.8V_1.2V_LAN	1.8V	1.2V	1.2V

DNS	BCM4401	BCM5788M
STU	Q16, Q17, U26 R327, R329	U55, R331, R332
	R331, R332, U55	Q16, Q17, U26

Lan Switch

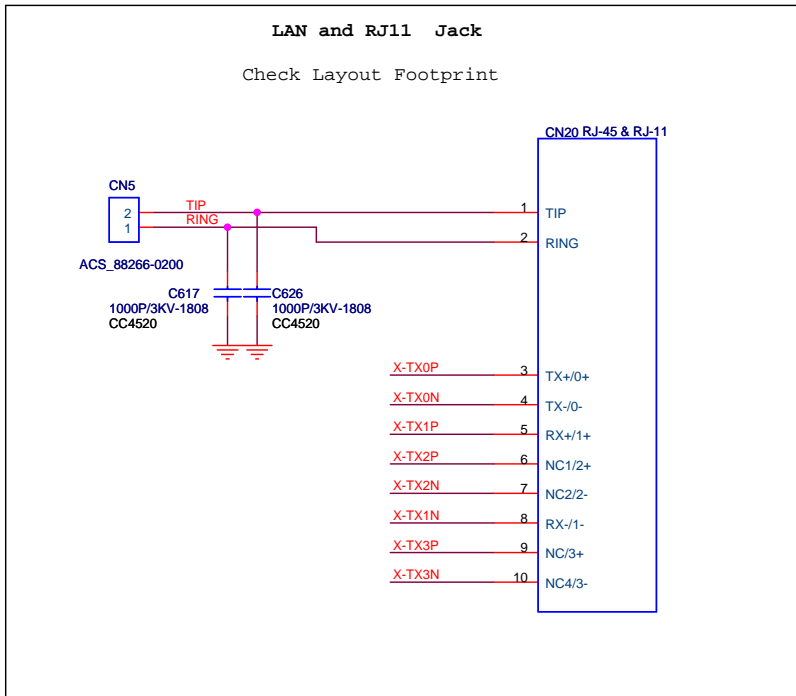


10/100/1000 M TRANSFORMER



LAN and RJ11 Jack

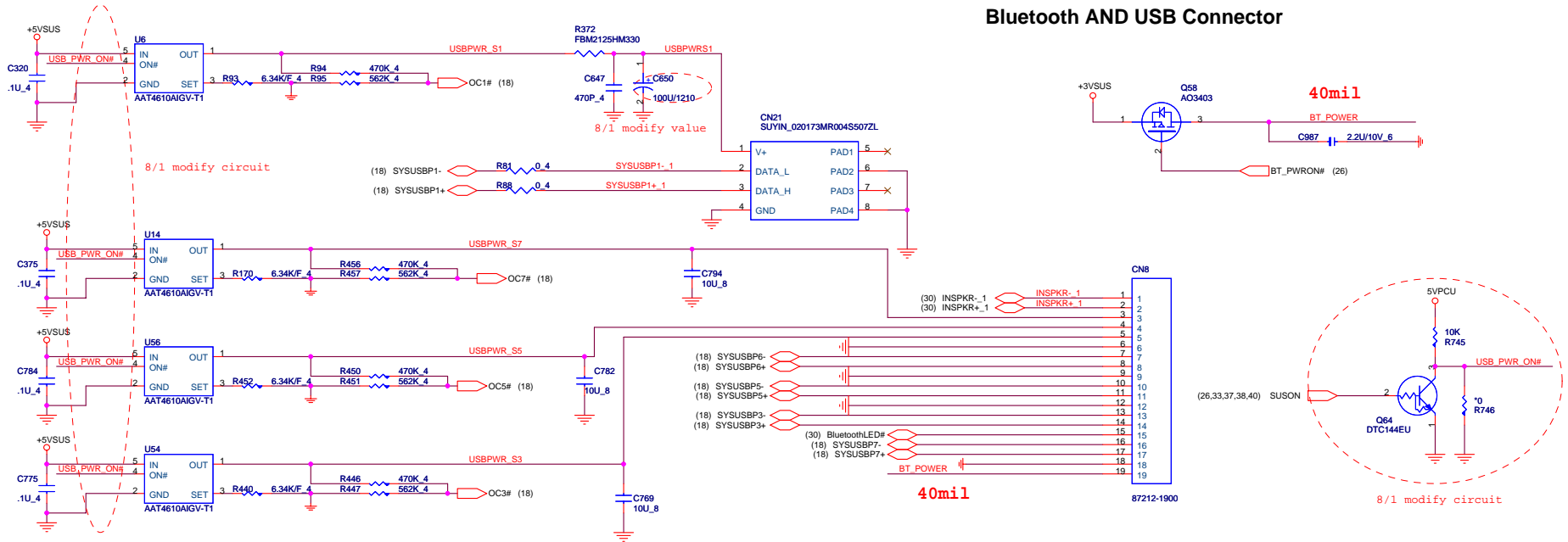
Check Layout Footprint



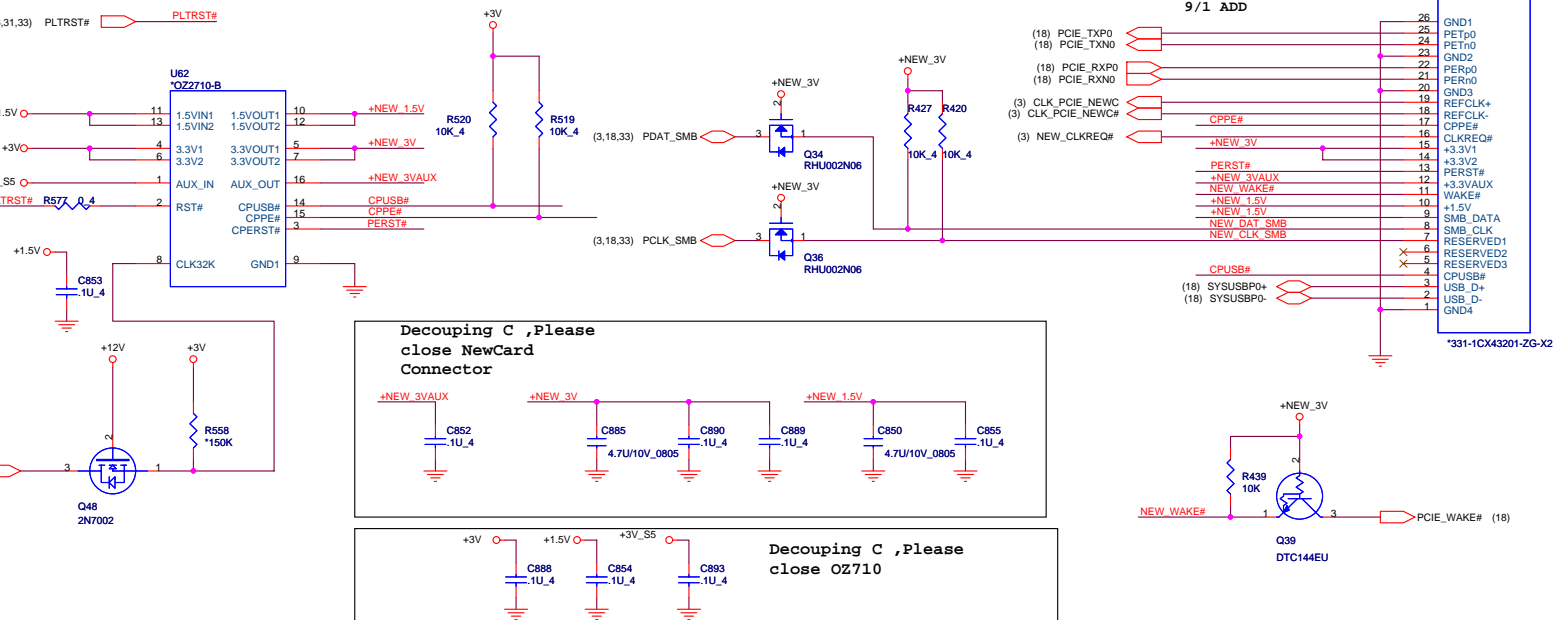
PROJECT : ZF1A
Quanta Computer Inc.

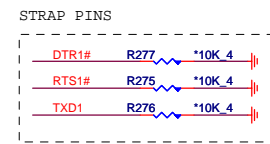
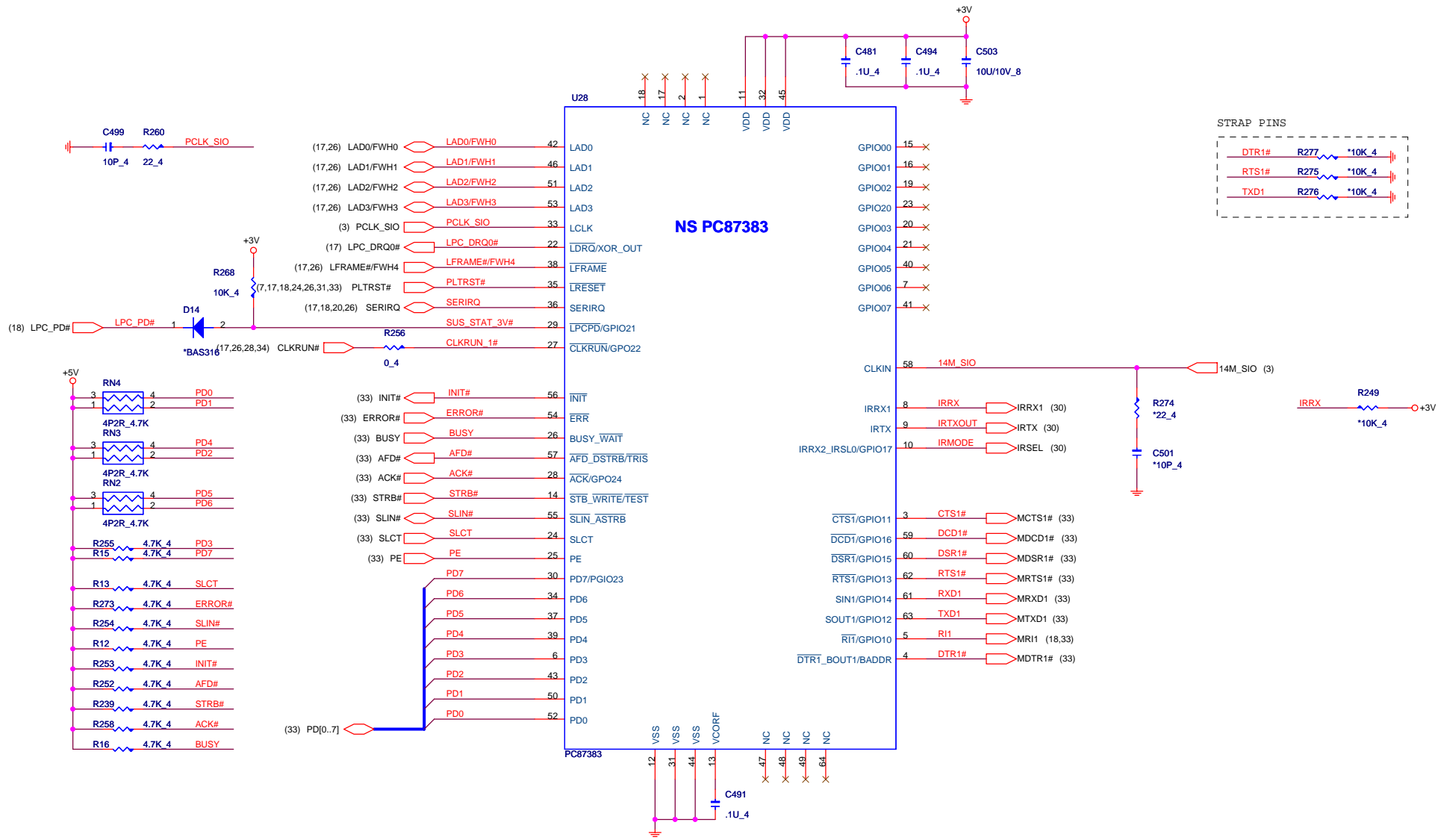
USB Connector and USB board

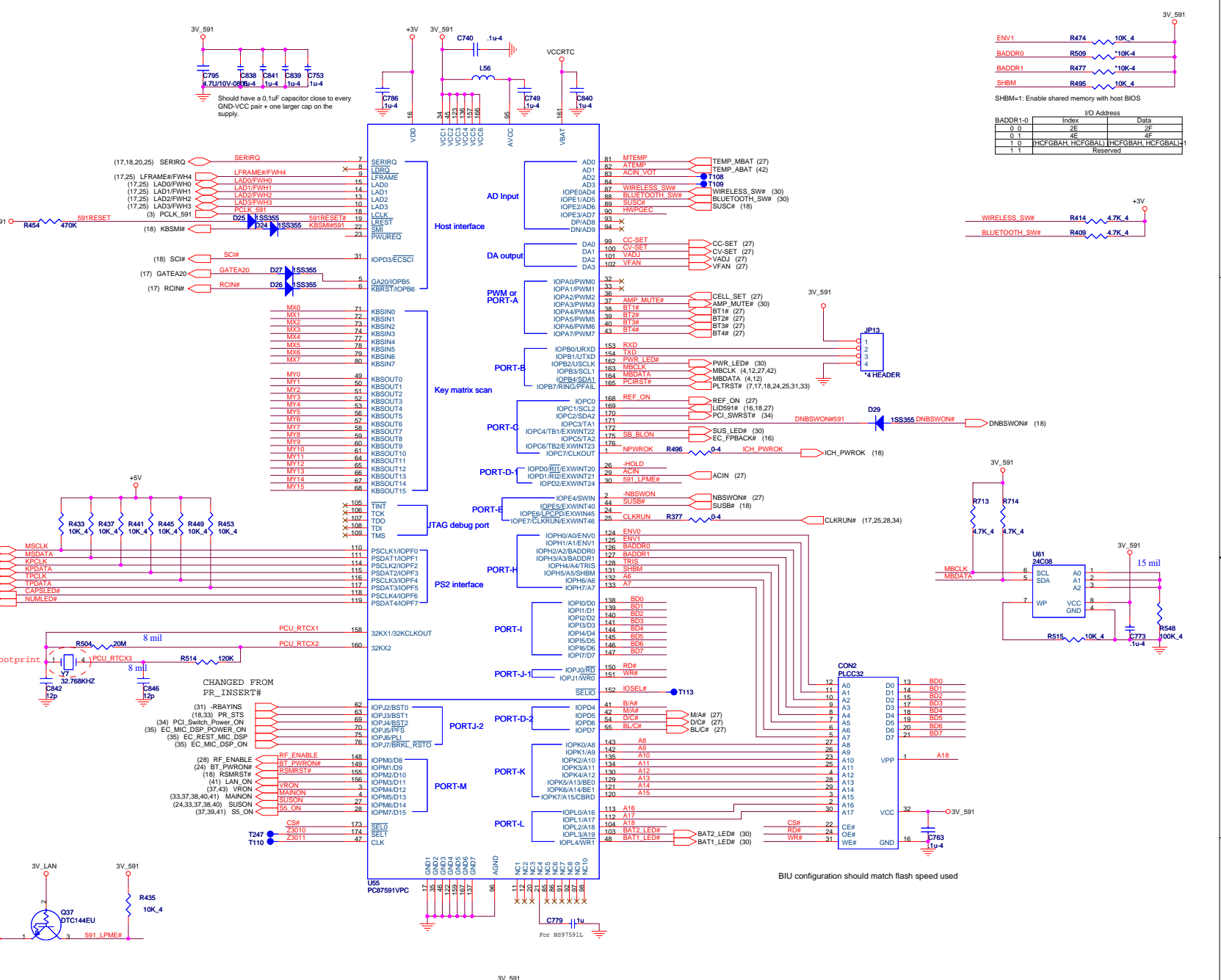
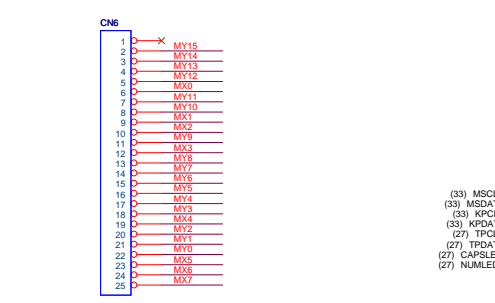
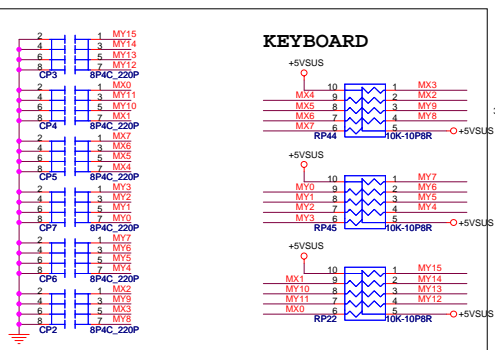
Bluetooth AND USB Connector



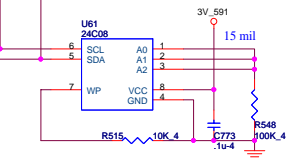
NewCard



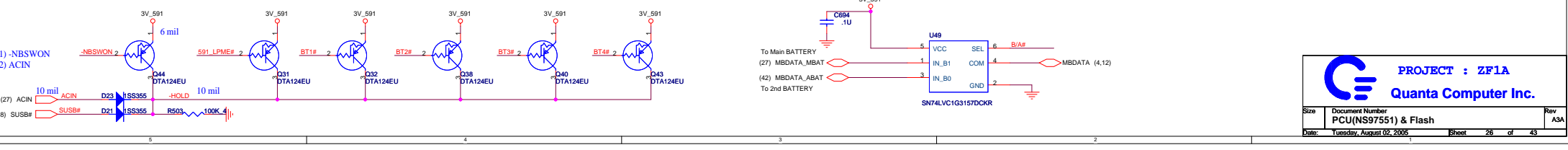




I/O Address		
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	HC-FGBAH, HC-FGBAL	HC-FGBAH, HC-FGBAL
1 1	Reserved	



BIU configuration should match flash speed used

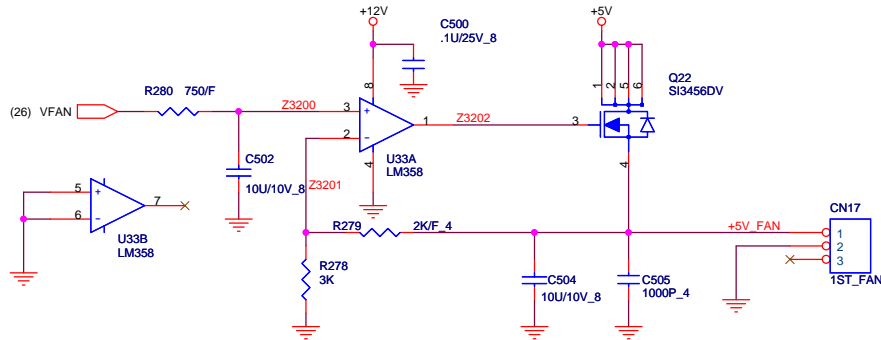


PROJECT : ZF1A
Quanta Computer Inc.

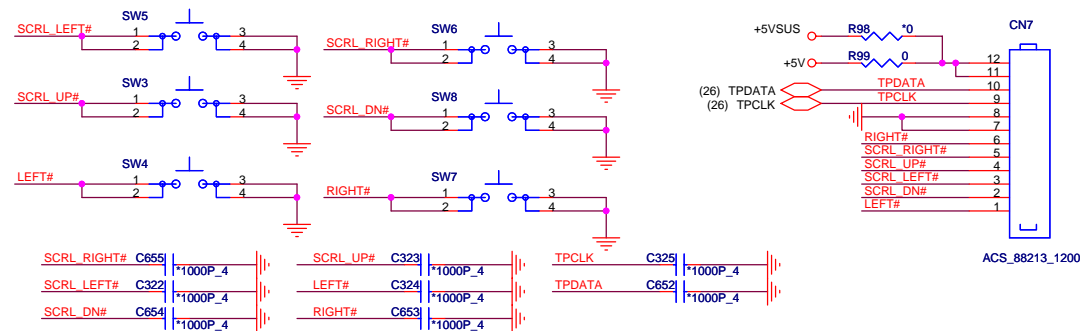
Size: _____ Document Number: **PCU(NS97551) & Flash** Rev: **ASA**

Date: **Tuesday, August 02, 2005** Sheet: **26** of **43**

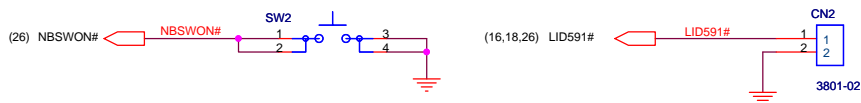
1st FAN OUT CONNECTOR



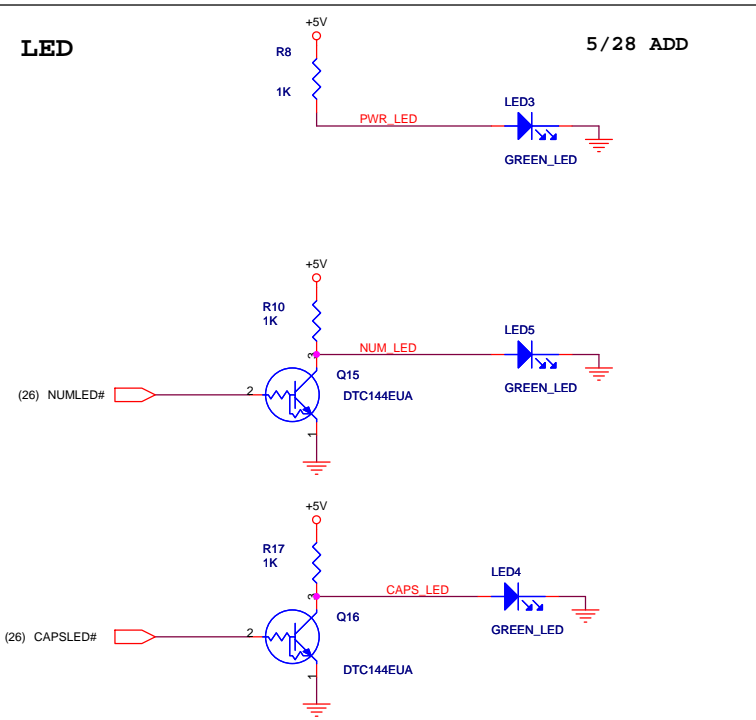
TouchPad Switch and T/P Module Connector



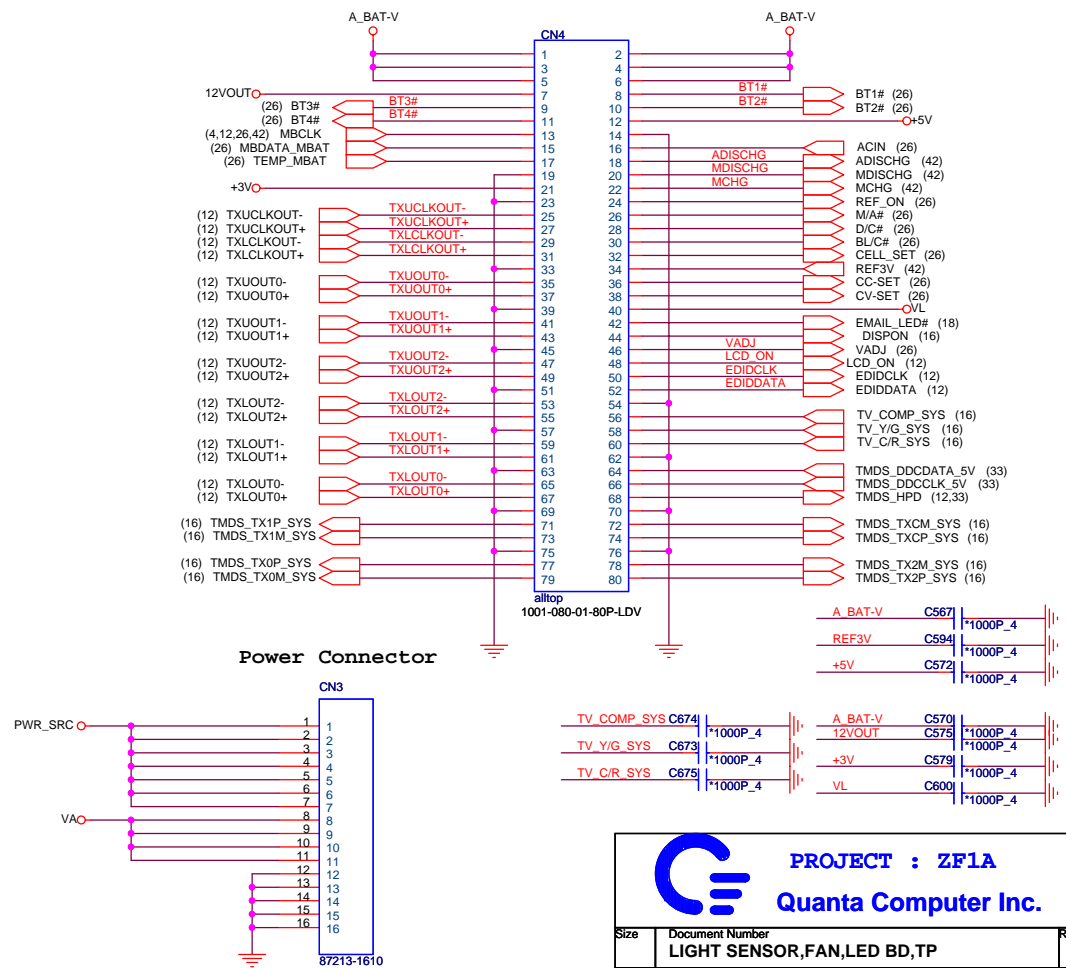
Power Switch



LED

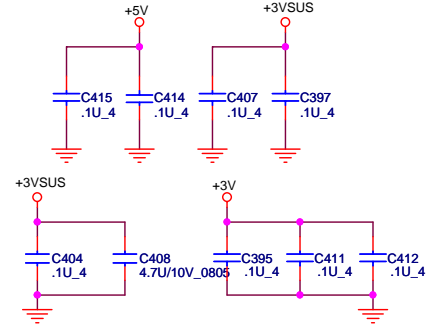
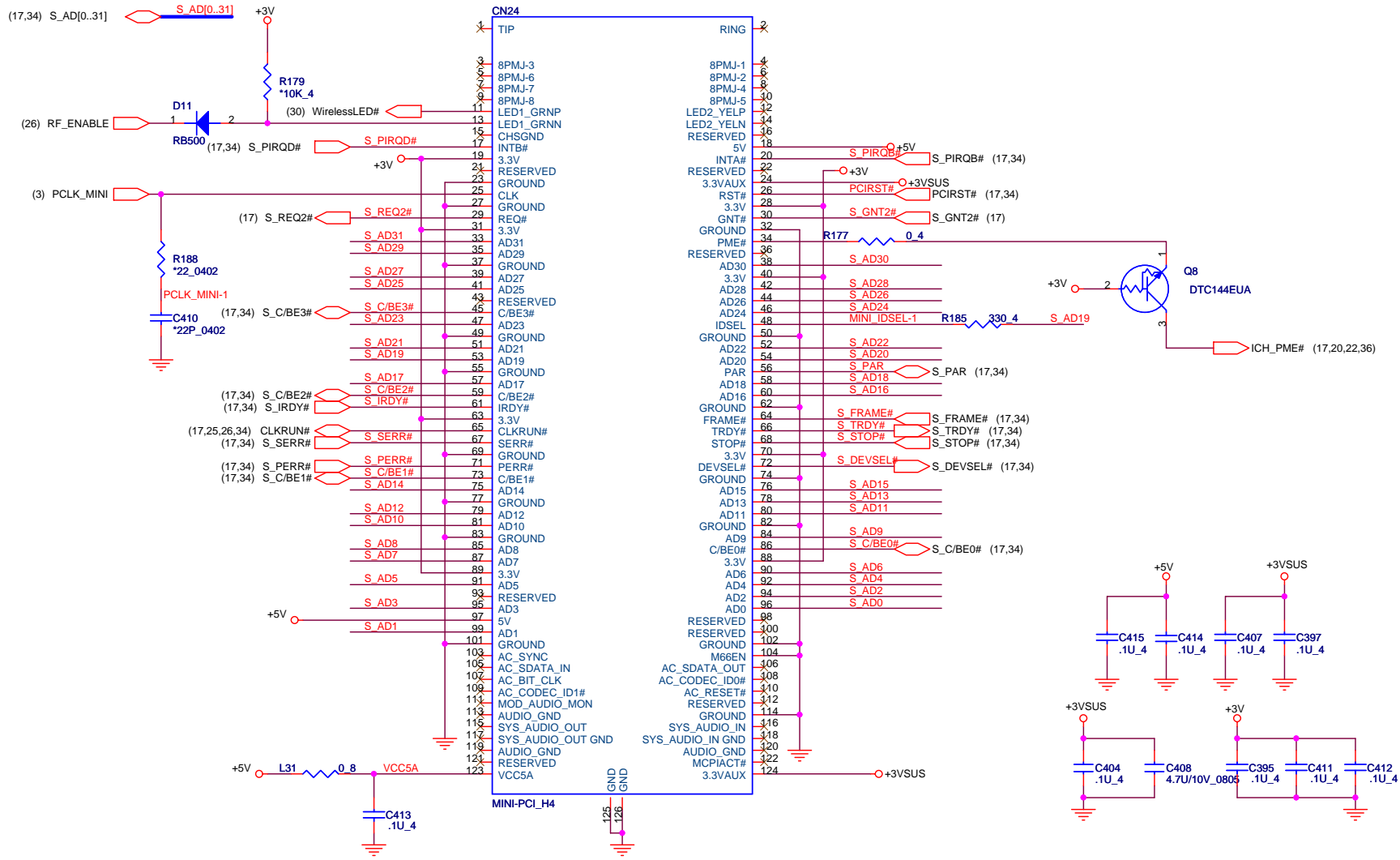



Power Connector



PROJECT : ZF1A
Quanta Computer Inc.

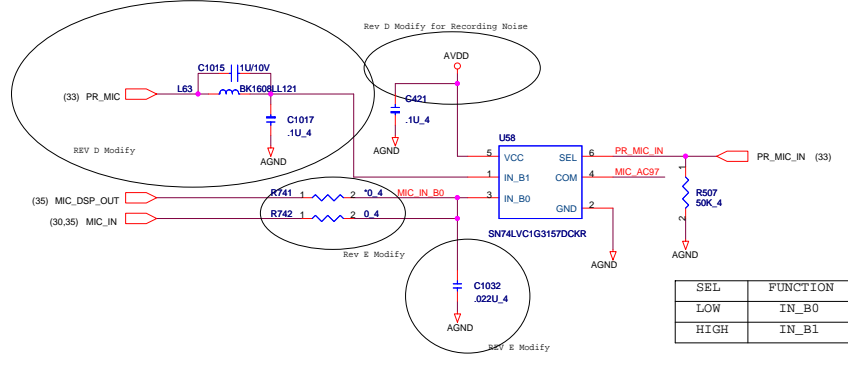
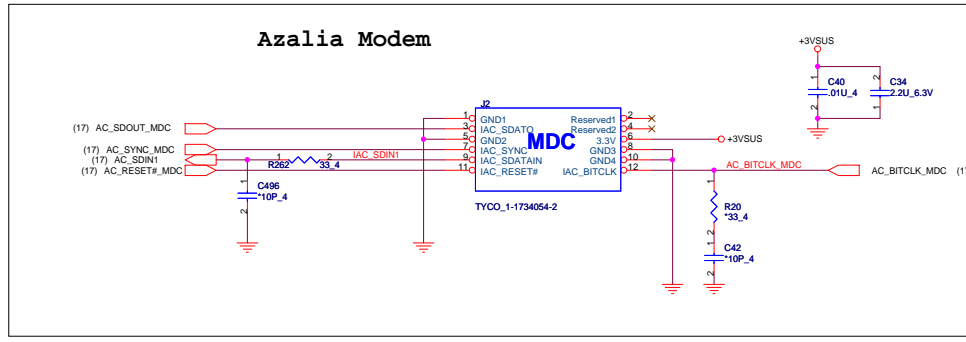
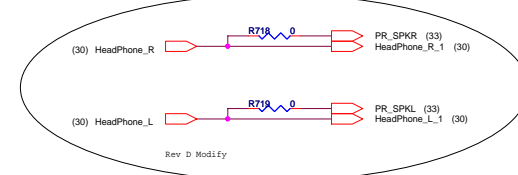
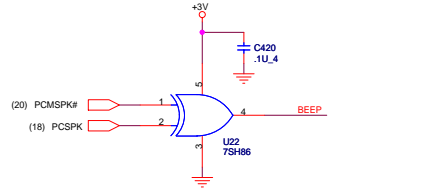
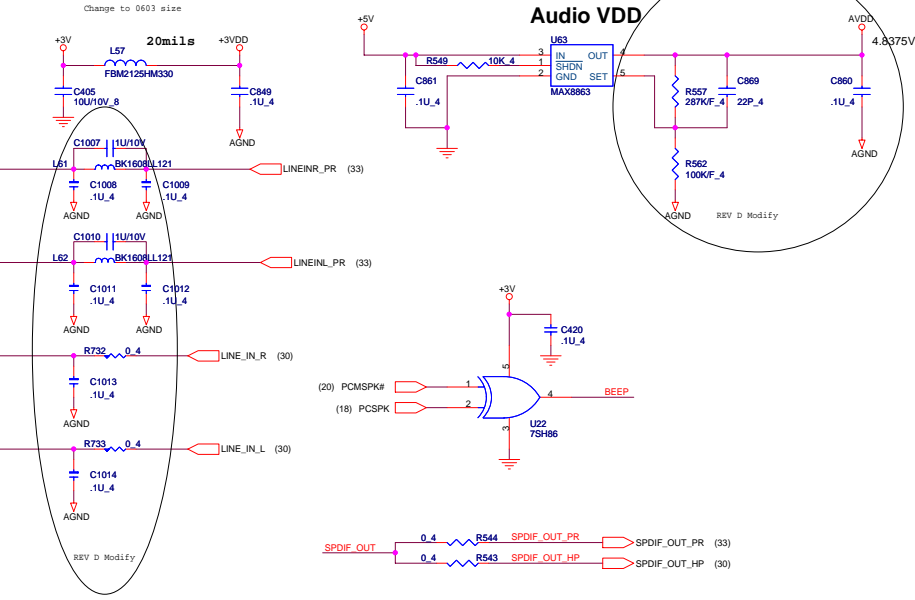
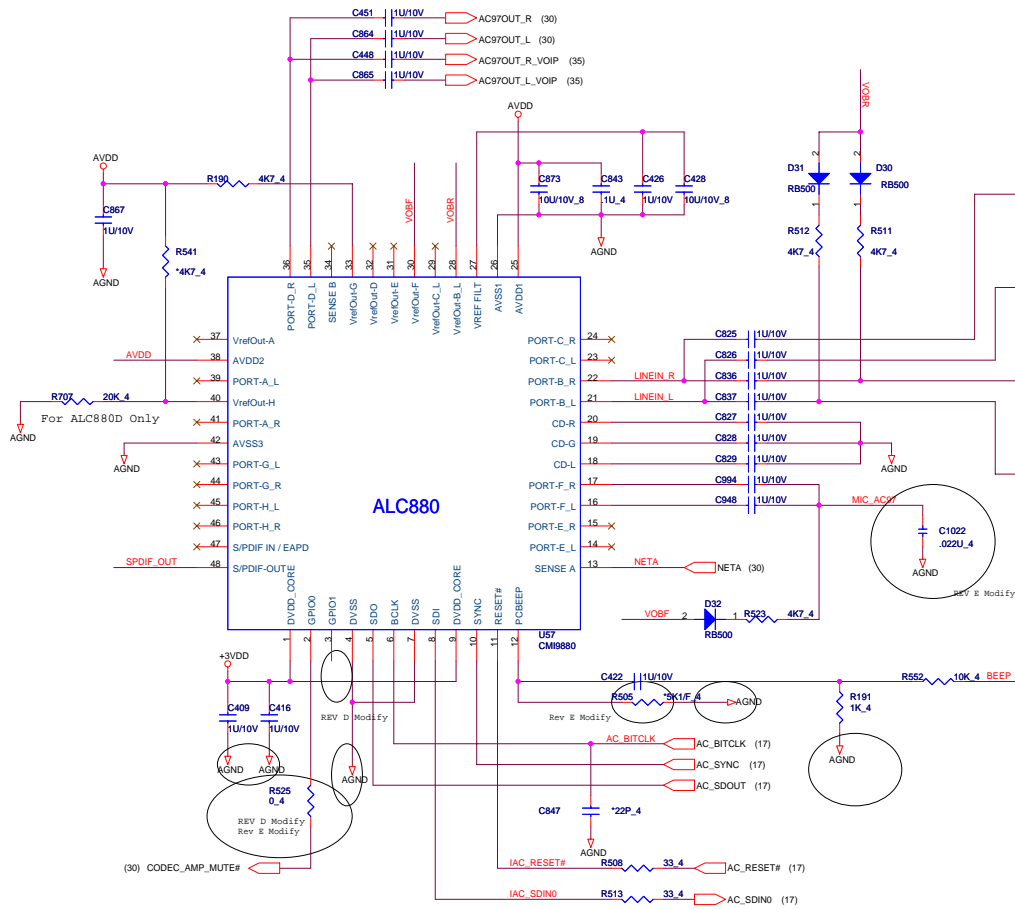
Size	Document Number	Rev
	LIGHT SENSOR,FAN,LED BD,TP	A3A
Date:	Tuesday, August 02, 2005	Sheet 27 of 43





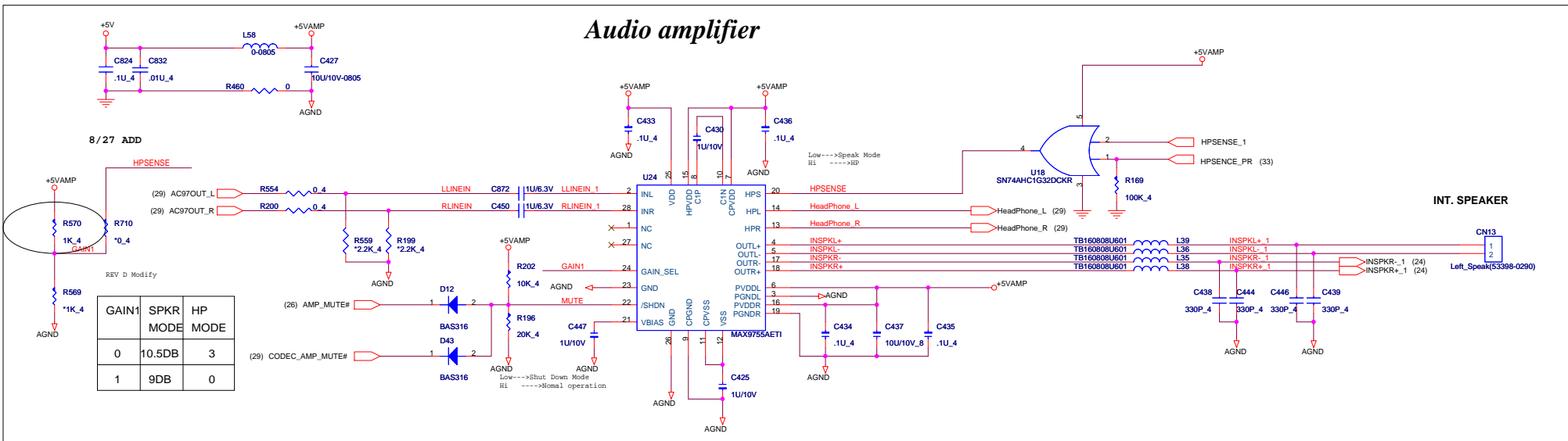
PROJECT : ZF1A
Quanta Computer Inc.

Size	Document Number	Rev
	MINI-PCI	A3A
Date:	Tuesday, August 02, 2005	Sheet 28 of 43

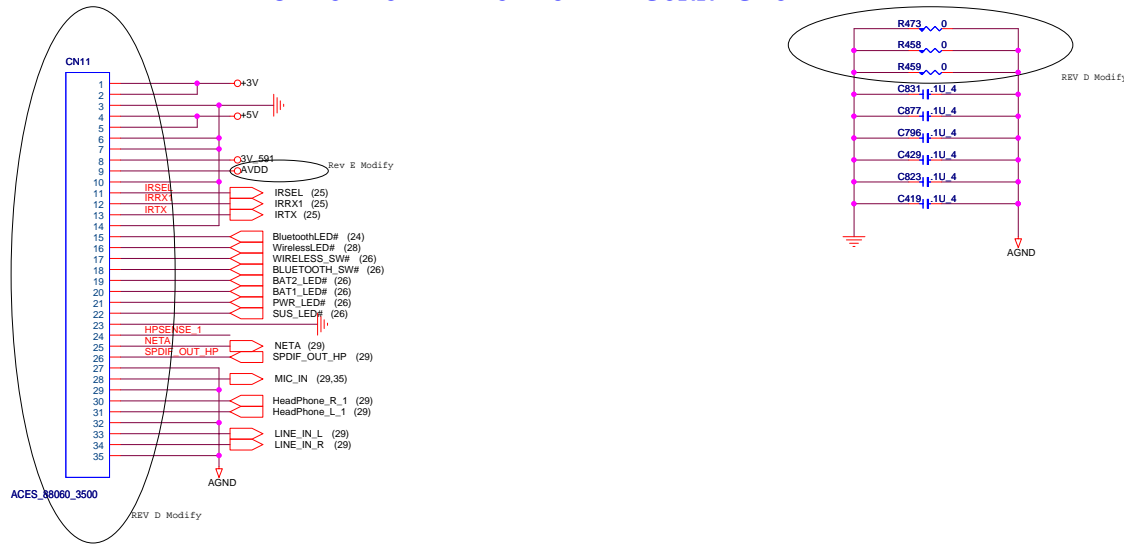


SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1

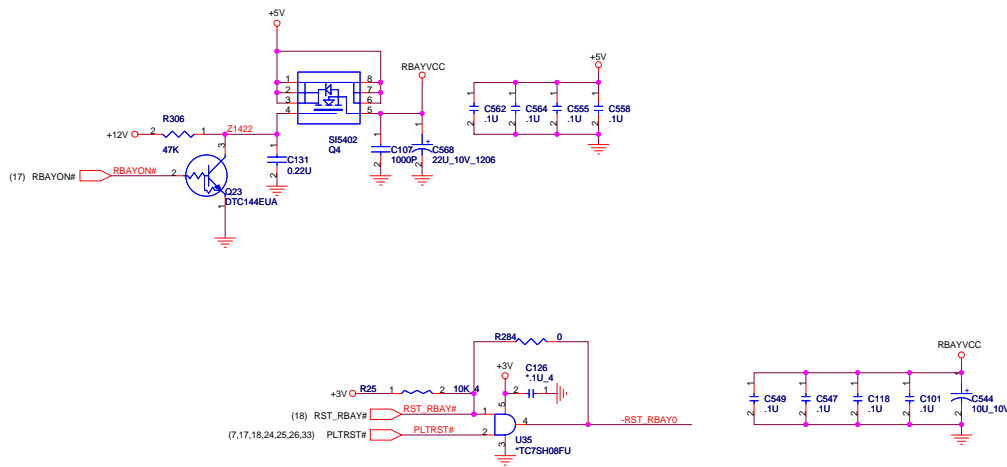
Audio amplifier



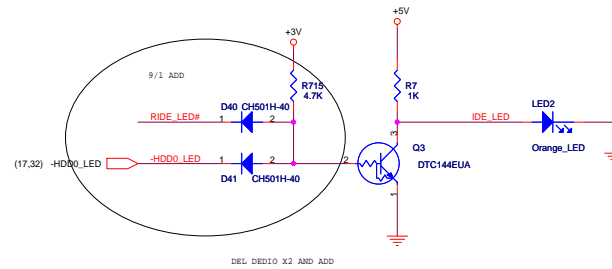
AUDIO BOARD TO BOARD CONNECTOR



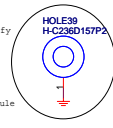
SWAP BAY POWER CONTROL & RESET



IDE LED CONTROL LOGIC

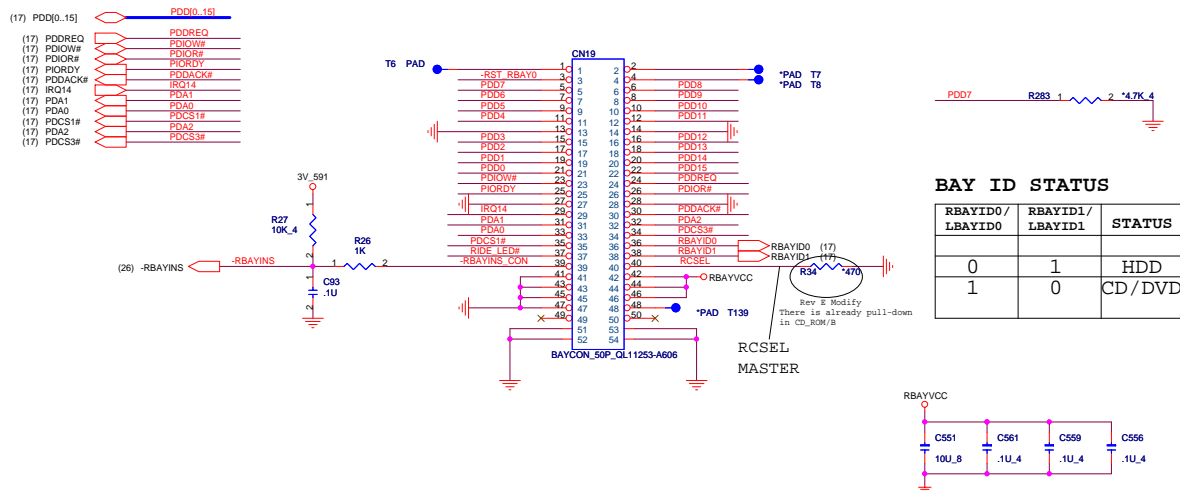


Rev E Modify



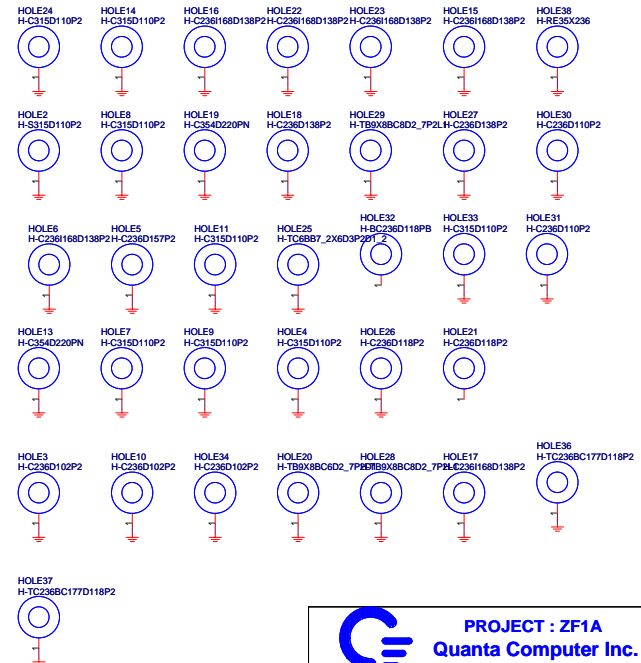
Screw hole for Modem Module

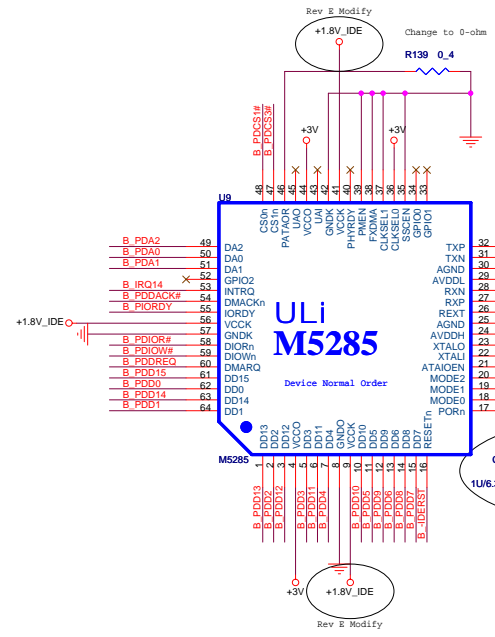
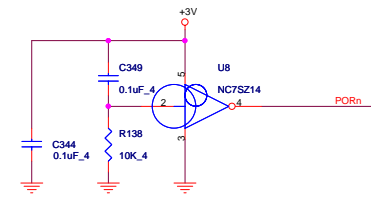
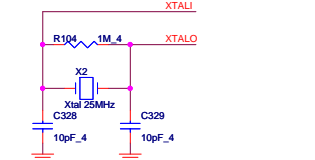
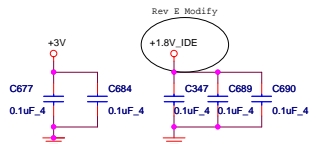
Multi-Bay Connector



BAY ID STATUS

RBAYID0 / LBAYID0	RBAYID1 / LBAYID1	STATUS
0	1	HDD
1	0	CD / DVD





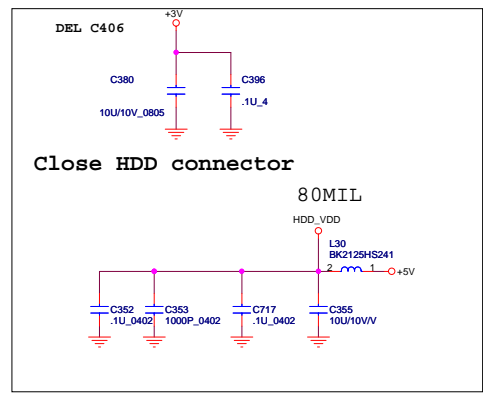
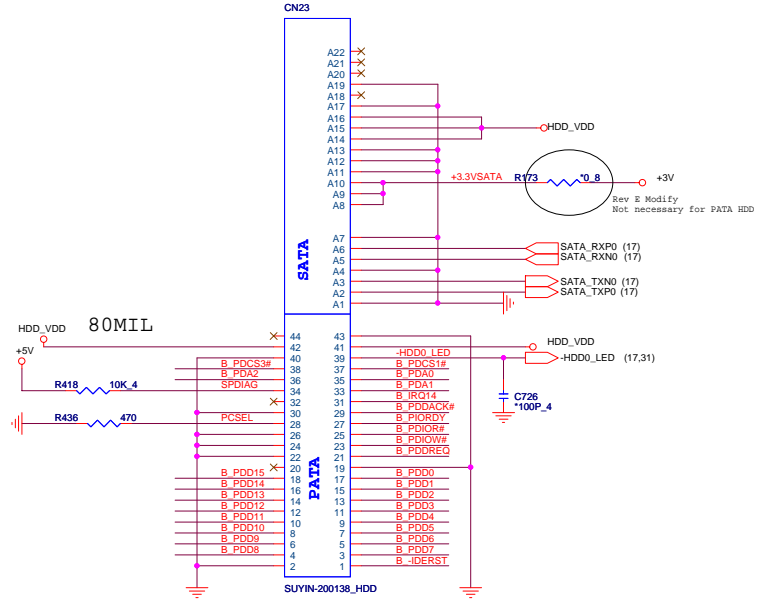
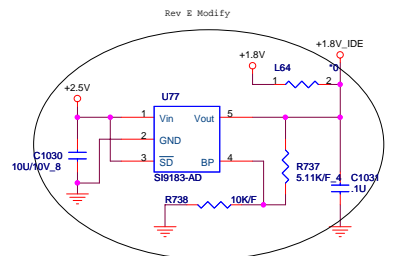
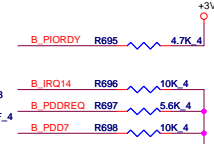
Rrxt Place near IC

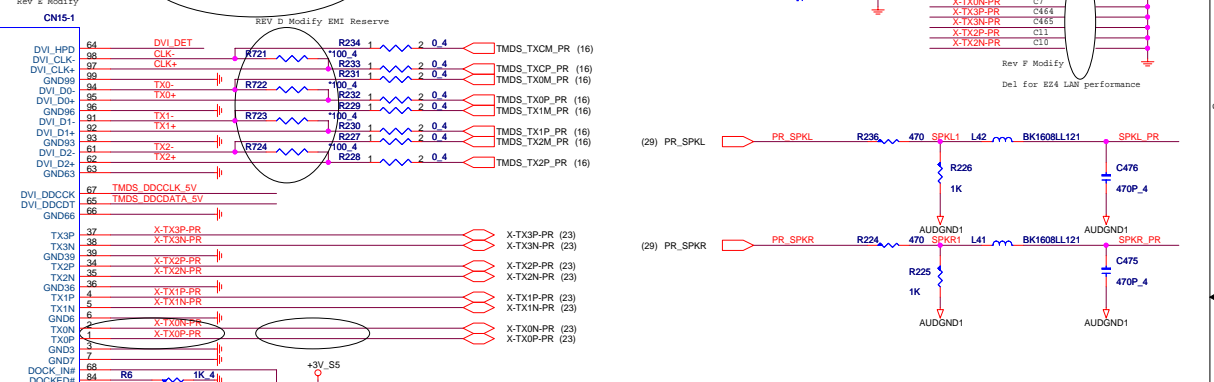
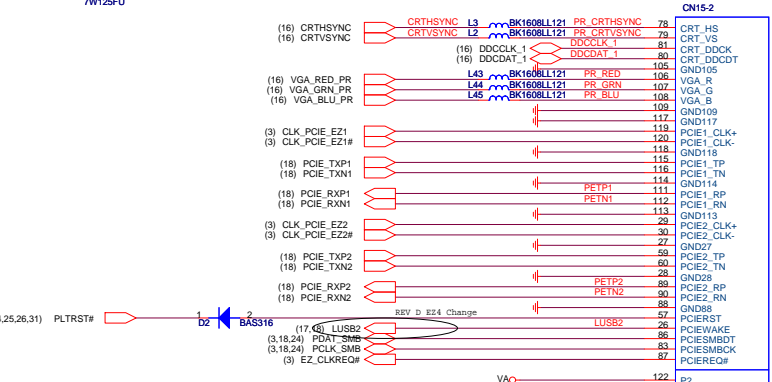
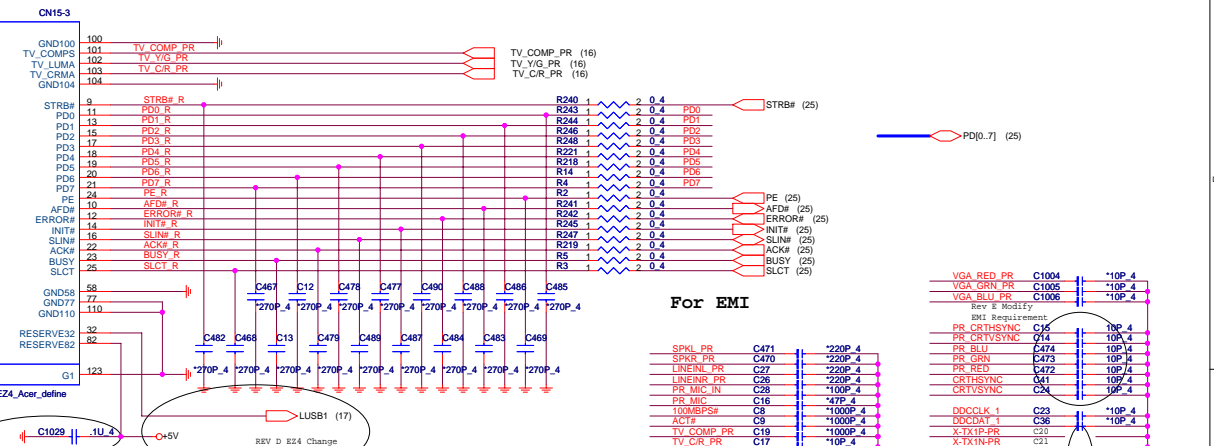
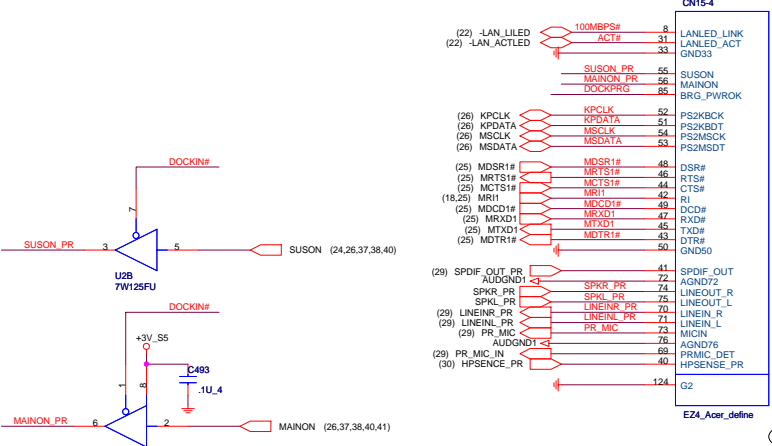
Operation Mode

MODR[2..0]	Device mode
0 0 0	Device mode 100MB/S
0 0 1	Device mode 133MB/S
0 1 0	Device mode 150MB/S
0 1 1	RESERVE
1 0 0	Host mode 100MB/S
1 0 1	Host mode 133MB/S
1 1 0	Host mode 150MB/S
1 1 1	RESERVE

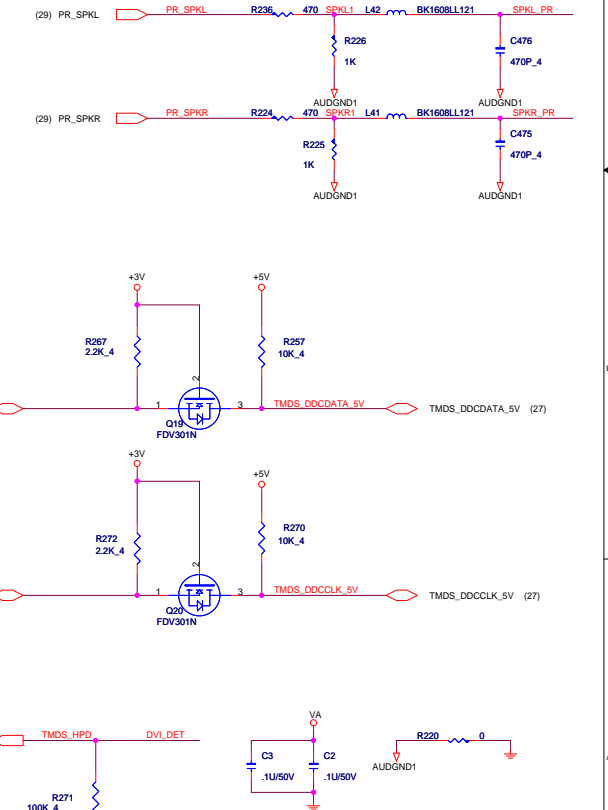
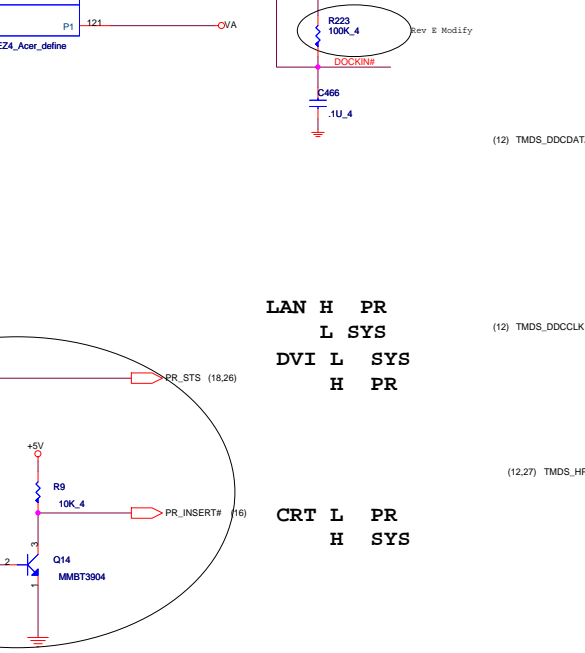
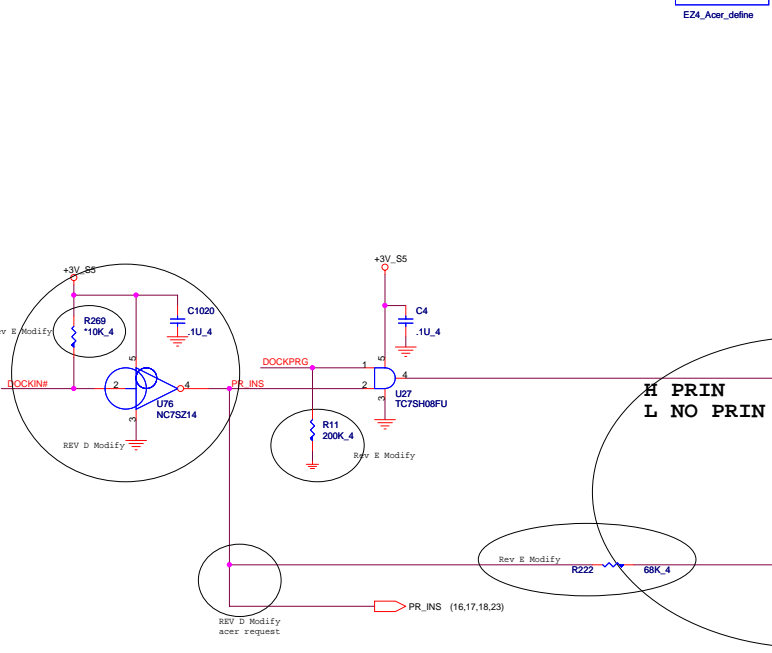
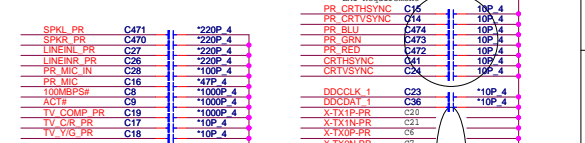
Reference clock select

CLKSEL[1..0]	External clock
0 0	20 MHz
0 1	25 MHz





FOR EMI

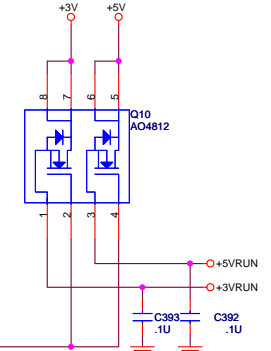
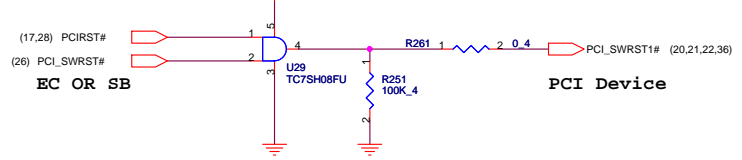
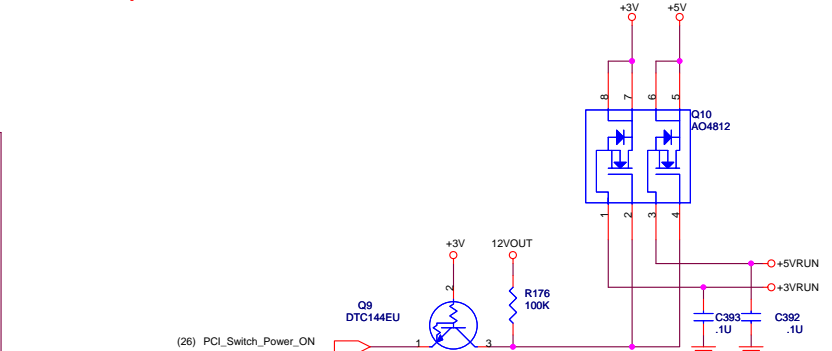
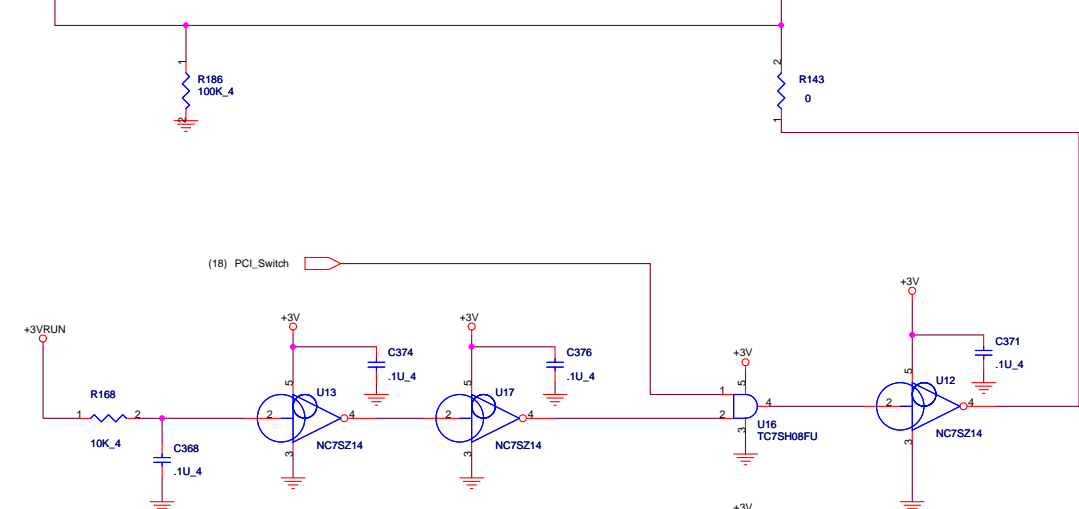
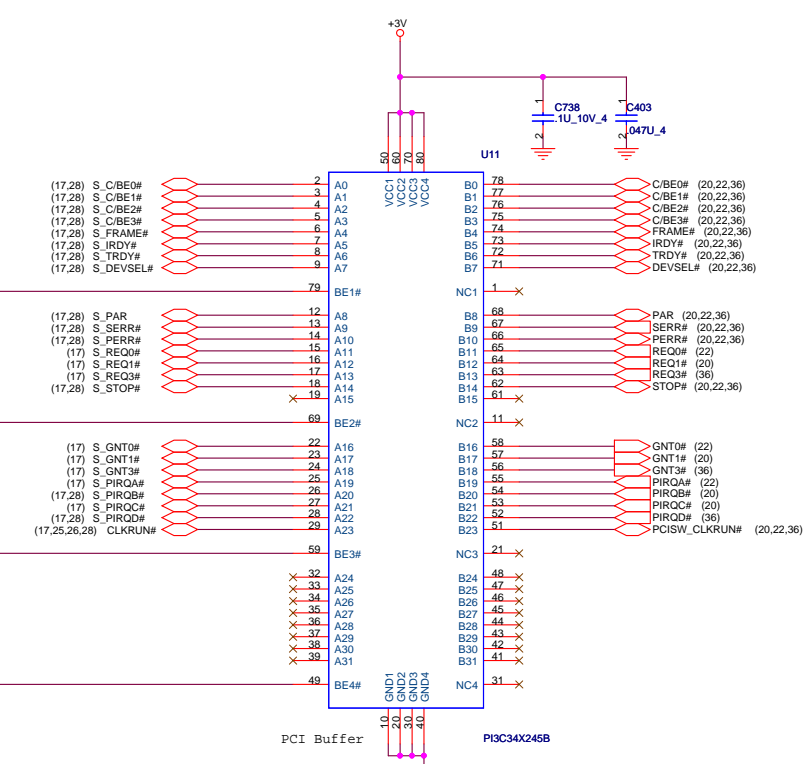
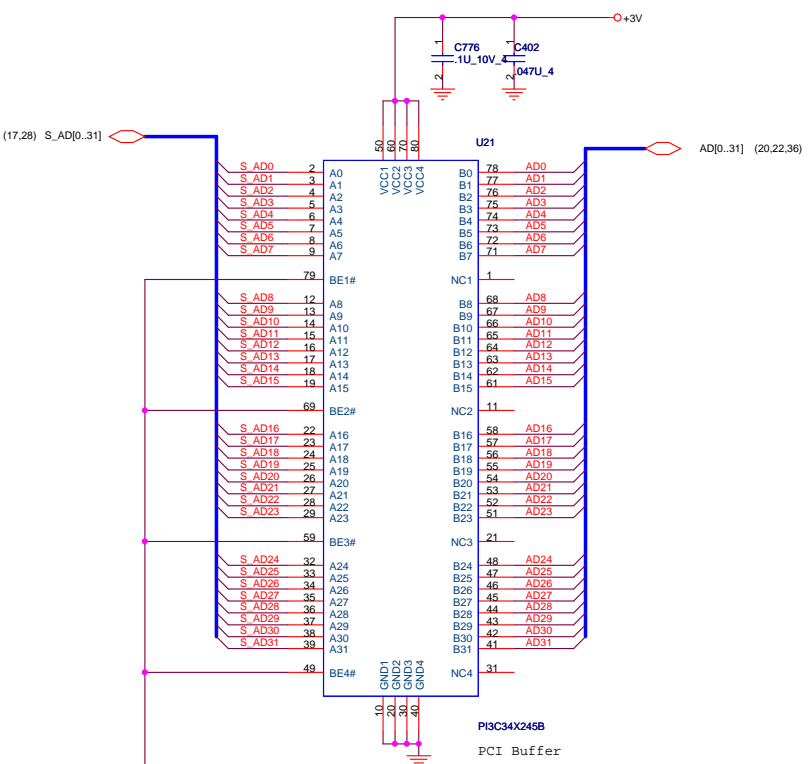


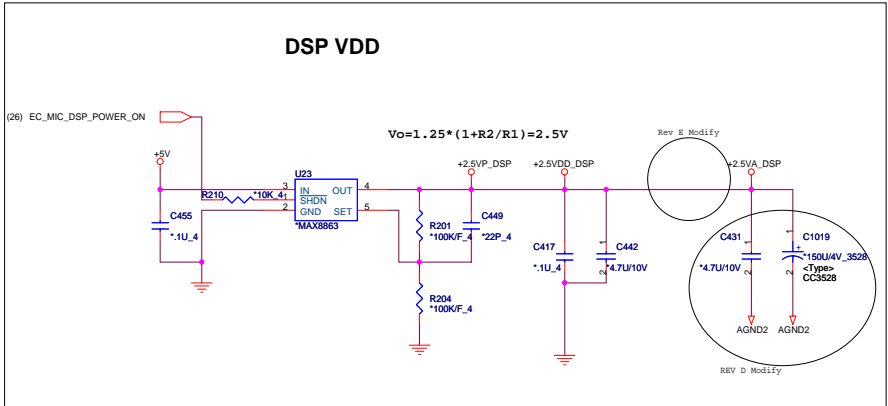
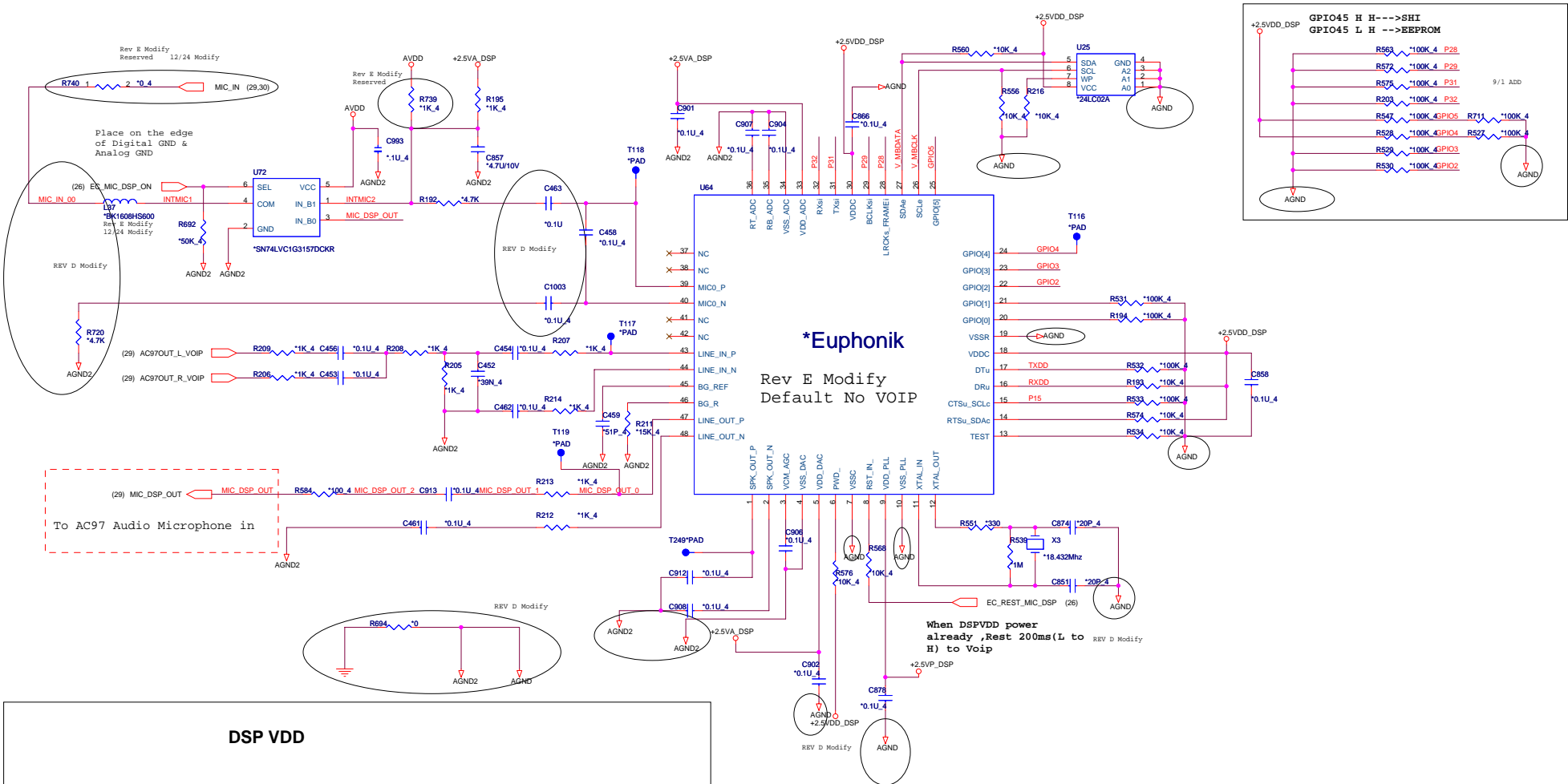
LAN H PR
L SYS

DVI L SYS
H PR

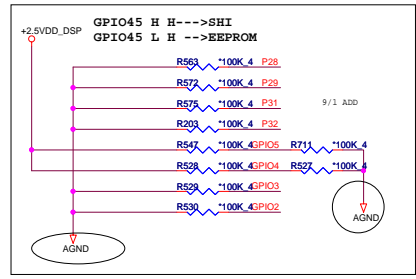
CRT L PR
H SYS

PROJECT : ZF1A
Quanta Computer Inc.

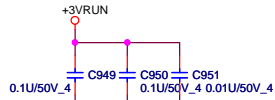




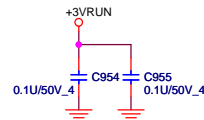
When EC_MIC_DSP_ON
 -->LOW Internal Mic bypass DSP
 When EC_MIC_DSP_ON
 -->Hi Internal Mic to DSP
 processor



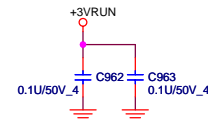
IEEE-1394



Used for vccp
(Pin20,35,48,62,78)



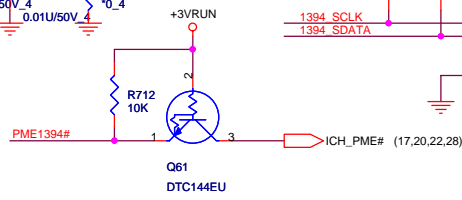
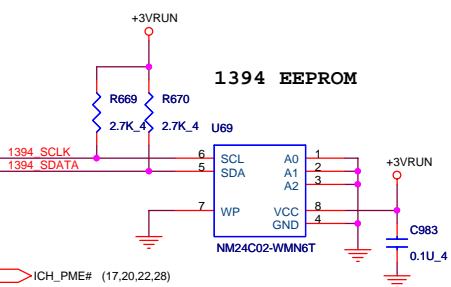
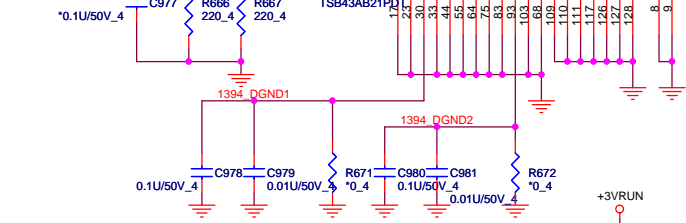
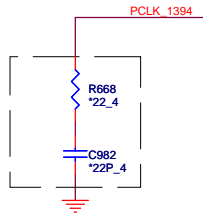
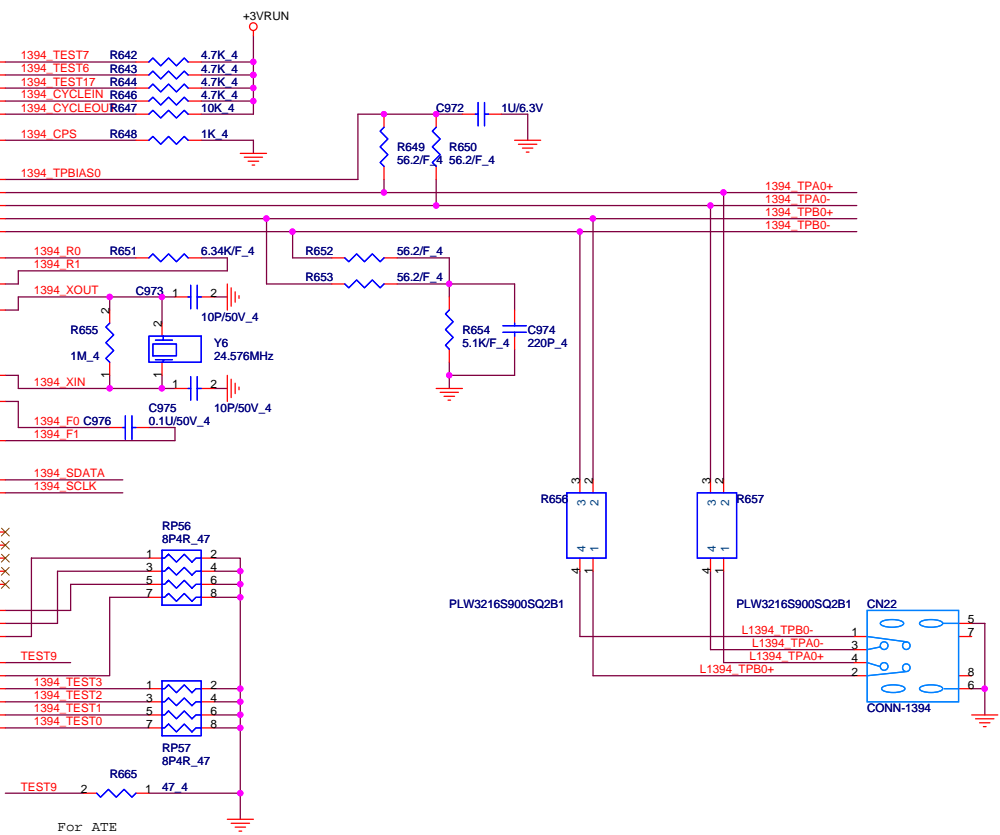
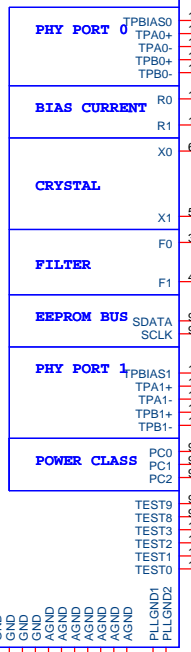
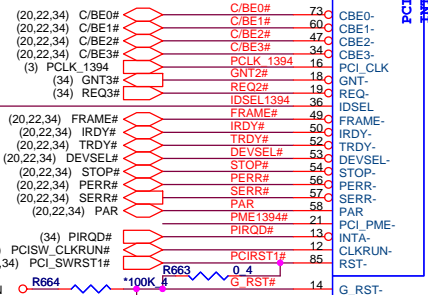
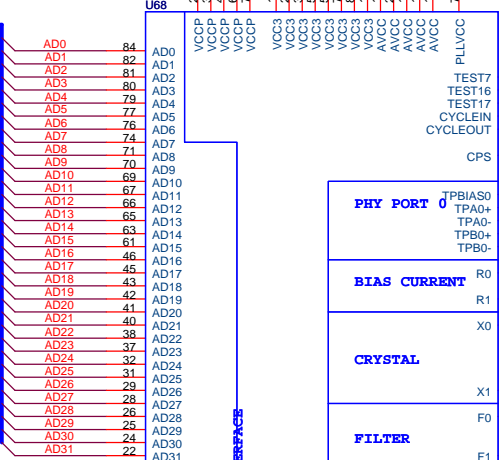
Used for vcc3
(Pin15,27,39,51,59,72,88,100)




Used for AVCC
(Pin1,2,107,108,120)

ID Select : AD23
Interrupt Pin : PIRQD#
Request indicates : REQ3#
Grant indicates : GNT3#

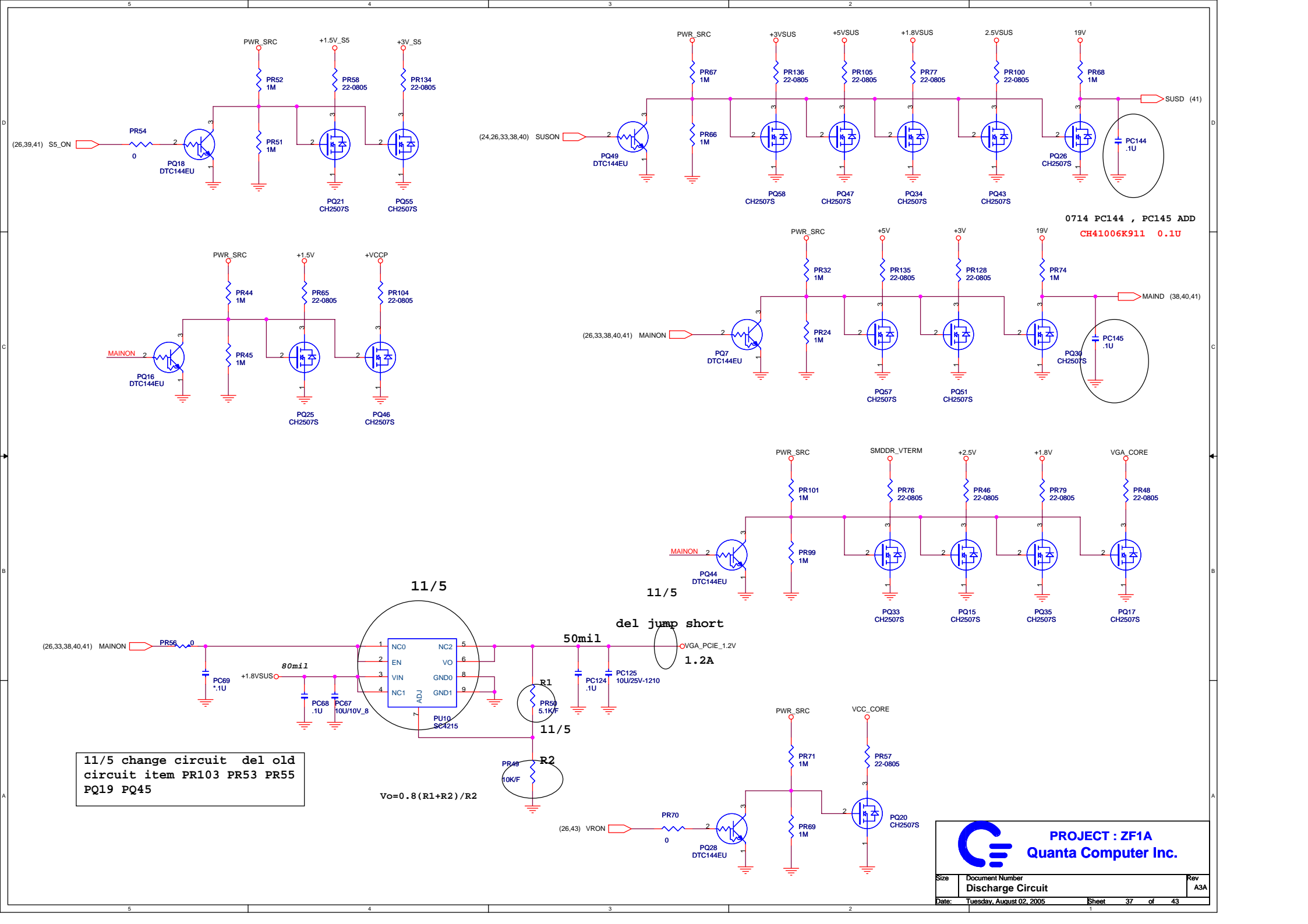
(20,22,34) AD[0..31] AD0..31





PROJECT : ZF1A
Quanta Computer Inc.

Size	Document Number IEEE 1394(TSB43AB21)	Rev A3A
Date:	Tuesday, August 02, 2005	Sheet 36 of 43



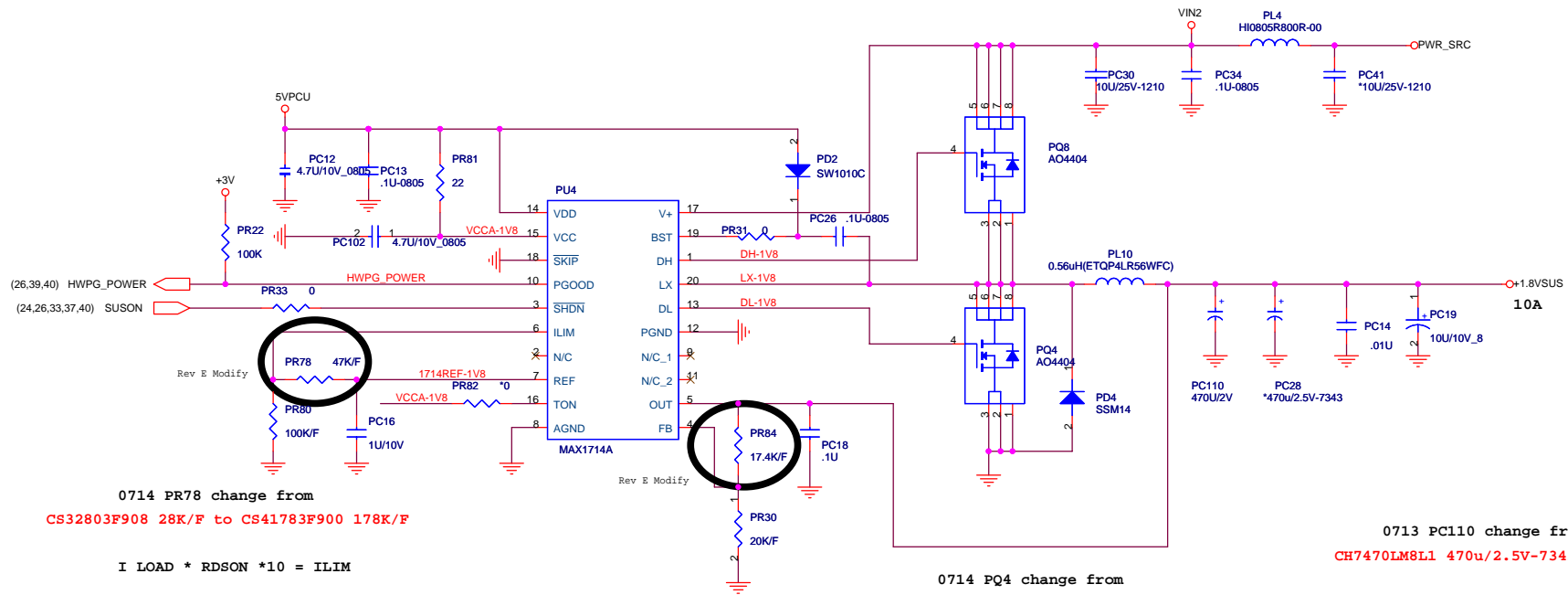
0714 PC144 , PC145 ADD
CH41006K911 0.1U

11/5 change circuit del old circuit item PR103 PR53 PR55 PQ19 PQ45

$$V_o = 0.8 (R1 + R2) / R2$$

PROJECT : ZF1A
Quanta Computer Inc.

Size	Document Number	Rev
	Discharge Circuit	ASA
Date:	Tuesday, August 02, 2005	Sheet 37 of 43

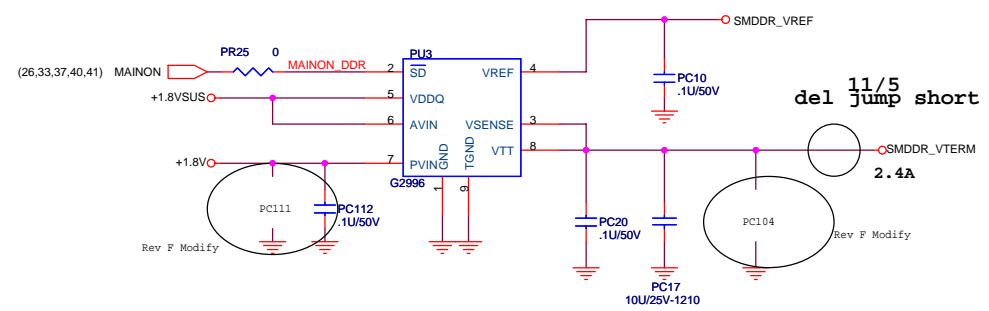
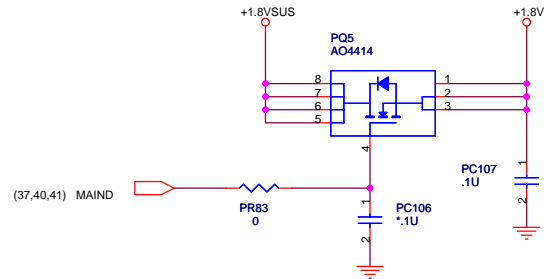
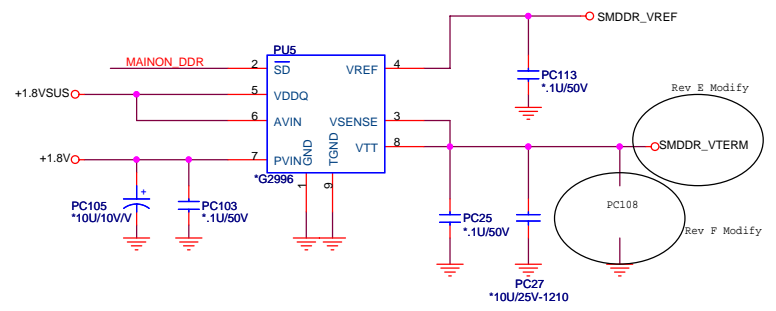


0714 PR78 change from
 CS32803F908 28K/F to CS41783F900 178K/F

I LOAD * RDSON * 10 = ILIM
 FDD6688 RDSON 4.5V = 0.006 ohm
 12 * 0.006 * 10 = 0.72V (ILIM)

0714 PQ4 change from
 BAM47040005 AO4704 to BAM66880201 FDD6688
 0714 PD4 change from
 NC to BC000014201 SSM14

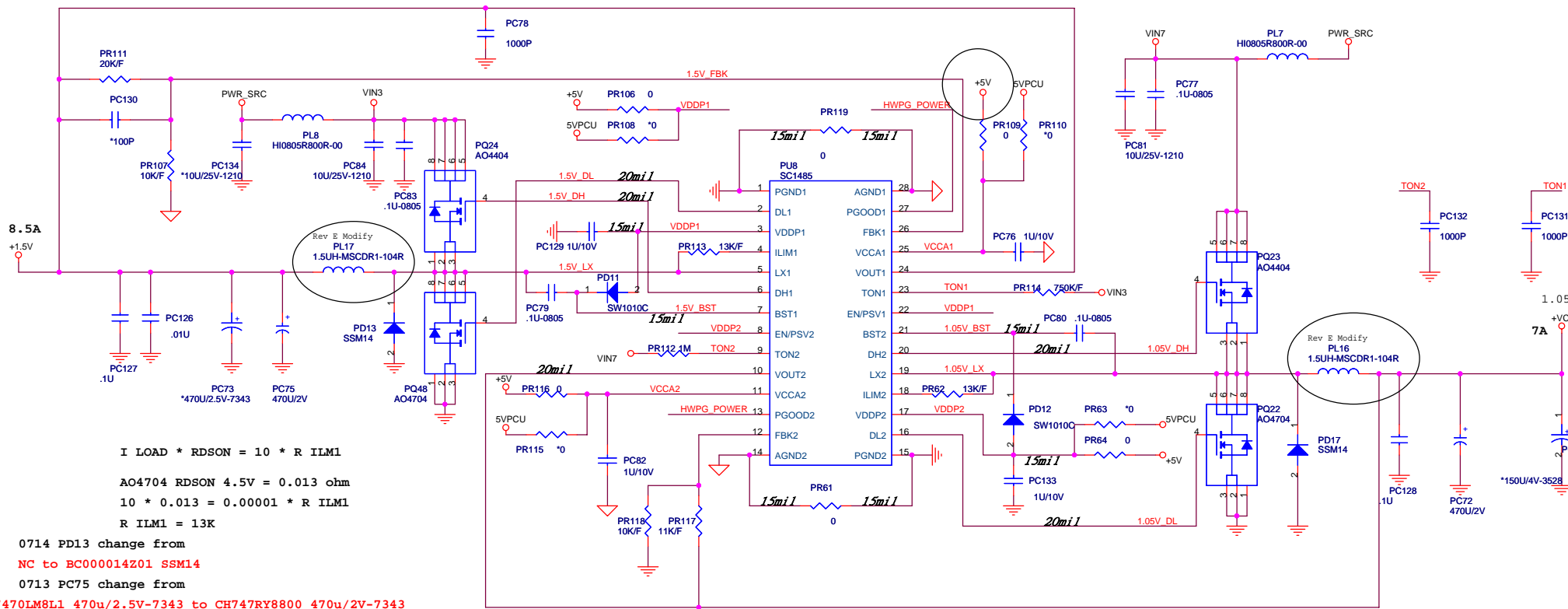
0713 PC110 change from
 CH7470LM8L1 470u/2.5V-7343 to CH747RY8800 470u/2V-7343



del 11/5
 jump short
 2.4A

PROJECT : ZF1A
Quanta Computer Inc.

Size	Document Number	Rev
	1.8VSUS/1.8V,0.9VDDR2	A3A
Date:	Tuesday, August 02, 2005	Sheet 38 of 43



$I_{LOAD} * RDSON = 10 * R_{ILM1}$
 $AO4704 RDSON 4.5V = 0.013 \text{ ohm}$
 $10 * 0.013 = 0.00001 * R_{ILM1}$
 $R_{ILM1} = 13K$

0714 PD13 change from
 NC to BC000014Z01 SSM14
 0713 PC75 change from
 CH7470LM8L1 470u/2.5V-7343 to CH747RY8800 470u/2V-7343

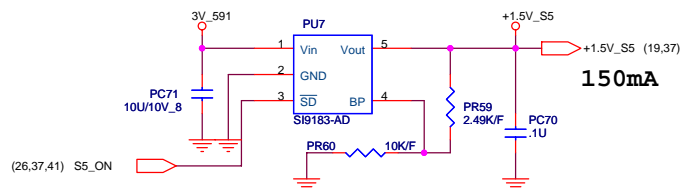
(26,38,40) HWPG_POWER ← HWPG_POWER

$I_{LOAD} * RDSON = 10 * R_{ILM}$

$AO4704 RDSON 4.5V = 0.013 \text{ ohm}$
 $10 * 0.013 = 0.00001 * R_{ILM}$
 $R_{ILM} = 13K$

0714 PD817 change from
 NC to BC000014Z01 SSM14

0713 PC72 change from
 CH7470LM8L1 470u/2.5V-7343 to CH747RY8800 470u/2V-7343

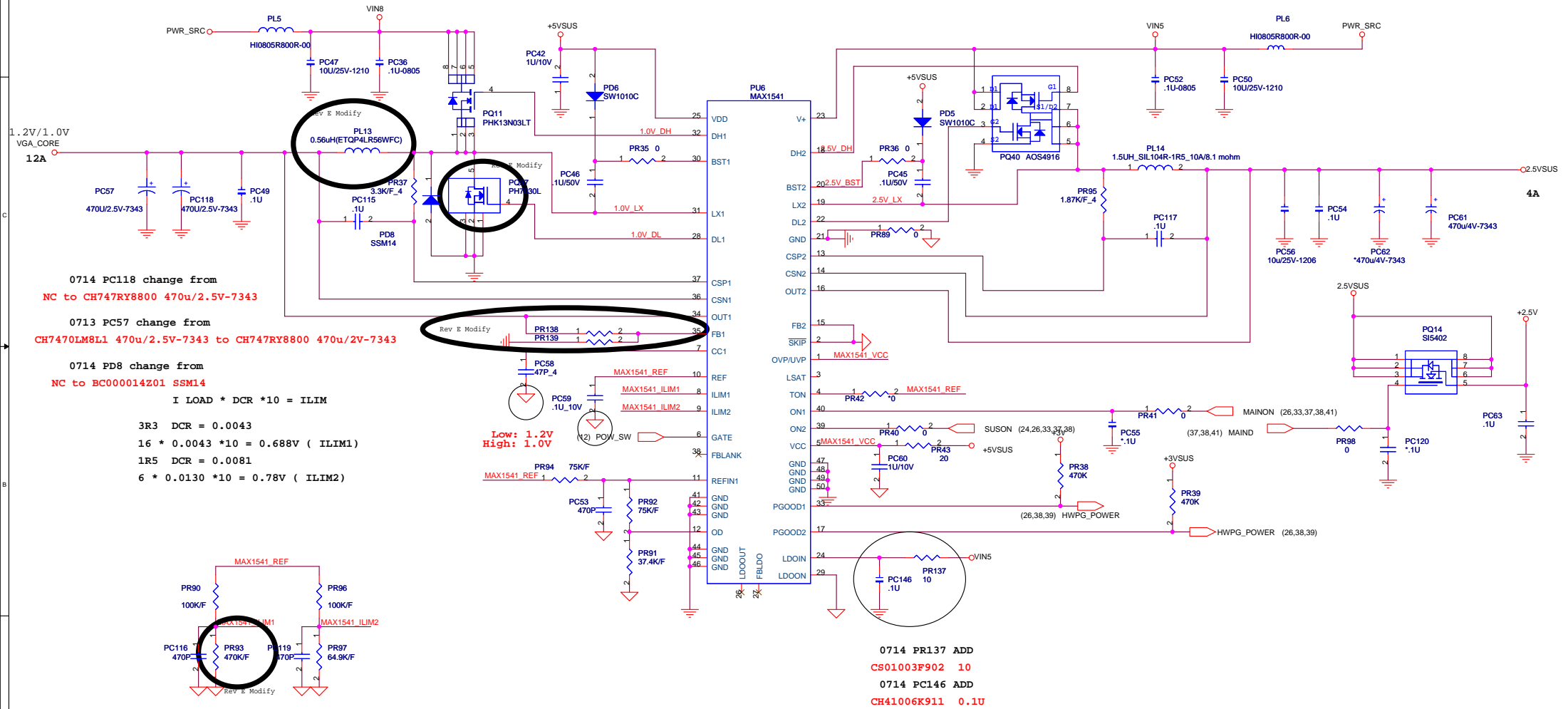


(26,37,41) SS_ON

$L / RL(DCR) = Cqe * Rqe$
 3R3 DCR = 0.0043
 $3.3u / 0.0043 = 0.1u * Rqe$
 $Rqe = 7.68K$

0714 PR37 change from
CS21823F902 1.82K/F to CS27683F909 7.68K/F
 0714 PL13 change from
CV-15A0MZ05 1R5 to CV-33E0MZ01 3R3
 0714 PQ11 change from
BAM44040012 AO4404 to BAM60300211 FDD6030L
 0714 PQ37 change from
BAM47040005 AO4704 to BAM66880201 FDD6688

$L / RL(DCR) = Cqe * Rqe$
 3R8 DCR = 0.0130
 $3.8u / 0.0130 = 0.1u * Rqe$
 $Rqe = 2.94K$



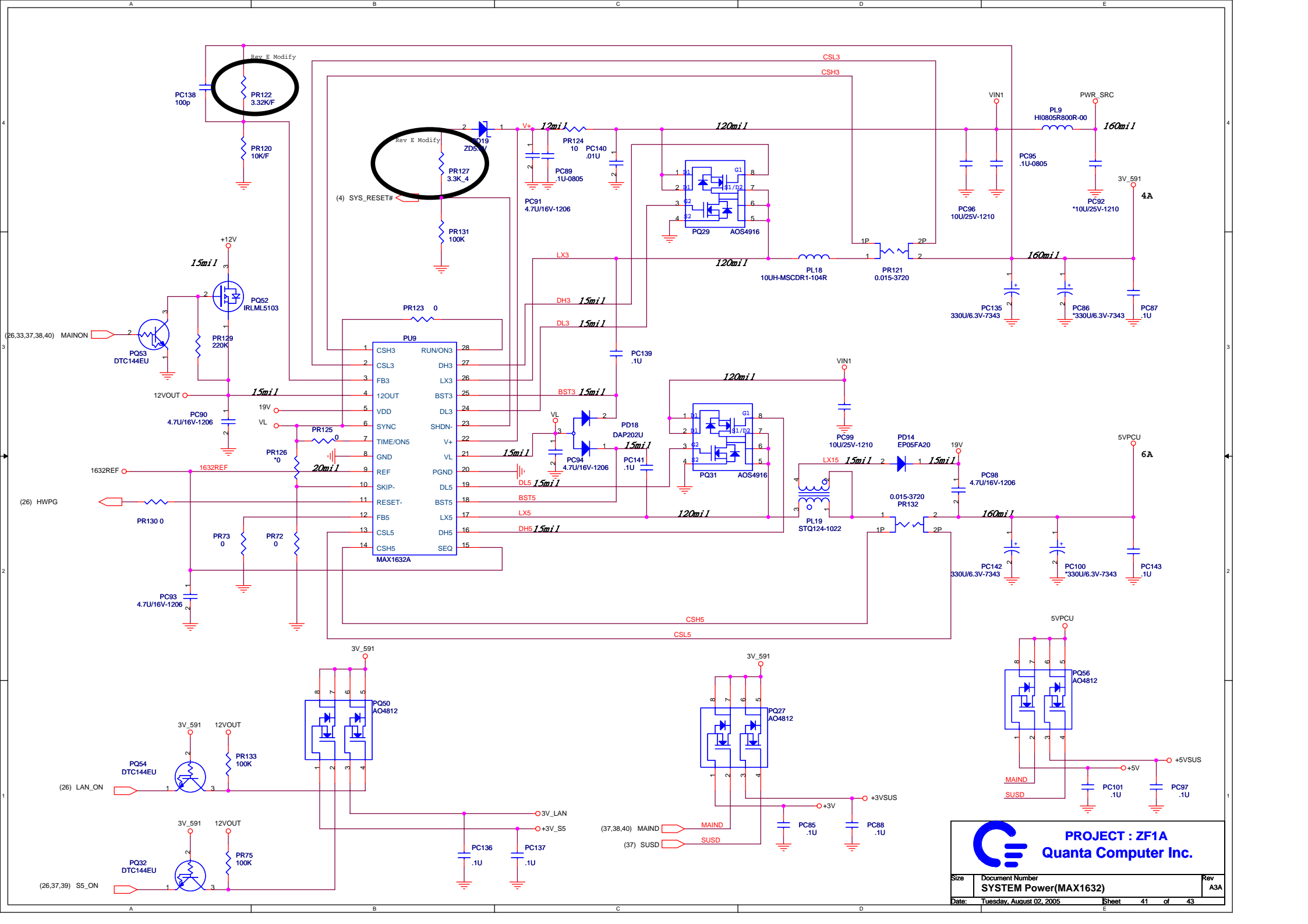
0714 PC118 change from
NC to CH747RY8800 470u/2.5V-7343
 0713 PC57 change from
CH7470LM8L1 470u/2.5V-7343 to CH747RY8800 470u/2V-7343
 0714 PD8 change from
NC to BC00014201 SSM14

$I_{LOAD} * DCR * 10 = ILIM$
 3R3 DCR = 0.0043
 $16 * 0.0043 * 10 = 0.688V (ILIM1)$
 1R5 DCR = 0.0081
 $6 * 0.0130 * 10 = 0.78V (ILIM2)$

Low: 1.2V
 High: 1.0V

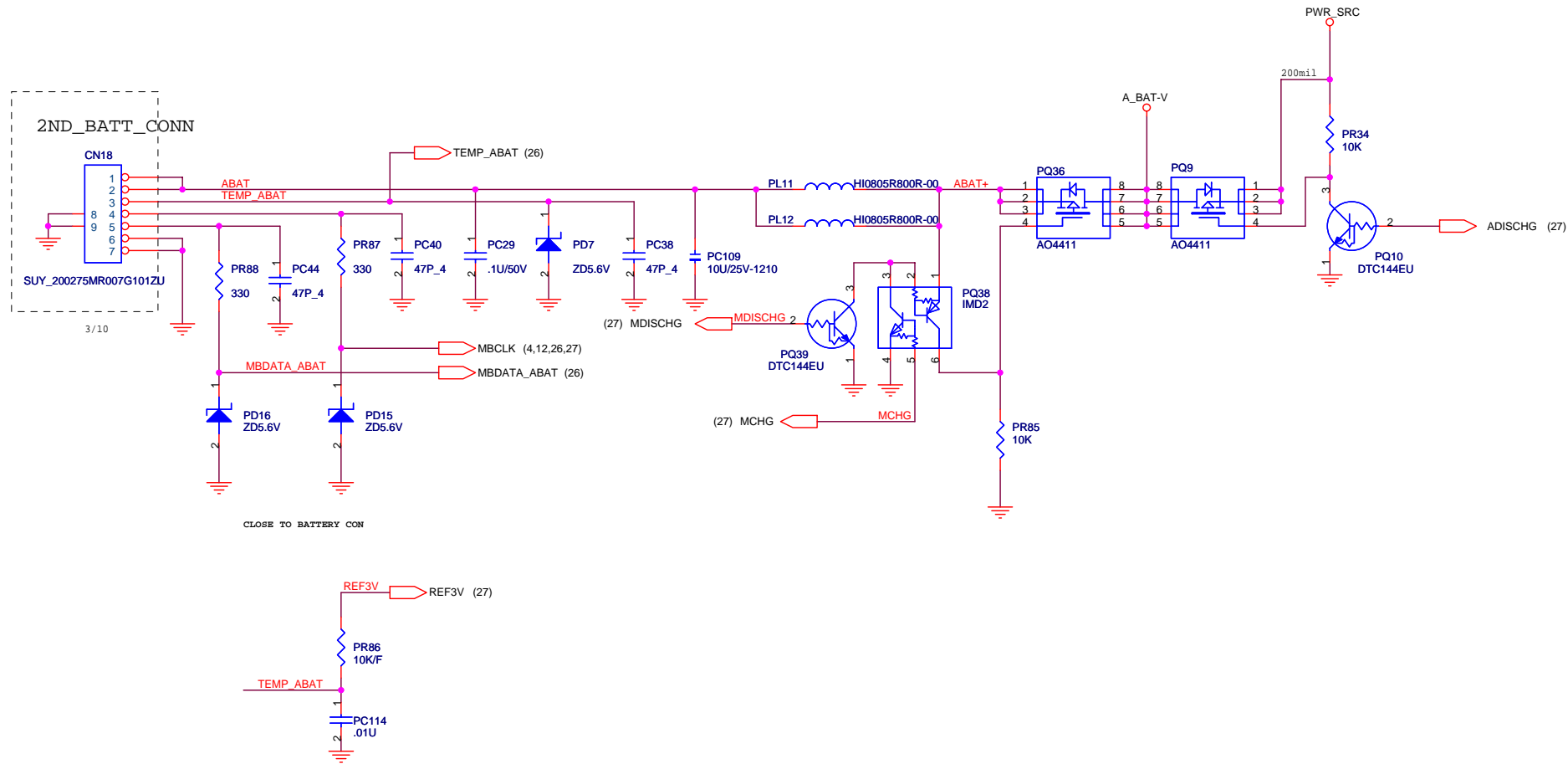
0714 PR137 ADD
CS01003F902 10
 0714 PC146 ADD
CH41006K911 0.1U

0714 PR93 change from
CS34993F908 49.9K/F to CS35233F908 52.3K/F



PROJECT : ZF1A
Quanta Computer Inc.

Size	Document Number	Rev
	SYSTEM Power(MAX1632)	A3A
Date:	Tuesday, August 02, 2005	Sheet 41 of 43

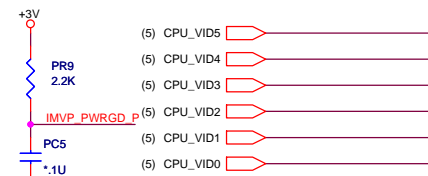
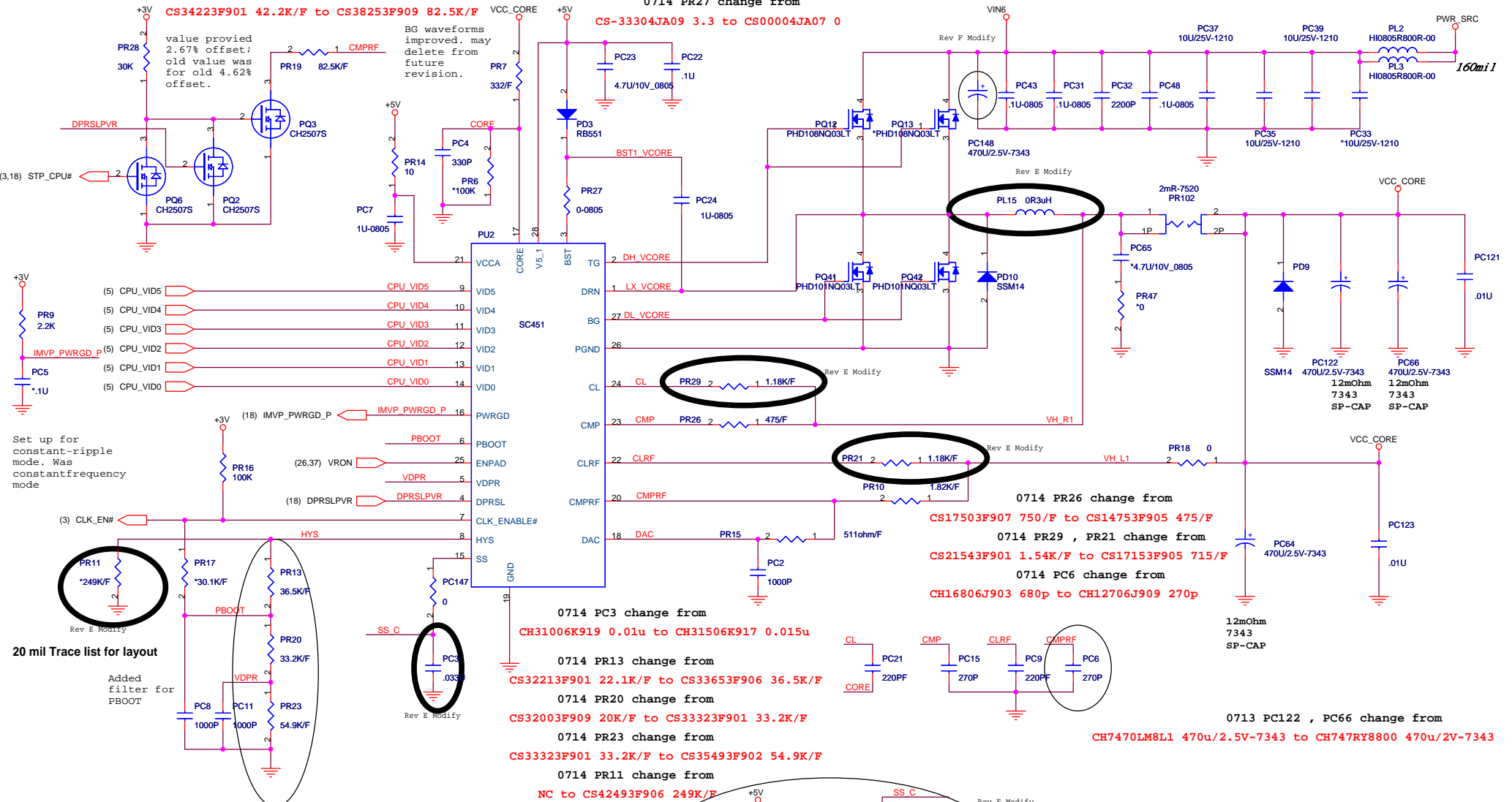


0714 PR19 change from

CS34223F901 42.2K/F to CS38253F909 82.5K/F
 value provided 2.67% offset; old value was for old 4.62% offset.
 BG waveforms improved, may delete from future revision.

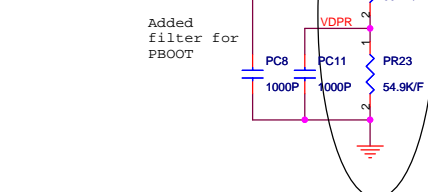
0714 PR27 change from

CS-33304JA09 3.3 to CS00004JA07 0



Set up for constant-ripple mode. Was constant-frequency mode

20 mil Trace list for layout



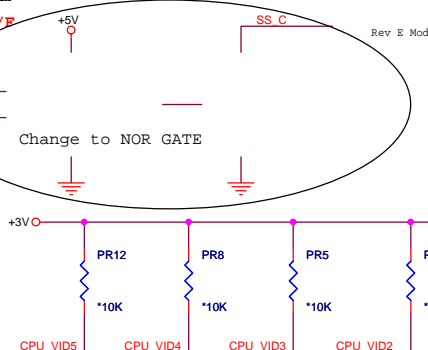
V I D						Vcore
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	V
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	1	0	1.292
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	1	1.212
1	0	0	0	0	1	1.180
1	0	0	0	1	1	1.148
1	0	0	1	1	0	1.100
1	0	1	0	0	1	1.052
1	0	1	0	1	1	1.020
1	0	1	1	1	0	0.972
1	1	0	0	0	0	0.940

100 mil Trace list for layout

DH_VCORE
 LX_VCORE
 DL_VCORE
 DH_VCORE2
 LX_VCORE2
 DL_VCORE2

10 mil Trace list for layout

SC1476
 pin 4 pin
 5 pin 7
 pin 25
 pin 30



PROJECT : ZF1A
Quanta Computer Inc.

Size: Document Number
CPU Power
 Date: Tuesday, August 02, 2005

Rev: A3A
 Sheet 43 of 43