Compal Confidential

PBL20 Project

LA-6772P REV 1.0 Schematic

Intel Sandy Bridge/Cougar Point(UMA)

2010-12-07 Rev. 1.0

Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

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Title: Cover Page

Size | Document Number: PBL20 LA6772P M/B | Rev: 1.0

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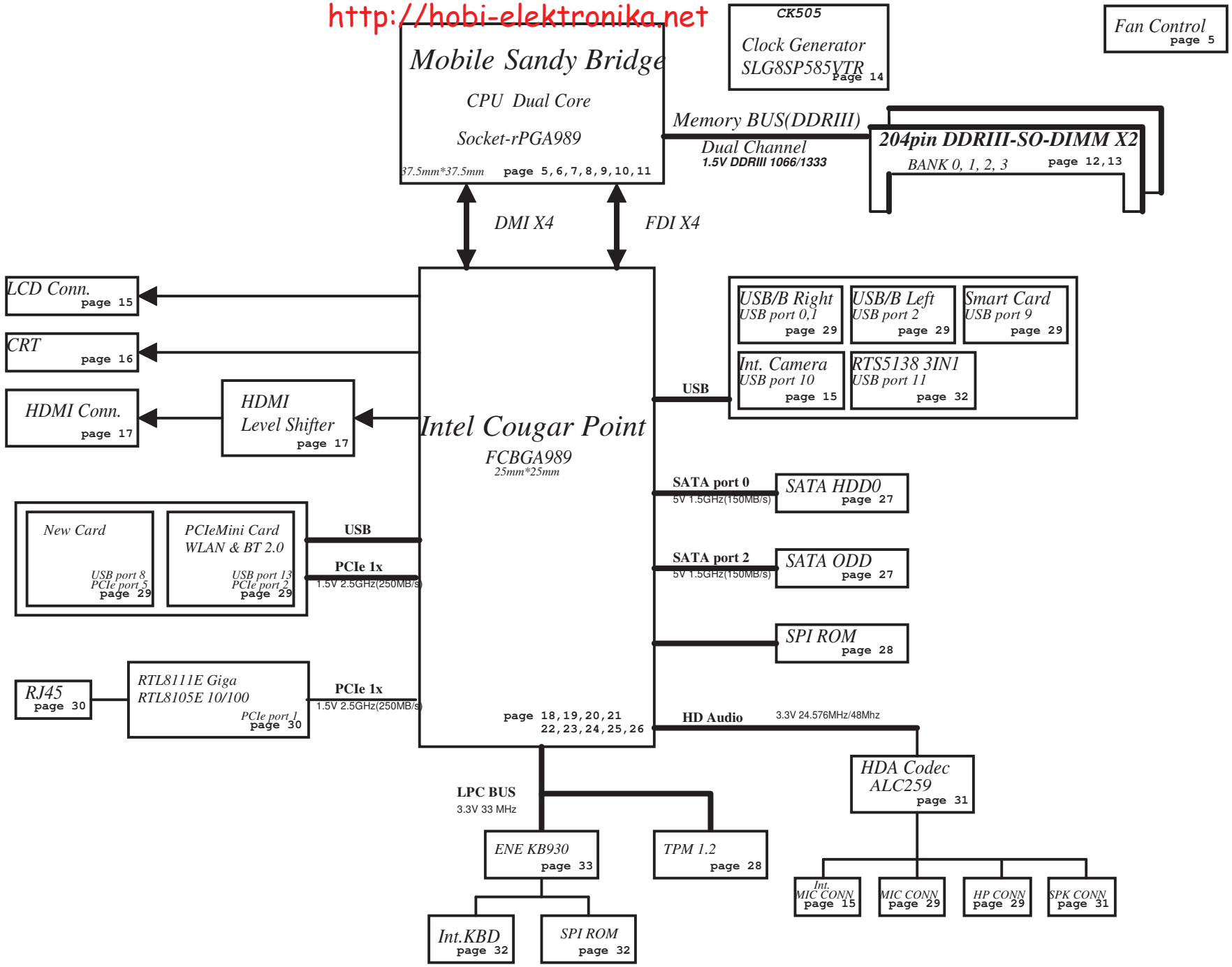
Compal Confidential
Model Name : PBL20
File Name : LA-6772P



Function/B page 29

Power/B page 34

Touch Pad/B page 34

RTC CKT. page 36

DC/DC Interface CKT. page 35

Power Circuit DC/DC page 36,37,38,39, 40,41,42,43,44

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Title: Block Diagrams

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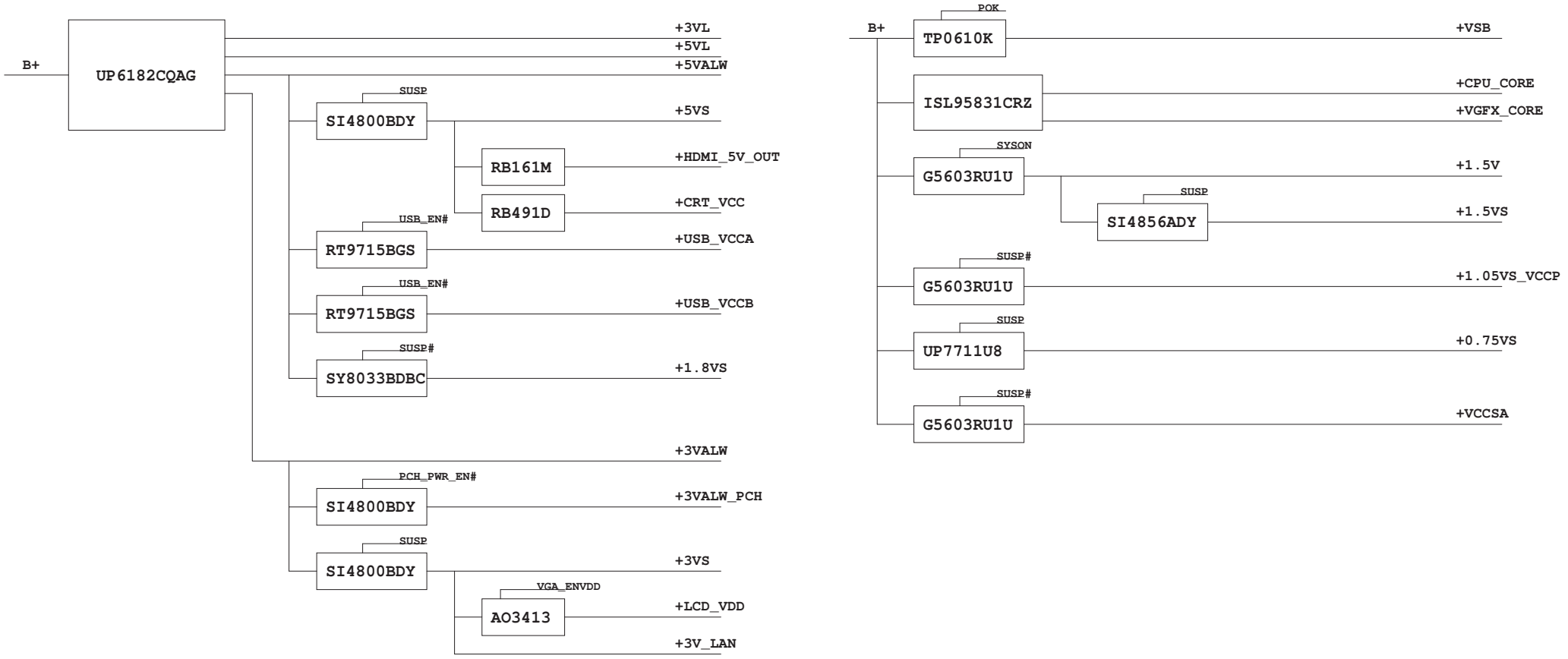

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Title: Power Map

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VCCP	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

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Title: Notes List

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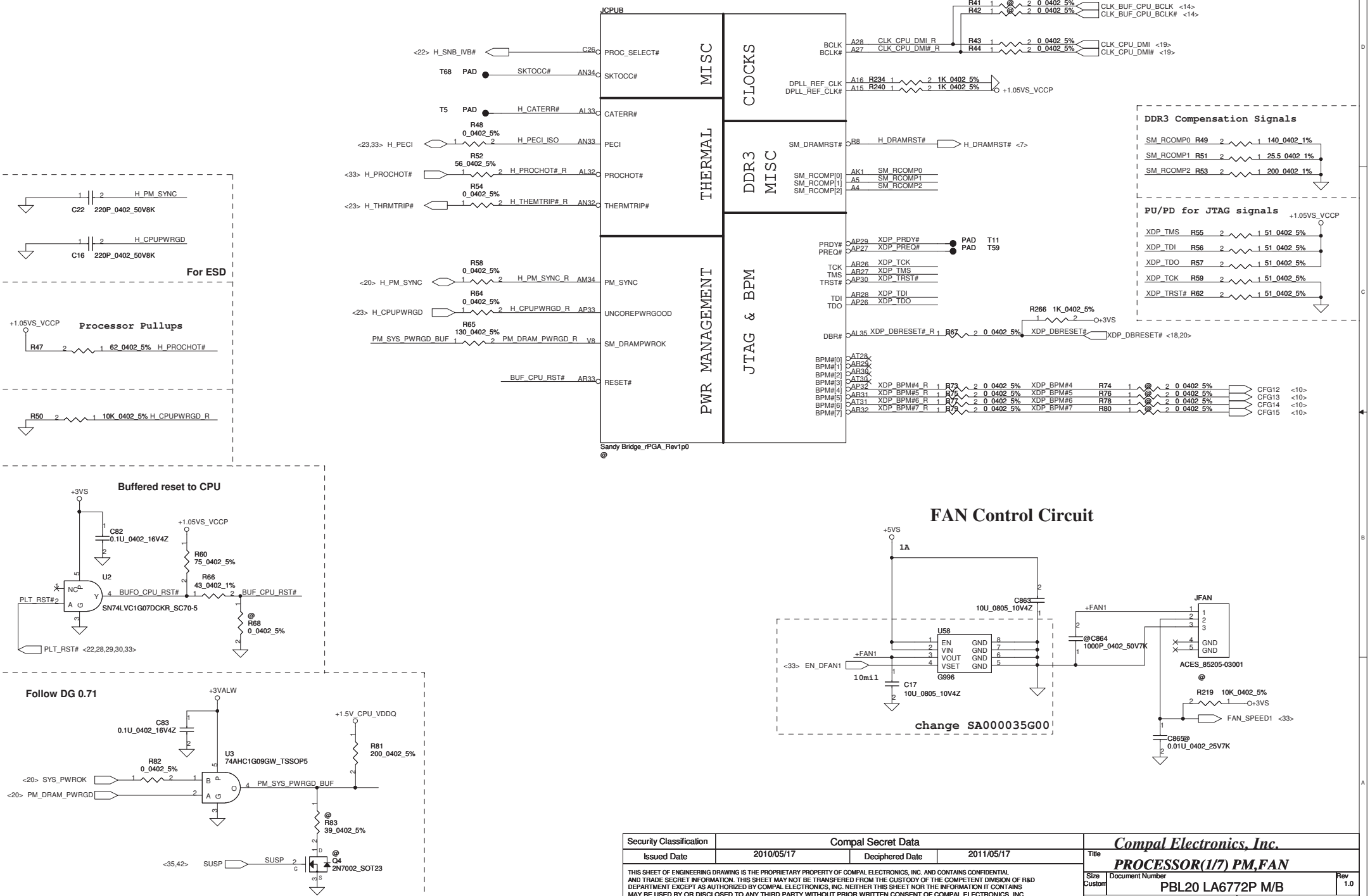

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Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.			
Title: PROCESSOR(1/7) PM,FAN			
Size: Custom	Document Number: PBL20 LA6772P M/B		Rev: 1.0
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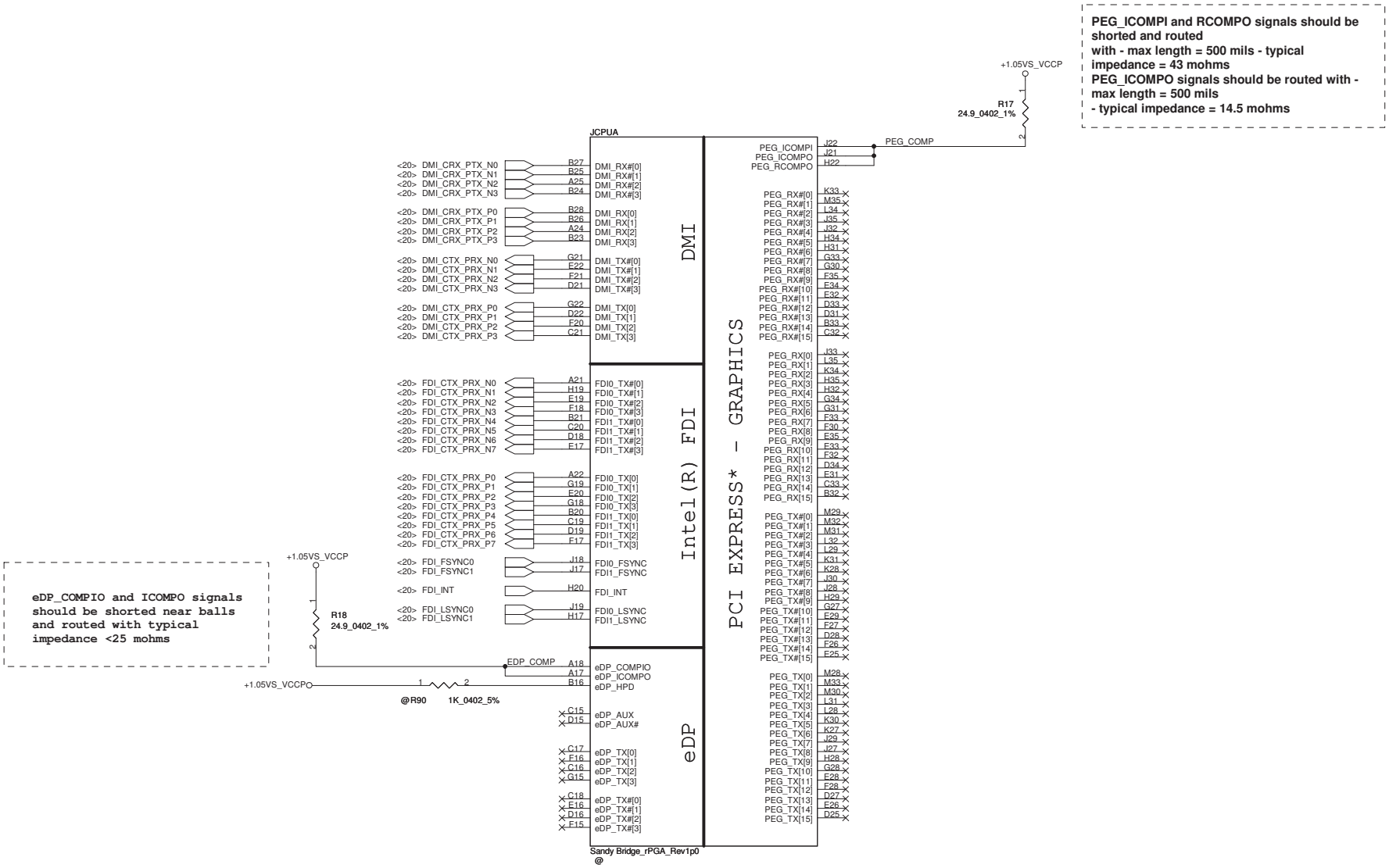

Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.

Title: PROCESSOR(2/7) DMI,FDI,PEG

Size	Document Number	Rev
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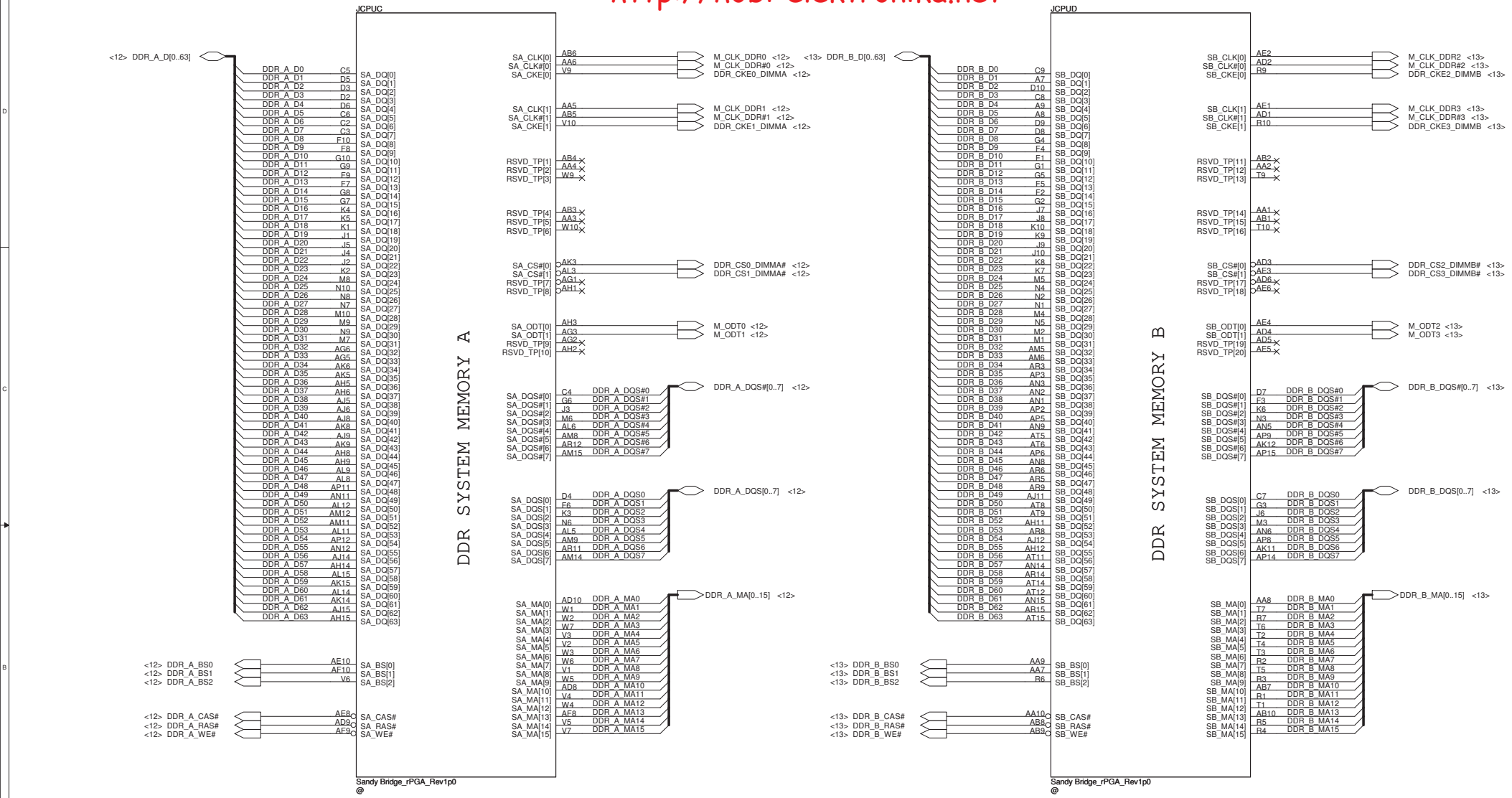

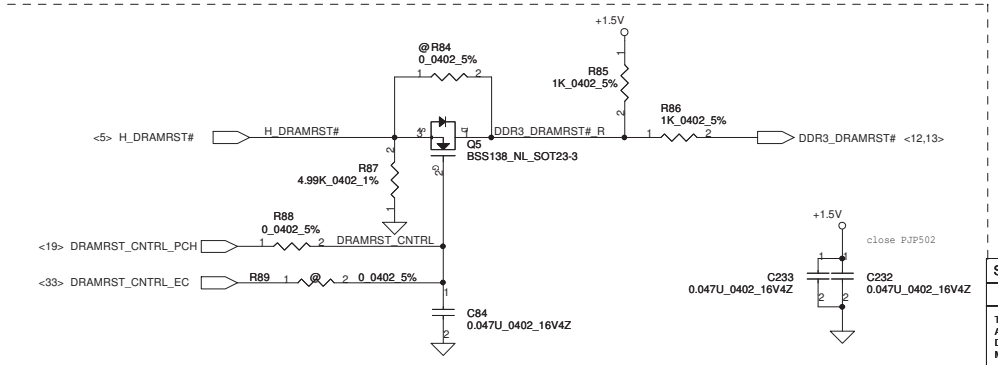

Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.

Title: PROCESSOR(3/7) DDRIII

Size	Document Number	Rev
Custom	PBL20 LA6772P M/B	1.0

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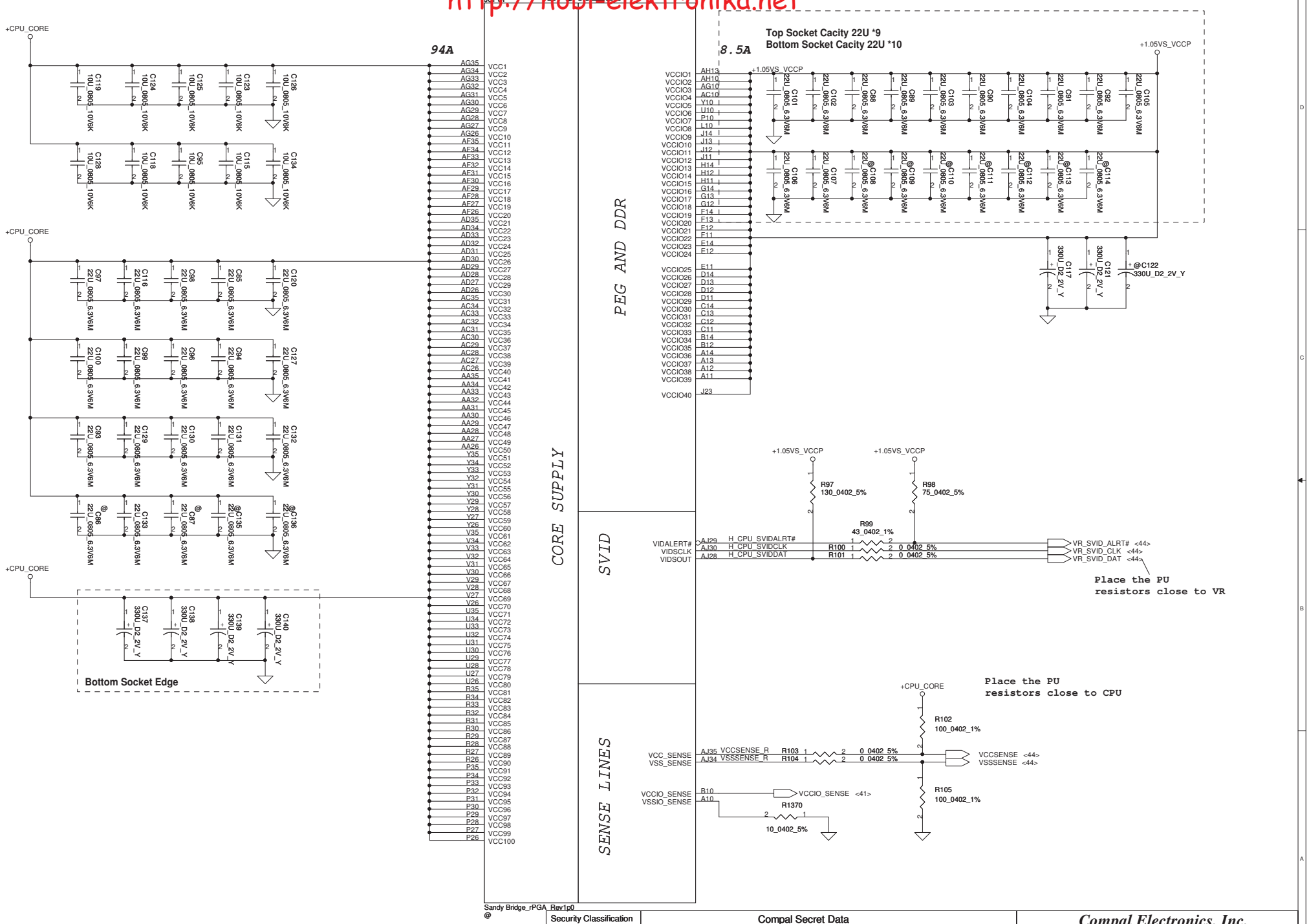

Sandy Bridge_rPGA_Rev1p0
@

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Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.

Title: PROCESSOR(4/7) PWR,BYPASS

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Custom	PBL20 LA6772P M/B	1.0

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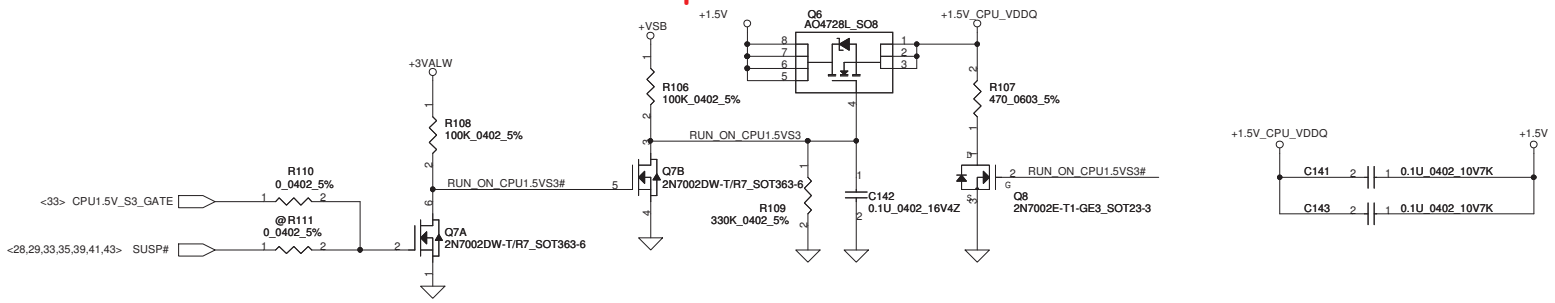
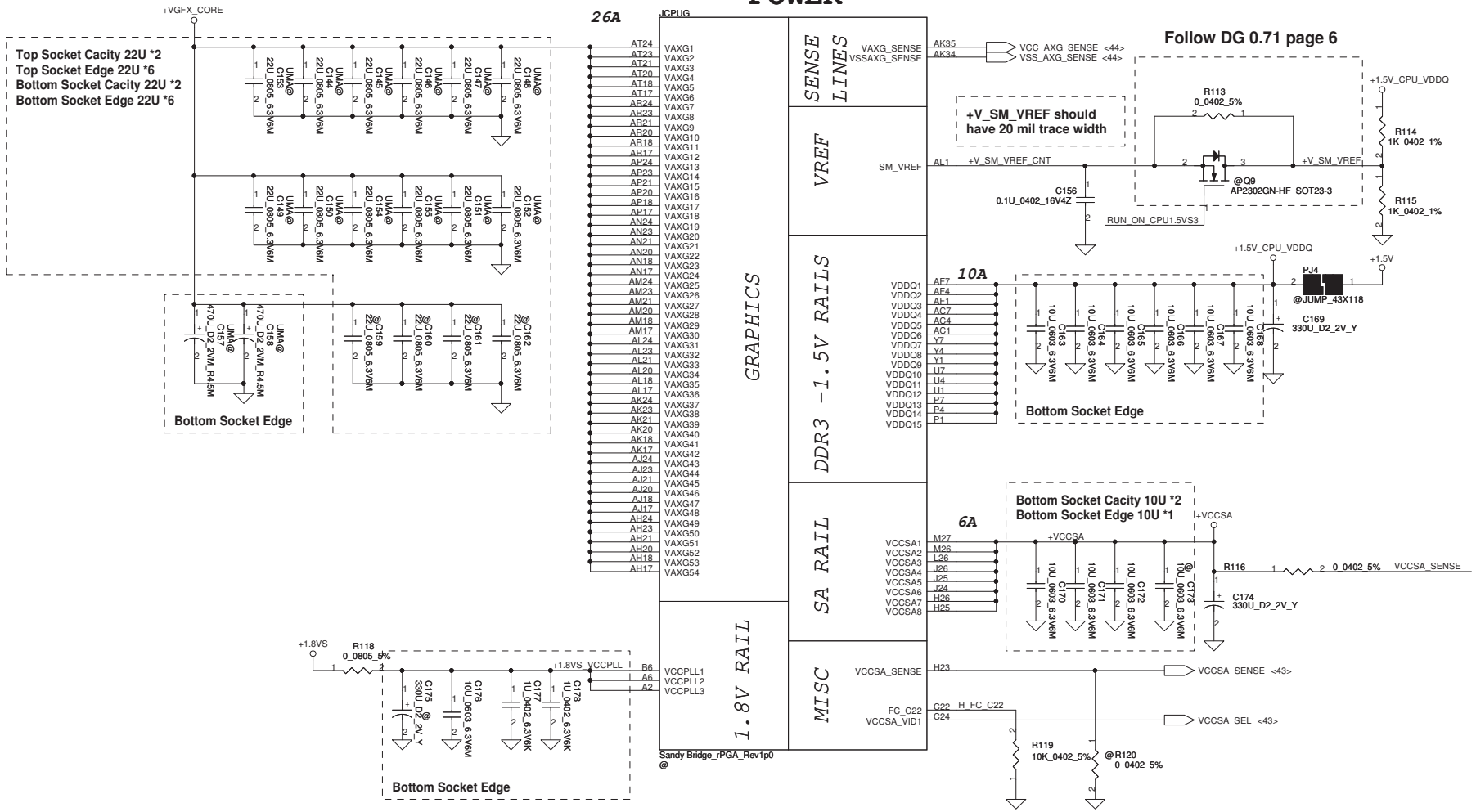
+1.5V_CPU_VDDQ Source



POWER



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Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.			
Title	PROCESSOR(5/7) PWR		
Size	Document Number		Rev
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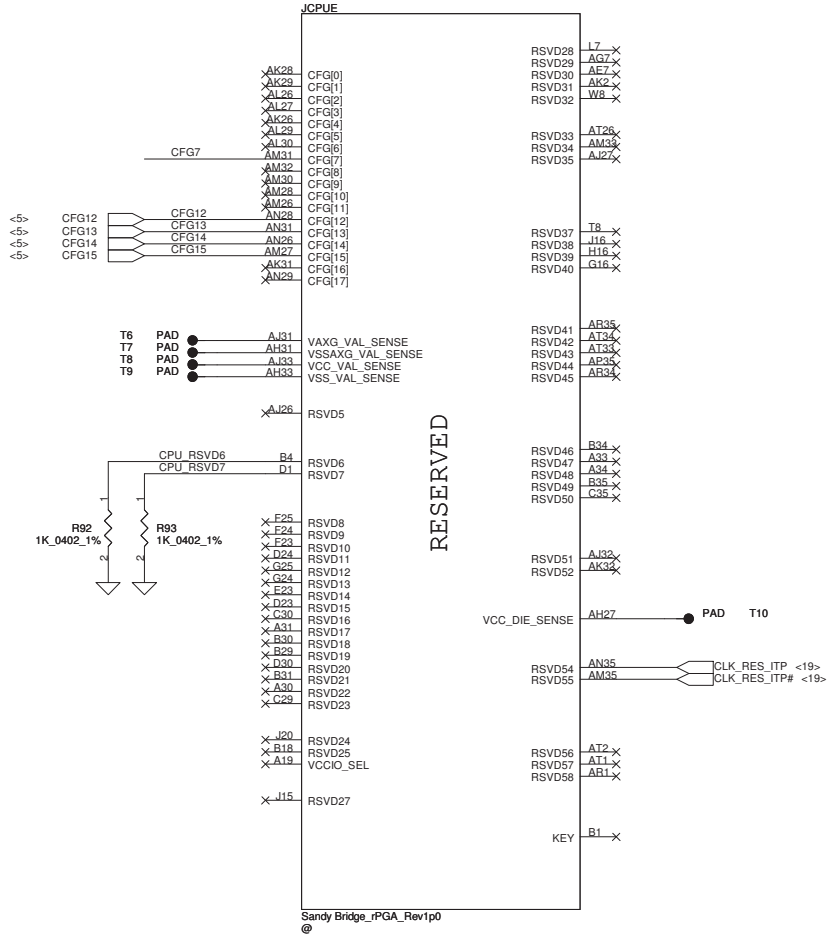


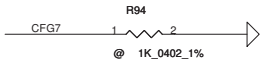
CFG Straps for Processor

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



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Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.			
Title: PROCESSOR(6/7) RSVD,CFG			
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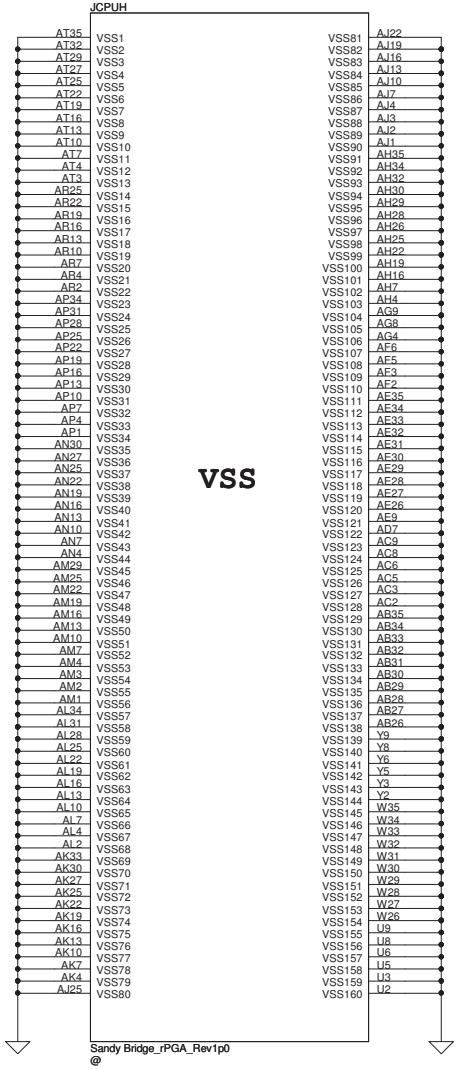

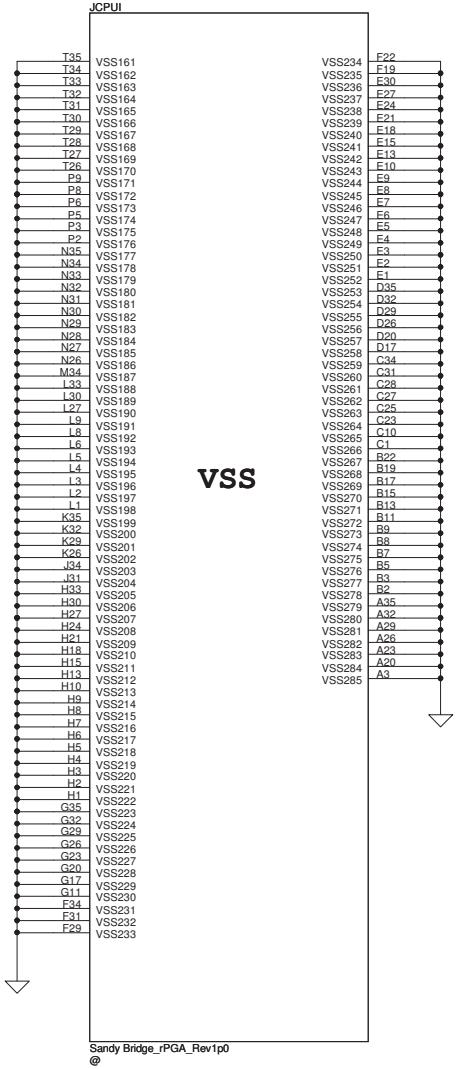

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Issued Date	2010/05/17	Deciphered Date	2011/05/17

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Title: PROCESSOR(7/7) VSS

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+1.5V
R122 1K_0402_1%
+V_DDR_REF
R123 1K_0402_1%

+V_DDR_REF
C179 2.2U_0603_6.3V6K
C180 0.1U_0402_16V4Z

All VREF traces should have 10 mil trace width

JDDRL

	VREF_DQ	VSS1	DDR_A_D4
DDR_A_D0	VSS2	DQ4	DDR_A_D5
DDR_A_D1	DQ0	DQ5	
	DQ1	VSS3	DDR_A_DQS#0
	VSS4	DQS#0	DDR_A_DQS0
	DM0	DQS0	
	VSS5	VSS6	DDR_A_D6
DDR_A_D2	DQ2	DQ6	DDR_A_D7
DDR_A_D3	DQ3	DQ7	
	VSS7	VSS8	
DDR_A_D8	DQ8	DQ12	DDR_A_D12
DDR_A_D9	DQ9	DQ13	DDR_A_D13
	VSS9	VSS10	
DDR_A_DQS#1	DQS#1	DM1	
DDR_A_DQS1	DQS1	RESET#	DDR3_DRAMRST# → DDR3_DRAMRST# <7,13>
	VSS11	VSS12	
DDR_A_D10	DQ10	DQ14	DDR_A_D14
DDR_A_D11	DQ11	DQ15	DDR_A_D15
	VSS13	VSS14	
DDR_A_D16	DQ16	DQ20	DDR_A_D20
DDR_A_D17	DQ17	DQ21	DDR_A_D21
	VSS15	VSS16	
DDR_A_DQS#2	DQS#2	DM2	
DDR_A_DQS2	DQS2	VSS17	
	VSS18	DQ22	DDR_A_D22
DDR_A_D18	DQ18	DQ23	DDR_A_D23
DDR_A_D19	DQ19	VSS19	
	VSS20	DQ28	DDR_A_D28
DDR_A_D24	DQ24	DQ29	DDR_A_D29
DDR_A_D25	DQ25	VSS21	
	VSS22	DQS3	DDR_A_DQS#3
	DM3	DQS3	DDR_A_DQS3
	VSS23	VSS24	
DDR_A_D26	DQ26	DQ30	DDR_A_D30
DDR_A_D27	DQ27	DQ31	DDR_A_D31
	VSS25	VSS26	
<7> DDR_CKE0_DIMMA	CKE0	CKE1	DDR_CKE1_DIMMA → DDR_CKE1_DIMMA <7>
	VDD1	VDD2	DDR_A_MA15
<7> DDR_A_BS2	NC1	A15	DDR_A_MA14
DDR_A_BS2	BA2	A14	
	VDD3	VDD4	DDR_A_MA11
DDR_A_MA12	A12/BC#	A11	DDR_A_MA7
DDR_A_MA9	A9	A7	
	VDD5	VDD6	DDR_A_MA6
DDR_A_MA8	A8	A6	DDR_A_MA4
DDR_A_MA5	A5	A4	
	VDD7	VDD8	DDR_A_MA2
DDR_A_MA3	A3	A2	DDR_A_MA0
DDR_A_MA1	A1	A0	
	VDD9	VDD10	
<7> M_CLK_DDR0 M_CLK_DDR#0	CK0	CK1	M_CLK_DDR1 → M_CLK_DDR1 <7> M_CLK_DDR#1 <7>
M_CLK_DDR0	CK0#	CK1#	M_CLK_DDR#1
	VDD11	VDD12	
DDR_A_MA10	A10/AP	BA1	DDR_A_BS1 → DDR_A_BS1 <7>
DDR_A_BS0	BA0	RAS#	DDR_A_RAS# → DDR_A_RAS# <7>
<7> DDR_A_BS0	VDD13	VDD14	
<7> DDR_A_WE# DDR_A_WE#	WE#	S0#	DDR_CS0_DIMMA# → DDR_CS0_DIMMA# <7>
<7> DDR_A_CAS# DDR_A_CAS#	CAS#	ODT0	M_ODT0 → M_ODT0 <7>
	VDD15	VDD16	
DDR_A_MA13	A13	ODT1	M_ODT1 → M_ODT1 <7>
<7> DDR_CS1_DIMMA# DDR_CS1_DIMMA#	S1#	NC2	
	VDD17	VDD18	
	NCTEST	VREF_CA	+VREF_CA
	VSS27	VSS28	
DDR_A_D32	DQ32	DQ36	DDR_A_D36
DDR_A_D33	DQ33	DQ37	DDR_A_D37
	VSS29	VSS30	
DDR_A_DQS#4	DQS#4	DM4	
DDR_A_DQS4	DQS4	VSS31	
	VSS32	DQ38	DDR_A_D38
DDR_A_D34	DQ34	DQ39	DDR_A_D39
DDR_A_D35	DQ35	VSS33	
	VSS34	DQ44	DDR_A_D44
DDR_A_D40	DQ40	DQ45	DDR_A_D45
DDR_A_D41	DQ41	VSS35	
	VSS36	DQS5	DDR_A_DQS#5
	DM5	DQS5	DDR_A_DQS5
	VSS37	VSS38	
DDR_A_D42	DQ42	DQ46	DDR_A_D46
DDR_A_D43	DQ43	DQ47	DDR_A_D47
	VSS39	VSS40	
DDR_A_D48	DQ48	DQ52	DDR_A_D52
DDR_A_D49	DQ49	DQ53	DDR_A_D53
	VSS41	VSS42	
DDR_A_DQS#6	DQS#6	DM6	
DDR_A_DQS6	DQS6	VSS43	
	VSS44	DQ54	DDR_A_D54
DDR_A_D50	DQ50	DQ55	DDR_A_D55
DDR_A_D51	DQ51	VSS45	
	VSS46	DQ60	DDR_A_D60
DDR_A_D56	DQ56	DQ61	DDR_A_D61
DDR_A_D57	DQ57	VSS47	
	VSS48	DQS7	DDR_A_DQS#7
	DM7	DQS7	DDR_A_DQS7
	VSS49	VSS50	
DDR_A_D58	DQ58	DQ62	DDR_A_D62
DDR_A_D59	DQ59	DQ63	DDR_A_D63
	VSS51	VSS52	
	SA0	EVENT#	
	VDDSPD	SDA	D_CK_SDATA → D_CK_SDATA <13,14,29>
	SA1	SCL	D_CK_SCLK → D_CK_SCLK <13,14,29>
	VTT1	VTT2	+0.75VS
	G1	G2	

LCN_DAN06-K4526-0100
@

+1.5V
R124 1K_0402_1%
R125 1K_0402_1%
C193 2.2U_0603_6.3V6K
C194 0.1U_0402_16V4Z

+3VS
+0.75VS
C199 0.1U_0402_16V4Z
C200 2.2U_0603_6.3V6K
R134 10K_0402_5%
R135 10K_0402_5%

+3VS
R1 4.7K_0402_5%
<19> PCH_SMBDATA
D_CK_SDATA
Q1 2N7002E-T1-GE3_SOT23-3

+3VS
R4 4.7K_0402_5%
<19> PCH_SMBCLK
D_CK_SCLK
Q2 2N7002E-T1-GE3_SOT23-3

DDR_A_DQS#[0..7] <7>
DDR_A_DQS[0..7] <7>
DDR_A_D[0..63] <7>
DDR_A_MA[0..15] <7>

Layout Note:
Place near JDIMM1

+1.5V
C181 1U_0402_6.3V6K
C182 1U_0402_6.3V6K
C183 1U_0402_6.3V6K
C184 1U_0402_6.3V6K

+1.5V
C185 10U_0603_6.3V6M
C186 10U_0603_6.3V6M
C187 10U_0603_6.3V6M
C188 10U_0603_6.3V6M
C189 10U_0603_6.3V6M
C190 10U_0603_6.3V6M
C191 10U_0603_6.3V6M
C192 330U_D2_2V_Y

Layout Note:
Place near JDIMM1.203,204

+0.75VS
C195 1U_0402_6.3V6K
C196 1U_0402_6.3V6K
C197 1U_0402_6.3V6K
C198 1U_0402_6.3V6K

For EMI

+3VS
C234 0.1U_0402_16V4Z
C235 0.1U_0402_16V4Z
C236 0.1U_0402_16V4Z
C237 0.1U_0402_16V4Z

+0.75VS
C238 0.1U_0402_16V4Z

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: DDRIII DIMMA

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All VREF traces should have 10 mil trace width

+V_DDR_REF

C201 2.2U_0603_6.3V6K

C202 0.1U_0402_16V4Z

JDDRIII

DDR_B_D0 DDR_B_D1 DDR_B_D2 DDR_B_D3 DDR_B_D8 DDR_B_D9 DDR_B_DQS#1 DDR_B_DQS1 DDR_B_D10 DDR_B_D11 DDR_B_D16 DDR_B_D17 DDR_B_DQS#2 DDR_B_DQS2 DDR_B_D18 DDR_B_D19 DDR_B_D24 DDR_B_D25 DDR_B_D26 DDR_B_D27 DDR_B_D32 DDR_B_D33 DDR_B_DQS#4 DDR_B_DQS4 DDR_B_D34 DDR_B_D35 DDR_B_D40 DDR_B_D41 DDR_B_D42 DDR_B_D43 DDR_B_D48 DDR_B_D49 DDR_B_DQS#6 DDR_B_DQS6 DDR_B_D50 DDR_B_D51 DDR_B_D56 DDR_B_D57 DDR_B_D58 DDR_B_D59

DDR_B_D4 DDR_B_D5 DDR_B_DQS#0 DDR_B_DQS0 DDR_B_D6 DDR_B_D7 DDR_B_D12 DDR_B_D13 DDR3_DRAMRST# DDR_B_D14 DDR_B_D15 DDR_B_D20 DDR_B_D21 DDR_B_D22 DDR_B_D23 DDR_B_D28 DDR_B_D29 DDR_B_DQS#3 DDR_B_DQS3 DDR_B_D30 DDR_B_D31 DDR_B_D36 DDR_B_D37 DDR_B_D38 DDR_B_D39 DDR_B_D44 DDR_B_D45 DDR_B_DQS#5 DDR_B_DQS5 DDR_B_D46 DDR_B_D47 DDR_B_D52 DDR_B_D53 DDR_B_D54 DDR_B_D55 DDR_B_D60 DDR_B_D61 DDR_B_DQS#7 DDR_B_DQS7 DDR_B_D62 DDR_B_D63

<7> DDR_CKE2_DIMMB — DDR_CKE2_DIMMB — DDR_CKE3_DIMMB — DDR_CKE3_DIMMB <7>

<7> DDR_B_BS2 — DDR_B_BS2

DDR_B_MA12 DDR_B_MA9 DDR_B_MA8 DDR_B_MA5 DDR_B_MA3 DDR_B_MA1

<7> M_CLK_DDR2 — M_CLK_DDR2
<7> M_CLK_DDR#2 — M_CLK_DDR#2

DDR_B_MA10 DDR_B_BS0

<7> DDR_B_BS0

<7> DDR_B_WE#
<7> DDR_B_CAS#

DDR_B_WE# DDR_B_CAS#

DDR_B_MA13 DDR_CS3_DIMMB#

<7> DDR_CS3_DIMMB#

DDR_B_MA15 DDR_B_MA14 DDR_B_MA11 DDR_B_MA7 DDR_B_MA6 DDR_B_MA4 DDR_B_MA2 DDR_B_MA0

M_CLK_DDR3 <7>
M_CLK_DDR#3 <7>

DDR_B_BS1 <7>
DDR_B_RAS# <7>

DDR_CS2_DIMMB# <7>
M_ODT2 <7>

M_ODT3 <7>

+VREF_CA

C219 2.2U_0603_6.3V6K

C220 0.1U_0402_16V4Z

+3VS

R149 10K_0402_5%

C221 0.1U_0402_16V4Z

C222 2.2U_0603_6.3V6K

+0.75VS

R150 10K_0402_5%

D_CK_SDATA <12,14,29>
D_CK_SCLK <12,14,29>

LCN_DAN06-K4926-0100
@

DDR_B_DQS#[0..7] <7>
DDR_B_DQS[0..7] <7>
DDR_B_D[0..63] <7>
DDR_B_MA[0..15] <7>

+1.5V

C203 1U_0402_6.3V6K
C204 1U_0402_6.3V6K
C205 1U_0402_6.3V6K
C206 1U_0402_6.3V6K

Layout Note:
Place near JDIMMB

C207 10U_0603_6.3V6M
C208 10U_0603_6.3V6M
C209 10U_0603_6.3V6M
C210 10U_0603_6.3V6M
C211 10U_0603_6.3V6M
C212 10U_0603_6.3V6M
C213 10U_0603_6.3V6M
C214 330U_D2_2V_Y @

Layout Note:
Place near JDIMMB.203,204

+0.75VS

C215 1U_0402_6.3V6K
C216 1U_0402_6.3V6K
C217 1U_0402_6.3V6K
C218 1U_0402_6.3V6K

Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.

Title: DDRIII DIMMB

Size: Custom | Document Number: PBL20 LA6772P M/B | Rev: 1.0

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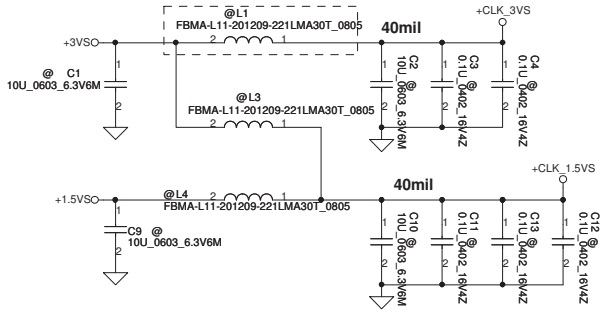
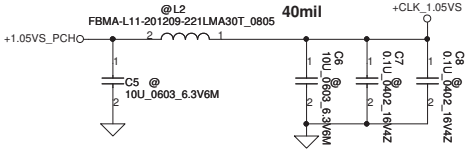
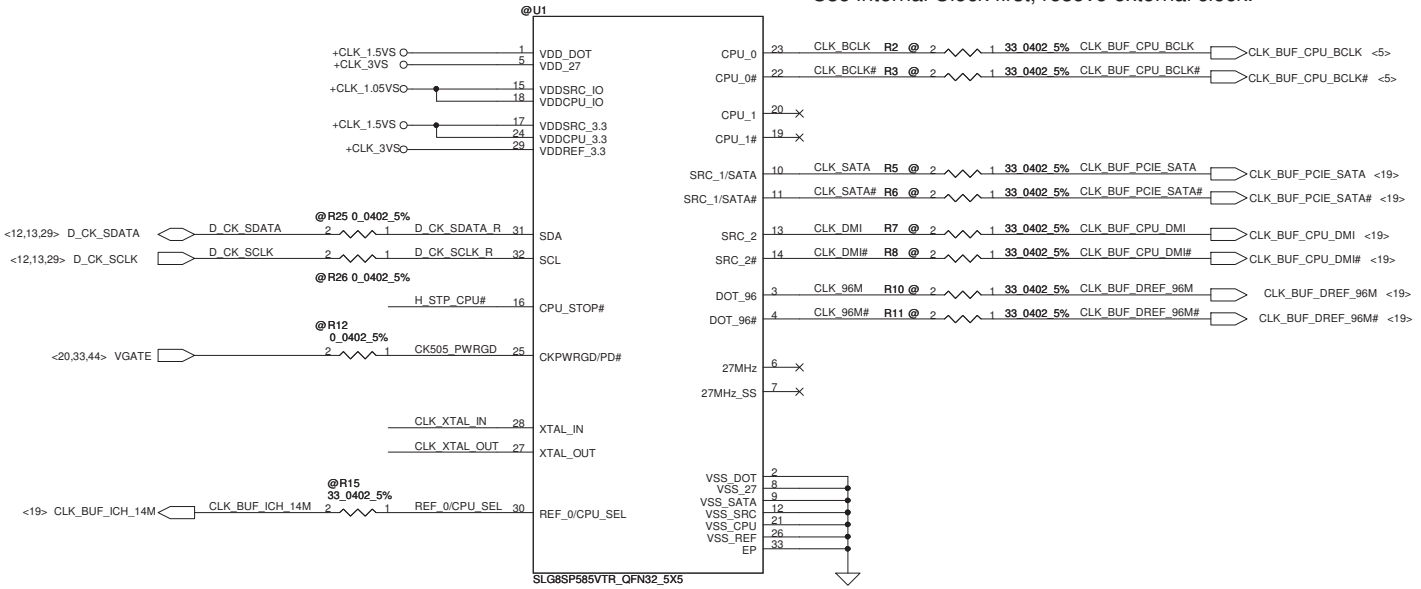
SM010014520 3000ma 220ohm@100mhz DCR 0.04



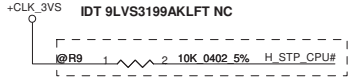


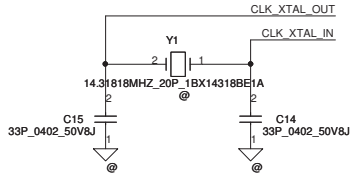
Use internal Clock first, reseve external clock.



Standard
IDT: 9LRS3199AKLFT, SA000030P00
SILEGO: SLG8SP587V(WF), SA00002XY10

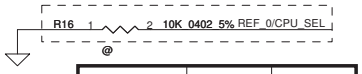
Silego Have Internal Pull-Up
IDT 9LVS3199AKLFT NC





IDT Have Internal Pull-Down

FOR Realtek



PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.

Title: Clock Generator (CK505)

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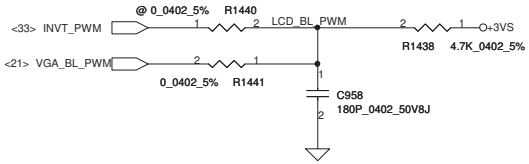
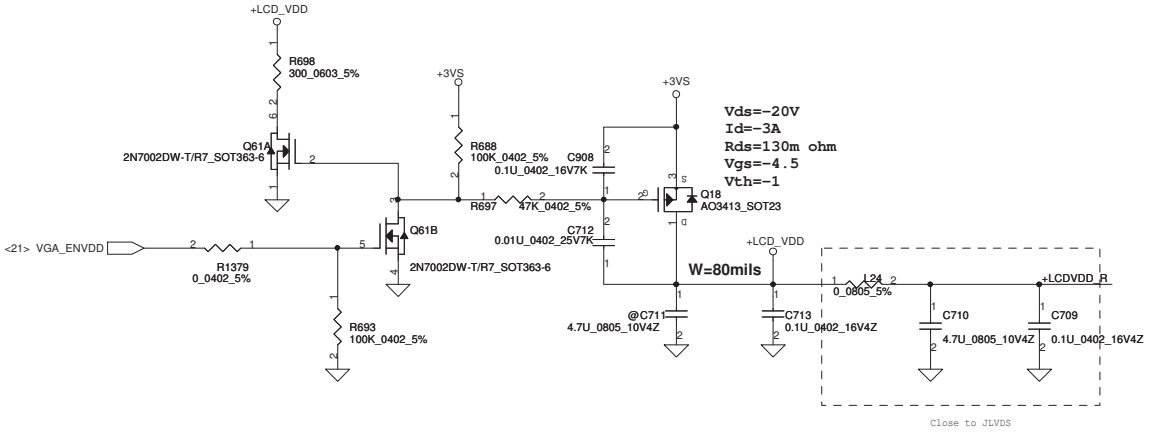
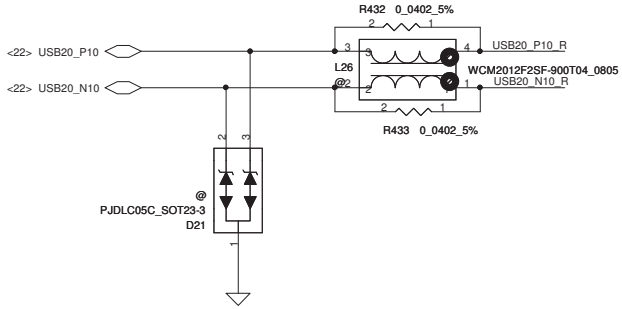
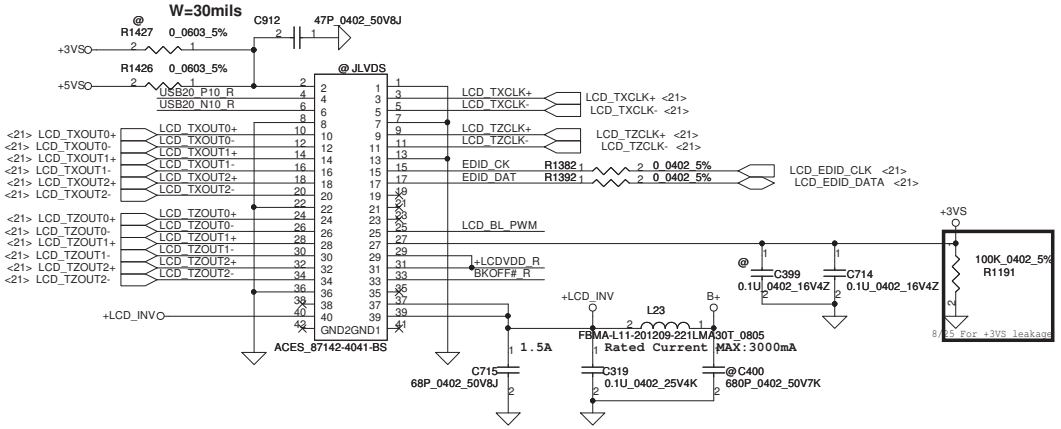
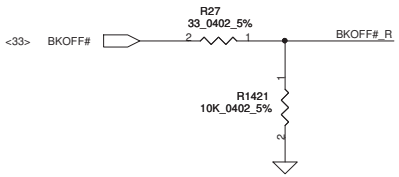




LCD/PANEL BD. Conn.







Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.

Title: LVDS Connector

Size: Custom | Document Number: PBL20 LA6772P M/B | Rev: 1.0

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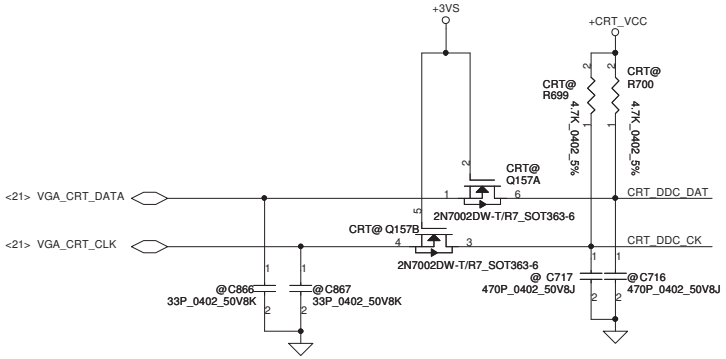

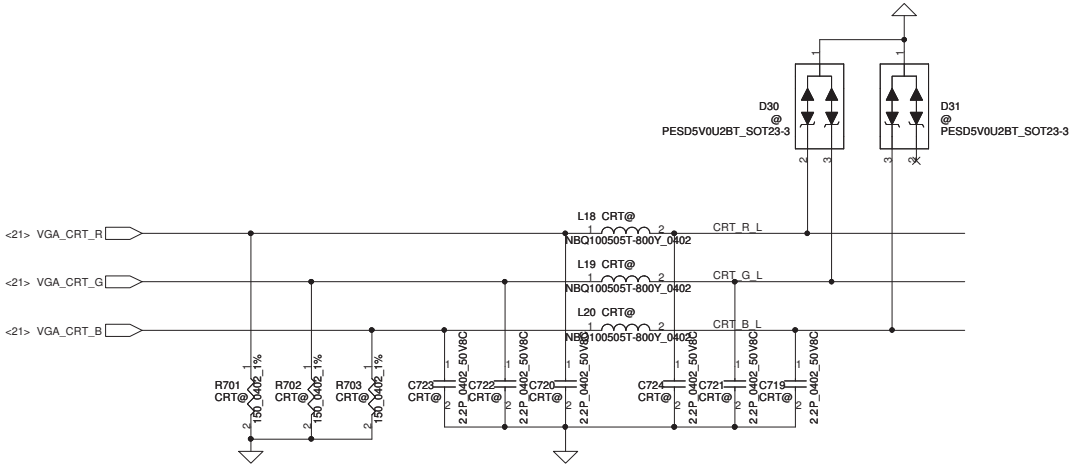

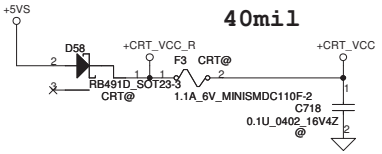

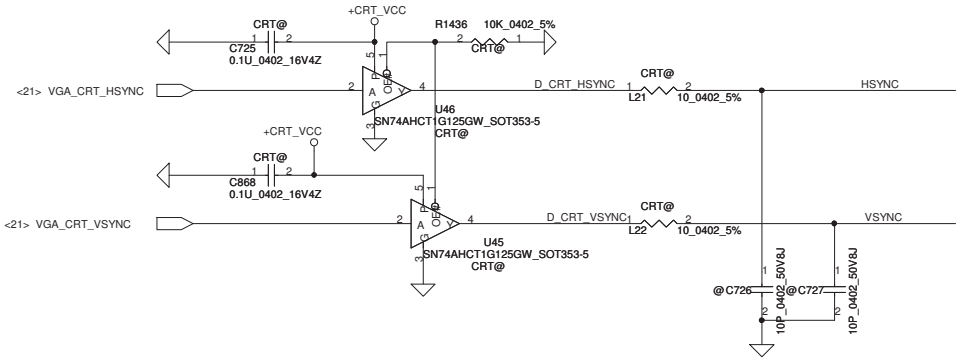

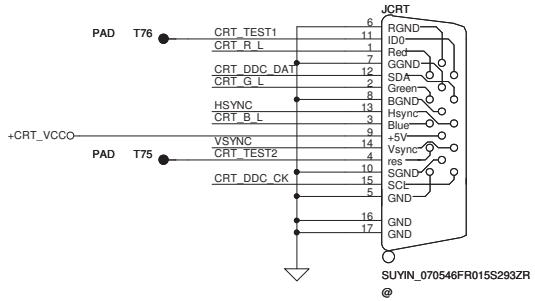

Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.

Title: CRT Connector

Size	Document Number	Rev
Custom	PBL20 LA6772P M/B	1.0

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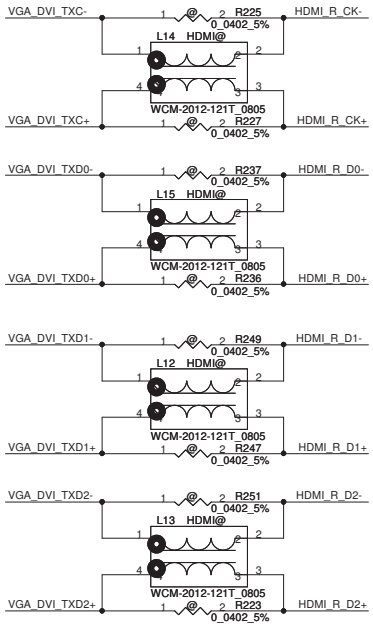
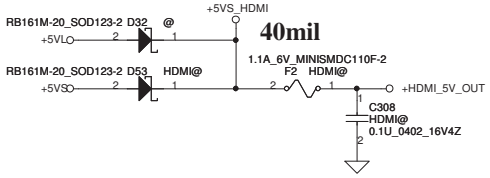
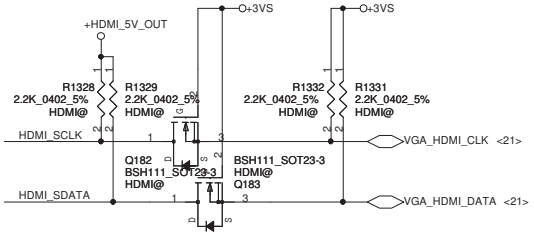
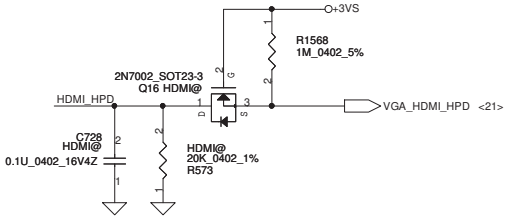
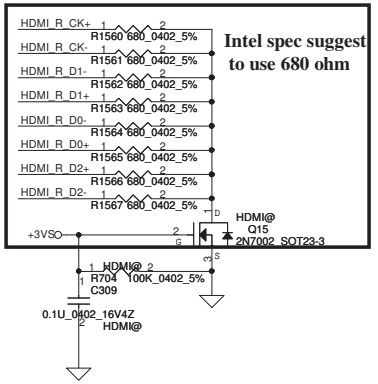
For EMI
Change 90 ohm
P/N:SM070000K00

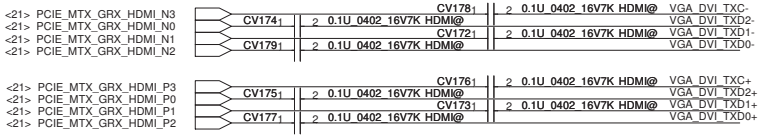




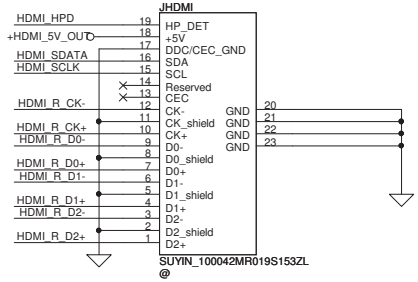








HDMI Connector



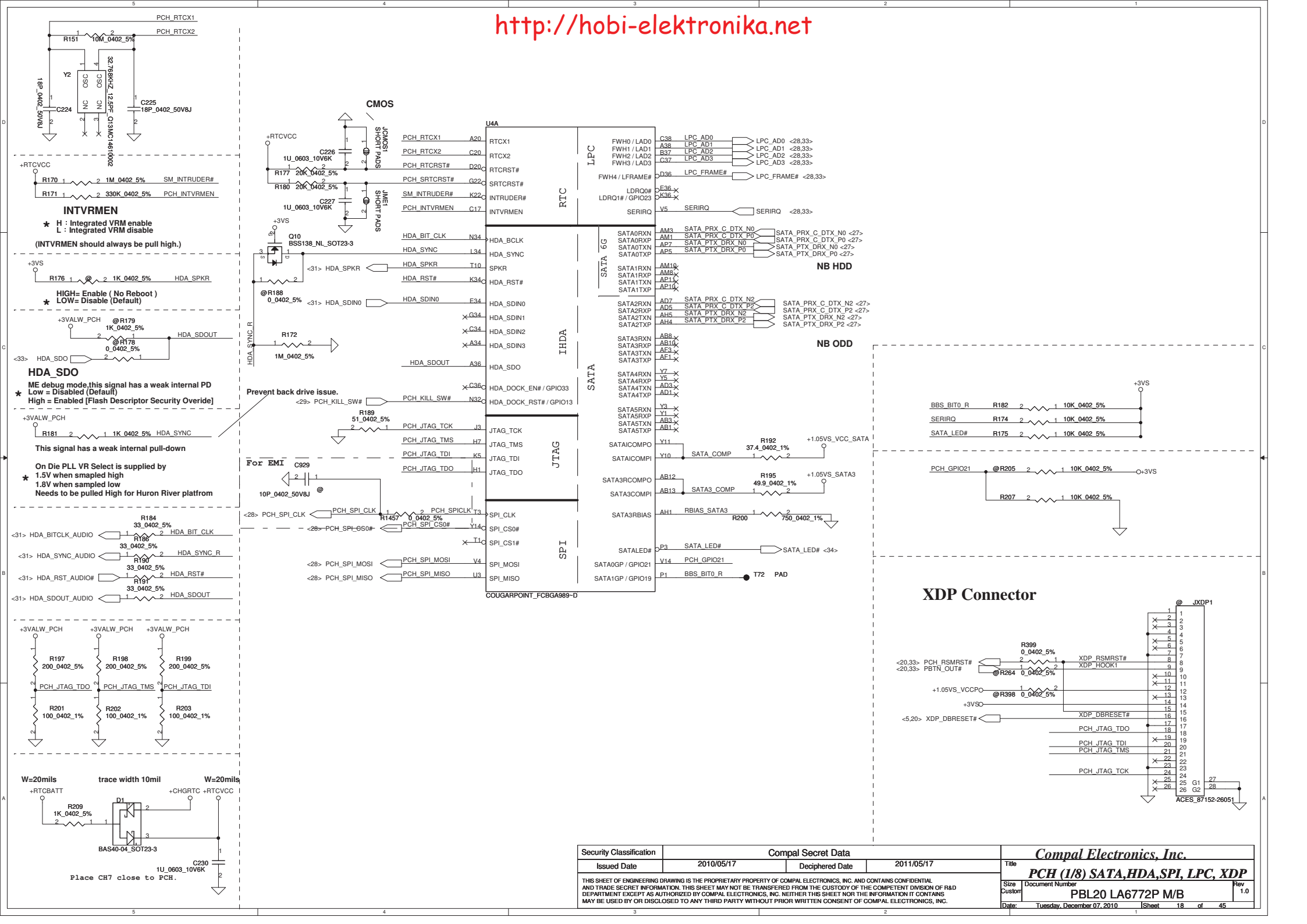
Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.

Title: HDMI Level Shift & Conn

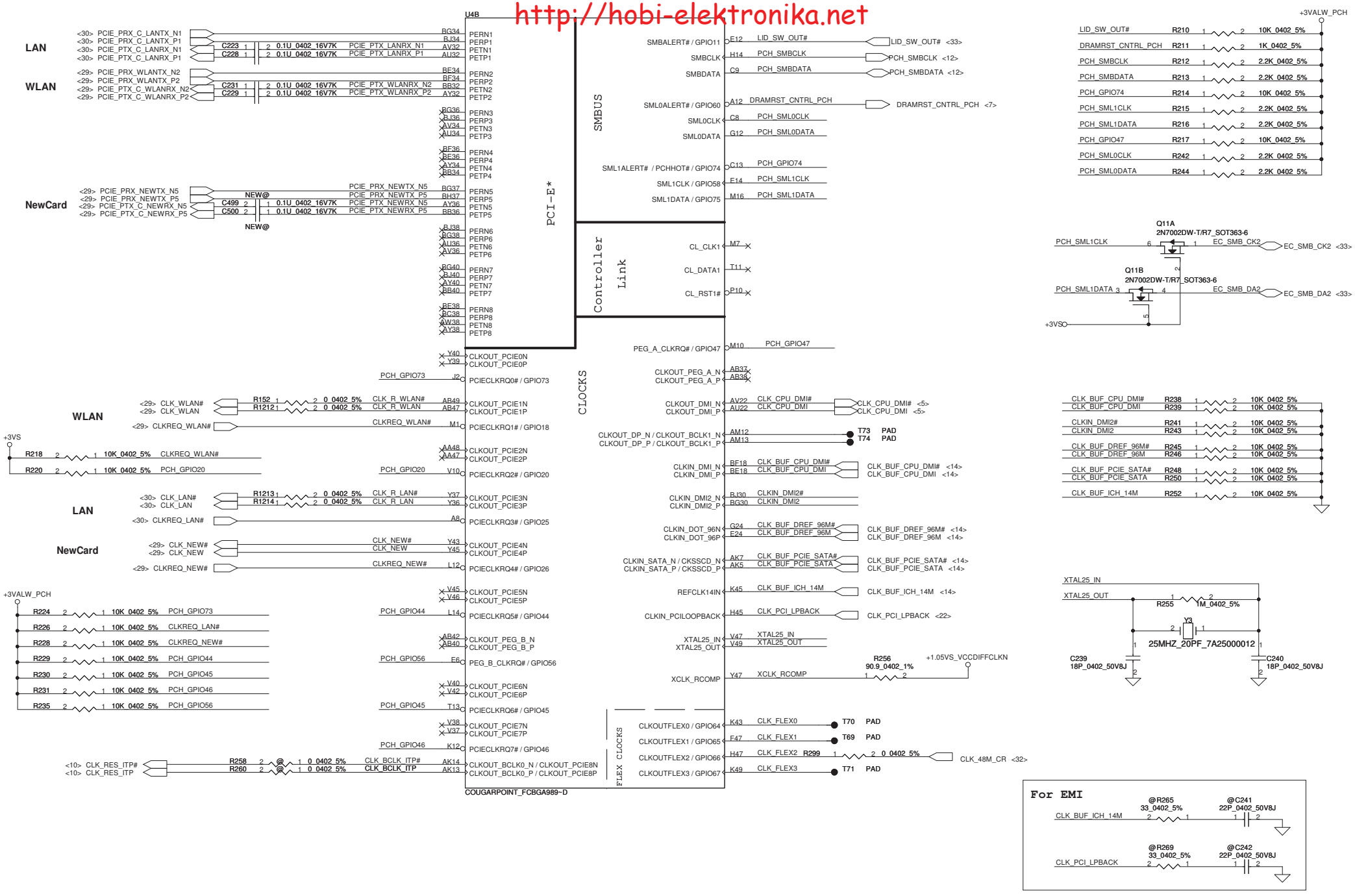
Size	Document Number	Rev
Custom	PBL20 LA6772P M/B	1.0

Date: Tuesday, December 07, 2010 Sheet 17 of 45



Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.			
Title: PCH (1/8) SATA,HDA,SPI, LPC, XDP			
Size: Custom	Document Number: PBL20 LA6772P M/B		Rev: 1.0
Date: Tuesday, December 07, 2010	Sheet 18 of 45		

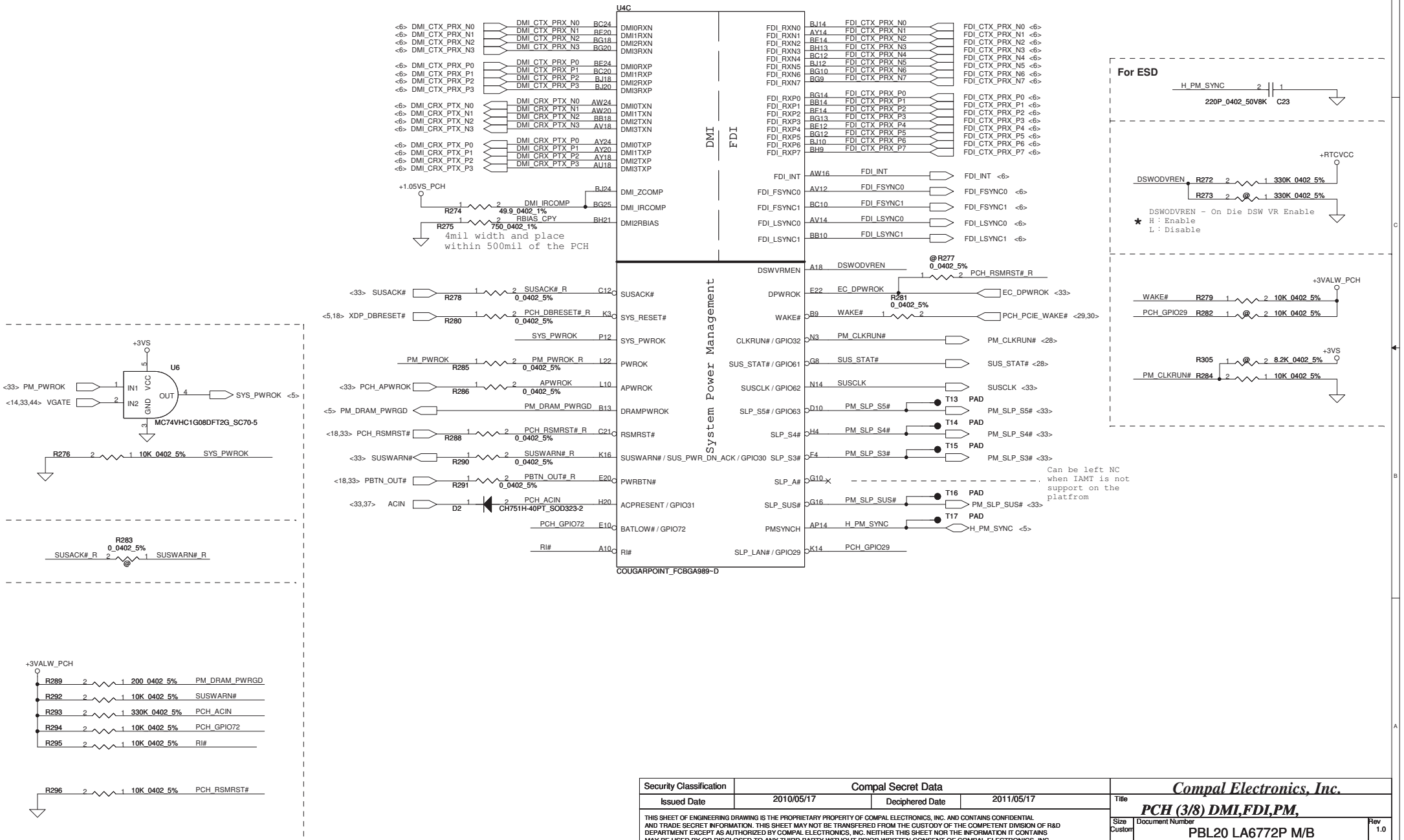


Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

Title: *PCH (2/8) PCIE, SMBUS, CLK*

Size: Custom | Document Number: PBL20 LA6772P M/B | Rev: 1.0

Date: Tuesday, December 07, 2010 | Sheet 19 of 45



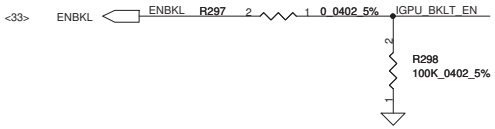
Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

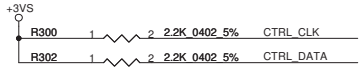
Compal Electronics, Inc.

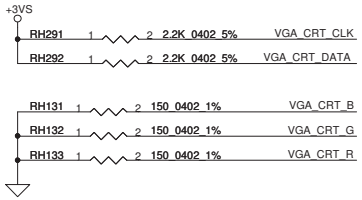
Title: PCH (3/8) DMI,FDI,PM,

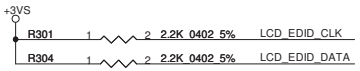
Size	Document Number	Rev
Custom	PBL20 LA6772P M/B	1.0

Date: Tuesday, December 07, 2010 Sheet 20 of 45

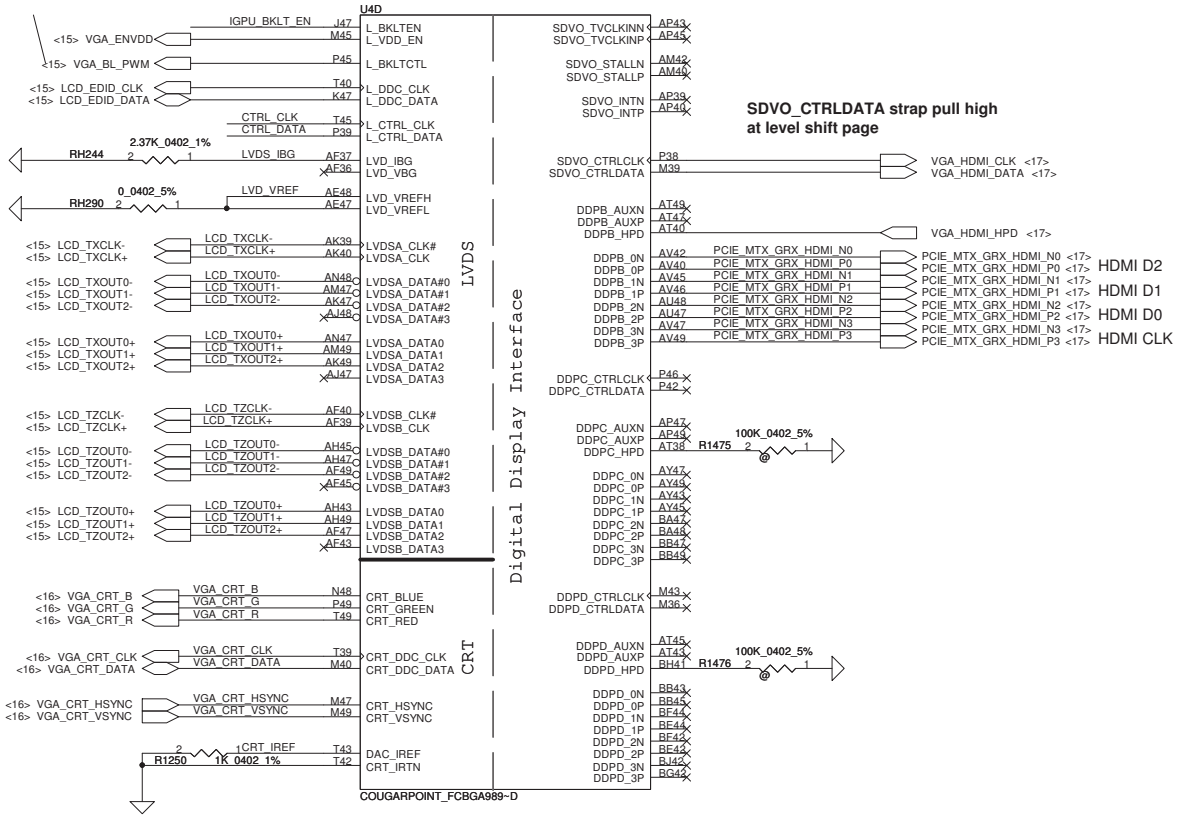








Pull high at LVDS conn side.



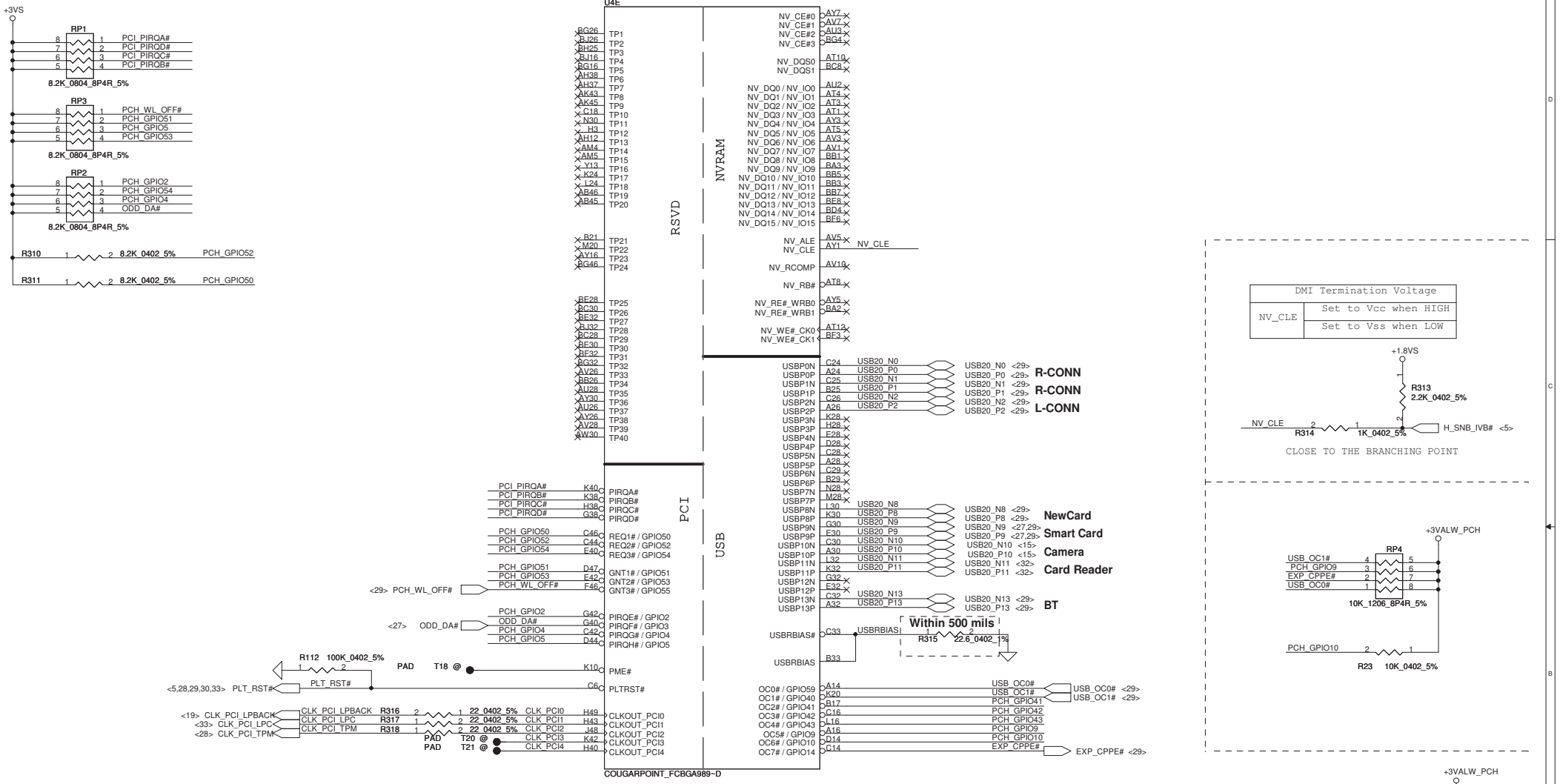
Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.

Title: *PCH (4/9) LVDS,CRT,DP,HDMI*

Size	Document Number	Rev
Custom	PBL20 LA6772P M/B	1.0

Date: Tuesday, December 07, 2010 Sheet 21 of 45



Boot BIOS Strap bit1 BBS1			
	Bit11	Bit10	Boot BIOS Destination
BBS bit1 /BBS bit0	0	1	Reserved
	1	0	PCI
	1	1	SPI ★
	0	0	LPC

	GPIO43	GPIO42	GPIO41
PBL00	0	0	0
PBL01	0	0	1
PBL10	0	1	0
PBL11	0	1	1
PBL20	1	0	0
PBL21	1	0	1

Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, NVRAM

Size: Custom | Document Number: PBL20 LA6772P M/B | Rev: 1.0

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+3VALW_PCH
R352 1 2 10K_0402_5%
R327 1 @ 2 1K_0402_5% EC_SMI#

Reserve for ICC enable.

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

+3VALW_PCH
R351 1 2 10K_0402_5%
R325 1 @ 2 1K_0402_5% PCH_GPIO28

PCH_GPIO27 (Have internal Pull-High)
*High: VCCVRM VR Enable
Low: VCCVRM VR Disable

R328 1 @ 2 10K_0402_5% PCH_GPIO27

PCH_GPIO37

+3VS
R426 1 @ 2 10K_0402_5% PCH_GPIO37
R332 1 2 10K_0402_5%

+3VS
R425 1 2 10K_0402_5% PCH_GPIO24
R424 1 2 10K_0402_5% PCH_GPIO0
R335 1 2 10K_0402_5% PCH_GPIO1
R336 1 2 10K_0402_5% PCH_GPIO6
R337 1 2 10K_0402_5% PCH_GPIO16
R338 1 2 10K_0402_5% PCH_GPIO17
R339 1 2 10K_0402_5% PCH_GPIO22
R340 1 2 10K_0402_5% PCH_GPIO38
R341 1 2 10K_0402_5% PCH_GPIO39
R342 1 2 10K_0402_5% ODD_DETECT#
R343 1 2 10K_0402_5% PCH_BT_PWRON
R344 1 2 10K_0402_5% PCH_GPIO48
R345 1 2 10K_0402_5% PCH_GPIO49

+3VALW_PCH
R346 1 2 10K_0402_5% PCH_GPIO12
R347 1 2 1K_0402_5% PCH_GPIO15
R349 1 2 10K_0402_5% PCH_GPIO57

R350 1 @ 2 10K_0402_5% PCH_GPIO35

H_CPUPWRGD 2 1
220P_0402_50V8K C19
For ESD

+3VS
KB_RST# R326 1 2 10K_0402_5%

U4F

PCH_GPIO0	T7	BMBUSY# / GPIO0		TACH4 / GPIO68	C40
PCH_GPIO1	A42	TACH1 / GPIO1		TACH5 / GPIO69	B41
PCH_GPIO6	H36	TACH2 / GPIO6		TACH6 / GPIO70	C41
<33> EC_SCI#	F38	TACH3 / GPIO7		TACH7 / GPIO71	A40
<33> EC_SMI#	C10	GPIO8			
PCH_GPIO12	C4	LAN_PHY_PWR_CTRL / GPIO12			
PCH_GPIO15	G2	GPIO15		A20GATE	P4
PCH_GPIO16	U2	SATA4GP / GPIO16		PECI	AU16
				RCIN#	P5
PCH_GPIO17	D40	TACH0 / GPIO17		PROCPWRGD	AY11
PCH_GPIO22	T5	SCLOCK / GPIO22		THRMTRIP#	AY10
PCH_GPIO24	E8	GPIO24 / MEM_LED		INIT3_3V#	T14
PCH_GPIO27	F16	GPIO27			
PCH_GPIO28	P8	GPIO28			
<29> PCH_BT_PWRON	K1	STP_PCI# / GPIO34		NC_1	AH8
PCH_GPIO35	K4	GPIO35		NC_2	AK11
<27> ODD_DETECT#	V8	SATA2GP / GPIO36		NC_3	AH10
PCH_GPIO37	M5	SATA3GP / GPIO37		NC_4	AK10
PCH_GPIO38	N2	SLOAD / GPIO38		NC_5	P37
PCH_GPIO39	M3	SDATAOUT0 / GPIO39			
PCH_GPIO48	V13	SDATAOUT1 / GPIO48		VSS_NCTF_15	BG2
PCH_GPIO49	V3	SATA5GP / GPIO49		VSS_NCTF_16	BG48
PCH_GPIO57	D6	GPIO57		VSS_NCTF_17	BH3
				VSS_NCTF_18	BH47
PAD T30 @	A4	VSS_NCTF_1		VSS_NCTF_19	BJ4
PAD T32 @	A44	VSS_NCTF_2		VSS_NCTF_20	BJ44
PAD T34 @	A45	VSS_NCTF_3		VSS_NCTF_21	BJ45
PAD T36 @	A46	VSS_NCTF_4		VSS_NCTF_22	BJ46
PAD T38 @	A5	VSS_NCTF_5		VSS_NCTF_23	BJ5
PAD T40 @	A6	VSS_NCTF_6		VSS_NCTF_24	BJ6
PAD T42 @	B3	VSS_NCTF_7		VSS_NCTF_25	C2
PAD T44 @	B47	VSS_NCTF_8		VSS_NCTF_26	C48
PAD T46 @	BD1	VSS_NCTF_9		VSS_NCTF_27	D1
PAD T48 @	BD49	VSS_NCTF_10		VSS_NCTF_28	D49
PAD T50 @	BE1	VSS_NCTF_11		VSS_NCTF_29	E1
PAD T52 @	BE49	VSS_NCTF_12		VSS_NCTF_30	E49
PAD T54 @	BF1	VSS_NCTF_13		VSS_NCTF_31	F1
PAD T56 @	BF49	VSS_NCTF_14		VSS_NCTF_32	F49

GPIO | CPU/MISC | NCTF

COUGARPOINT_FCBGA989~D

10K_0402_5% 2 1 R428 +3VS
ODD_EN# ODD_EN# <27>
B41 PCH_GPIO69 @T24 PAD
C41 PCH_GPIO70 @T25 PAD
A40 PCH_GPIO71 @T22 PAD

+3VS
R329 10K_0402_5%
P4 GATEA20 <33>
AU16 PCH_PECI_R 0_0402_5% R331 H_PECI <5,33>
P5 KB_RST# KB_RST# <33>
AY11 H_CPUPWRGD <5>
AY10 PCH_THRMTRIP#_R R334 390_0402_5% H_THRMTRIP# H_THRMTRIP# <5>

INIT3_3V
This signal has weak internal PU, can't pull low

Intel schematic review recommand.

VSS_NCTF_15	BG2	@T26	PAD		
VSS_NCTF_16	BG48	@T27	PAD		
VSS_NCTF_17	BH3	@T28	PAD		
VSS_NCTF_18	BH47	@T29	PAD		
VSS_NCTF_19	BJ4	@T31	PAD		
VSS_NCTF_20	BJ44	@T33	PAD		
VSS_NCTF_21	BJ45	@T35	PAD		
VSS_NCTF_22	BJ46	@T37	PAD		
VSS_NCTF_23	BJ5	@T39	PAD		
VSS_NCTF_24	BJ6	@T41	PAD		
VSS_NCTF_25	C2	@T43	PAD		
VSS_NCTF_26	C48	@T45	PAD		
VSS_NCTF_27	D1	@T47	PAD		
VSS_NCTF_28	D49	@T49	PAD		
VSS_NCTF_29	E1	@T51	PAD		
VSS_NCTF_30	E49				
VSS_NCTF_31	F1	@T55	PAD		
VSS_NCTF_32	F49				

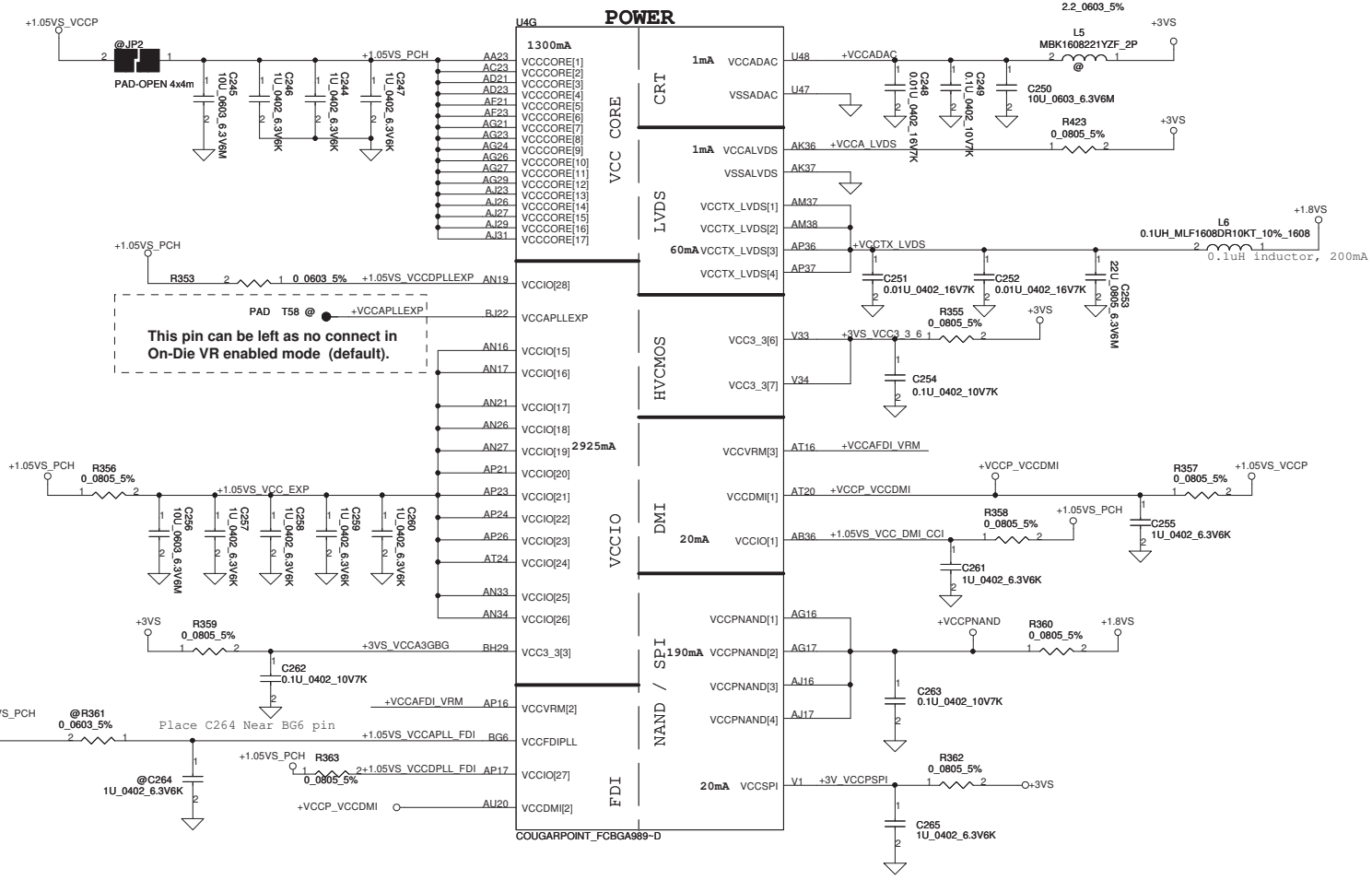
Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

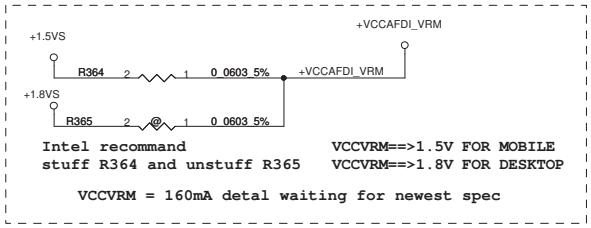
Size	Document Number	Rev
Custom	PBL20 LA6772P M/B	1.0

Date: Tuesday, December 07, 2010 Sheet 23 of 45

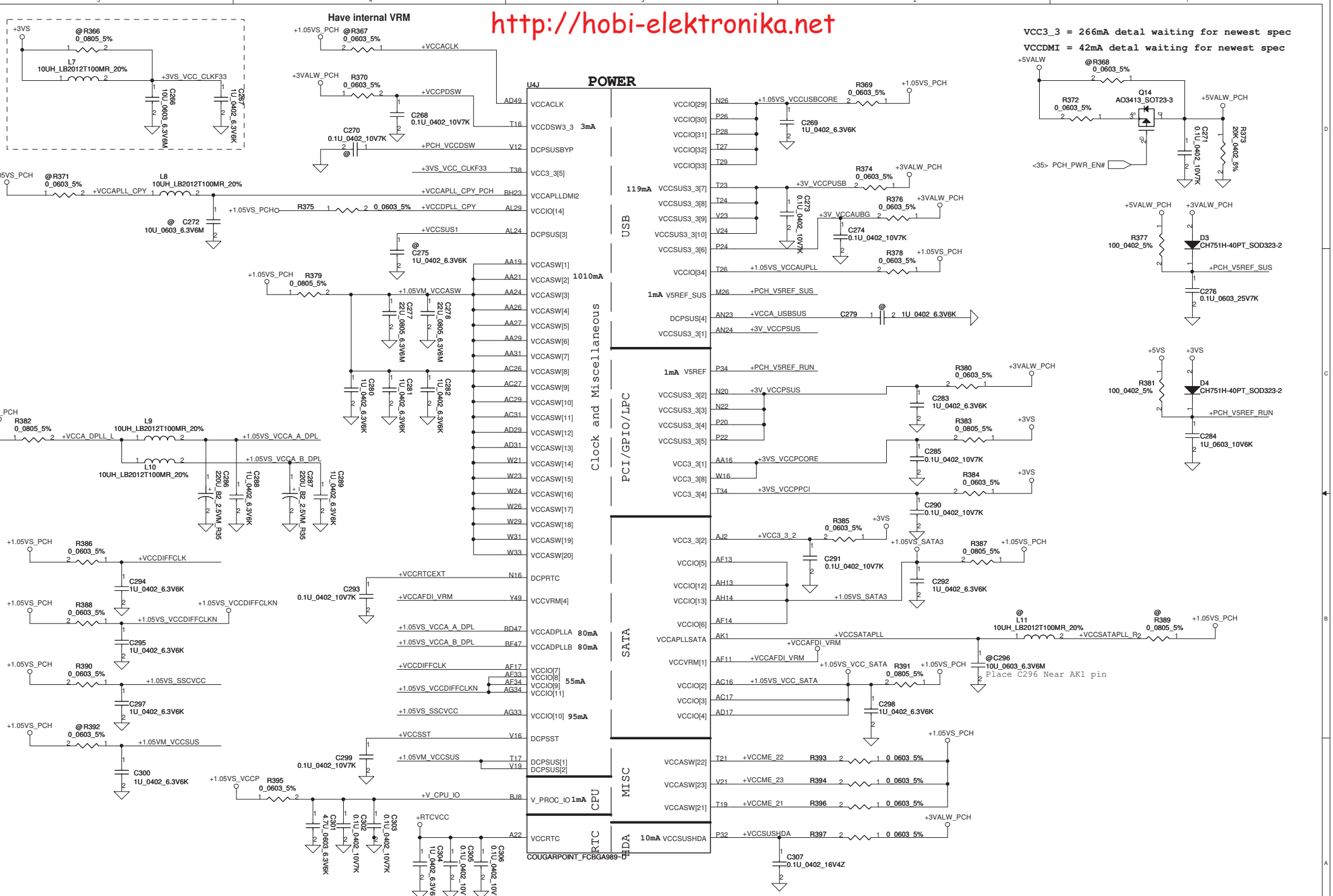


PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

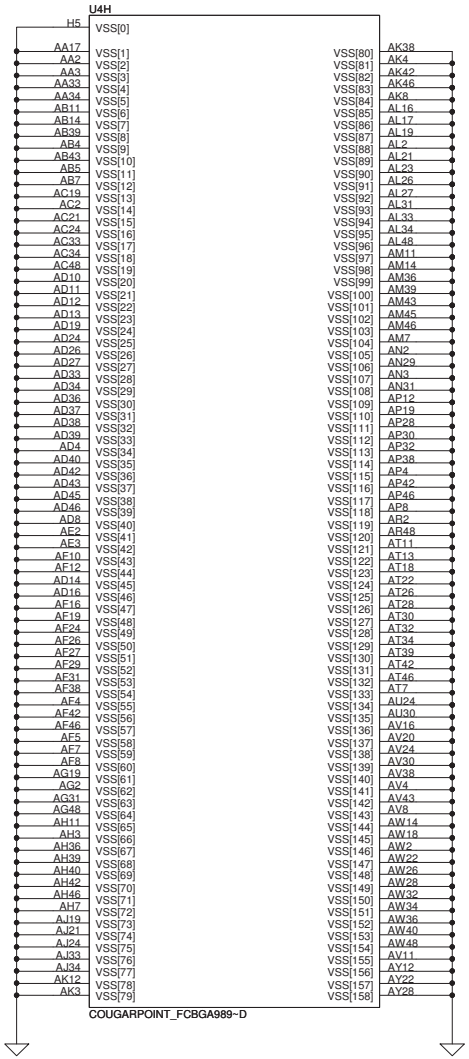


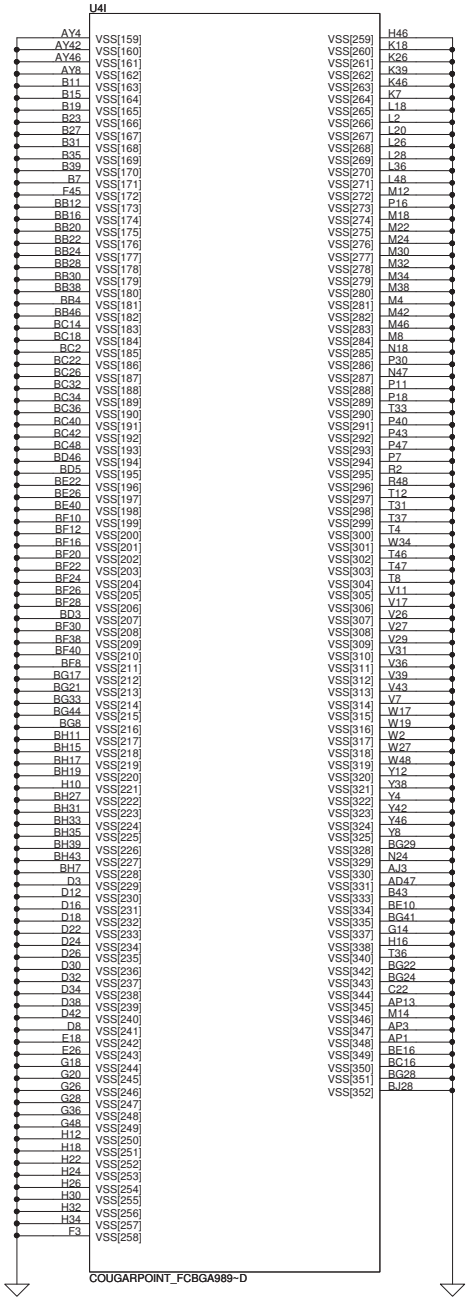
Compal Electronics, Inc.
Title: PCH (7/9) PWR
Size: Custom
Document Number: PBL20 LA6772P M/B
Rev: 1.0
Date: Tuesday, December 07, 2010
Sheet 24 of 45



Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.		
Title	PCH (8/9) PWR	
Size: Custom	Document Number: PBL20 LA6772P M/B	Rev: 1.0
Date: Tuesday, December 07, 2010	Sheet 25 of 45	





Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

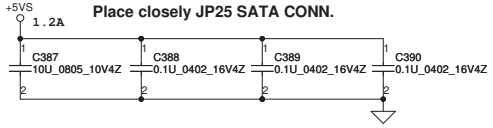
Compal Electronics, Inc.

Title: PCH (9/9) VSS

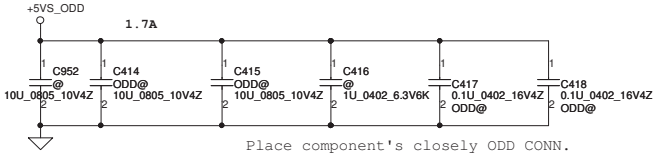
Size	Document Number	Rev
Custom	PBL20 LA6772P M/B	1.0

Date: Tuesday, December 07, 2010 Sheet 26 of 45

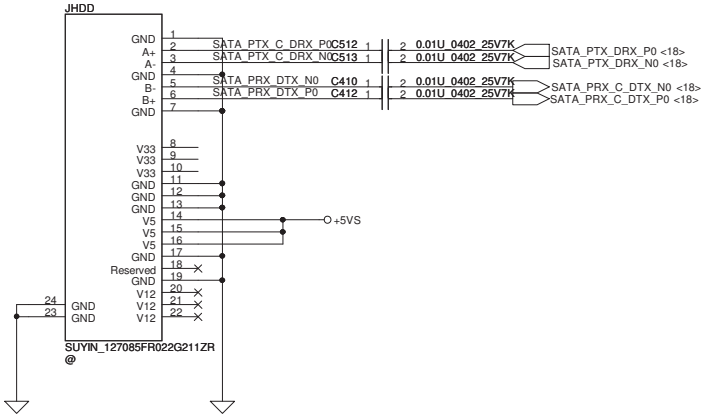
SATA HDD1 Conn.



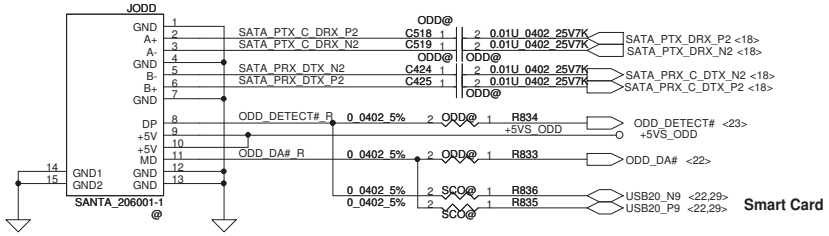
SATA ODD Conn

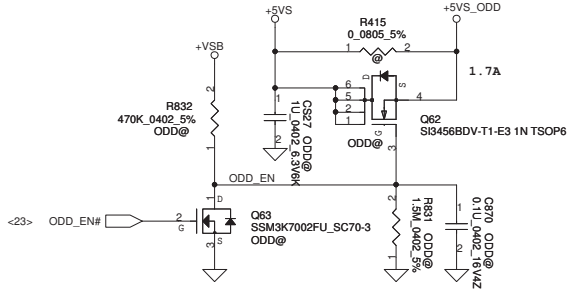


13.3" HDD



13.3" ODD





Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.

Title: HDD & ODD Connector

Size	Document Number	Rev
Custom	PBL20 LA6772P M/B	1.0

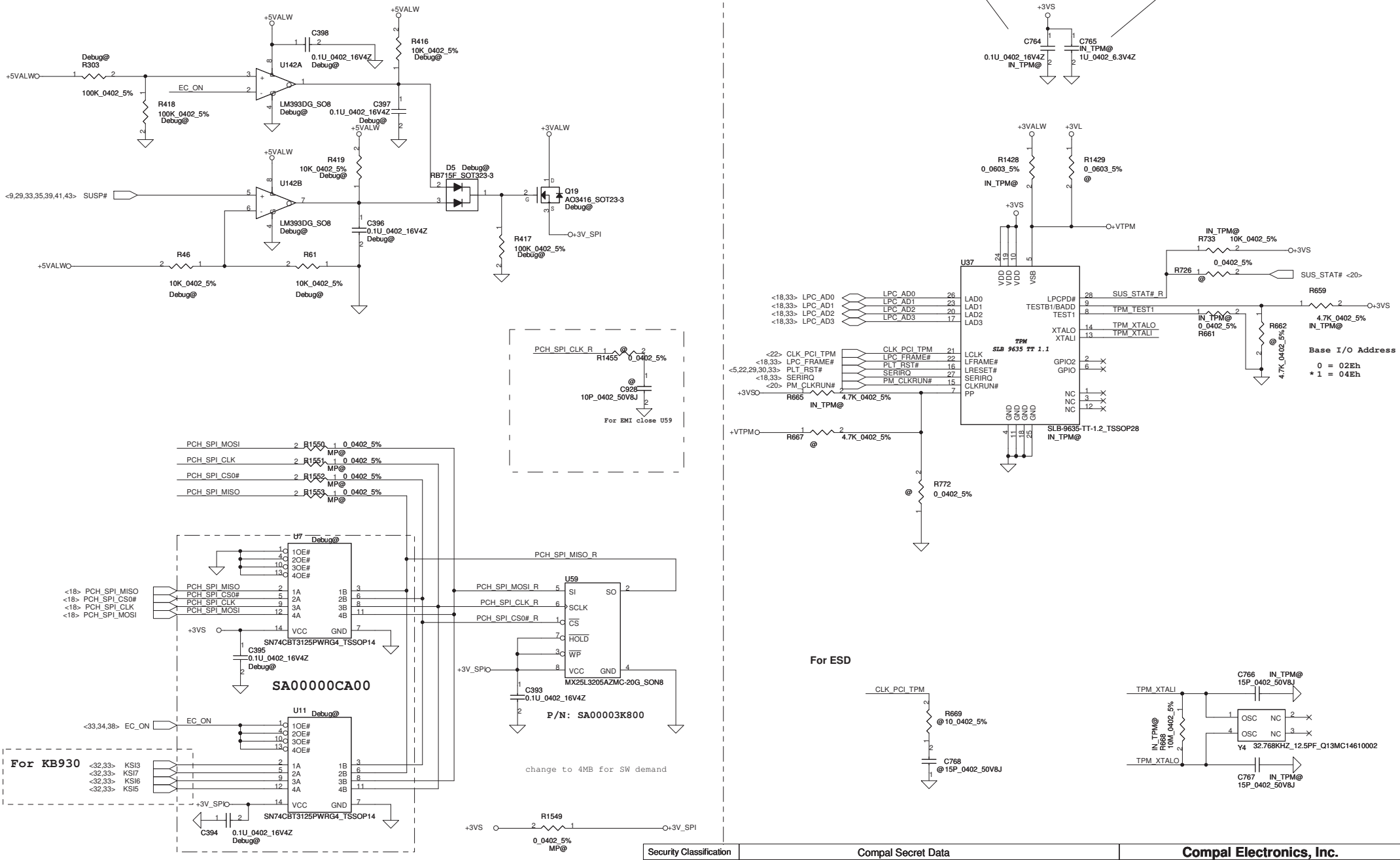
Date: Tuesday, December 07, 2010 Sheet 27 of 45

SPI ROM For Basic ME ROM size (w/o Braidwood & system BIOS): 4MByte

TPM 1.2

C764 close pin 24

C765 close pin 10



Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.

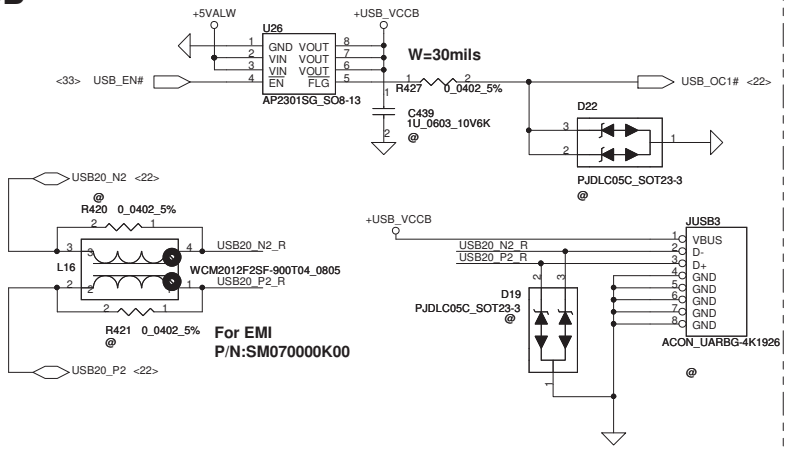
Title: *SPI ROM*

Size	Document Number	Rev
Custom	PBL20 LA6772P M/B	1.0

Date: Tuesday, December 07, 2010 Sheet 28 of 45

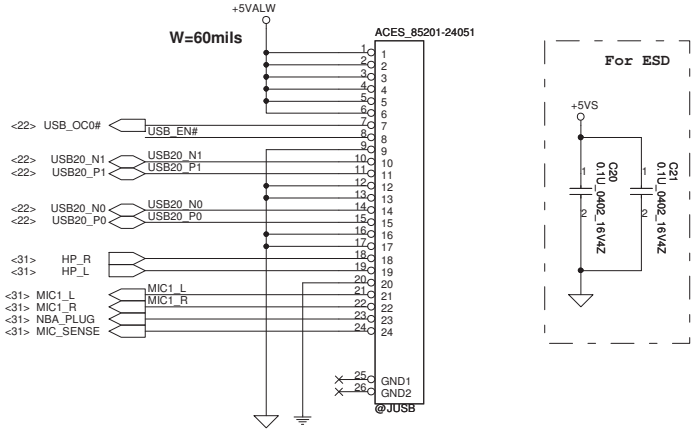
Function Board

Left USB

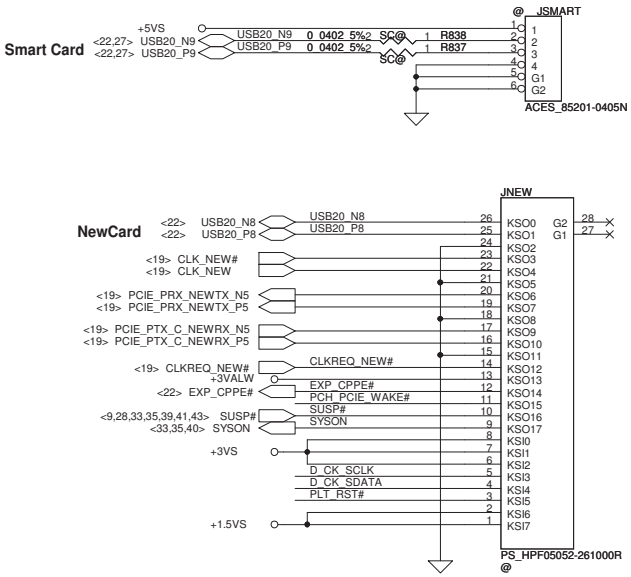


HeadPhone/LINE Out JACK

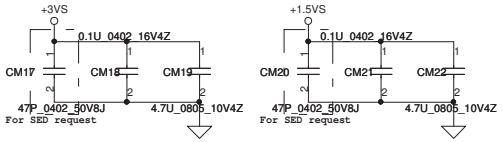
Ext.MIC/LINE IN JACK

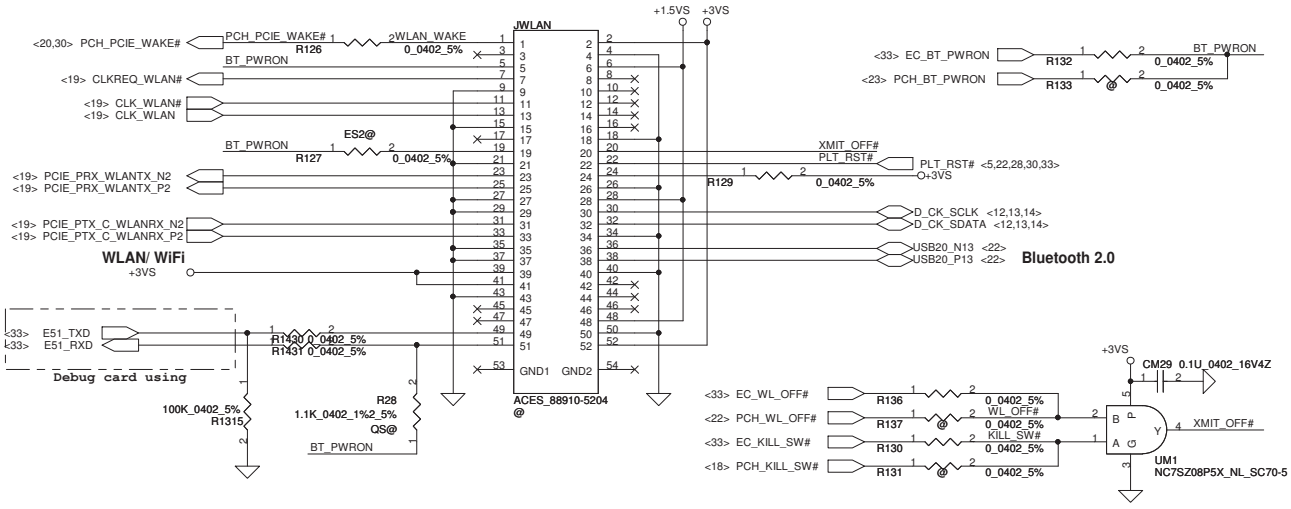


Smart Card and New Card

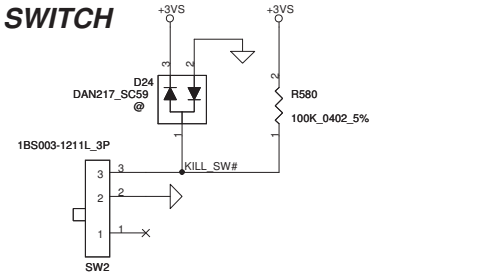


Slot 1 Half PCIe Mini Card-WLAN & BT2.0





Kill SWITCH



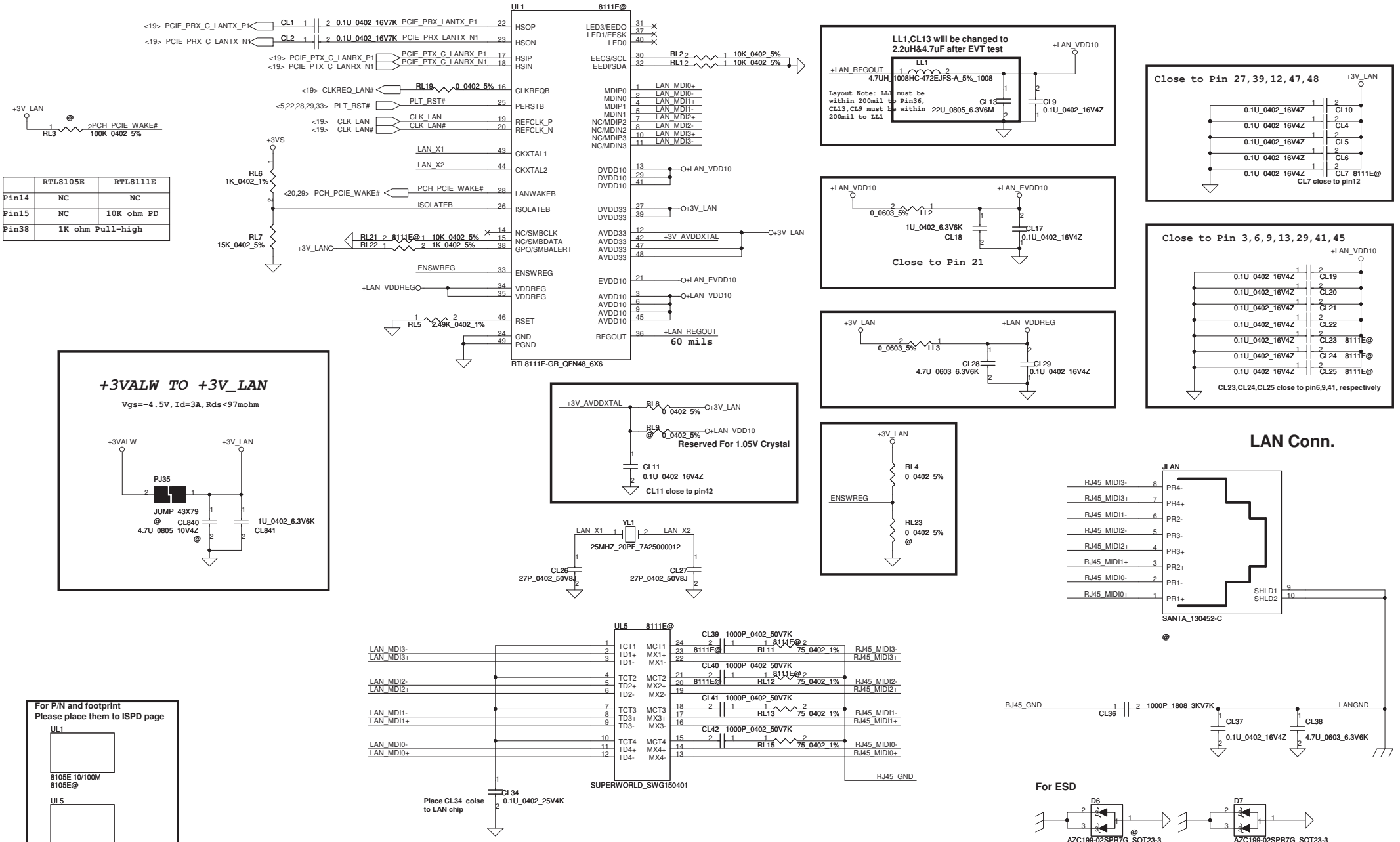
Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.

Title: Function Board/Left USB Port/WLAN/BT

Size	Document Number	Rev
Custom	PBL20 LA6772P M/B	1.0

Date: Tuesday, December 07, 2010 Sheet 29 of 45



	RTL8105E	RTL8111E
Pin14	NC	NC
Pin15	NC	10K ohm PD
Pin38	1K ohm Pull-high	

LAN Conn.

For P/N and footprint
Please place them to ISPD page

For ESD

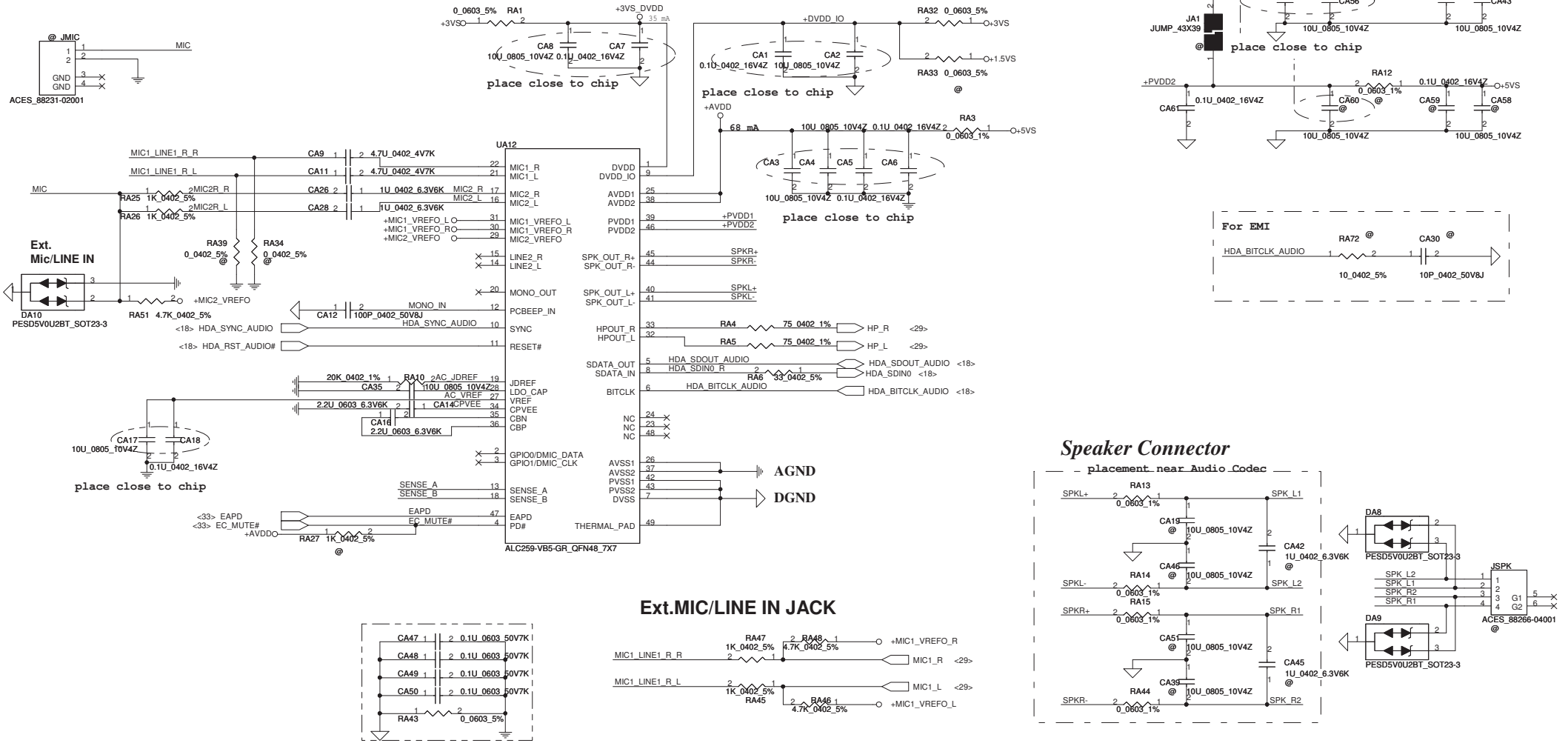
Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.

Title: RTL8105E/8111E

Size: Custom | Document Number: PBL20 LA6772P M/B | Rev: 1.0

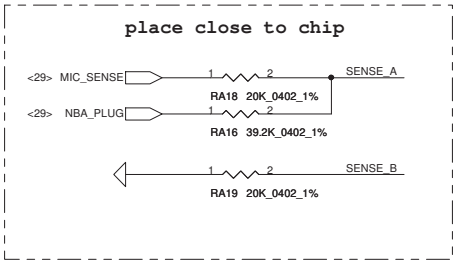
Date: Tuesday, December 07, 2010 | Sheet 30 of 45



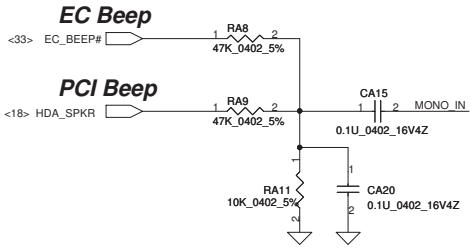
Speaker Connector

Ext.MIC/LINE IN JACK

Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	PORT-D (PIN 35, 36)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	



Beep sound



Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

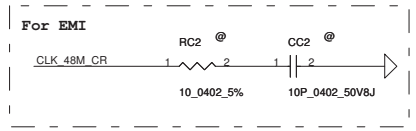
Compal Electronics, Inc.

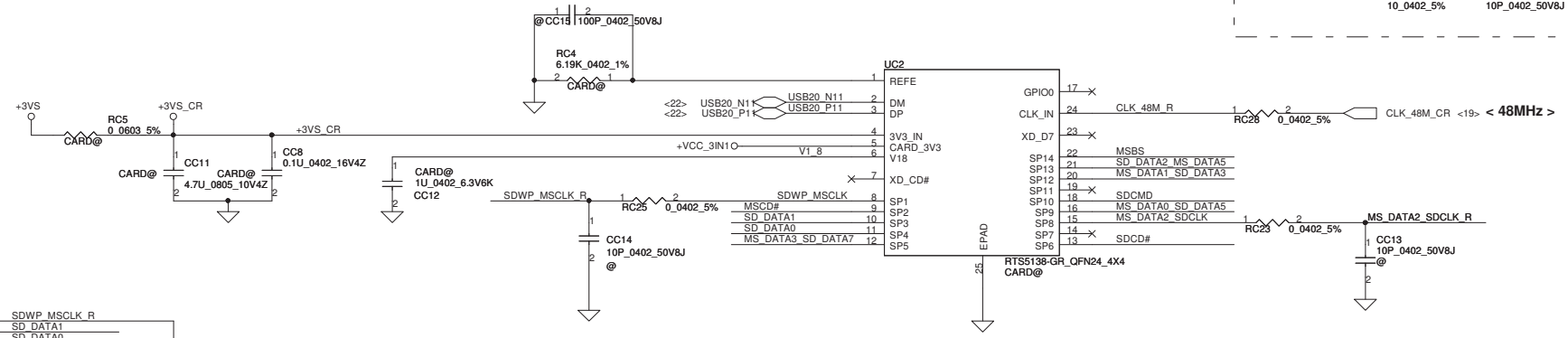
Title: HD Audio Codec ALC259

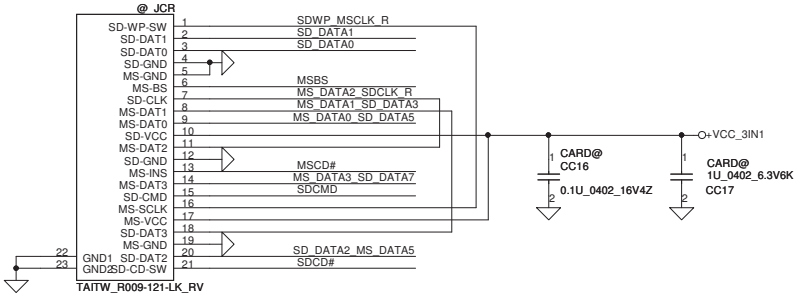
Size: Custom | Document Number: PBL20 LA6772P M/B | Rev: 1.0

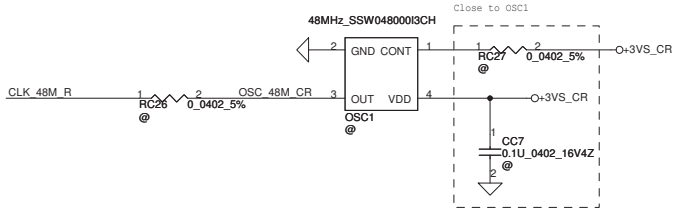
Date: Tuesday, December 07, 2010 | Sheet 31 of 45

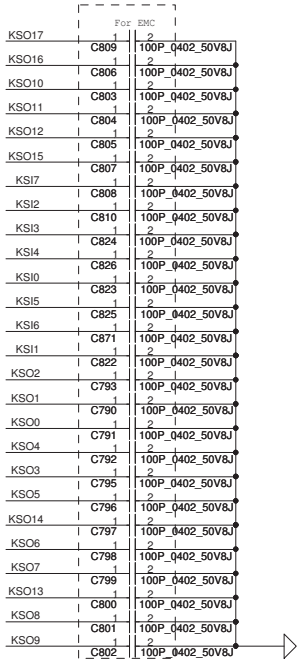
3 in 1 Card Reader



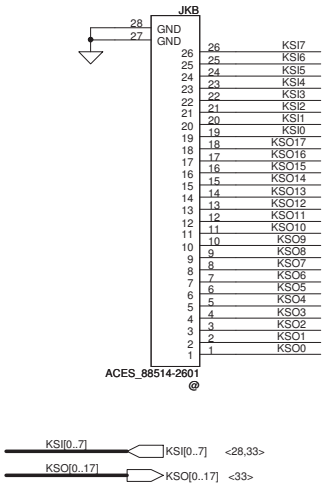








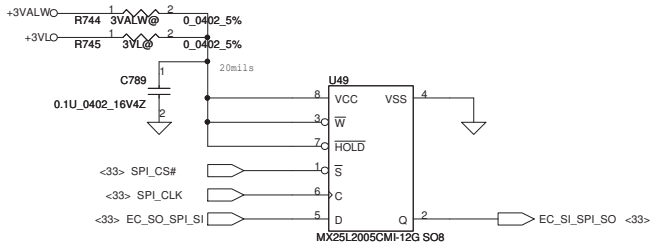
KEYBOARD CONN.



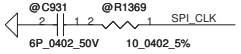
KSI[0..7] KSI[0..7] <28,33>

KSO[0..17] KSO[0..17] <33>

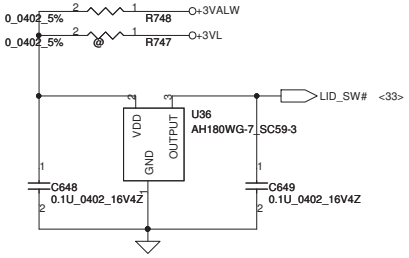
SPI Flash (1MByte*1)



P/N :SA00002C100



Lid SW



Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.

Title: RTS5138 CR/KB/EC SPI/LID

Size: Custom | Document Number: PBL20 LA6772P M/B | Rev: 1.0

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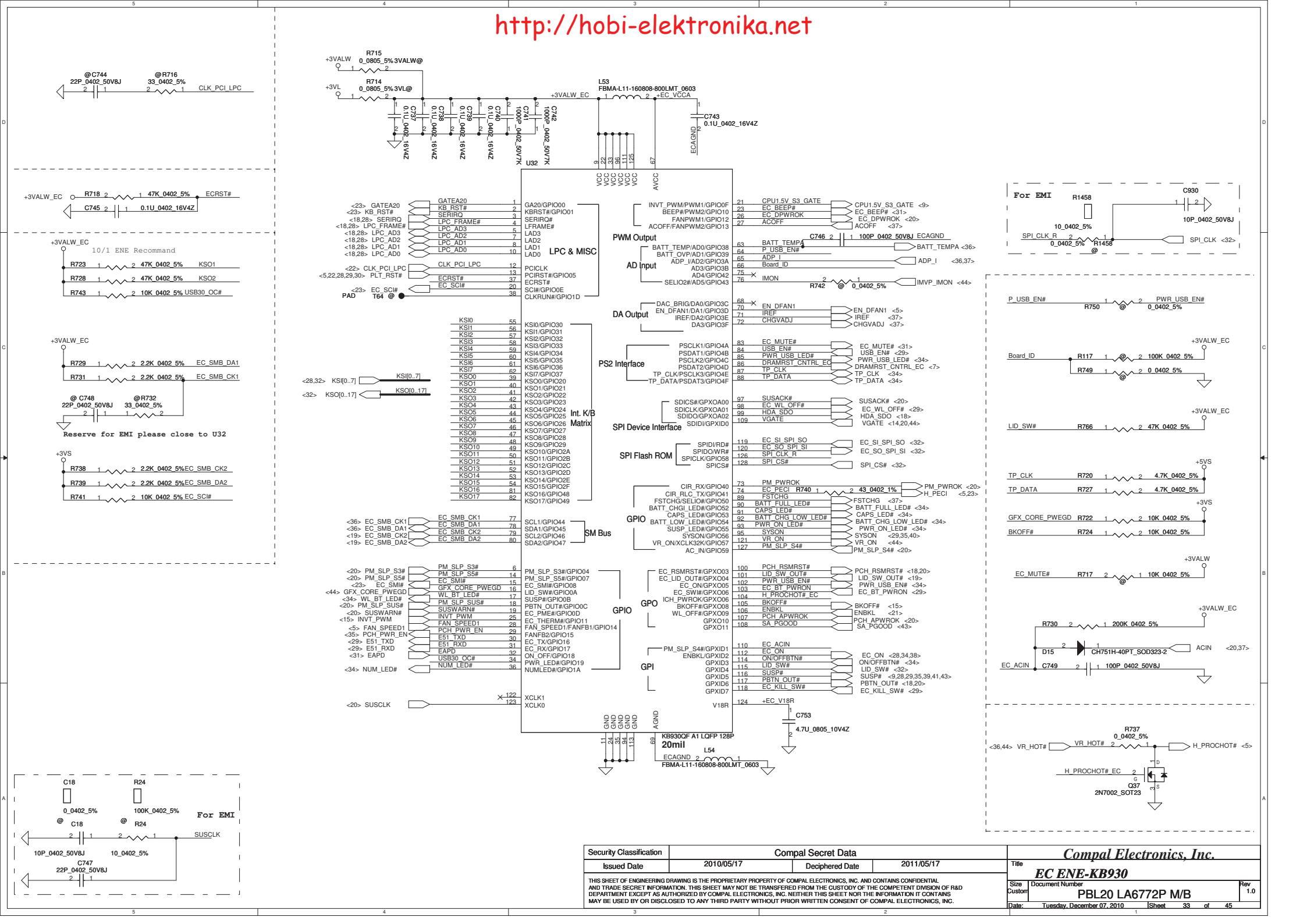

Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.

Title: EC ENE-KB930

Size: Custom | Document Number: PBL20 LA6772P M/B | Rev: 1.0

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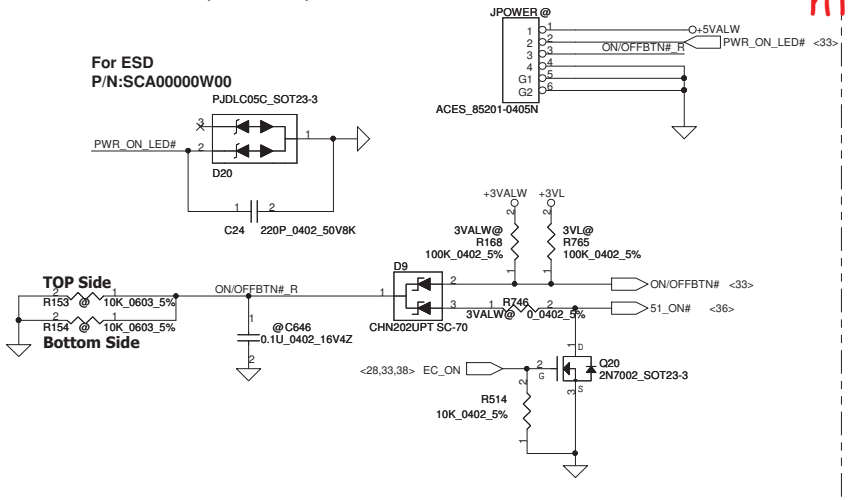
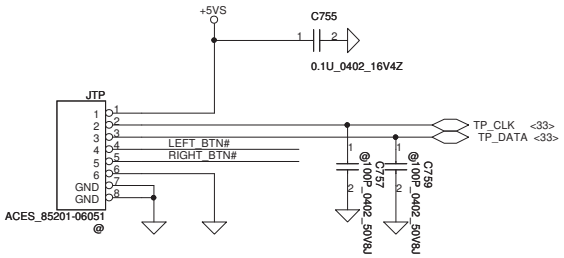
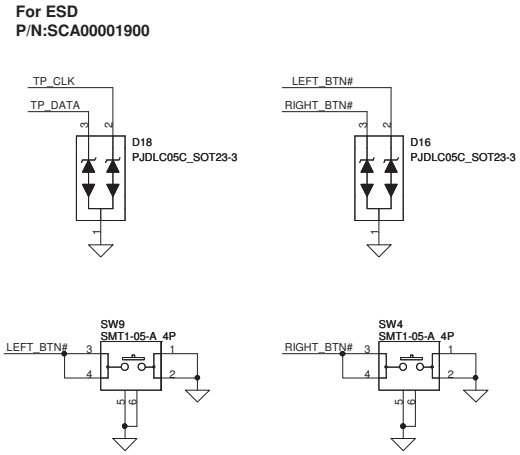
Power Button/ PWR/B

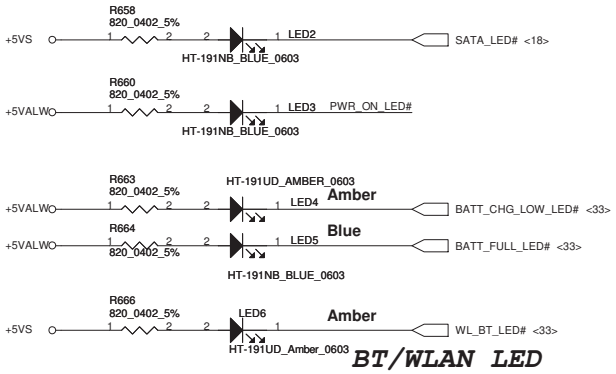


Touch/B Connector

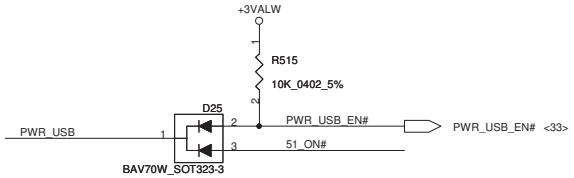




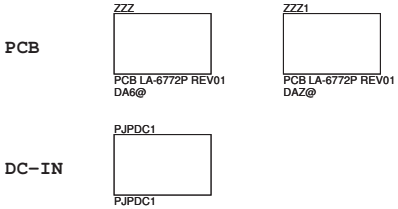
LED

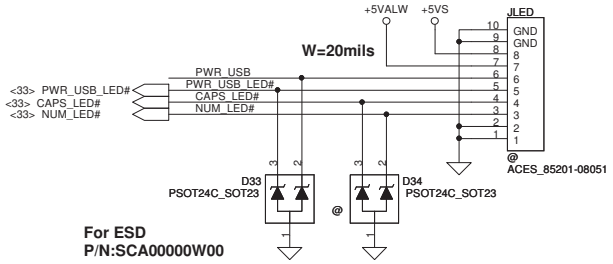


BT/WLAN LED

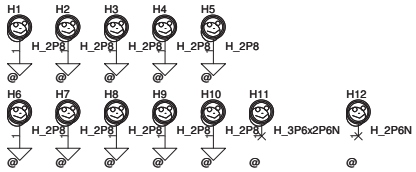


ISPD



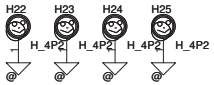


Screw Hole

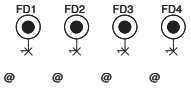


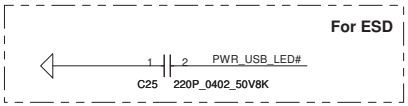
JWLAN

CPU



PCB Fedical Mark PAD





Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.

Title: Power B/TP/LED

Size	Document Number	Rev
B	PBL20 LA6772P M/B	1.0

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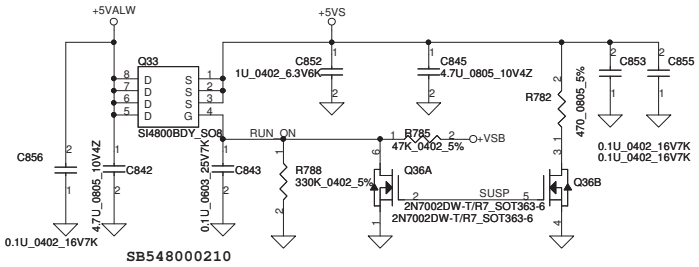
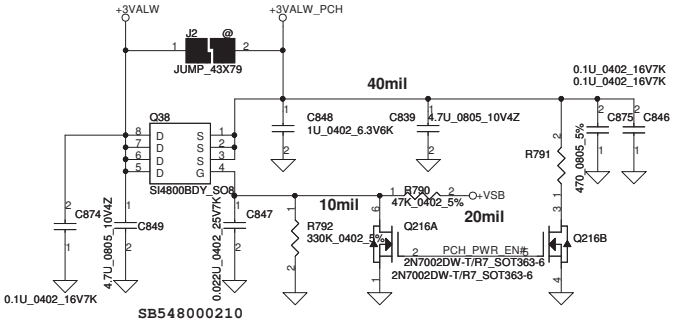
+5VALW TO +5VS

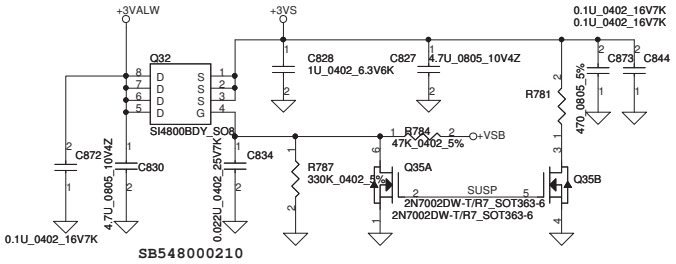


+3VALW TO +3VALW_PCH



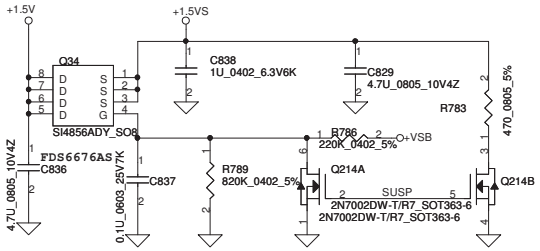
+3VALW TO +3VS

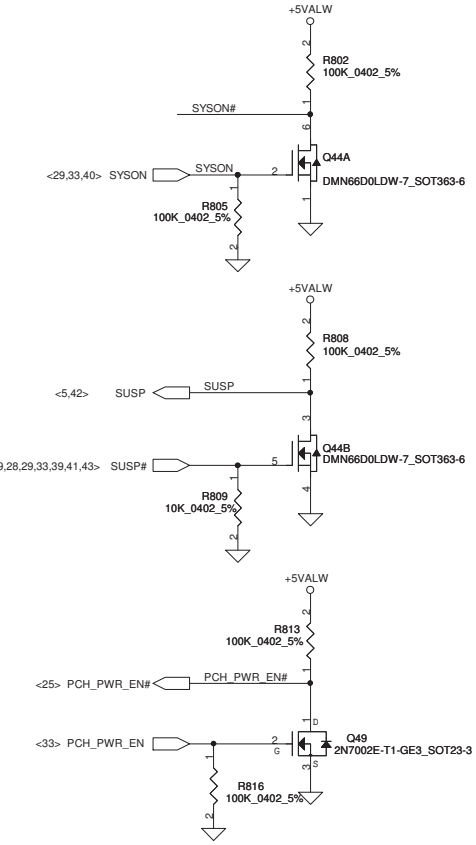
Vgs=-0V,Id=9A,Rds=18.5mohm

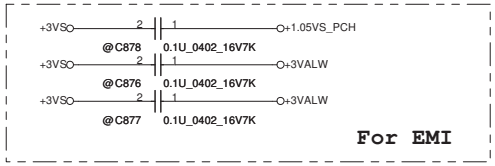


+1.5V to +1.5VS

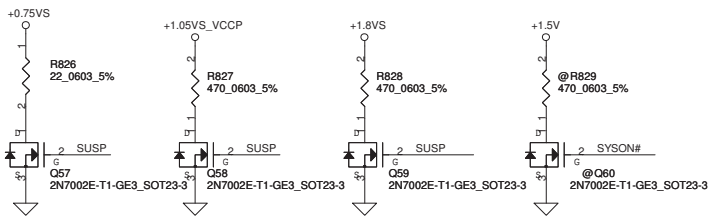
Vgs=10V,Id=14.5A,Rds=6mohm

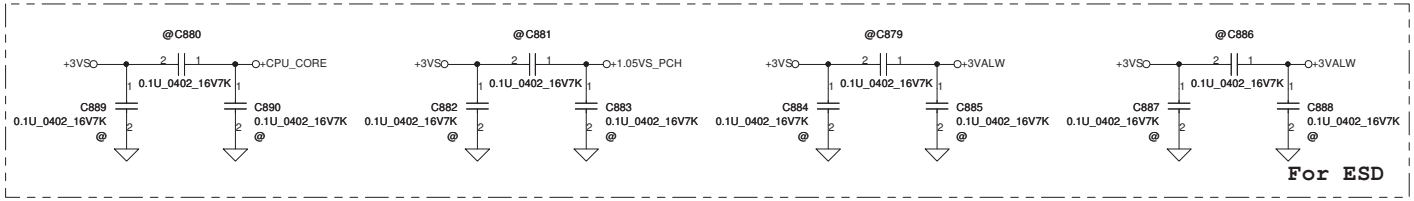






2009/08/14
CP_S3PowerReduction
WhitePaper_Rev0.9
0.75VS speed up discharge





Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.

Title: DC Interface

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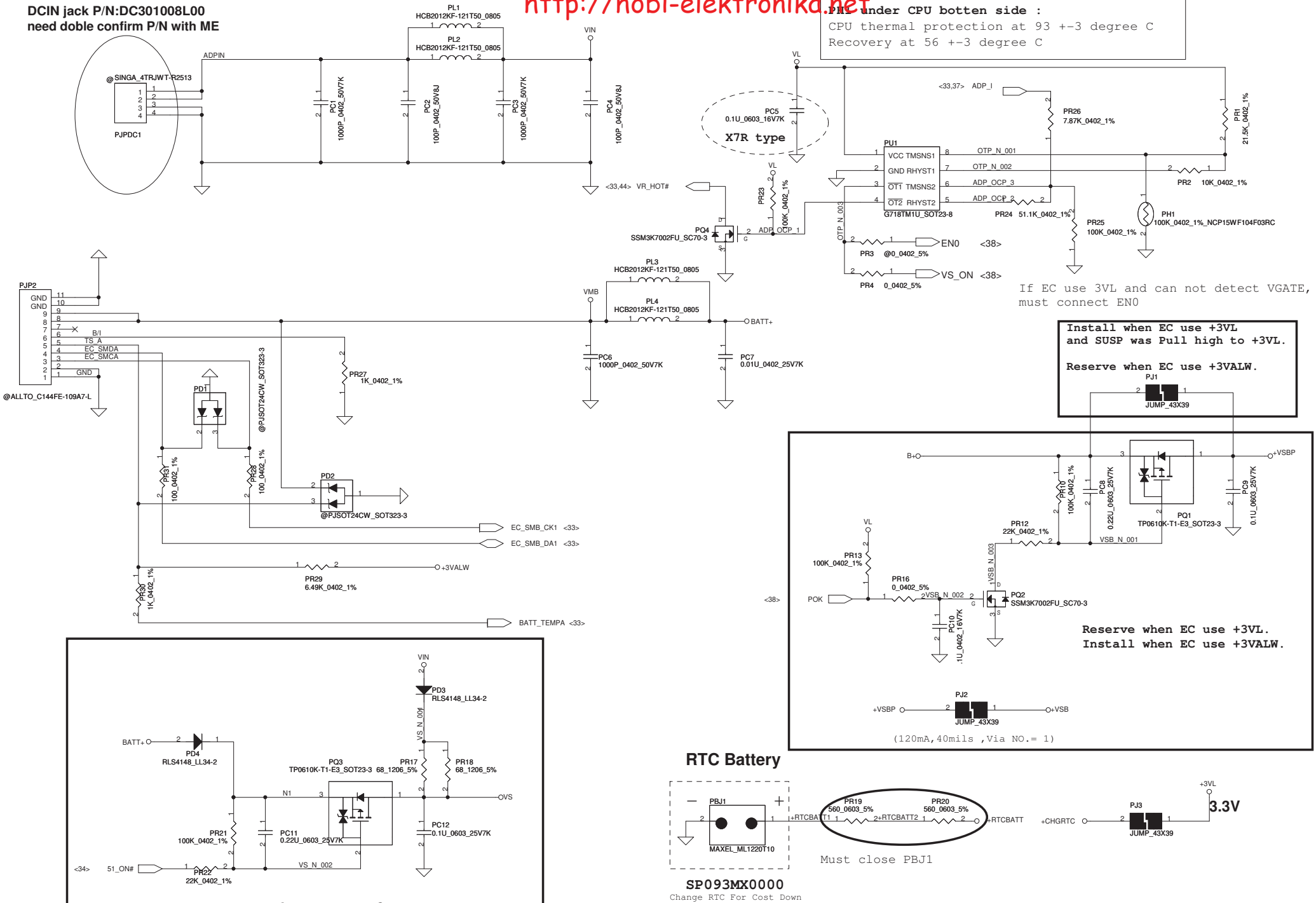
DCIN jack P/N:DC301008L00
need doble confirm P/N with ME

PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C



Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.	
Title	DCIN / BATT CONN / OTP
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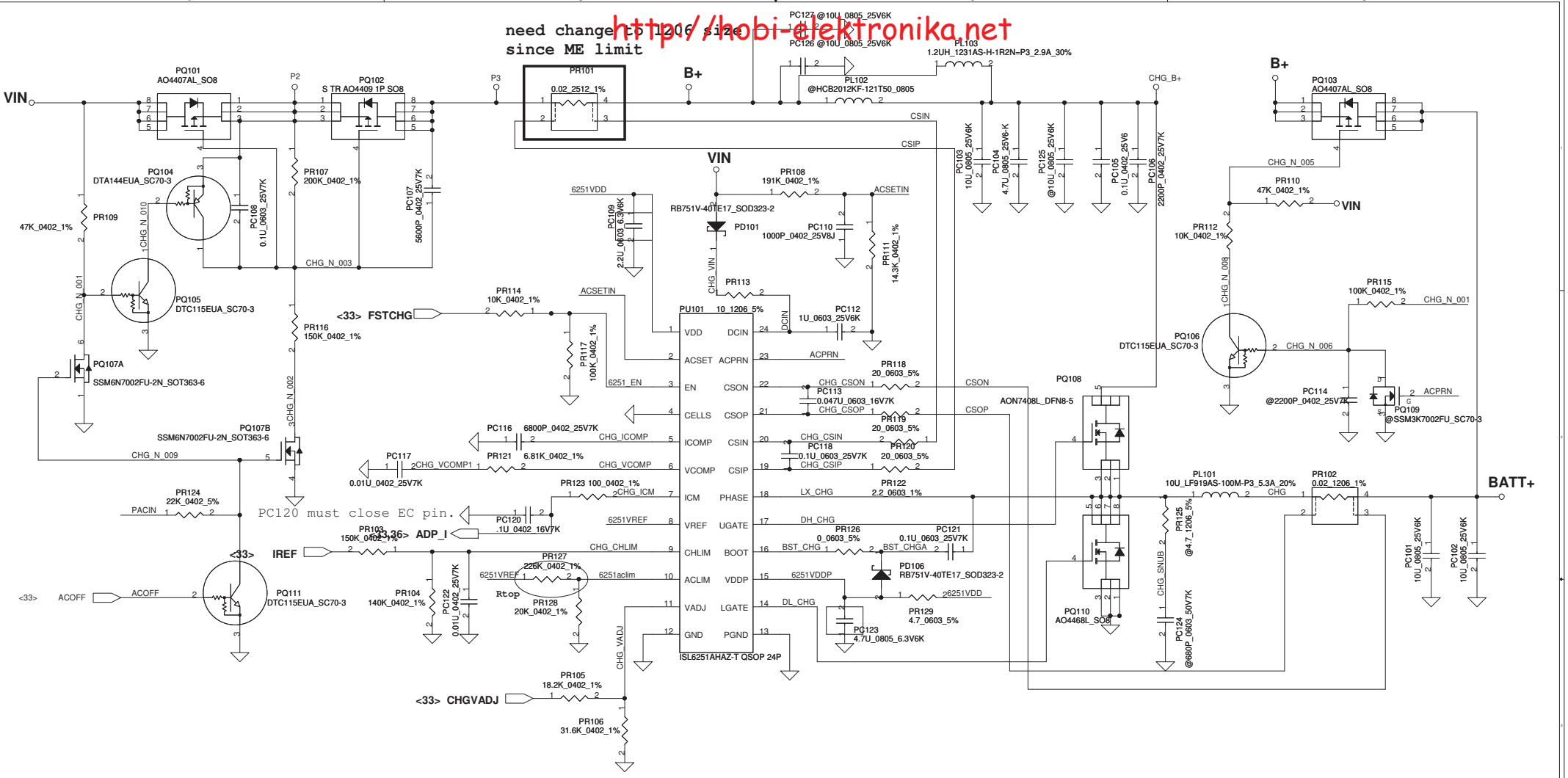
need change to 1206 size
since ME limit




```
CP= 85%*Iada;
Iada=0~4.737A(90W);CP=4.03A;where Racdet=0.020ohm,where Rtop=12.4K
90W for Dis:Rtop:SD00000AJ80
Iada=0~3.421A(65W);CP=2.91A;where Racdet=0.020ohm,where Rtop=226K
65W for UMA:Rtop:SD034226380
Astro2010_01_15 need confirm P/N
```

```
CP mode
Vaclim=VREF*(Rbot//Rinternal/(Rtop//Rinternal+Rbot//Rinternal))
when 90W Vaclim=2.39*(20K//152K/(20K//152K+12.4K//152K))=1.44966V
when 65W Vaclim=2.39*(20K//152K/(20K//152K+226K//152K))=0.38914V
Iinput=(1/Racdet)*((0.05*Vaclim/VREF+0.05))
when 90W,Iinput=(1/0.02)*(0.05*1.44966/2.39+0.05)=4.02A
when 65W,Iinput=(1/0.02)*(0.05*0.38914/2.39+0.05)=2.92A
```

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)/0.10627

Vcell	CHGVADJ
4V	0V
4.2V	1.882V

Add

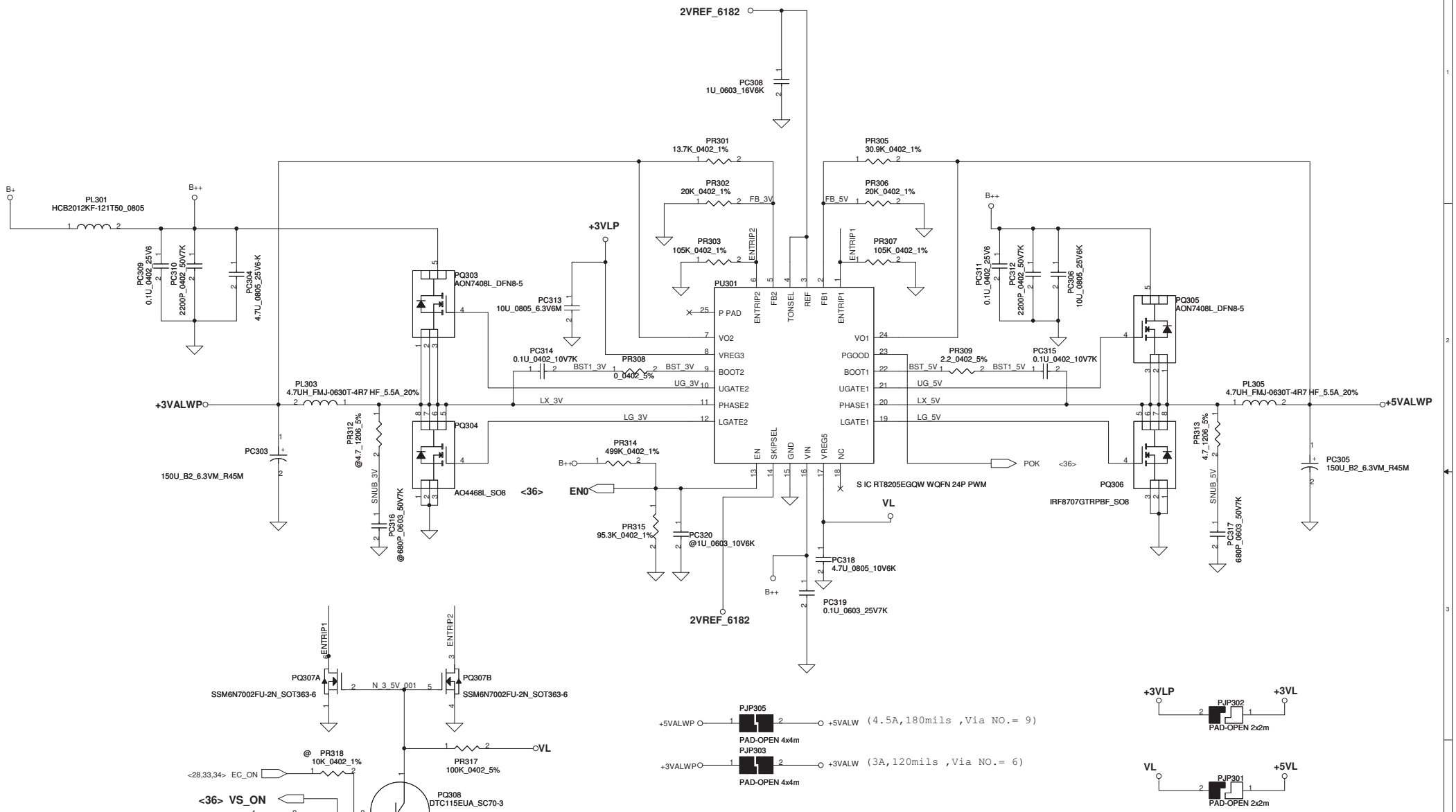
Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.

Title: CHARGER

Size	Document Number	Rev
	NCL61 LA-6321P M/B	1.0

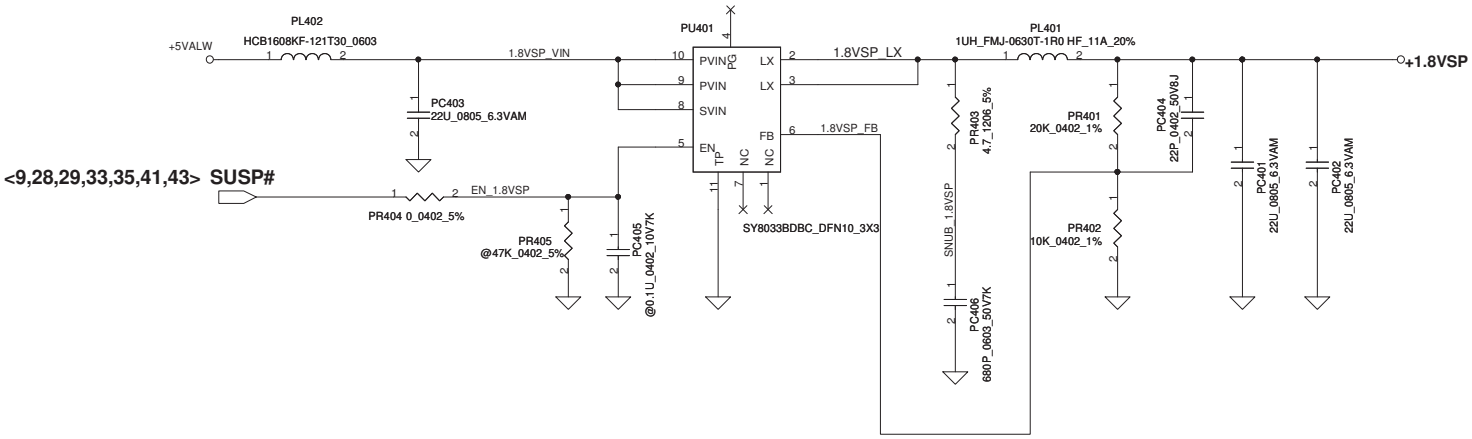
Date: Tuesday, December 07, 2010 | Sheet 37 of 45



EC:+3VL, reserve PR319, install PR318, PR320 100K
EC:+3VALW, reserve PR318, install PR319, PR320 40.2K

Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.			
Title	3.3VALWP/5VALWP		
Size: Custom	Document Number: PBL20 LA6772P M/B		Rev: 1.0
Date: Tuesday, December 07, 2010	Sheet 38 of 45		



<Vo=1.8V> VFB=0.6V
Vo=VFB*(1+PR401/PR402)=0.6*(1+20K/10K)=1.8V

(2A, 80mils, Via NO.= 4)

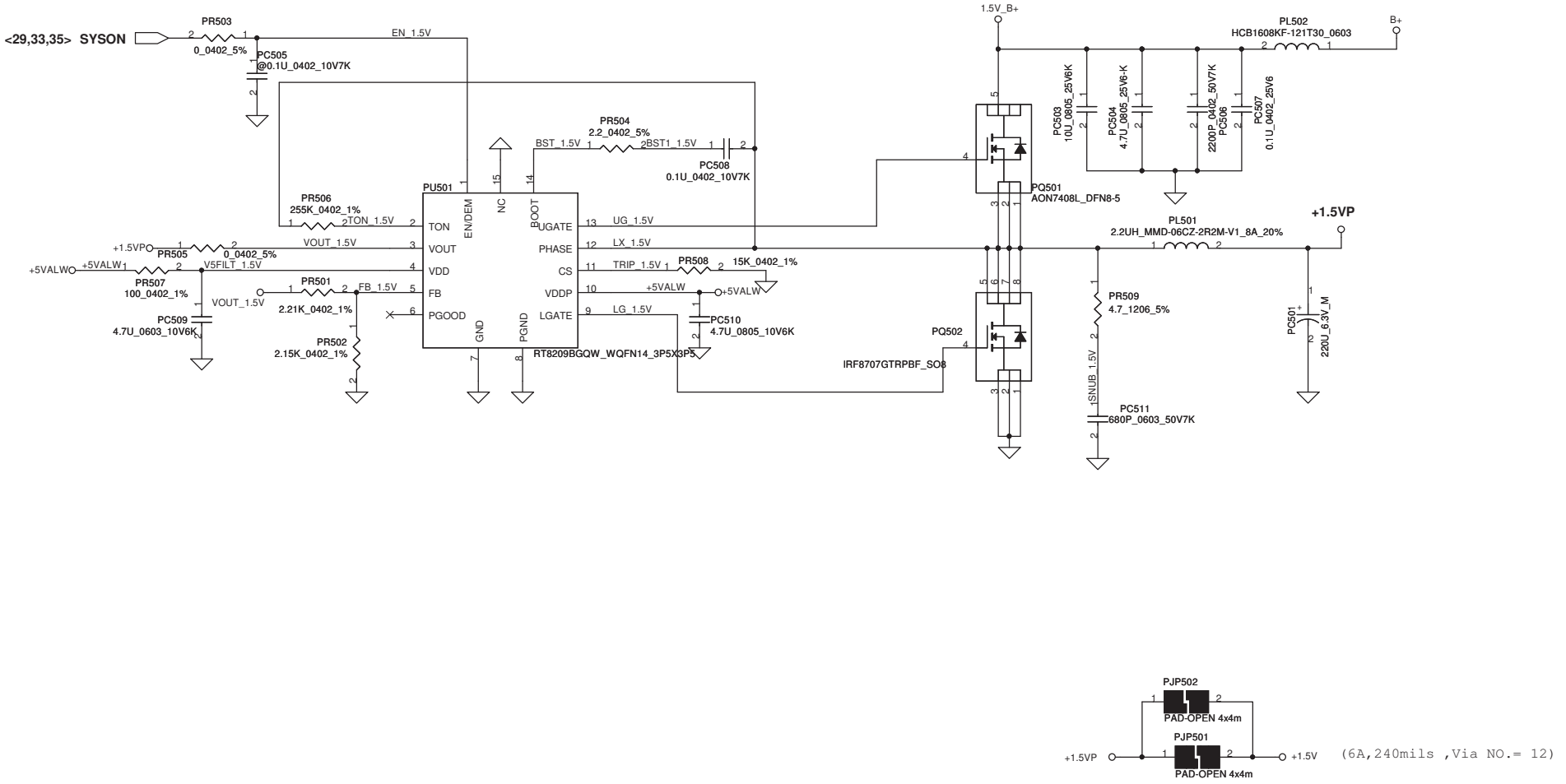
Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.

Title: **+1.8VSP**

Size	Document Number	Rev
	NCL61 LA-6321P M/B	1.0

Date: Tuesday, December 07, 2010 | Sheet 39 of 45



(6A,240mils ,Via NO.= 12)

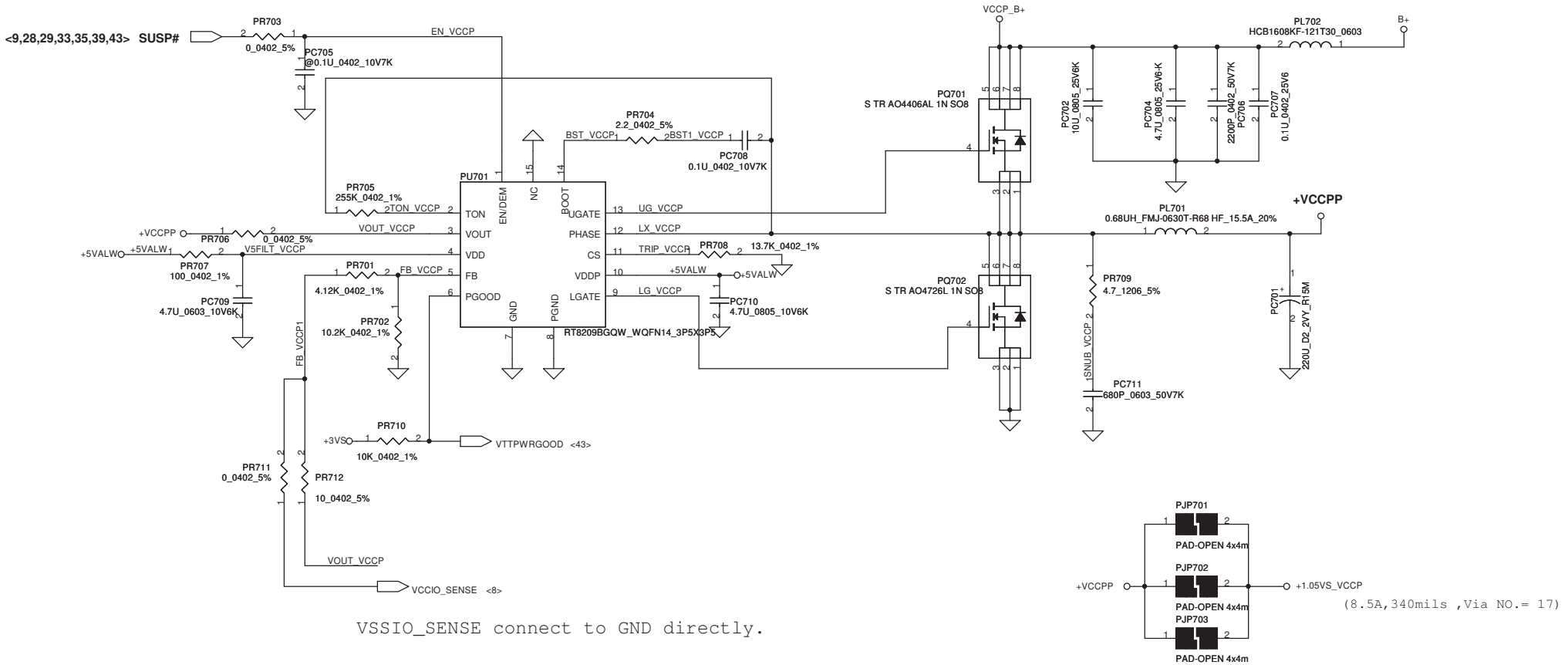
Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.

Title: **+1.5VP**

Size	Document Number	Rev
	PBL20 LA6772P M/B	1.0

Date: Tuesday, December 07, 2010 | Sheet 40 of 45



VSSIO_SENSE connect to GND directly.

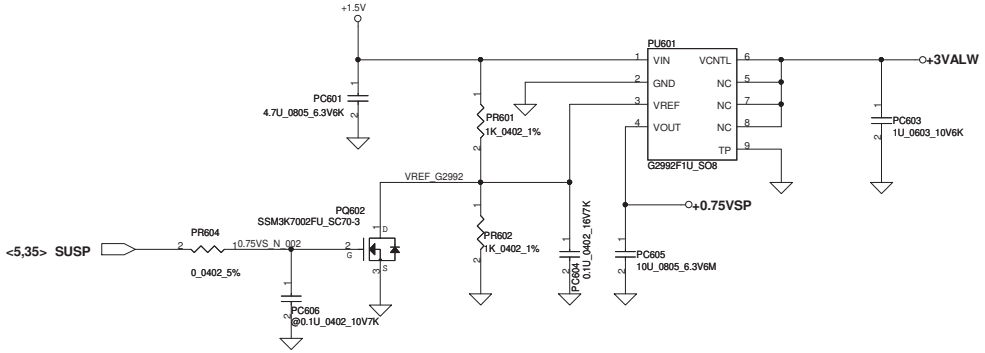
Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

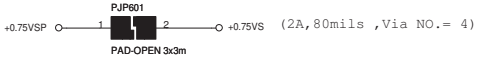
Compal Electronics, Inc.

Title: PWR+1.05VSP/+VCCPP

Size: Custom | Document Number: PBL20 LA6772P M/B | Rev: 1.0

Date: Tuesday, December 07, 2010 | Sheet 41 of 45





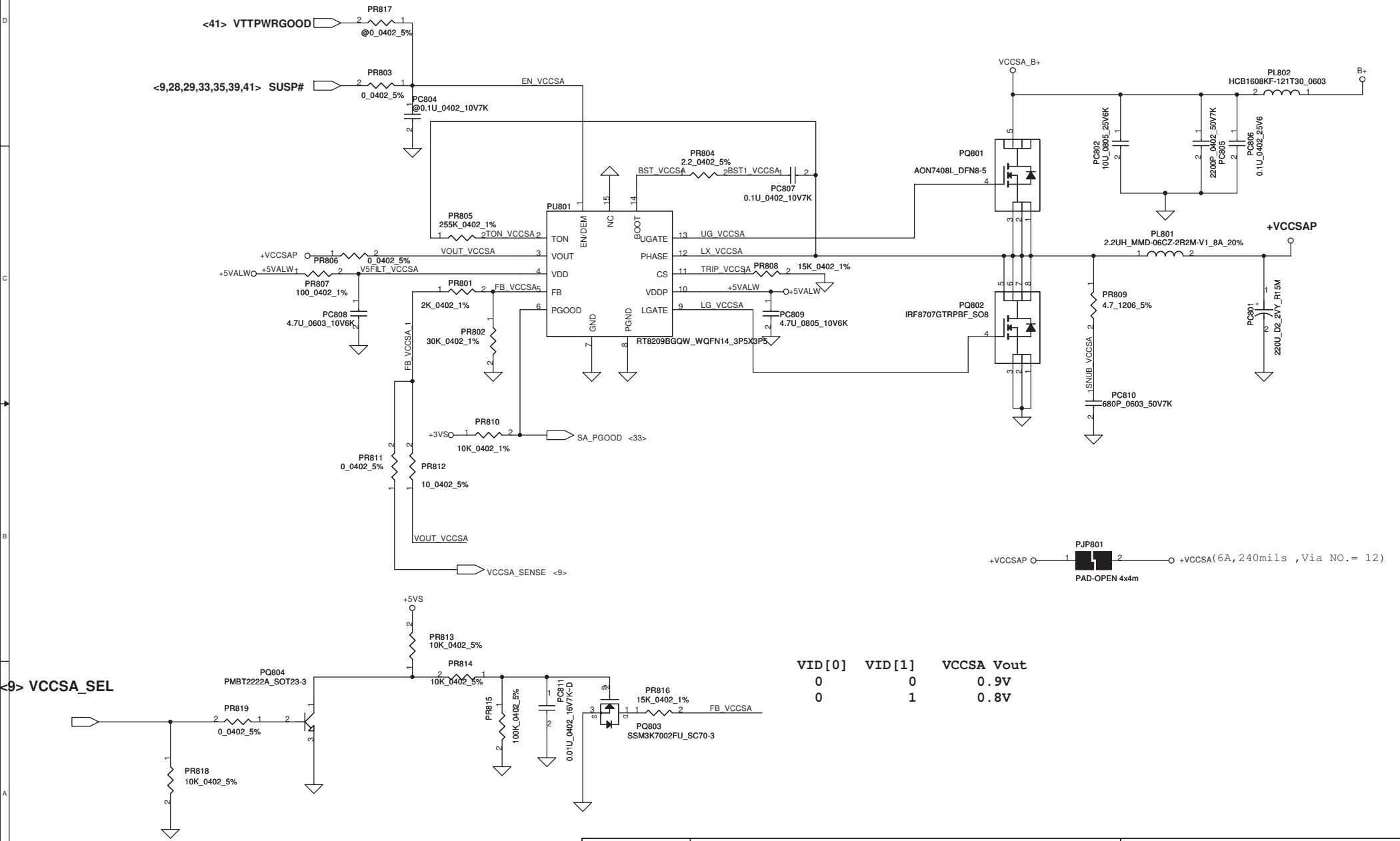
Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.

Title: 0.75VSP

Size | Document Number: PBL20 LA6772P M/B | Rev: 1.0

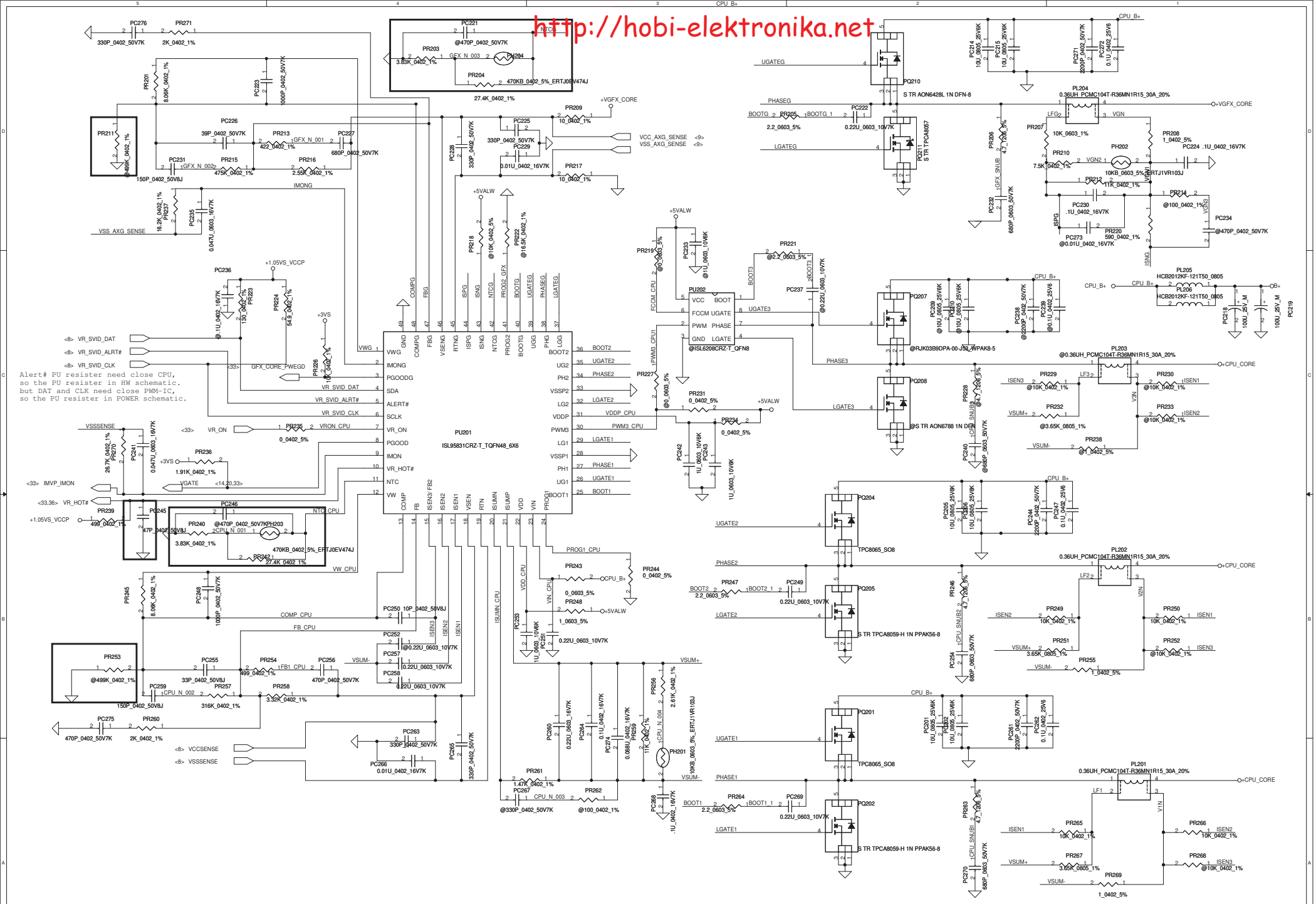
Date: Tuesday, December 07, 2010 | Sheet 42 of 45



VID[0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V

Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.			
Title: PWR+VCCSAP			
Size: Custom	Document Number: PBL20 LA6772P M/B		Rev: 1.0
Date: Tuesday, December 07, 2010	Sheet 43 of 45		



Security Classification	Compal Secret Data		
Issued Date	2010/05/17	Deciphered Date	2011/05/17

Compal Electronics, Inc.			
Title: PWR-CPU_CORE			
Size: C	Document Number: PBL20 LA6772P M/B		Rev: 1.0
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PIR (Product Improve Record)

PBL20 LA-6772P SCHEMATIC CHANGE LIST
REVISION CHANGE:

Revision Change: 0.1 to 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	08/03	17	DELETE U47, C869, R1530 and R572	For HDMI detect issue
2	08/03	17	Change R573 to 20K	For HDMI detect issue
3	08/03	31	Change RA16 to 39.2K	For Headphone detect issue
4	08/03	15	DELETE L25, C320 and C401	For cost down
5	08/04	31	Add RA19	For Headphone detect issue
6	08/20	5	Delete R61, R63, R206, R257, R208, R261, R259 and C16	For remove XDP connector
7	08/20	7	Add C233 and C232	For DDR3 1333 EMI issue
8	08/20	15	Delete L25, C401 and C320	For cost down
9	08/20	17	Delete U10, R405, R407, R410, R705, R409, R408, R406, R411, R403, R404, R402, R221, R253, R254 , R412, R413, R414 and R222	Remove level shift for cost down
10	08/20	19	Add C499 and C500	For add new card function
11	08/20	19	Delete R258 and R260	For remove XDP connector
12	08/20	23	Add R425	ODD_EN# pull-up 10K to +3VS
13	08/20	28	Add R303, R46 and R61	For SPI and ME ROM
14	08/20	29	Add JSMART connector	For add smart card connector
15	08/20	29	Add JNEW	For add new card connector
16	08/20	29	Add R127 ,R28 and R129	For support intel W/L
17	08/20	29	Add R132, R133, R136, R137, R130 and R131	For SW GPIO common
18	08/20	33	Delete X1, C751 and C752	For cost down
19	08/20	34	Add D20	For ESD issue

Revision Change: 0.2 to 0.3

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	09/01	34	Add R515	PWR_USB_EN# pull-up 10K to +3VALW
2	09/01	5	Add C16	FOR ESD issue
3	09/02	35	Add C880, C889, C890, C881, C882, C883, C879, C884 ,C885, C886, C887 and C888	FOR ESD issue
4	10/06	34	Add D25	For USB issue
5	10/11	18	Add R172	For Power Saving
6	10/14	27	Add R835 and R836	For smart card with ODD
7	10/14	29	Add R837 and R838	For smart card with ODD
8	10/18	30	Add D6 and D7	For ESD issue
9	10/20	33	Add R743	For common design
10	10/20	22	Add R318	For add TPM 1.2
11	10/20	28	Add C764, C765, U37, R733, R726, R659, R662, R661, R665, R772, R669, C768, R668, C766, C767 and Y4	For add TPM 1.2

Revision Change: 0.3 to 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	12/01	29	Change JNEW conn.	For ME
1	12/03	33	Add R117, R749 and R750	For EC
1	12/01	29	Add D22	For USB power switch issue

Compal Electronics, Inc.

Title: HW-PIR

Size | Document Number: PBL20 LA6772P M/B | Rev: 1.0

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