

# Compal Confidential

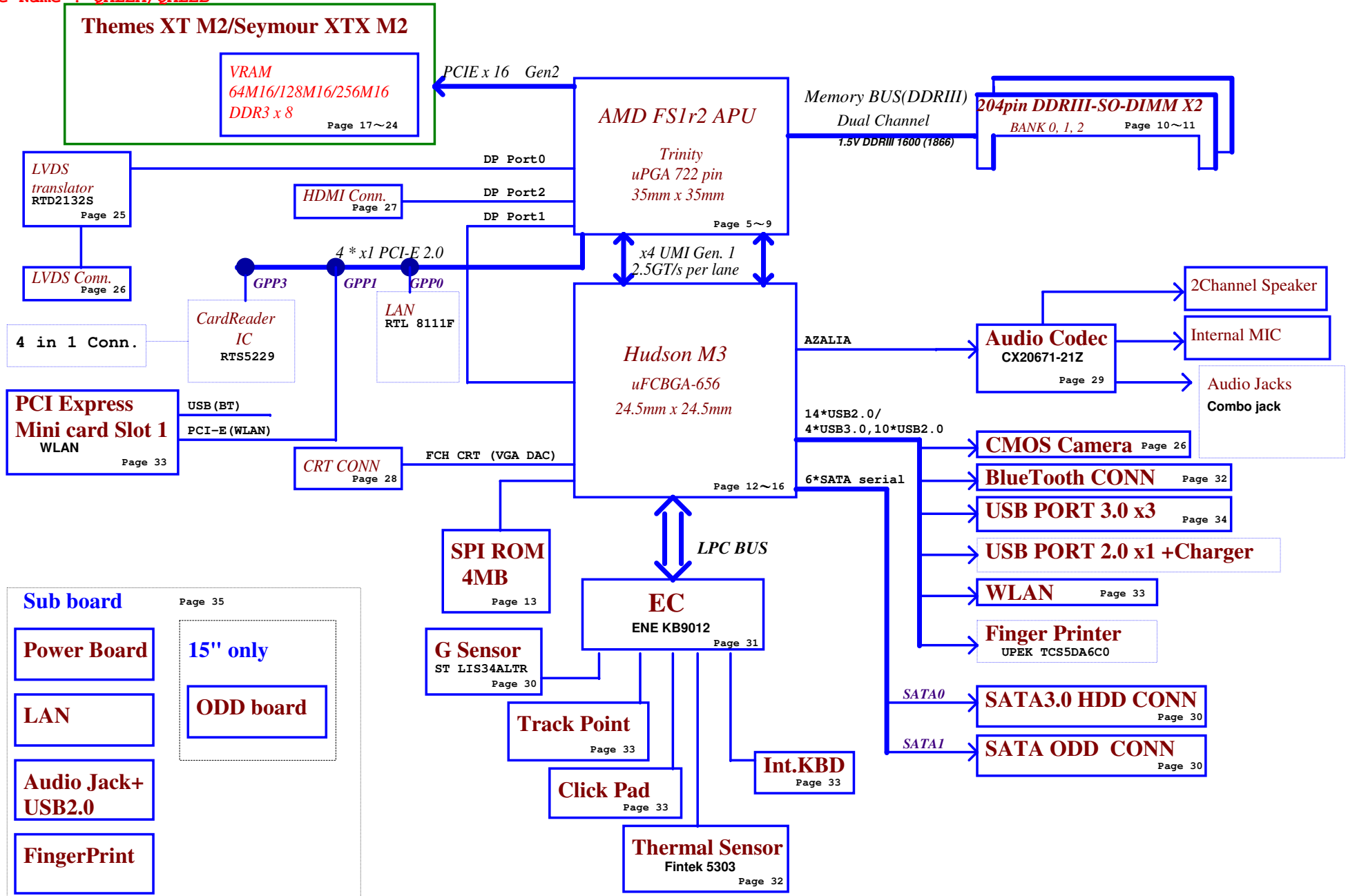
## QALEA/QALEB Schematics Document

AMD APU Trinity FS1r2 + FCH Hudson-M3 + GPU Seymour XTX/Thames XT

2012-01-16

REV: 0.4

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**Sub board** Page 35

- Power Board
- LAN
- Audio Jack+ USB2.0
- FingerPrint
- Card reader
- 15" only
- ODD board

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## Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+1.5V	1.5V power rail for APU VDDIO and DDR	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.2VS	1.2V (VDDR, VDDP) switched power rail for APU	ON	OFF	OFF
+2.5VS	2.5V for APU VDDA	ON	OFF	OFF
+1.1VALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VGS	1.5V switched power rail	ON	OFF	OFF
+1.8VGS	1.8V switched power rail	ON	OFF	OFF
+1.0VGS	1.0V switched power rail for VGA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS_WLAN	3.3V power rail for WLAN	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## FCH Hudson-M2/3 SATA Port List

SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

## Comal PCIE Port List

APU	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	NC
	PCIE3	Card Reader
FCH	PCIE0	NC
	PCIE1	NC
	PCIE2	NC
	PCIE3	NC

## FCH Hudson-M2/3 USB Port List

USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	USB2.0 Port
Port1	NC
Port2	NC
Port3	NC
Port4	NC
Port5	WLAN
Port6	CMOS
Port7	FP
Port8	BT
Port9	NC
Port10	USB 3.0
Port11	USB 3.0
Port12	USB 3.0
Port13	NC

## EC SM Bus1 address

## EC SM Bus2 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001-011xb	15H	F75303 (DDR,VRAM,CPUCORE)	1001-101xb	9AH
			SB-TSI	1001-100xb	98H
			Seymour XTX	1000-0010b	82H
			LVDS translator		

## BOM Structure

UMA@ : UMA only  
 DIS@ : DIS muxluss  
 PX40@ : PX4.0 Support  
 PX50@ : PX5.0 Support  
 CMOS@ : USB camera

CONN@ : ME components  
 X76@, H2G@, S2G@ : VRAM

Tha@ : Thames VGA  
 Sey@ : Seymour VGA

## BOM option and stencil

SDV:  
 CMOS@/DIS@/PX40@/SEY@ + X76@

PJ201, PJ401, PJ502, PJ503, PJ504, PJ601, PJ603, PJ604,  
 PJ701, PJ702, PJ703, PJ704, J1, J2301, J2401, J2402, J2403  
 PJ402, PJ403, PJ501, PJ602, PJ801, PJ802, PJ803, PJ804, PJ805

## FCH SMB0

(FCH\_SMB0)

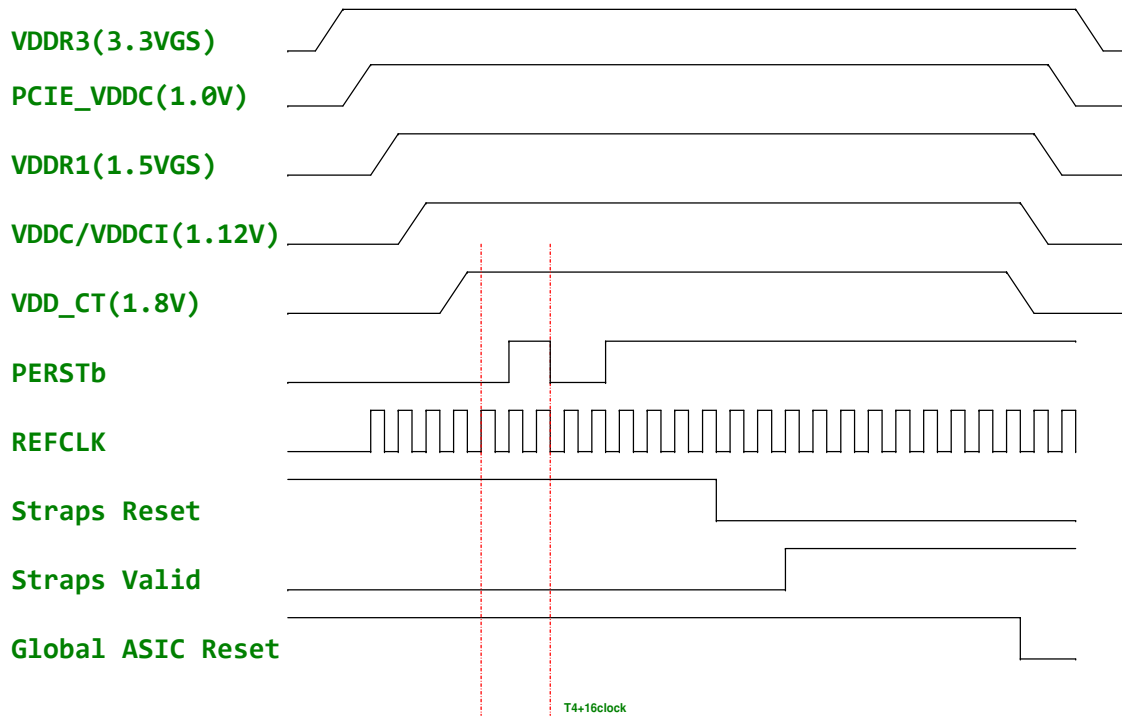
Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		
Security ROM		

## Stencil Memo

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## Power-Up/Down Sequence

- All the ASIC supplies, except for VDDR3, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. There is no timing requirement on the ramp up of VDDR3 relative to other power rails.
- The external pull-up resistors on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD\_CT have ramped up.
- VDDC and VDD\_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD\_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.



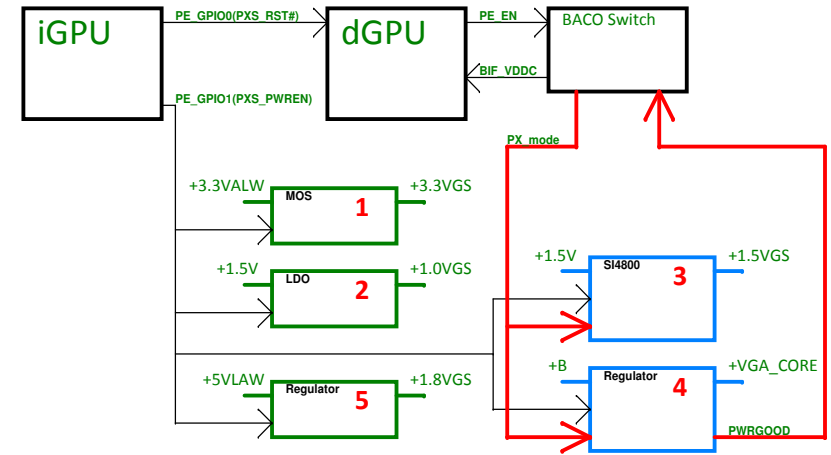
### Without BACO option :

PE\_GPIO0 : Low -> Reset dGPU ; High -> Normal operation  
 PE\_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

### BACO option :

PE\_GPIO0 : High -> Normal operation (dGPU is not reset on BACO mode)  
 PE\_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

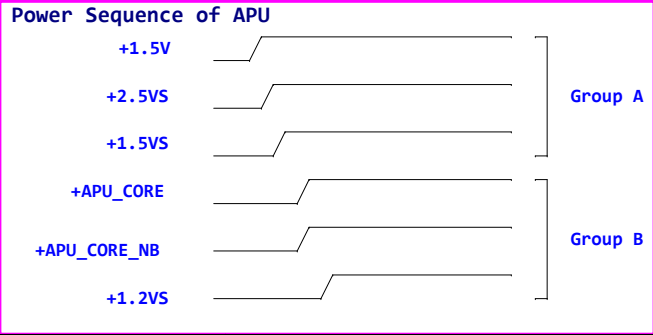
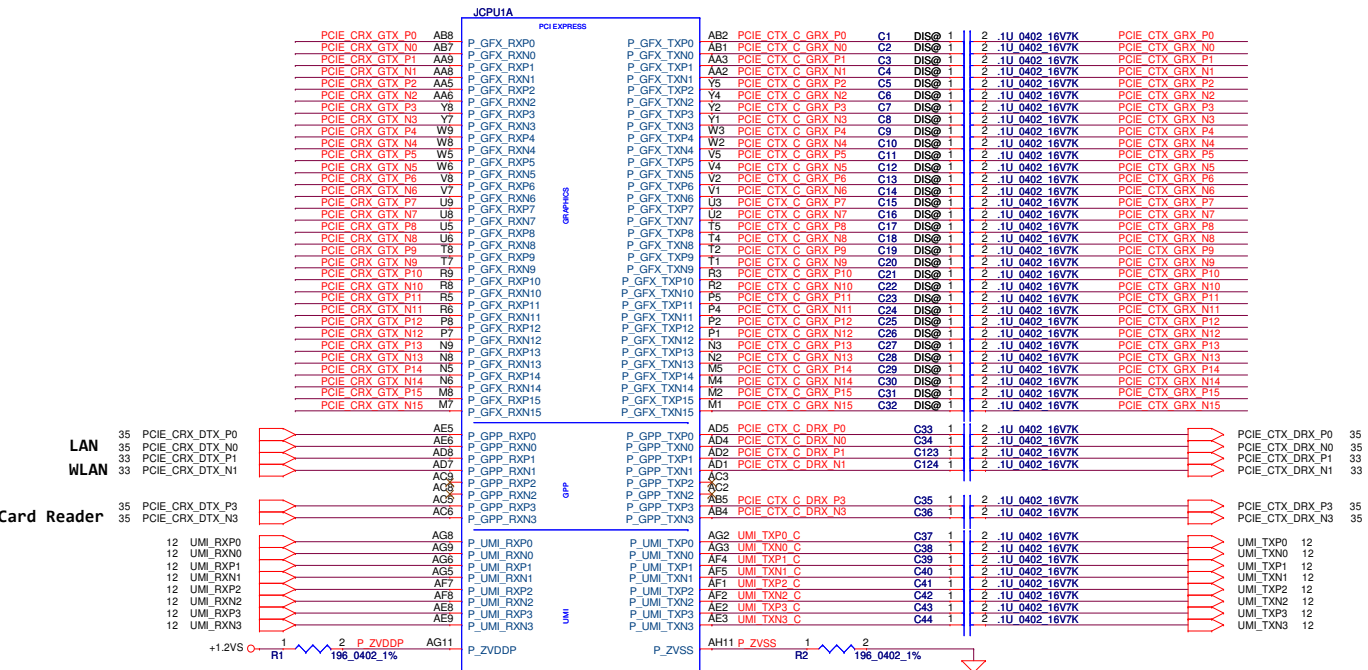
dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1D1, A2VDDQ, VDD2D1, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	775mA
PCIE_VDDC	1.0V	OFF	ON	1.1A
VDDR3	3.3V	OFF	ON	60mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	1.2A
VDDC/VDDCI	TBD	OFF	OFF	28



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17 PCIE\_CRX\_GTX\_P0[0..15]  
17 PCIE\_CRX\_GTX\_N0[0..15]

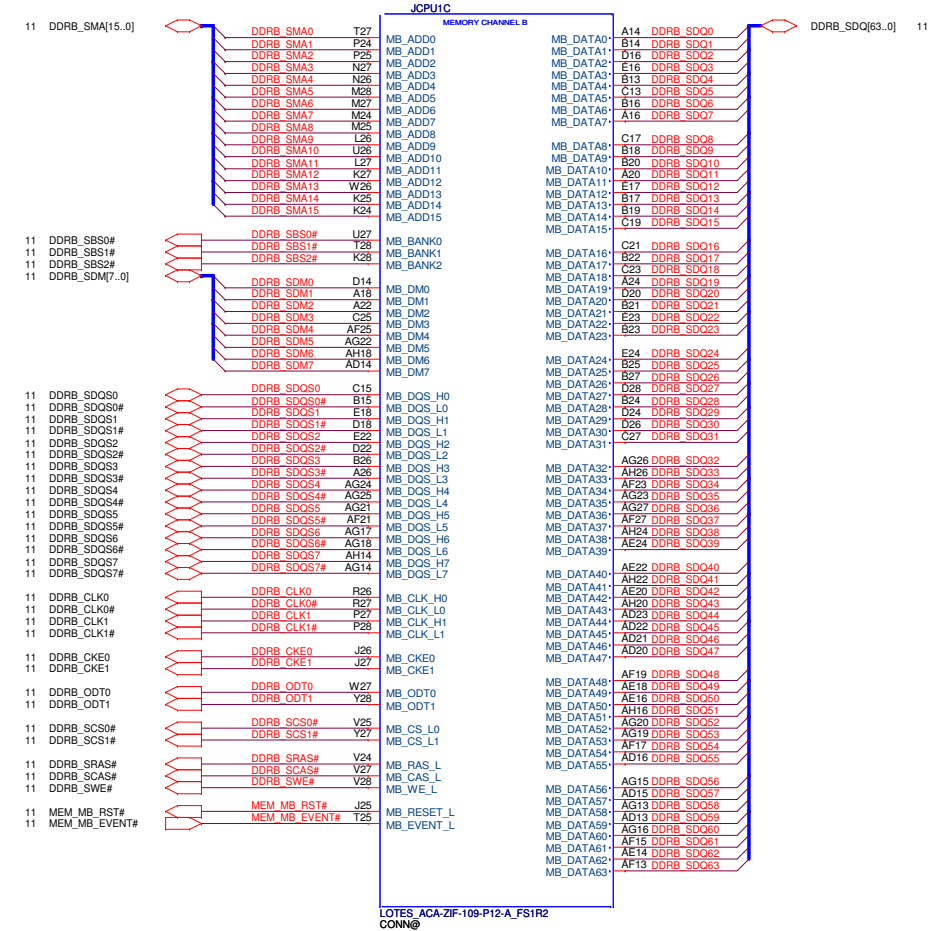
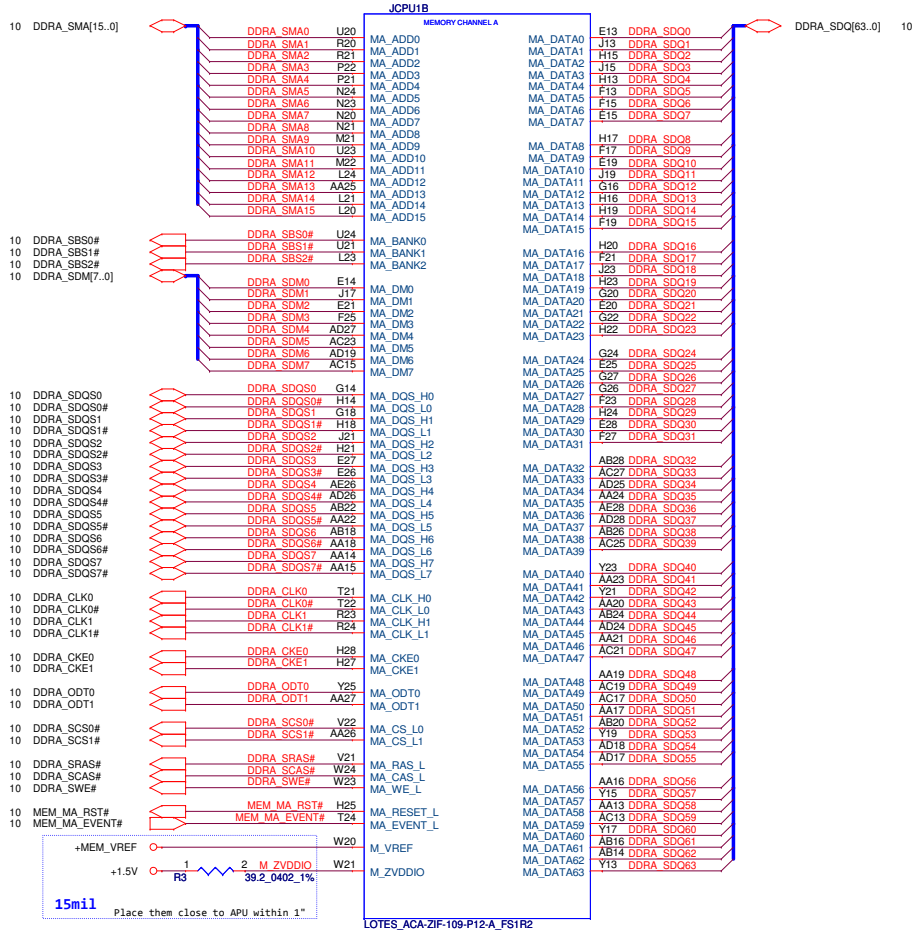
PCIE\_CTX\_GRX\_P0[0..15]  
PCIE\_CTX\_GRX\_N0[0..15]



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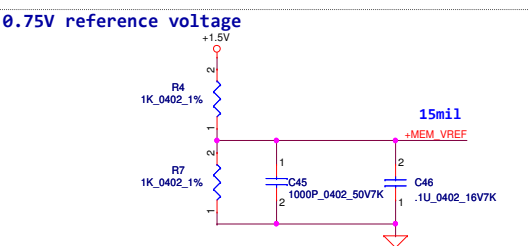
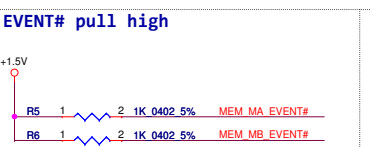
**FS1r2 PCIE/UMI**

**LA-8121P**

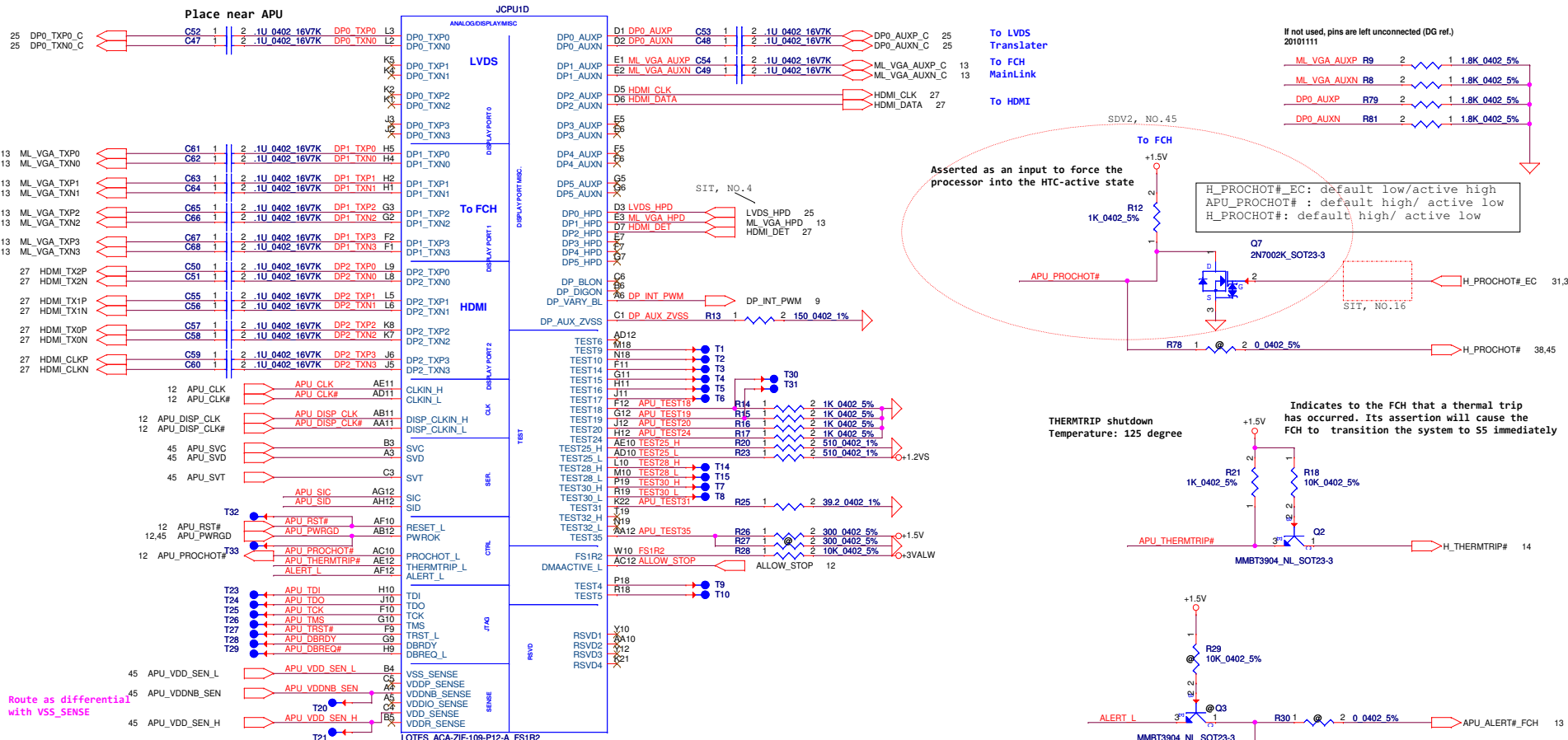


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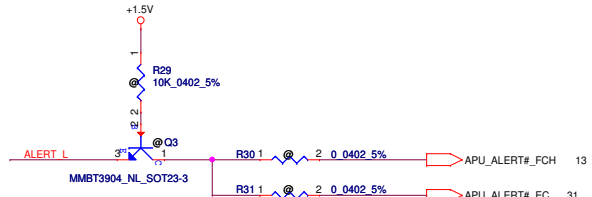
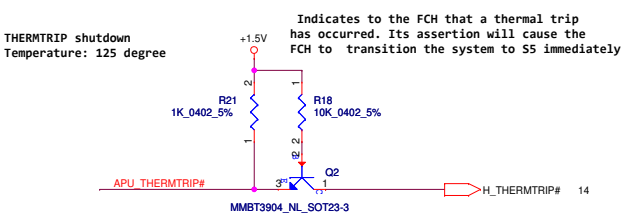
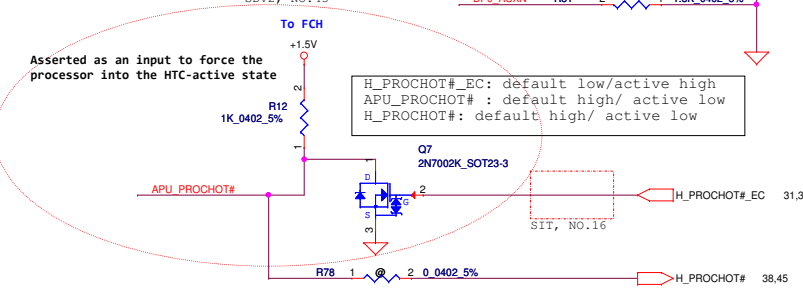
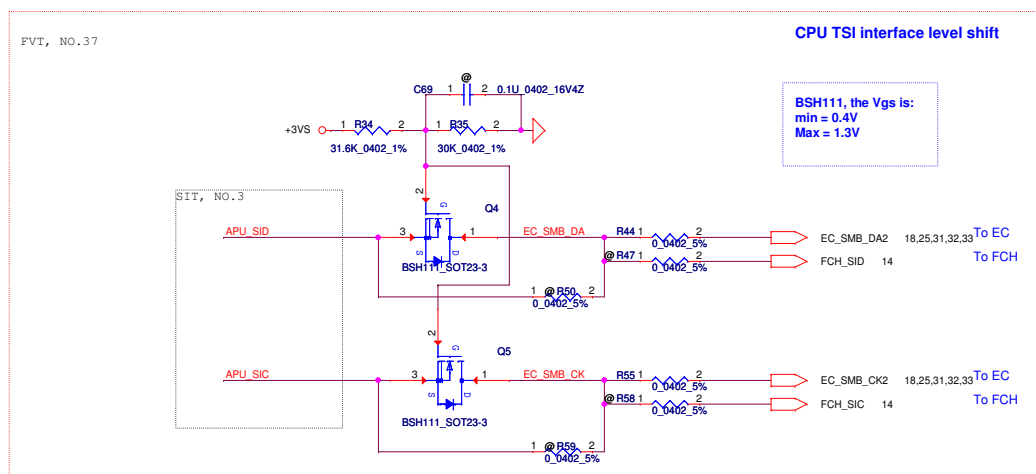
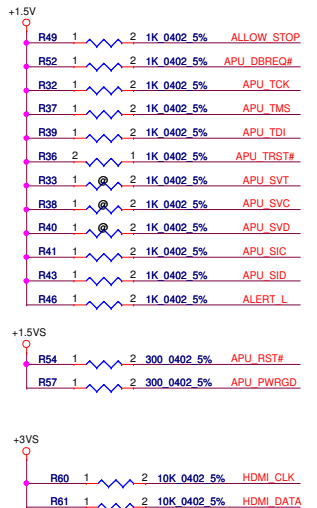
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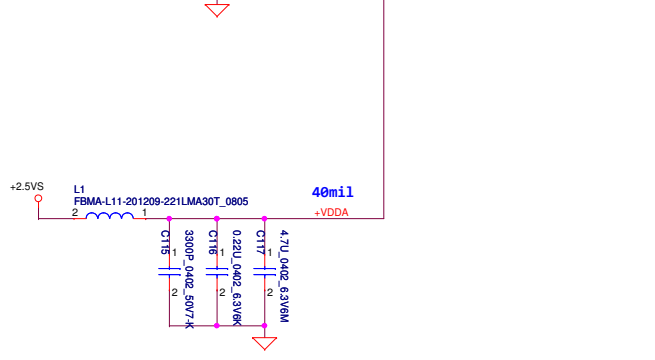
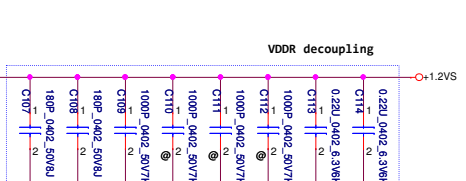
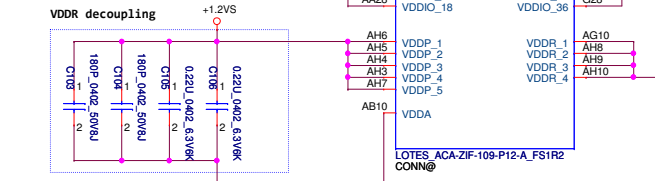
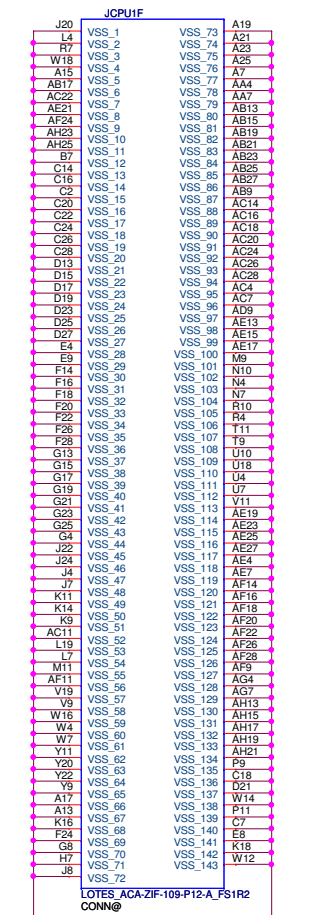
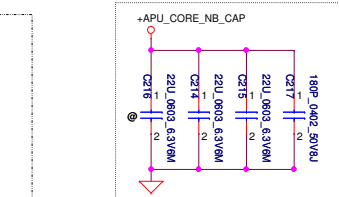
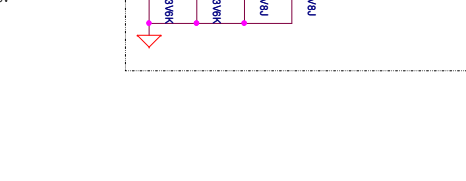
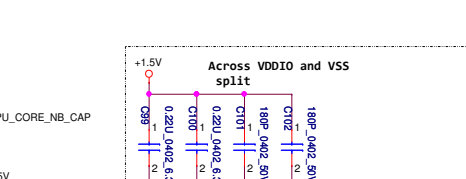
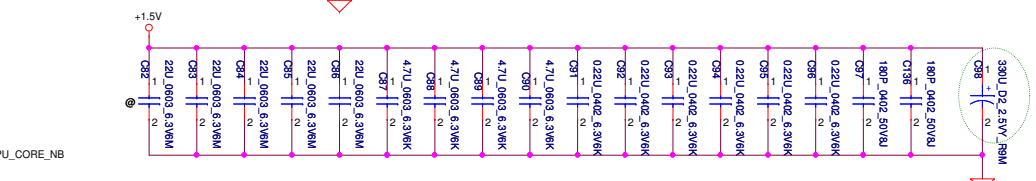
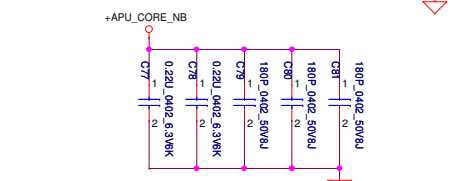
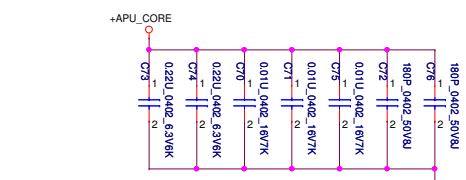
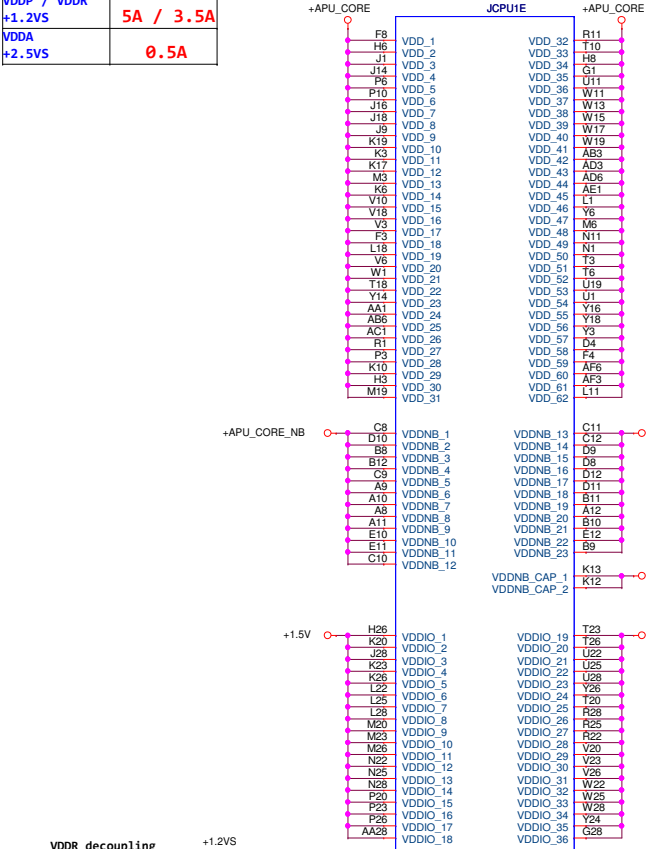


Route as differential with VSS\_SENSE



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Power Name	Consumption
VDD +APU_CORE	60A
VDDNB +APU_CORE_NB	44A
VDDIO +1.5V	3.2A
VDDP / VDDR +1.2VS	5A / 3.5A
VDDA +2.5VS	0.5A



### Demo Board Capacitor

APU_CORE	CORE_NB	CORE_NB_CAP	VDDIO_SUS
22uF x 10	22uF x 2	22uF x 2	(CPU side)
0.22uF x 2	10uF x 1	180pF x 1	22uF x 4
0.01uF x 3	0.22uF x 2		4.7uF x 4
180pF x 2	180pF x 3		0.22uF x 6 + 2(split)
			180pF x 1 + 2(split)

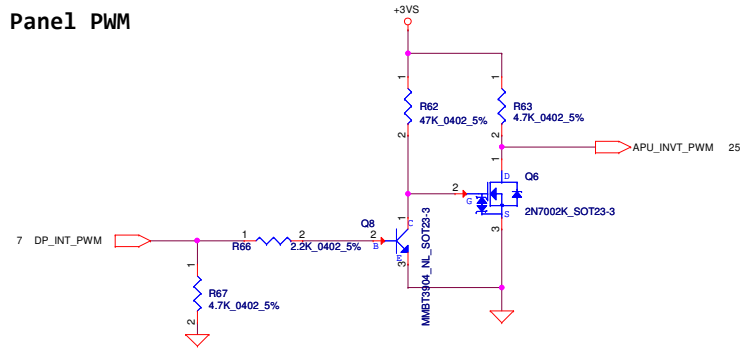
  

VDDP	VDDR	VDDA	VDDIO_SUS
0.22uF x 2	0.22uF x 2	4.7uF x 1	(DIMM x2)
180pF x 2	1nF x 4	0.22uF x 1	100uF x 2
	180pF x 2	3.3nF x 1	0.1uF x 12



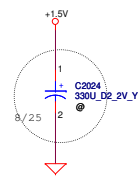
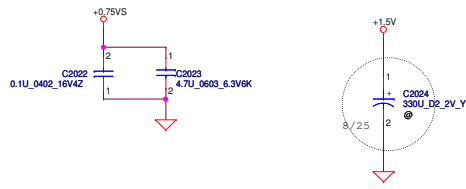
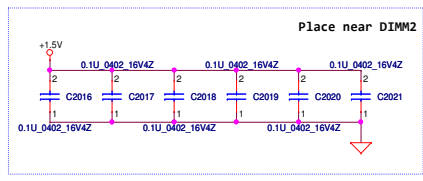
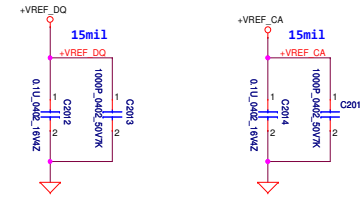
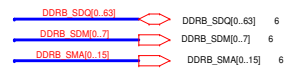
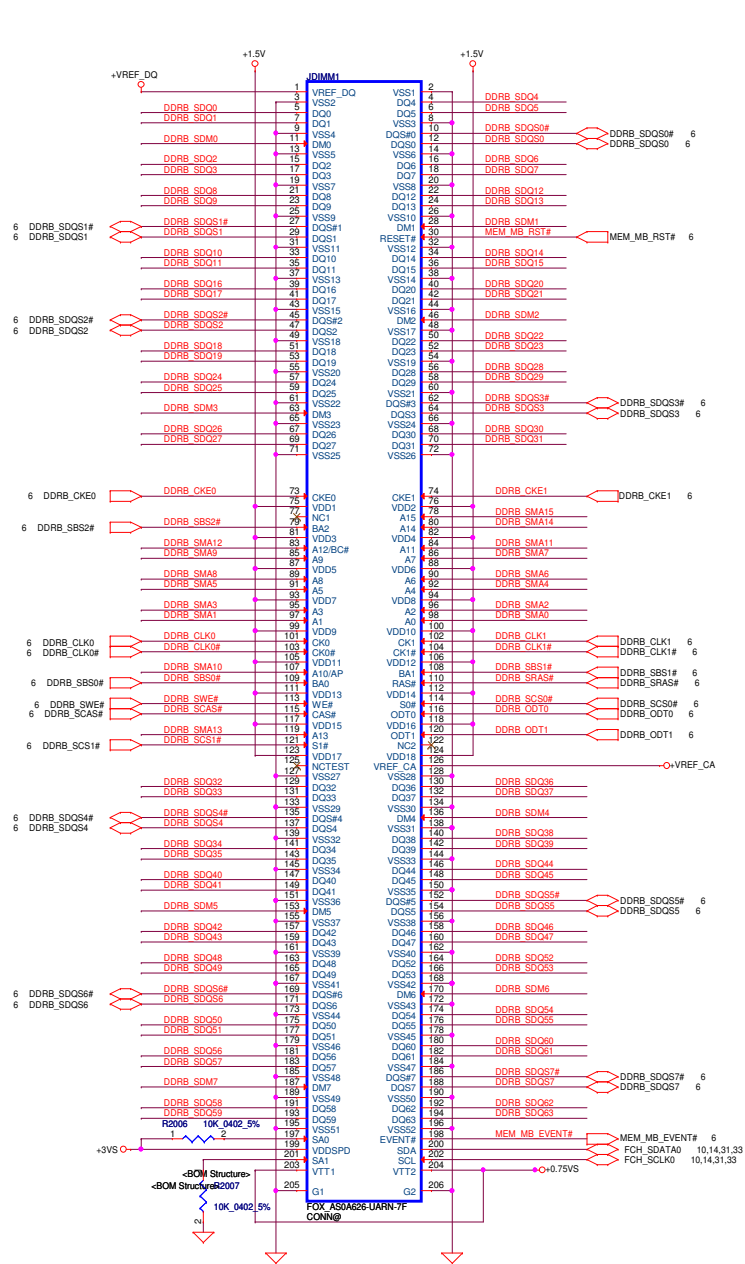
**HPD**  
SIT, NO.4

**Panel PWM**



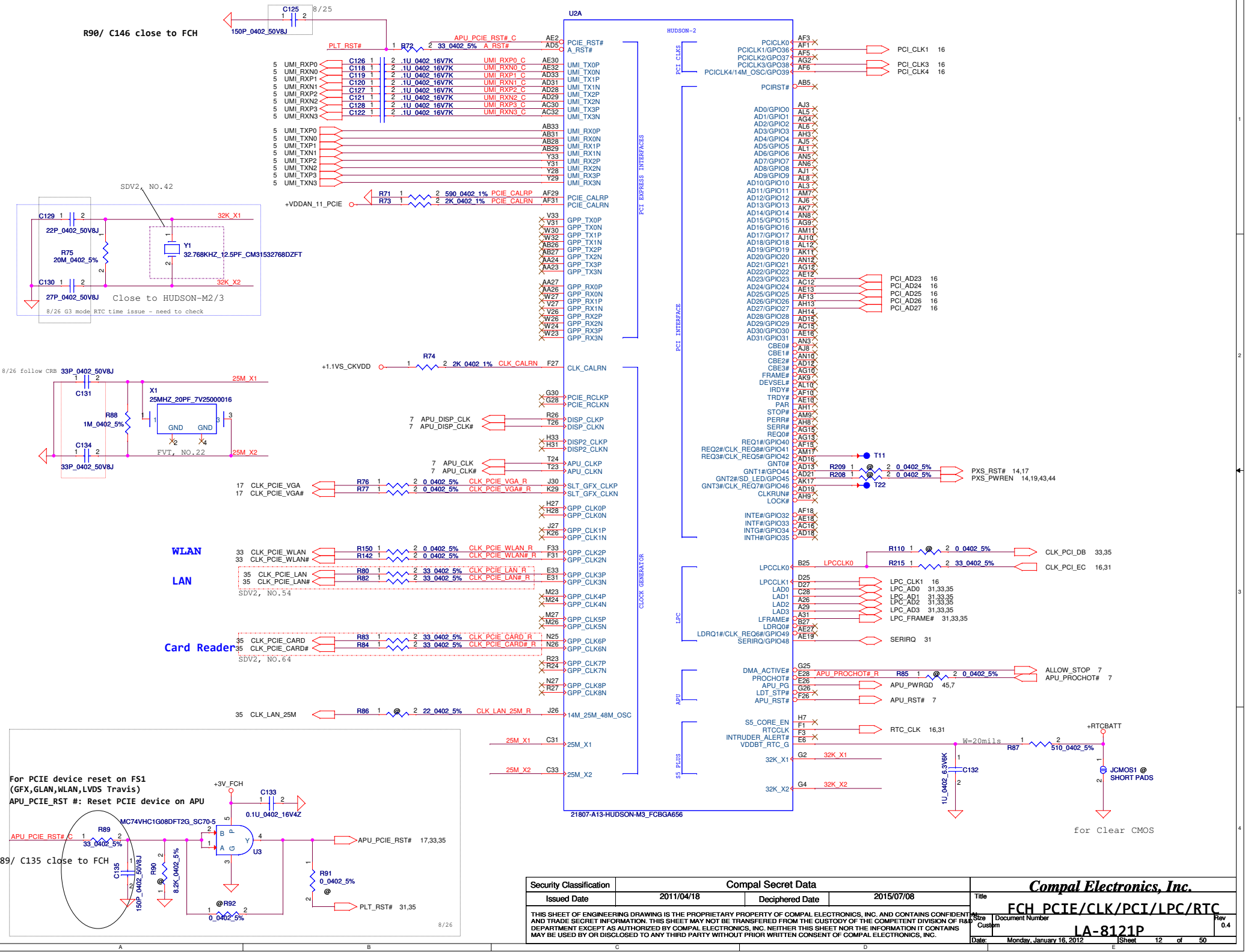
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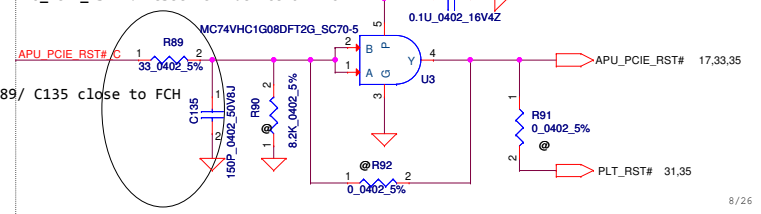


Reverse H: 9.2mm

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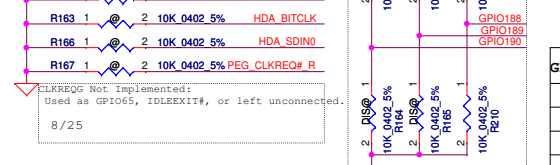
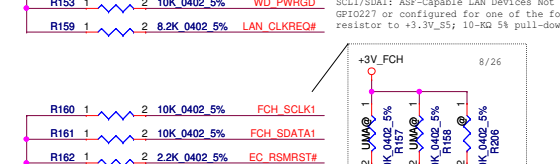
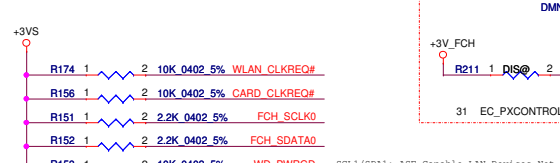
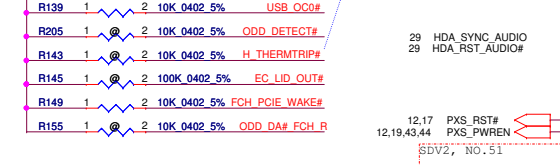
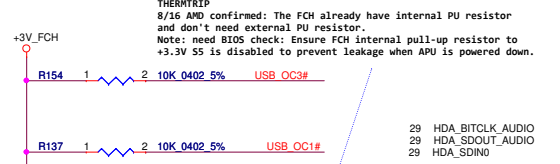
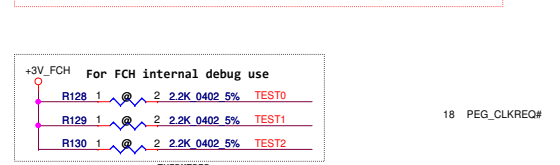
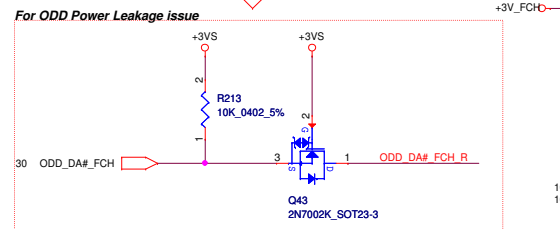
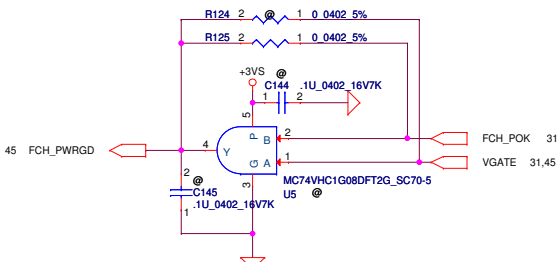


For PCIe device reset on F51 (GFX, GLAN, WLAN, LVDS Travis)  
 APU\_PCIE\_RST #: Reset PCIe device on APU

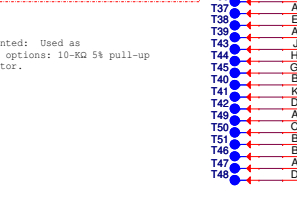
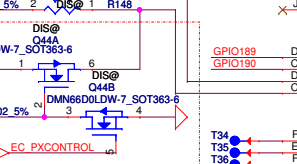
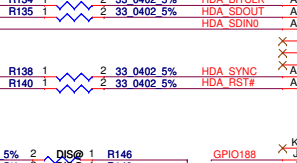
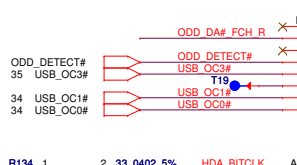
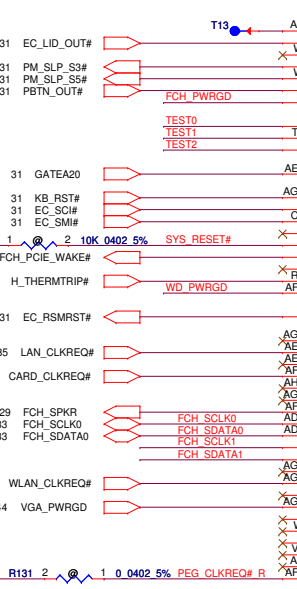


Security Classification	Compal Secret Data		2015/07/08		Title	
Issued Date	2011/04/18	Deciphered Date			FCH PCIe/CLK/PCI/LPC/RTC	
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Size	Document Number	Customer	LA-8121P		Rev	0.4
Date:	Monday, January 16, 2012	Sheet	12	of	50	



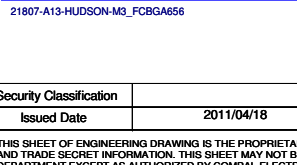
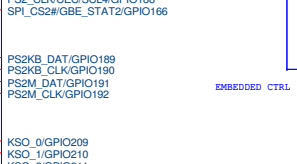
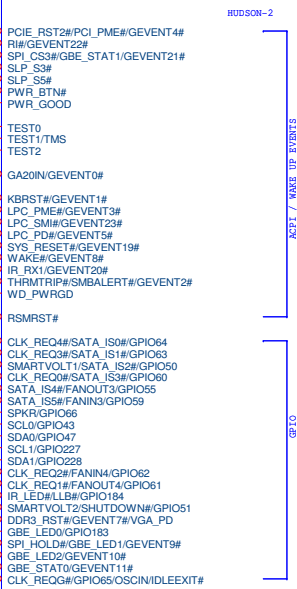


**PCIE\_RST2 : Reset PCIE device on Hudson2/3**

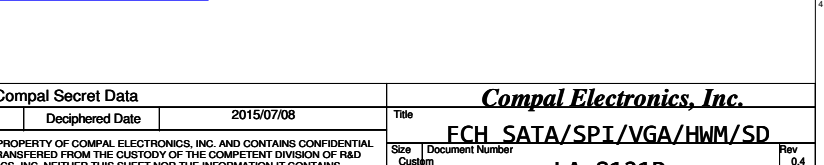
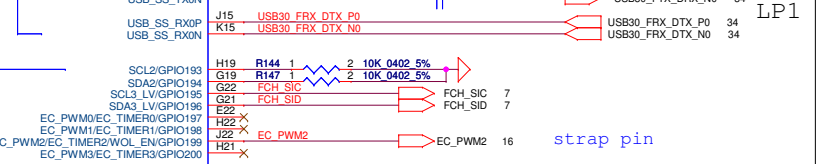
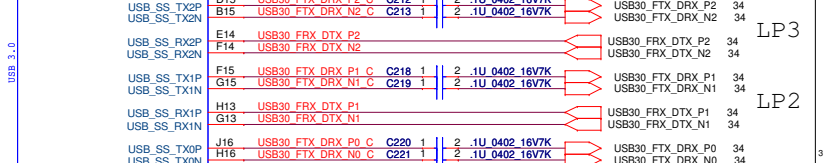
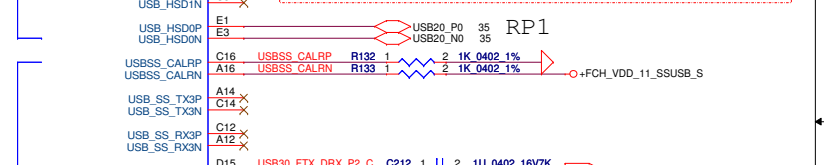
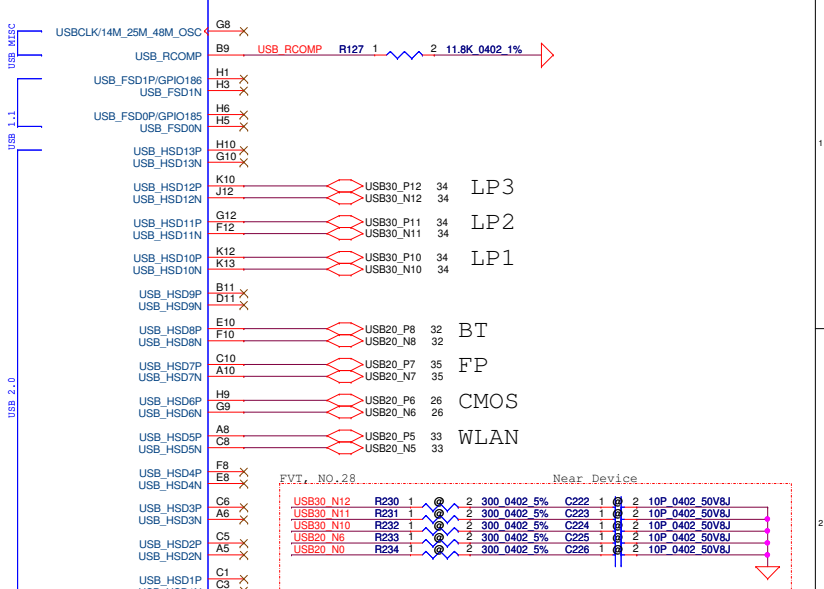


GPIO188	GPIO189	GPIO190	Function
0	0	0	PX
0	0	1	Reserved
0	1	0	DISCRET
0	1	1	UMA

**U2D**



**HUDSON-2**



GPIO188	GPIO189	GPIO190	Function
0	0	0	PX
0	0	1	Reserved
0	1	0	DISCRET
0	1	1	UMA

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**Compal Electronics, Inc.**  
**FCH SATA/SPI/VGA/HWM/SD**  
**LA-8121P**  
 Title: FCH SATA/SPI/VGA/HWM/SD  
 Size: Custom  
 Document Number: LA-8121P  
 Rev: 0.4  
 Date: Monday, January 16, 2012 14 of 50



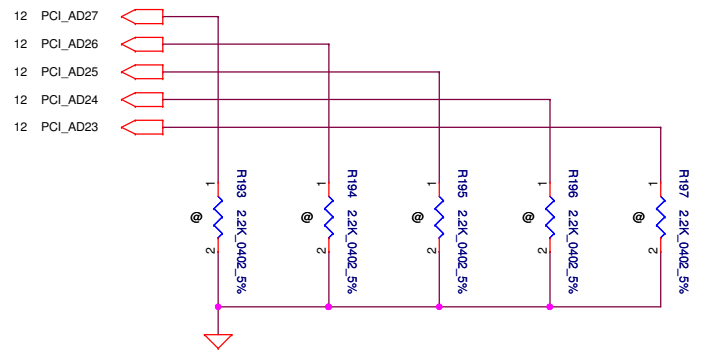
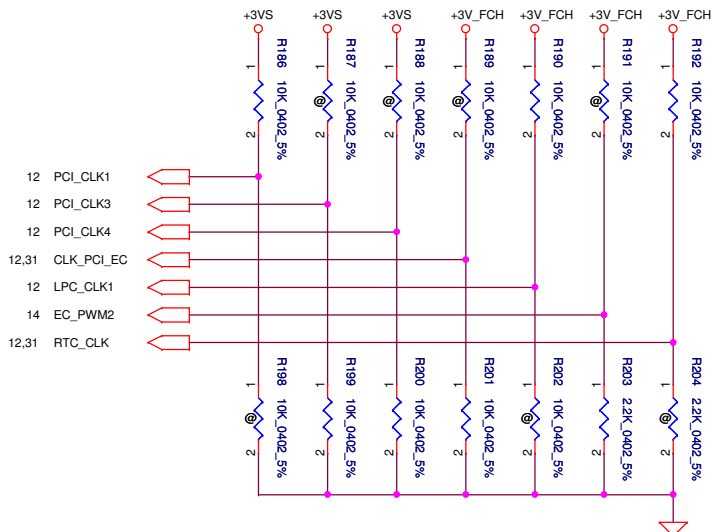
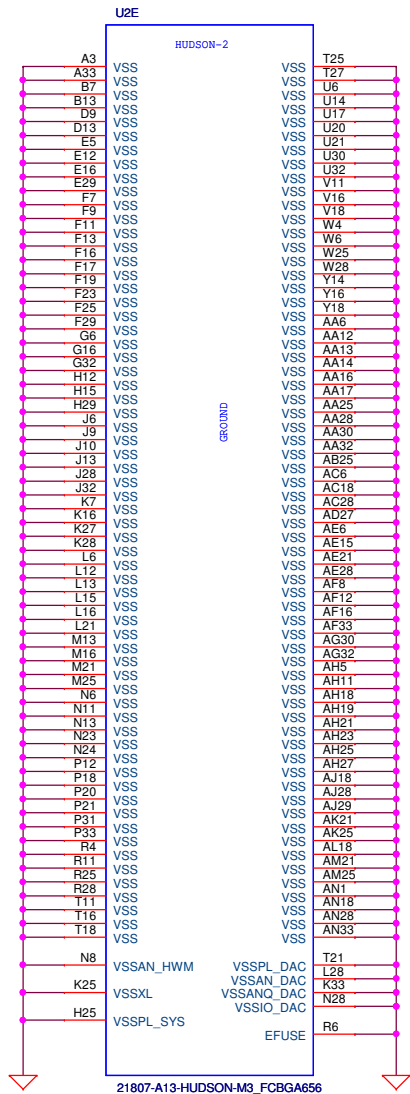
# STRAP PINS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
<b>PULL HIGH</b>	ALLOW PCIE GEN2 <i>DEFAULT</i>	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED	LPC ROM	S5 PLUS MODE DISABLED <i>DEFAULT</i>
<b>PULL LOW</b>	FORCE PCIE GEN1	IGNORE DEBUG STRAP <i>DEFAULT</i>	FUSION CLOCK MODE <i>DEFAULT</i>	EC DISABLED <i>DEFAULT</i>	CLKGEN DISABLE	SPI ROM <i>DEFAULT</i>	S5 PLUS MODE ENABLED

# DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

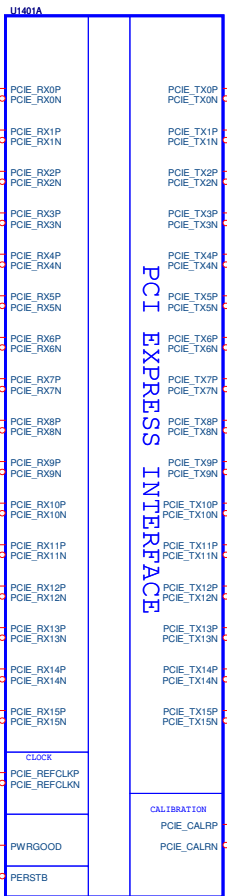
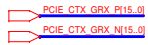
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE PCI PLL <i>DEFAULT</i>	DISABLE ILA AUTORUN <i>DEFAULT</i>	USE FC PLL <i>DEFAULT</i>	USE DEFAULT PCIE STRAPS <i>DEFAULT</i>	DISABLE PCI MEM BOOT <i>DEFAULT</i>
<b>PULL LOW</b>	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



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Issued Date	2011/04/18	Deciphered Date	2015/07/08		
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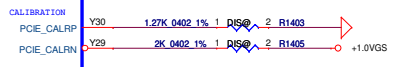


5 PCIE\_CTX\_GRX\_P[15..0]  
5 PCIE\_CTX\_GRX\_N[15..0]

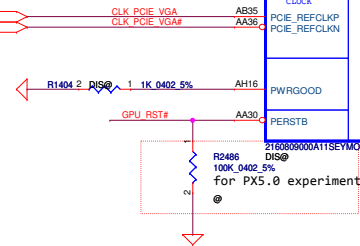


PCIE\_CRX\_GTX\_P[15..0]  
PCIE\_CRX\_GTX\_N[15..0]

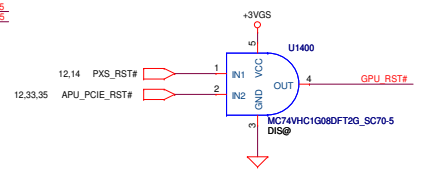
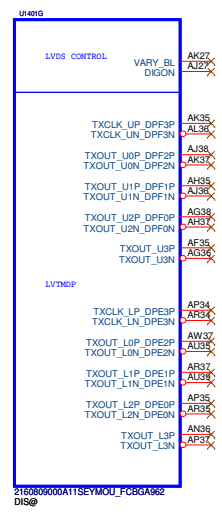
PCI EXPRESS INTERFACE



12 CLK\_PCIE\_VGA  
12 CLK\_PCIE\_VGA#



LVDS Interface

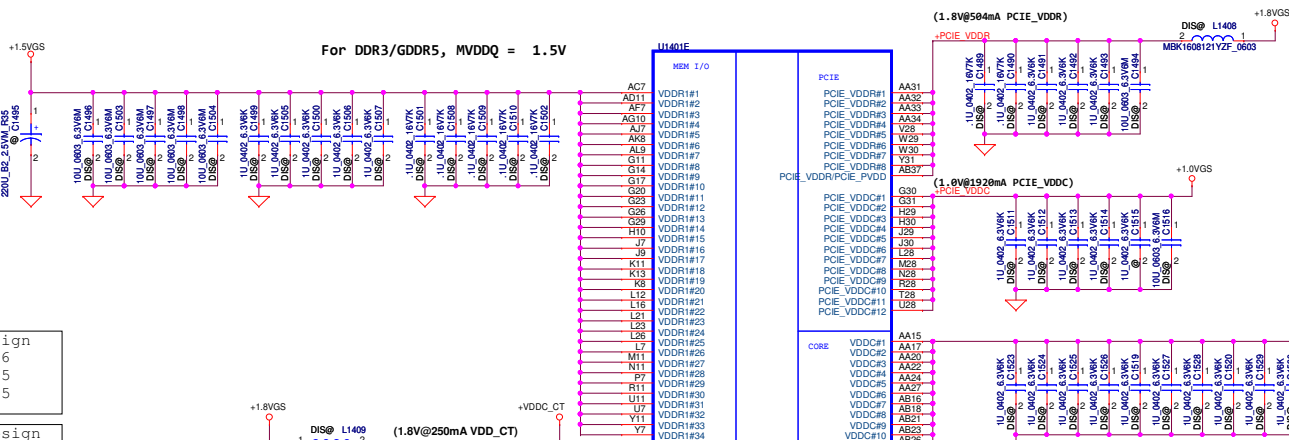








For DDR3/GDDR5, MVDDQ = 1.5V



VDD1	CRB	Design
0.1u	11	6
1u	10	5
10u	6	5

VDD_CT	CRB	Design
0.1u	1	1
1u	3	3
10u	1	1

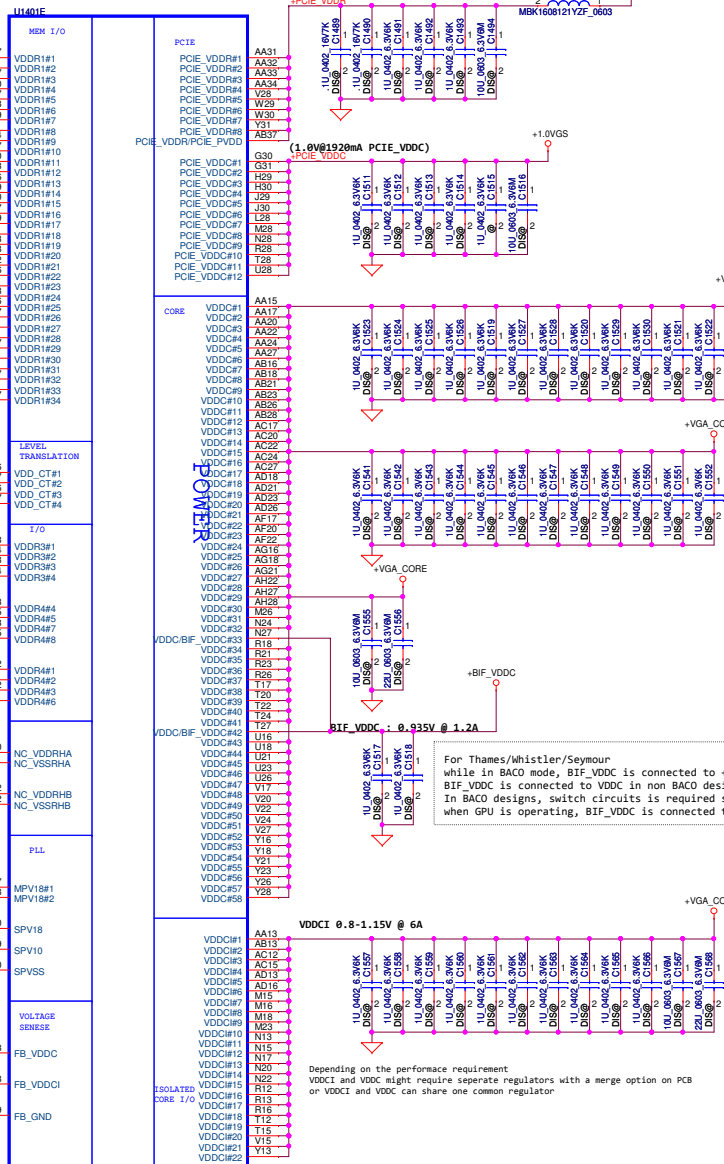
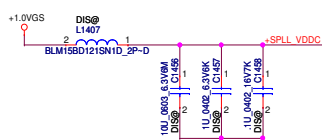
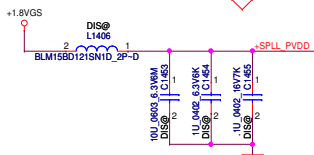
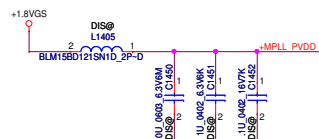
VDD3	CRB	Design
1u	3	3
10u	1	1

VDD4	CRB	Design
0.1u	2	1
1u	2	1
10u	2	0

MPV18	CRB	Design
0.1u	2	1
1u	2	1
10u	1	1

SPV18	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1

SPV10	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1



PCIE_VDDR	CRB	Design
0.01u	1	0
0.1u	1	2
1u	3 (2@)	3
10u	1	1

PCIE_VDDC	CRB	Design
0.1u	3	0
1u	10	5 (1@)
10u	2	1

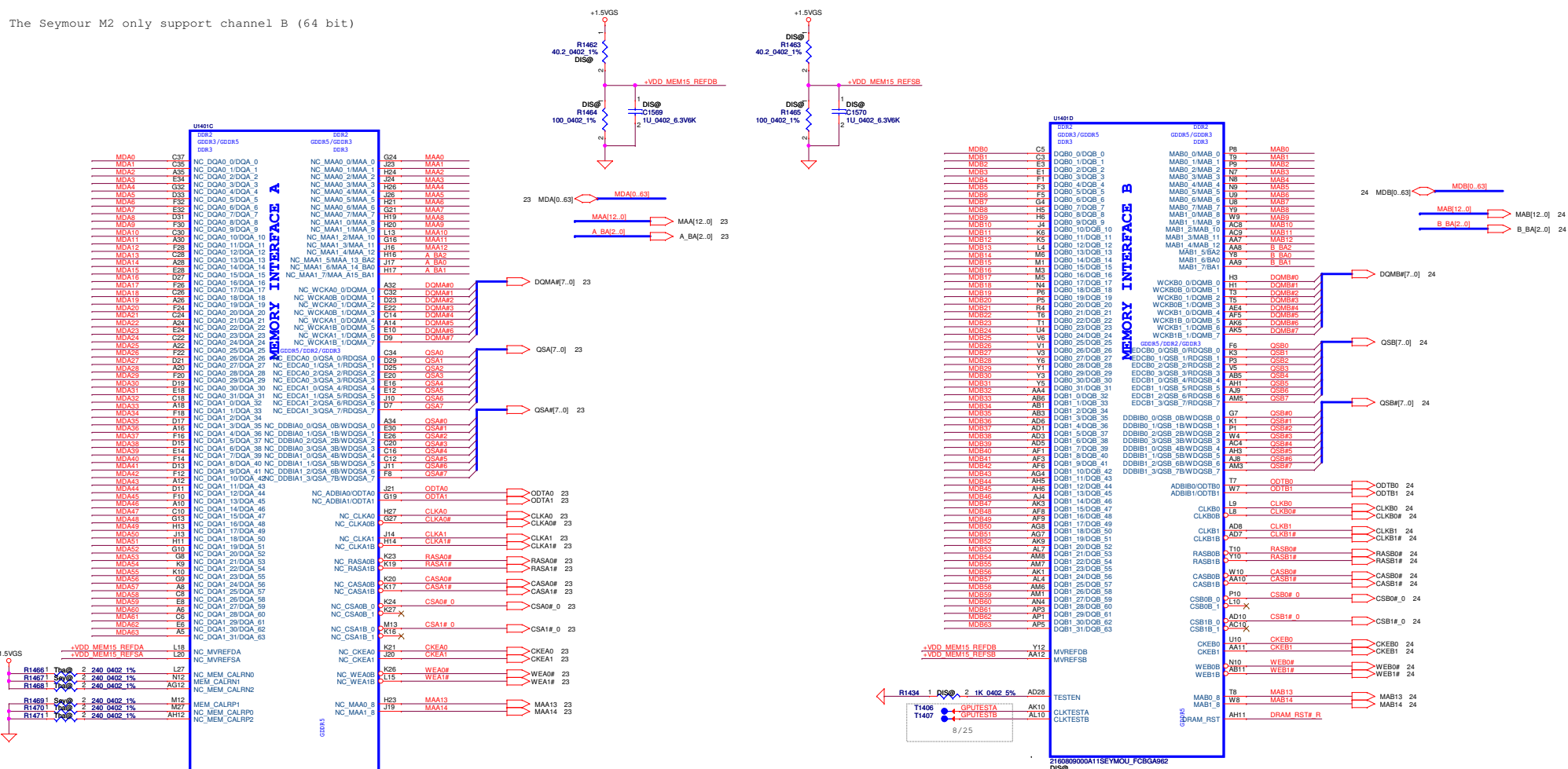
+BIF_VDDC	CRB	Design
1u	2	2
10u	1	0

VDDC	CRB	Design
1u	30	25
10u	9	1
22u	0	1

VDDCI	CRB	Design
1u	10	9
10u	3	2
22u	0	1

For Thames/Whistler/Seymour while in BACO mode, BIF\_VDDC is connected to +1.8V BIF\_VDDC is connected to VDDC in non BACO designs. In BACO designs, switch circuits is required so that when GPU is operating, BIF\_VDDC is connected to VDDC

Depending on the performance requirement VDDCI and VDDC might require separate regulators with a merge option on PCB or VDDCI and VDDC can share one common regulator



Themes XT	Seymour XT
R1466	POP @
R1467	@ POP
R1468	POP @
R1469	@ POP
R1470	POP @
R1471	POP @

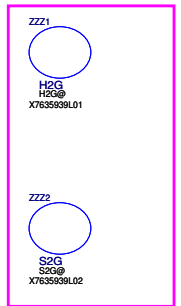
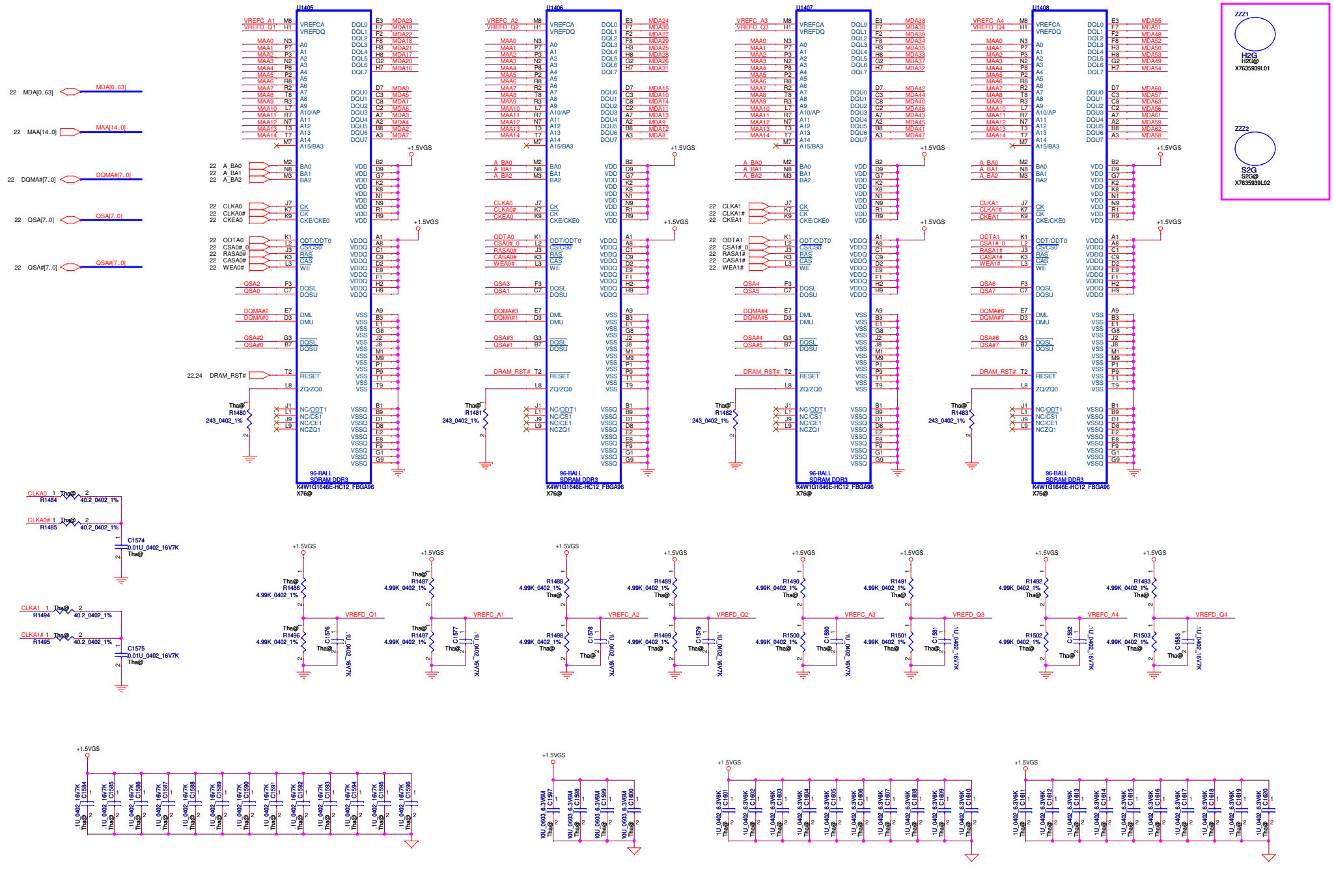
Place all these components very close to GPU (within 25mm) and keep all components close to each other  
 \*\* This basic topology should be used for DRAM\_RST for DR3/GDR5

These Capacitors and Resistor values are an example only  
 The series R and || cap values will depend on the DRAM loads and will have to be calculated for different Memory.  
 DRAM Loads and board to pass Reset Signal Spec



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The Seymour M2 only support channel B (64 bit),  
 this page unmount all parts



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Title		<b>Compal Electronics, Inc.</b> <b>ATI Themes XT_M2_VRAM_A</b>	
Size	Document Number	Rev	
	IA-8121P	0.4	
Date	Monday, January 16, 2012	Sheet	23 of 50

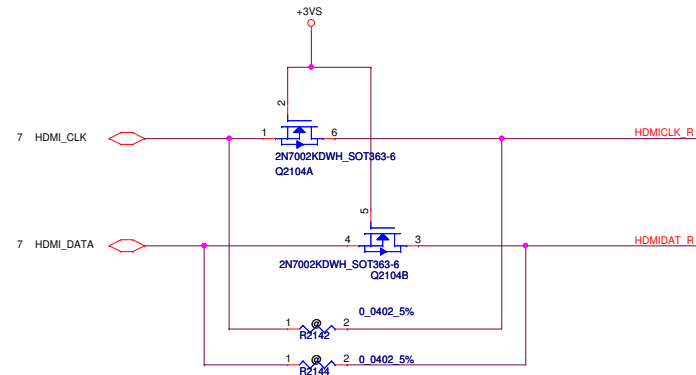
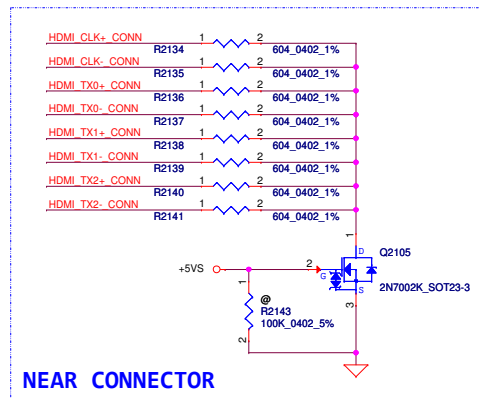
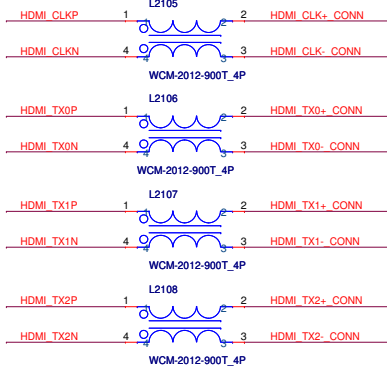




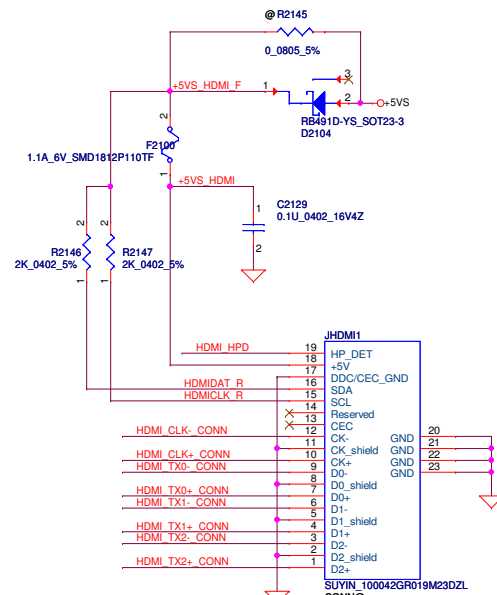
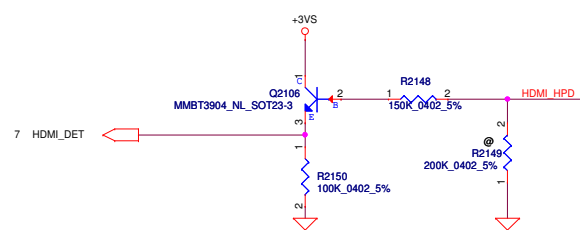
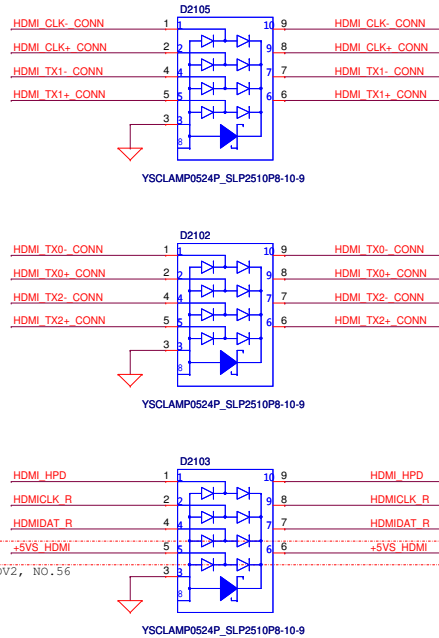




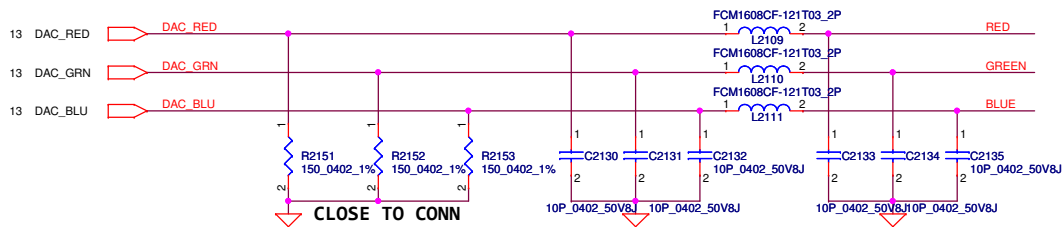
FVT_...NO.5						
7	HDMI_CLKP	R2126	1	2	0.0402_5%	HDMI_CLK+_CONN
7	HDMI_CLKN	R2127	1	2	0.0402_5%	HDMI_CLK-_CONN
7	HDMI_TX0P	R2128	1	2	0.0402_5%	HDMI_TX0+_CONN
7	HDMI_TX0N	R2129	1	2	0.0402_5%	HDMI_TX0-_CONN
7	HDMI_TX1P	R2130	1	2	0.0402_5%	HDMI_TX1+_CONN
7	HDMI_TX1N	R2131	1	2	0.0402_5%	HDMI_TX1-_CONN
7	HDMI_TX2P	R2132	1	2	0.0402_5%	HDMI_TX2+_CONN
7	HDMI_TX2N	R2133	1	2	0.0402_5%	HDMI_TX2-_CONN



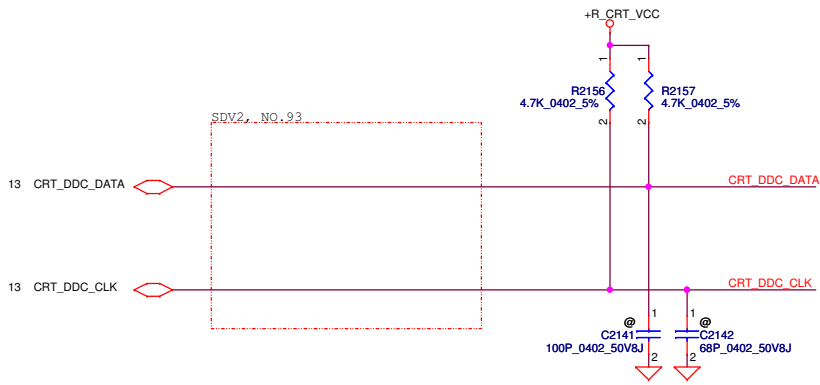
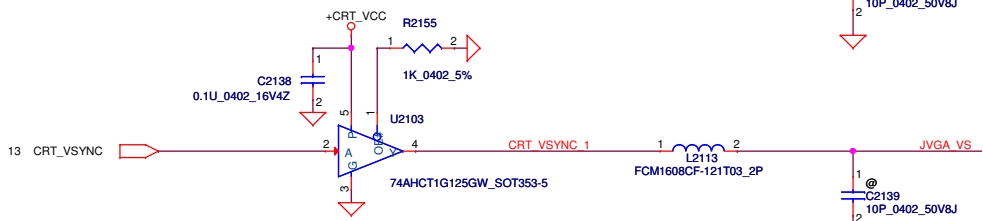
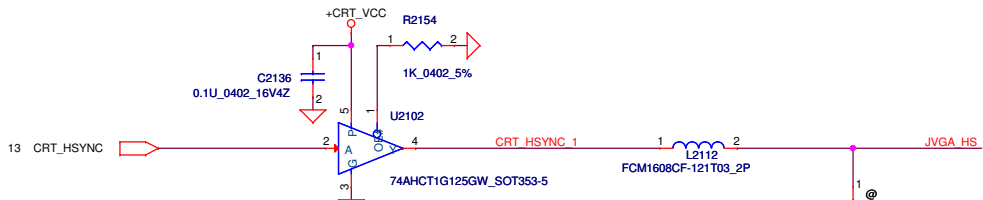
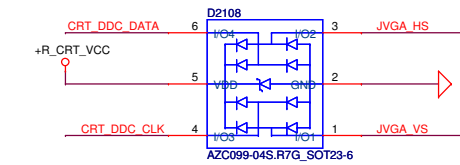
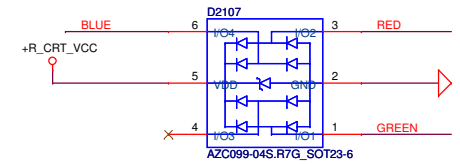
### ESD Request 2011.08.13



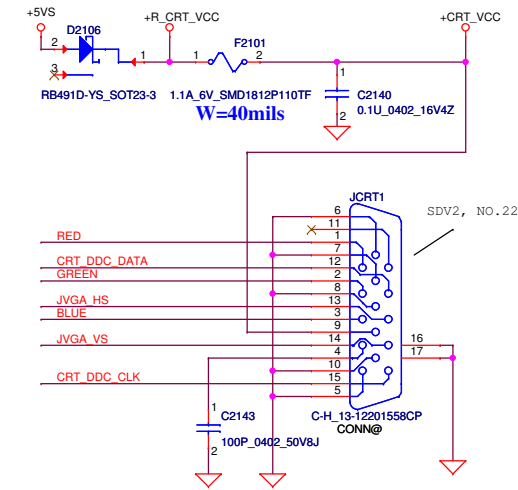
Security Classification	Compal Secret Data		Title	<b>Compal Electronics, Inc.</b>	
Issued Date	2011/04/18	Deciphered Date	2015/07/08	HDMI Connector	
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### ESD Request 2011.08.13



### CRT Connector

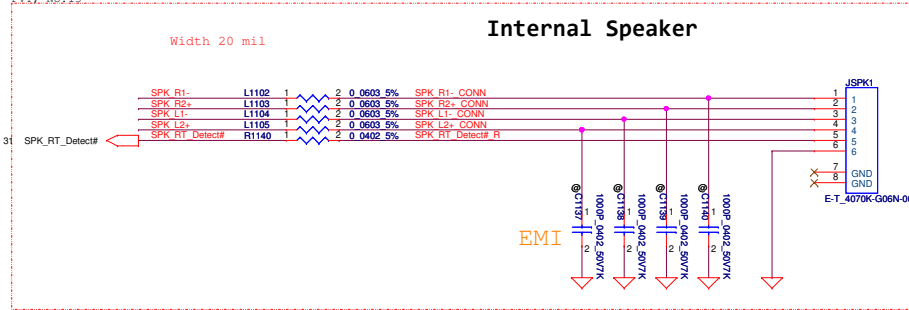
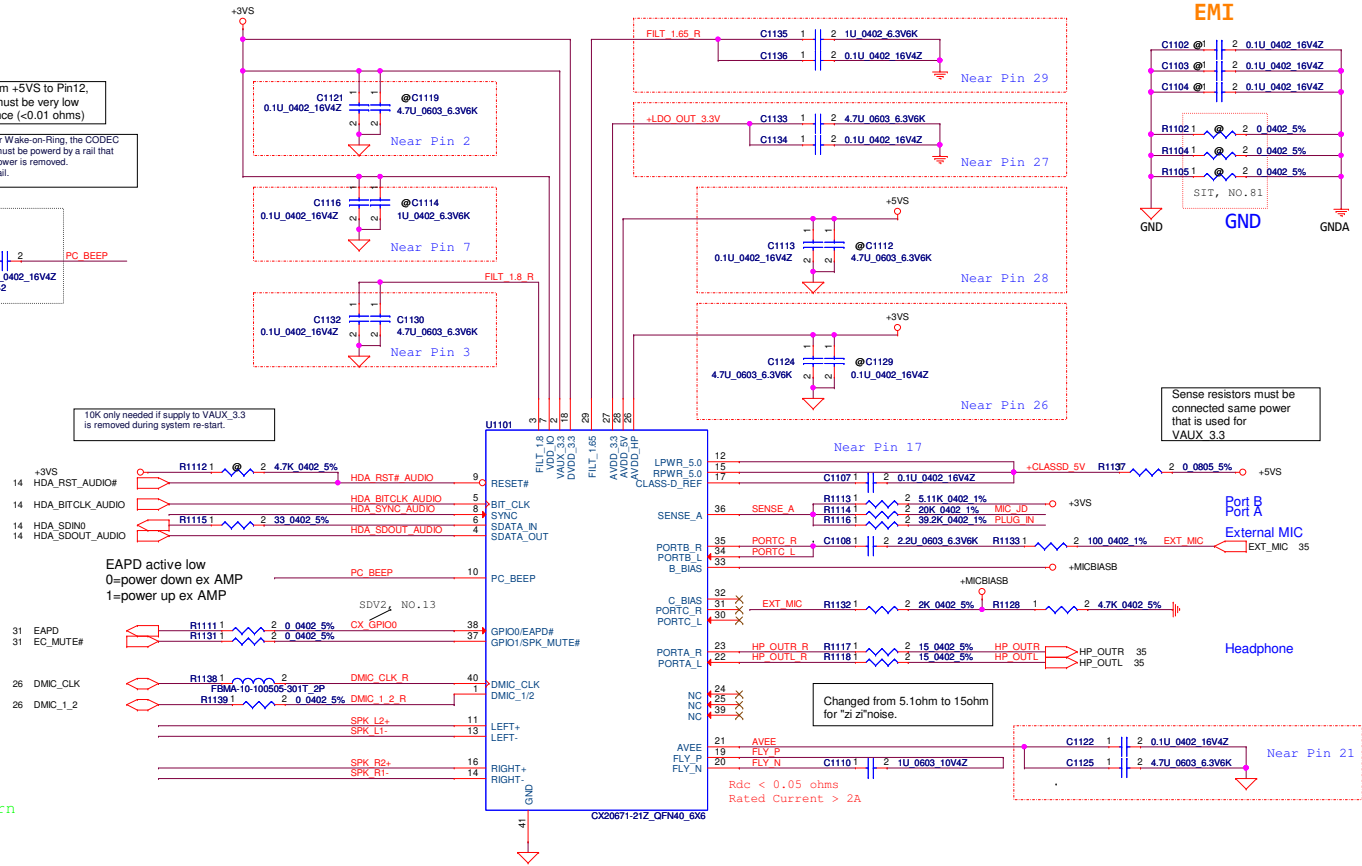
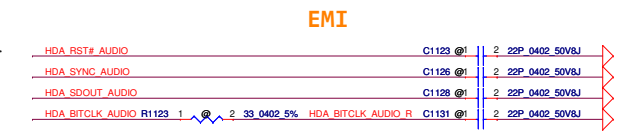
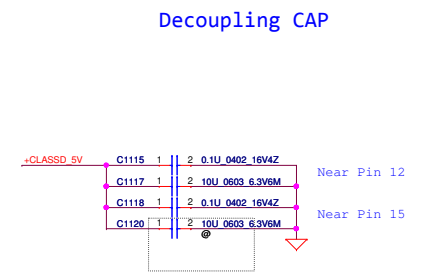
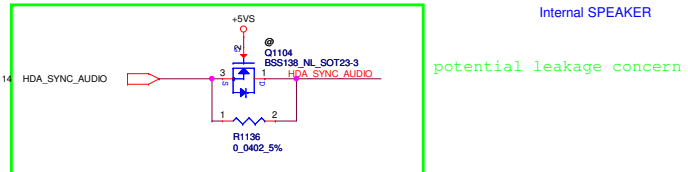
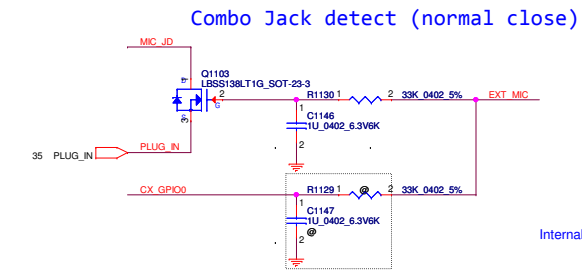
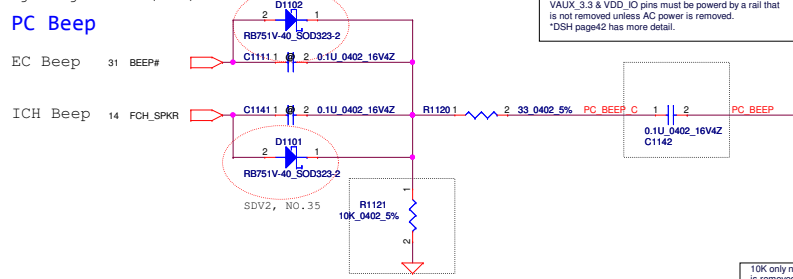


AMD check list update  
20101110

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CX20671  
 High Definition Audio Codec SoC  
 With Integrated Class-D Stereo  
 Amplifier.  
 An integrated 5 V to 3.3 V Low-dropout  
 voltage regulator (LDO).  
 An integrated 3.3 V to 1.8V Low-dropout  
 voltage regulator (LDO).

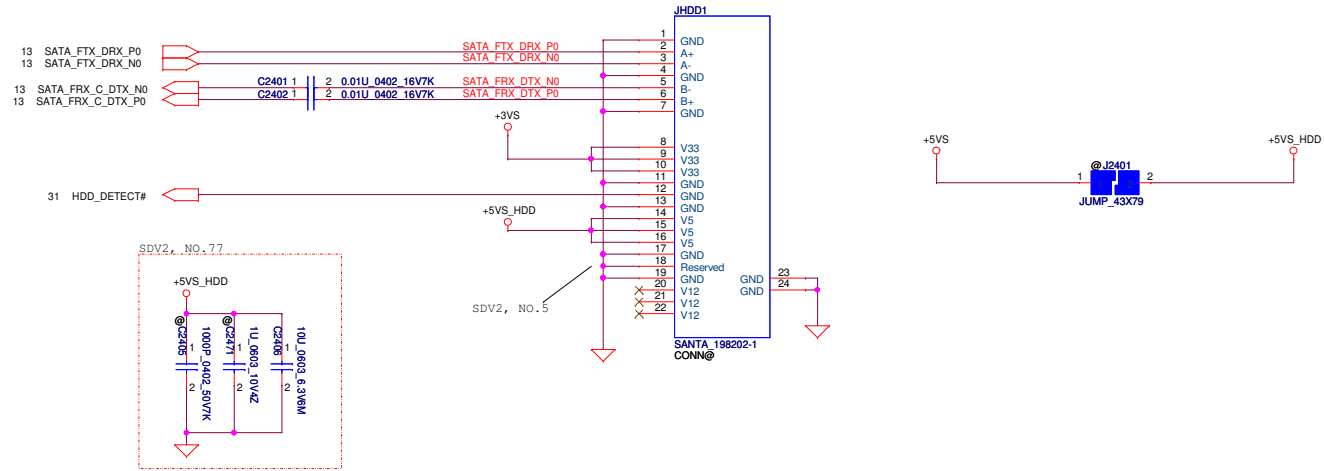
Layout Note: Path from +5VS to Pin12,  
 \*Pin15 must be very low  
 resistance (<0.01 ohms)  
 To support Wake-on-Jack or Wake-on-Ring, the CODEC  
 VAUX\_3.3 & VDD\_IQ pins must be powered by a rail that  
 is not removed unless AC power is removed.  
 \*DSH page42 has more detail.



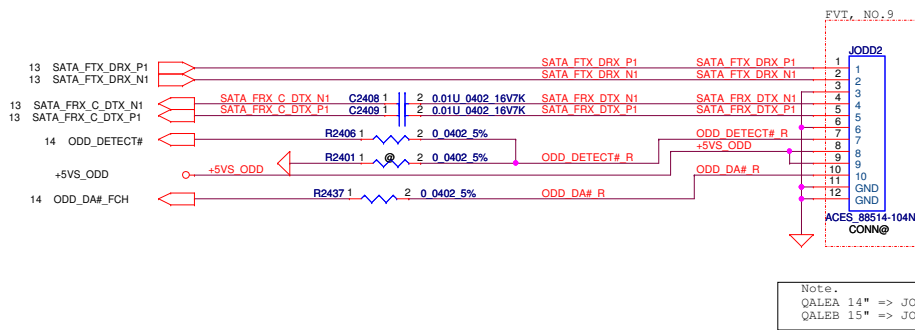
Note.  
 QALEA 14" => JSPK1 => 4Pin  
 QALEA 15" => JSPK1 => 6Pin

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Document Number	LA-8121P	Rev	0.4	Date: Monday, January 16, 2012
Sheet	29	of	50	

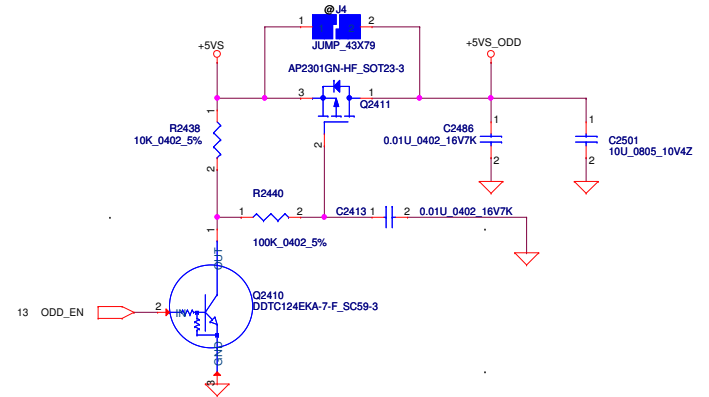
### SATA HDD Conn.



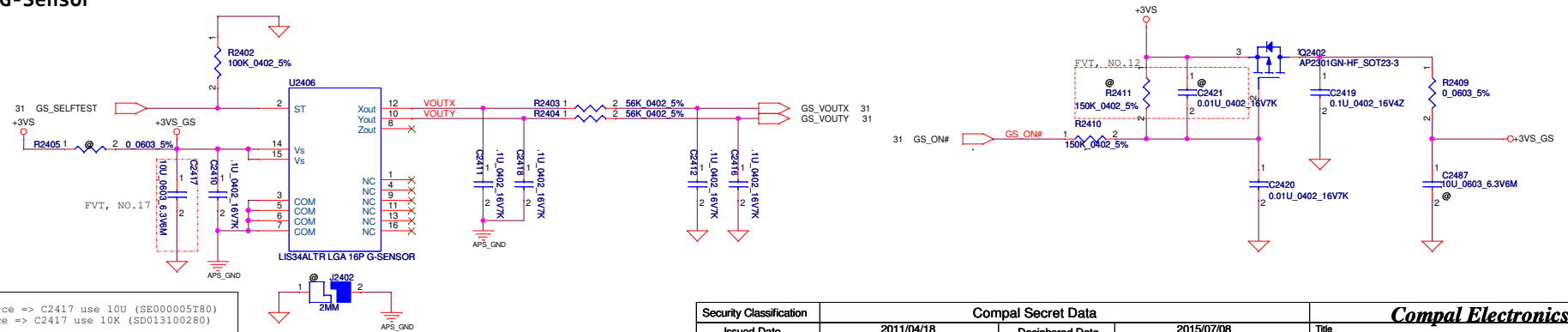
### SATA ODD Conn.



### ODD Power Control



### APS G-Sensor

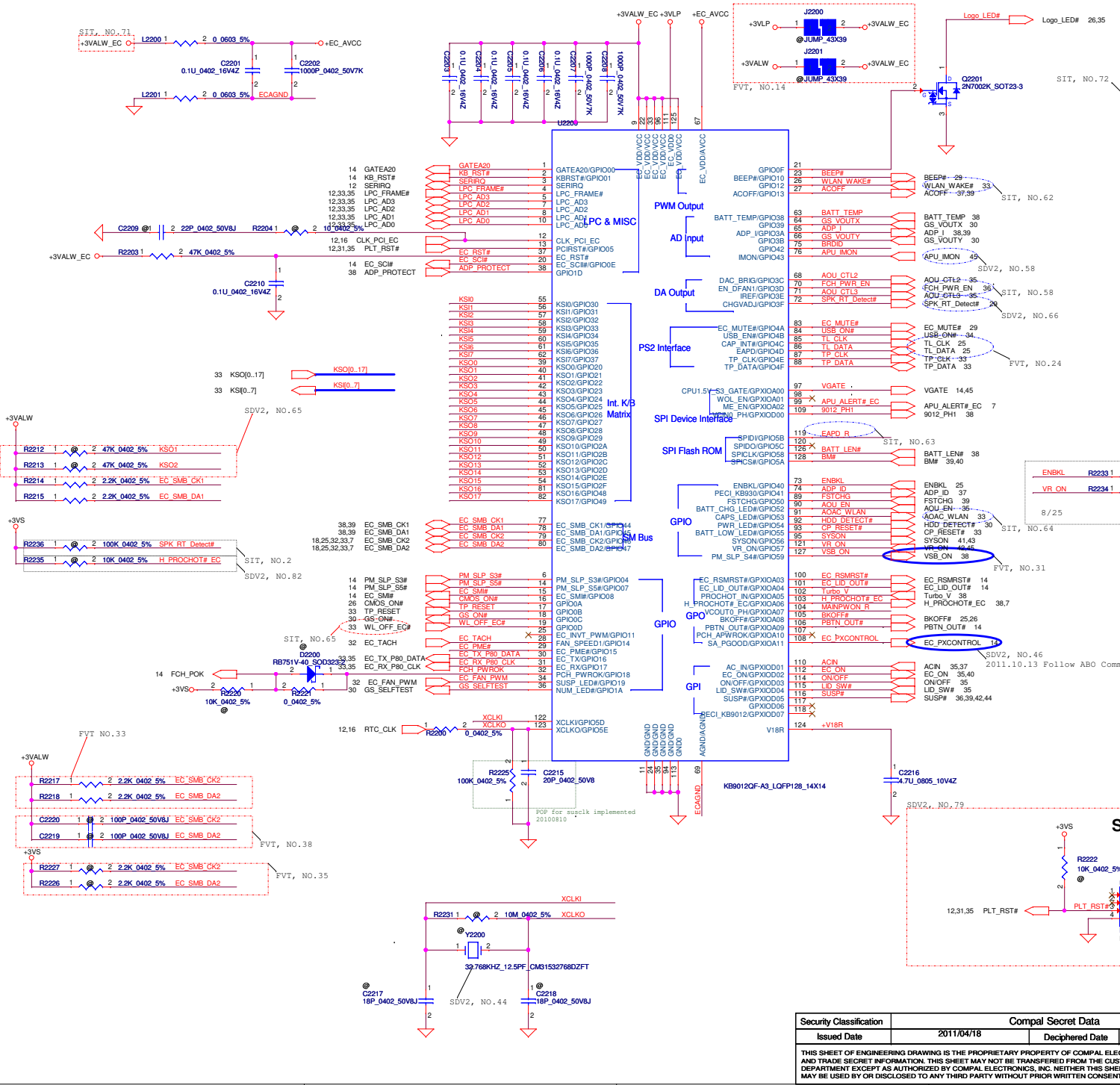


Note.  
Main Source => C2417 use 10U (SE000005T80)  
2nd Source => C2417 use 10K (SD013100280)

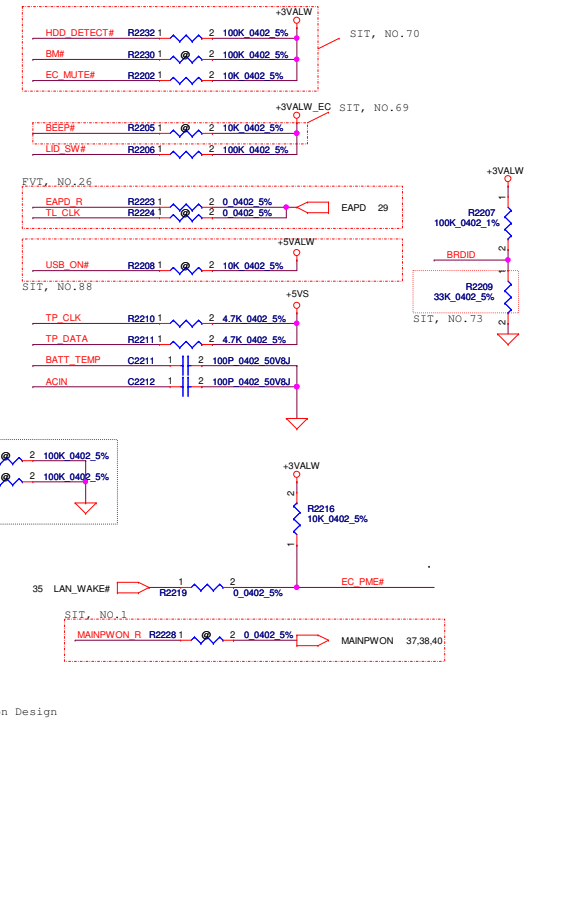
Security Classification		Compal Secret Data		Title	
Issued Date	2011/04/18	Deciphered Date	2015/07/08	HDD/ODD/G-Sensor	
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Size	Document Number	Date		Monday, January 16, 2012	Sheet 30 of 50
B	LA-8124P				Rev 0.4

Compal Electronics, Inc.

LA-8124P

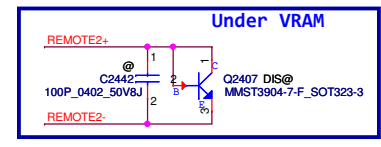
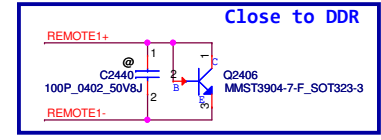
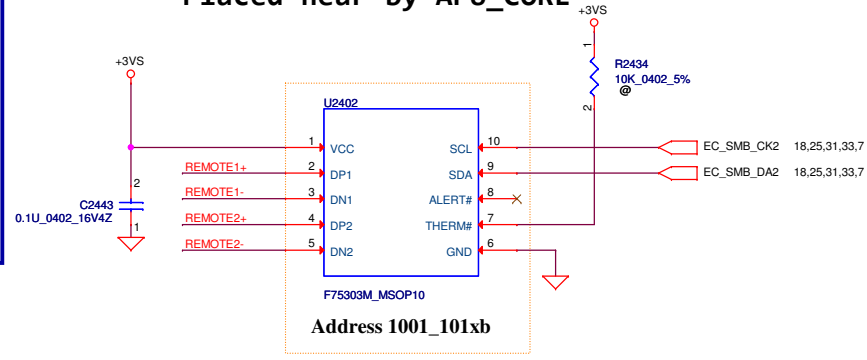
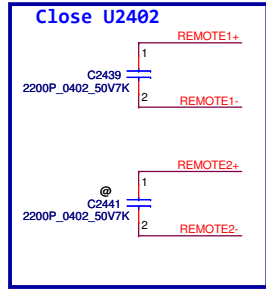


Vcc	3.3V +/- 5%				
R2207	100K +/- 5%				
Board ID	R2209	VAD_BID min	VAD_BID typ	VAD_BID max	SDV
0	0K +/- 5%	0 V	0 V	0 V	
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	SDV2
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	FVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	SIT
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	SVT



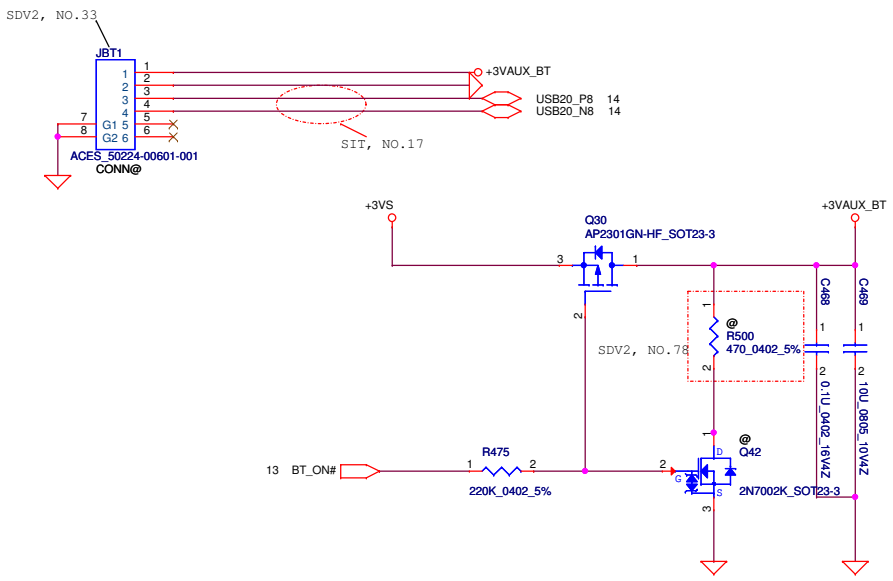
Security Classification	Compal Secret Data		Title
Issued Date	2011/04/18	Deciphered Date	2015/07/08
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Date:	Monday, January 16, 2012	Sheet	31 of 50

# Fintek Thermal sensor Placed near by APU\_CORE

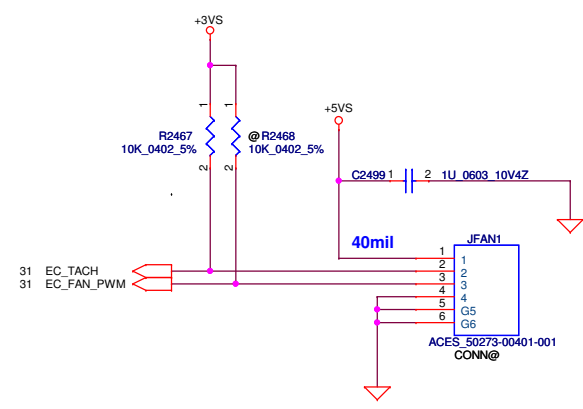


REMOTE1,2+/-:  
Trace width/space:10/10 mil  
Trace length:<8"

## BT Connector



## FAN1 Conn



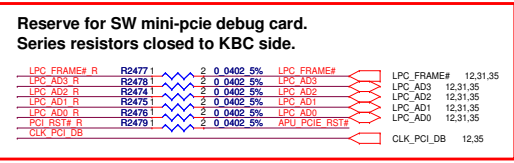
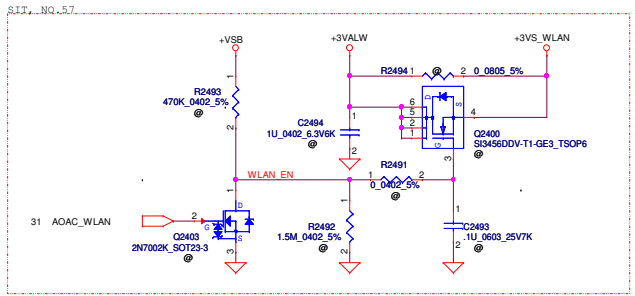
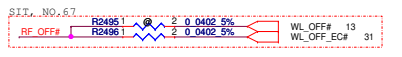
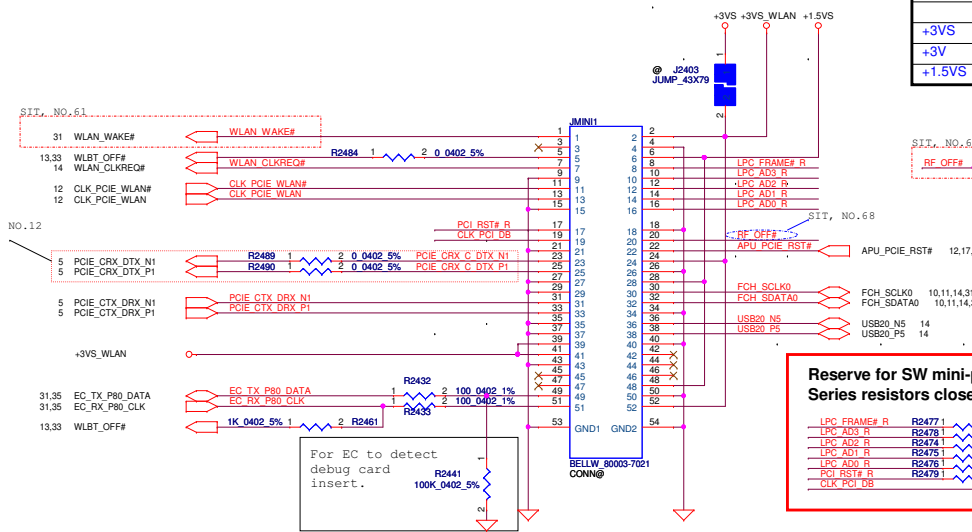
Security Classification	Compal Secret Data		Title	
Issued Date	2011/04/18	Deciphered Date	2015/07/08	Compal Electronics, Inc.
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Document Number			Rev	0.4
LA-8121P			Date:	Monday, January 16, 2012
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# WLAN Conn

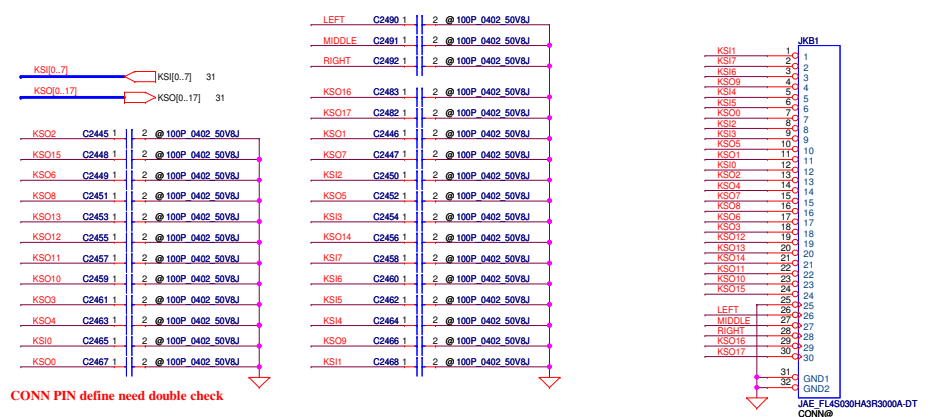
Mini Card Power Rating

Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	Normal
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

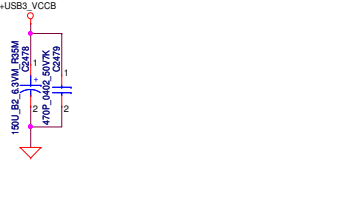
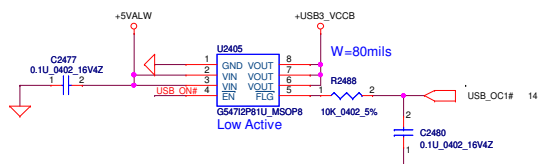
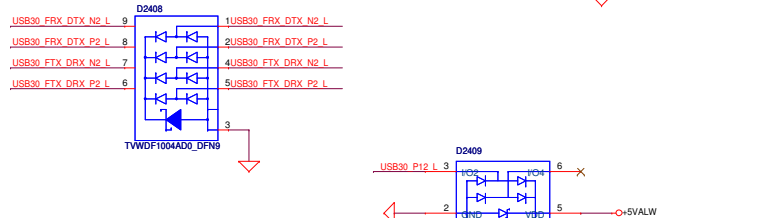
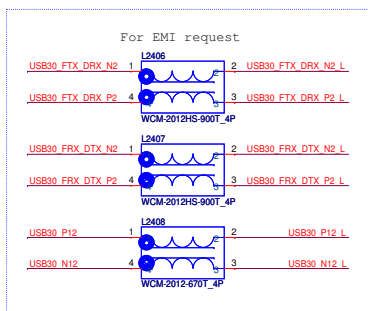
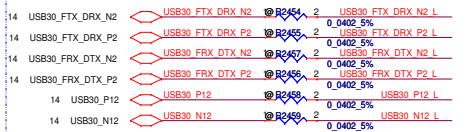
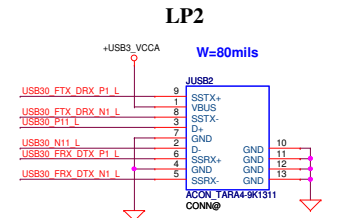
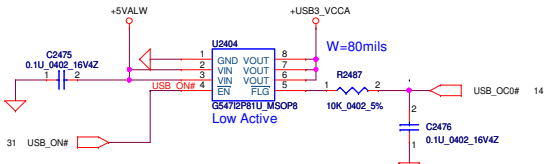
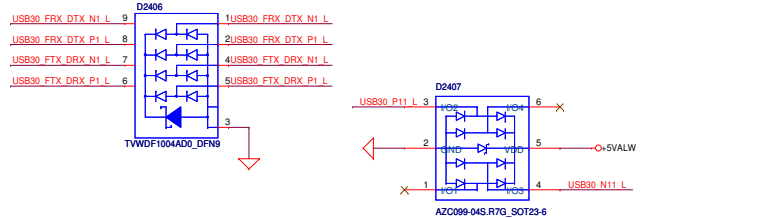
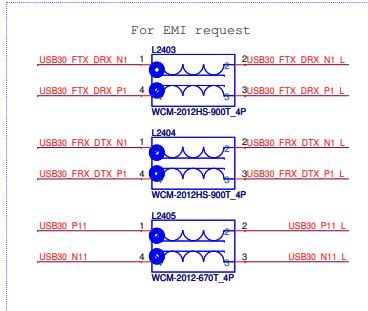
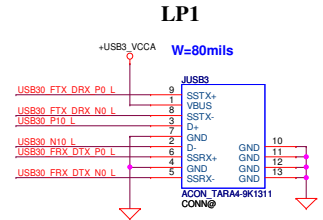
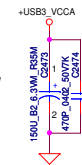
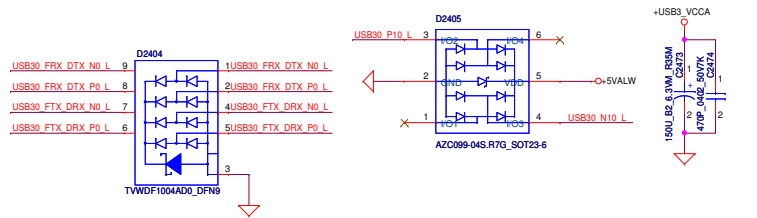
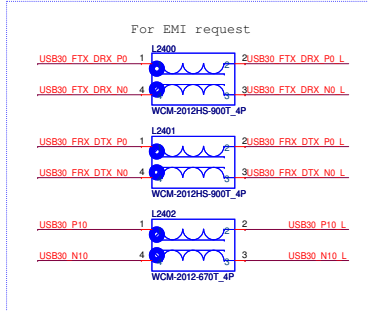
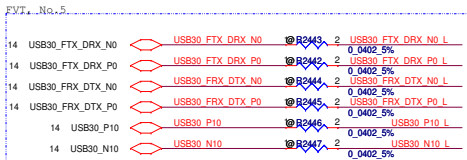


For AOAC assessment  
+3VS\_WLAN path:  
1. +3VS (default)  
2. +3VALW  
3. +3VALW + Switch

# INT\_KBD Conn.

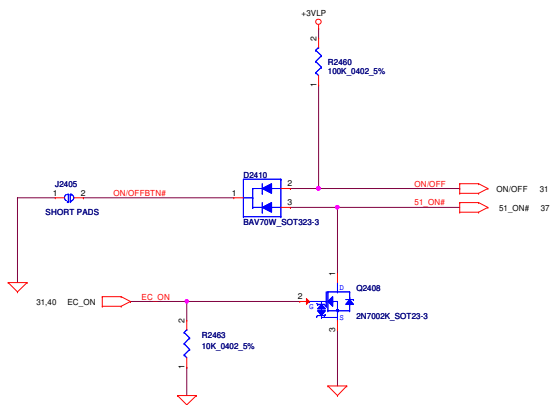


# USB3.0 Conn \*3

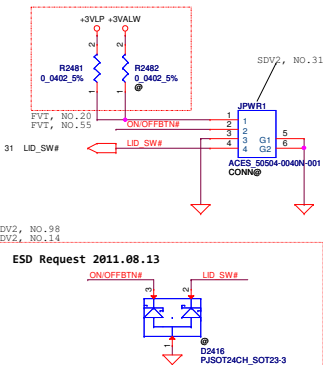


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Title	Compal Electronics, Inc.		
Doc No	USB 3.0 Conn		
Rev	1A-8121P		
Date	Monday, January 16, 2012	Sheet	34 of 50

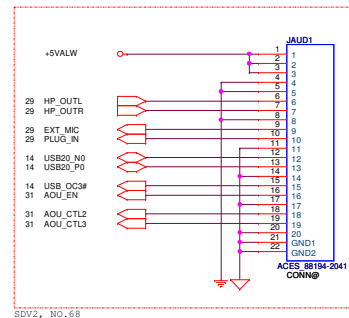
### ON/OFF switch



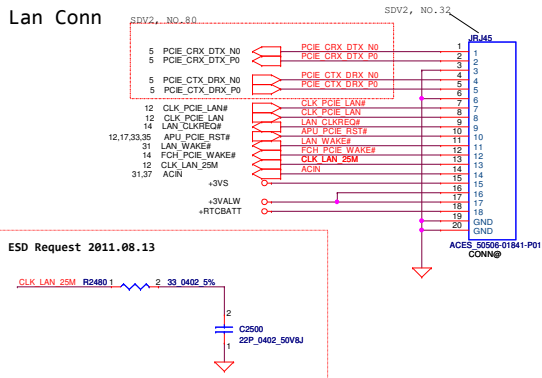
### Power Button Board Conn



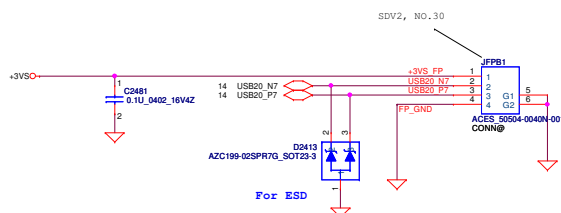
### USB2.0/Audio Jack SB CONN



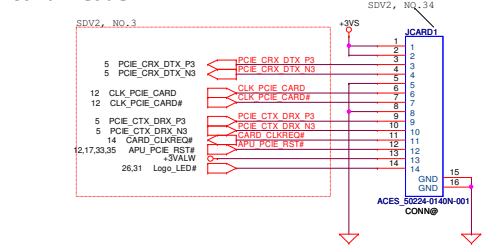
### Lan Conn



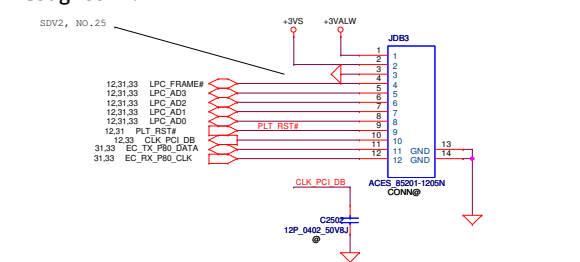
### Finger Printer



### Card Reader

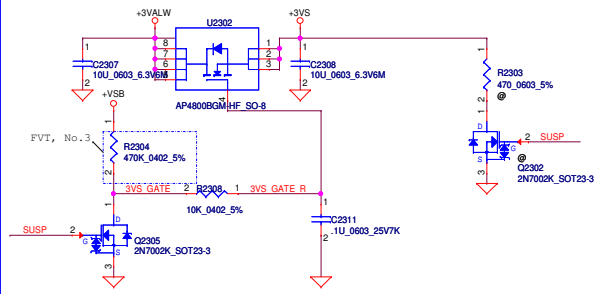


### Debug Conn.

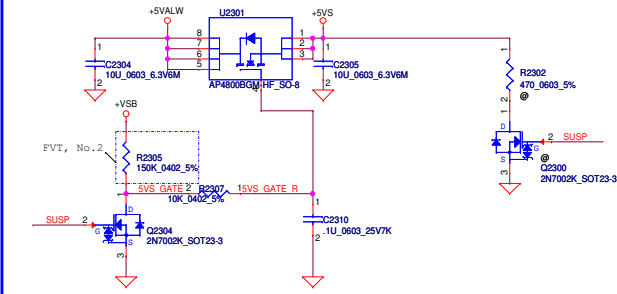


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Size	Document Number	Rev	LA-8121P	
Custom	0.4	Monday, January 16, 2012 35 of 50		

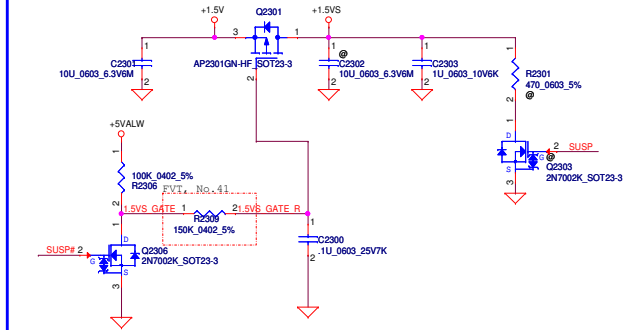
### +3VALW TO +3VS



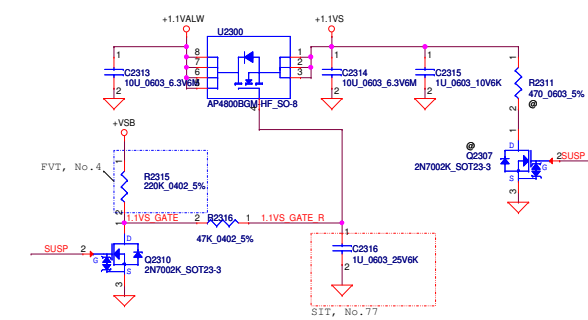
### +5VALW TO +5VS



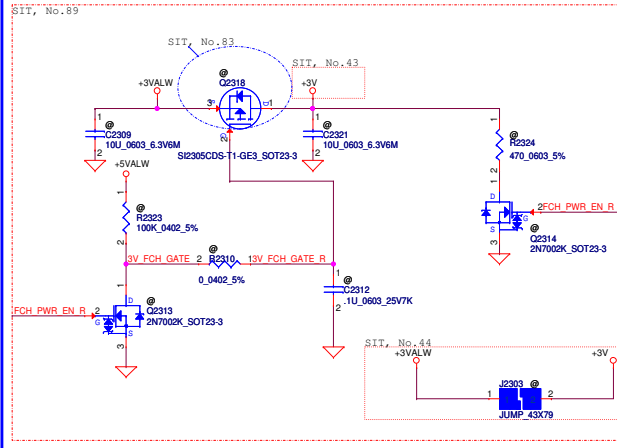
### +1.5V to +1.5VS



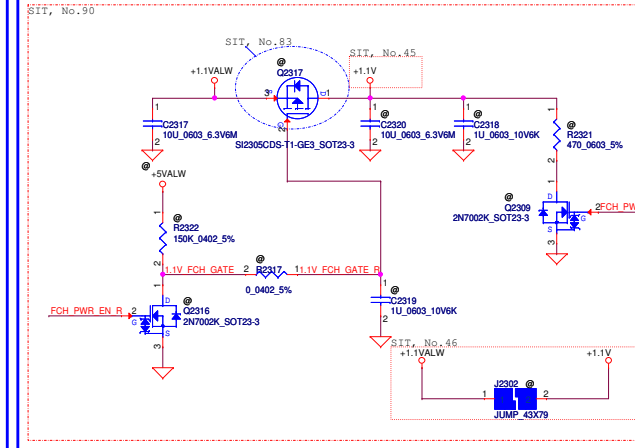
### +1.1VALW to +1.1VS



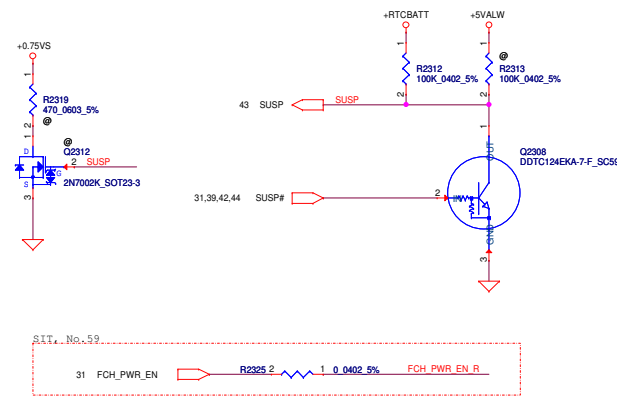
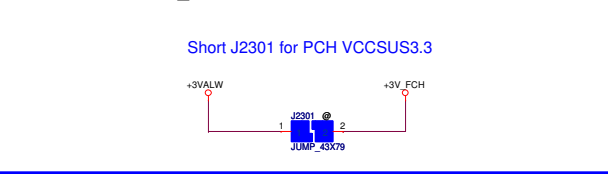
### +3VALW TO +3V



### +1.1VALW to +1.1V



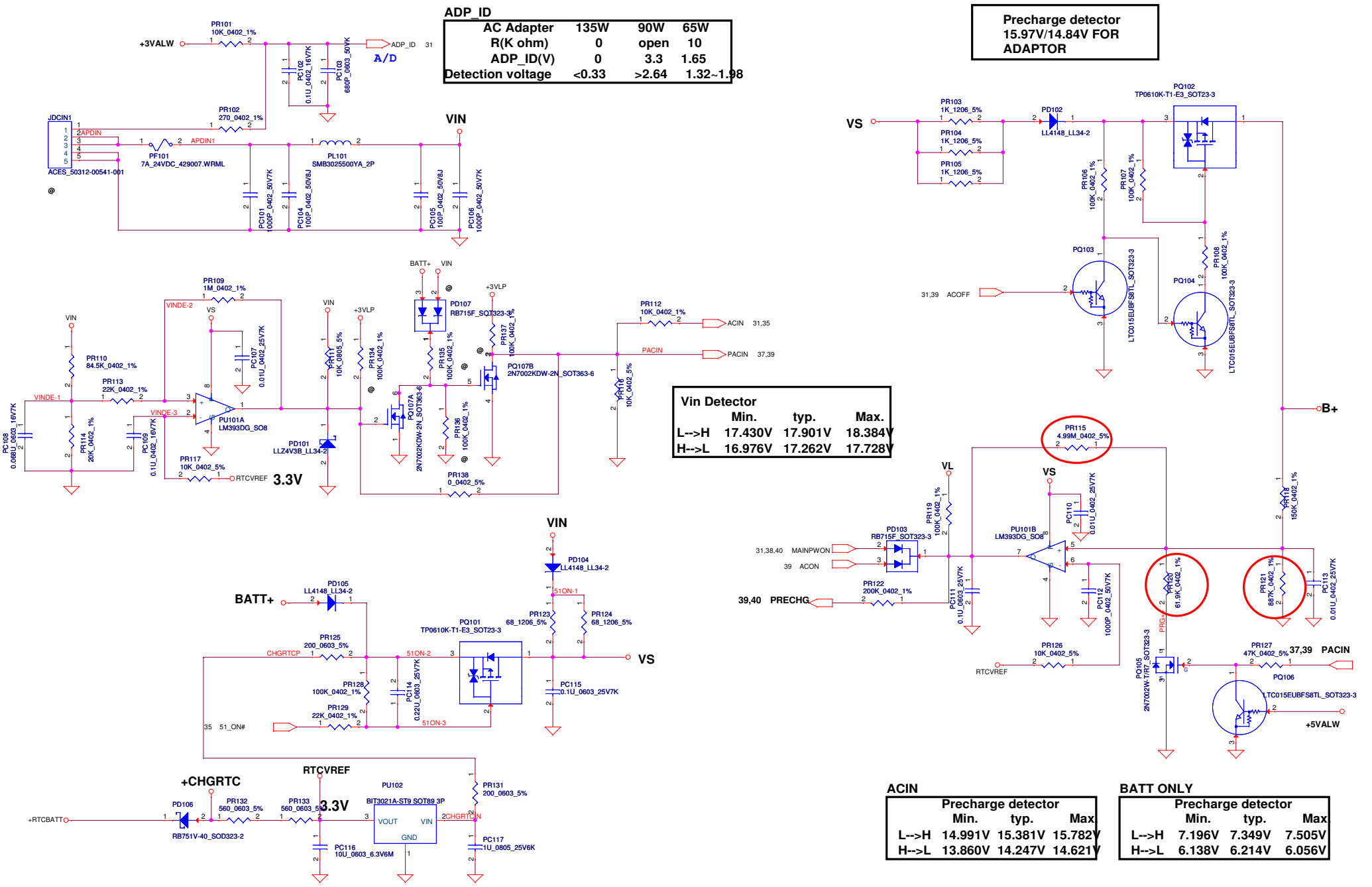
### +3VALW TO +3V\_FCH



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Size	C	Document Number	IA-8121P		Rev
Date	Monday, January 16, 2012	Sheet	36	of	50

ADP_ID			
AC Adapter	135W	90W	65W
R(K ohm)	0	open	10
ADP_ID(V)	0	3.3	1.65
Detection voltage	<0.33	>2.64	1.32~1.98

**Precharge detector  
15.97V/14.84V FOR  
ADAPTOR**



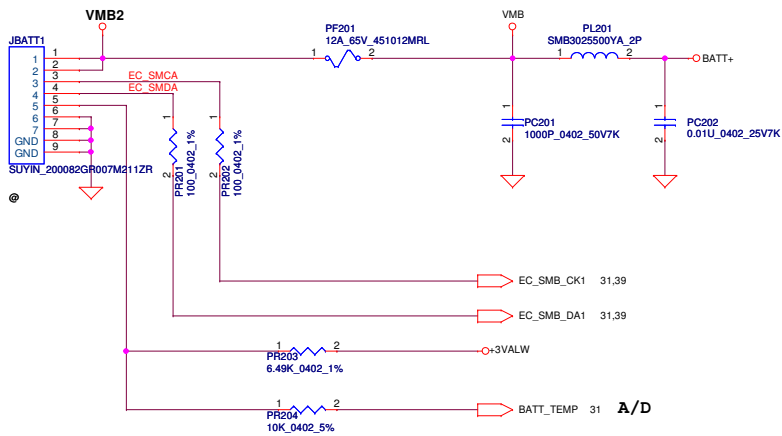
Vin Detector		
	Min.	typ.
L->H	17.430V	17.901V
H->L	16.976V	17.262V
		Max.
		18.384V

ACIN Precharge detector		
	Min.	typ.
L->H	14.991V	15.381V
H->L	13.860V	14.247V
		Max.
		15.782V

BATT ONLY Precharge detector		
	Min.	typ.
L->H	7.196V	7.349V
H->L	6.138V	6.214V
		Max.
		7.505V

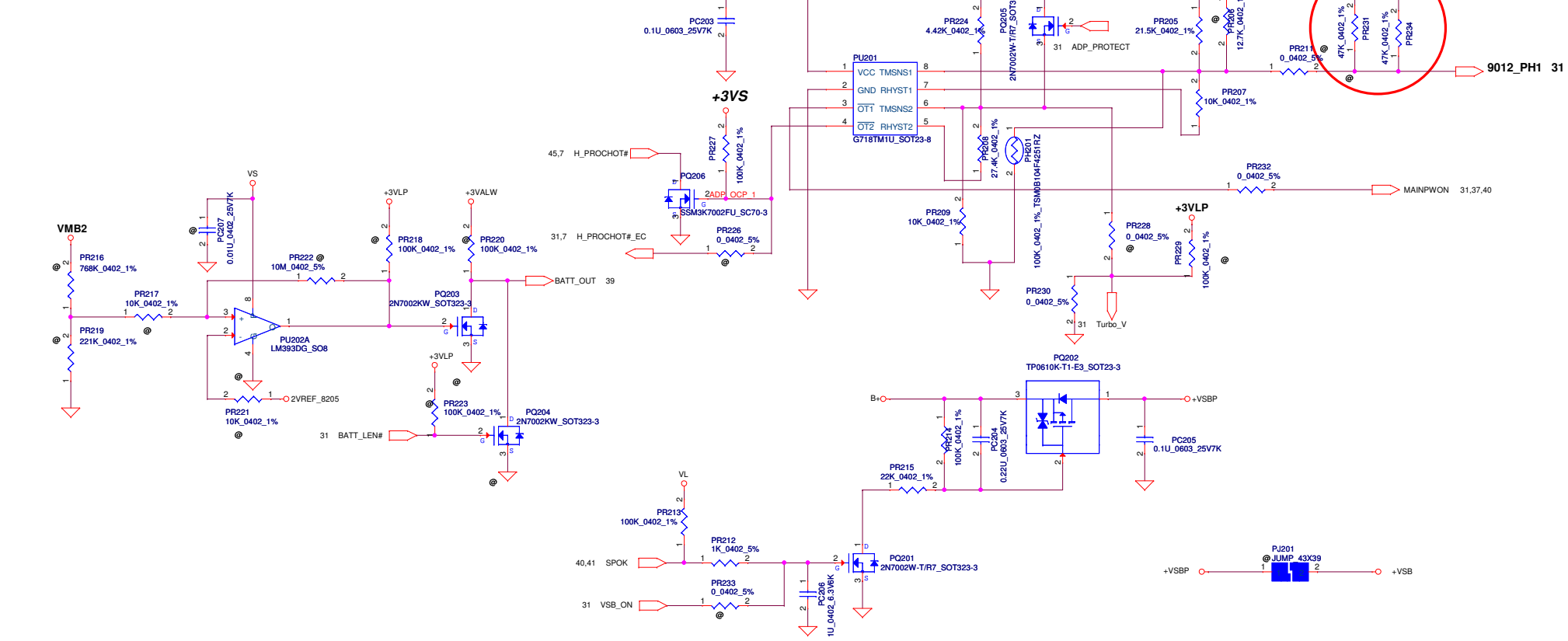
Security Classification	Compal Secret Data	
Issued Date	2011/04/18	Deciphered Date
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Compal Electronics, Inc.	
Title	PWR DCIN / Vin Detector /Pre-charge
Size	Document Number
Custom	C38-G series Chief River Schematic <sup>0.1</sup>
Date:	Monday, January 16, 2012
Sheet	37 of 48



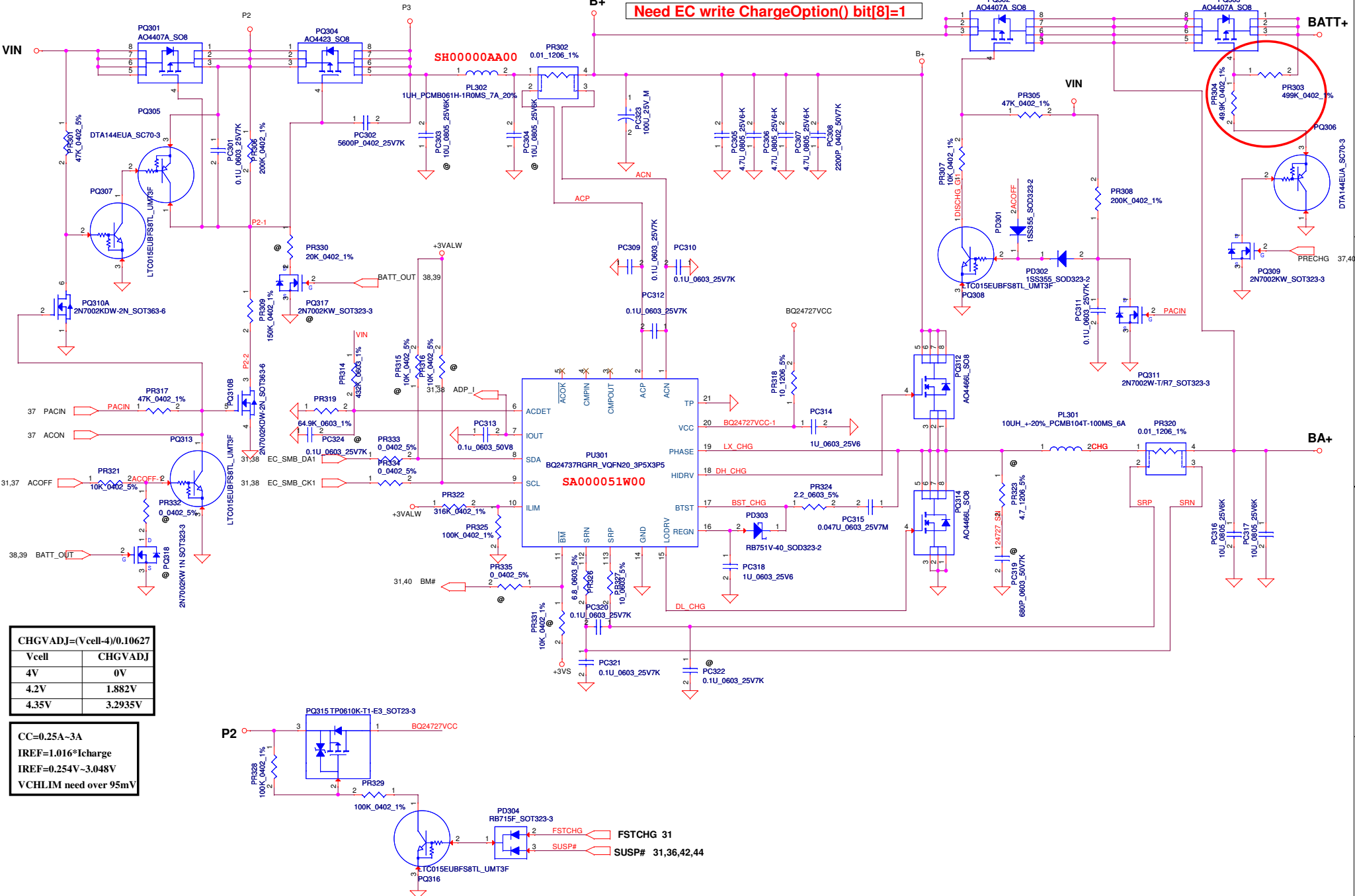
PH1 under CPU bottom side :  
 CPU thermal protection at 93 +/-3 degree C  
 Recovery at 56 +/-3 degree C

For KB930 --> Keep PU201 circuit  
 (Vth = 1.25V)  
 For KB9012 (Red square) --> Remove PU201 circuit, but keep PR206  
 PH201



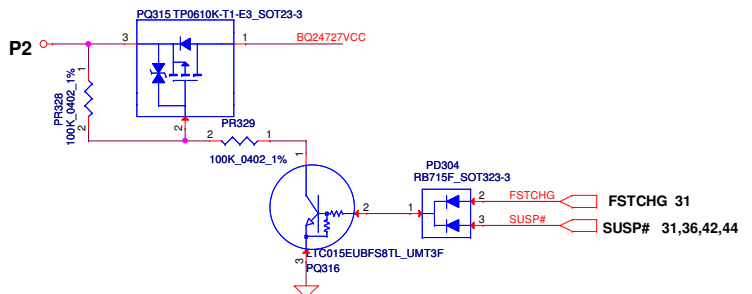
Security Classification	Compal Secret Data		Title <b>Compal Electronics, Inc.</b> <b>PWR-BATTERY CONN/OTP</b>
Issued Date	2011/04/18	Deciphered Date	
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Size Custom	Document Number <b>C38-G series Chief River Schematic</b>	Rev <b>0.1</b>	Date: Monday, January 16, 2012   Sheet 38 of 48

Need EC write ChargeOption() bit[8]=1



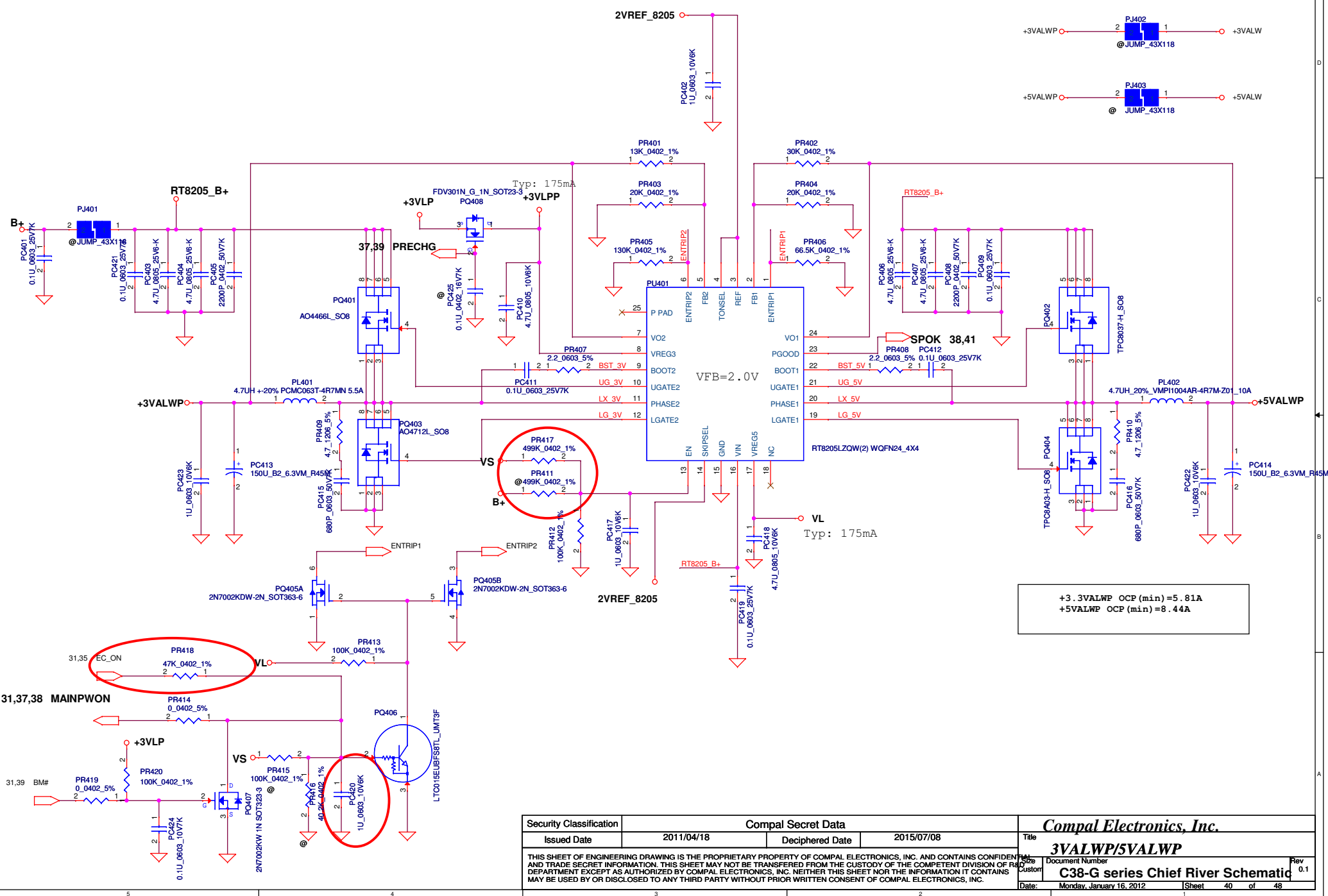
CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A-3A  
 IREF=1.016\*Icharge  
 IREF=0.254V~3.048V  
 VCHLIM need over 95mV



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Issued Date	2011/04/18	Deciphered Date	2015/07/08	Title
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				<b>C38-G series Chief River Schematic</b>
				Rev 0.1
				Date: Monday, January 16, 2012   Sheet 39 of 48

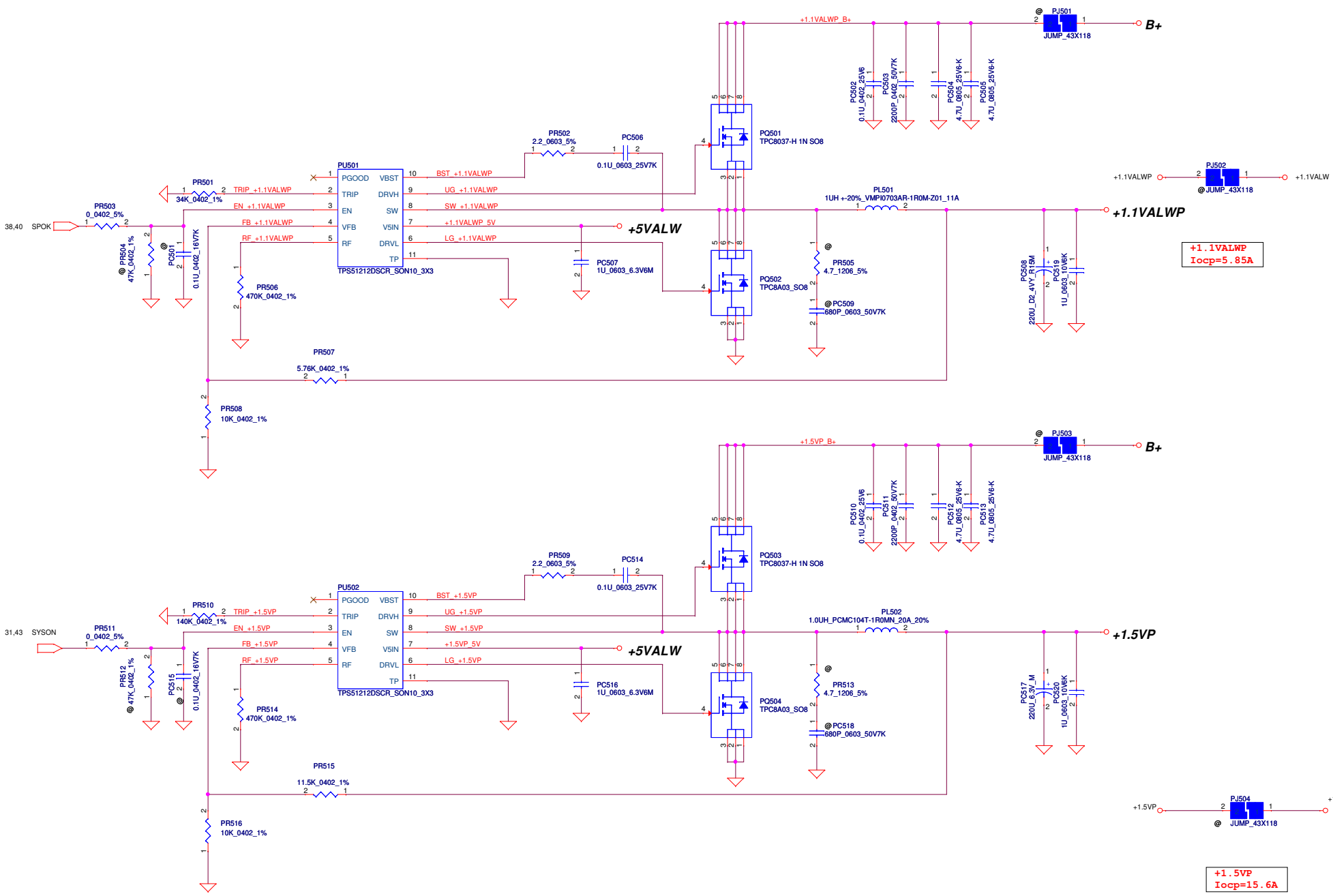
Note:  
 Use TPS51125 IC can remove RTC refernece LDO  
 Use TPS51427 IC must keep RTC refernece LDO



+3.3VALWP OCP (min) = 5.81A  
 +5VALWP OCP (min) = 8.44A

Security Classification	Compal Secret Data		Title <b>3VALWP/5VALWP</b>
Issued Date	2011/04/18	Deciphered Date	
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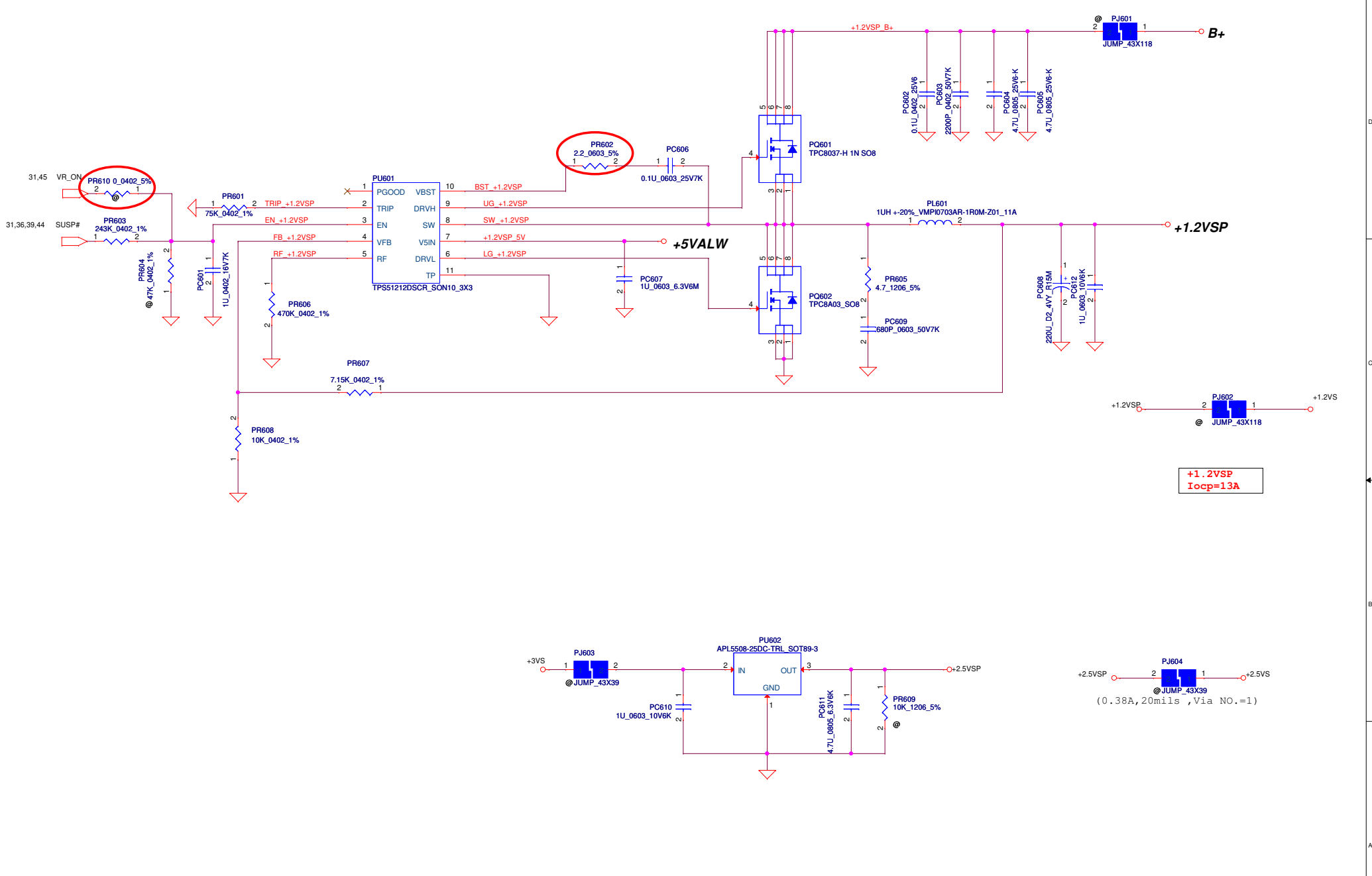




**+1.1VALWP**  
Iocp=5.85A

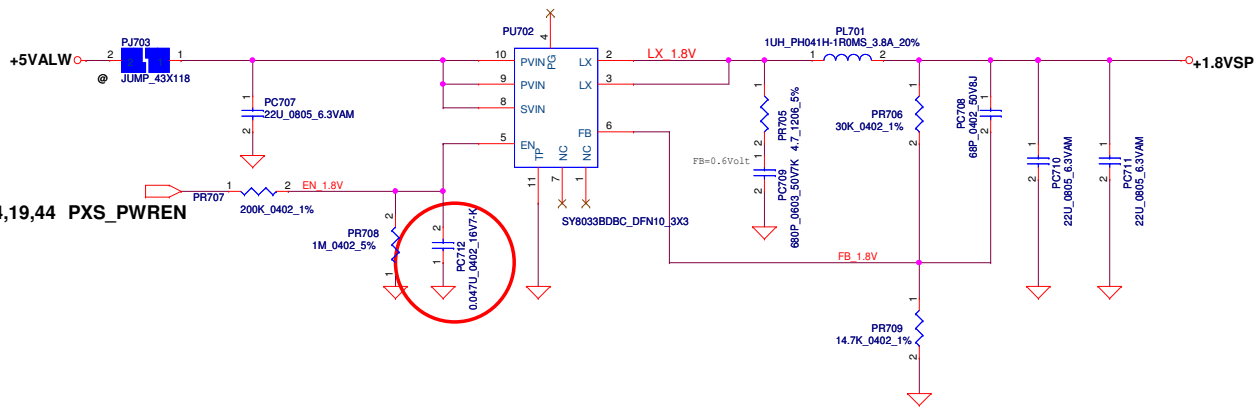
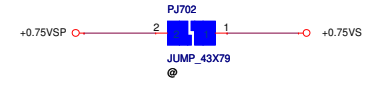
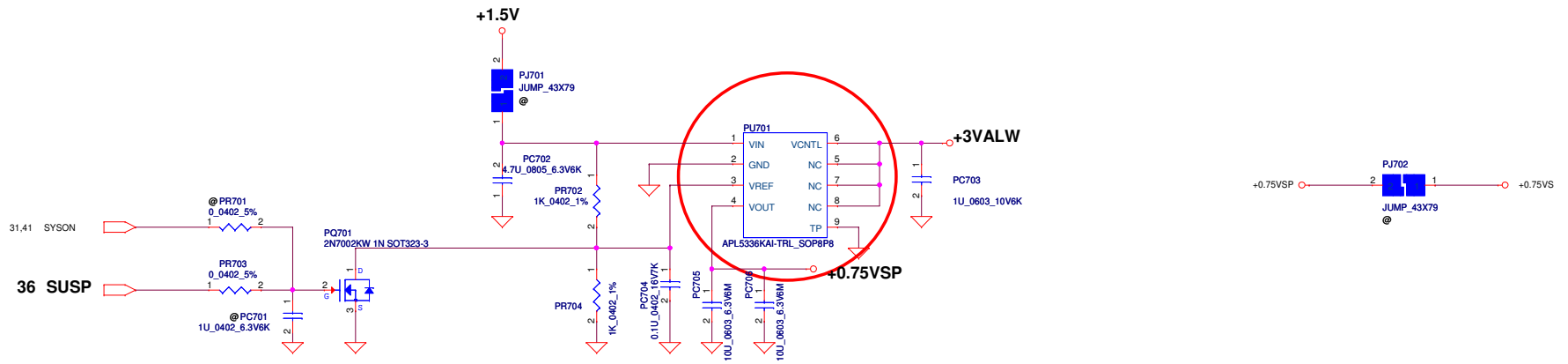
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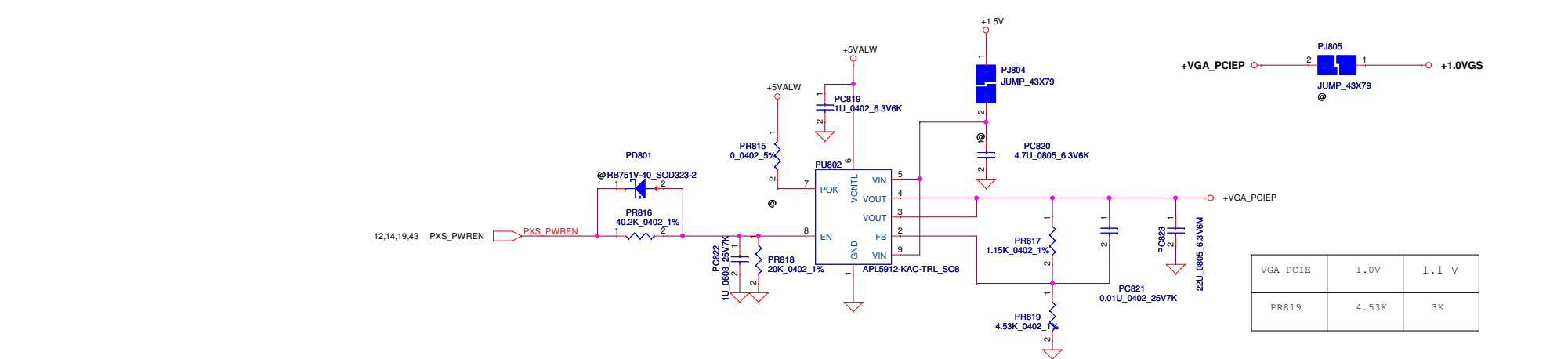
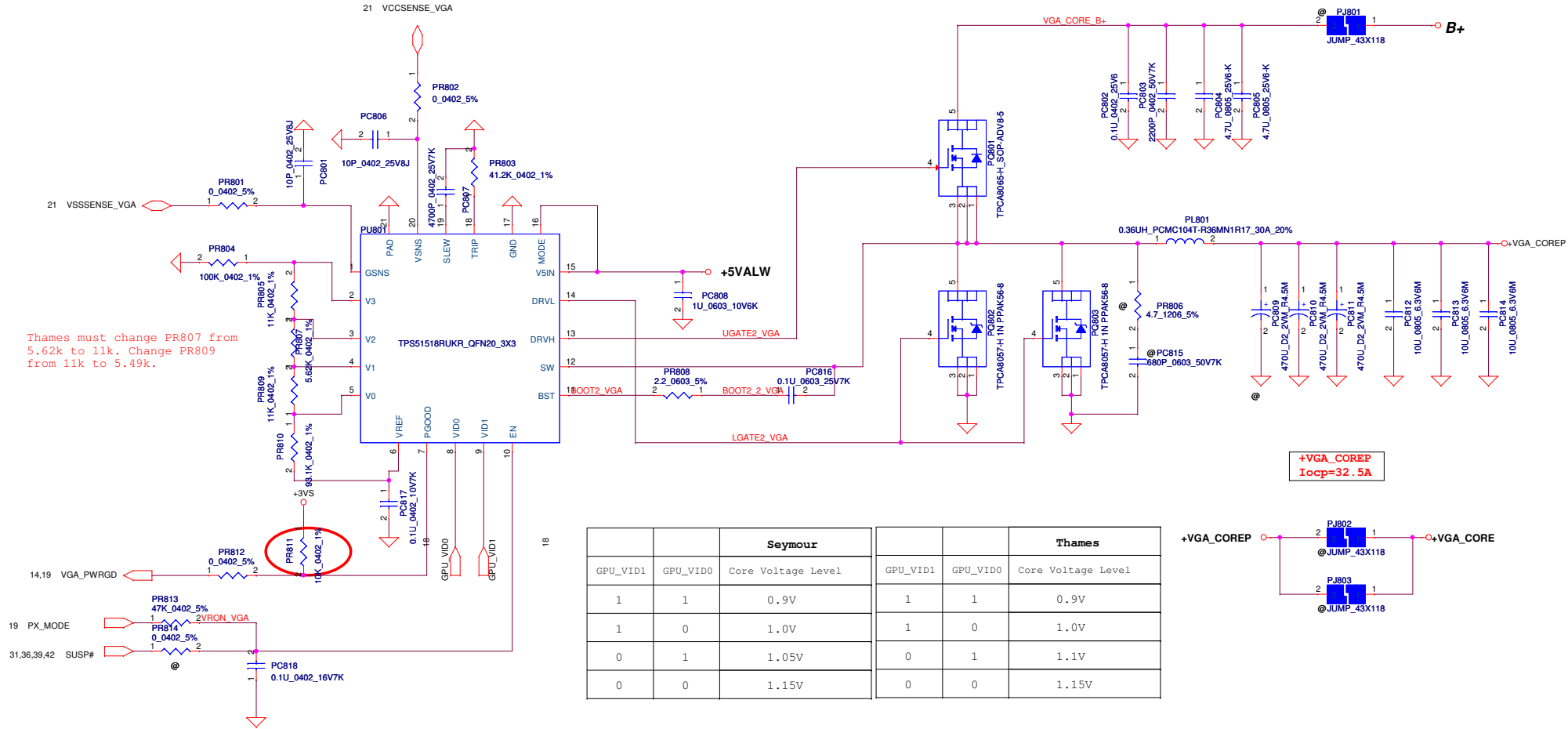


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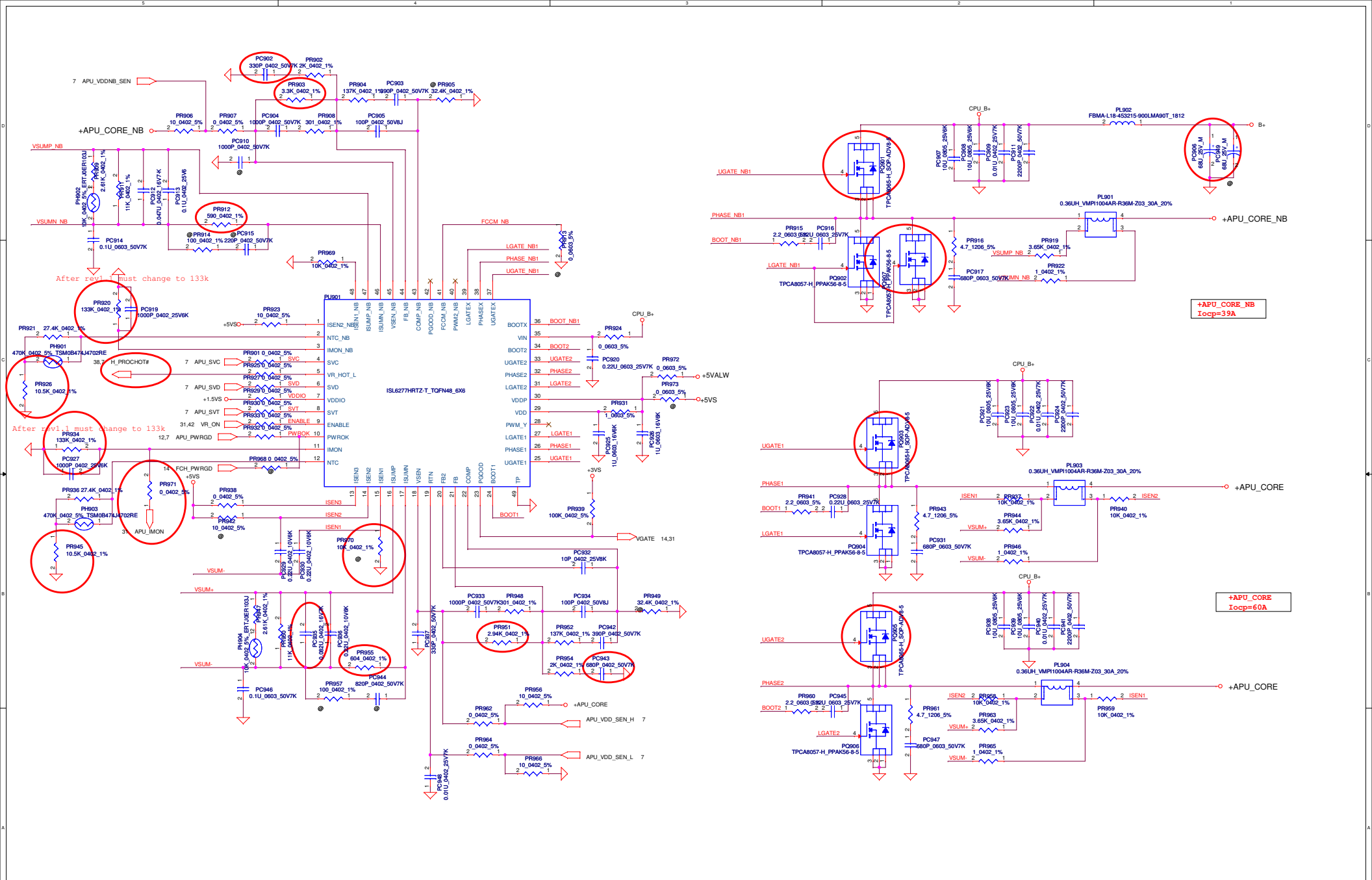
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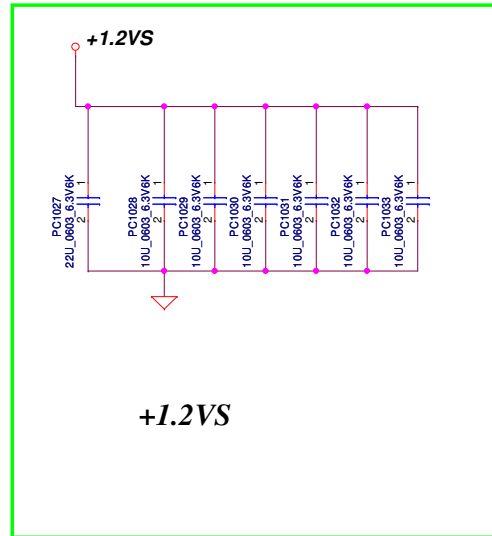
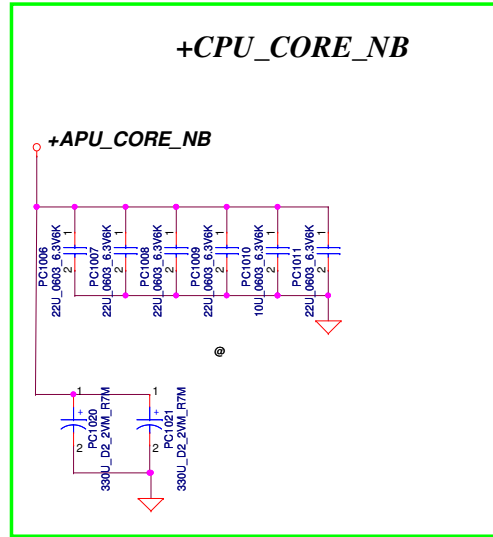
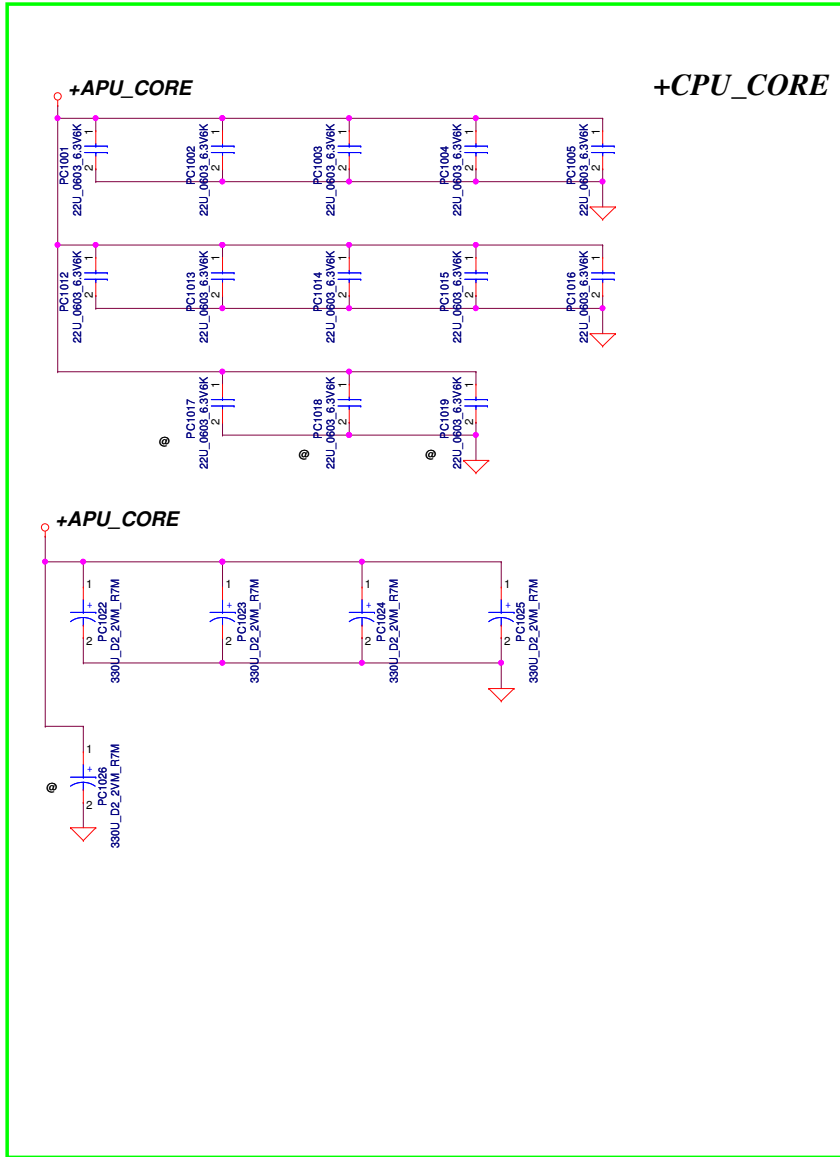
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Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
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6					
7					
8					
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11					
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<small>DATE: MONDAY, JANUARY 16, 2012</small>				Date	Monday, January 16, 2012
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Phase	Date	No.	BOM	Sch	Layout	Description
SDV2	2011/09/13	No.1	V			Page29, install R1102, R1104, R1105 for audio noise prevention
	2011/09/14	No.2	V			page12~16, change FCH P/N from SA0000431C0 to SA0000431G0
	2011/09/16	No.3	V	V		Page35, Swap JCARD1 Pin3,4 to Pin9,10 PCIE TX & RX for CardReader no function issue
	2011/09/16	No.4	V	V		Page33, Modify JTF1 Pin1 to TP_DATA2, JTF1 Pin6 to TP_CLK2 for Click Pad no function issue
	2011/09/17	No.5	V	V		Page30, Modify JHDD1 Pin1 connect to GND for SATA Gen2
	2011/09/17	No.6	V			Page5~9, Modify U1 to JCPU1
	2011/09/17	No.7	V			Page10~11, SWAP JDIMM1 & JDIMM2
	2011/09/17	No.8	V			Page33, Modify JFP1 to JFP2,Modify JWLAN1 to JMINI1,Modify JLAN1 to JRJ45
	2011/09/17	No.9	V			Page31, Modify CLRPI to JCMOS1
	2011/09/26	No.10	V			Page31, POP U2201,C2200,R2229 for Security ROM function not work issue
	2011/09/26	No.11	V			Page14, Modify D1103,D1104 to DIS8 for DIS only
	2011/09/28	No.12	V	V		Page349, Reserve R2490 with CRX_C_DTX_N1,PCIE_CRX_C_DTX_P1 for PCIE WLAN RX AC Decoupling
	2011/09/28	No.13	V	V		Page29, R1111.2 Connect to U1101 Pin38 add net name CX_GPIO0 for vendor request
	2011/09/28	No.14	V	V		Page35, Add D2416 to replace D2414 for ESD request
	2011/09/28	No.15	V	V		Page5~9, Modify JCPU1 Footprint to LOTES_ACA_ZIF-109_722P-A39 for A39 DFX Rule
	2011/09/28	No.16	V	V		Page12~16, Modify U2 JPDSON PCBGA 656P-A39 for A39 DFX Rule
	2011/09/28	No.17	V	V		Page17~22, Modify U1401 Footprint to 2160809000A11SEY_FCBGA_962P-A39 for A39 DFX Rule
	2011/09/28	No.18	V	V		Page23~24, Modify U1405~U1412 Footprint to K4W1G1646E-HC12_FBGA_96P-A39 for A39 DFX Rule
	2011/09/28	No.19	V	V		Page31, Modify Board ID Table for AMD Build Plan Change
	2011/09/28	No.20	V	V		Page31, Modify R2209 for QALEA FVT Build Board IC Mapping
	2011/09/28	No.21	V	V		Page29, Add Signal Name for USB30 [P..N] [10..12]_C , D1104.1 for PX control enable delay
	2011/09/30	No.22	V			Page28, update JCRT1 Footprint from SUVIN_070546PR015S2002R_15P to C-H_13-12201558CP_15P-T for ME Conn modify
	2011/10/03	No.23	V			Page14, Add C222~C237 connect to all USB2.0 port near connector for AMD request that about USB Signal Driving
	2011/10/04	No.24	V	V		Page14, Add C222~C237 connect to all USB2.0 port near connector for AMD request that about USB Signal Driving
	2011/10/05	No.25	V	V		Page35, Add JDB3 Conn for SW Debug request
	2011/10/05	No.26	V	V		Page12, Add TP52~T58 on U2 GPIO input pin for debug
	2011/10/05	No.27	V	V		Page13, Add TP59~T61, TP67~T74 on U2 GPIO input pin for debug
	2011/10/05	No.28	V	V		Page14, Add TP62~T93 on U2 GPIO input pin for debug
	2011/10/06	No.29	V	V		Page26, Q2101 P/N change to SB00007H10 for Component common
	2011/10/06	No.30	V	V		Page35, JFPB1 update P/N to SP010002300 for Conn List update
	2011/10/06	No.31	V	V		Page35, JFPW1 update P/N to SP010002300 for Conn List update
	2011/10/06	No.32	V	V		Page35, JRJ45 update Footprint to ACES_50516-01841-P01_18P-T for Conn List update
	2011/10/06	No.33	V	V		Page32, JBT1 update P/N to SP02000TF00 for Conn List update
	2011/10/06	No.34	V	V		Page35, JCARD1 update Footprint to ACES_50224-0140N-001_14P-T for Conn List update
	2011/10/07	No.35	V	V		Page29, reserve D1101 for Audio Noise issue
	2011/10/11	No.36	V	V		Del TP52~T58 on U2 GPIO input pin for debug
	2011/10/11	No.37	V	V		Page13, Del TP59~T61, TP67~T74 on U2 GPIO input pin for debug
	2011/10/11	No.38	V	V		Page14, Add TP62~T93 on U2 GPIO input pin for debug
	2011/10/12	No.39	V			Page22, Replace R1476 P/N From D028100A00 to SD028100A80 for HF Part modify
	2011/10/12	No.40	V			Page19, 30, 36, Replace Q1409, Q2309, Q2410 P/N From SB00001240010 to SB000007000 for HF Part modify
	2011/10/13	No.41	V			Page12, Replace X1 P/N From SJ100003300 to SJ10000EL00 for Sourcer request (No Footprint, Use SJ10000DJ00)
	2011/10/13	No.42	V			Page12, Replace Y1 P/N From SJ132P7KW10 to SJ10000BM00 for Sourcer request
	2011/10/13	No.43	V			Page18, Replace Y400 P/N From SJ100006800 to SJ10000D000 for Sourcer request (No Footprint, Use SJ10000DJ00)
	2011/10/13	No.44	V			Page31, Replace U2200 P/N From SJ132P7KW10 to SJ10000BM00 for Sourcer request
	2011/10/13	No.45	V	V		Page31, Modify U2200 Pin107 EC_PXCNTROL to U2200 Pin108 for ABO Common Design
	2011/10/14	No.46	V	V		Page31, Add R2235 pull up to +3VS for EPROCHOT#_EC
	2011/10/14	No.47	V	V		Page19, Replace Q1401,Q1402,Q1405 P/N From SB00000FG00 to SB00000FG10 for Sourcer request
	2011/10/17	No.48	V	V		Page26, Add C2144,C2145 1000P Caps connect to DMIC_CLK & DMIC_L2 for EMI Request(Noise issue)
	2011/10/17	No.49	V	V		Page25, Add R2171 connect to LVDS_HPD_R for Vendor Request (Noise Filtering)
	2011/10/17	No.50	V	V		Page7, 9, 27 Replace Q2,Q3,Q8,Q2106 P/N From SB000006A00 to SB000006A10 for HF Part modify
	2011/10/17	No.51	V	V		Page14, Del D1103,D1104 with CRX_C_DTX_N1 & CRX_C_DTX_P1 for Control FXS_PWREN ON/OFF Timing for VGA Sequence tuning
	2011/10/17	No.52	V	V		Page19, Modify C1463,D1400,R1442 BOM Structure from DIS8 to FX400 & D1400 use 0_0603_58 for FX50
	2011/10/17	No.53	V			Page7, Modify R65,R69 BOM Structure to 0 for Power Leakage issue
	2011/10/17	No.54	V			Page12, Modify R80,R82 value from 0 ohm to 33 ohm for EMI Noise Issue
	2011/10/18	No.55	V	V		Page7, 31, Modify Input/Output direction: H_PROCHOT#, Turbo_V
	2011/10/18	No.56	V	V		Page27, Add Net +5VS_HDMI on D2103 Pin5 & Pin6 for ESD Request
	2011/10/18	No.57	V			Page19, Modify R1454,Q1412,R1450,R1451,R1449,C1470,U1404,C1467,C1468,C1469,C1470 BOM Structure from PX40 to DIS8 for FX50 Function workable
	2011/10/19	No.58	V	V		Page31, Add Net APU_LMON on U2200 Pin76 for Power Team Request
	2011/10/19	No.59	V	V		Page35, Add intersheet of PLT_RST# on debug card
	2011/10/19	No.60	V	V		Page25, modify net name: LVDS_HPD_R to LVDS_HPD_C
	2011/10/20	No.61	V	V		Page33, Del A0AC circuit for Customer request
	2011/10/20	No.62	V	V		Page31, Del A0AC Powe Control Pin WLAN_POWER# for Customer request
	2011/10/20	No.63	V	V		Page14, Modify USB Signal net name from USB20_[P..N] [10..12]_C to USB30_[P..N] [10..12]_C for USB30 net name error
	2011/10/21	No.64	V	V		Page12, Modify R83,R84 value from 0 ohm to 33 ohm for EMI Noise Issue
	2011/10/21	No.65	V	V		Page31, Modify R2212,R2213 BOM Structure to 0 for ENE Suggestion
	2011/10/21	No.66	V	V		Page31, Modify U2200 Pin 72 Net Name From AOU_ILIM to SPK_RT_Detect# for Speaker main stream & retail
	2011/10/21	No.67	V	V		Page31, Add R2236 pull up to +3VS for SPK_RT_Detect#
	2011/10/21	No.68	V	V		Page35, Modify JAUD1 Pin20 Net Name From AOU_ILIM to GND , Pin17 From AOU_CTL1 to GND ,Pin4 From NC to AGNDFor USB Charger Function
	2011/10/21	No.69	V	V		Page29, Modify JSPEK1 P/N From DC030008W00 to SP02000N000 & Add JSPEK1 Pin5 connect to SPK_RT_Detect#,JSPEK1 Pin6 connect to GND for Speaker main stream & retail
	2011/10/21	No.70	V	V		Page31, Modify U2200 Pin120 Net Name From AOU_CTL1 to NC for USB Charger Function1
	2011/10/24	No.71	V	V		reserve D1102 for Audio Noise issue
	2011/10/24	No.72	V	V		Page35, Modify D2415 BOM Structure to POP for ESD Request
	2011/10/24	No.73	V	V		Page33, Modify D2402,D2403 BOM Structure to POP for ESD Request
	2011/10/24	No.74	V	V		Page34, Modify D2402,D2403 BOM Structure to POP for ESD Request
	2011/10/24	No.75	V	V		Del R2116,R2117, Add R2172~R2176 & Reverse D2110 for PWM Power Leakage issue
	2011/10/24	No.76	V	V		Page26, Del R2116,R2117, Add R2172~R2176 & Reverse D2110 for PWM Power Leakage issue
	2011/10/24	No.77	V	V		Page30, Del C2404,Reserve C2471,C2405 for Intel Circuit Common
	2011/10/24	No.78	V	V		Page32, Modify R500 BOM Structure to 0 for BOM Error
	2011/10/24	No.79	V	V		Page31, Del R2223~R2229, Q2200 to update Security ROM Circuit for Intel Circuit Common
	2011/10/24	No.80	V	V		Page35, Swap JRJ45 PCIE_CRX_DTX_P0 to PCIE_CRX_DTX_N0, PCIE_CTX_DRX_P0 to PCIE_CTX_DRX_N0 For LAN Board Common
	2011/10/24	No.81	V	V		Page35, Del R2462 to update Power OK circuit for Intel Circuit Common
	2011/10/24	No.82	V	V		Page36, Del R2300, R2310, C2312, R2317 update Power OK circuit for Intel Circuit Common
	2011/10/24	No.83	V	V		Page31, Modify R2235 BOM Structure to 0 for H_PROCHOT#_EC
	2011/10/24	No.84	V	V		Page34, Modify D2404,D2406,D2408 P/N from SC300001D00 to SC300002800 for ESD Request
	2011/10/24	No.85	V	V		Page34, Modify D2404~D2409,L2400~L2408 BOM Structure from 0 to POP for EMC Request
	2011/10/24	No.86	V	V		Page27, Modify L2105~L2108 BOM Structure from 0 to POP for EMI Request
	2011/10/24	No.87	V	V		Page34, Modify L2402,L2405,L2408 P/N from SC300000I00 to SM070000000 for ESD Request (Footprint SM0700000I00)
	2011/10/24	No.88	V	V		Page34, Modify L2403, L2404, L2400, L2401, L2406, L2407 P/N from SC300000I00 to SM070001500 for ESD Request
	2011/10/24	No.89	V	V		Page27, Modify D2102,D2103,D2105 P/N from SC300001Y00 to SC300002C00 for ESD Request
	2011/10/24	No.90	V	V		Page35, Modify D2413 P/N from SC300001600 to SC300001200 for EMI Request
	2011/10/25	No.91	V	V		Page29, Modify JSPEK1 P/N From SP02000N000 to SC300008W00 for LD Requirement
	2011/10/25	No.92	V	V		Page29, Add R1140 connect to SPK_RT_Detect# to GND for Speaker Verify
	2011/10/25	No.93	V	V		Page28, Del Q2412 with CRT_DDC_DATA & CRT_DDC_CLK for AMD Design Guide Require
	2011/10/26	No.94	V	V		Page26, Del R2122,R2123,R2124 with EDID_DATA & EDID_CLK pull up for Duplicate Pull up error
	2011/10/26	No.95	V	V		Page26, Modify R2174 BOM Structure to 0 for BOM Error
	2011/10/26	No.96	V	V		Page25, Reserve R2116, R2117 to Connect from CSCL & CSCA to EC_SMB_DA2 & EC_SMB_CB2 for Power Leakage issue
	2011/10/26	No.97	V	V		Page29, Modify D1101, D1102 BOM Structure From 0 to POP for Audio Noise issue
	2011/10/27	No.98	V	V		Page24, Modify P/N From SC300001000 to SC300001000 for ESD Request
	2011/10/27	No.99	V	V		Page29, Modify C1111 ,C1141 BOM Structure From POP to 0 for Audio Noise issue

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Phase	Date	No.	BOM	Sch	Layout	Description
FVT	2011/11/14	No.1	V			Page17-24, Modify U1401 P/N From SA000047H00 to SA000047H50 for GPU Version update
	2011/11/14	No.2	V			Page36, Modify R2305 P/N From SD028200280 (20K_0402_5%) to SD028150380 (150K_0402_5%) for Power Consumption & Power Sequence tuning
	2011/11/14	No.3	V			Page36, Modify R2304 P/N From SD028470280 (47K_0402_5%) to SD028470380 (470K_0402_5%) for Power Consumption & Power Sequence tuning
	2011/11/14	No.4	V			Page36, Modify R2315 P/N From SD028750280 (75K_0402_5%) to SD028220380 (220K_0402_5%) for Power Consumption & Power Sequence tuning
	2011/11/14	No.5	V			Page34, Modify R2442-R2459 BOM Structure From POP to @ for EMI Request
	2011/11/14	No.6	V			Page27, Modify R2126-R2133 BOM Structure From POP to @ for EMI Request
	2011/11/14	No.7	V	V	V	Page14, Replace C222-C237 to R216-R231 on all usb port signal for AMD Design checklist update (USB no function issue)
	2011/11/14	No.8	V	V	V	Page19, Add R1461 to connect PK5_PWREN to RUNPWOK for PK50 Power Enable
	2011/11/14	No.9	V	V	V	Page30, Modify J0DD1 Location to J0DD2 for ME BOM Common
	2011/11/14	No.10	V	V	V	Page14, Remove R230-R231 on all usb port signal for AMD Design checklist update (USB no function issue)
	2011/11/15	No.11	V	V	V	Page35, Remove D2415 for ESD Request
	2011/11/21	No.12	V	V	V	Page31, Reserve R2411, C2421 for G Sensor Vendor Suggestion
	2011/11/21	No.13	V	V	V	Page29, Modify JSPK1 Conn From 4Pin to 6Pin & Move R1140 to connect JSPK1 Pin5 For Speaker main stream & retail
	2011/11/21	No.14	V	V	V	Page31, Add J2200, J2201 to improve EC Power Source +3VLP or +3VALM to +3VALW_EC Power Source Option and modify +3VALW Net Name to +3VALW_EC for Lenovo S4 Lid Function
	2011/11/21	No.15	V	V	V	Page31, Update Borad ID Table For FVT Phase
	2011/11/21	No.16	V	V	V	Page31, Modify R2209 From 8_2K to 18K for FVT BRDID update
	2011/11/21	No.17	V	V	V	Page30, C2417 BOM Change from 10U (SE000005T80) to 10K (SD013100280) for G Sensor Vendor Suggestion
	2011/11/21	No.18	V	V	V	Page36, Add R2321, R2322, C2317, C2318, C2319, Q2313, Q2314 for +3V_FCH Power Control
	2011/11/21	No.19	V	V	V	Page31, U2200 Pin7 Add FCH_PWR_EN# for +3V_FCH Power Control
	2011/11/22	No.20	V	V	V	Page35, Add R2481 Pull up to +3VLP & Reserve R2482 Pull up to +3VALM for Lenovo S4 LID Function
	2011/11/22	No.21	V	V	V	Page18, Y1400 P/N From SJ10000DY00 to SJ10000CV00 for BOM Change
	2011/11/22	No.22	V	V	V	Page12, X1 P/N From SJ10000E100 to SJ10000CX00 for BOM Change
	2011/11/22	No.23	V	V	V	Page25, Modify R2117 connect to TL_DATA & R2116 connect to TL_CLK, Two signals connect to R2177, R2178 pull up to +3VS for LVDS Translator EEPROM Reserve
	2011/11/22	No.24	V	V	V	Page31, Modify U2200 Pin86 EAPD to TL_DATA & Add U2200 Pin85 TL_CLK for LVDS Translator EEPROM Reserve Function
	2011/11/22	No.25	V	V	V	Page31, Add U2200 Pin26 EAPD_R for LVDS Translator EEPROM Reserve Function
	2011/11/22	No.26	V	V	V	Page31, Add R2223 & R2224 to option EAPD GPIO Output signal from Pin26 (EAPD_R) or Pin86 (TL_DATA) for LVDS Translator EEPROM Reserve Function
	2011/11/23	No.27	V	V	V	Page14, Del R216-R229 for USB2.0 Signals tuning circuit remove
	2011/11/23	No.28	V	V	V	Page14, Reserve R230-R234 & C222-C226 with USB2.0 N signals port 0, 6, 10, 11, 12 for AMD Suggestion
	2011/11/24	No.29	V	V	V	Page36, Del R2321, R2322, C2317, C2318, C2319, Q2313, Q2314 for +3V_FCH Power Control
	2011/11/24	No.30	V	V	V	Page31, U2200 Pin70 Del FCH_PWR_EN# for +3V_FCH Power Control
	2011/11/24	No.31	V	V	V	Page31, U2200 Pin127 Add VSB_ON & Reserve R2226 for +VSB Power Control
	2011/11/25	No.32	V	V	V	Page35, Add H18 for ME Drawing lose
	2011/11/25	No.33	V	V	V	Page31, Modify R2217, R2218 Power Source from +3VS to +3VALM for +3VGS Power Leakage issue
	2011/11/25	No.34	V	V	V	Page18, Install Q1400, R1427, R1428 & Remove R1433, R1435 for +3VGS Power Leakage issue
	2011/11/25	No.35	V	V	V	Page31, Del R2226 for VSB_ON resistor double reserve
	2011/11/26	No.36	V	V	V	Page31, Add R2226, R2227 Pull up to +3VS & Reserve R2217, R2218 pull up to +3VALM for SMBUS Leakage issue
	2011/11/28	No.37	V	V	V	Page7, Del R65, R69 & Reserve R45 & R45 with APU_SID & APU_SIC By Pass APU_SID_R & APU_SIC_R for SMBUS Power Leakage Issue
	2011/11/28	No.38	V	V	V	Page31, Reserve C2219, C2210 to +3VALM For SMBUS2 AC Decoupling
	2011/11/28	No.39	V	V	V	Page31, Del C2213, C2214 & Modify R2226, R2227 BOM Structure to @ & R2217, R2218 to POP For SMBUS Power Leakage issue
	2011/11/29	No.40	V	V	V	Page7, Modify R45, R48 BOM Structure to POP & Q9 to @ For SMBUS Power Leakage issue
	2011/11/29	No.41	V	V	V	Page36, Modify R2309 P/N from SD028750180 (7.5K) to SD028150380 (150K) for Power Sequence tuning
	2011/11/29	No.42	V	V	V	Page36, Modify C2316 P/N from SE042104K80 (0.1U) to SE080105K80 (1U) for Power Sequence tuning
	2011/11/29	No.43	V	V	V	Page19, Modify R1450 P/N from SD028150380 (150K) to SD028150380 (150K) for Power Sequence tuning
	2011/11/29	No.44	V	V	V	Page18, Modify C1470 P/N from SE042104K80 (0.1U) to SE080105K80 (1U) for Power Sequence tuning
	2011/11/29	No.45	V	V	V	Page13, Modify U4 P/N from SA000041P00 (MXIC) to SA00003K800 (Winbond) for ROM Part Issue
	2011/11/30	No.46	V	V	V	Page19, Modify C1470 P/N from SE080105K80 (1U) to SE042104K80 (0.1U) for Power Sequence tuning
	2011/11/30	No.47	V	V	V	Page19, Modify R1450 P/N from SD028150380 (150K) to SD028200280 (20K) for Power Sequence tuning
	2011/11/30	No.48	V	V	V	Page19, Modify R1449 P/N from SD028200280 (20K) to SD02830380 (330K) for Power Sequence tuning
	2011/11/30	No.49	V	V	V	Page35, unmount R2481 and mount R2482 for LID SW function reserved
	2011/12/02	No.50	V	V	V	Page12, Modify C129 P/N from SE071150J80 (15P) to SE071220J80 (22P) For Crystal Clock Tuning
	2011/12/02	No.51	V	V	V	Page12, Modify C130 P/N from SE071150J80 (15P) to SE071270J80 (27P) For Crystal Clock Tuning
	2011/12/02	No.52	V	V	V	Page12, Modify C131, C134 P/N from SE071270J80 (27P) to SE071330J80 (33P) For Crystal Clock Tuning
	2011/12/02	No.53	V	V	V	Page18, Modify C1445, C1446 P/N from SE071120J80 (12P) to SE071200J80 (20P) For Crystal Clock Tuning
	2011/12/05	No.54	V	V	V	Page26, Modify C2144, C2145 BOM Structure to @ for DMIC no function issue
MEMO	2011/12/09	No.55	V			Page35, unmount R2482 and mount R2481 for LID SW function implement when SMT
	2011/12/09	power				power schematics 20110208.dsn

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Phase	Date	No.	BOM	Sch	Layout	Description
SIT	2012/01/03	No.1	V	V	V	Page31, Add R2228 connect from MAINPWON_R to MAINPWON for Power Circuit update
	2012/01/03	No.2	V	V	V	Page31, Modify R2236 BOM Structure from POP to @ for +3VS Power Leakage Issue
	2012/01/04	No.3	V	V	V	Page7, delete Q9, short and remove 0 ohm: R45&R48
	2012/01/04	No.4	V	V	V	Page7,9,13, short and remove R64&R68, change Page13 net name ML_VGA_HPD, change page7 net name LVDS_HPD
	2012/01/04	No.5	V	V	V	Page15, Modify +VDDCR_11V_USB power source from +1.1VALW to +1.1V_FCH for reduce power consumption
	2012/01/04	No.6	V	V	V	Page15, Modify +VDDAN_11_SSUSB & +VDDCR_11_SSUSB power source from +1.1VALW to +1.1V_FCH for reduce power consumption
	2012/01/04	No.7	V	V	V	Page15, Modify +VDDAN_11_SSUSB power source from +3V_FCH to +3VALW for reduce power consumption
	2012/01/04	No.8	V	V	V	Page15, Modify +VDDXL_3.3V power source from +3V_FCH to +3VALW for reduce power consumption
	2012/01/04	No.9	V	V	V	Page15, Modify +VDDPL_11_SYS_S power source from +1.1VALW to +1.1V_FCH for reduce power consumption
	2012/01/04	No.10	V	V	V	Page15, Modify +VDDAN_33_HWM power source from +3V_FCH to +3VALW for reduce power consumption
	2012/01/04	No.11	V	V	V	Page15, Modify +VDDAN_33_HWM power source from +3V_FCH to +3VALW for reduce power consumption
	2012/01/04	No.12	V	V	V	Page36, Add R2314,R2318,R2320,Q2311 BOM Structure from @ to POP for Reduce Power Consumption
	2012/01/04	No.13	V	V	V	Page36, Add Q2313,Q2314,U2304,C2309,C2312,C2321,R2323,R2310,R2324 for +3VALW to +3V_FCH Circuit (Reduce Power Consumption)
	2012/01/04	No.14	V	V	V	Page36, Add Q2316,Q2309,U2303,C2317,C2320,C2318,C2319,R2322,R2317 for +1.1VALW to +1.1V_FCH Circuit (Reduce Power Consumption)
	2012/01/04	No.15	V	V	V	Page15, Remove R207 for component part reduce
	2012/01/04	No.16	V	V	V	Page32, Remove R471 & R472 for component part reduce
	2012/01/04	No.17	V	V	V	Page29, Remove R1106,R1107,R1119,R1134,R1109 for component part reduce
	2012/01/04	No.18	V	V	V	Page35, Remove R2465,R2466 for component part reduce
	2012/01/04	No.19	V	V	V	Page33, Reserve R2485 & R2485 to connect EC_SMB_CK2 & EC_SMB_DA2 for Lenovo Multi-Touch function
	2012/01/04	No.20	V	V	V	Page15, Modify +VDDAN_33_HWM power source from +3VALW to +3V_FCH for reduce power consumption
	2012/01/04	No.21	V	V	V	Page26, Del R2176 to connect to EC_INVFWM for common QILEX
	2012/01/05	No.22	V	V	V	Page14, Add R146 & R148 for component part reduce
	2012/01/05	No.23	V	V	V	Page15, Modify +VDDAN_33_HWM power source from +3VALW to +3V_FCH for component part reduce
	2012/01/05	No.24	V	V	V	Page36, Modify +1.1V_FCH netname to +1.1VS_FCH for component part reduce
	2012/01/05	No.25	V	V	V	Page15, Modify +VDDAN_11_USB_S power source from +1.1V_FCH to +1.1VS_FCH for reduce power consumption
	2012/01/05	No.26	V	V	V	Page15, Modify +VDDCR_11V_USB power source from +1.1V_FCH to +1.1VS_FCH for reduce power consumption
	2012/01/05	No.27	V	V	V	Page15, Modify +VDDAN_11_SSUSB & +VDDCR_11_SSUSB power source from +1.1V_FCH to +1.1VS_FCH for reduce power consumption
	2012/01/05	No.28	V	V	V	Page15, Modify +VDDIO_33_S power source from +3VALW to +3VS_FCH for reduce power consumption
	2012/01/05	No.29	V	V	V	Page15, Modify +VDDXL_3.3V power source from +3VALW to +3VS_FCH for reduce power consumption
	2012/01/05	No.30	V	V	V	Page15, Modify +VDDPL_11_SYS_S power source from +1.1V_FCH to +1.1VS_FCH for reduce power consumption
	2012/01/05	No.31	V	V	V	Page15, Modify +VDDAN_33_HWM power source from +3VALW to +3V_FCH for reduce power consumption
	2012/01/05	No.32	V	V	V	Page29, Remove R1108,R1135,R1110,C1127 for component part reduce
	2012/01/05	No.33	V	V	V	Page31, Remove Pin25 EC_INVNT_PWM for Circuit Common
	2012/01/05	No.34	V	V	V	Page31, Modify EC_U2200 I1Pin from +3VALW_EC to +3VLP for S4 LID Function (common QILEX)
	2012/01/05	No.35	V	V	V	Page15, Modify +VDDAN_33_HWM power source from +3VALW to +3V_FCH for component part reduce
	2012/01/05	No.36	V	V	V	Page15, Modify +VDDAN_33_USB power source from +3VS_FCH to +3V_FCH for reduce power consumption
	2012/01/05	No.37	V	V	V	Page15, Modify +VDDPL_33_SSUSB_S power source from +3VS_FCH to +3V_FCH for reduce power consumption
	2012/01/05	No.38	V	V	V	Page15, Modify +VDDPL_33_SSUSB_S power source from +3VS_FCH to +3V_FCH for reduce power consumption
	2012/01/05	No.39	V	V	V	Page15, Modify +VDDPL_33_USB_S power source from +3V_FCH to +3VALW for reduce power consumption
	2012/01/05	No.40	V	V	V	Page15, Modify +VDDIO_33_S power source from +3V_FCH to +3VALW for reduce power consumption
	2012/01/05	No.41	V	V	V	Page15, Modify +VDDAN_33_HWM power source from +3V_FCH to +3VALW for reduce power consumption
	2012/01/05	No.42	V	V	V	Page36, Add R2302 from +1.1VALW to +1.1V_FCH for reduce power consumption
	2012/01/05	No.43	V	V	V	Page36, Modify U2304 Power source from +3V_FCH to +3V for reduce power consumption
	2012/01/05	No.44	V	V	V	Page36, Add J2303 from +3VALW to +3V for reduce power consumption
	2012/01/05	No.45	V	V	V	Page36, Modify U2303 Power source from +1.1V_FCH to +1.1V for reduce power consumption
	2012/01/05	No.46	V	V	V	Page36, Modify J2302 From +1.1V_FCH to +1.1V for reduce power consumption
	2012/01/05	No.47	V	V	V	Page15, Modify +VDDAN_11_USB_S power source from +1.1V_FCH to +1.1V for reduce power consumption
	2012/01/05	No.48	V	V	V	Page15, Modify +VDDCR_11V_USB power source from +1.1V_FCH to +1.1V for reduce power consumption
	2012/01/05	No.49	V	V	V	Page15, Modify +VDDAN_11_SSUSB & +VDDCR_11_SSUSB power source from +1.1V_FCH to +1.1V for reduce power consumption
	2012/01/05	No.50	V	V	V	Page15, Modify +VDDPL_11_SYS_S power source from +1.1V_FCH to +1.1V for reduce power consumption
	2012/01/05	No.51	V	V	V	Page15, Modify +VDDAN_33_USB power source from +3V_FCH to +3V for reduce power consumption
	2012/01/05	No.52	V	V	V	Page15, Modify +VDDPL_33_SSUSB_S power source from +3V_FCH to +3V for reduce power consumption
	2012/01/05	No.53	V	V	V	Page15, Modify +VDDPL_33_USB_S power source from +3V_FCH to +3V for reduce power consumption
	2012/01/05	No.54	V	V	V	Page15, Modify +VDDIO_33_S power source from +3VALW to +3V_FCH for reduce power consumption
	2012/01/05	No.55	V	V	V	Page15, Modify +VDDAN_33_HWM power source from +3VALW to +3V_FCH for reduce power consumption
	2012/01/06	No.56	V	V	V	Page15, Modify +VDDXL_3.3V power source from +3V_FCH to +3V for reduce power consumption
	2012/01/09	No.57	V	V	V	Page33, Add R2493,R2492,R2491,R2494,Q2403,Q2400,C2494,C2493 for AOAC Power Circuit
	2012/01/09	No.58	V	V	V	Page31, U2200 add netname FCH_PWR_EN# on Pin70 for +3V & +1.1V Power Control
	2012/01/09	No.59	V	V	V	Page36, Add R2325 from FCH_PWR_EN# to FCH_PWR_EN# for +3V & +1.1V Power Control
	2012/01/09	No.60	V	V	V	Page36, Add FCH_PWR_EN#_R on Q2313.2,Q2314.2,Q2315.2,Q2309.2 for +3V & +1.1V Power Control Enable Option
	2012/01/09	No.61	V	V	V	Page33, Modify JMIN11 pin1 from FCH_PCIE_WAKE# to WLAN_WAKE# for AOAC Function
	2012/01/09	No.62	V	V	V	Page31, Modify U2200 Pin26 from EAPD_R to WLAN_WAKE# for AOAC Function
	2012/01/09	No.63	V	V	V	Page31, Add U2200 Pin19 from NC to EAPD_R for Audio Function
	2012/01/09	No.64	V	V	V	Page31, Add U2200 Pin91 from NC to AOAC_WLAN for AOAC Function
	2012/01/10	No.65	V	V	V	Page31, Modify U2200 Pin19 net name from ODD_DA# to WL_OFF_EC# for Circuit common with Intel
	2012/01/10	No.66	V	V	V	Page30, Del R2435 for component reduce
	2012/01/10	No.67	V	V	V	Page33, Add R2496 & reserve R2495 for RF_OFF# source option
	2012/01/10	No.68	V	V	V	Page33, Modify JMIN11 Pin20 net name from WL_OFF# to RF_OFF# for Circuit common with Intel
	2012/01/10	No.69	V	V	V	Page31, Modify R2205 BOM Structure to @ for Common Circuit with Intel
	2012/01/10	No.70	V	V	V	Page31, Modify R2232,R2230 from 10K to 100K & Modify R2202,R2230,R2232 pull up from +3VALW_EC to +3VALW for Common Circuit with Intel
	2012/01/11	No.71	V	V	V	Page31, Modify L2200.1 Power Source from +3VALW to +3VALW_EC for EC_AVCC Power Leakage Issue
	2012/01/11	No.72	V	V	V	Page12, BRDID Table update for SIT Build
	2012/01/11	No.73	V	V	V	Page31, Modify R2209 from 18K to 33K for FVT BRDID update
	2012/01/11	No.74	V	V	V	Page26, Modify R2166 P/N from SD028330080 (33ohm) to SD034499180 (4.99K) for logo led brightness fine tune
	2012/01/11	No.75	V	V	V	Page35, Remove R2469 for logo led brightness fine tune
MEMO	2012/01/11	No.76	V	V	V	Page18, Modify C1445,C1446 P/N from SE071200JN0 to SE071200J80 for FVT SMT Memo
	2012/01/11	No.77	V	V	V	Page36, Modify C2316 P/N from SE080105K80 to SE0000069L0 for FVT SMT Memo
	2012/01/11	No.78	V	V	V	Page26, Add C2144, C2145 P/N SE071220J80 (22P) for FVT SMT Memo
	2012/01/11	No.79	V	V	V	Page36, Add Q2317 to Replace U2303 for +1.1V Power Mos layout space not enough issue
	2012/01/11	No.80	V	V	V	Page36, Add Q2318 to Replace U2304 for +3V Power Mos layout space not enough issue
	2012/01/11	No.81	V	V	V	Page29, Modify R1102,R1104,R1105 BOM Structure to @ for Vendor suggestion
	2012/01/12	No.82	V	V	V	Page36, Modify R2323.1 & R2322.1 from +VSB to +5VALW for VGS over spec issue
	2012/01/12	No.83	V	V	V	Page36, Modify Q2317 & Q2318 P/N: from SB0000L0000 to SB923050030 for VGS over spec issue
	2012/01/12	No.84	V	V	V	Page31,35 Modify U2200 Pin70 Net name from FCH_PWR_EN# to FCH_PWR_EN# for +3V & +1.1V power control solution change
	2012/01/12	No.85	V	V	V	Page36, Modify R2325 to POP from FCH_PWR_EN to FCH_PWR_EN# for +3V & +1.1V Power Control
	2012/01/12	No.86	V	V	V	Page36, Delete R2314,R2318,R2320,Q2311 for Reduce Power Consumption
	2012/01/16	No.87	V	V	V	Page31, Modify R2230 BOM Structure from POP to @ for double pull up error
	2012/01/16	No.88	V	V	V	Page31, Modify R2208 BOM Structure from POP to @ for internal pull high solution
	2012/01/16	No.89	V	V	V	Page36, Modify Q2313,Q2314,U2304,C2309,C2312,C2321,R2323,R2310,R2324 to @ for +3VALW to +3V_FCH Circuit (Reduce Power Consumption)
	2012/01/16	No.90	V	V	V	Page36, Modify Q2316,Q2309,U2303,C2317,C2320,C2318,C2319,R2322,R2317 to @ for +1.1VALW to +1.1V_FCH Circuit (Reduce Power Consumption)

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