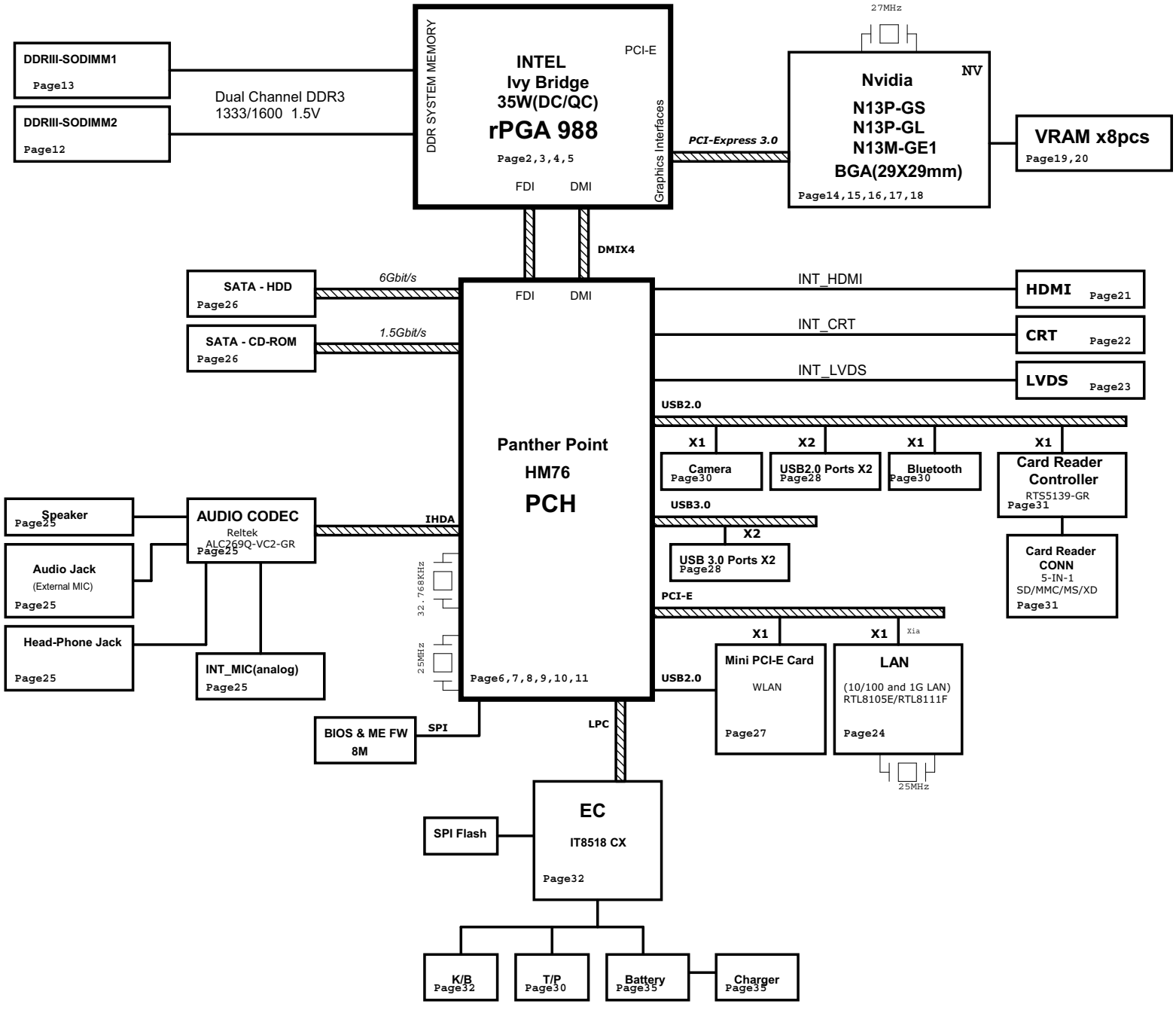
http://adf.ly/3o8pJ

LZ2/LZ2A (Z480) Intel Chief River Platform (Optimus) Block Diagram

01



PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Front page	1A

Date: Wednesday, November 30, 2011 Sheet 1 of 45

Ivy Bridge Processor (DMI,PEG,FDI)

http://adf.ly/3o8pJ

PEG_COMP connect to PIN J22 W:12mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.

[4,6,7,8,10,33,34,38,43] +1.05V_PCH
[4,10,12,13,33,34,37,43] +1.5V_SUS
[6,7,8,9,10,27,31,34] +3V_S5
[4,33] +1.5V_CPU

02

U36A

DMI
[6] DMI_TXN0 B27 DMI_RX#[0]
[6] DMI_TXN1 B25 DMI_RX#[1]
[6] DMI_TXN2 A25 DMI_RX#[2]
[6] DMI_TXN3 B24 DMI_RX#[3]
[6] DMI_TXP0 B28 DMI_RX[0]
[6] DMI_TXP1 B26 DMI_RX[1]
[6] DMI_TXP2 A24 DMI_RX[2]
[6] DMI_TXP3 B23 DMI_RX[3]
[6] DMI_RXN0 G21 DMI_TX#[0]
[6] DMI_RXN1 E22 DMI_TX#[1]
[6] DMI_RXN2 F21 DMI_TX#[2]
[6] DMI_RXN3 D21 DMI_TX#[3]
[6] DMI_RXP0 G22 DMI_TX[0]
[6] DMI_RXP1 D22 DMI_TX[1]
[6] DMI_RXP2 F20 DMI_TX[2]
[6] DMI_RXP3 C21 DMI_TX[3]

FDI
[6] FDI_TXN0 A21 FDI0_TX#[0]
[6] FDI_TXN1 H19 FDI0_TX#[1]
[6] FDI_TXN2 E19 FDI0_TX#[2]
[6] FDI_TXN3 F18 FDI0_TX#[3]
[6] FDI_TXN4 B21 FDI1_TX#[0]
[6] FDI_TXN5 C20 FDI1_TX#[1]
[6] FDI_TXN6 D18 FDI1_TX#[2]
[6] FDI_TXN7 E17 FDI1_TX#[3]
[6] FDI_TXP0 A22 FDI0_TX[0]
[6] FDI_TXP1 G19 FDI0_TX[1]
[6] FDI_TXP2 E20 FDI0_TX[2]
[6] FDI_TXP3 G18 FDI0_TX[3]
[6] FDI_TXP4 B20 FDI1_TX[0]
[6] FDI_TXP5 C19 FDI1_TX[1]
[6] FDI_TXP6 D19 FDI1_TX[2]
[6] FDI_TXP7 F17 FDI1_TX[3]
[6] FDI_FSYNC0 J18 FDI0_FSYNC
[6] FDI_FSYNC1 J17 FDI1_FSYNC
[6] FDI_INT H20 FDI_INT
[6] FDI_LSYNC0 J19 FDI0_LSYNC
[6] FDI_LSYNC1 H17 FDI1_LSYNC

eDP
eDP_COMP A18 eDP_COMPIO
INT_eDP_HPD_Q B16 eDP_HPD
A17 eDP_ICOMPO
C15 eDP_AUX
D15 eDP_AUX#
C17 eDP_TX[0]
E16 eDP_TX[1]
C16 eDP_TX[2]
G15 eDP_TX[3]
C18 eDP_TX[0]
E16 eDP_TX[1]
D16 eDP_TX[2]
E15 eDP_TX[3]

eDP_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils. eDP_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.

Ivy Bridge_rPGA_2DPC_Rev0p61

PCI EXPRESS* - GRAPHICS

PEG_ICOMPI J22 PEG_COMP
PEG_ICOMPO J21
PEG_RCOMPO H22

PEG_RXN[0..15] [14]
PEG_RX#[0] K33 PEG_RXN0
PEG_RX#[1] M35 PEG_RXN1
PEG_RX#[2] L34 PEG_RXN2
PEG_RX#[3] J35 PEG_RXN3
PEG_RX#[4] J32 PEG_RXN4
PEG_RX#[5] H34 PEG_RXN5
PEG_RX#[6] H31 PEG_RXN6
PEG_RX#[7] G33 PEG_RXN7
PEG_RX#[8] G30 PEG_RXN8
PEG_RX#[9] F35 PEG_RXN9
PEG_RX#[10] E34 PEG_RXN10
PEG_RX#[11] E32 PEG_RXN11
PEG_RX#[12] D33 PEG_RXN12
PEG_RX#[13] D31 PEG_RXN13
PEG_RX#[14] B33 PEG_RXN14
PEG_RX#[15] C32 PEG_RXN15

PEG_RXP[0..15] [14]
PEG_RX[0] J33 PEG_RXP0
PEG_RX[1] L35 PEG_RXP1
PEG_RX[2] K34 PEG_RXP2
PEG_RX[3] H35 PEG_RXP3
PEG_RX[4] K32 PEG_RXP4
PEG_RX[5] G34 PEG_RXP5
PEG_RX[6] G31 PEG_RXP6
PEG_RX[7] F33 PEG_RXP7
PEG_RX[8] F30 PEG_RXP8
PEG_RX[9] E35 PEG_RXP9
PEG_RX[10] E33 PEG_RXP10
PEG_RX[11] F32 PEG_RXP11
PEG_RX[12] D34 PEG_RXP12
PEG_RX[13] E31 PEG_RXP13
PEG_RX[14] C33 PEG_RXP14
PEG_RX[15] B32 PEG_RXP15

PEG_TX#[0] M29 PEG_TXN0_C
PEG_TX#[1] M32 PEG_TXN1_C
PEG_TX#[2] M31 PEG_TXN2_C
PEG_TX#[3] L32 PEG_TXN3_C
PEG_TX#[4] L29 PEG_TXN4_C
PEG_TX#[5] K31 PEG_TXN5_C
PEG_TX#[6] K28 PEG_TXN6_C
PEG_TX#[7] J30 PEG_TXN7_C
PEG_TX#[8] J28 PEG_TXN8_C
PEG_TX#[9] H29 PEG_TXN9_C
PEG_TX#[10] G27 PEG_TXN10_C
PEG_TX#[11] E29 PEG_TXN11_C
PEG_TX#[12] F27 PEG_TXN12_C
PEG_TX#[13] D28 PEG_TXN13_C
PEG_TX#[14] F26 PEG_TXN14_C
PEG_TX#[15] E25 PEG_TXN15_C

PEG_TX[0] M28 PEG_TXP0_C
PEG_TX[1] M33 PEG_TXP1_C
PEG_TX[2] M30 PEG_TXP2_C
PEG_TX[3] L31 PEG_TXP3_C
PEG_TX[4] L28 PEG_TXP4_C
PEG_TX[5] K30 PEG_TXP5_C
PEG_TX[6] K27 PEG_TXP6_C
PEG_TX[7] J29 PEG_TXP7_C
PEG_TX[8] J27 PEG_TXP8_C
PEG_TX[9] H28 PEG_TXP9_C
PEG_TX[10] G28 PEG_TXP10_C
PEG_TX[11] E28 PEG_TXP11_C
PEG_TX[12] F28 PEG_TXP12_C
PEG_TX[13] D27 PEG_TXP13_C
PEG_TX[14] E26 PEG_TXP14_C
PEG_TX[15] D25 PEG_TXP15_C

Ivy Bridge Processor (CLK,MISC,JTAG)

U36B

MISC
[7] H_SNB_IVB# C26 PROC_SELECT#
TP12 SKTOCC# AN34 SKTOCC#

THERMAL
TP9 TP_CATERR# AL33 CATERR#
[32] EC_PECI AN33 PECI
[32,41] H_PROCHOT# R168 56_4 H_PROCHOT#_R AL32 PROCHOT#
[9] PM_THRMTRIP# AN32 THERMTRIP#

PWR MANAGEMENT
[6] PM_SYNC R448 *0_4_S PM_SYNC_R AM34 PM_SYNC
[9] H_PWRGOOD R450 *0_4_S H_PWRGOOD_R AP33 UNCOREPWRGOOD
R461 10K_4
C524 *0.1U/10V_4
PM_DRAM_PWRGD_R V8 SM_DRAMPWROK
+1.05V_PCH
R421 75_4
CPU_PLTRST# R444 *43_4 CPU_PLTRST#_R AR33 RESET#
R160 750/F_4
RV11 *EGA-0402
For ESD

Ivy Bridge_rPGA_2DPC_Rev0p61

CLOCKS
BCLK A28 CLK_CPU_BCLKP [8]
BCLK# A27 CLK_CPU_BCLKN [8]
DPLL_REF_CLK A16 DPLL_SSCLKP_R R534 *0_4 CLK_DPLL_SSCLKP [8]
DPLL_REF_CLK# A15 DPLL_SSCLKN_R R537 *0_4 CLK_DPLL_SSCLKN [8]
R533 1K/F_4
R536 1K/F_4 +1.05V_PCH

DDR3 MISC
SM_DRAMRST# R8 CPU_DRAMRST#
SM_RCOMP[0] AK1 SM_RCOMP_0 R565 140/F_4
SM_RCOMP[1] A5 SM_RCOMP_1 R559 25.5/F_4
SM_RCOMP[2] A4 SM_RCOMP_2 R560 200/F_4
SM_RCOMP[0] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils,

JTAG & BPM
PRDY# AP29 XDP_PRDY#
PREQ# AP27 XDP_PREQ# TP19 TP17
TCK AR26 XDP_TCLK
TMS AR27 XDP_TMS TP47
TRST# AP30 XDP_TRST# TP41 TP38
TDI AR28 XDP_TDI_R
TDO AP26 XDP_TDO TP43 TP56
DBR# AL35 XDP_DBRST# XDP_DBRST# [6]
BPM#[0] AT28
BPM#[1] AR29
BPM#[2] AR30
BPM#[3] AT30
BPM#[4] AP32
BPM#[5] AR31
BPM#[6] AT31
BPM#[7] AR32

[12,13] DDR3_DRAMRST# R280 1K/F_4 CPU_DRAMRST#_R
For ESD SC52 *0.1U/10V_4
+1.5V_SUS R278 1K/F_4
R275 *0_4
Q31 ME2N7002E
CPU_DRAMRST#
[8] DRAMRST_CNTRL_PCH R613 0_4
FOR DEEP S3 [32] EC_DRAMRST_GATE R614 *0_4
C289 0.047U/10V_4
R271 4.99K/F_4
[12,13] DRAMRST_CNTRL_DDR

CPU_PLTRST#_R
+3V_S5
R147 1.5K/F_4
C500 *0.1U/10V_4
U32 NC VCC IN GND OUT
[8,14,24,27] PLTRST#
CPU_PLTRST#
*74LVC1G07GW

+3V_S5
C290 *0.1U/10V_4
U15
[6] SYS_PWROK
[6] PM_DRAM_PWRGD R268 *0_4
PM_DRAM_PWRGD_Q
*74AHC1G09GW
R270 *0_4_S
PM_DRAM_PWRGD_Q R272 *3K/F_4
+1.5V_CPU
R274 200/F_4
PM_DRAM_PWRGD_Q R269 130/F_4 PM_DRAM_PWRGD_R
R273 39_4
Q30 ME2N7002E
MAINON# [4,34]

PEG x16 (UMA Non-stuff)

0.1uF AC coupling Caps for PCIE GEN2
0.22uF AC coupling Caps for PCIE GEN3

PEG_TXP[0..15] [14]
PEG_TXP0_C C499 DIS@0.1U/10V/X5R_4 PEG_TXP0
PEG_TXP1_C C475 DIS@0.1U/10V/X5R_4 PEG_TXP1
PEG_TXP2_C C513 DIS@0.1U/10V/X5R_4 PEG_TXP2
PEG_TXP3_C C493 DIS@0.1U/10V/X5R_4 PEG_TXP3
PEG_TXP4_C C487 DIS@0.1U/10V/X5R_4 PEG_TXP4
PEG_TXP5_C C508 DIS@0.1U/10V/X5R_4 PEG_TXP5
PEG_TXP6_C C477 DIS@0.1U/10V/X5R_4 PEG_TXP6
PEG_TXP7_C C504 DIS@0.1U/10V/X5R_4 PEG_TXP7
PEG_TXP8_C C478 DIS@0.1U/10V/X5R_4 PEG_TXP8
PEG_TXP9_C C502 DIS@0.1U/10V/X5R_4 PEG_TXP9
PEG_TXP10_C C481 DIS@0.1U/10V/X5R_4 PEG_TXP10
PEG_TXP11_C C494 DIS@0.1U/10V/X5R_4 PEG_TXP11
PEG_TXP12_C C483 DIS@0.1U/10V/X5R_4 PEG_TXP12
PEG_TXP13_C C491 DIS@0.1U/10V/X5R_4 PEG_TXP13
PEG_TXP14_C C484 DIS@0.1U/10V/X5R_4 PEG_TXP14
PEG_TXP15_C C497 DIS@0.1U/10V/X5R_4 PEG_TXP15

0.1uF AC coupling Caps for PCIE GEN2
0.22uF AC coupling Caps for PCIE GEN3

PEG_TXN[0..15] [14]
PEG_TXN0_C C498 DIS@0.1U/10V/X5R_4 PEG_TXN0
PEG_TXN1_C C474 DIS@0.1U/10V/X5R_4 PEG_TXN1
PEG_TXN2_C C514 DIS@0.1U/10V/X5R_4 PEG_TXN2
PEG_TXN3_C C492 DIS@0.1U/10V/X5R_4 PEG_TXN3
PEG_TXN4_C C486 DIS@0.1U/10V/X5R_4 PEG_TXN4
PEG_TXN5_C C509 DIS@0.1U/10V/X5R_4 PEG_TXN5
PEG_TXN6_C C476 DIS@0.1U/10V/X5R_4 PEG_TXN6
PEG_TXN7_C C503 DIS@0.1U/10V/X5R_4 PEG_TXN7
PEG_TXN8_C C479 DIS@0.1U/10V/X5R_4 PEG_TXN8
PEG_TXN9_C C501 DIS@0.1U/10V/X5R_4 PEG_TXN9
PEG_TXN10_C C480 DIS@0.1U/10V/X5R_4 PEG_TXN10
PEG_TXN11_C C495 DIS@0.1U/10V/X5R_4 PEG_TXN11
PEG_TXN12_C C482 DIS@0.1U/10V/X5R_4 PEG_TXN12
PEG_TXN13_C C490 DIS@0.1U/10V/X5R_4 PEG_TXN13
PEG_TXN14_C C485 DIS@0.1U/10V/X5R_4 PEG_TXN14
PEG_TXN15_C C496 DIS@0.1U/10V/X5R_4 PEG_TXN15

DP & PEG Compensation

+1.05V_PCH R527 24.9/F_4 PEG_COMP

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils
typical impedance = 14.5 mohms

+1.05V_PCH R532 *10K_4 INT_eDP_HPD_Q
+1.05V_PCH R528 24.9/F_4 eDP_COMP

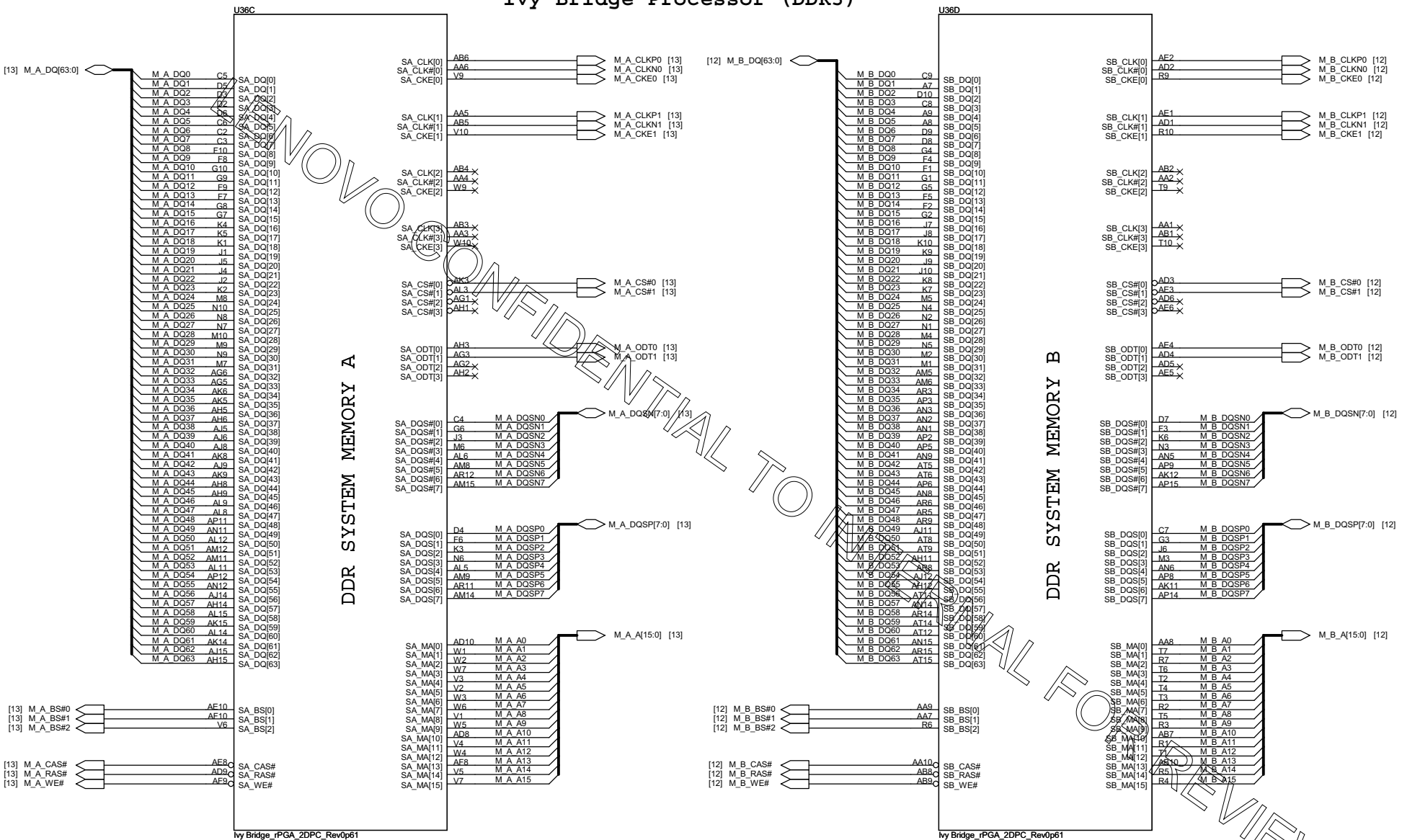
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Processor pull-up(CPU)

+1.05V_PCH
H_PROCHOT# R164 62/F_4
XDP_TDO R178 51_4
XDP_TMS R480 51_4
XDP_TDI_R R477 51_4
XDP_PREQ# R172 *51_4
XDP_TCLK R487 51_4
XDP_TRST# R470 51_4

PROJECT : LZ2A
Quanta Computer Inc.
Size: Document Number: IVY Bridge 1/4 Rev: 1A
Date: Wednesday, November 30, 2011 Sheet 2 of 45

Ivy Bridge Processor (DDR3)



PROJECT : LZ2A			
Quanta Computer Inc.			
Size	Document Number		Rev
	IVY Bridge 2/4		1A
Date: Wednesday, November 30, 2011	Sheet 3	of 45	

Ivy Bridge Processor (GRAPHIC POWER)

[33,41] +VCC_CORE
[2,6,7,8,10,33,34,38,43] +1.05V_PCH
[34] MAINON_15V
[2,10,12,13,33,34,37,43] +1.5V_SUS
[2,33] +1.5V_CPU
[10,27] +1.5V
[7,10,33,34,40] +1.8V
[33,34,39] +0.85V
[33,41] +VCC_GFX

POWER

U36F

CORE SUPPLY

SNB: 55A
IVY: 55A

+VCC_CORE

C218 22U/6.3V_8 C219 22U/6.3V_8 C216 22U/6.3V_8 C220 22U/6.3V_8
22uF_8 x8 Socket TOP cavity
C222 22U/6.3V_8 C221 22U/6.3V_8 C230 22U/6.3V_8 C217 22U/6.3V_8

C519 22U/6.3V_8 C198 22U/6.3V_8 C193 22U/6.3V_8 C175 22U/6.3V_8
C517 22U/6.3V_8 C516 22U/6.3V_8 C520 22U/6.3V_8 C518 22U/6.3V_8

C583 10U/6.3V_8 C576 10U/6.3V_8 C591 10U/6.3V_8 C592 10U/6.3V_8
10uF_8 x10 Socket BOT cavity
C582 10U/6.3V_8 C568 10U/6.3V_8 C574 10U/6.3V_8 C573 10U/6.3V_8

+VCC_CORE:
22uF_8 x8 TOP Socket cavity
22uF_8 x8 TOP Socket edge
10uF_8 x10 BOT Socket cavity

C575 10U/6.3V_8 C584 10U/6.3V_8

VCC1 AG35 VCC2 AG34 VCC3 AG33 VCC4 AG32 VCC5 AG31 VCC6 AG30 VCC7 AG29 VCC8 AG28 VCC9 AG27 VCC10 AG26 VCC11 AF35 VCC12 AF34 VCC13 AF33 VCC14 AF32 VCC15 AF31 VCC16 AF29 VCC17 AF28 VCC18 AF27 VCC19 AF26 VCC20 AD35 VCC21 AD34 VCC22 AD33 VCC23 AD32 VCC24 AD31 VCC25 AD30 VCC26 AD29 VCC27 AD28 VCC28 AD27 VCC29 AD26 VCC30 AC35 VCC31 AC34 VCC32 AC33 VCC33 AC32 VCC34 AC31 VCC35 AC30 VCC36 AC29 VCC37 AC28 VCC38 AC27 VCC39 AC26 VCC40 AA35 VCC41 AA34 VCC42 AA33 VCC43 AA32 VCC44 AA31 VCC45 AA30 VCC46 AA29 VCC47 AA28 VCC48 AA27 VCC49 AA26 VCC50 Y35 VCC51 Y34 VCC52 Y33 VCC53 Y32 VCC54 Y31 VCC55 Y30 VCC56 Y29 VCC57 Y28 VCC58 Y27 VCC59 Y26 VCC60 V35 VCC61 V34 VCC62 V33 VCC63 V32 VCC64 V31 VCC65 V30 VCC66 V29 VCC67 V28 VCC68 V27 VCC69 V26 VCC70 U35 VCC71 U34 VCC72 U33 VCC73 U32 VCC74 U31 VCC75 U30 VCC76 U29 VCC77 U28 VCC78 U27 VCC79 U26 VCC80 R35 VCC81 R34 VCC82 R33 VCC83 R32 VCC84 R31 VCC85 R30 VCC86 R29 VCC87 R28 VCC88 R27 VCC89 R26 VCC90 P35 VCC91 P34 VCC92 P33 VCC93 P32 VCC94 P31 VCC95 P30 VCC96 P29 VCC97 P28 VCC98 P27 VCC99 P26 VCC100

PEG AND DDR

+1.05V_PCH

SNB: 8.5A
IVY: 8.5A

VCCIO1 AH13 VCCIO2 AH10 VCCIO3 AG10 VCCIO4 AC10 VCCIO5 Y10 VCCIO6 U10 VCCIO7 P10 VCCIO8 L10 VCCIO9 J14 VCCIO10 J13 VCCIO11 J12 VCCIO12 J11 VCCIO13 H14 VCCIO14 H12 VCCIO15 H11 VCCIO16 G14 VCCIO17 G13 VCCIO18 G12 VCCIO19 F14 VCCIO20 F13 VCCIO21 F12 VCCIO22 F11 VCCIO23 E14 VCCIO24 E12 VCCIO25 E11 VCCIO26 D14 VCCIO27 D13 VCCIO28 D12 VCCIO29 D11 VCCIO30 C14 VCCIO31 C13 VCCIO32 C12 VCCIO33 C11 VCCIO34 B14 VCCIO35 B12 VCCIO36 A14 VCCIO37 A13 VCCIO38 A12 VCCIO39 A11 VCCIO40 J23

C246 22U/6.3V_8 C251 22U/6.3V_8 C247 22U/6.3V_8 C245 22U/6.3V_8 C244 22U/6.3V_8 C243 22U/6.3V_8

C598 22U/6.3V_8 C597 22U/6.3V_8 C596 22U/6.3V_8 C248 22U/6.3V_8
22uF_8 x7 TOP Socket cavity
22uF_8 x5 BOT Socket cavity

C602 22U/6.3V_8 C601 22U/6.3V_8 C252 *22U/6.3V_8 C249 *22U/6.3V_8 C600 *22U/6.3V_8
22uF (Reserved)

C593 22U/6.3V_8 C250 22U/6.3V_8 C262 *22U/6.3V_8 C599 *22U/6.3V_8

+1.05V_PCH R526 *0_4_S +1.05V_PCH

SVID

VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 H_CPU_SVIDCLK
VIDSOUT AJ28 H_CPU_SVIDDAT

SENSE LINES

VCC_SENSE AJ35 R455 100_4 +VCC_CORE
VSS_SENSE AJ34 R454 100_4
VCC_SENSE [41]
VSS_SENSE [41]

VCCIO_SENSE B10 VTT_SENSE
VSS_SENSE_VCCIO A10 VSSP_SENSE
VTT_SENSE [38]
VSSP_SENSE [38]

+1.05V_PCH
VTT_SENSE R550 10/F_4
VSSP_SENSE R556 10/F_4

Ivy Bridge_rPGA_2DPC_Rev0p61

POWER

U36G

GRAPHICS

SNB: 21.5A
IVY: 33A

+VCC_GFX

C580 22U/6.3V_8 C586 22U/6.3V_8 C590 22U/6.3V_8 C210 22U/6.3V_8
C226 22U/6.3V_8 C232 22U/6.3V_8 C236 22U/6.3V_8 C239 22U/6.3V_8
C237 22U/6.3V_8 C565 22U/6.3V_8 C241 22U/6.3V_8 C240 22U/6.3V_8

+VCC_GFX:
22uF_8 x2 TOP Socket cavity
22uF_8 x4 TOP Socket edge
22uF_8 x2 BOT Socket cavity
22uF_8 x4 BOT Socket edge

VAXG1 AT24 VAXG2 AT23 VAXG3 AT21 VAXG4 AT20 VAXG5 AT18 VAXG6 AT17 VAXG7 AR24 VAXG8 AR23 VAXG9 AR21 VAXG10 AR20 VAXG11 AR18 VAXG12 AR17 VAXG13 AP24 VAXG14 AP23 VAXG15 AP21 VAXG16 AP20 VAXG17 AP18 VAXG18 AP17 VAXG19 AN24 VAXG20 AN23 VAXG21 AN21 VAXG22 AN20 VAXG23 AN18 VAXG24 AN17 VAXG25 AM24 VAXG26 AM23 VAXG27 AM21 VAXG28 AM20 VAXG29 AM18 VAXG30 AM17 VAXG31 AL24 VAXG32 AL23 VAXG33 AL21 VAXG34 AL20 VAXG35 AL18 VAXG36 AL17 VAXG37 AK24 VAXG38 AK23 VAXG39 AK21 VAXG40 AK20 VAXG41 AK18 VAXG42 AK17 VAXG43 AJ24 VAXG44 AJ23 VAXG45 AJ21 VAXG46 AJ20 VAXG47 AJ18 VAXG48 AJ17 VAXG49 AH24 VAXG50 AH23 VAXG51 AH21 VAXG52 AH20 VAXG53 AH18 VAXG54 AH17

1.8V RAIL

+1.8V

C280 10U/6.3V_6 C603 1U/6.3V_4 C605 1U/6.3V_4 + C284 *330U/2.5V_7343

VCCPLL1 B6 VCCPLL2 A6 VCCPLL3 A2

CPU VCCPL
SNB 45W:1.5A
330uF/7mohm x 1
10uF x 1
1uF x 2

Ivy Bridge_rPGA_2DPC_Rev0p61

SENSE LINES

VAXG_SENSE AK35 R423 100/F_4 +VCC_GFX
VSSAXG_SENSE AK34 R425 100/F_4
TP34 TP36
VCC_AXG_SENSE [41]
VSS_AXG_SENSE [41]

VREF

SM_VREF AL1 +VDDR_REF_CPU
CAD Note: +VDDR_REF_CPU should have 10 mil trace width
SA_DIMM_VREFDQ B4
SB_DIMM_VREFDQ D1
R561 *1K_4
R564 *1K_4
SMDDR_VREF_DQ0_M3 [13]
SMDDR_VREF_DQ1_M3 [12]

DDR3 -1.5V RAILS

SNB: 5A
IVY: 5A

VDDQ1 AF7 VDDQ2 AF4 VDDQ3 AF1 VDDQ4 AC7 VDDQ5 AC4 VDDQ6 AC1 VDDQ7 Y7 VDDQ8 Y4 VDDQ9 Y1 VDDQ10 U7 VDDQ11 U4 VDDQ12 U1 VDDQ13 P7 VDDQ14 P4 VDDQ15 P1

C282 10U/6.3V_6 C287 10U/6.3V_6 C281 10U/6.3V_6 C283 10U/6.3V_6
330uF x1, 10uF_8 x6 Socket BOT edge.
C279 10U/6.3V_6 C286 10U/6.3V_6 + C285 220U/2.5V_7343
+1.5V_CPU

SA RAIL

SNB: 6A
IVY: 6A

VCCSA1 M27 VCCSA2 M26 VCCSA3 L26 VCCSA4 J26 VCCSA5 J25 VCCSA6 J24 VCCSA7 H26 VCCSA8 H25

C231 10U/6.3V_6 C572 10U/6.3V_6 C566 10U/6.3V_6
330uF x1, 10uF_8 x1 Socket BOT edge, 10uF_8 x2 Socket BOT cavity.
+0.85V

MISC

VCCSA_SENSE H23 R610 *0_4_S VCCUSA_SENSE [39]
VCCSA_SEL0 [39]
VCCSA_VID[0] C22 R241 1K_4
VCCSA_VID[1] C24 R235 1K_4
VCCSA_SEL [39]
VCCIO_SEL A19 R521 *0_4 H_VTTVID1 [38]

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK
+1.05V_PCH
Close to VR
R484 54.9/F_4
H_CPU_SVIDCLK R169 *0_4_S VR_SVID_CLK [41]

Place PU resistor close to CPU
+1.05V_PCH
R158 130/F_4

SVID DATA
+1.05V_PCH
Close to VR
R469 130/F_4
H_CPU_SVIDDAT R171 *0_4_S VR_SVID_DATA [41]

Place PU resistor close to CPU
+1.05V_PCH
R157 75_4

SVID ALERT
H_CPU_SVIDALRT# R170 43_4 R156 *0_4_S VR_SVID_ALERT# [41]

+1.5V_CPU +1.5V
R276 *0_8_S
40mile routing

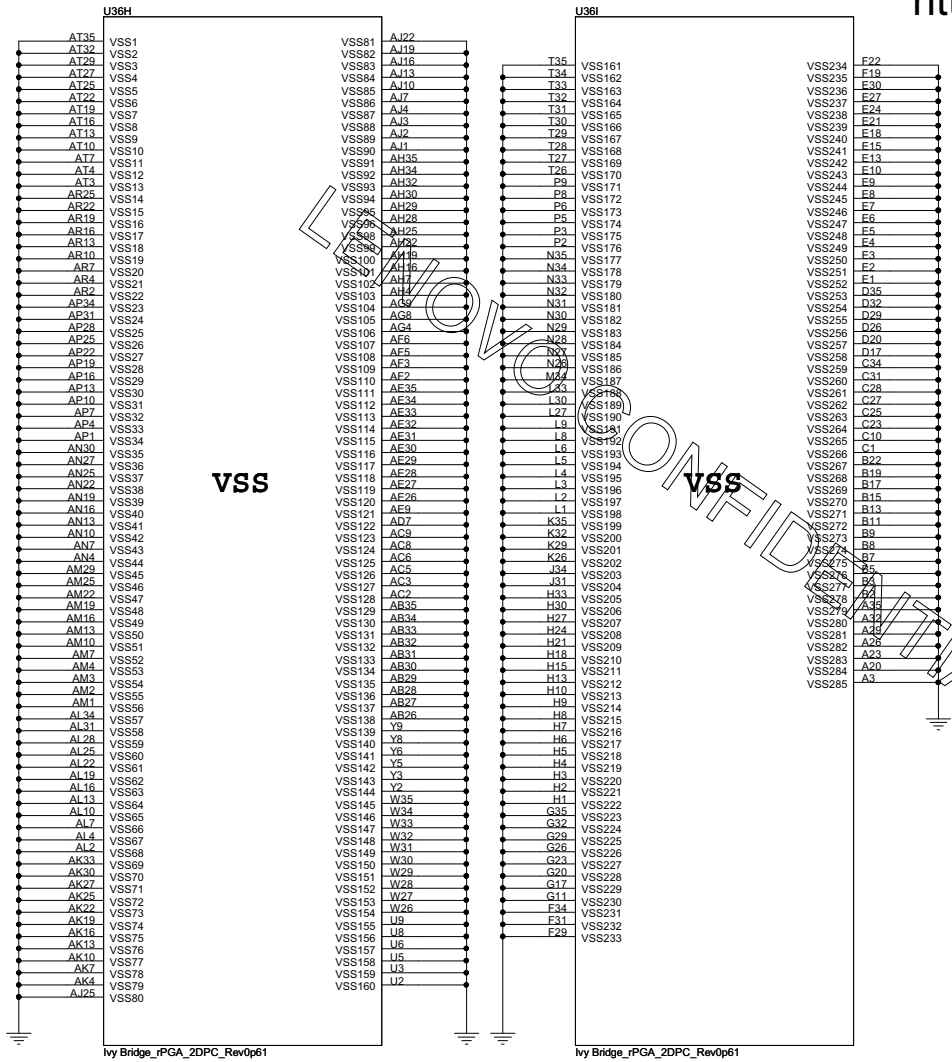
+1.5V_SUS 5A +1.5V_CPU +1.5V_SUS
Q35 AON7406
C293 0.1U/10V_4
C294 0.1U/10V_4
C291 0.1U/10V_4
C292 0.1U/10V_4
Placement close to CPU.
[34] MAINON_15V
C288 470P/25V/X7R_4
R277 220_8
[2,34] MAINON#
Q36 ME2N7002E

[12,13,37] SMDDR_VREF R566 *0_8 +VDDR_REF_CPU
Q51 ME2N7002E
[34] MAINON_15V
R563 100K_4

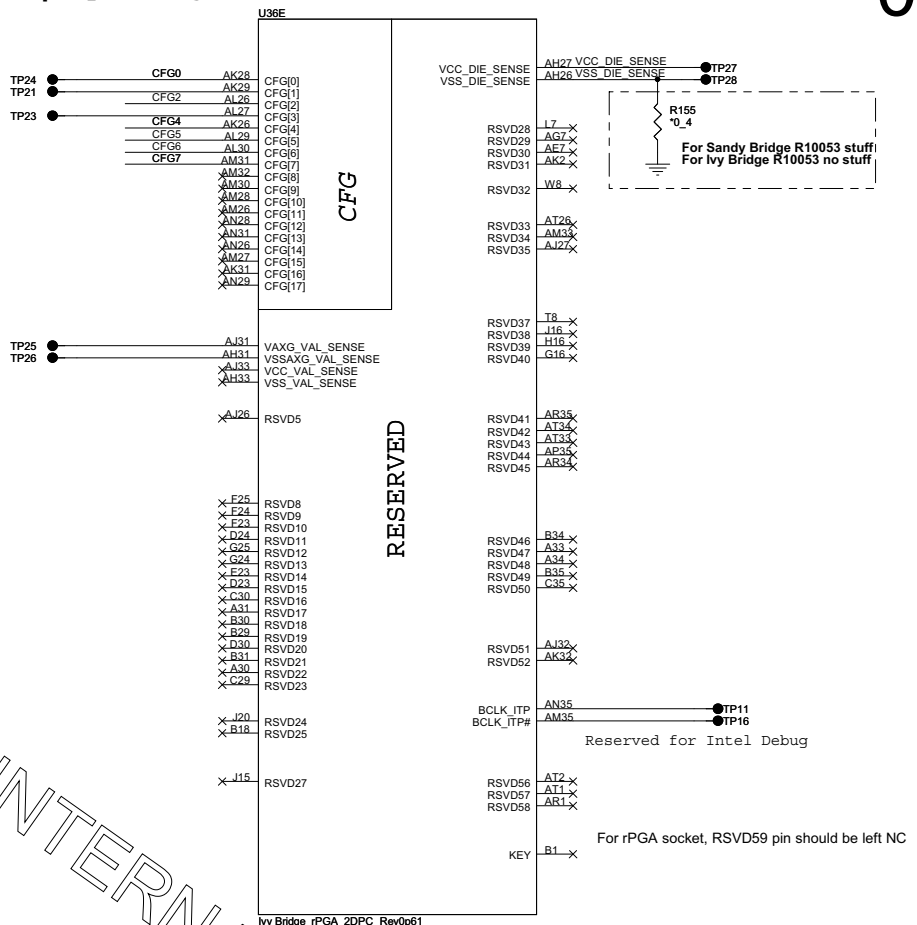
PROJECT : LZ2A
Quanta Computer Inc.
Size: Document Number: IVY Bridge 3/4 Rev: 1A
Date: Wednesday, November 30, 2011 Sheet 4 of 45

Ivy Bridge Processor (GND)

http://adf.ly/3o8pJ



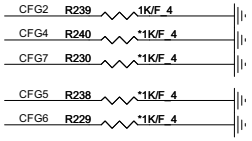
Ivy Bridge Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	IVY Bridge 4/4	1A
Date: Wednesday, November 30, 2011	Sheet 5 of 45	

[2,4,7,8,10,33,34,38,43] +1.05V_PCH
[7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43] +3V
[2,7,8,9,10,27,31,34] +3V_S5
[7,10,32] +3V_RTC

Cougar Point/Panther Point (DMI,FDI,PM)

U13C

DMI0RXN BC24 ← [2] DMI_RXN0
DMI1RXN BE20 ← [2] DMI_RXN1
DMI2RXN BG18 ← [2] DMI_RXN2
DMI3RXN BG20 ← [2] DMI_RXN3
DMI0RXP BE24 ← [2] DMI_RXP0
DMI1RXP BC20 ← [2] DMI_RXP1
DMI2RXP BJ18 ← [2] DMI_RXP2
DMI3RXP BJ20 ← [2] DMI_RXP3
DMI0TXN AW24 → [2] DMI_TXN0
DMI1TXN AW20 → [2] DMI_TXN1
DMI2TXN BB18 → [2] DMI_TXN2
DMI3TXN AY18 → [2] DMI_TXN3
DMI0TXP AY24 → [2] DMI_TXP0
DMI1TXP AY20 → [2] DMI_TXP1
DMI2TXP AY18 → [2] DMI_TXP2
DMI3TXP AU18 → [2] DMI_TXP3
DMI_ZCOMP BJ24
DMI_COMP BG25 ← R543 49.9/F_4 ← +1.05V_PCH
DMI_IRCOMP
DMI_RBIAS BH21 ← R260 750/F_4
DMI2RBIAS

DMI

FDI_RXN0 BJ14 ← FDI_TXN0 [2]
FDI_RXN1 AY14 ← FDI_TXN1 [2]
FDI_RXN2 BE14 ← FDI_TXN2 [2]
FDI_RXN3 BH13 ← FDI_TXN3 [2]
FDI_RXN4 BC12 ← FDI_TXN4 [2]
FDI_RXN5 BJ12 ← FDI_TXN5 [2]
FDI_RXN6 BG10 ← FDI_TXN6 [2]
FDI_RXN7 BG9 ← FDI_TXN7 [2]
FDI_TXP0 BG14 → FDI_TXP0 [2]
FDI_TXP1 BB14 → FDI_TXP1 [2]
FDI_TXP2 BE14 → FDI_TXP2 [2]
FDI_TXP3 BG13 → FDI_TXP3 [2]
FDI_TXP4 BE12 → FDI_TXP4 [2]
FDI_TXP5 BG12 → FDI_TXP5 [2]
FDI_TXP6 BJ10 → FDI_TXP6 [2]
FDI_TXP7 BH9 → FDI_TXP7 [2]
FDI_INT AW16 → FDI_INT [2]
FDI_FSYNC0 AV12 → FDI_FSYNC0 [2]
FDI_FSYNC1 BC10 → FDI_FSYNC1 [2]
FDI_LSYNC0 AV14 → FDI_LSYNC0 [2]
FDI_LSYNC1 BB10 → FDI_LSYNC1 [2]

FDI

FOR DEEP S3
[32] SUSACK# → SUSACK# R620 0_4 → C12 SUSACK#
SUSWARN#_R R436 *0_4
[2] XDP_DBRST# → XDP_DBRST# K3
SYS_PWROK → C522 *1U/6.3V_4, R451 *0_4_S → SYS_PWROK_R P12 SYS_PWROK
R426 *0_4
[32] EC_PWROK → R460 *0_4_S → EC_PWROK_R L22 PWROK
EC_PWROK_R R428 *0_4_S → APWROK_R L10 APWROK
[2] PM_DRAM_PWRGD → PM_DRAM_PWRGD B13 DRAMPWROK
[32] RSMRST# → RSMRST# C21 RSMRST#
FOR DEEP S3
[32] SUSWARN# → R410 0_4 → SUSWARN# R K16 SUSWARN#/SUSPWRDNACK/GPIO30
[32] SIO_PWRBTN# → E20 PWRBTN#
[17,32] AC_PRESENT → R459 *0_4_S → AC_PRESENT_R H20 ACPRESENT / GPIO31
PM_BATLOW# E10 BATLOW# / GPIO72
PM_RI# A10 RI#

System Power Management

+3V_S5
+3V_S5
+3V_S5
+3V_S5
+3V_S5
+3V_S5
+3V_S5
+3V_S5

CLKRUN# / GPIO32 N3 CLKRUN# → CLKRUN# [32]
SUS_STAT# / GPIO61 G8 LPC_PD# → T18
SUSCLK / GPIO62 N14 PCH_SUSCLK → T21
SLP_S5# / GPIO63 D10 SLP_S5# → T17
SLP_S4# H4 → PM_SLP_S4# [32]
SLP_S3# F4 → SIO_SLP_S3# [32]
SLP_A# G10 SLP_A# → T16
SLP_SUS# G16 → SLP_SUS# [10,32]
PMSYNCH AP14 → PM_SYNC [2]
SLP_LAN# / GPIO29 K14 WLAN_AOAC_ON → WLAN_AOAC_ON [27]

DSWVRMEN A18 DSWVREN
FOR DEEP S3
DPWROK E22 ← R615 *0_4 DPWROK, R124 0_4 RSMRST# ← RSMRST# [32]
WAKE# B9 PCIE_WAKE# → PCIE_WAKE# [24,27,32]

CPT_PPT_Rev_0p5

Cougar Point/Panther Point (LVDS,DDI)

U13D

[23] INT_LVDS_BLON → J47 L_BKLTEN
[23] INT_LVDS_VDDEN → M45 L_VDD_EN
[23] PCH_BRIGHT_PWM → P45 L_BKLTCTL
[23] INT_EDIDCLK → T40 L_DDC_CLK
[23] INT_EDIDDAT → K47 L_DDC_DATA
+3VO → R496 2.2K_4, R489 2.2K_4 → T45 L_CTRL_CLK, P39 L_CTRL_DATA
R511 2.37K/F_4 ← LVD_IBG AF37 LVD_IBG
T22 AF36 LVD_VBG
AE48 LVD_VREFH
AE47 LVD_VREFL

[23] INT_TXLCLKOUTN → AK39 LVDSA_CLK#
[23] INT_TXLCLKOUTP → AK40 LVDSA_CLK
[23] INT_TXLOUTN0 → AN48 LVDSA_DATA#0
[23] INT_TXLOUTN1 → AM47 LVDSA_DATA#1
[23] INT_TXLOUTN2 → AK47 LVDSA_DATA#2
AJ48 LVDSA_DATA#3
[23] INT_TXLOUTP0 → AN47 LVDSA_DATA0
[23] INT_TXLOUTP1 → AM49 LVDSA_DATA1
[23] INT_TXLOUTP2 → AK49 LVDSA_DATA2
AJ47 LVDSA_DATA3
AF40 LVDSB_CLK#
AF39 LVDSB_CLK
AH45 LVDSB_DATA#0
AH47 LVDSB_DATA#1
AF49 LVDSB_DATA#2
AF45 LVDSB_DATA#3
AH43 LVDSB_DATA0
AH49 LVDSB_DATA1
AF47 LVDSB_DATA2
AF43 LVDSB_DATA3

LVDS

R place close to PCH
R183 150/F_4 INT_CRT_BLU
R193 150/F_4 INT_CRT_GRE
R192 150/F_4 INT_CRT_RED

[22] INT_CRT_BLU → INT_CRT_BLU N48 → CRT_BLUE
[22] INT_CRT_GRE → INT_CRT_GRE P49 → CRT_GREEN
[22] INT_CRT_RED → INT_CRT_RED T49 → CRT_RED
[22] INT_DDCCLK → T39 CRT_DDC_CLK
[22] INT_DDCDAT → M40 CRT_DDC_DATA
[22] INT_CRT_HSYNC → R176 33_4 → INT_CRT_HSYNC_R M47 → CRT_HSYNC
[22] INT_CRT_VSYNC → R182 33_4 → INT_CRT_VSYNC_R M49 → CRT_VSYNC
DAC_IREF T43
T42 DAC_IREF
R506 1K/F_4 → CRT_IRTN

CRT

SDVO_TVCLKINN AP43
SDVO_TVCLKINP AP45
SDVO_STALLN AM42
SDVO_STALLP AM40
SDVO_INTN AP39
SDVO_INTP AP40
SDVO_CTRLCLK P38 → INT_HDMI_SCL [21]
SDVO_CTRLDATA M39 → INT_HDMI_SDA [21]
DDPB_AUXN AT49
DDPB_AUXP AT47
DDPB_HPD AT40 → INT_HDMI_HPD_Q
DDPB_0N AV42 → INT_HDMI_TXDN2 [21]
DDPB_0P AV40 → INT_HDMI_TXDP2 [21]
DDPB_1N AV45 → INT_HDMI_TXDN1 [21]
DDPB_1P AV46 → INT_HDMI_TXDP1 [21]
DDPB_2N AU48 → INT_HDMI_TXDN0 [21]
DDPB_2P AU47 → INT_HDMI_TXDP0 [21]
DDPB_3N AV47 → INT_HDMI_TXCN [21]
DDPB_3P AV49 → INT_HDMI_TXCP [21]
DDPC_CTRLCLK P46
DDPC_CTRLDATA P42
DDPC_AUXN AP47
DDPC_AUXP AP49
DDPC_HPD AT38 → DDPC_HPD_PU R548 10K_4 → +3V
DDPC_0N AY47
DDPC_0P AY49
DDPC_1N AY43
DDPC_1P AY45
DDPC_2N BA47
DDPC_2P BA48
DDPC_3N BB47
DDPC_3P BB49
DDPD_CTRLCLK M43
DDPD_CTRLDATA M36
DDPD_AUXN AT45
DDPD_AUXP AT43
DDPD_HPD BH41 → DDPD_HPD_PU R547 10K_4 → +3V
DDPD_0N BB43
DDPD_0P BB45
DDPD_1N BF44
DDPD_1P BE44
DDPD_2N BF42
DDPD_2P BE42
DDPD_3N BJ42
DDPD_3P BC42

Digital Display Interface

INT. HDMI
INT. DP

Follow PDG eDP disable guide
Follow PDG eDP disable guide

CPT_PPT_Rev_0p5

INT_HDMI_HPD_Q R535 *0_4_S → INT_HDMI_HPD [21]
R523 *100K_4
R540 100K_4

DPWROK FOR DSW (DEEP S3)

FOR DEEP S3
+3V_DSW
+3VPCU
+3VPCU
+3V_S5 → D28 *RB500V-40 → DPWROK
+3VPCU → D29 *RB500V-40
R616 *10K_4
R617 *10K_4
Q55 *LTC044EUBFS8TL
Q56 *2N7002
C665 *0.1U/10V/X5R_4 add cap to timing tune

System PWR_OK(CLG)

+3V_S5
C171 0.1U/10V_4
U7 TC7SH08FU
[2] SYS_PWROK → SYS_PWROK → DELAY_VR_PWRGOOD [41]
EC_PWROK
R117 *0_4
R112 100K_4

+3V_RTC
R127 330K_4
DSWVREN
R140 *330K_4

On Die DSW VR Enable
High = Enable (Default)
Low = Disable

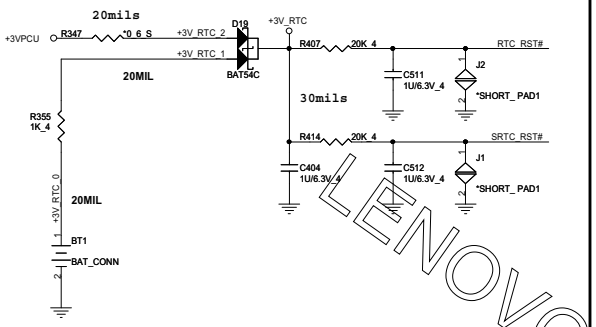
PCH Pull-high/low(CLG)

+3V
+3V_S5
CLKRUN# R198 8.2K_4
XDP_DBRST# R180 1K_4
R173 *1K_4
RSMRST# R139 10K_4
SYS_PWROK R457 100K_4
PM_RI# R142 10K_4
PM_BATLOW# R445 8.2K_4
PCIE_WAKE# R146 10K_4
WLAN_AOAC_ON R418 10K_4
For AOAC
SUSWARN# R409 10K_4
AC_PRESENT R442 10K_4
PM_DRAM_PWRGD R435 *200/F_4

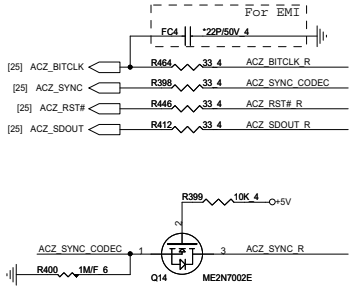
PROJECT : LZ2A
Quanta Computer Inc.
Size Document Number Rev 1A
Panther Point 1/6
Date: Wednesday, November 30, 2011 Sheet 6 of 45

http://adf.ly/3o8pJ

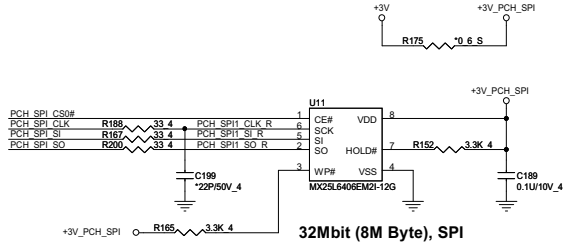
RTC Circuitry(RTC)



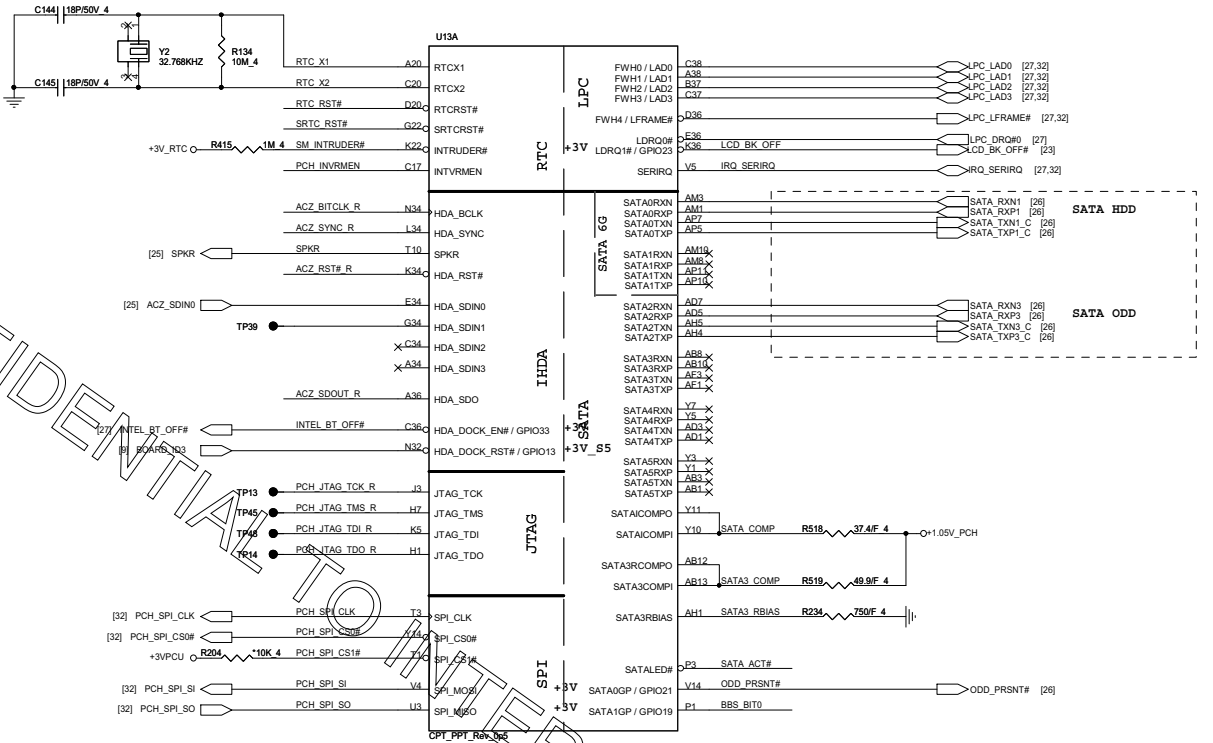
HDA Bus(CLG)



PCH Dual SPI (CLG)

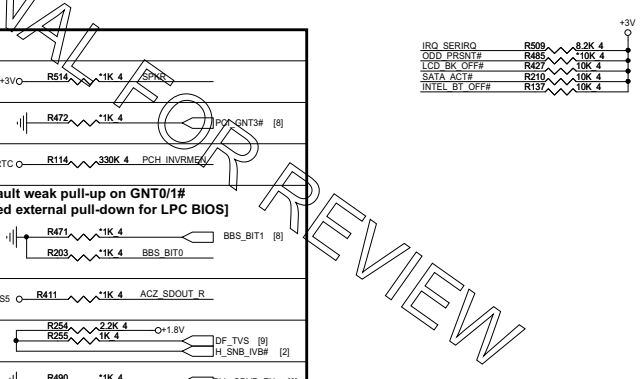


Cougar Point/Panther Point (HDA,JTAG,SATA)



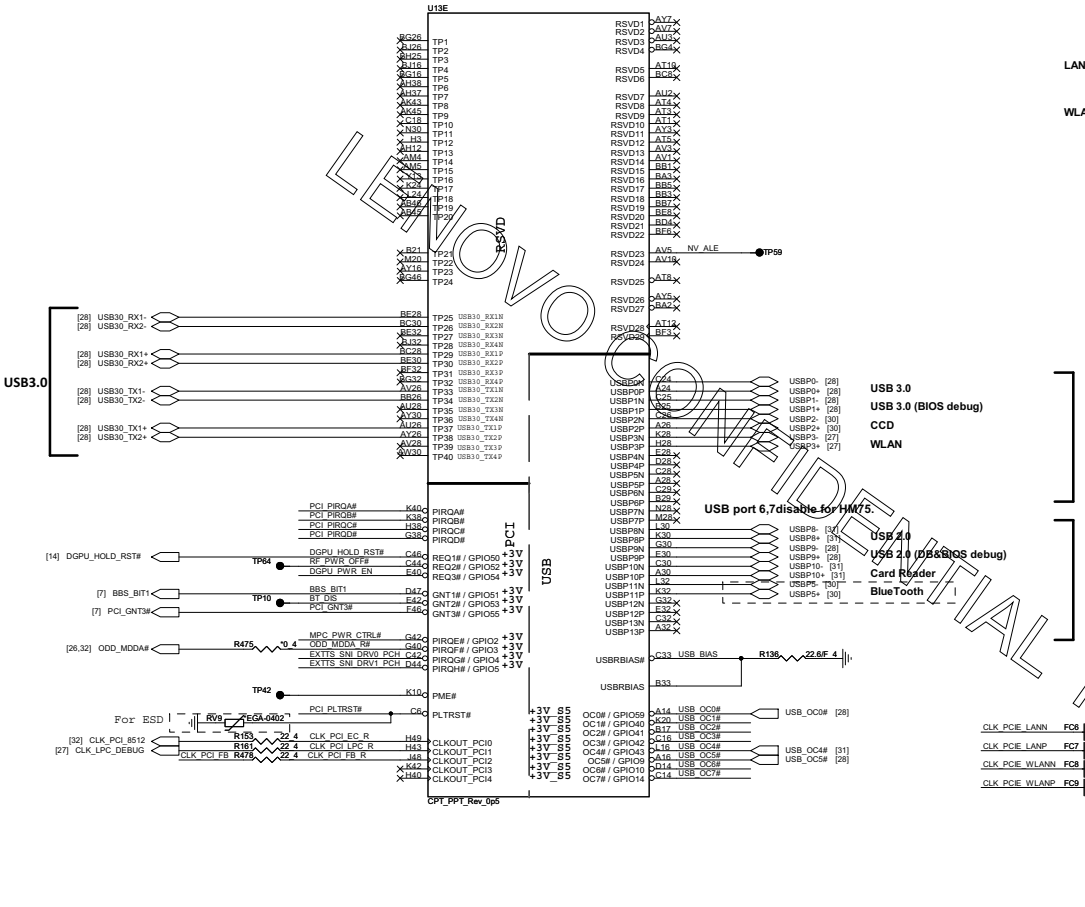
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / **SPI** *; 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
HDA_SDO	Flash Descriptor Security	**RSMRST**	0 = Override 1 = Default (weak pull-up 20K)
DF_TVS	**DMI/FDI Termination voltage**	**PWROK**	**0 = Set to Vss** **1 = Set to Vcc (weak pull-down 20K)**
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)
HDA_SYNC	**On-Die PLL VR Voltage Select**	**RSMRST**	**0 = Support by 1.8V (weak pull-down)** **1 = Support by 1.5V**
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)

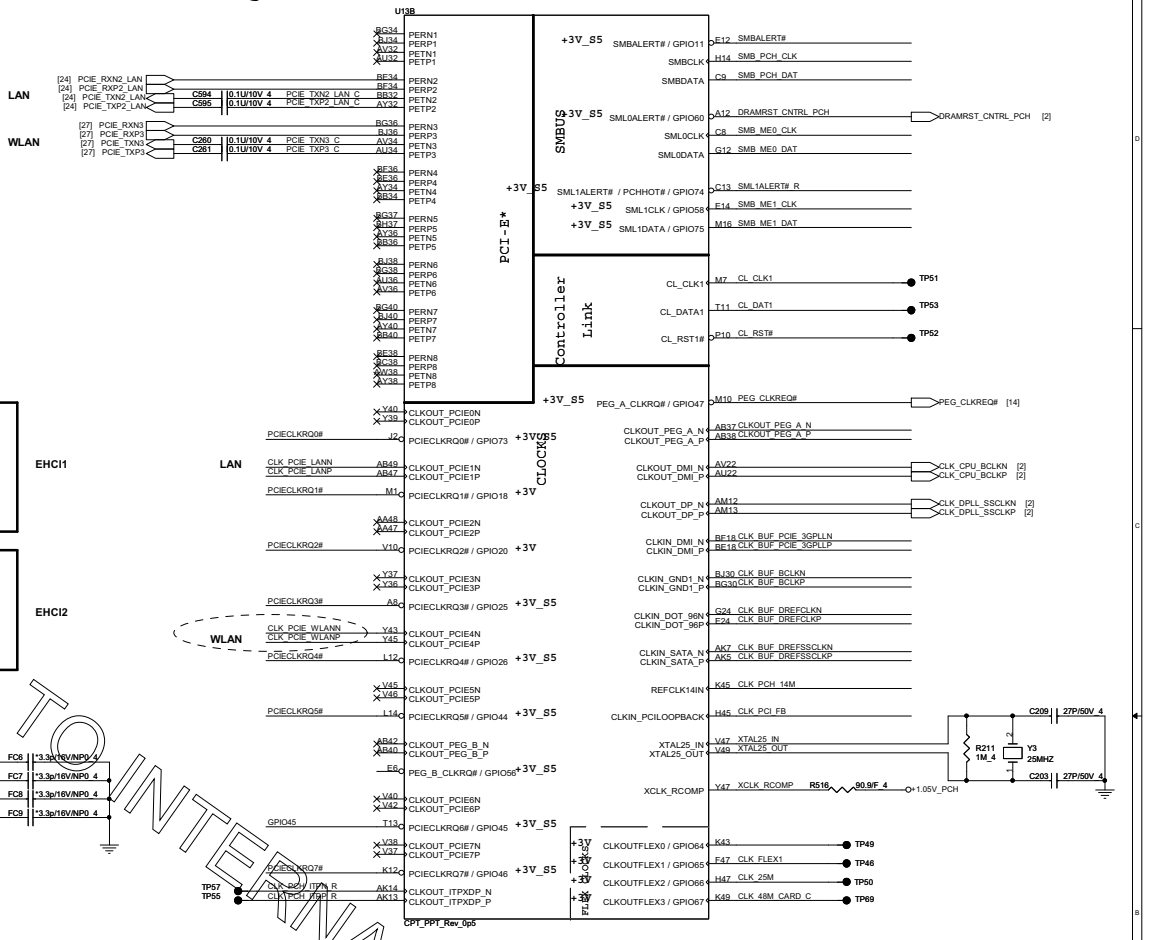


PROJECT : LZ2A
Quanta Computer Inc.
Size | Document Number: Panther Point 2/6 | Rev: 1A
Date: Wednesday, November 30, 2011 | Sheet 7 of 45

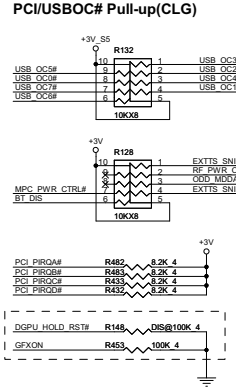
Cougar Point-M/Panther Point (PCI,USB,NVRAM)



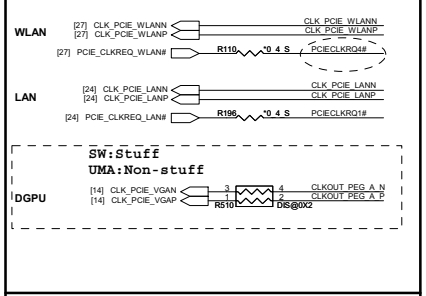
Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)



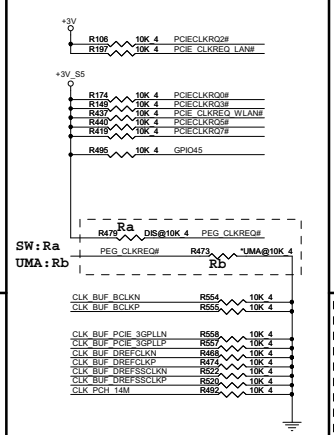
PCI/USBOC# Pull-up(CLG)



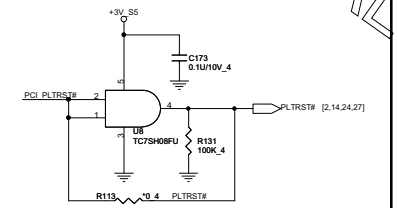
PCIE CLOCK



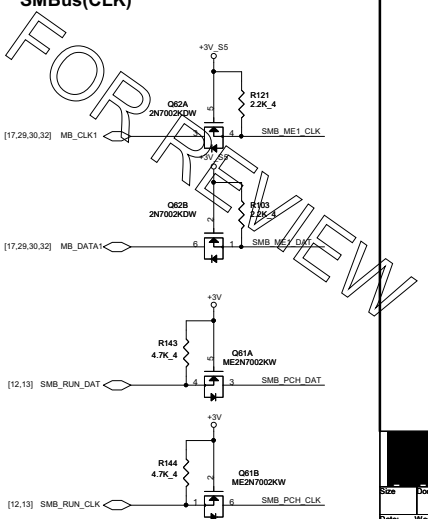
CLK_REQ/Strap Pin(CLG)



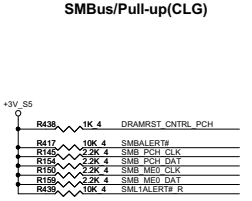
PLTRST#(CLG)



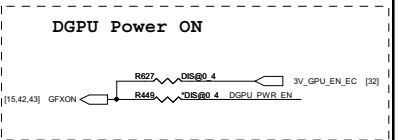
SMBus(CLK)



SMBus/Pull-up(CLG)



DGPU Power ON



MPC Switch Control

MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

MPC_PWR_CTRL# R465 *1K_4

PROJECT : LZ2A
Quanta Computer Inc.
Size: Document Number: Panther Point 3/6 Rev: 1A
Date: Wednesday, November 30, 2011 Sheet 8 of 45

Cougar Point/Panther Point (GPIO,MISC,NCTF)

[2,6,7,8,10,27,31,34] +3V_S5
[6,7,8,10,12,13,14,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43] +3V

U13F

CPU/MISC GPIO

S_GPIO	R507 100_4	T7	BMBUSY# / GPIO0	+3V	+3V	TACH4 / GPIO68	C40
[32] EC_EXT_SMI#		A42	TACH1 / GPIO1	+3V	+3V	TACH5 / GPIO69	B41
BOARD_ID1		H36	TACH2 / GPIO6	+3V	+3V	TACH6 / GPIO70	C41
[32] EC_EXT_SCI#		E38	TACH3 / GPIO7	+3V	+3V	TACH7 / GPIO71	A40
TP8		C10	GPIO8	+3V_S5			
[27] LAN_DISABLE#		C4	LAN_PHY_PWR_CTRL / GPIO12	+3V_S5			
HOST_ALERT#1_R		G2	GPIO15	+3V_S5			
BOARD_ID2		U2	SATA4GP / GPIO16	+3V			
[14,43] GFXPG	R100 *0_4_S GFXPG_R	D40	TACH0 / GPIO17	+3V			
BIOS_REC		T5	SCLOCK / GPIO22	+3V			
SYSTEM_ID1		F8	GPIO24 / MEM_LED	+3V_S5			
GPIO27		E16	GPIO27	DSW			
[7] PLL_ODVR_EN	R494 *0_4_S PLL_ODVR_EN_R	P8	GPIO28	+3V_S5			
SYSTEM_ID0		K1	STP_PCI# / GPIO33	+3V			
[30] BT_ON#		K4	GPIO35	+3V			
[30] CCD_ON#		V8	SATA2GP / GPIO36	+3V			
FDI_OVRVLTG		M5	SATA3GP / GPIO37	+3V			
MFG_MODE		N2	SLOAD / GPIO38	+3V			
DGPU_PRSNT#		M3	SDATAOUT0 / GPIO39	+3V			
TEST_SET_UP		V13	SDATAOUT1 / GPIO48	+3V			
[29,32] TEMP_ALERT#		V3	SATA5GP / GPIO49	+3V			
SV_DET		D6	GPIO57	+3V_S5			

			A20GATE			P4	EC_A20GATE [32]
			PECI			AU16	TP58
			RCIN#		EC_RCIN#	P5	EC_RCIN# [32]
			PROCPWRGD			AY11	H_PWRGOOD [2]
			THRMTRIP#		PCH_THRMTRIP# R539 390_4	AY10	PM_THRMTRIP# [2]
			INIT3_3V#			T14	
			DF_TVS			AY1	DF_TVS [7]
			TS_VSS1			AH8	
			TS_VSS2			AK11	
			TS_VSS3			AH10	
			TS_VSS4			AK10	
			NC_1			P37	

NCTF

		A4	VSS_NCTF_1			BG2	
		A44	VSS_NCTF_2			BG48	
		A45	VSS_NCTF_3			BH3	
		A46	VSS_NCTF_4			BH47	
		A5	VSS_NCTF_5			BJ4	
		A6	VSS_NCTF_6			BJ44	
		B3	VSS_NCTF_7			BJ45	
		B47	VSS_NCTF_8			BJ46	
		BD1	VSS_NCTF_9			BJ5	
		BD49	VSS_NCTF_10			BJ6	
		BE1	VSS_NCTF_11			C2	
		BE49	VSS_NCTF_12			C48	
		BF1	VSS_NCTF_13			D1	
		BF49	VSS_NCTF_14			D49	
			VSS_NCTF_15			E1	
			VSS_NCTF_16			F49	
			VSS_NCTF_17			F1	
			VSS_NCTF_18			F49	
			VSS_NCTF_19				
			VSS_NCTF_20				
			VSS_NCTF_21				
			VSS_NCTF_22				
			VSS_NCTF_23				
			VSS_NCTF_24				
			VSS_NCTF_25				
			VSS_NCTF_26				
			VSS_NCTF_27				
			VSS_NCTF_28				
			VSS_NCTF_29				
			VSS_NCTF_30				
			VSS_NCTF_31				
			VSS_NCTF_32				

CPT_PPT_Rev_0p5

R25 10K/F_4 — R118 *GS@0_4 — FB_CLAMP [15]
R122 1.5K/F_4
R462 *GS@0_4 — GPU_EVENT# [17]
R634 10K/F_4@GS@NC — +3V

NVidia N13P-GS

NVidia N13P-GS

Board ID For Function	ID1 GPIO6	ID2 GPIO16	ID3 GPIO13
SDV	0	0	0
SIV	0	0	1
SIT	0	1	0
SVT			
SOVP			

Board ID use below GPIO:
BOARD_ID1
BOARD_ID2
BOARD_ID3

PCB_LAYER_ID:
0-->6 layer
1-->8 layer

System ID[0],ID[1]:
-->LZ1 [0,0]
-->LZ2 [0,1]
-->LZ3 [1,0]

+3V
R209 *10K_4 BOARD_ID2 R213 10K_4
R429 10K_4 BOARD_ID1 R430 *10K_4
R129 *10K_4 PCB_LAYER_ID R138 10K_4
R187 10K_4 SYSTEM_ID0 R179 10K_4
+3V_S5
R476 *10K_4 SYSTEM_ID1 R467 10K_4
R503 10K_4 BOARD_ID3 R443 *10K_4
BOARD_ID3 [7]

GPIO Pull-up/Pull-down(CLG)

LAN_DISABLE# R162 10K_4 +3V_S5
+3V
EC_EXT_SMI# R130 10K_4
EC_EXT_SC# R431 10K_4
EC_A20GATE R498 10K_4
EC_RCIN# R500 10K_4
TEMP_ALERT# R223 10K_4
BT_ON# R481 10K_4
GPIO27 R441 10K_4

SATA2GP/GPIO36	Reserved	Rising edge of PWROK	This signal has a weak internal pull-down. NOTES: 1. The internal pull-down is disabled after PLTRST# deasserts. 2. [redacted]

CCD_ON# R515 *200K/F_4 +3V

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

R491 100K_4 FDI_OVRVLTG R486 *1K/F_4 +3V

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

SGPIO

S_GPIO R508 10K_4 R505 *0_4 +3V

BIOS_REC R499 10K_4 R501 *0_4 +3V

BIOS RECOVERY	High = Disable (Default) Low = Enable

SV_SET_UP
High = Strong (Default)

TEST_SET_UP R194 10K_4 R185 *0_4 +3V

HOST_ALERT#1_R R466 1K_4 +3V_S5

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

MFG-TEST

MFG_MODE R199 10K_4 R202 *0_4 +3V

+3V_S5
R456 *10K_4 SV_DET R458 100K_4

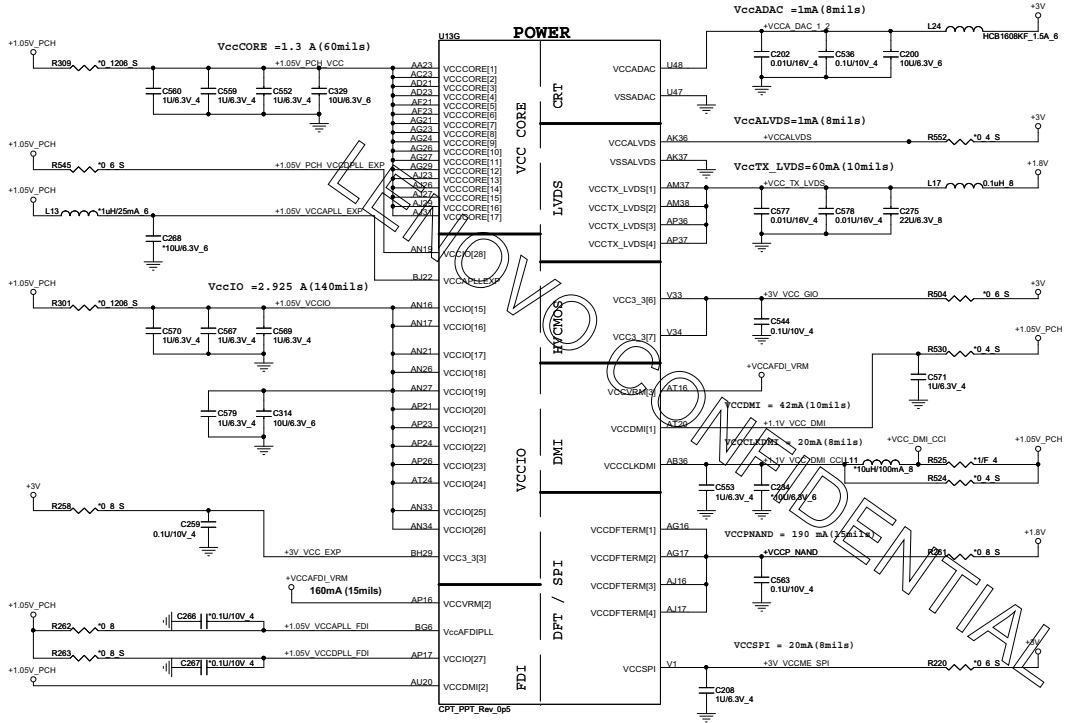
	SWITCHABLE	UMA
Stuff	R186	R195
No Stuff	R195	R186

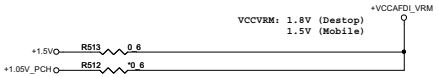
+3V
R195 *UMA@10K_4 DGPU_PRSNT# R186 DIS@100K_4

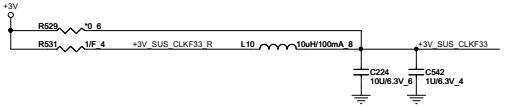
PROJECT : LZ2A
Quanta Computer Inc.

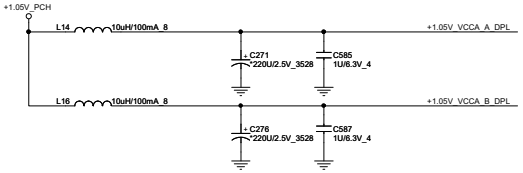
Size	Document Number	Rev
	Panther Point 4/6	1A
Date: Wednesday, November 30, 2011	Sheet 9 of 45	

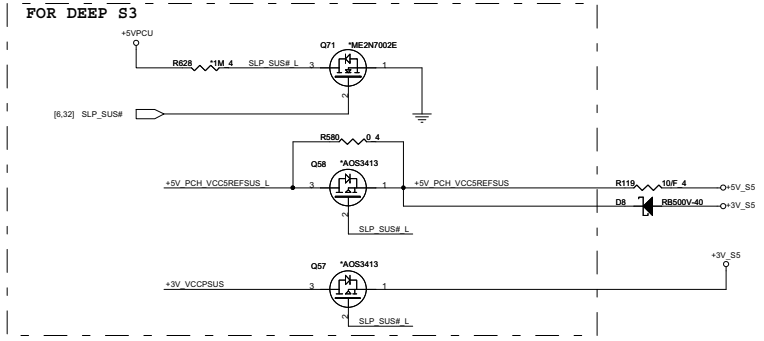
Cougar Point/Panther Point (POWER)



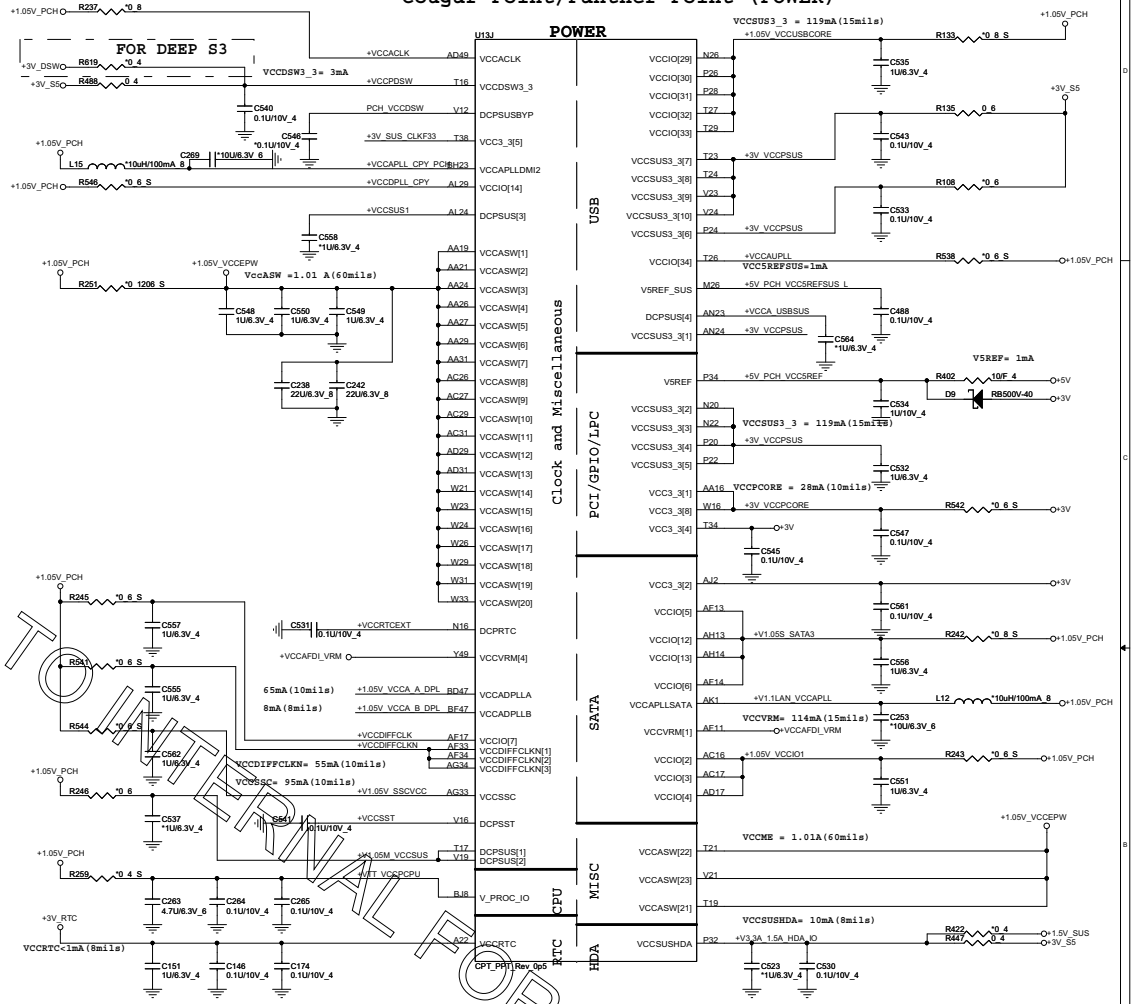








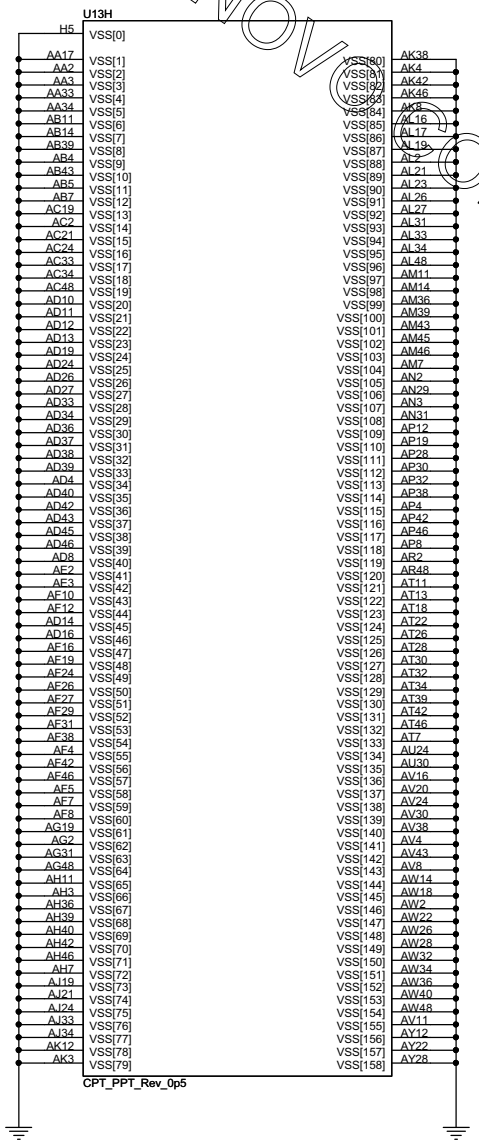
Cougar Point/Panther Point (POWER)

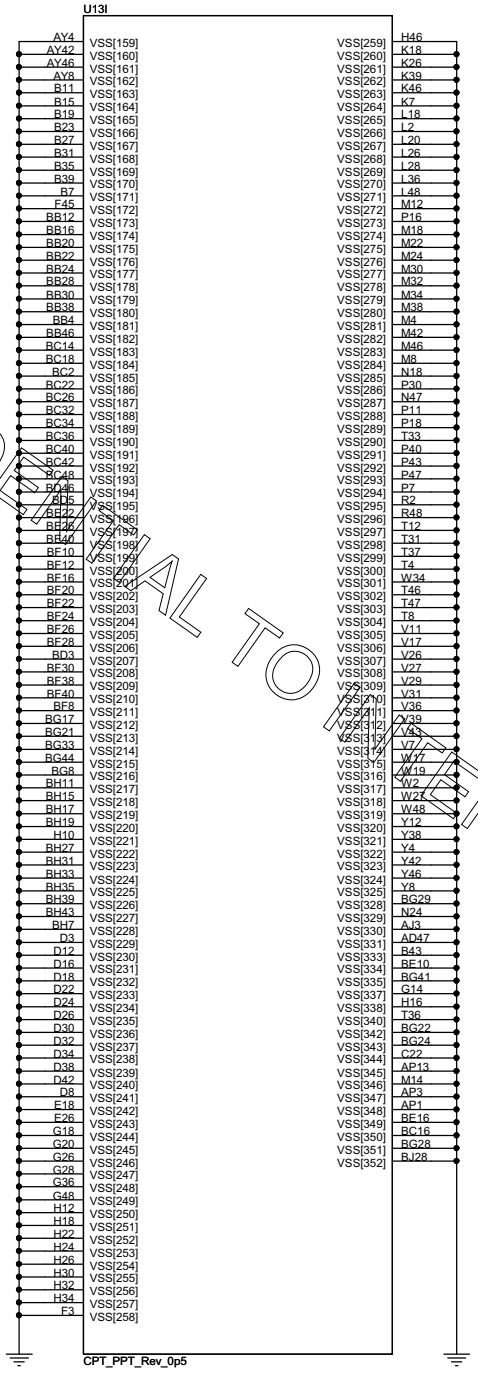


PROJECT : LZ2A	
Quanta Computer Inc.	
Size	Document Number: Panther Point 5/6 — Rev: 1A
Date: Wednesday, November 30, 2011	Sheet 10 of 45

http://adf.ly/3o8pJ

Cougar Point/Panther Point (GND)

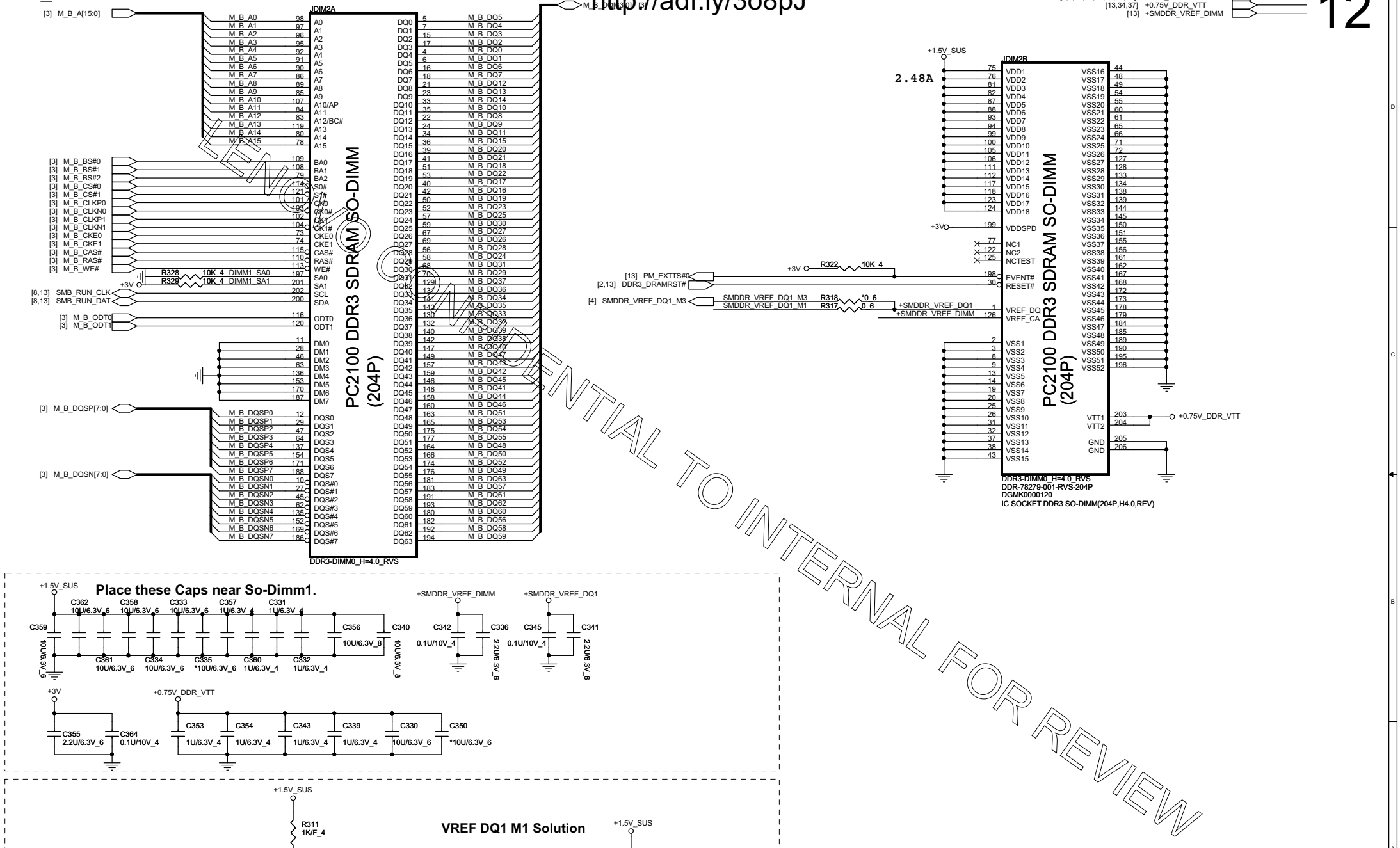


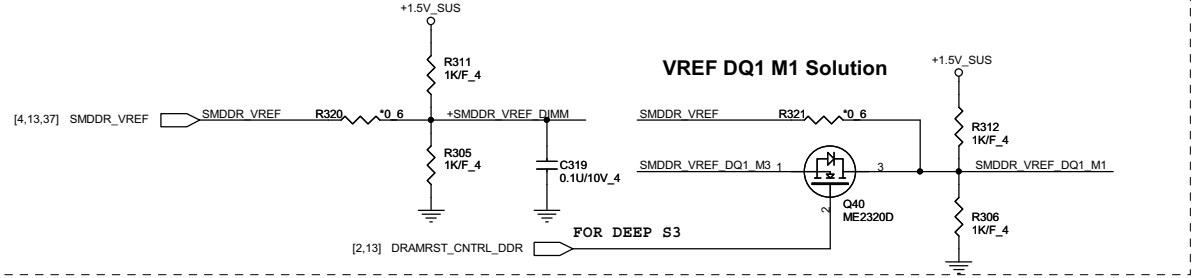


PROJECT : LZ2A

Quanta Computer Inc.

Size	Document Number	Rev
	Panther Point 6/6	1A
Date: Wednesday, November 30, 2011	Sheet 11 of 45	





PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	DDRIII SO-DIMM-0	1A
Date: Wednesday, November 30, 2011	Sheet 12 of 45	

http://adf.ly/3o8pJ

[6,7,8,9,10,12,14,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43] +3V
[2,4,10,12,33,34,37,43] +1.5V_SUS
[12,34,37] +0.75V_DDR_VTT
[12] +SMDDR_VREF_DIMM

[3] M_A_A[15:0]

JDIM1A

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM1_H=8.0_RVS

[3] M_A_BS#0
[3] M_A_BS#1
[3] M_A_BS#2
[3] M_A_CS#0
[3] M_A_CS#1
[3] M_A_CLKP0
[3] M_A_CLKN0
[3] M_A_CLKP1
[3] M_A_CLKN1
[3] M_A_CKE0
[3] M_A_CKE1
[3] M_A_CAS#
[3] M_A_RAS#
[3] M_A_WE#

R308 10K_4 DIMM0_SA0
R307 10K_4 DIMM0_SA1

[8,12] SMB_RUN_CLK
[8,12] SMB_RUN_DAT

[3] M_A_ODT0
[3] M_A_ODT1

[3] M_A_DQSP[7:0]
[3] M_A_DQSN[7:0]

M_A_DQ[63:0] [3]

2.48A

JDIM1B

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM1_H=8.0_RVS

+1.5V_SUS
+3V

R286 10K_4

[12] PM_EXTTS#0
[2,12] DDR3_DRAMRST#

SMDDR_VREF_DQ0_M1 R303 0_6
SMDDR_VREF_DQ0_M3 R314 *0_6
[4] SMDDR_VREF_DQ0_M3

+SMDDR_VREF_DQ0
+SMDDR_VREF_DIMM

VTT1 VTT2 → +0.75V_DDR_VTT

GND GND

Place these Caps near So-Dimm0.

+1.5V_SUS

C300 10U/6.3V_6
C303 10U/6.3V_6
C324 10U/6.3V_6
C306 10U/6.3V_6
C301 1U/6.3V_4
C326 1U/6.3V_4
C307 10U/6.3V_6
C325 10U/6.3V_6
C322 *10U/6.3V_6
C305 1U/6.3V_4
C327 1U/6.3V_4
C296 *330U/2V/ESR9_7343
C297 10U/6.3V_8
C323 10U/6.3V_8

+SMDDR_VREF_DIMM
+SMDDR_VREF_DQ0

C299 0.1U/10V_4
C304 2.2U/6.3V_6
C317 0.1U/10V_4
C318 2.2U/6.3V_6

+3V
C316 2.2U/6.3V_6
C321 0.1U/10V_4

+0.75V_DDR_VTT
C298 1U/6.3V_4
C302 1U/6.3V_4
C328 1u/6.3V_4
C320 1U/6.3V_4
C308 10U/6.3V_6
C311 *10U/6.3V_6

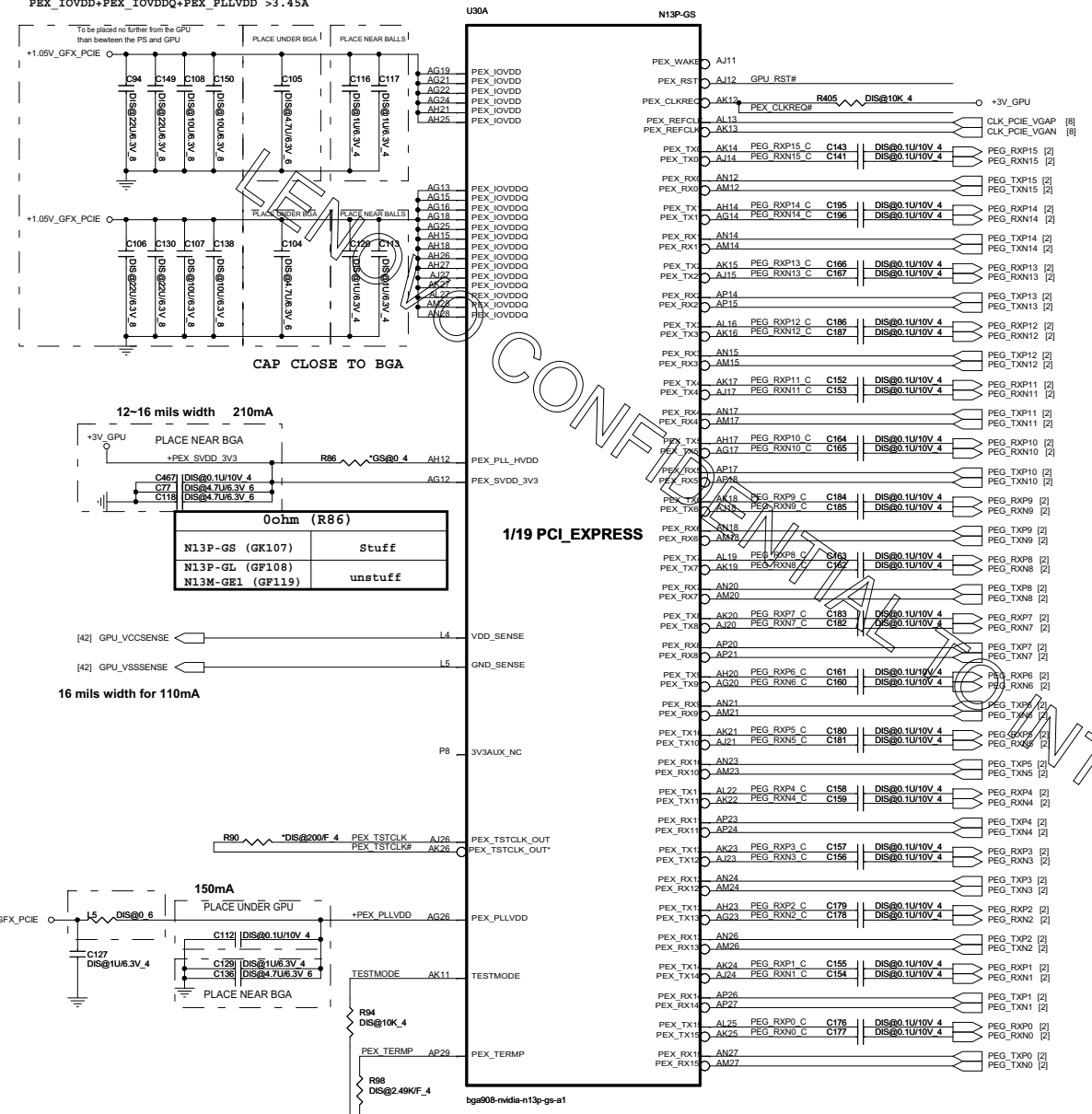
VREF DQ0 M3 Solution

+1.5V_SUS
R325 1K/F_4
R324 1K/F_4
[4,12,37] SMDDR_VREF
R323 *0_6
SMDDR_VREF_DQ0_M1
SMDDR_VREF_DQ0_M3
Q41 ME2320D
FOR DEEP S3
[2,12] DRAMRST_CNTRL_DDR

PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	DDRIII SO-DIMM-1	1A
Date: Wednesday, November 30, 2011	Sheet 13 of 45	

PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >3.45A



12~16 mils width 210mA

0ohm (R86)	
N13P-GS (GK107)	Stuff
N13P-GL (GF108) N13M-GE1 (GF119)	unstuff

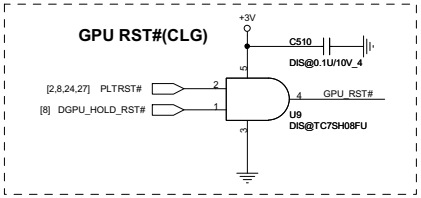
16 mils width for 110mA

P8 3V3AUX_NC

150mA

PEG Capacitance	
N13P-GS (GK107)	CH4222K9B04: CAP CHIP 0.22U 10V(+-10%,X5R,0402)
N13P-GL (GF108) N13M-GE1 (GF119)	CH41002KB93: CAP CHIP 0.1U 10V(+-10%,X5R,0402)

GPU RST#(CLG)



All GPU power rails must ramp up after VDD33. The following conditions must be met:

- tNVVDD ≥ 0
- tFBVDD ≥ 0
- tPEX_VDD > 0
- tIFPx_IOVDD ≥ 0
- tIFPy_IOVDD ≥ 0
- The ramp time for any rail must be more than 40 us.

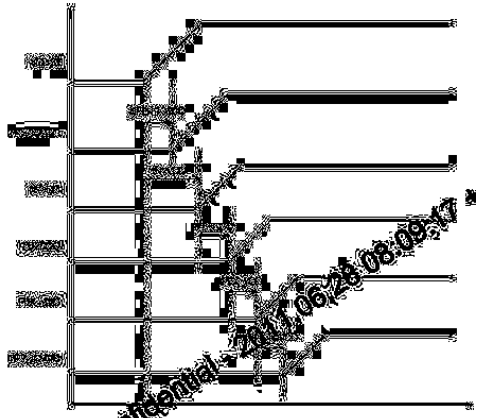


Figure 17. Recommended Power On Sequencing Order

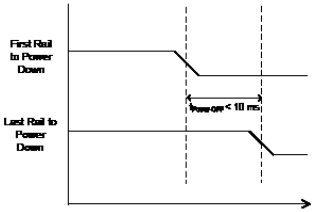
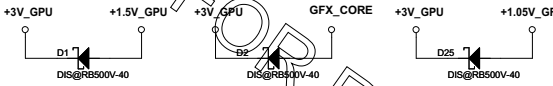
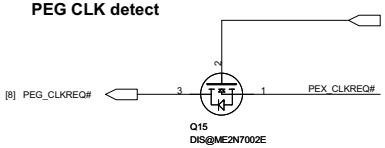


Figure 18. Recommended Power Off Sequencing Order

For power-down sequency



PEG CLK detect

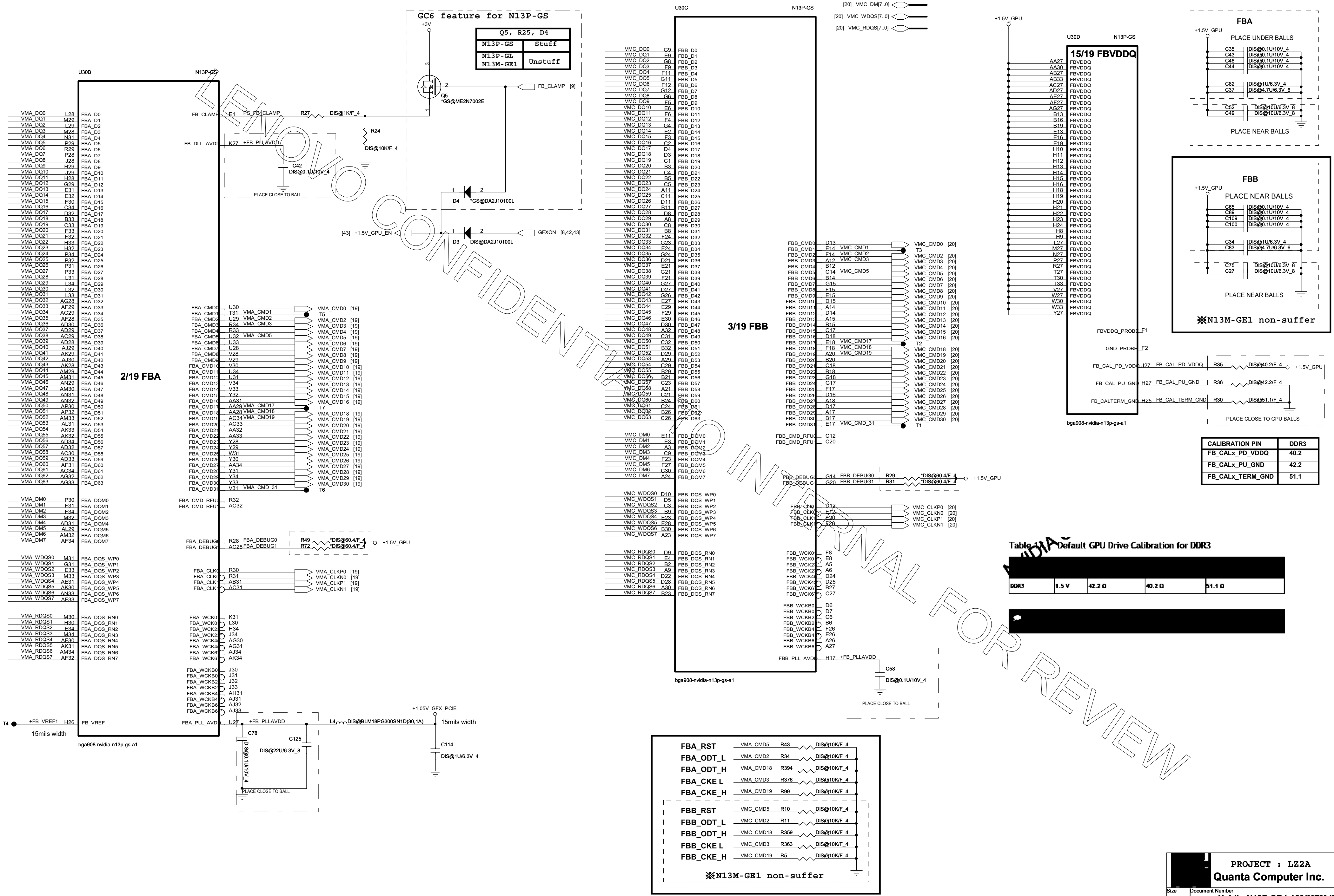


PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	Nvidia-N13P GB4-128(PCIe)	1A

Date: Wednesday, November 30, 2011 Sheet 14 of 45

http://adf.ly/3o8pJ


[19] VMA_DQ[63..0]
[19] VMA_DM[7..0]
[19] VMA_WDQS[7..0]
[19] VMA_RDQS[7..0]
[20] VMC_DQ[63..0]
[20] VMC_DM[7..0]
[20] VMC_WDQS[7..0]
[20] VMC_RDQS[7..0]
[14,16,33,43] +1.05V_GFX_PCIE
[14,19,20,33,43] +1.5V_GPU
[6,7,8,9,10,12,13,14,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43] +3V
GC6 feature for N13P-GS
Q5, R25, D4
N13P-GS Stuff
N13P-GL N13M-GE1 Unstuff
+3V
Q5 *GS@ME2N7002E
FB_CLAMP [9]
R27 DIS@1K/F_4
R24 DIS@10K/F_4
D4 *GS@DA2J10100L
D3 DIS@DA2J10100L
[43] +1.5V_GPU_EN
GFXON [8,42,43]
U30B N13P-GS
2/19 FBA
VMA_DQ0–VMA_DQ63 → FBA_D0–FBA_D63 (L28, M29, L29, M28, N31, P29, R29, P28, J28, H29, J29, H28, G29, E31, E32, F30, C34, D32, B33, C33, F33, F32, H33, H32, P34, P32, P31, P33, L31, L34, L32, L33, AG28, AF29, AG29, AF28, AD30, AD29, AC29, AD28, AJ29, AK29, AJ30, AK28, AM29, AM31, AN29, AM30, AN31, AN32, AP30, AP32, AM33, AL31, AK33, AK32, AD34, AD32, AC30, AD33, AF31, AG34, AG32, AG33)
VMA_DM0–VMA_DM7 → FBA_DQM0–FBA_DQM7 (P30, F31, F34, M32, AD31, AL29, AM32, AF34)
VMA_WDQS0–VMA_WDQS7 → FBA_DQS_WP0–FBA_DQS_WP7 (M31, G31, E33, M33, AE31, AK30, AN33, AF33)
VMA_RDQS0–VMA_RDQS7 → FBA_DQS_RN0–FBA_DQS_RN7 (M30, H30, E34, M34, AF30, AK31, AM34, AF32)
FB_CLAMP E1 PS_FB_CLAMP
FB_DLL_AVDD K27 +FB_PLLAVDD
C42 DIS@0.1U/10V_4
PLACE CLOSE TO BALL
FBA_CMD0–FBA_CMD31 (U30, T31, U29, R34, R33, U32, U33, U28, V28, V29, V30, U34, U31, V34, V33, Y32, AA31, AA29, AA28, AC34, AC33, AA32, AA33, Y28, Y29, W31, Y30, AA34, Y31, Y34, Y33, V31) → VMA_CMD0–VMA_CMD30 [19], VMA_CMD_31
T5 T6 T7
FBA_CMD_RFU0 R32
FBA_CMD_RFU1 AC32
FBA_DEBUG0 R28 FBA_DEBUG0
FBA_DEBUG1 AC28 FBA_DEBUG1
R49 *DIS@60.4/F_4
R72 *DIS@60.4/F_4
+1.5V_GPU
FBA_CLK0 R30 VMA_CLKP0 [19]
FBA_CLK0 R31 VMA_CLKN0 [19]
FBA_CLK1 AB31 VMA_CLKP1 [19]
FBA_CLK1 AC31 VMA_CLKN1 [19]
FBA_WCK01 K31, L30; FBA_WCK23 H34, J34; FBA_WCK45 AG30, AG31; FBA_WCK67 AJ34, AK34
FBA_WCKB01 J30, J31; FBA_WCKB23 J32, J33; FBA_WCKB45 AH31, AJ31; FBA_WCKB67 AJ32, AJ33
T4 +FB_VREF1 H26 FB_VREF
15mils width
FBA_PLL_AVDD U27 +FB_PLLAVDD
C78 DIS@0.1U/10V_4
C125 DIS@22U/6.3V_8
PLACE CLOSE TO BALL
L4 DIS@BLM18PG300SN1D(30,1A)
+1.05V_GFX_PCIE
15mils width
C114 DIS@1U/6.3V_4
bga908-nvidia-n13p-gs-a1
U30C N13P-GS
3/19 FBB
VMC_DQ0–VMC_DQ63 → FBB_D0–FBB_D63 (G9, E9, G8, F9, F11, G11, F12, G12, G6, F5, E6, F6, F4, G4, E2, F3, C2, D4, D3, C1, B3, C4, B5, C5, A11, C11, D11, B11, D8, A8, C8, B8, F24, G23, E24, G24, D21, E21, G21, F21, G27, D27, G26, E27, E29, F29, E30, D30, A32, C31, C32, B32, D29, A29, C29, B29, B21, C23, A21, C21, B24, C24, B26, C26)
VMC_DM0–VMC_DM7 → FBB_DQM0–FBB_DQM7 (E11, E3, A3, C9, F23, F27, C30, A24)
VMC_WDQS0–VMC_WDQS7 → FBB_DQS_WP0–FBB_DQS_WP7 (D10, D5, C3, B9, E23, E28, B30, A23)
VMC_RDQS0–VMC_RDQS7 → FBB_DQS_RN0–FBB_DQS_RN7 (D9, E4, B2, A9, D22, D28, A30, B23)
FBB_CMD0–FBB_CMD31 (D13, E14, F14, A12, B12, C14, B14, G15, F15, E15, D15, A14, D14, A15, B15, C17, D18, E18, F18, A20, B20, C18, B18, G18, G17, F17, D16, A18, D17, A17, B17, E17) → VMC_CMD0–VMC_CMD30 [20], VMC_CMD_31
T1 T2 T3
FBB_CMD_RFU0 C12
FBB_CMD_RFU1 C20
FBB_DEBUG0 G14 FBB_DEBUG0 R29 *DIS@60.4/F_4
FBB_DEBUG1 G20 FBB_DEBUG1 R31 *DIS@60.4/F_4
+1.5V_GPU
FBB_CLK0 D12 VMC_CLKP0 [20]
FBB_CLK0 E12 VMC_CLKN0 [20]
FBB_CLK1 E20 VMC_CLKP1 [20]
FBB_CLK1 F20 VMC_CLKN1 [20]
FBB_WCK01 F8, E8; FBB_WCK23 A5, A6; FBB_WCK45 D24, D25; FBB_WCK67 B27, C27
FBB_WCKB01 D6, D7; FBB_WCKB23 C6, B6; FBB_WCKB45 F26, E26; FBB_WCKB67 A26, A27
FBB_PLL_AVDD H17 +FB_PLLAVDD
C58 DIS@0.1U/10V_4
PLACE CLOSE TO BALL
bga908-nvidia-n13p-gs-a1
+1.5V_GPU
U30D N13P-GS
15/19 FBVDDQ
FBVDDQ: AA27, AA30, AB27, AB33, AC27, AD27, AE27, AF27, AG27, B13, B16, B19, E13, E16, E19, H10, H11, H12, H13, H14, H15, H16, H18, H19, H20, H21, H22, H23, H24, H8, H9, L27, M27, N27, P27, R27, T27, T30, T33, V27, W27, W30, W33, Y27
FBVDDQ_PROBE F1
GND_PROBE F2
FB_CAL_PD_VDDQ J27 FB_CAL_PD_VDDQ R35 DIS@40.2/F_4 +1.5V_GPU
FB_CAL_PU_GND H27 FB_CAL_PU_GND R36 DIS@42.2/F_4
FB_CALTERM_GND H25 FB_CAL_TERM_GND R30 DIS@51.1/F_4
PLACE CLOSE TO GPU BALLS
bga908-nvidia-n13p-gs-a1
FBA
+1.5V_GPU
PLACE UNDER BALLS
C35 DIS@0.1U/10V_4
C43 DIS@0.1U/10V_4
C48 DIS@0.1U/10V_4
C44 DIS@0.1U/10V_4
C82 DIS@1U/6.3V_4
C37 DIS@4.7U/6.3V_6
C52 DIS@10U/6.3V_8
C49 DIS@10U/6.3V_8
PLACE NEAR BALLS
FBB
+1.5V_GPU
PLACE NEAR BALLS
C65 DIS@0.1U/10V_4
C89 DIS@0.1U/10V_4
C109 DIS@0.1U/10V_4
C100 DIS@0.1U/10V_4
C34 DIS@1U/6.3V_4
C83 DIS@4.7U/6.3V_6
C75 DIS@10U/6.3V_8
C27 DIS@10U/6.3V_8
PLACE NEAR BALLS
※N13M-GE1 non-suffer
FBA_RST VMA_CMD5 R43 DIS@10K/F_4
FBA_ODT_L VMA_CMD2 R34 DIS@10K/F_4
FBA_ODT_H VMA_CMD18 R394 DIS@10K/F_4
FBA_CKE L VMA_CMD3 R376 DIS@10K/F_4
FBA_CKE_H VMA_CMD19 R99 DIS@10K/F_4
FBB_RST VMC_CMD5 R10 DIS@10K/F_4
FBB_ODT_L VMC_CMD2 R11 DIS@10K/F_4
FBB_ODT_H VMC_CMD18 R359 DIS@10K/F_4
FBB_CKE L VMC_CMD3 R363 DIS@10K/F_4
FBB_CKE_H VMC_CMD19 R5 DIS@10K/F_4
※N13M-GE1 non-suffer

CALIBRATION PIN	DDR3
FB_CALx_PD_VDDQ	40.2
FB_CALx_PU_GND	42.2
FB_CALx_TERM_GND	51.1

Table 1 Default GPU Drive Calibration for DDR3

[redacted]				
DDR3	1.5 V	42.2 Ω	40.2 Ω	51.1 Ω

[redacted]

PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	Nvidia-N13P GB4-128(MEM IF)	1A

Date: Wednesday, November 30, 2011 Sheet 15 of 45

http://adf.ly/3o8pJ

[14,15,33,43] +1.05V_GFX_PCIE

50 mA

160 mA+160 mA

200 mA

U30J N13P-GS

6/19 IFPAB

ALL PINS NC FOR GF117

IFPAB

+IFPAB_PLLVDD AH8 IFPAB_PLLVDD

R91 DIS@10K/F_4

+IFPAB_IOVDD AG8 IFPA_IOVDD AG9 IFPB_IOVDD

R83 DIS@10K/F_4

AJ8 IFPAB_RSET

IFPA_TXC AN6 IFPA_TXC AM6

IFPA_TXD AN3 IFPA_TXD AP3

IFPA_TXD AM5 IFPA_TXD AN5

IFPA_TXD AK6 IFPA_TXD AL6

IFPA_TXD AH6 IFPA_TXD AJ6

IFPB_TXC AH9 IFPB_TXC AJ9

IFPB_TXD AP5 IFPB_TXD AP6

IFPB_TXD AL7 IFPB_TXD AM7

IFPB_TXD AM8 IFPB_TXD AN8

IFPB_TXD AL8 IFPB_TXD AK8

GPIO14 N4

bga908-nvidia-n13p-gs-a1

U30K N13P-GS

7/19 IFPC

ALL PINS NC FOR GF117

IFPC

AF8 IFPC_RSET

+IFPCD_PLLVDD AF7 IFPC_PLLVDD

R79 DIS@10K/F_4

+IFPCD_IOVDD AF6 IFPC_IOVDD

R84 DIS@10K/F_4

DVI/HDMI DP

I2CW_SDA I2CW_SCL

TXC TXC

TXD0 TXD0

TXD1 TXD1

TXD2 TXD2

IFPC_AUX AG2 IFPC_AUX AG3

IFPC_L3 AG4 IFPC_L3 AG5

IFPC_L2 AH4 IFPC_L2 AH3

IFPC_L1 AJ2 IFPC_L1 AJ3

IFPC_L0 AJ1 IFPC_L0 AK1

GPIO15 P2

bga908-nvidia-n13p-gs-a1

U30L N13P-GS

8/19 IFPD

ALL PINS NC FOR GF117

IFPD

AN3 IFPD_RSET

+IFPCD_PLLVDD AG7 IFPD_PLLVDD

+IFPCD_IOVDD AG6 IFPD_IOVDD

DVI/HDMI DP

I2CX_SDA I2CX_SCL

TXC TXC

TXD0 TXD0

TXD1 TXD1

TXD2 TXD2

IFPD_AUX AK2 IFPD_AUX AK3

IFPD_L3 AK5 IFPD_L3 AK4

IFPD_L2 AL4 IFPD_L2 AL3

IFPD_L1 AM4 IFPD_L1 AM3

IFPD_L0 AM2 IFPD_L0 AM1

GPIO17 M6

bga908-nvidia-n13p-gs-a1

U30M N13P-GS

9/19 IFPEF

ALL PINS NC FOR GF117

IFPE

IFPF

R60 DIS@10K_4 +IFPEF_PLLVDD AB8 IFPEF_PLLVDD

AD8 IFPEF_RSET

R61 DIS@10K_4 +IFPEF_IOVDD AC7 IFPE_IOVDD AC8 IFPF_IOVDD

DVI-DL DVI-SL/HDMI DP

I2CY_SDA I2CY_SCL

TXC TXC

TXD0 TXD0

TXD1 TXD1

TXD2 TXD2

HPD_E

IFPE_AUX AB4 IFPE_AUX AB3

IFPE_L3 AC5 IFPE_L3 AC4

IFPE_L2 AC3 IFPE_L2 AC2

IFPE_L1 AC1 IFPE_L1 AD1

IFPE_L0 AD3 IFPE_L0 AD2

GPIO18 R1

I2CZ_SDA I2CZ_SCL

IFPF_AUX AF2 IFPF_AUX AF3

IFPF_L3 AF1 IFPF_L3 AG1

IFPF_L2 AD5 IFPF_L2 AD4

IFPF_L1 AF5 IFPF_L1 AF4

IFPF_L0 AE4 IFPF_L0 AE3

HPD_F

GPIO19 P3

bga908-nvidia-n13p-gs-a1

U30N N13P-GS

4/19 DACA

GF108/GKx GF117

DACA_VDD NC

DACA_VREF TSEN_VREF

DACA_RSET NC

R78 DIS@10K_4 AG10 AP9 AP8

TP29 TP31

GF117 GF108/GKx

I2CA_SCL R4 I2CA_SDA R5

EV_CRTDCLK R630 DIS@2.2K_4

EV_CRTDDAT R631 DIS@2.2K_4

+3V_GPU

DACA_HSYNC AM9 DACA_VSYNC AN9

DACA_RED AK9 DACA_GREEN AL10 DACA_BLUE AL9

TP6 TP30 TP4 TP3 TP5

bga908-nvidia-n13p-gs-a1

60mA 12~16 mil

90mA 12~16 mil

+1.05V_GFX_PCIE

L2 DIS@BLM18PG300SN1D(30,1A)

C122 DIS@22U/6.3V_8

C96 DIS@0.1U/10V_4

PLACE CLOSE TO BGA

PLACE UNDER BGA

+PLLVDD

+NV_PLLVDD

L3 DIS@HCB1608KF(180,1.5A)_6

C126 DIS@1U/6.3V_4

C111 DIS@22U/6.3V_8

C101 DIS@4.7U/6.3V_6

C98 DIS@1U/10V_4

C97 DIS@1U/10V_4

C99 DIS@1U/10V_4

U30O N13P-GS

12/19 XTAL_PLL

PLLVDD SP_PLLVDD VID_PLLVDD

GF108/GKx GF117 NC

XTALSSIN XTALIN XTALOUTBUF BXTALOUT XTALOUT

XTAL_SSIN H1 H3 J4 L2

R33 DIS@10K_4

R38 DIS@10K_4

XTALI_27M XTALO_27M

Y1 DIS@27MHZ

C39 DIS@27P/50V_4

C41 DIS@33P/50V/NPO_4

bga908-nvidia-n13p-gs-a1

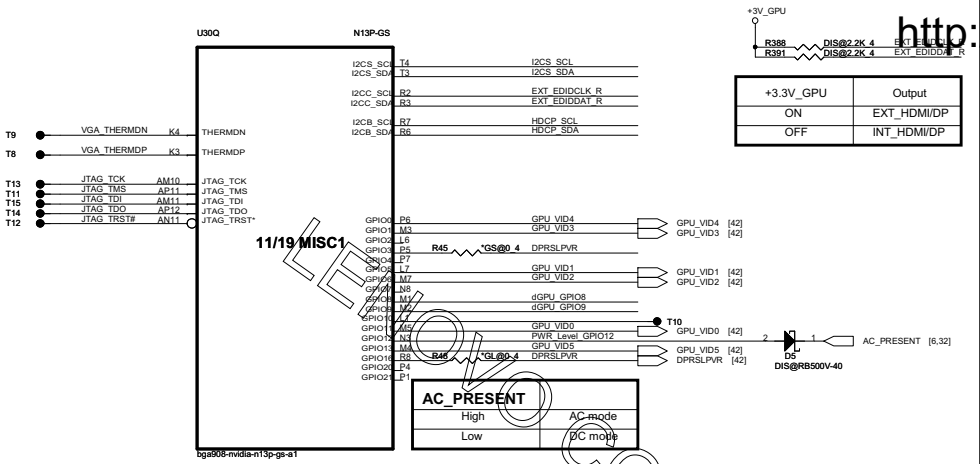
PROJECT : LZ2A

Quanta Computer Inc.

Size Document Number Rev

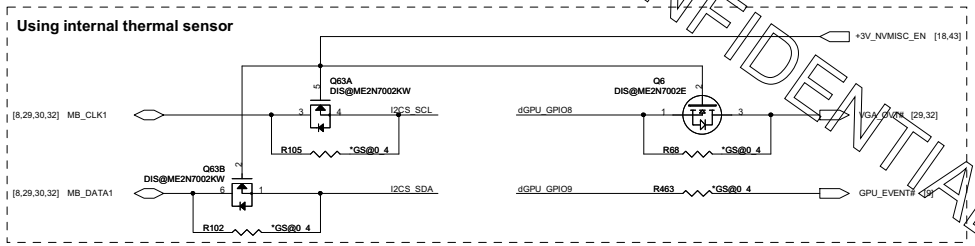
Nvidia-N13P GB4-128(Display) 1A

Date: Wednesday, November 30, 2011 Sheet 16 of 45



AC_PRESENT	
High	AC mode
Low	DC mode

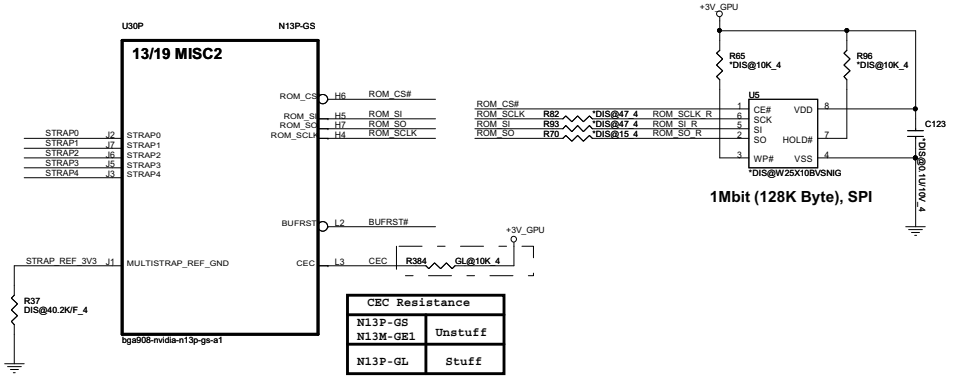
+3.3V_GPU	Output
ON	EXT_HDMI/DP
OFF	INT_HDMI/DP



	Q6,Q63, R81,R104	R68,R102, R105,R463
N13P-GS	Unstuff	Stuff
N13P-GL N13M-GE1	Stuff	Unstuff

Table 5. Stuffing Options

N13P-GT/-GS/-LP, N14P-Q1/-Q3	I2C and GPIO	No stuff FET Stuff 0Ω bypass resistor
	3V3M5C	Stuff FET No stuff 0Ω bypass resistor
Other N13P and N13M	I2C and GPIO	Stuff FET No stuff 0Ω bypass resistor
	3V3M5C	No stuff FET Stuff 0Ω bypass resistor



CEC Resistance	
N13P-GS N13M-GE1	Unstuff
N13P-GL	Stuff

Table 2. GB4-128 Ballout Compatibility

L3	CEC	NC	NC	NC	Place a 10k pull-up to 3V3 on N13P-PES/-GL/-NS1.

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	XXXX
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	XXXX
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V	XXXX

Resistance	Quanta PN	DESCRIPTION
4.99K/F_4	CS24992FB26	RES CHIP 4.99K 1/16W +1%(0402)
10K/F_4	CS31002FB26	RES CHIP 10K 1/16W +1% (0402)
15K/F_4	CS31502FB24	RES CHIP 15K 1/16W +1% (0402)
20K/F_4	CS32002FB29	RES CHIP 20K 1/16W +-1%(0402)
24.9K/F_4	CS32492FB16	RES CHIP 24.9K 1/16W +-1%(0402)
30K/F_4	CS33002FB13	RES CHIP 30K 1/16W +-1%(0402)]
34.8K/F_4	CS33482FB22	RES CHIP 34.8K 1/16W +-1%(0402)
45.3K/F_4	CS34532FB18	RES CHIP 45.3K 1/16W +-1% (0402)

VRAM Configuration Table ※ROM_SI Strap Bit for RAM Mapping

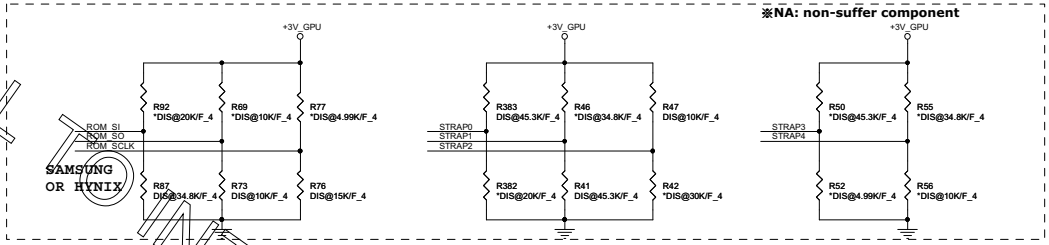
VRAM Configure	Quanta PN(Q buy)	Quanta PN(W buy)	Vendor PN	RAMCFG [3:0]	ROM_SI
900MHz 2GB(128M*16) Samsung	AKD5MGWT500		K4W2G1646C-HC11	0x7(0111)	R87 (45.3K ohm)
900MHz 2GB(128M*16) Hynix	AKD5MGWTW00		H5TQ2G63BFR-11C	0x6(0110)	R87 (34.8K ohm)
900MHz 1GB(64M*16) Samsung	AKD5EGGT500		K4W1G1646G-BC11	0x3(0011)	R87 (20K ohm)
900MHz 1GB(64M*16) Hynix	AKD5LZWTW02		H5TQ1G63DFR-11C	0x2(0010)	R87 (15K ohm)

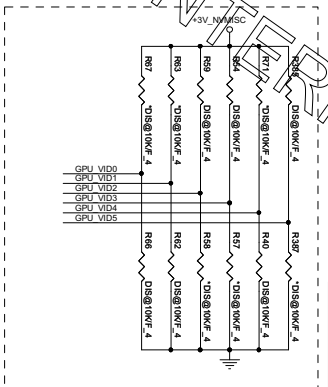
Res	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPU Model Strap Table

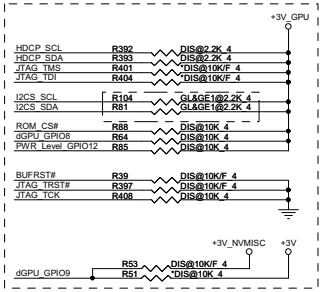
GPU Model	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13M-GE1-A1 (GF119)	R73 (30K ohm) PD	R77 (4.99K ohm) PU	R383 (45.3K ohm) PU	R41 (34.8K ohm) PD	R47 (4.99K ohm) PU	R52 (4.99K ohm) PD	R56 (10K ohm) PD
N13P-GL-A1 (GF108)	R73 (10K ohm) PD	R76 (15K ohm) PD	R383 (45.3K ohm) PU	R41 (45.3K ohm) PD	R47 (10K ohm) PU	NA	NA
N13P-GS-A2 (GK107)	R69 (10K ohm) PU	R77 (4.99K ohm) PU	R383 (45.3K ohm) PU	R41 (34.8K ohm) PD	R42 (15K ohm) PD	R52 (4.99K ohm) PD	R56 (10K ohm) PD

※NA: non-suffer component





NVVDD Table	N13M-GE1-A1 (GF119)	N13P-GL-A1 (GF108)	N13P-GS-A1 (GK107)
	NVVDD (0.9V)	NVVDD (0.95V)	NVVDD (0.9V)
GPU_VID0	0 (R66)	0 (R66)	0 (R66)
GPU_VID1	0 (R62)	0 (R62)	0 (R62)
GPU_VID2	0 (R58)	1 (R59)	0 (R58)
GPU_VID3	0 (R57)	1 (R54)	0 (R57)
GPU_VID4	1 (R71)	0 (R40)	1 (R71)
GPU_VID5	1 (R385)	1 (R385)	1 (R385)



GPIO ASSIGNMENTS

GPIO0	GPU_VID4	O	GPU Core VDD VID4
GPIO1	GPU_VID3	O	GPU Core VDD VID3
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control
GPIO3	LCD_VCC or PSI	O	Panel Power Enable or Phase Shedding
GPIO4	LCD_BLEN	O	Panel Backlight Enable
GPIO5	GPU_VID1	O	GPU Core VDD VID1
GPIO6	GPU_VID2	O	GPU Core VDD VID2
GPIO7	3D Vision	O	3D Vision Left/Right signal
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature
GPIO9	ALERT	I/O	Active Low Thermal Alert
GPIO10	MEM_VREF_CTL	O	Memory VREF Control
GPIO11	GPU_VID0	O	GPU Core VDD VID0
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input
GPIO13	GPU_VID5	O	GPU Core VDD VID5
GPIO14	HPD_AB	I	Hot Plug Detect for IFPAB
GPIO15	HPD_C	I	Hot Plug Detect for IFPC
GPIO16	PSI or MEM_VDD_CTL	O	Phase Shedding or Memory VDD VID
GPIO17	HPD_D	I	Hot Plug Detect for IFPD
GPIO18	HPD_E	I	Hot Plug Detect for IFPE
GPIO19	HPD_F	I	Hot Plug Detect for IFPF
GPIO20	Reserved		
GPIO21	Reserved		

PROJECT : LZ2A
Quanta Computer Inc.
Size: Document Number: Nvidia-N13P GB4-128(GPIO/STRAP) Rev: 1A
Date: Wednesday, November 30, 2011 Sheet 17 of 45

U30E N13P-GS

14/19 NVVDD

GFX_CORE

VDD AA12, AA14, AA16, AA19, AA21, AA23, AB13, AB15, AB17, AB18, AB20, AB22, AC12, AC14, AC16, AC19, AC21, AC23, M12, M14, M16, M19, M21, M23, N13, N15, N17, N18, N20, N22, P12, P14, P16, P19, P21, P23, R13, R15, R17, R18, R20, R22, T12, T14, T16, T19, T21, T23, U13, U15, U17, U18, U20, U22, V13, V15, V17, V18, V20, V22, W12, W14, W16, W19, W21, W23, Y13, Y15, Y17, Y18, Y20, Y22

bga908-nvidia-n13p-gs-a1

GFX_CORE — PLACE UNDER BALLS

C85	DIS@0.1U/10V_4
C54	DIS@0.1U/10V_4
C46	DIS@0.1U/10V_4
C47	DIS@0.1U/10V_4
C59	DIS@4.7U/6.3V_6
C68	DIS@4.7U/6.3V_6
C79	DIS@4.7U/6.3V_6
C72	DIS@4.7U/6.3V_6
C80	DIS@4.7U/6.3V_6
C71	DIS@4.7U/6.3V_6
C63	DIS@4.7U/6.3V_6
C67	DIS@4.7U/6.3V_6
C50	DIS@4.7U/6.3V_6
C86	DIS@4.7U/6.3V_6

GFX_CORE — PLACE NEAR BALLS

C93	DIS@22U/6.3V_8
C66	DIS@47U/6.3V_8
C61	DIS@4.7U/6.3V_6
C73	DIS@4.7U/6.3V_6
C74	DIS@4.7U/6.3V_6
C90	DIS@4.7U/6.3V_6
C87	DIS@4.7U/6.3V_6
C76	*DIS@330U/2V/ESR9_7343

U30G N13P-GS

16/19 GND_1/2

GND A2, AA17, AA18, AA20, AA22, AB12, AB14, AB16, AB19, AB2, AB21, A33, AB23, AB28, AB30, AB32, AB5, AB7, AC13, AC15, AC17, AC18, AA13, AC20, AC22, AE2, AE28, AE30, AE32, AE33, AE5, AE7, AH10, AA15, AH13, AH16, AH19, AH2, AH22, AH24, AH28, AH29, AH30, AH32, AH33, AH5, AH7, AJ7, AK10, AK7, AL12, AL14, AL15, AL17, AL18, AL2, AL20, AL21, AL23, AL24, AL26, AL28, AL30, AL32, AL33, AL5, AM13, AM16, AM19, AM22

GND AM25, AN1, AN10, AN13, AN16, AN19, AN22, AN25, AN30, AN34, AN4, AN7, AP2, AP33, B1, B10, B22, B25, B28, B31, B34, B4, B7, C10, C13, C19, C22, C25, C28, C7, D2, D31, D33, E10, E22, E25, E5, E7, F28, F7, G10, G13, G16, G19, G2, G22, G25, G28, G3, G30, G32, G33, G5, G7, K2, K28, K30, K32, K33, K5, K7, M13, M15, M17, M18, M20, M22, N12, N14, N16

bga908-nvidia-n13p-gs-a1

U30I N13P-GS

17/19 GND_2/2

GND N19, N2, N21, N23, N28, N30, N32, N33, N5, N7, P13, P15, P17, P18, P20, P22, R12, R14, R16, R19, R21, R23, T13, T15, T17, T18, T2, T20, T22

GND T28, T32, T5, T7, U12, U14, U16, U19, U21, U23, V12, V14, V16, V19, V21, V23, W13, W15, W17, W18, W20, W22, W28, Y12, Y14, Y16, Y19, Y21, Y23

AG11 GND — GND AH11

Optional CMD GNDs (2)
NC for 4-Lyr cards

GND_OPT C16
GND_OPT W32

bga908-nvidia-n13p-gs-a1

To be configured as needed on the PCB

U30H N13P-GS

CONFIGURABLE POWER CHANNELS

10/19 XVDD

XVDD U1, U2, U3, U4, U5, U6, U7, U8, V1, V2, V3, V4, V5, V6, V7, V8, W2, W3, W4, W5, W7, W8, Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8, AA1, AA2, AA3, AA4, AA5, AA6, AA7, AA8

bga908-nvidia-n13p-gs-a1

U30F N13P-GS

18/19 NC/VDD33

	N13P-GT N13P-GS N13P-LP N14P-Q1 N14P-Q3	Other N13M N13P
3V3MISC	VDD33	J8
3V3MISC	VDD33	K8
	VDD33	L8
	VDD33	M8

NC AC6, AJ28, AJ4, AJ6, AL1, C1, D1, D2, D23, D26, H32, T8, V32

bga908-nvidia-n13p-gs-a1

+3V_NVMISC

PLACE NEAR BALLS

C55 DIS@0.1U/10V_4
C53 DIS@0.1U/10V_4

+3V_NVMISC_EN [17,43]

Q12
*GS@AO3404(30V 5.8A)

R74 DIS@0_6

C64 DIS@0.1U/10V_4
C69 DIS@0.1U/10V_4

+3V_GPU

C84 DIS@1U/6.3V_4
C56 DIS@4.7U/6.3V_6

PLACE NEAR BALLS

PLACE NEAR BGA

	R74	Q12
N13P-GS	Unstuff	Stuff
N13P-GL N13M-GE1	Stuff	Unstuff

Table 5. Stuffing Options

N13P-GT/-GS/-LP, N14P-Q1/-Q3	I2C and GPIO	No stuff FET Stuff 0Ω bypass resistor
	3V3MISC	Stuff FET No stuff 0Ω bypass resistor
Other N13P and N13M	I2C and GPIO	Stuff FET No stuff 0Ω bypass resistor
	3V3MISC	No stuff FET Stuff 0Ω bypass resistor

[redacted]
PROJECT : LZ2A
Quanta Computer Inc.

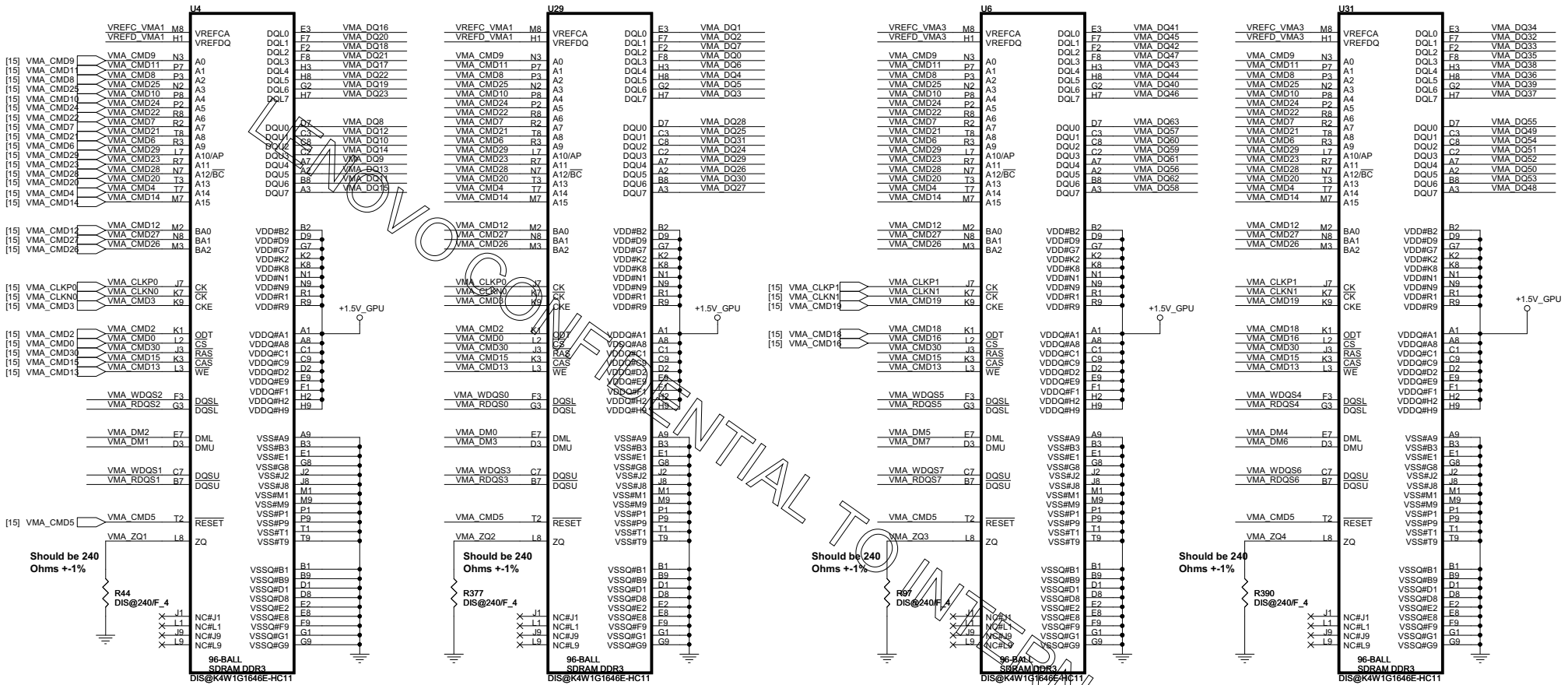
Size	Document Number	Rev
	Nvidia-N13P GB4-128(POWER)	1A

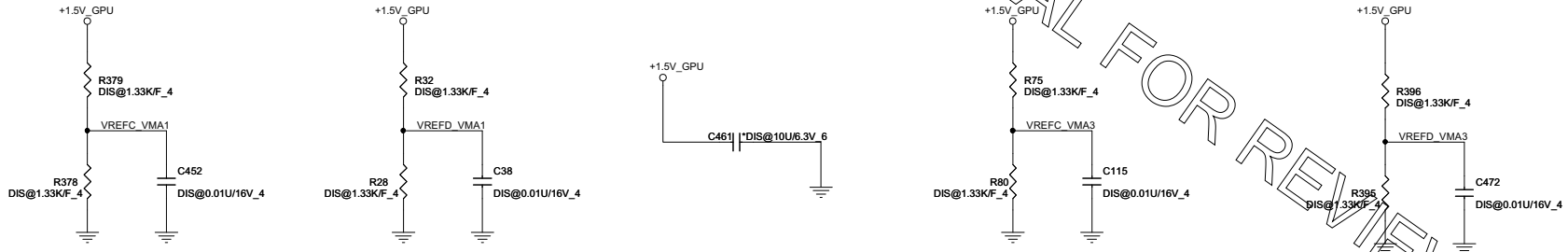
Date: Wednesday, November 30, 2011 Sheet 18 of 45

CHANNEL A: 512MB/1024MB DDR3

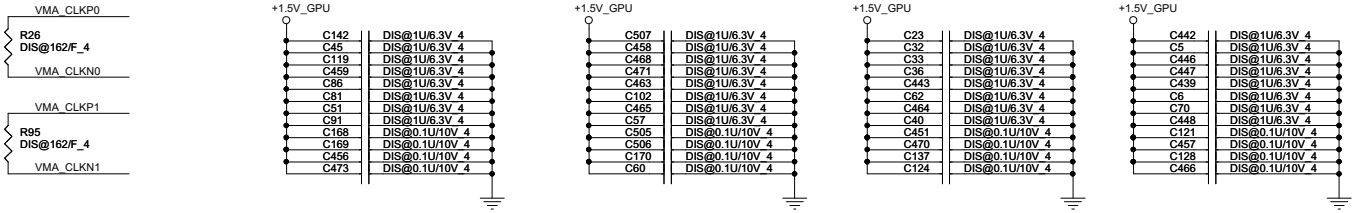
[15] VMA_DQ[63..0]
[15] VMA_DM[7..0]
[15] VMA_WDQS[7..0]
[15] VMA_RDQS[7..0]

[14,15,20,33,43] +1.5V_GPU





Placement has to be close to VRAM



PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	Nvidia-N13P GB4-128(VRAM-1)	1A

Date: Wednesday, November 30, 2011 Sheet 19 of 45

CHANNEL B: 512MB/1024MB DDR3

[15] VMC_DQ[63..0]
[15] VMC_DM[7..0]
[15] VMC_WDQS[7..0]
[15] VMC_RDQS[7..0]

[14,15,19,33,43] +1.5V_GPU

U1 — 96-BALL SDRAM DDR3 — DIS@K4W1G1646E-HC11

U26 — 96-BALL SDRAM DDR3 — DIS@K4W1G1646E-HC11

U2 — 96-BALL SDRAM DDR3 — DIS@K4W1G1646E-HC11

U27 — 96-BALL SDRAM DDR3 — DIS@K4W1G1646E-HC11

Should be 240 Ohms +-1%
R9 DIS@240/F_4

Should be 240 Ohms +-1%
R362 DIS@240/F_4

Should be 240 Ohms +-1%
R6 DIS@240/F_4

Should be 240 Ohms +-1%
R23 DIS@240/F_4

R360 DIS@1.33K/F_4
15 mil width and <500 mil
R361 DIS@1.33K/F_4
C418 DIS@0.01U/16V_4

R4 DIS@1.33K/F_4
R12 DIS@1.33K/F_4
C9 DIS@0.01U/16V_4

C438 *DIS@10U/6.3V_6

R8 DIS@1.33K/F_4
R7 DIS@1.33K/F_4
C4 DIS@0.01U/16V_4

R364 DIS@1.33K/F_4
R358 DIS@1.33K/F_4
C411 DIS@0.01U/16V_4

Placement has to be close to VRAM

R13 DIS@162/F_4
R14 DIS@162/F_4

C25	DIS@1U/6.3V_4
C421	DIS@1U/6.3V_4
C13	DIS@1U/6.3V_4
C110	DIS@1U/6.3V_4
C22	DIS@1U/6.3V_4
C428	DIS@1U/6.3V_4
C11	DIS@1U/6.3V_4
C414	DIS@1U/6.3V_4
C426	DIS@0.1U/10V_4
C431	DIS@0.1U/10V_4
C15	DIS@0.1U/10V_4
C14	DIS@0.1U/10V_4

C415	DIS@1U/6.3V_4
C444	DIS@1U/6.3V_4
C441	DIS@1U/6.3V_4
C422	DIS@1U/6.3V_4
C26	DIS@1U/6.3V_4
C7	DIS@1U/6.3V_4
C10	DIS@1U/6.3V_4
C12	DIS@1U/6.3V_4
C19	DIS@0.1U/10V_4
C140	DIS@0.1U/10V_4
C423	DIS@0.1U/10V_4
C425	DIS@0.1U/10V_4

C419	DIS@1U/6.3V_4
C17	DIS@1U/6.3V_4
C16	DIS@1U/6.3V_4
C429	DIS@1U/6.3V_4
C450	DIS@1U/6.3V_4
C95	DIS@1U/6.3V_4
C417	DIS@1U/6.3V_4
C436	DIS@1U/6.3V_4
C420	DIS@0.1U/10V_4
C424	DIS@0.1U/10V_4
C18	DIS@0.1U/10V_4
C20	DIS@0.1U/10V_4

C413	DIS@1U/6.3V_4
C455	DIS@1U/6.3V_4
C416	DIS@1U/6.3V_4
C412	DIS@1U/6.3V_4
C445	DIS@1U/6.3V_4
C440	DIS@1U/6.3V_4
C24	DIS@1U/6.3V_4
C434	DIS@1U/6.3V_4
C433	DIS@0.1U/10V_4
C435	DIS@0.1U/10V_4
C449	DIS@0.1U/10V_4
C8	DIS@0.1U/10V_4

PROJECT : LZ2A
Quanta Computer Inc.
Size | Document Number: Nvidia-N13P GB4-128(VRAM-2) | Rev 1A
Date: Wednesday, November 30, 2011 | Sheet 20 of 45

Change to KL6/BC HDMI CONN

[6] INT_HDMI_TXDP2 — C620 0.1U/10V_4 — HDMI_TX2+
[6] INT_HDMI_TXDN2 — C619 0.1U/10V_4 — HDMI_TX2-
[6] INT_HDMI_TXDP1 — C618 0.1U/10V_4 — HDMI_TX1+
[6] INT_HDMI_TXDN1 — C617 0.1U/10V_4 — HDMI_TX1-
[6] INT_HDMI_TXDP0 — C616 0.1U/10V_4 — HDMI_TX0+
[6] INT_HDMI_TXDN0 — C615 0.1U/10V_4 — HDMI_TX0-
[6] INT_HDMI_TXCP — C613 0.1U/10V_4 — HDMI_CLK+
[6] INT_HDMI_TXCN — C611 0.1U/10V_4 — HDMI_CLK-

[6] INT_HDMI_SCL — INT_HDMI_SCL
[6] INT_HDMI_SDA — INT_HDMI_SDA
[6] INT_HDMI_HPD — INT_HDMI_HPD

R315 590/F_4 HDMI_TX2+
R310 590/F_4 HDMI_TX2-
R304 590/F_4 HDMI_TX1+
R302 590/F_4 HDMI_TX1-
R300 590/F_4 HDMI_TX0+
R298 590/F_4 HDMI_TX0-
R294 590/F_4 HDMI_CLK+
R291 590/F_4 HDMI_CLK-

SC51 *0.1U/10V_4
3HDMI_LF
Q42 2N7002K
+5V

+3V
R316 2.2K_4
R297 2.2K_4
Q43 DMN5L06K-7
INT_HDMI_SCL
INT_HDMI_SDA
Q39 DMN5L06K-7
+5V
R313 2.2K_4
R568 2.2K_4
F2 FUSE_1.1A_8V_POLY
C668 *68p/50V_4
C669 *68p/50V_4
C667 0.1U/10V_4

CN16 CONN_HDMI

HDMI_TX2+	1	D2+	SHELL1 20
	2	D2 Shield	SHELL2 21
HDMI_TX2-	3	D2-	
HDMI_TX1+	4	D1+	
	5	D1 Shield	
HDMI_TX1-	6	D1-	
HDMI_TX0+	7	D0+	
	8	D0 Shield	
HDMI_TX0-	9	D0-	
HDMI_CLK+	10	CK+	
	11	CK Shield	
HDMI_CLK-	12	CK-	
	13	CE Remote	
	14	NC	
HDMI_DDC_CLK	15	DDC CLK	
HDMI_DDC_DAT	16	DDC DATA	
	17	GND	
HDMIC_5V	18	+5V	
HP_DET	19	HP DET	SHELL3 22
			SHELL4 23

+3V
R551 10K_4
INT_HDMI_HPD
Q69A ME2N7002DKW-G
R553 10K_4
HP_DET
Q69B ME2N7002DKW-G
R549 20K_4
Place close to PCH

For ESD

U39 *CM1225

HDMI_TX2+	6	NC CH4	5 HDMI_TX2+
HDMI_TX2-	7	NC CH3	4 HDMI_TX2-
	8	GND GND	3
HDMI_TX1+	9	NC CH2	2 HDMI_TX1+
HDMI_TX1-	10	NC CH1	1 HDMI_TX1-

U38 *CM1225

HDMI_TX0+	6	NC CH4	5 HDMI_TX0+
HDMI_TX0-	7	NC CH3	4 HDMI_TX0-
	8	GND GND	3
HDMI_CLK+	9	NC CH2	2 HDMI_CLK+
HDMI_CLK-	10	NC CH1	1 HDMI_CLK-

U37 *CM1225

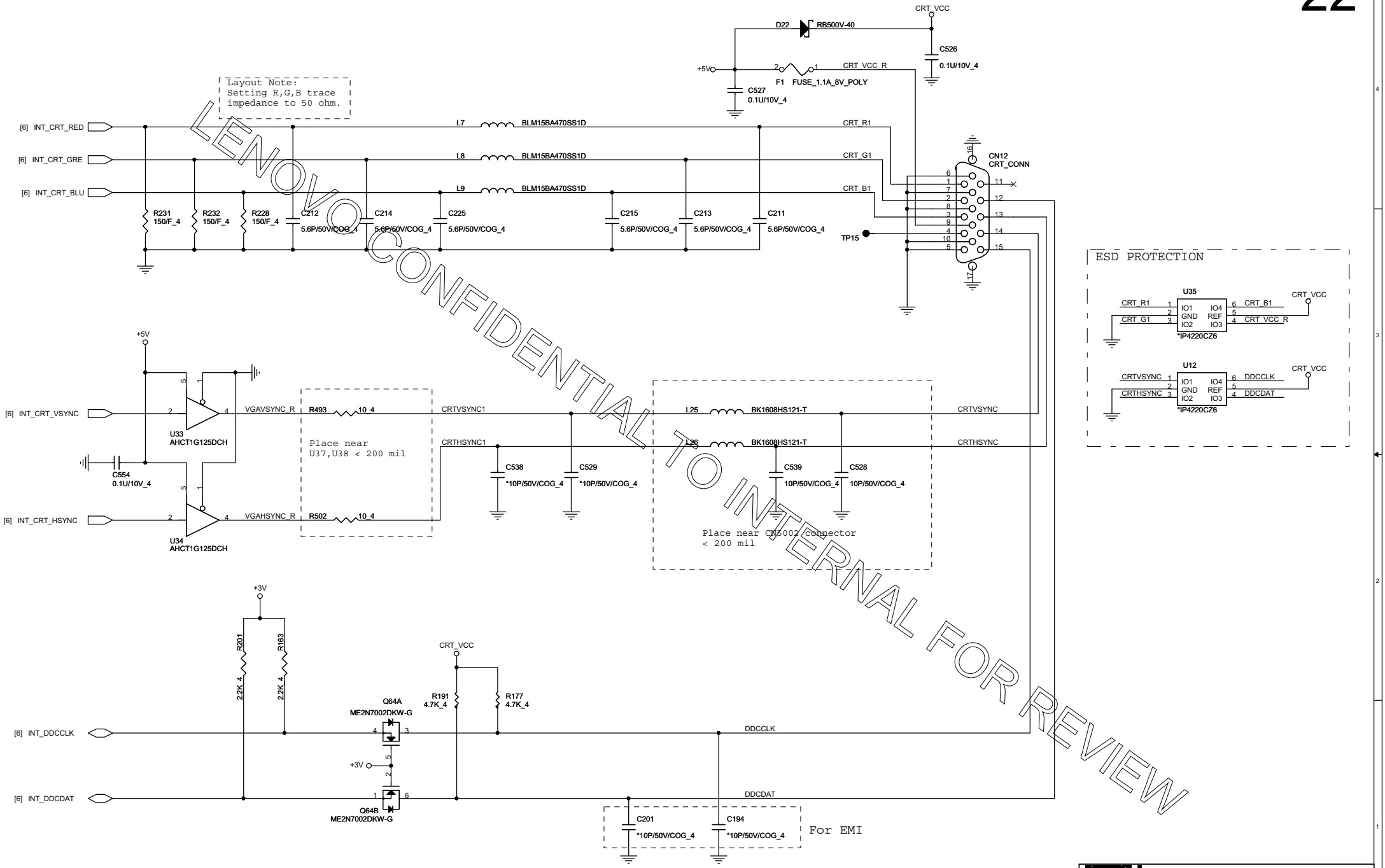
HDMI_DDC_DAT	6	NC CH4	5 HDMI_DDC_DAT
HDMI_DDC_CLK	7	NC CH3	4 HDMI_DDC_CLK
	8	GND GND	3
HDMIC_5V	9	NC CH2	2 HDMIC_5V
HP_DET	10	NC CH1	1 HP_DET

For EMI

HDMI_TX2+ — R574 150/F_4
HDMI_TX2-
HDMI_TX1+ — R573 150/F_4
HDMI_TX1-
HDMI_TX0+ — R572 150/F_4
HDMI_TX0-
HDMI_CLK+ — R569 150/F_4
HDMI_CLK-

PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Madison_LVDS/HDMI/CRT switchable	1A
Date: Wednesday, November 30, 2011	Sheet 21 of 45	



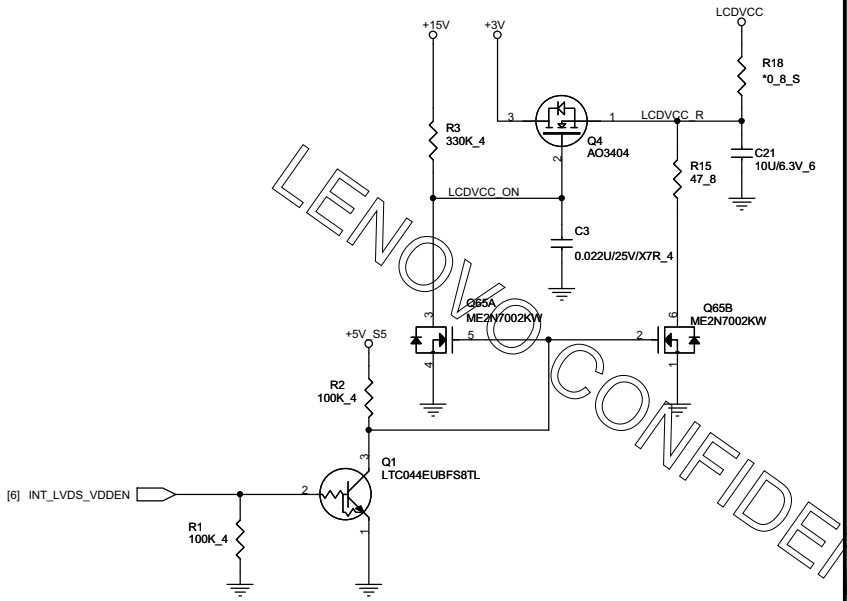
PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT CONN	1A

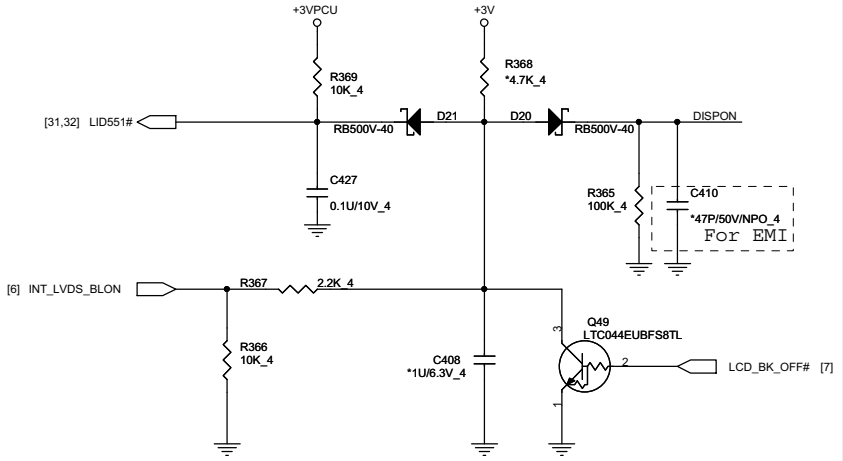
Date: Wednesday, November 30, 2011 Sheet 22 of 45

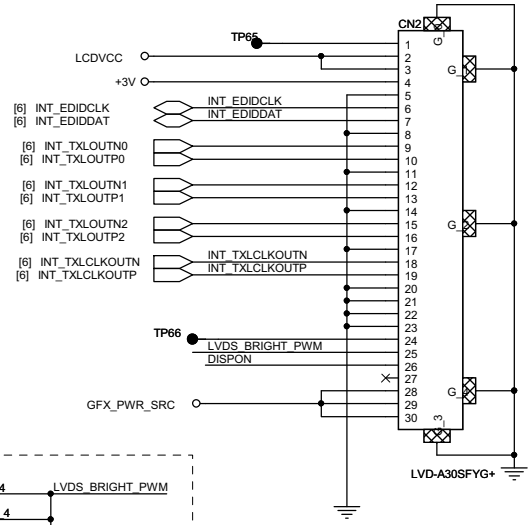
[26,30,34,36,43] +15V
[6,7,8,9,10,12,13,14,15,17,21,22,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43] +3V
[10,26,28,31,33,34] +5V_S5
[6,7,24,26,27,31,32,34,35,36,40] +3VPCU
[33,35,36,37,38,39,41,42] VIN

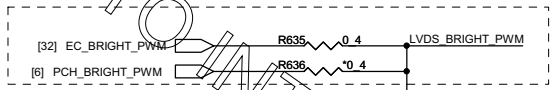
LCDVCC

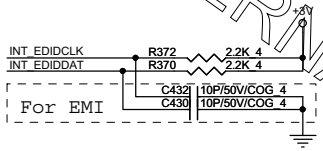


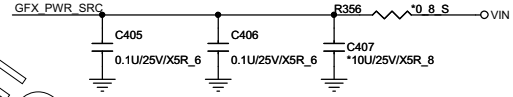
Back Light

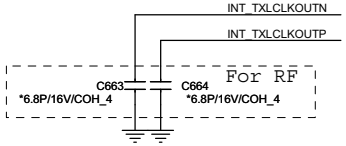












PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN	1A
Date: Wednesday, November 30, 2011	Sheet 23 of 45	

LANVCC

+3VPCU, LANVCC
Q47 AO6402A
[34] LAN_ON
R341 *0_8_S
LANVCC_R
C394 *10U/6.3V_8
C393 0.1U/10V_4

* R594 open when use RTL8105E

TP60, R594 *LAN1G@10K_4, R599 1K/F_4, TP62, R606 10K_4, R603 10K_4
C650 *10P/50V/COG_4 RJ45_LINKUP#
C644 *10P/50V/COG_4 RJ45_ACTIVITY#
LED3/EEDO, EECS, EEDI

RTL81111F/RTL8105E

U45

CTRL12/VDD	34,35	VDDREG	
LANVCC	47,48,42,12,27,39	AVDD33 / AVDD33(NC) / DVDD33 / DVDD3	
CTRL12A	36	REGOUT	
LAN_DVDD12	45,3,6,9,13,29,41	AVDD10 / AVDD10(NC) / DVDD10 / DVDD10(NC)	
LAN_EVDD12	21	EVDD10	
	25	PERSTB	[2,8,14,27] PLTRST#
	16	CLKREQB	[8] PCIE_CLKREQ_LAN#
	17	HSOP	
	18	HSON	
	19	HSIN	
	20	HSIP	
	22	REFCLK_P	
	23	REFCLK_N	
	24	GND	
	49	GND	
	46	RSET	R593 2.49K/F_4
	43	CKXTAL1	Y4 25MHZ, C637 33P/50V/NPO_4
	44	CKXTAL2	C638 33P/50V/NPO_4
	38	GPO/SMBALERT	
	14	SMBCLK(NC)/SMBDATA(NC)	
	15	LED1/EESK	
	37	LED0	
	40	LED3/EEDO	
	31	EECS/SCL	
	30	EEDI/SDA	
	32		

MDIP0 / MDIN0	1 / 2	MDI_0+ / MDI_0-
MDIP1 / MDIN1	4 / 5	MDI_1+ / MDI_1-
MDIP2(NC) / MDIN2(NC)	7 / 8	MDI_2+ / MDI_2-
MDIP3(NC) / MDIN3(NC)	10 / 11	MDI_3+ / MDI_3-
ISOLATEB	26	ISOLATEB
LANWAKEB	28	PCIE_WAKE# [6,27,32]
ENSWREG	33	LANVCC

+3V, R601 1K_4, R600 15K_4, D24 RB500V-40, LAN_ISOLATEB [32]

GPP_TX2N_LAN C649 0.1U/10V_4 → PCIE_RXN2_LAN [8]
GPP_TX2P_LAN C646 0.1U/10V_4 → PCIE_RXP2_LAN [8]
CLK_PCIE_LANN [8]
CLK_PCIE_LANP [8]
PCIE_TXN2_LAN [8]
PCIE_TXP2_LAN [8]

LANVCC: C656 0.1U/10V_4, C654 0.1U/10V_4, C633 0.1U/10V_4, C648 0.1U/10V_4, C639 0.1U/10V_4, R607 *0_8_S, C634 0.1U/10V_4, C653 0.1U/10V_4, C657 4.7U/6.3V_6

CTRL12/VDD

* C5110 to C5113 are for U5006 VDD33 pins-- 1, 29, 37 and 40.

Place C5113 ,C5094 closed to U5006 pins44,45.

* C476 and C472 are for U24 LAN_EVDD12 pin 21.

CTRL12A, L28 4.7uH, CTRL12A_R, C662 4.7U/6.3V_6, C661 0.1U/10V_4, R609 *0_8_S, R611 *0_8_S, LAN_EVDD12, C659 1U/6.3V_4, C642 0.1U/10V_4

LAN_DVDD12: C635, C632, C636, C655, C641, C630, C631 0.1U/10V_4

* C5119 to C5123 are for U5006 VDD12 pins-- 10, 13, 30, 36, 39.

Tramsformer

Reserve for Surge
Line to Line TVS
U41 *UCLAMP2512T.TCT

U43 *CM1293A-04SO
U22 *LAN1G@CM1293A-04SO
10/100 non-stuff
Reserve for Surge
Line to GND TVS

MDI_0-	R590 1/F_4	MDI_0-_C	
MDI_0+	R589 1/F_4	MDI_0+_C	
MDI_1-	R584 1/F_4	MDI_1-_C	
MDI_1+	R583 1/F_4	MDI_1+_C	
MDI_2-	R588 *LAN1G@1/F_4	MDI_2-_C	
MDI_2+	R587 *LAN1G@1/F_4	MDI_2+_C	
MDI_3-	R586 *LAN1G@1/F_4	MDI_3-_C	
MDI_3+	R585 *LAN1G@1/F_4	MDI_3+_C	

U40 TST1284R LF

12	TD4-	MX4-	13 LAN_MX0-
11	TD4+	MX4+	14 LAN_MX0+
10	TCT4	MCT4	15 LAN_MCT0
9	TD3-	MX3-	16 LAN_MX1-
8	TD3+	MX3+	17 LAN_MX1+
7	TCT3	MCT3	18 LAN_MCT1
6	TD2-	MX2-	19 LAN_MX2-
5	TD2+	MX2+	20 LAN_MX2+
4	TCT2	MCT2	21 LAN_MCT2
3	TD1-	MX1-	22 LAN_MX3-
2	TD1+	MX1+	23 LAN_MX3+
1	TCT1	MCT1	24 LAN_MCT3

Layout:All termination signal should have 30 mil trace

R570 75/F_8 LANCT3 → D30 *BS201N-LV_1206 → LANCT5
Gas Tube Discharge _ Reserve for Surge
R571 75/F_8 → D31 *BS201N-LV_1206
Gas Tube Discharge _ Reserve for Surge
R296 0/F_8 For EMI → D32 *BS201N-LV_1206
Gas Tube Discharge _ Reserve for Surge
R295 0/F_8 For EMI → D33 *BS201N-LV_1206
Gas Tube Discharge _ Reserve for Surge
Reserve for Surge
Line to GND Gas Tube Discharge
C366 10P/3KV/NPO_1808, R327 1M_8

U20 *LAN1G@UCLAMP2512T.TCT
Reserve for Surge
Line to Line TVS
C623 0.01U/50V/X7R_4

PJP18 *SHORTPAD

RJ45 Connector

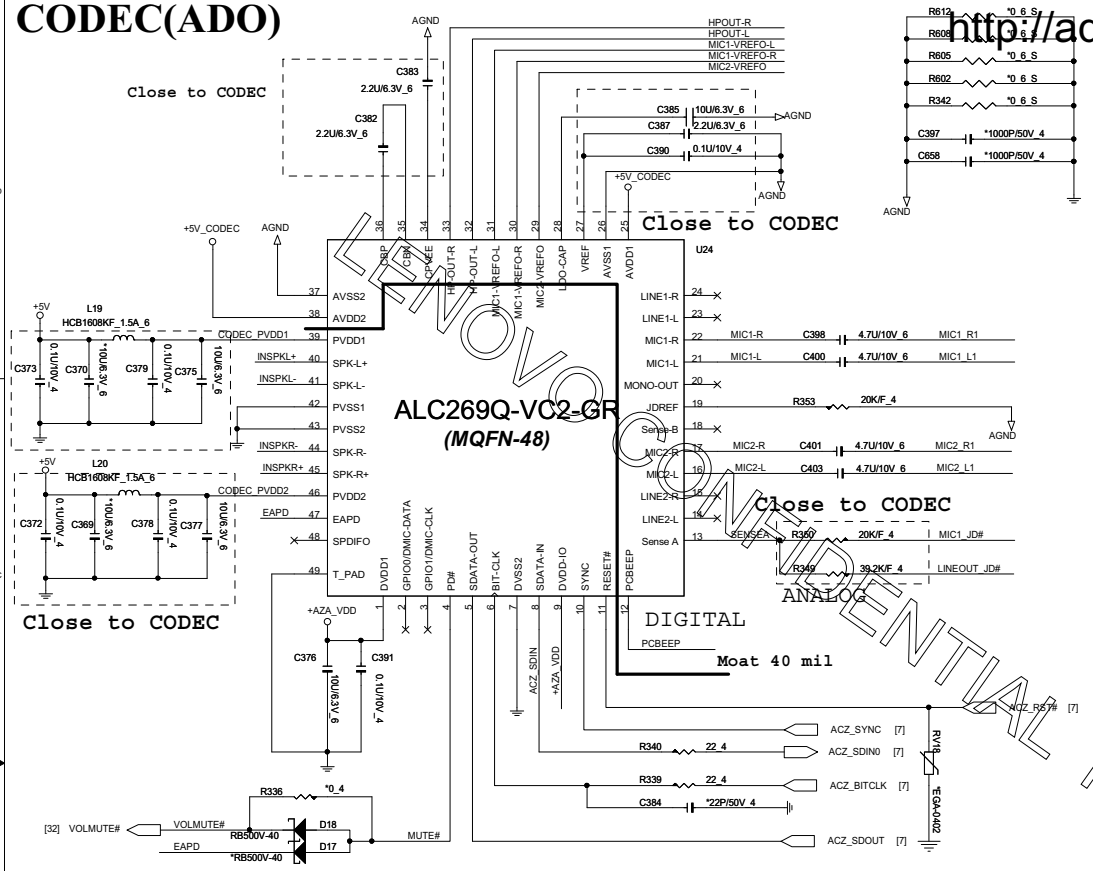
RV15 *AZ5123-01H, RV14 *AZ5123-01H
EMI:close RJ45
C270 *0.1U/10V_4
CN13
Orange LED
LANVCC, R256 150_4, LAN_OLED
RJ45_LINKUP#
LAN_MX0+ 1, LAN_MX0- 2, LAN_MX1+ 3, LAN_MX2+ 4, LAN_MX2- 5, LAN_MX1- 6, LAN_MX3+ 7, LAN_MX3- 8
LANVCC, R567 150_4, LAN_GLED
RJ45_ACTIVITY#
GREEN LED
RJ45
13, 14, 15, 16
RV26 *AZ5123-01H, RV27 *AZ5123-01H
C609 *0.1U/10V_4
EMI:close RJ45

PROJECT : LZ2A
Quanta Computer Inc.

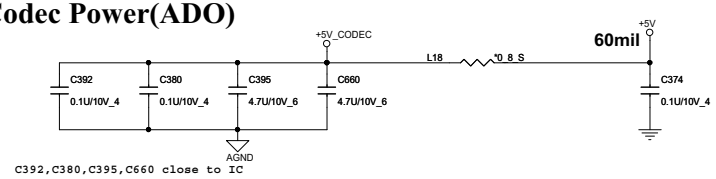
Size	Document Number	Rev
Custom	RTL81111F/RTL8105E	1A

Date: Wednesday, November 30, 2011 Sheet 24 of 45

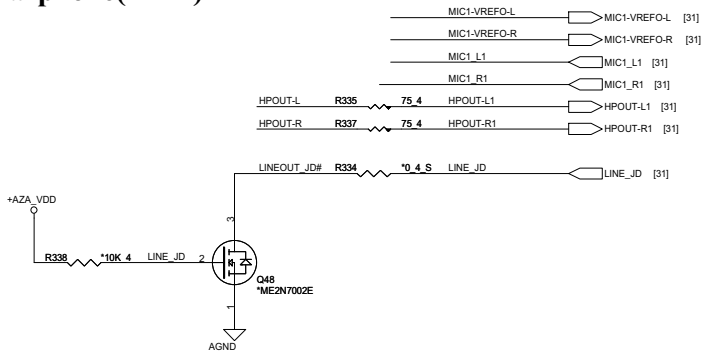
CODEC(ADO)



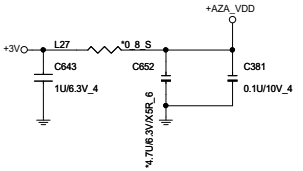
Codec Power(ADO)



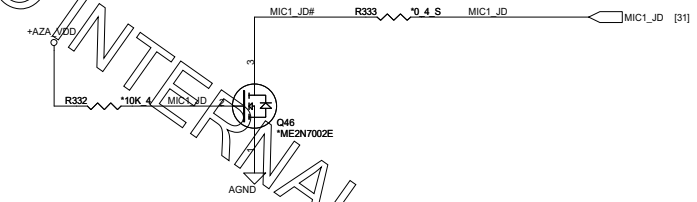
Earphone(AMP)



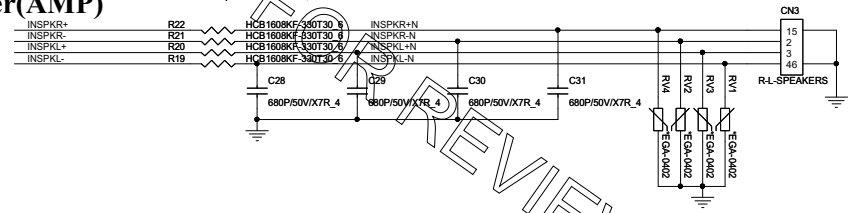
HDA Power(ADO)



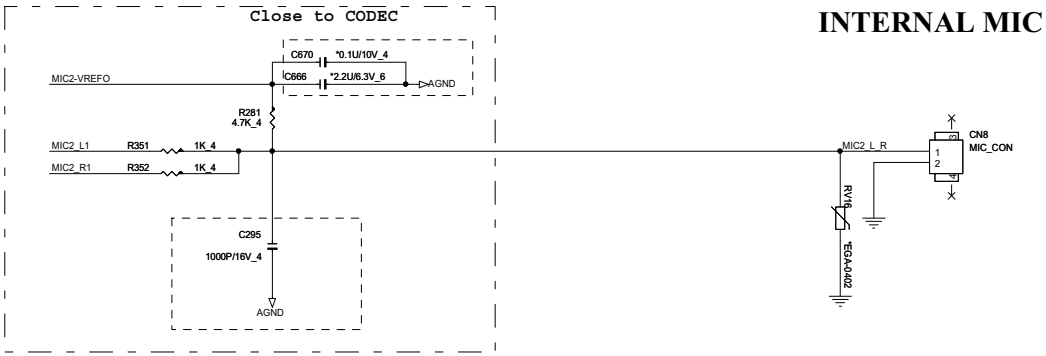
System MIC(AMP)



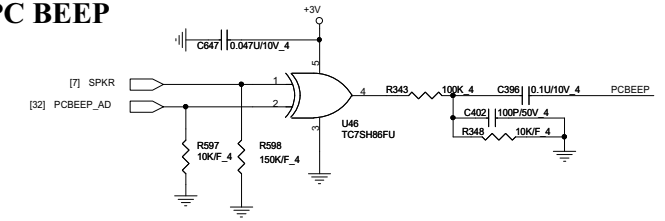
Speaker(AMP)



INTERNAL MIC



PC BEEP



PROJECT : LZ2A	
Quanta Computer Inc.	
Size: Custom	Document Number: ALC269/MIC/Line out
Rev: 1A	
Date: Wednesday, November 30, 2011	Sheet 25 of 45

SATA HDD Connector.

[7,10,21,22,25,29,30,33,34] +5V
[6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,27,29,30,31,32,33,34,37,38,41,42,43] +3V
[10,34,35,36,37,38,39,40,41,42,43] +5VPCU
[6,7,23,24,27,31,32,34,35,36,40] +3VPCU
[23,30,34,36,43] +15V

+5V_HDD
R326 0_8
+5V
C351 0.1U/10V_4
C344 10U/6.3V_6
Place caps close to connector.

+3V_HDD
R319 *0_8_S
+3V
C347 0.1U/10V_4
C337 *10U/6.3V_6
Place caps close to connector.

CN17
GND1 TXP TXN GND2 RXN RXP GND3
3.3V 3.3V 3.3V GND GND GND
5V 5V 5V GND RSVD GND 12V 12V 12V
hole2 hole1
127043FB022G201ZR

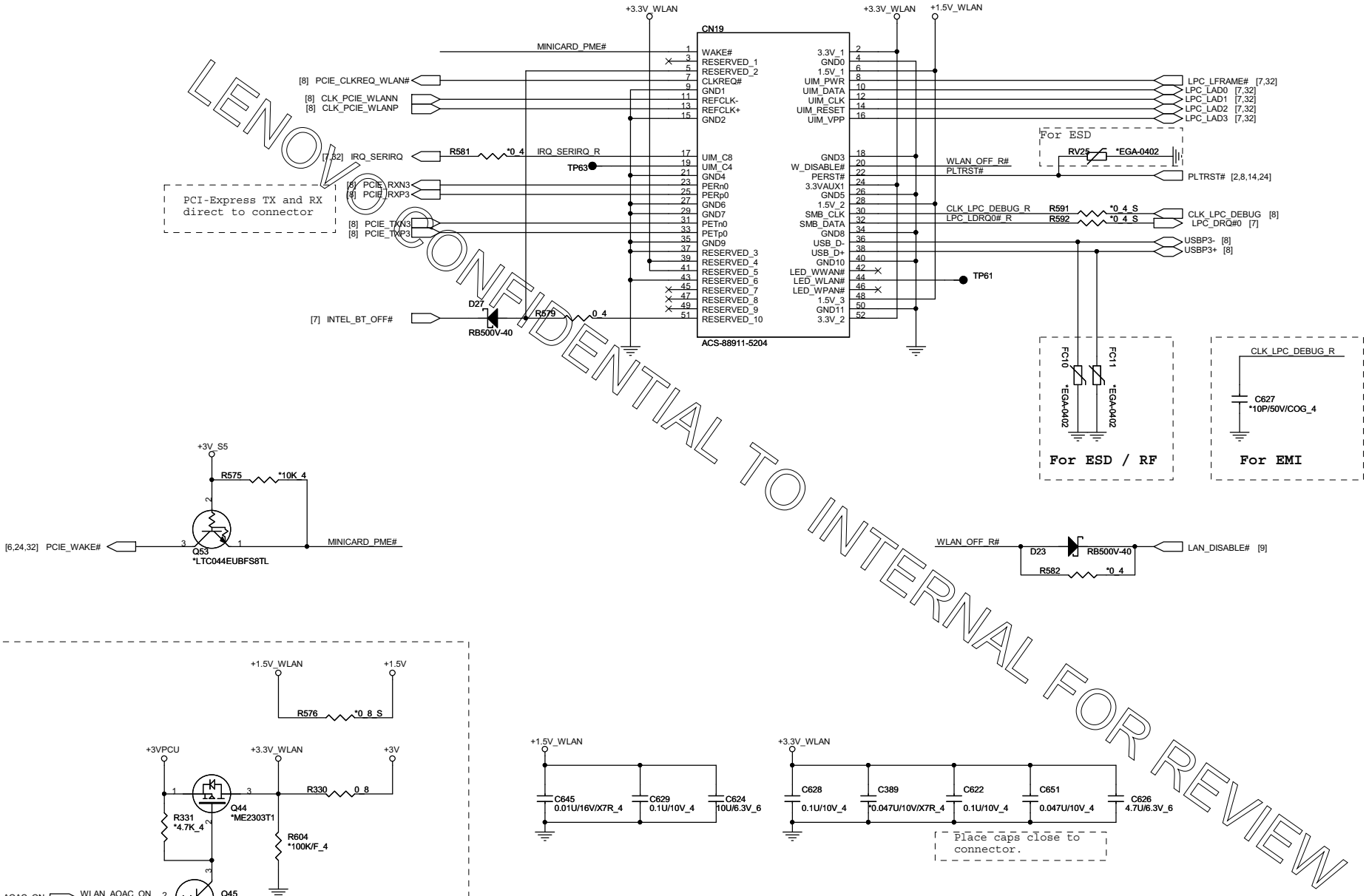
SATA_TXP1 C588 0.01U/16V_4 SATA_TXP1_C [7]
SATA_TXN1 C589 0.01U/16V_4 SATA_TXN1_C [7]
SATA_RXN1_C C612 0.01U/16V/X7R_4 SATA_RXN1 [7]
SATA_RXP1_C C614 0.01U/16V/X7R_4 SATA_RXP1 [7]
Place caps close to connector(<200mil).
+3V_HDD
+5V_HDD

+5V_ODD
120 mils
C258 10U/10V_8
C257 0.1U/10V_4
C255 0.1U/10V_4
C256 0.1U/10V_4
C254 0.1U/10V_4
C272 10U/10V_8
Place caps close to connector.

+5V_S5
Q28 AO6402A
+5V_ODD
+3VPCU
C273 0.1U/10V_4
R257 100K_4
R253 100K_4
+15V
R267 100K_4
OOD_EN_5V
Q66A ME2N7002KW
C274 0.1U/25V_4
Q66B ME2N7002KW
[32] ODD_EN
R264 100K_4

Place caps close to connector(<200mil).
CN14
GND1 TXP TXN GND2 RXN RXP GND3 DP +5V +5V MD GND GND
ODD_CONN
[7] SATA_TXP3_C
[7] SATA_TXN3_C
0.01U/16V_4 C223 SATA_TXP3
0.01U/16V_4 C227 SATA_TXN3
[7] SATA_RXN3
[7] SATA_RXP3
0.01U/16V/X7R_4 C228 SATA_RXN3_C
0.01U/16V/X7R_4 C277 SATA_RXP3_C
[7] ODD_PRSNT#
R266 *0_4_S
[8,32] ODD_MDDA#
R250 *0_4_S
+5V_ODD
R249 10K_4
+3V
R265 1K/F_4

PROJECT : LZ2A
Quanta Computer Inc.
Size Custom
Document Number SATA HDD/CD-ROM
Rev 1A
Date: Wednesday, November 30, 2011 Sheet 26 of 45



PROJECT : LZ2A

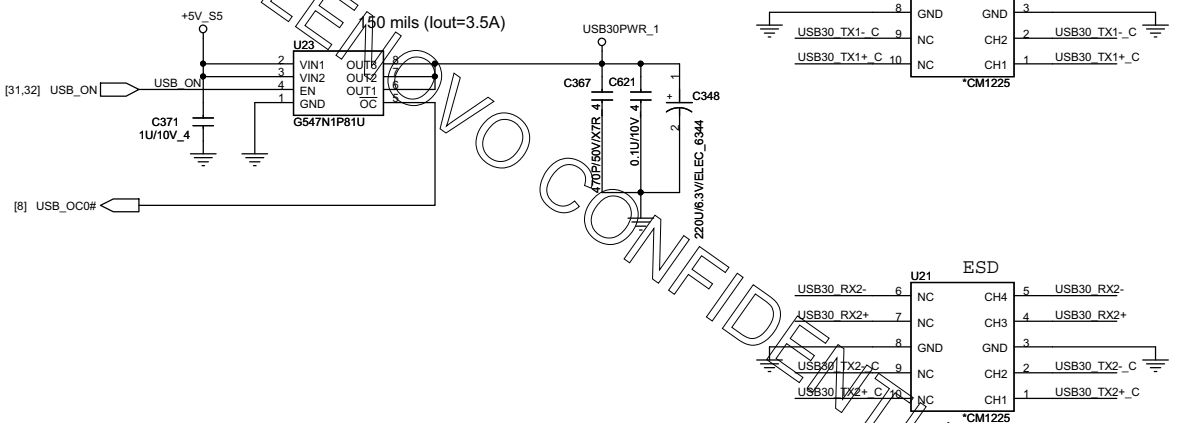
Quanta Computer Inc.

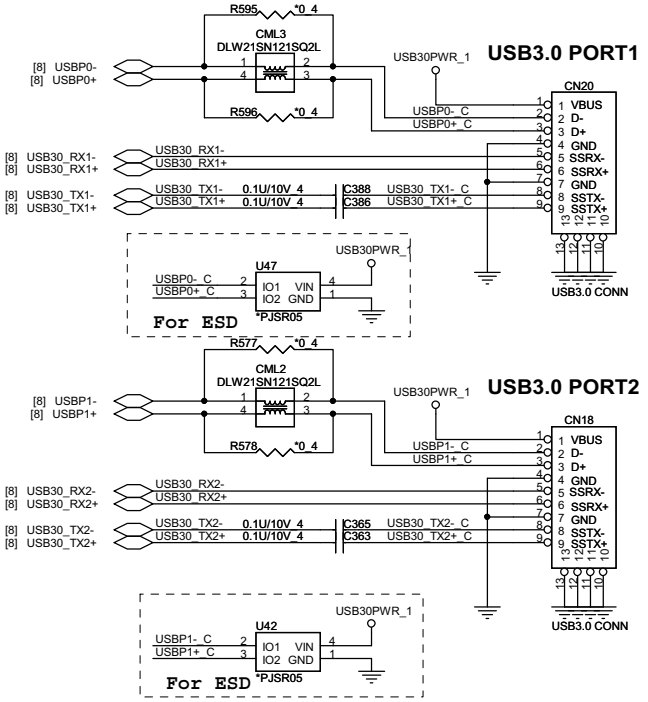
Size	Document Number	Rev
Custom	USB2.0*2/WLAN/BT	1A

Date: Wednesday, November 30, 2011 Sheet 27 of 45

USB3.0*2

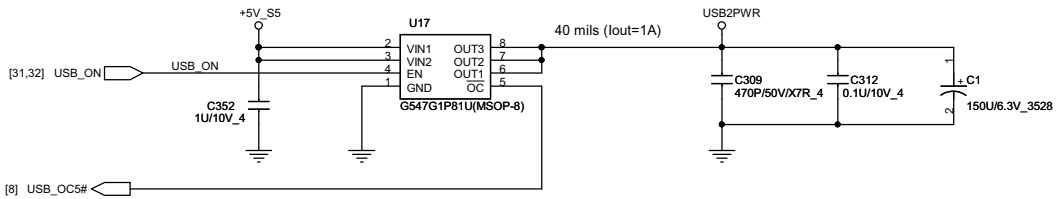
http://adf.ly/3o8pJ

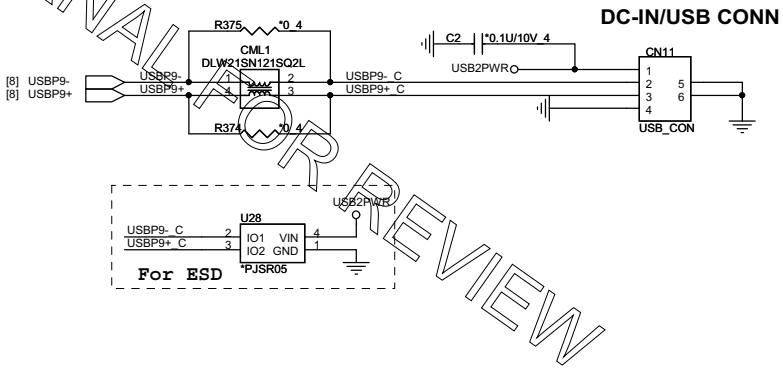




USB2.0*1

DC-IN Board



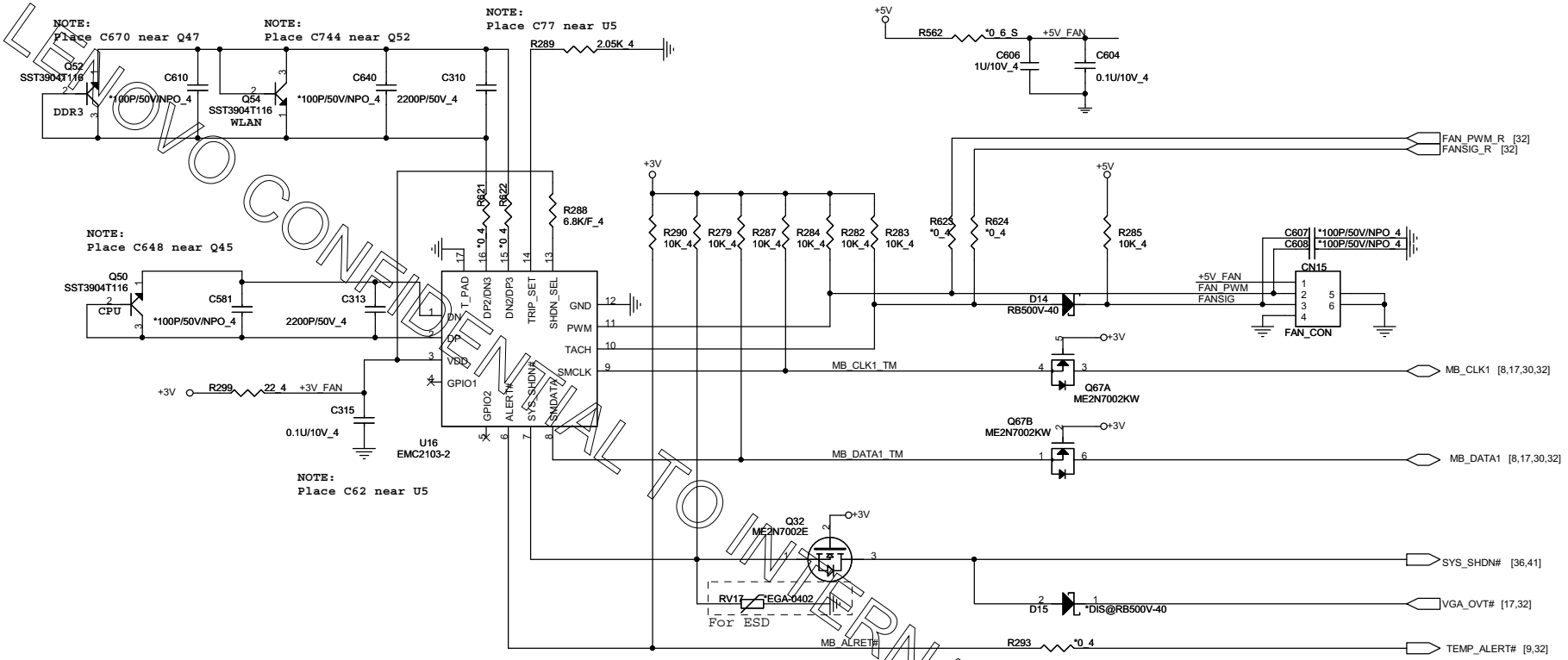


PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB3.0 *1	1A

Date: Wednesday, November 30, 2011 Sheet 28 of 45

FAN CONTROL

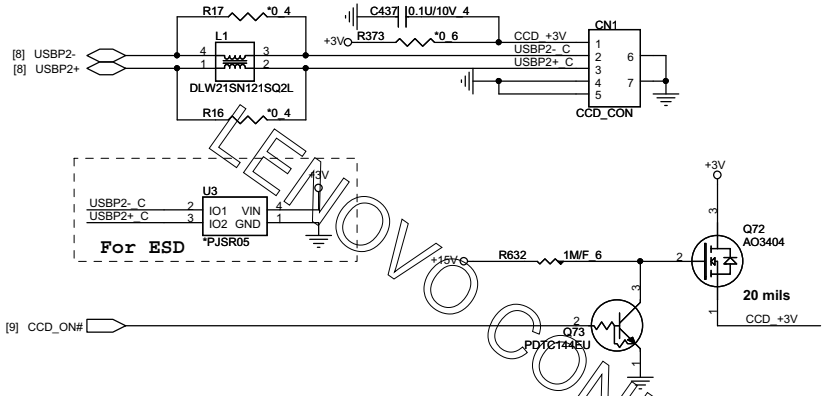


PROJECT : LZ2A
Quanta Computer Inc.

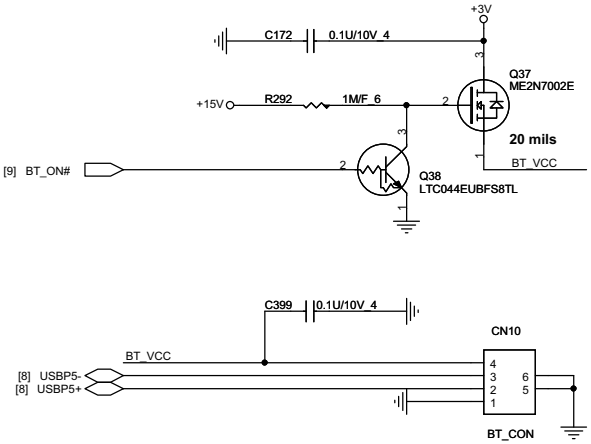
Size	Document Number	Rev
Custom	FAN /THERMAL	1A

Date: Wednesday, November 30, 2011 Sheet 29 of 45

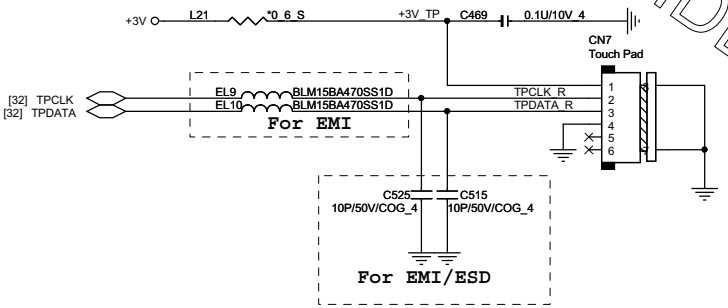
CCD BOARD



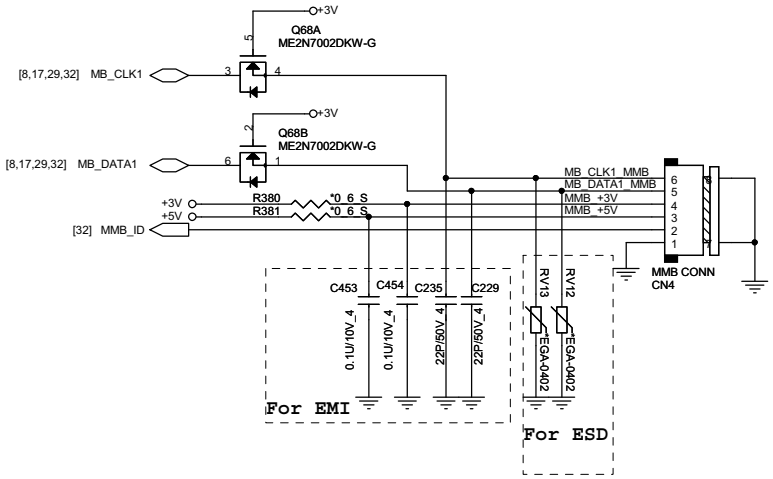
BLUETOOTH



Touch pad



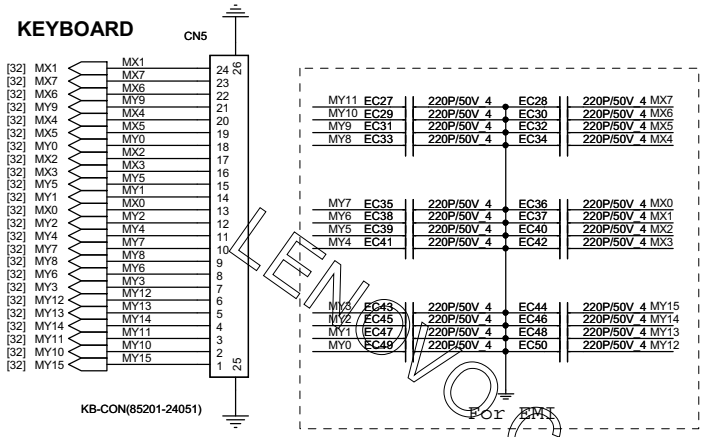
MMB

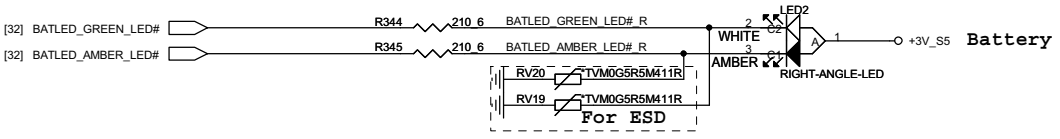


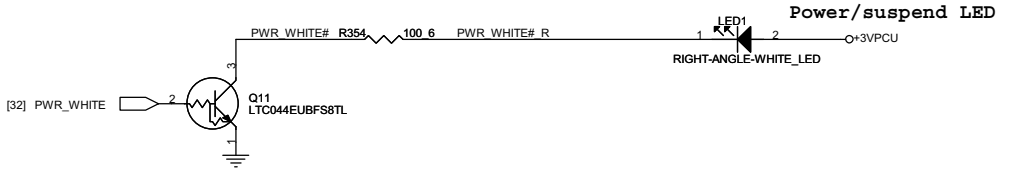
PROJECT : LZ2A
Quanta Computer Inc.

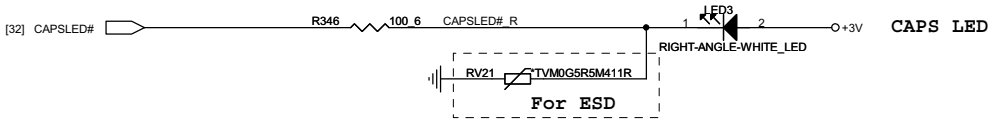
Size	Document Number	Rev
Custom	CCD/TP/BT/MMB	1A
Date: Wednesday, November 30, 2011	Sheet 30 of 45	

KEYBOARD

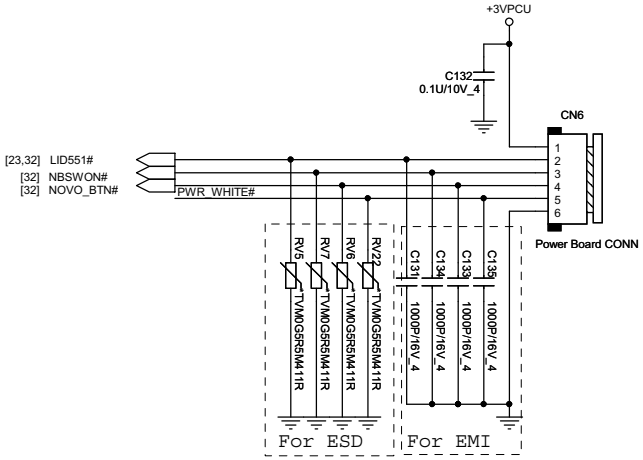




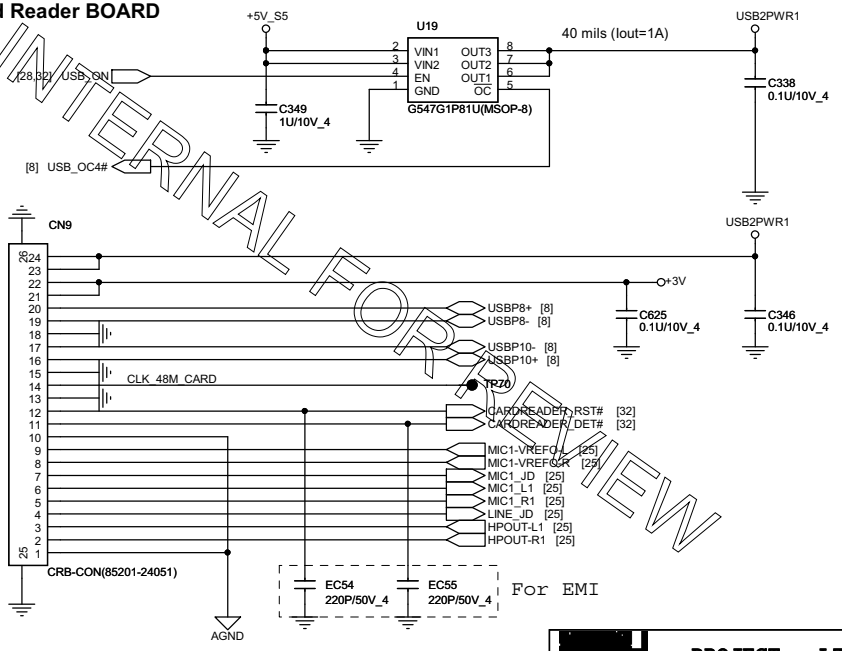




POWER BOARD



Card Reader BOARD



PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB/PB/LED/CRB	1A

Date: Wednesday, November 30, 2011 Sheet 31 of 45

IT8518
IT8519

Board ID

+3VPCU
R116 DIS@10K_4
BOARD_ID
R115 *UMA@10K_4

DIS =>R116
UMA=>R115

POWER SWITCH/ NOVO BUTTON

+3VPCU R216 10K_4 NBSWON# C206 0.1U/10V_4
+3.3V_EC R434 10K_4 NOVO_BTN# C521 0.1U/10V_4

4Mbit (512K Byte), SPI

+3VPCU

Winbond	AKE38ZP0N00
SST	AKE28FP0K07
MX	AKE37FP0Z13

R252 10K_4, R244 10K_4
U14 W25X40BVSSIG
8512_SCE# R236 47_4 8512_SCK1
8512_SCK R247 47_4 8512_SI
8512_SI R248 15_4 8512_SO1
8512_SO
ER3 33_4
EC8 10P/50V_4
C233 0.1U/10V_4
For EMI

Project	PU/PD
Z380(LZ1)-INTEL	PU
Z480(LZ2)-INTEL	PU
Z485(LZ2)-AMD	PU
Z580(LZ3)-INTEL	PD
Z585(LZ3)-AMD	PD

+3V R420 @Z380&Z480_10K_4 KB_ID R406 *@Z580_10K_4

H_PROCHOT# Q R89 *0_4_S H_PROCHOT# [2,41]
Q10 ME2N7002E
H_PROCHOT# EC
R111 100K_4

PROJECT : LZ2A
Quanta Computer Inc.
Size: Custom | Document Number: KBC IT8518 | Rev: 1A
Date: Wednesday, November 30, 2011 | Sheet 32 of 45

Screw for ME

SPAD1 *SPAD-Z480-1
SPAD3 *SPAD-Z480-1
SPAD4 *SPAD-Z480-2
SPAD2 *SPAD-Z480-2

VGA
HOLE12 DIS@H-TC5_5BC4I3D3P2
HOLE13 H-TC5_5BC4I3D3P2

SMT NUT H=4/7mm

HOLE8 *HG-TC276BC315D106P2
HOLE10 *HG-TC276BC315D106P2
HOLE6 *HG-TC256BC315D106P2
HOLE11 *HG-TC276BC315D106P2

CPU BKT

HOLE4 *H-C86D86N
HOLE7 *C142D102N
HOLE3 *H-TC217BC256D118P2
HOLE14 *H-TC7IC3_7BC8D2_7P2
HOLE9 *H-C87D87N
HOLE5 *H-O316X276ID91P2
HOLE2 *H-O316X276ID91P2
HOLE1 *H-TC6_3IC3_7BC8D2_7P2

For ESD

+0.85V +1.8V SC23 *0.1U/10V_4 SC24 *0.1U/10V_4
+1.05V_GFX_PCIE +1.05V_PCH SC31 *0.1U/10V_4 SC32 *0.1U/10V_4
+0.85V +1.5V_CPU SC11 *0.1U/10V_4 SC13 *0.1U/10V_4 SC12 *0.1U/10V_4 SC27 *0.1U/10V_4 SC26 *0.1U/10V_4
+5V_S5 SC42 *0.1U/10V_4
+5V_S5 SC41 *0.1U/10V_4
+1.5V_SUS +1.5V_CPU SC29 *0.1U/10V_4 SC28 *0.1U/10V_4
+1.5V_SUS VIN SC40 0.1U/25V_4 SC39 0.1U/25V_4
+3V +5V SC33 0.1U/10V_4 SC30 0.1U/10V_4
+VCC_CORE VIN SC9 0.1U/25V_4 SC46 0.1U/25V_4
+VCC_GFX SC15 *0.1U/10V_4 SC18 *0.1U/10V_4
+5V SC38 0.1U/10V_4 SC25 0.1U/10V_4 SC37 0.1U/10V_4
+1.05V_GFX_PCIE GFX_CORE SC4 *0.1U/10V_4
+VCC_GFX SC17 *0.1U/10V_4 SC16 *0.1U/10V_4 SC14 *0.1U/10V_4
+1.05V_PCH SC20 *0.1U/10V_4 SC19 *0.1U/10V_4 SC21 *0.1U/10V_4
+1.05V_PCH SC49 *0.1U/10V_4 SC22 *0.1U/10V_4 SC50 *0.1U/10V_4 SC47 *0.1U/10V_4 SC48 *0.1U/10V_4
+1.05V_GFX_PCIE SC6 *0.1U/10V_4 SC5 *0.1U/10V_4
+VCC_CORE SC8 *0.1U/10V_4 SC10 *0.1U/10V_4
+1.5V_GPU SC2 *0.1U/10V_4 SC43 *0.1U/10V_4 SC3 *0.1U/10V_4
+1.5V_GPU SC7 *0.1U/10V_4 SC45 *0.1U/10V_4
+1.5V_GPU SC44 *0.1U/10V_4 SC1 *0.1U/10V_4
+1.5V_SUS SC35 *0.1U/10V_4 SC34 *0.1U/10V_4 SC36 *0.1U/10V_4

For EMI

VIN EC6 0.1U/25V_4 EC20 0.1U/25V_4 EC12 0.1U/25V_4 EC25 0.1U/25V_4 EC1 0.1U/25V_4 EC18 0.1U/25V_4 EC2 0.1U/25V_4 EC21 0.1U/25V_4 EC5 0.1U/25V_4 EC3 0.1U/25V_4 EC16 0.1U/25V_4
LANVCC EC11 0.1U/10V_4
VBATT EC22 0.1U/25V_4
+1.5V_SUS FC2 3.3p/16V/NP0_4
+1.5V_SUS FC1 3.3p/16V/NP0_4
+1.5V_WLAN FC5 47P/50V/NPO_4
+3.3V_WLAN FC3 47P/50V/NPO_4
+5V EC51 0.1U/10V_4 EC52 *0.1U/10V_4

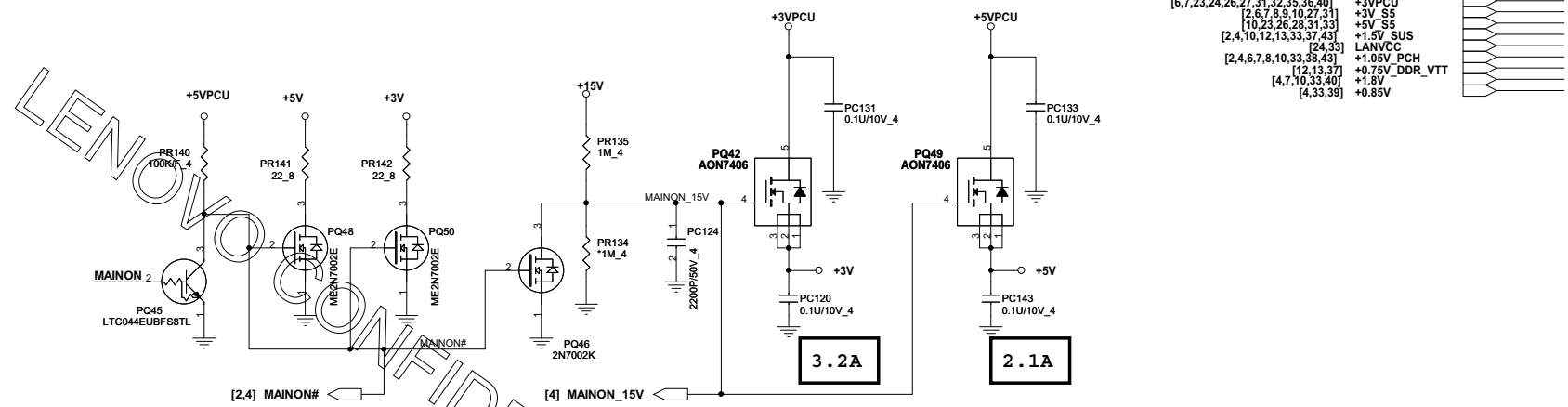
PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
B	HOLD/SKEW/ESD/EMI	1A
Date: Wednesday, November 30, 2011	Sheet 33 of 45	

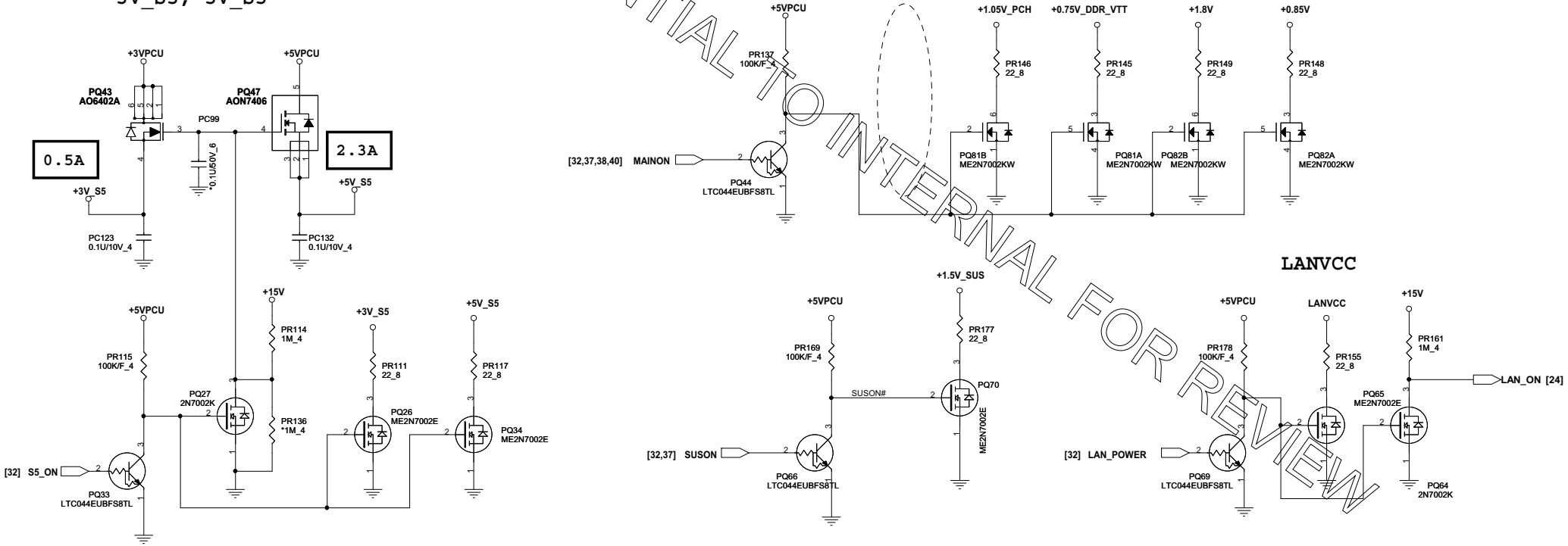
http://adf.ly/3o8pJ

+3V, +5V

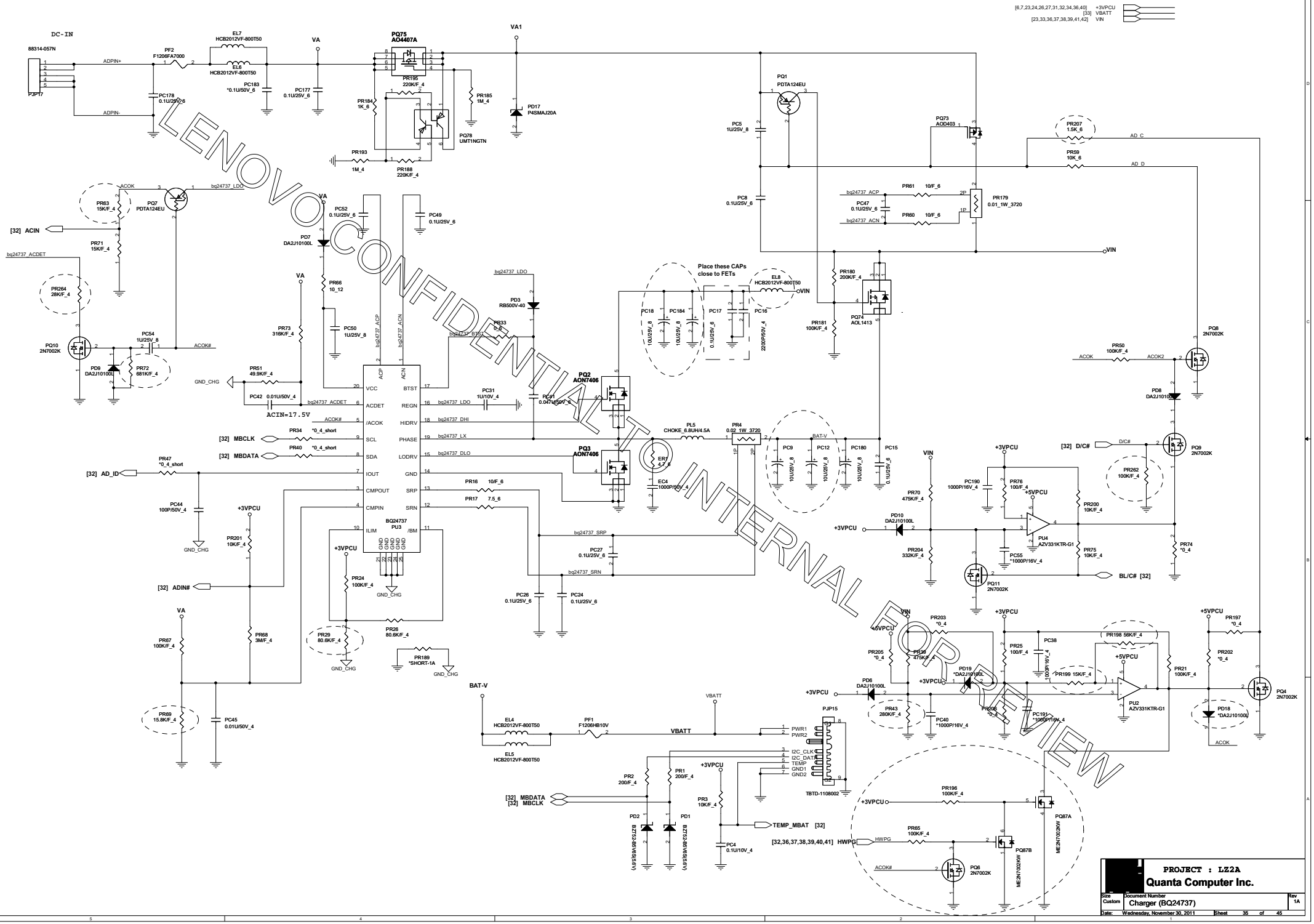
[10,35,36,37,38,39,40,41,42,43] +5VPCU
[7,10,21,22,25,26,29,30,33] +5V
[6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,27,29,30,31,32,33,37,38,41,42,43] +3V
[23,26,30,36,43] +15V
[6,7,23,24,26,27,31,32,35,36,40] +3VPCU
[2,6,7,8,9,10,27,31] +3V_S5
[10,23,26,28,31,33] +5V_S5
[2,4,10,12,13,33,37,43] +1.5V_SUS
[24,33] LANVCC
[2,4,6,7,8,10,33,38,43] +1.05V_PCH
[12,13,37] +0.75V_DDR_VTT
[4,7,10,33,40] +1.8V
[4,33,39] +0.85V

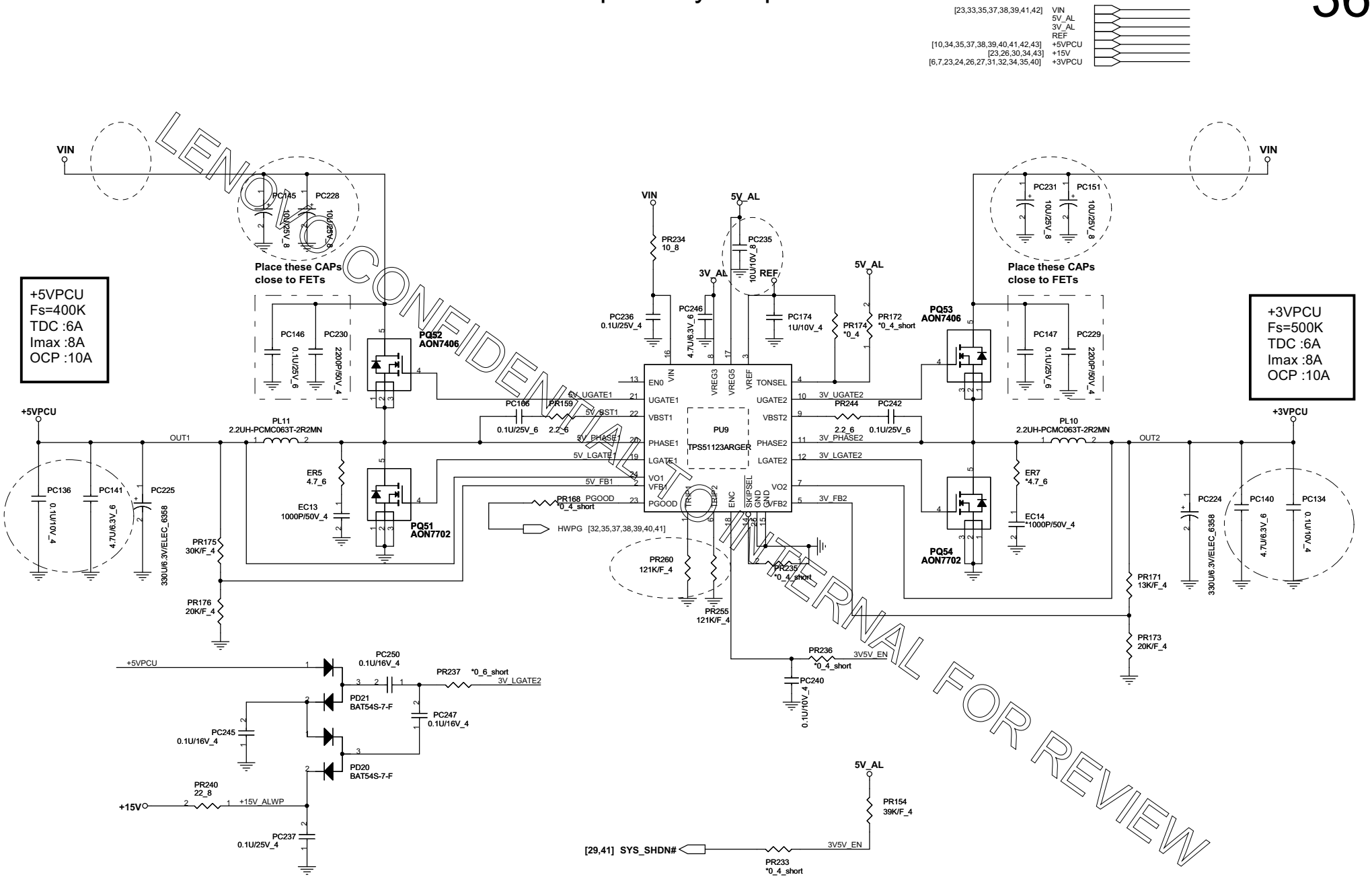


3V_S5, 5V_S5



PROJECT : LZ2A		
Quanta Computer Inc.		
Size	Document Number: Discharge	Rev
Date: Wednesday, November 30, 2011	Sheet 34 of 45	





PROJECT : LZ2A

Quanta Computer Inc.

Size	Document Number	Rev
	3V/5V (TPS51123ARGER)	

Date: Wednesday, November 30, 2011 Sheet 36 of 45

[12,13,34] +0.75V_DDR_VTT

[23,33,35,36,38,39,41,42] VIN
[2,4,10,12,13,33,34,43] +1.5V_SUS

+0.75V_DDR_VTT
TDC : 1A

+0.75V_DDR_VTT

PC165 *0.1U/10V_4
PC163 10U/6.3V_6
PC164 10U/6.3V_6

PR165 100K/F_4

+1.5V_SUS

PC159 10U/6.3V_6

VTTGND
VTTSNS
GND
MODE
VREF
VLDOIN
VBST
DRVH
LL
DRVL
PGND
V5IN
REFIN
VDDQSNS
VTTREF
S3
S5
PGOOD
TRIP

PU6
TPS51216

DDR_VBST
DDR_LL
DRVH
DRVL
DDR_V5IN
DDR_VREF
DDR_REFIN
DDR_VDDQS
DDR_VTTREF_R
DDR_TRIP

PR157 2.2_6
PC161 0.1U/25V_6

PR152 *0_6_short
PC156 1U/10V_4

PR167 10K/F_4
+3V

PR166 *0_4_short
PD15 RB500V-40
PD14 RB500V-40
HWPG [32,35,36,38,39,40,41]
DRAMPWRGD [32]

PR164 71.5K/F_4

PR151 10K/F_4
PR150 53.6K/F_4
R1
R2

PC150 0.1U/10V_4
PC149 0.01U/50V_4

Vo=1.8*R2/(R1+R2)

PR153 0_4
PC154 0.22U/10V_4

[4,12,13] SMDDR_VREF

PR143 *0_4
[32] EC_SLP_S4#
EC_SLP_S4#
PR163 100K_4
[32,34,38,40] MAINON
PD16 DA2J10100L
PC170 0.1U/10V_4

PR162 0_4
[32,34] SUSON
PR144 *0_4
EC_SLP_S4#
PC169 *0.1U/10V_4

Place these CAPs close to FETs

VIN

PC173 0.1U/25V_6
PC162 2200P/50V_4
PC153 10U/25V_8
PC158 10U/25V_8

PQ68
SK850305KL

PQ67
SK8603020L

PL2
1.0uH/PCMC104T-1R0MN

ER9 *4.7_6
EC17 *1000P/50V_4

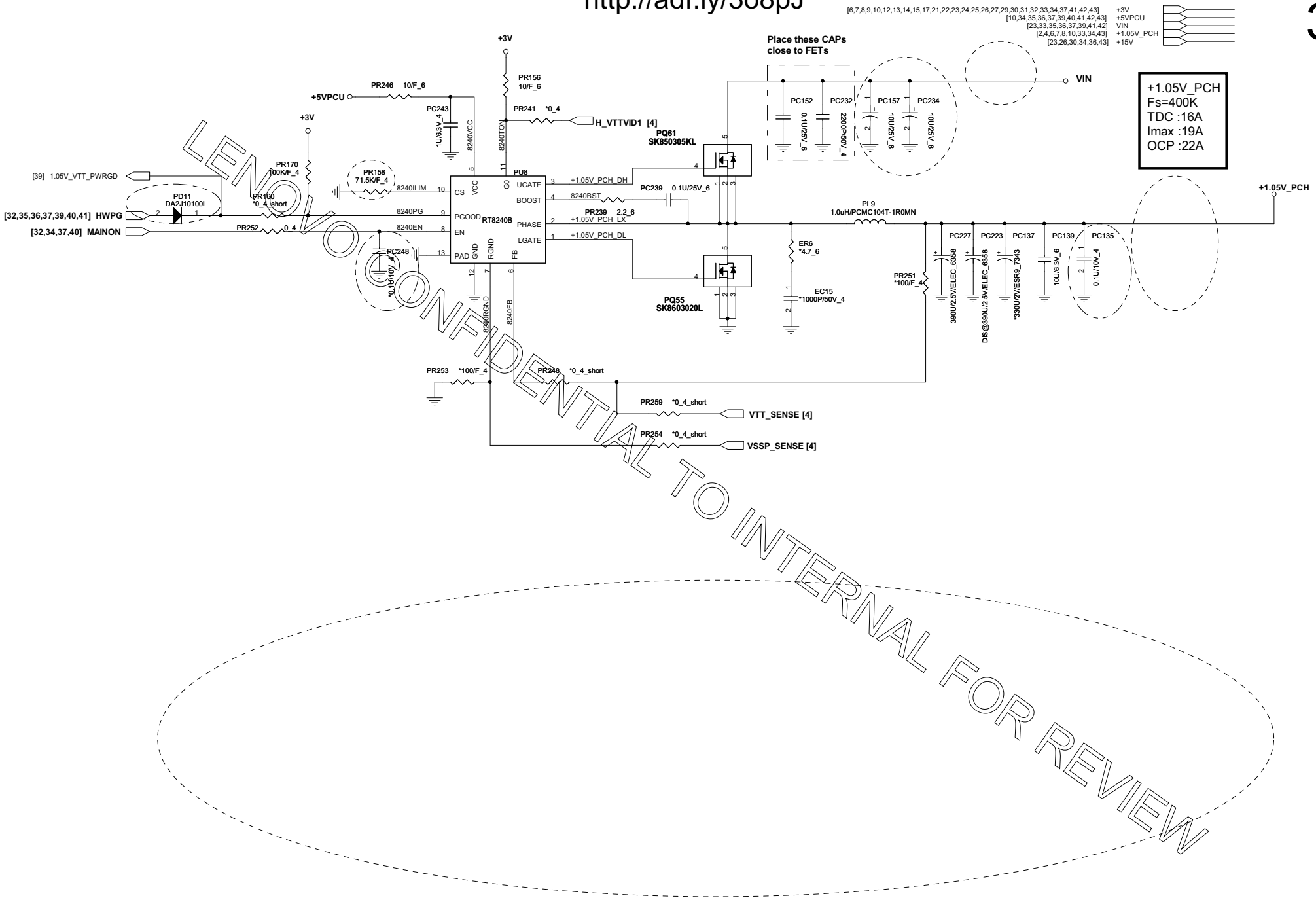
+1.5V_SUS
Fs=300K
TDC :16A
Imax :19A
OCP :22A

+1.5V_SUS

PC168 330U/2.5V/ELEC_6344
PC167 DS@330U/2.5V/ELEC_6344
PC148 *330U/2V/ESR9_7343
PC171 10U/6.3V_6
PC172 0.1U/10V_4

+5VPCU

PROJECT : LZ2A	
Quanta Computer Inc.	
Size	Document Number: DDR3/0.75V (TPS51216) — Rev
Date: Wednesday, November 30, 2011	Sheet 37 of 45

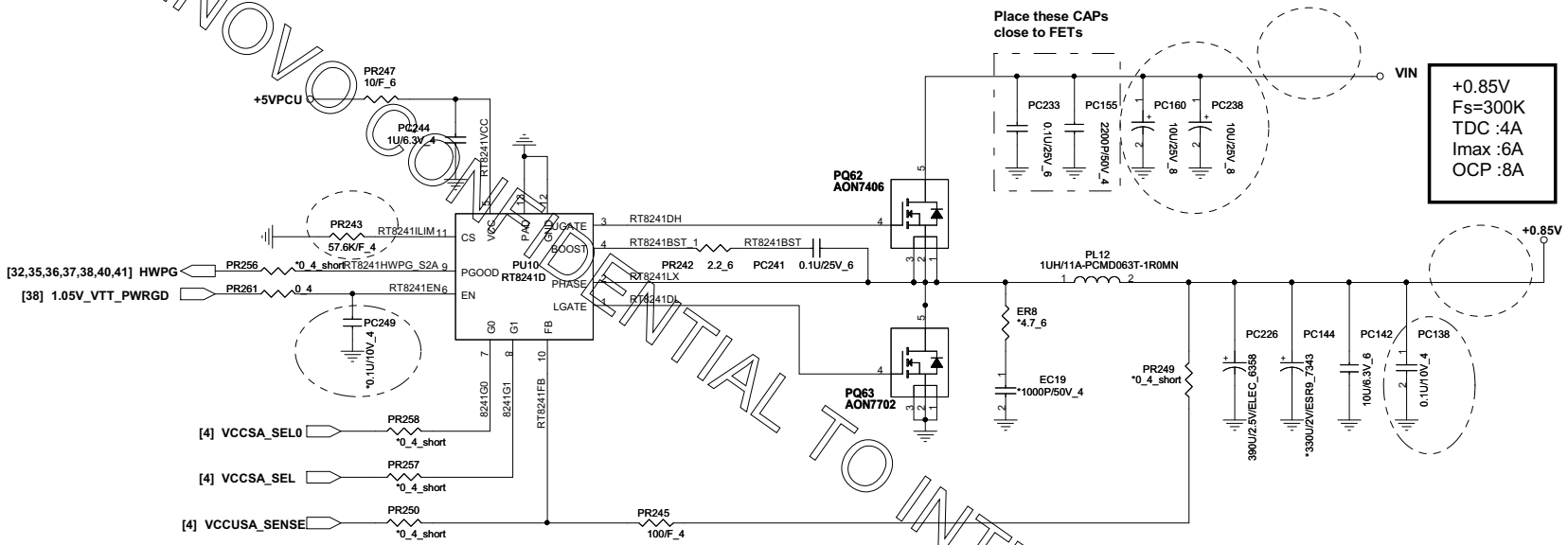


PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	+1.05V_PCH	

Date: Wednesday, November 30, 2011 Sheet 38 of 45

[10,34,35,36,37,38,40,41,42,43] +5VPCU
[23,33,35,36,37,38,41,42] VIN
[4,33,34] +0.85V



G0	G1	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

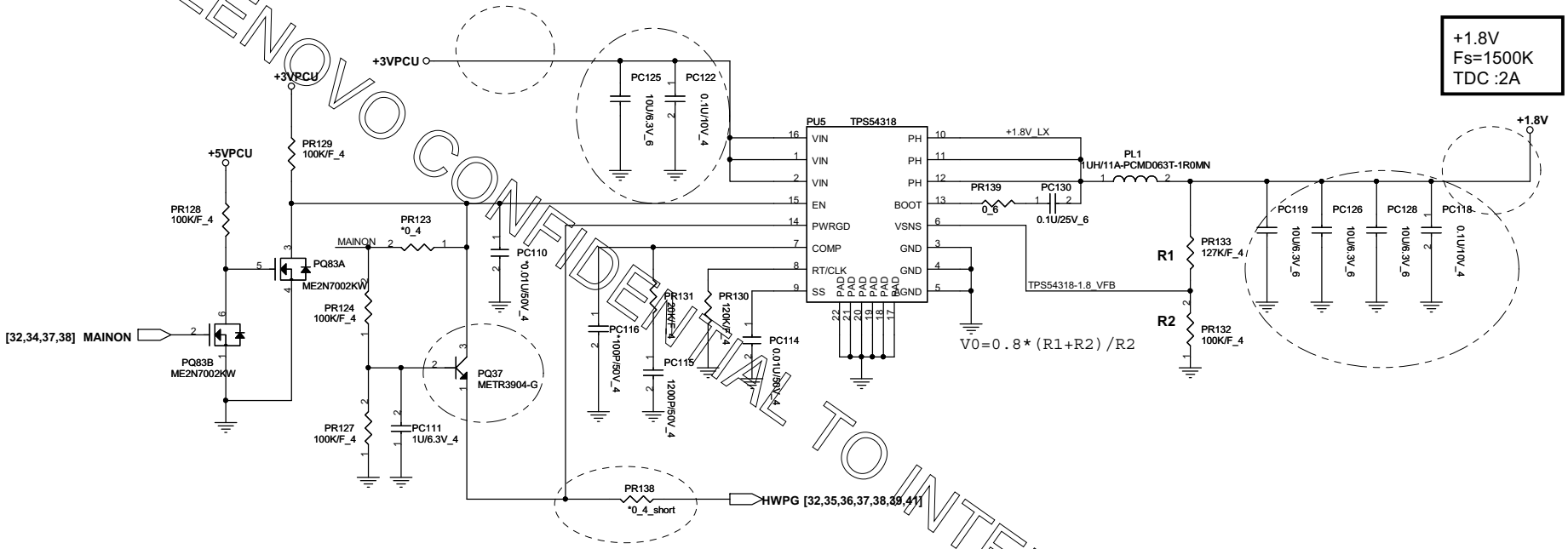
default 0.9V

PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	VCCSA (RT8241A)	

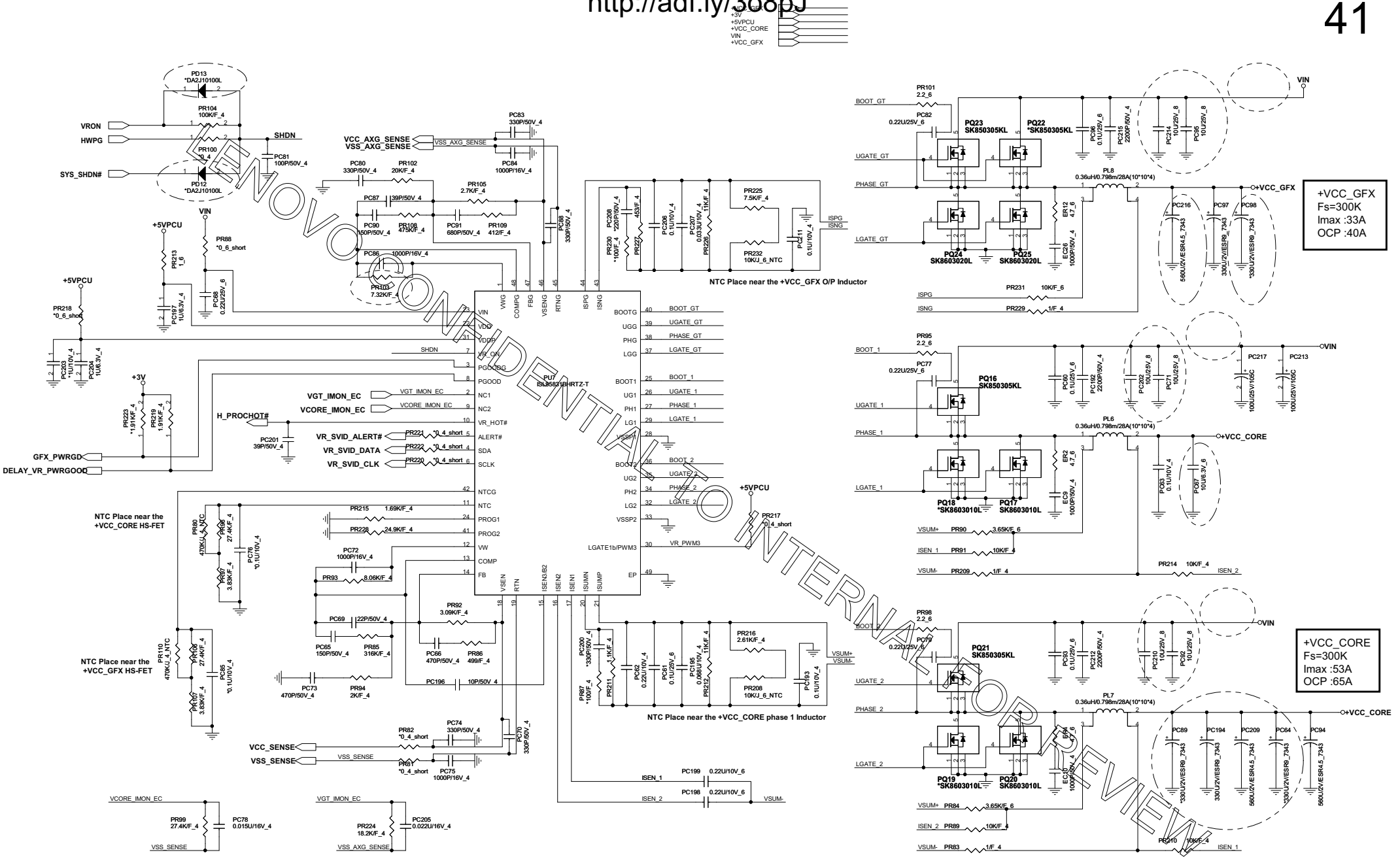
Date: Wednesday, November 30, 2011 Sheet 39 of 45

[10,34,35,36,37,38,39,41,42,43] +5VPCU
[6,7,23,24,26,27,31,32,34,35,36] +3VPCU
[4,7,10,33,34] +1.8V

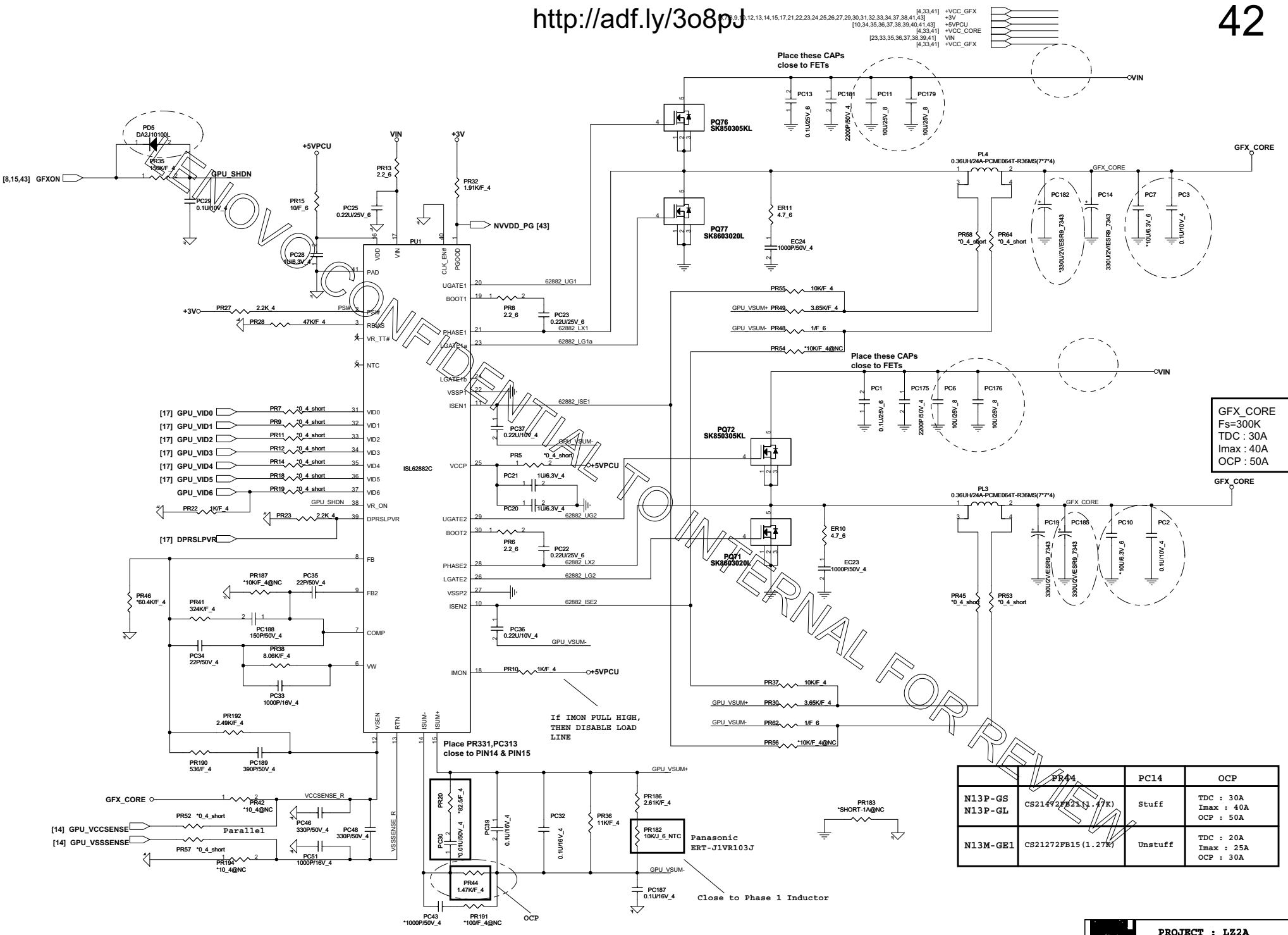


PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	1.8V (TPS54318)	
Date: Wednesday, November 30, 2011	Sheet 40 of 45	



PROJECT : LZ2A		
Quanta Computer Inc.		
Size	Document Number: CPU(ISL95831)IMVP2+1	Rev
Date: Wednesday, November 30, 2011	Sheet 41 of 45	



PROJECT : LZ2A
Quanta Computer Inc.
Size | Document Number: DGPU (ISL62882C) 2 Phase | Rev
Date: Wednesday, November 30, 2011 | Sheet 42 of 45

[5,7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42] +3V
[14,16,17,18] +3V_GPU
[10,34,35,36,37,38,39,40,41,42] +5VPCU
[14,15,19,20,33] +1.5V_GPU
[23,26,30,34,36] +15V
[2,4,10,12,13,33,34,37] +1.5V_SUS
[14,15,16,33] +1.05V_GFX_PCIE
[2,4,6,7,8,10,33,34,38] +1.05V_PCH

5.5A

+3V_GPU
+3V
R109 EV@10K/F_4
R141 EV@10K/F_4
GFXPG
GFXPG [9,14]
Q16 METR3904-G
+1.5V_GPU R120 EV@10K/F_4
*EV@1000P/50V_4@NC C147
Q18 METR3904-G
+1.05V_GFX_PCIE R107 EV@10K/F_4
*EV@1000P/50V_4@NC C139
Q17 METR3904-G

+1.5V_GPU
+15V
PR79 DIS@22_8
PR77 DIS@1M_4
+5VPCU
PQ85A
ME2N7002KW
PR78 DIS@100K/F_4
PQ85B
ME2N7002KW
[15] +1.5V_GPU_EN
R688 100K_4
PQ14 DIS@ME2N7002E

+1.5V_SUS
PQ40 DIS@SK8603020L
+1.5V_GPU
PC112 DIS@10U/6.3V_6
PC117 DIS@10U/6.3V_6
PC107 DIS@10U/6.3V_6
PC106 DIS@10U/6.3V_6
PC101 *330U/2.5V/9m_3528
PC102 *0.1U/10V_4
PC100 DIS@0.022U/25V/X7R_4

1.4A

+3V_GPU
+15V
+3V
PQ15 DIS@AO6402A
+3V_GPU
+3V_GPU [14,16,17,18]
PR113 DIS@22_8
PR125 DIS@1M_4
PC59 DIS@10U/6.3V_6
PC57 DIS@10U/6.3V_6
PC58 *0.1U/10V_4
PQ28 DIS@ME2N7002E
+5VPCU
PR118 DIS@100K/F_4
PQ84A 2N7002DW
PC56 *2200P/50V_4
[8,15,42] GFXON
GFXON
PQ84B 2N7002DW
+3V_NVMISC_EN [17,18]

+1.05V_GFX_PCIE
+15V
PR116 DIS@22_8
PR265 DIS@1M_4
+5VPCU
PQ32 DIS@ME2N7002E
PR266 DIS@100K/F_4
PQ86A
ME2N7002KW
[42] NVVDD_PG
NVVDD_PG
PQ86B
ME2N7002KW
PC109 *0.022U/25V_4

+1.05V_PCH
PQ41 DIS@AON7406
3.9A
+1.05V_GFX_PCIE
PC121 DIS@10U/6.3V_6
PC127 DIS@10U/6.3V_6
PC104 DIS@10U/6.3V_6
PC105 DIS@10U/6.3V_6
PC108 *330U/2.5V/9m_3528
PC113 DIS@0.1U/10V_4

PROJECT : LZ2A
Quanta Computer Inc.
Size: Document Number: GPU Rev:
Date: Wednesday, November 30, 2011 Sheet 43 of 45