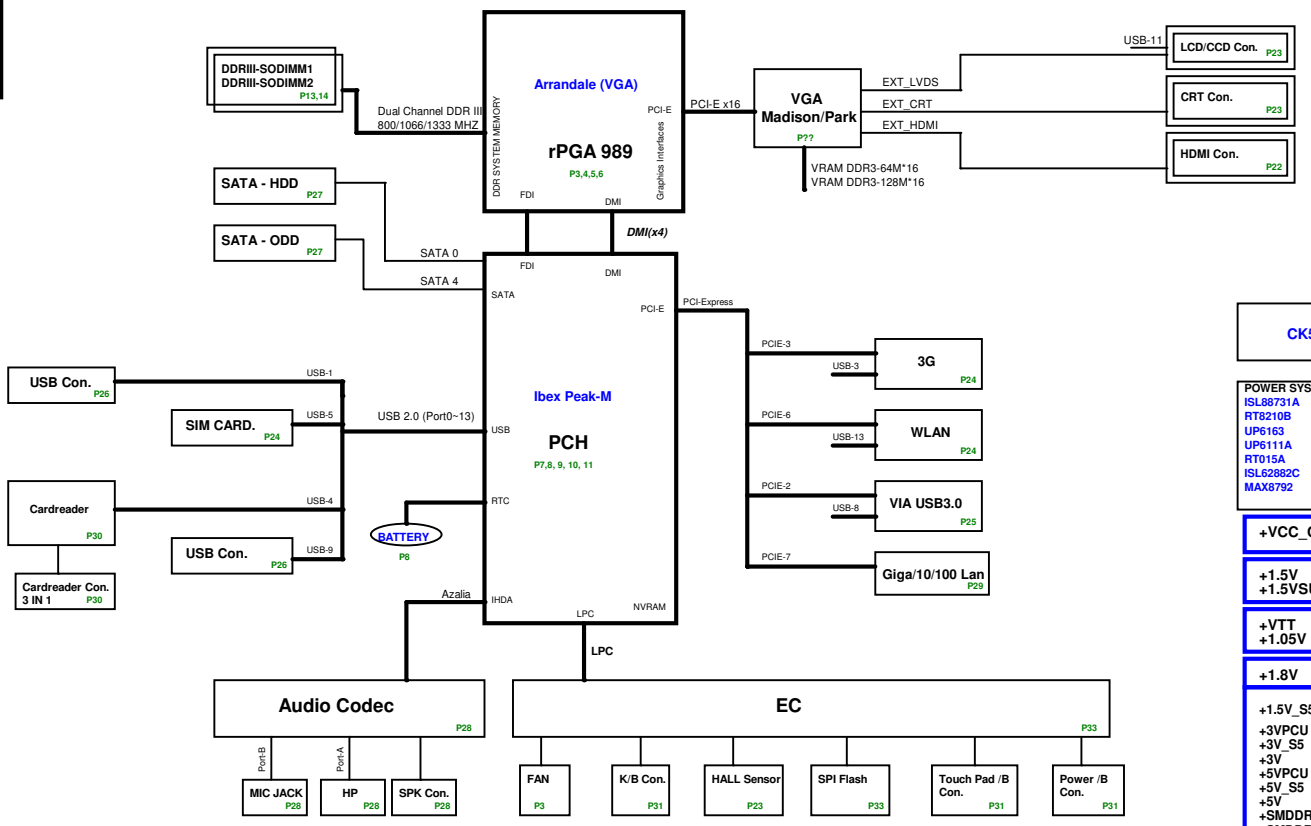
BU5D Block Diagram

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND1
- LAYER 3 : IN1
- LAYER 4 : VCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : GND2
- LAYER 8 : BOT



CK505 P2

POWER SYSTEM

ISL88731A	P33
RT8210B	P34
UP6163	P35
UP6111A	P36
RT015A	P37
ISL62882C	P38
MAX8792	P40

+VCC_CORE

+1.5V
+1.5VSUS

+VTT
+1.05V

+1.8V

+1.5V_S5

+3VPCU
+3V_S5
+3V
+5VPCU
+5V_S5
+5V
+SMDDR_VTERM
+SMDDR_VREF

Quanta Computer Inc.
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Table of Contents

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
+VCCRTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
+5V_TMA	+5V	MAIN_ON	S0
WIMAX_P	+3.3V	WMAX_P for EC	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_S5	+1.5V	S5_ON	S0~S5
+1.5V_SUS	+1.5V	SUSON	S0~S3
+VCC_CORE		VRON	S0
+VTT	+1.05V~+1.1V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		GFXVR_EN	S0

GND PLANE	PAGE
GND_SIGNAL	32
CARD_GND	21
AGND_DC/DC	31
GND	ALL

ITEM	Value Code	FUNCTIONS
1	EV@	DISCRETE
2	IV@	UMA
3	U3@	USB 3.0
4	U2@	USB 2.0 (colay W USB 3.0)
5	HM@	HDMI
6	NHM@	No HDMI
7	EHM@	External HDMI
8	3G@	3G
9	C@	Cost issue
10	MDC@	Modem
11	S3@	S3 Power Reduction
12	NS3@	No S3 Power Reduction
13	NGS@	No G-SENSOR
14	51@	1G LAN
15	52@	10/100 LAN
16	GS@	G-SENSOR
17	NMDC@	No Modem

Quanta Computer Inc.

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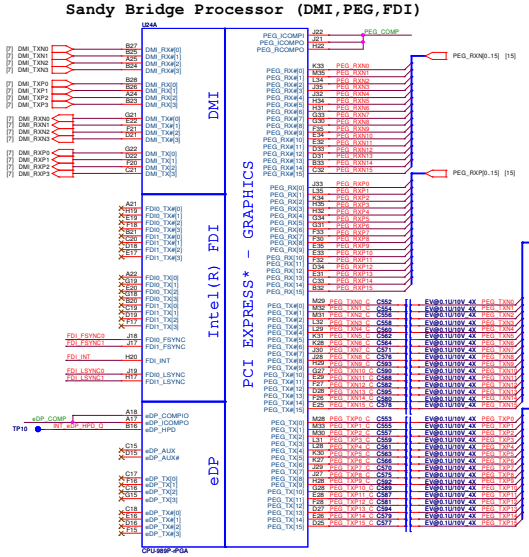
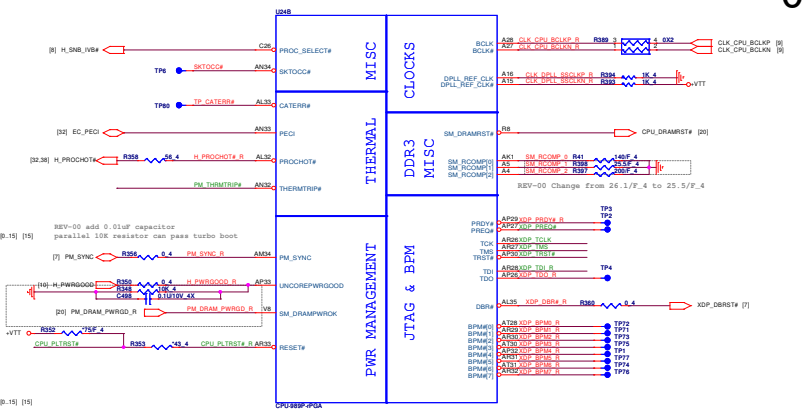
<CPU/VGA>

Sandy Bridge Processor (DMI,PEG,FDI)



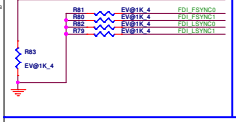
Sandy Bridge Processor (CLK,MISC,JTAG)



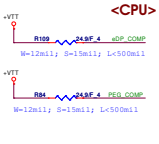
REV-00 add 0.01uF capacitor
parallel 10K resistor can pass turbo boot

REV-00 Change from 26.1/F_4 to 25.5/F_4

FDI Disabling (Discrete Only) <VGA>

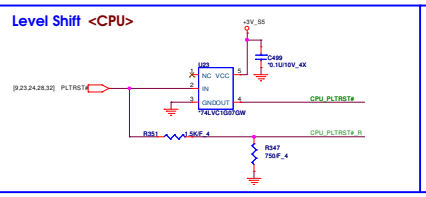


DP & PEG Compensation <CPU>

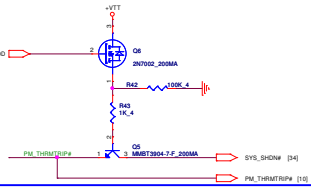


Processor pull-up <CPU>

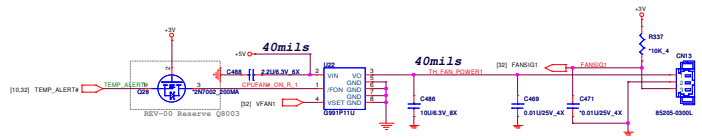
Level Shift <CPU>



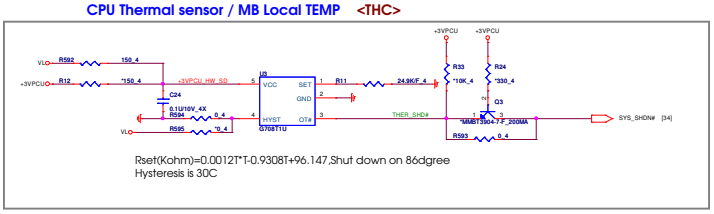
Thermal Trip<CPU>



FAN Control-->For one FAN solution <THC>



CPU Thermal sensor / MB Local TEMP <THC>



Rset(Kohm)=0.0012T^2-0.9308T+96.147,Shut down on 86dgree
Hysteresis is 30C

REV-C3A Change VCC PIN5 of U3 from +3VPCU to VL
Add R592,R594,R593
Reverse R12,R595,R33,R24,Q3

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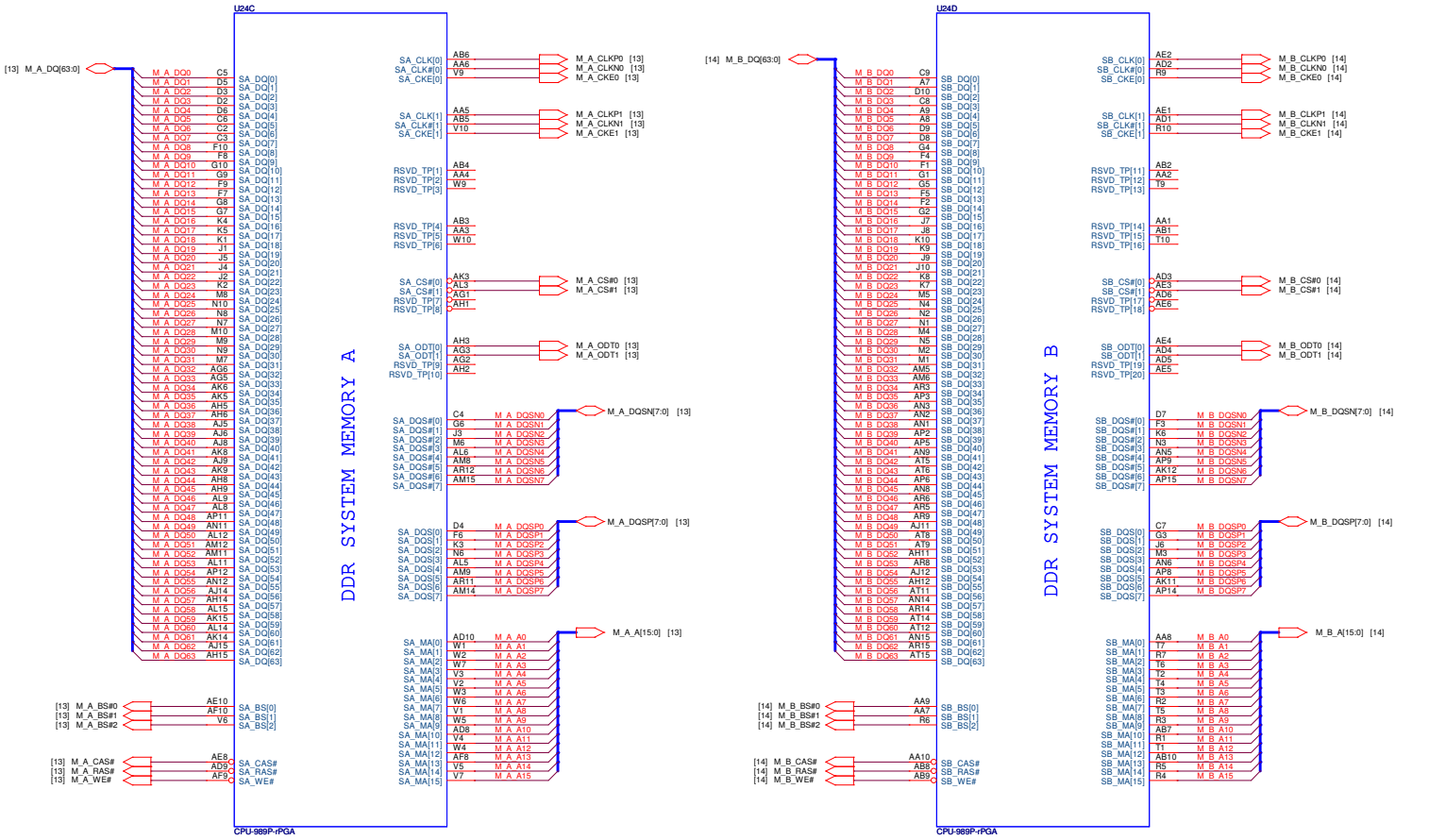
Sandy Bridge Processor (DDR3)



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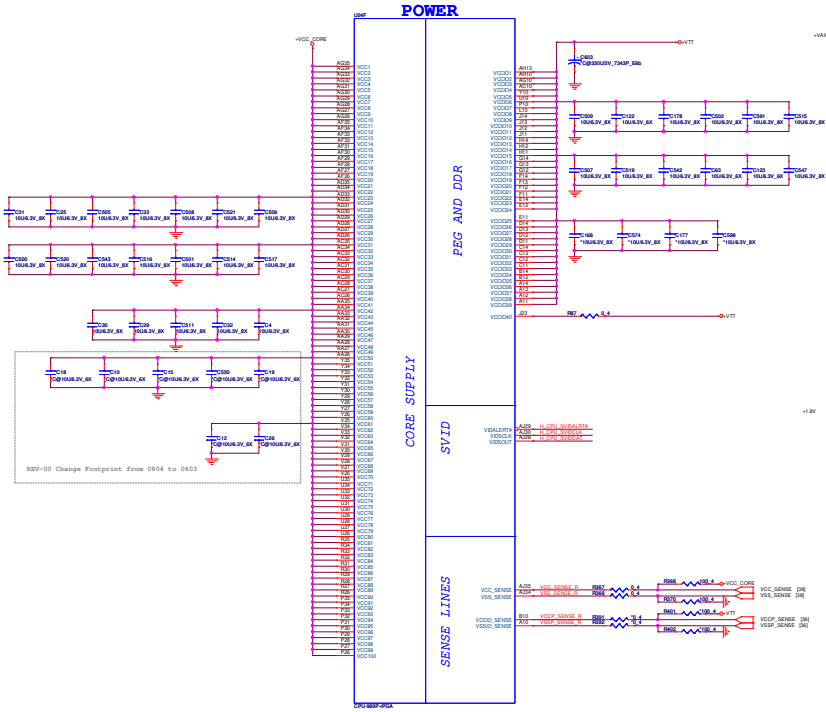
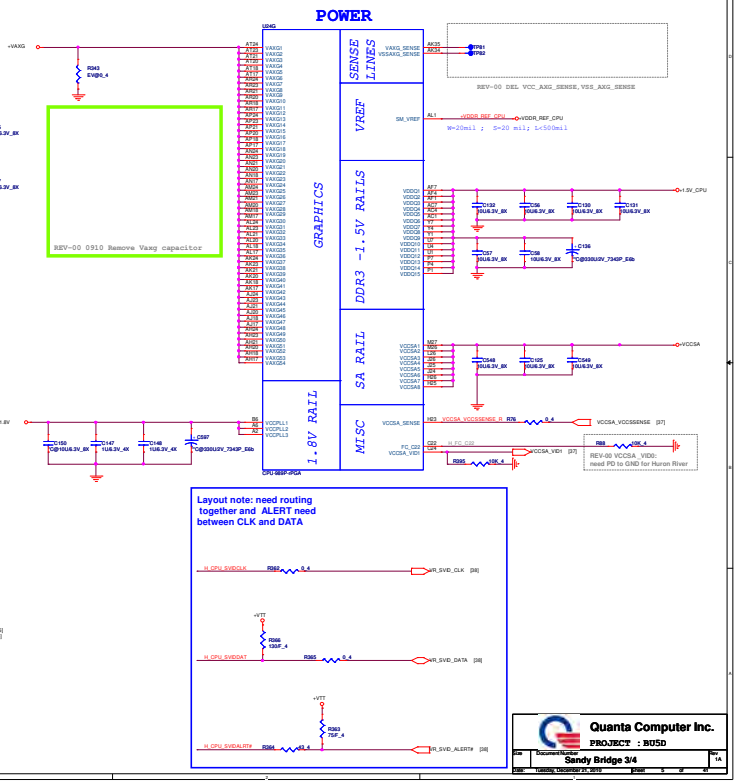
Sandy Bridge Processor (POWER)



Sandy Bridge Processor (GRAPHIC POWER)



Layout note: need routing together and ALERT need between CLK and DATA

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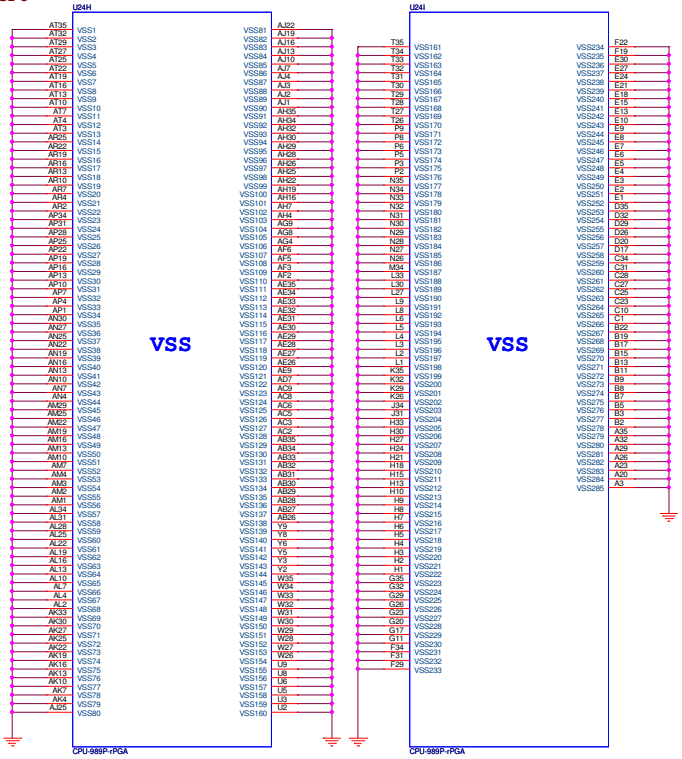
Sandy Bridge 3/4

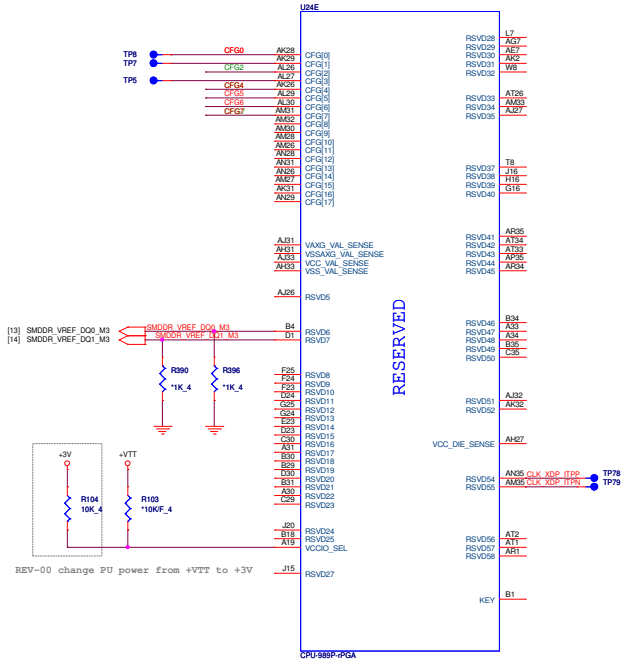
Rev 1A

<CPU>

Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)



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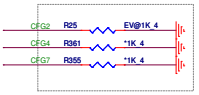
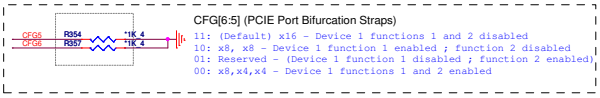
Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



REV-00 change to 5% tolerance



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<CLG>

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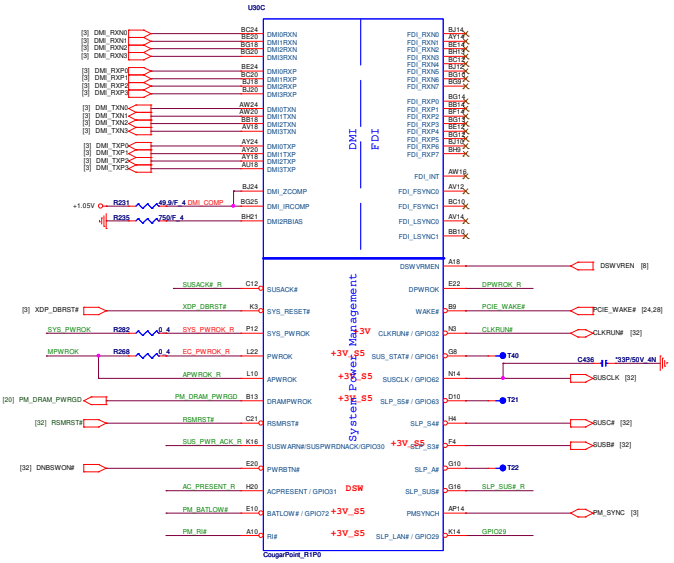
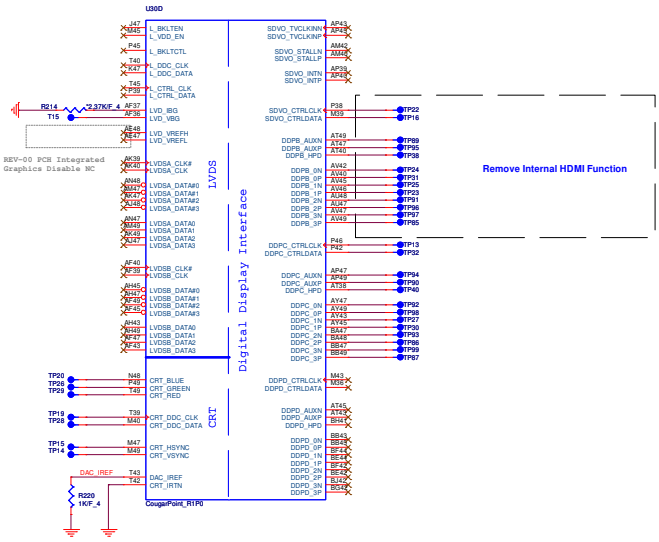
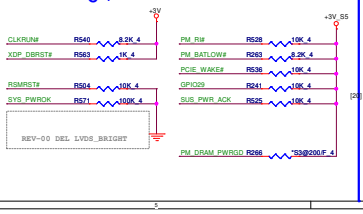
Cougar Point (DMI,FDI,PM)



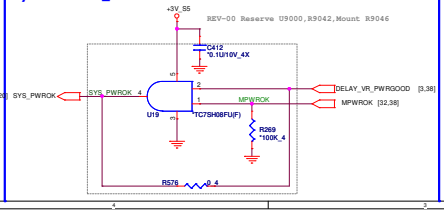
Cougar Point (LVDS,DDI)



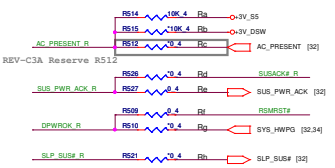
PCH Pull-high/low <CLG>



System PWR_OK <CLG>



Deep Sx <CLG>



Net Name	Deep Sx Support	Deep Sx No Support
AC_PRESENT	Rb,Rc stuff	Ra stuff
SUS_PWR_ACK	Rd stuff	Re stuff
DPWROK	Rg stuff	Rf stuff
SLP_SUS	Rh stuff	Rh No stuff

Quanta Computer Inc.

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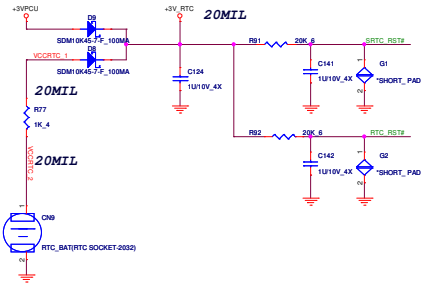
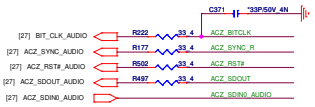
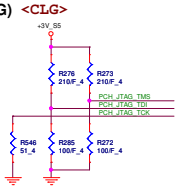
RTC Circuitry(RTC) <RTC>



HDA Bus(CLG) <ADO>

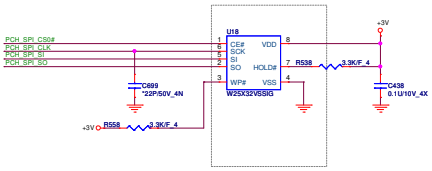


PCH JTAG Debug (CLG) <CLG>



PCH Dual SPI (CLG) <CLG>

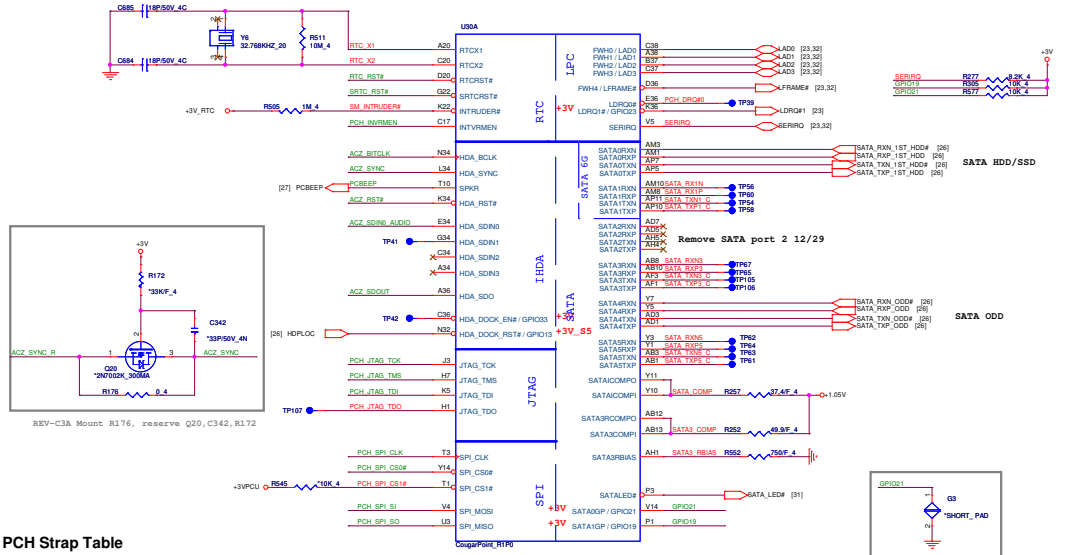
MX25L3205DM2I-12G: AKE39FP0Z00
W25X32VSSIG: AKE39ZP0N00



REV-00 change footprint
from socket type to W25X32VSSIG

PCH2 (CLG) <CLG> <ADO>

Cougar Point (HDA,JTAG,SATA)



REV-C3A Mount R176, reserve Q20,C342,R172

REV-B2A Add G3 for Clear CMOS password

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R281 *1K_4 PCBEEP
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R483 *1K_4 PCI_GNT3# [9]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R513 330K_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GPIO19 / Boot Location: 1 1 SPI *; 0 0 LPC	R479 *1K_4 GNT1# [9] R560 *1K_4 GPIO19
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	+3V R498 *1K_4 ACZ_SDOUT ACZ_SDOUT [32]
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R543 2.2K_4 R544 2.7K_4 1.8V DF_TVS [10] H_SNB_IVB# [3]
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	+3VPCU R265 *10K_4 R271 *1K_4 PLL_ODVR_EN [10]
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5 R179 1K_4 ACZ_SYNC
GPIO15	TLS Confidentiality	RSMRST	0 = Default. TLS no Confidentiality 1 = TLS Confidentiality	+3V_S5 R542 1K_4 GPIO15 [10]
DSWVRMEN	Deep S4/S5 Well On -Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable	DSWVRMEN [7] +3V_RTC R518 330K_4 R517 *330K_4
INIT3_3V#	Reserved	PWROK	1 = Default (weak pull-up 20K)	Should not pull low. leave as No Connect
GNT2#/ GPIO53	ESI Strap (Server Only)	PWROK	1 = Default. Should not be pulled low for desktop and mobile	Should not pull low for desktop and mobile
L_DDC_DATA	LVDS Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V
SDVO_CTRLDATA	Port B Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V
DDPC_CTRLDATA	Port C Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC
DDPD_CTRLDATA	Port D Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC
SATA3GP/ GPIO37	Reserved	PWROK	0 = Default	Should not be pulled high when strap is sampled
SATA2GP/ GPIO36	Reserved	PWROK	0 = Default	Should not be pulled high when strap is sampled

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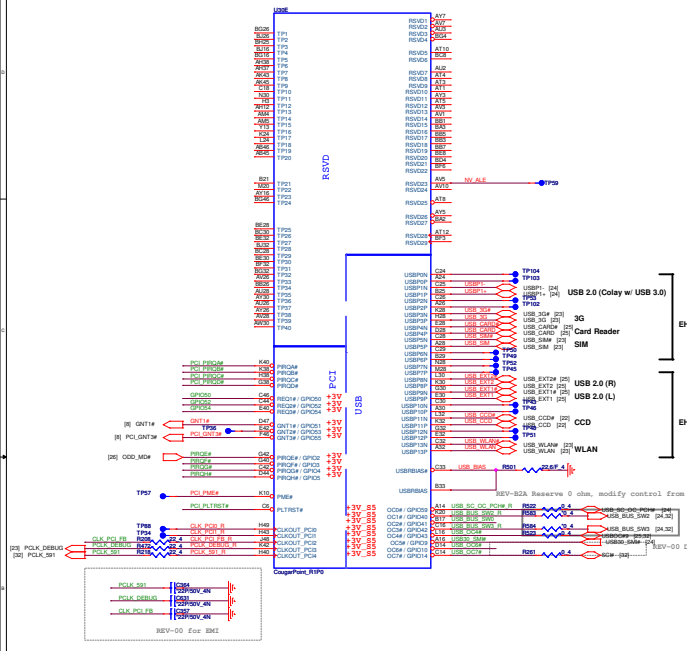
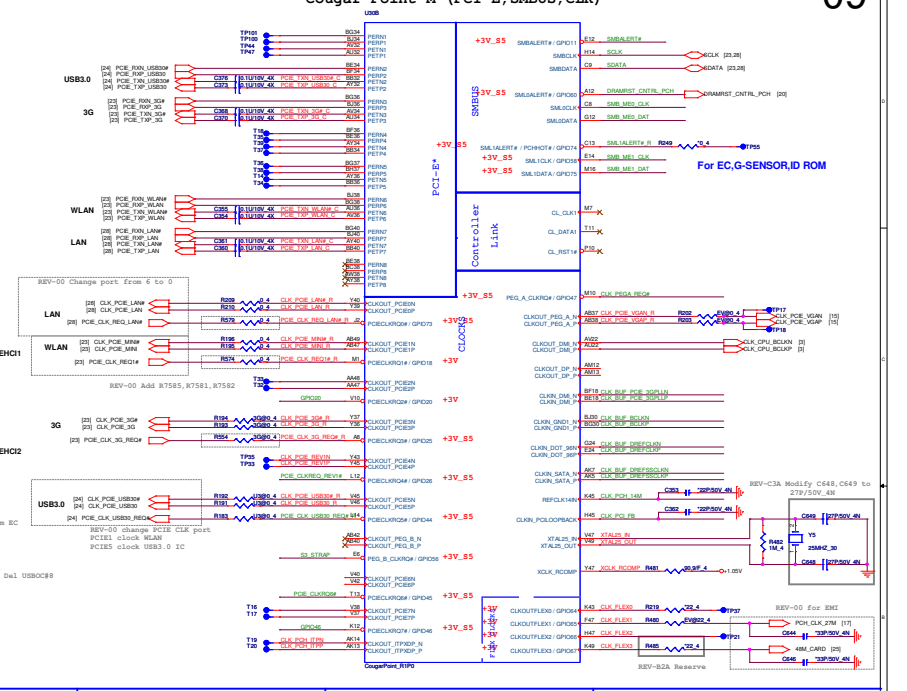
<CLG> <U3B> <MNT> <MNW> <LAN> <MMC> <VGA>

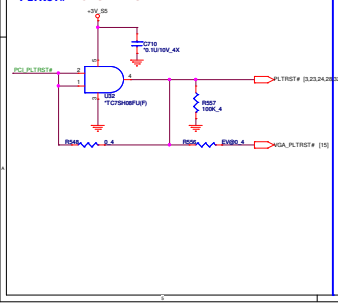
Cougar Point-M (PCI,USB,NVRAM)



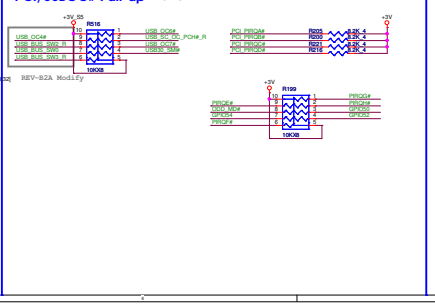
Cougar Point-M (PCI-E,SMBUS,CLK)



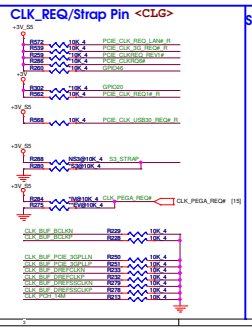
PLTRST# <CLG> <VGA>



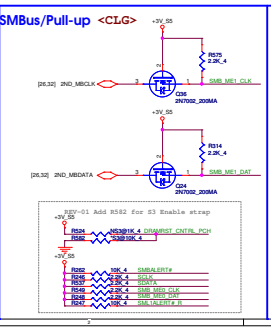
PCI/USBOC# Pull-up <CLG>



CLK_REQ/Strap Pin <CLG>



SMBus/Pull-up <CLG>



	33MHz	27MHz	48/24MHz	14.318MHz	25MHz
CLK_FLEX0	●	●	●	●	
CLK_FLEX1		●	●	●	
CLK_FLEX2	●	●	●	●	●
CLK_FLEX3		●	●	●	

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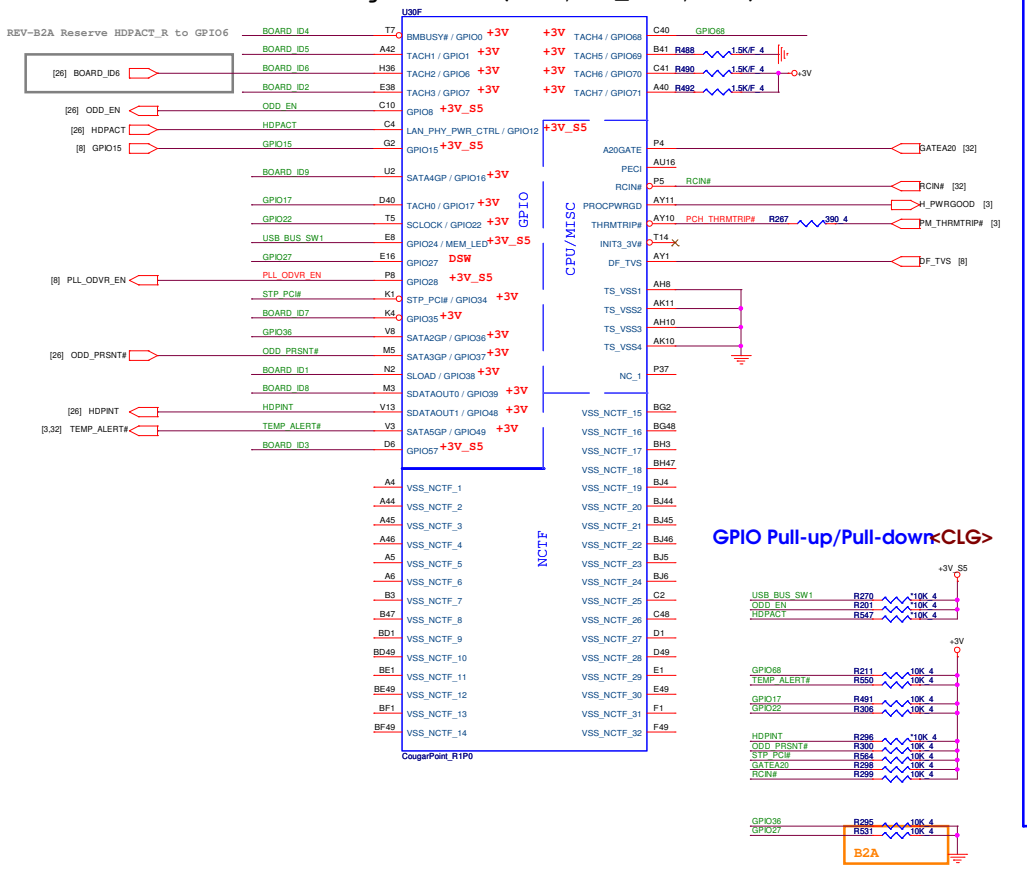
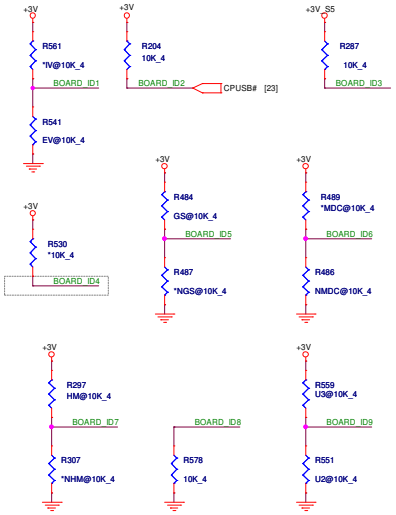
Cougar Point (GPIO,VSS_NCTF,RSVD)



GPIO Pull-up/Pull-down<CLG>

BOARD ID SETTING

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID9
UMA SKU VGA SKU	H L								
W/O 3G W/ 3G		H L							
W/O LED_KB W/ LED_KB			H L						
14" 15"				H L					
W G-SNR W/O G-SNR					H L				
W/ MDC W/O MDC						H L			
W/ HDMI W/O HDMI							H L		
NC 13"								H L	
W/ USB3.0 W/O USB3.0									H L



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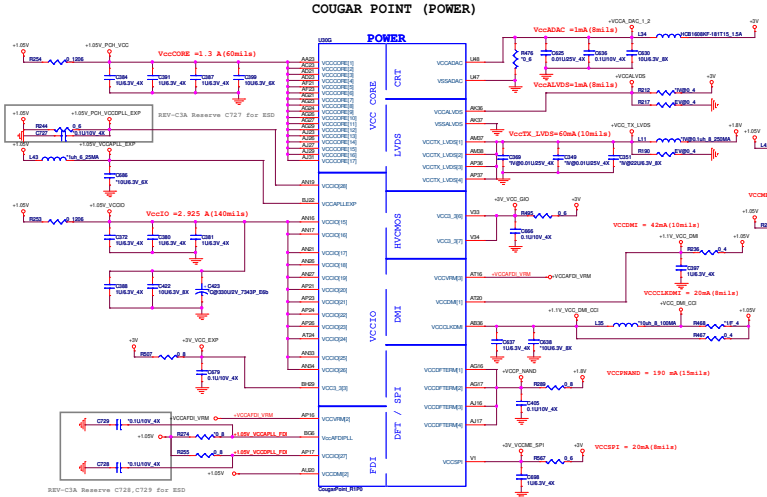
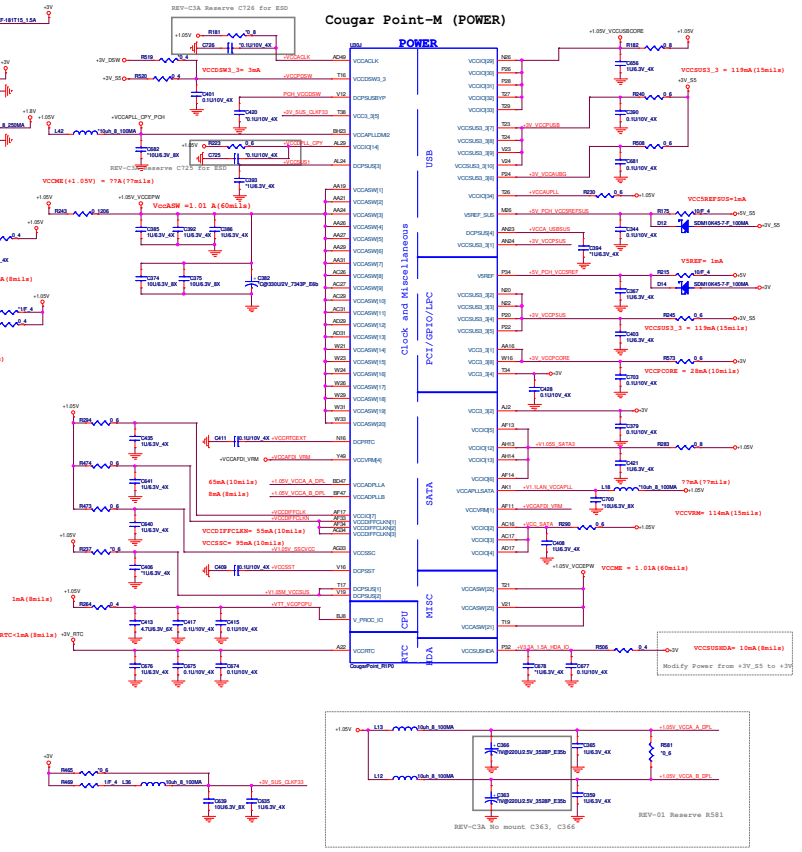
COUGAR POINT (POWER)

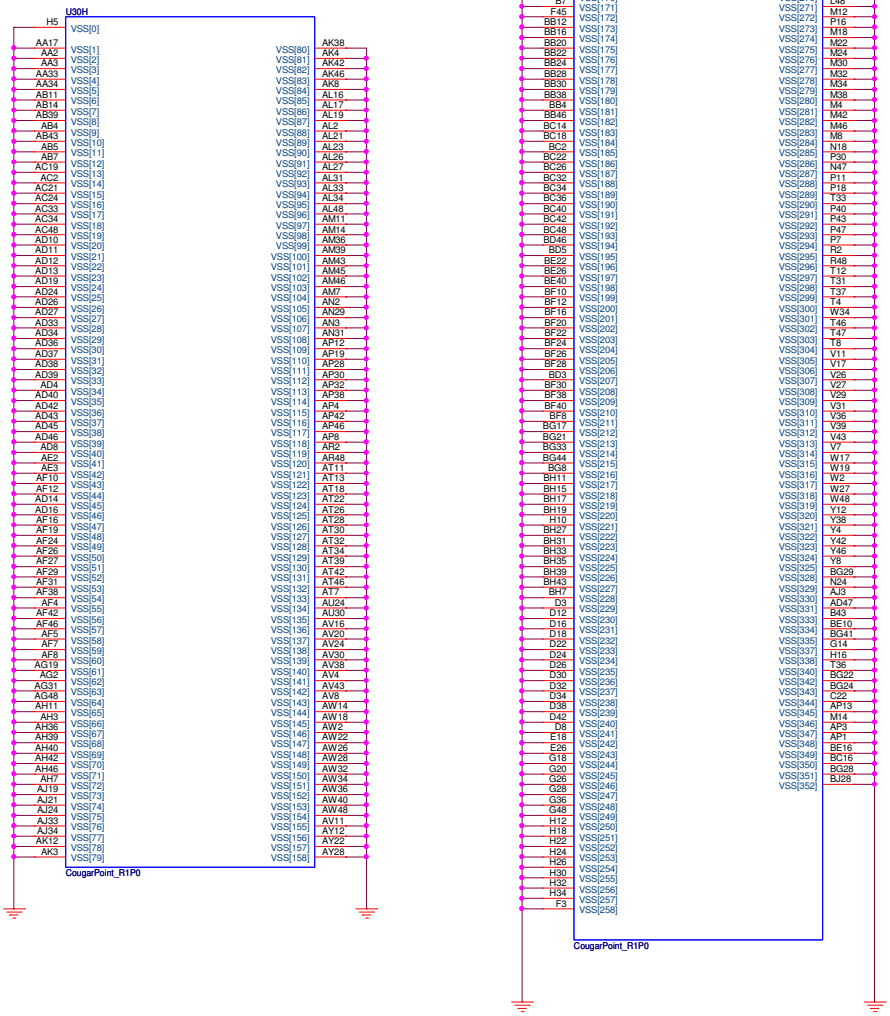


Cougar Point-M (POWER)

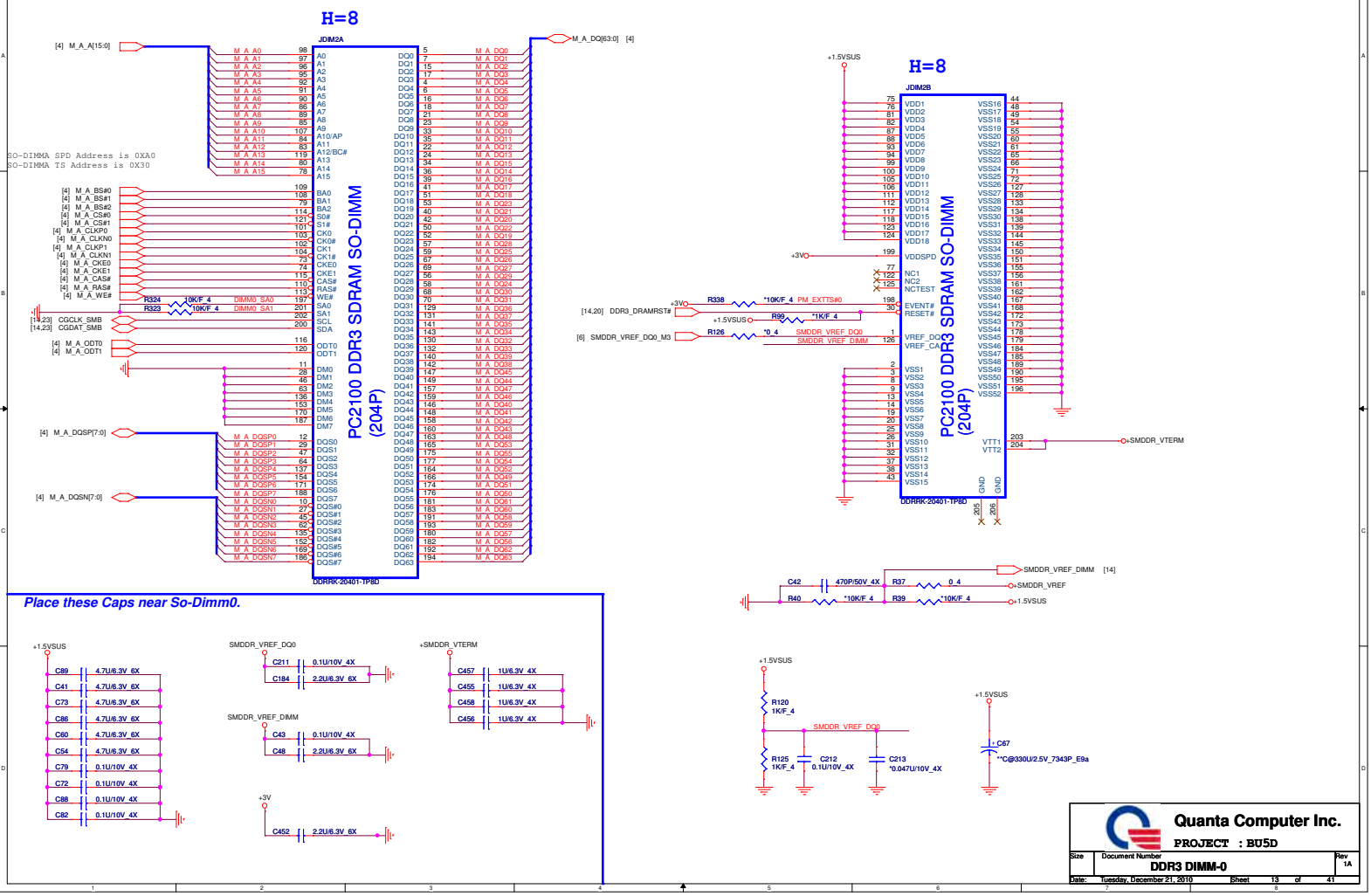


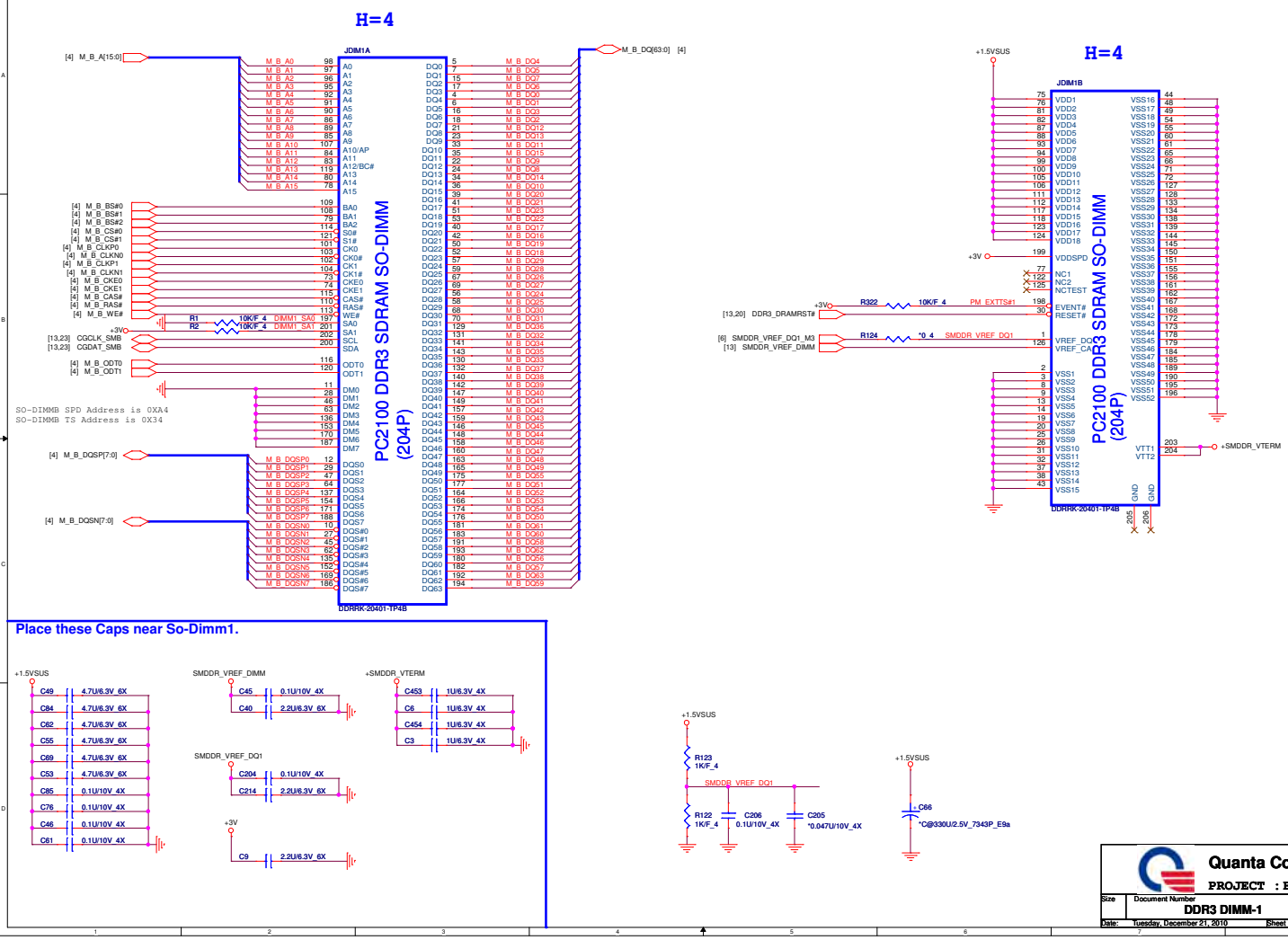
Quanta Computer Inc.	
PROJECT : BU5D	
Size:	Document Number: Cougar Point 5/6
Date: Tuesday, December 21, 2010	Sheet 11 of 41

IBEX PEAK-M (GND)



Quanta Computer Inc.		
PROJECT : BU5D		
Size	Document Number: Cougar Point 6/6	Rev: 1A
Date: Tuesday, December 21, 2010	Sheet 12 of 41	

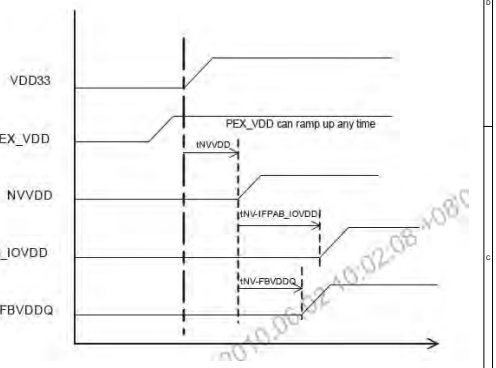

H=8
JDIM2A
PC2100 DDR3 SDRAM SO-DIMM
(204P)
DDRRK-20401-TP8D
SO-DIMMA SPD Address is 0XA0
SO-DIMMA TS Address is 0X30
H=8
JDIM2B
PC2100 DDR3 SDRAM SO-DIMM
(204P)
DDRRK-20401-TP8D
Place these Caps near So-Dimm0.
Quanta Computer Inc.
PROJECT : BU5D
DDR3 DIMM-0
Tuesday, December 21, 2010



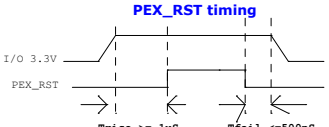
Place these Caps near So-Dimm1.

Quanta Computer Inc.		
PROJECT : BU5D		
Size	Document Number	Rev 1A
	DDR3 DIMM-1	
Date: Tuesday, December 21, 2010	Sheet 14 of 41	

power up sequence



PEX_RST timing



~ 500mA

1600mA

18.19A

120mA

120mA

12~16 mils

REV-00 Modify to test point

REV-00 Angelo 0928 Modified

Modify

Add

Del

+1.05V for N12M-GE/NS GPU

Quanta Computer Inc.	
PROJECT : BU5D	
Size:	Document Number: N12M-GE (PCIE I/F) Rev: 1A
Date: Tuesday, December 21, 2010	Sheet 15 of 41

2.16A

+1.5V_GFX

U27B

PBGA533-NVIDIA-GEFORCE6250

COMMON

2/13 FRAME_BUFFER

C257 0.047U/25V 4X
C265 0.047U/25V 4X
C235 0.047U/25V 4X
C248 0.01U/25V 4X
C241 0.01U/25V 4X
C232 0.01U/25V 4X
C231 4.7U/6.3V 6
C525 4.7U/6.3V 6

FBVDDQ_01 A13
FBVDDQ_02 B13
FBVDDQ_03 C13
FBVDDQ_04 D13
FBVDDQ_05 D14
FBVDDQ_06 E13
FBVDDQ_07 F13
FBVDDQ_08 F14
FBVDDQ_09 F15
FBVDDQ_10 F16
FBVDDQ_11 F17
FBVDDQ_12 F19
FBVDDQ_13 F22
FBVDDQ_14 H23
FBVDDQ_15 H26
FBVDDQ_16 J15
FBVDDQ_17 J16
FBVDDQ_18 J18
FBVDDQ_19 J19
FBVDDQ_20 L19
FBVDDQ_21 L23
FBVDDQ_22 L26
FBVDDQ_23 M19
FBVDDQ_24 N22
FBVDDQ_25 U22
FBVDDQ_26 Y22

FBA_D0 D22 VMA_DQ0
FBA_D1 E24 VMA_DQ1
FBA_D2 E22 VMA_DQ2
FBA_D3 D24 VMA_DQ3
FBA_D4 D26 VMA_DQ4
(FBA_D4)FBA_D7 D27 VMA_DQ5
FBA_D5 C27 VMA_DQ6
FBA_D6 B27 VMA_DQ7
(FBA_D7)FBA_D4 A21 VMA_DQ8
FBA_D7 B21 VMA_DQ9
FBA_D8 C21 VMA_DQ10
FBA_D9 C19 VMA_DQ11
FBA_D10 C18 VMA_DQ12
FBA_D11 D18 VMA_DQ13
FBA_D12 B18 VMA_DQ14
FBA_D13 C16 VMA_DQ15
FBA_D14 E21 VMA_DQ16
FBA_D15 F21 VMA_DQ17
FBA_D16 D20 VMA_DQ18
FBA_D17 F20 VMA_DQ19
FBA_D18 D17 VMA_DQ20
FBA_D19 F18 VMA_DQ21
FBA_D20 D16 VMA_DQ22
FBA_D21 E16 VMA_DQ23
FBA_D22 A22 VMA_DQ24
FBA_D23 C24 VMA_DQ25
FBA_D24 D21 VMA_DQ26
FBA_D25 B22 VMA_DQ27
FBA_D26 C22 VMA_DQ28
FBA_D27 A25 VMA_DQ29
FBA_D28 B25 VMA_DQ30
FBA_D29 A26 VMA_DQ31
FBA_D30 U24 VMA_DQ32
FBA_D31 V24 VMA_DQ33
FBA_D32 V23 VMA_DQ34
FBA_D33 R24 VMA_DQ35
FBA_D34 T23 VMA_DQ36
FBA_D35 R23 VMA_DQ37
FBA_D36 P24 VMA_DQ38
FBA_D37 P22 VMA_DQ39
FBA_D38 AC24 VMA_DQ40
FBA_D39 AB23 VMA_DQ41
FBA_D40 AB24 VMA_DQ42
FBA_D41 W24 VMA_DQ43
FBA_D42 AA22 VMA_DQ44
FBA_D43 W23 VMA_DQ45
FBA_D44 W22 VMA_DQ46
FBA_D45 V22 VMA_DQ47
FBA_D46 AA25 VMA_DQ48
FBA_D47 W27 VMA_DQ49
FBA_D48 W26 VMA_DQ50
FBA_D49 W25 VMA_DQ51
FBA_D50 AB25 VMA_DQ52
FBA_D51 AB26 VMA_DQ53
FBA_D52 AD38 VMA_DQ54
FBA_D53 AD27 VMA_DQ55
FBA_D54 V25 VMA_DQ56
FBA_D55 R25 VMA_DQ57
FBA_D56 V26 VMA_DQ58
FBA_D57 V27 VMA_DQ59
FBA_D58 R26 VMA_DQ60
FBA_D59 T25 VMA_DQ61
FBA_D60 N25 VMA_DQ62
FBA_D61 N26 VMA_DQ63
FBA_D62
FBA_D63

REV-00 Change ball name and net for GB1b.

REV-00 Change ball name and net for GB1b.

[19] FBA_CMD0 G24 (FBA_CMD25)FBA_CMD0
[19] FBA_CMD1 F27 (FBA_CMD23)FBA_CMD1
[19] FBA_CMD2 F25 FBA_CMD2
[19] FBA_CMD3 F26 (FBA_CMD9)FBA_CMD3
[19] FBA_CMD4 G26 (FBA_CMD10)FBA_CMD4
[19] FBA_CMD5 G27 (FBA_CMD26)FBA_CMD5
[19] FBA_CMD6 G25 (FBA_CMD14)FBA_CMD6
[19] FBA_CMD7 J25 FBA_CMD7
[19] FBA_CMD8 J24 (FBA_CMD1)FBA_CMD8
[19] FBA_CMD9 H24 (FBA_CMD22)FBA_CMD9
[19] FBA_CMD10 H22 (FBA_CMD20)FBA_CMD10
[19] FBA_CMD11 J26 (FBA_CMD24)FBA_CMD11
[19] FBA_CMD12 G22 (FBA_CMD18)FBA_CMD12
[19] FBA_CMD13 G23 (FBA_CMD9)FBA_CMD13
[19] FBA_CMD14 J22 (FBA_CMD29)FBA_CMD14
[19] FBA_CMD15 J27 (FBA_CMD6)FBA_CMD15
[19] FBA_CMD16 M24 (FBA_CMD27)FBA_CMD16
L24 (FBA_CMD15)FBA_CMD17
[19] FBA_CMD18 J23 (FBA_CMD11)FBA_CMD18
[19] FBA_CMD19 K23 (FBA_CMD16)FBA_CMD19
[19] FBA_CMD20 K22 (FBA_CMD28)FBA_CMD20
[19] FBA_CMD21 M23 (FBA_CMD3)FBA_CMD21
[19] FBA_CMD22 K24 (FBA_CMD17)FBA_CMD22
[19] FBA_CMD23 M27 (FBA_CMD6)FBA_CMD23
[19] FBA_CMD24 N27 (FBA_CMD4)FBA_CMD24
[19] FBA_CMD25 M26 (FBA_CMD21)FBA_CMD25
[19] FBA_CMD26 K26 (FBA_CMD6)FBA_CMD26
[19] FBA_CMD27 K27 (FBA_CMD13)FBA_CMD27
[19] FBA_CMD28 K25 (FBA_CMD19)FBA_CMD28
[19] FBA_CMD29 M25 (FBA_CMD12)FBA_CMD29
[19] FBA_CMD30 L22 FBA_CMD30

TP83 FBA_CMD1
TP1 FBA_CMD17

[19] VMA_CLK0 F24 VMA_CLK0
[19] VMA_CLK0# F23 VMA_CLK0#
[19] VMA_CLK1 N24 VMA_CLK1
[19] VMA_CLK1# N23 VMA_CLK1#

FBA_CLK0
FBA_CLK0*
FBA_CLK1
FBA_CLK1*

FBA_DQM0 C26 VMA_DM0
FBA_DQM1 B19 VMA_DM1
FBA_DQM2 D19 VMA_DM2
FBA_DQM3 D23 VMA_DM3
FBA_DQM4 T24 VMA_DM4
FBA_DQM5 AA23 VMA_DM5
FBA_DQM6 AB27 VMA_DM6
FBA_DQM7 T26 VMA_DM7

+1.5V_GFX R414 40.2/F_4 FB_CAL_PD_VDDQ B15
FB_CAL_PD_VDDQ
R415 40.2/F_4 FB_CAL_PU_GND A15
FB_CAL_PU_GND
R413 60.4/F_4 FB_CAL_TERM_GND B16
FB_CAL_TERM_GND

+1.5V_GFX R136 10K/F_4 FB_DEBUG M22
(FBA_DEBUG)FBA_DEBUG0
For debug only
10mA

+1.05V_GFX 15mils width 200mA
L32 PBY160808T-301Y-N_6 +FB_PLLAVDD R19
300 ohm/100MHz
ESR=0.25ohm
C611 4.7U/6.3V_6
C234 1U/6.3V_4
C610 0.1U/10V_4
C613 10U/6.3V_8X
T19 AC19
FB_PLLAVDD
FB_DLLAVDD

FBA_DQS_WP0 C25 VMA_WDQS0
FBA_DQS_WP1 A19 VMA_WDQS1
FBA_DQS_WP2 E19 VMA_WDQS2
FBA_DQS_WP3 A24 VMA_WDQS3
FBA_DQS_WP4 T22 VMA_WDQS4
FBA_DQS_WP5 AA24 VMA_WDQS5
FBA_DQS_WP6 AA26 VMA_WDQS6
FBA_DQS_WP7 T27 VMA_WDQS7

FBA_DQS_RN0 D25 VMA_RDQS0
FBA_DQS_RN1 A18 VMA_RDQS1
FBA_DQS_RN2 E18 VMA_RDQS2
FBA_DQS_RN3 B24 VMA_RDQS3
FBA_DQS_RN4 R22 VMA_RDQS4
FBA_DQS_RN5 Y24 VMA_RDQS5
FBA_DQS_RN6 AA27 VMA_RDQS6
FBA_DQS_RN7 R27 VMA_RDQS7

FB_VREF A16 +FB_VREF1 TP84

[19] VMA_DQ[63..0]
[19] VMA_DM[7..0]
[19] VMA_WDQS[7..0]
[19] VMA_RDQS[7..0]

FBA_CMD0 R388 10K/F_4
FBA_CMD3 R387 10K/F_4
FBA_CMD16 R110 10K/F_4
FBA_CMD19 R111 10K/F_4
FBA_CMD20 R112 10K/F_4

U27I

COMMON PBGA533-NVIDIA-GEFORCE6250

13/13 GND_NC

AC11 AC14 AC17 AC2 AC20 AC23 AC26 AC5 AC8 AF11 AF14 AF17 AF2 AF20 AF23 AF26 AF5 AF8 B11 B14 B17 B2 B20 B23 B26 B5 B8 E11 E17 E2 E20 E23 E26 E5 E8 H2 H5 J11 J14 J17 K19 K5 L11 L13 L14 L15 L16 L17 L2 L4 M12 M13 M14 M15 M16 P19 P2 P23 P26 P5 P8 T12 T13 T14 T15 T16 U11 U12 U13 U14 U15 U16 U17 U2 U23 U26 U5 V19 V9 W11 W14 W17 Y2 Y23 Y26 Y5

GND_01 GND_02 GND_03 GND_04 GND_05 GND_06 GND_07 GND_08 GND_09 GND_10 GND_11 GND_12 GND_13 GND_14 GND_15 GND_16 GND_17 GND_18 GND_19 GND_20 GND_21 GND_22 GND_23 GND_24 GND_25 GND_26 GND_27 GND_28 GND_30 GND_31 GND_32 GND_33 GND_34 GND_35 GND_36 GND_37 GND_38 GND_39 GND_40 GND_41 GND_42 GND_43 GND_44 GND_45 GND_46 GND_47 GND_48 GND_49 GND_50 GND_51 GND_52 GND_53 GND_54 GND_55 GND_56 GND_57 GND_58 GND_59 GND_60 GND_61 GND_62 GND_63 GND_64 GND_65 GND_66 GND_67 GND_68 GND_69 GND_70 GND_71 GND_72 GND_73 GND_74 GND_75 GND_76 GND_77 GND_78 GND_79 GND_80 GND_81 GND_82 GND_83 GND_84 GND_85 GND_86 GND_87 GND_88

NC_01 C15
NC_02 D15
(NC_03)PGOOD R147 10K/F_4

nVIDIA comment 8/18

[3,5,6,7,8,9,11,15,17,32,36,38,40] +1.05V_GFX
[19,40] +1.5V_GFX

Quanta Computer Inc.

PROJECT : BU5D

Size	Document Number	Rev
	N12M-GE (MEMORY/GND)	1A
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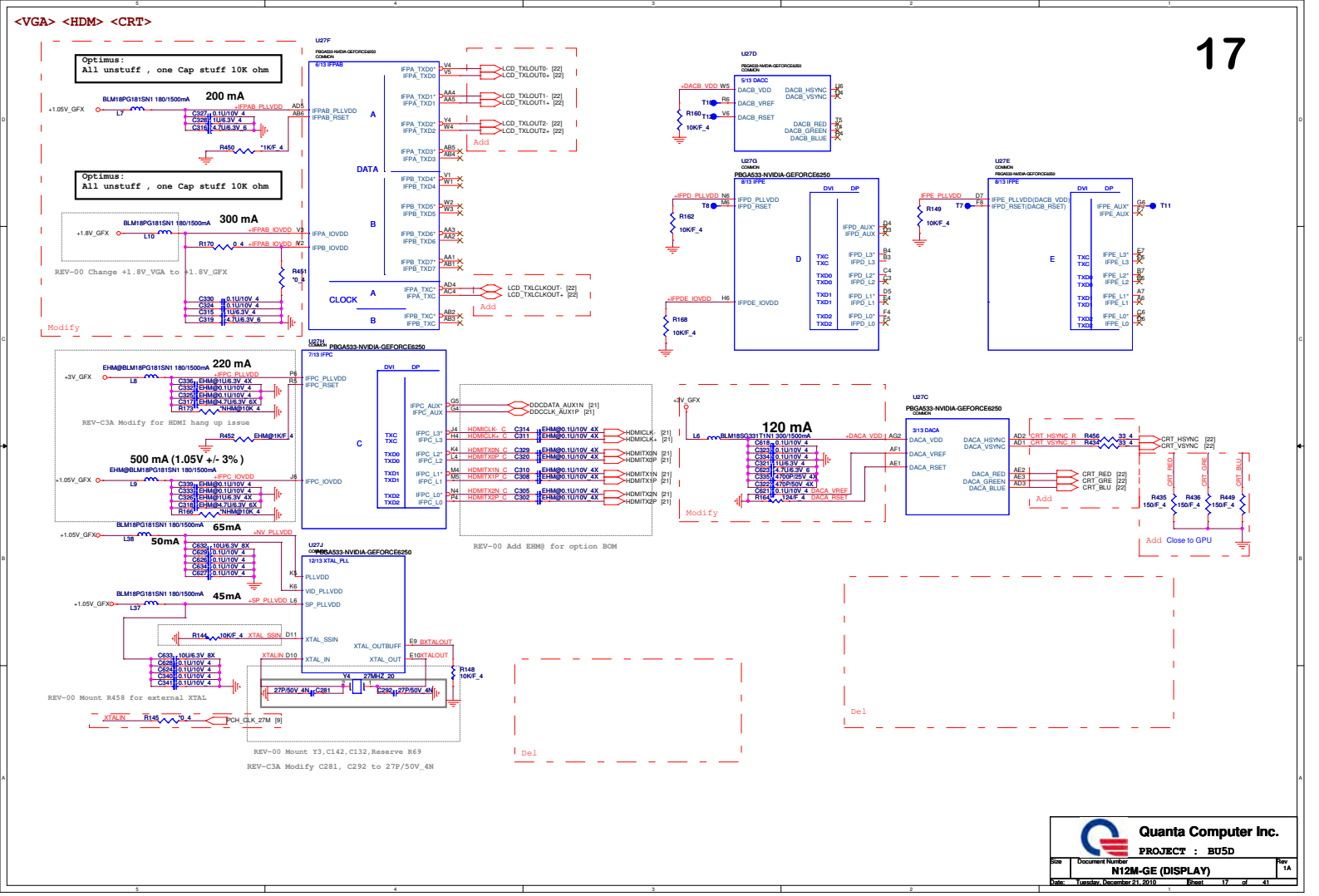
Optimus:
All unstuff , one Cap stuff 10K ohm
200 mA
300 mA
REV-00 Change +1.8V_VGA to +1.8V_GFX
Modify
220 mA
REV-C3A Modify for HDMI hang up issue
500 mA (1.05V +/- 3%)
65mA
50mA
45mA
REV-00 Mount R458 for external XTAL
REV-00 Mount Y3,C142,C132,Reserve R69
REV-C3A Modify C281, C292 to 27P/50V_4N
REV-00 Add EHM@ for option BOM
120 mA
Add
Close to GPU
Del
Quanta Computer Inc.
PROJECT : BU5D
N12M-GE (DISPLAY)
Tuesday, December 21, 2010
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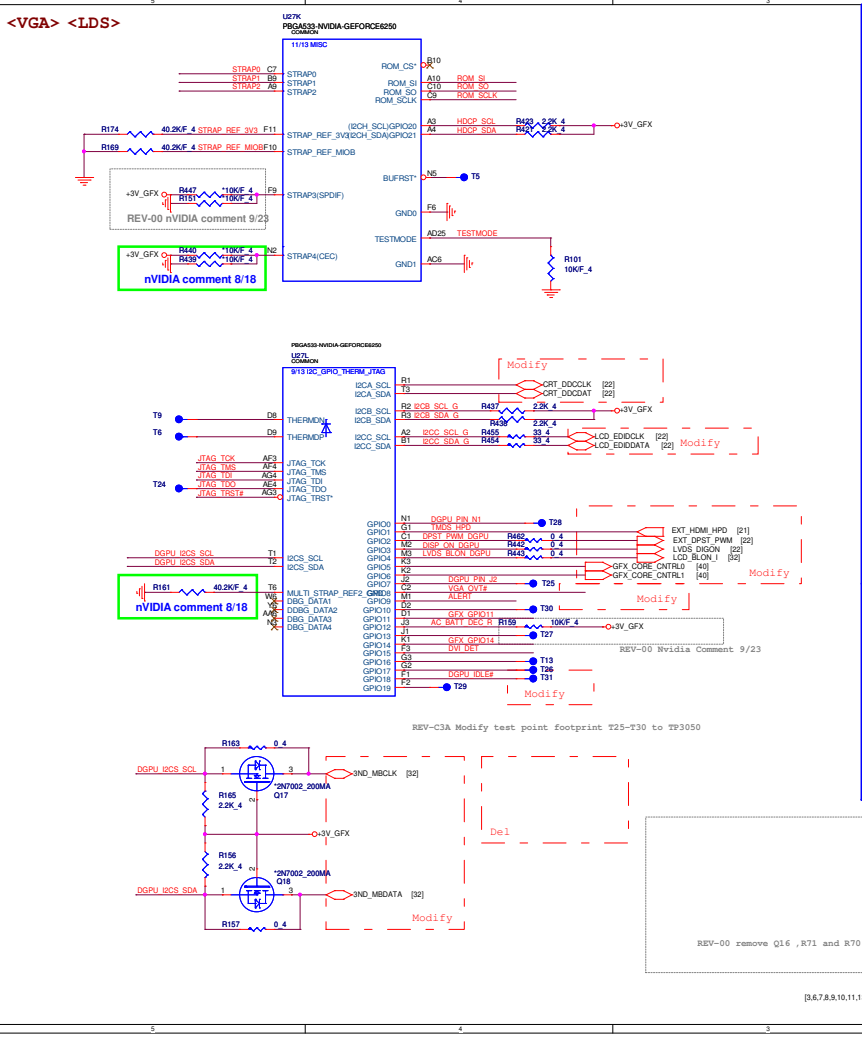
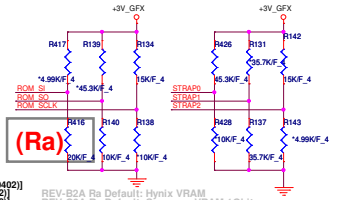


N12M-GE Device ID: 0X0A7A

N12M-GE -> 0xA7A 1010 ->PU15K

PCI_DEVID[4]/SUBVENDOR

Logical Strap Bit Mapping		
	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



REV-B2A Ra Default: Hynix VRAM
REV-C3A Ra Default: Samsung VRAM 1Gbit

4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
30.1K/F_4: CS33012FB18 [RES CHIP 30.1K 1/16W +1%(0402)]
35.7K/F_4: CS33572FB13 [RES CHIP 35.7K 1/16W +1%(0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +1% (0402)]
20K/F_4: CS32002FB29 [RES CHIP 20K 1/16W +-1%(0402)]

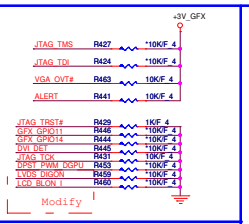
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	XCLK_417 [0]	FB_0_BAR_SIZE [0]	SMB_ALT_ADDR [0]	VGA_DEVICE [1]
ROM_SCLK	PCI_DEVIDE[4] [1]	SUB_VENDOR [0]	SLOT_CLK_CFG [1]	PEX_PLL_EN_TERM [0]
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	PCI_DEVID[3] [1]	PCI_DEVID[2] [0]	PCI_DEVID[1] [1]	PCI_DEVID[0] [0]
STRAP1	3GIO_PADCFG[3][0]	3GIO_PADCFG[2][1]	3GIO_PADCFG[1][1]	3GIO_PADCFG[0][0]
STRAP0	USER[3] [1]	USER[2] [1]	USER[1] [1]	USER[0] [1]

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000		Reserved		
0010	DDR3 64Mx16x4pcs, 128bit, 512MB,800MHz	Hynix		PD 15K
0011	DDR3 64Mx16x4pcs, 128bit, 512MB,800MHz	Samsung		PD 20K
0110	DDR3 128Mx16x4pcs, 128bit, 1GB,800MHz	Hynix		PD 35K
0111	DDR3 128Mx16x4pcs, 128bit, 1GB,800MHz	Samsung		PD 45K
XXXX				
XXXX				

(Ra)

REV-B2A



GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	Memory VREF SELECT
11	I/O	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	THERM_LOAD_STEP_DOWN
14	OUT	N/A	THERM_LOAD_STEP_UP

Quanta Computer Inc.
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	N12M-GE (GPIO/STRAPS)	1A
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<VGA>

REV-B2A Hynix 64Mx16 P/N: AKD5LZWTW02--1st
Hynix 128Mx16 P/N: AKD5MGWTW00--2nd

CHANNEL A: 256MB/512MB DDR3

REV-C3A Default Samsung 1Gbit

[16] VMA_DQ[63..0]
[16] VMA_DM[7..0]
[16] VMA_WDQS[7..0]
[16] VMA_RDQS[7..0]

U12 U26 U11 U25

96-BALL SDRAM DDR3 VRAM_DDR3

U10 U31 U11 U30

Left Right

[16,40] +1.5V_GFX

Quanta Computer Inc.
PROJECT : BU5D

Size	Document Number	Rev
	DDR3 VRAM (BGA96)	1A
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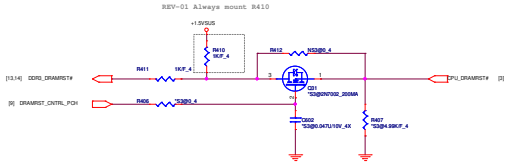
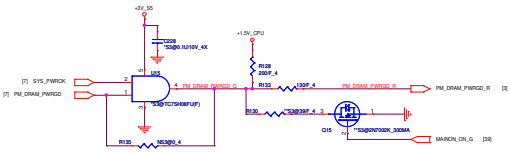
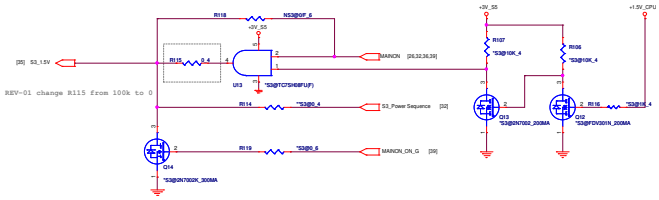
S3 power Reduction (SM_DRAMRST#)<S3P> <CLG> <4>



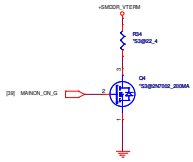
S3 power Reduction (SM_DRAMPWROK)<S3P> <3>



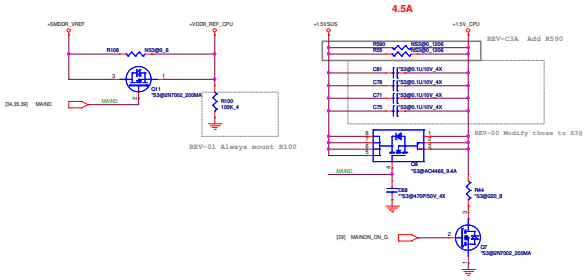
For S3 power Reduction Sequence<S3P> <3>



For S3 power Reduction VTT discharge<S3P> <13>



S3 power Reduction (CPU Power)<S3P> <5>



Quanta Computer Inc.

PROJECT : BU5D

Size: Document Number: S3 power Reduction Rev: 1A

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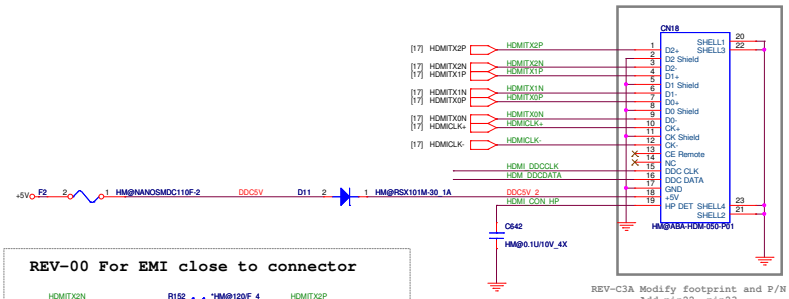
HDMI Conn <HDM>

HDMI-CONN

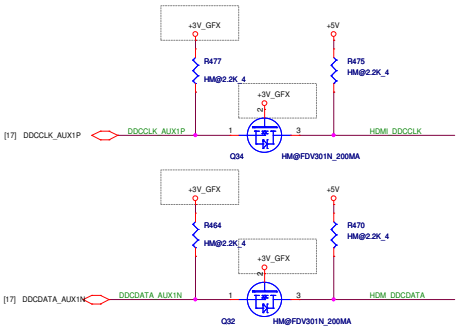


REV-C3A Modify footprint and P/N
Add pin22, pin23

REV-00 For EMI close to connector

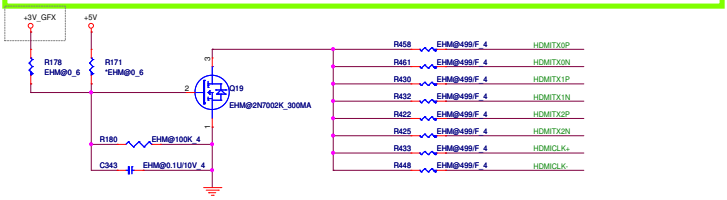
HDMITX2N	R152	*HM@120/F_4	HDMITX2P
HDMITX1N	R155	*HM@120/F_4	HDMITX1P
HDMITX0N	R167	*HM@120/F_4	HDMITX0P
HDMICLK-	R158	*HM@120/F_4	HDMICLK+

HDMI-SMBus <HDM>

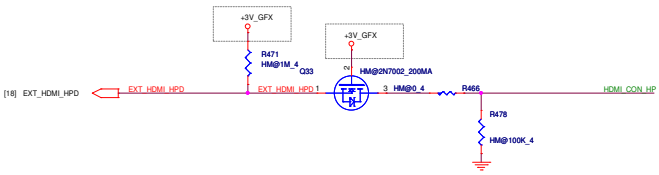


REV-00 Nvidia Comment +3V_GFX to instead of +3V
as below power rails to avoid power leakage issue

HDMI-passive level shift <HDM>



HDMI-HPD <HDM>



REV-00 Del External HDMI-HPD

Quanta Computer Inc.
PROJECT : BU5D

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	HDMI CONN	1A
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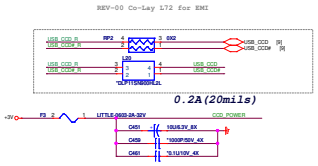
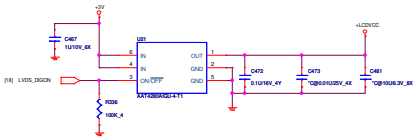
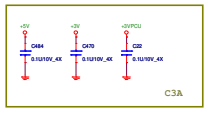
CCD <CCD>

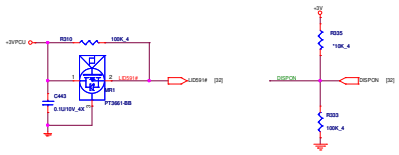


LCD POWER SWITCH <LDS>

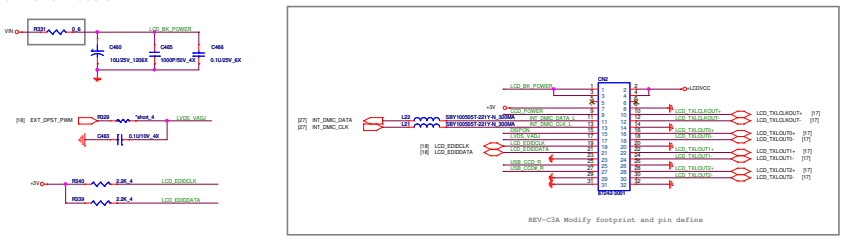


HALL SENSOR&BACK LIGHT SWITCH <HSR>

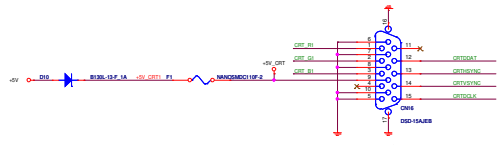




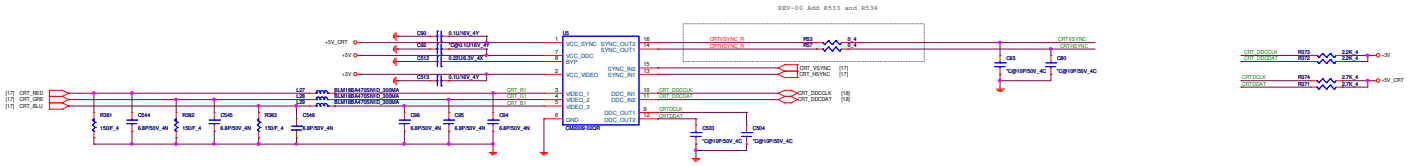
LCD Panel Module <LDS> <ADO>



CRT CONN Interface <CRT>



<CRT>



Quanta Computer Inc.		
PROJECT : BU5D		
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	LCD/LED Panel/CCD	1A
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MINI Card Slot#1 <MNW>
(WiFi)

Before RAMP must to remove
debug card component

REV-C3A Mount C474

SMBus(DDR3/WLAN/3G)

MINI Card Slot#2 <MNT>
3G

REV-C3A Add R591

For SIM Card on daughtor board

REV-00 Co-Lay L77 for EMI

REV-00 update NEW footprint bl121-12r-tand-12p-1
REV-02A Modify footprint and pin define

REV-00 Add Q10,R7,R201 for CLK REQ#

Quanta Computer Inc.
PROJECT : BU5D

Size	Document Number	Rev
	MINI CARD(WLAN/3G/SIM Card)	1A
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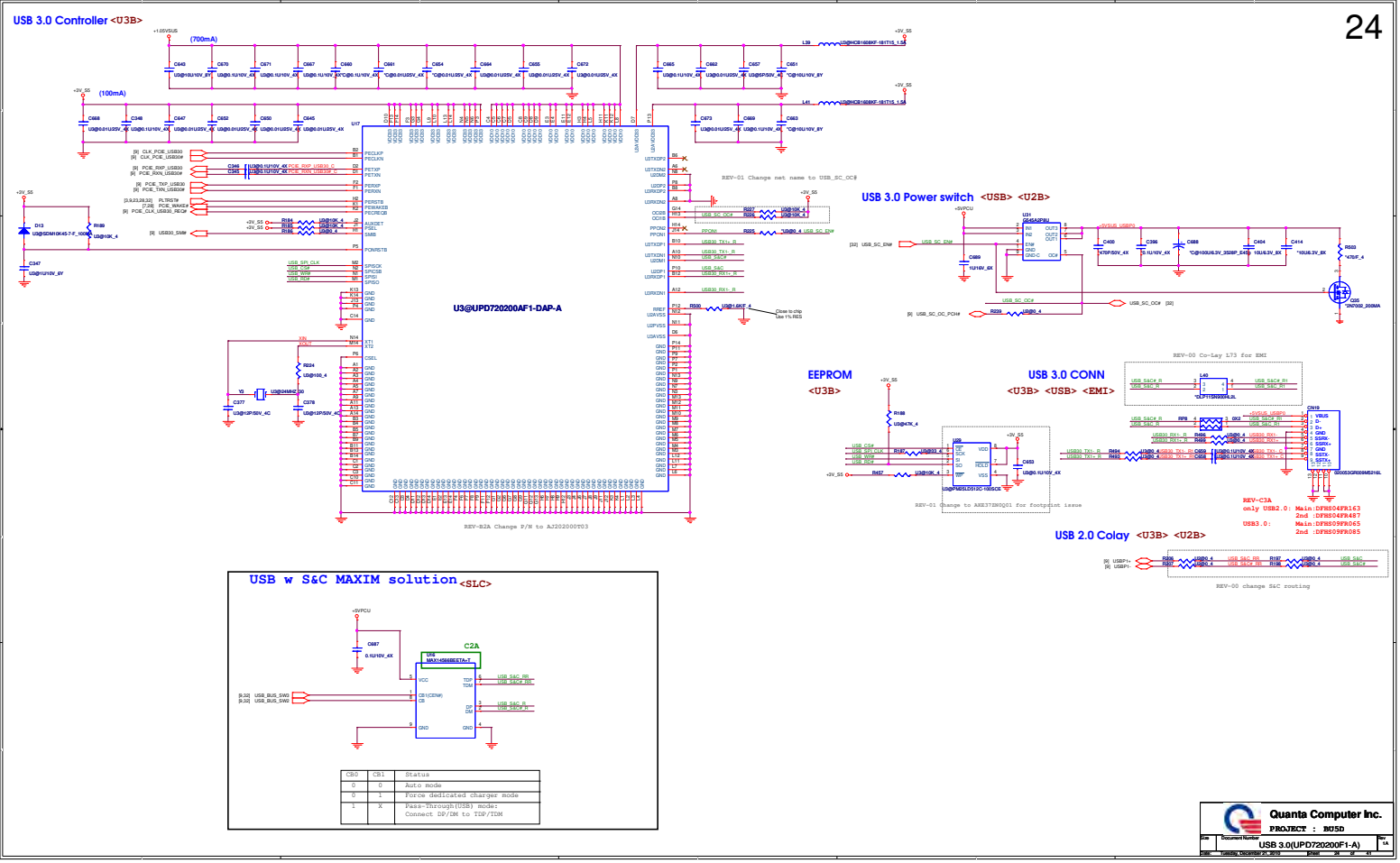
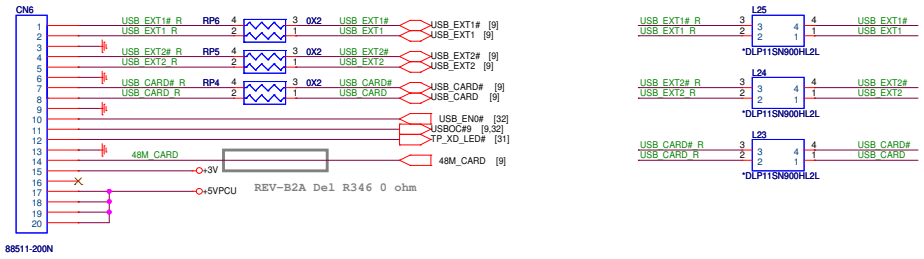


Quanta Computer Inc.
PROJECT : BU5D
USB 3.0(UPD720200F1-A)

USB2.0 Left 1
USB2.0 Left 2 <U2B> <MMC> <EMI>



REV-00 Co-Lay L74,L75,L76 for EMI

Quanta Computer Inc.
PROJECT : BU5D

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	HDMI CONN	1A

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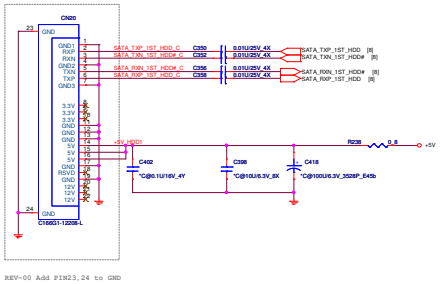
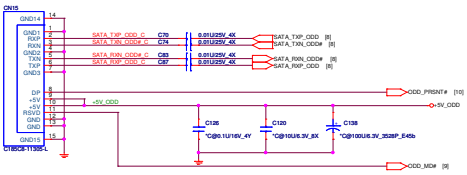
HDD Interface <H1D>

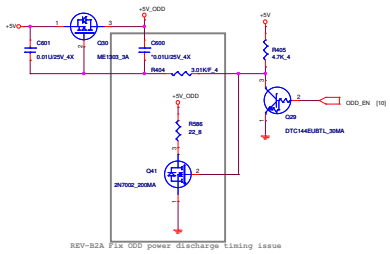


REV-00 Add PIN23,24 to GND

ODD Interface <ODD>

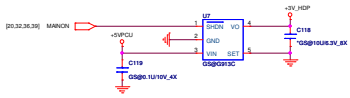


ODD Zero power . (Only for Intel) <OZP>

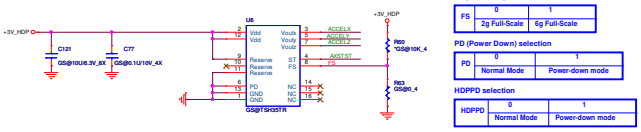


REV-B2A Fix ODD power discharge timing issue

3D-LDO Power <GSR>



3D-Sensor IC <GSR>



FS (Full Scale) selection

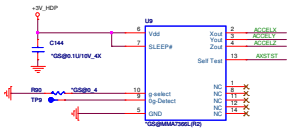
FS	0	1
	2g Full-Scale	6g Full-Scale

PD (Power Down) selection

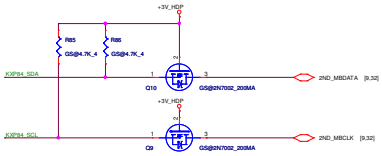
PD	0	1
	Normal Mode	Power-down mode

HDPPD selection

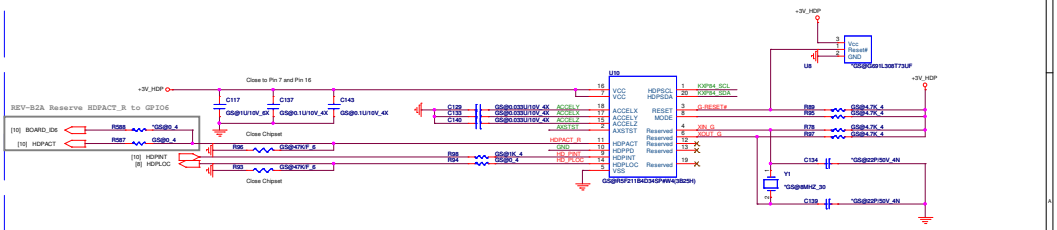
HDPPD	0	1
	Normal Mode	Power-down mode



3D-SMBus <GSR>



3D-u-micro P <GSR>



Quanta Computer Inc.

PROJECT : BU5D

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	HDD/ODD/MDC	1A

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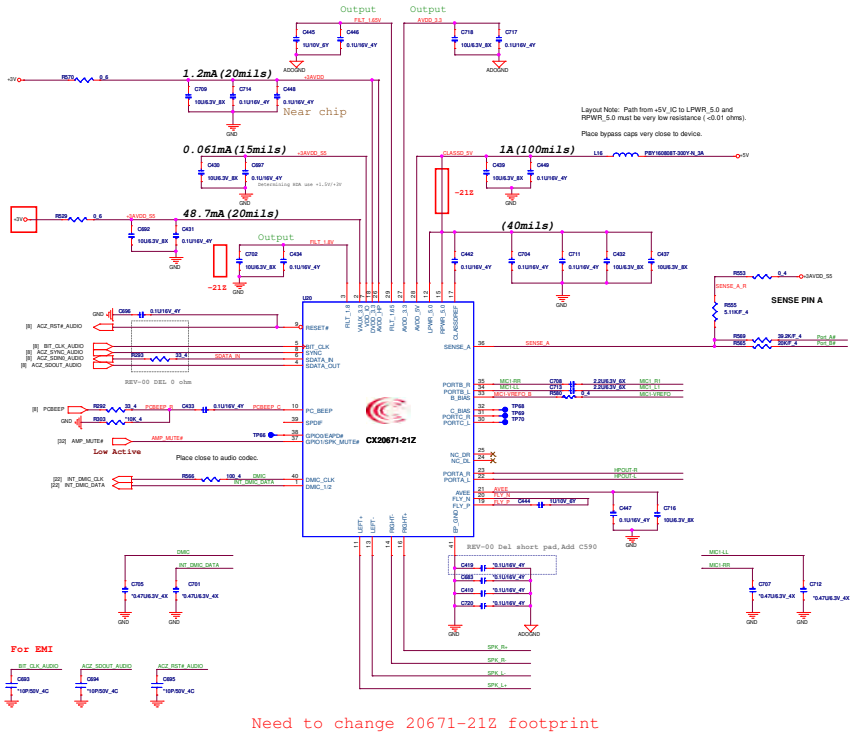
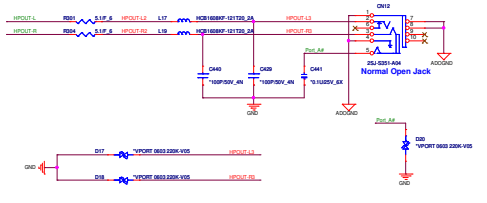
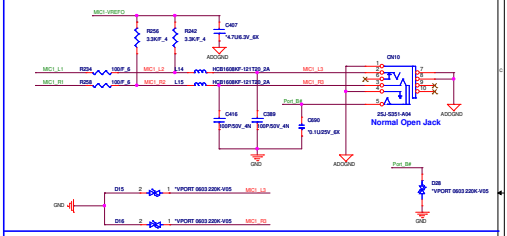
Codec (CX20671-21Z) <ADO>



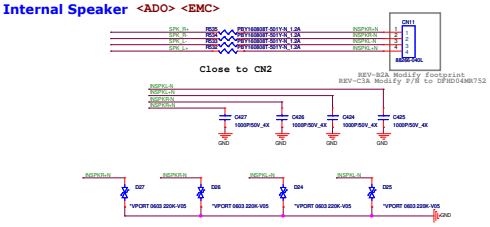
HP <ADO> <EMC>



External MIC <ADO> <EMC>



Internal Speaker <ADO> <EMC>



Quanta Computer Inc.		
PROJECT : BU5D		
Size	Document Number: Audio Codec(CX20671-21Z)	Rev: 1A
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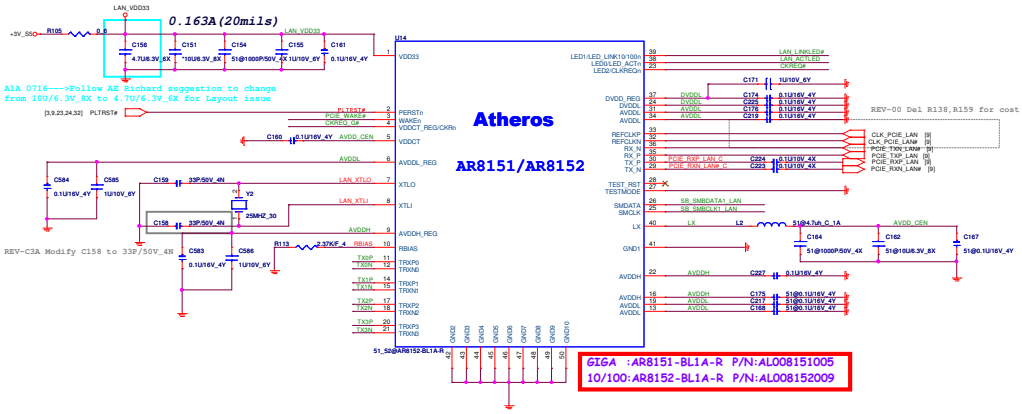
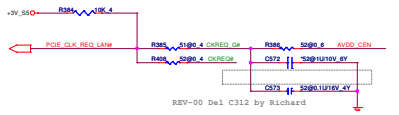
Atheros Lan <LAN> <LNG> <LN1> Default 10/100



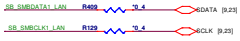
<LAN> <LNG> <LN1>



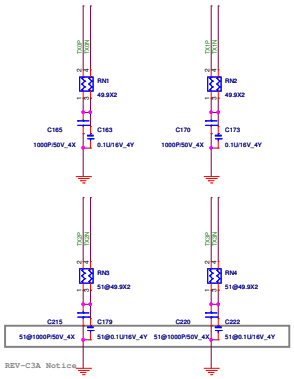
REV-00 Del R138,R159 for cost down

LAN-Wake up function

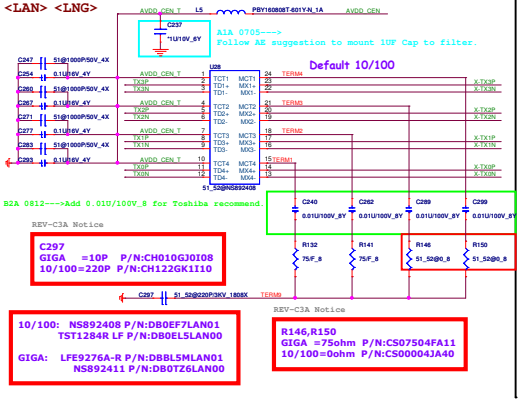
LAN-SM-Bus <LAN>



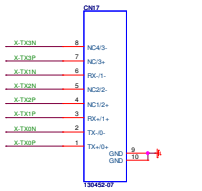
PLACE NEAR LAN IC SIDE <LAN> <LNG>



TRANSFORMER <LAN> <LNG>



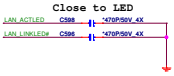
RJ45 <LAN> <LNG> <LN1>



LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G#	1	Normal function
	0	ATE test mode

Power on Strapping pin

Close to LED



Quanta Computer Inc.			
PROJECT : BU5D			
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	Atheros Lan		1A
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3 IN 1 CARD READER

3 IN 1 CARD READER

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	Card Reader (RTS5138)	1A
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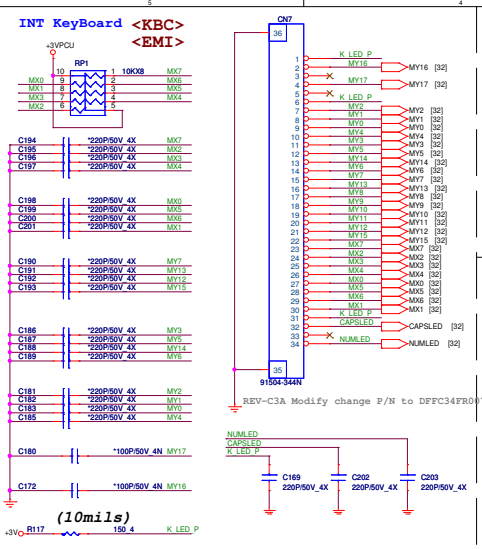
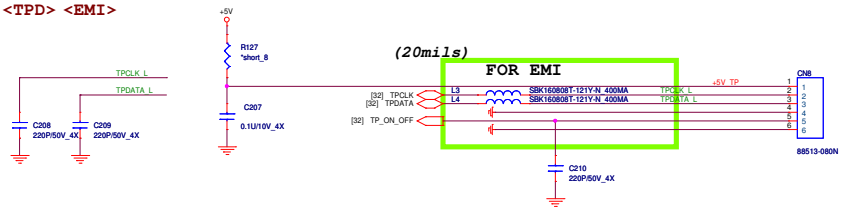
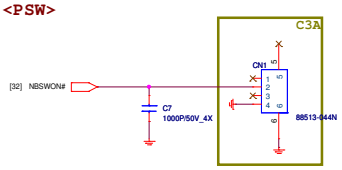
INT KeyBoard <KBC> <EMI>



TP board <TPD> <EMI>



Power board <PSW>



HOLE

CPU h-tc276bc217d146p2

HOLE9 *h-tc276bc217d146p2
HOLE10 *h-tc276bc217d146p2
HOLE14 *h-tc276bc217d146p2

VGA

HOLE15 *h-tc276bc217d146p2
HOLE17 *h-tc276bc217d146p2

REV-B2A Change to h-tc276bc217d146p2

MINI CARD H-TC217BC142D102P2

REV-B2A Change to h-tc217bc138d102p2

HOLE6 H-TC217BC142D102P2
HOLE7 h-tc217bc138d102p2

HDD&ODD

H-TC236BC315D110P2

HOLE19 *H-TC236BC315D110P2

Pad-c197

HOLE4 *pad-c197
HOLE3 *pad-c197
HOLE12 *pad-c197
HOLE11 *pad-c197
HOLE18 *pad-c197
HOLE20 *pad-c197

h-tc315bc256d110p2

HOLE5 *h-tc315bc256d110p2

REV-B2A Change to h-tc315bc256d110p2

REV-00 Change GND to ADOGND

H-C91D91N

HOLE8 *H-C91D91N
HOLE2 *H-C91D91N

HG-TC315BC236D110P2

HOLE16 *HG-TC315BC236D110P2

HG-C236D110P2

HOLE1 *HG-C236D110P2

HG-TC236BC315D110P2

HOLE13 *HG-TC236BC315D110P2

hg-c315d110p2

HOLE22 *hg-c315d110p2
HOLE21 *hg-c315d110p2 ADOGND

REV-B2A Change to hg-c315d110p2

H-C91D91N

HOLE23 *H-C91D91N

REV-C3A Add

Quanta Computer Inc.
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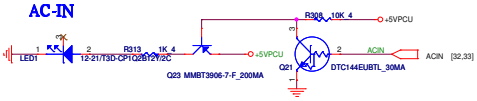
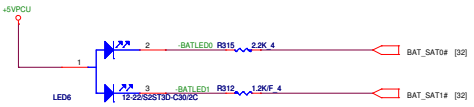
LED <LED>

AC-IN

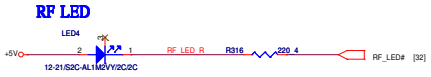


BATERRY

D3A : LED luminance to light,1K-ohm change 2.2K-ohm.

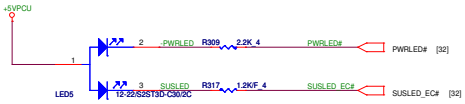


RF LED

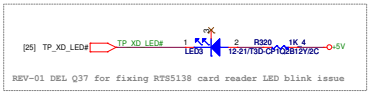


POWER

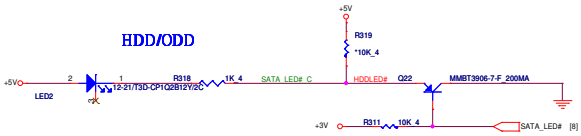
D3A : LED luminance to light,1K-ohm change 2.2K-ohm.



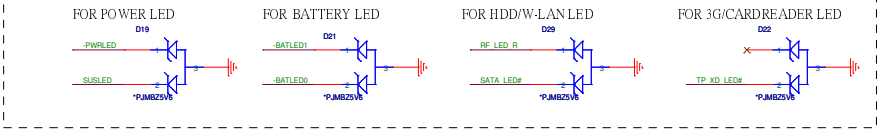
CARDREADER



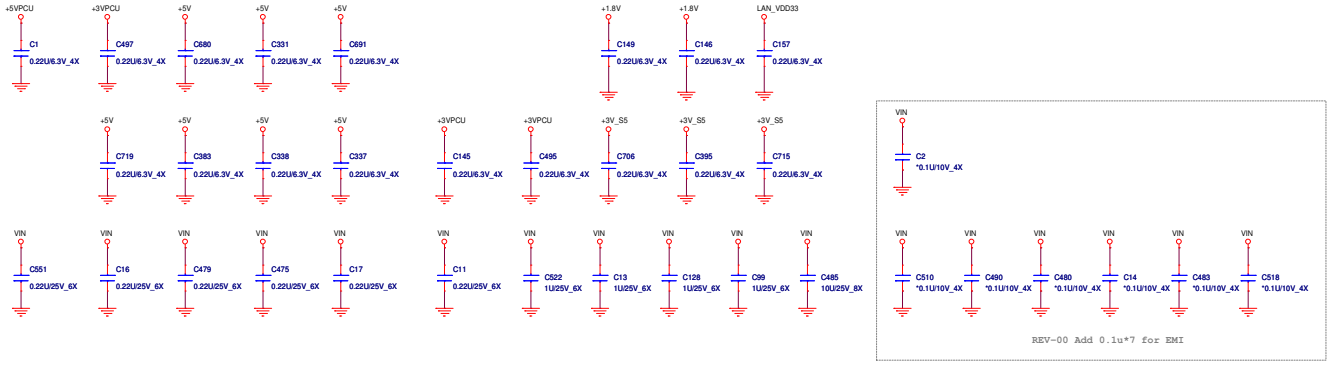
HDD/ODD



ESD Protect <EMC>



<EMI>



Quanta Computer Inc.

PROJECT : BU5D

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	LED/HOLE	1A
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EC <KBC>

0.01A(20mils)

0.03A(30mils)

H=1.6mm

REV-00 Del USBOC#8

REV-00 Del USB_EN1#

REV-C3A Add 2.2/F_4

REV-00 Del SKU strap pin

CLK 32.768K Hz from PCH

Intel Turbo mode only <CPU>

SM BUS PU/Address <KBC>

REV-00 change power from +3VPCU to +3V

3Cell Battery protect & K/B LED Control <KBC>

Strap <KBC>

ID EEPROM <KBC>

0.003A(20mils)

ADDRESS: A0H

SPI FLASH <KBC>

0.025A(20mils)

REV-B2A Add for EMI

Intel	512KB	W25X40BVSSIG
AMD	2MB	W25Q16BVSSIG

INTERNAL KEYBOARD STRIP SET <KBC>

HWPG circuit <KBC> <VGA>

SMBUS Table

SMBUS	Devices	Address
1	Battery	12H
2	CPU Board Thermal Sensor	
	EC EEPROM	A0H
3	VGA Board Thermal Sensor	98H

Close to U12

SKU strap pin <KBC>

13MS UMA = 000
13MS VGA = 001

Power Button <KBC>

LED PU/PD <LED>

REV-B2A Reserve CN4
REV-00 Add C32,C30 for EMI

REV-B2A Add USB_BUS_SW2

REV-B2A Add USB_BUS_SW3

REV-00 Del USB30_PWR_EN

Quanta Computer Inc.
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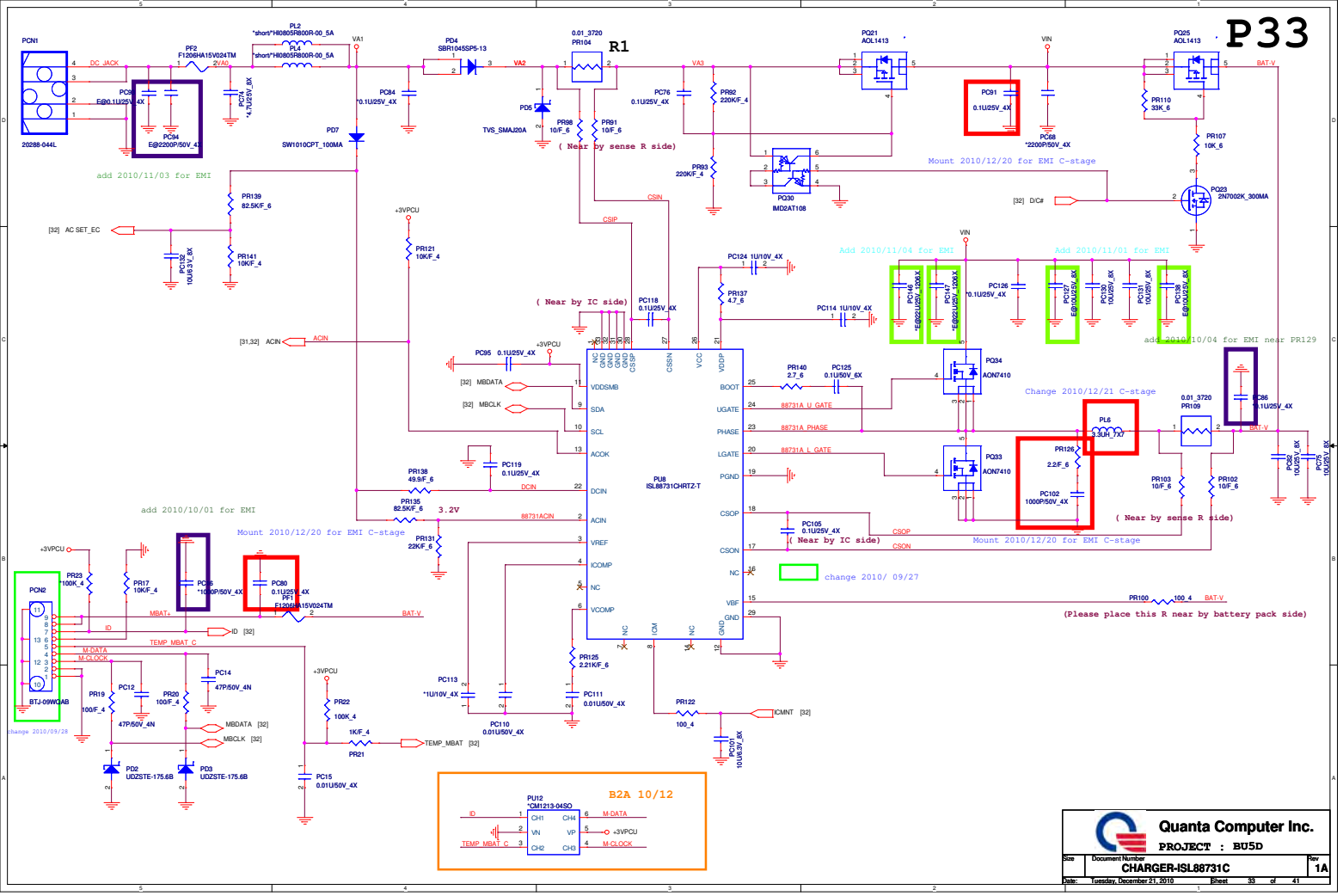
P33
R1
PCN1
20288-044L
DC_JACK
PF2
F1206HA15V024TM
2VA0
PL2
*short*HI0805R800R-00_5A
PL4
*short*HI0805R800R-00_5A
VA1
PD4
SBR1045SP5-13
VA2
PD5
TVS_SMAJ20A
PD7
SW1010CPT_100MA
0.01_3720
PR104
PR98
10/F_6
PR91
10/F_6
(Near by sense R side)
PC76
0.1U/25V_4X
PR92
220K/F_4
PR93
220K/F_4
PQ30
IMD2AT108
PQ21
AOL1413
PC91
0.1U/25V_4X
VIN
PC68
*2200P/50V_4X
PQ25
AOL1413
BAT-V
PR110
33K_6
PR107
10K_6
PQ23
2N7002K_300MA
[32] D/C#
Mount 2010/12/20 for EMI C-stage
add 2010/11/03 for EMI
PC92
E@0.1U/25V_4X
PC94
E@2200P/50V_4X
PC84
*0.1U/25V_4X
PC93
*4.7U/25V_6X
PR139
82.5K/F_6
PR141
10K/F_4
[32] AC SET_EC
PC102
10U/6.3V_6X
+3VPCU
PR121
10K/F_4
CSIN
CSIP
(Near by IC side)
PC118
0.1U/25V_4X
PC124 1U/10V_4X
PR137
4.7_6
PC114 1U/10V_4X
Add 2010/11/04 for EMI
Add 2010/11/01 for EMI
PC148
*E@220U/25V_10X6X
PC147
*E@220U/25V_10X6X
PC126
*0.1U/25V_4X
PC127
E@10U/25V_6X
PC130
10U/25V_6X
PC131
10U/25V_6X
PC138
E@10U/25V_6X
add 2010/10/04 for EMI near PR129
[31,32] ACIN
ACIN
PC95 0.1U/25V_4X
[32] MBDATA
[32] MBCLK
PU8
ISL88731CHRTZ-T
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
PR140
2.7_6
PC125
0.1U/50V_6X
PQ34
AON7410
88731A_U_GATE
88731A_PHASE
88731A_L_GATE
PQ33
AON7410
Change 2010/12/21 C-stage
PL6
3.3UH_7X7
PR126
2.2/F_6
PC102
1000P/50V_4X
(Near by sense R side)
0.01_3720
PR109
PC26
0.1U/25V_4X
BAT-V
PR103
10/F_6
PR102
10/F_6
PC103
10U/25V_6X
PC75
10U/25V_6X
PC119
0.1U/25V_4X
DCIN
PR138
49.9/F_6
PR135
82.5K/F_6
3.2V
88731ACIN
PR131
22K/F_6
PC105
0.1U/25V_4X
(Near by IC side)
CSOP
CSON
Mount 2010/12/20 for EMI C-stage
change 2010/ 09/27
PR100
100_4
BAT-V
(Please place this R near by battery pack side)
add 2010/10/01 for EMI
Mount 2010/12/20 for EMI C-stage
+3VPCU
PCN2
BTJ-099WCAB
PR23
100K_4
PR17
10K/F_4
PC86
*1000P/50V_4X
PC80
0.1U/25V_4X
PF1
F1206HA15V024TM
MBAT+
BAT-V
ID
ID [32]
TEMP_MBAT_C
M-DATA
M-CLOCK
change 2010/09/28
PR19
100/F_4
PC12
47P/50V_4N
PR20
100/F_4
PC14
47P/50V_4N
MBDATA [32]
MBCLK [32]
PD2
UDZSTE-175.6B
PD3
UDZSTE-175.6B
+3VPCU
PR22
100K_4
1K/F_4
PR21
TEMP_MBAT [32]
PC15
0.01U/50V_4X
PC113
*1U/10V_4X
PC110
0.01U/50V_4X
PR125
2.21K/F_6
PC111
0.01U/50V_4X
PR122
100_4
ICMNT [32]
PC101
10U/6.3V_6X
B2A 10/12
PU12
*QM1213-04SO
ID
TEMP_MBAT_C
CH1
VN
CH2
CH4
VP
CH3
M-DATA
+3VPCU
M-CLOCK
Quanta Computer Inc.
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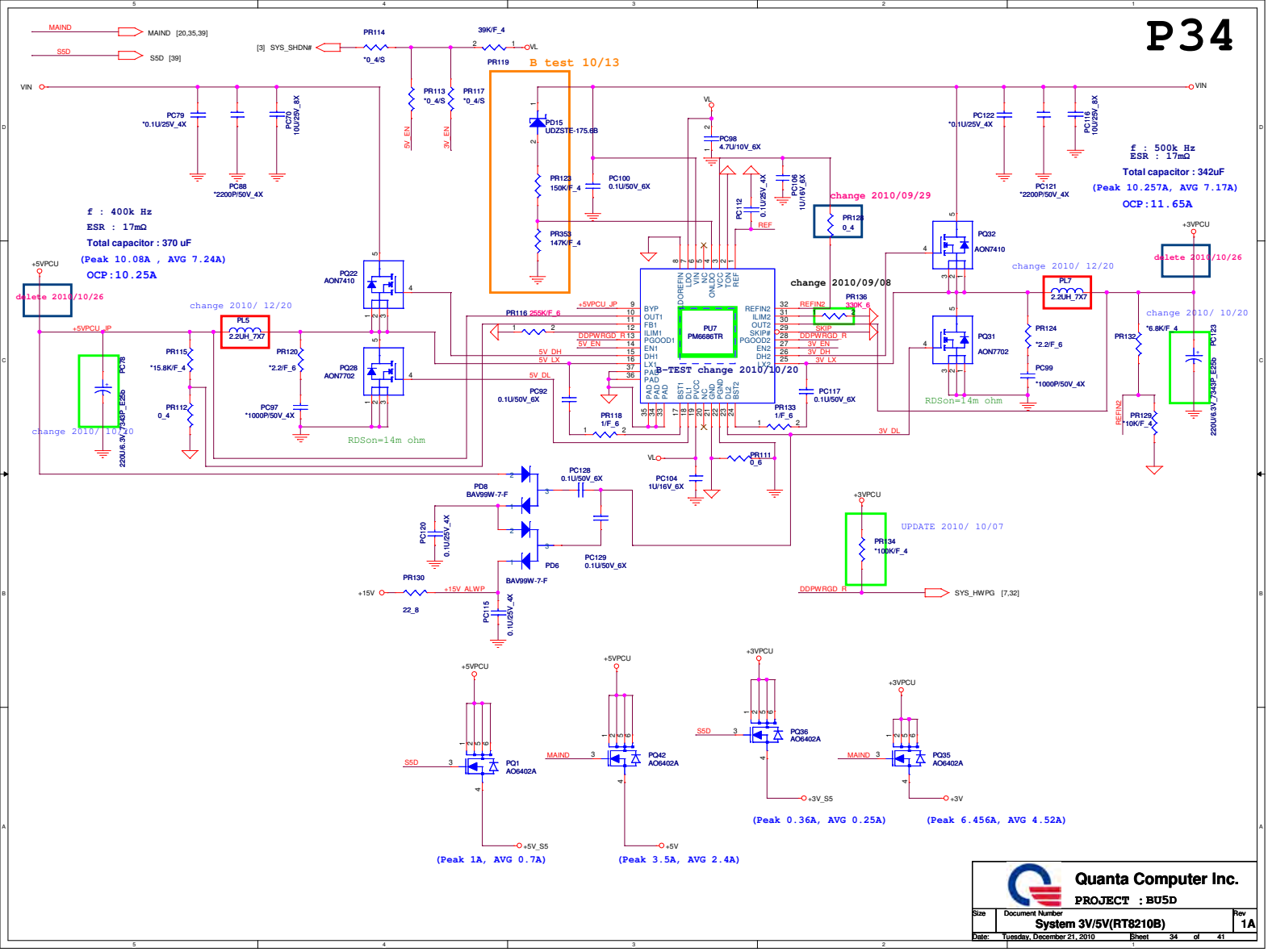

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	System 3V/5V(RT8210B)	1A

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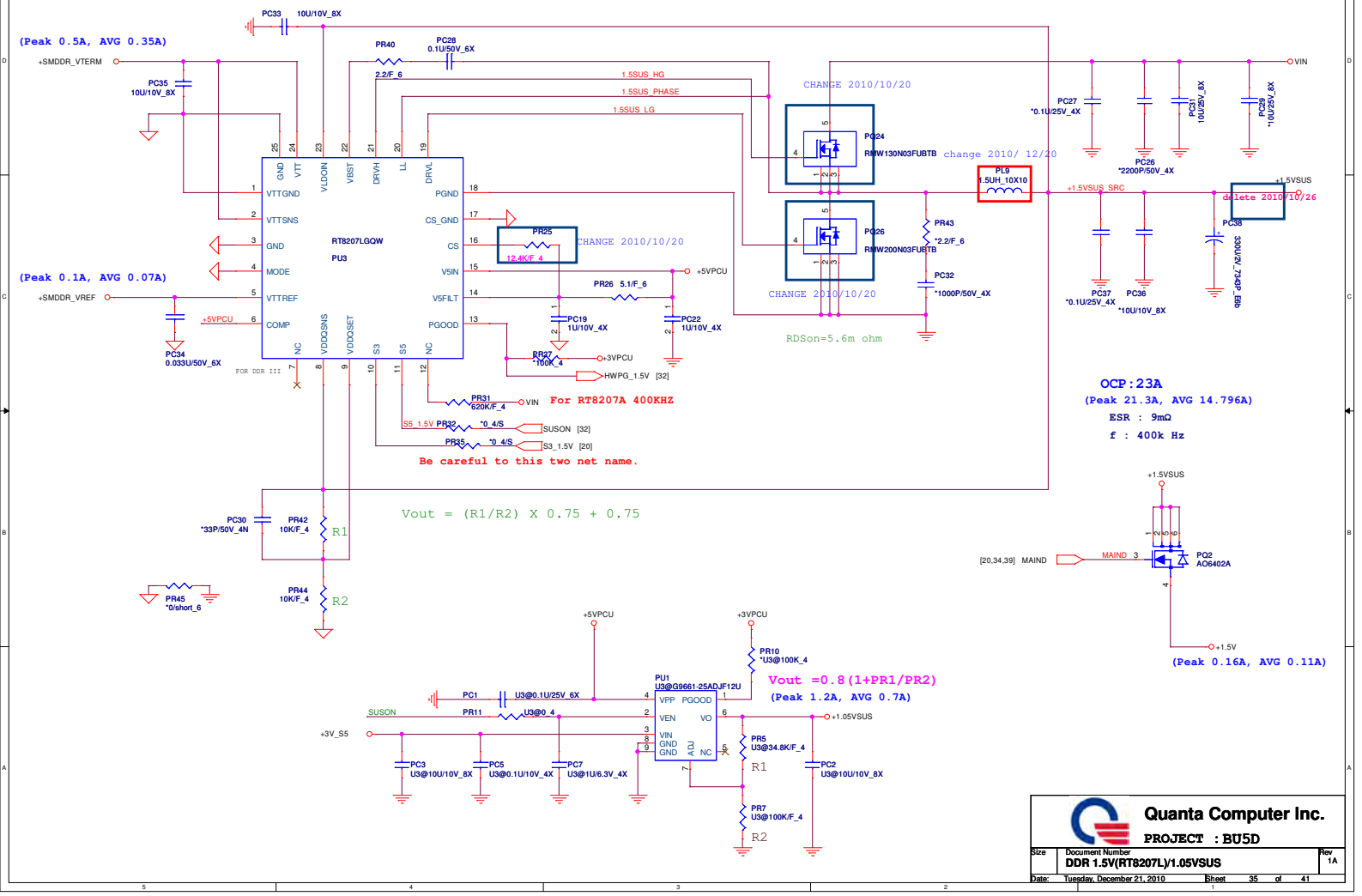
(Peak 0.5A, AVG 0.35A)
(Peak 0.1A, AVG 0.07A)
RT8207LGQW
PU3
FOR DDR III
CHANGE 2010/10/20
change 2010/ 12/20
delete 2010/10/26
RDSon=5.6m ohm
For RT8207A 400KHZ
Be careful to this two net name.
OCP:23A
(Peak 21.3A, AVG 14.796A)
ESR : 9mΩ
f : 400k Hz
Vout = (R1/R2) X 0.75 + 0.75
Vout =0.8(1+PR1/PR2)
(Peak 1.2A, AVG 0.7A)
(Peak 0.16A, AVG 0.11A)
Quanta Computer Inc.
PROJECT : BU5D
DDR 1.5V(RT8207L)/1.05VSUS
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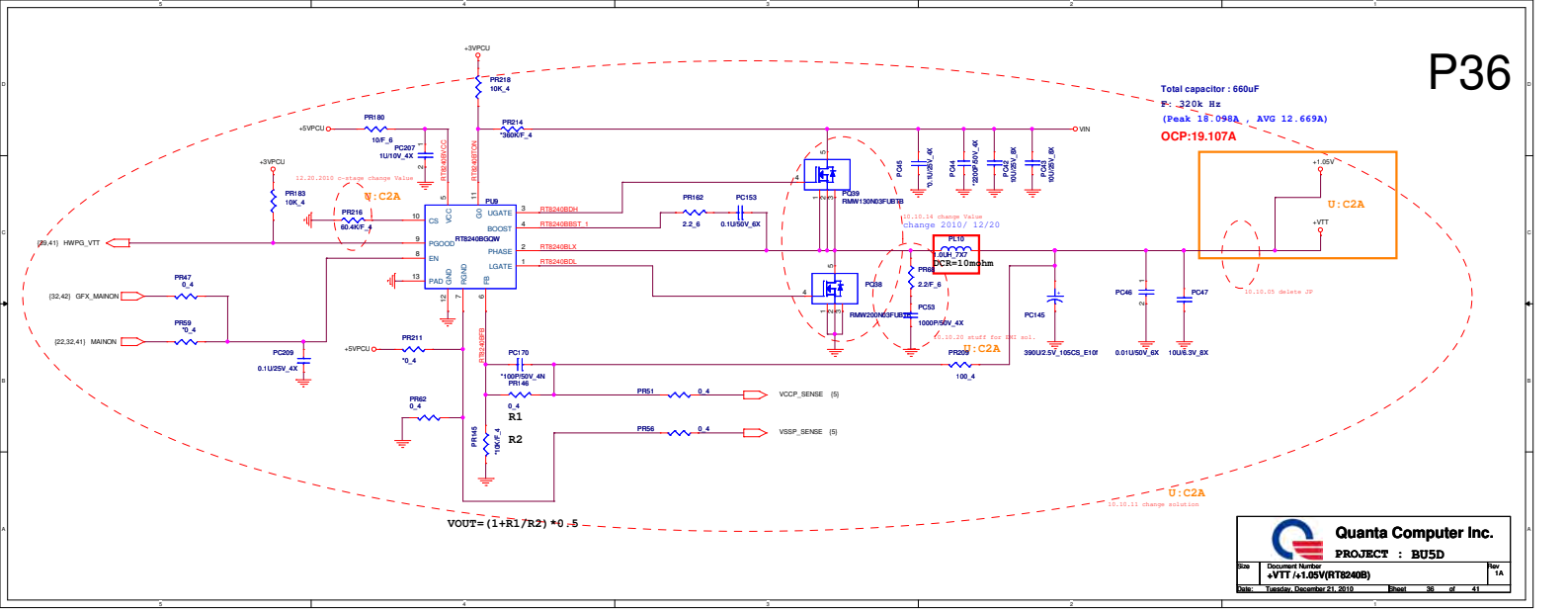
Total capacitor : 660uF
F: 320k Hz
(Peak 18.098A , AVG 12.669A)
OCP:19.107A
VOUT= (1+R1/R2) *0.5
R1
R2
RT8240BGQW
change 2010/ 12/20
U:C2A
VCCP_SENSE (5)
VSSP_SENSE (5)
+VTT /+1.05V(RT8240B)
PROJECT : BU5D
Quanta Computer Inc.
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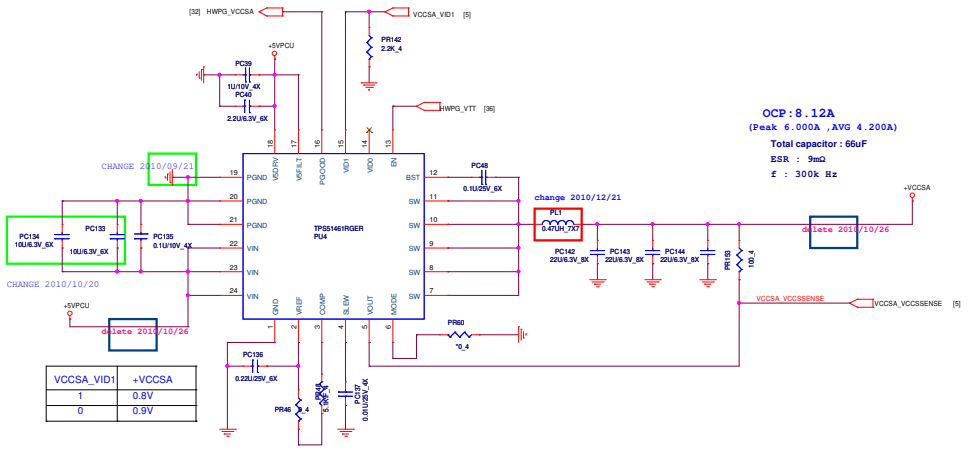

VCCSA_VID1	+VCCSA
1	0.8V
0	0.9V

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		1A

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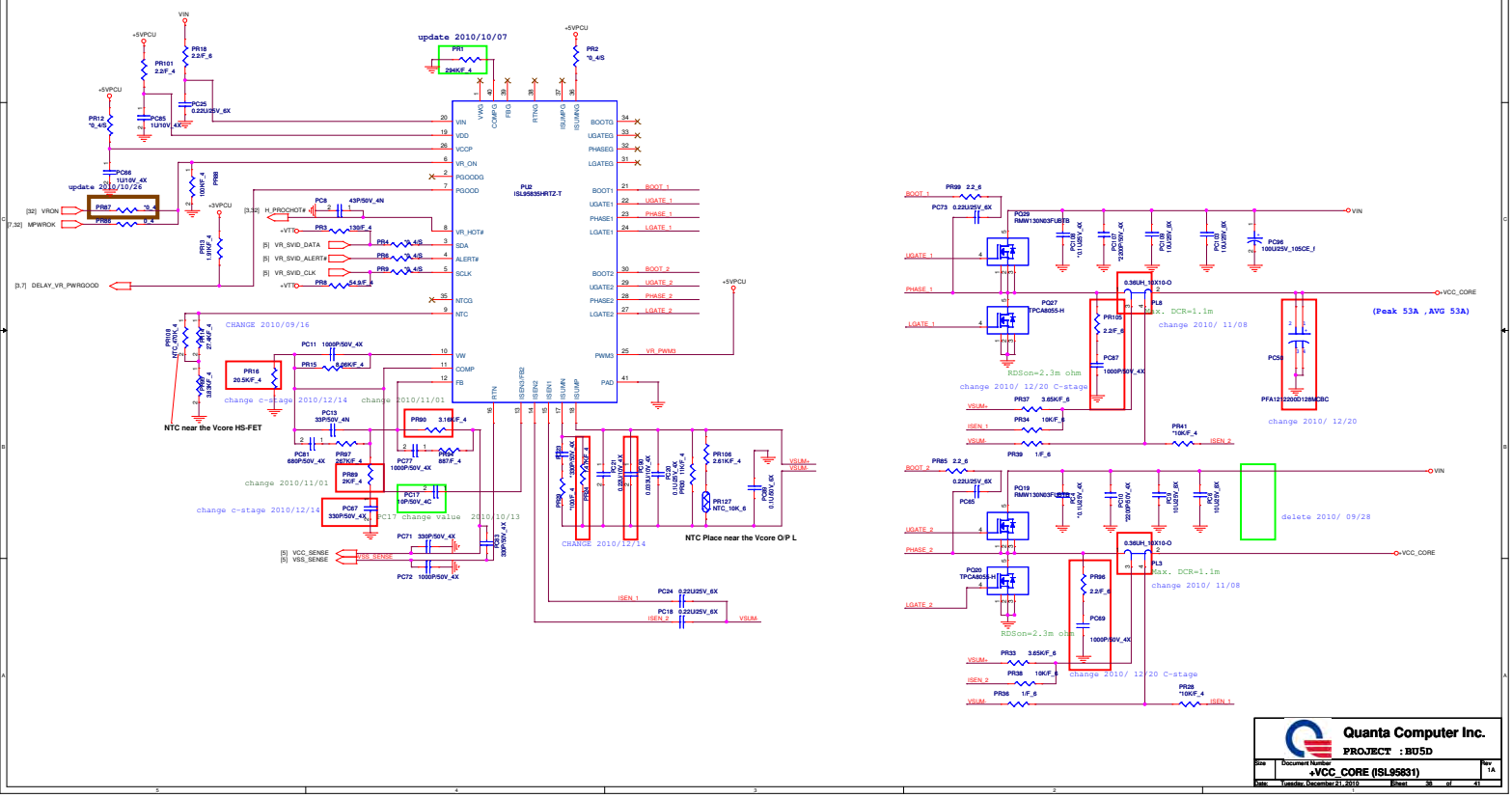

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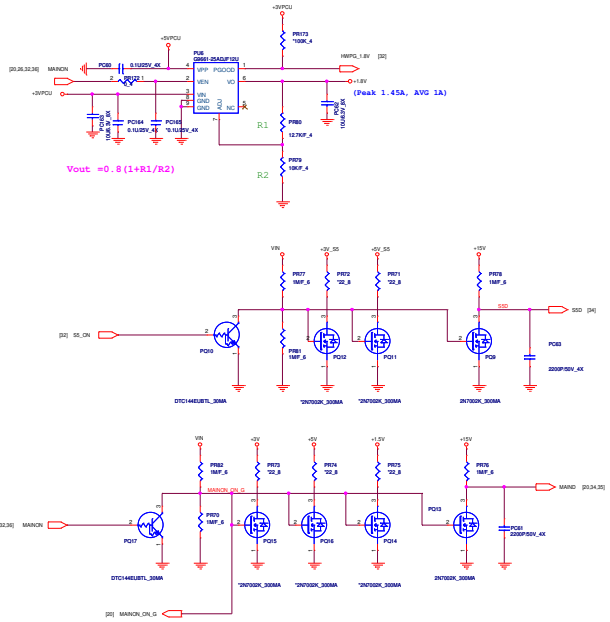

Quanta Computer Inc.		
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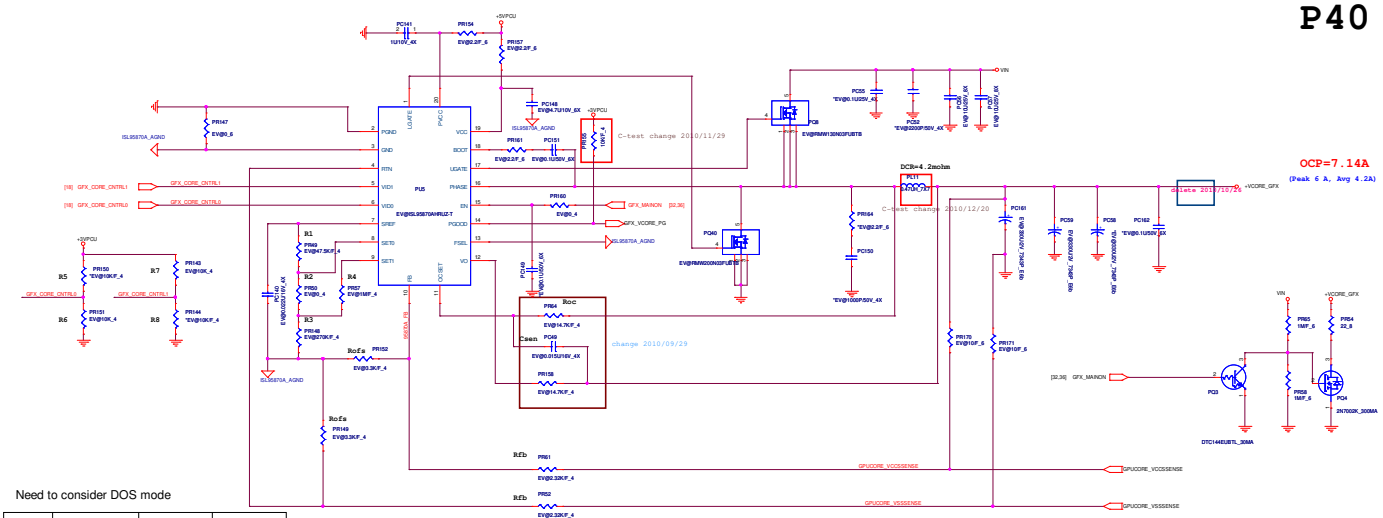
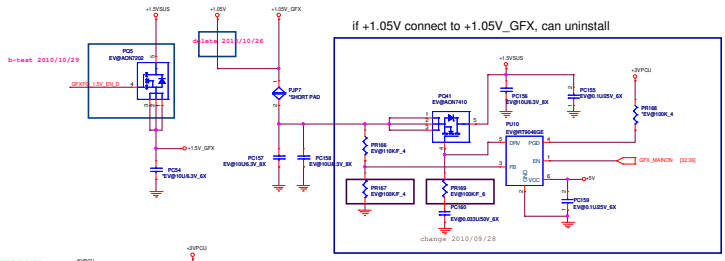
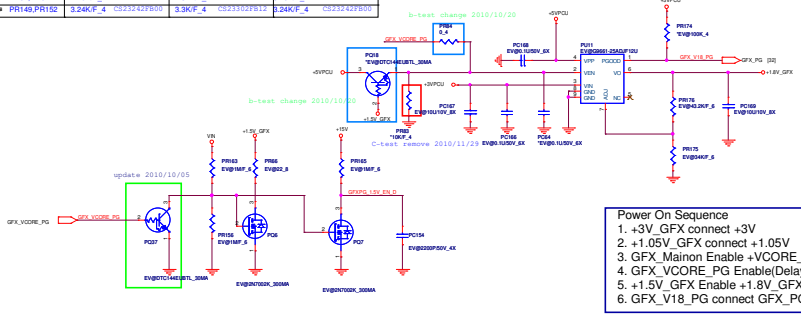


Default	N12P-LP	N12M-GE	N12P-GV
PR150 R5	10K CS31002JB28	NC	10K CS31002JB28
PR151 R6	NC	10K CS31002JB28	NC
PR143 R7	NC	10K CS31002JB28	10K CS31002JB28
PR144 R8	10K CS31002JB28	NC	NC

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	N12P-LP	N12M-GE	N12P-GV
LOW	LOW	0.925V	1.0V	0.98V
LOW	HIGH	0.90V Default	1.0V	0.98V
HIGH	LOW	0.9V	1.0V Default	0.98V
HIGH	HIGH	0.825V	0.85V	0.98V Default

		N12P-LP	N12M-GE	N12P-GV
R1	PR149	22.6K/F_4 CS32262FB15	47.5K/F_4 CS34752FB14	0_4 CS00002JB38
R2	PR50	0_4 CS00002JB38	0_4 CS00002JB38	0_4 CS00002JB38
R3	PR148	243K/F_4 CS42432FB02	270K/F_4 CS42702JB10	300K/F_4 CS43002JB18
R4	PR57	750K/F_4 CS47502FB14	1M/F_4 CS51002FB11	1M/F_4 CS51002FB11
Rfb	PR61,PR52	2.10K/F_4 CS22102FB12	2.32K/F_4 CS22322FB00	3.16K/F_4 CS23162FB00
Rofs	PR149,PR152	3.24K/F_4 CS23242FB00	3.3K/F_4 CS23302FB13	3.24K/F_4 CS23242FB00





Power On Sequence
1. +3V_GFX connect +3V
2. +1.05V_GFX connect +1.05V
3. GFX_Mainon Enable +VCORE_GFX
4. GFX_VCORE_PG Enable(Delay) +1.5V_GFX
5. +1.5V_GFX Enable +1.8V_GFX
6. GFX_V18_PG connect GFX_PG

Power Off Sequence
compare +VCC3_GFX with +V1.8_GFX

Quanta Computer Inc.			
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	+VGACORE(ISL95870AHRUZ-T)		1A
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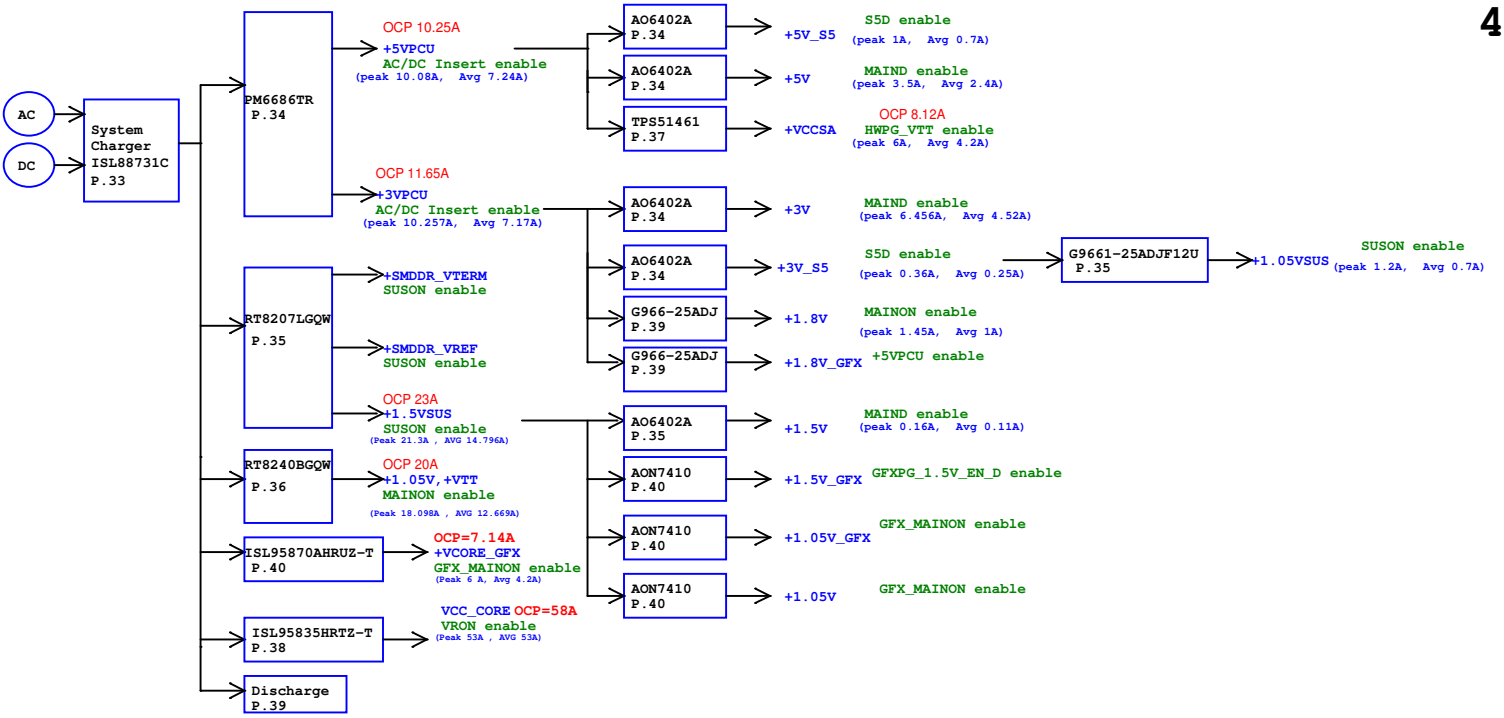

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