

ZZZ1



PCB

Compal Confidential

KAWGO Schematics Document

AMD S1g1 / RS690MC / SB600

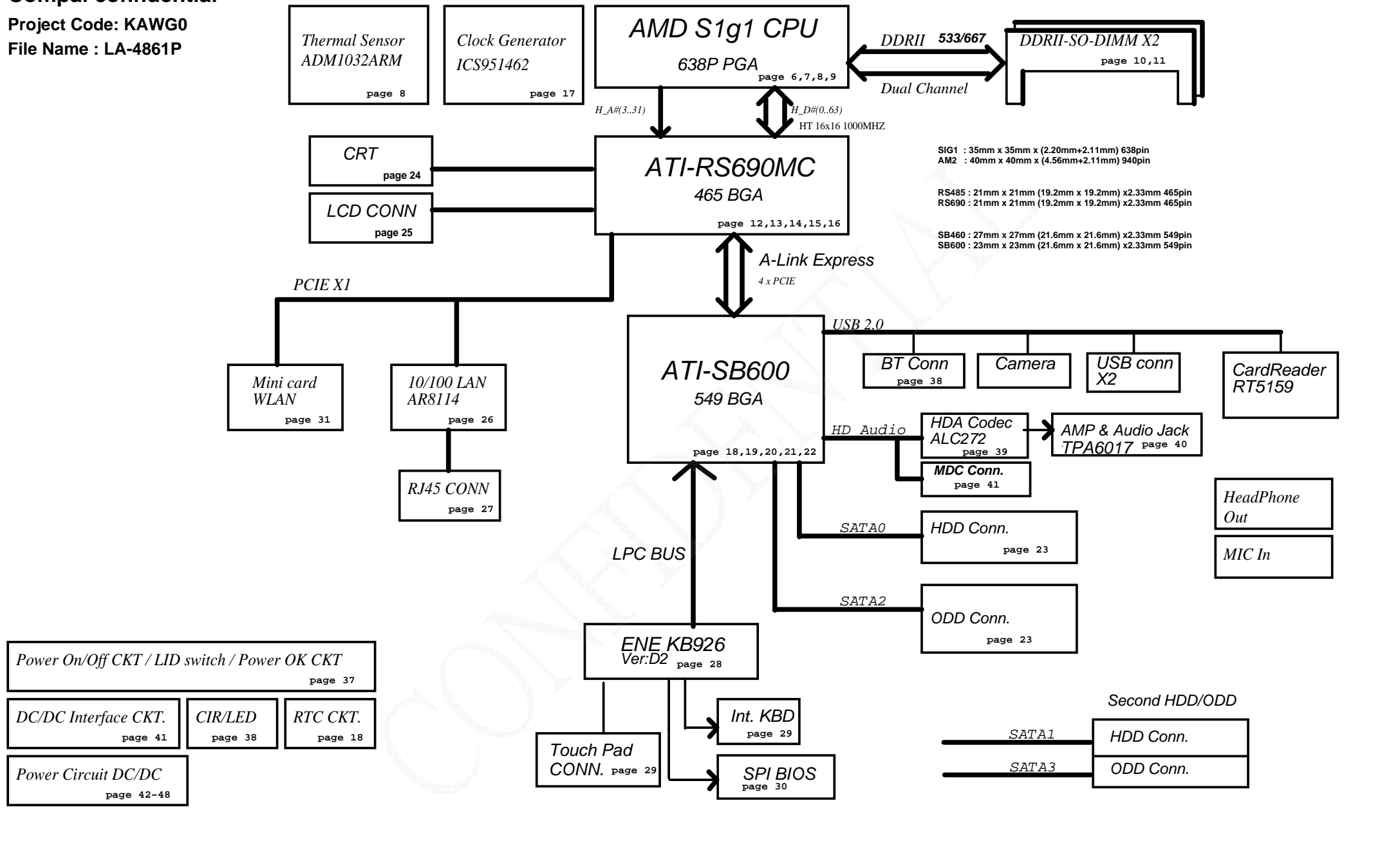
2009 / 04 / 09

Rev:1.0

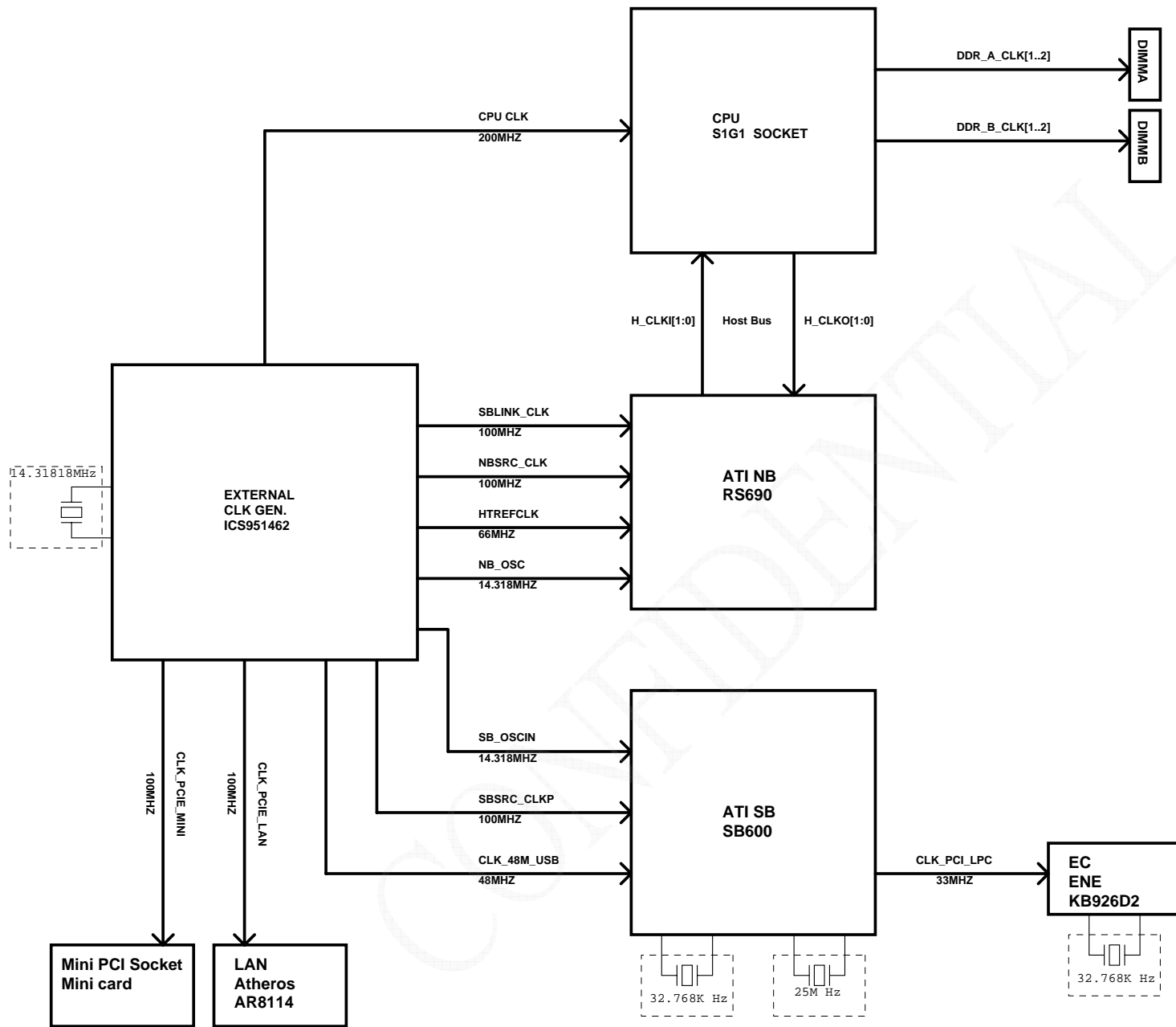
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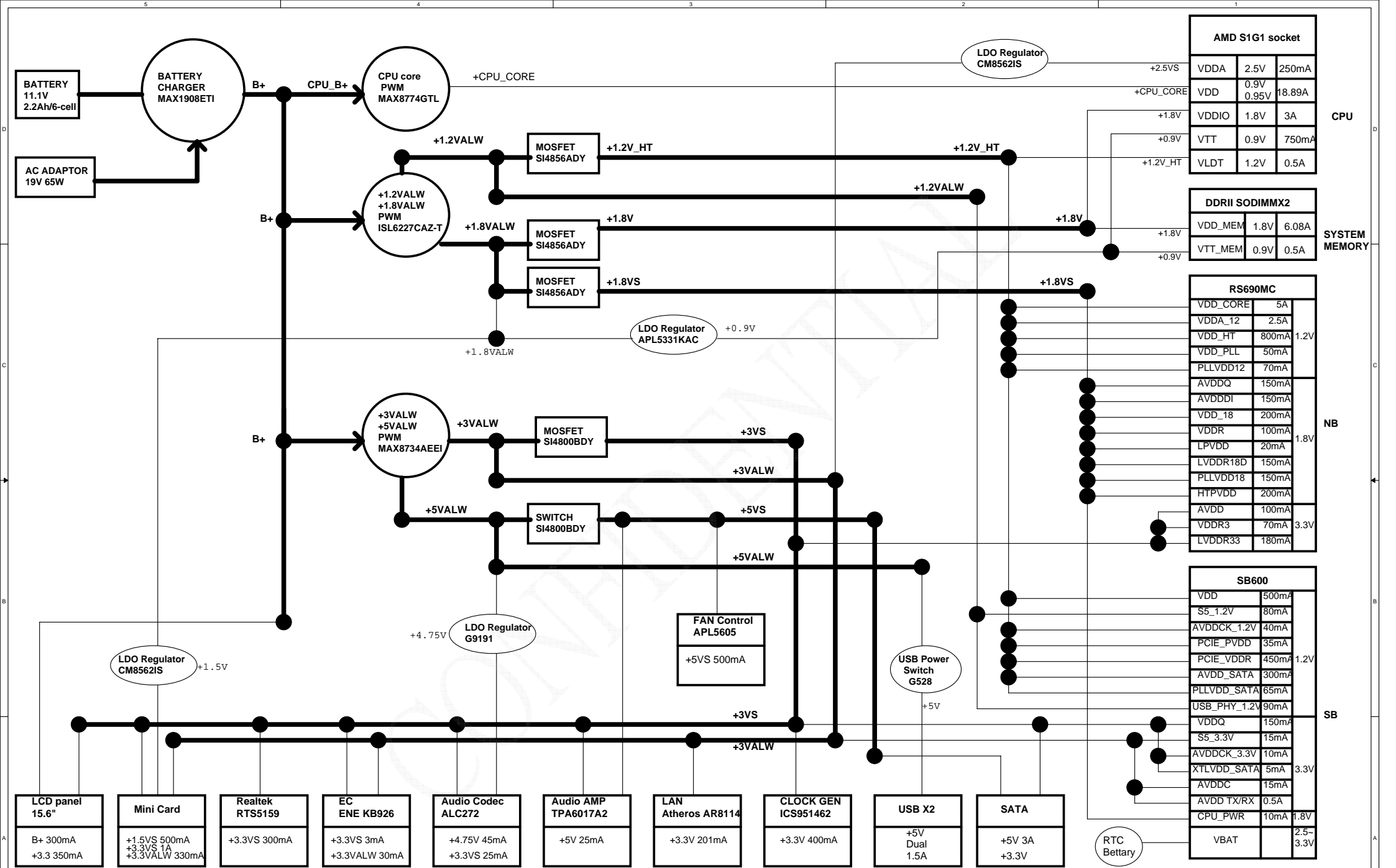
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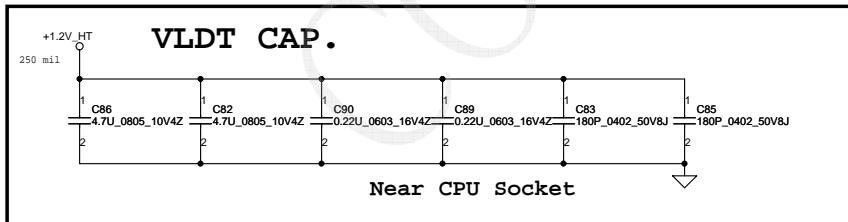
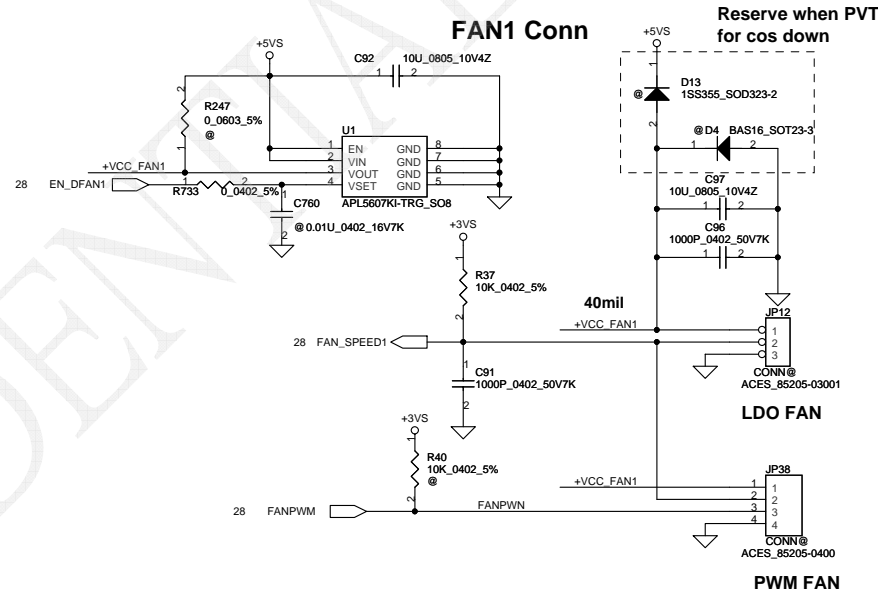
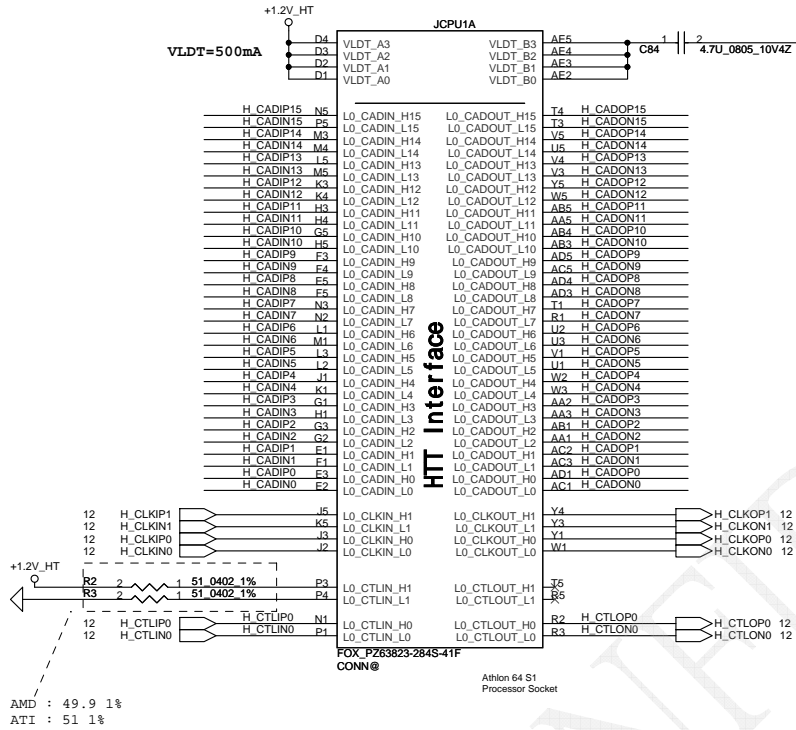


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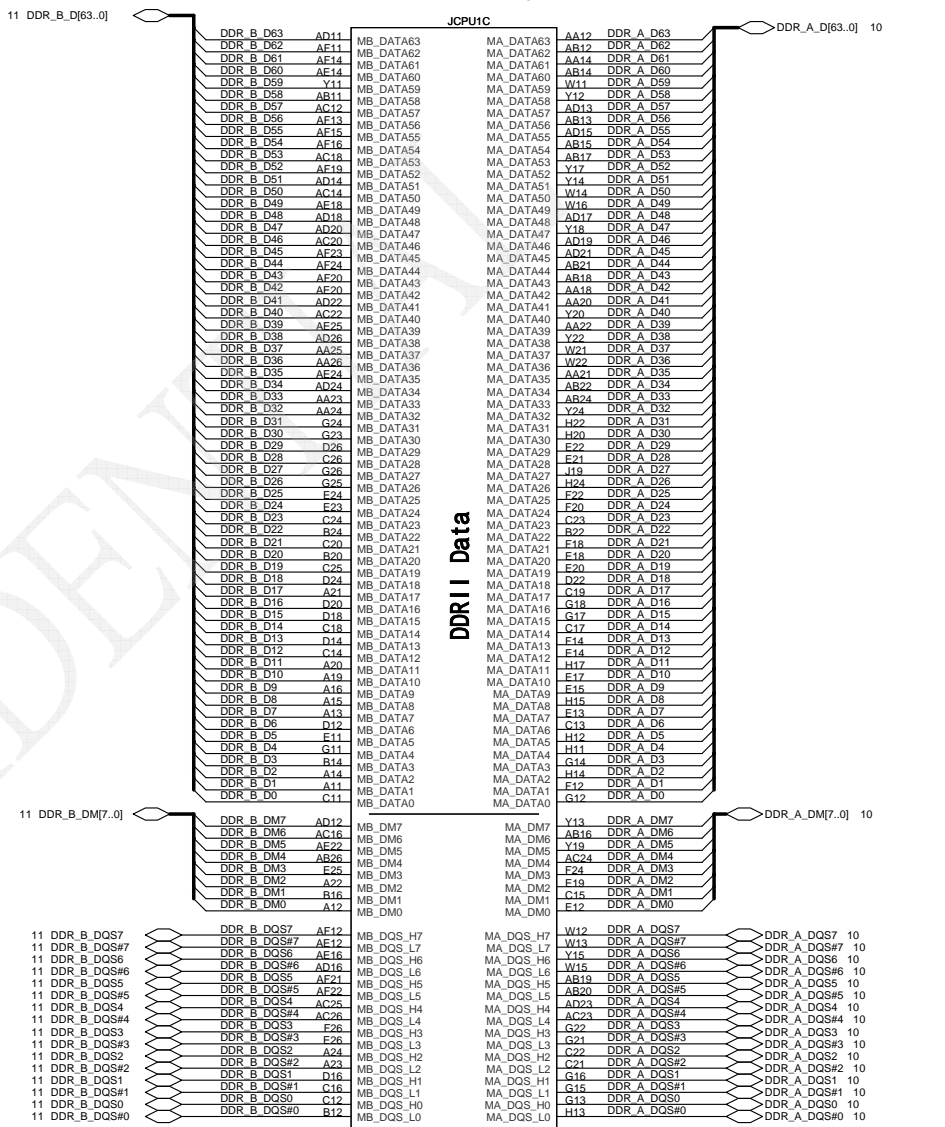
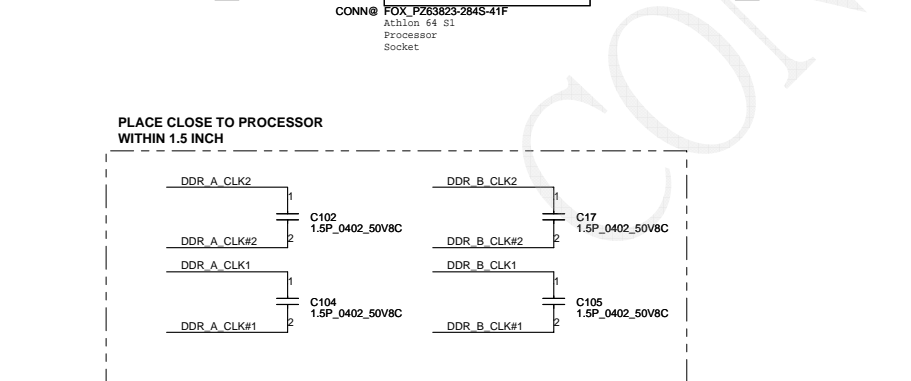
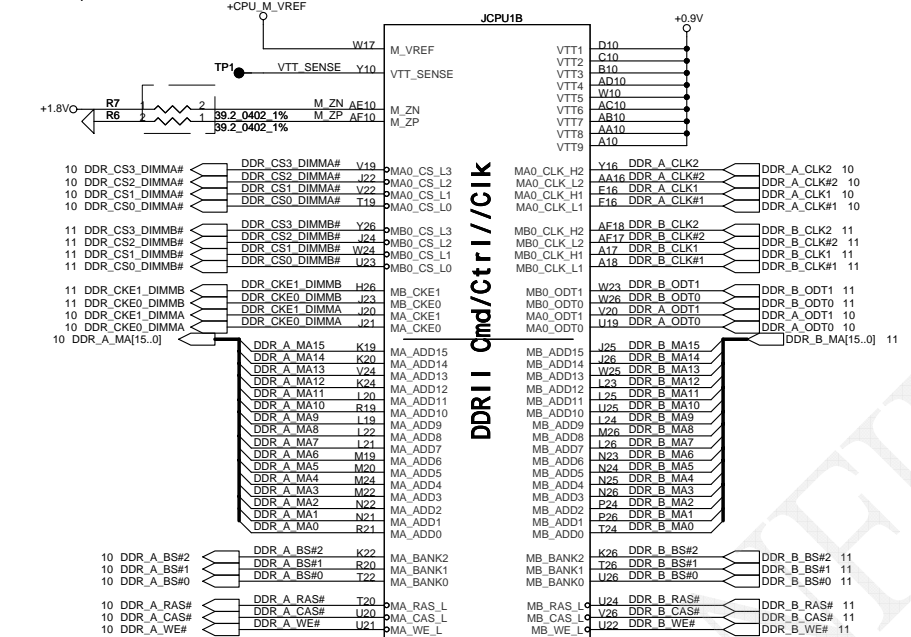
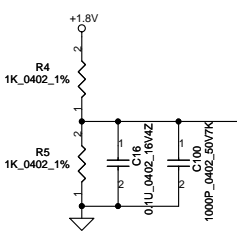
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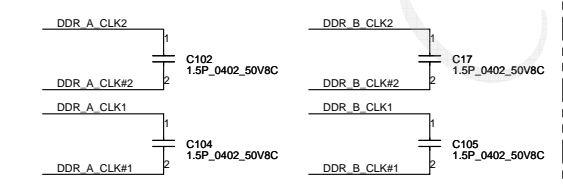


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Processor DDR2 Memory Interface

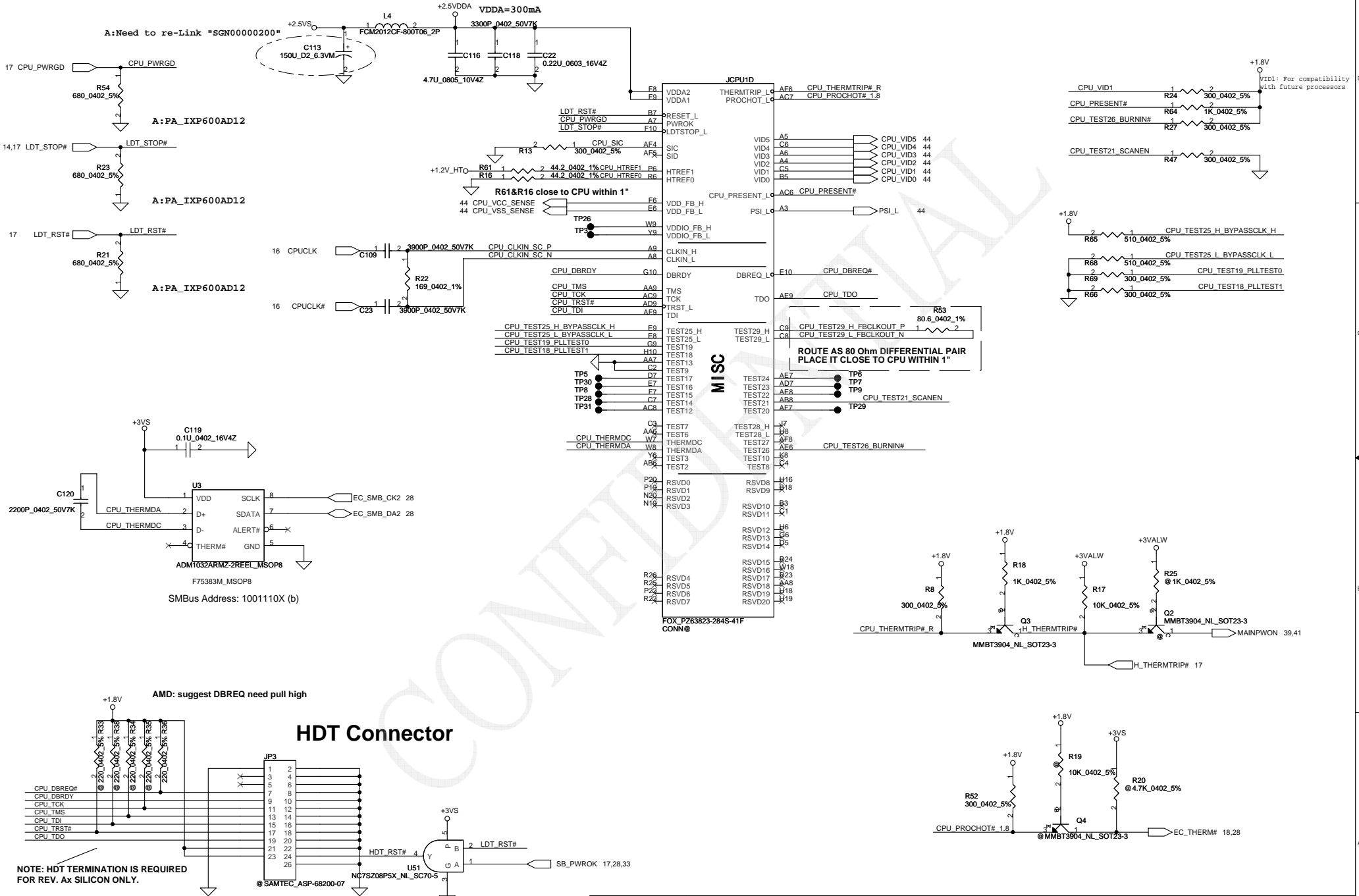


PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH



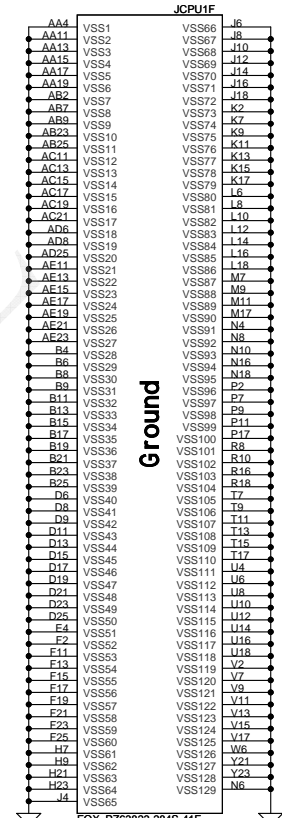
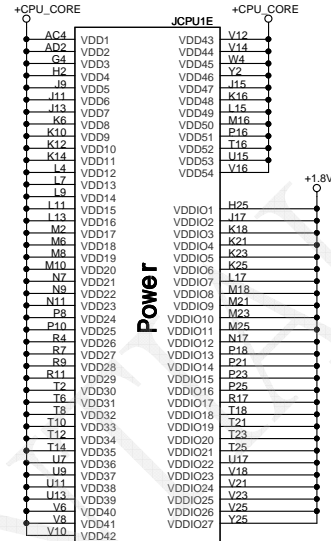
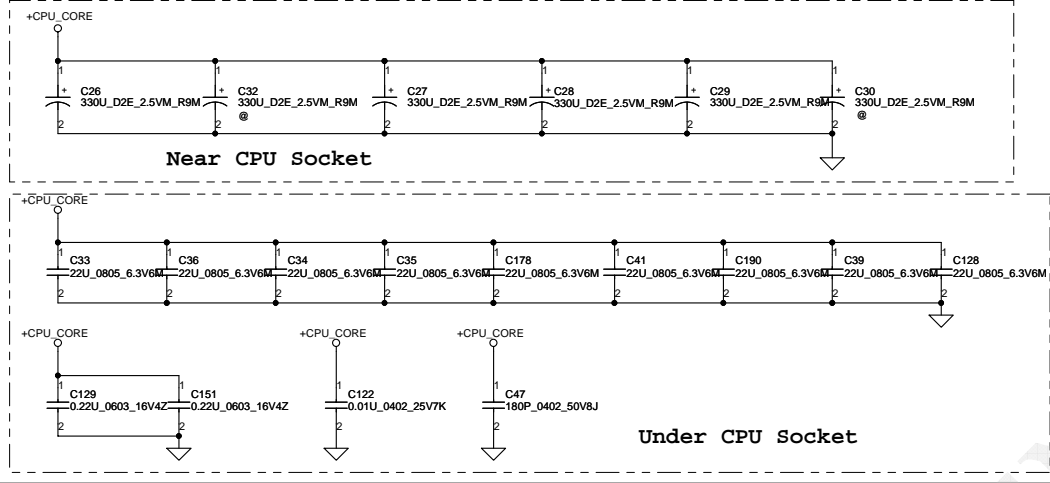
CONN@ FOX_P263823-284S-41F
Athlon 64 S1
Processor Socket

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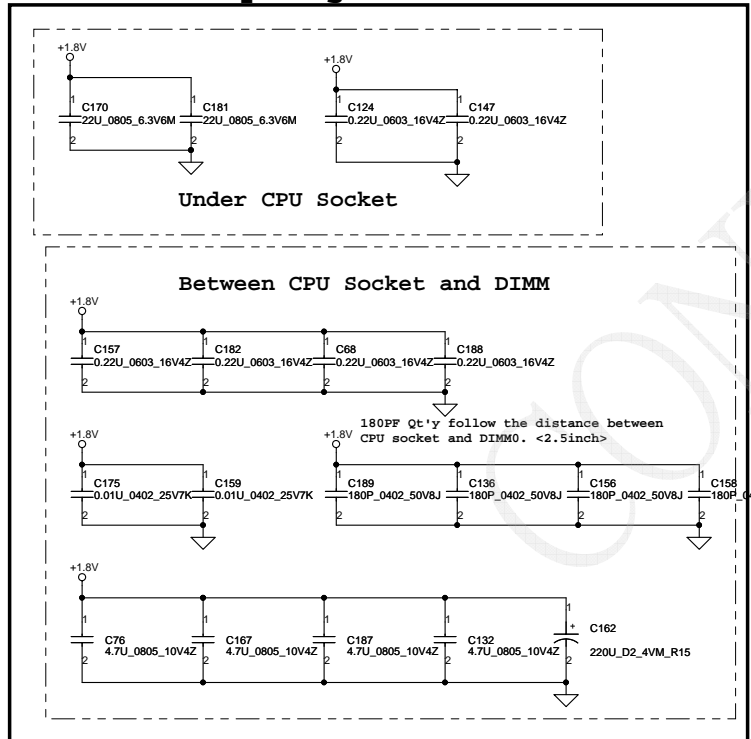
VDD(+CPU_CORE) decoupling.



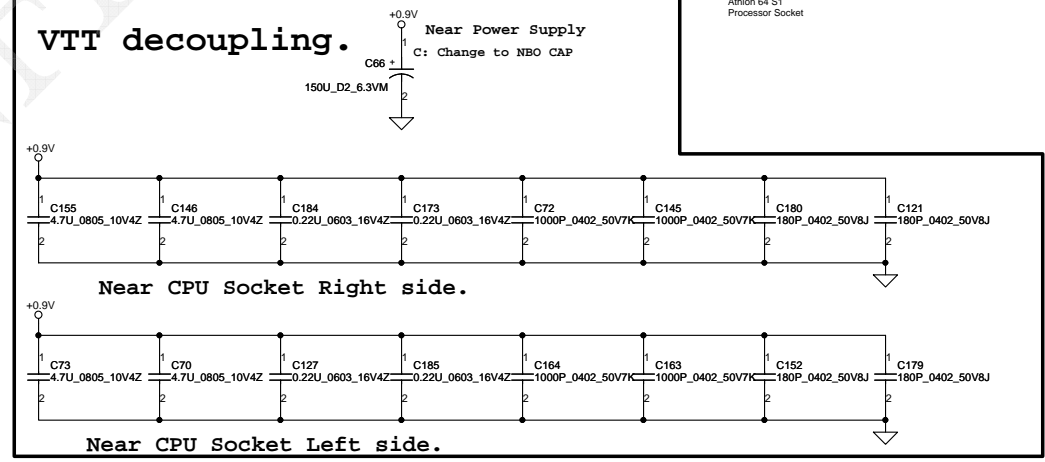
FOX_P263823-284S-41F
CONN@
Athlon 64 S1
Processor Socket

FOX_P263823-284S-41F
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Athlon 64 S1
Processor Socket

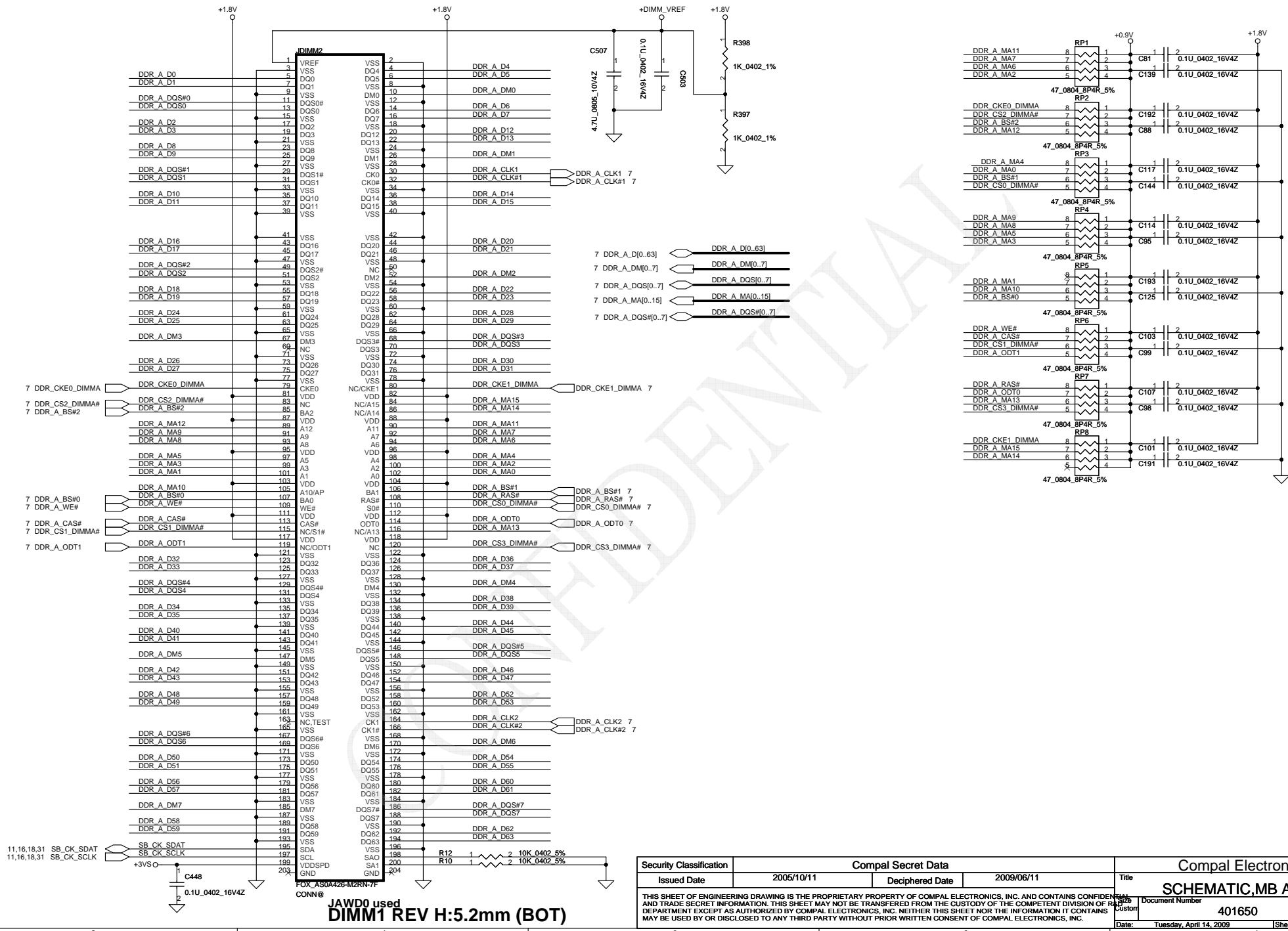
VDDIO decoupling.



VTT decoupling.

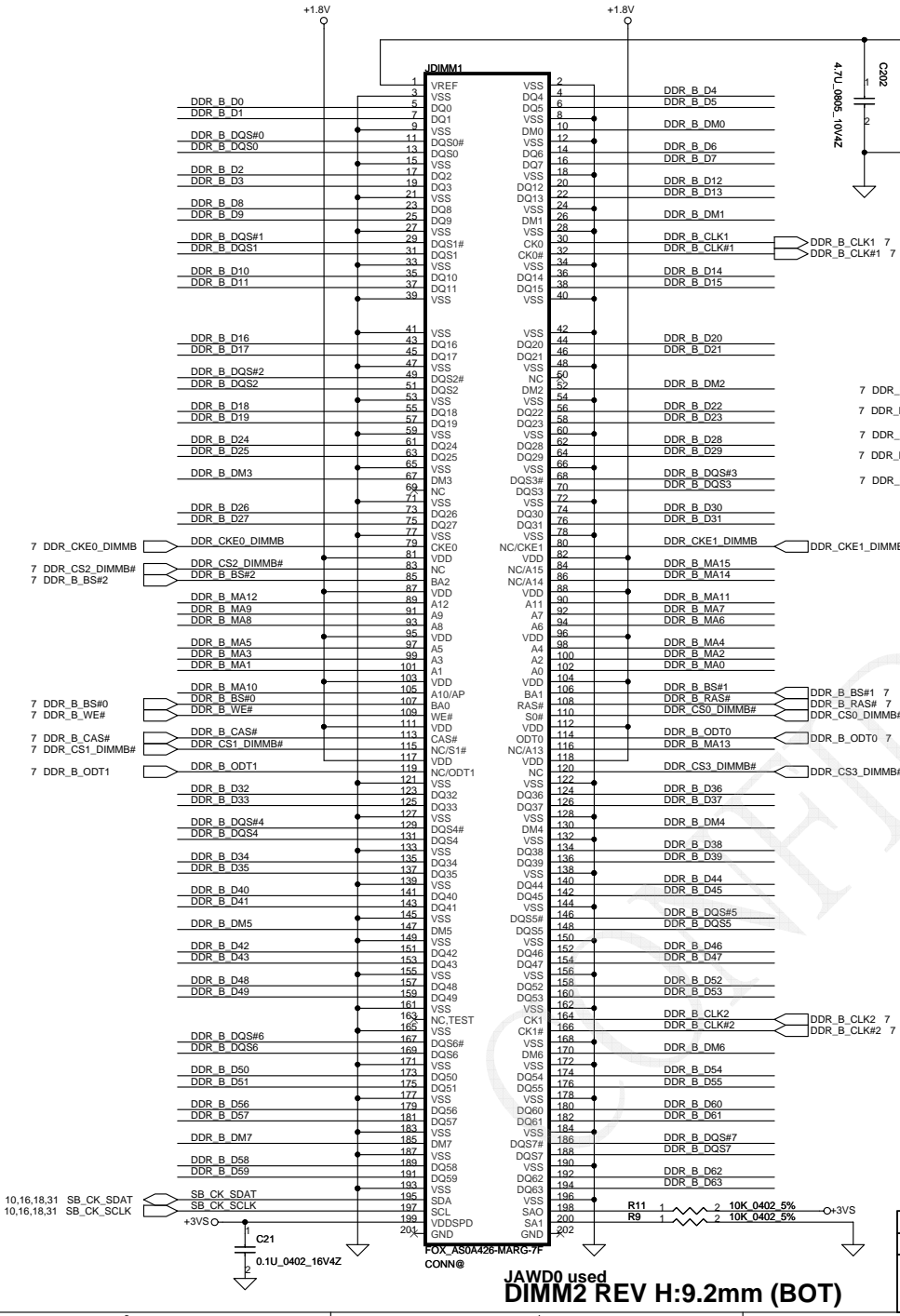


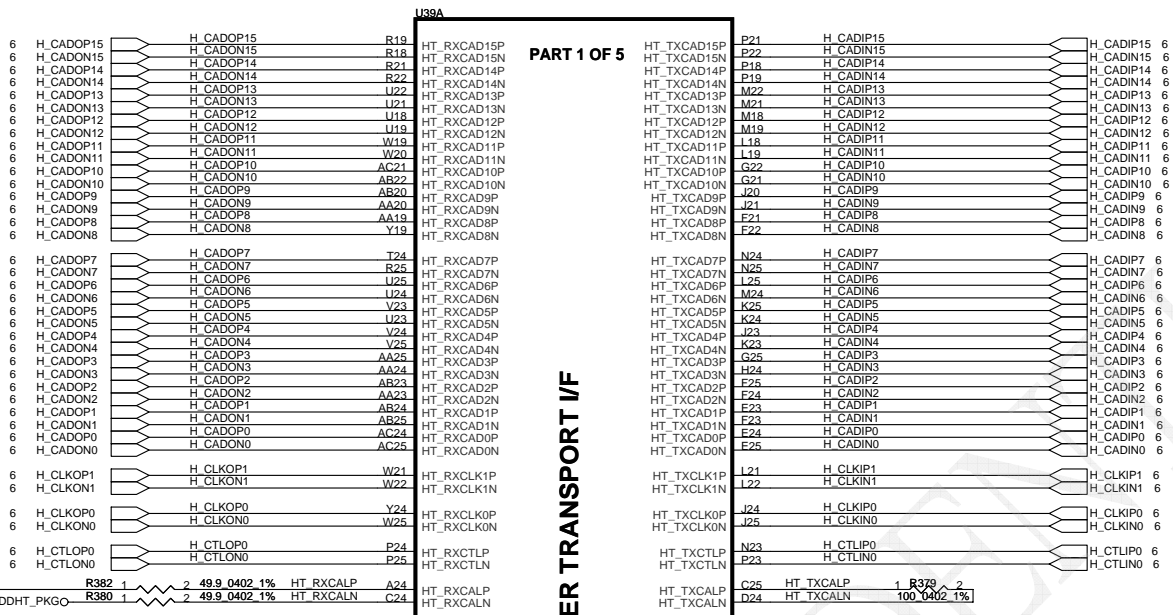
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**JAWD0 used
DIMM1 REV H:5.2mm (BOT)**

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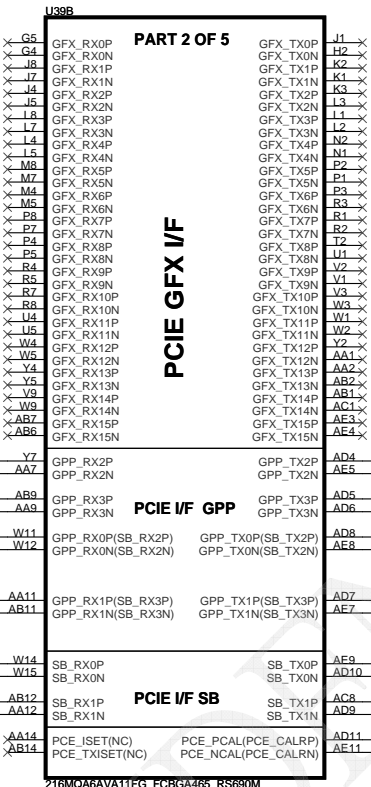




216MQA6AVA11FG_FCBGA666_RS690M

RS690MC : SA00011480 / S IC 216LQA6AVA12FG RS690MC BGA 465P 0FA

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WLAN

LAN

A-Link

WLAN

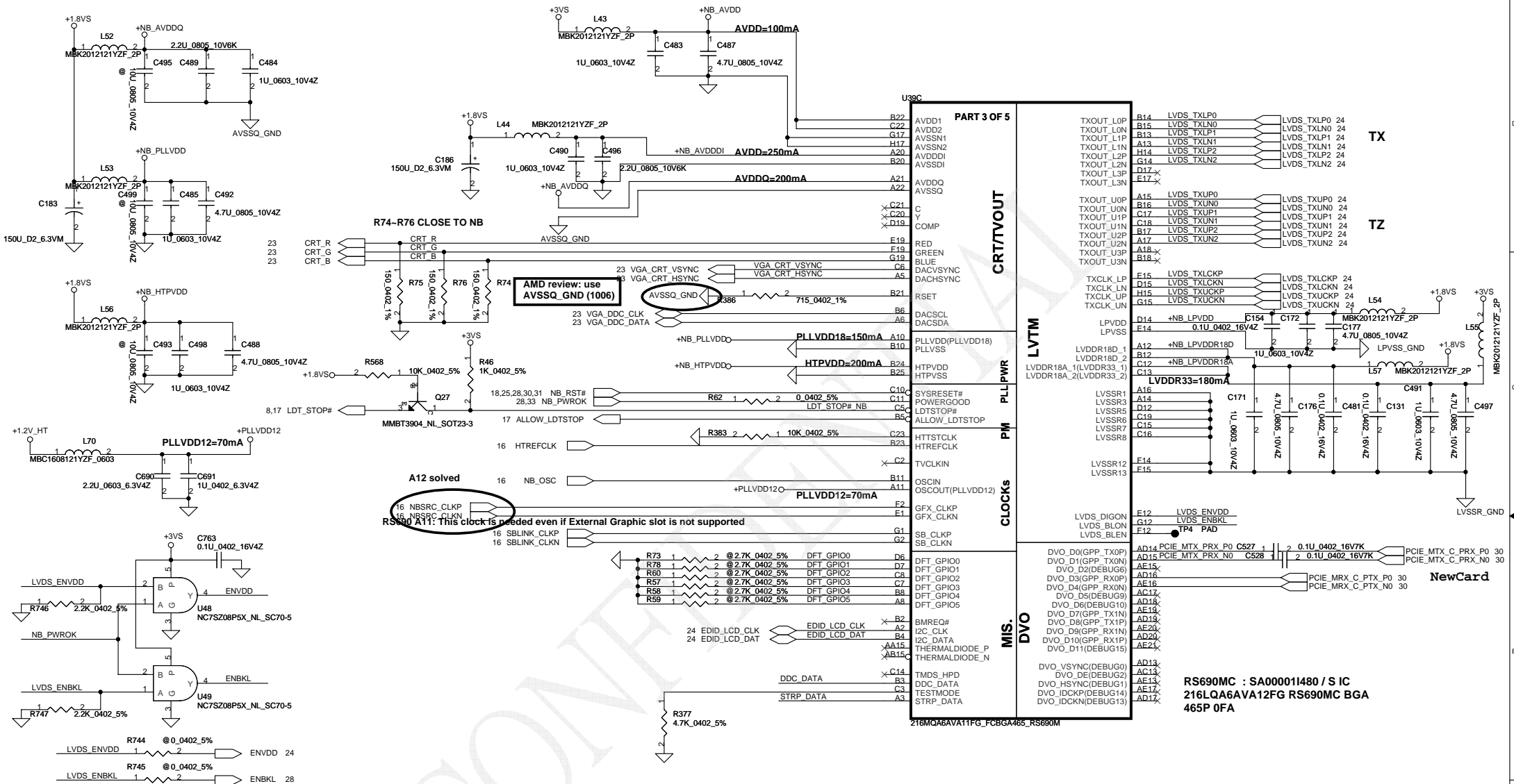
LAN

A-Link

R375: 150 Ohm FOR RS485
562 Ohm FOR RS690
R376: 82.5 Ohm FOR RS485
2K0hm FOR RS690

RS690MC : SA00001I480 / S IC 216LQA6AVA12FG RS690MC BGA 465P 0FA

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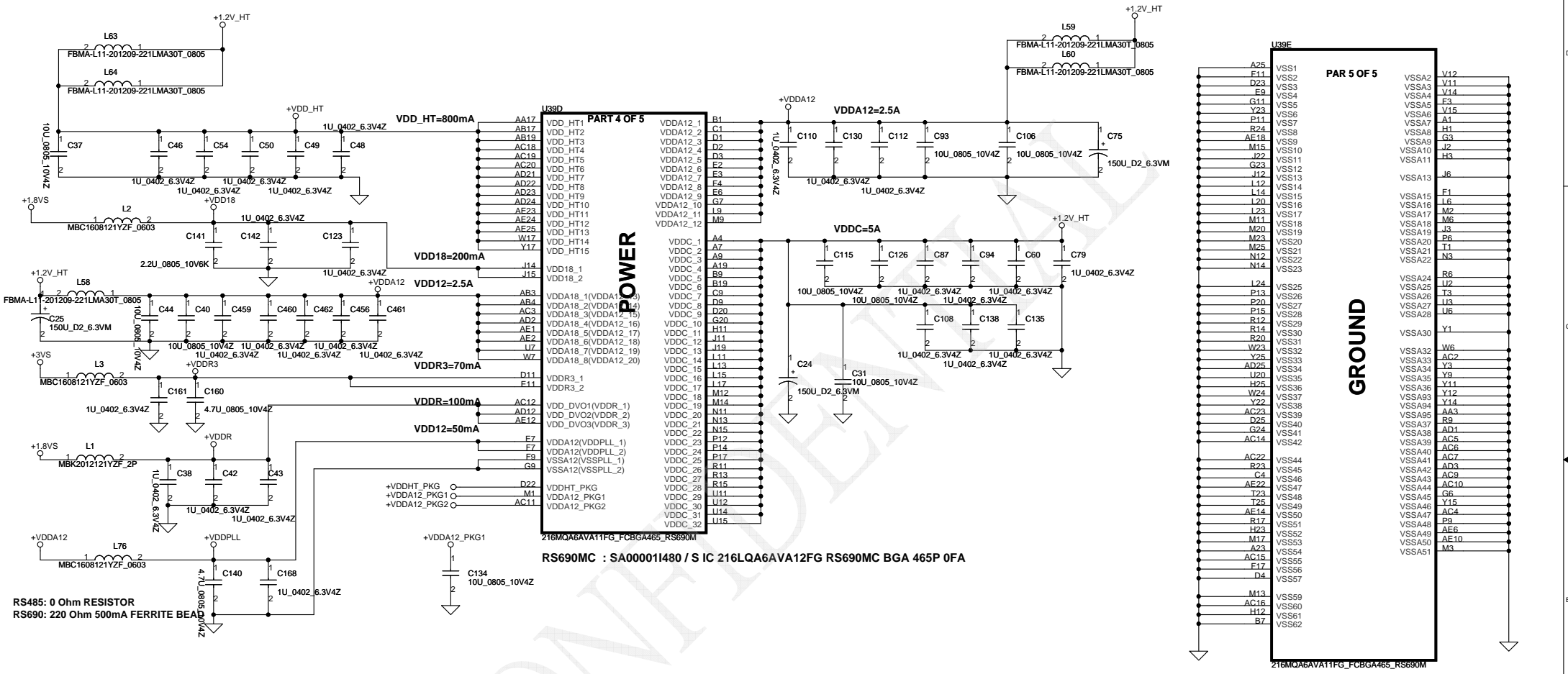


RS690		RS690 only	
PULL HIGH (internally pulled high)	DFT_GPIO0	DFT_GPIO1	DFT_GPIO[4:2]
Memory side port not available	Not available	Bypass the loading of EEPROM straps and use Hardware default values	These pin straps are used to configure PCI-E GPP mode: 111: register defined (register default to Config E) 110: 4-0-0-0 Config A 101: 4-4 Config B 100: 4-2-2 Config C 011: 4-2-1-1 Config D 010: 4-1-1-1 Config E
PULL LOW	Memory side port available	I2C Master can load strap values from EEPROM if connected, or use default values if not connected	others: register defined (register default to Config E)
			Enable debug bus via the memory IO pads, if available in the package use default values use the memory data bus to output the debug bus

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STRP_DATA set PowerPlay mode PWM output: won't support

RS690MC : SA000011480 / S IC
216LQA6A1V2FG RS690MC BGA
465P 0FA

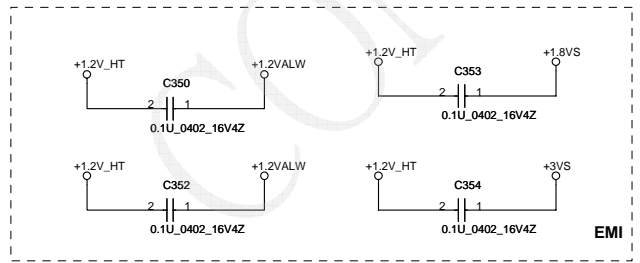


RS485: 0 Ohm RESISTOR
RS690: 220 Ohm 500mA FERRITE BEAD

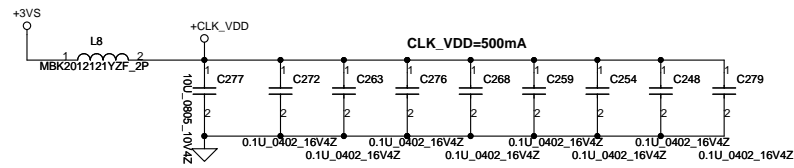
RS690MC : SA000011480 / S IC 216LQA6AVA12FG RS690MC BGA 465P 0FA

PAR 5 OF 5

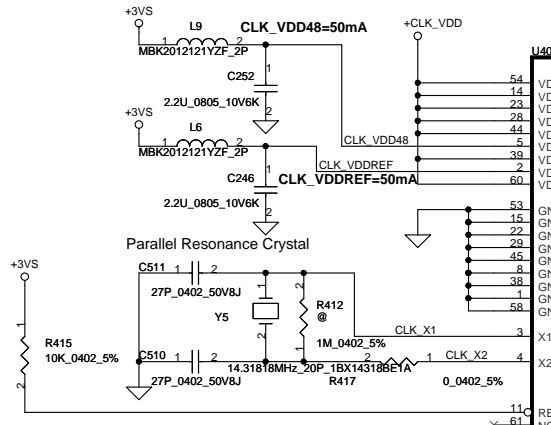
GROUND



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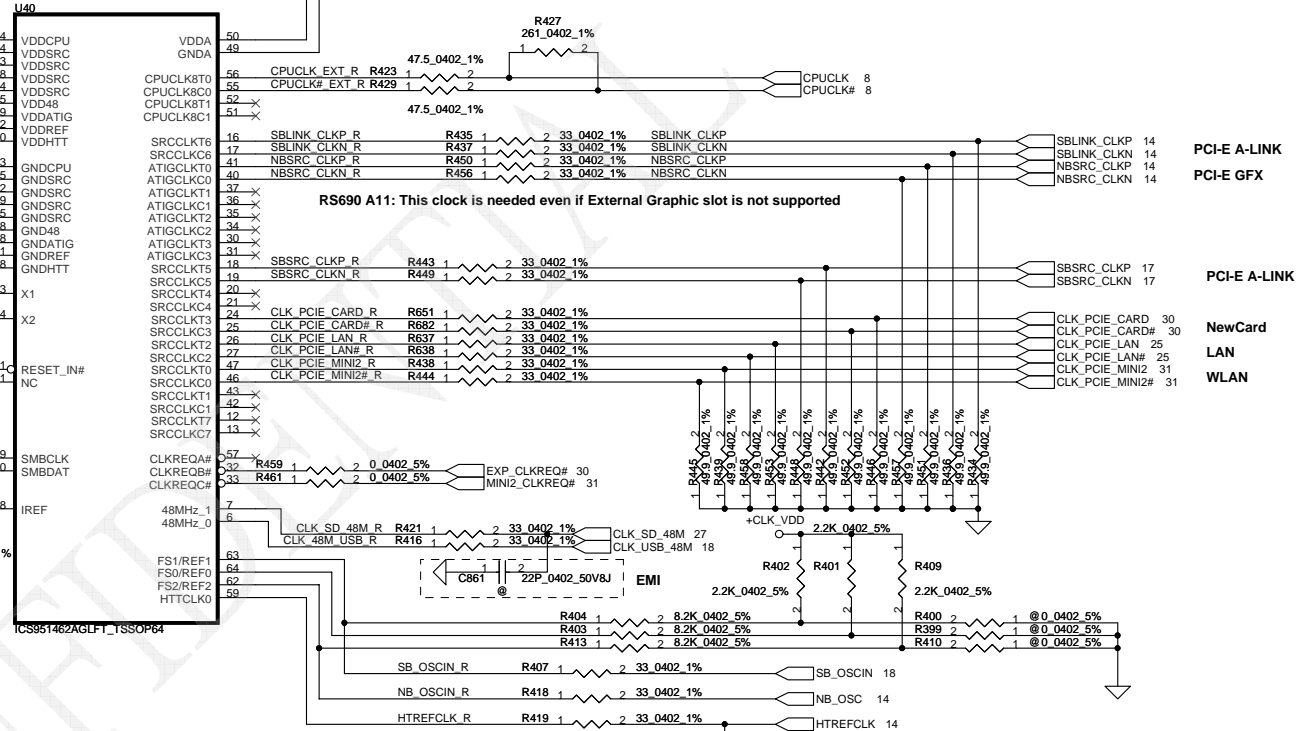
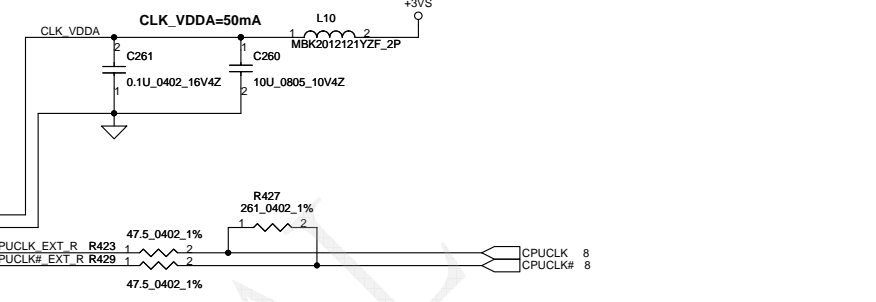


- 1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO U40
- 2- PUT DECOUPLING CAPS CLOSE TO U40 POWER PIN



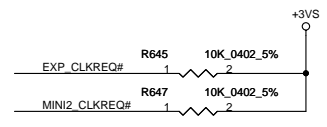
$$I_{oh} = 5 * I_{ref} \text{ (2.32mA)}$$

$$V_{oh} = 0.71V @ 60 \text{ ohm}$$

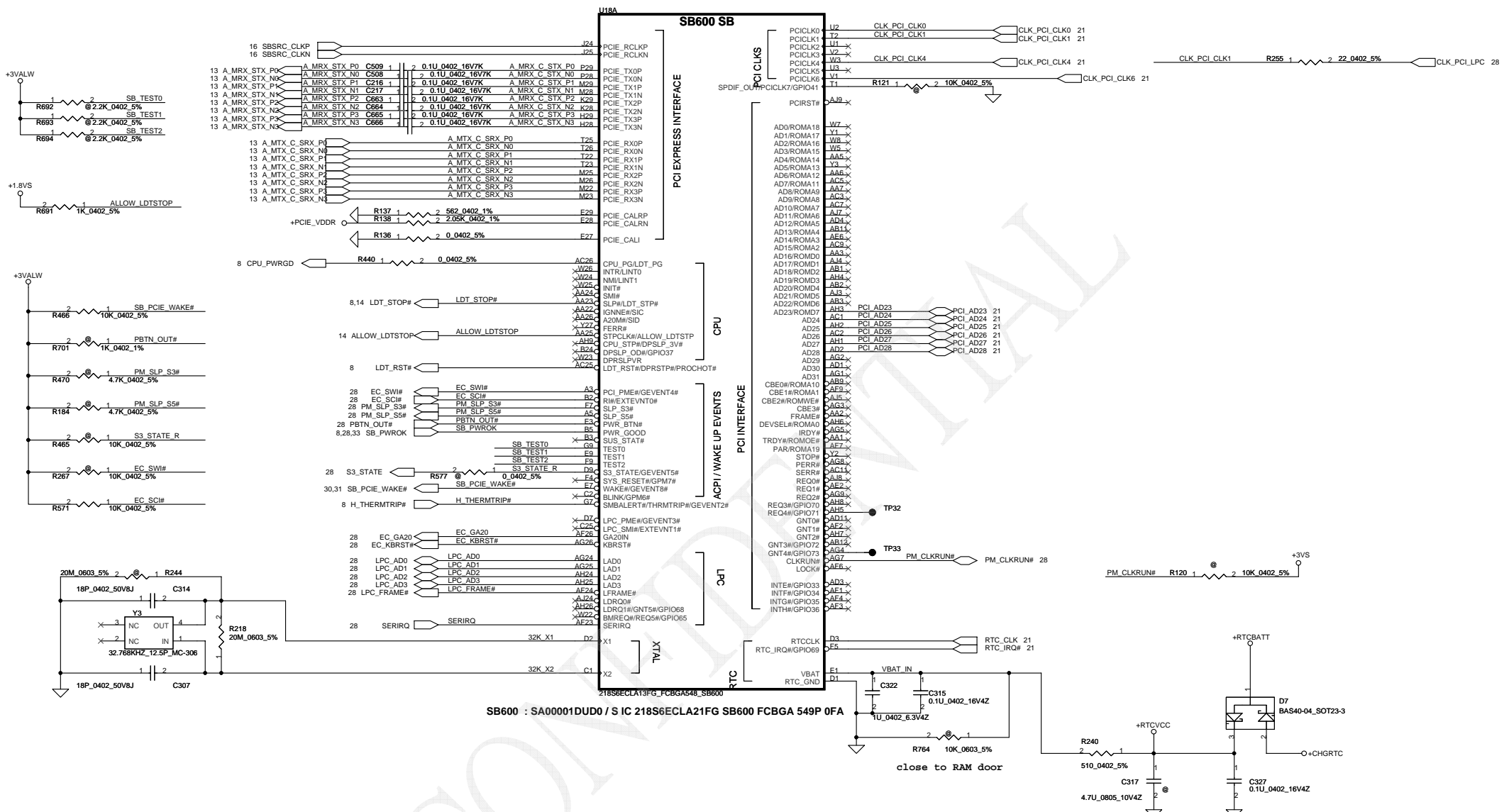


EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation



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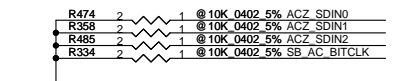
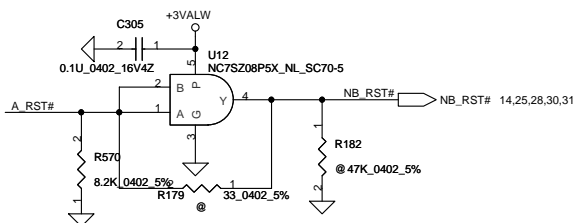
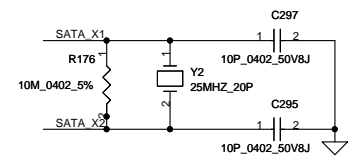


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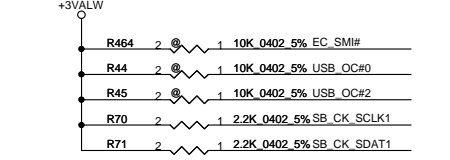
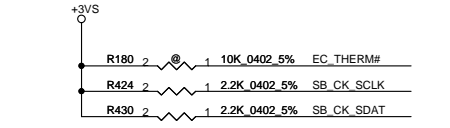
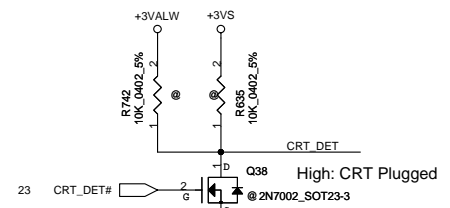
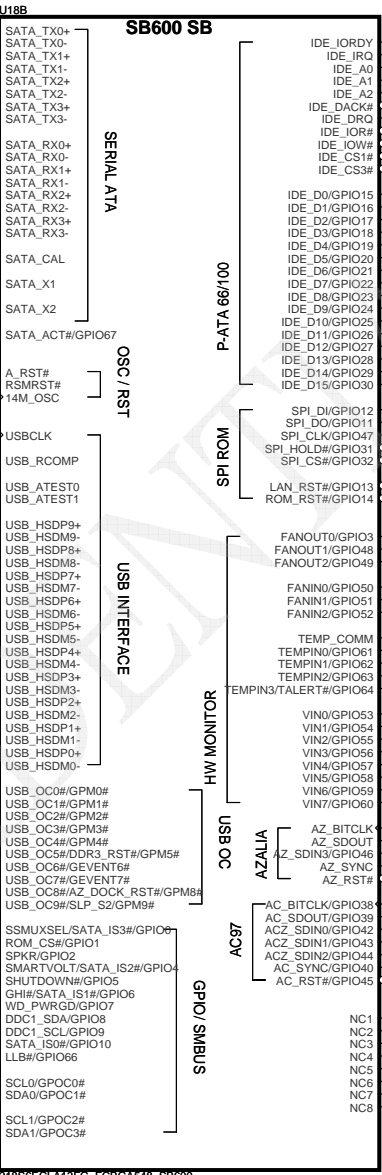
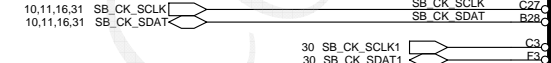
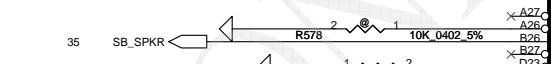
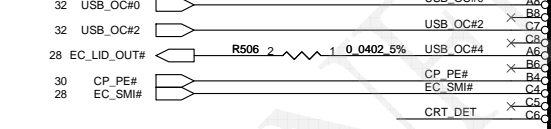
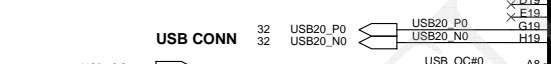
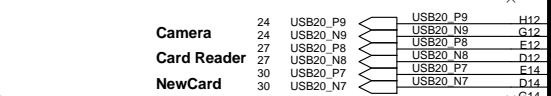
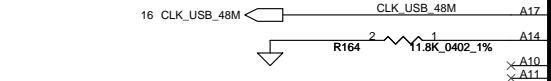
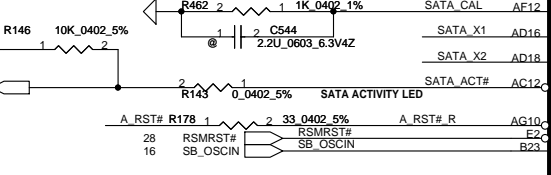
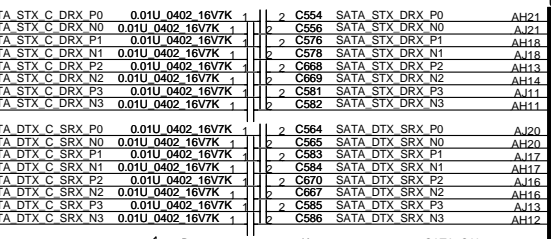
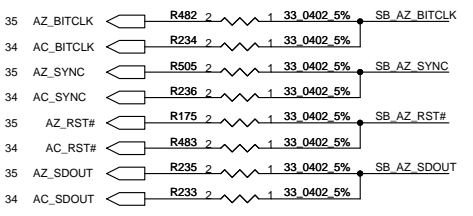
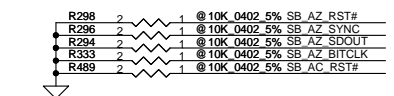
NOTE:
 R462 IS 1K 1% FOR
 25MHz XTAL, 4.99K 1%
 FOR 100MHz INTERNAL
 CLOCK

PLACE SATA AC COUPLING
 CAPS CLOSE TO CONN.

PORT0 : MAIN HDD
PORT1 : SECOND HDD
PORT2 : MAIN ODD
PORT3 : SECOND ODD

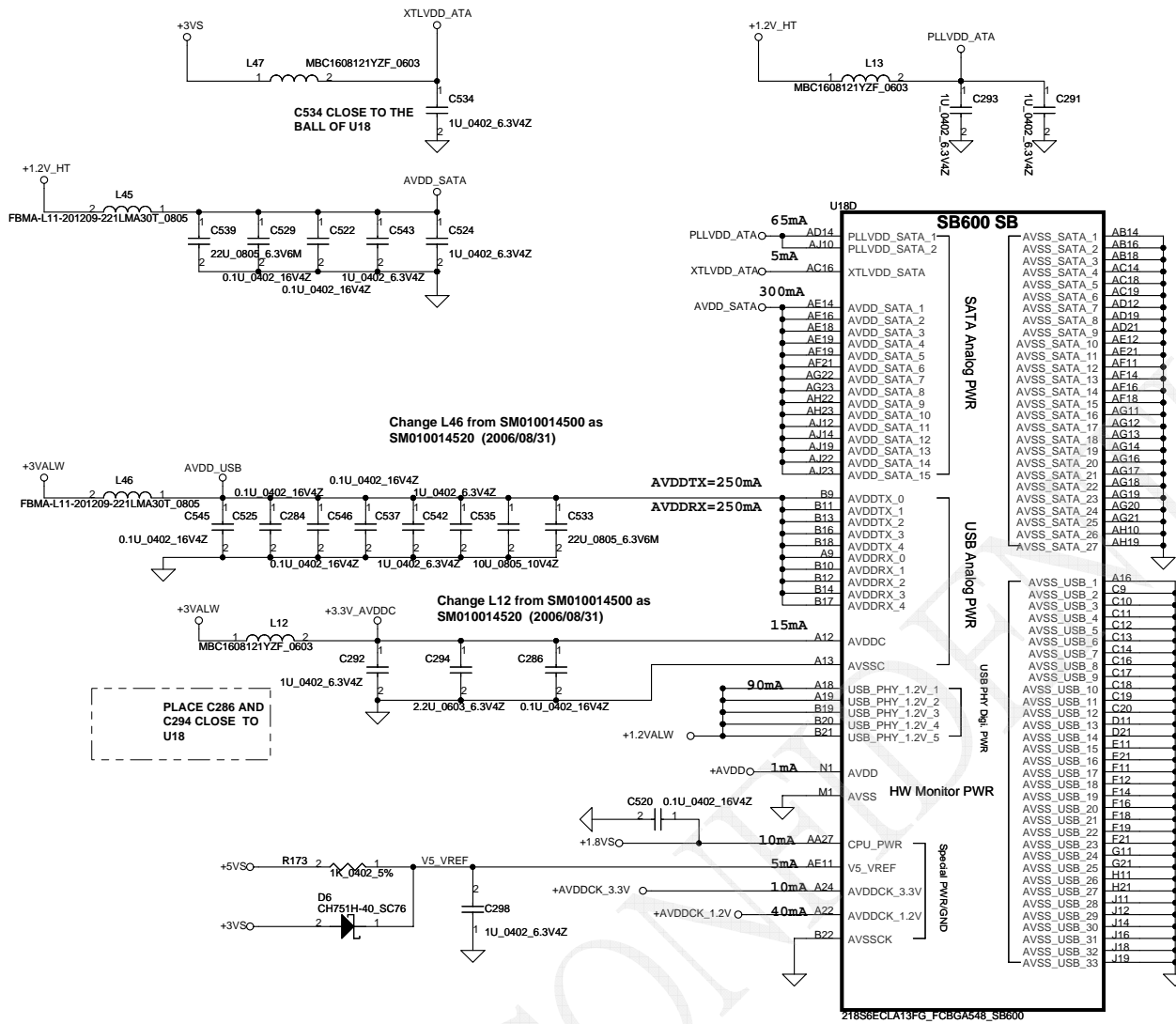


SB600 A21 and newer: Made provision for an external 10-kohm 5% pull-down resistor, not installed by default.



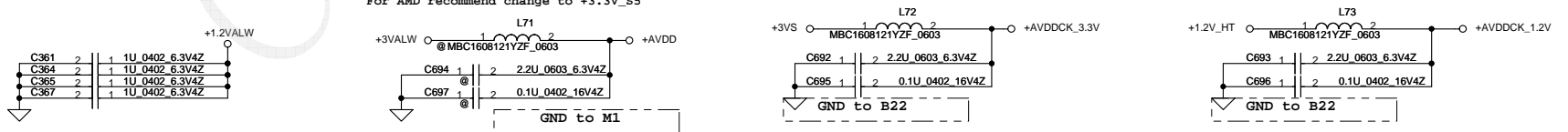
SB600 : SA00001DUD0 / S IC 218S6ECLA21FG SB600 FCBGA 549P 0FA

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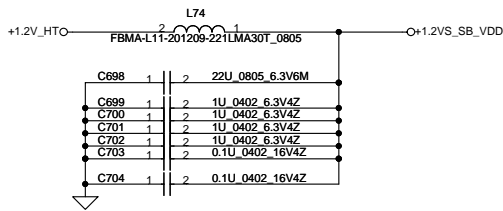
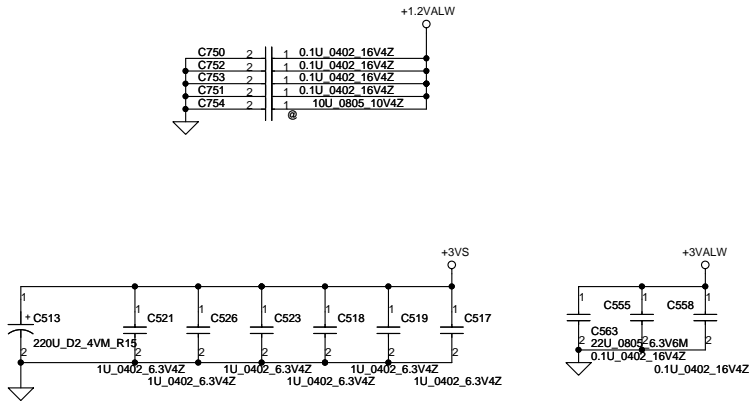


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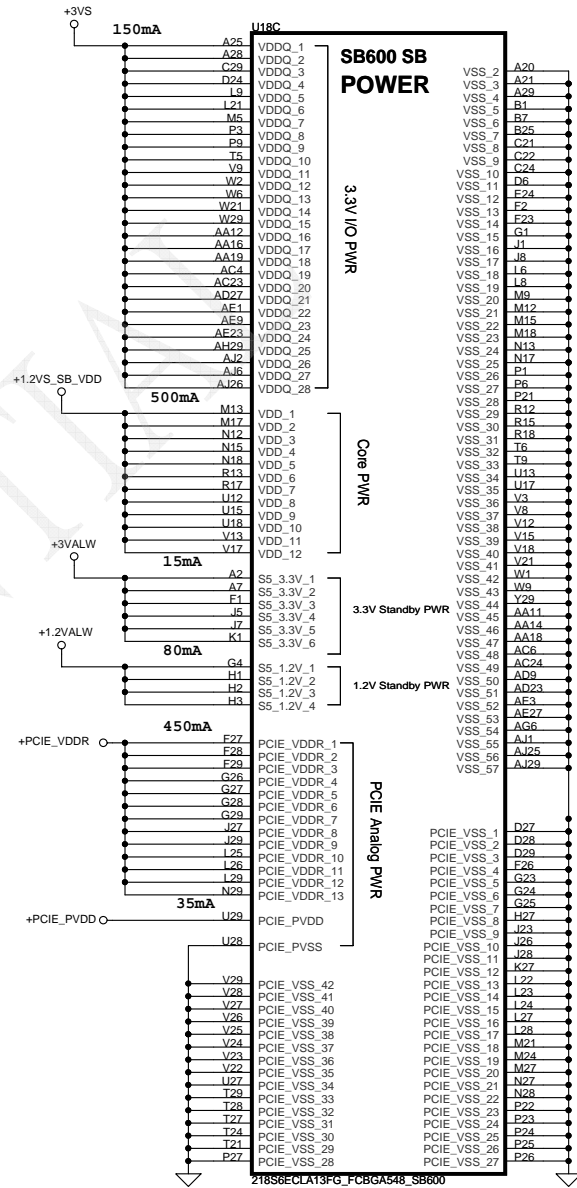
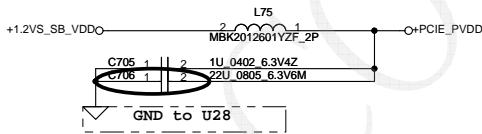
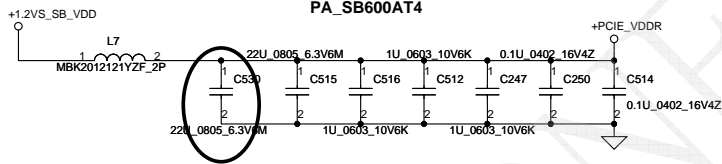
For AMD recommend change to +3.3V_S5



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Delay PCIE_VDDR / PCIE_PVDD
Add C530 to 22u
PA_SB600AT4

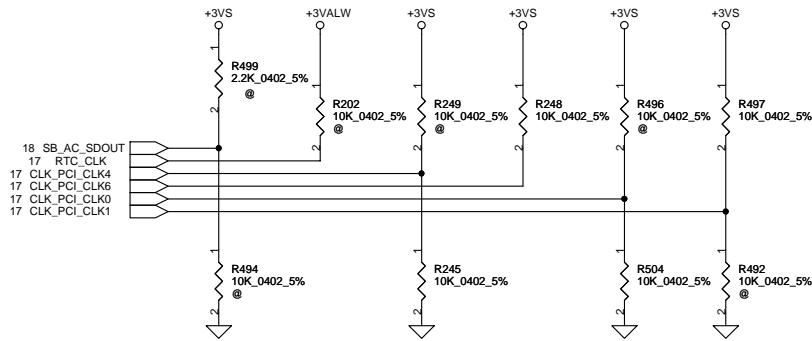


SB600 : SA00001DUD0 / S IC 218S6ECLA21FG SB600 FCBGA 549P 0FA

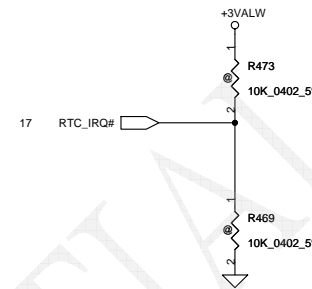
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REQUIRED STRAPS

SB600 HAS 15K INTERNAL PD FOR AC_SDOUT, 15K PU FOR RTC_CLK, EXTERNAL PU/PD IS NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE REQUIRED



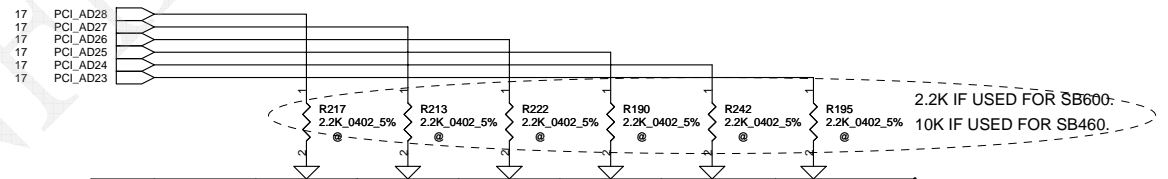
Internal RTC: Not connected. *
 External RTC: Connected to IRQ# pin on external RTC.
 External RTC supports S5 wake capability (from S5 power rail or battery).



	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4	DEFAULT	

DEBUG STRAPS

SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	IDE_DACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
PULL LOW	USE SHORT RESET	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

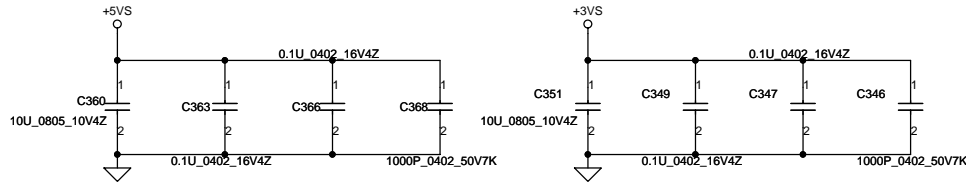
SB600 ONLY

NOTE: FOR SB460, PCI_AD23 IS RESERVED

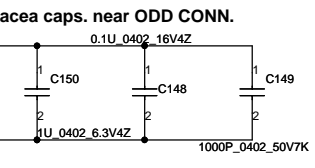
SB460 ONLY

SB600 ONLY

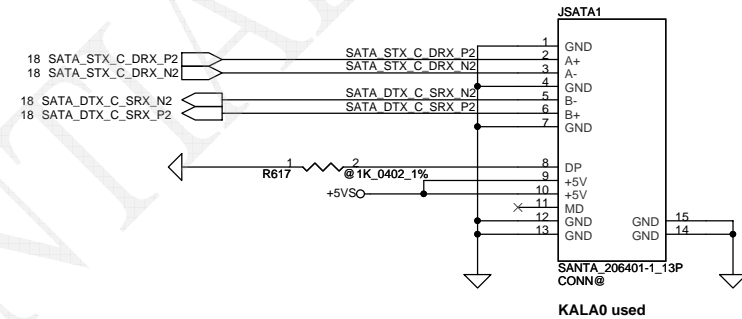
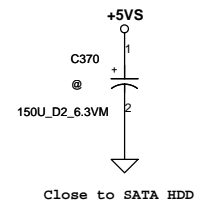
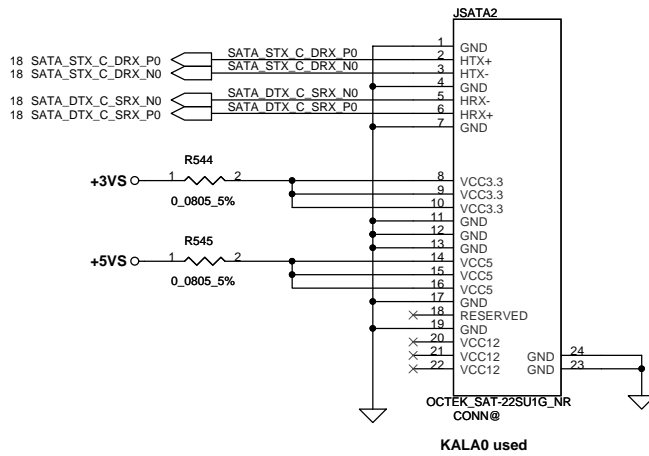
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SATA HDD CONN

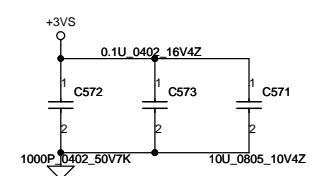
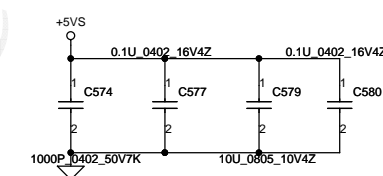
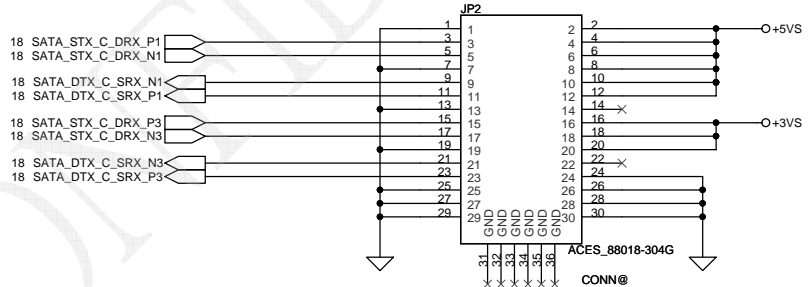


SATA ODD CONN



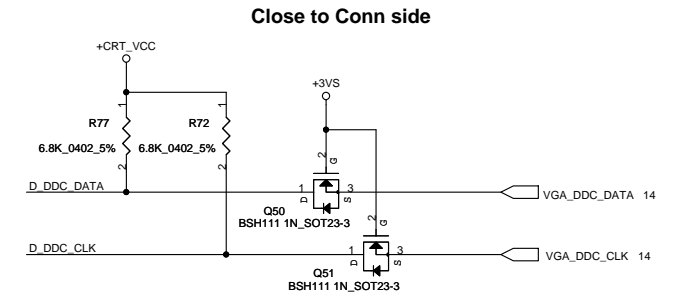
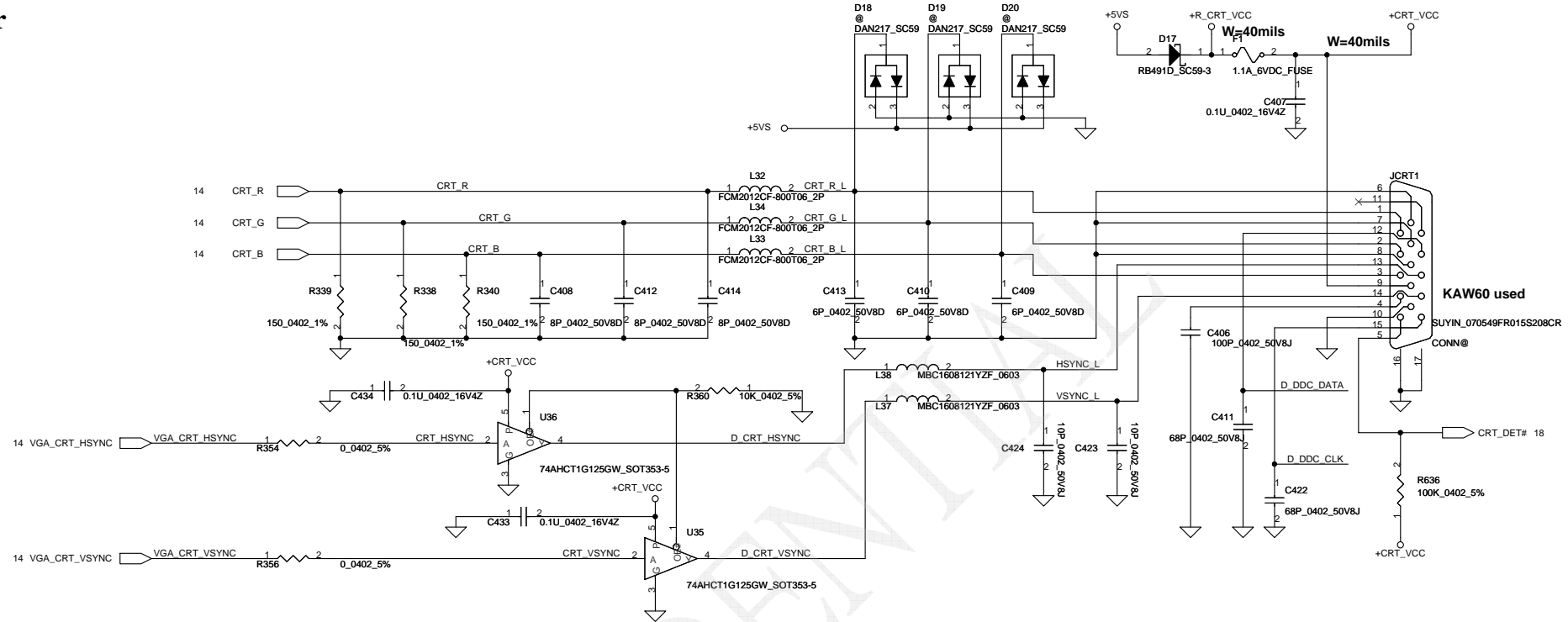
Second HDD

Second ODD



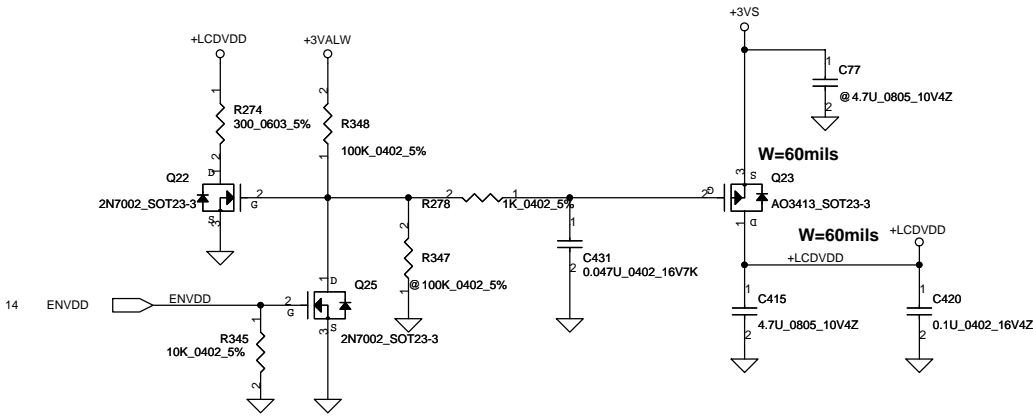
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CRT Connector

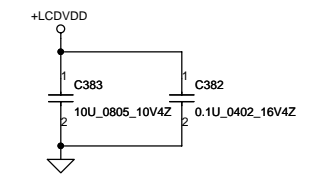
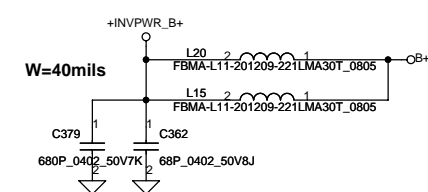
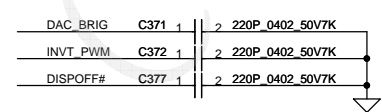
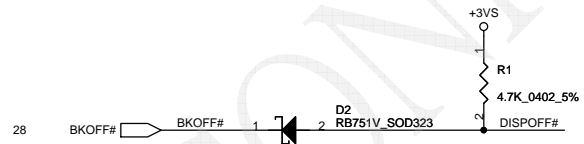
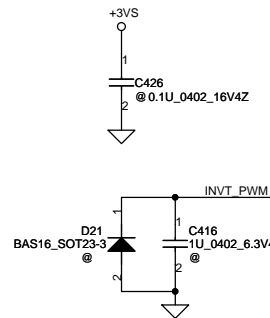
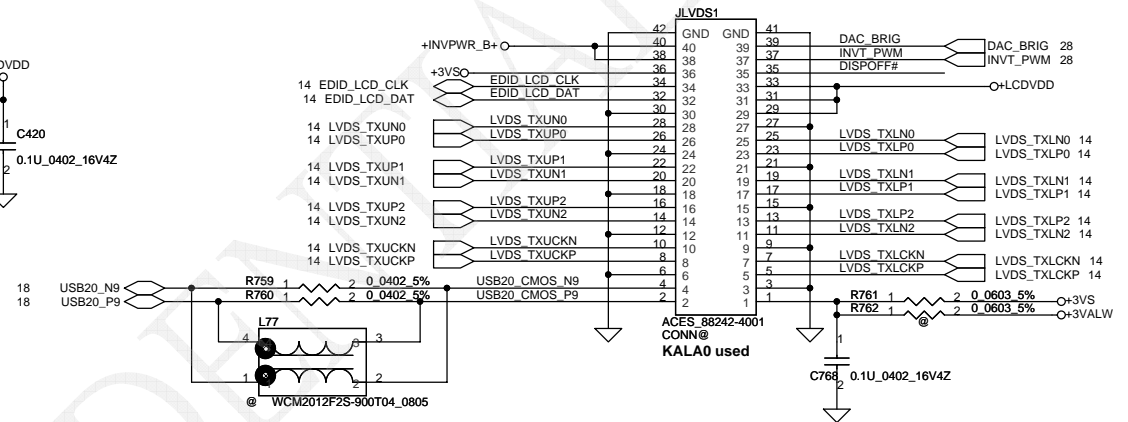


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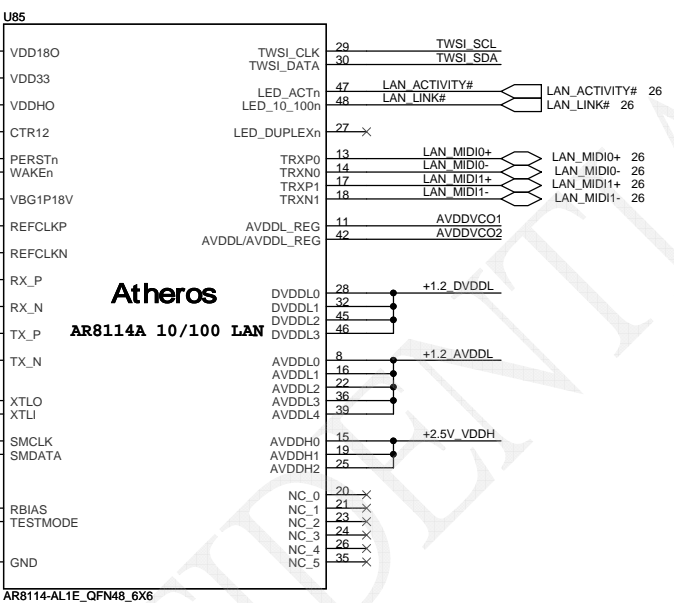
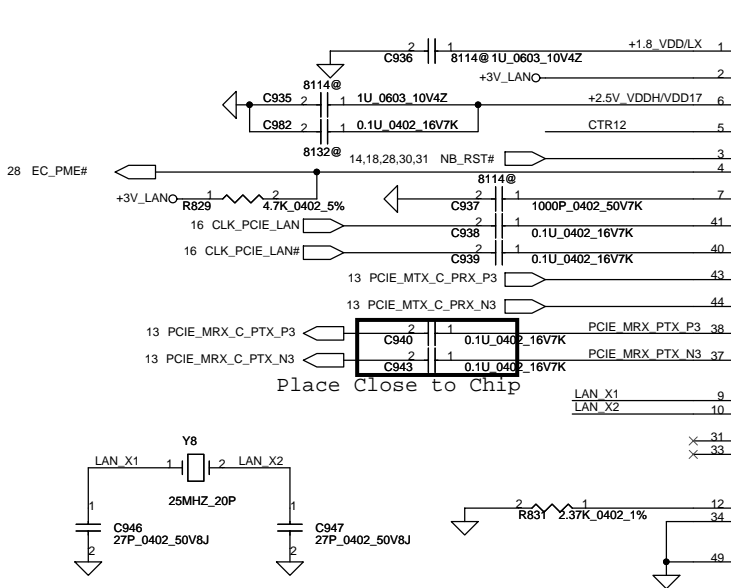
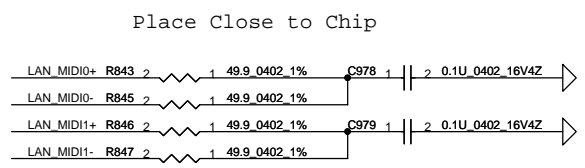
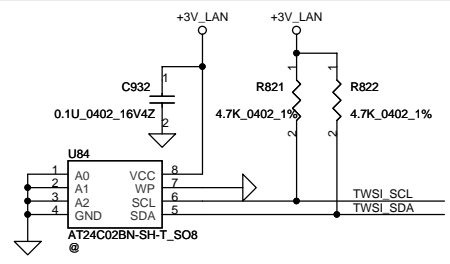
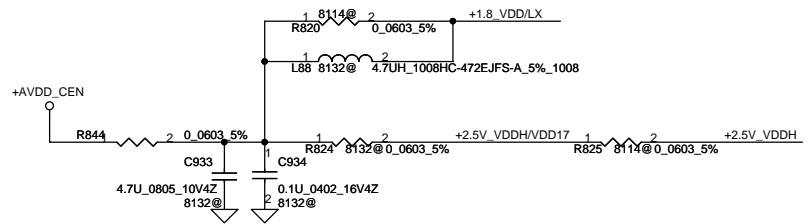
LCD POWER CIRCUIT



LCD/PANEL CONN.



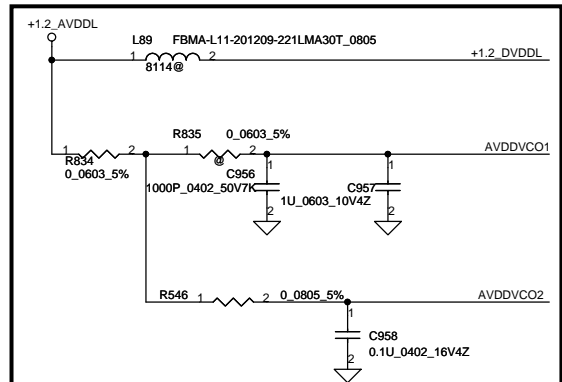
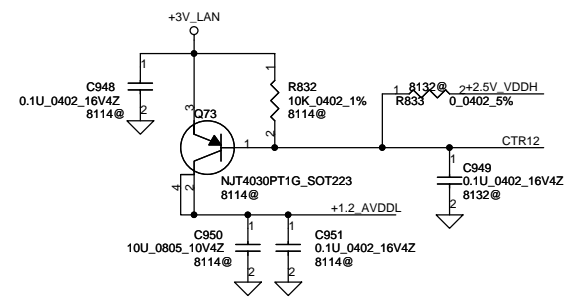
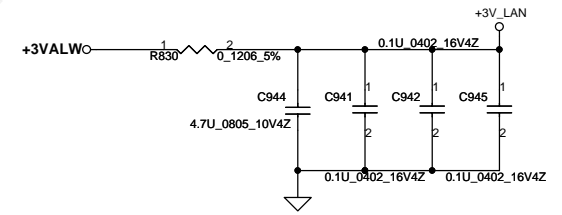
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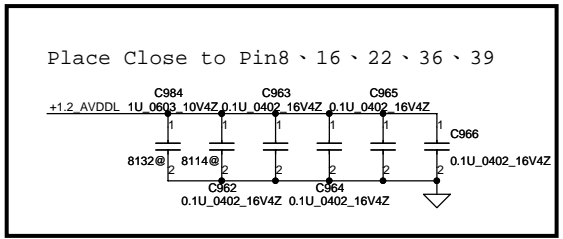
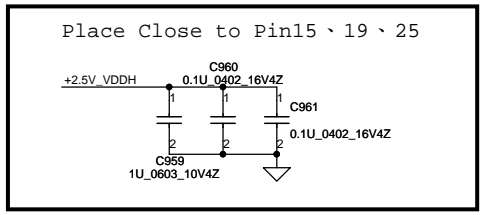
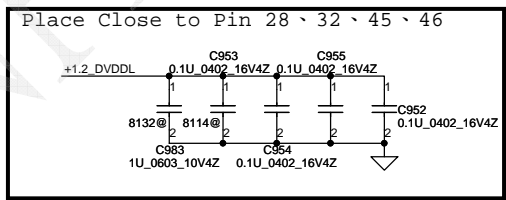
change AR8132-AL1E for pre-PVT

For AR8131V1

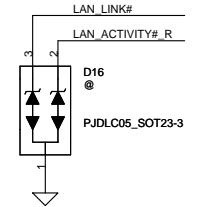
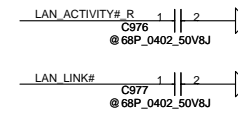
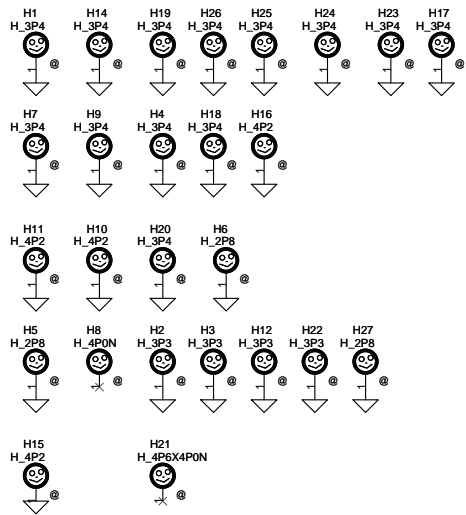
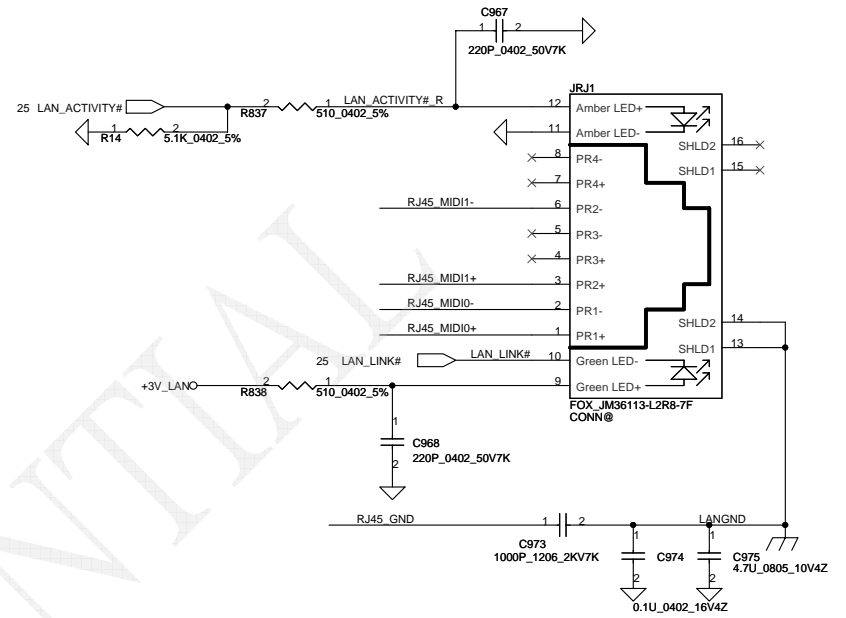
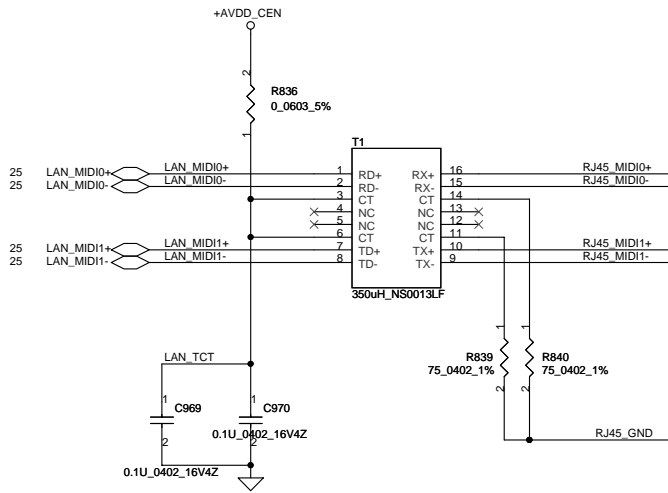
Layout Notice : Close to chip



If overclocking, R638, L30 stuffed and R637 removed.
If not overclocking, R637, L30 stuffed and R638 removed.
AR8132:L30=0ohm,C856=0.1uF. remove C857

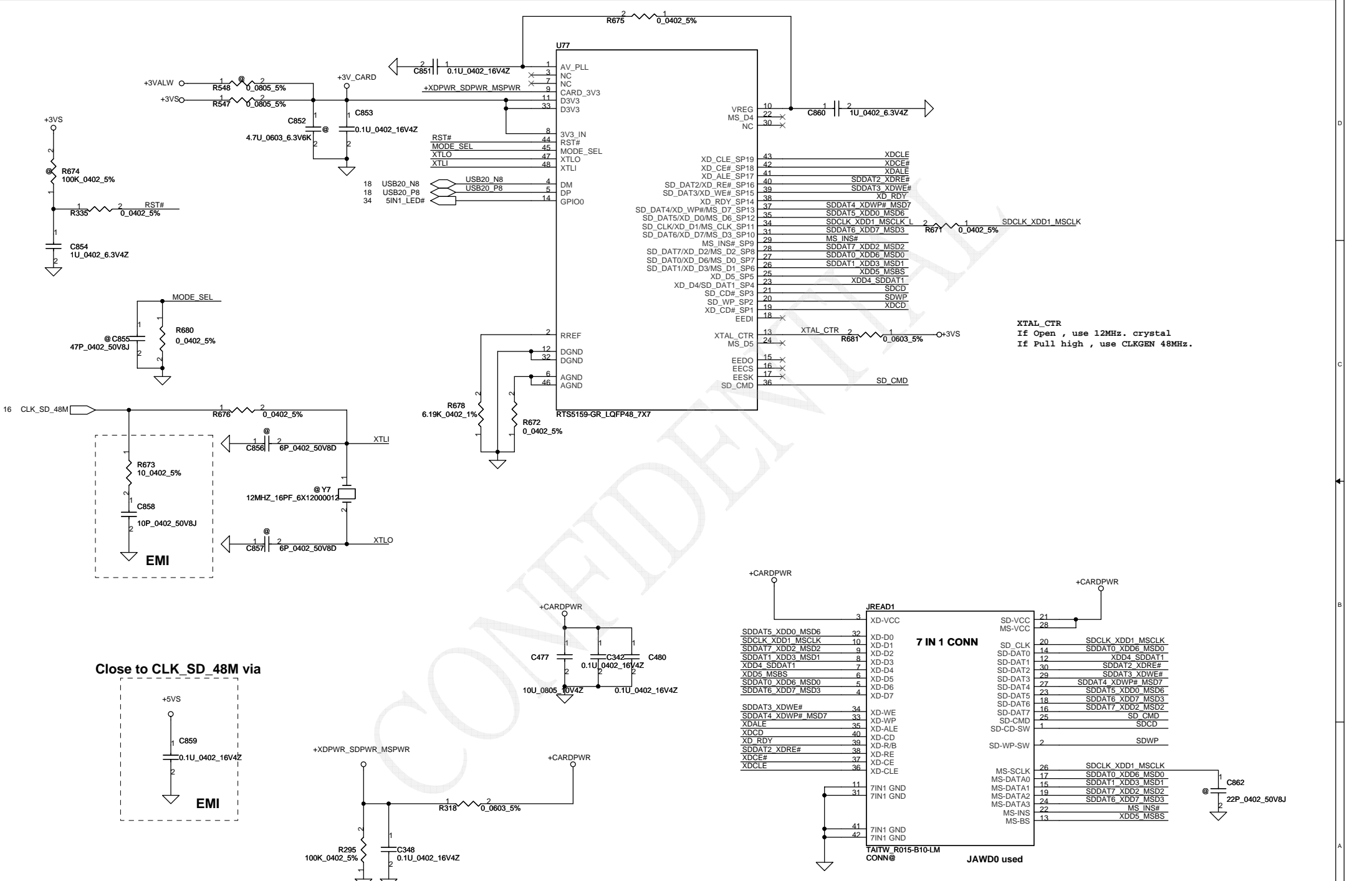


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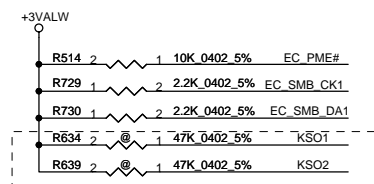
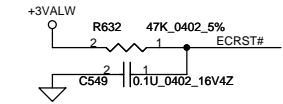
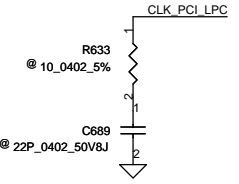
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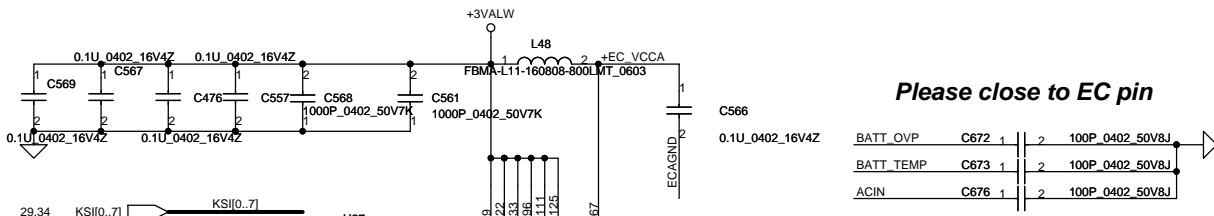
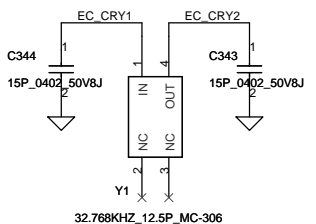
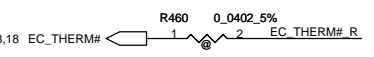
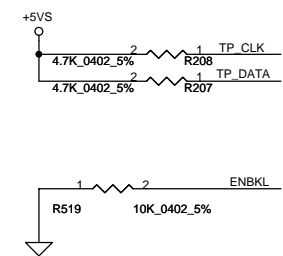
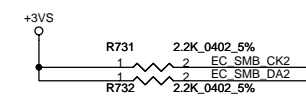
XTAL_CTR
If Open, use 12MHz. crystal
If Pull high, use CLKGEN 48MHz.

Close to CLK_SD 48M via

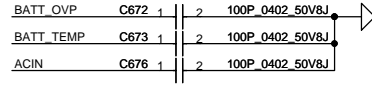
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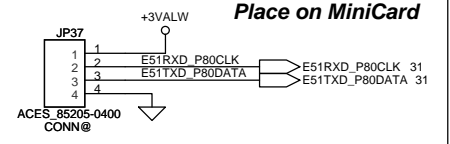
EC test-mode issue



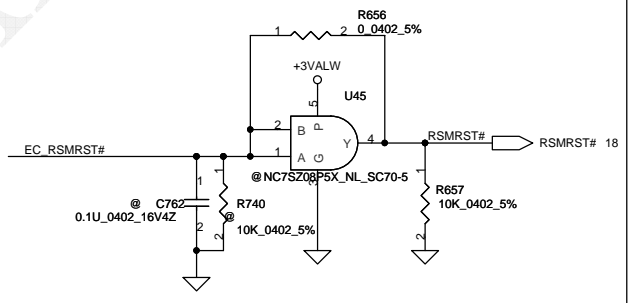
Please close to EC pin



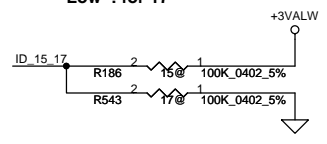
For EC Tools



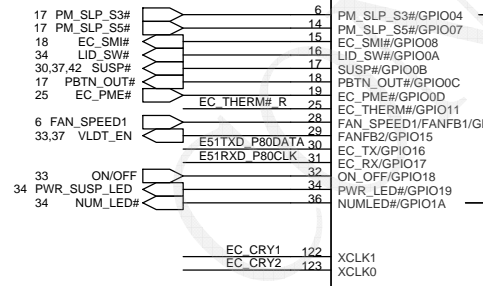
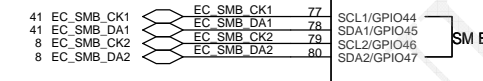
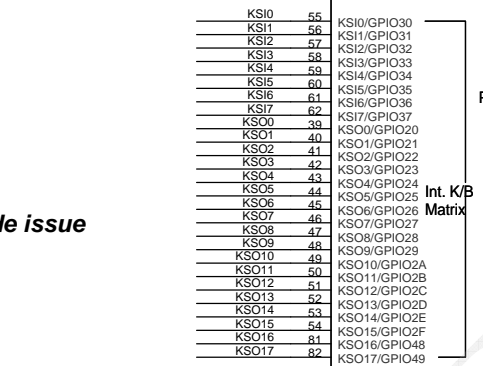
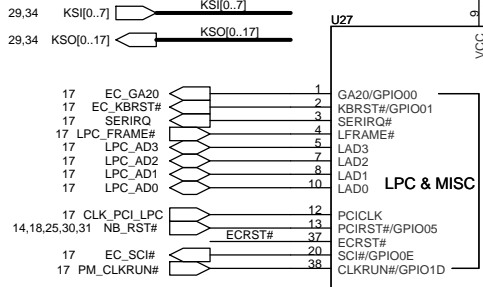
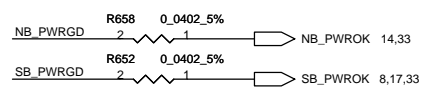
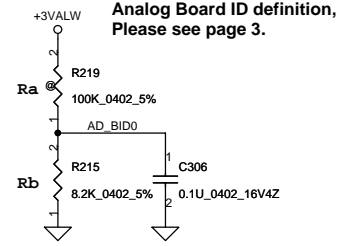
Place on MiniCard



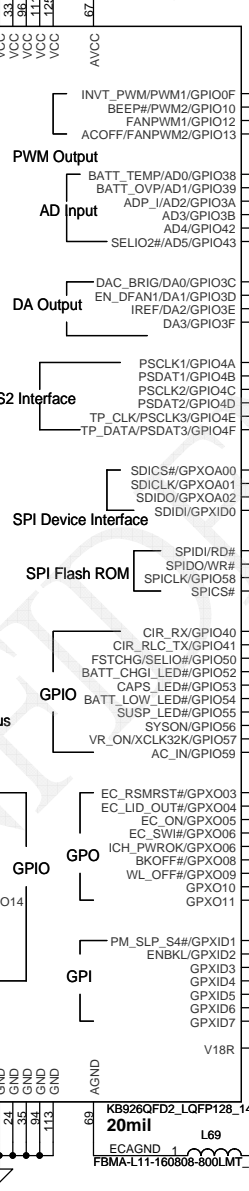
ID DETECT
High : for 15"
Low : for 17"



Analog Board ID definition,
Please see page 3.

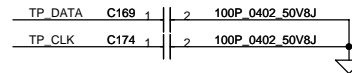
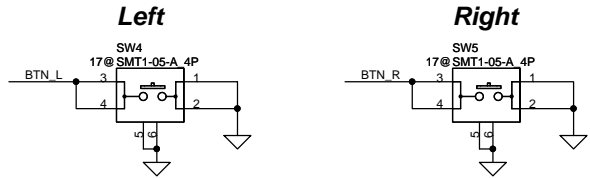


Chagne to D3 version

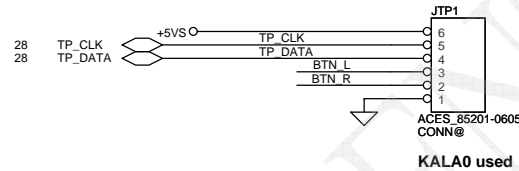


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For 17"

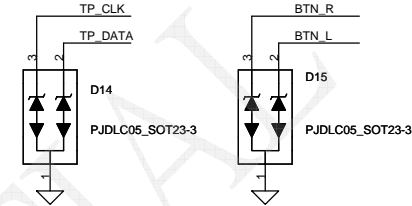
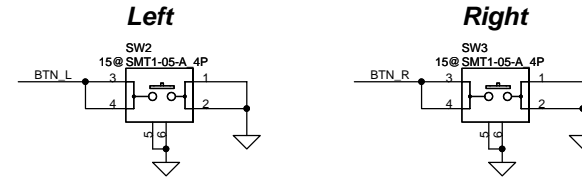


To TP/B Conn.



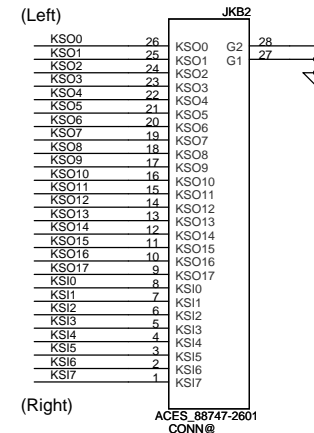
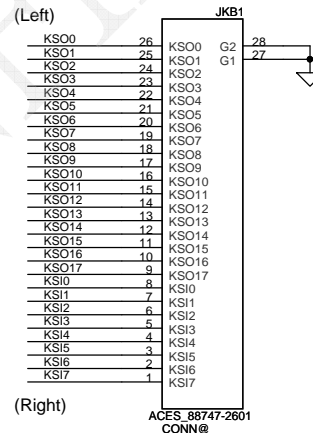
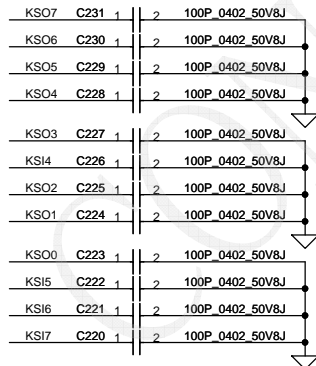
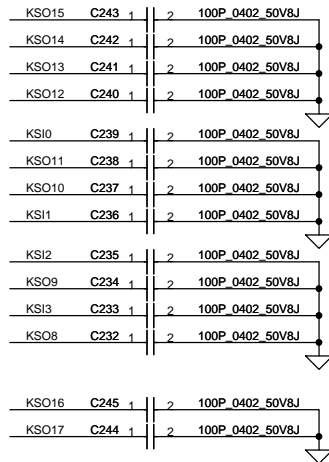
KALA0 used

For 15"



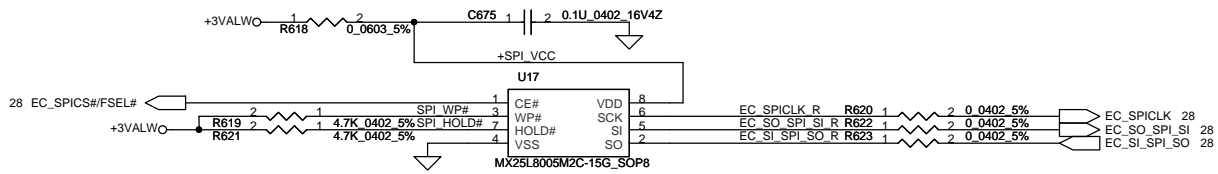
Change to SCA00000200

INT_KBD Conn.



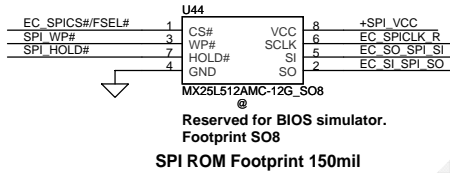
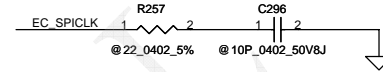
KB1 for 15"
KB2 for 17"

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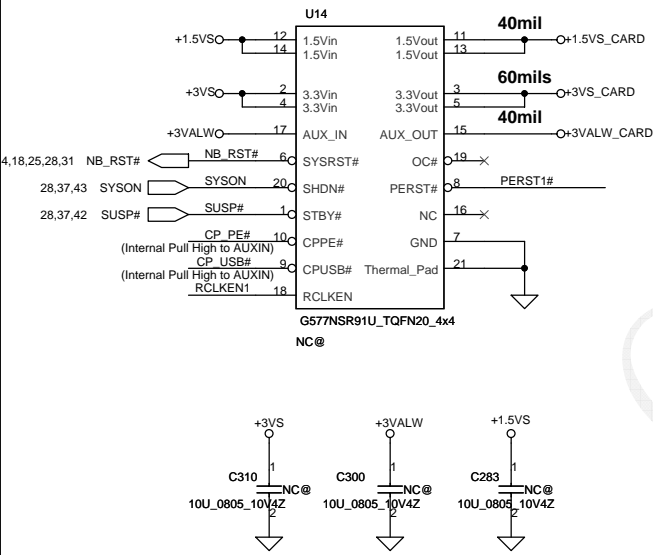


SA00000XT00 : S IC FL 8M MX25L8005M2C-15G SOP 8P
 ENE suggestion SPI Frequency over 66MHz
 SST: 50MHz
 MXIC: 70MHz
 ST: 40MHz

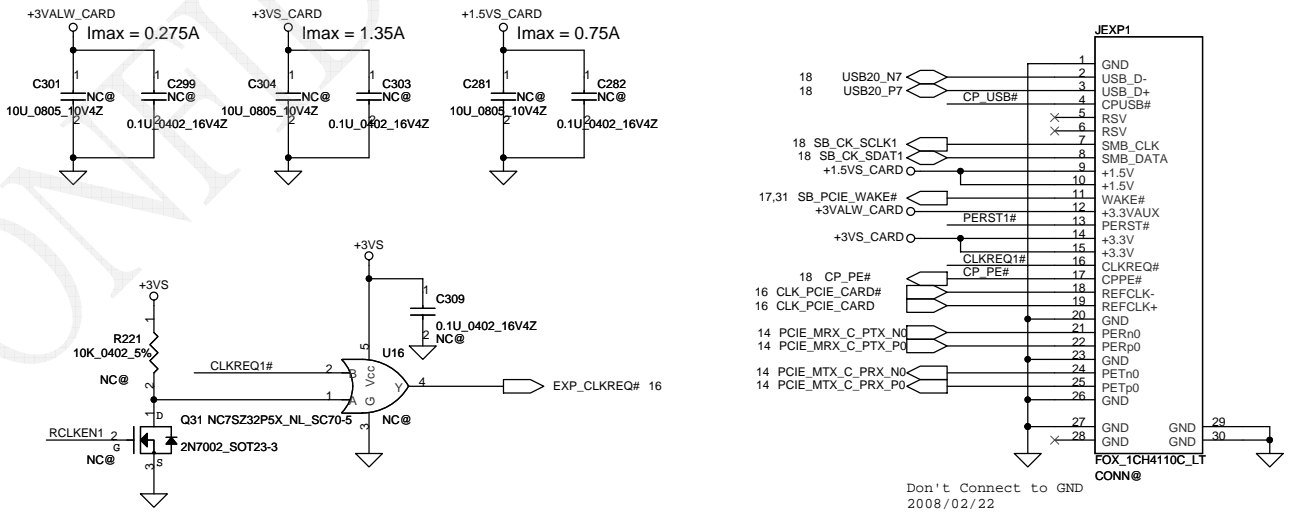
ONLY MXIC used in this project (66MHz)



New Card Power Switch



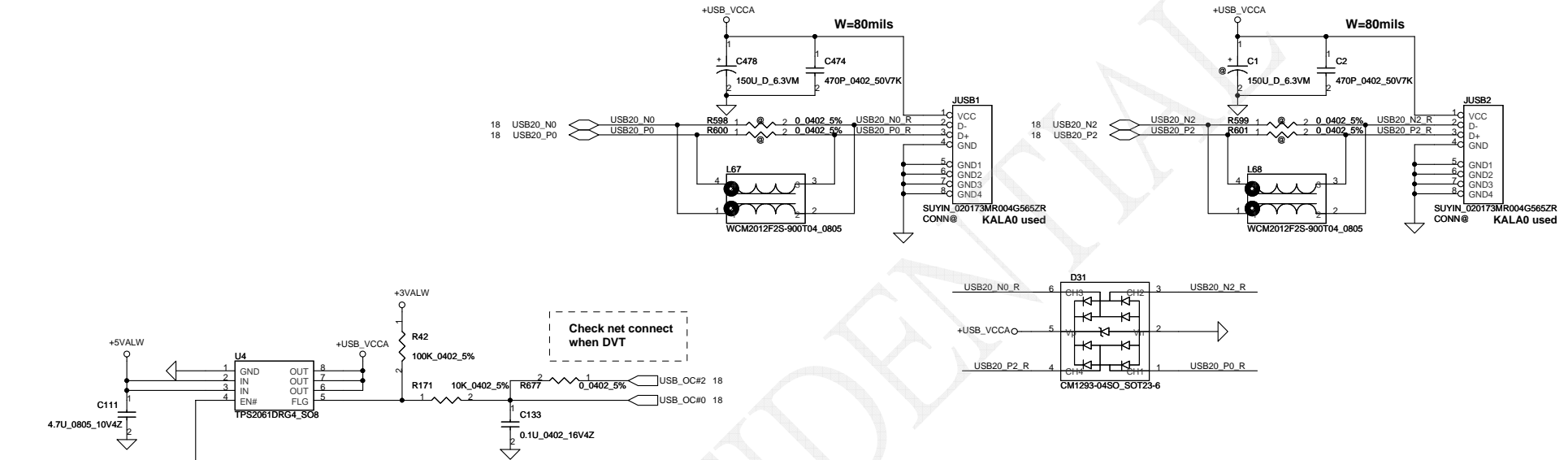
New Card Socket (Left/TOP)



Don't Connect to GND
 2008/02/22

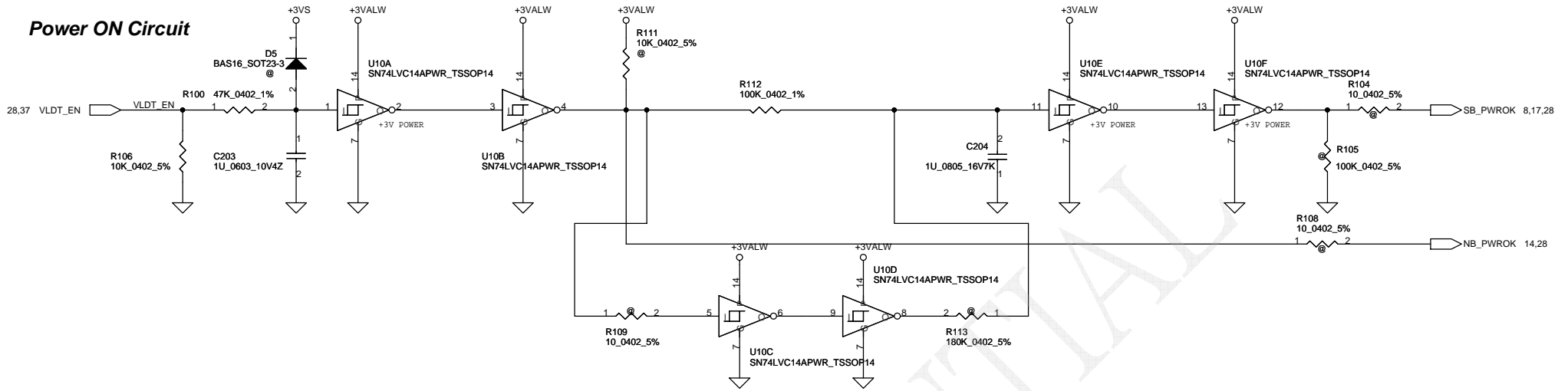
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USB CONN. 1 & 2

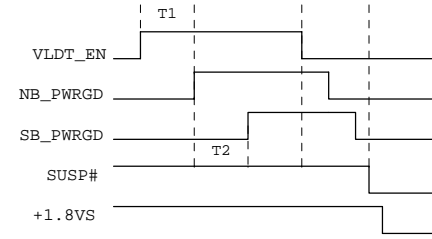


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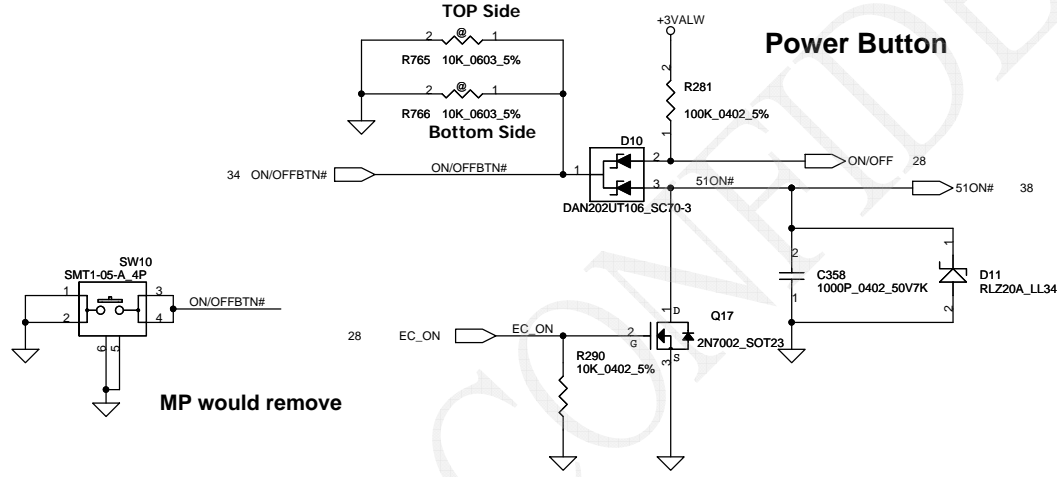
Power ON Circuit



note:T1 minimum 15ms,T2 minimum 33ms/maximum 500ms, SUSP# goes to low after SB_PWRGD goes to low for power down.

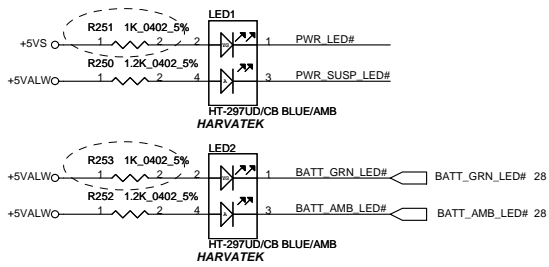
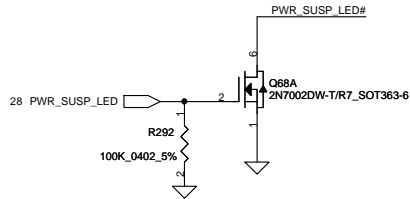
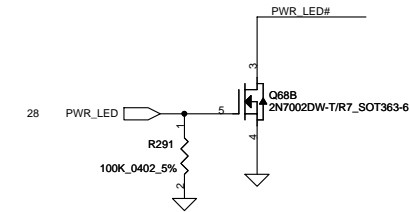


Power Button

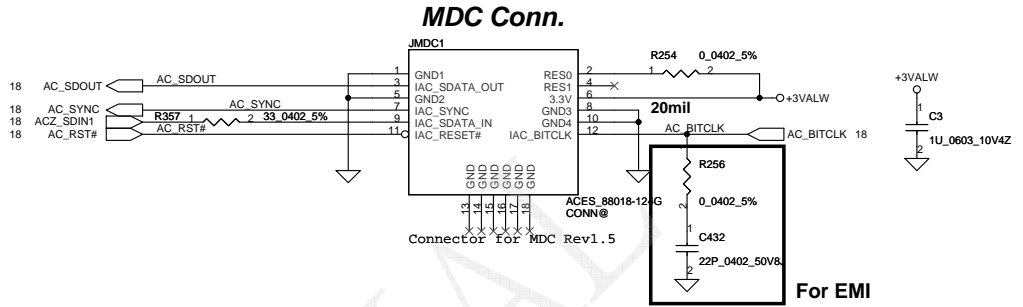


MP would remove

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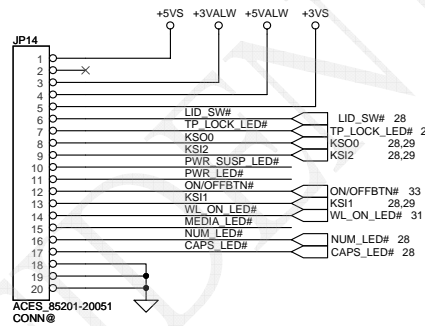


BLUE/AMB LED

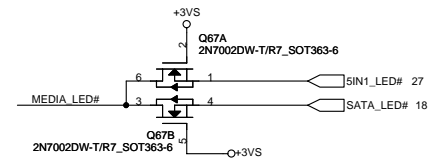
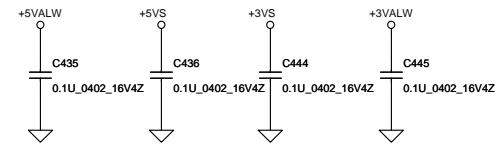


For EMI

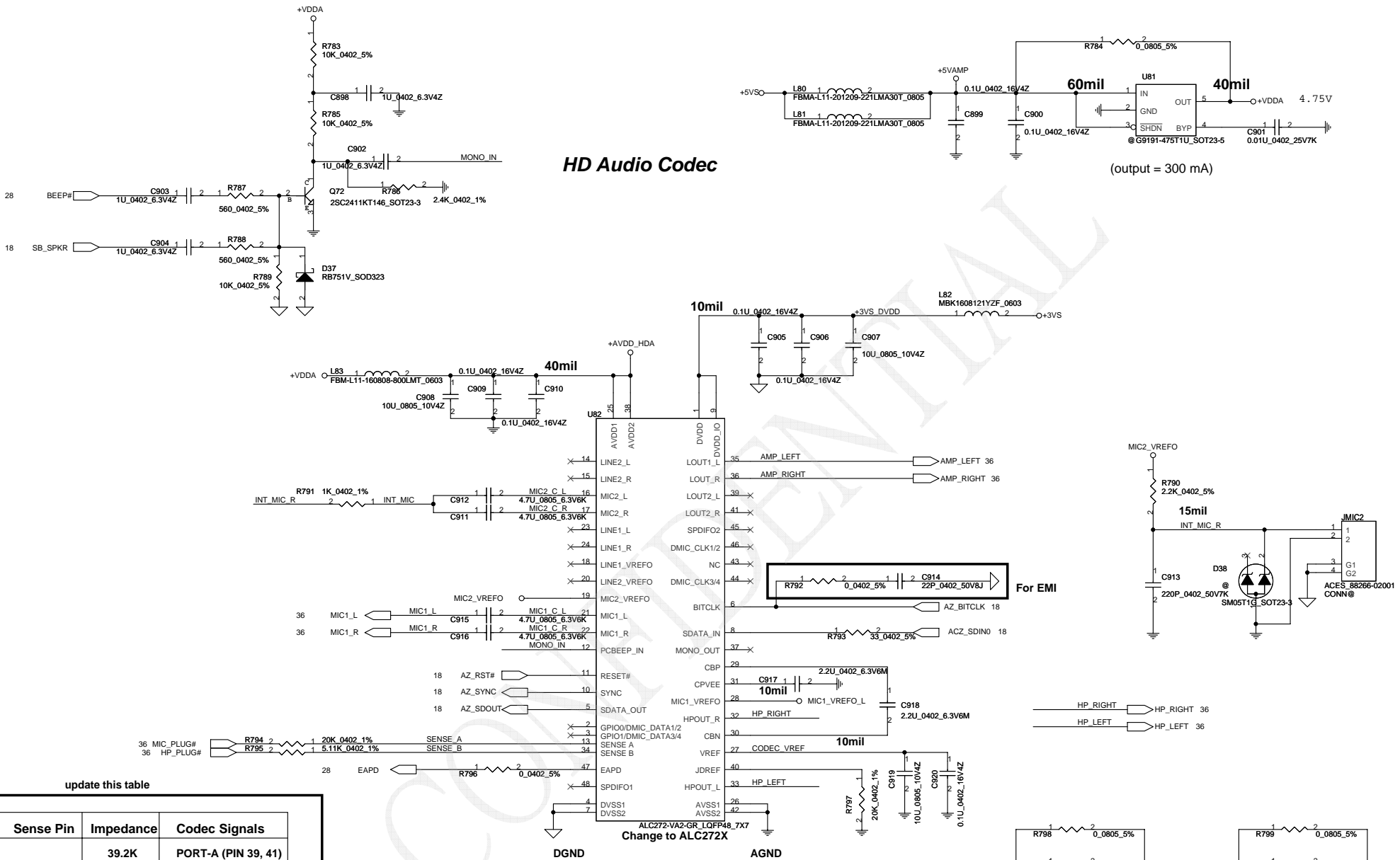
To PWR LED/B



	KSO0
KSI1	WL_BTN#
KSI2	TP_LOCK_BTN#
KSI3	
KSI4	
KSI5	
KSI6	



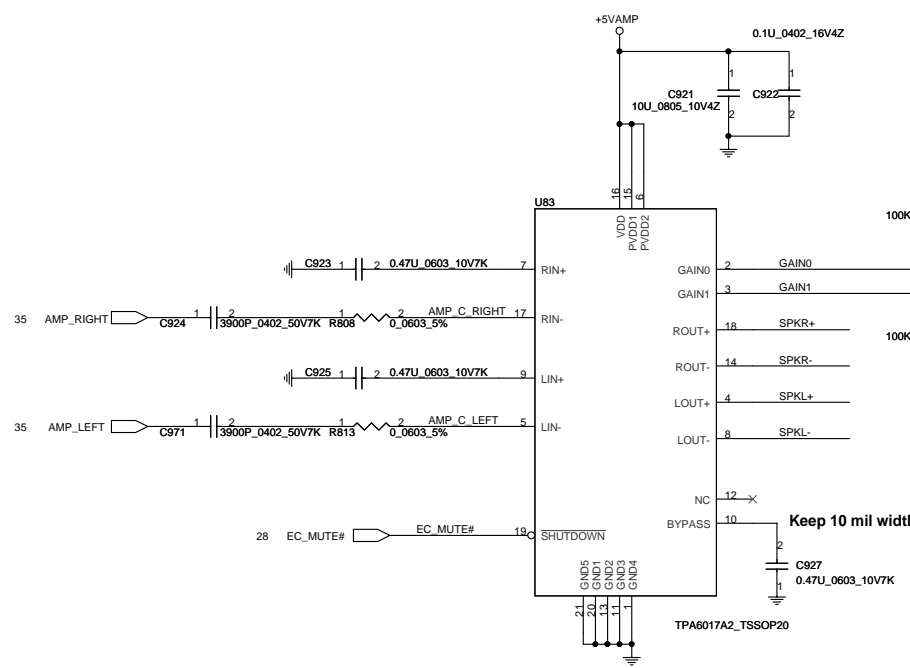
HD Audio Codec



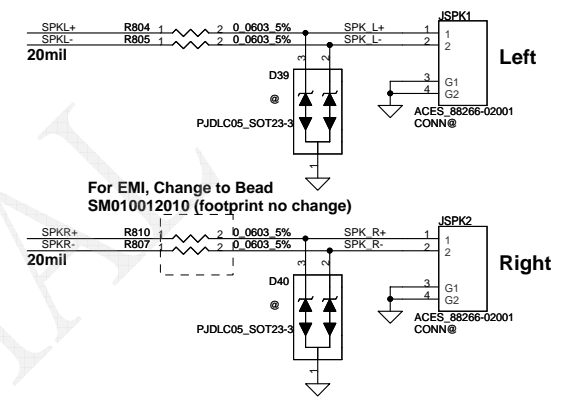
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

Change to ALC272X

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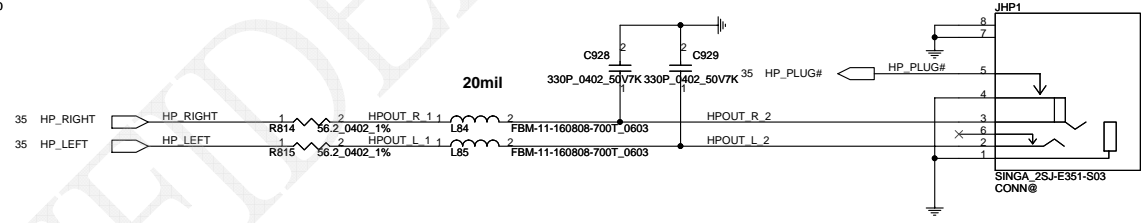


Int. Speaker Conn.

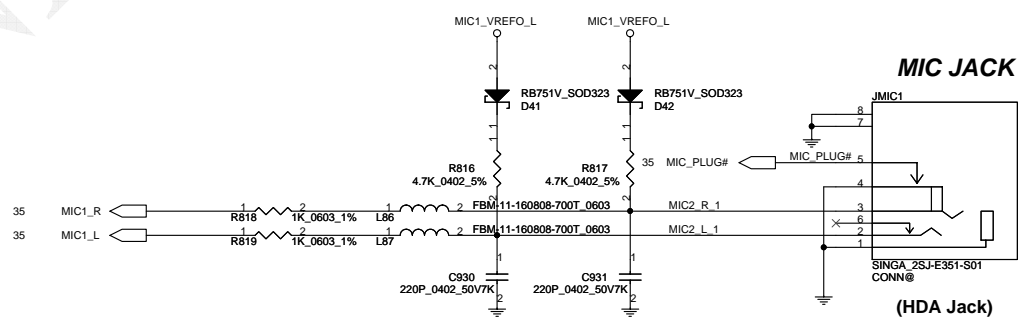


For EMI, Change to Bead SM010012010 (footprint no change)

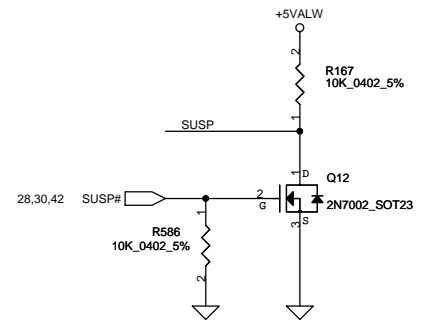
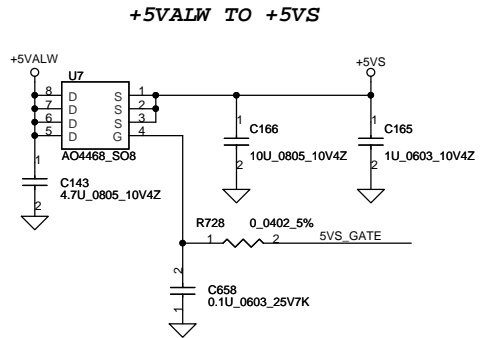
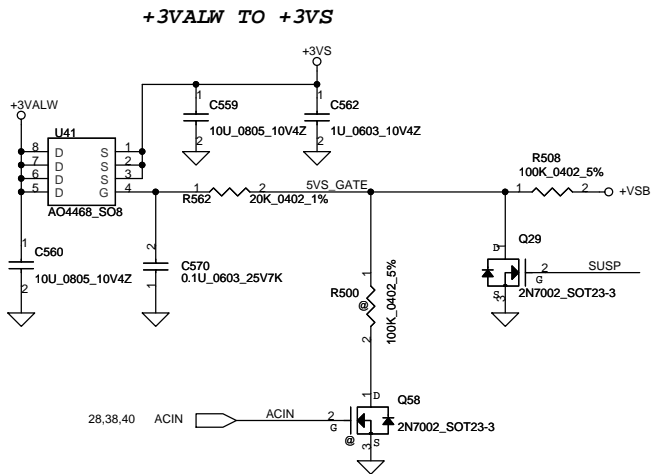
LINE Out/Headphone Out



MIC JACK

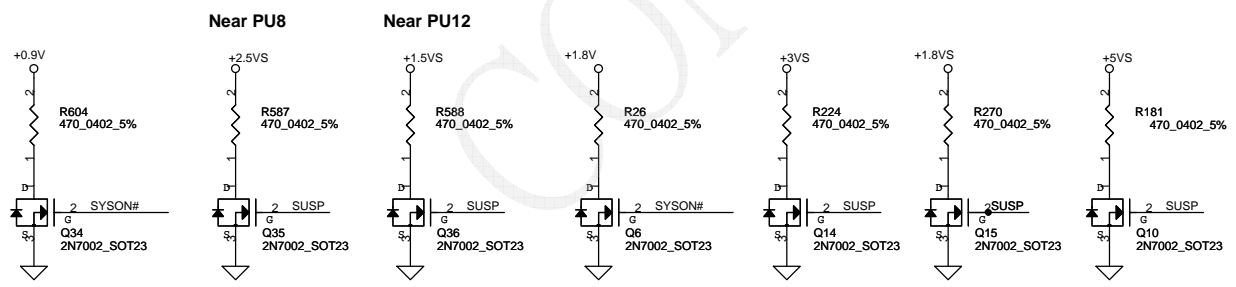
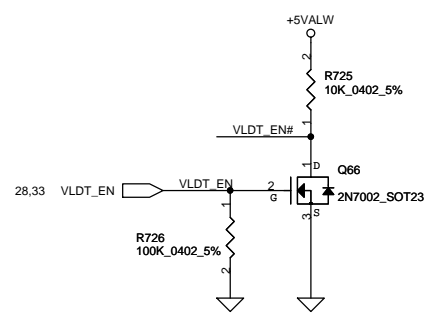
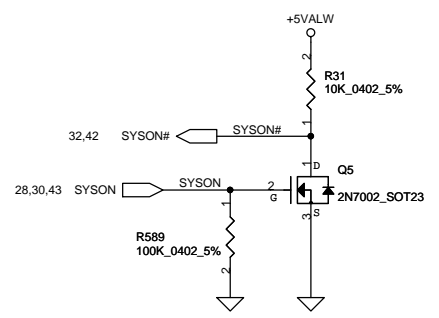
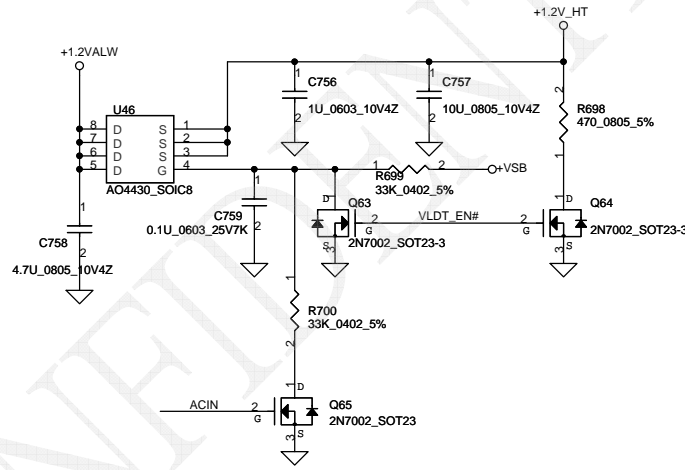
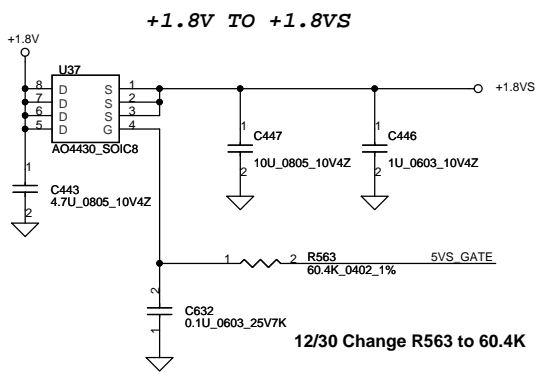


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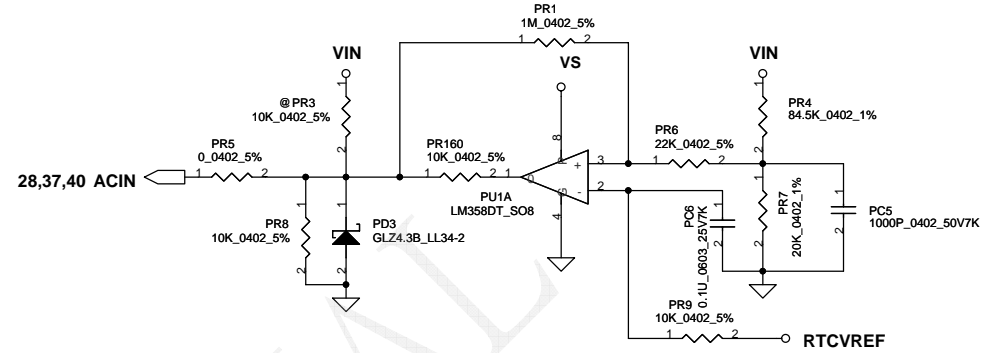
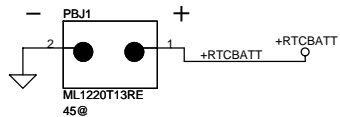
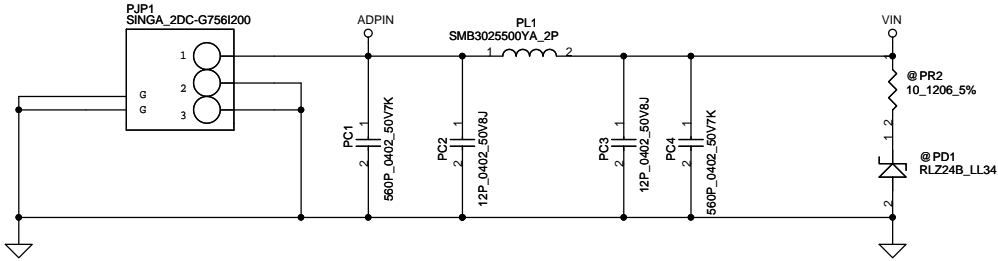
2006/2/22 Add C658 0.1uF

+1.2VALW TO +1.2V_HT

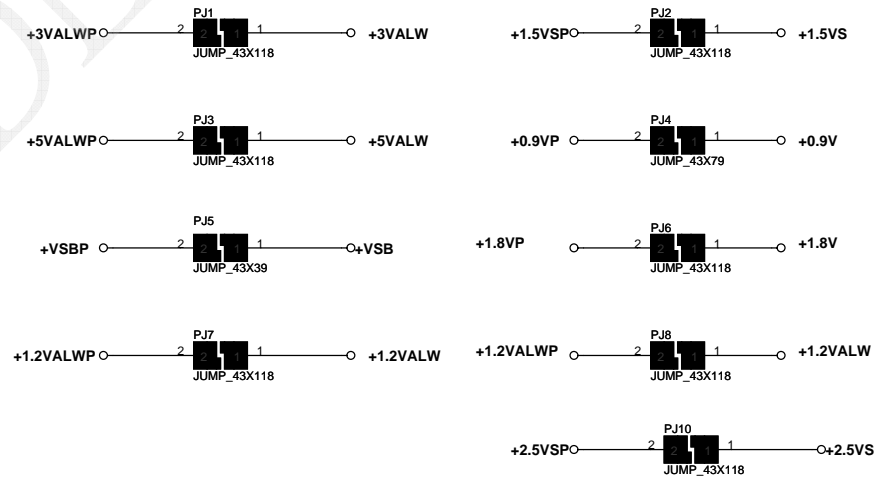
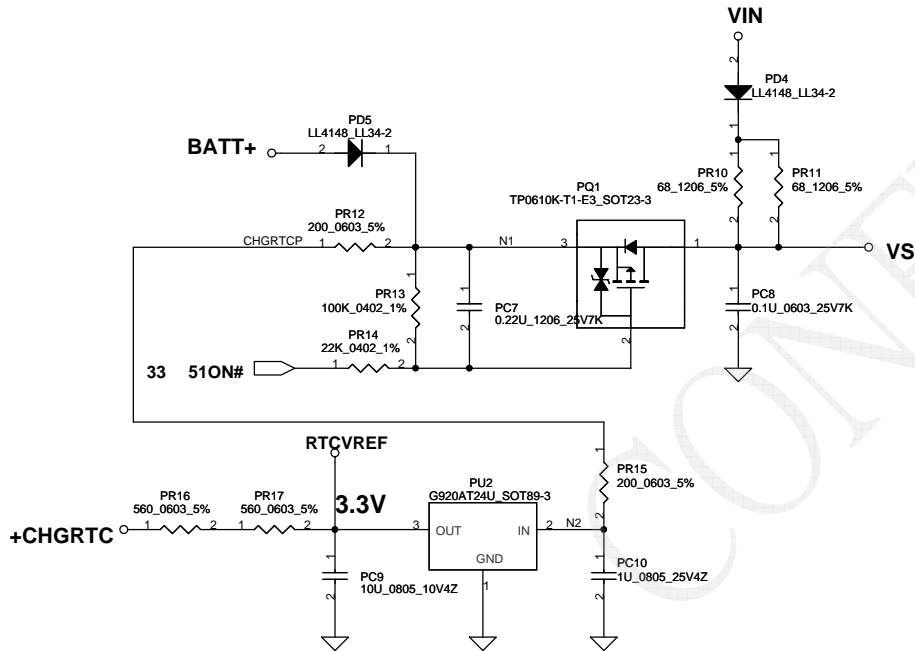


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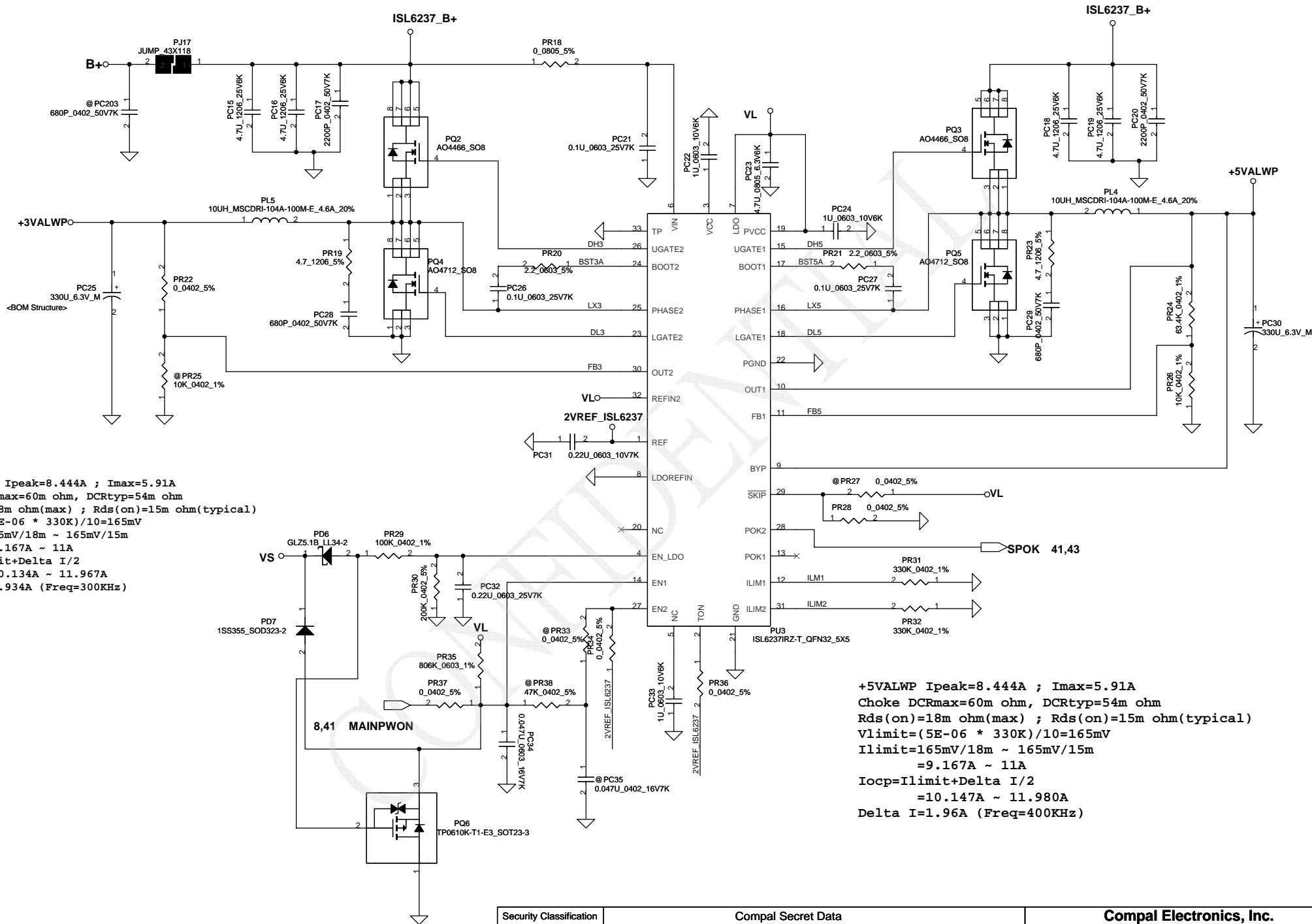
DC231000500



Vin Detector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



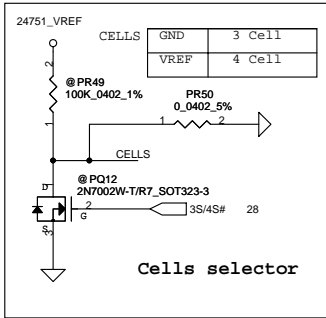
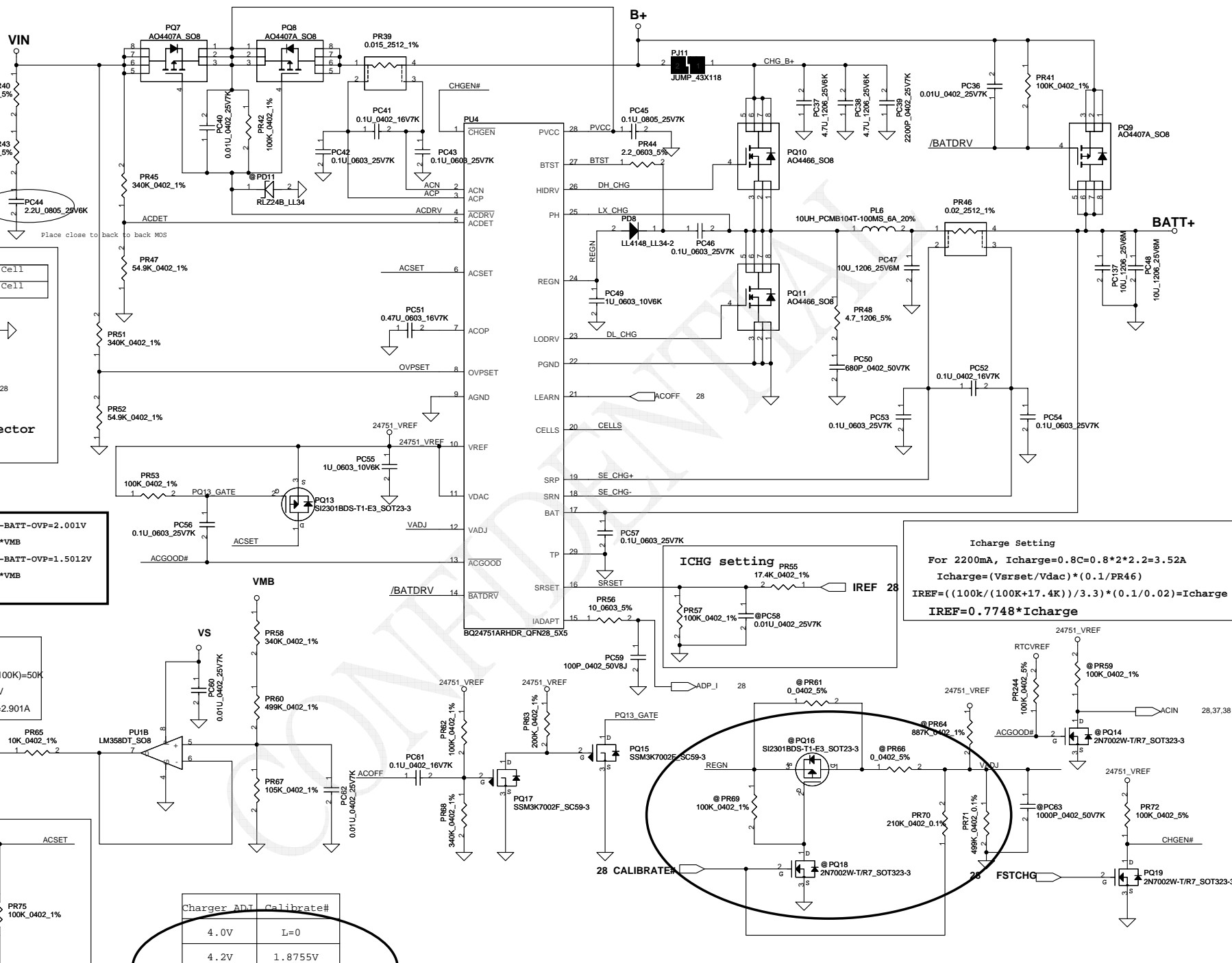
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+3.3VALWP Ipeak=8.444A ; Imax=5.91A
 Choke DCRmax=60m ohm, DCRtyp=54m ohm
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 $Vlimit=(5E-06 * 330K)/10=165mV$
 $Ilimit=165mV/18m \sim 165mV/15m$
 $=9.167A \sim 11A$
 $Iocp=Ilimit+Delta I/2$
 $=10.134A \sim 11.967A$
 $Delta I=1.934A (Freq=300KHz)$

+5VALWP Ipeak=8.444A ; Imax=5.91A
 Choke DCRmax=60m ohm, DCRtyp=54m ohm
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 $Vlimit=(5E-06 * 330K)/10=165mV$
 $Ilimit=165mV/18m \sim 165mV/15m$
 $=9.167A \sim 11A$
 $Iocp=Ilimit+Delta I/2$
 $=10.147A \sim 11.980A$
 $Delta I=1.96A (Freq=400KHz)$

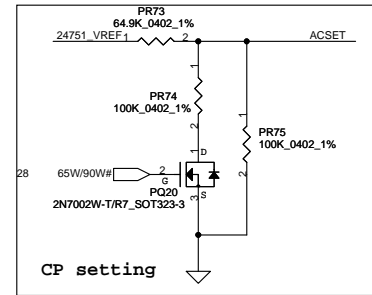
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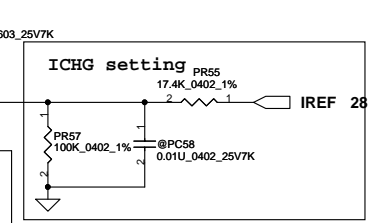
Input OVP : 22.3V
 Input UVP : 17.26V
 Fsw : 300KHz

LI-4S :18.0V----BATT-OVP=2.001V
 BATT-OVP=0.1112*VMB
 LI-3S :13.5V----BATT-OVP=1.5012V
 BATT-OVP=0.1112*VMB
 per cell=3.5V

CP Point Setting
 CP point=ladapter*85%
 65W adapter R=(100K*100K)/(100K+100K)=50K
 Vacset=3.3*(50K/(50K+64.9K))=1.436V
 CP POINT=(1.436V/3.3V)*(0.1/0.015)=2.901A

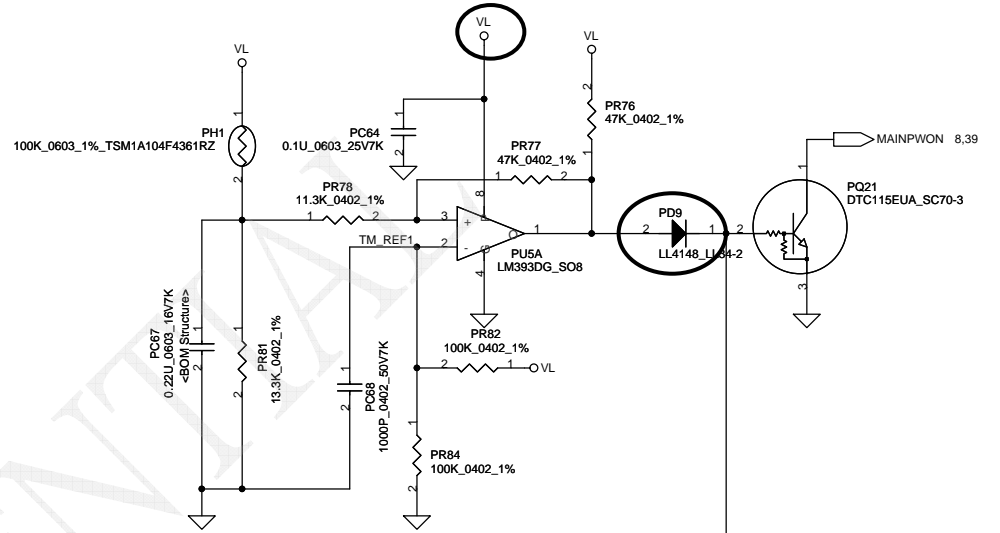


Charger ADI	Calibrate#
4.0V	L=0
4.2V	1.8755V
4.3V	2.8132V
4.35V	H=3.3V

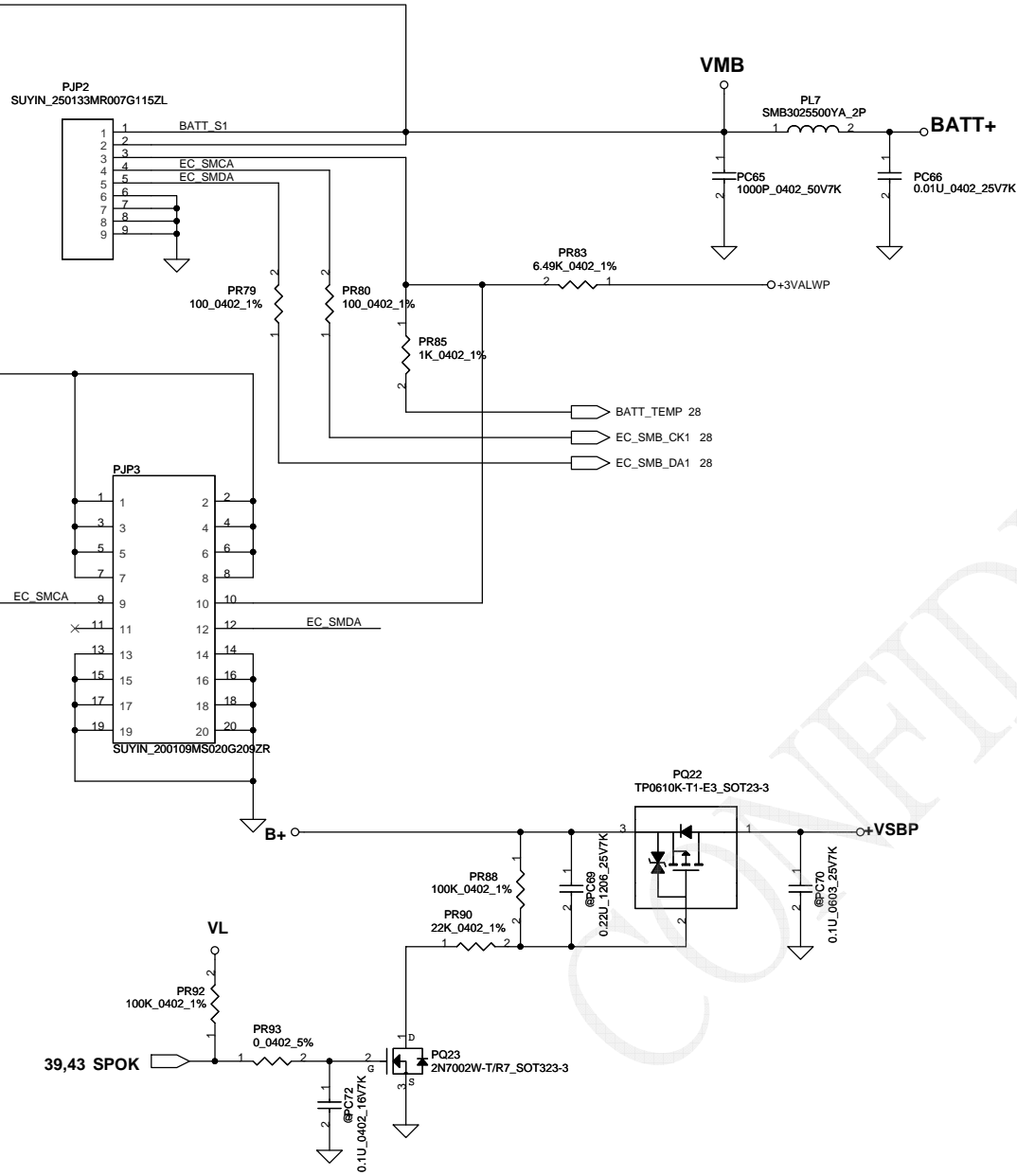
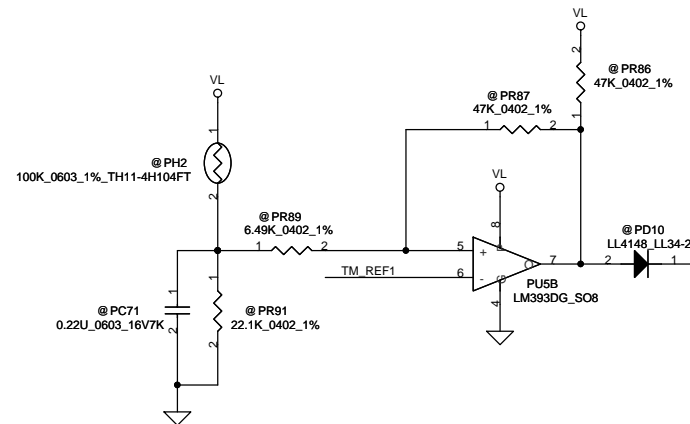


Icharge Setting
 For 2200mA, Icharge=0.8C=0.8*2*2.2=3.52A
 Icharge=(Vsrset/Vdac)*(0.1/PR46)
 IREF=((100k/(100K+17.4K))/3.3)*(0.1/0.02)=Icharge
 IREF=0.7748*Icharge

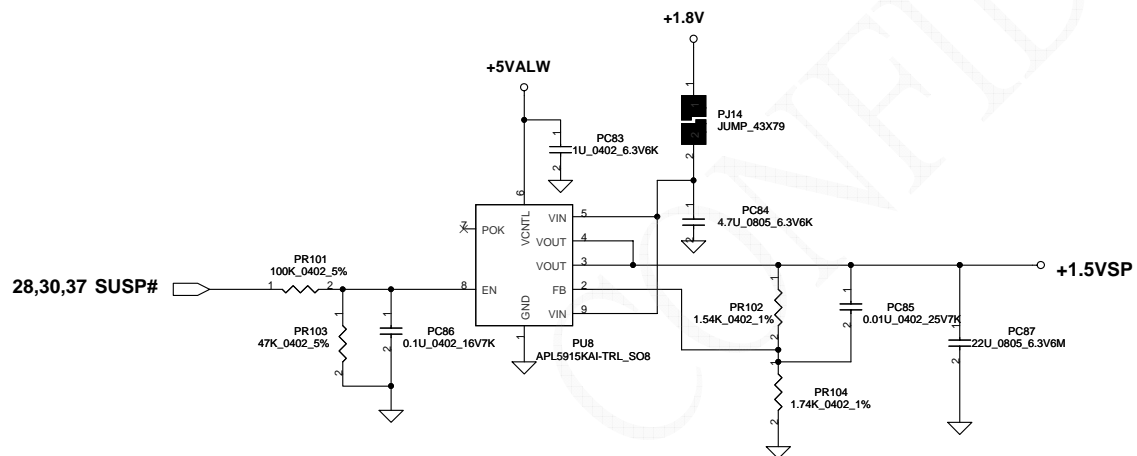
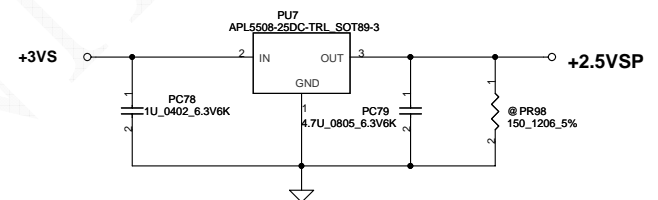
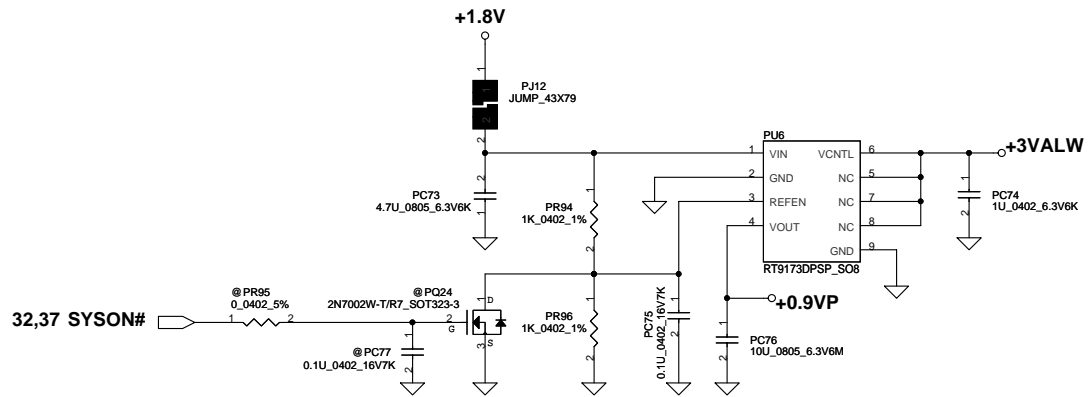
PH1 under CPU botten side :
CPU thermal protection at 92 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 75 degree C



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28,30,37 SYSON

VFB=0.75V
 $V_o = VFB * (1 + PR111 / PR112) = 0.75 * (1 + 14K / 10K) = 1.8V$
 $R_{ton} = 267K \Rightarrow F_{sw} = 297KHz$

Cout ESR=15m ohm
 $I_{peak} = 11.96A$, $I_{max} = 8.372A$, $I_{ocp} = 14.352A$
 $\Delta I = ((19-1.8) * (1.8/19)) / (L * F_{sw})$
 $((19-1.8) * (1.8/19)) / (1.8u * 297000) = 3.048A$
 $\Rightarrow 1/2 \Delta I = 1.524A$

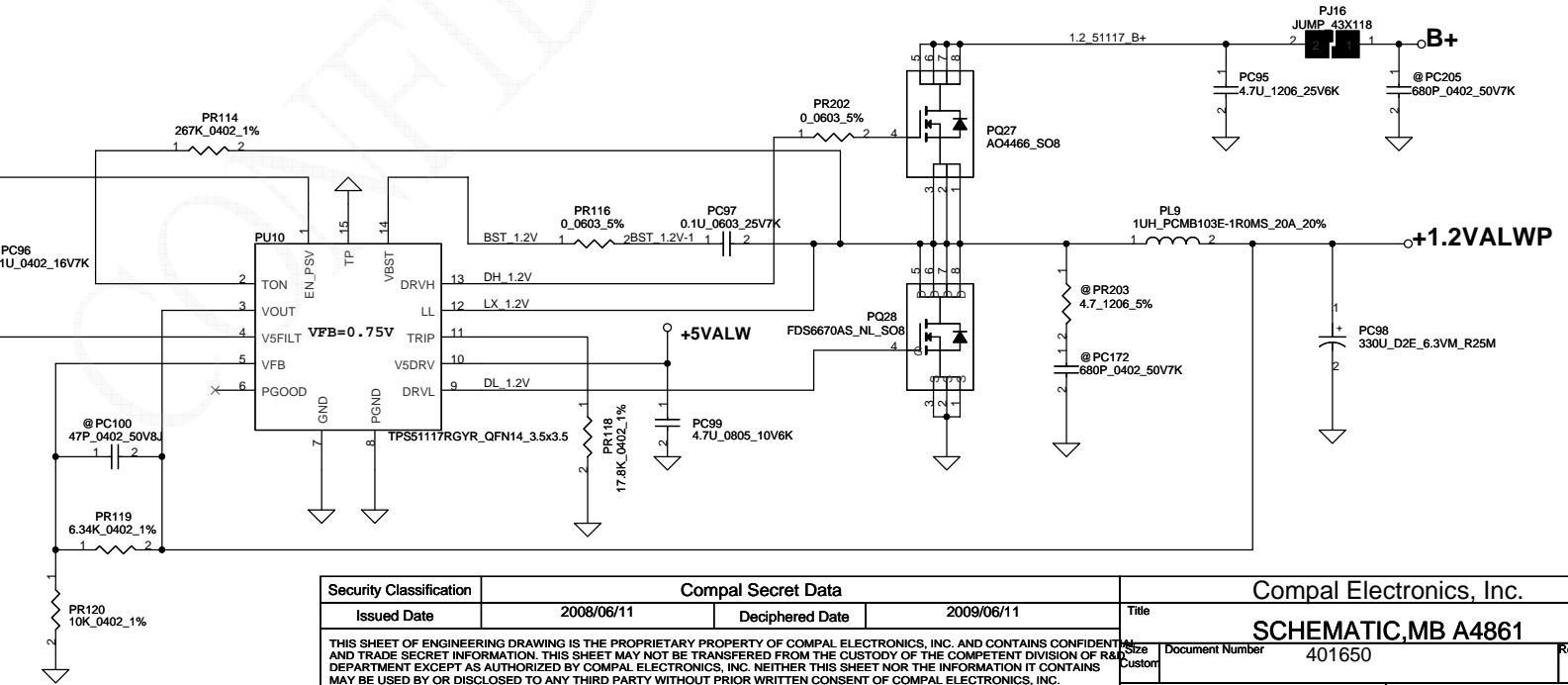
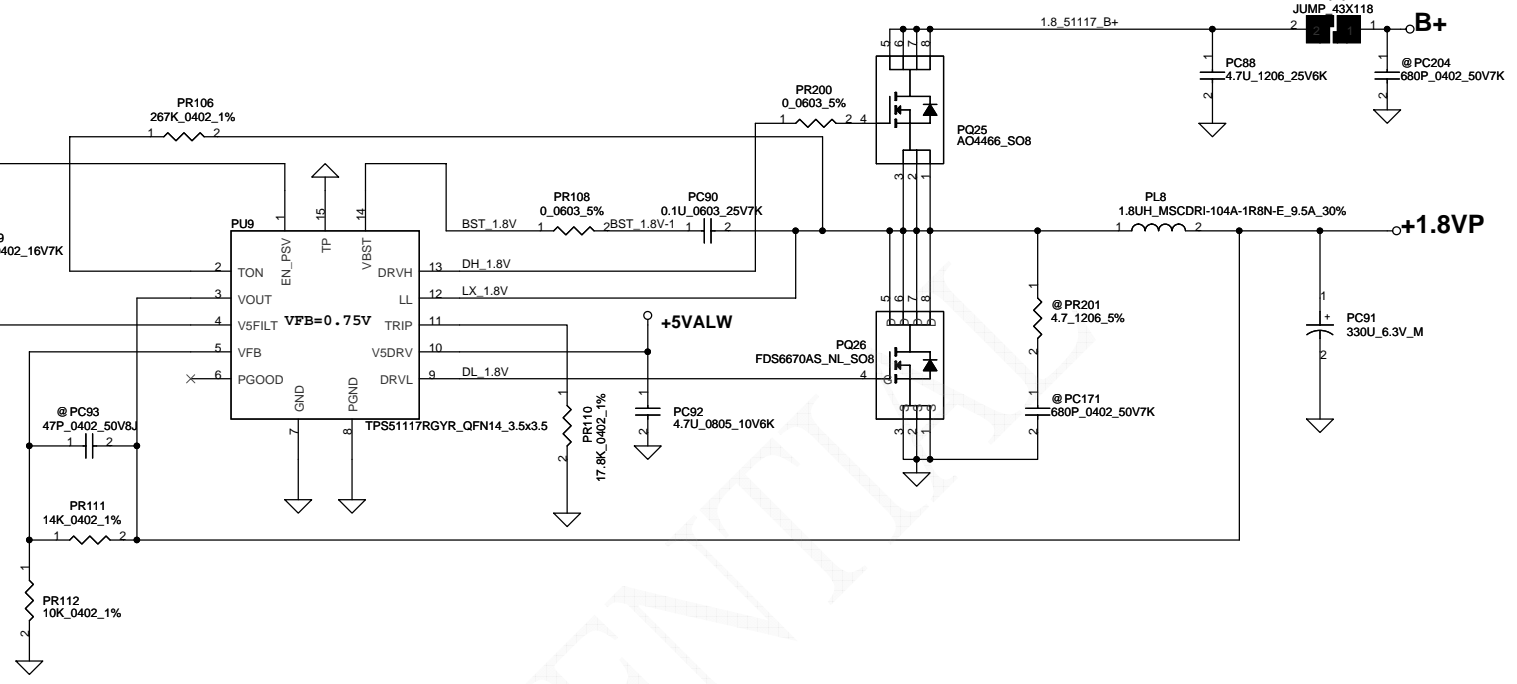
$R_{trip} = 17.8K$
 $I_{ocp} = 13.04A \sim 21.41A$

39,41 SPOK

VFB=0.75V
 $V_o = VFB * (1 + PR119 / PR120) = 0.75 * (1 + 6.04K / 10K) = 1.203V$
 $R_{ton} = 267K \Rightarrow F_{sw} = 298KHz$

Cout ESR=15m ohm
 $I_{peak} = 10.80A$, $I_{max} = 7.56A$, $I_{ocp} = 12.96A$
 $\Delta I = ((19-1.2) * (1.2/19)) / (L * F_{sw})$
 $((19-1.2) * (1.2/19)) / (1.8u * 298000) = 2.10A$
 $\Rightarrow 1/2 \Delta I = 1.05A$

$R_{trip} = 17.8K$
 $I_{ocp} = 12.75A \sim 20.83A$



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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Customer changed CPU to TF36/38.	TF36/38 is 31W CPU, must change MOS to 1H2L.	0.1	44	Add PQ31 and PQ34 SB000009F80(S TR AO4456 1N SO8)	08, 11/13	to DVT
2	Change CP OCP setting.	TF36/38 CPU OCP setting change.	0.1	44	Change PR198 to SD034402180(S RES 1/16W 4.02K 0402 1%)	08, 11/13	to DVT
3	S3 Mode issue.	Because APL5915 has 0.4V enable voltage, so add PR103 to pull down enable voltage when system in S3 mode	0.1	42	Add PR103 SD028470280(S RES 1/16W 47K 0402 5%)	08, 11/13	to DVT
4	AMD issue.	AMD request add 1.2V to 1.22V for chipset.	0.1	43	Change PR119 from SD034604180 to SD034634180.	08, 11/17	to DVT
5	EMI issue.	EMI request add charger snubber.	0.1	40	Add PR48 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC50 SE074681K80(S CER CAP 680P 50V K X7R 0402)	08, 11/17	to DVT
6	Cost issue.	Cost issue.	0.1	44	Change PC201 from SF000000G80(S ELE CAP 220U 25V M HA0 MVY) to SF22004M210(S ELE CAP 220U 25V M 8X10.2 CE-AX)	08, 11/17	to DVT
7	Support charge voltage.	Support charge voltage.	0.1	40	Delete PQ18 SB000006800(S TR 2N7002W T/R7 1N SOT-323)	08, 11/26	to DVT
8	Support charge voltage.	Support charge voltage.	0.1	40	Delete PQ16 SB923010020(S TR SI2301BDS-T1-E3 1P SOT23)	08, 11/26	to DVT
9	Support charge voltage.	Support charge voltage.	0.1	40	Delete PR66 SD028000080(S RES 1/16W 0 0402 5%)	08, 11/26	to DVT
10	Support charge voltage.	Support charge voltage.	0.1	40	Delete PR69 SD034100380(S RES 1/16W 100K 0402 1%)	08, 11/26	to DVT
11	Support charge voltage.	Support charge voltage.	0.1	40	Delete PC63 SE074102K80(S CER CAP 1000P 50V K X7R 0402)	08, 11/26	to DVT
12	Support charge voltage.	Support charge voltage.	0.1	40	Add PR70 SD034210380(S RES 1/16W 210K 0402 1%)	08, 11/26	to DVT
13	Support charge voltage.	Support charge voltage.	0.1	40	Add PR71 SD034499380(S RES 1/16W 499K 0402 1%)	08, 11/26	to DVT
14							
15							
16							
17							
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Version change list (P.I.R. List) for HW

Item	Reason for change	Modify List	Rev.	PG#	Item	Reason for change	Modify List	Rev.	PG#
1	Material Change	Change U1 to APL5607	DVT	P06	26	Material Change	Change U82 to ALC272X-GR (SA00002CI20)	PVT	P35
2	Material Change	Change U85 to AR8132	DVT	P25	27	Material Change	Change U27 to KB926QFD3 (SA00001J580)	PVT	P28
3	8132 issue, OS black screen	Change L90 to R546 (0_0805)	DVT	P25	28	Material Change	Change U85 to AR8132M-ALLIE (SA000034V00)	PVT	P25
4	Circuit issue	Add R677	DVT	P32	29	Material Change	Change U85 to AR8132-ALLIE (SA000036Y00)	Pre-PVT	P25
5	RT5159 ID issue	Pop R680 to 0_0402_5%	DVT	P27	30	BOM change	Del D13,D4	Pre-PVT	P06
6	[EMI] Camera co-layout choke	Change R759,R760 to 0_0402 Reserve L77	DVT	P24	31	ESD Cost down	Del D16,D39,D40	Pre-PVT	
7	[Cost Down] audio LDO	Reserve U81 Pop784	DVT	P35	32	ESD Cost down	Change D15 to SCA00000200	Pre-PVT	
8	RT5159 unknow issue	Reserve R548, pop R547	DVT	P27	33	BOM change	Change R251,R253 to 1K	Pre-PVT	
9	[ESD]	Pop D39,D40	DVT	P36					
10	[ESD]	Pop D14,D15	DVT	P36					
11	[ESD]	Pop D16	DVT	P29					
12	[EMI]	Reserve C859 for EMI	DVT	P27					
13	Modify PWR Sequence	Reserve R104,R108 Pop R658,R652	DVT	P34 P28					
14	[EMI]	Reserve C861 for EMI	DVT	P16					
15	Material Change	Change JRJ1 type	DVT	P26					
16	Material Change	Change C924,C971 to 3900pF_0402	DVT	P36					
17	[EMI]	Reserve C350,C352,C353,C354	DVT	P15					
18	[EMI]	Pop R673 to 10ohm_0402 Pop C858 to 10pF_0402	PVT	P27					
19	[EMI]	Pop C859 to 0.1uF_0402	PVT	P27					
20	[EMI]	Pop C350,C352,C353,C354 to 0.1uF_0402	PVT	P15					
21	Material Change	Change R251,R253 to 1.1Kohm Change R250,R252 to 1.2Kohm	PVT	P34					
22	Material Change	Change Y2 footprint to correct	PVT	P18					
23	Material Change	Only cChange R810,R807 P/N to SM010012010	PVT	P36					
24	Circuit Change	Reserve PWN FAN function. Add R247,R40,JP38	PVT	P06					
25	Material Change	Change R814,R815 to 56.2ohm_0402	PVT	P36					

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