# PCA70/61

## Sugar Bay

# LA-7521P REV 0.2
# LA-7522P REV 0.1

# Schematic

**Intel Processor(Sandy Bridge) / PCH(Cougar Point)**

**Tuesday, April 12, 2011 Rev 0.2**

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |



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Title: ***Cover Page***

| Size | Document Number | Rev |
|---|---|---|
| Custom | **PCA70 LA-7521P M/B** | 0.1 |

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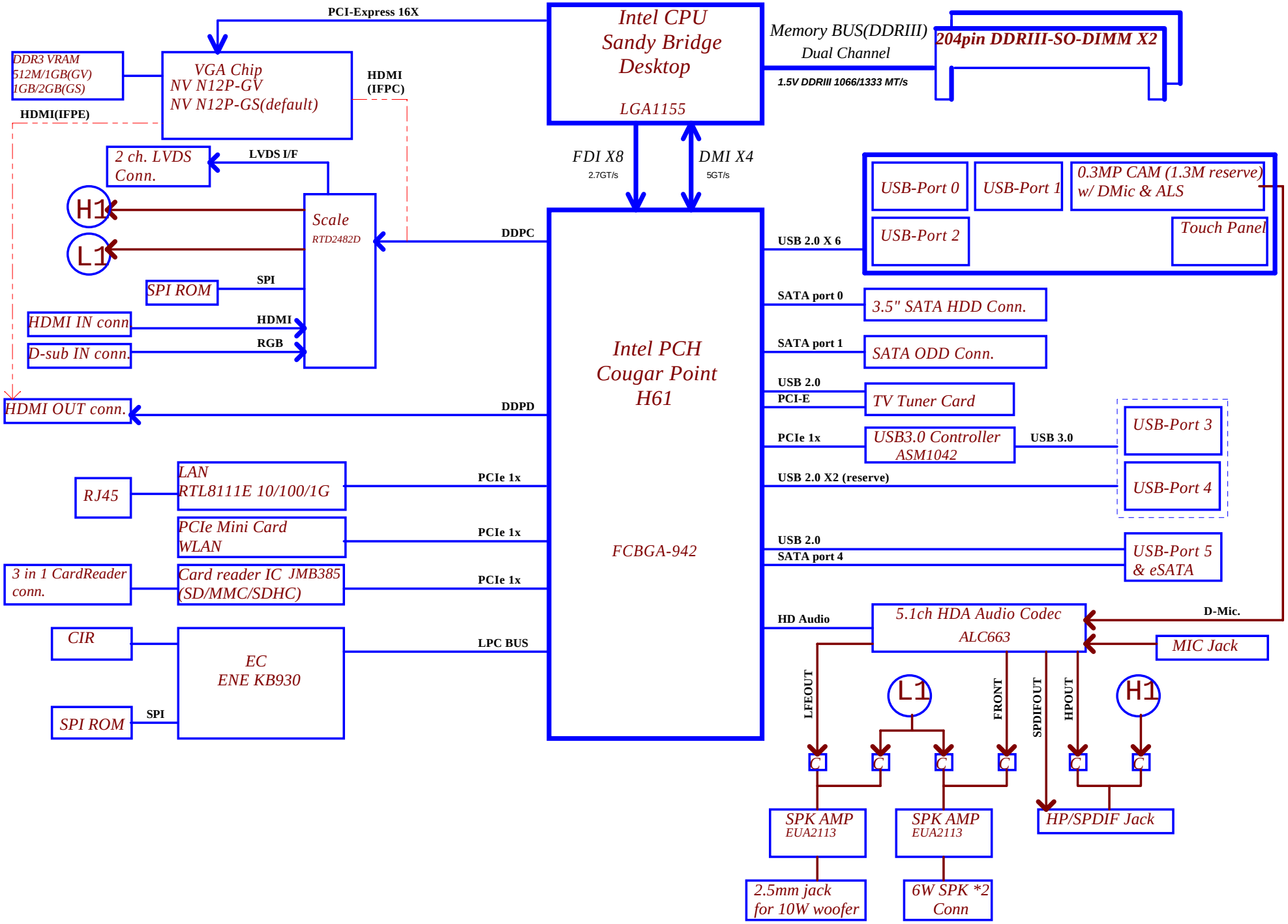


| | | | |
|---|---|---|---|
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Title: **Block Diagram**

Size | Document Number: **PCA70 LA-7521P M/B** | Rev: 0.1

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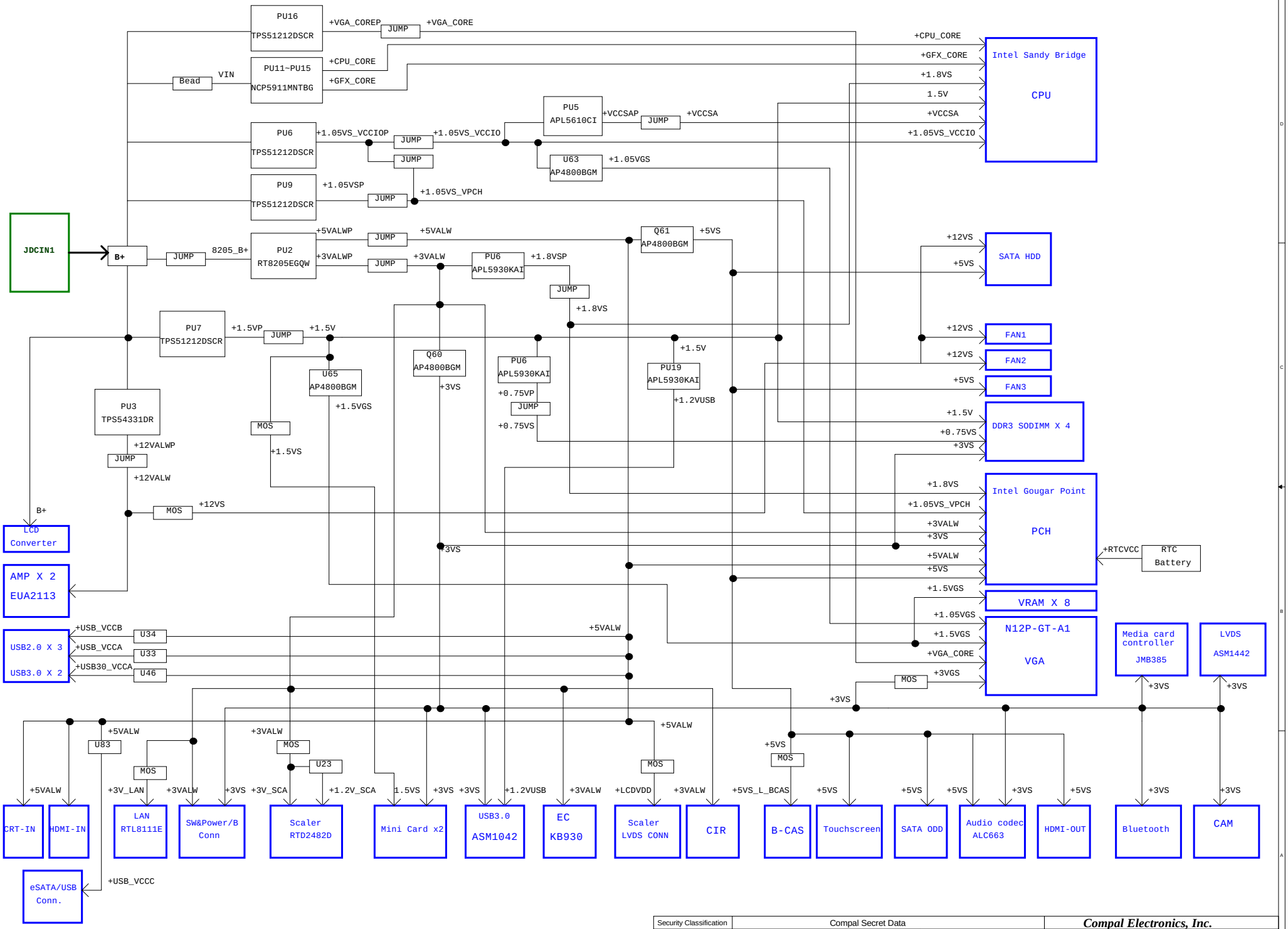


| | | | |
|---|---|---|---|
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**Compal Electronics, Inc.**

Title: **Power Tree**

| Size | Document Number | Rev |
|---|---|---|
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## Voltage Rails

| Power Plane | Description | S0 | S3 | S5 |
|---|---|---|---|---|
| VIN | Adapter power supply (19V) | N/A | N/A | N/A |
| B+ | AC power rail for power circuit. | N/A | N/A | N/A |
| +CPU_CORE | Core voltage for CPU | ON | OFF | OFF |
| +GFX_CORE | Graphics voltage for CPU | ON | OFF | OFF |
| +VCCSA | System Agent core voltage for CPU | ON | OFF | OFF |
| +1.05VS_VCCIO | 1.05V power rail for CPU | ON | OFF | OFF |
| +1.05VS_VPCH | 1.05V power rail for PCH | ON | OFF | OFF |
| +0.75VS | 0.75V power rail for DDR terminator | ON | OFF | OFF |
| +1.5V | 1.5V power rail for DDRIII | ON | ON | OFF |
| +1.5VS | 1.5V switched power rail | ON | OFF | OFF |
| +1.8VS | 1.8V switched power rail | ON | OFF | OFF |
| +3VALW | 3.3V always on power rail once AC plug in | ON | ON | ON |
| +3V_LAN | 3.3V power rail for LAN | ON | ON | OFF |
| +3VS | 3.3V switched power rail | ON | OFF | OFF |
| +3V_SCA | 3.3V switched power rail for scaler | ON | N/A | N/A |
| +1.2V_SCA | 1.2V switched power rail for scaler | ON | N/A | N/A |
| +1.2V_USB | 1.2V power rail for USB3.0 | ON | OFF | OFF |
| +5VALW | 5V always on power rail once AC plug in | ON | ON | ON |
| +5VS | 5V switched power rail | ON | OFF | OFF |
| +LCDVDD | 5V switched power rail for panel | ON | N/A | N/A |
| +RTCVCC | RTC power | ON | ON | ON |
| +3VGS | 3.3V power rail for GPU | ON | OFF | OFF |
| +VGA_CORE | Graphics power rail for GPU | ON | OFF | OFF |
| +1.05VGS | 1.05VS switched power rail for GPU | ON | OFF | OFF |
| +1.5VGS | 1.5VS power rail for GPU and VRAM | ON | OFF | OFF |
| +12VALW | 12V always on power rail once AC plug in | ON | N/A | N/A |
| +12VS | 5V switched power rail | ON | OFF | OFF |

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

## PCH SM Bus Address

| Power | Device | HEX | Address |
|---|---|---|---|
| +3VS | DDR(JDDRL2) | | 1010 000X b |
| +3VS | DDR(JDDRH1) | | 1010 010X b |

## PCH SML1 Bus Address

| Power | Device | HEX | Address |
|---|---|---|---|
| | VGA Ext. thermal sensor | | 1001_1010b |
| | VGA Int. thermal sensor (defaulta) | | 1001_1110b |

## EC SM Bus2 Address

| Power | Device | HEX | Address |
|---|---|---|---|
| | Scaler | | 0000_0101b |

| Board ID | Rb | $V_{BID}$ min | $V_{BID}$ typ | $V_{BID}$ max | EC AD3 |
|---|---|---|---|---|---|
| 0 | 0 | 0 V | 0 V | 0.155 V | 0x00 - 0x0C |
| 1 | 8.2K +/- 5% | 0.168 V | 0.250 V | 0.362 V | 0x0D - 0x1C |
| 2 | 18K +/- 5% | 0.375 V | 0.503 V | 0.621 V | 0x1D - 0x30 |
| 3 | 33K +/- 5% | 0.634 V | 0.819 V | 0.945 V | 0x31 - 0x49 |
| 4 | 56K +/- 5% | 0.958 V | 1.185 V | 1.359 V | 0x4A - 0x69 |
| 5 | 100K +/- 5% | 1.372 V | 1.650 V | 1.838 V | 0x6A - 0x8E |
| 6 | 200K +/- 5% | 1.851 V | 2.200 V | 2.420 V | 0x8F - 0xBB |
| 7 | NC | 2.433 V | 3.300 V | 3.300 V | 0xBC - 0xFF |

| STATE \ SIGNAL | SLP_S3# | SLP_S4# | SLP_S5# | +VALW | +VS |
|---|---|---|---|---|---|
| Full ON | HIGH | HIGH | HIGH | ON | ON |
| S1(Power On Suspend) | HIGH | HIGH | HIGH | ON | ON |
| S3 (Suspend to RAM) | LOW | HIGH | HIGH | ON | OFF |
| S4 (Suspend to Disk) | LOW | LOW | HIGH | ON | OFF |
| S5 (Soft OFF) | LOW | LOW | LOW | OFF | OFF |

## USB Port Table

| USB 2.0 | USB 1.1 | Port | Device |
|---|---|---|---|
| EHCI1 | UHCI0 | 0 | Co-lay w/USB30 PORT0 |
| | | 1 | Co-lay w/USB30 PORT1 |
| | UHCI1 | 2 | Touch Screen |
| | | 3 | Web Camera |
| | UHCI2 | 4 | eSATA+USB Conn |
| | | 5 | USB Conn 6 |
| | UHCI3 | 6 | Disabled on H61 |
| | | 7 | Disabled on H61 |
| EHCI2 | UHCI4 | 8 | USB Conn 4 |
| | | 9 | USB Conn 3 |
| | UHCI5 | 10 | Mini Card(TV Tuner) |
| | | 11 | Blue Tooth |
| | UHCI6 | 12 | Disabled on H61 |
| | | 13 | Disabled on H61 |

## SATA Port Table

| Port | | Device |
|---|---|---|
| 6G | 0 | HDD |
| | 1 | ODD |
| 3G | 2 | Disabled on H61 |
| | 3 | Disabled on H61 |
| | 4 | eSATA+USB Conn |
| | 5 | NC |

## PCIE Port Table

| Port | Device |
|---|---|
| 1 | NC |
| 2 | USB30 |
| 3 | WLAN |
| 4 | TV |
| 5 | Card reader |
| 6 | LAN |
| 7 | Disabled on H61 |
| 8 | Disabled on H61 |

## BOARD ID Table

| Board ID | PCB Revision |
|---|---|
| * 0 | 0.1 |
| 1 | 0.2 |
| 2 | |
| 3 | |
| 4 | |

## BOM Structure Table

| BTO Item | BOM Structure |
|---|---|
| ME components | CONN@ |
| VGA-N12P-GS | GS@ |
| VGA-N12P-GV | GV@ |
| UMA Only | UMA@ |
| DISCRETE ONLY | DIS@ |
| USB30 | USB30@ |
| No USB30 SKU | USB20@ |
| D-sub IN | VGAIN@ |
| HDMI IN | HDMIIN@ |
| HDMI OUT | HDMIO@ |
| HDMI OUT from DIS | HDMIOD@ |
| HDMI OUT from UMA | HDMIOU@ |
| VGA w/o Senergy | DISO@ |
| BCAS | TV@ |
| VRAM select | X76@ |
| VRAM 1G Hynix X7630488L01 | X76_HY1G@ |
| VRAM 1G Samsung X7630488L02 | X76_SAM1G@ |
| SKU IO Select | GPIO69_H@ |
| | GPIO69_L@ |
| | GPIO70_H@ |
| | GPIO70_L@ |
| | GPIO71_H@ |
| | GPIO71_L@ |
| Unpop | @ |
| LA-7521P 6 Layer PCB | 6LOCB@ |
| LA-7522P 8 Layer PCB | 8LPCB@ |

## SKU ID(Project) Table

| Project_ID2 (GPIO69) | Project_ID1 (GPIO70) | Project_ID0 (GPIO71) | Project | SKU | |
|---|---|---|---|---|---|
| 0 | 0 | 0 | PCA70 | UMA USB30 w/o HDMI 4319D588L03 | UMA@ USB30@ 8LPCB@ GPIO69_L@ GPIO70_L@ GPIO71_L@ |
| 0 | 0 | 1 | | DIS-Hynix USB30 w/ HDMI 4319D588L04 | GS@ DIS@ USB30@ VGAIN@ HDMIO@ HDMIOD@ DISO@ HDMIIN@ 8LPCB@ X76_HY1G@ GPIO69_L@ GPIO70_L@ GPIO71_H@ |
| 0 | 1 | 0 | | UMA USB30 w/ HDMI 4319D588L05 | UMA@ USB30@ VGAIN@ HDMIO@ HDMIOU@ DEBUG@ HDMIIN@ 8LPCB@ GPIO69_L@ GPIO70_H@ GPIO71_L@ |
| 0 | 1 | 1 | PCA61 | DIS-Hynix USB30 w/ HDMI 4319D588L11 | GV@ DIS@ USB30@ VGAIN@ HDMIO@ HDMIOD@ DISO@ HDMIIN@ 6LOCB@ GPIO69_L@ GPIO70_H@ GPIO71_H@ |
| 1 | 0 | 0 | | UMA USB20 w/ HDMI 4319D588L12 | UMA@ USB20@ VGAIN@ HDMIO@ HDMIOU@ DEBUG@ HDMIIN@ 6LOCB@ GPIO69_H@ GPIO70_L@ GPIO71_L@ |
| 1 | 0 | 1 | | X | |
| 1 | 1 | 0 | | X | |
| 1 | 1 | 1 | | X | |



| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |

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Title: Notes List

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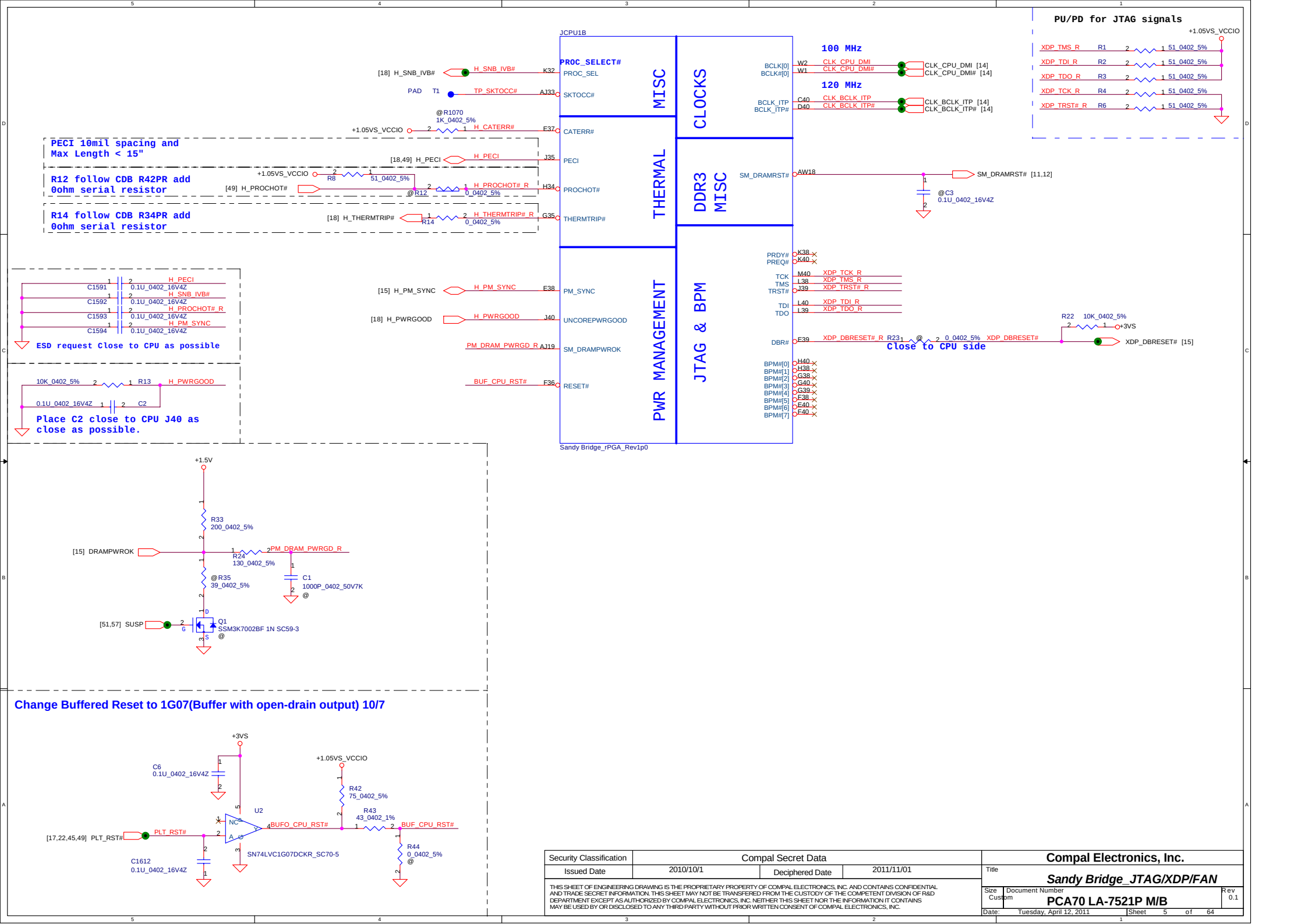
PU/PD for JTAG signals
+1.05VS_VCCIO
XDP_TMS_R R1 51_0402_5%
XDP_TDI_R R2 51_0402_5%
XDP_TDO_R R3 51_0402_5%
XDP_TCK_R R4 51_0402_5%
XDP_TRST#_R R6 51_0402_5%
JCPU1B
PROC_SELECT#
PROC_SEL K32
SKTOCC# AJ33
CATERR# E37
PECI J35
PROCHOT# H34
THERMTRIP# G35
PM_SYNC E38
UNCOREPWRGOOD J40
SM_DRAMPWROK AJ19
RESET# F36
MISC
THERMAL
PWR MANAGEMENT
CLOCKS
DDR3 MISC
JTAG & BPM
100 MHz
120 MHz
BCLK[0] W2 CLK_CPU_DMI
BCLK#[0] W1 CLK_CPU_DMI#
CLK_CPU_DMI [14]
CLK_CPU_DMI# [14]
BCLK_ITP C40 CLK_BCLK_ITP
BCLK_ITP# D40 CLK_BCLK_ITP#
CLK_BCLK_ITP [14]
CLK_BCLK_ITP# [14]
SM_DRAMRST# AW18
SM_DRAMRST# [11,12]
@C3 0.1U_0402_16V4Z
PRDY# K38
PREQ# K40
TCK M40 XDP_TCK_R
TMS L38 XDP_TMS_R
TRST# J39 XDP_TRST#_R
TDI L40 XDP_TDI_R
TDO L39 XDP_TDO_R
DBR# E39 XDP_DBRESET#_R R23 0_0402_5% XDP_DBRESET#
R22 10K_0402_5% +3VS
XDP_DBRESET# [15]
Close to CPU side
BPM#[0] H40
BPM#[1] H38
BPM#[2] G38
BPM#[3] G40
BPM#[4] G39
BPM#[5] F38
BPM#[6] E40
BPM#[7] F40
Sandy Bridge_rPGA_Rev1p0
[18] H_SNB_IVB# H_SNB_IVB#
PAD T1 TP_SKTOCC#
+1.05VS_VCCIO @R1070 1K_0402_5% H_CATERR#
[18,49] H_PECI H_PECI
+1.05VS_VCCIO R8 51_0402_5%
[49] H_PROCHOT# @R12 0_0402_5% H_PROCHOT#_R
[18] H_THERMTRIP# R14 0_0402_5% H_THERMTRIP#_R
PECI 10mil spacing and Max Length < 15"
R12 follow CDB R42PR add 0ohm serial resistor
R14 follow CDB R34PR add 0ohm serial resistor
[15] H_PM_SYNC H_PM_SYNC
[18] H_PWRGOOD H_PWRGOOD
PM_DRAM_PWRGD_R
BUF_CPU_RST#
C1591 H_PECI 0.1U_0402_16V4Z
C1592 H_SNB_IVB# 0.1U_0402_16V4Z
C1593 H_PROCHOT#_R 0.1U_0402_16V4Z
C1594 H_PM_SYNC 0.1U_0402_16V4Z
ESD request Close to CPU as possible
10K_0402_5% R13 H_PWRGOOD
0.1U_0402_16V4Z C2
Place C2 close to CPU J40 as close as possible.
+1.5V
R33 200_0402_5%
[15] DRAMPWROK
R24 130_0402_5% PM_DRAM_PWRGD_R
@R35 39_0402_5%
C1 1000P_0402_50V7K @
[51,57] SUSP
Q1 SSM3K7002BF 1N SC59-3 @
Change Buffered Reset to 1G07(Buffer with open-drain output) 10/7
+3VS
C6 0.1U_0402_16V4Z
+1.05VS_VCCIO
R42 75_0402_5%
R43 43_0402_1%
U2
[17,22,45,49] PLT_RST#
PLT_RST#
BUFO_CPU_RST#
BUF_CPU_RST#
SN74LVC1G07DCKR_SC70-5
C1612 0.1U_0402_16V4Z
R44 0_0402_5% @
Security Classification
Compal Secret Data
Issued Date
2010/10/1
Deciphered Date
2011/11/01
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Title
Sandy Bridge_JTAG/XDP/FAN
Size Custom
Document Number
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PEG_ICOMPI and RCOMPO signals should be shorted and routed with
- max length = 500 mils
- typical impedance = 43 m ohm (4 mils/15mils)
PEG_ICOMPO signals should be routed with
- max length = 500 mils
- typical impedance = 14.5 m ohm (12 mils/15mils)

SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLETRACE TO R?
ROUTE B5 TO R? AS A SEPERATE TRACE

Intel confirm pull high is correct

+1.05VS_VCCIO

R45 24.9_0402_1%

JCPU1A

DMI

Intel(R) FDI

PCI EXPRESS* - GRAPHICS

PCI-EXPRESS

PEG_COMPI
PEG_ICOMPO
PEG_RCOMPO
B4 PEG_COMP
B5
C4

[15] DMI_PTX_CRX_N0 DMI_PTX_CRX_N0 W4 DMI_RX#[0]
[15] DMI_PTX_CRX_N1 DMI_PTX_CRX_N1 V4 DMI_RX#[1]
[15] DMI_PTX_CRX_N2 DMI_PTX_CRX_N2 Y4 DMI_RX#[2]
[15] DMI_PTX_CRX_N3 DMI_PTX_CRX_N3 AA5 DMI_RX#[3]

[15] DMI_PTX_CRX_P0 DMI_PTX_CRX_P0 W5 DMI_RX[0]
[15] DMI_PTX_CRX_P1 DMI_PTX_CRX_P1 V3 DMI_RX[1]
[15] DMI_PTX_CRX_P2 DMI_PTX_CRX_P2 Y3 DMI_RX[2]
[15] DMI_PTX_CRX_P3 DMI_PTX_CRX_P3 AA4 DMI_RX[3]

[15] DMI_CTX_PRX_N0 DMI_CTX_PRX_N0 V6 DMI_TX#[0]
[15] DMI_CTX_PRX_N1 DMI_CTX_PRX_N1 W8 DMI_TX#[1]
[15] DMI_CTX_PRX_N2 DMI_CTX_PRX_N2 Y7 DMI_TX#[2]
[15] DMI_CTX_PRX_N3 DMI_CTX_PRX_N3 AA8 DMI_TX#[3]

[15] DMI_CTX_PRX_P0 DMI_CTX_PRX_P0 V7 DMI_TX[0]
[15] DMI_CTX_PRX_P1 DMI_CTX_PRX_P1 W7 DMI_TX[1]
[15] DMI_CTX_PRX_P2 DMI_CTX_PRX_P2 Y6 DMI_TX[2]
[15] DMI_CTX_PRX_P3 DMI_CTX_PRX_P3 AA7 DMI_TX[3]

[15] FDI_CTX_PRX_N0 FDI_CTX_PRX_N0 AC7 FDI_TX#[0]
[15] FDI_CTX_PRX_N1 FDI_CTX_PRX_N1 AC3 FDI_TX#[1]
[15] FDI_CTX_PRX_N2 FDI_CTX_PRX_N2 AD1 FDI_TX#[2]
[15] FDI_CTX_PRX_N3 FDI_CTX_PRX_N3 AD3 FDI_TX#[3]
[15] FDI_CTX_PRX_N4 FDI_CTX_PRX_N4 AD6 FDI_TX#[4]
[15] FDI_CTX_PRX_N5 FDI_CTX_PRX_N5 AE8 FDI_TX#[5]
[15] FDI_CTX_PRX_N6 FDI_CTX_PRX_N6 AF2 FDI_TX#[6]
[15] FDI_CTX_PRX_N7 FDI_CTX_PRX_N7 AG1 FDI_TX#[7]

[15] FDI_CTX_PRX_P0 FDI_CTX_PRX_P0 AC8 FDI_TX[0]
[15] FDI_CTX_PRX_P1 FDI_CTX_PRX_P1 AC2 FDI_TX[1]
[15] FDI_CTX_PRX_P2 FDI_CTX_PRX_P2 AD2 FDI_TX[2]
[15] FDI_CTX_PRX_P3 FDI_CTX_PRX_P3 AD4 FDI_TX[3]
[15] FDI_CTX_PRX_P4 FDI_CTX_PRX_P4 AD7 FDI_TX[4]
[15] FDI_CTX_PRX_P5 FDI_CTX_PRX_P5 AE7 FDI_TX[5]
[15] FDI_CTX_PRX_P6 FDI_CTX_PRX_P6 AE3 FDI_TX[6]
[15] FDI_CTX_PRX_P7 FDI_CTX_PRX_P7 AG2 FDI_TX[7]

[15] FDI_FSYNC0 FDI_FSYNC0 AC5 FDI_FSYNC[0]
[15] FDI_FSYNC1 FDI_FSYNC1 AE5 FDI_FSYNC[1]

[15] FDI_INT FDI_INT AG3 FDI_INT

[15] FDI_LSYNC0 FDI_LSYNC0 AC4 FDI_LSYNC[0]
[15] FDI_LSYNC1 FDI_LSYNC1 AE4 FDI_LSYNC[1]

+1.05VS_VCCIO R46 1 2 24.9_0402_1% FDI_COMP AE2 FDI_COMPIO
AE1 FDI_ICOMPO

FDI_COMP signals should be shorted near balls and routed with width 10mils, length<250mils.

P3 PE_RX[0]
R2 PE_RX[1]
T4 PE_RX[2]
U2 PE_RX[3]

P4 PE_RX#[0]
R1 PE_RX#[1]
T3 PE_RX#[2]
U1 PE_RX#[3]

P8 PE_TX[0]
T7 PE_TX[1]
R6 PE_TX[2]
U5 PE_TX[3]

P7 PE_TX#[0]
T8 PE_TX#[1]
R5 PE_TX#[2]
U6 PE_TX#[3]

7/20 PE_RX[0~3]/PE_RX#[0~3] PE_TX[0~3]/PE_TX#[0~3] only use on Server/Workstation.

Sandy Bridge_rPGA_Rev1p0

PEG_RX#[0] B12 PCIE_GTX_C_CRX_N15
PEG_RX#[1] D11 PCIE_GTX_C_CRX_N14
PEG_RX#[2] C9 PCIE_GTX_C_CRX_N13
PEG_RX#[3] E9 PCIE_GTX_C_CRX_N12
PEG_RX#[4] B7 PCIE_GTX_C_CRX_N11
PEG_RX#[5] C5 PCIE_GTX_C_CRX_N10
PEG_RX#[6] A6 PCIE_GTX_C_CRX_N9
PEG_RX#[7] E1 PCIE_GTX_C_CRX_N8
PEG_RX#[8] F3 PCIE_GTX_C_CRX_N7
PEG_RX#[9] G1 PCIE_GTX_C_CRX_N6
PEG_RX#[10] H4 PCIE_GTX_C_CRX_N5
PEG_RX#[11] J2 PCIE_GTX_C_CRX_N4
PEG_RX#[12] K4 PCIE_GTX_C_CRX_N3
PEG_RX#[13] L2 PCIE_GTX_C_CRX_N2
PEG_RX#[14] M4 PCIE_GTX_C_CRX_N1
PEG_RX#[15] N2 PCIE_GTX_C_CRX_N0

PCIE_GTX_C_CRX_N[0..15] [22]

PEG_RX[0] B11 PCIE_GTX_C_CRX_P15
PEG_RX[1] D12 PCIE_GTX_C_CRX_P14
PEG_RX[2] C10 PCIE_GTX_C_CRX_P13
PEG_RX[3] E10 PCIE_GTX_C_CRX_P12
PEG_RX[4] B8 PCIE_GTX_C_CRX_P11
PEG_RX[5] C6 PCIE_GTX_C_CRX_P10
PEG_RX[6] A5 PCIE_GTX_C_CRX_P9
PEG_RX[7] E2 PCIE_GTX_C_CRX_P8
PEG_RX[8] F4 PCIE_GTX_C_CRX_P7
PEG_RX[9] G2 PCIE_GTX_C_CRX_P6
PEG_RX[10] H3 PCIE_GTX_C_CRX_P5
PEG_RX[11] J1 PCIE_GTX_C_CRX_P4
PEG_RX[12] K3 PCIE_GTX_C_CRX_P3
PEG_RX[13] L1 PCIE_GTX_C_CRX_P2
PEG_RX[14] M3 PCIE_GTX_C_CRX_P1
PEG_RX[15] N1 PCIE_GTX_C_CRX_P0

PCIE_GTX_C_CRX_P[0..15] [22]

PEG_TX[0] C14 PCIE_CTX_GRX_N15 C7 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_N15
PEG_TX[1] E13 PCIE_CTX_GRX_N14 C8 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_N14
PEG_TX[2] G13 PCIE_CTX_GRX_N13 C9 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_N13
PEG_TX[3] F11 PCIE_CTX_GRX_N12 C10 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_N12
PEG_TX[4] J13 PCIE_CTX_GRX_N11 C11 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_N11
PEG_TX[5] D7 PCIE_CTX_GRX_N10 C12 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_N10
PEG_TX[6] C3 PCIE_CTX_GRX_N9 C13 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_N9
PEG_TX[7] E5 PCIE_CTX_GRX_N8 C14 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_N8
PEG_TX[8] F7 PCIE_CTX_GRX_N7 C15 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_N7
PEG_TX[9] G9 PCIE_CTX_GRX_N6 C16 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_N6
PEG_TX[10] G6 PCIE_CTX_GRX_N5 C17 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_N5
PEG_TX[11] K8 PCIE_CTX_GRX_N4 C18 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_N4
PEG_TX[12] J6 PCIE_CTX_GRX_N3 C19 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_N3
PEG_TX[13] M7 PCIE_CTX_GRX_N2 C20 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_N2
PEG_TX[14] L5 PCIE_CTX_GRX_N1 C21 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_N1
PEG_TX[15] N6 PCIE_CTX_GRX_N0 C22 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_N0

PCIE_CTX_C_GRX_N[0..15] [22]

PEG_TX[0] C13 PCIE_CTX_GRX_P15 C23 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_P15
PEG_TX[1] E14 PCIE_CTX_GRX_P14 C24 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_P14
PEG_TX[2] G14 PCIE_CTX_GRX_P13 C25 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_P13
PEG_TX[3] F12 PCIE_CTX_GRX_P12 C26 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_P12
PEG_TX[4] J14 PCIE_CTX_GRX_P11 C27 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_P11
PEG_TX[5] D8 PCIE_CTX_GRX_P10 C28 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_P10
PEG_TX[6] D3 PCIE_CTX_GRX_P9 C29 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_P9
PEG_TX[7] E6 PCIE_CTX_GRX_P8 C30 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_P8
PEG_TX[8] F8 PCIE_CTX_GRX_P7 C31 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_P7
PEG_TX[9] G10 PCIE_CTX_GRX_P6 C32 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_P6
PEG_TX[10] G5 PCIE_CTX_GRX_P5 C33 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_P5
PEG_TX[11] K7 PCIE_CTX_GRX_P4 C34 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_P4
PEG_TX[12] J5 PCIE_CTX_GRX_P3 C35 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_P3
PEG_TX[13] M8 PCIE_CTX_GRX_P2 C36 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_P2
PEG_TX[14] L6 PCIE_CTX_GRX_P1 C37 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_P1
PEG_TX[15] N5 PCIE_CTX_GRX_P0 C38 1 2 DIS@ 0.1U_0402_16V7K PCIE_CTX_C_GRX_P0

PCIE_CTX_C_GRX_P[0..15] [22]

Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIE Gen3 (8GT/s)

Close to CPU

FDI_INT 1 @ 2 R47 1K_0402_5%
FDI_FSYNC0 1 @ 2 R48 1K_0402_5%
FDI_FSYNC1 1 @ 2 R49 1K_0402_5%
FDI_LSYNC0 1 @ 2 R50 1K_0402_5%
FDI_LSYNC1 1 @ 2 R51 1K_0402_5%

Leverage LA-6831 and LA6951(B520) used 1000P connect to GND to substitute for 1K ohm PD resistor.

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |



Compal Electronics, Inc.

Title: Sandy Bridge_DMI/PEG/FDI

| Size | Document Number | Rev |
|---|---|---|
| Custom | PCA70 LA-7521P M/B | 0.1 |

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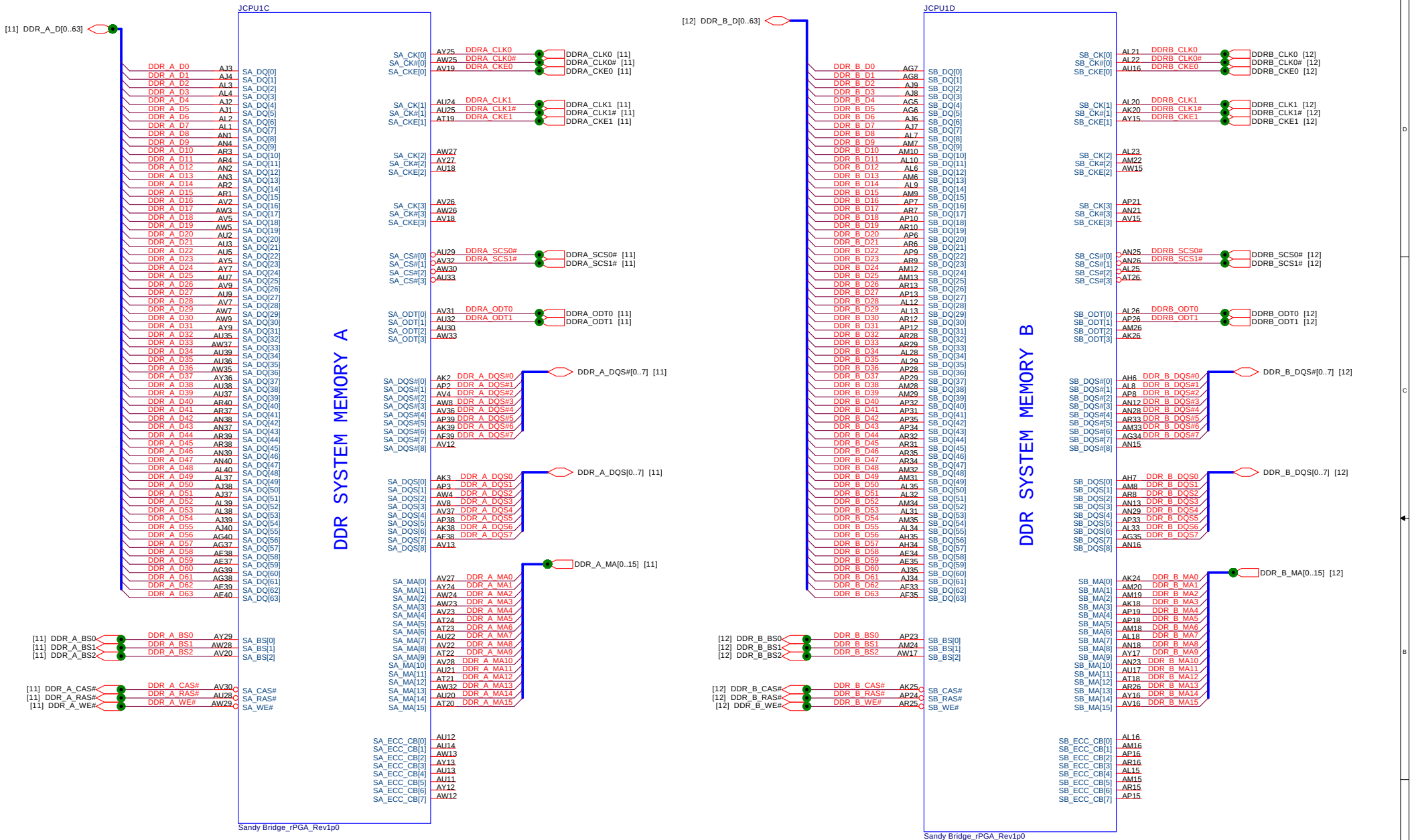


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|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |



**Compal Electronics, Inc.**

Title: ***Sandy Bridge_DDR3***

| Size | Document Number | Rev |
|---|---|---|
| Custom | PCA70 LA-7521P M/B | 0.1 |

Date: Tuesday, April 12, 2011 | Sheet 7 of 64

# POWER

JCPU1F
76A (Quad Core 65W)
8.5A

## CORE SUPPLY

### PEG AND DDR

VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7 VCCIO8 VCCIO9 VCCIO10 VCCIO11 VCCIO12 VCCIO13 VCCIO14 VCCIO15 VCCIO16 VCCIO17 VCCIO18 VCCIO19 VCCIO20 VCCIO21 VCCIO22 VCCIO23 VCCIO24 VCCIO25 VCCIO26 VCCIO27 VCCIO28 VCCIO29 VCCIO30 VCCIO31 VCCIO32 VCCIO33 VCCIO34 VCCIO35 VCCIO36 VCCIO37 VCCIO38 VCCIO39 VCCIO40 VCCIO41 VCCIO42 VCCIO43 VCCIO44 VCCIO45

### SVID

VIDALERT# VIDSCLK VIDSOUT

### SENSE LINES

VCC_SENSE VSS_SENSE

VCCIO_SENSE VSSIO_SENSE

VCC121 VCC122 VCC123 VCC124 VCC125 VCC126 VCC127 VCC128 VCC129 VCC130 VCC131 VCC132 VCC133 VCC134 VCC135 VCC136 VCC137 VCC138 VCC139 VCC140 VCC141 VCC142 VCC143 VCC144 VCC145 VCC146 VCC147 VCC148 VCC149 VCC150 VCC151 VCC152 VCC153 VCC154 VCC155 VCC156 VCC157 VCC158 VCC159 VCC160 VCC161

VSS_SENSE_VCCIO

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100 VCC101 VCC102 VCC103 VCC104 VCC105 VCC106 VCC107 VCC108 VCC109 VCC110 VCC111 VCC112 VCC113 VCC114 VCC115 VCC116 VCC117 VCC118 VCC119 VCC120

Sandy Bridge_rPGA_Rev1p0

## TOP Socket Cavity

+1.05VS_VCCIO

**+1.05VS_VCCP Decoupling:**
**3X 560U (6m ohm), 9X 22U**

22U_0805_6.3V6M: C39 C40 C41 C42 C43 C44 C45 C46 C47

560U_2.5V_M: C48 C49 C50

HR's R52=130 ohm
SB CRB suggst 110ohm

90.9_0402_1%
R52 110_0402_5%
R53 @
R54 75_0402_5%
R55 43_0402_1%

**Pull high resistor close to CPU**
**SVID signal 50 ohm impedance**
**spacing >12mil length 3-6"**

H_CPU_SVIDALRT#
VR_SVID_CLK_R
VR_SVID_DAT_R
R1037 0_0402_5%
R1038 0_0402_5%

VR_SVID_ALRT# [58]
VR_SVID_CLK [58]
VR_SVID_DAT [58]

VCCSENSE [58]
VSSSENSE [58]

VCCIO_SENSE
VCCIO_SENSE [54]
R56 100_0402_1%

+CPU_CORE

**+CPU_CORE Decoupling:**
**5X 560U (4m ohm), 2X330U, 18X 22U**

## TOP Socket Edge

C52 560U_2.5V_M
C54 560U_2.5V_M
C51 560U_2.5V_M
C53 560U_2.5V_M
C59 560U_2.5V_M

## Bottom Socket Edge

C55 330U_D2_2V_Y
@C56
C58 330U_D2_2VM_R6M
@ 330U_D2_2V_Y

## 14 pcs in TOP and 4pcs in BOT Socket Cavity

22U_0805_6.3V6M: C60 C61 C62 C63 C64 C65 C66 C67 C68 C69 C70 C71 C72 C73 C74 C75 C76 C77

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |



**Compal Electronics, Inc.**

Title: *Sandy Bridge_POWER-1*

Size: Custom | Document Number: PCA70 LA-7521P M/B | Rev: 0.1

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# POWER

**+GFX_CORE Decoupling:**
**2X 470U (4m ohm), 12X 22U**

**Bottom Socket Edge**

**Top Socket Edge**

**Top Socket Cavity**

**Bottom Socket Edge**

**VCCPLL Decoupling:**
**1X 220U, 2X 10U**

**+V_SM_VREF should have 20 mil trace width**

**+1.5V Decoupling:**
**3X 330U , 9X 22U**

**TOP Socket Cavity**

**+VCCSA Decoupling:**
**1X 560U, 2X 10U**

| VCCSA_VID1 | +VCCSA |
|---|---|
| 0 | 0.925 V (Default) |
| 1 | 0.85 V |

**R66,R67 should place close to DIMM for minimum stubs trace**

JCPU1G

35A
VCCAXG1 VCCAXG2 VCCAXG3 VCCAXG4 VCCAXG5 VCCAXG6 VCCAXG7 VCCAXG8 VCCAXG9 VCCAXG10 VCCAXG11 VCCAXG12 VCCAXG13 VCCAXG14 VCCAXG15 VCCAXG16 VCCAXG17 VCCAXG18 VCCAXG19 VCCAXG20 VCCAXG21 VCCAXG22 VCCAXG23 VCCAXG24 VCCAXG25 VCCAXG26 VCCAXG27 VCCAXG28 VCCAXG29 VCCAXG30 VCCAXG31 VCCAXG32 VCCAXG33 VCCAXG34 VCCAXG35 VCCAXG36 VCCAXG37 VCCAXG38 VCCAXG39 VCCAXG40 VCCAXG41 VCCAXG42 VCCAXG43 VCCAXG44

GRAPHICS

VCCAXG_SENSE VSSAXG_SENSE

SENSE LINES

VCC_AXG_SENSE [58]
VSS_AXG_SENSE [58]

SM_VREF

VREF

4.75A
VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15 VDDQ16 VDDQ17 VDDQ18 VDDQ19 VDDQ20 VDDQ21 VDDQ22 VDDQ23

DDR3 -1.5V RAILS

8.8A
VCCSA1 VCCSA2 VCCSA3 VCCSA4 VCCSA5 VCCSA6 VCCSA7 VCCSA8 VCCSA9 VCCSA10 VCCSA11

SA RAIL

VCCSA_SENSE VCCSA_VID

VCCSA_SENSE [56]
VCCSAP_VID1 [56]

1.5A
VCCPLL1 VCCPLL2

1.8V RAIL

FC_AH1 FC_AH4

MISC

Sandy Bridge_rPGA_Rev1p0

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |



Compal Electronics, Inc.

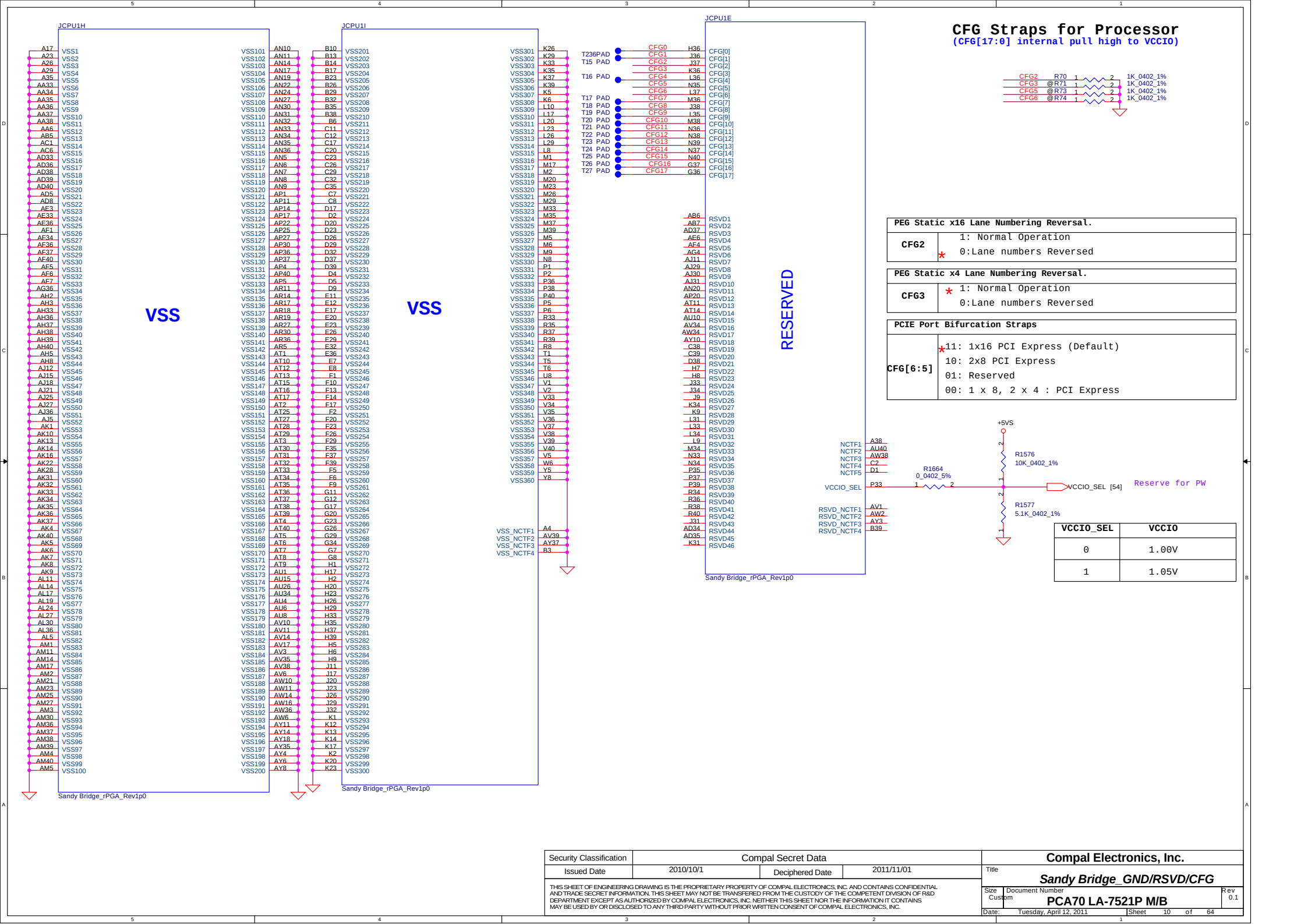
Title: *Sandy Bridge_POWER-2*

Size: Custom | Document Number: PCA70 LA-7521P M/B | Rev: 0.1

Date: Tuesday, April 12, 2011 | Sheet 9 of 64

# CFG Straps for Processor

**(CFG[17:0] internal pull high to VCCIO)**




| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |



**Compal Electronics, Inc.**

Title: ***Sandy Bridge_GND/RSVD/CFG***

| Size | Document Number | Rev |
|---|---|---|
| Custom | PCA70 LA-7521P M/B | 0.1 |

Date: Tuesday, April 12, 2011 Sheet 10 of 64

# CHA SO-DIMM 0(A0)

[7] DDR_A_DQS[0..7]
[7] DDR_A_DQS#[0..7]
[7] DDR_A_D[0..63]
[7] DDR_A_MA[0..15]

R91 1K_0402_1% +1.5V +VREF_DQA
R93 1K_0402_1%
C114 0.1U_0402_16V4Z
C115 2.2U_0603_6.3V6K
Close to JDDRL.1

JDDRL2
CONN@
TYCO_2-2013290-1

**Layout Note:**
**Place near JDDRL1.203 and 204**

+0.75VS
C134 10U_0805_6.3V6M
C135 1U_0402_6.3V6K
C136 1U_0402_6.3V6K
C139 1U_0402_6.3V6K
C140 1U_0402_6.3V6K

**Layout Note:**
**Place near JDDRL1**

+1.5V
C143 390U_2.5V_M_R10
C145 10U_0805_6.3V6M
C147 10U_0805_6.3V6M
C149 10U_0805_6.3V6M
C151 10U_0805_6.3V6M
C152 10U_0805_6.3V6M
C153 10U_0805_6.3V6M

**Layout Note: Place these 4 Caps near Command and Control signals of JDDRL1**

+1.5V
C144 0.1U_0402_16V4Z
C146 0.1U_0402_16V4Z
C148 0.1U_0402_16V4Z
C150 0.1U_0402_16V4Z

R97 10K_0402_5% +3VS
C154 2.2U_0603_6.3V6K
C155 0.1U_0402_16V4Z
R98 10K_0402_5% +0.75VS

R94 1K_0402_1% +1.5V
R96 1K_0402_1%
C137 2.2U_0603_6.3V6K
C138 0.1U_0402_16V4Z
close to JDDRL1.126

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |



**Compal Electronics, Inc.**

Title: ***DDRIII-SODIMMA***

Size: Custom | Document Number: **PCA70 LA-7521P M/B** | Rev: 0.1

Date: Tuesday, April 12, 2011 | Sheet 11 of 64

# CHB SO-DIMM 0(A4)

[7] DDR_B_DQS#[0..7]
[7] DDR_B_DQS[0..7]
[7] DDR_B_D[0..63]
[7] DDR_B_MA[0..15]

R101 1K_0402_1% +1.5V +VREF_DQB
R103 1K_0402_1%
C158 2.2U_0603_6.3V6K
C159 0.1U_0402_16V4Z
Close to JDDRL2.1

JDDRH1 TYCO_2-2013311-1 @

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | VREF_DQ | 1 | 2 | VSS1 | | DDR_B_D4 | |
| | VSS2 | 3 | 4 | DQ4 | | DDR_B_D5 | |
| DDR_B_D0 | DQ0 | 5 | 6 | DQ5 | | | |
| DDR_B_D1 | DQ1 | 7 | 8 | VSS3 | | | |
| | VSS4 | 9 | 10 | DQS#0 | | DDR_B_DQS#0 | |
| | DM0 | 11 | 12 | DQS0 | | DDR_B_DQS0 | |
| | VSS5 | 13 | 14 | VSS6 | | | |
| DDR_B_D2 | DQ2 | 15 | 16 | DQ6 | | DDR_B_D6 | |
| DDR_B_D3 | DQ3 | 17 | 18 | DQ7 | | DDR_B_D7 | |
| | VSS7 | 19 | 20 | VSS8 | | | |
| DDR_B_D8 | DQ8 | 21 | 22 | DQ12 | | DDR_B_D12 | |
| DDR_B_D9 | DQ9 | 23 | 24 | DQ13 | | DDR_B_D13 | |
| | VSS9 | 25 | 26 | VSS10 | | | |
| DDR_B_DQS#1 | DQS#1 | 27 | 28 | DM1 | | | |
| DDR_B_DQS1 | DQS1 | 29 | 30 | RESET# | | SM_DRAMRST# | SM_DRAMRST# [5,11] |
| | VSS11 | 31 | 32 | VSS12 | | | |
| DDR_B_D10 | DQ10 | 33 | 34 | DQ14 | | DDR_B_D14 | |
| DDR_B_D11 | DQ11 | 35 | 36 | DQ15 | | DDR_B_D15 | |
| | VSS13 | 37 | 38 | VSS14 | | | |
| DDR_B_D16 | DQ16 | 39 | 40 | DQ20 | | DDR_B_D20 | |
| DDR_B_D17 | DQ17 | 41 | 42 | DQ21 | | DDR_B_D21 | |
| | VSS15 | 43 | 44 | VSS16 | | | |
| DDR_B_DQS#2 | DQS#2 | 45 | 46 | DM2 | | | |
| DDR_B_DQS2 | DQS2 | 47 | 48 | VSS17 | | | |
| | VSS18 | 49 | 50 | DQ22 | | DDR_B_D22 | |
| DDR_B_D18 | DQ18 | 51 | 52 | DQ23 | | DDR_B_D23 | |
| DDR_B_D19 | DQ19 | 53 | 54 | VSS19 | | | |
| | VSS20 | 55 | 56 | DQ28 | | DDR_B_D28 | |
| DDR_B_D24 | DQ24 | 57 | 58 | DQ29 | | DDR_B_D29 | |
| DDR_B_D25 | DQ25 | 59 | 60 | VSS21 | | | |
| | VSS22 | 61 | 62 | DQS#3 | | DDR_B_DQS#3 | |
| | DM3 | 63 | 64 | DQS3 | | DDR_B_DQS3 | |
| | VSS23 | 65 | 66 | VSS24 | | | |
| DDR_B_D26 | DQ26 | 67 | 68 | DQ30 | | DDR_B_D30 | |
| DDR_B_D27 | DQ27 | 69 | 70 | DQ31 | | DDR_B_D31 | |
| | VSS25 | 71 | 72 | VSS26 | | | |
| [7] DDRB_CKE0 | DDRB_CKE0 | 73 | 74 | CKE1 | | DDRB_CKE1 | DDRB_CKE1 [7] |
| | CKE0 | 75 | 76 | VDD2 | | | |
| | VDD1 | 77 | 78 | A15 | | DDR_B_MA15 | |
| [7] DDR_B_BS2 | NC1 | 79 | 80 | A14 | | DDR_B_MA14 | |
| DDR_B_MA12 | BA2 | 81 | 82 | VDD4 | | | |
| DDR_B_MA9 | VDD3 | 83 | 84 | A11 | | DDR_B_MA11 | |
| | A12/BC# | 85 | 86 | A7 | | DDR_B_MA7 | |
| DDR_B_MA8 | A9 | 87 | 88 | VDD6 | | | |
| DDR_B_MA5 | VDD5 | 89 | 90 | A6 | | DDR_B_MA6 | |
| | A8 | 91 | 92 | A4 | | DDR_B_MA4 | |
| DDR_B_MA3 | A5 | 93 | 94 | VDD8 | | | |
| DDR_B_MA1 | VDD7 | 95 | 96 | A2 | | DDR_B_MA2 | |
| | A3 | 97 | 98 | A0 | | DDR_B_MA0 | |
| | A1 | 99 | 100 | | | | |
| [7] DDRB_CLK0 | VDD9 | 101 | 102 | VDD10 | | | |
| [7] DDRB_CLK0# | CK0 | 103 | 104 | CK1 | | DDRB_CLK1 | DDRB_CLK1 [7] |
| | CK0# | 105 | 106 | CK1# | | DDRB_CLK1# | DDRB_CLK1# [7] |
| DDR_B_MA10 | VDD11 | 107 | 108 | VDD12 | | | |
| [7] DDR_B_BS0 | A10/AP | 109 | 110 | BA1 | | DDR_B_BS1 | DDR_B_BS1 [7] |
| | BA0 | 111 | 112 | RAS# | | DDR_B_RAS# | DDR_B_RAS# [7] |
| [7] DDR_B_WE# | VDD13 | 113 | 114 | VDD14 | | | |
| [7] DDR_B_CAS# | WE# | 115 | 116 | S0# | | DDRB_SCS0# | DDRB_SCS0# [7] |
| DDR_B_MA13 | CAS# | 117 | 118 | ODT0 | | DDRB_ODT0 | DDRB_ODT0 [7] |
| [7] DDRB_SCS1# | VDD15 | 119 | 120 | VDD16 | | | |
| | A13 | 121 | 122 | ODT1 | | DDRB_ODT1 | DDRB_ODT1 [7] |
| | S1# | 123 | 124 | NC2 | | | |
| | VDD17 | 125 | 126 | VDD18 | | | |
| | NCTEST | 127 | 128 | VREF_CA | | +VREF_CAB | |
| | VSS27 | 129 | 130 | VSS28 | | | |
| DDR_B_D37 | DQ32 | 131 | 132 | DQ36 | | DDR_B_D32 | |
| DDR_B_D36 | DQ33 | 133 | 134 | DQ37 | | DDR_B_D33 | |
| | VSS29 | 135 | 136 | VSS30 | | | |
| DDR_B_DQS#4 | DQS#4 | 137 | 138 | DM4 | | | |
| DDR_B_DQS4 | DQS4 | 139 | 140 | VSS31 | | | |
| | VSS32 | 141 | 142 | DQ38 | | DDR_B_D38 | |
| DDR_B_D34 | DQ34 | 143 | 144 | DQ39 | | DDR_B_D39 | |
| DDR_B_D35 | DQ35 | 145 | 146 | VSS33 | | | |
| | VSS34 | 147 | 148 | DQ44 | | DDR_B_D44 | |
| DDR_B_D40 | DQ40 | 149 | 150 | DQ45 | | DDR_B_D45 | |
| DDR_B_D41 | DQ41 | 151 | 152 | VSS35 | | | |
| | VSS36 | 153 | 154 | DQS#5 | | DDR_B_DQS#5 | |
| | DM5 | 155 | 156 | DQS5 | | DDR_B_DQS5 | |
| | VSS37 | 157 | 158 | VSS38 | | | |
| DDR_B_D42 | DQ42 | 159 | 160 | DQ46 | | DDR_B_D46 | |
| DDR_B_D43 | DQ43 | 161 | 162 | DQ47 | | DDR_B_D47 | |
| | VSS39 | 163 | 164 | VSS40 | | | |
| DDR_B_D48 | DQ48 | 165 | 166 | DQ52 | | DDR_B_D52 | |
| DDR_B_D49 | DQ49 | 167 | 168 | DQ53 | | DDR_B_D53 | |
| | VSS41 | 169 | 170 | VSS42 | | | |
| DDR_B_DQS#6 | DQS#6 | 171 | 172 | DM6 | | | |
| DDR_B_DQS6 | DQS6 | 173 | 174 | VSS43 | | | |
| | VSS44 | 175 | 176 | DQ54 | | DDR_B_D50 | |
| DDR_B_D54 | DQ50 | 177 | 178 | DQ55 | | DDR_B_D51 | |
| DDR_B_D55 | DQ51 | 179 | 180 | VSS45 | | | |
| | VSS46 | 181 | 182 | DQ60 | | DDR_B_D60 | |
| DDR_B_D56 | DQ56 | 183 | 184 | DQ61 | | DDR_B_D61 | |
| DDR_B_D57 | DQ57 | 185 | 186 | VSS47 | | | |
| | VSS48 | 187 | 188 | DQS#7 | | DDR_B_DQS#7 | |
| | DM7 | 189 | 190 | DQS7 | | DDR_B_DQS7 | |
| | VSS49 | 191 | 192 | VSS50 | | | |
| DDR_B_D58 | DQ58 | 193 | 194 | DQ62 | | DDR_B_D62 | |
| DDR_B_D59 | DQ59 | 195 | 196 | DQ63 | | DDR_B_D63 | |
| | VSS51 | 197 | 198 | VSS52 | | | |
| | SA0 | 199 | 200 | EVENT# | | PM_SMBDATA | PM_SMBDATA [11,14,40] |
| | VDDSPD | 201 | 202 | SDA | | PM_SMBCLK | PM_SMBCLK [11,14,40] |
| | SA1 | 203 | 204 | SCL | | | |
| | VTT1 | 205 | 206 | VTT2 | | +0.75VS | +0.75VS |
| | G1 | | | G2 | | | |

R107 10K_0402_5% +3VS
R108 10K_0402_5% +0.75VS
C198 2.2U_0603_6.3V6K
C199 0.1U_0402_16V4Z

R104 1K_0402_1% +1.5V
R106 1K_0402_1%
C180 2.2U_0603_6.3V6K
C181 0.1U_0402_16V4Z
Close to JDDRL2.126

**Layout Note:**
**Place near JDDRL2.203 and 204**

+0.75VS
C178 10U_0805_6.3V6M
C179 1U_0402_6.3V6K
C182 1U_0402_6.3V6K
C183 1U_0402_6.3V6K
C184 1U_0402_6.3V6K

**Layout Note:**
**Place near JDDRL2**

**Layout Note: Place these 4 Caps near Command and Control signals of JDDRL2**

+1.5V
C187 390U_2.5V_M_R10
C189 10U_0805_6.3V6M
C191 10U_0805_6.3V6M
C193 10U_0805_6.3V6M
C195 10U_0805_6.3V6M
C196 10U_0805_6.3V6M
C197 10U_0805_6.3V6M

+1.5V
C188 0.1U_0402_16V4Z
C190 0.1U_0402_16V4Z
C192 0.1U_0402_16V4Z
C194 0.1U_0402_16V4Z

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |



**Compal Electronics, Inc.**

Title: ***DDRIII-SODIMM B***

| Size | Document Number | Rev |
|---|---|---|
| Custom | PCA70 LA-7521P M/B | 0.1 |

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**CMOS Setting, near DDR Door**

+RTCVCC — R111 20K_0402_5% — PCH_RTCRST# — JCOMS1 CONN@ — C203 1U_0402_6.3V6K

**RC Delay 18~25mS**

**iME Setting.**

R115 20K_0402_5% — PCH_SRTCRST# — JME1 CONN@ — C205 1U_0402_6.3V6K

**RC Delay 18~25mS**

**Integrated SUS 1.05V VRM Enable**

| PCH_INTVRMEN | High - Enable Internal VRs (must be always pulled high) |
|---|---|

+RTCVCC — R122 390K_0402_5% — PCH_INTVRMEN

+RTCVCC — R121 1M_0402_5% — SM_INTRUDER#

+3VS — R126 10K_0402_5% — PCH_GPIO33

+3VALW — R133 10K_0402_5% — PCH_GPIO13

**PCH_SPKR**

* High = Enabled (No Reboot)

Low = Disabled (Default)

+3VS — R131 1K_0402_5% — PCH_SPKR

**HDA_SYNC**

This signal has a weak internal pull down

*H=>On Die PLL is supplied by 1.5V (mobile)

L=>On Die PLL is supplied by 1.8V (DT)

Need to pull high for Huron River platform

+3VALW — @R136 1K_0402_5% — AZ_SYNC

No mention on SB PDG but HR mention on PDG reserve for Potential Leakage Concern

+5VS — @ Q2 BSS138LT1G_SOT23-3

[47] AZ_SYNC_HD — R139 33_0402_5% — AZ_SYNC_R

R140 0_0402_5%

**HDA_SDO**

ME debug mode,

this signal has a weak internal pull down

*Low = Disable (default)

High = Enable (flash descriptor security overide)

[49] PWRME_CTRL# — PWRME_CTRL# R129 @ 0_0402_5% AZ_SDOUT

R134 @ 1K_0402_5%

PCH_SPIDI R143 0_0402_5% DI

PCH_SPICLK R144 0_0402_5% CLK

PCH_SPICS# R145 0_0402_5% CS#

PCH_SPIDO R146 0_0402_5% DO

+3VALW

**4M Byte**

C212 0.1U_0402_16V4Z

U6 W25Q32BVSSIG_SO8

CS# DO WP# GND VCC HOLD# CLK DI

**Socket: SP07000F500/SP07000H900**

**Please close to U2 PCH**

U4A — BD82CPDS-QMZP-B0_FCBGA942

C202 15P_0402_50V8J — Y1 32.768KHZ_12.5PF_Q13MC14610002 — C204 15P_0402_50V8J — R113 10M_0402_5%

PCH_RTCX1 BR39 — RTCX1

PCH_RTCX2 BN39 — RTCX2

PCH_RTCRST# BT41 — RTCRST#

PCH_SRTCRST# BN37 — SRTCRST#

SM_INTRUDER# BM38 — INTRUDER#

PCH_INTVRMEN BN41 — INTVRMEN

RTC

[47] AZ_BITCLK_HD — R118 33_0402_5% — AZ_BITCLK BU22 — HDA_BCLK

AZ_SYNC BP23 — HDA_SYNC

[47] PCH_SPKR — PCH_SPKR BE56 — SPKR

[47] AZ_RST_HD# — R120 33_0402_5% — AZ_RST# BC22 — HDA_RST#

[47] AZ_SDIN0_HD — AZ_SDIN0_HD BD22 — HDA_SDIN0

BF22 — HDA_SDIN1

BK22 — HDA_SDIN2

+3VALW — R124 1K_0402_5% — BJ22 — HDA_SDIN3

[47] AZ_SDOUT_HD — R125 33_0402_5% — AZ_SDOUT BT23 — HDA_SDO

IHDA

PCH_GPIO33 BC25 — HDA_DOCK_EN# / GPIO33

PCH_GPIO13 BA25 — HDA_DOCK_RST# / GPIO13

PCH_JTAG_TCK BA43 — JTAG_TCK

PCH_JTAG_TMS BC50 — JTAG_TMS

PCH_JTAG_TDI BC52 — JTAG_TDI

PCH_JTAG_TDO BF47 — JTAG_TDO

JTAG

PCH_SPICLK AR54 — SPI_CLK

PCH_SPICS# AT57 — SPI_CS0#

AR56 — SPI_CS1#

PCH_SPIDI AU53 — SPI_MOSI

PCH_SPIDO AT55 — SPI_MISO

SPI

FWH0 / LAD0 BK15 — LPC_AD0 — LPC_AD0 [49]

FWH1 / LAD1 BJ17 — LPC_AD1 — LPC_AD1 [49]

FWH2 / LAD2 BJ20 — LPC_AD2 — LPC_AD2 [49]

FWH3 / LAD3 BG20 — LPC_AD3 — LPC_AD3 [49]

FWH4 / LFRAME# BG17 — LPC_FRAME# — LPC_FRAME# [49]

LDRQ0# BK17

LDRQ1# / GPIO23 BA20

SERIRQ AV52 — SERIRQ — SERIRQ [49]

LPC

SATA 6G

SATA0RXN AC56 — SATA_PRX_C_DTX_N0 — SATA_PRX_C_DTX_N0 [41]

SATA0RXP AB55 — SATA_PRX_C_DTX_P0 — SATA_PRX_C_DTX_P0 [41]

SATA0TXN AE46 — SATA_PTX_DRX_N0 — C206 0.01U_0402_25V7K — SATA_PTX_C_DRX_N0 [41]

SATA0TXP AE44 — SATA_PTX_DRX_P0 — C207 0.01U_0402_25V7K — SATA_PTX_C_DRX_P0 [41]

HDD

SATA1RXN AA53 — SATA_PRX_C_DTX_N1 — SATA_PRX_C_DTX_N1 [41]

SATA1RXP AA56 — SATA_PRX_C_DTX_P1 — SATA_PRX_C_DTX_P1 [41]

SATA1TXN AG49 — SATA_PTX_DRX_N1 — C208 0.01U_0402_25V7K — SATA_PTX_C_DRX_N1 [41]

SATA1TXP AG47 — SATA_PTX_DRX_P1 — C209 0.01U_0402_25V7K — SATA_PTX_C_DRX_P1 [41]

ODD

SATA2RXN AL50

SATA2RXP AL49

SATA2TXN AL56

SATA2TXP AL53

**SATA port2 and port3 are disabled on H61**

SATA3RXN AN46

SATA3RXP AN44

SATA3TXN AN56

SATA3TXP AM55

SATA4RXN AN49 — SATA_PRX_C_DTX_N4 — SATA_PRX_C_DTX_N4 [40]

SATA4RXP AN50 — SATA_PRX_C_DTX_P4 — SATA_PRX_C_DTX_P4 [40]

SATA4TXN AT50 — SATA_PTX_DRX_N4 — C1390 0.01U_0402_25V7K — SATA_PTX_C_DRX_N4 [40]

SATA4TXP AT49 — SATA_PTX_DRX_P4 — C1391 0.01U_0402_25V7K — SATA_PTX_C_DRX_P4 [40]

SATA5RXN AT46

SATA5RXP AT44

SATA5TXN AV50

SATA5TXP AV49

**Place R128 and R130 within 500 mils of the PCH. Avoid routing next to clock pins.**

SATAICOMPO AJ53

SATAICOMPI AJ55 — SATAICOMP — R128 37.4_0402_1% — +1.05VS_VPCH

SATA3RCOMPO AE52

SATA3COMPI AE54 — SATA3_COMP — R130 49.9_0402_1% — +1.05VS_VPCH

SATA3RBIAS AC52 — RBIAS_SATA3 — R132 750_0402_1%

SATALED# BF57 — SATA_LED# — SATA_LED# [50]

SATA0GP / GPIO21 BC54 — CR_WAKE# — CR_WAKE# [44]

SATA1GP / GPIO19 AY52 — GPIO19

SATA

+3VS — SERIRQ R112 10K_0402_5%

+3VS — SATA_LED# R114 10K_0402_5%

CR_WAKE# R116 10K_0402_5%

GPIO19 R117 10K_0402_5%

**for EMI**

CLK — R137 10_0402_5% @ — C214 10P_0402_50V8J @

+RTCVCC — R1039 1K_0402_5% — D1 DAN202UT106_SC70-3 — +RTCBATT — +3VALW

C210 0.1U_0402_16V4Z

+3VALW — R147 200_0402_5% @ — PCH_JTAG_TMS — R151 100_0402_1%

+3VALW — R148 200_0402_5% @ — PCH_JTAG_TDO — R152 100_0402_1%

+3VALW — R149 200_0402_5% @ — PCH_JTAG_TDI — R153 100_0402_1%

R154 51_0402_1% — PCH_JTAG_TCK

| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |



Compal Electronics, Inc.

Title: *PCH_HDA/JTAG/SATA/SPI/LPC*

Size: Custom | Document Number: PCA70 LA-7521P M/B | Rev: 0.1

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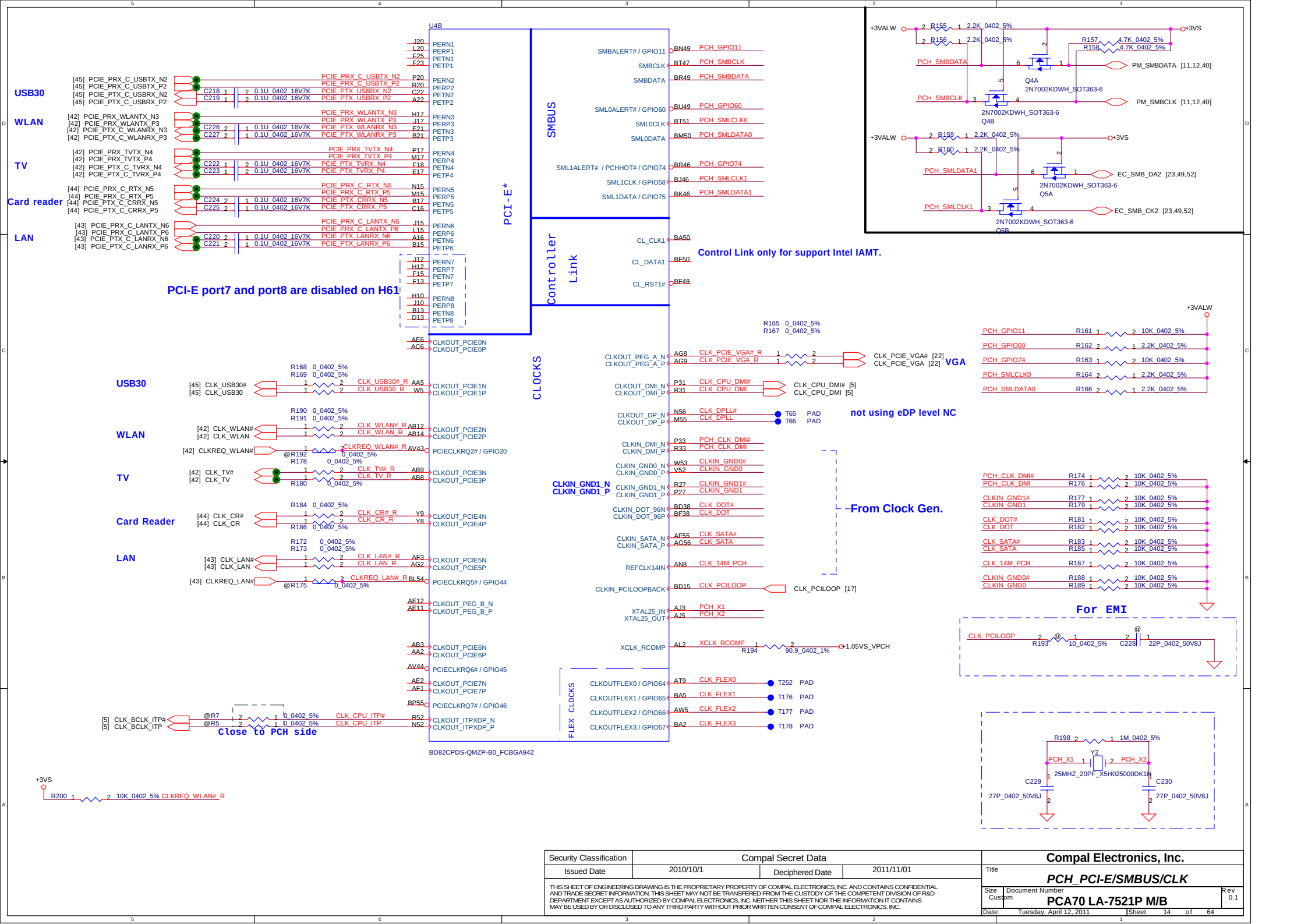



| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |

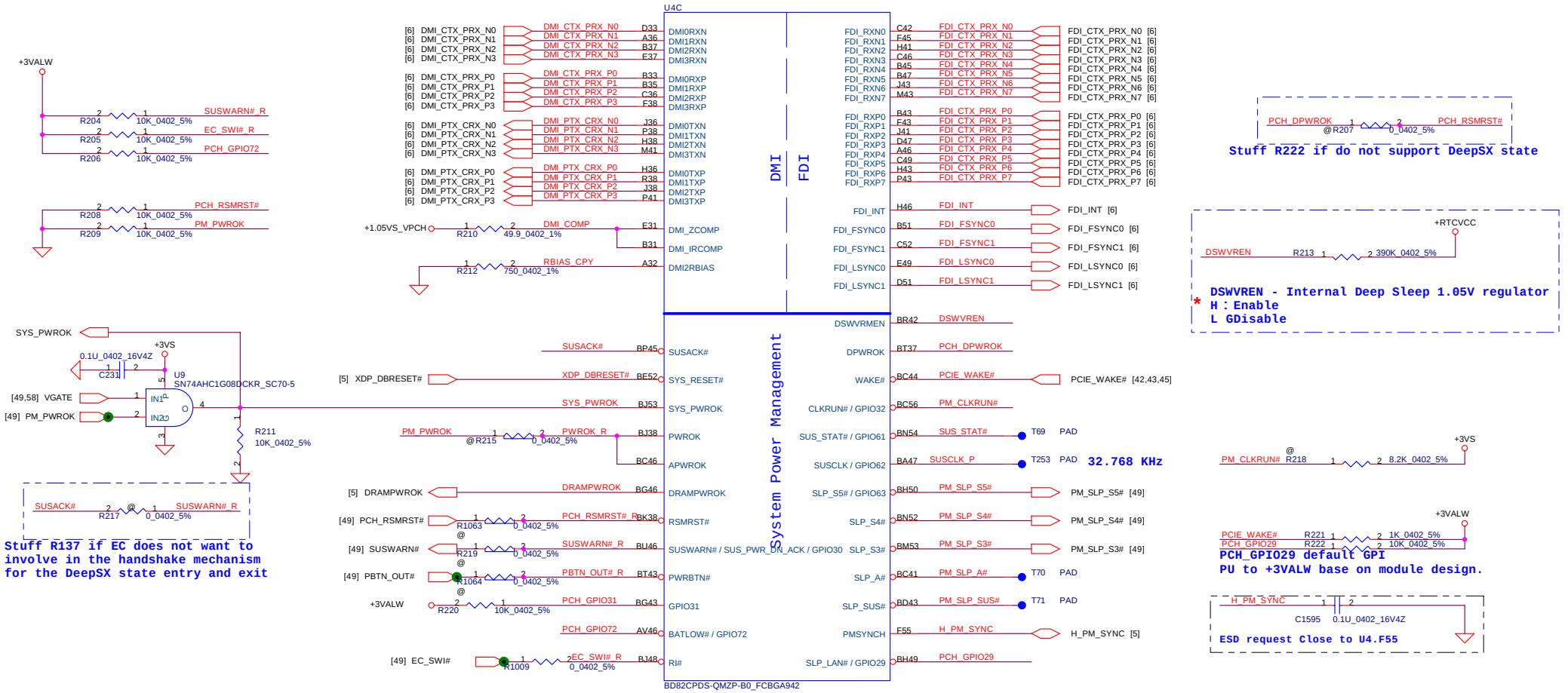


**Compal Electronics, Inc.**

Title: ***PCH_PCI-E/SMBUS/CLK***

| Size | Document Number | Rev |
|---|---|---|
| Custom | PCA70 LA-7521P M/B | 0.1 |

Date: Tuesday, April 12, 2011 | Sheet 14 of 64




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |



**Compal Electronics, Inc.**

Title: *PCH_DMI/FDI/PM*

| Size | Document Number | Rev |
|---|---|---|
| Custom | PCA70 LA-7521P M/B | 0.1 |

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**NOTE:PCH adds support for panel power sequencing required for embedded DisplayPort support. L_VDDEN, L_BKLTEN and L_BKLTCTL pins are added on the PCH for panel power sequencing. It is important to note that a 6 layer board design may be required to access these pins on the PCH package in a fully featured platform design.**

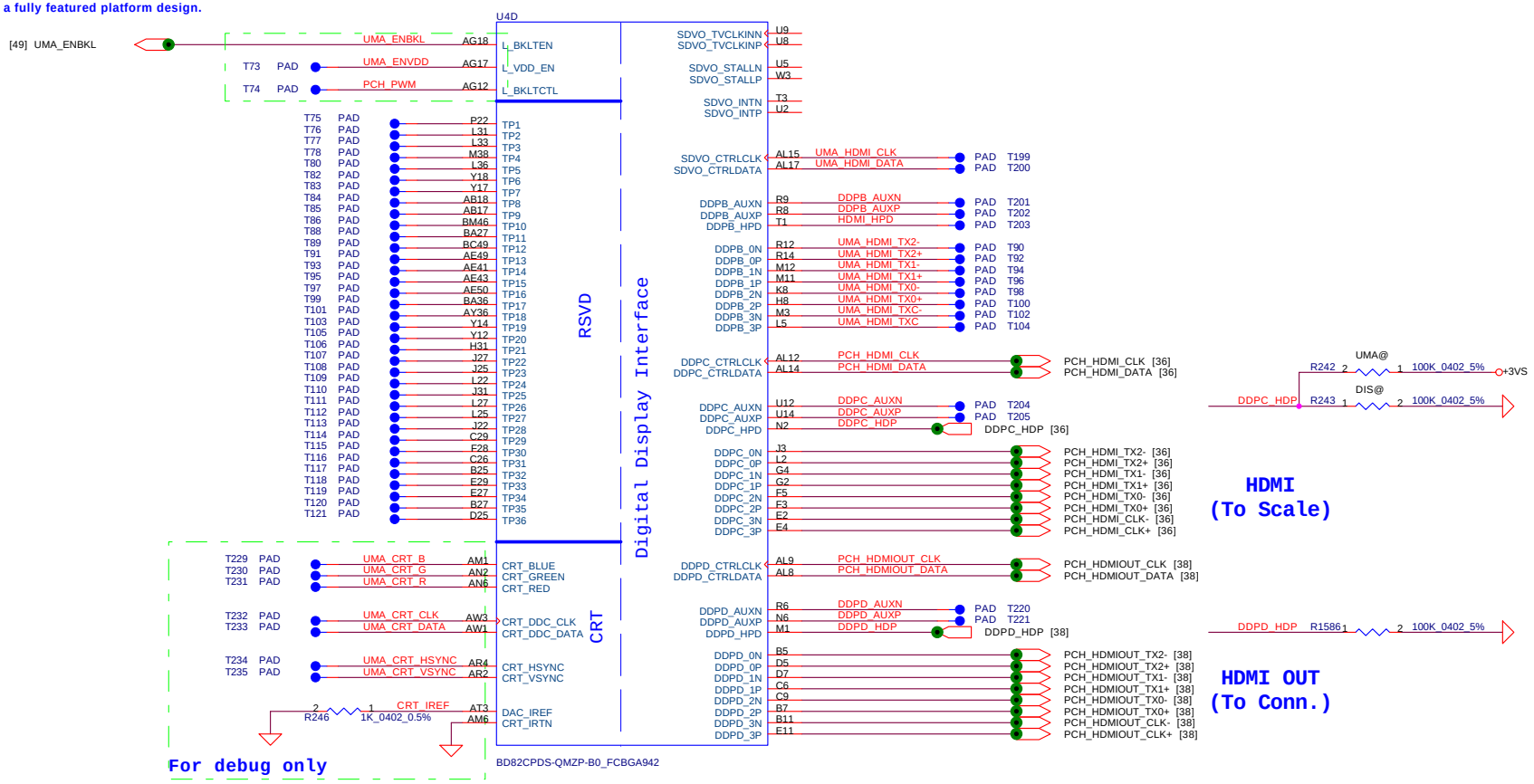


Table 5-60. PCH Digital Port Pin Mapping

| Port Description | DisplayPort* Signals | HDMI* Signals | SDVO Signals | PCH Display Port Pin details |
|---|---|---|---|---|
| Port B | DPB_LANE3 | TMDSB_CLK | SDVOB_CLK | DDPB_[3]P |
| | DPB_LANE3# | TMDSB_CLKB | SDVOB_CLK# | DDPB_[3]N |
| | DPB_LANE2 | TMDSB_DATA0 | SDVOB_BLUE | DDPB_[2]P |
| | DPB_LANE2# | TMDSB_DATA0B | SDVOB_BLUE# | DDPB_[2]N |
| | DPB_LANE1 | TMDSB_DATA1 | SDVOB_GREEN | DDPB_[1]P |
| | DPB_LANE1# | TMDSB_DATA1B | SDVOB_GREEN# | DDPB_[1]N |
| | DPB_LANE0 | TMDSB_DATA2 | SDVOB_RED | DDPB_[0]P |
| | DPB_LANE0# | TMDSB_DATA2B | SDVOB_RED* | DDPB_[0]N |
| | DPB_HPD | TMDSB_HPD | | DDPB_HPD |
| | DPB_AUX | | | DDPB_AUXP |
| | DPB_AUXB | | | DDPB_AUXN |
| Port C | DPC_LANE3 | TMDSC_CLK | | DDPC_[3]P |
| | DPC_LANE3# | TMDSC_CLKB | | DDPC_[3]N |
| | DPC_LANE2 | TMDSC_DATA0 | | DDPC_[2]P |
| | DPC_LANE2# | TMDSC_DATA0B | | DDPC_[2]N |
| | DPC_LANE1 | TMDSC_DATA1 | | DDPC_[1]P |
| | DPC_LANE1# | TMDSC_DATA1B | | DDPC_[1]N |
| | DPC_LANE0 | TMDSC_DATA2 | | DDPC_[0]P |
| | DPC_LANE0# | TMDSC_DATA2B | | DDPC_[0]N |
| | DPC_HPD | TMDSC_HPD | | DDPC_HPD |
| | DPC_AUX | | | DDPC_AUXP |
| | DPC_AUXC | | | DDPC_AUXN |
| Port D | DPD_LANE3 | TMDSD_CLK | | DDPD_[3]P |
| | DPD_LANE3# | TMDSD_CLKB | | DDPD_[3]N |
| | DPD_LANE2 | TMDSD_DATA0 | | DDPD_[2]P |
| | DPD_LANE2# | TMDSD_DATA0B | | DDPD_[2]N |
| | DPD_LANE1 | TMDSD_DATA1 | | DDPD_[1]P |
| | DPD_LANE1# | TMDSD_DATA1B | | DDPD_[1]N |
| | DPD_LANE0 | TMDSD_DATA2 | | DDPD_[0]P |
| | DPD_LANE0# | TMDSD_DATA2B | | DDPD_[0]N |
| | DPD_HPD | TMDSD_HPD | | DDPD_HPD |
| | DPD_AUX | | | DDPD_AUXP |
| | DPD_AUXD | | | DDPD_AUXN |



**Compal Electronics, Inc.**

Title: ***PCH_CRT/LVDS/HDMI***

| Size | Document Number | Rev |
|---|---|---|
| Custom | PCA70 LA-7521P M/B | 0.1 |

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## PCI PU resistor

+3VS

| | | | | |
|---|---|---|---|---|
| R253 | 1 | 2 | 8.2K_0402_5% | PCI_DEVSEL# |
| R254 | 1 | 2 | 8.2K_0402_5% | PCI_FRAME# |
| R255 | 1 | 2 | 8.2K_0402_5% | PCI_IRDY# |
| R256 | 1 | 2 | 8.2K_0402_5% | PCI_TRDY# |
| R259 | 1 | 2 | 8.2K_0402_5% | PCI_STOP# |
| R260 | 1 | 2 | 8.2K_0402_5% | PCI_PERR# |
| R261 | 1 | 2 | 8.2K_0402_5% | PCI_SERR# |
| R262 | 1 | 2 | 8.2K_0402_5% | PCI_PLOCK# |
| R263 | 1 | 2 | 8.2K_0402_5% | PCI_PIRQA# |
| R264 | 1 | 2 | 8.2K_0402_5% | PCI_PIRQB# |
| R266 | 1 | 2 | 8.2K_0402_5% | PCI_PIRQC# |
| R267 | 1 | 2 | 8.2K_0402_5% | PCI_PIRQD# |
| R269 | 1 | 2 | 8.2K_0402_5% | PCH_REQ0# |

+3VS

| | | | | |
|---|---|---|---|---|
| R270 | 1 | 2 | 8.2K_0402_5% | DGPU_HOLD_RST# |
| R271 | 1 | 2 | 8.2K_0402_5% | PCH_GPIO52 |
| R272 | 1 | 2 | 8.2K_0402_5% | DGPU_PWR_EN |
| R276 | 1 | 2 | 8.2K_0402_5% | PCH_GPIO2 |
| R277 | 1 | 2 | 8.2K_0402_5% | PCH_GPIO3 |
| R278 | 1 | 2 | 8.2K_0402_5% | PCH_GPIO4 |
| R279 | 1 | 2 | 8.2K_0402_5% | CR_CPPE# |

Intel confirm GPIO19 is correct.

**Boot BIOS Strap**

| PCH_GNT1# | GPIO19 | Boot BIOS Loaction |
|---|---|---|
| 0 | 0 | LPC |
| 0 | 1 | Reserved |
| 1 | 0 | PCI |
| 1 | 1 | SPI * |

U4E

PCI

| | | | |
|---|---|---|---|
| BF15 | AD0 | DEVSEL# | BH9 PCI_DEVSEL# |
| BF17 | AD1 | | |
| BT7 | AD2 | FRAME# | BC11 PCI_FRAME# |
| BT13 | AD3 | | |
| BG12 | AD4 | IRDY# | BF11 PCI_IRDY# |
| BN11 | AD5 | | |
| BJ12 | AD6 | TRDY# | BC8 PCI_TRDY# |
| BU9 | AD7 | | |
| BR12 | AD8 | STOP# | BC12 PCI_STOP# |
| BJ3 | AD9 | | |
| BR9 | AD10 | PAR | BH8 PAR — PAD T122 |
| BJ10 | AD11 | | |
| BM8 | AD12 | PERR# | BM3 PCI_PERR# |
| BF3 | AD13 | | |
| BN2 | AD14 | SERR# | BR6 PCI_SERR# |
| BE4 | AD15 | | |
| BE6 | AD16 | PCIRST# | AV14 |
| BG15 | AD17 | | |
| BC6 | AD18 | PLOCK# | BA17 PCI_PLOCK# |
| BT11 | AD19 | | |
| BA14 | AD20 | | |
| BL2 | AD21 | | |
| BC4 | AD22 | | |
| BL4 | AD23 | | |
| BC2 | AD24 | | |
| BM13 | AD25 | | |
| BA9 | AD26 | | |
| BF9 | AD27 | | |
| BA8 | AD28 | | |
| BF8 | AD29 | | |
| AV17 | AD30 | | |
| BK12 | AD31 | | |

| | | |
|---|---|---|
| BN4 | C/BE0# | |
| BP7 | C/BE1# | |
| BG2 | C/BE2# | |
| BP13 | C/BE3# | |

| | | |
|---|---|---|
| PCI_PIRQA# | BK10 | PIRQA# |
| PCI_PIRQB# | BJ5 | PIRQB# |
| PCI_PIRQC# | BM15 | PIRQC# |
| PCI_PIRQD# | BP5 | PIRQD# |

| | | | |
|---|---|---|---|
| PCH_REQ0# | BG5 | REQ0# | |
| [22] DGPU_HOLD_RST# | DGPU_HOLD_RST# BT5 | REQ1# / GPIO50 | |
| PCH_GPIO52 | BK8 | REQ2# / GPIO52 | |
| [26,60] DGPU_PWR_EN | DGPU_PWR_EN AV11 | REQ3# / GPIO54 | |

Have internal PU

| | | | | |
|---|---|---|---|---|
| T195 | PAD | PCH_GNT0# | BA15 | GNT0# |
| T196 | PAD | PCH_GNT1# | AV8 | GNT1# / GPIO51 |
| T197 | PAD | PCH_GNT2# | BU12 | GNT2# / GPIO53 |
| T198 | PAD | PCH_GNT3# | BE2 | GNT3# / GPIO55 |

| | | | |
|---|---|---|---|
| PCH_GPIO2 | BN9 | PIRQE# / GPIO2 | |
| PCH_GPIO3 | AV9 | PIRQF# / GPIO3 | |
| PCH_GPIO4 | BT15 | PIRQG# / GPIO4 | |
| CR_CPPE# | BR4 | PIRQH# / GPIO5 | |

For CR D3E wake up reserve [44] CR_CPPE#

T123PAD — PCH_PME# AV15 — PME#

PCH_PLT_RST# BK48 — PLTRST#

| | | | | |
|---|---|---|---|---|
| T179 | PAD | | AT11 | CLKOUT_PCI0 |
| T180 | PAD | | AN14 | CLKOUT_PCI1 |
| [14] CLK_PCILOOP | 22_0402_5% 1 | 2 R281 CLK_PCILOOP_R | AT12 | CLKOUT_PCI2 |
| [49] CLK_PCI_EC | 22_0402_5% 1 | 2 R282 CLK_PCI_EC_R | AT17 | CLKOUT_PCI3 |
| T181 | PAD | | AT14 | CLKOUT_PCI4 |

BD82CPDS-QMZP-B0_FCBGA942

USB

EHCI 1

| | | | |
|---|---|---|---|
| USBP0N | BF36 | USB20_N0 | USB20_N0 [46] |
| USBP0P | BD36 | USB20_P0 | USB20_P0 [46] |
| USBP1N | BC33 | USB20_N1 | USB20_N1 [46] |
| USBP1P | BA33 | USB20_P1 | USB20_P1 [46] |
| USBP2N | BM33 | USB20_N2 | USB20_N2 [50] |
| USBP2P | BM35 | USB20_P2 | USB20_P2 [50] |
| USBP3N | BT33 | USB20_N3 | USB20_N3 [50] |
| USBP3P | BU32 | USB20_P3 | USB20_P3 [50] |
| USBP4N | BR32 | USB20_N4 | USB20_N4 [40] |
| USBP4P | BT31 | USB20_P4 | USB20_P4 [40] |
| USBP5N | BN29 | USB20_N5 | USB20_N5 [41] |
| USBP5P | BM30 | USB20_P5 | USB20_P5 [41] |

Reserve for USB30 PORT0@ CONN2
Reserve for USB30 PORT1@ CONN1
Touch
Int. Camera
eSATA+USB
USB PORT5 CONN6

USB port6 and port7 are disabled on H61

EHCI 2

| | | | |
|---|---|---|---|
| USBP6N | BK33 | | |
| USBP6P | BJ33 | | |
| USBP7N | BF31 | | |
| USBP7P | BD31 | | |
| USBP8N | BN27 | USB20_N8 | USB20_N8 [41] |
| USBP8P | BR29 | USB20_P8 | USB20_P8 [41] |
| USBP9N | BR26 | USB20_N9 | USB20_N9 [41] |
| USBP9P | BT27 | USB20_P9 | USB20_P9 [41] |
| USBP10N | BK25 | USB20_N10 | USB20_N10 [42] |
| USBP10P | BJ25 | USB20_P10 | USB20_P10 [42] |
| USBP11N | BJ31 | USB20_N11 — PAD T254 | |
| USBP11P | BK31 | USB20_P11 — PAD T255 | |
| USBP12N | BF27 | | |
| USBP12P | BD27 | | |
| USBP13N | BJ27 | | |
| USBP13P | BK27 | | |

USB20_N8 [41] — USB PORT8 CONN4
USB20_P8 [41] — USB PORT9 CONN3
USB20_N9 [41] — TV Tuner #1
USB20_P9 [41] — Reserve
USB20_N10 [42]
USB20_P10 [42]

USB port12 and port13 are disabled on H61

USBRBIAS# BP25 — USBBIAS — R280 1 2 22.6_0402_1%

USBRBIAS BM25

Layout Note:USB_BIAS WITH LENGTH NO MORE THAN 500 MILS TO RESISTOR.

| | | | |
|---|---|---|---|
| OC0# / GPIO59 | BM43 | USB_OC1 | USB_OC1 [45,46] |
| OC1# / GPIO40 | BD41 | USB_OC#1 | |
| OC2# / GPIO41 | BG41 | USB_OC#2 | USB_OC#2 [40,41] |
| OC3# / GPIO42 | BK43 | USB_OC#3 | |
| OC4# / GPIO43 | BP43 | USB_OC#4 | USB_OC#4 [41] |
| OC5# / GPIO9 | BJ41 | USB_OC#5 | |
| OC6# / GPIO10 | BT45 | USB_OC#6 | |
| OC7# / GPIO14 | BM45 | USB_OC#7 | |

USB30 PORT 0,1
USB PORT 4,5
USB PORT 8,9

@R250 0_0402_5%

+3VS

U10 NC7SZ08P5X_NL_SC70-5

PCH_PLT_RST# — PLT_RST# — PLT_RST# [5,22,45,49]

C1047 0.1U_0402_16V4Z

R257 100K_0402_5%

C1048 0.1U_0402_16V4Z

U57 NC7SZ08P5X_NL_SC70-5

PLT_A_RST# [42,43,44]

R1067 100K_0402_5%

+3VALW

| | | | |
|---|---|---|---|
| USB_OC1 | R283 | 1 2 | 10K_0402_5% |
| USB_OC#1 | R284 | 1 2 | 10K_0402_5% |
| USB_OC#4 | R285 | 1 2 | 10K_0402_5% |
| USB_OC#2 | R286 | 1 2 | 10K_0402_5% |
| USB_OC#3 | R287 | 1 2 | 10K_0402_5% |
| USB_OC#5 | R288 | 1 2 | 10K_0402_5% |
| USB_OC#6 | R1011 | 1 2 | 10K_0402_5% |
| USB_OC#7 | R1012 | 1 2 | 10K_0402_5% |

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |



Compal Electronics, Inc.

Title: PCH_PCI/USB/NAND

Size: Custom | Document Number: PCA70 LA-7521P M/B | Rev: 0.1

Date: Tuesday, April 12, 2011 | Sheet 17 of 64

| Project ID | GPIO69 | GPIO70 | GPIO71 |
|---|---|---|---|
| SKU1 | 0 | 0 | 0 |
| SKU2 | 0 | 0 | 1 |
| SKU3 | 0 | 1 | 0 |
| SKU4 | 0 | 1 | 1 |
| x | 1 | 0 | 0 |
| x | 0 | 0 | 1 |
| x | 0 | 1 | 0 |
| x | 0 | 1 | 1 |
| x | 1 | 0 | 0 |
| x | 1 | 0 | 1 |
| x | 1 | 1 | 0 |
| x | 1 | 1 | 1 |

**PROJECT ID TABLE**

**GPIO8**

**Integrated Clock Chip Enable (Removed)**
* **H: Disable**
**L: Enable**

**Integrated clock enable functionality is achieved by soft-strap**
**The current default is clock enable**

**In Deep Sleep Power Well. Unmuxed.**
**Defaults to GPI.**
**Not used Weak pull-up 10kΩ to VccDSW3_3**
**-->Check list1.5 P402.**
**PD to GND for Huron River!!**

**GPIO28**

**On-Die PLL Voltage Regulator**
* **H: Enable**
**L: Disable**

**SATA2GP/GPIO36 & SATA3GP/GPIO37Sampled at Rising edge of PWROK.Weak internal pull-down. (weak internal pull-down is disabled after PLTRST# de-asserts)**
**NOTE: This signal should NOT be pulled high when strap is sampled**

**ISDBT_DET**

**For OPT**

**DMI & FDI Termination Voltage**

| NV_CLE | |
|---|---|
| | Set to VCC when HIGH |
| | Set to VSS when LOW |

**Internal Pull Down**

**Note:Place R329 close to U1.R47 and <=100 mils**

**ESD request Close to U4.BB57**

**ESD request Close to U4.R47**

BD82CPDS-QMZP-B0_FCBGA942

| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |



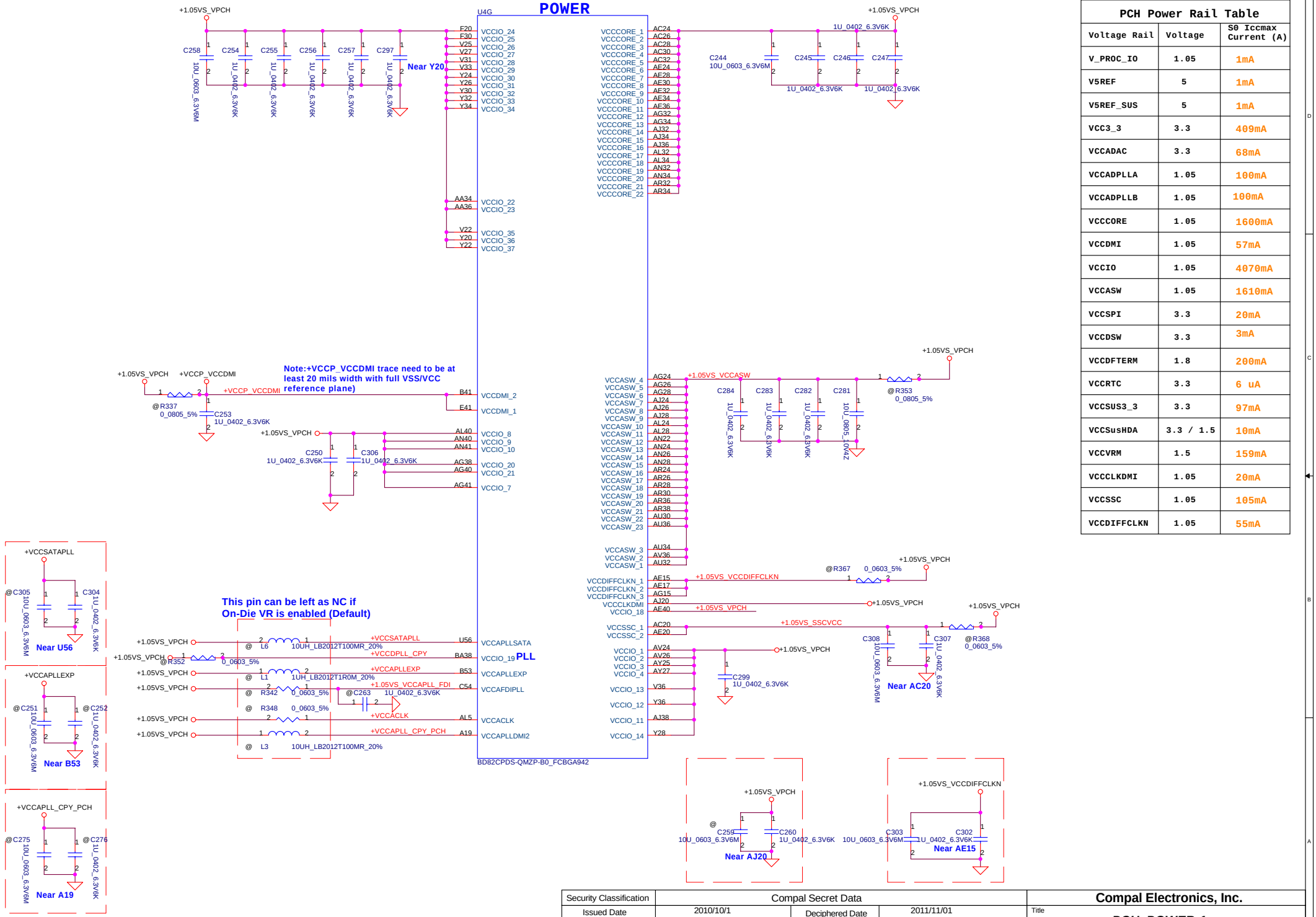
**Compal Electronics, Inc.**

Title: ***PCH_CPU/GPIO***

| Size | Document Number | Rev |
|---|---|---|
| Custom | PCA70 LA-7521P M/B | 0.1 |

Date: Tuesday, April 12, 2011 | Sheet 18 of 64

# POWER




## PCH Power Rail Table

| Voltage Rail | Voltage | S0 Iccmax Current (A) |
|---|---|---|
| V_PROC_IO | 1.05 | 1mA |
| V5REF | 5 | 1mA |
| V5REF_SUS | 5 | 1mA |
| VCC3_3 | 3.3 | 409mA |
| VCCADAC | 3.3 | 68mA |
| VCCADPLLA | 1.05 | 100mA |
| VCCADPLLB | 1.05 | 100mA |
| VCCCORE | 1.05 | 1600mA |
| VCCDMI | 1.05 | 57mA |
| VCCIO | 1.05 | 4070mA |
| VCCASW | 1.05 | 1610mA |
| VCCSPI | 3.3 | 20mA |
| VCCDSW | 3.3 | 3mA |
| VCCDFTERM | 1.8 | 200mA |
| VCCRTC | 3.3 | 6 uA |
| VCCSUS3_3 | 3.3 | 97mA |
| VCCSusHDA | 3.3 / 1.5 | 10mA |
| VCCVRM | 1.5 | 159mA |
| VCCCLKDMI | 1.05 | 20mA |
| VCCSSC | 1.05 | 105mA |
| VCCDIFFCLKN | 1.05 | 55mA |

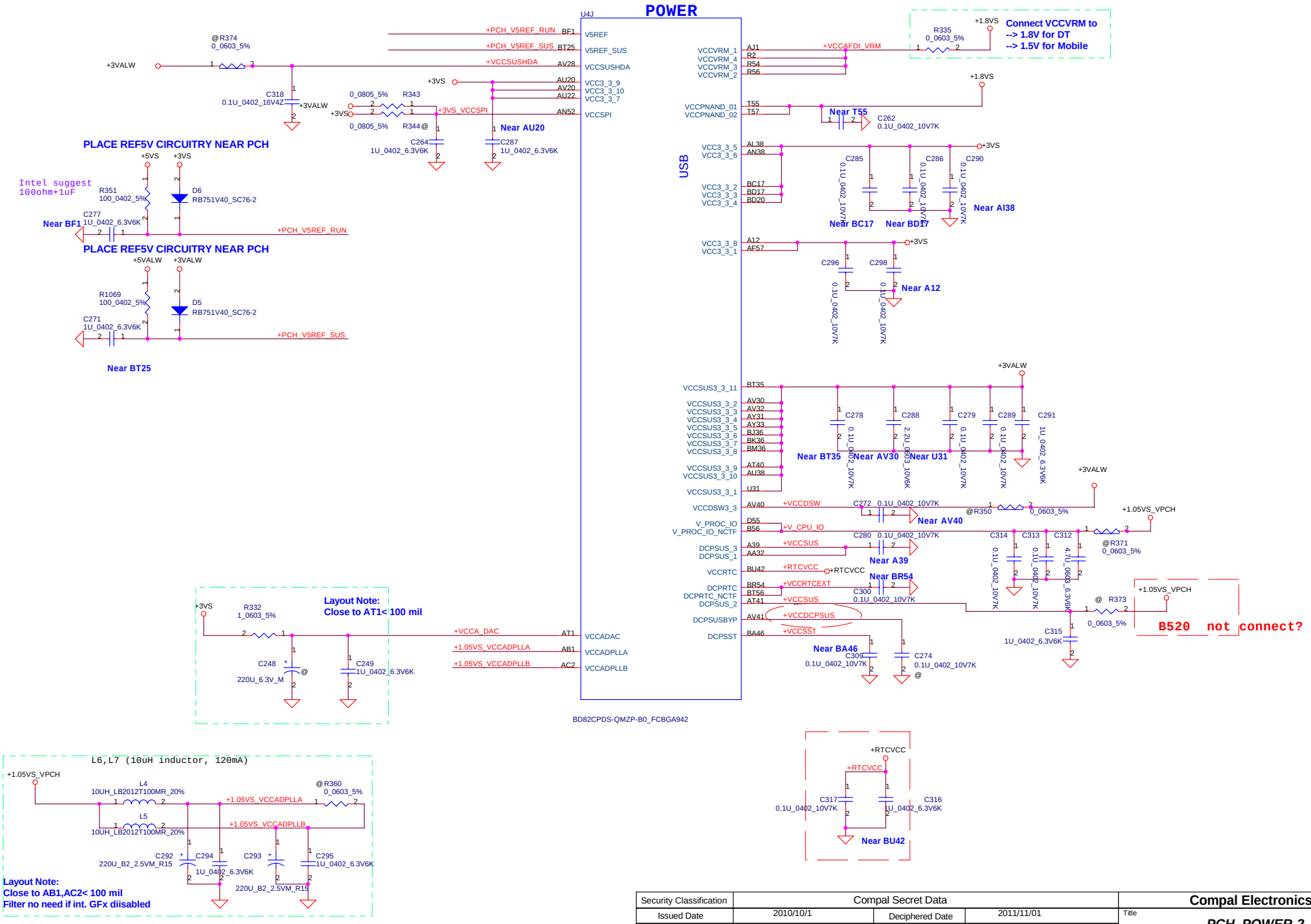


**Compal Electronics, Inc.**

Title: *PCH_POWER-1*

Size: Custom | Document Number: PCA70 LA-7521P M/B | Rev: 0.1

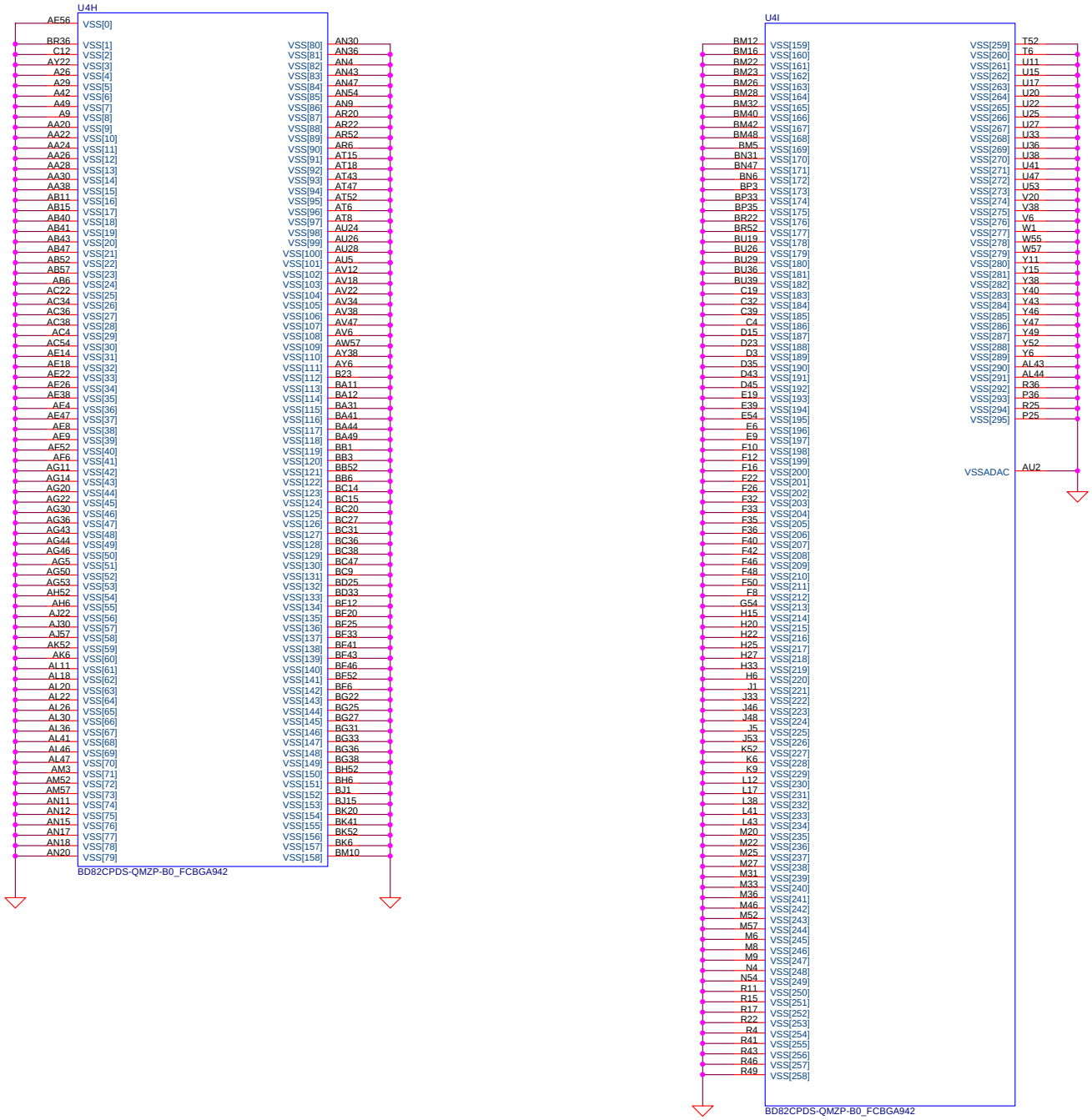
Date: Tuesday, April 12, 2011 | Sheet 19 of 64




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |



| | |
|---|---|
| Compal Electronics, Inc. | |
| Title | PCH_POWER-2 |
| Size: Custom | Document Number: PCA70 LA-7521P M/B |
| Rev | 0.1 |
| Date: Tuesday, April 12, 2011 | Sheet 20 of 64 |




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |



**Compal Electronics, Inc.**

Title: ***PCH_GND***

| Size | Document Number | Rev |
|---|---|---|
| Custom | PCA70 LA-7521P M/B | 0.1 |

Date: Tuesday, April 12, 2011 | Sheet 21 of 64

## GPIO Description

| GPIO | I/O | ACTIVE | USAGE |
|---|---|---|---|
| GPIO0 | IN | N/A | IFPAB HOTPLUG DETECT |
| GPIO1 | IN | N/A | IFPC HOTPLUG DETECT |
| GPIO2 | OUT | HIGH | PANEL BACKLIGHT PWM |
| GPIO3 | OUT | HIGH | PANEL POWER ENABLE |
| GPIO4 | OUT | HIGH | PANEL BACKLIGHT ENABLE |
| GPIO5 | OUT | HIGH | NVVDD ALTV0 |
| GPIO6 | OUT | HIGH | NVVDD ALTV1 |
| GPIO7 | OUT | HIGH | FBVDDQ ALTV |
| GPIO8 | IN/OUT | LOW | OVERTEMP ALERT |
| GPIO9 | OUT | LOW | THERMAL ALERT |
| GPIO10 | OUT | HIGH | FB_VREF CONTROL |
| GPIO11 | OUT | HIGH | RESERVED |
| GPIO12 | IN | N/A | AC DETECT |
| GPIO13 | OUT | LOW | LOAD STEP DOWN |
| GPIO14 | OUT | HIGH | LOAD STEP UP |
| GPIO15 | IN | N/A | IFPE HOTPLUG DETECT |
| GPIO16 | IN | N/A | FAN PWM OUT |
| GPIO17 | IN | N/A | FAN TACH IN |
| GPIO18 | IN | N/A | RESERVED |
| GPIO19 | IN | N/A | IFPD HOTPLUG DETECT |
| GPIO20 | IN | N/A | RESERVED |
| GPIO21 | IN | N/A | IFPF HOTPLUG DETECT |
| GPIO22 | IN | N/A | RESERVED |
| GPIO23 | IN | N/A | RESERVED |
| GPIO24 | IN | N/A | RESERVED |

PCI-Express Gen2 x16 Interface

Close to GPU (Reserve for debug)

(Reserve for debug)

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2009/01/01 | Deciphered Date | 2010/01/01 |



**Compal Electronics, Inc.**

Title: VGA_PCIE/DAC/GPIO

Size: | Document Number: PCA70 LA-7521P M/B | Rev: 0.1

Date: Tuesday, April 12, 2011 | Sheet 22 of 64

For GB2-128 & GB2b-128 colayout....

| Display | Interface Support |
|---|---|
| LinkA | LVDS(Single Link or Dual Link with IFPB) |
| LinkB | LVDS(Dual Link with IFPA) |
| LinkC | Display Port/HDMI |
| LinkD | Display Port/eDP |
| LinkE | Display Port/DVI(Single Link or Dual Link with IFPF))/HDMI |
| LinkF | Display Port/DVI(Dual Link with IFPE) |

U58D
Part 4 of 7
N12P-GS-A1_BGA_973P
GS@

LVDS/TMDS
Channel A
Channel B
NC
TEST
SERIAL
GENERAL

IFPA_TXC, IFPA_TXC_N, IFPA_TXD0, IFPA_TXD0_N, IFPA_TXD1, IFPA_TXD1_N, IFPA_TXD2, IFPA_TXD2_N, IFPA_TXD3, IFPA_TXD3_N
IFPB_TXC, IFPB_TXC_N, IFPB_TXD4, IFPB_TXD4_N, IFPB_TXD5, IFPB_TXD5_N, IFPB_TXD6, IFPB_TXD6_N, IFPB_TXD7, IFPB_TXD7_N
IFPC_L0, IFPC_L0_N, IFPC_L1, IFPC_L1_N, IFPC_L2, IFPC_L2_N, IFPC_L3, IFPC_L3_N
IFPD_L0, IFPD_L0_N, IFPD_L1, IFPD_L1_N, IFPD_L2, IFPD_L2_N, IFPD_L3, IFPD_L3_N
IFPE_L0, IFPE_L0_N, IFPE_L1, IFPE_L1_N, IFPE_L2, IFPE_L2_N, IFPE_L3, IFPE_L3_N
IFPF_L0, IFPF_L0_N, IFPF_L1, IFPF_L1_N, IFPF_L2, IFPF_L2_N, IFPF_L3, IFPF_L3_N

NC_0 … NC_29

STRAP4 → STRAP4 [33]
STRAP3 → STRAP3 [33]
VPGOOD → R1643 1 2 10K_0402_5% GV@
STRAP_REF2 → R1646 1 2 40.2K_0402_1% GV@

[36] VGA_SHDMI_ETXD2+
[36] VGA_SHDMI_ETXD2-
[36] VGA_SHDMI_ETXD1+
[36] VGA_SHDMI_ETXD1-
[36] VGA_SHDMI_ETXD0+
[36] VGA_SHDMI_ETXD0-
[36] VGA_SHDMI_ETXC+
[36] VGA_SHDMI_ETXC-

To HDMI OUT

[38] VGA_HDMI_ETXD2+
[38] VGA_HDMI_ETXD2-
[38] VGA_HDMI_ETXD1+
[38] VGA_HDMI_ETXD1-
[38] VGA_HDMI_ETXD0+
[38] VGA_HDMI_ETXD0-
[38] VGA_HDMI_ETXC+
[38] VGA_HDMI_ETXC-

To HDMI OUT

+3VGS
R1578 1 2 2.2K_0402_5% DIS@
R1579 1 2 2.2K_0402_5% DIS@
[36] VGA_SHDMI_ECLK
[36] VGA_SHDMI_EDATA

+3VGS
R1138 1 2 2.2K_0402_5% DIS@
R1139 1 2 2.2K_0402_5% DIS@
[38] VGA_HDMI_ECLK
[38] VGA_HDMI_EDATA

VDD_SENSE_0, VDD_SENSE_1, VDD_SENSE_2 → D35, P7, AD20 → VGA_SENSE [60]
GND_SENSE_0, GND_SENSE_1, GND_SENSE_2 → AD19, E35, R7 → GND_SENSE [60]

TESTMODE, JTAG_TCK, JTAG_TDI, JTAG_TDO, JTAG_TMS, JTAG_TRST_N
AP35 TESTMODE
AP14 T216
AN14 T217
AN16 T218
AR14 T219
AP16 → R1141 1 2 10K_0402_5% DIS@
R1140 10K_0402_5% DIS@

ROM_CS_N, ROM_SI, ROM_SO, ROM_SCLK
C3 ROM_CS#
D3 ROM_SI
C4 ROM_SO
D4 ROM_SCLK
ROM_SI [33]
ROM_SO [33]
ROM_SCLK [33]

if unuse this pin , pull down 36k
A5 R1627 2 DIS@ 1 36K_0402_1%
N9 R11431 2 DIS@ 40.2K_0402_1%
M9 R11451 2 DIS@ 40.2K_0402_1%

R1144 10K_0402_5% DIS@ +3VGS
A4 BUFRST_N
AB5 CEC
[33] STRAP0
[33] STRAP1
[33] STRAP2
W5 STRAP0
W7 STRAP1
V7 STRAP2

NC/SPDIF_NC
MULTI_STRAP_REF0_GND
MULTI_STRAP_REF1_GND
THERMDP
THERMDN
B5 THERM_D+
B4 THERM_D-

## External VGA Thermal Sensor

Address: 0x9A H

+3VGS
C1122 @ 2 1 0.1U_0402_16V4Z
THERM_D+
THERM_D-
C1123 @ 2200P_0402_50V7K
U60
VDD, D+, D-, THERM#, SCLK, SDATA, ALERT#, GND
SMB_CLK_GPU
SMB_DATA_GPU
ADM1032ARMZ-2REEL_MSOP8
@

## Internal Thermal Sensor

Address: 0x9E H

To VGA
SMB_CLK_GPU [22]
SMB_DATA_GPU [22]
THERM#_VGA_R [22]
+3VGS
R1134 DIS@ 100K_0402_5%

+3VGS
R1135 2.2K_0402_5% DIS@
R1136 2.2K_0402_5% DIS@
SMB_CLK_GPU
SMB_DATA_GPU
Q75A DIS@ 2N7002KDWH_SOT363-6
Q75B DIS@ 2N7002KDWH_SOT363-6
EC_SMB_CK2 [14,49,52]
EC_SMB_DA2 [14,49,52]
To EC

## Reserve VBIOS for NV suggest (1Mbit)

+3VGS
R379 10K_0402_5%
R754 4.7K_0402_5% SPI_WP#_VGA
R750 4.7K_0402_5% SPI_HOLD#_VGA
ROM_CS#
U54
CE#, WP#, HOLD#, VSS, VDD, SCK, SI, SO
MX25L1005AMC-12G_SOP8
C1447 0.1U_0402_16V4Z
ROM_SCLK
ROM_SI
ROM_SO

| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2009/01/01 | Deciphered Date | 2010/01/01 |

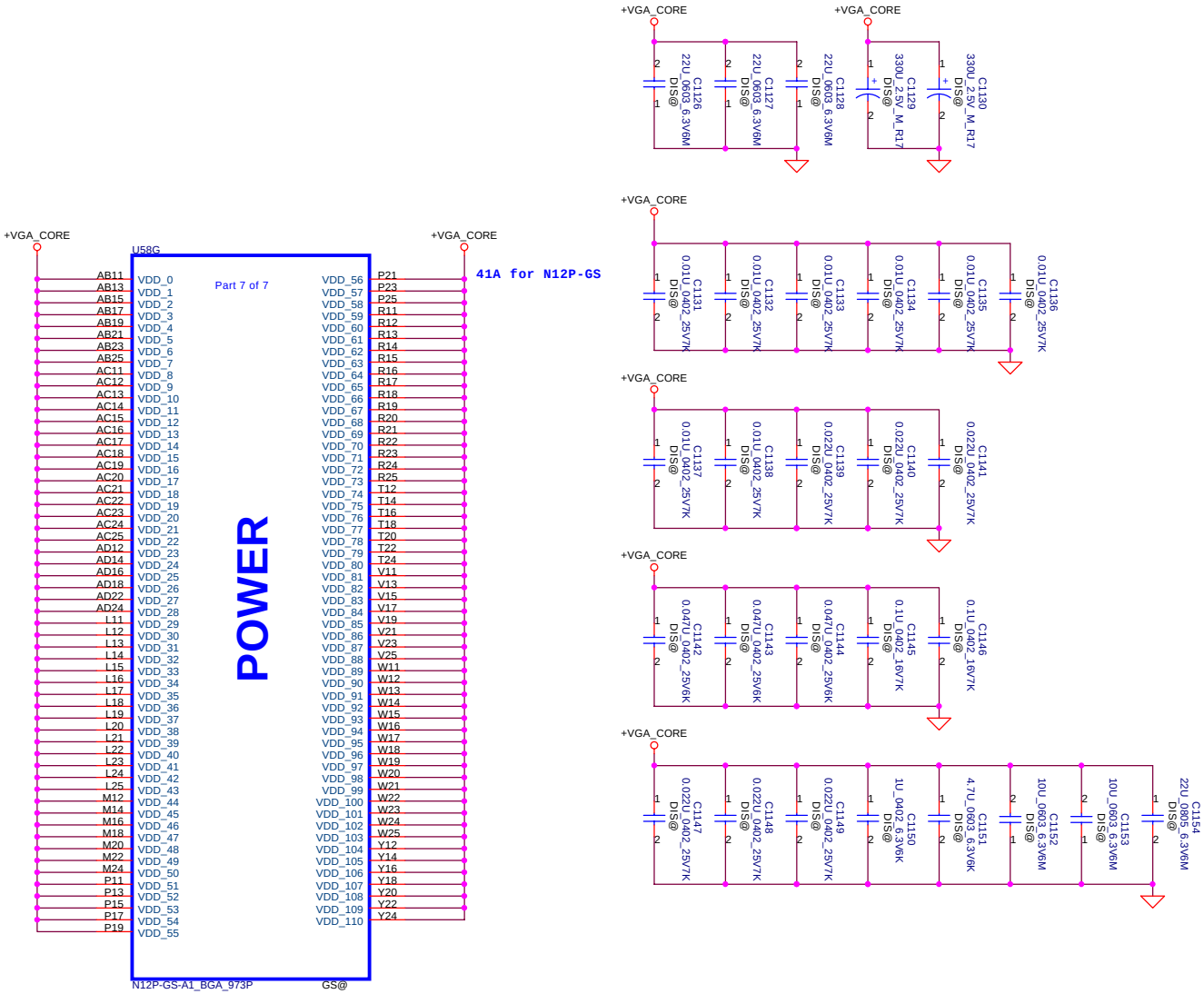


Compal Electronics, Inc.

Title: VGA_LVDS/HDMI/THERM/eDP

Size | Document Number: PCA70 LA-7521P M/B | Rev: 0.1

Date: Tuesday, April 12, 2011 | Sheet 23 of 64




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2009/01/01 | Deciphered Date | 2010/01/01 |

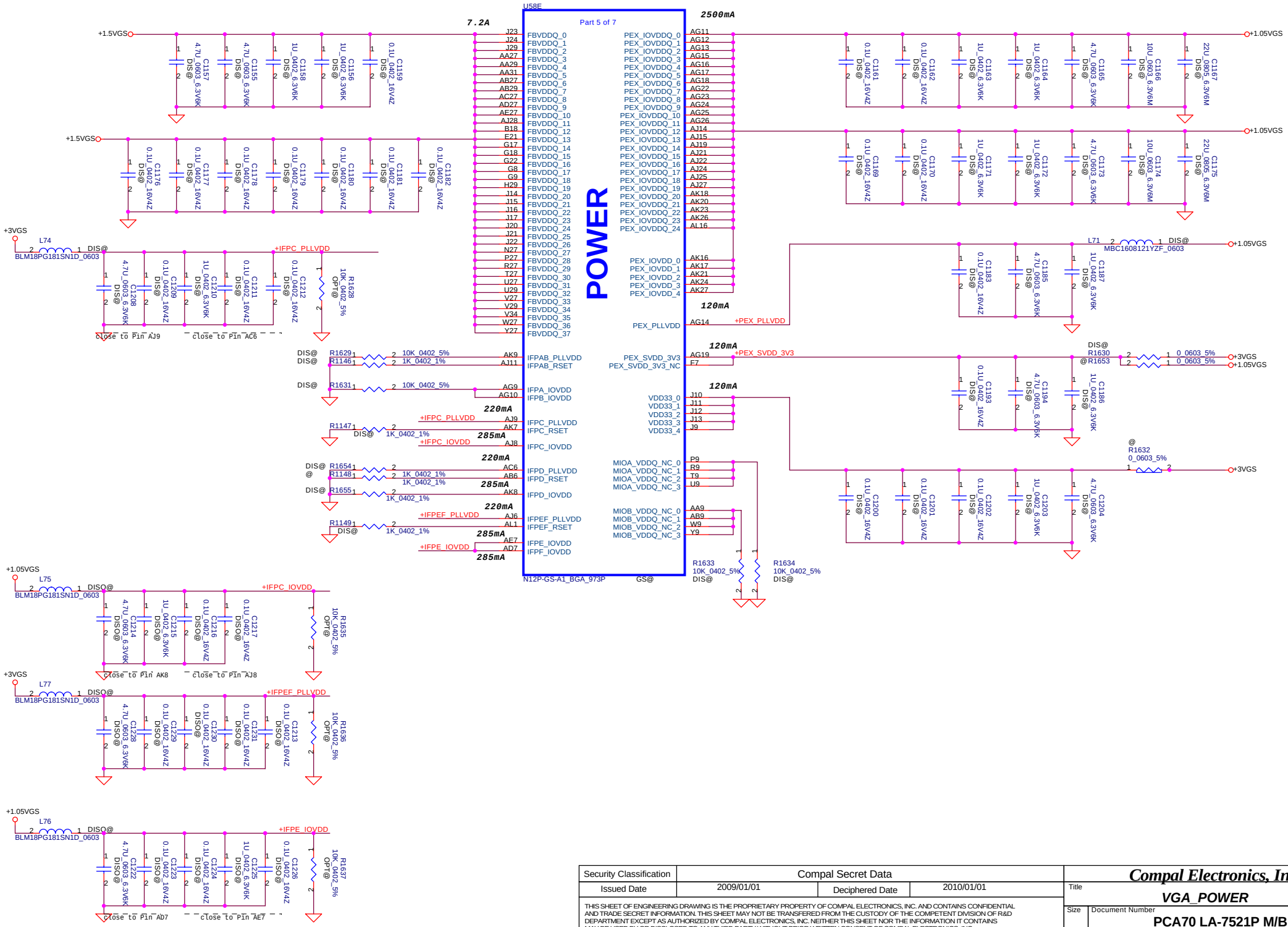


**Compal Electronics, Inc.**

Title: VGA_VGA CORE

Size | Document Number: PCA70 LA-7521P M/B | Rev: 0.1

Date: Tuesday, April 12, 2011 | Sheet 24 of 64




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2009/01/01 | Deciphered Date | 2010/01/01 |

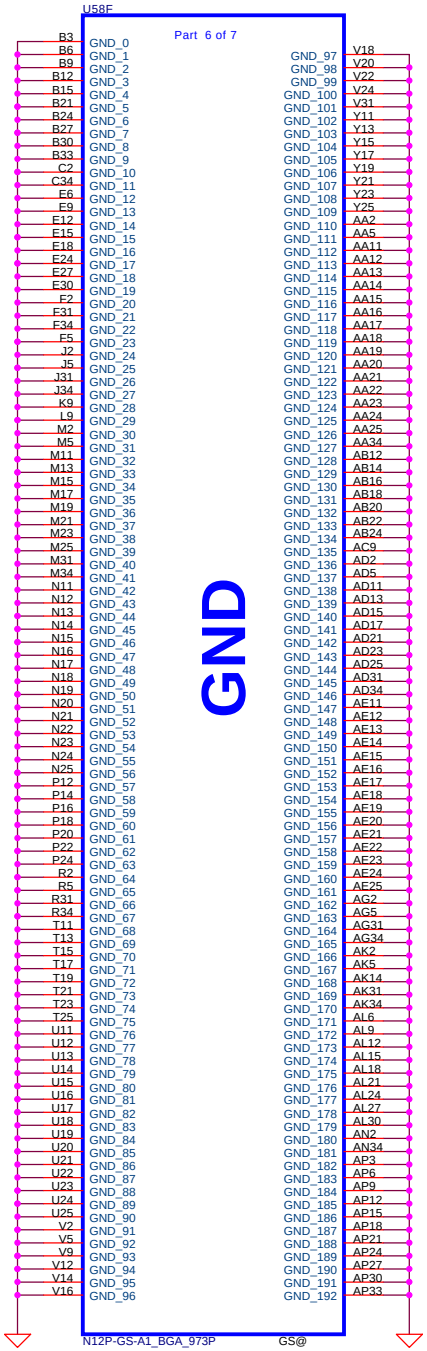


**Compal Electronics, Inc.**

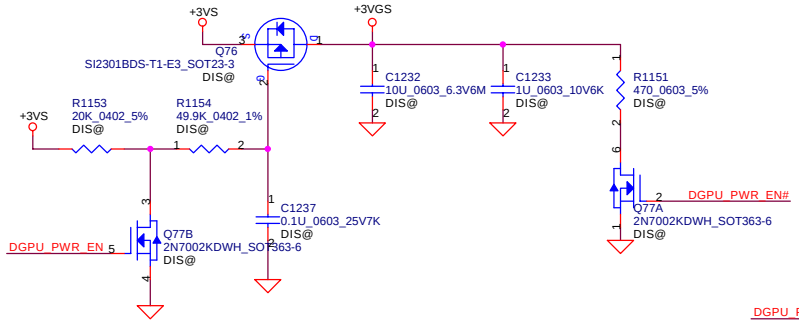
Title: VGA_POWER

Size | Document Number: PCA70 LA-7521P M/B | Rev: 0.1

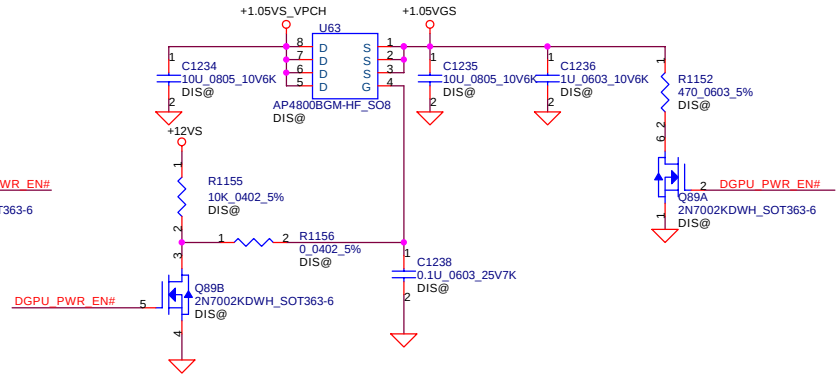
Date: Tuesday, April 12, 2011 | Sheet 25 of 64

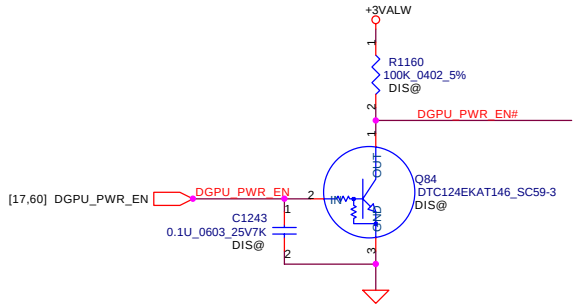



## +3.3VS TO +3.3VGS

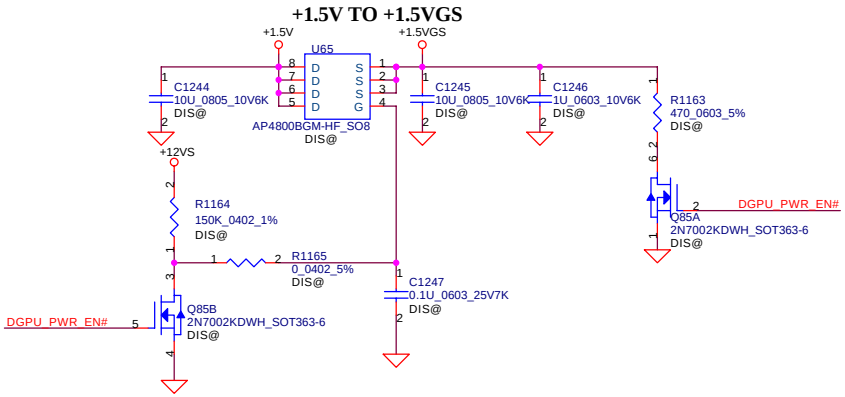



## +1.05VS_VCCIO TO +1.05VGS

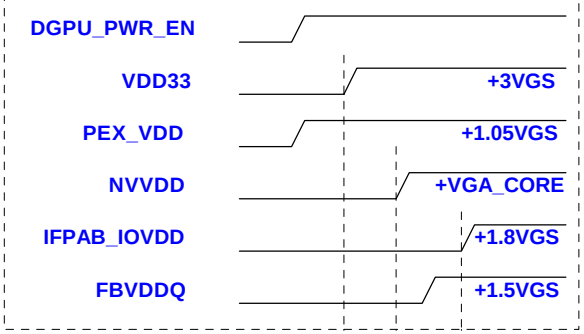



## +1.5V TO +1.5VGS




## Power Sequence of N12P_GS/GE,N12M_GE




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2009/01/01 | Deciphered Date | 2010/01/01 |

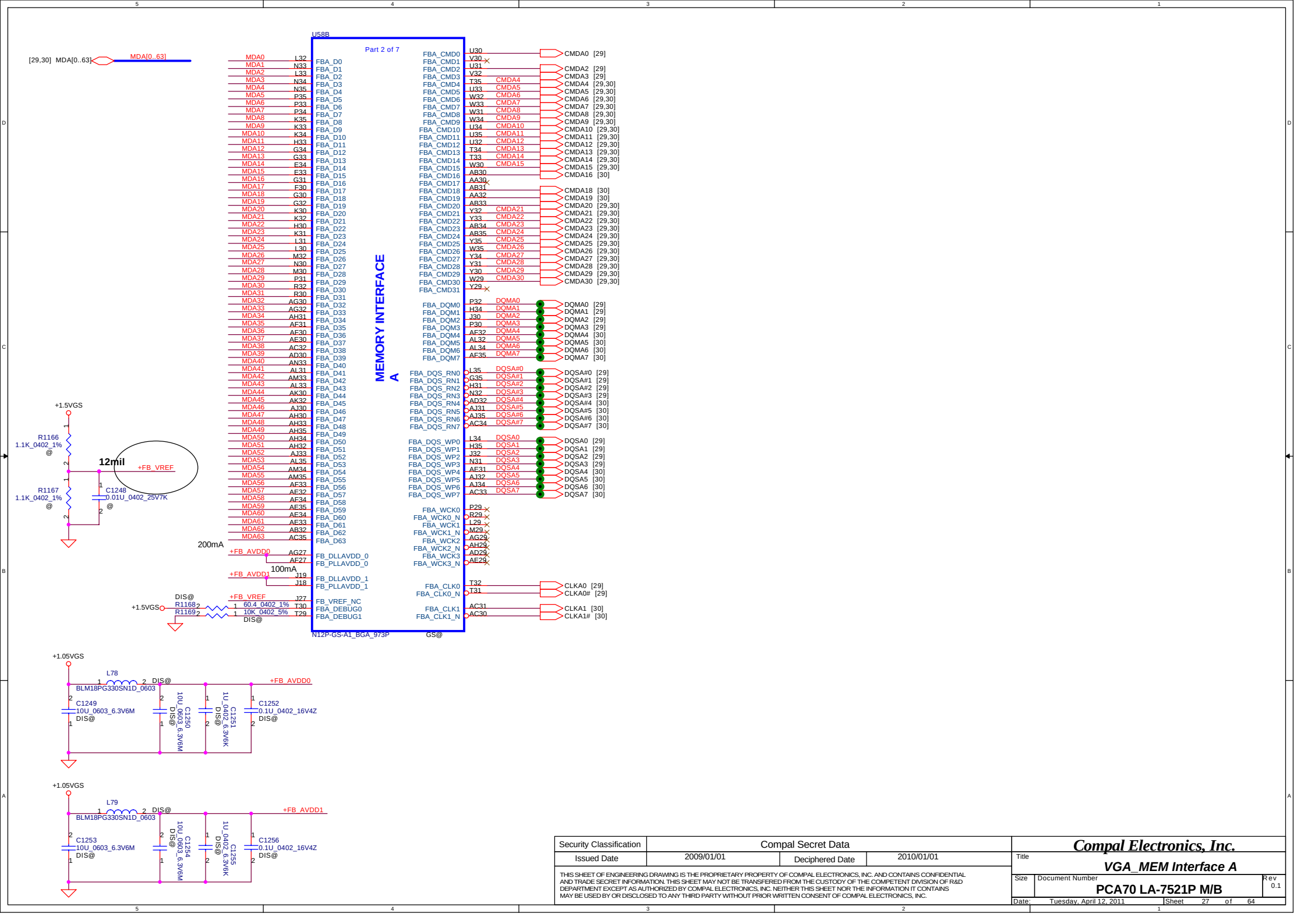


**Compal Electronics, Inc.**

Title: VGA_GND/POWER

Size | Document Number: PCA70 LA-7521P M/B | Rev: 0.1

Date: Tuesday, April 12, 2011 | Sheet 26 of 64




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2009/01/01 | Deciphered Date | 2010/01/01 |

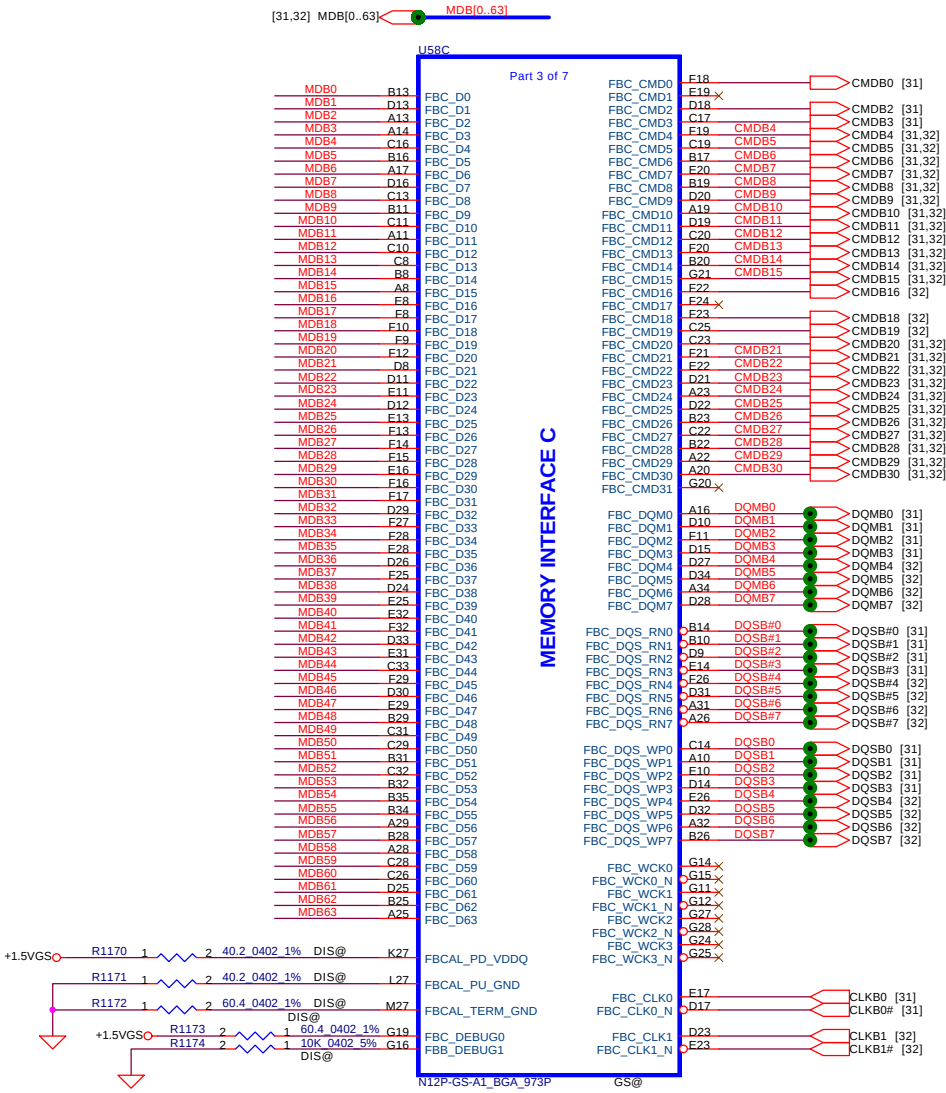


**Compal Electronics, Inc.**

Title: VGA_MEM Interface A

Size | Document Number: PCA70 LA-7521P M/B | Rev: 0.1

Date: Tuesday, April 12, 2011 | Sheet 27 of 64




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2009/01/01 | Deciphered Date | 2010/01/01 |



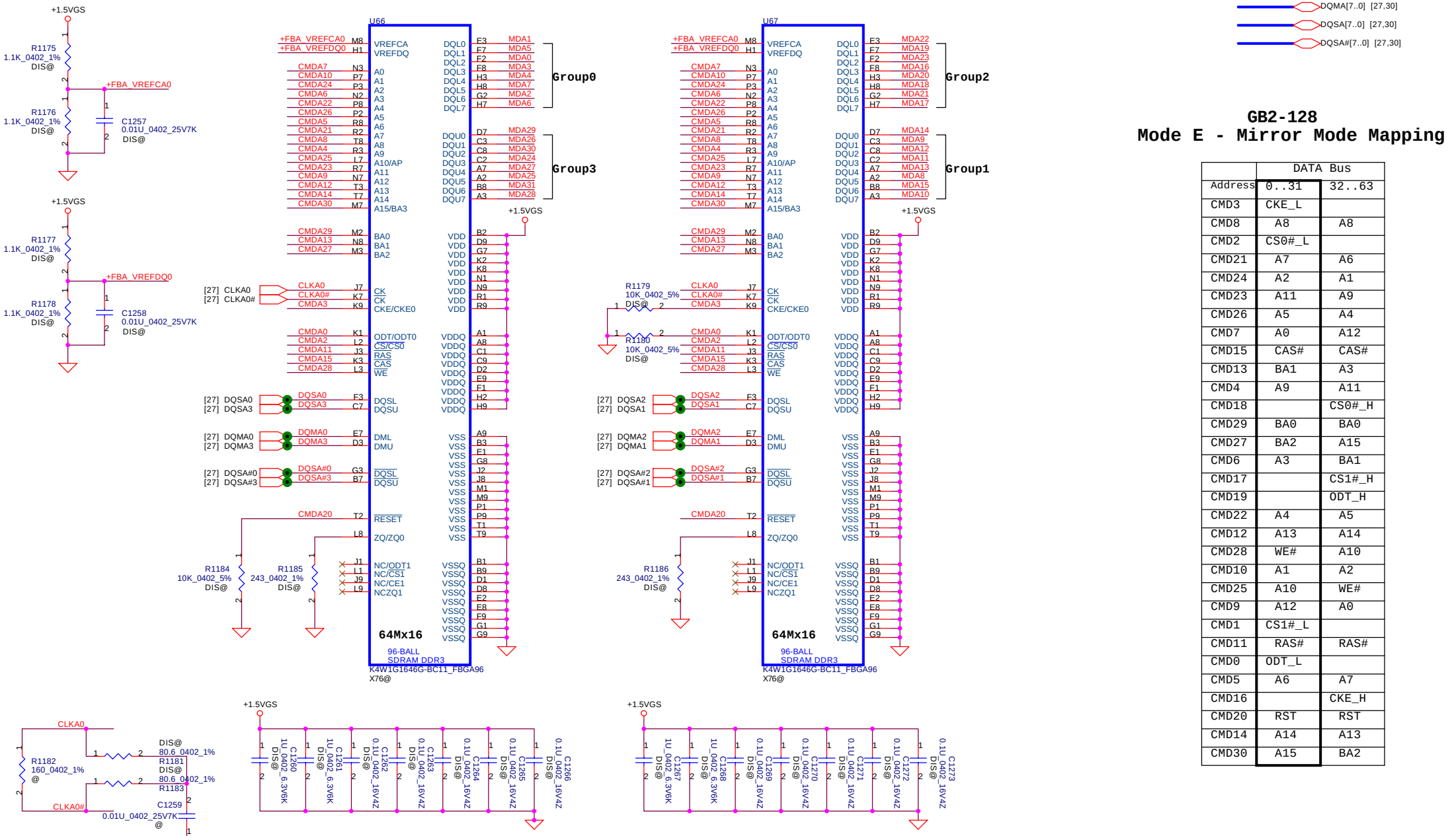
**Compal Electronics, Inc.**

Title: VGA_MEM Interface C

Size | Document Number: PCA70 LA-7521P M/B | Rev: 0.1

Date: Tuesday, April 12, 2011 | Sheet 28 of 64

# Memory Partition A - Lower 32 bits




## GB2-128
## Mode E - Mirror Mode Mapping

| | DATA Bus | |
|---|---|---|
| Address | 0..31 | 32..63 |
| CMD3 | CKE_L | |
| CMD8 | A8 | A8 |
| CMD2 | CS0#_L | |
| CMD21 | A7 | A6 |
| CMD24 | A2 | A1 |
| CMD23 | A11 | A9 |
| CMD26 | A5 | A4 |
| CMD7 | A0 | A12 |
| CMD15 | CAS# | CAS# |
| CMD13 | BA1 | A3 |
| CMD4 | A9 | A11 |
| CMD18 | | CS0#_H |
| CMD29 | BA0 | BA0 |
| CMD27 | BA2 | A15 |
| CMD6 | A3 | BA1 |
| CMD17 | | CS1#_H |
| CMD19 | | ODT_H |
| CMD22 | A4 | A5 |
| CMD12 | A13 | A14 |
| CMD28 | WE# | A10 |
| CMD10 | A1 | A2 |
| CMD25 | A10 | WE# |
| CMD9 | A12 | A0 |
| CMD1 | CS1#_L | |
| CMD11 | RAS# | RAS# |
| CMD0 | ODT_L | |
| CMD5 | A6 | A7 |
| CMD16 | | CKE_H |
| CMD20 | RST | RST |
| CMD14 | A14 | A13 |
| CMD30 | A15 | BA2 |

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2009/01/01 | Deciphered Date | 2010/01/01 |



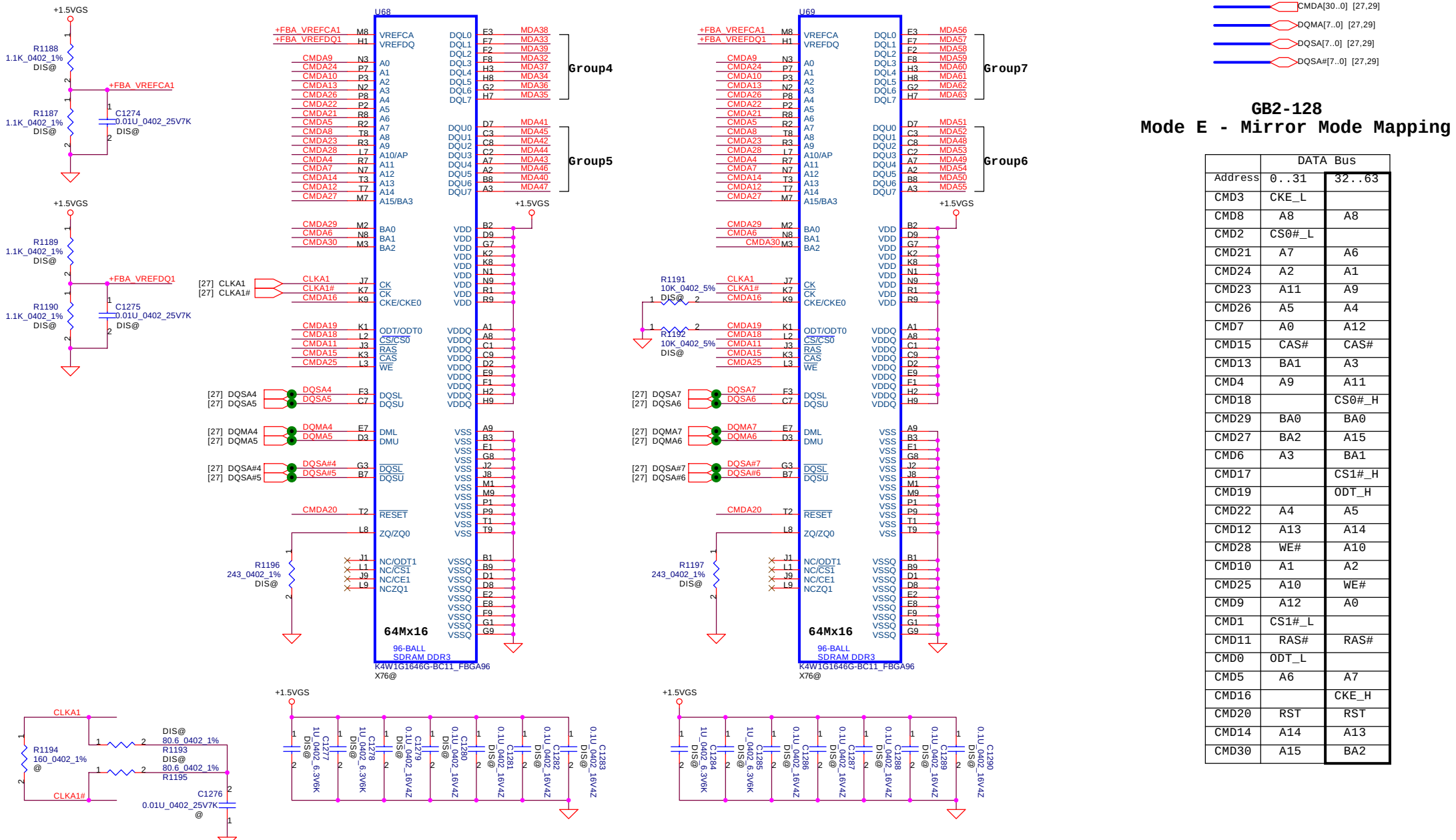
**Compal Electronics, Inc.**

Title: VGA_VRAM_A Lower

Size | Document Number: PCA70 LA-7521P M/B | Rev: 0.1

Date: Tuesday, April 12, 2011 | Sheet 29 of 64

# Memory Partition A - Upper 32 bits




## GB2-128
## Mode E - Mirror Mode Mapping

| | DATA Bus | |
|---|---|---|
| Address | 0..31 | 32..63 |
| CMD3 | CKE_L | |
| CMD8 | A8 | A8 |
| CMD2 | CS0#_L | |
| CMD21 | A7 | A6 |
| CMD24 | A2 | A1 |
| CMD23 | A11 | A9 |
| CMD26 | A5 | A4 |
| CMD7 | A0 | A12 |
| CMD15 | CAS# | CAS# |
| CMD13 | BA1 | A3 |
| CMD4 | A9 | A11 |
| CMD18 | | CS0#_H |
| CMD29 | BA0 | BA0 |
| CMD27 | BA2 | A15 |
| CMD6 | A3 | BA1 |
| CMD17 | | CS1#_H |
| CMD19 | | ODT_H |
| CMD22 | A4 | A5 |
| CMD12 | A13 | A14 |
| CMD28 | WE# | A10 |
| CMD10 | A1 | A2 |
| CMD25 | A10 | WE# |
| CMD9 | A12 | A0 |
| CMD1 | CS1#_L | |
| CMD11 | RAS# | RAS# |
| CMD0 | ODT_L | |
| CMD5 | A6 | A7 |
| CMD16 | | CKE_H |
| CMD20 | RST | RST |
| CMD14 | A14 | A13 |
| CMD30 | A15 | BA2 |

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2009/01/01 | Deciphered Date | 2010/01/01 |



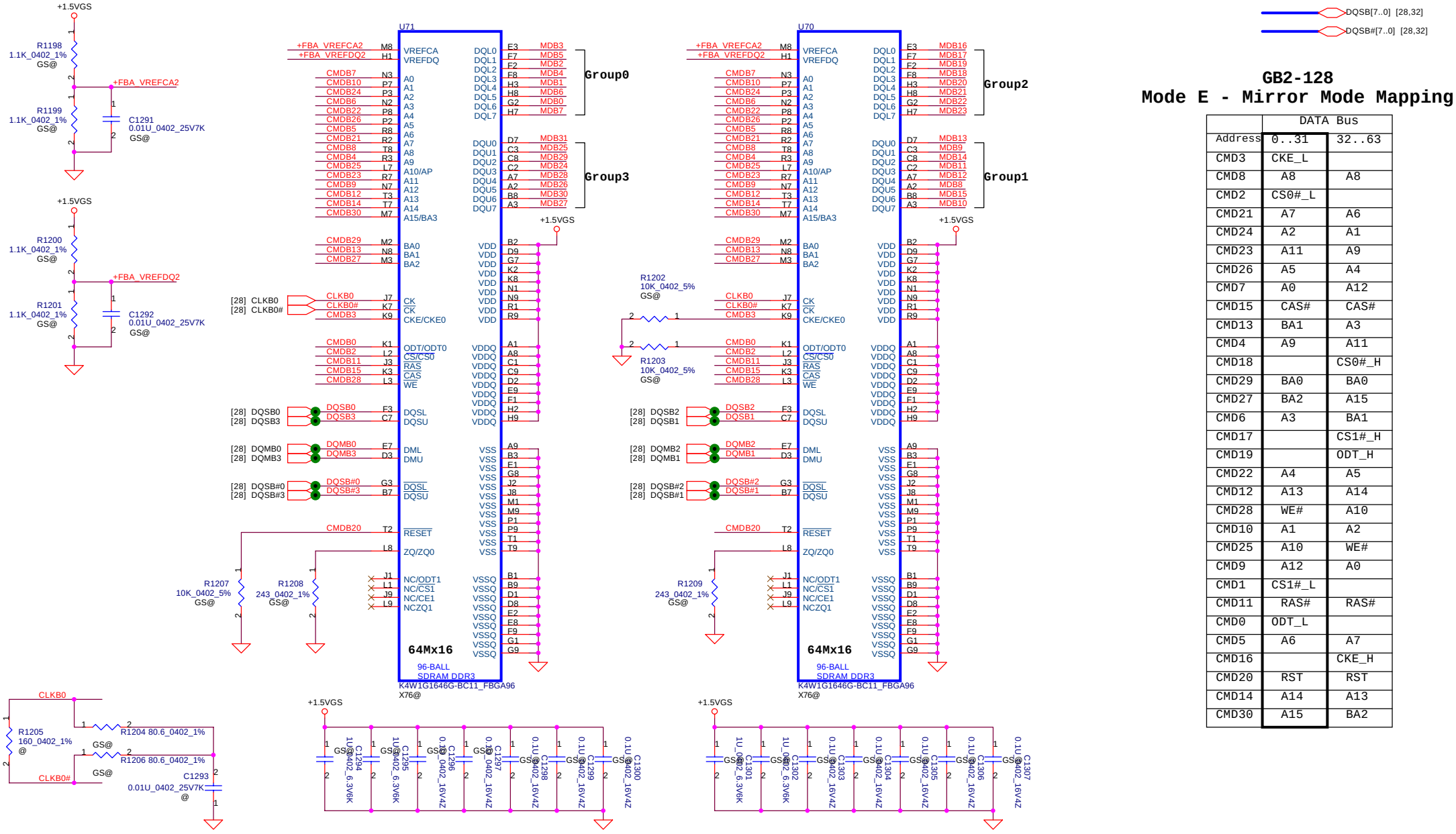
**Compal Electronics, Inc.**

Title: VGA_VRAM_A Upper

Size | Document Number: PCA70 LA-7521P M/B | Rev: 0.1

Date: Tuesday, April 12, 2011 | Sheet 30 of 64

# Memory Partition C - Lower 32 bits




## GB2-128
## Mode E - Mirror Mode Mapping

| | DATA Bus | |
|---|---|---|
| Address | 0..31 | 32..63 |
| CMD3 | CKE_L | |
| CMD8 | A8 | A8 |
| CMD2 | CS0#_L | |
| CMD21 | A7 | A6 |
| CMD24 | A2 | A1 |
| CMD23 | A11 | A9 |
| CMD26 | A5 | A4 |
| CMD7 | A0 | A12 |
| CMD15 | CAS# | CAS# |
| CMD13 | BA1 | A3 |
| CMD4 | A9 | A11 |
| CMD18 | | CS0#_H |
| CMD29 | BA0 | BA0 |
| CMD27 | BA2 | A15 |
| CMD6 | A3 | BA1 |
| CMD17 | | CS1#_H |
| CMD19 | | ODT_H |
| CMD22 | A4 | A5 |
| CMD12 | A13 | A14 |
| CMD28 | WE# | A10 |
| CMD10 | A1 | A2 |
| CMD25 | A10 | WE# |
| CMD9 | A12 | A0 |
| CMD1 | CS1#_L | |
| CMD11 | RAS# | RAS# |
| CMD0 | ODT_L | |
| CMD5 | A6 | A7 |
| CMD16 | | CKE_H |
| CMD20 | RST | RST |
| CMD14 | A14 | A13 |
| CMD30 | A15 | BA2 |



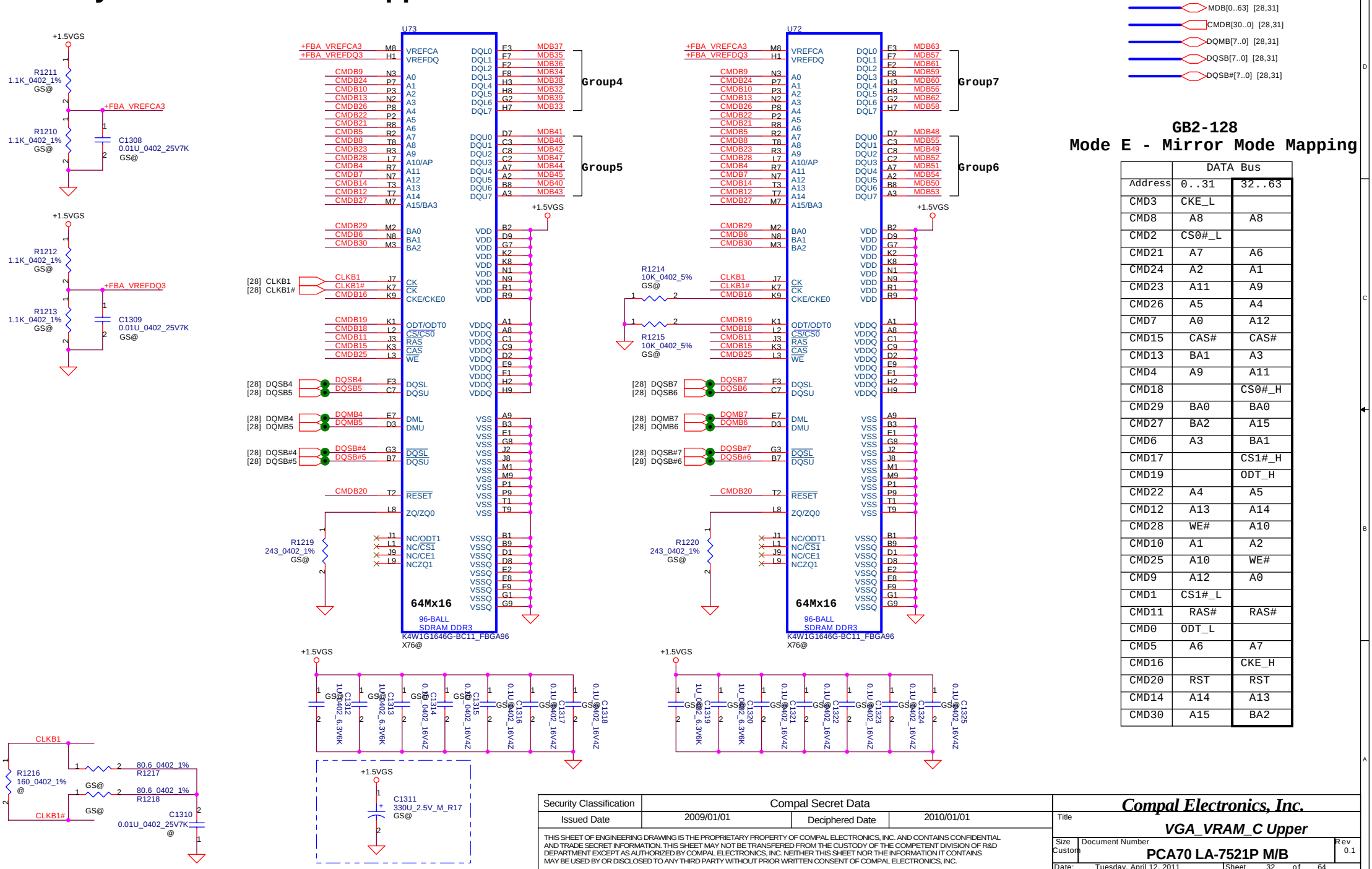
Compal Electronics, Inc.

Title: VGA_VRAM_C Lower

Size: Custom | Document Number: PCA70 LA-7521P M/B | Rev: 0.1

Date: Tuesday, April 12, 2011 | Sheet 31 of 64

# Memory Partition C - Upper 32 bits




## GB2-128
## Mode E - Mirror Mode Mapping

| | DATA Bus | |
|---|---|---|
| Address | 0..31 | 32..63 |
| CMD3 | CKE_L | |
| CMD8 | A8 | A8 |
| CMD2 | CS0#_L | |
| CMD21 | A7 | A6 |
| CMD24 | A2 | A1 |
| CMD23 | A11 | A9 |
| CMD26 | A5 | A4 |
| CMD7 | A0 | A12 |
| CMD15 | CAS# | CAS# |
| CMD13 | BA1 | A3 |
| CMD4 | A9 | A11 |
| CMD18 | | CS0#_H |
| CMD29 | BA0 | BA0 |
| CMD27 | BA2 | A15 |
| CMD6 | A3 | BA1 |
| CMD17 | | CS1#_H |
| CMD19 | | ODT_H |
| CMD22 | A4 | A5 |
| CMD12 | A13 | A14 |
| CMD28 | WE# | A10 |
| CMD10 | A1 | A2 |
| CMD25 | A10 | WE# |
| CMD9 | A12 | A0 |
| CMD1 | CS1#_L | |
| CMD11 | RAS# | RAS# |
| CMD0 | ODT_L | |
| CMD5 | A6 | A7 |
| CMD16 | | CKE_H |
| CMD20 | RST | RST |
| CMD14 | A14 | A13 |
| CMD30 | A15 | BA2 |

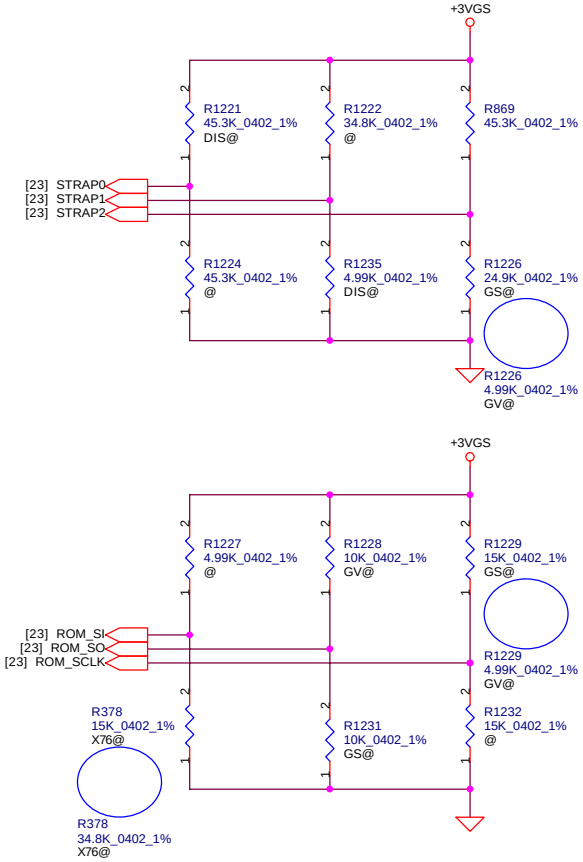


**Compal Electronics, Inc.**

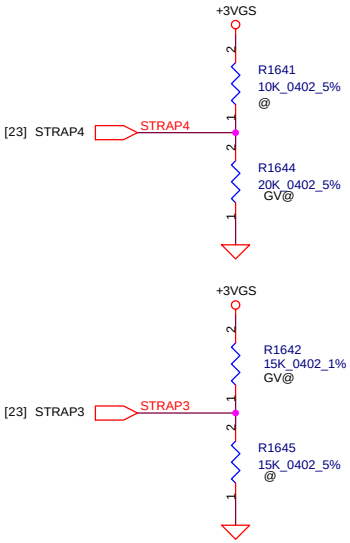
Title: VGA_VRAM_C Upper

Size: Custom | Document Number: PCA70 LA-7521P M/B | Rev: 0.1

Date: Tuesday, April 12, 2011 | Sheet 32 of 64




| Resistor Values | Pull-up to +3VGS | Pull-down to Gnd |
|---|---|---|
| 5K | 1000 | 0000 |
| 10K | 1001 | 0001 |
| 15K | 1010 | 0010 |
| 20K | 1011 | 0011 |
| 25K | 1100 | 0100 |
| 30K | 1101 | 0101 |
| 35K | 1110 | 0110 |
| 45K | 1111 | 0111 |




| Physical Strapping pin | | Power Rail | Logical Strapping Bit3 | Logical Strapping Bit2 | Logical Strapping Bit1 | Logical Strapping Bit0 |
|---|---|---|---|---|---|---|
| ROM_SO | GS | +3VGS | XCLK_417 | FB_0_BAR_SIZE | SMB_ALT_ADDR | VGA_DEVICE |
| | GV | | FB[1] | FB[0] | | |
| ROM_SCLK | GS | +3VGS | PCI_DEVID[4] | SUB_VENDOR | SLOT_CLK_CFG | PEX_PLL_EN_TERM |
| | GV | | | | PCI_DEVID[5] | |
| ROM_SI | | +3VGS | RAMCFG[3] | RAMCFG[2] | RAMCFG[1] | RAMCFG[0] |
| STRAP0 | | +3VGS | USER[3] | USER[2] | USER[1] | USER[0] |
| STRAP1 | | +3VGS | 3GIO_PADCFG[3] | 3GIO_PADCFG[2] | 3GIO_PADCFG[1] | 3GIO_PADCFG[0] |
| STRAP2 | | +3VGS | PCI_DEVID[3] | PCI_DEVID[2] | PCI_DEVID[1] | PCI_DEVID[0] |
| STRAP3 | | +3VGS | SOR3_EXPOSED | SOR2_EXPOSED | SOR1_EXPOSED | SOR0_EXPOSED |
| STRAP4 | | +3VGS | RESERVED | RESERVED | PCIE_MAX_SPEED | DP_PLL_VDD33V |

| GPU | Frenq. | Memory Size | Memory Config | strap0 | strap1 | strap2 | strap3 | strap4 | ROM_SI | ROM_SO | ROM_SCLK |
|---|---|---|---|---|---|---|---|---|---|---|---|
| N12P-GS | 900 MHz | 64M* 16* 8 1GB | Hynix (0x2) H5TQ1G63DFR-11C SA000041S60 | 1111 R1221 PU 45K | 0000 R1235 PD 5K | 0100 R1226 PD 25K | NC | NC | 0010 R453 PD 15K | 0001 R1231 PD 10K | 1010 R1229 PU 15K |
| N12P-GS | 900 MHz | 64M* 16* 8 1GB | Samsung (0x3) K4W1G1646G-BC11 SA00004GS30 | 1111 R1221 PU 45K | 0000 R1235 PD 5K | 0100 R1226 PD 25K | NC | NC | 0011 R378 PD 20K | 0001 R1231 PD 10K | 1010 R1229 PU 15K |
| N12P-GV | 900 MHz | 64M* 16* 4 512MB | Hynix (0x2) H5TQ1G63DFR-11C SA000041S60 | 1111 R1221 PU 45K | 0000 R1235 PD 5K | 0000 R1226 PD 5K | 1010 R1642 PU 15K | 0011 R1644 PD 20K | 0010 R378 PD 15K | 1001 R1228 PU 10K | 1000 R1229 PU 5K |
| N12P-GV | 900 MHz | 64M* 16* 4 512MB | Samsung (0x3) K4W1G1646G-BC11 SA00004GS30 | 1111 R1221 PU 45K | 0000 R1235 PD 5K | 0000 R1226 PD 5K | 1010 R1642 PU 15K | 0011 R1644 PD 20K | 0011 R378 PD 20K | 1001 R1228 PU 10K | 1000 R1229 PU 5K |
| N12P-GV | 800 MHz | 128M* 16* 4 1GB | Hynix (0x6) H5TQ2G63BFR-12C SA00003VS30 | 1111 R1221 PU 45K | 0000 R1235 PD 5K | 0000 R1226 PD 5K | 1010 R1642 PU 15K | 0011 R1644 PD 20K | 0110 R378 PD 35K | 1001 R1228 PU 10K | 1000 R1229 PU 5K |

**SUB_VENDOR**

| | |
|---|---|
| **0** | No VBIOS ROM (Default) |
| 1 | BIOS ROM is present |

**XCLK_417**

| | |
|---|---|
| **0** | 277MHz (Default) |
| 1 | Reserved |

**FB_0_BAR_SIZE**

| | |
|---|---|
| 0 | 256MB (Default) |
| 1 | Reserved |

**User [3:0]**

| | |
|---|---|
| 1111 | EDID is used 1920x1080 |
| 1000-1100 | Customer defined |

**3GIO_PADCFG[3:0]**

| | |
|---|---|
| 0000 | RESERVED |
| 0110 | Notebook Default |

**PEX_PLL_EN_TERM**

| | |
|---|---|
| **0** | Disable (Default) |
| 1 | Enable |

**SLOT_CLOCK_CFG**

| | |
|---|---|
| 0 | GPU and MCH don't share a common reference clock |
| 1 | GPU and MCH share a common reference clock (Default) |

**SMBUS_ALT_ADDR**

| | |
|---|---|
| **0** | 0x9E (Default) |
| 1 | 0x9C (Multi-GPU usage) |

**VGA_DEVICE**

| | |
|---|---|
| 0 | 3D Device |
| **1** | VGA Device (Default) |

**PCIE_MAX_SPEED**

| | |
|---|---|
| 1 | Default |

**DP_PLL_VDD33V**

| | |
|---|---|
| 0 | Default |

| GPU | Package | DeviceID | PCI_DEVID[5..0] |
|---|---|---|---|
| N12P-GS | GB2-128 | 0x0DF4 | (..1111 0100) |
| N12P-GV-B | GB2b-128 | 0x1050 | (..0101 0000) |

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2009/01/01 | Deciphered Date | 2010/01/01 |



*Compal Electronics, Inc.*

Title: *VGA_MSIC*

Size: Custom | Document Number: PCA70 LA-7521P M/B | Rev: 0.1

Date: Tuesday, April 12, 2011 | Sheet 33 of 64

pre-MP Scaler power soft start

PVT change to KBC control for EUP S5 over 1W

+3V TO +1.2VALW

151mA

600mA

MP for S5 HDMI_IN no function.

+1.2VALW=1+R533/R535

FOR Scalar Firmware Code

58mA

116mA

INTERNAL HDMI

EXTERNAL HDMI-IN

HDMI-Port0

HDMI-Port1

0.67mA

EXTERNAL D-Sub-IN

LVDS

DVT add Pull high for PNL_STAT, HDMI_CABLE_DET

To AMP SPK Enable pin

PVT for DIS/UMA FW control.

| Mode | PNL_STAT | PNL_STAT2 |
|---|---|---|
| PC | 0 | 0 |
| HDMI | 1 | 0 |
| VGA | 0 | 1 |

HDMI_STAT
High: OSD OFF
Low : OSD ON

MP change from 0ohm for ENI

FOR OSD/HDCP Parameter Value

To AMP Input

To HP Out

To EC ADC

DVT add test point for Scalar dubug.

For Port1

For Port0

HDMI Port0 HPD

HDMI-IN

PCH

change to 75 ohm for HDCP protect.

close to U55( Scaler)

88mA

RTD2472D-GR_LQFP128_20X14

| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |

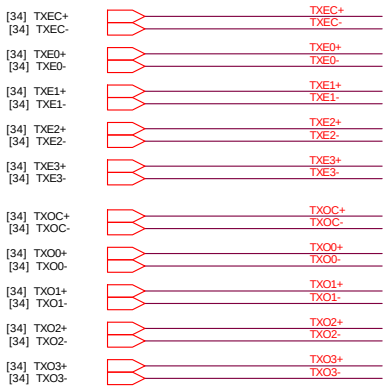


Compal Electronics, Inc.

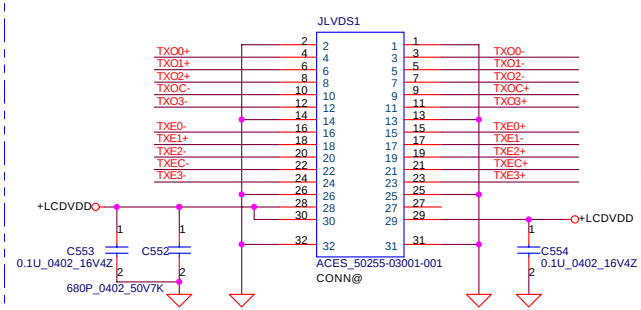
Title: Scaler RTD2472/82D

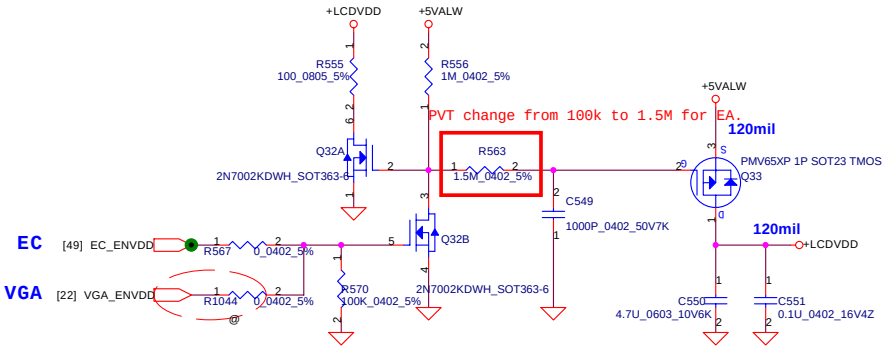
Size: | Document Number: PCA70 LA-7521P M/B | Rev: 0.1

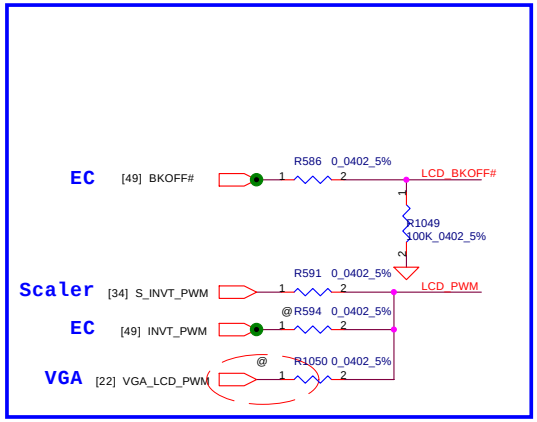
Date: Tuesday, April 12, 2011 | Sheet 34 of 64



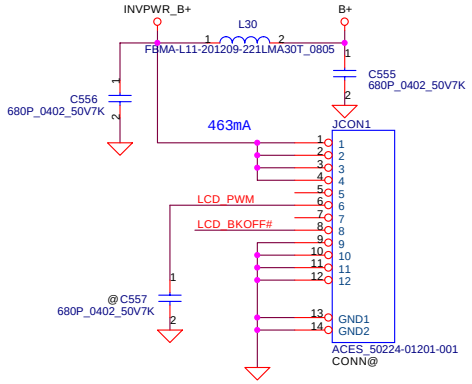

## For Scaler LVDS Conn.




## Converter




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |



**Compal Electronics, Inc.**

Title: ***LVDS***

| Size | Document Number | Rev |
|---|---|---|
| Custom | PCA70 LA-7521P M/B | 0.1 |

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DIS only

[23] VGA_SHDMI_ETXC+
[23] VGA_SHDMI_ETXC-
VGA_SHDMI_ETXC+ — DIS@ C1556 — 0.1U_0402_10V7K — HDMI_C_CLK+ — HDMI_C_CLK+ [34]
VGA_SHDMI_ETXC- — DIS@ C1557 — 0.1U_0402_10V7K — HDMI_C_CLK- — HDMI_C_CLK- [34]

[23] VGA_SHDMI_ETXD0+
[23] VGA_SHDMI_ETXD0-
VGA_SHDMI_ETXD0+ — DIS@ C1558 — 0.1U_0402_10V7K — HDMI_C_TX0+ — HDMI_C_TX0+ [34]
VGA_SHDMI_ETXD0- — DIS@ C1559 — 0.1U_0402_10V7K — HDMI_C_TX0- — HDMI_C_TX0- [34]

[23] VGA_SHDMI_ETXD1+
[23] VGA_SHDMI_ETXD1-
VGA_SHDMI_ETXD1+ — DIS@ C1560 — 0.1U_0402_10V7K — HDMI_C_TX1+ — HDMI_C_TX1+ [34]
VGA_SHDMI_ETXD1- — DIS@ C1561 — 0.1U_0402_10V7K — HDMI_C_TX1- — HDMI_C_TX1- [34]

[23] VGA_SHDMI_ETXD2+
[23] VGA_SHDMI_ETXD2-
VGA_SHDMI_ETXD2+ — DIS@ C1562 — 0.1U_0402_10V7K — HDMI_C_TX2+ — HDMI_C_TX2+ [34]
VGA_SHDMI_ETXD2- — DIS@ C1563 — 0.1U_0402_10V7K — HDMI_C_TX2- — HDMI_C_TX2- [34]

UMA only

[16] PCH_HDMI_CLK+
[16] PCH_HDMI_CLK-
PCH_HDMI_CLK+ — UMA@C1564 — 0.1U_0402_10V7K — HDMI_C_CLK+
PCH_HDMI_CLK- — UMA@C1565 — 0.1U_0402_10V7K — HDMI_C_CLK-

[16] PCH_HDMI_TX0+
[16] PCH_HDMI_TX0-
PCH_HDMI_TX0+ — UMA@C1566 — 0.1U_0402_10V7K — HDMI_C_TX0+
PCH_HDMI_TX0- — UMA@C1567 — 0.1U_0402_10V7K — HDMI_C_TX0-

[16] PCH_HDMI_TX1+
[16] PCH_HDMI_TX1-
PCH_HDMI_TX1+ — UMA@C1568 — 0.1U_0402_10V7K — HDMI_C_TX1+
PCH_HDMI_TX1- — UMA@C1569 — 0.1U_0402_10V7K — HDMI_C_TX1-

[16] PCH_HDMI_TX2+
[16] PCH_HDMI_TX2-
PCH_HDMI_TX2+ — UMA@C1570 — 0.1U_0402_10V7K — HDMI_C_TX2+
PCH_HDMI_TX2- — UMA@C1571 — 0.1U_0402_10V7K — HDMI_C_TX2-

INTEL use 680 Ohm for terminationn

UMA@ R635 680_0402_5%
UMA@ R636 680_0402_5%
UMA@ R637 680_0402_5%
UMA@ R638 680_0402_5%
UMA@ R639 680_0402_5%
UMA@ R640 680_0402_5%
UMA@ R642 680_0402_5%
UMA@ R643 680_0402_5%

+3VS
Q36
SSM3K7002BF 1N SC59-3
UMA@

pull down for HDMI 1.3 standard, remove in PVT phase.

NV use 499 Ohm for terminationn

DIS@ R642 499_0402_5%
DIS@ R643 499_0402_5%
DIS@ R639 499_0402_5%
DIS@ R640 499_0402_5%
DIS@ R635 499_0402_5%
DIS@ R636 499_0402_5%
DIS@ R637 499_0402_5%
DIS@ R638 499_0402_5%

+3VS
UMA@ R617 2.2K_0402_5%
R618 UMA@ 2.2K_0402_5%

[16] PCH_HDMI_DATA
[23] VGA_SHDMI_EDATA
PCH_HDMI_DATA — R1580 0_0402_5% UMA@ — R1581 0_0402_5% DIS@

[16] PCH_HDMI_CLK
[23] VGA_SHDMI_ECLK
PCH_HDMI_CLK — R1582 0_0402_5% UMA@ — R1583 0_0402_5% DIS@

+3VS
+5VS
R619 4.7K_0402_5%
R620 4.7K_0402_5%
Q35A
2N7002KDW_SOT363-6
Q35B
2N7002KDW_SOT363-6

S_HDMI_DATA — S_HDMI_DATA [34]
S_HDMI_CLK — S_HDMI_CLK [34]

[16] DDPC_HDP
DDPC_HDP — UMA@ R641 0_0402_5% — HDMI_HPD_LS — HDMI_HPD_LS [34]

[22] VGA_SHDMI_HPD
VGA_SHDMI_HPD — DIS@ R1584 0_0402_5%

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |

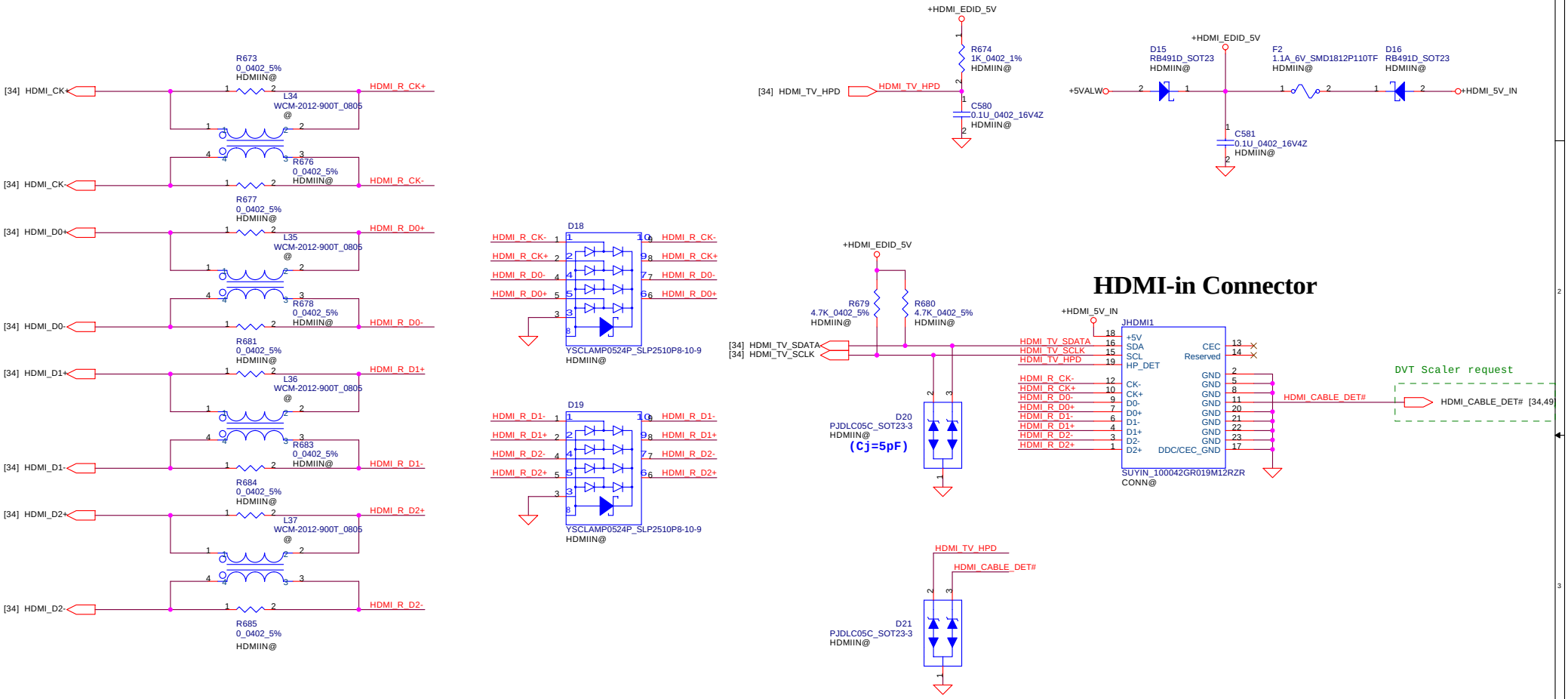


Compal Electronics, Inc.

Title: *HDMI Level Shift Scaler*

Size: Custom | Document Number: PCA70 LA-7521P M/B | Rev: 0.1

Date: Tuesday, April 12, 2011 | Sheet 36 of 64




# HDMI-in Connector

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |



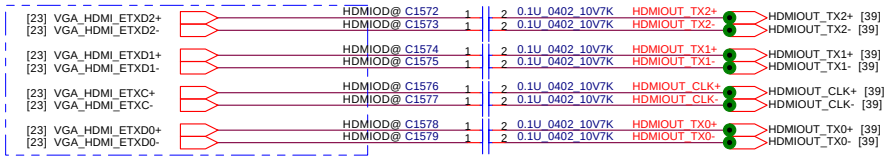
**Compal Electronics, Inc.**

Title: **HDMI-IN**

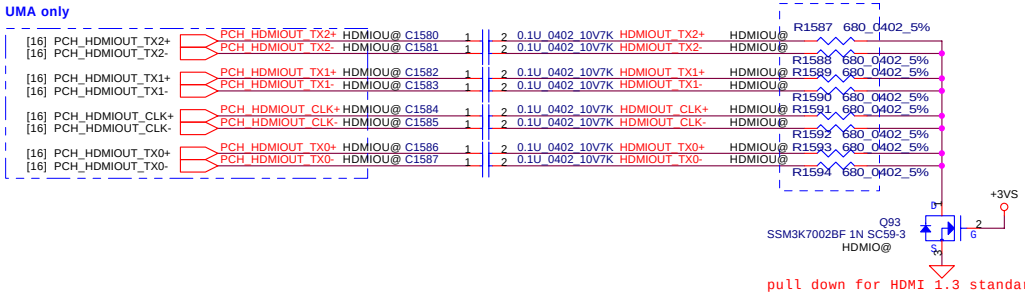
| Size | Document Number | Rev |
|---|---|---|
| Custom | PCA70 LA-7521P M/B | 0.1 |

Date: Tuesday, April 12, 2011 | Sheet 37 of 64

DIS only

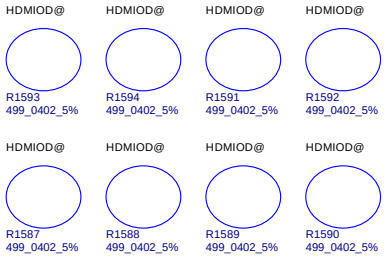



UMA only

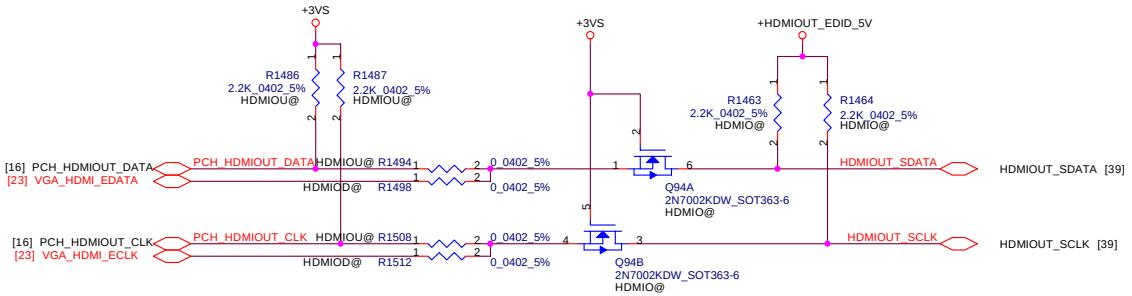



INTEL use 680 Ohm for terminationn

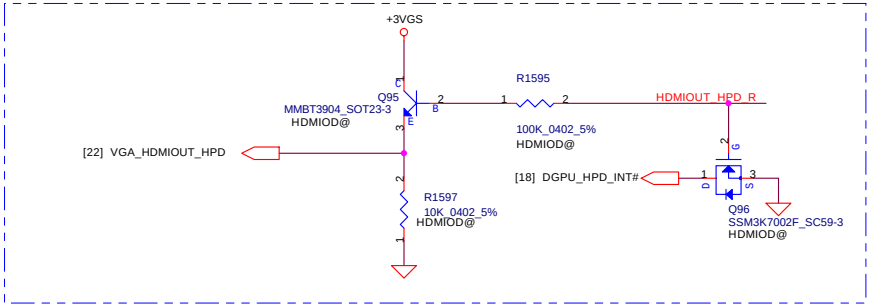
NV use 499 Ohm for terminationn



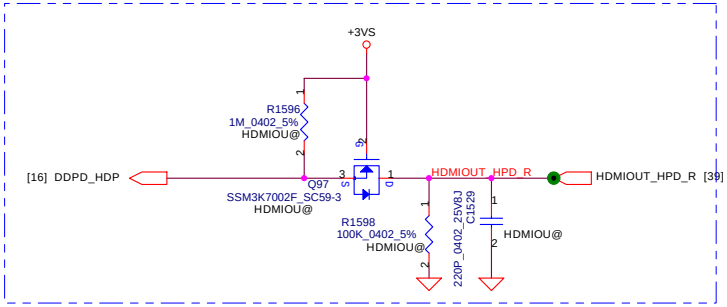

pull down for HDMI 1.3 standard, remove in PVT phase.




DIS only




UMA only




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |



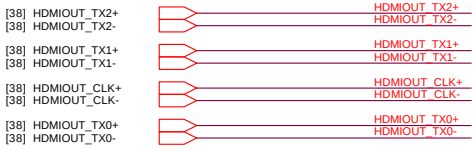
**Compal Electronics, Inc.**

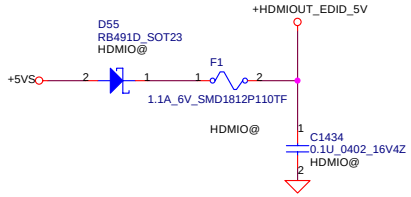
Title: ***HDMI-OUT Level Shift***

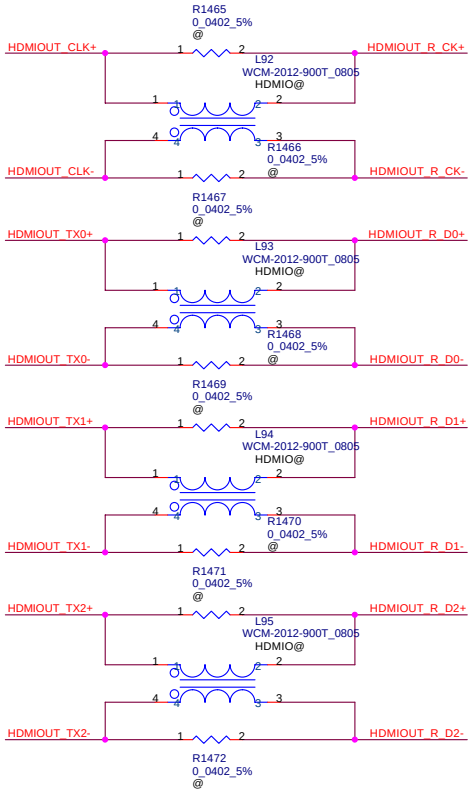
| Size | Document Number | Rev |
|---|---|---|
| Custom | PCA70 LA-7521P M/B | 0.1 |

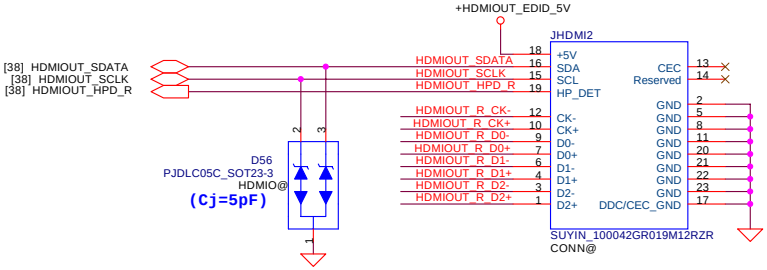
Date: Tuesday, April 12, 2011 | Sheet 38 of 64

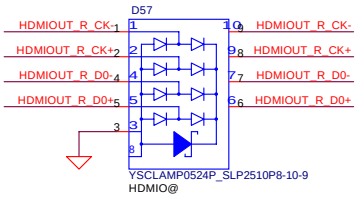
# HDMI-OUT Connector

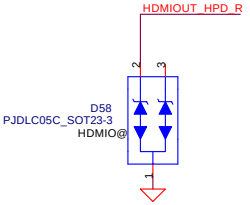


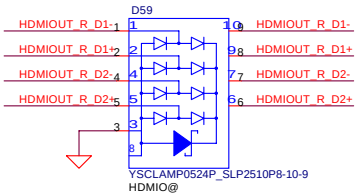




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |

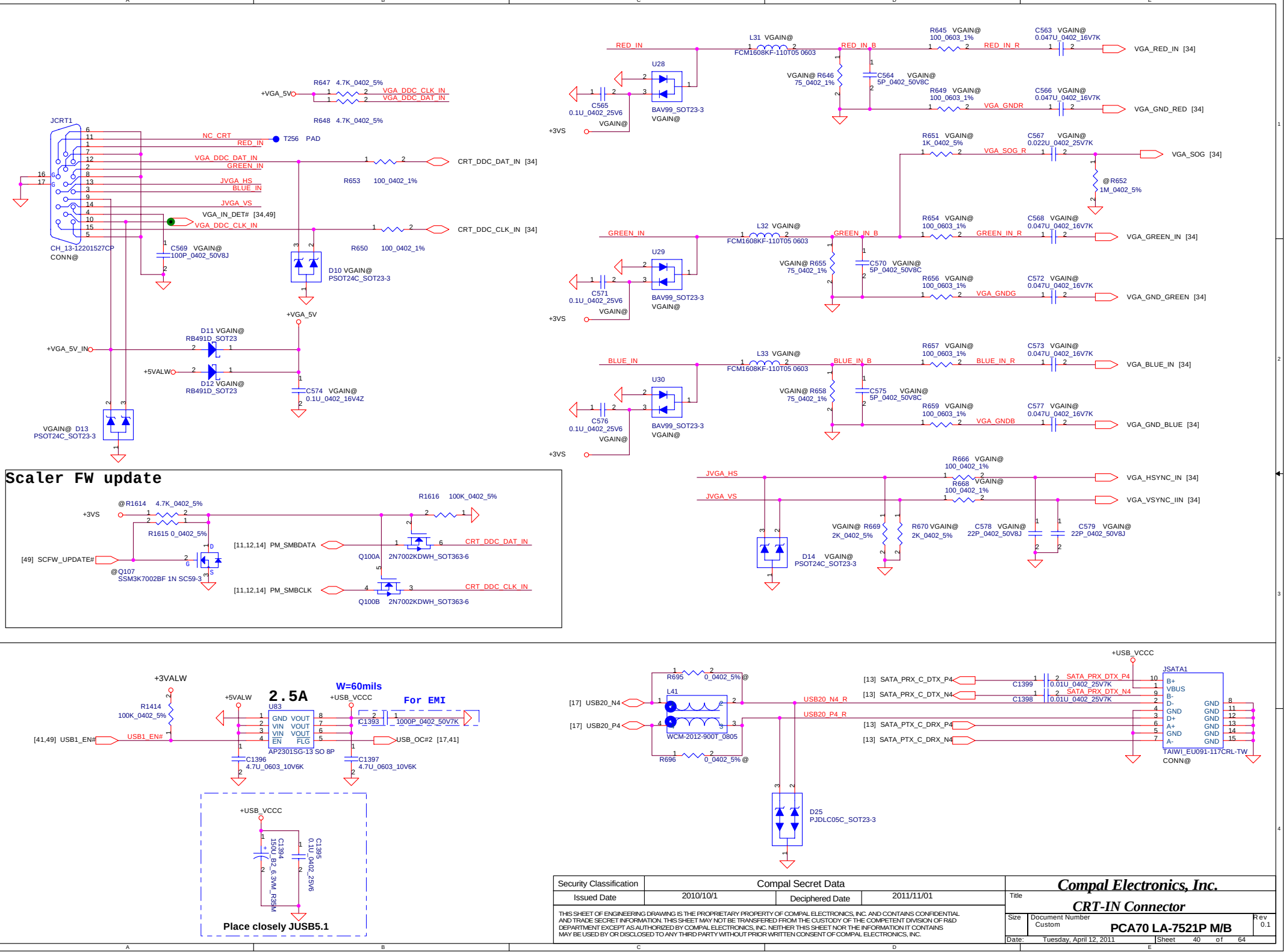


**Compal Electronics, Inc.**

Title: **HDMI-OUT**

| Size | Document Number | Rev |
|---|---|---|
| Custom | PCA70 LA-7521P M/B | 0.1 |

Date: Tuesday, April 12, 2011 | Sheet 39 of 64




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |



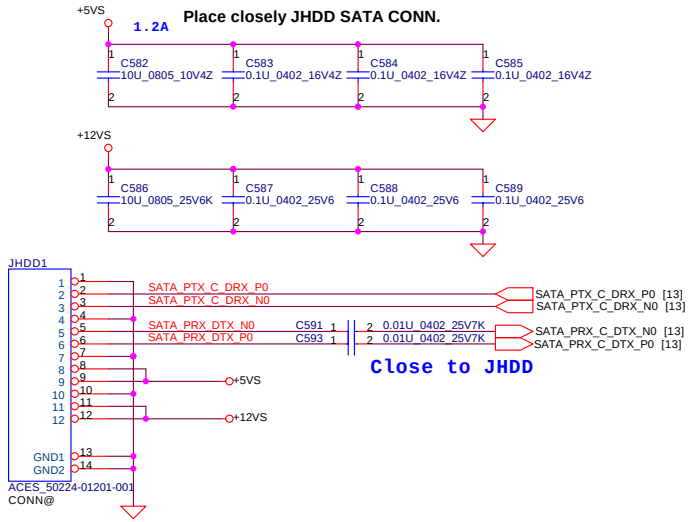
**Compal Electronics, Inc.**

Title: **CRT-IN Connector**

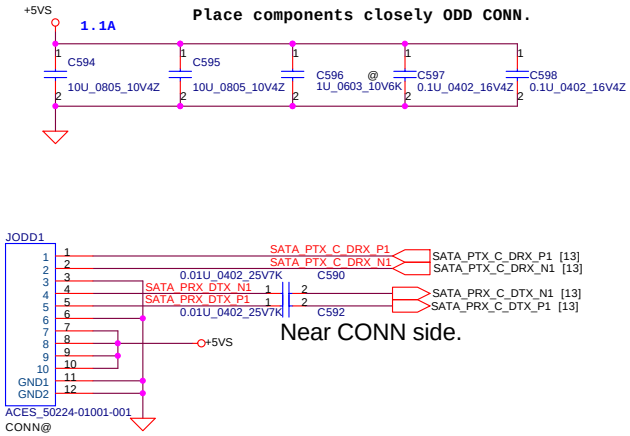
| Size | Document Number | Rev |
|---|---|---|
| Custom | PCA70 LA-7521P M/B | 0.1 |

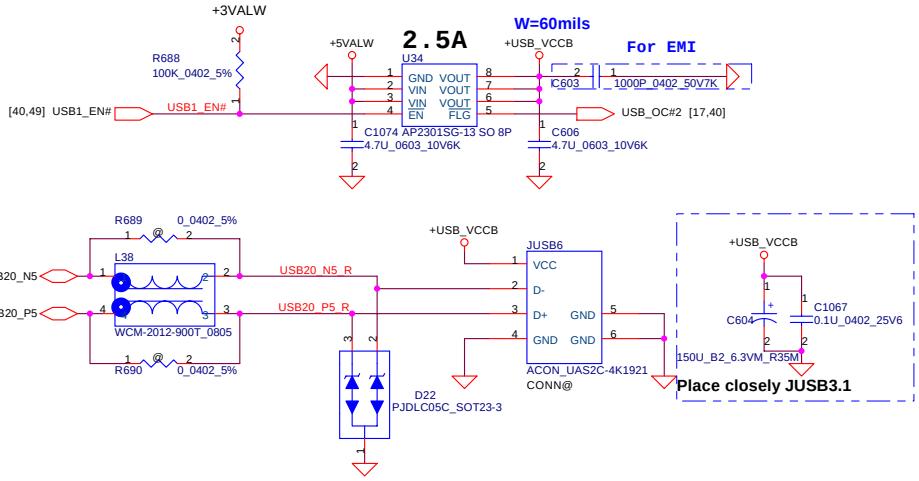
Date: Tuesday, April 12, 2011 Sheet 40 of 64

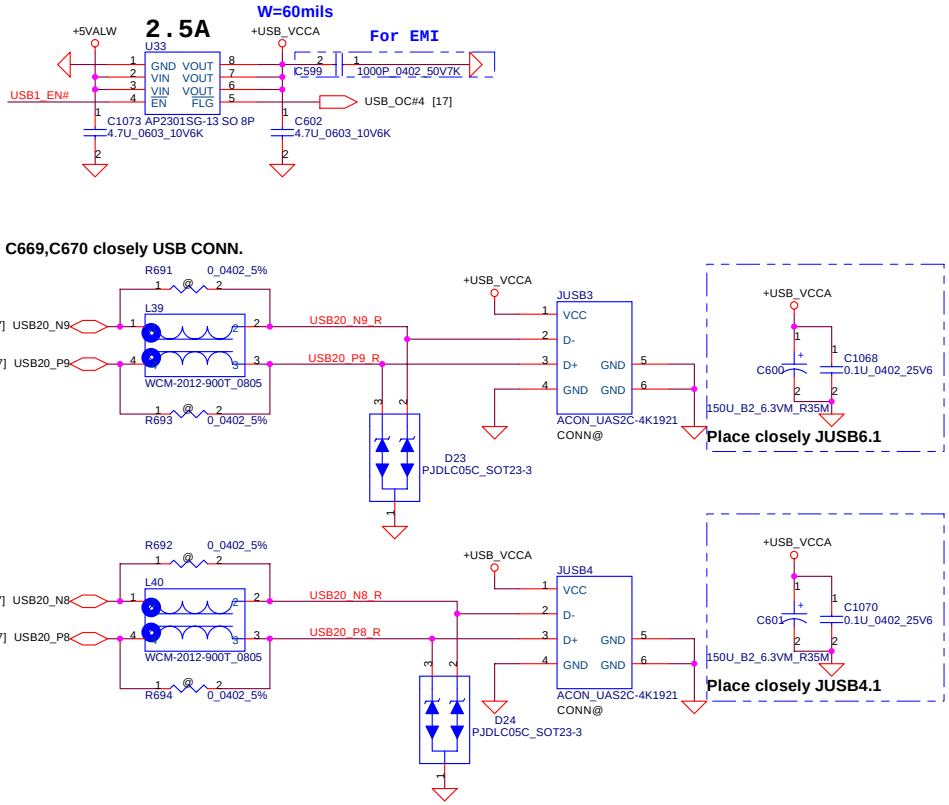
# SATA HDD Conn.




# SATA ODD Conn



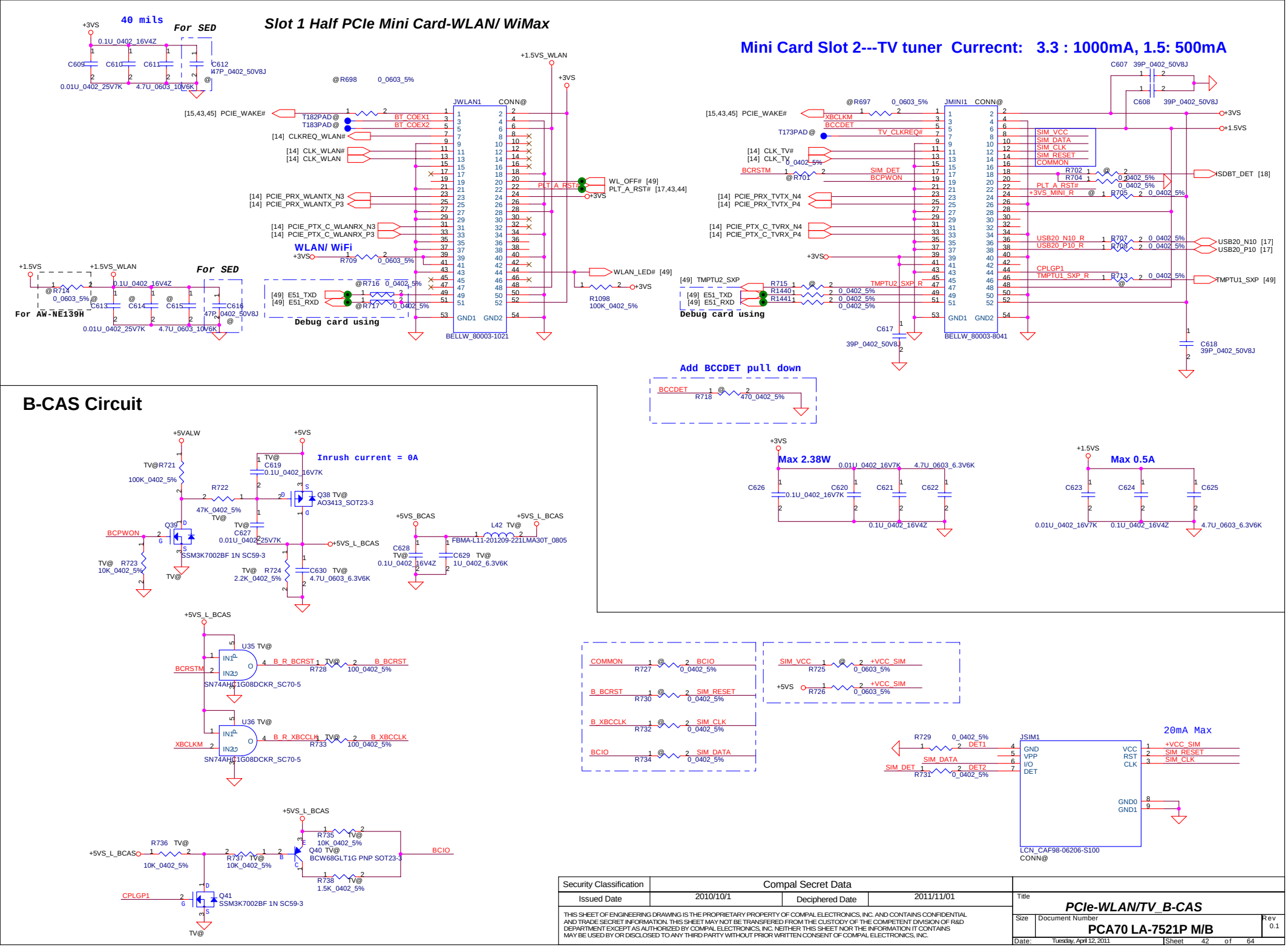




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |



| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title | SATA-HDD/ODD/USB | | |
| Size | Document Number | | Rev |
| | PCA70 LA-7521P M/B | | 0.1 |
| Date: Tuesday, April 12, 2011 | Sheet 41 of 64 | | |



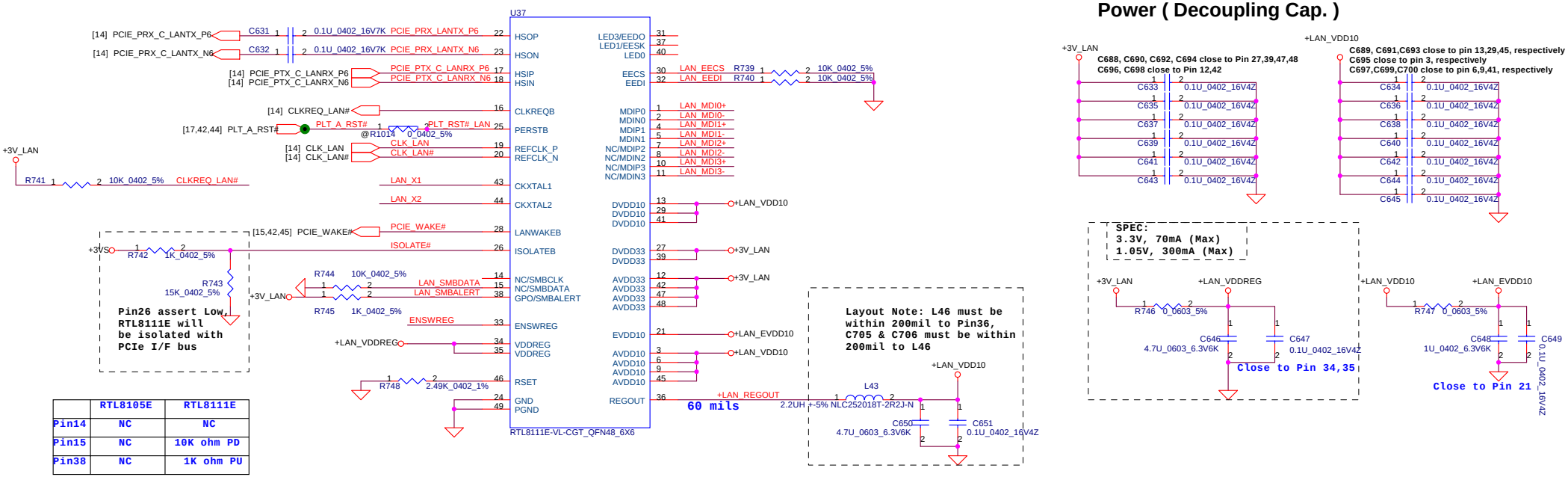

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |



Title: **PCIe-WLAN/TV_B-CAS**

| Size | Document Number | Rev |
|---|---|---|
| | PCA70 LA-7521P M/B | 0.1 |

Date: Tuesday, April 12, 2011 Sheet 42 of 64

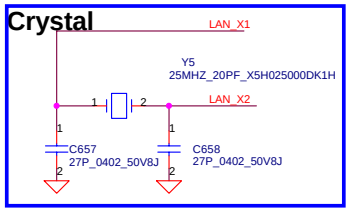


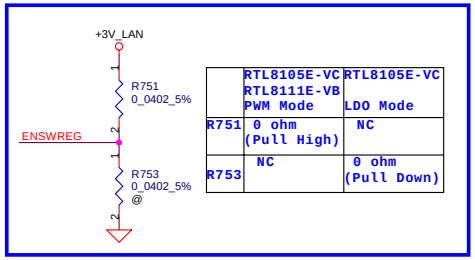

| | RTL8105E | RTL8111E |
|---|---|---|
| Pin14 | NC | NC |
| Pin15 | NC | 10K ohm PD |
| Pin38 | NC | 1K ohm PU |

## Power ( Decoupling Cap. )



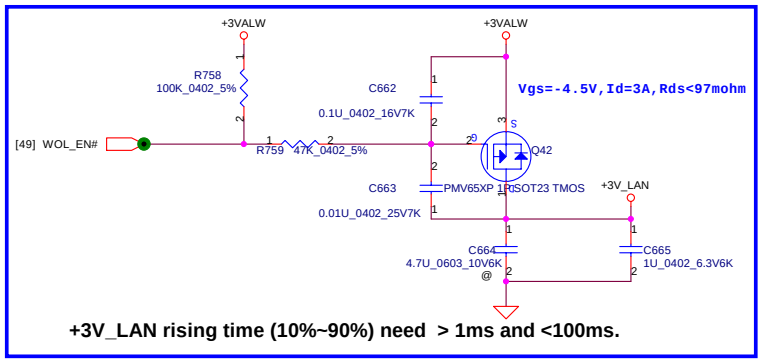

## Crystal



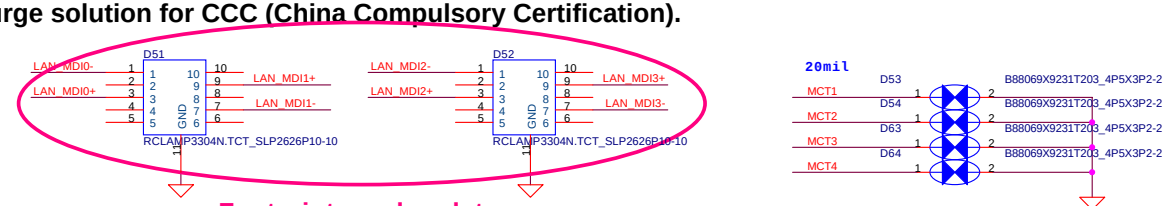

| | RTL8105E-VC RTL8111E-VB PWM Mode | RTL8105E-VC LDO Mode |
|---|---|---|
| R751 | 0 ohm (Pull High) | NC |
| R753 | NC | 0 ohm (Pull Down) |

## WOL circuit (Connect +3V_LAN to +3VALW)



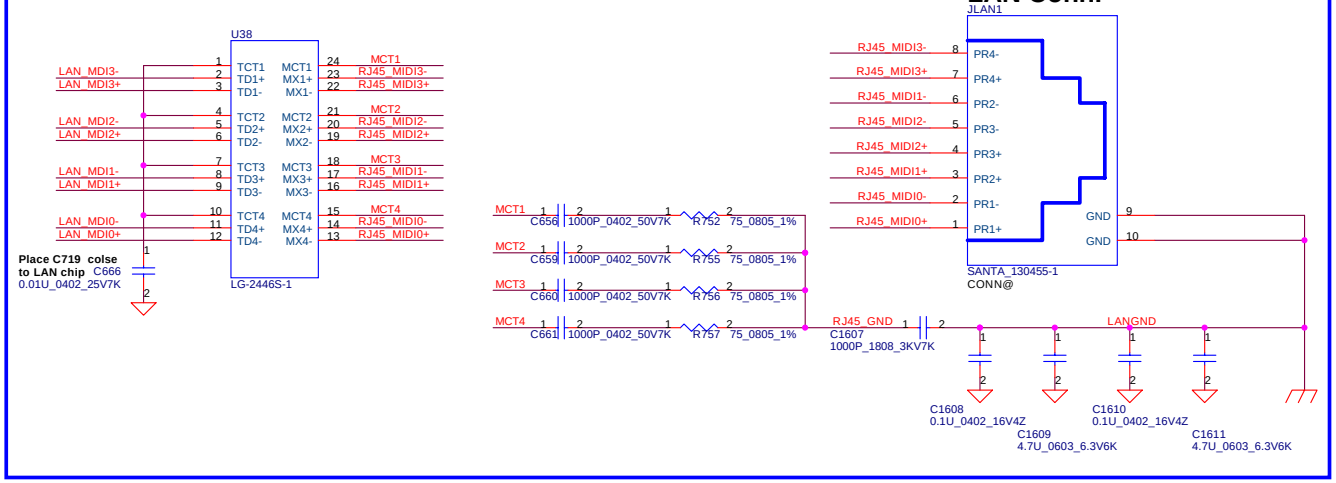

+3V_LAN rising time (10%~90%) need > 1ms and <100ms.

## EMI surge solution for CCC (China Compulsory Certification).




Footprint need update

## LAN Conn.




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |

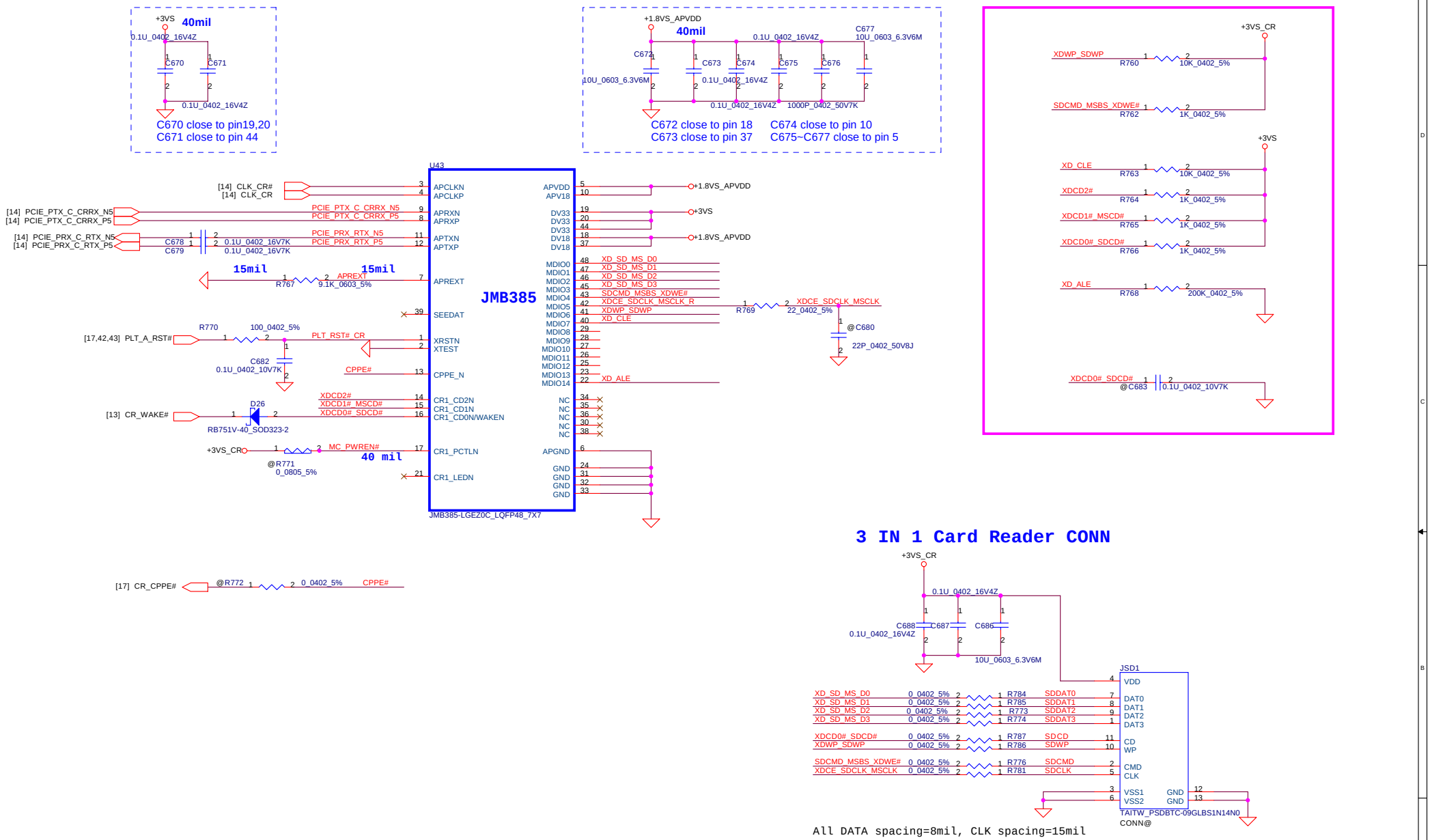


Compal Electronics, Inc.

Title: PCIe-LAN-RTL8111E

Size: Custom | Document Number | Rev 0.1

Date: Tuesday, April 12, 2011 | Sheet 43 of 64




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |



**Compal Electronics, Inc.**

Title: **JMB385 Media Card Controller**

| Size | Document Number | Rev |
|---|---|---|
| Custom | PCA70 LA-7521P M/B | 0.1 |

Date: Tuesday, April 12, 2011 | Sheet 44 of 64

## USB_PEPWRDET
For WAKE Function

| | R809 | R826 |
|---|---|---|
| D3 Hot | @ | Mount |
| D3 Cold | Mount | @ |

update PEPWRDET at D3 hot mode pull low

## USB_PESEL

| | R808 | R825 |
|---|---|---|
| Other applaction | Mount | @ |
| Express Card/Mini Card | @ | Mount |

**Close to ASM1042**

U44 ASM1042 (TQFN 64)
ASM1042_TQFN64_9X9
USB30@

U45 MX25L5121EMC-20G SOP 8P
USB30@

### Power On Sequence Timing Specification

| Symbols | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{VDR}$ | Rising time for Suspend Power Ready | | 10 | ms |
| $t_{PWRRDY}$ | Timing for Normal Power Ready | 50 | | ms |
| $t_{PORST1}$ | Timing for 1.2V/3.3V Normal Power Ready to Power On Reset (D3Cold) | 2 | 80 | ms |
| $t_{PORST2}$ | Timing for 1.2V/3.3V Normal Power Ready to Power On Reset (D3Hot) | 50 | 80 | ms |
| $t_{PECLK}$ | Timing for PE_CLK Ready to PE_RST# | 100 | | μs |
| $t_{CLK}$ | Timing for 20MHz Crystal Clock Ready to Power On Reset | | 20 | ms |
| $t_{PERST1}$ | Timing for PE_RST# delay after Normal Power Ready | 100 | | ms |
| $t_{PERST2}$ | Timing for PE_RST# delay after PORST# comes up | 20 | | ms |

### Power Sequence

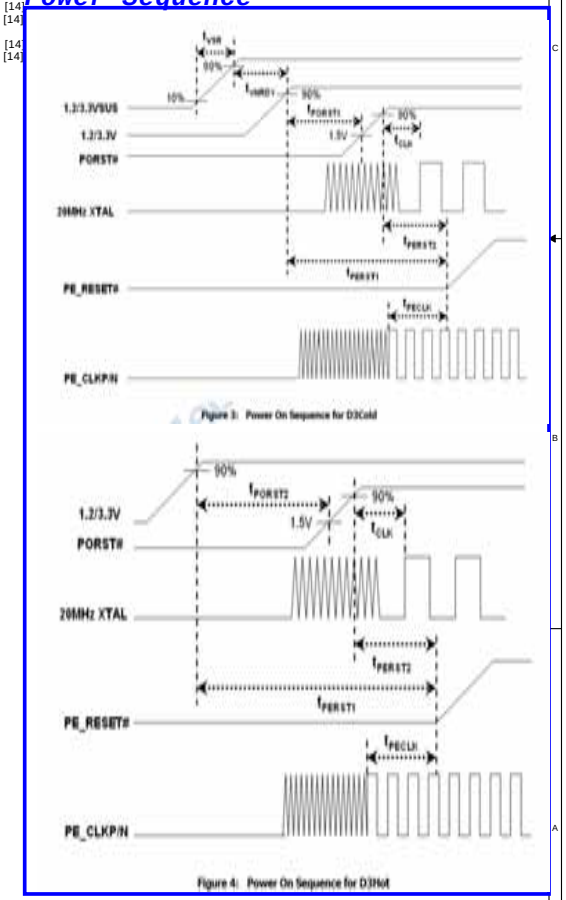



Figure 3: Power On Sequence for D3Cold




Figure 4: Power On Sequence for D3Hot

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |



**Compal Electronics, Inc.**

Title: USB3.0

Size: Custom | Document Number: PCA70 LA-7521P M/B | Rev: 0.2

Date: Tuesday, April 12, 2011 | Sheet 45 of 64

## For USB2.0 ESD diode

D27 PJUSB208H_SOT23-6

USB20_N1_L, USB20_P1_L, +USB30_VCCA

## For USB3.0 ESD diode

D38 YSCLAMP0524P_SLP2510P8-10-9 USB30@

U3TXDP_A_R, U3TXDN_A_R, U3RXDP_A_R_0, U3RXDN_A_R_0

## For USB2.0 ESD diode

D28 PJUSB208H_SOT23-6

USB20_N0_L, USB20_P0_L, +USB30_VCCA

## For USB3.0 ESD diode

D39 YSCLAMP0524P_SLP2510P8-10-9 USB30@

U3TXDP_B_R, U3TXDN_B_R, U3RXDP_B_R_1, U3RXDN_B_R_1

## USB3.0 Port A Connector

[17] USB20_N1 / [45] U2DN_A → USB20@ R880 / USB30@ R881 → USB20_N1_R

[17] USB20_P1 / [45] U2DP_A → USB20@ R882 / USB30@ R883 → USB20_P1_R

Layout placement as close as possable

R879 0_0402_5% @

L49 WCM-2012-900T_0805 USB30@

R884 0_0402_5% @

R885 0_0402_5% @

L50 USB30@ WCM-2012-900T_0805

R888 0_0402_5% @

R889 0_0402_5% @

L51 USB30@ WCM-2012-900T_0805

R890 0_0402_5% @

[45] U3TXDN_A_C → USB30@ C767 0.1U_0402_16V7K → U3TXDN_A

[45] U3TXDP_A_C → USB30@ C768 0.1U_0402_16V7K → U3TXDP_A

must to close to JUSB1

USB20_N1_L, USB20_P1_L, U3RXDN_A_R_0, U3RXDP_A_R_0, U3TXDN_A_R, U3TXDP_A_R

+USB30_VCCA W=60mils

JUSB1 OCTEK_USB-09EAEB CONN@

SSTX+, VBUS, SSTX-, D-, GND, D+, SSRX+, GND, SSRX-

+USB30_VCCA C765 150U_B2_6.3VM_R35M C1071 0.1U_0402_25V6

Place closely JUSB1.1

## USB2.0 Connector Co-lay with JUSB1 When USB30 not used

+USB30_VCCA JUSB7 OCTEK_USB-04APEB CONN@

USB20_N1_L, USB20_P1_L, GND

## USB3.0 Port B Connector

[17] USB20_N0 / [45] U2DN_B → USB20@ R892 / USB30@ R893 → USB20_N0_R

[17] USB20_P0 / [45] U2DP_B → USB20@ R894 / USB30@ R895 → USB20_P0_R

Layout placement as close as possable

R891 0_0402_5% @

L52 WCM-2012-900T_0805 USB30@

R896 0_0402_5% @

R897 0_0402_5% @

L53 USB30@ WCM-2012-900T_0805

R900 0_0402_5% @

R901 0_0402_5% @

L54 USB30@ WCM-2012-900T_0805

R902 0_0402_5% @

[45] U3TXDN_B_C → USB30@ C769 0.1U_0402_16V7K → U3TXDN_B

[45] U3TXDP_B_C → USB30@ C770 0.1U_0402_16V7K → U3TXDP_B

must to close to JUSB2

USB20_N0_L, USB20_P0_L, U3RXDN_B_R_1, U3RXDP_B_R_1, U3TXDN_B_R, U3TXDP_B_R

+USB30_VCCA W=60mils

JUSB2 OCTEK_USB-09EAEB CONN@

SSTX+, VBUS, SSTX-, D-, GND, D+, SSRX+, GND, SSRX-

+USB30_VCCA C766 150U_B2_6.3VM_R35M C1072 0.1U_0402_25V6

Place closely JUSB2.1

## USB2.0 Connector Co-lay with JUSB2 When USB30 not used

+USB30_VCCA JUSB8 OCTEK_USB-04APEB CONN@

USB20_N0_L, USB20_P0_L, GND

+3VALW R1019 0_0402_5% USB2_EN# [49]

R1020 100K_0402_5% USB20@ USB_PPON_A#

[45] USB_PPON_A → USB_PPON_A Q49 SSM3K7002FU_SC70-3 USB30@

+5VALW C713 1U_0603_10V6K

2.5A U46 RT9715BGS_SO8

GND, VIN, EN, VOUT, VOUT, FLG

USB_PPON_A# USB_OCI [17,45] USB_OCI

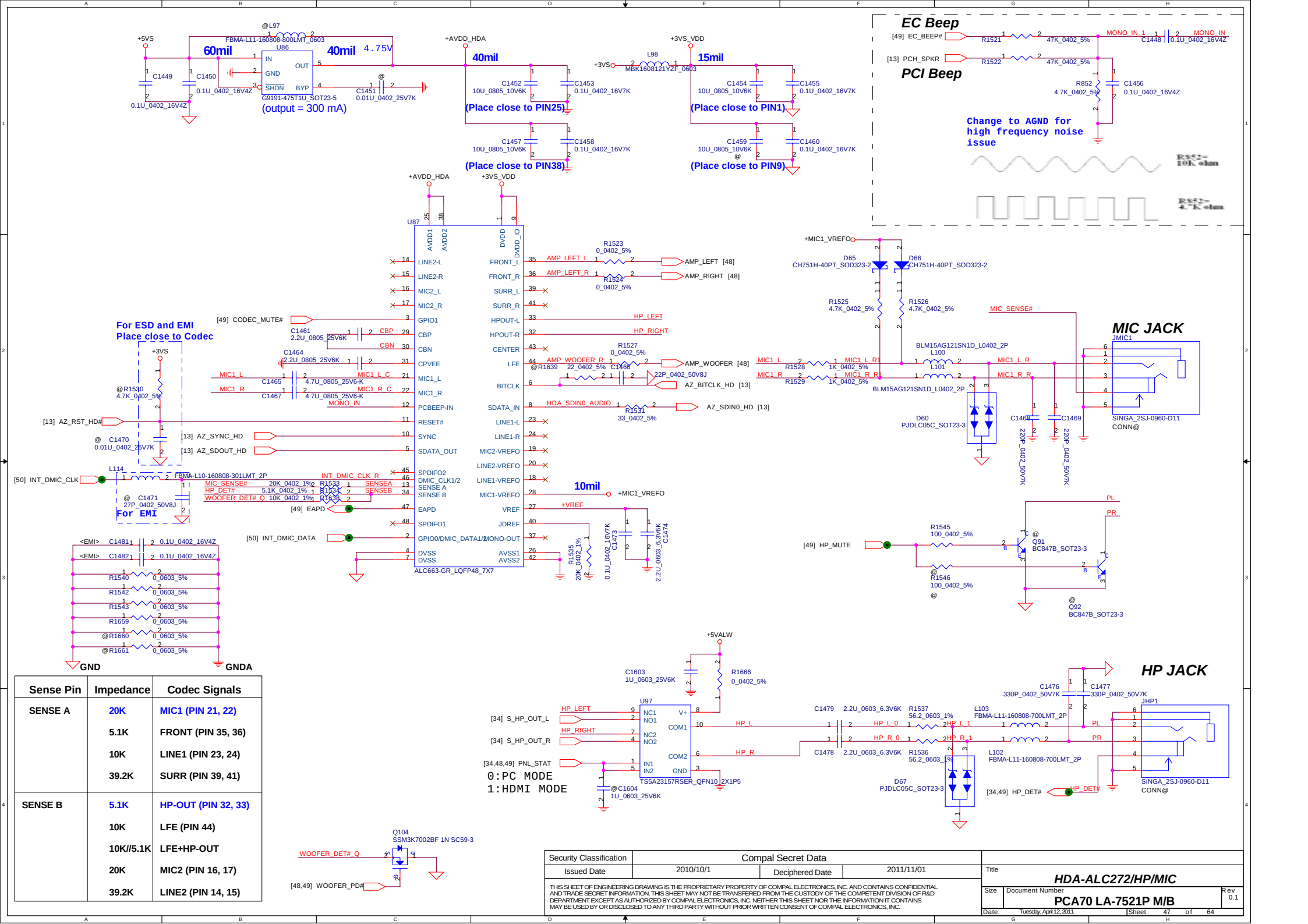
+USB30_VCCA W=60mils

C710 4.7U_0805_10V4Z C711 0.1U_0402_16V4Z C712 1000P_0402_50V7K

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |



| | | | |
|---|---|---|---|
| Title | USB3.0 CONN | | |
| Size | Document Number | PCA70 LA-7521P M/B | Rev 0.1 |
| Date: | Tuesday, April 12, 2011 | Sheet 46 of 64 | |




| Sense Pin | Impedance | Codec Signals |
|---|---|---|
| SENSE A | 20K | MIC1 (PIN 21, 22) |
| | 5.1K | FRONT (PIN 35, 36) |
| | 10K | LINE1 (PIN 23, 24) |
| | 39.2K | SURR (PIN 39, 41) |
| SENSE B | 5.1K | HP-OUT (PIN 32, 33) |
| | 10K | LFE (PIN 44) |
| | 10K//5.1K | LFE+HP-OUT |
| | 20K | MIC2 (PIN 16, 17) |
| | 39.2K | LINE2 (PIN 14, 15) |

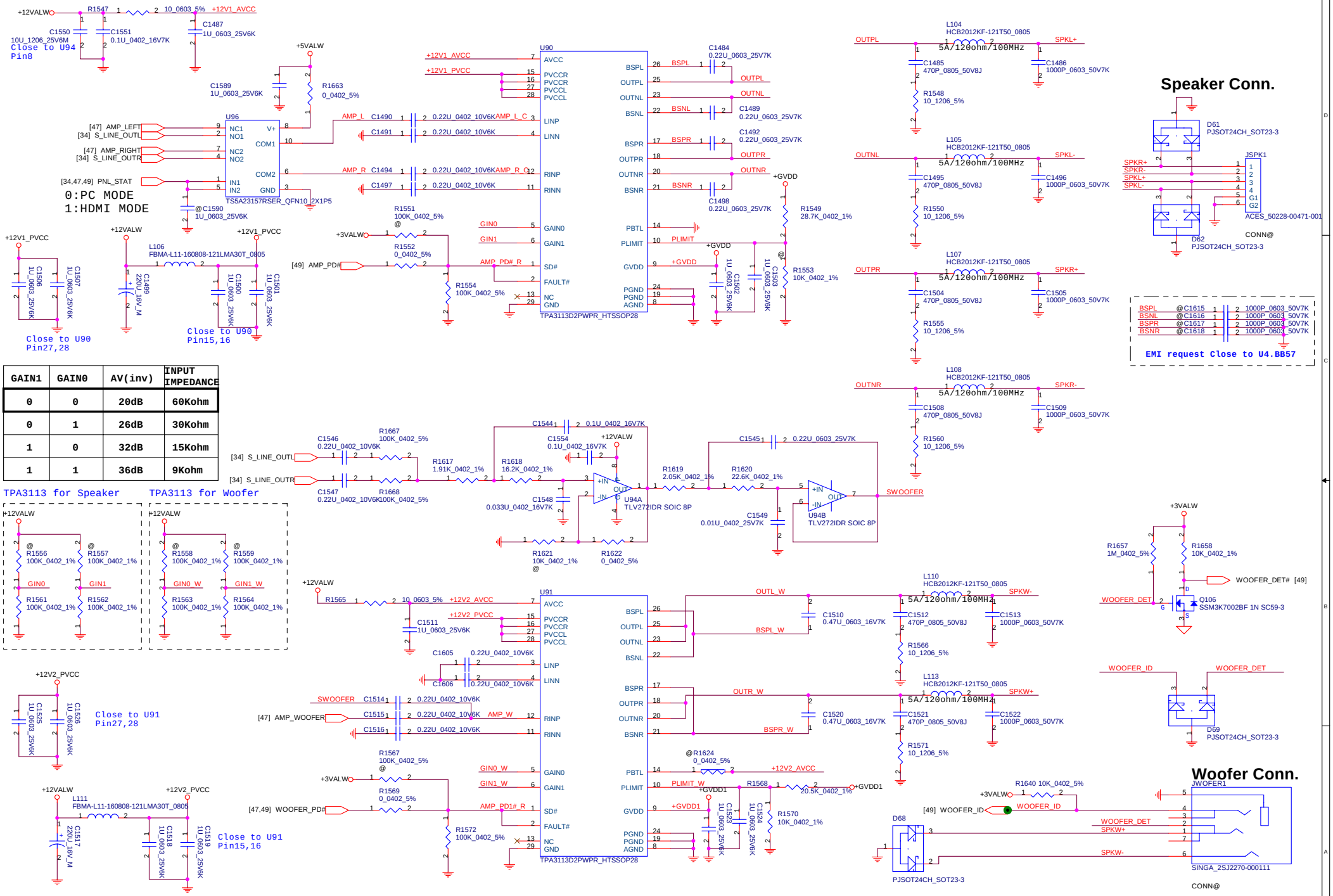
| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |



Title: HDA-ALC272/HP/MIC

Size | Document Number: PCA70 LA-7521P M/B | Rev: 0.1

Date: Tuesday, April 12, 2011 | Sheet 47 of 64

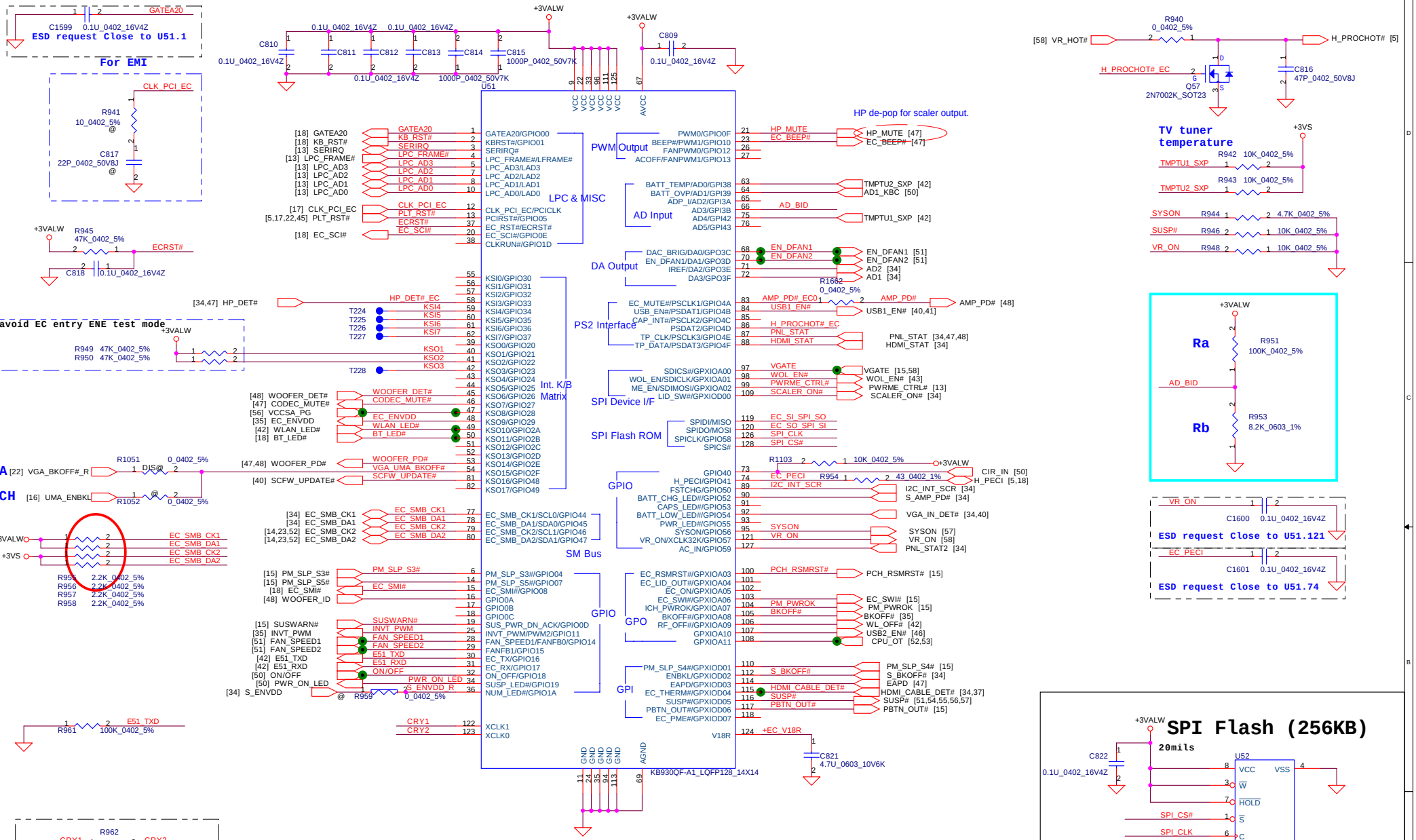



| GAIN1 | GAIN0 | AV(inv) | INPUT IMPEDANCE |
|---|---|---|---|
| 0 | 0 | 20dB | 60Kohm |
| 0 | 1 | 26dB | 30Kohm |
| 1 | 0 | 32dB | 15Kohm |
| 1 | 1 | 36dB | 9Kohm |

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/04/14 | Deciphered Date | 2011/04/14 |



| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: AMP & Audio Jack | | | |
| Size: Custom | Document Number: PCA70 LA-7521P M/B | | Rev: 1.0 |
| Date: Tuesday, April 12, 2011 | | Sheet 48 of 64 | |




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |



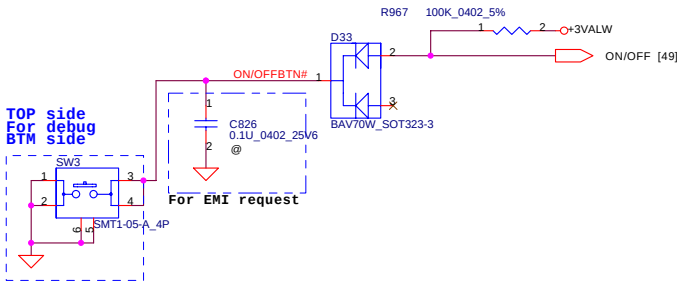
**Compal Electronics, Inc.**

Title: **LPC-EC-KB930**

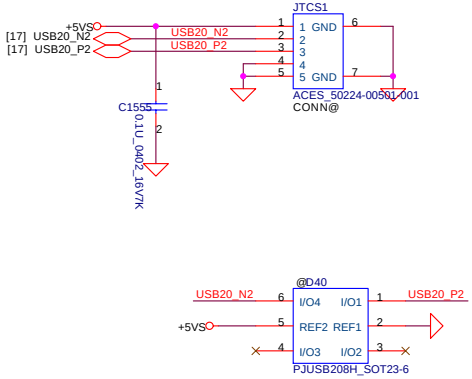
Size: | Document Number: **PCA70 LA-7521P M/B** | Rev: 0.1

Date: Tuesday, April 12, 2011 | Sheet 49 of 64

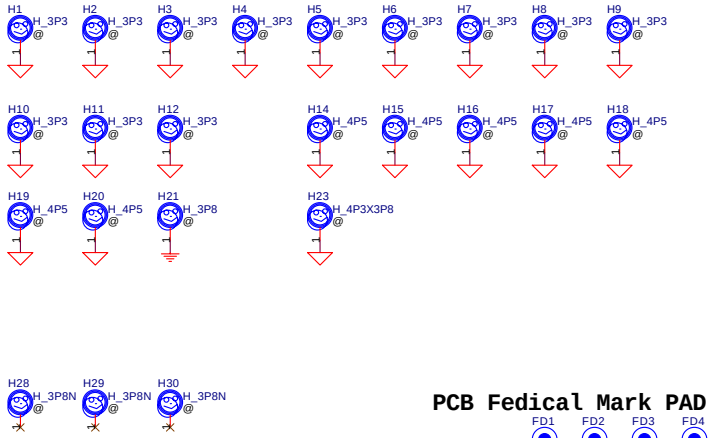
# Power Button



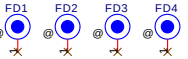

# Touchscreen



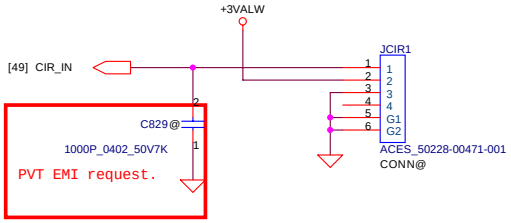

# Screw Hole



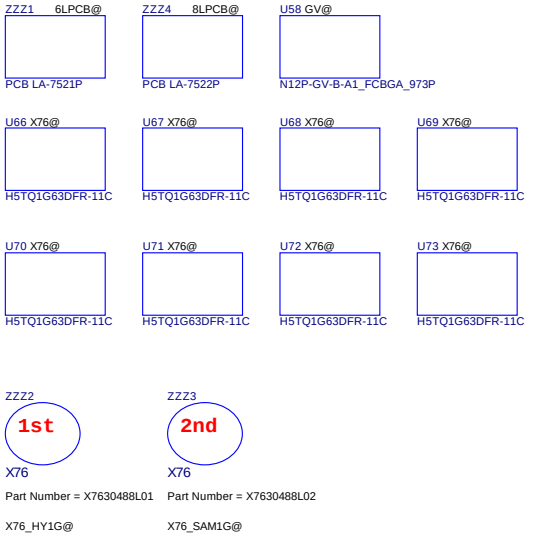

## PCB Fedical Mark PAD



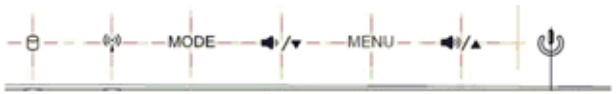

# CIR

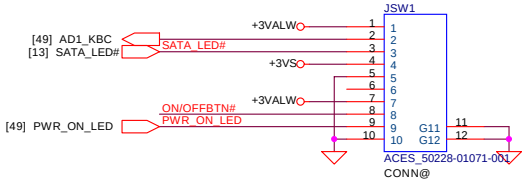


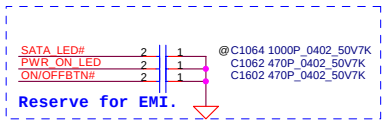

# ISPD



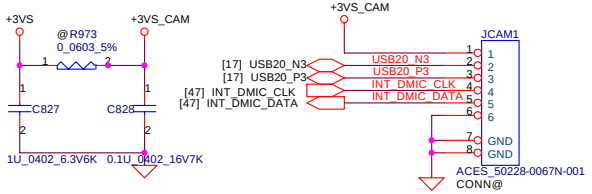

# CAP Button/B Connector

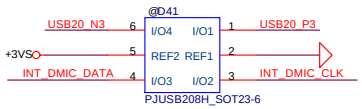



# CAM




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |



Title: PWR/Cap./TP/LED/LP/LS/Screw

Size | Document Number: PCA70 LA-7521P M/B | Rev: 0.1

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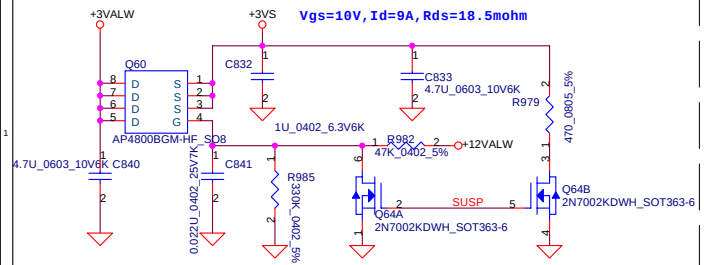
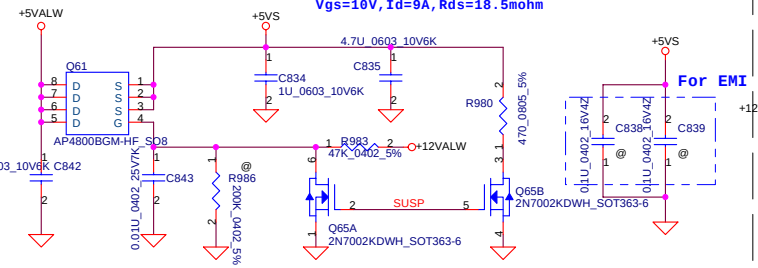
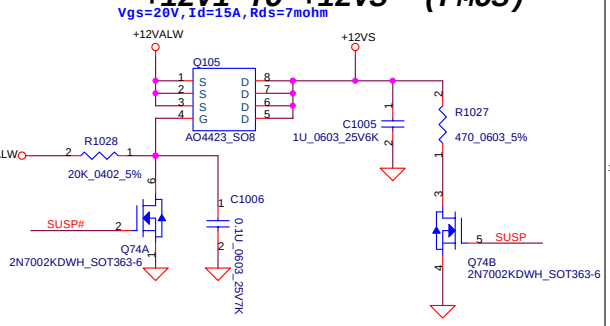
## +3VALW TO +3VS



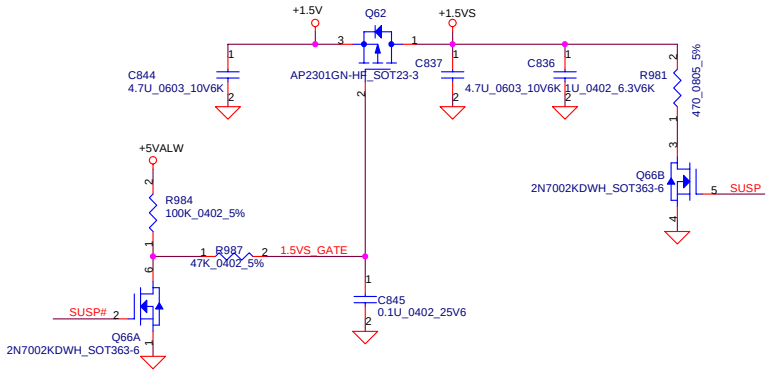

## +5VALW TO +5VS



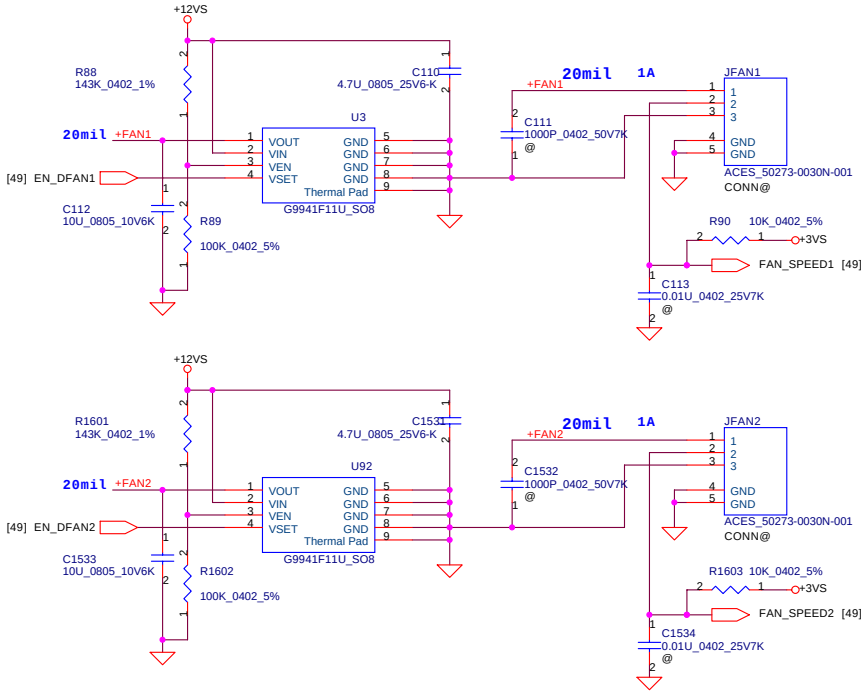

## +12V1 TO +12VS (PMOS)



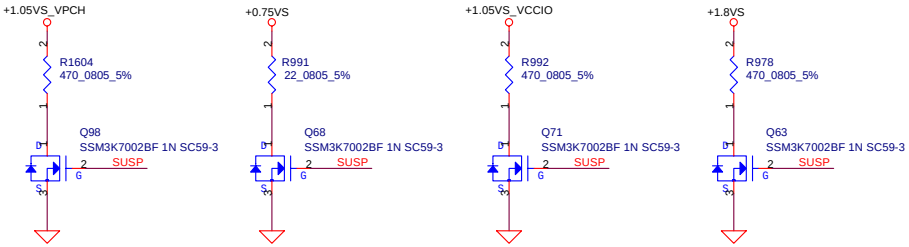

## +1.5V to +1.5VS

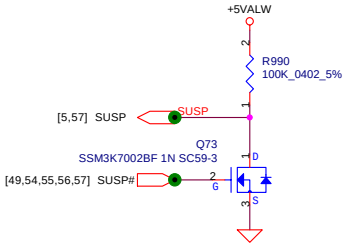



## FAN Control Circuit




## Discharge circuit

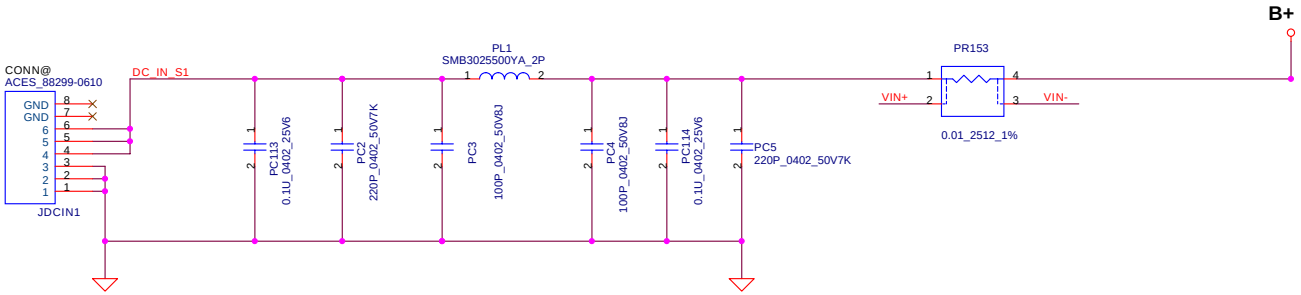


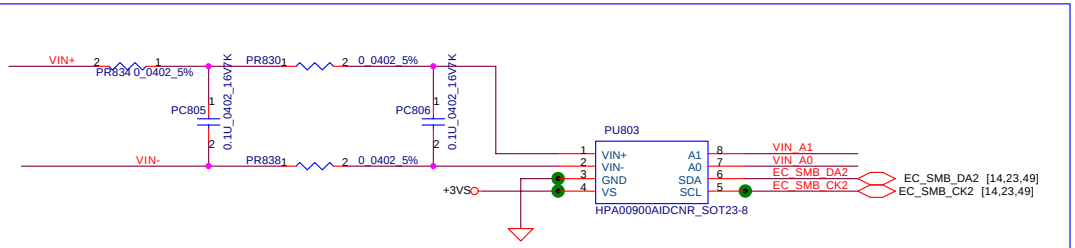



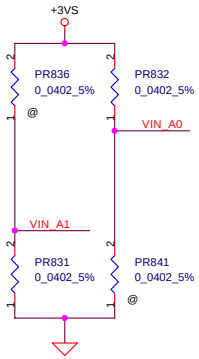

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |



| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title | DC-DC INTERFACE | | |
| Size | Document Number | PCA70 LA-7521P M/B | Rev 0.1 |
| Date: Tuesday, April 12, 2011 | Sheet 51 of 64 | | |

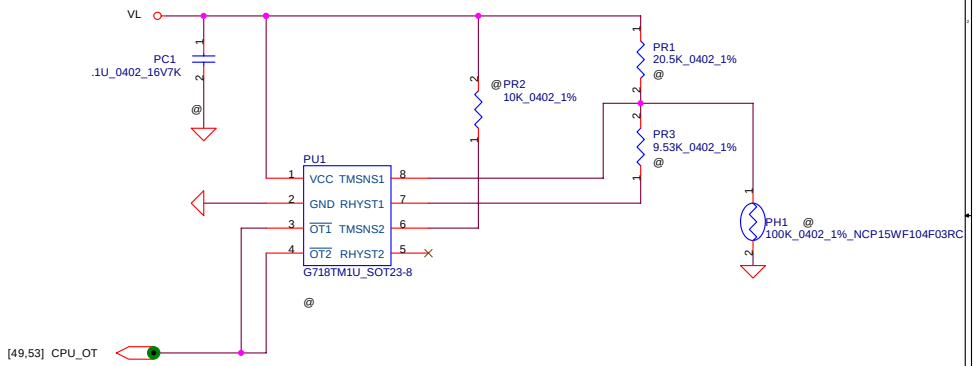


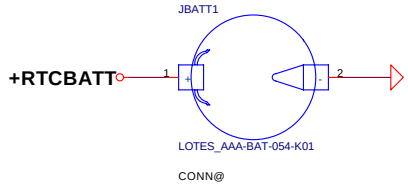




## Current sense solution 2

Ventura for CPU side
slave address : 1000001
please placemnet near R-sense




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |

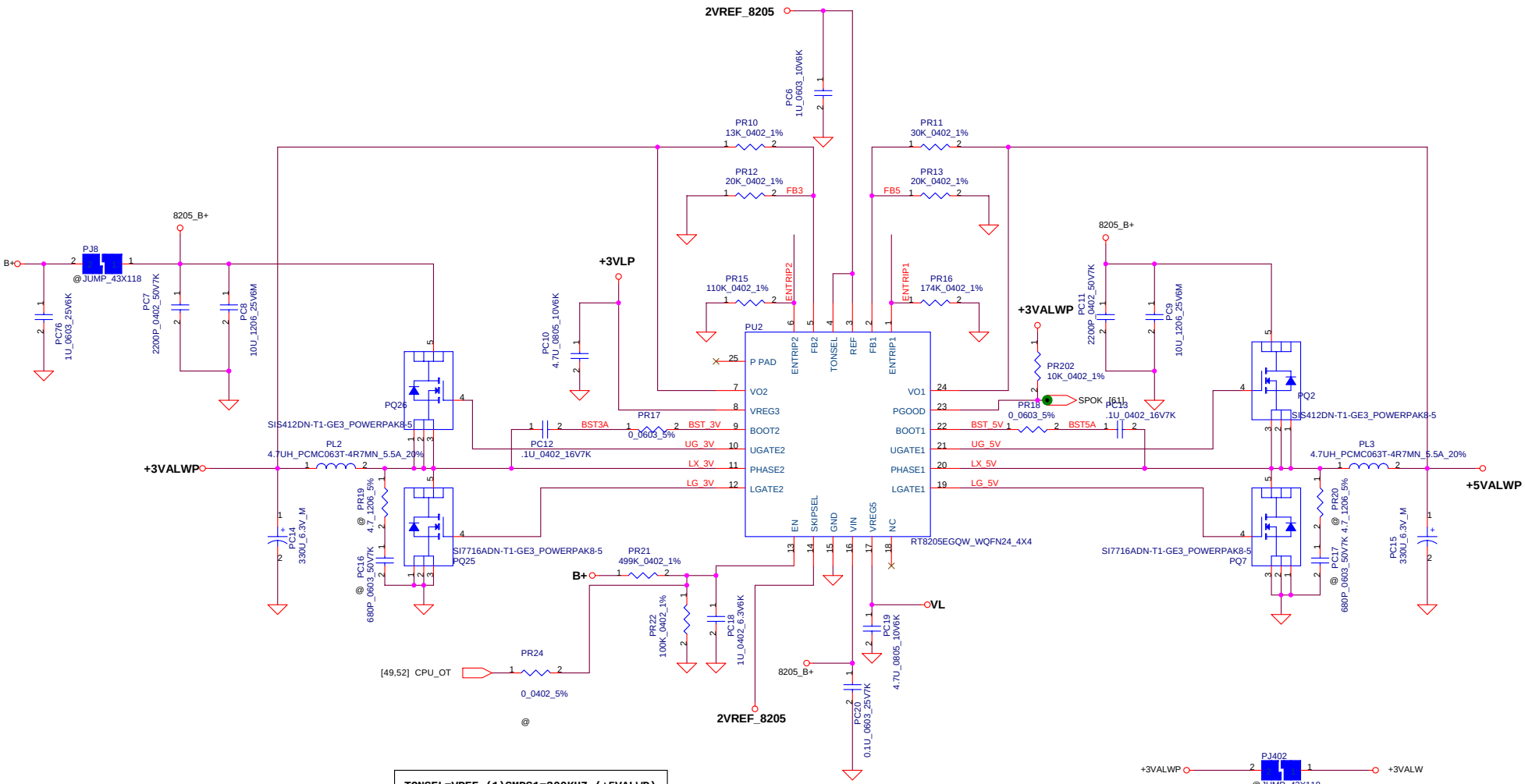


**Compal Electronics, Inc.**

Title: **P51_PWR_DC-IN**

Size | Document Number: **PCA70 LA-7521P M/B** | Rev: 0.1

Date: Tuesday, April 12, 2011 | Sheet 52 of 64




**TONSEL=VREF (1)SMPS1=300KHZ (+5VALWP)**
**(2)SMPS2=375KHZ(+3VALWP)**

**+3.3VALWP**
**Ipeak=5.71A ; 1.2Ipeak=6.852A; Imax=3.997A**
**f=375KHz, L=4.7UH**
**Rdson=15~18m ohm**
**1/2Delta I = 1/2 *(19-3.3)*(3.3/19)/(375KHz*4.7UH)=0.773A**
**Vlimit=10*10^-6*110Kohm/10=0.11V**
**Ilimit=0.11/(18m*1.2)~0.11/(15m)=6.34A~9.13A**
**Iocp=7.113A~10.073A (7.113A>6.852A -> ok) -DVT-**

**+5VALWP**
**Ipeak=7.376A ; 1.2Ipeak=8.85A; Imax=5.16A**
**f=300KHz, L=4.7UH,Rentrip=174k ohm**
**Rdson=15~18m ohm**
**1/2Delta I = 1/2 *(19-5)*(5/19)/(300KHz*4.7UH)=1.306A**
**Vlimit=10*(10^-6)*174Kohm/10=0.174V**
**Ilimit=0.174/(18m*1.2)~0.174/(15m)=8.055~11.6A**
**Iocp=9.361~12.906A (9.361>8.85 -> OK)**

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |

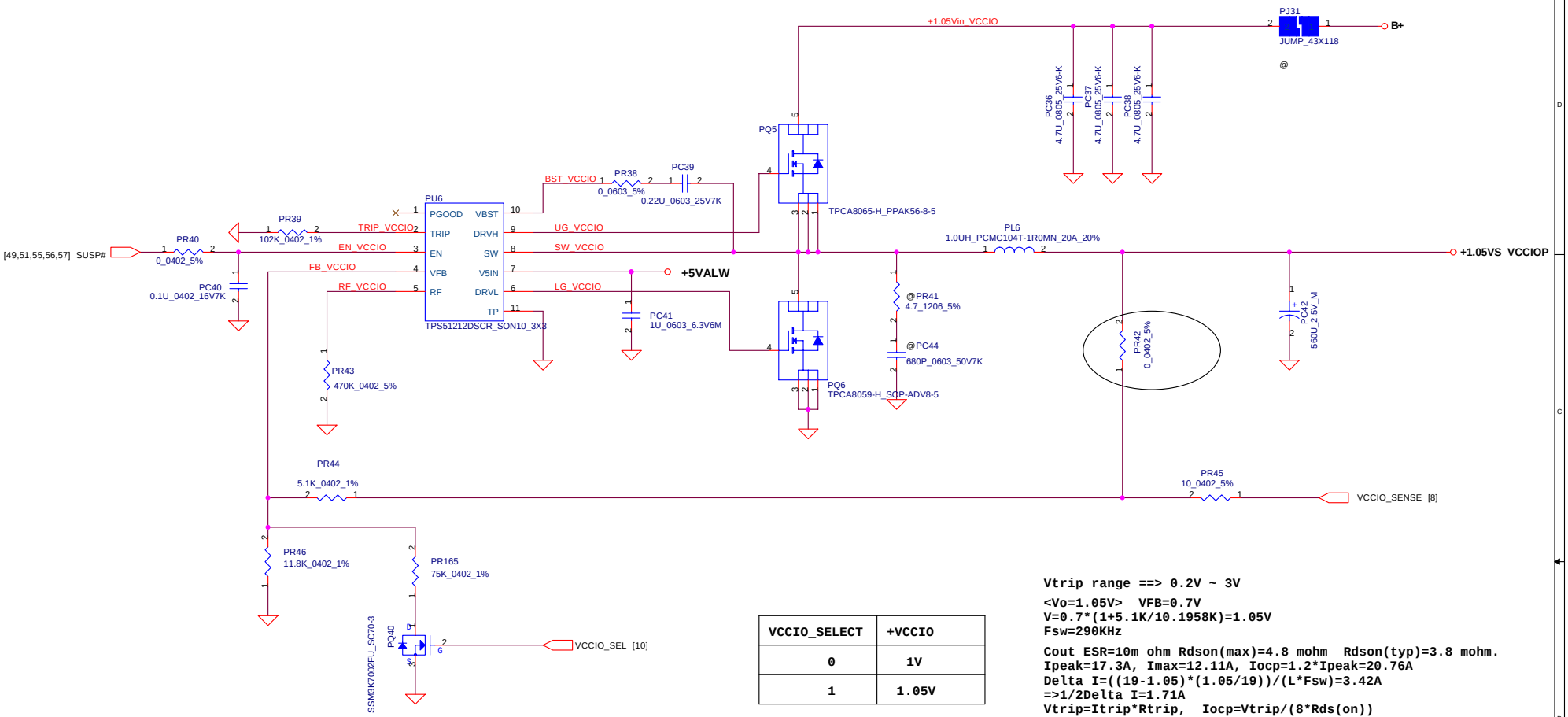


**Compal Electronics, Inc.**

Title: **P52-PWR-+3VALW/+5VALW**

| Size | Document Number | Rev |
|---|---|---|
| | PCA70 LA-7521P M/B | 0.1 |

Date: Tuesday, April 12, 2011 | Sheet 53 of 64



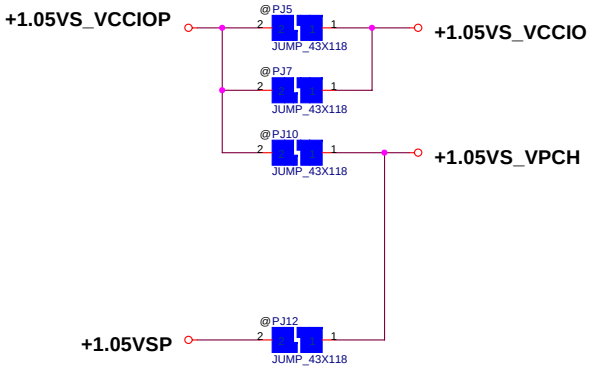

| VCCIO_SELECT | +VCCIO |
|---|---|
| 0 | 1V |
| 1 | 1.05V |

**Vtrip range ==> 0.2V ~ 3V**

**<Vo=1.05V>  VFB=0.7V**
**V=0.7*(1+5.1K/10.1958K)=1.05V**
**Fsw=290KHz**

**Cout ESR=10m ohm Rdson(max)=4.8 mohm  Rdson(typ)=3.8 mohm.**
**Ipeak=17.3A, Imax=12.11A, Iocp=1.2*Ipeak=20.76A**
**Delta I=((19-1.05)*(1.05/19))/(L*Fsw)=3.42A**
**=>1/2Delta I=1.71A**
**Vtrip=Itrip*Rtrip,  Iocp=Vtrip/(8*Rds(on))**
**Iocpmax=((102K*11uA)/(8*0.0038))+1.71A=38.617A**
**Iocpmin=((102K*9uA)/(8*0.0048))+1.71A=25.616A**
**Iocp=25.616A~38.617A**

(17A,680mils ,Via NO.=34)




**<Vo=1.0V>  VFB=0.7V**
**V=0.7*(1+5.1K/11.8K)=1.0V**
**Fsw=290KHz**

**Cout ESR=10m ohm Rdson(max)=4.8 mohm  Rdson(typ)=3.8 mohm.**
**Ipeak=17.3A, Imax=12.11A, Iocp=1.2*Ipeak=20.76A**
**Delta I=((19-1.0)*(1.0/19))/(L*Fsw)=3.266A**
**=>1/2Delta I=1.633A**
**Vtrip=Itrip*Rtrip,  Iocp=Vtrip/(8*Rds(on))**
**Iocpmax=((102K*11uA)/(8*0.0038))+1.633A=38.54A**
**Iocpmin=((102K*9uA)/(8*0.0048))+1.633A=25.539A**
**Iocp=25.539A~38.54A**

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2009/11/13 | Deciphered Date | 2009/04/28 |



Compal Electronics, Inc.

Title: *+1.05VSP*

| Size | Document Number | Rev |
|---|---|---|
| | PCA60/70 LA-7001P M/B | 0.1 |

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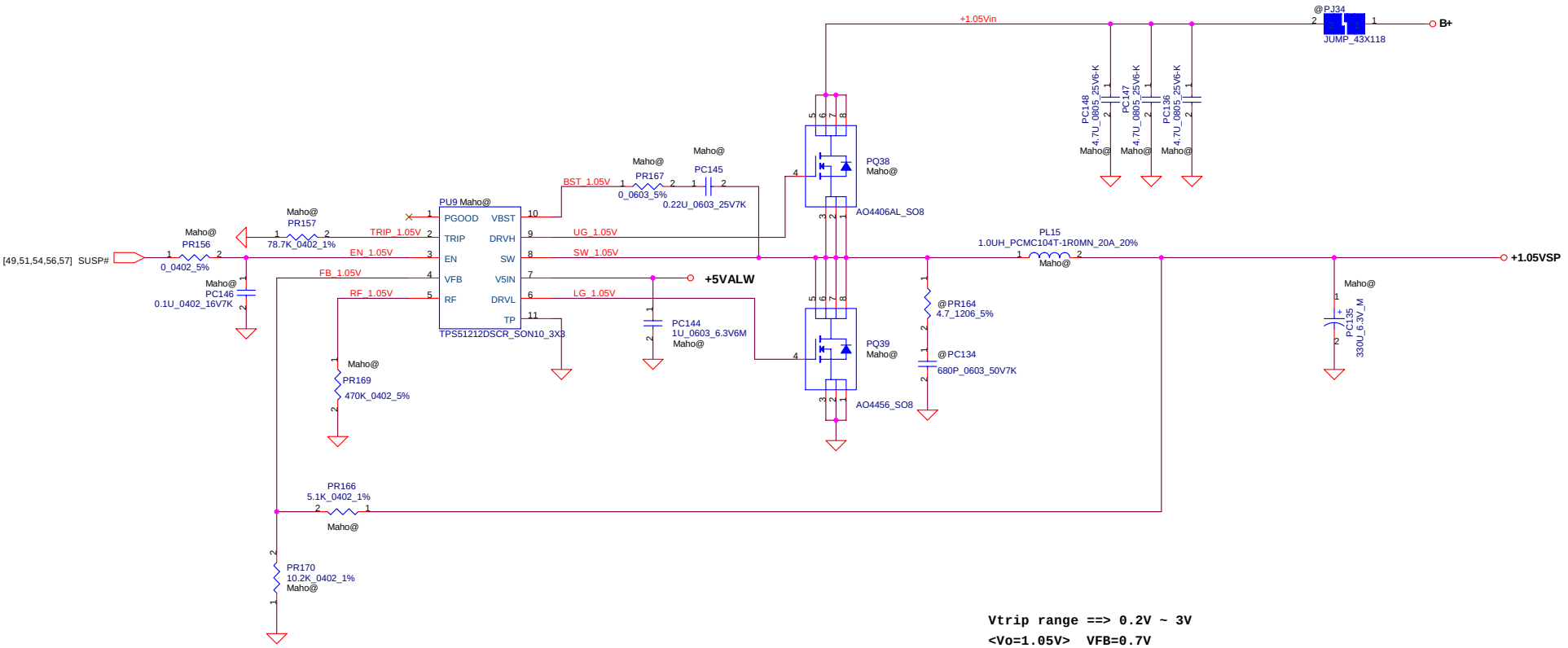


**Vtrip range ==> 0.2V ~ 3V**

**<Vo=1.05V> VFB=0.7V**
**V=0.7*(1+5.1K/10.2K)=1.05V**
**Fsw=290KHz**

**Cout ESR=10m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.**
**Ipeak=7.3A, Imax=5.11A, Iocp=1.2*Ipeak=8.76A**
**Delta I=((19-1.05)*(1.05/19))/(L*Fsw)=3.42A**
**=>1/2Delta I=1.71A**
**Vtrip=Itrip*Rtrip, Iocp=Vtrip/(8*Rds(on))**
**Iocpmax=((78.7K*11uA)/(8*0.0045))+1.71A=25.75A**
**Iocpmin=((78.7K*9uA)/(8*0.0056*1.3))+1.71A=13.871A**
**Iocp=13.871A~25.75A**

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |



**Compal Electronics, Inc.**

Title: ***P54_PWR-+1.05VSP***

| Size | Document Number | Rev |
|---|---|---|
| | **PCA70 LA-7521P M/B** | 0.1 |

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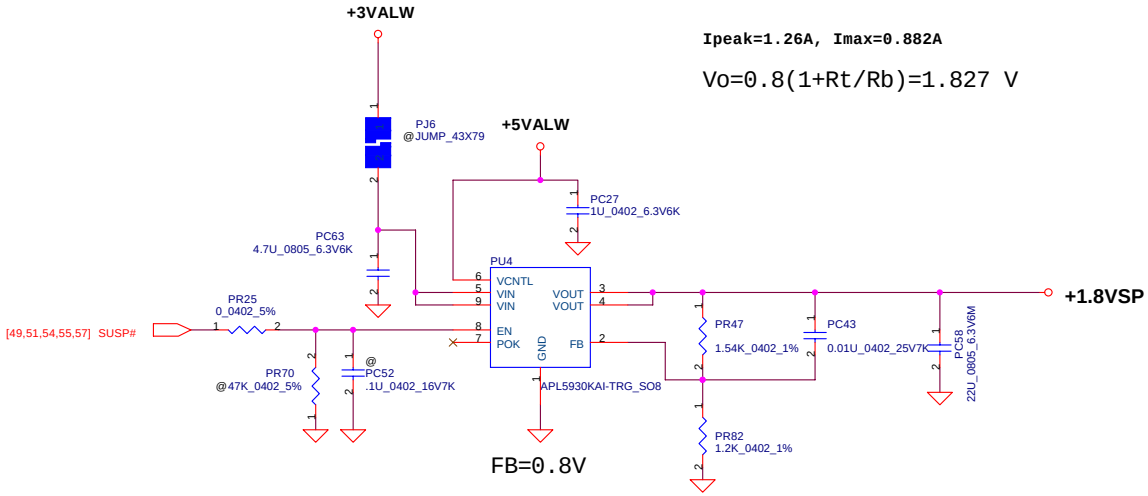
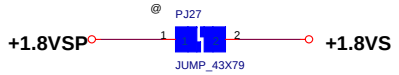
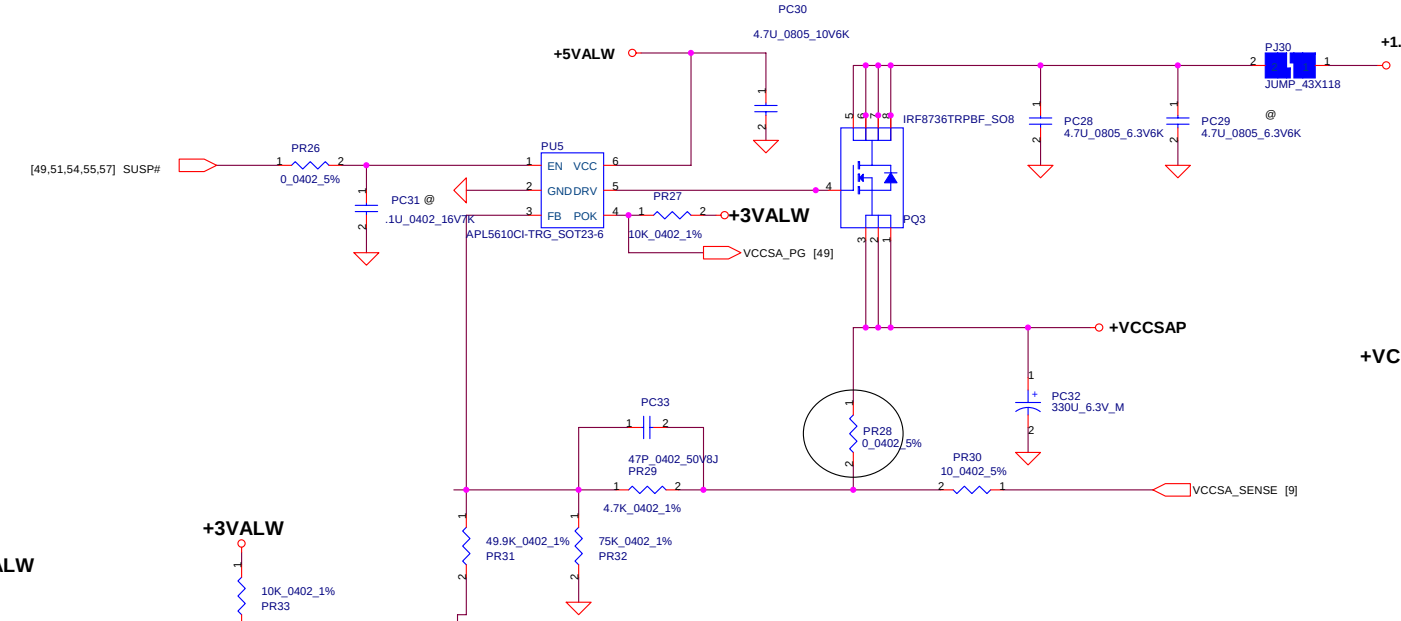



3.3A,140mils ,Via NO.= 7

Ipeak=8.8A
Imax=6.2A
Toatal Capacitor ??u
ESR=15mohm
Vout=0.8(1+Rt/Rb)





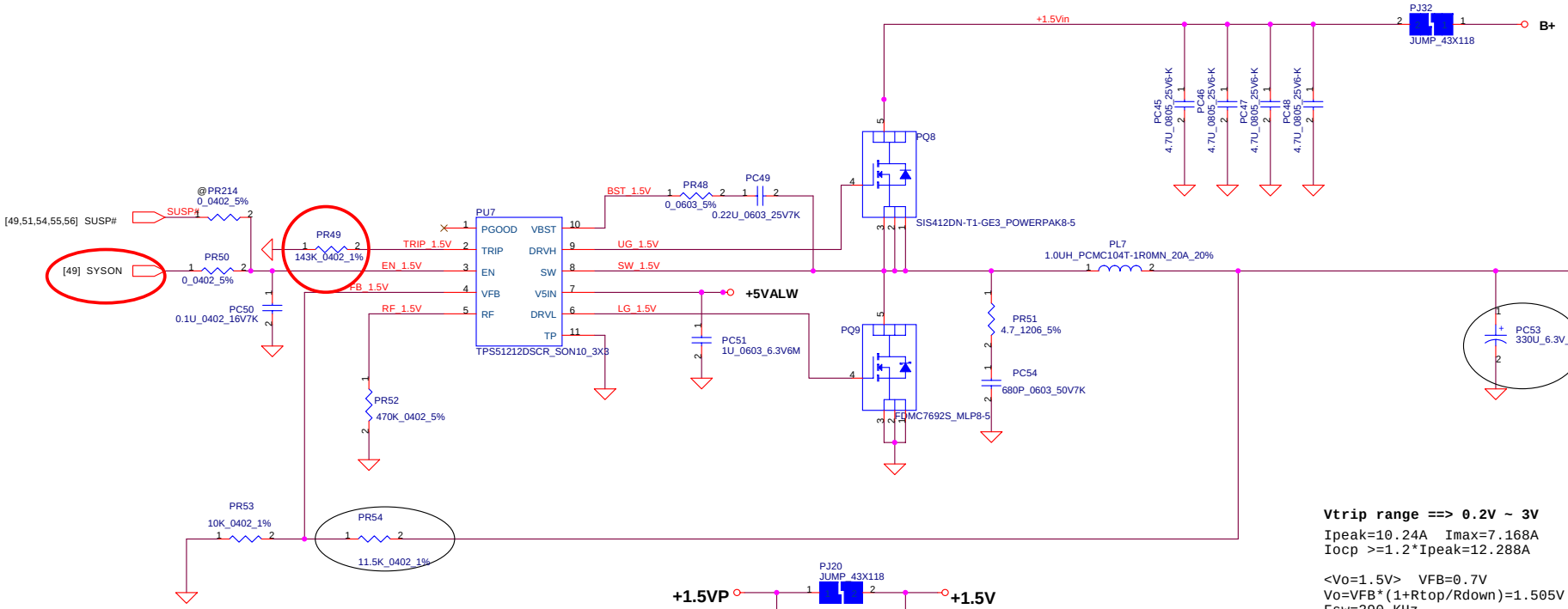
(6A,240mils ,Via NO.= 12)

| VCCSA_VID | +VCCSAP |
|---|---|
| 0 | 0.925V |
| 1 | 0.85V |

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/01/25 | Deciphered Date | 2009/04/28 |



| | | | |
|---|---|---|---|
| Title | +VCCSA/+1.8VSP | | |
| Size Custom | Document Number PCA60/70 LA-7001P M/B | | Rev 0.1 |
| Date: Tuesday, April 12, 2011 | Sheet 56 of 64 | | |

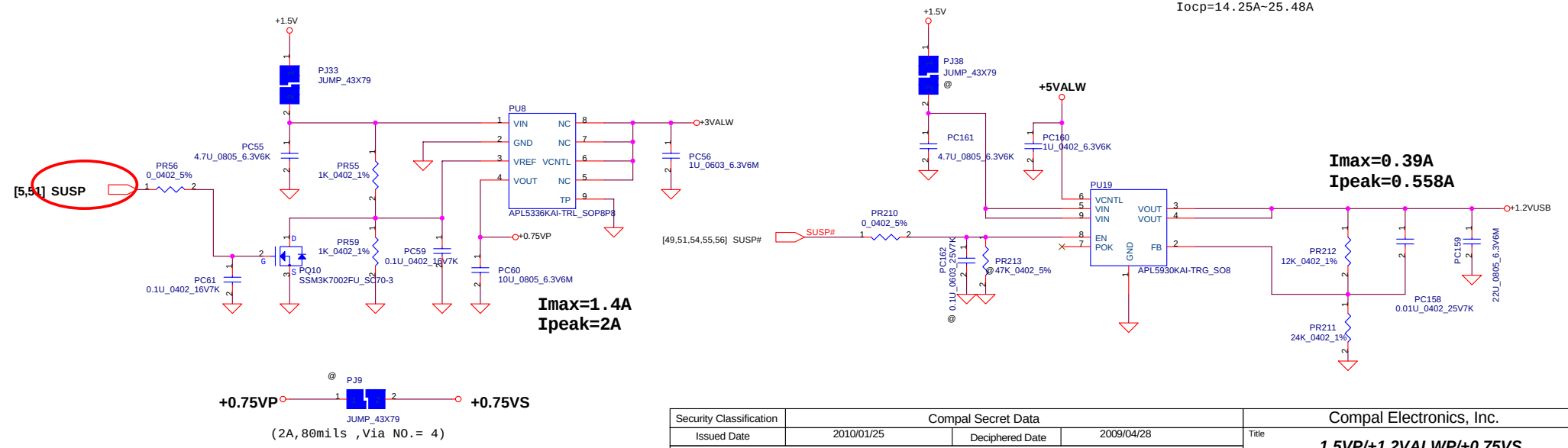



**Vtrip range ==> 0.2V ~ 3V**

```
Ipeak=10.24A  Imax=7.168A
Iocp >=1.2*Ipeak=12.288A

<Vo=1.5V>  VFB=0.7V
Vo=VFB*(1+Rtop/Rdown)=1.505V
Fsw=290 KHz
Cout ESR=15m ohm Rdson(max)=5.6m ohm, Rdson(typ)=4.5 mohm

Delta I=((19-1.5)*(1.5/19))/(1u*290 K)=4.764 A
=>1/2DeltaI=2.382A
Vtrip=Itrip*Rtrip,  Iocp=Vtrip/(8*Rds(on))
Iocpmax=((76.8K*11uA)/(8*0.0045))+2.382A=25.848A
 Iocpmin=((76.8K*9uA)/(8*0.0056*1.3))+2.382A=14.25A
Iocp=14.25A~25.48A
```




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/01/25 | Deciphered Date | 2009/04/28 |



Compal Electronics, Inc.

Title: *1.5VP/+1.2VALWP/+0.75VS*

| Size | Document Number | Rev |
|---|---|---|
| Custom | PCA60/70 LA-7001P M/B | 0.1 |

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CPU CORE OCP: 90A-----65W
136A----95W

65W CPU IMAX=75A

95W CPU IMAX=112A

Iout_MAX=35A

GFX OCP:42A

ESD request Close to PU10.9

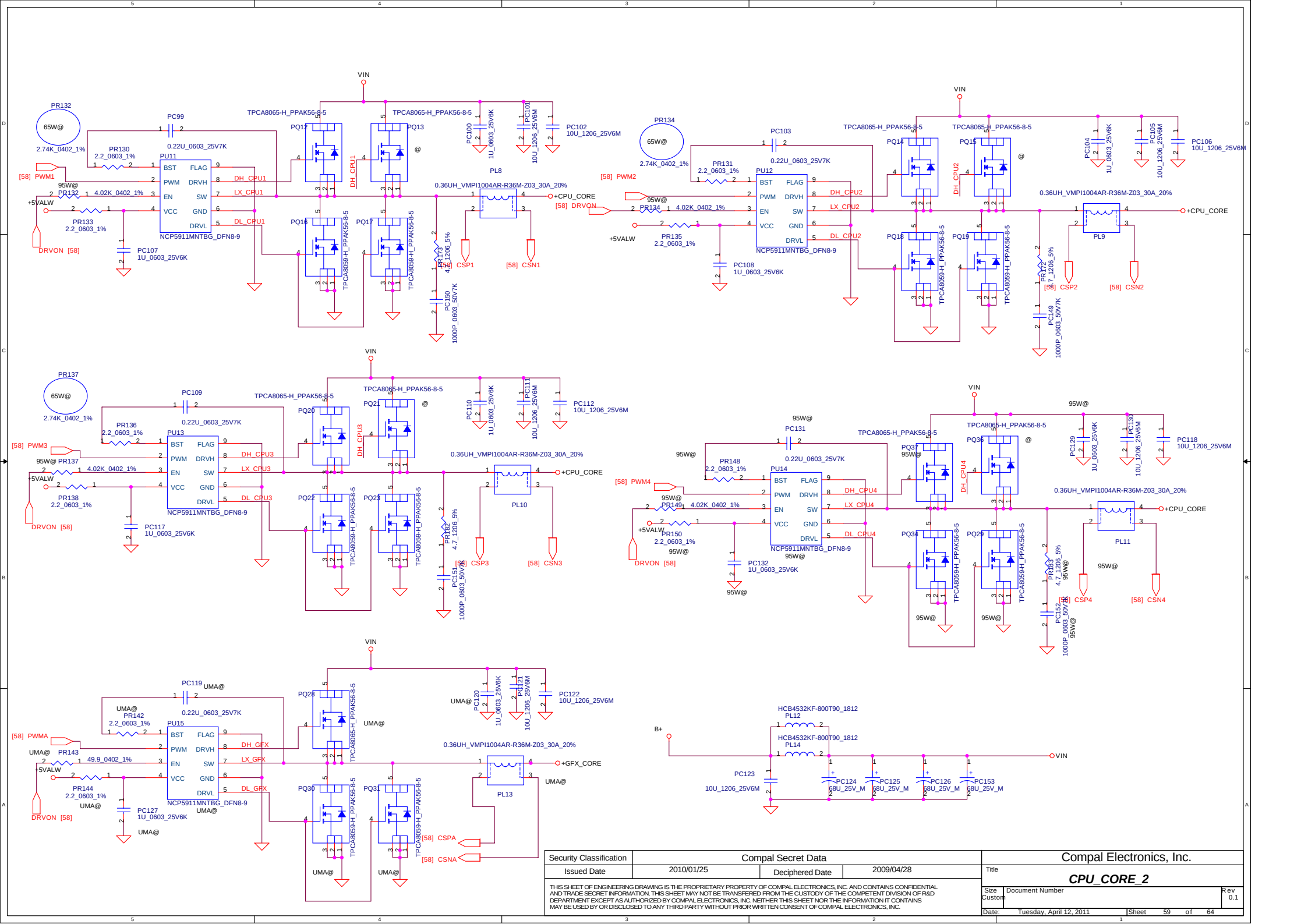
| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
| Issued Date | 2010/01/25 | Deciphered Date | 2009/04/28 |



Title: *CPU_CORE_1*

Size: C | Document Number: PCA60/70 LA-7001P M/B | Rev: 0.1

Date: Tuesday, April 12, 2011 | Sheet 58 of 64




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/01/25 | Deciphered Date | 2009/04/28 |

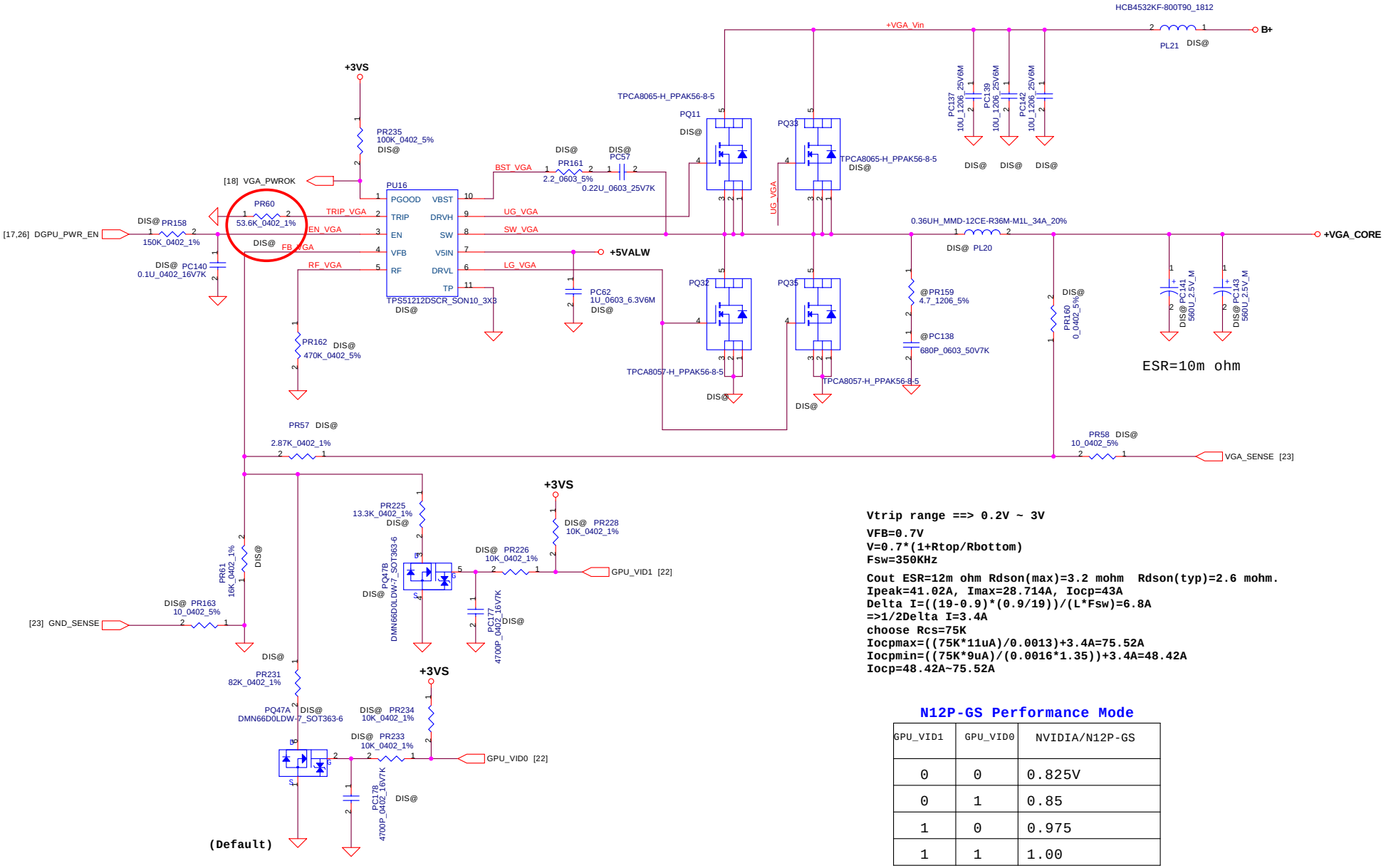


Compal Electronics, Inc.

Title: **CPU_CORE_2**

| Size | Document Number | Rev |
|---|---|---|
| Custom | | 0.1 |

Date: Tuesday, April 12, 2011 | Sheet 59 of 64




**Vtrip range ==> 0.2V ~ 3V**

**VFB=0.7V**
**V=0.7*(1+Rtop/Rbottom)**
**Fsw=350KHz**

**Cout ESR=12m ohm Rdson(max)=3.2 mohm  Rdson(typ)=2.6 mohm.**
**Ipeak=41.02A, Imax=28.714A, Iocp=43A**
**Delta I=((19-0.9)*(0.9/19))/(L*Fsw)=6.8A**
**=>1/2Delta I=3.4A**
**choose Rcs=75K**
**Iocpmax=((75K*11uA)/0.0013)+3.4A=75.52A**
**Iocpmin=((75K*9uA)/(0.0016*1.35))+3.4A=48.42A**
**Iocp=48.42A~75.52A**

## N12P-GS Performance Mode

| GPU_VID1 | GPU_VID0 | NVIDIA/N12P-GS |
|---|---|---|
| 0 | 0 | 0.825V |
| 0 | 1 | 0.85 |
| 1 | 0 | 0.975 |
| 1 | 1 | 1.00 |

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/01/25 | Deciphered Date | 2009/04/28 |

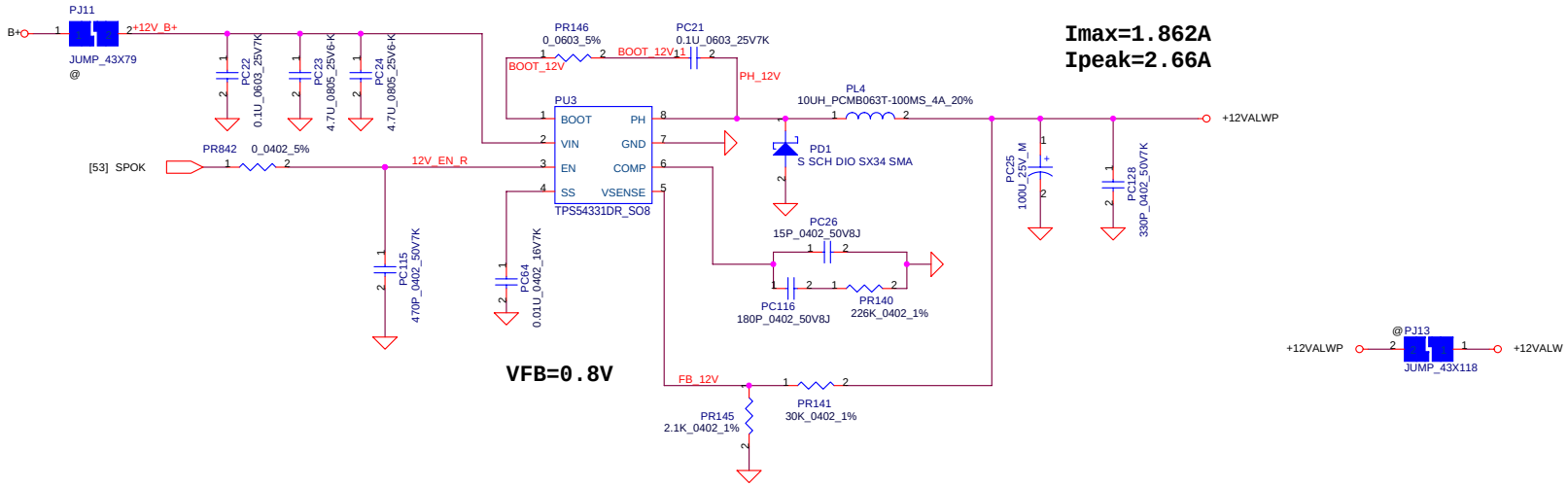


Compal Electronics, Inc.

Title: ***VGA_CORE***

| Size | Document Number | Rev |
|---|---|---|
| Custom | PCA60/70 LA-7001P M/B | 0.1 |

Date: Tuesday, April 12, 2011 Sheet 60 of 64




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |



**Compal Electronics, Inc.**

Title: ***P60_PWR-+12V***

| Size | Document Number | Rev |
|---|---|---|
| | PCA70 LA-7521P M/B | 0.1 |

Date: Tuesday, April 12, 2011 | Sheet 61 of 64

| NO | DATE | PAGE | MODIFICATION LIST | PURPOSE |
|---|---|---|---|---|
| 1 | 2010/09/30 | P48~49 | Change PR39 to 118k ohm<br>Change PR49 to 95.3k ohm | Modify OCP setting value |
| 2 | 2010/10/01 | P48 | Remove reserved 1.05VP power rail | Because VCCIO will not be changeable voltage on Sandy Bridge platform. We don't need another 1.05V for PCH |
| 3 | 2010/10/28 | P50 | PC124,PC125 change to 220u_25V<br>Remove PC126 | Modify for input cap |
| 4 | 2010/10/28 | P49 | Remove PR70, PR82, PR84, PR171, PR172, PR173, PR174, PC76 | Remove forth phase related components |
| 5 | 2010/10/28 | P49 | PR62, PR65, PR66 change to 90.9K_0603_1%<br>PC72 change to 1500P_0402_50V | Change for correct droop setting |
| 6 | 2010/10/28 | P49 | PR129 change to 39.2K_0603_1%<br>PR117 change to 25.5k_0402_1%<br>PC92 change to 220P_0402_50V | Change for correct GT droop setting |
| 7 | 2011/01/27 | P58 | update Net name "IMAX " | update after vender review layout |
| 8 | 2011/01/27 | P61 | change PC25 part number to SF000004S00 | material shoretage |
| 9 | 2011/01/27 | P59 | change PC124/125/126/153 part number from SF000004L00 to SF000004M00 | material shoretage |
| 10 | 2011/02/09 | P52 | add "@" at BOM structure of PR836 and PR841 | change for EC |
| 11 | 2011/02/16 | P53 | change PU2 part number to SA00004NY00 | change for part EOL |
| 12 | 2011/03/07 | P60 | change PR60 from 75Kohm to 53.6Kohm | change for OCP setting point |
| | 2011/03/07 | P57 | change PR49 from 76.8Kohm to 143Kohm | change for OCP setting point |
| 13 | 2011/03/25 | P60 | change BOM structure PQ11 from @ to DIS@ | for Thermal team concern |
| 14 | 2011/03/30 | P60 | Remove VGA_core Jump for impedence concern | |
| 15 | 2011/03/30 | P52 | change PR153 from 15m ohm to 10m ohm for Inrush concern | |
| 16 | 2011/03/30 | P59 | change PC124/125/126/153 part number from SF000004M00 to SF000004T00 | |
| 17 | 2011/03/30 | | change PC101/102/105/106/111/112/118/121/122/123/130/137/139/142 part number from SE142106K80 to SE142106M80 | |
| 18 | 2011/04/06 | P52 | Remove JDCIN1 pin.7 and pin.8 from GND | Layout modification |
| 19 | 2011/04/08 | P58 | add PC807 at PU10.9 for ESD request<br>change PR68=5.49Kohm, PC67=1nF, PR62=PR65=PR66=PR152=95.3Kohm, PC65=470pF, PC69=10pF, PC66=220pF, PR80=1.5kohm, PR79=2.8kohm, PR129=39.2Kohm, PC88=2.2nF, PC97=680pF, PC90=10pF, PC95=220pF, PR116=1.24kohm, PR109=887ohm, PC92=820pF | |
| 20 | 2011/04/08 | P60 | change PC141/PC143 part number to SF000002P00 | |

# HW PIR (Product Improve Record)

**NWQAA LA-6062P SCHEMATIC CHANGE LIST**
**REVISION CHANGE: 0.1 TO 0.2**
**GERBER-OUT DATE: 2009/12/30**

| NO | DATE | PAGE | MODIFICATION LIST | PURPOSE |
|---|---|---|---|---|

| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2010/10/1 | Deciphered Date | 2011/11/01 |



Compal Electronics, Inc.

Title: ***HW-PIR***

Size | Document Number: **PCA70 LA-7521P M/B** | Rev: 0.1

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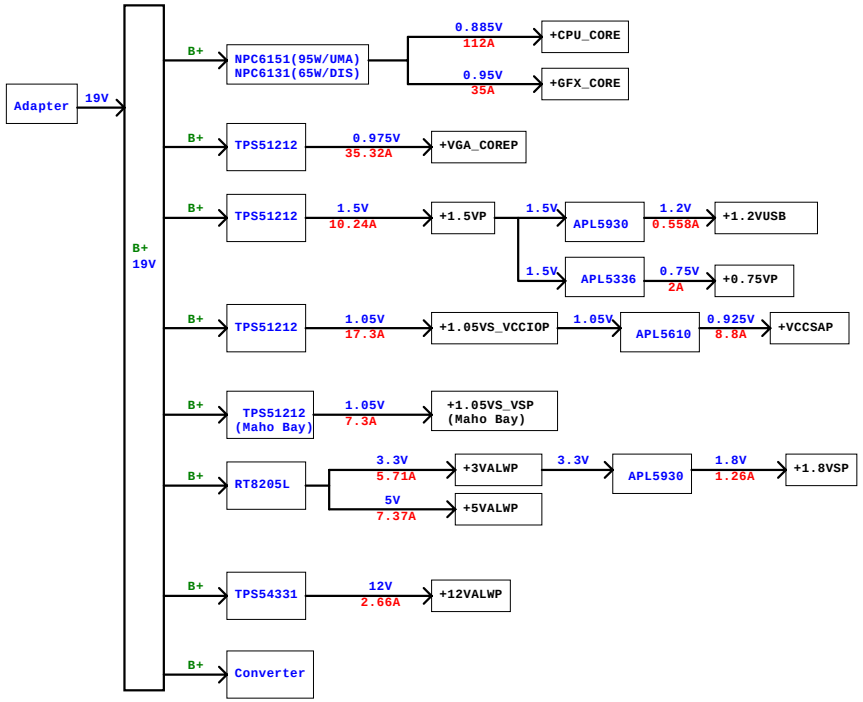


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| Security Classification | Compal Secret Data | | |
| Issued Date | 2010/10/28 | Deciphered Date | 2011/11/01 |



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Title: ***Power Rail***

| Size | Document Number | Rev |
|---|---|---|
| | | 0.1 |

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