Compal Confidential

QIWY4 M/B Schematics Document

Intel IVY Bridge Processor with DDRIII + Panther Point PCH
nVIDIA N13X

2011-12-23

REV:1.0

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File Name : Y580

Chief River

nVIDIA N13E-GE
VRAM 64*32
GDDR5*8

PCI-E X16
Gen 1/2/3

Intel
IVY Bridge
Processor
Socket-rPGA989
37.5mm*37.5mm

Dual Channel
DDR3-1333(1.5V)
DDR3-1600(1.5V)

DDR3-SO-DIMM X2
BANK 0, 1, 2, 3
UP TO 16G

HDMI CONN
HDMI1.4a

CRT Connector
optimus 2012

LVDS Connector
optimus 2012

FDI *8
100MHz
2.7GT/s

DMI2 *4
100MHz
5GT/s

Intel
Panther Point
PCH
FCBGA 989 Balls
25mm*25mm

6*SATA
(port0,1 Support SATA3)
SATA3.0 HDD CONN
SATA3.0 HDD (SSD)
SATA ODD CONN

4*USB3.0

14*USB2.0
BlueTooth CONN
CMOS Camera
USB PORT 3.0 x2(Left)
WLAN/WiMAX
USB PORT 2.0 x1(Right)
TV
USB PORT 3.0 x1 (Right)
with USB charger
Audio Board

HD Audio

PCI Express
Mini card Slot 1
WLAN/WiMAX
USB(WiMAX)
PCI-E(WLAN)

PCI Express
Mini card Slot 2
SSD
SATA(SSD)

PCI Express
Mini card Slot 3
TV
PCI-E
USB

6*PCI-E x1

SPI ROM
BIOS

LPC BUS

EC
ENE KB9012

Card Reader
JBM389C
SD/MMC/MS/XD
Audio Board

WLAN/WiMAX

TV

LAN(Gbe)
ATHEROS
AR8161/AR8151

RJ45 CONN

Touch Pad

Int.KBD

Thermal Sensor
EMC1403/2103

Audio Codec
RealTek
ALC269-VC

2Channel Speaker
Array Digital MIC
Audio Jacks
Stereo
HeadPhone Output
Microphone Input
Audio Board

Sub-borad
POWER BOARD
Function Board
Audio Board

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Title: MB Block Diagram
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Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCSA +V1.5S_VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +1.05VS +0.75VS +3.3VS_VGA +1.5VS_VGA +1.05VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	10K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	Project	
0	0	0 V	0 V	0 V	QIWY3	EVT
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	QIWY3	DVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	QIWY3	PVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	QIWY3	MP
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	QIWY4	EVT
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	QIWY4	DVT
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	QIWY4	PVT
7	NC	2.500 V	3.300 V	3.300 V	QIWY4	MP

SMBUS Control Table

	SOURCE	VGA	BATT	KE9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X

USB Port Table

USB 2.0	USB 3.0		Port	4 External USB Port
EHCI1	XHCI	1	0	USB Port (Right Side)
		2	1	
		3	2	USB Port (Left Side)
		4	3	USB Port (Left Side)
			4	
			5	Camera
			6	
			7	
EHCI2			8	
			9	USB Port (Right Side)
			10	Mini Card(WLAN)
			11	
			12	Mini Card(TV)
			13	Blue Tooth

PCIE PORT LIST

Port	Device
1	LAN
2	WLAN
3	TV
4	Card Reader
5	
6	
7	
8	

BOM Structure Table

BOM Structure	BTO Item
OPTI@	OPTIMUS part
HDMI@	HDMI part
TV@	TV module part
CHG@	USB charger part
NOCHG@	No USB charger part
BT@	Blue Tooth part
CMOS@	CMOS Camera part
8161@	AR8161 LAN part
8151@	AR8151 LAN part
8161S@	AR8161 LAN surge part
8151S@	AR8151 LAN surge part
SURGE@	AR8151&8161 LAN surge part
61@	X76 P/N for AR8161
51@	X76 P/N for AR8151
X76@	X76 Level part for VRAM
S1G@	X76 P/N for Samsun VRAM 1G
S2G@	X76 P/N for Samsun VRAM 2G
H1G@	X76 P/N for Hynix VRAM 1G
H2G@	X76 P/N for Hynix VRAM 2G
GL@	N13P-GL part
GT@	N13P-GT part
GE@	N13E-GE part
GTGE@	N13P-GT&N13E-GE common part
GC6@	NV CG6 support part
NOGC6@	NV no CG6 support part
1403@	EMC1403 thermal part
2103@	EMC2103 thermal part
KBL@	K/B Light part
ME@	ME part
@	Unpop

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

ZZZ1

DA80000Q900

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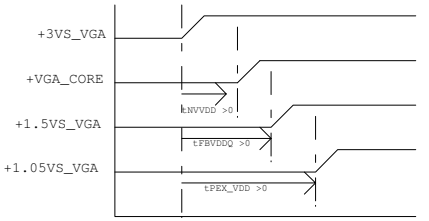
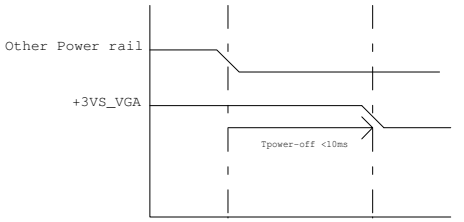
Hot plug detect for IFP link C

VGA and GDDR5 Voltage Rails (N13Px GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	N/A	
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	GC6 event
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	N/A	
GPIO15	IN	N/A	(100K pull low)
GPIO16	OUT	N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	



1. all power rail ramp up time should be larger than 40us



1.all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

Performance Mode P0 TDP at Tj = 102 C* (GDDR5)

Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.35V) (A)	FBVDD (1.35V) (W)	FBVDDQ (GPU+Mem) (1.35V) (A)	FBVDDQ (GPU+Mem) (1.35V) (W)	PCI Express (1.05V) (6) (mA)	PCI Express (1.05V) (6) (W)	I/O and PLLVDD (1.8V) (mA)	I/O and PLLVDD (1.8V) (W)	I/O and PLLVDD (1.05V) (mA)	I/O and PLLVDD (1.05V) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N13X 128bit 1GB GDDR5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

	Device ID
N13P-GT (28nm)	0x0FDB
N13E-GE (28nm)	0x0FDB
N13P-GL1 (40nm)	0x0DE9

GPU	ROM_SO	ROM_SCLK	STRAP4	STRAP3	STRAP2	STRAP1	STRAP0
N13P-GT	PU 10K	PU 5K	PD 45K	PD 5K	PD 10K	PD 35K	PU 45K
N13E-GE	PU 10K	PU 5K	PD 45K	PD 5K	PD 25K	PD 35K	PU 45K
N13P-GL	PD 10K	PD 15K	NC	NC	PU 10K	PD 45K	PU 45K

GPU		N13P-GT	N13E-GE	N13P-GL
FB Memory (GDDR5)		ROM_SI	ROM_SI	ROM_SI
Samsung 2500MHz	K4G10325FG-HC04			
	32Mx32	PD 45K	PD 45K	PD 45K
Hynix 2500MHz	H5GQ1H24BFR-T2C			
	32Mx32	PD 35K	PD 35K	PD 35K
Samsung 2500MHz	K4G20325FG-HC04			
	64Mx32	PD 30K	PD 30K	PD 30K
Hynix 2500MHz	H5GQ2H24MFR-T2C			
	64Mx32	PD 25K	PD 25K	PD 25K

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Title: VGA Notes List

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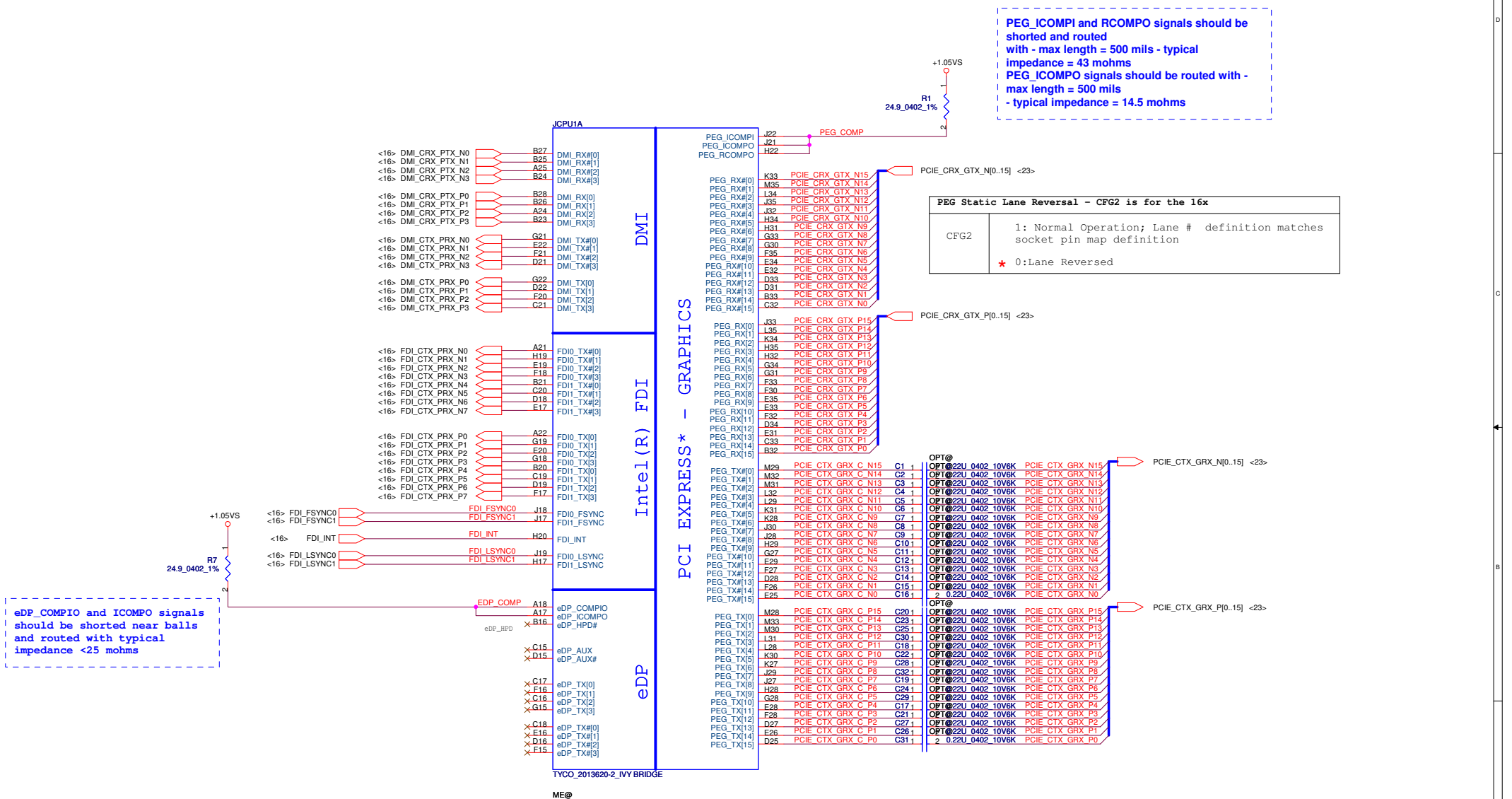

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Compal Electronics, Inc.

Title: PROCESSOR(1/7) DMI,FDI,PEG

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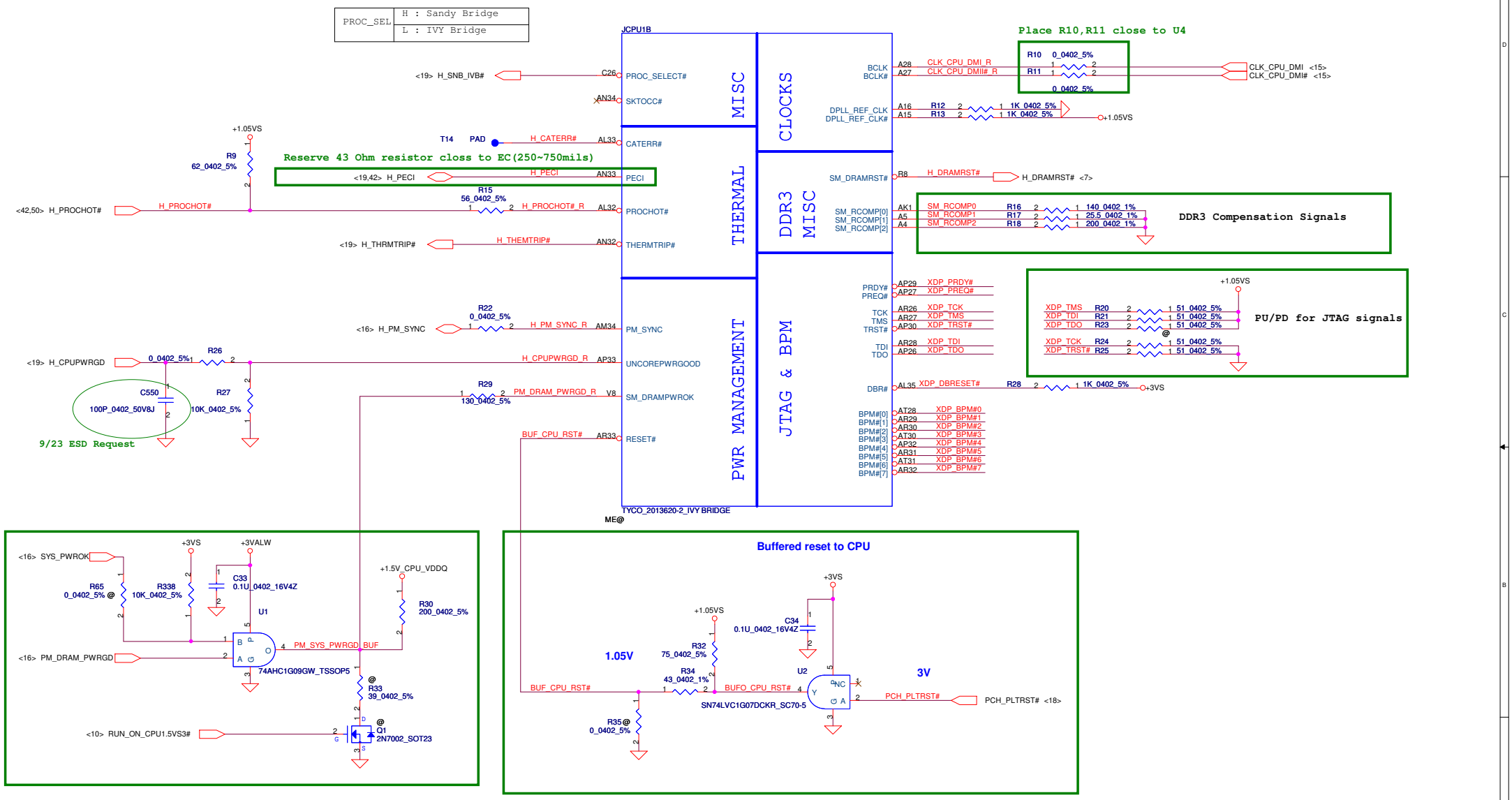

Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title	PROCESSOR(2/7) PM,XDP,CLK		
Size: Custom	Document Number: QIWY4 LA-8002P		Rev: 1.0
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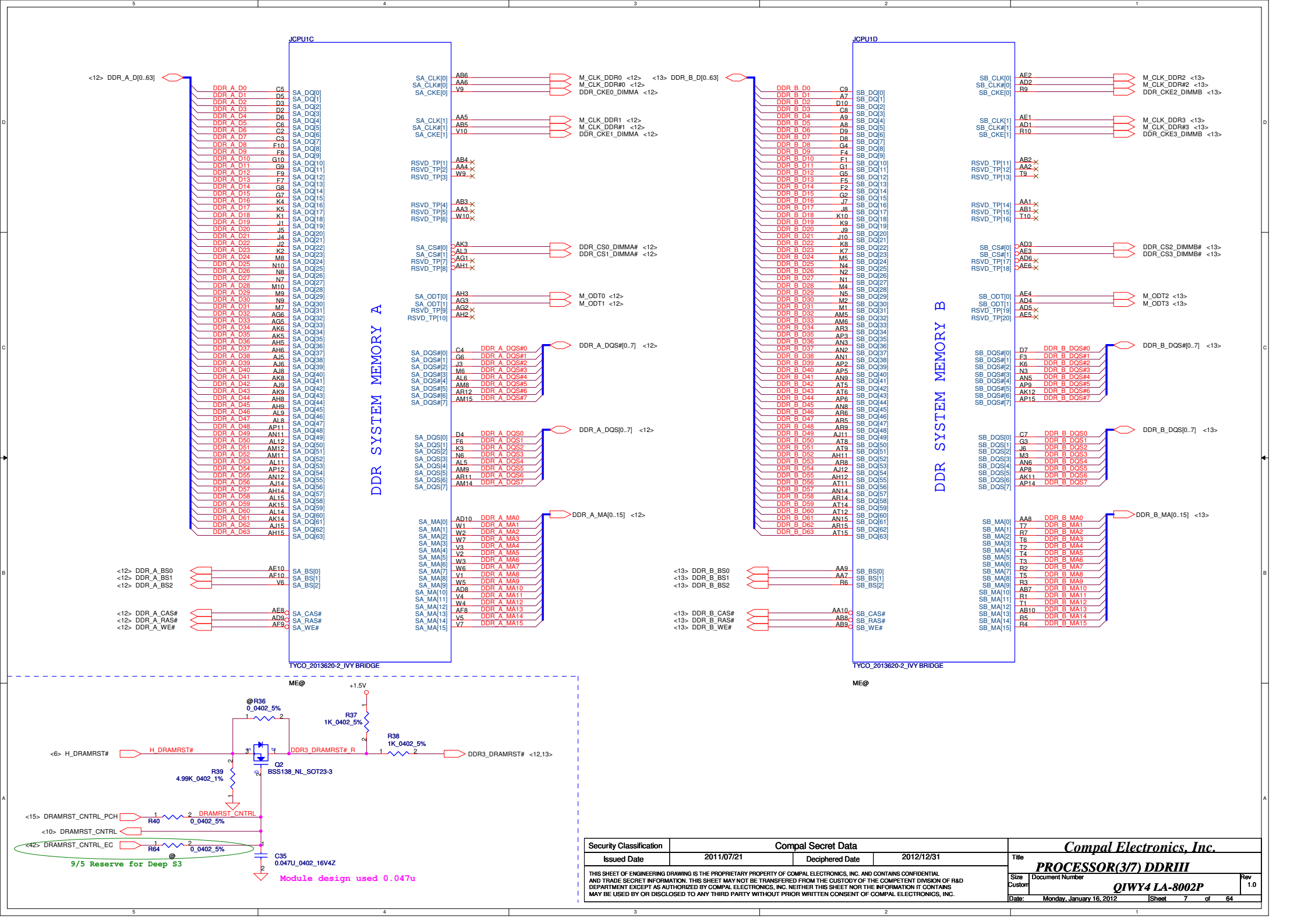

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: PROCESSOR(3/7) DDRIII

Size: Custom | Document Number: QIWY4 LA-8002P | Rev: 1.0

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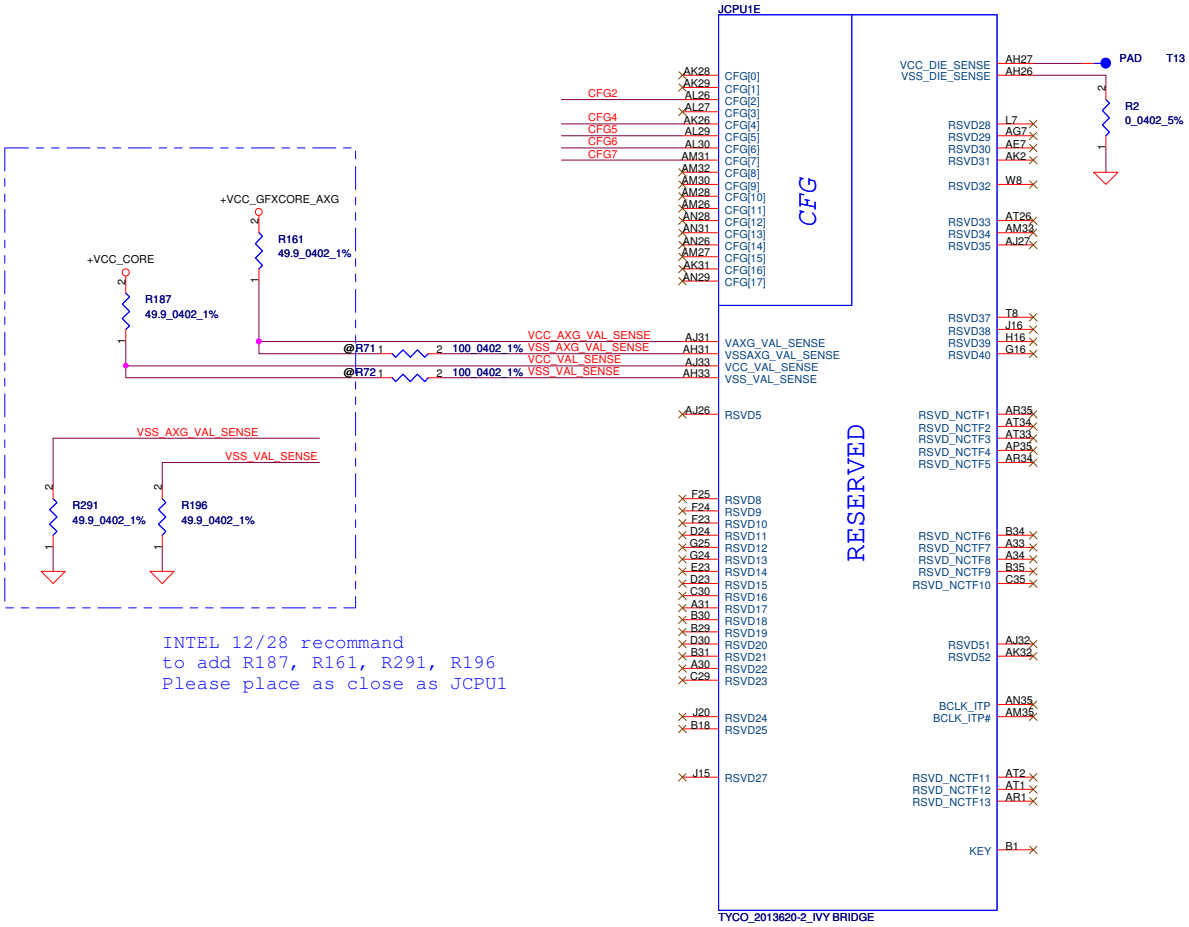
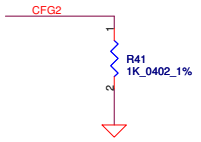
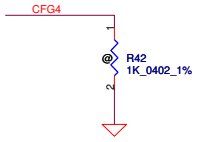
CFG Straps for Processor



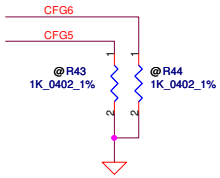
INTEL 12/28 recommand
to add R187, R161, R291, R196
Please place as close as JCPU1



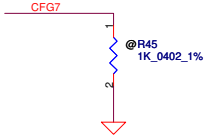
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: PROCESSOR(4/7) RSVD,CFG			
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POWER

JCPU1F

+VCC_CORE

QC=94A
DC=53A

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

CORE SUPPLY

PEG AND DDR

+1.05VS

8.5A

VCCIO1 AH13
VCCIO2 AH10
VCCIO3 AG10
VCCIO4 AC10
VCCIO5 Y10
VCCIO6 U10
VCCIO7 P10
VCCIO8 L10
VCCIO9 J14
VCCIO10 J13
VCCIO11 J12
VCCIO12 J11
VCCIO13 H14
VCCIO14 H12
VCCIO15 H11
VCCIO16 G14
VCCIO17 G13
VCCIO18 G12
VCCIO19 F14
VCCIO20 F13
VCCIO21 F12
VCCIO22 F11
VCCIO23 E14
VCCIO24 E12
VCCIO25 E11
VCCIO26 D14
VCCIO27 D13
VCCIO28 D12
VCCIO29 D11
VCCIO30 C14
VCCIO31 C13
VCCIO32 C12
VCCIO33 C11
VCCIO34 B14
VCCIO35 B12
VCCIO36 A14
VCCIO37 A13
VCCIO38 A12
VCCIO39 A11
VCCIO40 J23

SVID

+1.05VS

Place the PU resistor close to CPU

C36 0.1U_0402_10V7K

R46 75_0402_5%

VIDALERT# AJ29 H_CPU_SVIDALRT# R47 43_0402_5%
VIDSCLK AJ30 H_CPU_SVIDCLK R48 0_0402_5%
VIDSOUT AJ28 H_CPU_SVIDDAT R49 0_0402_5%

VR_SVID_ALRT# <57>
VR_SVID_CLK <57>
VR_SVID_DAT <57>

R50 130_0402_5% +1.05VS

Place the PU resistor close to CPU

VCC_SENCE 100ohm +-1% pull-up to VCC near processor

SENSE LINES

+VCC_CORE

R51 100_0402_1%

VCC_SENSE AJ35 VCCSENSE_R R52 0_0402_5%
VSS_SENSE AJ34 VSSSENSE_R R53 0_0402_5%

VCCSENSE <57>
VSSSENSE <57>

R1294 10_0402_1% +1.05VS

@R73 100_0402_1%

R54 100_0402_1%

VCCIO_SENSE B10 VCCIO_SENSE <55>
VSS_SENSE_VCCIO A10 VSSIO_SENSE VSSIO_SENSE <55>

R1297 10_0402_1%

VSS_SENCE 100ohm +-1% pull-down to GND near processor

TYCO_2013620-2_VX BRIDGE

ME@

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Compal Electronics, Inc.

Title: PROCESSOR(5/7) PWR,BYPASS

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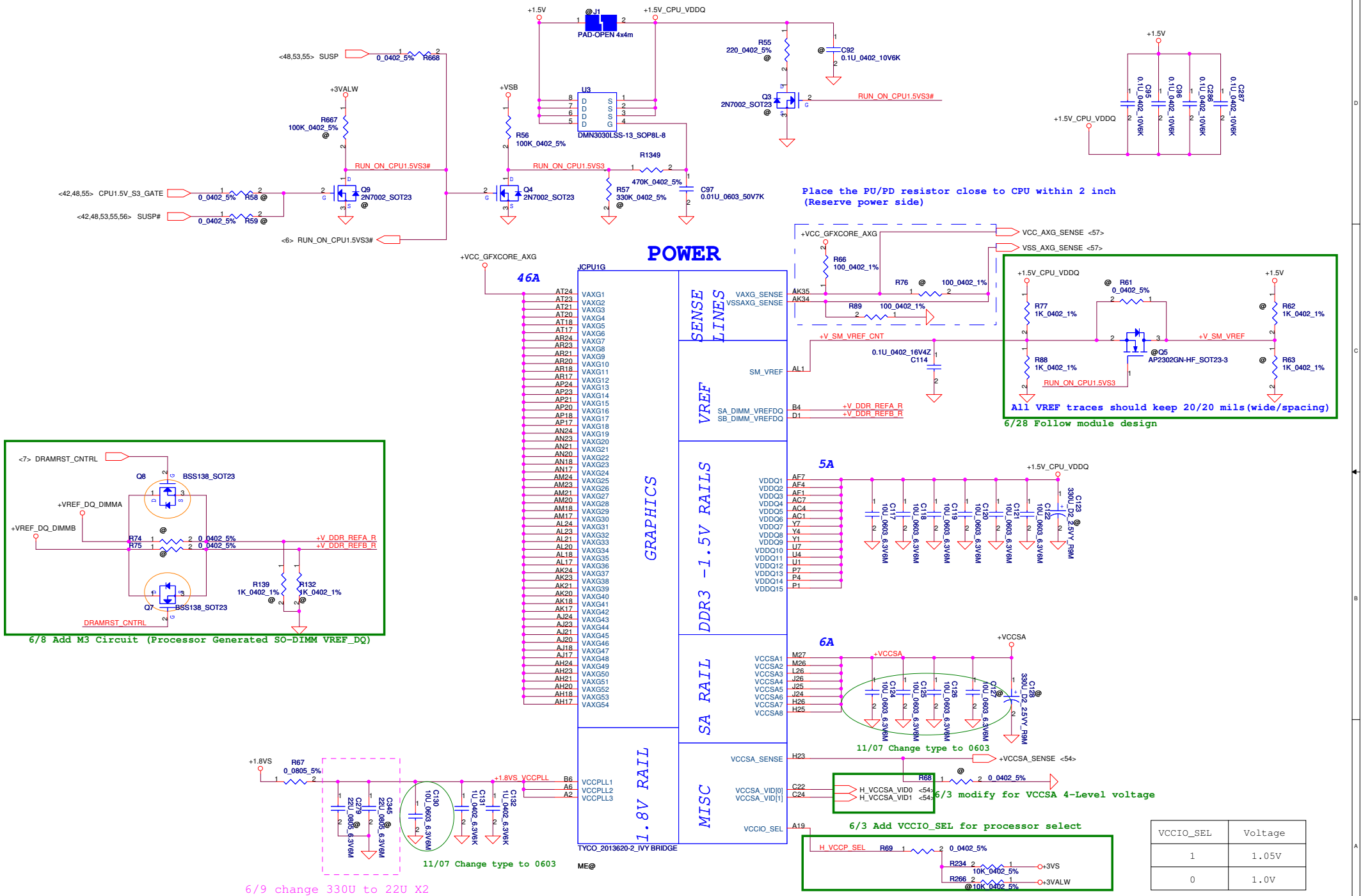
POWER



VCCIO_SEL	Voltage
1	1.05V
0	1.0V

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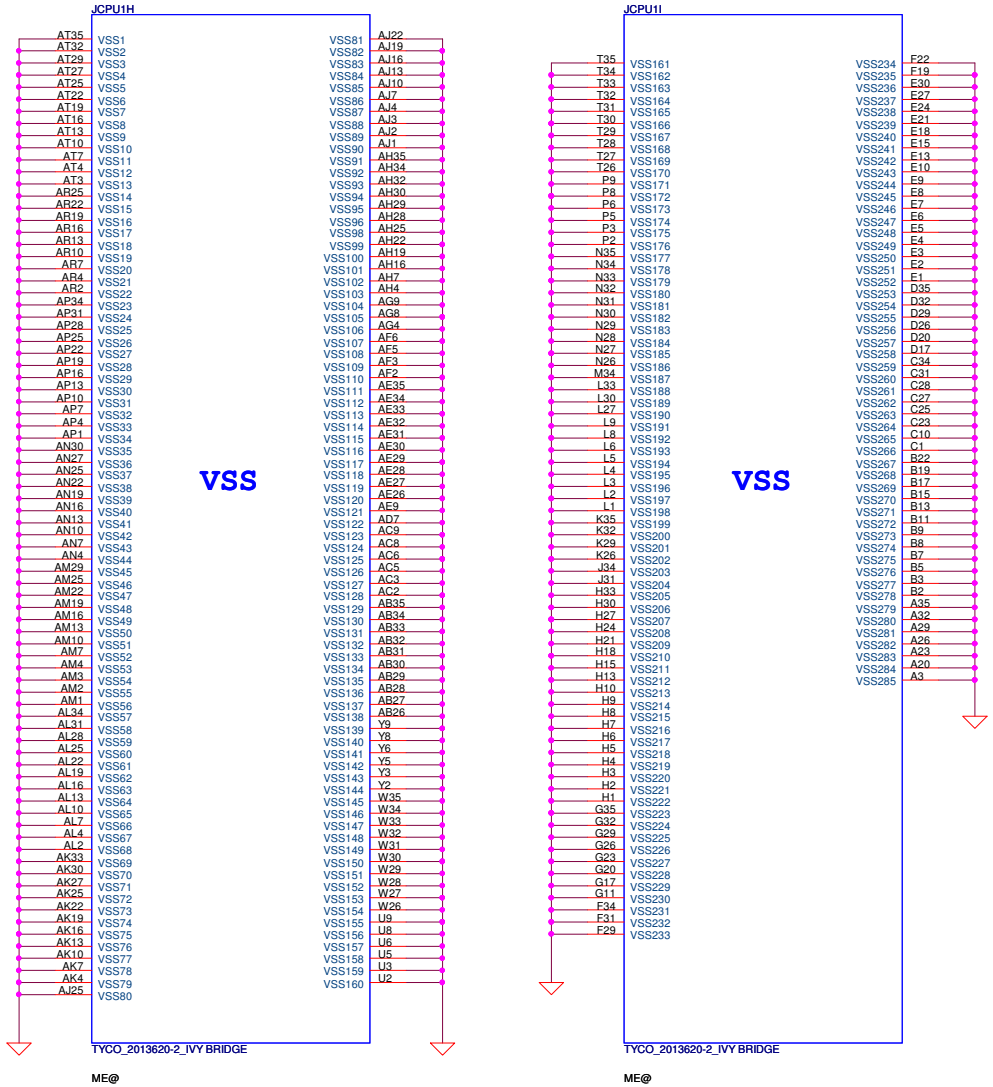

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Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

Size	Document Number	Rev
Custom	QIWY4 LA-8002P	1.0

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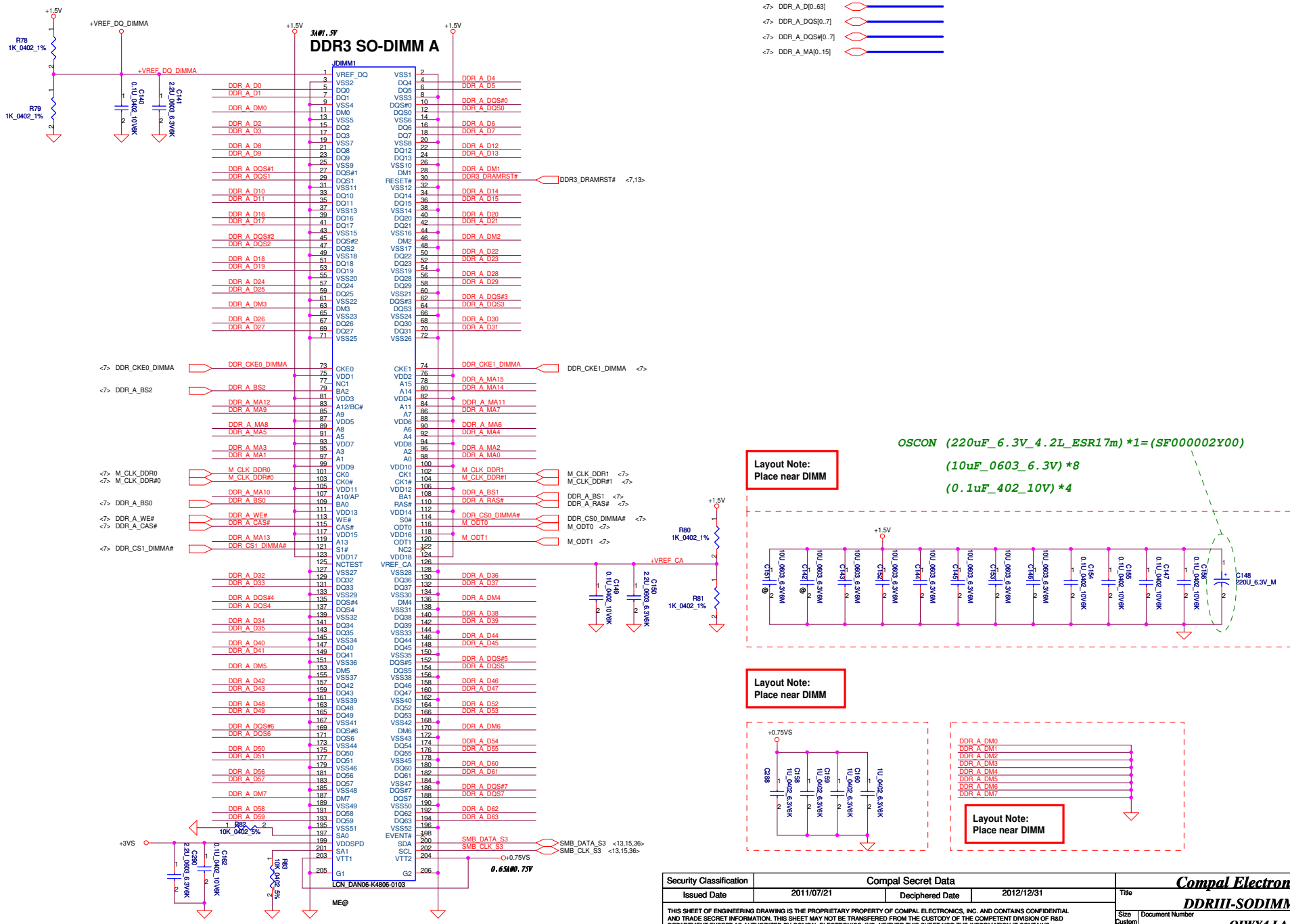


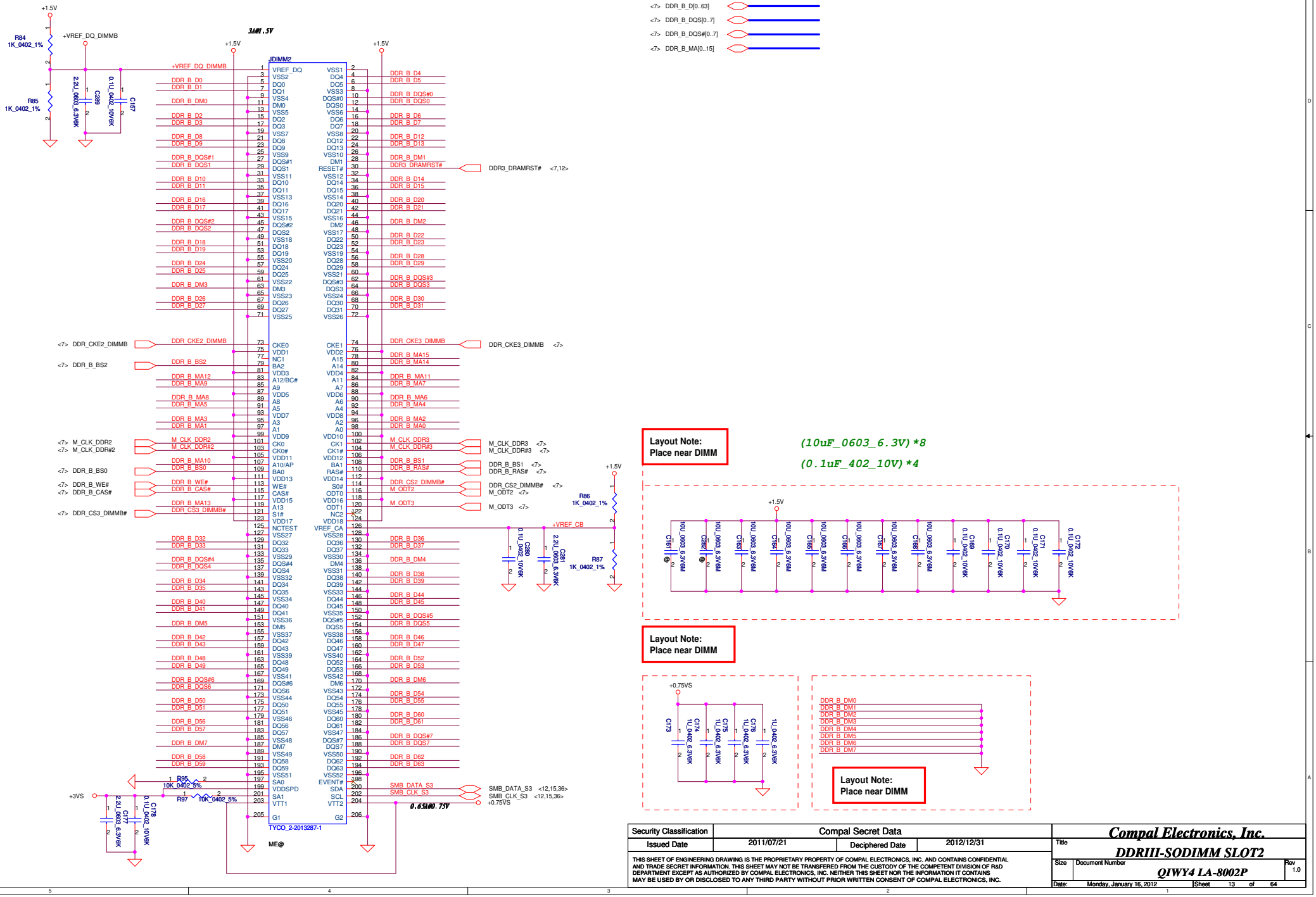
Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT1**

Size	Document Number	Rev
Custom	QIWY4 LA-8002P	1.0

Date: Monday, January 16, 2012 | Sheet 12 of 64



Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT2**

Size | Document Number: **QIWY4 LA-8002P** | Rev: 1.0

Date: Monday, January 16, 2012 | Sheet 13 of 64

W=20mils
W=20mils
+RTCVCC
+RTCBATT
R99
1K_0402_5%
C179
1U_0603_10V4Z
CLRP1
SHORT PADS
PCH_RTCX1
PCH_RTCX2
R98
10M_0402_5%
Y1
32.768KHZ_12.5PF_CM31532768DZFT
15P_0402_50V8J
C180
C181
18P_0402_50V8J
CMOS
+RTCVCC
R101
1M_0402_5%
SM_INTRUDER#
R102
330K_0402_5%
PCH_INTVRMEN
INTVRMEN
★ H : Integrated VRM enable
L : Integrated VRM disable
(INTVRMEN should always be pull high.)
+RTCVCC
C183
1U_0603_10V4Z
R103
20K_0402_5%
R100
20K_0402_5%
C182
1U_0603_10V4Z
CLRP2
SHORT PADS
CLRP3
SHORT PADS
PCH_RTCX1
PCH_RTCX2
PCH_RTCRST#
PCH_SRTCRST#
SM_INTRUDER#
PCH_INTVRMEN
U4A
RTCX1 A20
RTCX2 C20
RTCRST# D20
SRTCRST# G22
INTRUDER# K22
INTVRMEN C17
RTC
+3VS
R105
1K_0402_5%
HDA_SPKR
HIGH= Enable (No Reboot)
★ LOW= Disable (Default)
HDA_BIT_CLK
HDA_SYNC
HDA_SPKR
HDA_RST#
<41> HDA_SPKR
HDA_BCLK N34
HDA_SYNC L34
SPKR T10
HDA_RST# K34
+3V_PCH
R106
1K_0402_5%
HDA_SDOUT
★ Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Overide]
<41> HDA_SDIN0
HDA_SDIN0
HDA_SDIN0 E34
HDA_SDIN1 G34
HDA_SDIN2 C34
HDA_SDIN3 A34
IHDA
<42> ME_FLASH
R109
0_0402_5%
HDA_SDO A36
+3V_PCH
R108
1K_0402_5%
HDA_SYNC
This signal has a weak internal pull-down
R107
1K_0402_1%
PCH_GPIO33
R317
10K_0402_5%
PCH_GPIO13
HDA_DOCK_EN# / GPIO33 C36
HDA_DOCK_RST# / GPIO13 N32
On Die PLL VR Select is supplied by
★ 1.5V when smapled high
1.8V when sampled low
Needs to be pulled High for Chief River platfrom
PCH_JTAG_TCK
PCH_JTAG_TMS
PCH_JTAG_TDI
PCH_JTAG_TDO
R110
51_0402_5%
JTAG_TCK J3
JTAG_TMS H7
JTAG_TDI K5
JTAG_TDO H1
JTAG
11/08 Follow DG change to +5VS
+5VS
Q10
BSS138_NL_SOT23-3
R1353
1M_0402_5%
R112
33_0402_5%
R114
33_0402_5%
R116
33_0402_5%
R118
33_0402_5%
<41> HDA_BITCLK_AUDIO
<41> HDA_SYNC_AUDIO
<41> HDA_RST_AUDIO#
<41> HDA_SDOUT_AUDIO
HDA_BIT_CLK
HDA_SYNC_R
HDA_RST#
HDA_SDOUT
SPI_CLK_PCH
SPI_SB_CS0#
SPI_SB_CS1#
SPI_SI
SPI_SO_R
SPI_CLK T3
SPI_CS0# Y14
SPI_CS1# T1
SPI_MOSI V4
SPI_MISO U3
SPI
+3V_PCH
+3V_PCH
+3V_PCH
R121
200_0402_5%
R122
200_0402_5%
R123
200_0402_5%
PCH_JTAG_TDO
PCH_JTAG_TMS
PCH_JTAG_TDI
R125
100_0402_1%
R126
100_0402_1%
R128
100_0402_1%
PANTHER-POINT_FCBGA989
LPC
FWH0 / LAD0 C38 LPC_AD0
FWH1 / LAD1 A38 LPC_AD1
FWH2 / LAD2 B37 LPC_AD2
FWH3 / LAD3 C37 LPC_AD3
LPC_AD0 <36,42>
LPC_AD1 <36,42>
LPC_AD2 <36,42>
LPC_AD3 <36,42>
EC and Mini card debug port
FWH4 / LFRAME# D36 LPC_FRAME#
LPC_FRAME# <36,42>
LDRQ0# E36
LDRQ1# / GPIO23 K36
SERIRQ V5
R104
10K_0402_5%
+3VS
SERIRQ
SERIRQ <42>
SATA 6G
SATA0RXN AM3
SATA0RXP AM1
SATA0TXN AP7
SATA0TXP AP5
SATA_ITX_C_DRX_N0
SATA_ITX_C_DRX_P0
0.01U_0402_16V7K
C184
C185
SATA_ITX_DRX_N0
SATA_ITX_DRX_P0
SATA_DTX_C_IRX_N0
SATA_DTX_C_IRX_P0
SATA_DTX_C_IRX_N0 <36>
SATA_DTX_C_IRX_P0 <36>
SATA_ITX_DRX_N0 <36>
SATA_ITX_DRX_P0 <36>
SSD
SATA1RXN AM10
SATA1RXP AM8
SATA1TXN AP11
SATA1TXP AP10
SATA_ITX_C_DRX_N1
SATA_ITX_C_DRX_P1
0.01U_0402_16V7K
C273
C272
SATA_ITX_DRX_N1
SATA_ITX_DRX_P1
SATA_DTX_C_IRX_N1
SATA_DTX_C_IRX_P1
SATA_DTX_C_IRX_N1 <40>
SATA_DTX_C_IRX_P1 <40>
SATA_ITX_DRX_N1 <40>
SATA_ITX_DRX_P1 <40>
HDD
SATA2RXN AD7
SATA2RXP AD5
SATA2TXN AH5
SATA2TXP AH4
SATA_ITX_C_DRX_N2
SATA_ITX_C_DRX_P2
0.01U_0402_16V7K
C186
C187
SATA_ITX_DRX_N2_CONN
SATA_ITX_DRX_P2_CONN
SATA_DTX_C_IRX_N2
SATA_DTX_C_IRX_P2
SATA_DTX_C_IRX_N2 <40>
SATA_DTX_C_IRX_P2 <40>
SATA_ITX_DRX_N2_CONN <40>
SATA_ITX_DRX_P2_CONN <40>
ODD
SATA3RXN AB8
SATA3RXP AB10
SATA3TXN AF3
SATA3TXP AF1
SATA4RXN Y7
SATA4RXP Y5
SATA4TXN AD3
SATA4TXP AD1
SATA5RXN Y3
SATA5RXP Y1
SATA5TXN AB3
SATA5TXP AB1
SATA
SATAICOMPO Y11
SATAICOMPI Y10
SATA_COMP
R111
37.4_0402_1%
+1.05VS_VCC_SATA
SATA3RCOMPO AB12
SATA3RCOMPI AB13
SATA3_COMP
R113
49.9_0402_1%
+1.05VS_SATA3
SATA3RBIAS AH1
RBIAS_SATA3
R115
750_0402_1%
SATALED# P3
SATALED#
R120
10K_0402_5%
+3VS
SATA0GP / GPIO21 V14
PCH_GPIO21
R119
10K_0402_5%
+3VS
SATA1GP / GPIO19 P1
BBS_BIT0_R
R1418
0_0402_5%
SATA_DET# <36>
R316
10K_0402_5%
+3VS
SPI ROM FOR ME
& Non-share ROM.
2MB P/N : SA00003FO10
+3VS
R292
3.3K_0402_5%
SPI_WP#_1
R246
3.3K_0402_5%
SPI_HOLD#_1
R303
0_0402_5%
SPI_SB_CS1#
SPI_SO_R
R294
33_0402_5%
U9
CS# VCC
DO(IO1) HOLD#(IO3)
WP#(IO2) CLK
GND DI(IO0)
W25Q16BVSSIG_SO8
+3VS
C275
0.1U_0402_16V4Z
R299
33_0402_5%
SPI_HOLD#_1
SPI_CLK_PCH_1
SPI_SI_R1
R199
33_0402_5%
SPI_CLK_PCH
SPI_SI
4MB P/N : SA00003K800
+3VS
R127
3.3K_0402_5%
SPI_WP#
R129
3.3K_0402_5%
SPI_HOLD#
R130
0_0402_5%
SPI_SB_CS0#
SPI_SO_R
R131
33_0402_5%
U5
CS# VCC
DO HOLD#
WP# CLK
GND DI
W25Q32BVSSIG_SO8
+3VS
C191
0.1U_0402_16V4Z
R298
33_0402_5%
SPI_HOLD#
SPI_CLK_PCH_0
SPI_SI_R
R133
33_0402_5%
SPI_CLK_PCH
SPI_SI
SPI_CLK_PCH
R124
33_0402_5%
C190
22P_0402_50V8J

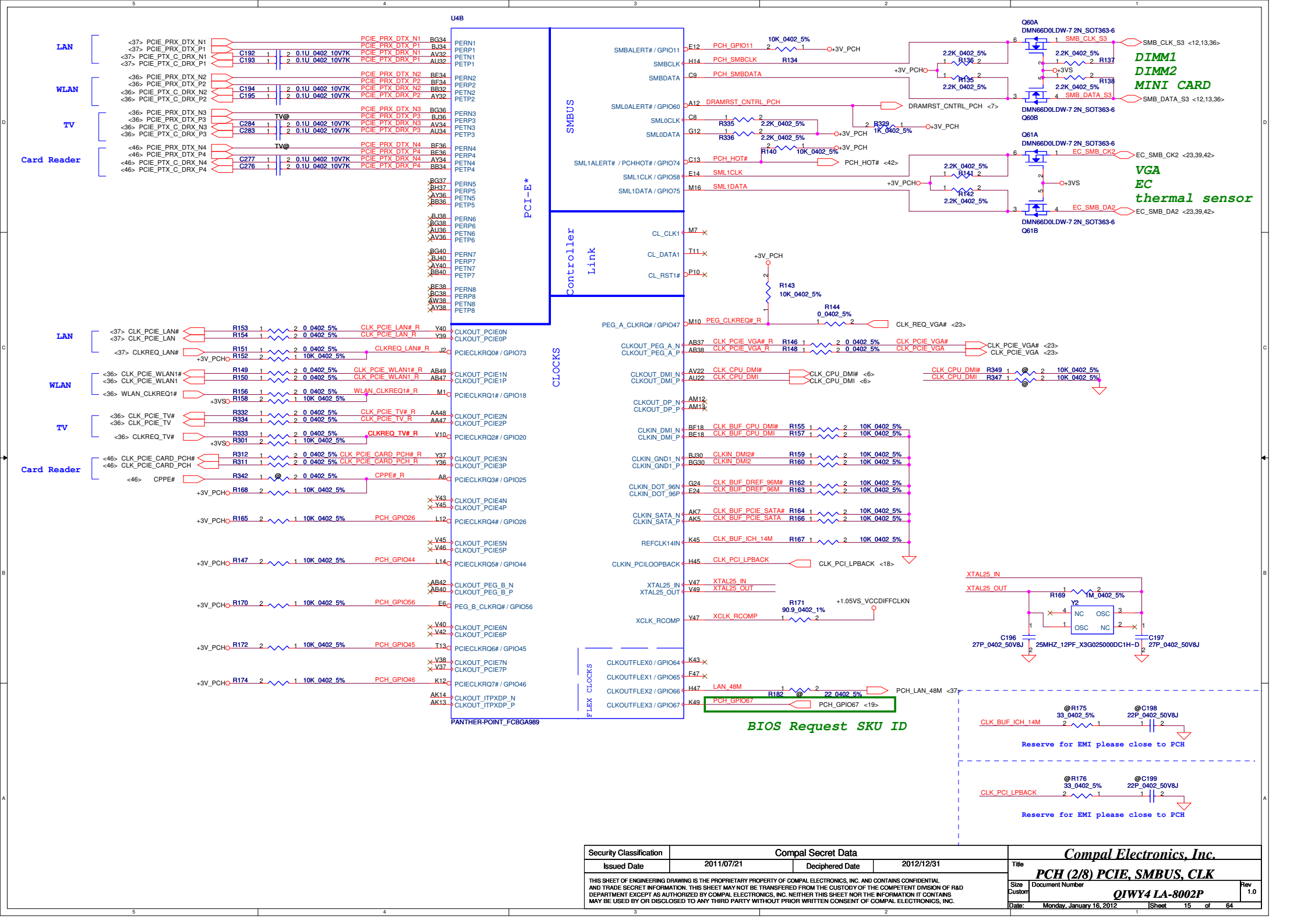
Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PCH (1/8) SATA,HDA,SPI, LPC, XDP

Size	Document Number	Rev
Custom	QIWY4 LA-8002P	1.0

Date: Monday, January 16, 2012 Sheet 14 of 64



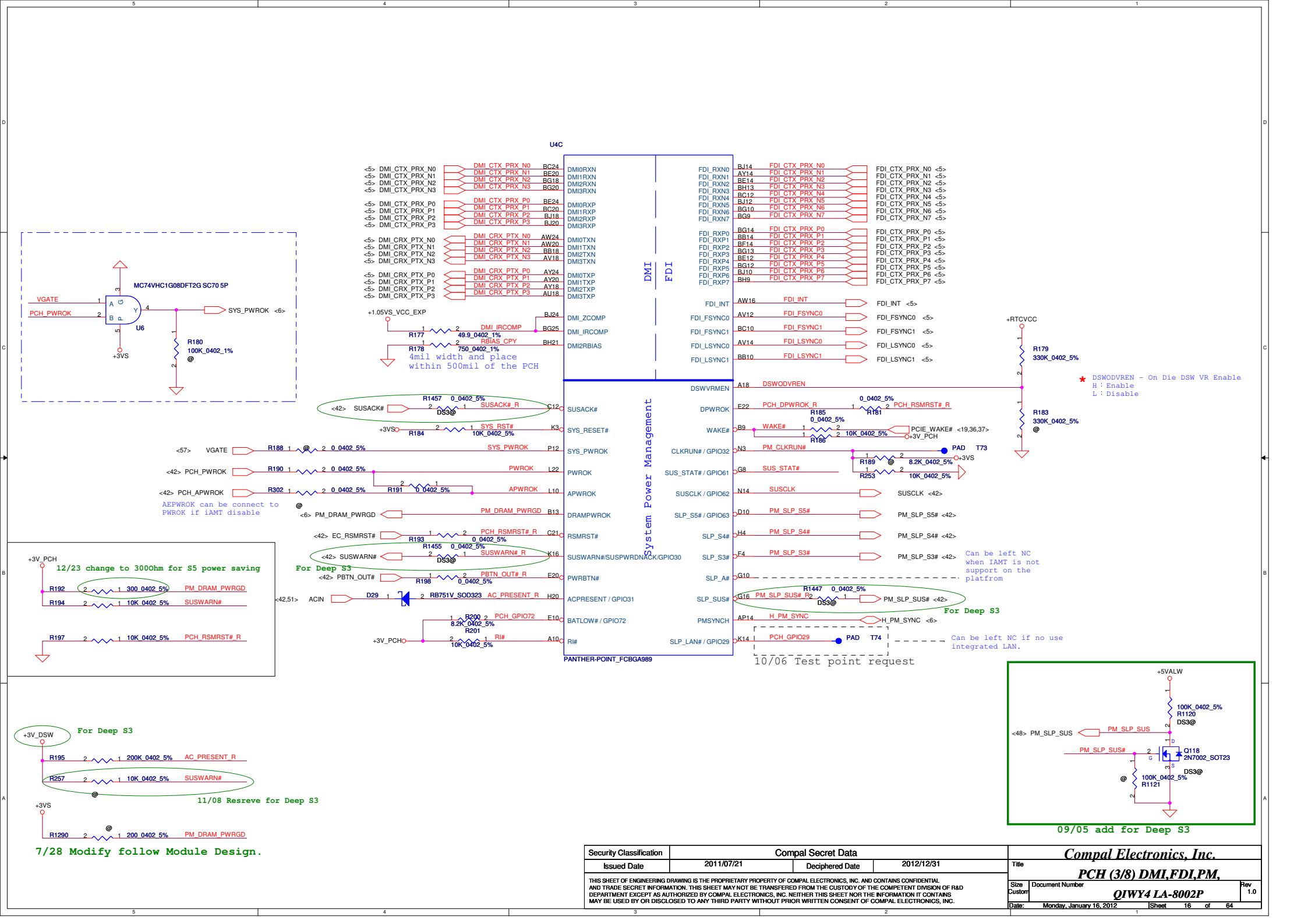
Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PCH (2/8) PCIE, SMBUS, CLK

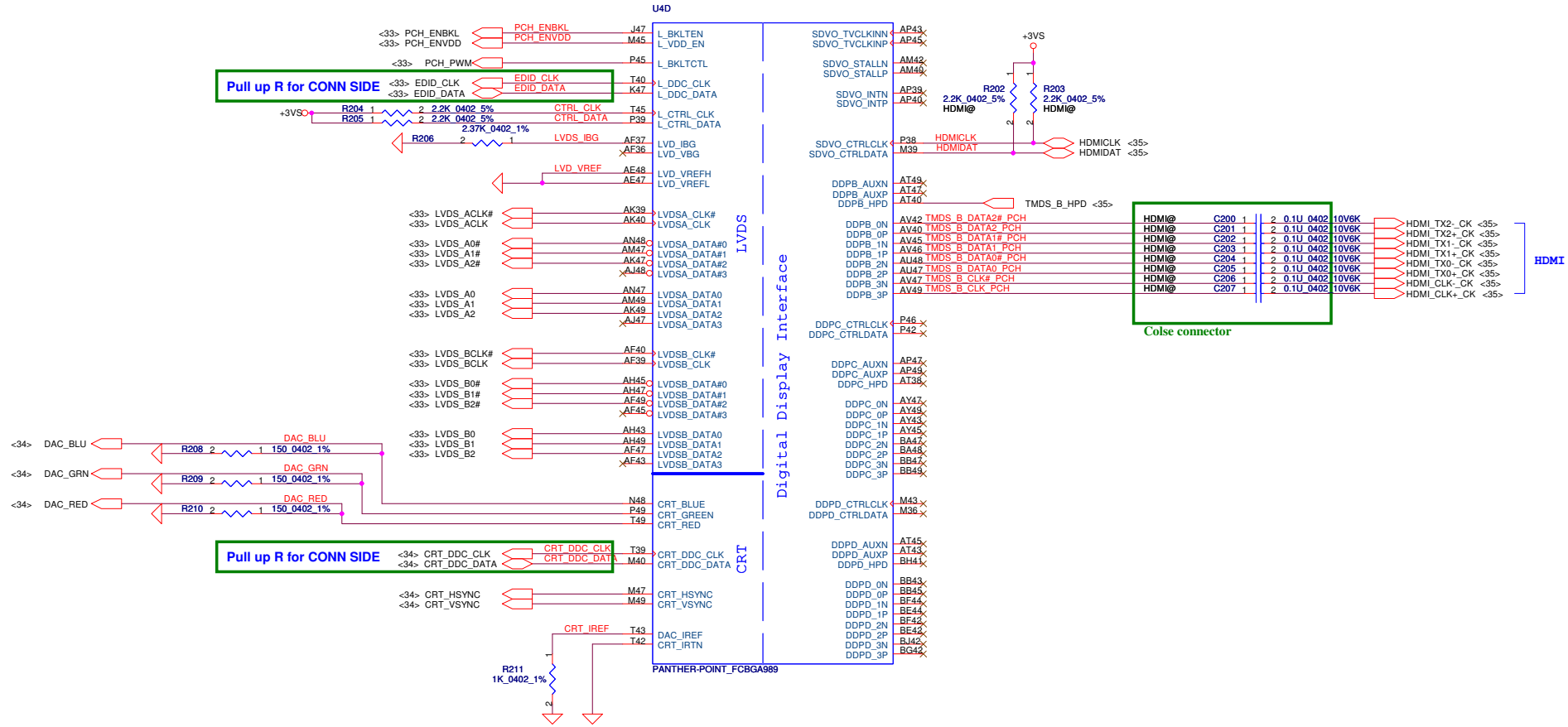
Size	Document Number	Rev
Custom	QIWY4 LA-8002P	1.0

Date: Monday, January 16, 2012 Sheet 15 of 64



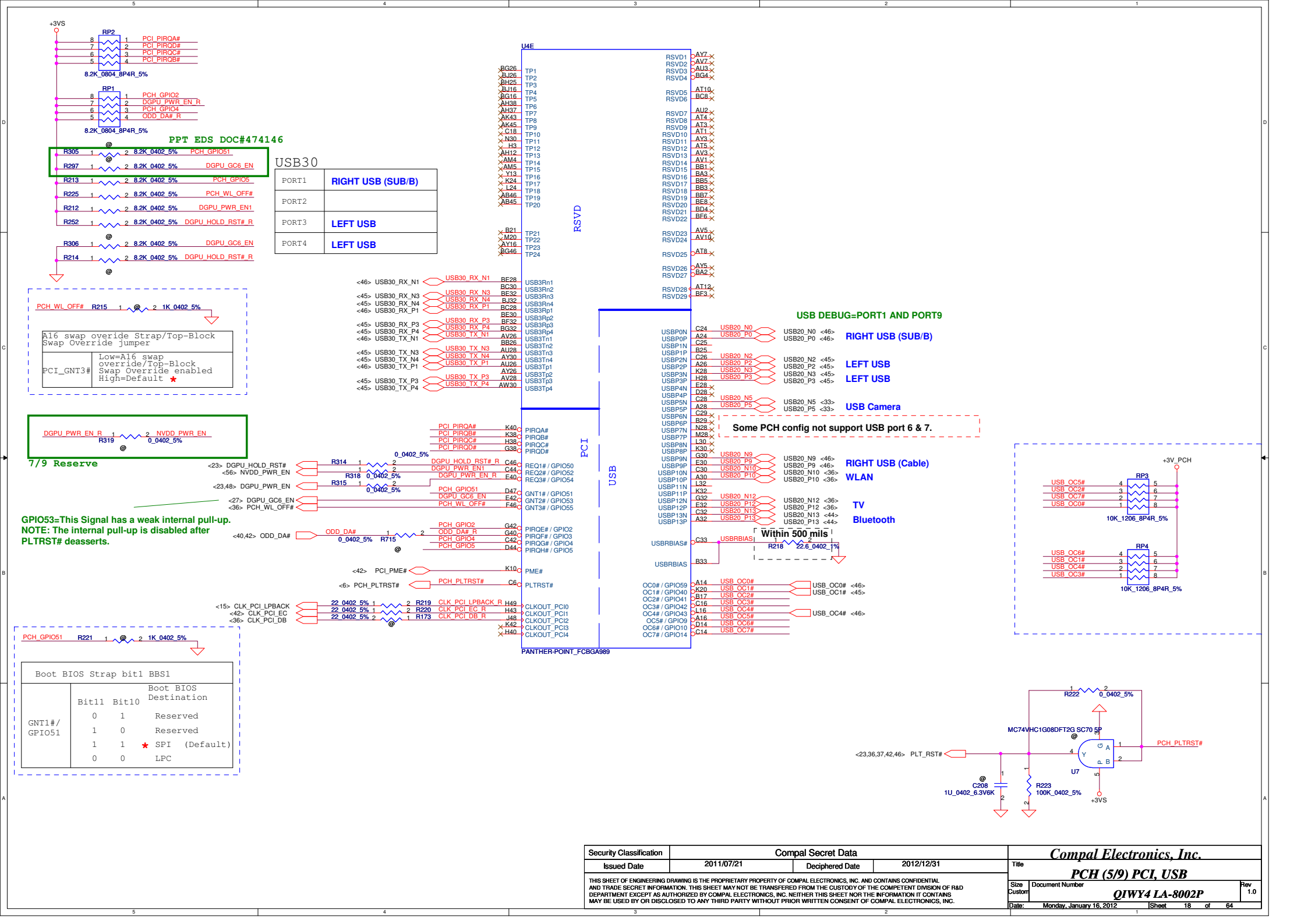
Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title	PCH (3/8) DMI,FDI,PM,		
Size: Custom	Document Number: QIWY4 LA-8002P		Rev: 1.0
Date: Monday, January 16, 2012	Sheet 16 of 64		



Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title	PCH (4/9) LVDS,CRT,DP,HDMI		
Size: Custom	Document Number: QIWY4 LA-8002P		Rev: 1.0
Date: Monday, January 16, 2012	Sheet 17 of 64		



Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB

Size: Custom | Document Number: QIWY4 LA-8002P | Rev: 1.0

Date: Monday, January 16, 2012 | Sheet 18 of 64

Function	PCH_GPIO38	PCH_GPIO67	PCH_GPIO70	PCH_GPIO69
SG	0	0	X	X
Reserve	0	1	X	X
DIS	1	0	X	X
UMA	1	1	X	X
14"	X	X	0	0
14"L	X	X	0	1
15"	X	X	1	0
Reserve	X	X	1	1

MB ID

+3VS R711 R708 R704 R703 10K_0402_5%

PCH_GPIO38 PCH_GPIO67 PCH_GPIO69 PCH_GPIO70

<15> PCH_GPIO67

R712 R709 R706 R705 10K_0402_5%

+3V_PCH R280 @ 10K_0402_5% R235 1K_0402_5% EC_SMI#

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable
R240 @ 1K_0402_5% PCH_GPIO28

PCH_GPIO27 (Have internal Pull-High)
★High: VCCVRM VR Enable
Low: VCCVRM VR Disable

+3V_DSW R207 AOAC@ 10K_0402_5% R245 @ 10K_0402_5% AOAC_WAKE#

+3VS R250 200_0402_5% PCH_GPIO36 R264 10K_0402_5% @

+3VS R244 @ 10K_0402_5% PCH_GPIO37 R259 10K_0402_5%

<23> GC6_EVENT# GC6_EVENT#

+3VS R233 10K_0402_5%

+3VS R227 10K_0402_5% PCH_GPIO1
+3VS R228 10K_0402_5% PCH_GPIO6
<42> EC_SCI# EC_SCI#
<42> EC_SMI# EC_SMI#
+3V_PCH R229 @ 10K_0402_5% PCH_GPIO12
R230 10K_0402_5% EC_LID_OUT#
<42> EC_LID_OUT#
+3VS R231 10K_0402_5% PCH_GPIO16
R232 @ 10K_0402_1%
<27,53,56> DGPU_PWROK R339 0_0402_5% DGPU_PWROK_R
+3VS R238 10K_0402_5% BT_DISABLE
<36> BT_DISABLE
AOAC@ R224 0_0402_5% AOAC_WAKE#
<16,36,37> PCIE_WAKE#
+3V_PCH R241 10K_0402_5% PCH_GPIO28
<36,44> PCH_BT_ON# +3VS R242 10K_0402_5% PCH_BT_ON#
R243 10K_0402_5% PCH_GPIO35
PCH_GPIO36
PCH_GPIO37
PCH_GPIO38
+3VS R247 10K_0402_5% PCH_GPIO39
R248 10K_0402_5% PCH_GPIO48
+3VS R249 10K_0402_5% PCH_GPIO49
+3V_PCH R251 10K_0402_5% PCH_GPIO57

<40> ODD_EN ODD_EN

U4F

T7	BMBUSY# / GPIO0	TACH4 / GPIO68	C40 PCH_GPIO68
A42	TACH1 / GPIO1	TACH5 / GPIO69	B41 PCH_GPIO69
H36	TACH2 / GPIO6	TACH6 / GPIO70	C41 PCH_GPIO70
E38	TACH3 / GPIO7	TACH7 / GPIO71	A40
C10	GPIO8		
C4	LAN_PHY_PWR_CTRL / GPIO12		
G2	GPIO15		
U2	SATA4GP / GPIO16		
D40	TACH0 / GPIO17		
T5	SCLOCK / GPIO22		
E8	GPIO24		
E16	GPIO27		
P8	GPIO28		
K1	STP_PCI# / GPIO34		
K4	GPIO35		
V8	SATA2GP / GPIO36		
M5	SATA3GP / GPIO37		
N2	SLOAD / GPIO38		
M3	SDATAOUT0 / GPIO39		
V13	SDATAOUT1 / GPIO48		
V3	SATA5GP / GPIO49 / TEMP_ALERT#		
D6	GPIO57		

GPIO

P4	A20GATE		
AU16	PECI	PCH_PECI_R 0_0402_5% R237	H_PECI <6,42>
P5	RCIN#	KBRST#	KBRST# <42>
AY11	PROCPWRGD		H_CPUPWRGD <6>
AY10	THRMTRIP#	PCH_THRMTRIP#_R R239 390_0402_5% H_THRMTRIP#	H_THRMTRIP# <6>
T14	INIT3_3V#		PCH_THRMTRIP#_R <23>
AY1	DF_TVS	NV_CLE	
AH8	TS_VSS1		
AK11	TS_VSS2		
AH10	TS_VSS3		
AK10	TS_VSS4		
P37	NC_1		

CPU/MISC

+3VS R236 10K_0402_5%

INIT3_3V
This signal has weak internal PU, can't pull low

Intel schematic reviwe recommand.

PCH_GPIO68 R255 10K_0402_5%
KBRST# R226 10K_0402_5%

A4	VSS_NCTF_1	VSS_NCTF_15	BG2
A44	VSS_NCTF_2	VSS_NCTF_16	BG48
A45	VSS_NCTF_3	VSS_NCTF_17	BH3
A46	VSS_NCTF_4	VSS_NCTF_18	BH47
A5	VSS_NCTF_5	VSS_NCTF_19	BJ4
A6	VSS_NCTF_6	VSS_NCTF_20	BJ44
B3	VSS_NCTF_7	VSS_NCTF_21	BJ45
B47	VSS_NCTF_8	VSS_NCTF_22	BJ46
BD1	VSS_NCTF_9	VSS_NCTF_23	BJ5
BD49	VSS_NCTF_10	VSS_NCTF_24	BJ6
BE1	VSS_NCTF_11	VSS_NCTF_25	C2
BE49	VSS_NCTF_12	VSS_NCTF_26	C48
BF1	VSS_NCTF_13	VSS_NCTF_27	D1
BF49	VSS_NCTF_14	VSS_NCTF_28	D49
		VSS_NCTF_29	E1
		VSS_NCTF_30	E49
		VSS_NCTF_31	F1
		VSS_NCTF_32	F49

NCTF

PANTHER-POINT_FCBGA989

PROC_SEL	H : Sandy Bridge
	L : INV Bridge

+1.8VS R216 2.2K_0402_5%

NV_CLE R217 1K_0402_5% H_SNB_IVB# <6>

CLOSE TO THE BRANCHING POINT

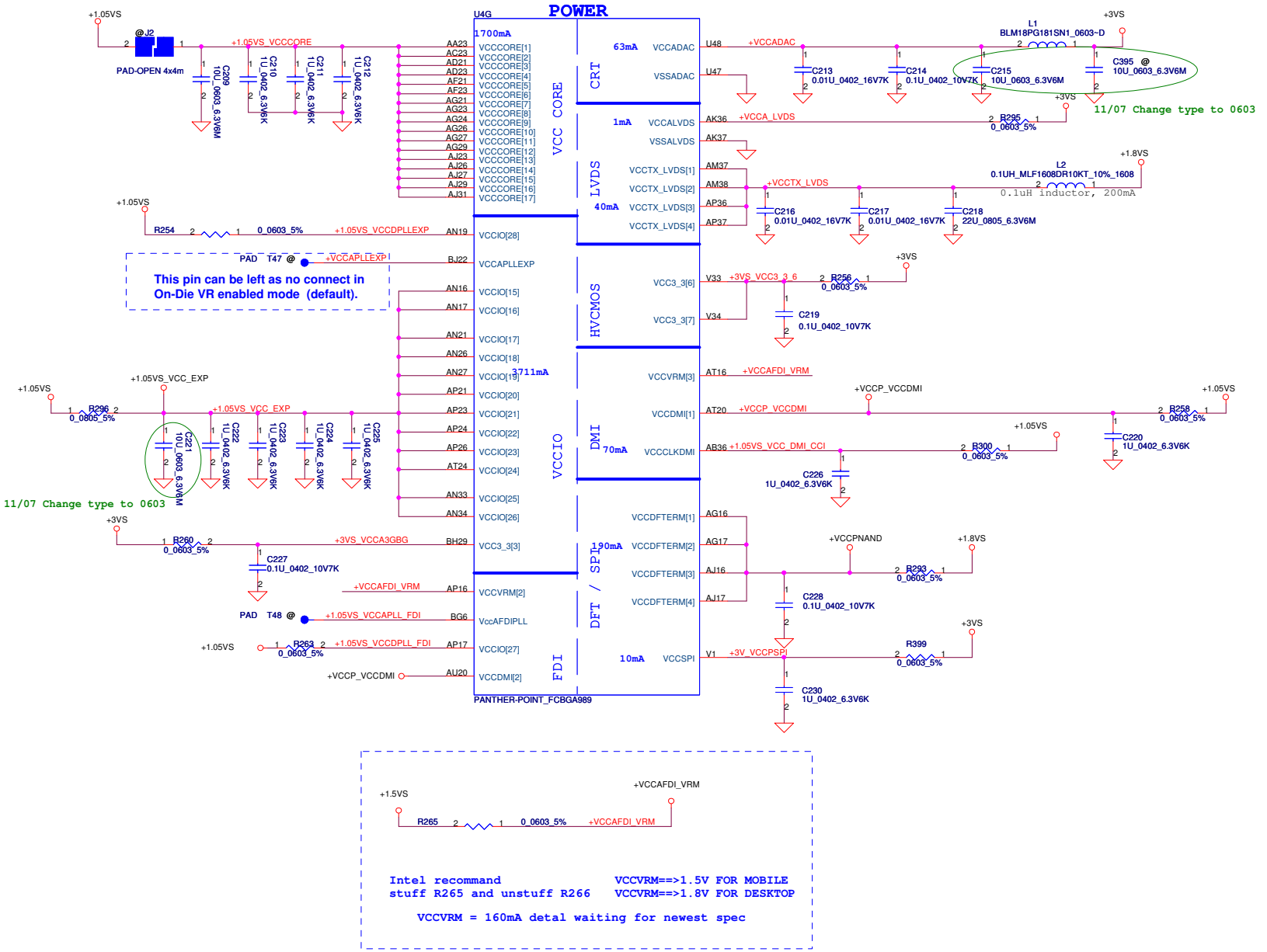
Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size	Document Number	Rev
Custom	QIWY4 LA-8002P	1.0

Date: Monday, January 16, 2012 Sheet 19 of 64



PCH Power Rail Table
Refer to CPU EDS R1.5

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.05	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.095
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: QIWY4 LA-8002P | Rev: 1.0

Date: Monday, January 16, 2012 | Sheet 20 of 64

Have internal VRM

VCC3_3 = 266mA detal waiting for newest spec

VCCDMI = 42mA detal waiting for newest spec

POWER

U4J

PANTHER-POINT_FCBGA989

Clock and Miscellaneous

USB

PCI/GPIO/LPC

SATA

CPU

MISC

RTC

SUSPWR

On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL,VCCAPLLEXP,VCCAPLLDMI2
,VCCAPLLSATA

11/07 Change type to 0603

For Deep S3

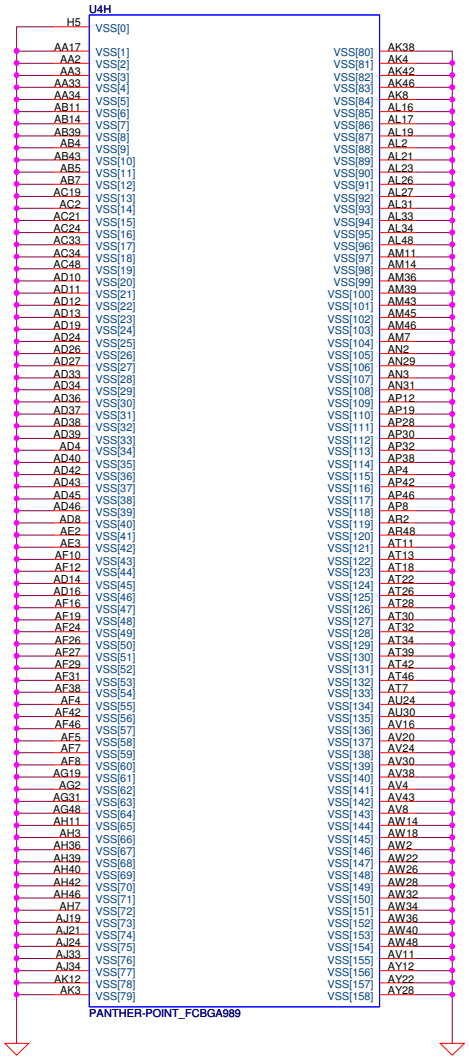
Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

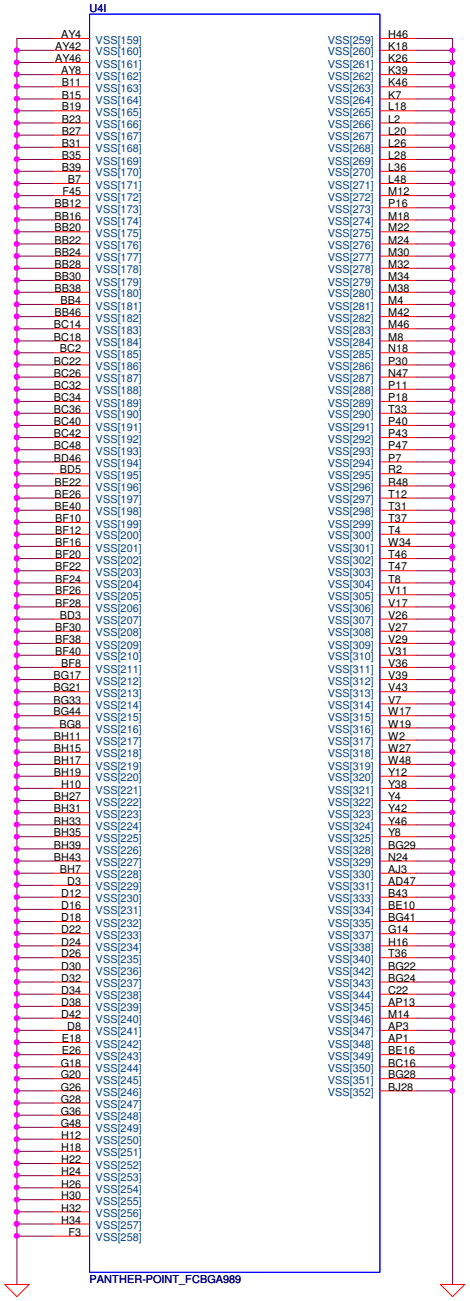
Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size: Custom | Document Number: QIWY4 LA-8002P | Rev: 1.0

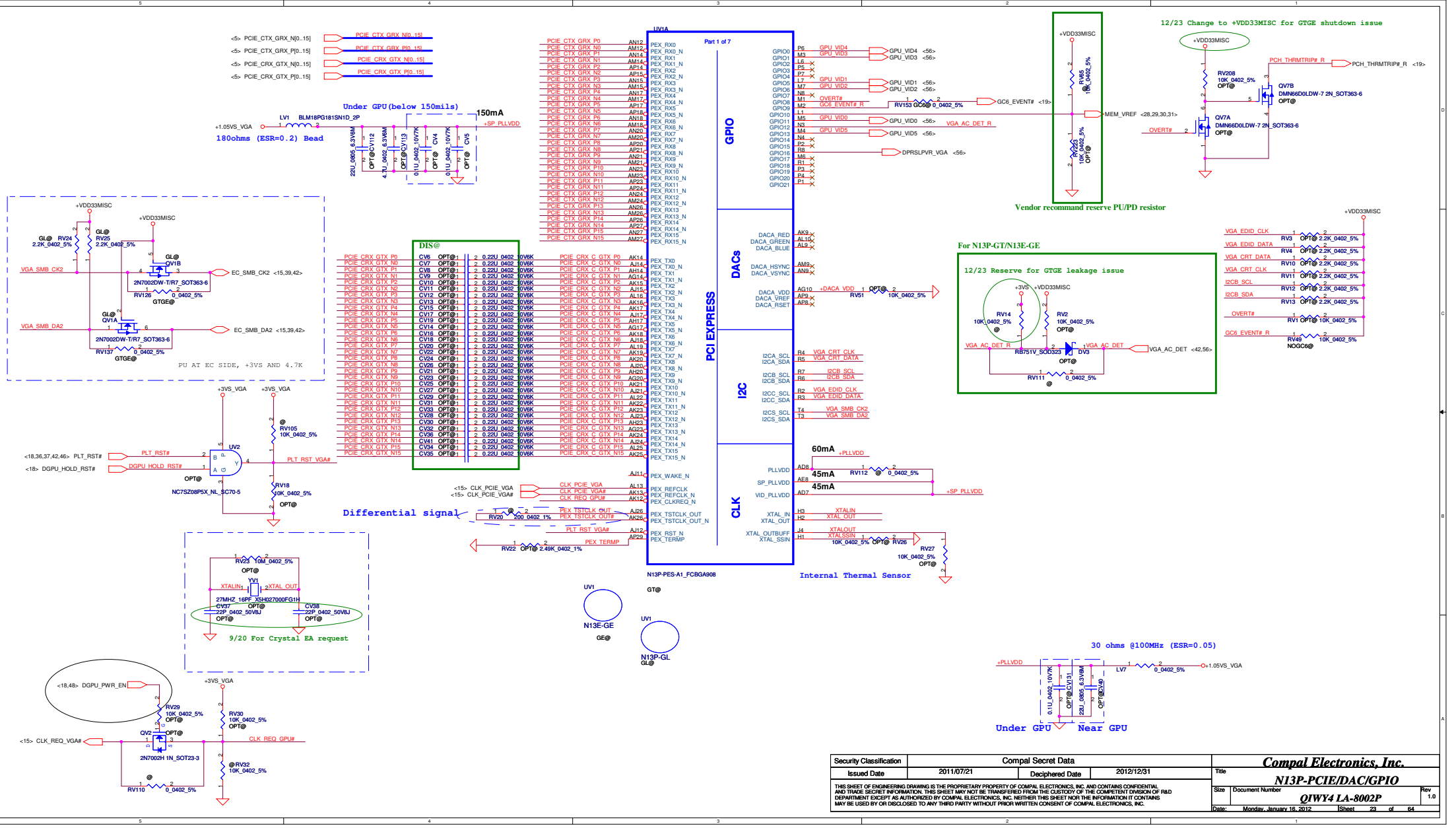
Date: Monday, January 16, 2012 | Sheet 21 of 64





Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title	PCH (9/9) VSS		
Size: Custom	Document Number: QIWY4 LA-8002P		Rev: 1.0
Date: Monday, January 16, 2012	Sheet 22 of 64		



Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

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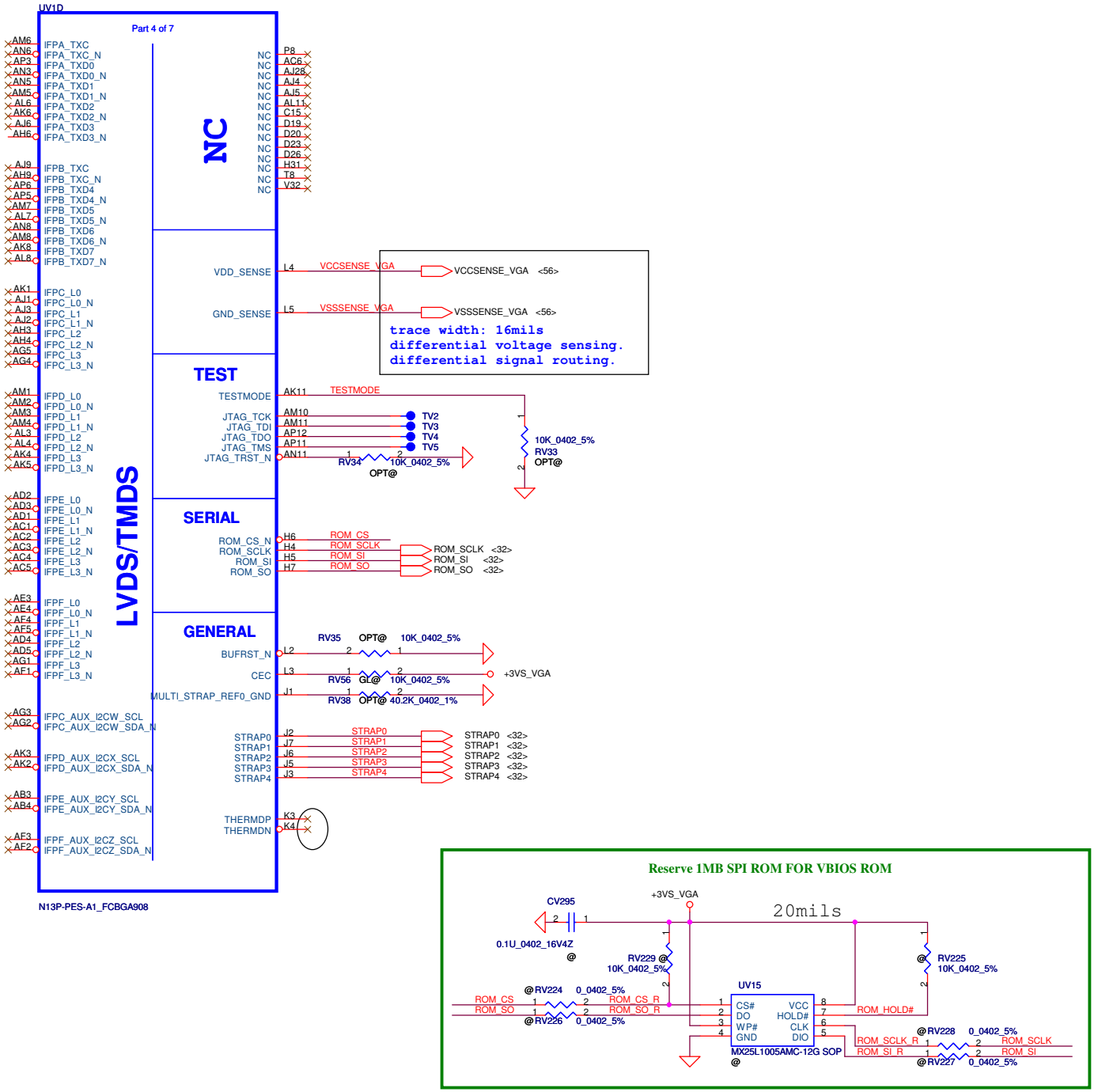
Compal Electronics, Inc.

Title: N13P-PCIE/DAC/GPIO

Size	Document Number	Rev
	QIWY4 LA-8002P	1.0

Date: Monday, January 16, 2012 Sheet 23 of 64



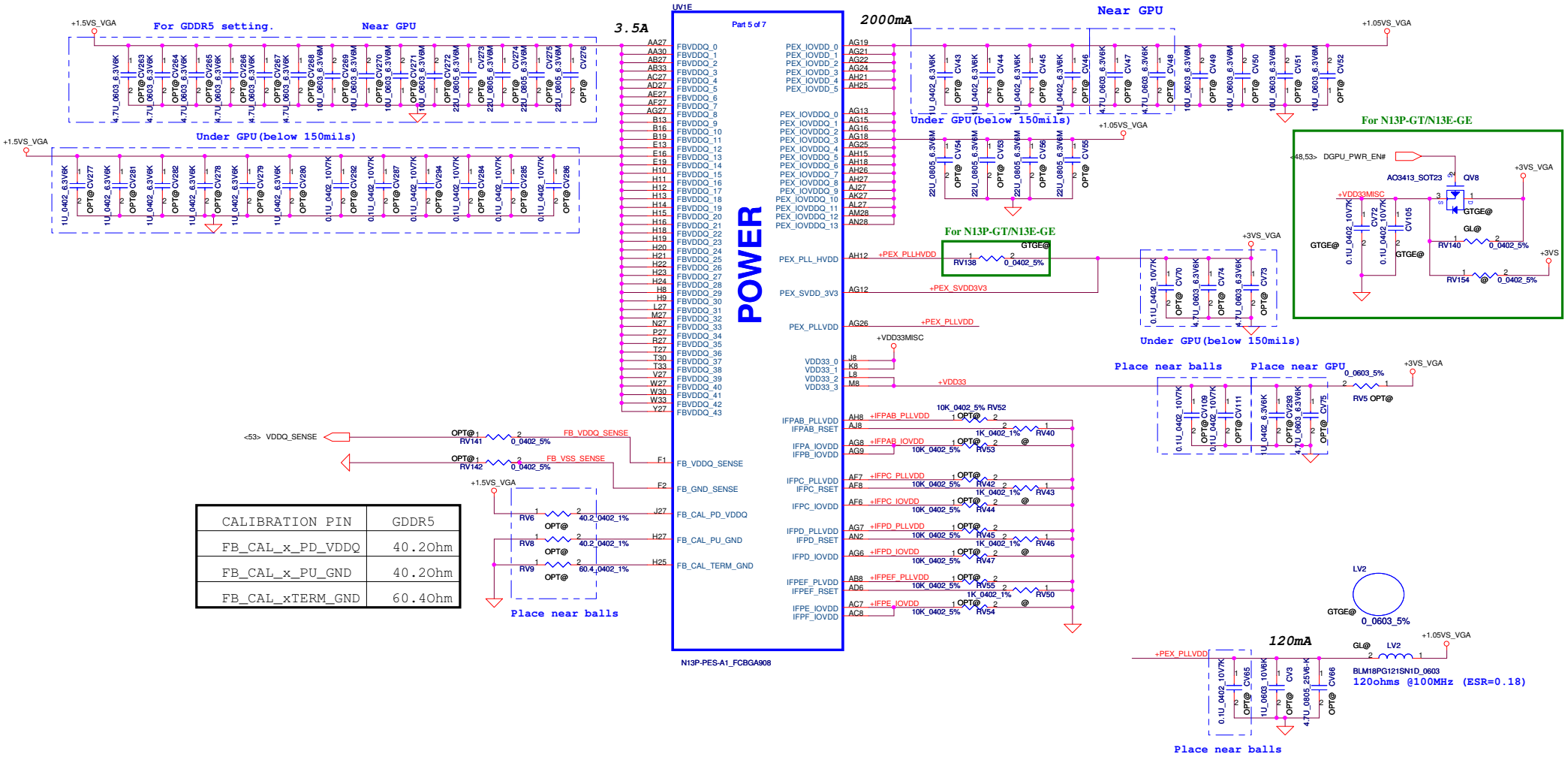
Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **N13P-LVDS/HDMI/DP/THM**

Size	Document Number	Rev
	QIWY4 LA-8002P	1.0

Date: Monday, January 16, 2012 | Sheet 24 of 64



CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	40.2Ohm
FB_CAL_xTERM_GND	60.4Ohm

Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: N13P-POWER

Size	Document Number	Rev
	QIWY4 LA-8002P	1.0

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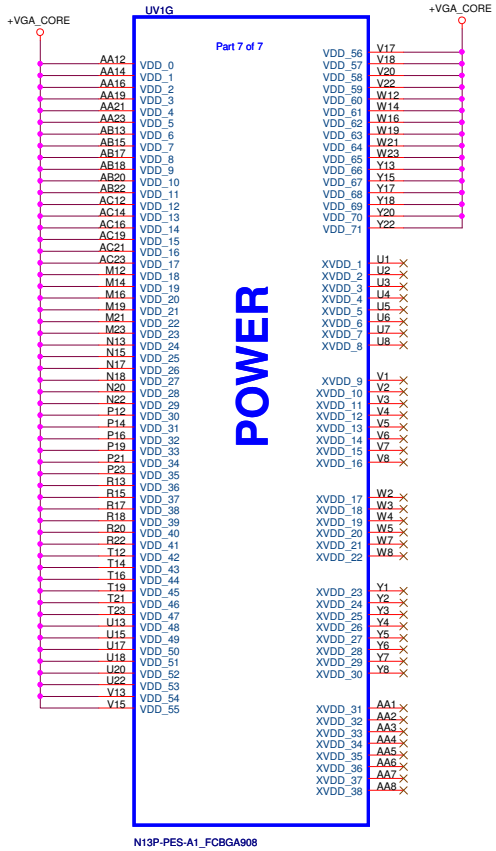
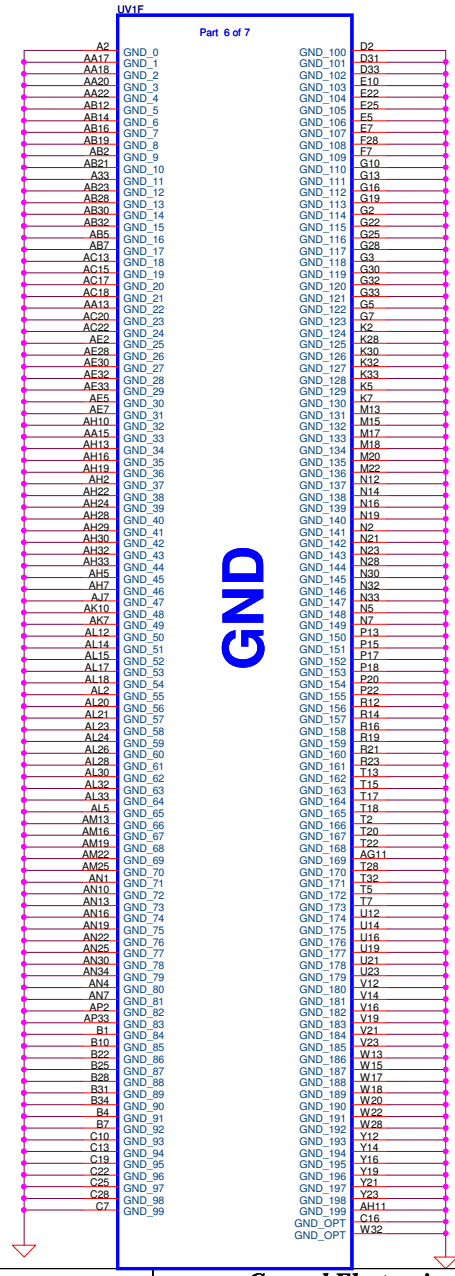




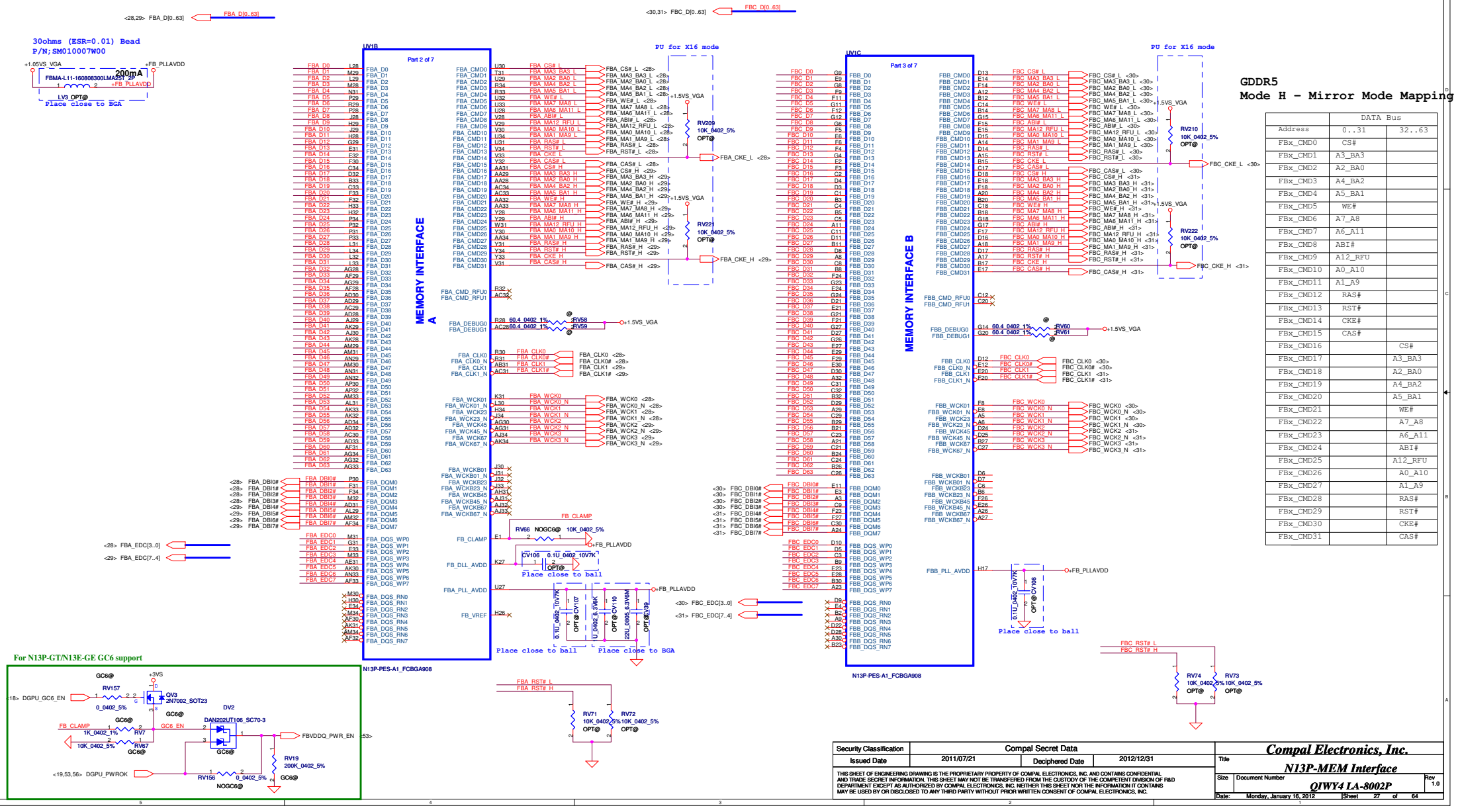
Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: N13P-VGA CORE, GND

Size	Document Number	Rev
	QIWY4 LA-8002P	1.0

Date: Monday, January 16, 2012 | Sheet 26 of 64



	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: N13P-MEM Interface

Size: | Document Number: QIWY4 LA-8002P | Rev: 1.0

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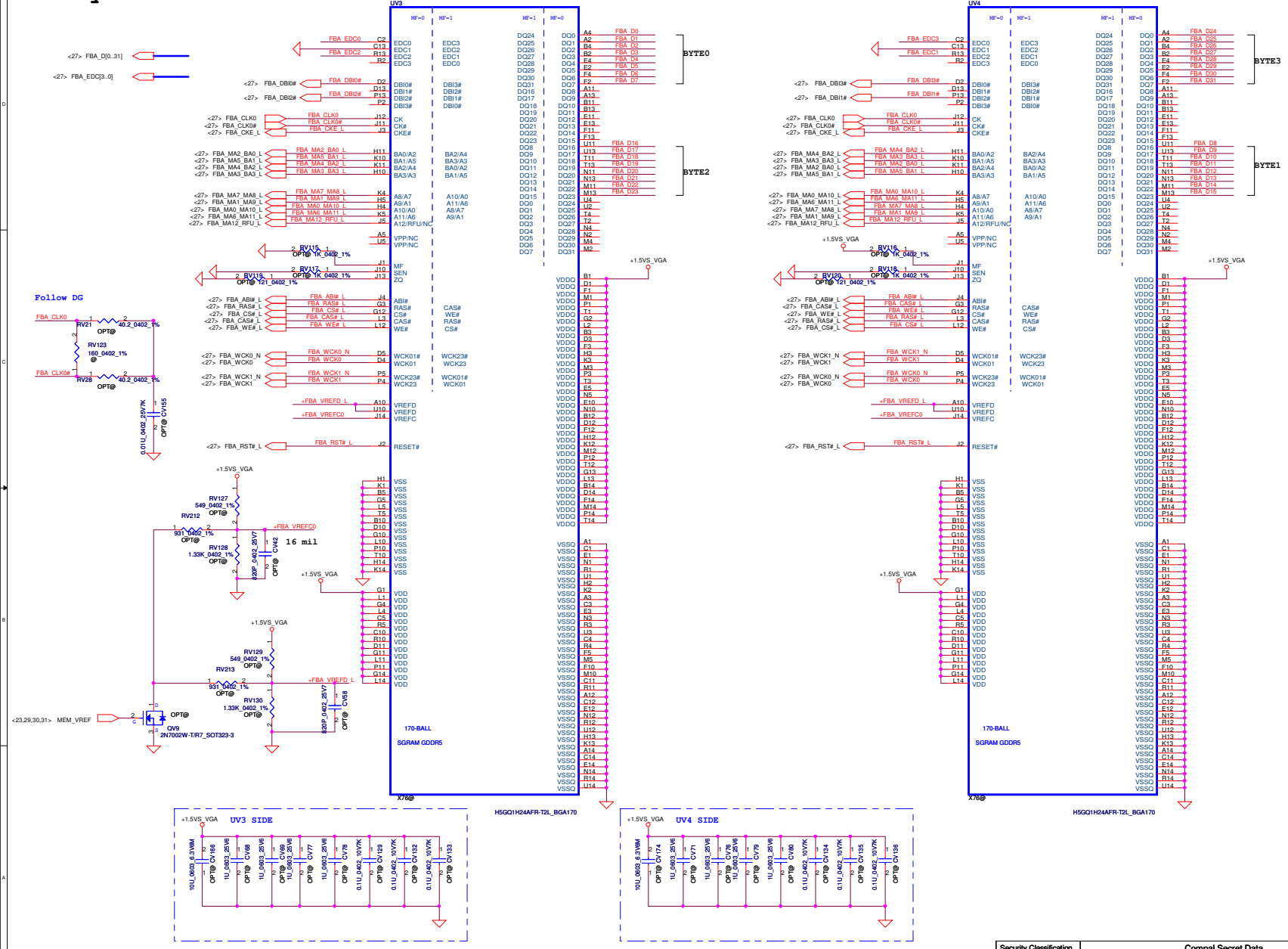
Memory Partition A - Lower 32 bits



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: N13P-VRAM A Lower

Size	Document Number	Rev
	QIWY4 LA-8002P	1.0

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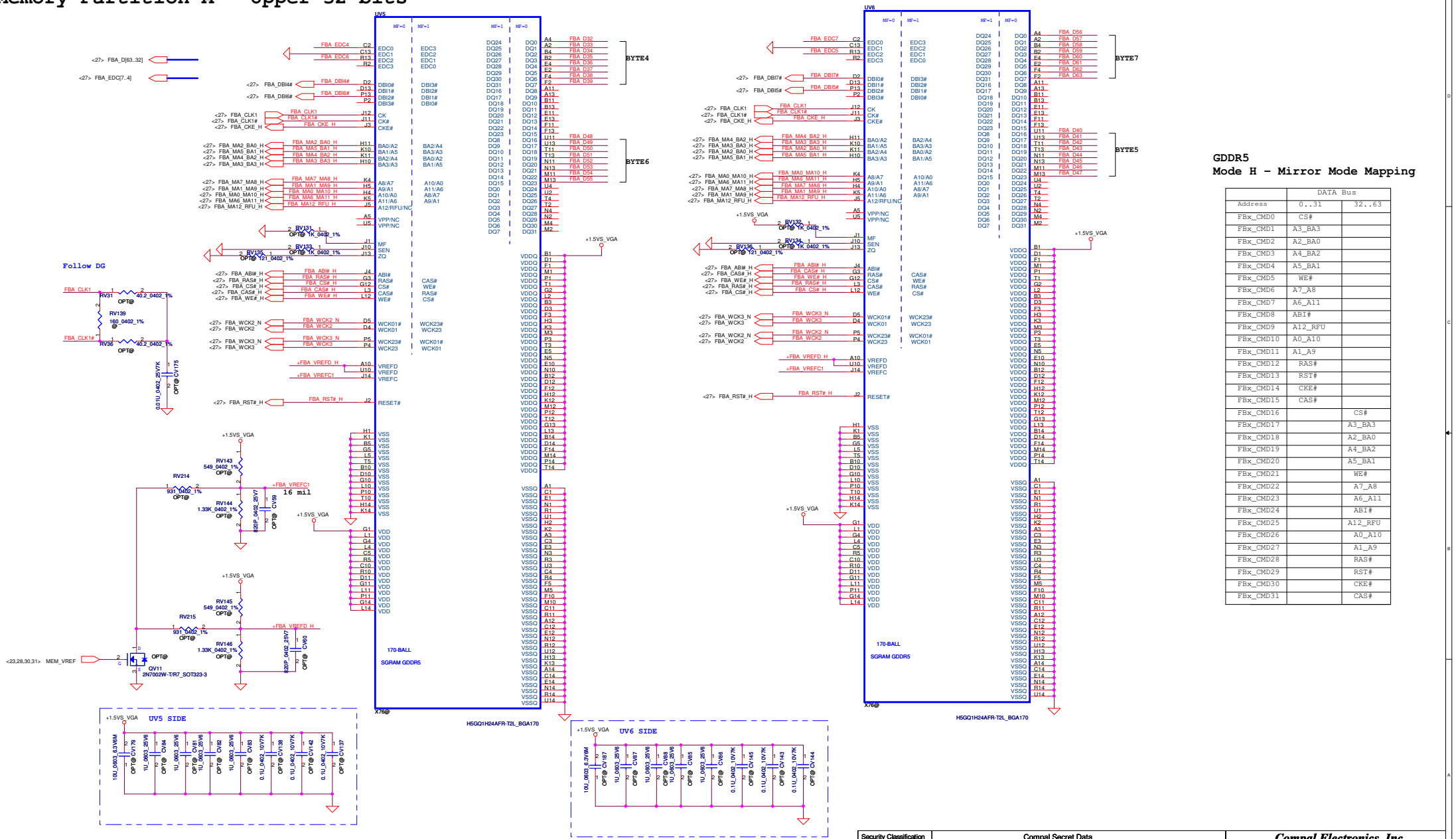
Memory Partition A - Upper 32 bits



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Compal Electronics, Inc.

Title: N13P-VRAM A Upper

Size: | Document Number: QIWY4 LA-8002P | Rev: 1.0

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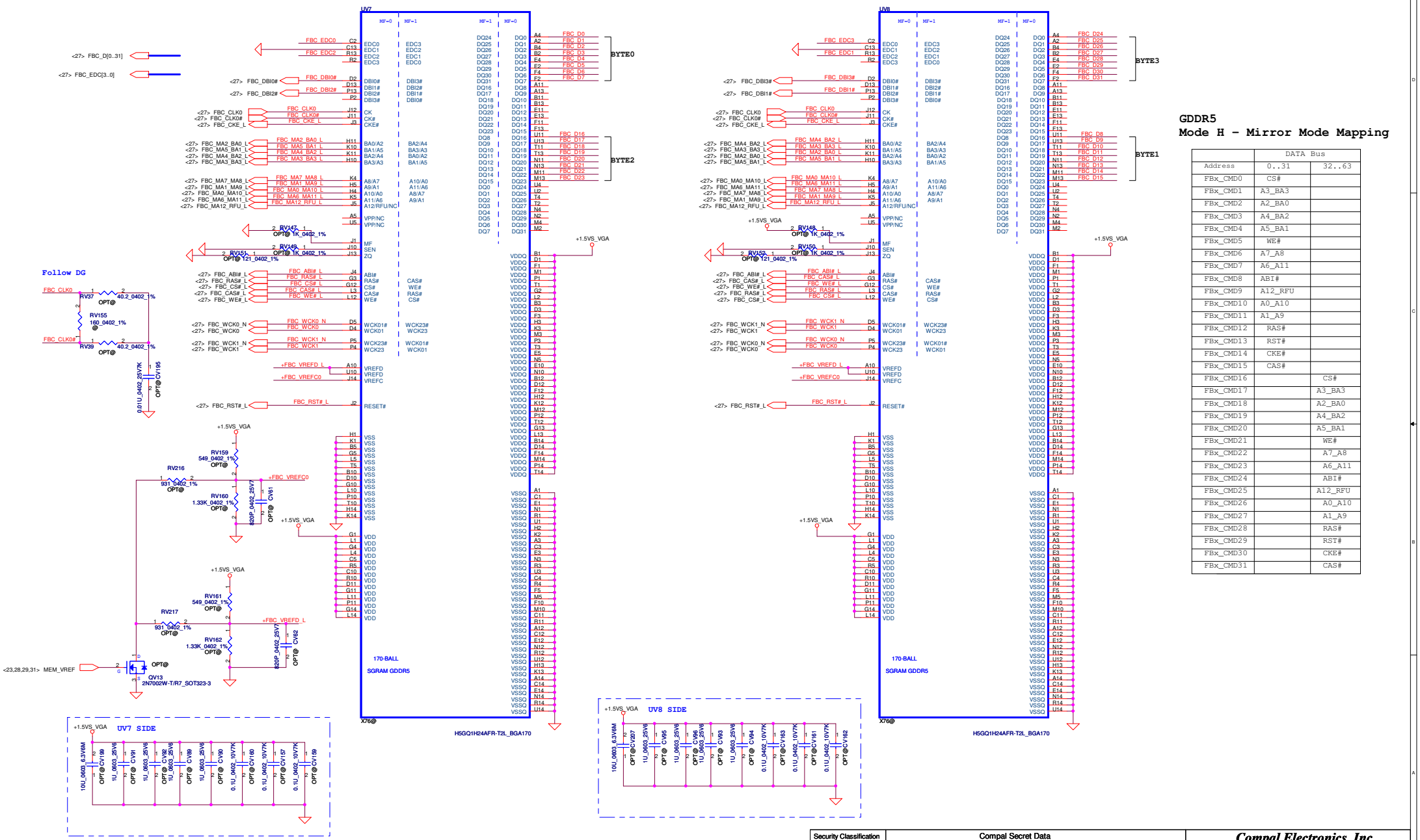
Memory Partition C - Lower 32 bits



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: *NI3P-VRAM C Lower*

Size: Custom | Document Number: *QIWY4 LA-8002P* | Rev: 1.0

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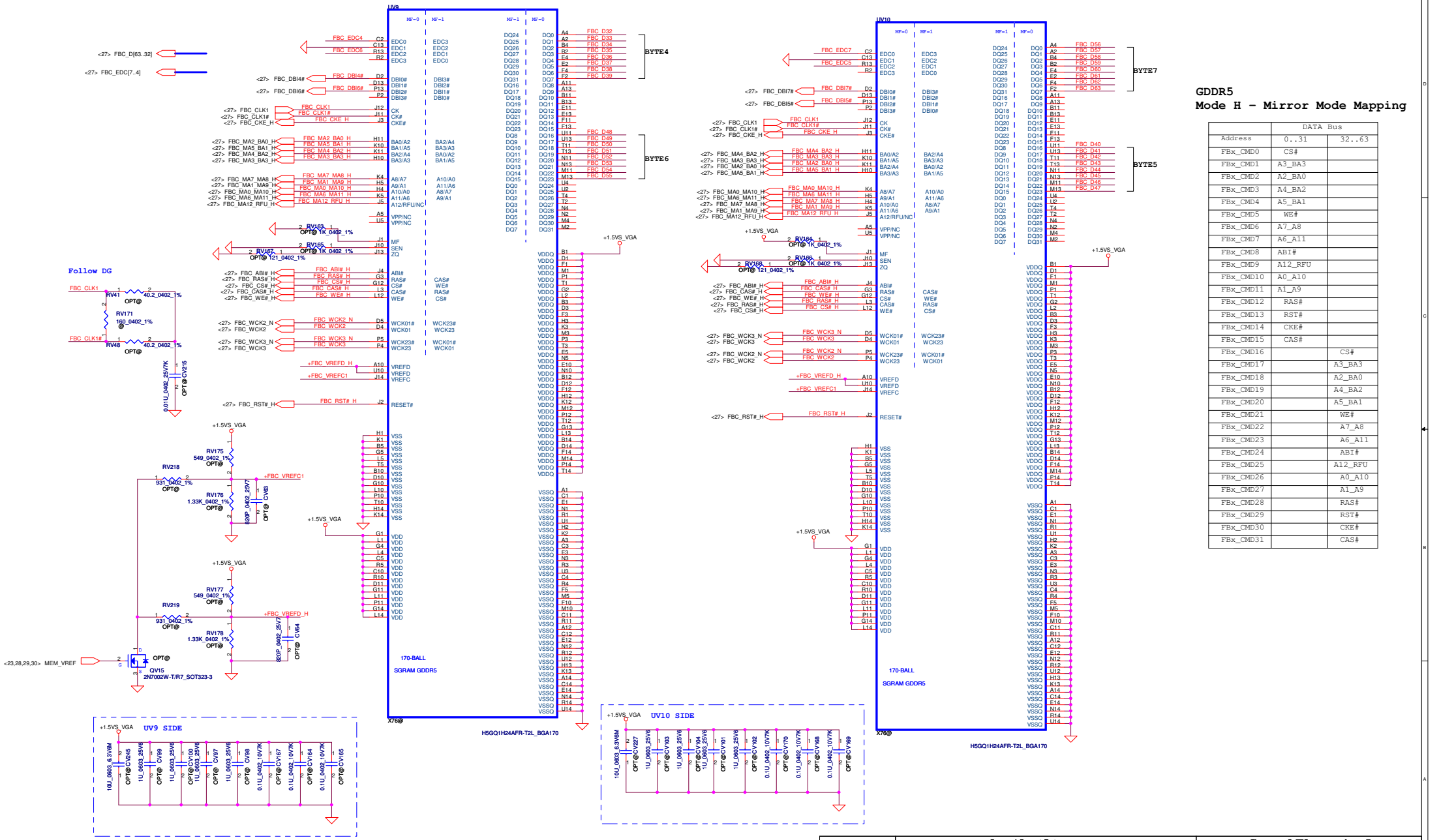
Memory Partition C – Upper 32 bits



GDDR5
Mode H – Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

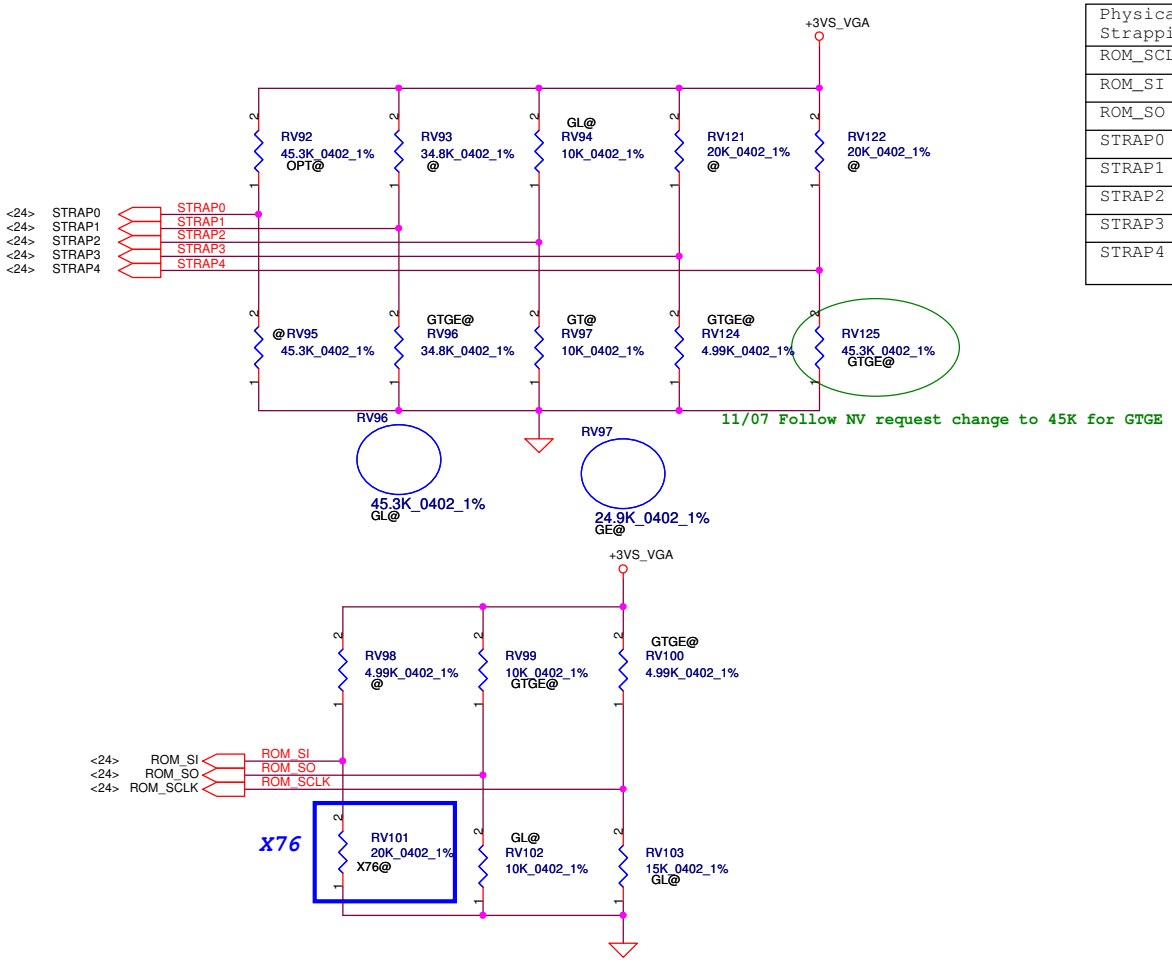
Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: *N13P-VRAM C Upper*

Size: Custom | Document Number: *QIWY4 LA-8002P* | Rev: 1.0

Date: Monday, January 16, 2012 | Sheet 31 of 64



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

XCLK_417	
0	277MHz (Default)
1	Reserved

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

USER Straps	
User[3:0]	
1000-1100	Customer defined

FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

PCIE_MAX_SPEED	
0	Limit to PCIE Gen1
1	PCIE Gen 2/3 Capable

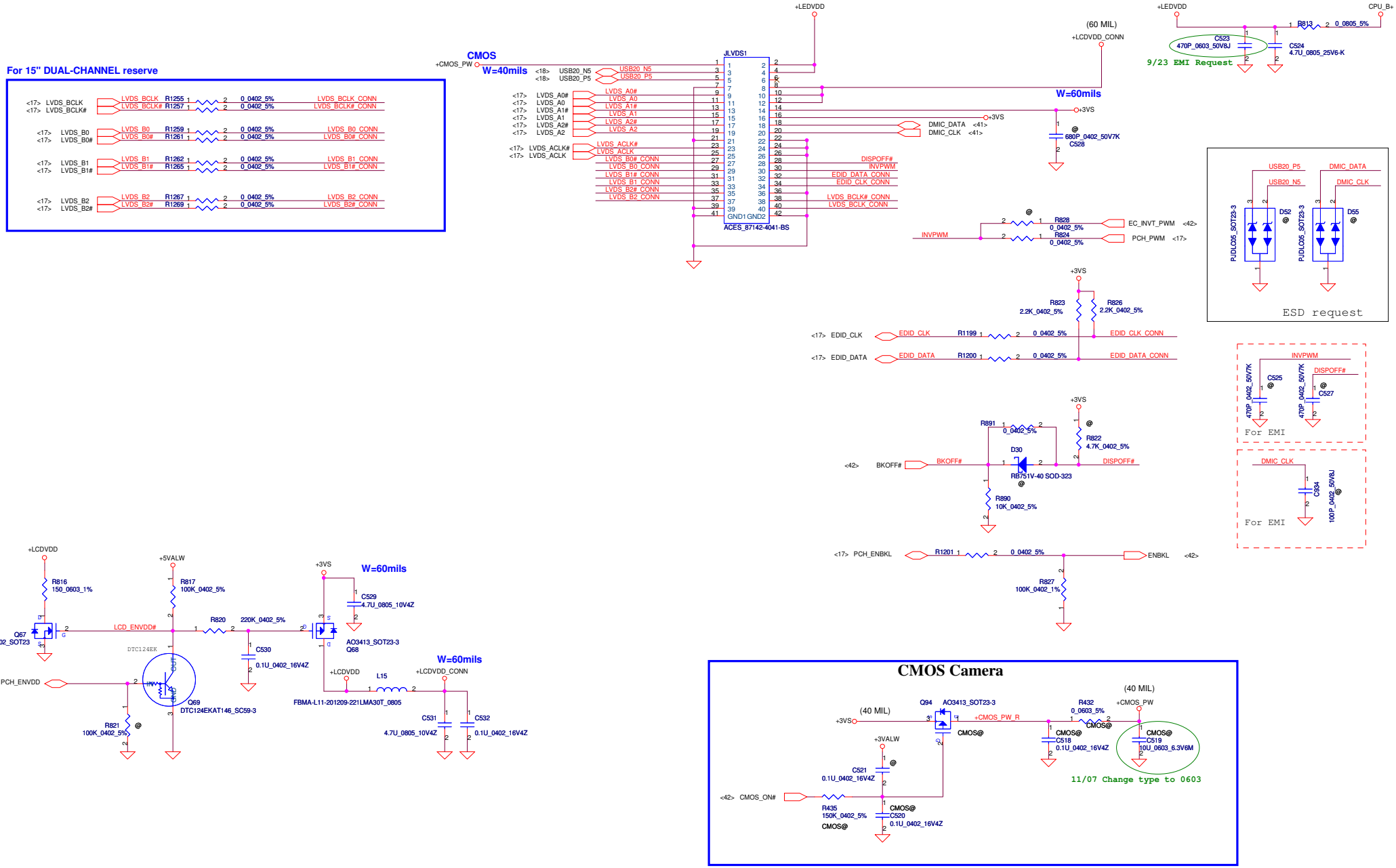
Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: N13P_MISC

Size: Custom | Document Number: QIWY4 LA-8002P | Rev: 1.0

Date: Monday, January 16, 2012 | Sheet 32 of 64



Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **LVDS/CAMERA**

Size	Document Number	Rev
Custom	QIWY4 LA-8002P	1.0

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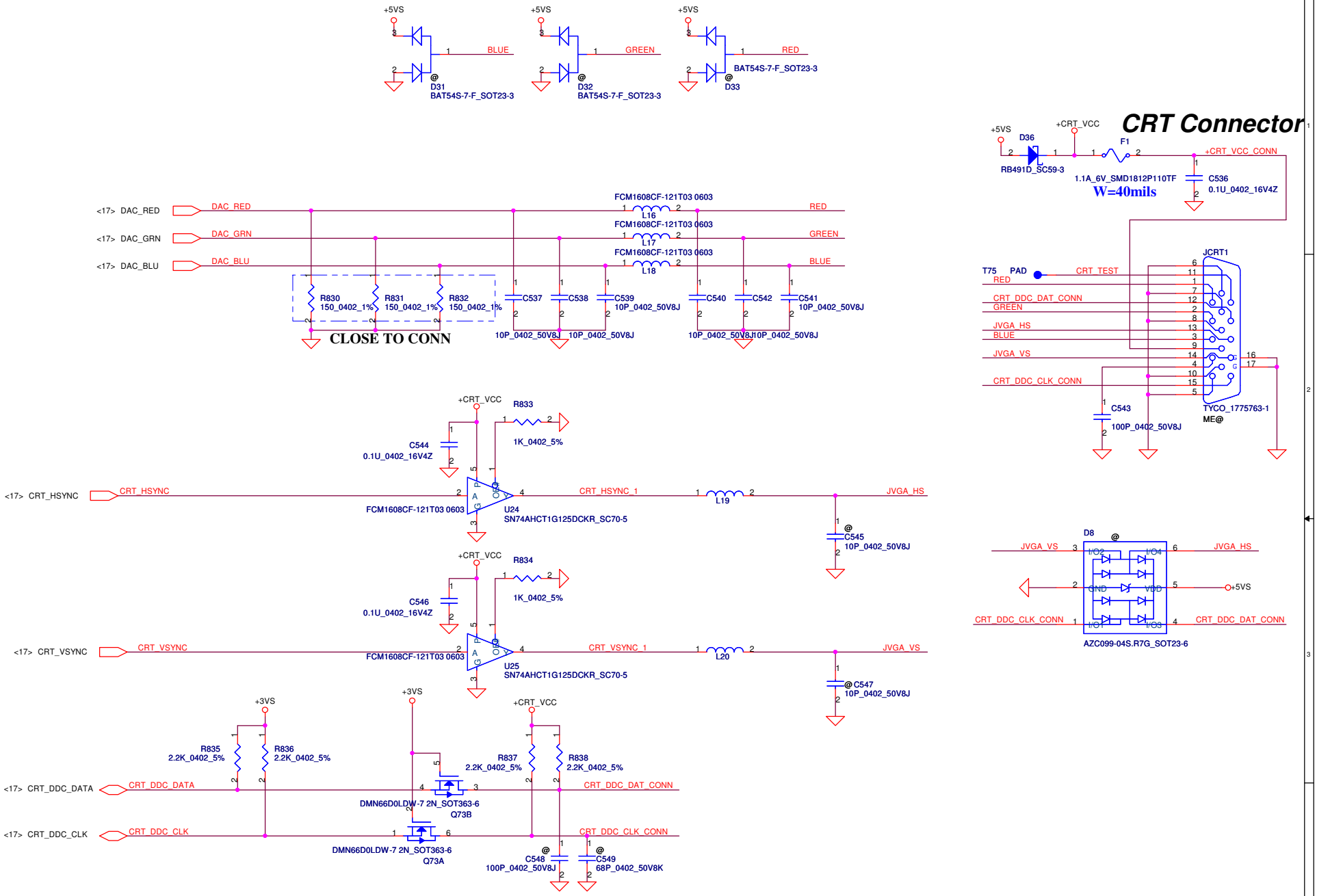

Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: CRT Connector

Size	Document Number	Rev
Custom	QIWY4 LA-8002P	1.0

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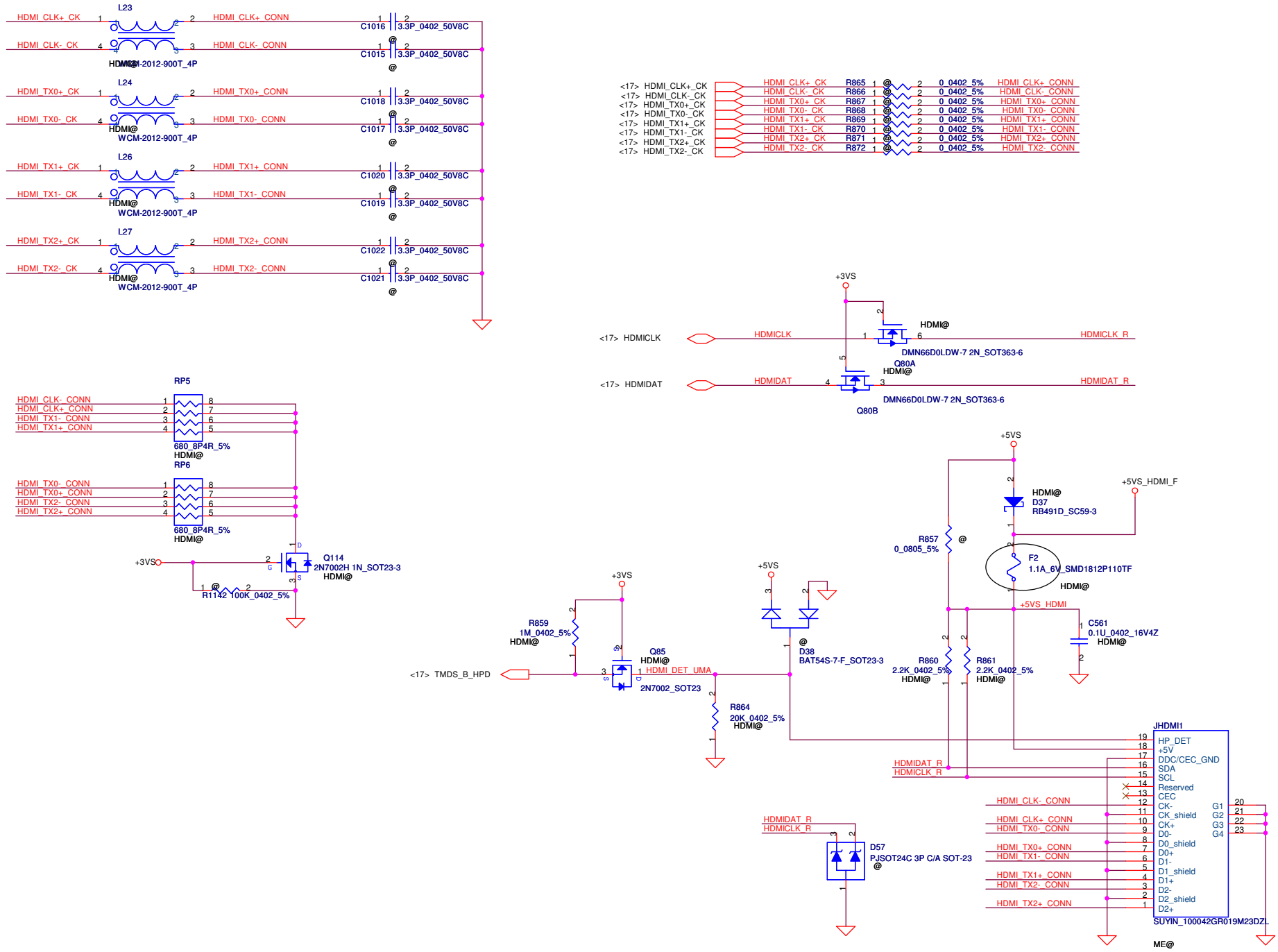

Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics,Ltd.

Title: **HDMI CONN**

Size	Document Number	Rev
Custom	QIWY4 LA-8002P	1.0

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Mini-Express Card for WLAN/WiMAX(Half)
Mini-Express Card for SSD(Full)

Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LPC_FRAME# R	R873	@	0 0402 5%	LPC_FRAME#	LPC_FRAME# <14,42>
LPC_AD3 R	R874	@	0 0402 5%	LPC_AD3	LPC_AD3 <14,42>
LPC_AD2 R	R875	@	0 0402 5%	LPC_AD2	LPC_AD2 <14,42>
LPC_AD1 R	R876	@	0 0402 5%	LPC_AD1	LPC_AD1 <14,42>
LPC_AD0 R	R878	@	0 0402 5%	LPC_AD0	LPC_AD0 <14,42>
PCI_RST# R	R879	@	0 0402 5%	PLT_RST#	
CLK_PCI_DB					CLK_PCI_DB <18>

+3VS +3VS_WLAN
J3 JUMP_43X79 @
C563 0.1U_0402_16V4Z
@ C570 10U_0603_6.3V6M
11/08 Reserve

9/18 JP1 Pin2,24,52 contact to +3VS_WLAN for AOAC function

Mini-Express Card(WLAN/WiMAX)

+3VS_WLAN_AOAC
R289 0_0603_5%
+1.5VS
C564 0.1U_0402_16V4Z
C565 0.1U_0402_16V4Z

<19,44> PCH_BT_ON#
R892 @ 1 2 0_0402_5%
<19> BT_DISABLE
R897 1 2 0_0402_5%
<16,19,37> PCIE_WAKE#
<44> BT_ACTIVE
R877 1 2 @0_0402_5%
PCIE_WAKE#
BT_ACTIVE
BT_DISABLE_R
<15> WLAN_CLKREQ1#
WLAN_CLKREQ1#

JP1
WAKE# 3.3V
NC GND
NC 1.5V
CLKREQ# NC
GND NC
REFCLK- NC
REFCLK+ NC
GND NC
NC GND
NC GND
GND PERST#
PERn0 +3.3Vaux
PERp0 GND
GND +1.5V
GND SMB_CLK
PETn0 SMB_DATA
PETp0 GND
GND USB_D-
NC USB_D+
GND
NC LED_WWAN#
NC LED_WLAN#
NC LED_WPAN#
NC +1.5V
NC GND
NC +3.3V
GND GND

+1.5VS_WLAN
LPC_FRAME# R
LPC_AD3 R
LPC_AD2 R
LPC_AD1 R
LPC_AD0 R

<15> CLK_PCIE_WLAN1#
<15> CLK_PCIE_WLAN1
PCI_RST# R
CLK_PCI_DB
<15> PCIE_PRX_DTX_N2
<15> PCIE_PRX_DTX_P2
<15> PCIE_PTX_C_DRX_N2
<15> PCIE_PTX_C_DRX_P2
+3VS_WLAN
100_0402_1% R887
<42,43> EC_TX EC_TX
<42,43> EC_RX EC_RX
R888 100_0402_1%
For EC to detect debug card insert.
R889 100K_0402_5%
TAITW_PFPET0-AFGLBG1ZZ4N0
ME@

R880 1 2 0_0402_5% WL_RST# PCH_WL_OFF# <18>
R881 1 2 @0_0402_5% +3VALW
R882 1 2 0_0402_5% +3VS_WLAN_AOAC
R883 1 2 @0_0402_5% SMB_CLK_S3 <12,13,15>
R884 1 2 @0_0402_5% SMB_DATA_S3 <12,13,15>
USB20_N10 <18>
USB20_P10 <18>
2 1 PLT_RST# R1343 PLT_RST# <18,23,37,42,46>

+3VS_WLAN +3VS_WLAN_AOAC
R267 2 1 0_0603_5%
+3VALW
Q104 AO3413_SOT23-3
AOAC@
AOAC@ C533 0.1U_0402_16V4Z
<42> AOAC_ON#
R436 150K_0402_5% AOAC@
AOAC@ C526 0.1U_0402_16V4Z

9/18 Increase for Intel AOAC function

Mini-Express Card(SSD)

SSD Active:4.5W(1.5A)

+3VS_SSD
0.1U_0402_16V4Z C566
C567
C568
10U_0603_6.3V6M @ C569
0.01U_0402_25V7K
10U_0603_6.3V6M
11/07 Change type to 0603

+3VS +3VS_SSD
J5 JUMP_43X79 @

JP3
WAKE# 3.3V
NC GND
NC 1.5V
CLKREQ# NC
GND NC
REFCLK- NC
REFCLK+ NC
GND NC
NC GND
NC NC
GND PERST#
PERn0 +3.3Vaux
PERp0 GND
GND +1.5V
GND SMB_CLK
PETn0 SMB_DATA
PETp0 GND
GND USB_D-
NC USB_D+
NC GND
NC LED_WWAN#
NC LED_WLAN#
NC LED_WPAN#
NC +1.5V
NC GND
NC +3.3V
GND GND

0.01U_0402_16V7K
<14> SATA_DTX_C_IRX_P0 SATA_DTX_C_IRX_P0
<14> SATA_DTX_C_IRX_N0 SATA_DTX_C_IRX_N0
C572 SATA_DTX_IRX_P0
C573 SATA_DTX_IRX_N0
0.01U_0402_16V7K
<14> SATA_ITX_DRX_N0 SATA_ITX_DRX_N0
<14> SATA_ITX_DRX_P0 SATA_ITX_DRX_P0
+3VS_SSD
<42,43> EC_TX EC_TX
<42,43> EC_RX EC_RX
R893 100_0402_1%
R894 100_0402_1%
<14> SATA_DET# SATA_DET#
For SSD use:
TAITW_PFPET0-AFGLBG1ZZ4N0
ME@

Mini-Express Card(TV)

+3VS_TV +1.5VS_TV

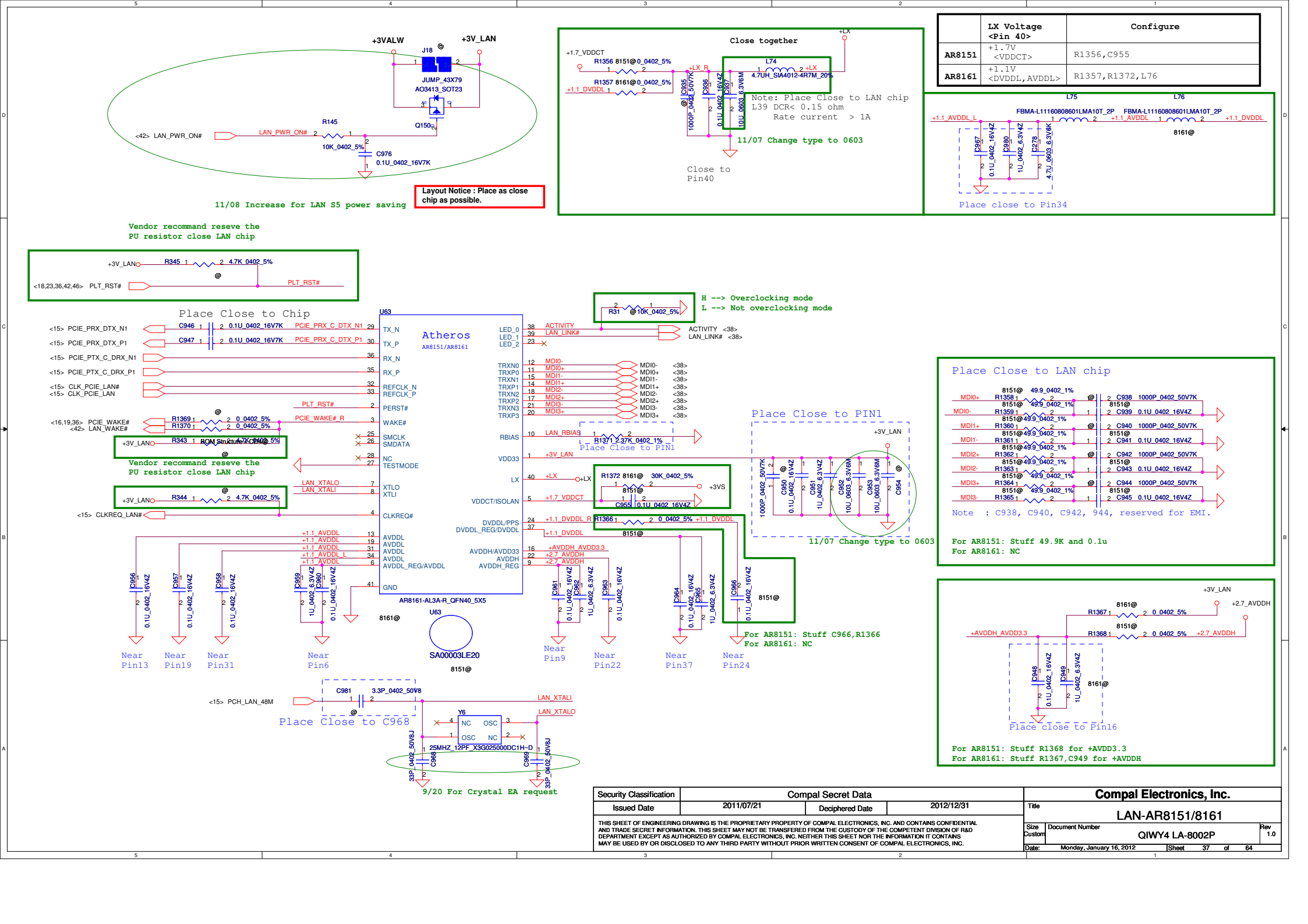
JP2
WAKE# 3.3V
NC GND
NC 1.5V
CLKREQ# NC
GND NC
REFCLK- NC
REFCLK+ NC
GND NC
NC GND
NC NC
GND PERST#
PERn0 +3.3Vaux
PERp0 GND
GND +1.5V
GND SMB_CLK
PETn0 SMB_DATA
PETp0 GND
GND USB_D-
NC USB_D+
NC GND
NC LED_WWAN#
NC LED_WLAN#
NC LED_WPAN#
NC +1.5V
NC +3.3V
GND GND

<15> CLKREQ_TV# CLKREQ_TV#
<15> CLK_PCIE_TV#
<15> CLK_PCIE_TV
<15> PCIE_PRX_DTX_N3
<15> PCIE_PRX_DTX_P3
<15> PCIE_PTX_C_DRX_N3
<15> PCIE_PTX_C_DRX_P3
+3VS_TV
@ 100_0402_1% R1209
<42,43> EC_TX EC_TX
<42,43> EC_RX EC_RX
R1208 @ 100_0402_1%
TAITW_PFPET0-AFGLBG1ZZ4N0
ME@

TV_RST# 0_0402_5% R1207 PLT_RST# <18,23,37,42,46>
USB20_N12 <18>
USB20_P12 <18>
+3VS_TV R1204 0_0805_5% +3VS
C902 4.7U_0805_10V4Z TV@
+1.5VS_TV R1206 0_0603_5% +1.5VS
C901 4.7U_0805_10V4Z TV@

Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.
Title: Mini-Card
Size: | Document Number: QIWY4 LA-8002P | Rev: 1.0
Date: Monday, January 16, 2012 | Sheet 36 of 64



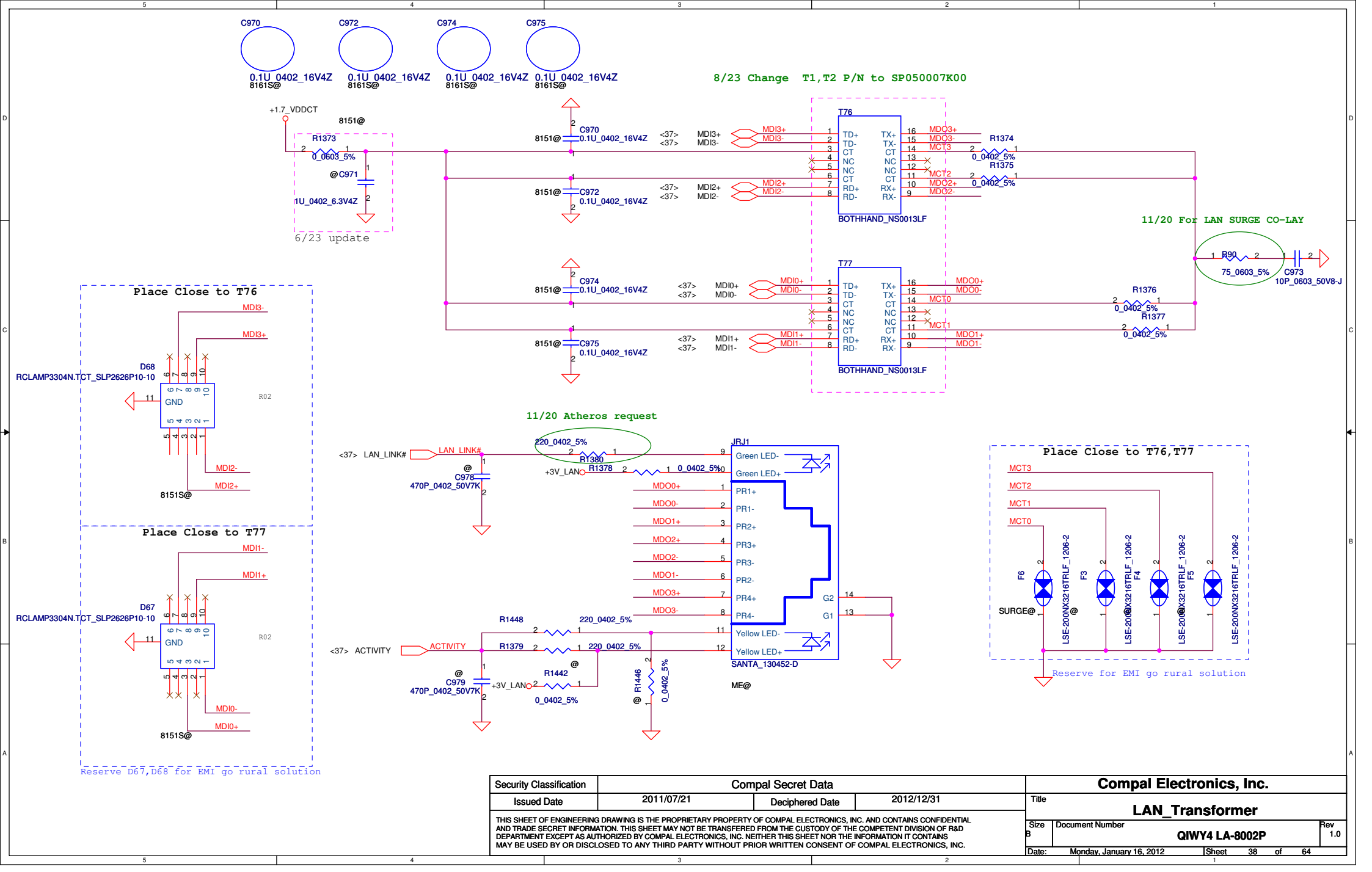
Security Classification	Compal Secret Data	
Issued Date	2011/07/21	Deciphered Date 2012/12/31

Compal Electronics, Inc.

Title: LAN-AR8151/8161

Size: Custom | Document Number: QIWY4 LA-8002P | Rev: 1.0

Date: Monday, January 16, 2012 | Sheet 37 of 64



Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

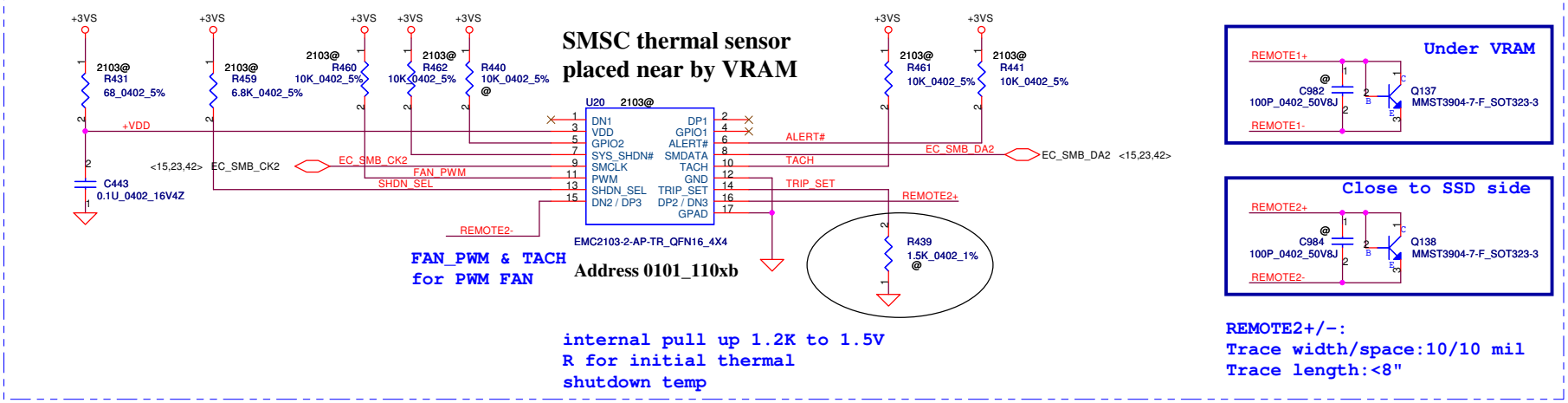
Title: **LAN_Transformer**

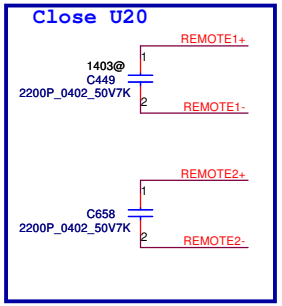
Size	Document Number	Rev
B	QIWY4 LA-8002P	1.0

Date: Monday, January 16, 2012 Sheet 38 of 64

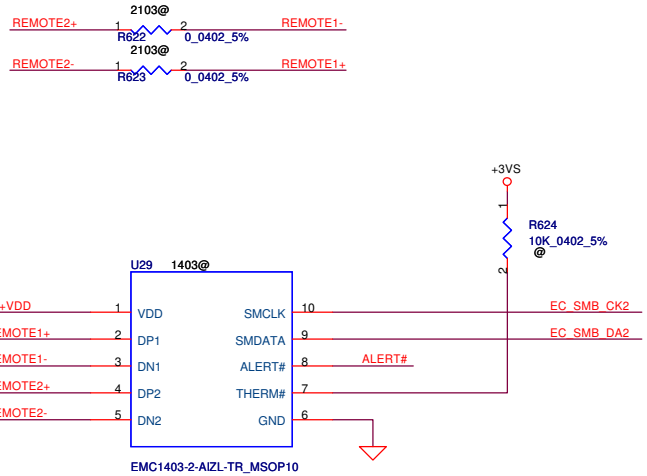
R431 1403@
0_0402_5%

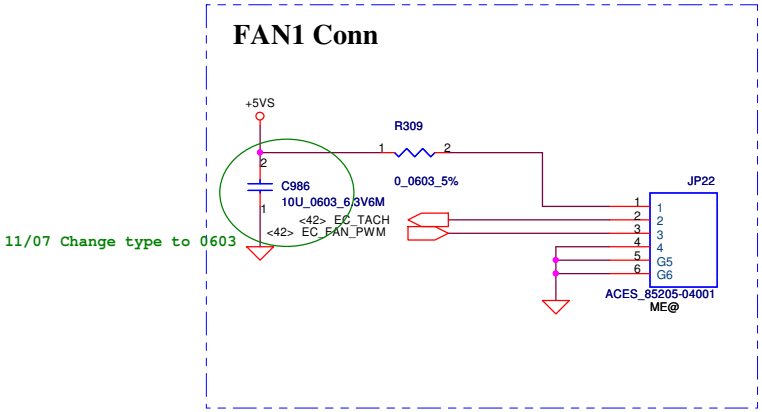
1403:
@C982/@C984=100p





Shutdown Temp	TRIP_SET R1387(1%)
93	953ohm
94	1020ohm
95	1100ohm
96	1150ohm
97	1240ohm
98	1330ohm
99	1400ohm
100	1500ohm
101	1580ohm
102	1690ohm
103	1820ohm
104	1960ohm
105	2050ohm





Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

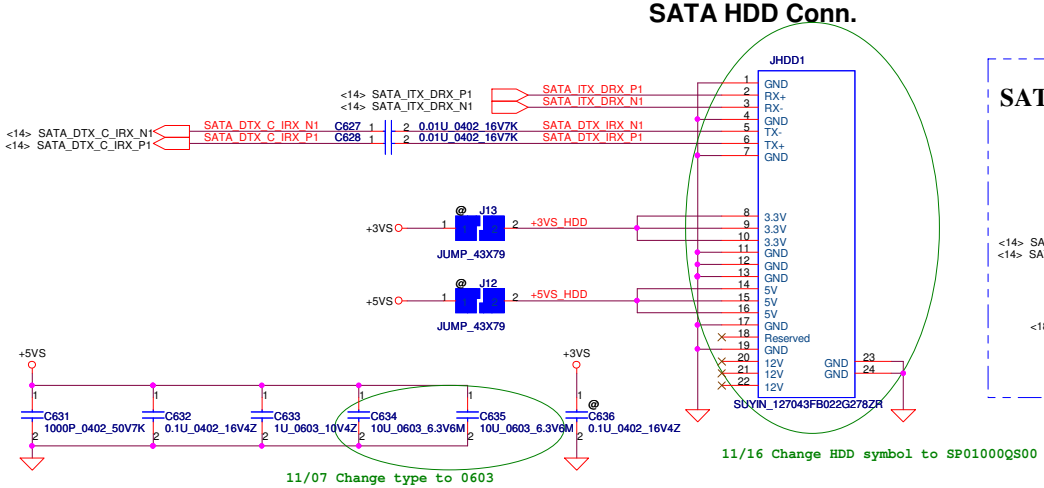
Compal Electronics,Ltd.

Title: EMC1403/2103_Thermal sensor/FAN

Size: Custom | Document Number: QIWY4 LA-8002P | Rev: 1.0

Date: Monday, January 16, 2012 | Sheet 39 of 64

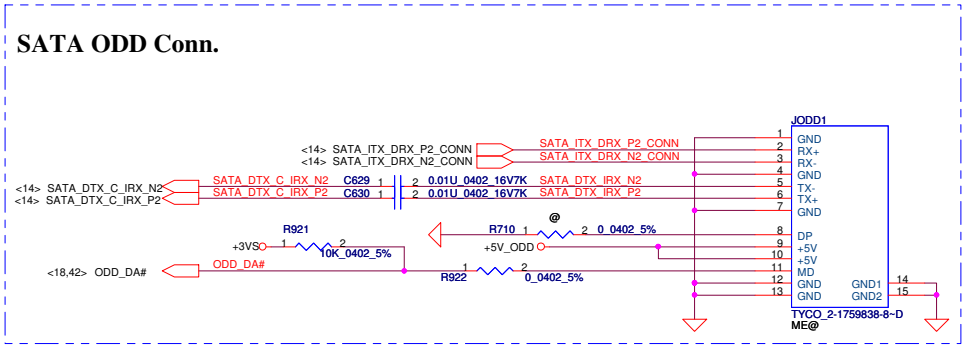
SATA HDD Conn.



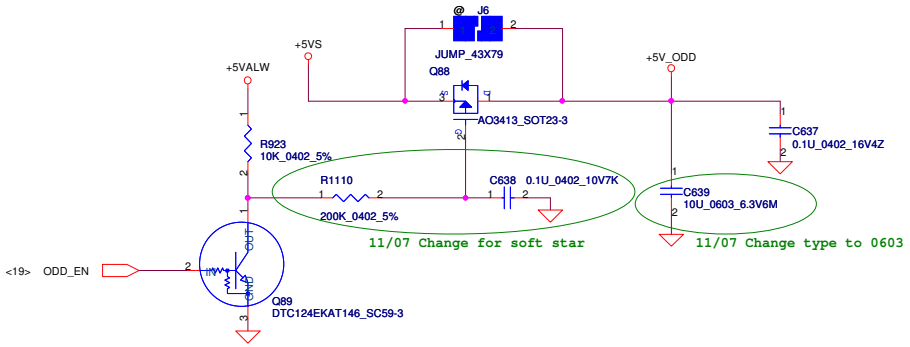
11/07 Change type to 0603

11/16 Change HDD symbol to SP01000QS00

SATA ODD Conn.



ODD Power Control

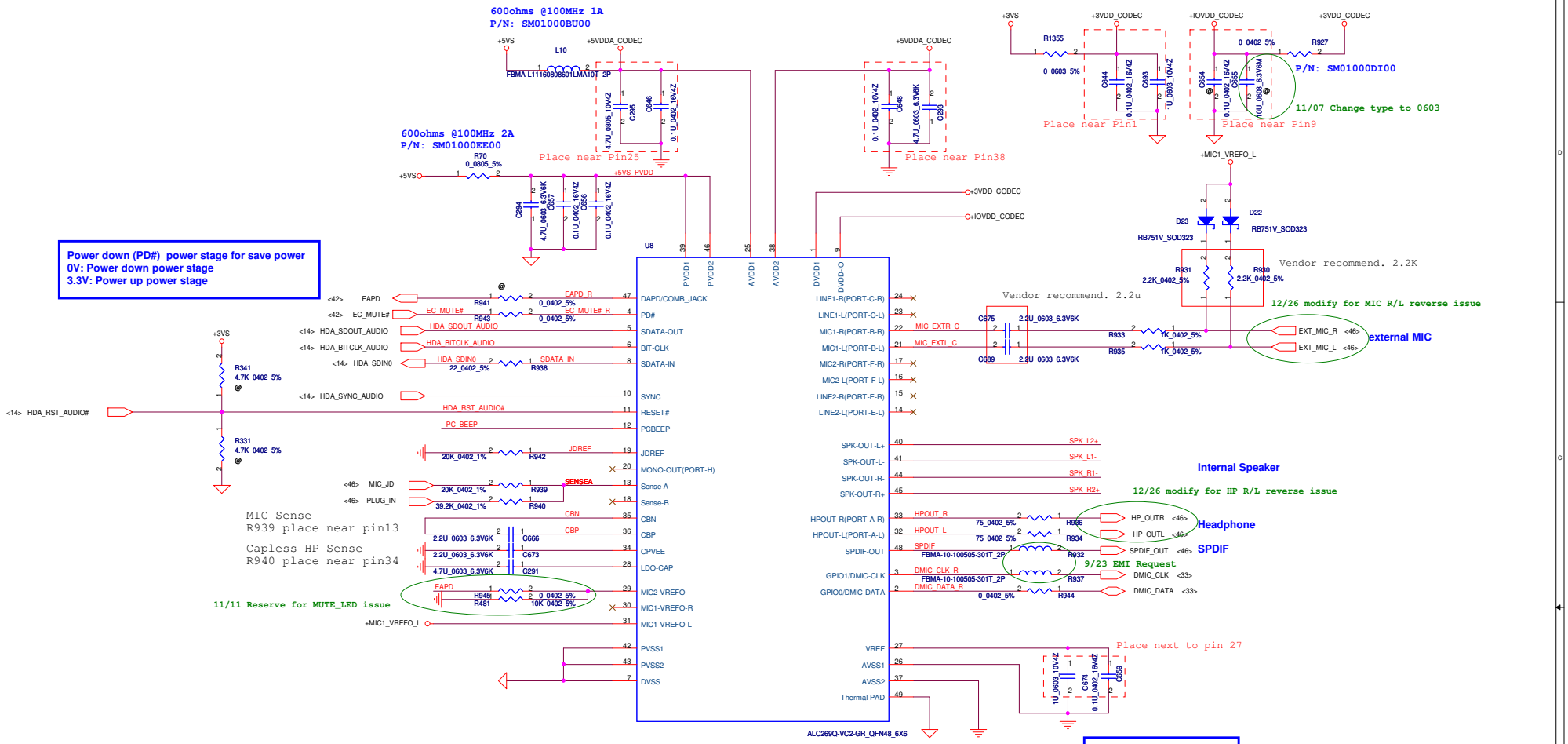


11/07 Change for soft star

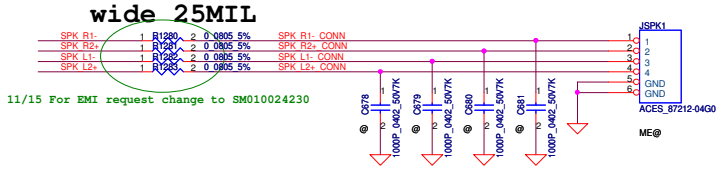
11/07 Change type to 0603

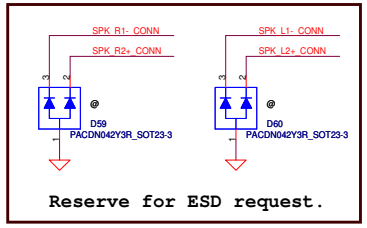
Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

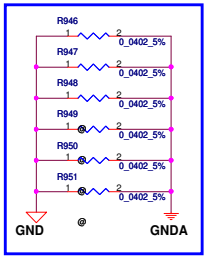
Compal Electronics, Inc.	
Title	HDD/ODD Connector
Size B	Document Number QIWY4 LA-8002P
Rev	1.0
Date: Monday, January 16, 2012	Sheet 40 of 64

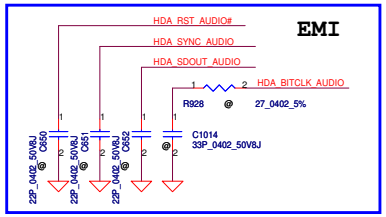


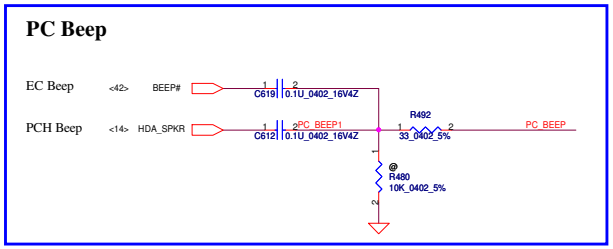
Pin Assignment	Location	Function
SPK-OUT (Pin40/41/44/45)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
MIC1(Pin21/22)	External	Mic in











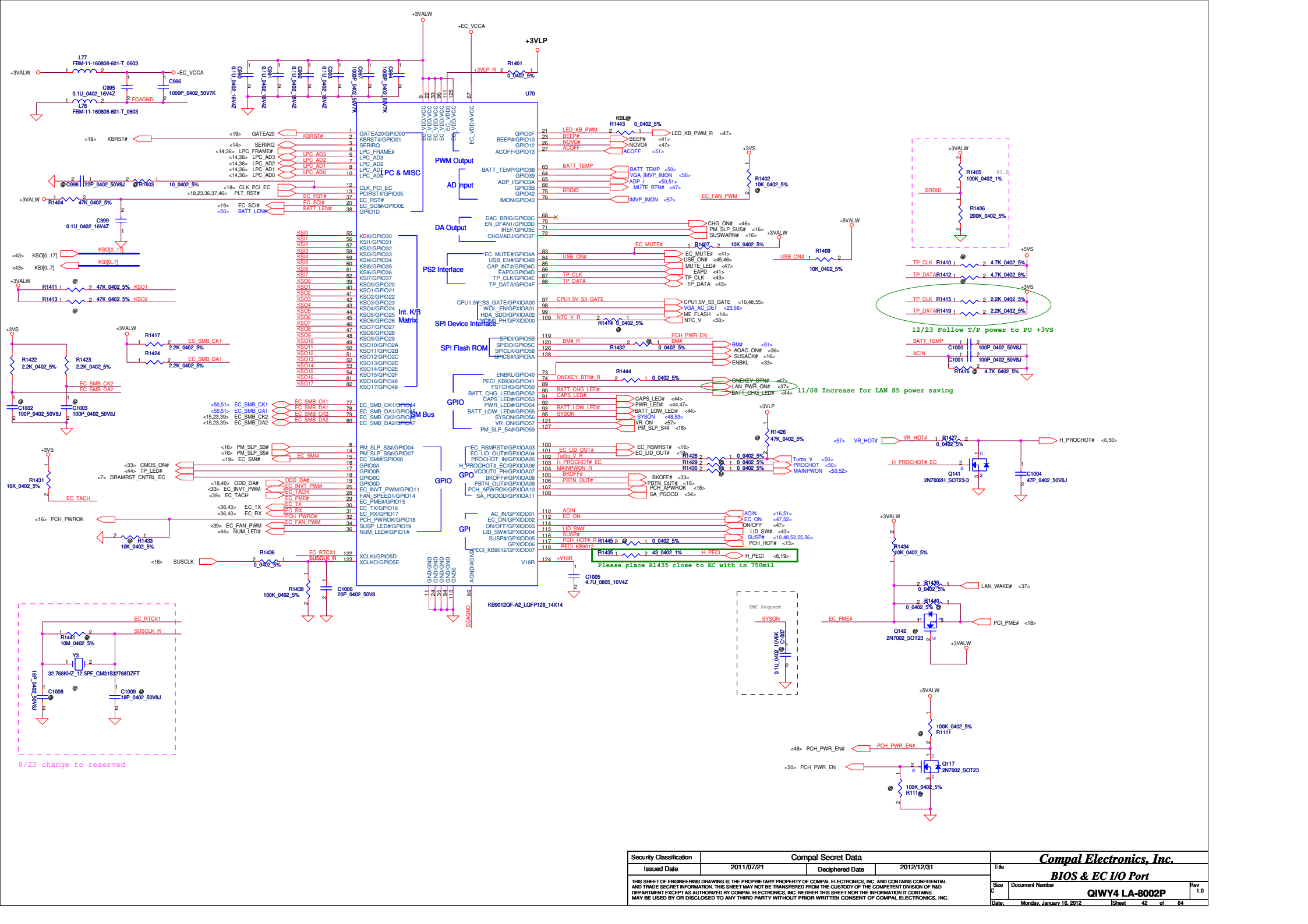
Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics,Ltd.

Title: HD Audio Codec_ALC269Q-VC

Size	Document Number	Rev
C	QIWY4 LA-8002P	1.0

Date: Monday, January 16, 2012 Sheet 41 of 64



Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.	
Title	BIOS & EC I/O Port
Size	C
Document Number	QIWY4 LA-8002P
Rev	1.0
Date:	Monday, January 16, 2012
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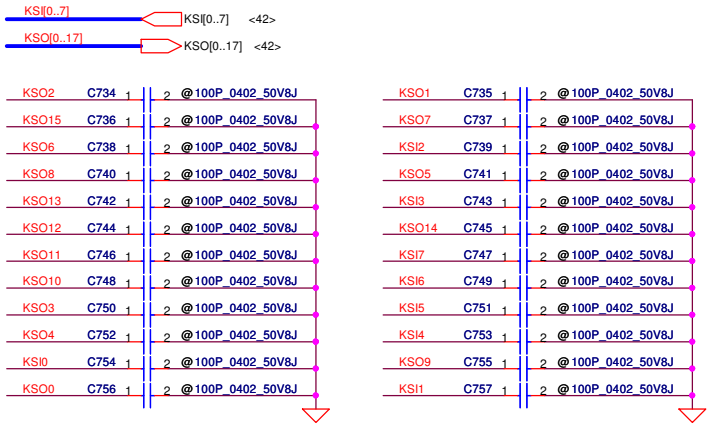
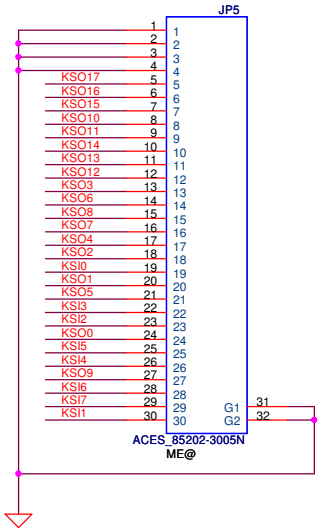
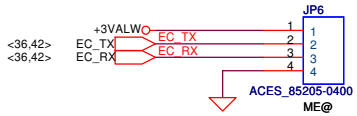
INT_KBD Conn.



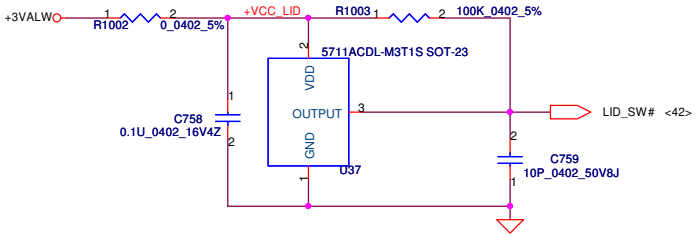
CONN PIN define need double check



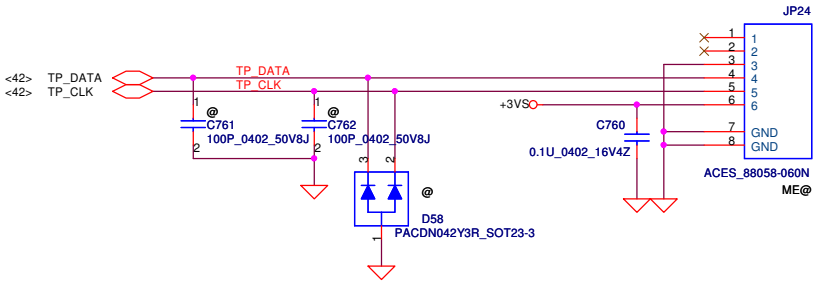
EC DEBUG PORT



Lid Switch



To TP/B Conn.

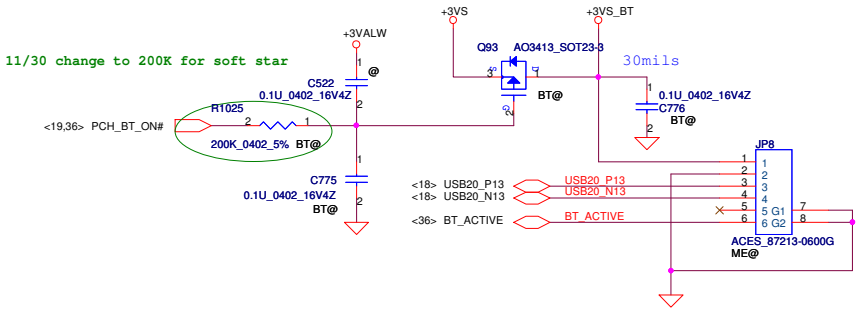


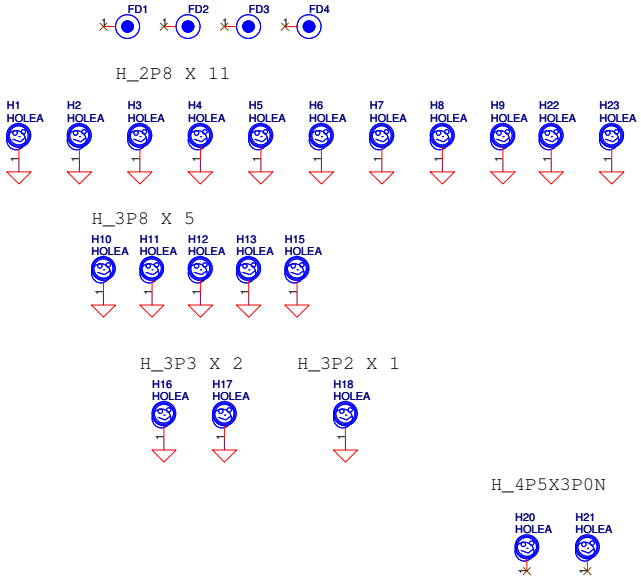
Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title: KB /SW /LPC Debug Conn.			
Size: B	Document Number: QIWY4 LA-8002P		Rev: 1.0
Date: Monday, January 16, 2012	Sheet 43 of 64		

LED

BT MODULE CONN





Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **LED/EC SPI ROM/BT**

Size	Document Number	Rev
B	QIWY4 LA-8002P	1.0

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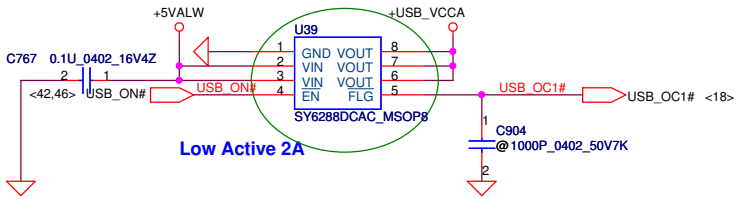
LEFT SIDE USB3.0 PORT X2

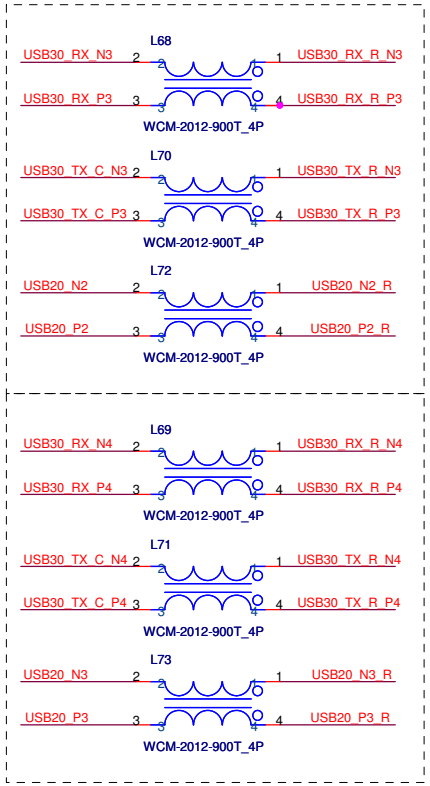
11/07 Change source to SA00004KB00

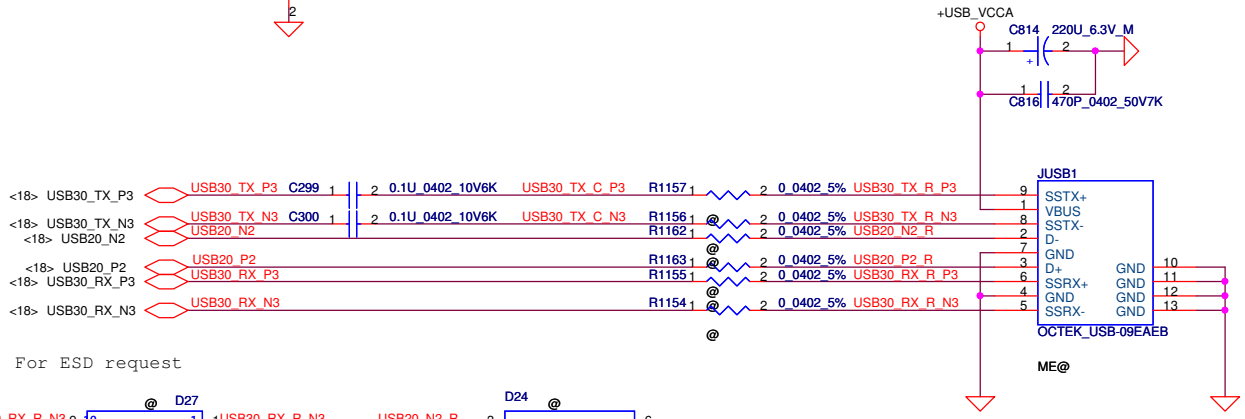


For EMI request

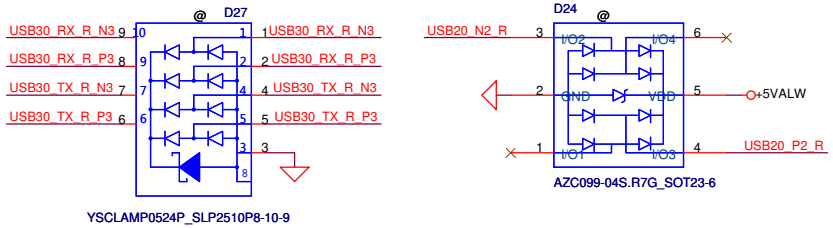
USB2.0 choke --> SM070000I00

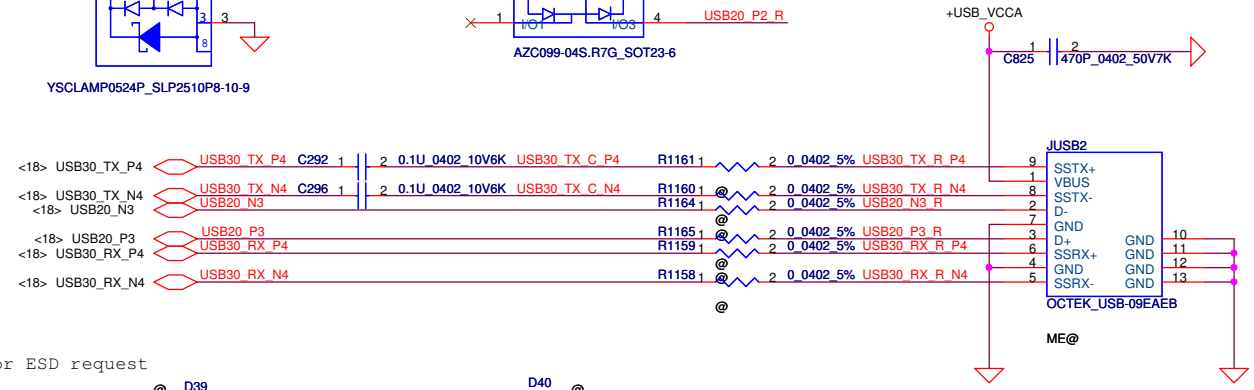
USB3.0 Choke --> SM070001U00



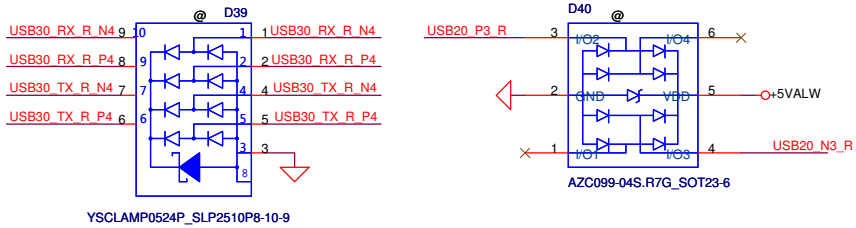


For ESD request





For ESD request



Security Classification	Compal Secret Data For EMI request		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **USB3.0 ports**

Size	Document Number	Rev
Custom	QIWY4 LA-8002P	1.0

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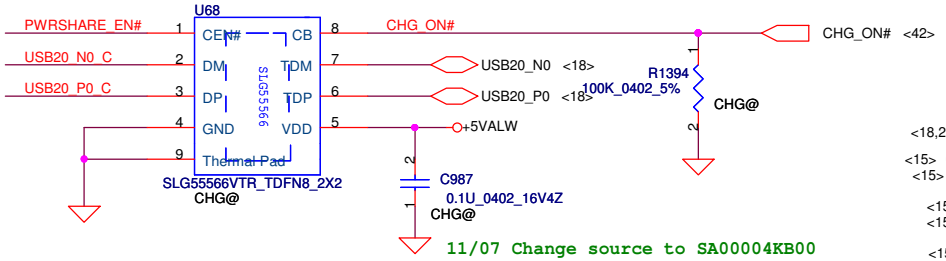
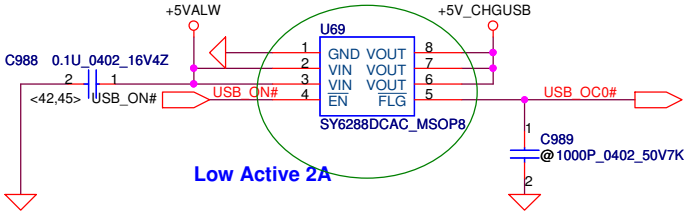
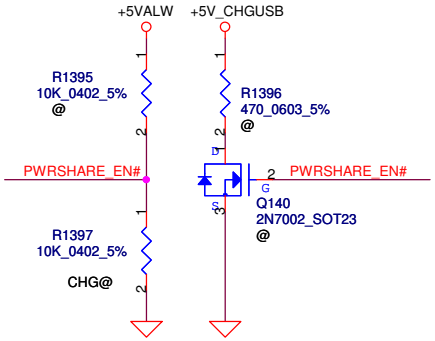
Right side USB Charger

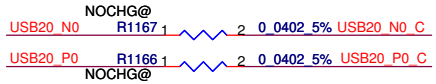


11/07 Change source to SA00004KB00



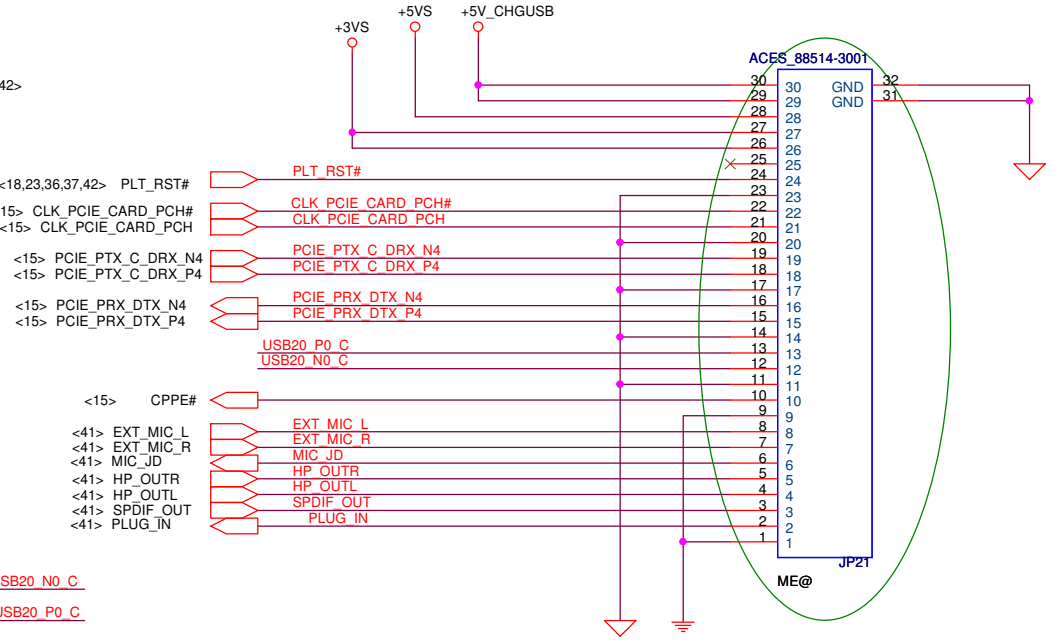
Low Active 2A





CB	Function
L	auto detection charger identification active
H	DP/DM=TDP/TDM

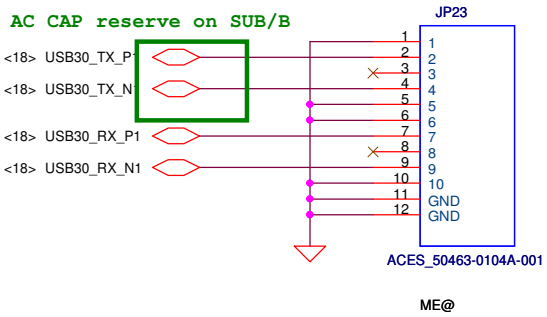
USB2.0/3.0 choke and ESD diode at sub-B.



12/23 Change to SP010011A00 for ASSY issue

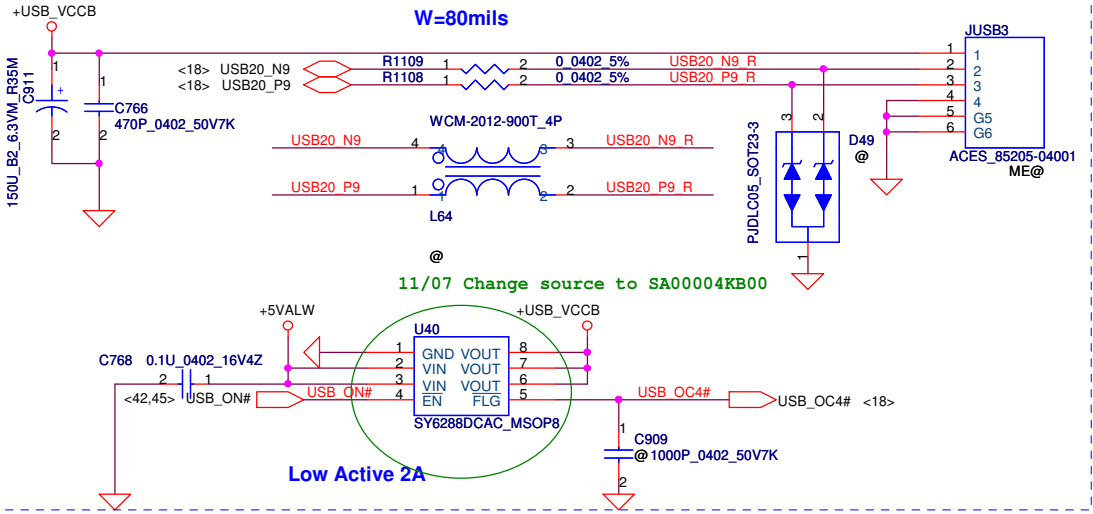
Right side USB3.0 port (Option)

AC CAP reserve on SUB/B



Right USB Conn.(Cable)

W=80mils



Low Active 2A

Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **Audio B Conn/USB charger**

Size	Document Number	Rev
Custom	QIWY4 LA-8002P	1.0

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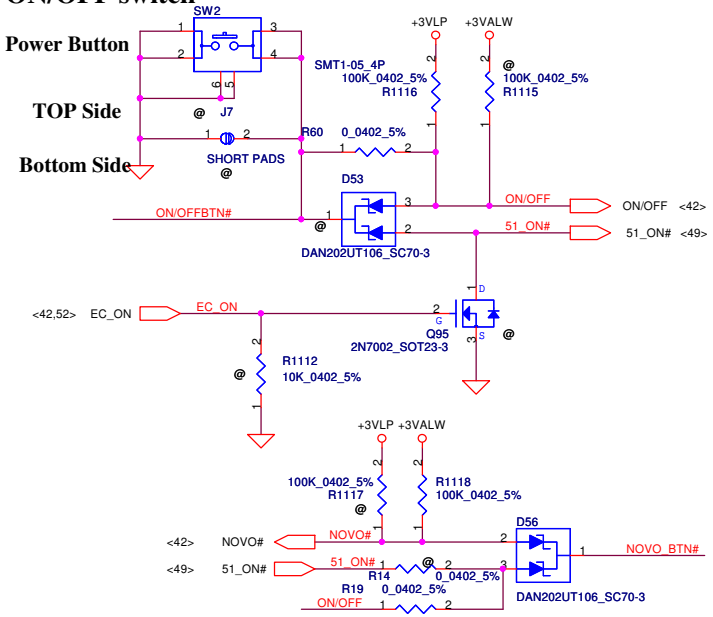
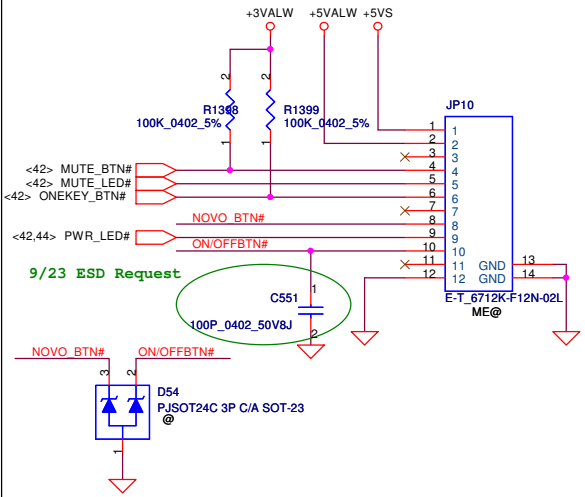
ON/OFF switch

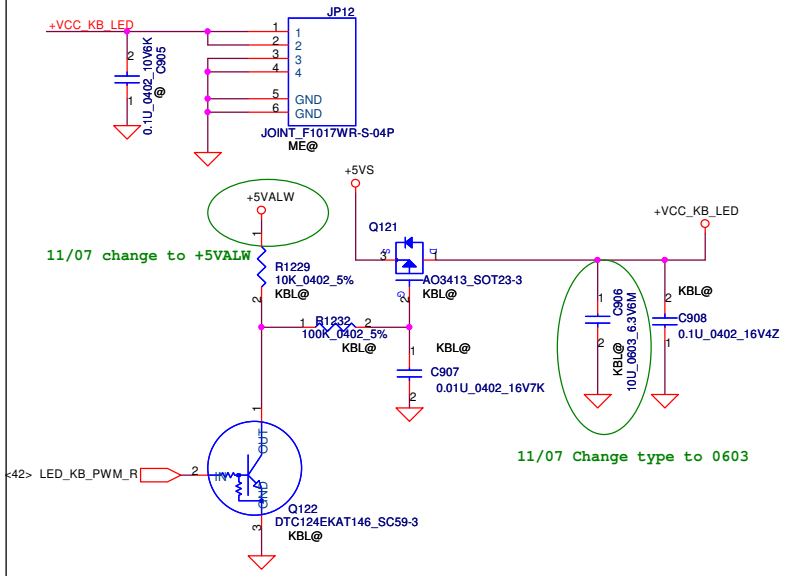


Power Button/B link to Function/B Conn. 10pin



EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

KB Lighting CONN.4pin



Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics,Ltd.

Title: ***other IO connector***

Size	Document Number	Rev
Custom	***QIWY4 LA-8002P***	1.0

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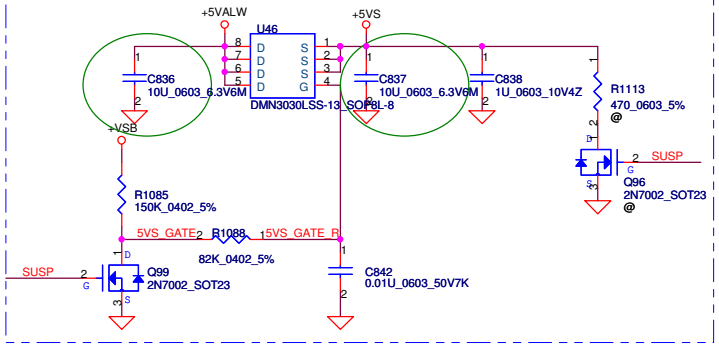
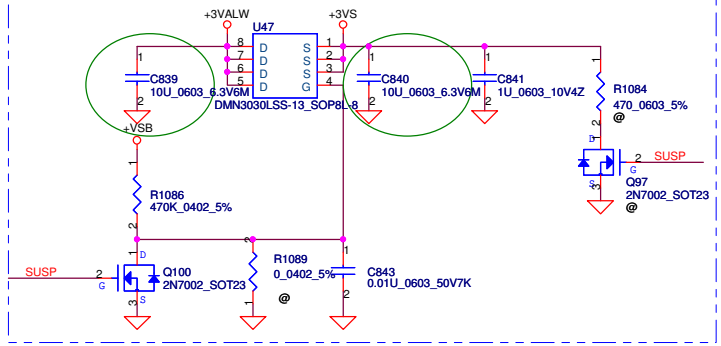
+5VALW TO +5VS

11/07 Change type to 0603



+3VALW TO +3VS

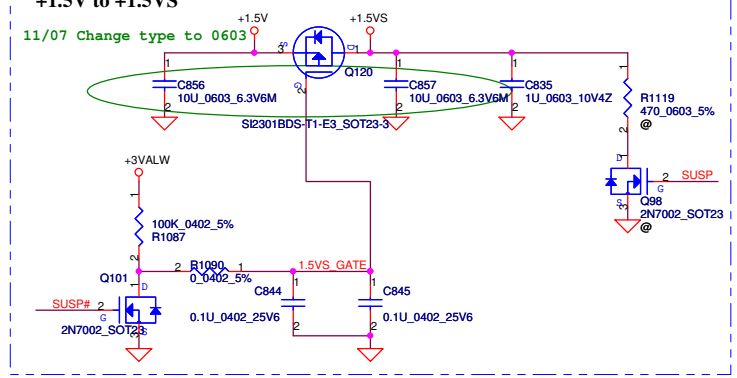
11/07 Change type to 0603



+1.5V to +1.5VS

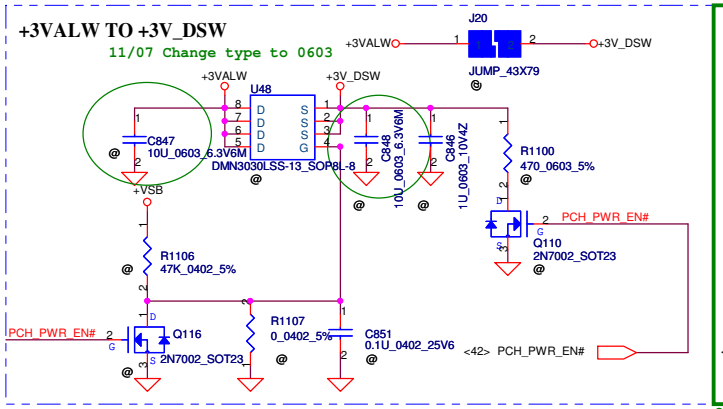
7/26 change SI4800 to SI2301

11/07 Change type to 0603

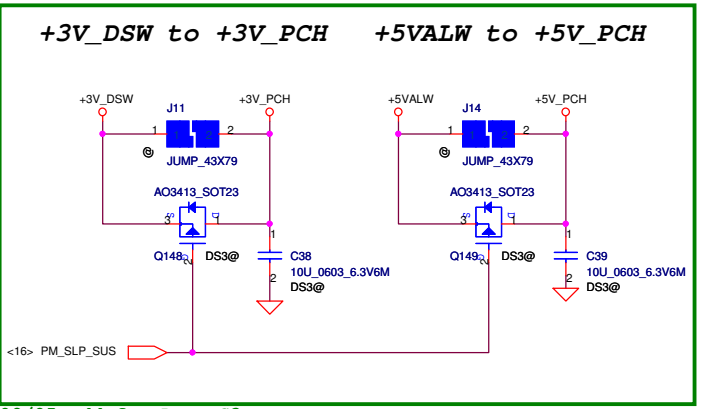


+3VALW TO +3V_DSW

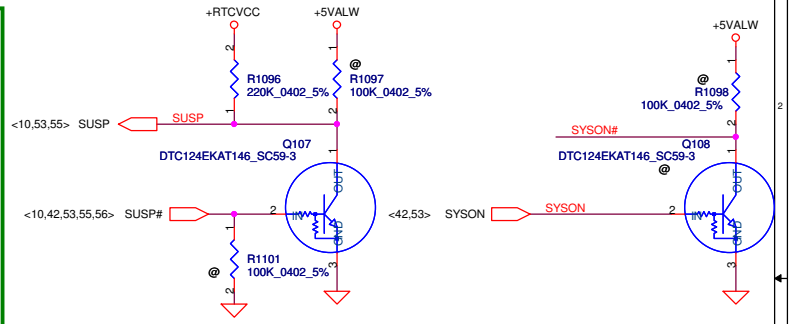
11/07 Change type to 0603



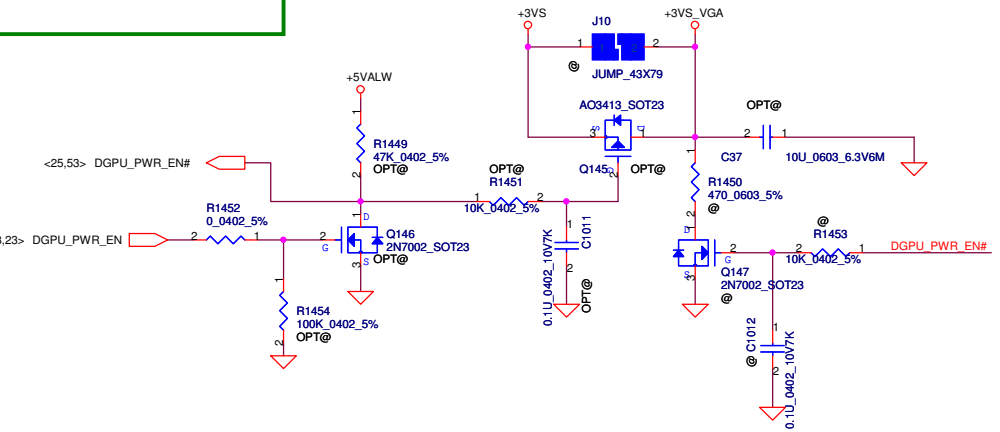
+3V_DSW to +3V_PCH +5VALW to +5V_PCH

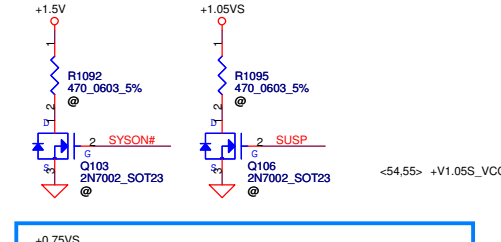


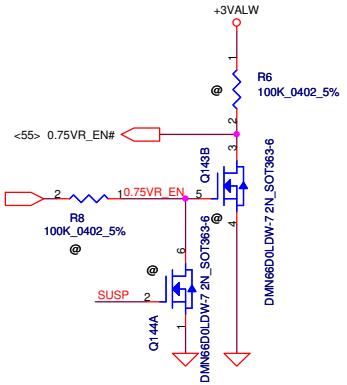
09/05 add for Deep S3

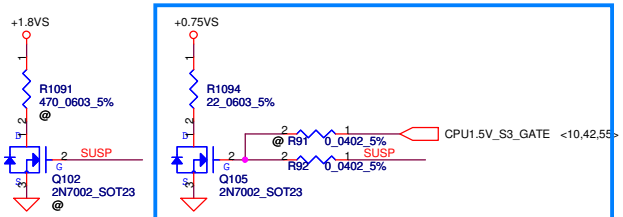


+3VS to +3VS_VGA









For Intel S3 Power Reduction.

Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **DC Interface**

Size	Document Number	Rev
Custom	QIWY4 LA-8002P	1.0

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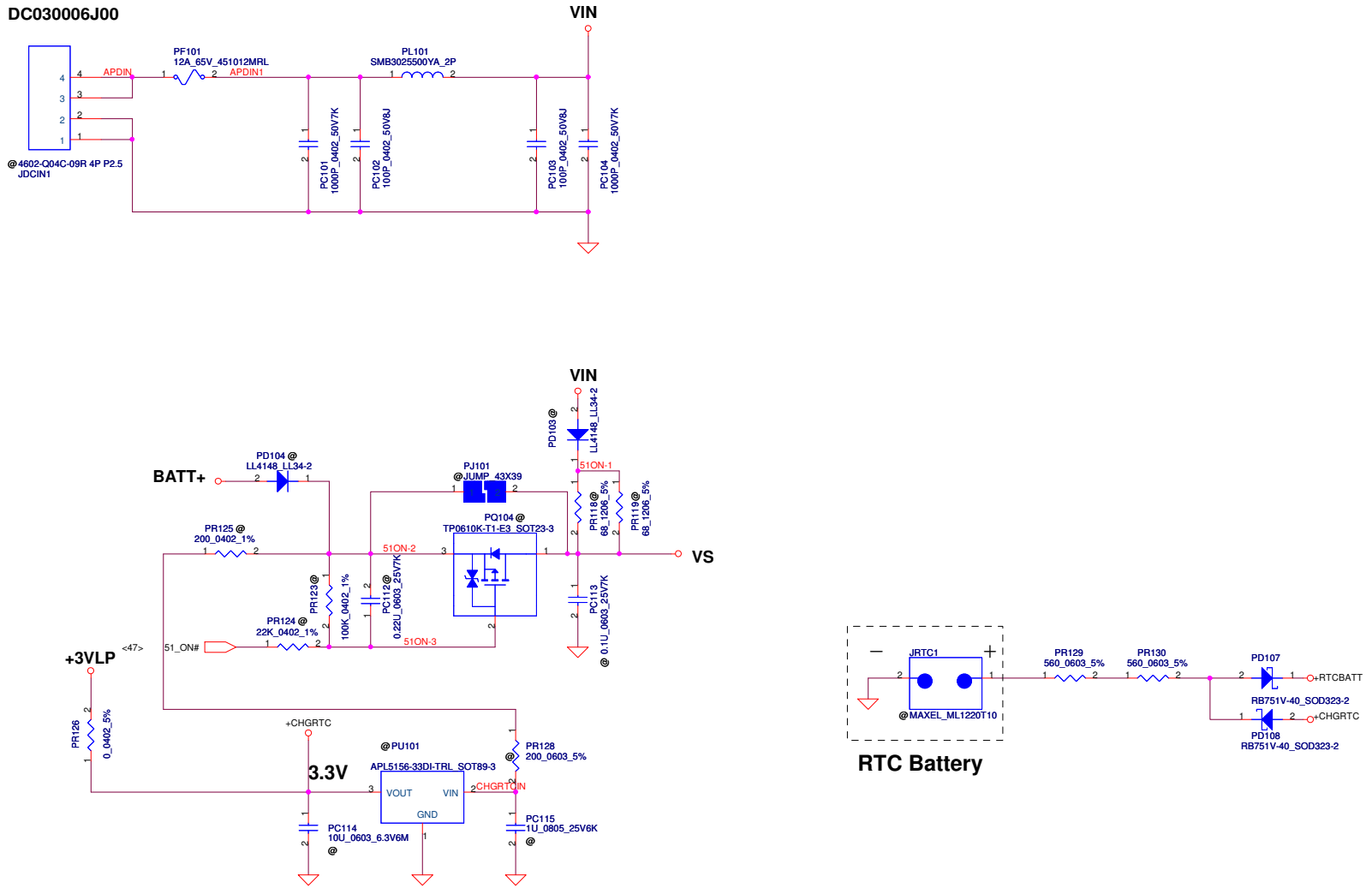

Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: Vin Detector

Size	Document Number	Rev
Custom	QIWY4	1.0

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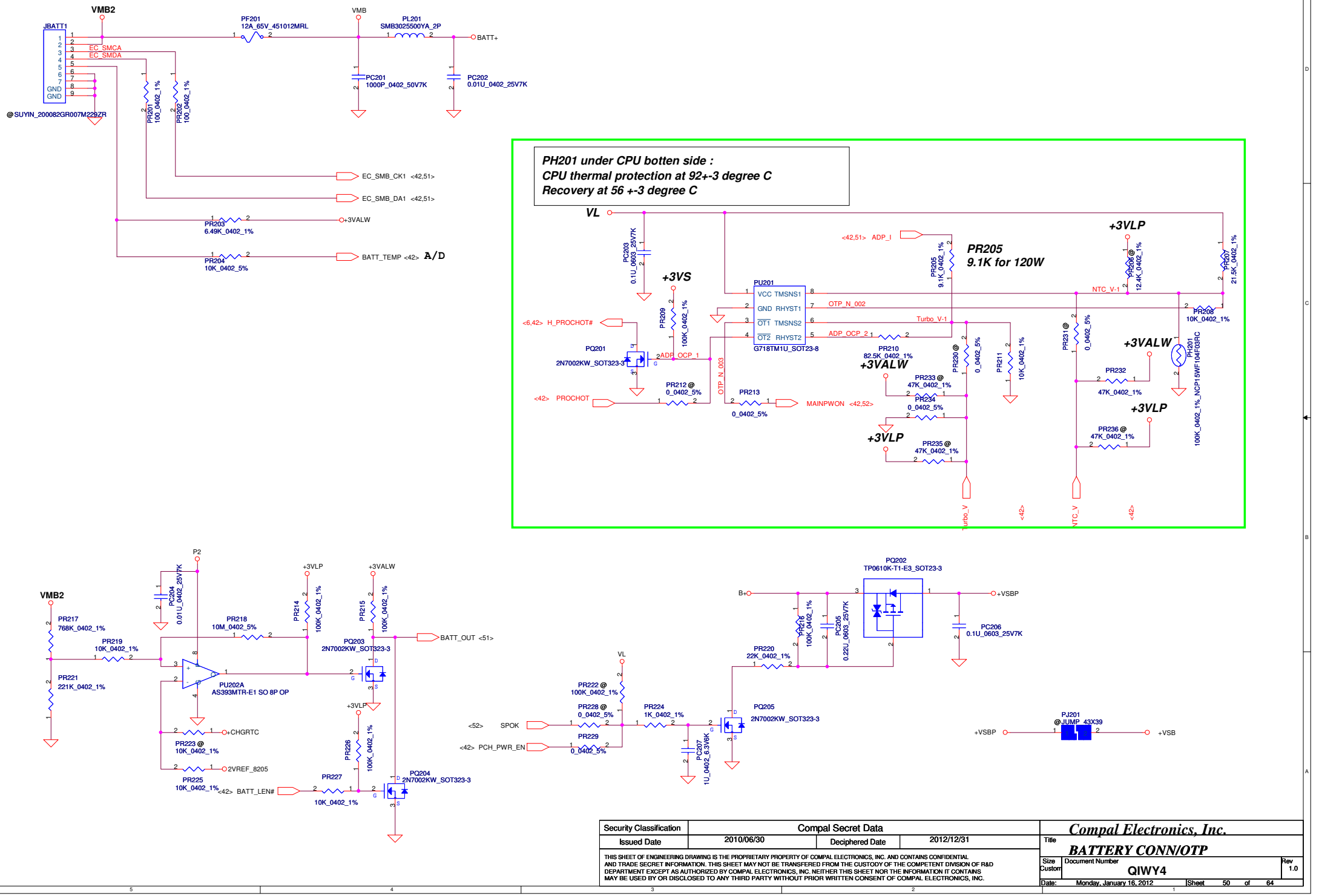
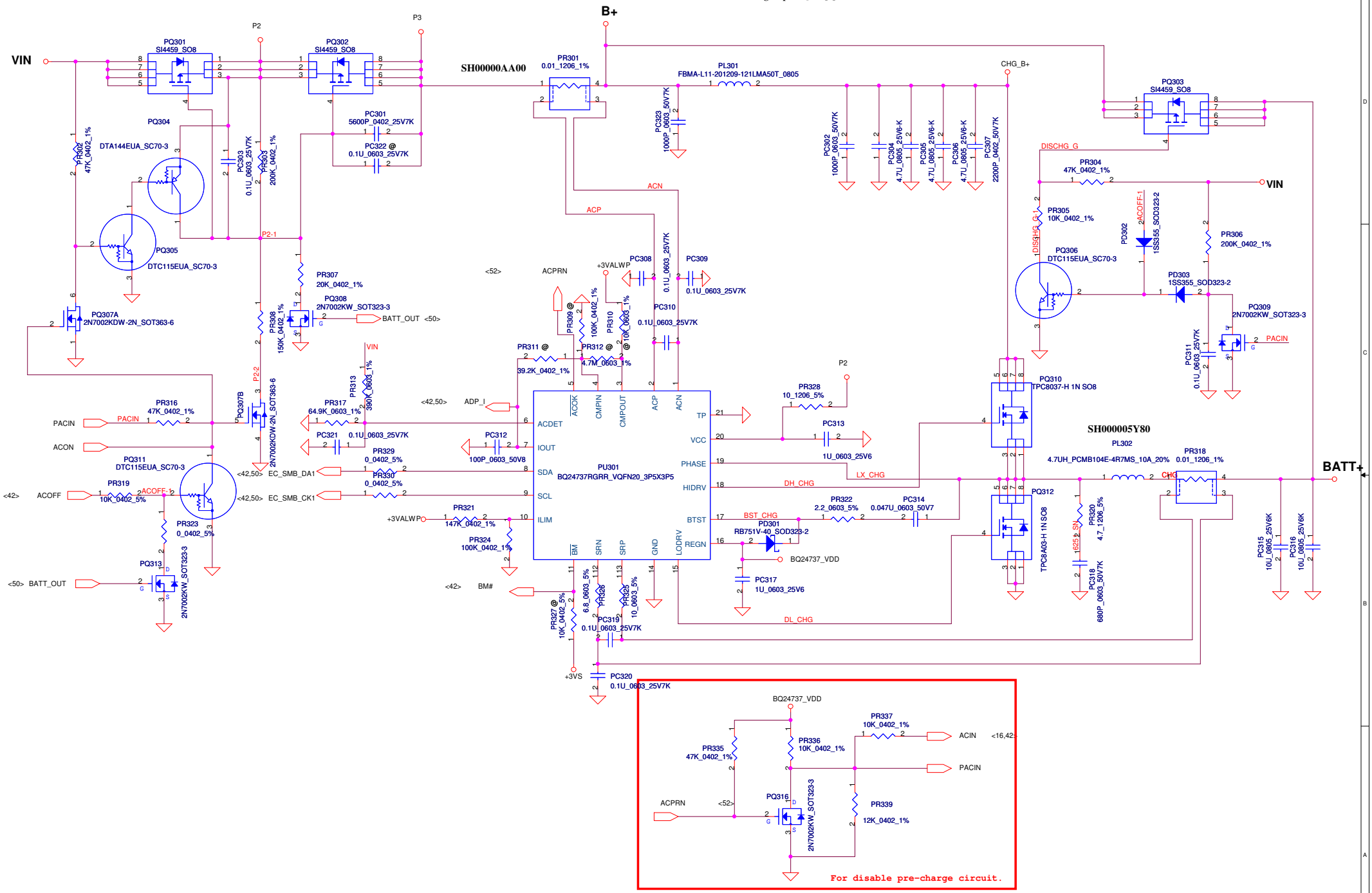


Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title: BATTERY CONN/OTP			
Size: Custom	Document Number: QIWY4		Rev: 1.0
Date: Monday, January 16, 2012	Sheet 50 of 64		

Charge Option() bit[8]=1



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/12/31

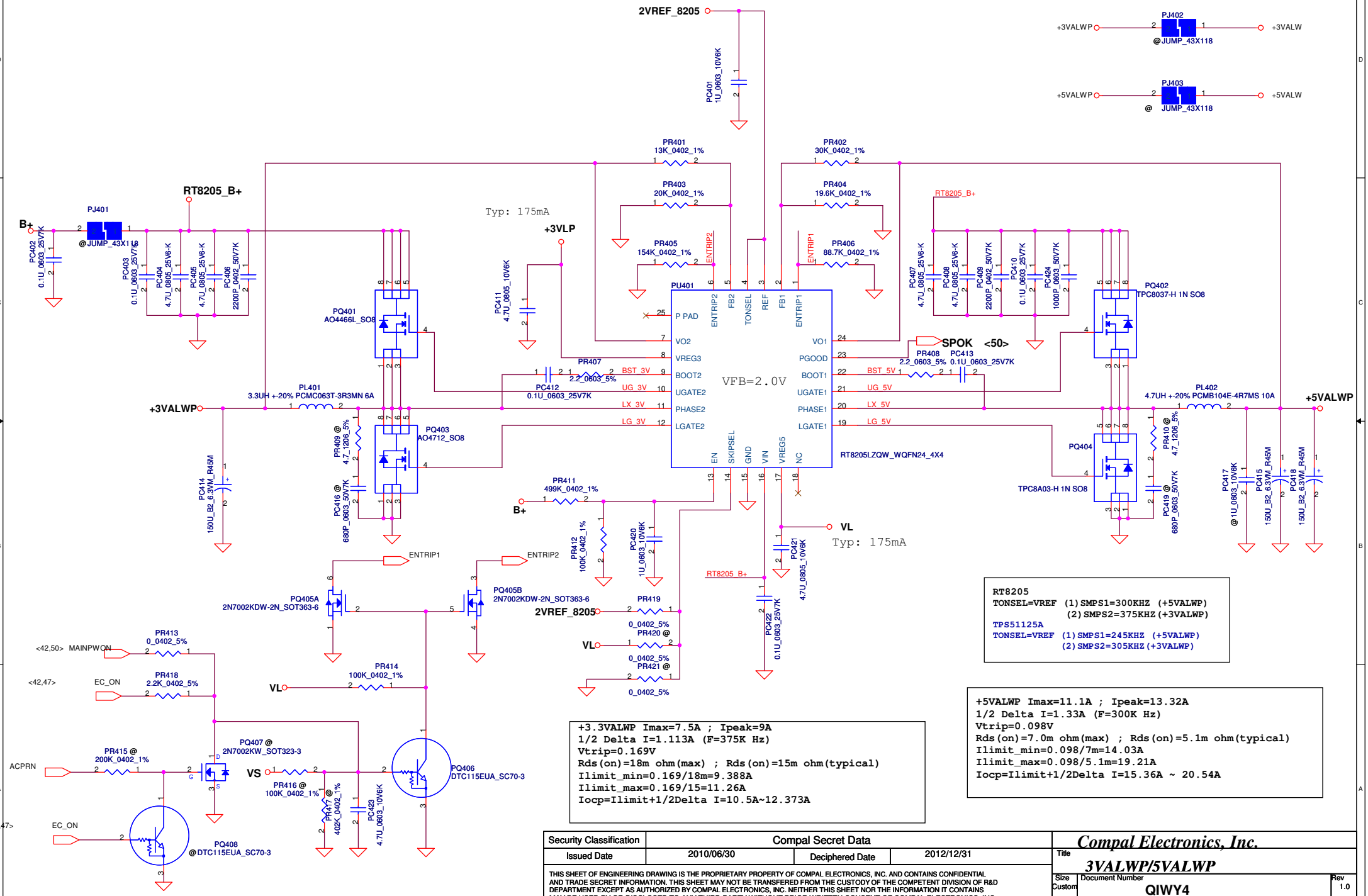
Compal Electronics, Inc.

Title: CHARGER

Size: | Document Number: QIWY4 | Rev: 1.0

Date: Monday, January 16, 2012 | Sheet 51 of 64

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



RT8205
TONSEL=VREF (1) SMPS1=300KHZ (+5VALWP)
(2) SMPS2=375KHZ (+3VALWP)
TPS51125A
TONSEL=VREF (1) SMPS1=245KHZ (+5VALWP)
(2) SMPS2=305KHZ (+3VALWP)

+3.3VALWP Imax=7.5A ; Ipeak=9A
1/2 Delta I=1.113A (F=375K Hz)
Vtrip=0.169V
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Ilimit_min=0.169/18m=9.388A
Ilimit_max=0.169/15=11.26A
Iocp=Ilimit+1/2Delta I=10.5A~12.373A

+5VALWP Imax=11.1A ; Ipeak=13.32A
1/2 Delta I=1.33A (F=300K Hz)
Vtrip=0.098V
Rds(on)=7.0m ohm(max) ; Rds(on)=5.1m ohm(typical)
Ilimit_min=0.098/7m=14.03A
Ilimit_max=0.098/5.1m=19.21A
Iocp=Ilimit+1/2Delta I=15.36A ~ 20.54A

Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size	Document Number	Rev
Custom	QIWY4	1.0

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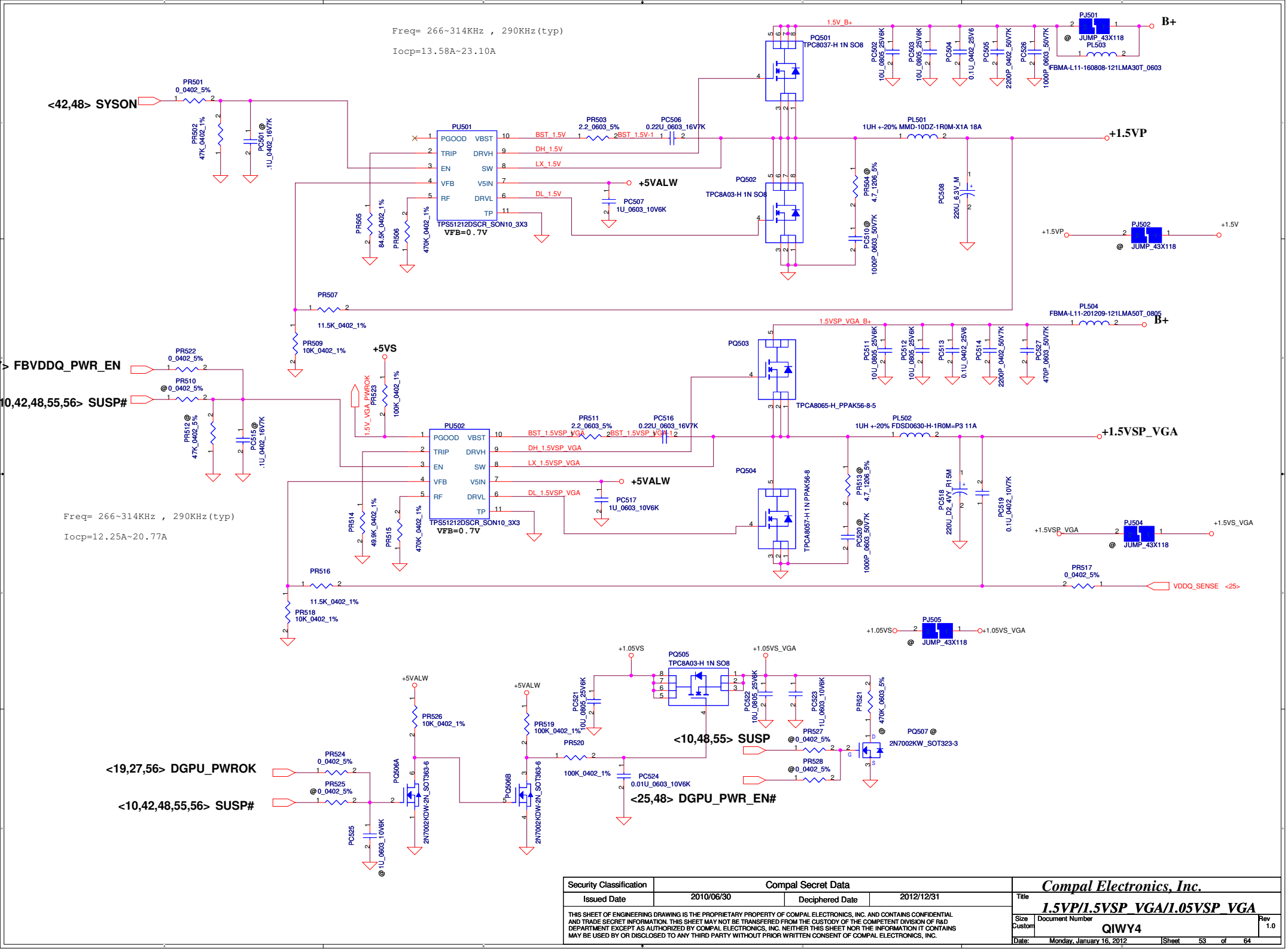


Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: 1.5VP/1.5VSP_VGA/1.05VSP_VGA

Size	Document Number	Rev
Custom	QIWY4	1.0

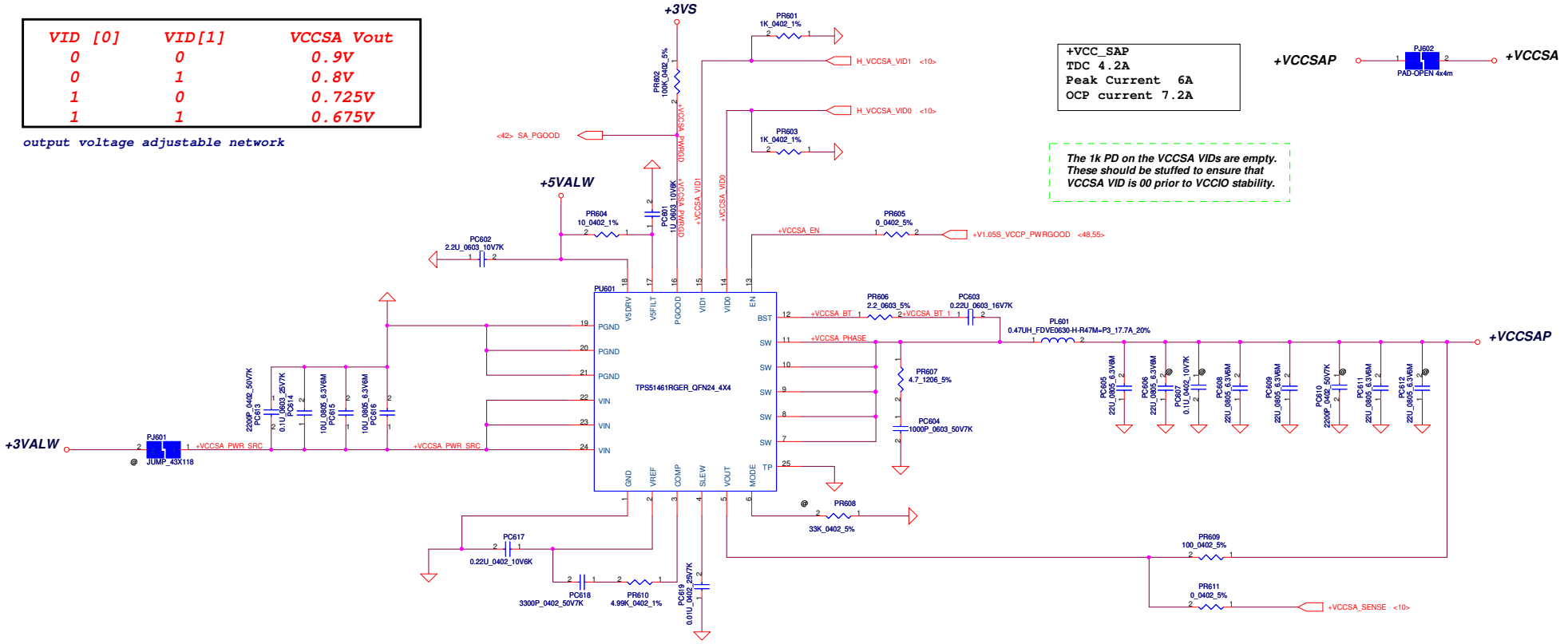
Date: Monday, January 16, 2012 | Sheet 53 of 64

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



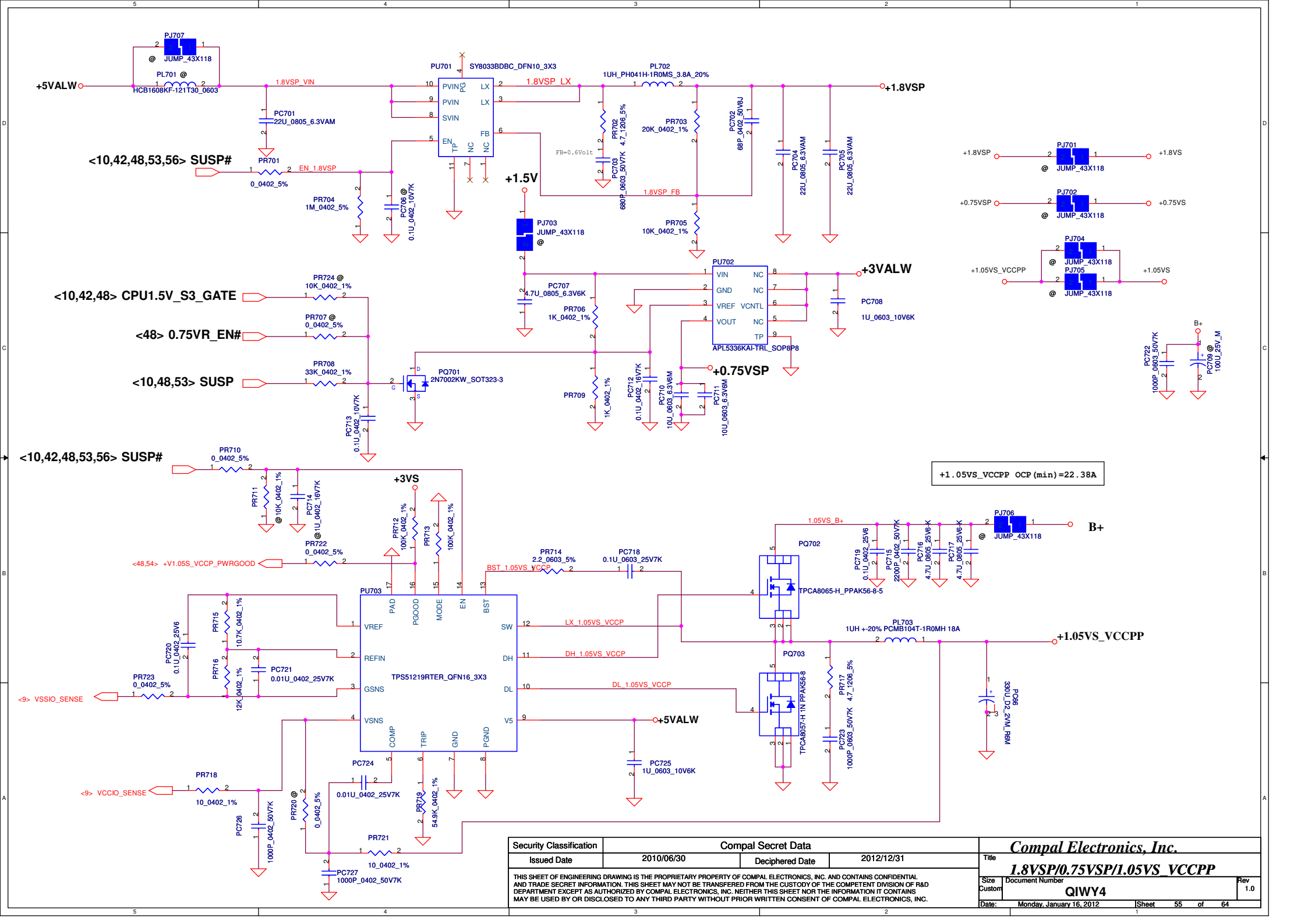
Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: VCCSAP/1.05S_VCCPP

Size	Document Number	Rev
C	QIWY4	1.0

Date: Monday, January 16, 2012 Sheet 54 of 64



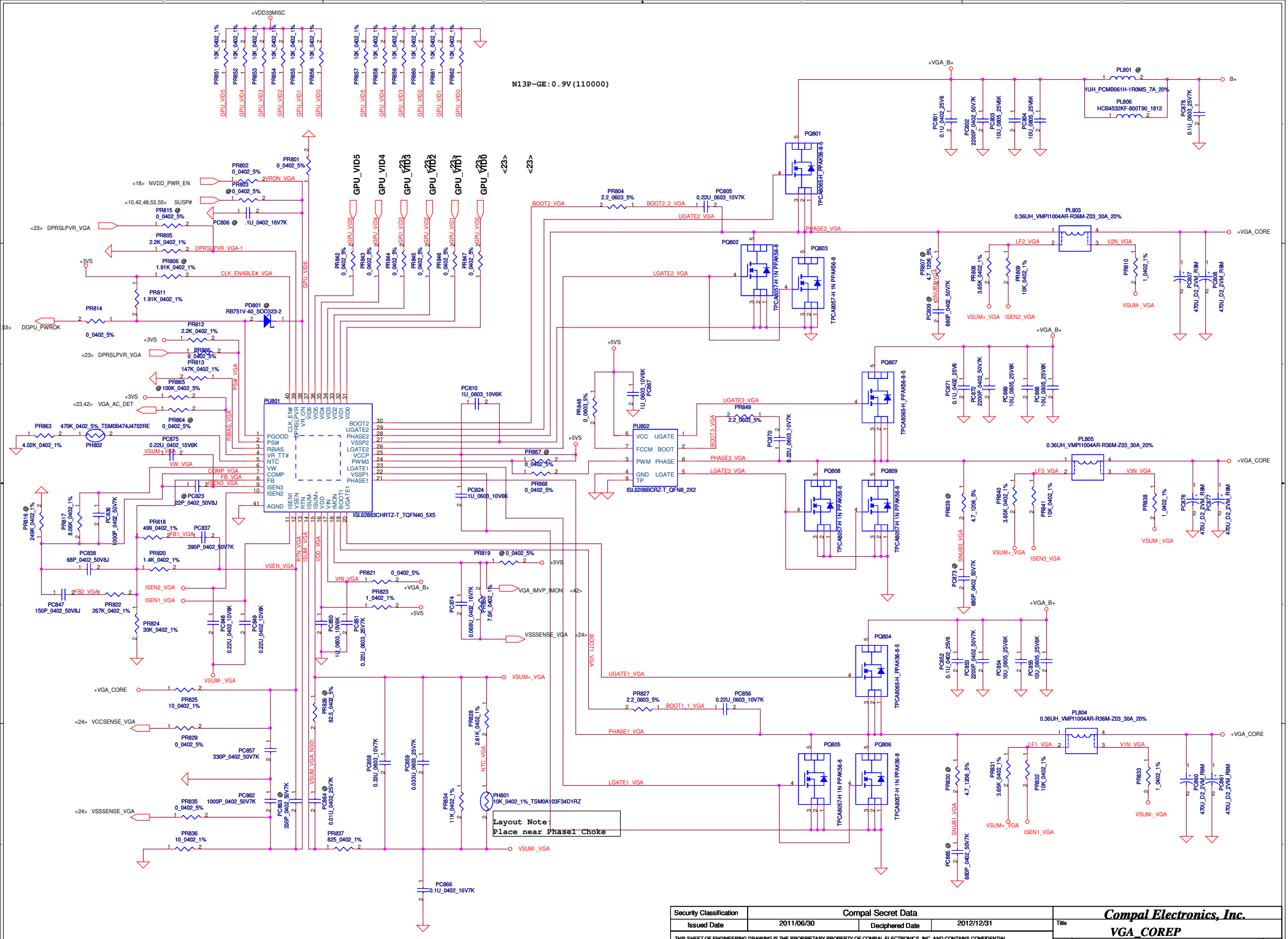
Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: 1.8VSP/0.75VSP/1.05VS_VCCPP

Size	Document Number	Rev
Custom	QIWY4	1.0

Date: Monday, January 16, 2012 Sheet 55 of 64



Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2012/12/31

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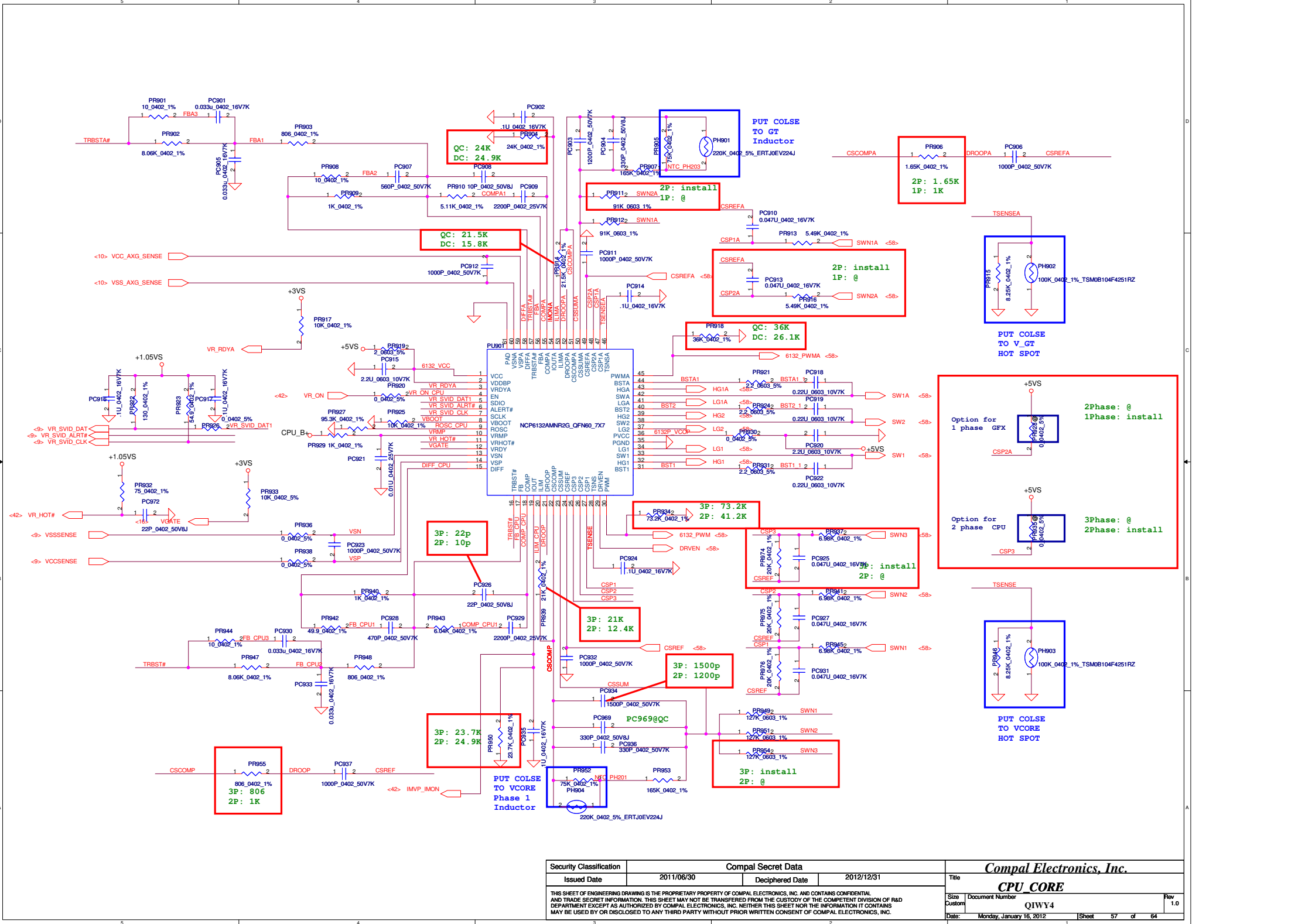
Compal Electronics, Inc.

Title: VGA_COREP

Size	Document Number	Rev
	QIWY4 LA-8002P	1.0

Date: Monday, January 16, 2012 Sheet 56 of 64



Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2012/12/31

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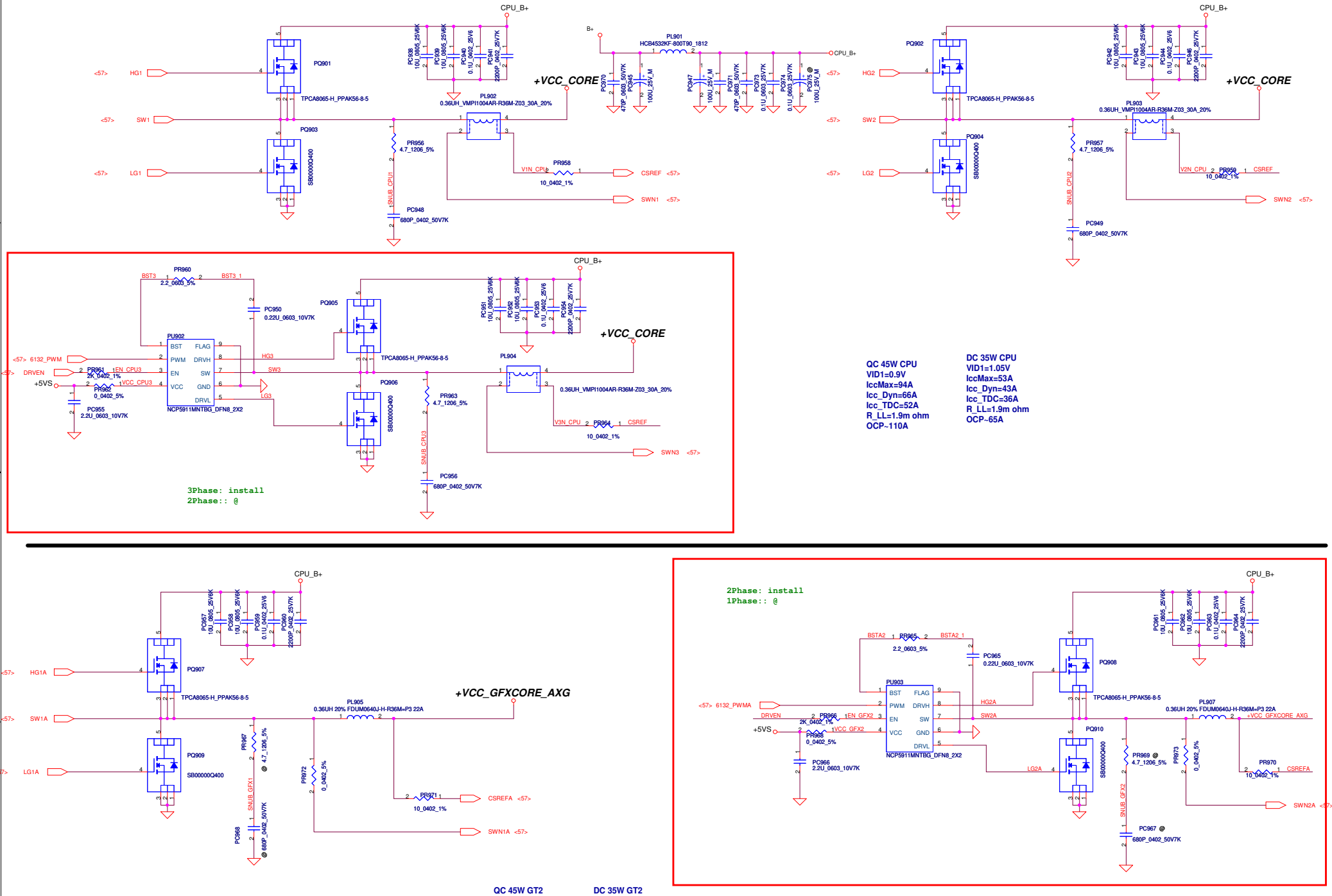
Compal Electronics, Inc.

Title: **CPU_CORE**

Size	Document Number	Rev
Custom	QIWY4	1.0

Date: Monday, January 16, 2012 | Sheet 57 of 64



Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: CPU_CORE

Size	Document Number	Rev
C	QIWY4	1.0

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+CPU_CORE

+VCC_CORE

PC1 10U_0805_6.3VAM, PC2 10U_0805_6.3VAM, PC3 10U_0805_6.3VAM, PC4 10U_0805_6.3VAM, PC5 10U_0805_6.3VAM

PC6 10U_0805_6.3VAM, PC7 10U_0805_6.3VAM, PC8 10U_0805_6.3VAM, PC9 10U_0805_6.3VAM, PC10 10U_0805_6.3VAM, PC11 10U_0805_6.3VAM

+VCC_CORE

PC20 22U_0805_6.3V6M, PC21 22U_0805_6.3V6M, PC22 22U_0805_6.3V6M, PC23 22U_0805_6.3V6M, PC24 22U_0805_6.3V6M

PC44 22U_0805_6.3V6M, PC45 22U_0805_6.3V6M, PC46 22U_0805_6.3V6M, PC47 22U_0805_6.3V6M, PC48 22U_0805_6.3V6M

PC61 22U_0805_6.3V6M, PC62 22U_0805_6.3V6M, PC63 22U_0805_6.3V6M, PC64 22U_0805_6.3V6M, PC65 22U_0805_6.3V6M

PC69 22U_0805_6.3V6M, PC70 22U_0805_6.3V6M, PC71 22U_0805_6.3V6M, PC72 22U_0805_6.3V6M

+VCC_CORE

PC73 330U_D2_2VM_R9M, PC74 330U_D2_2VM_R9M, PC75@DC 330U_D2_2VM_R9M, PC76 330U_D2_2VM_R9M, PC77 @ 330U_D2_2VM_R9M, PC78 470U_D2_2VM_R9M

PC8,PC21,PC22,PC63

DC:PC73,PC74,PC76(330uF/9m)+PC78(330uF/6m)
QC:PC73,PC74,PC75,PC76(330uF/9m)+PC78(470uF/9m)

PC818
PC825,PC827,PC828,PC829
PC839,PC841,PC844,PC845

+VCC_GFXCORE_AXG

+VCC_GFXCORE_AXG

PC12 22U_0805_6.3V6M, PC13 22U_0805_6.3V6M, PC14 22U_0805_6.3V6M, PC15 22U_0805_6.3V6M, PC16 22U_0805_6.3V6M, PC17 22U_0805_6.3V6M, PC18 22U_0805_6.3V6M, PC19 22U_0805_6.3V6M

PC36 22U_0805_6.3V6M, PC37 22U_0805_6.3V6M, PC38 22U_0805_6.3V6M, PC39 22U_0805_6.3V6M, PC40 22U_0805_6.3V6M, PC41 22U_0805_6.3V6M, PC42 22U_0805_6.3V6M, PC43 22U_0805_6.3V6M

PC57 330U_D2_2VM_R9M, PC58 330U_D2_2VM_R9M, PC59 330U_D2_2VM_R9M

PC59@DC

PC38,PC39,PC40,PC41

Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites

+1.05VS

PC25 22U_0805_6.3V6M, PC26 22U_0805_6.3V6M, PC27 22U_0805_6.3V6M, PC28 22U_0805_6.3V6M, PC29 22U_0805_6.3V6M, PC30 22U_0805_6.3V6M, PC31 22U_0805_6.3V6M, PC32 22U_0805_6.3V6M, PC33 22U_0805_6.3V6M, PC34 22U_0805_6.3V6M, PC35 22U_0805_6.3V6M

PC49 22U_0805_6.3V6M, PC50 22U_0805_6.3V6M, PC51 22U_0805_6.3V6M, PC52 22U_0805_6.3V6M, PC53 22U_0805_6.3V6M, PC54 22U_0805_6.3V6M, PC55 22U_0805_6.3V6M, PC56 22U_0805_6.3V6M

PC67 330U_D2_2VM_R8M, PC68 330U_D2_2VM_R8M

PC32,PC49,PC54,PC55,PC56

+VGA_CORE Under VGA Core

PC811 4.7U_0603_6.3V6M, PC812 4.7U_0603_6.3V6M, PC813 4.7U_0603_6.3V6M, PC814 4.7U_0603_6.3V6M, PC815 4.7U_0603_6.3V6M, PC816 4.7U_0603_6.3V6M, PC817 4.7U_0603_6.3V6M, PC818 4.7U_0603_6.3V6M

PC825 4.7U_0603_6.3V6M, PC826 4.7U_0603_6.3V6M, PC827 4.7U_0603_6.3V6M, PC828 4.7U_0603_6.3V6M, PC829 4.7U_0603_6.3V6M, PC830 4.7U_0603_6.3V6M, PC831 4.7U_0603_6.3V6M

PC839 0.1U_0402_10V7K, PC840 0.1U_0402_10V7K, PC841 0.1U_0402_10V7K, PC842 0.1U_0402_10V7K, PC843 0.1U_0402_10V7K, PC844 0.1U_0402_10V7K, PC845 0.1U_0402_10V7K, PC846 0.1U_0402_10V7K

+VGA_CORE Near VGA Core

PC819 22U_0805_6.3V6M, PC820 47U_0805_6.3V6M, PC821 22U_0805_6.3V6M, PC822 4.7U_0805_6.3V6K

PC832 4.7U_0805_6.3V6K, PC833 4.7U_0805_6.3V6K, PC834 4.7U_0805_6.3V6K, PC835 4.7U_0805_6.3V6K

Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PROCESSOR DECOUPLING

Size	Document Number	Rev
	QIWY4 LA-8002P	1.0

Date: Monday, January 16, 2012 Sheet 59 of 64

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Reserve 0.1uF for Charger IC	51	Reserve PC321	2011/09/27	B test
2	EMI Request		change PR322,PR407,PR408,PR503,PR511,PR606,PR804,PR827 to 2.2 ohm add PC526,PC527,PC970,PC971(470pF)	2011/09/27	B test
3	Combine 1.05V	51	Remove one power rail +V1.05S_VCCPP Pop PR722,PR712,PR718	2011/09/27	B test
4	Discharge for +1.05VS_VGA by NV Request	53	Reserve PR528	2011/09/27	B test
5	Set VGA_CORE VBOOT voltage	56	unpop PR806 change PR813 to 147K ohm	2011/09/27	B test
6	For VGA_CORE power saving by NV Request	56	add PR838 0ohm	2011/09/27	B test
7	for CPU_CORE load line adjust	57	add PC969	2011/09/27	B test
8	to prevent MOS over temperature	55/58	change PQ702,PQ901,PQ902,PQ905 TPCA8065	2011/09/27	B test
9	for CPU_CORE test	59	Reserve PC77,PC778	2011/09/27	B test
10	for VGA_CORE Current Balance	56	pop PC875	2011/09/27	B test
11	for debug	51	add PR329,PR330	2011/11/30	C test
12	for VCCIO remote sense	55	add PR723	2011/11/30	C test
13	RC filter to reduce noise	55	add PR721,PC727	2011/11/30	C test
14	VGA_CORE 2 phase or 3 phase option	56	add PR867,PR868	2011/11/30	C test
15	G718 for adapter and OTP	50	pop PC203,PQ201,PR209,PU201,PR213 unpop PR206	2011/11/30	C test
16	for CPU transient	58	change PR911,PR912 to 91K	2011/11/30	C test
17	for EMI Request		add PL301,PC503,PL504,PL801 add PC302,PC323,PC424,PC526,PC722,PC970,PC974	2011/11/30	C test
18	HW reqeust	50 55	reserve connect PCH_PWR_EN for power sequence reserve connect CPU1.5V_S3_GATE for power sequence	2011/11/30	C test
19	for thermal request to reduce temperature	53	change PQ503,PQ504	2011/11/30	C test
20	adjust 1.5VSP_VGA OCP	53	change PR514 to 49.9K	2011/11/30	C test

Item	Reason for change	PG#	Modify List	Date	Phase
21	For HW power sequence adjustment	50	change PR222,PR228 to NA change PR229 to 0 ohm	2011/12/02	C test
22	To adjust +5VALW by HW request	52	change PR404 to 19.6K	2011/12/16	C test
23	Using G718 to replace KB9012 function need to add or reserve resistor	50	Add PR232 and reserve PR233 pull high to +3VALW Add PR234 pull down	2011/12/28	Pre MP
24	TI's Suggestion that snubber should be first at R then C	54	Change PR607 and PC604 order	2011/12/28	Pre MP
25	Reserve resistor for adjust current balance	57	Reserve PR974,PR975,PR976	2011/12/28	Pre MP

QIWY4 HW PIR List

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
				EVT TO DVT
1		P7	Reserve R64	Reserve EC DRAMRST control pin for Deep S3
2		P16	Reserve R1457,R1455,R1447	Reserve SUSACK#,SUSWARN#,SLP_SUS# control signal for Deep S3
3		P16	Reserve Q118,R1120,R1121	Reverse SLP_SUS# to control +3V_PCH&+5V_PCH
4		P16	Change AC_PRESENT Pull high source to +3V_DSW	For Deep S3 function
5		P21	Remove R289	+5V_PCH control circuit change for Deep S3
6		P36	Reserve J8,Q104,C533,C526,R436	Reserve for AOAC function
7		P36	Change JP1 pin2,24,52 power source to +3VS_WLAN_AOAC	Reserve for AOAC function
8		P42	Change EC GPIO pin setting (Impact pin 18,71,72,126,128)	For DeepS3/AOAC function
9		P48	Reserve J11,J14,Q148,Q149,C38,C39	+3V_PCH&+5V_PCH control circuit for Deep S3
10		P45	change U49 symbol (without GND pad)	For DFx issue
11		P46	change U40,U69 symbol (without GND pad)	For DFx issue
12		P47	change JP10 type to SP01001B800	For DFx issue
13		P43	change JP24 type to SP010010T00	For DFx issue
14		P19	Reserve R207,R224 to contact WLAN wake even	Reserve for AOAC function
15		P19	Reserve R704 and R706 for GPIO69 PU&PD	For SKU ID
16		P23	Change CV37,CV38 to 22P	For Crystal EA request
17		P37	Change C968,C969 to 33P	For Crystal EA request
				DVT TO PVT
1		P14	Change power source to +5VS (Q10 pin 2)	Follow intel Design Guide
2		P16	Reserve R257 PU 10K to +3V_DSW	For Deep S3 function
3		P40	Change R1110 to 200K,C638 to 0.1u	For ODD soft star
4		P10	Change C124,C125,C126,C127,C130 to 0603 type	For commond design
5		P20	Change C215,C221,C395 to 0603 type	For commond design
6		P21	Change C231 to 0603 type	For commond design
7		P33	Change C519 to 0603 type	For commond design
8		P36	Change C568,C569 to 0603 type	For commond design
9		P37	Change C937,C954,C953 to 0603 type	For commond design
10		P39	Change C986 to 0603 type	For commond design
11		P40	Change C634,C635,C639 to 0603 type	For commond design
12		P41	Change C655 to 0603 type	For commond design
13		P48	Change C836,C837,C839,C840,C847 C848,C856,C857 to 0603 type	For commond design
14		P47	Change C906 to 0603 type	For commond design
15		P47	Modify gate powr rail of MOS to +5VALW	Avoid leakage issue.
16		P45	Change U39 source to SA00004KB00	For main source issue
17		P46	Change U40,U69 source to SA00004KB00	For main source issue
18		P37	Add Q150,R145,C976	For LAN power control
19		P42	Reserve LAN_PWR_ON# net on EC pin 89	For LAN power control
20		P41	Stuff R945,R481 for EAPD contact U8 pin29	For MUTE_LED issue
21		P38	Add R90	For LAN SURGE CO-LAY
22		P38	Add R1380	Atheros request

Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title	PIR (HW)		
Size: Custom	Document Number: LA-6882P		Rev: 1.0
Date: Monday, January 16, 2012	Sheet 62 of 64		

QIWY4 HW PIR List

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
				PVT TO SVT
1		P46	change JP21 type (SP010011A00)	For ASSY issue
2		P23	RV208 change to contact +VDD33MISC	For N13P-GT/N13E-GE shutdown issue
3		P23	Reserve RV14	For N13P-GT/N13E-GE +VDD33MISC leakage issue
4		P41	Swap HP R/L	For HP R/L reverse issue
5		P42	Add R1415,R1419	T/P SM BUS pull high voltage change

Compal Electronics, Inc.

Title: PIR (HW)

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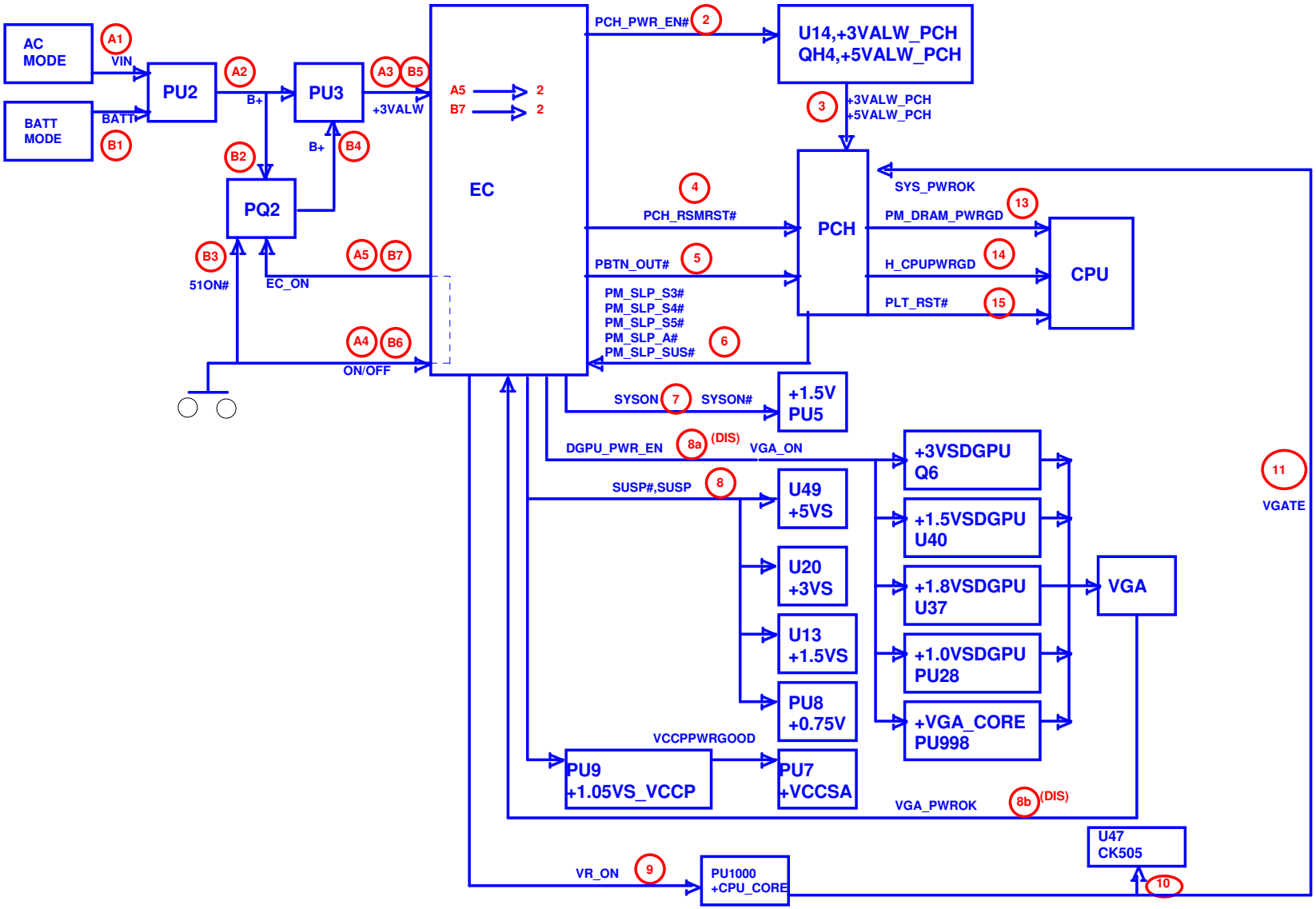

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