

Storm 2

UMA Schematics Document

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Storm2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover

Size
A4

Document Number

Storm 2

Rev
-1

Date: Wednesday, March 13, 2013

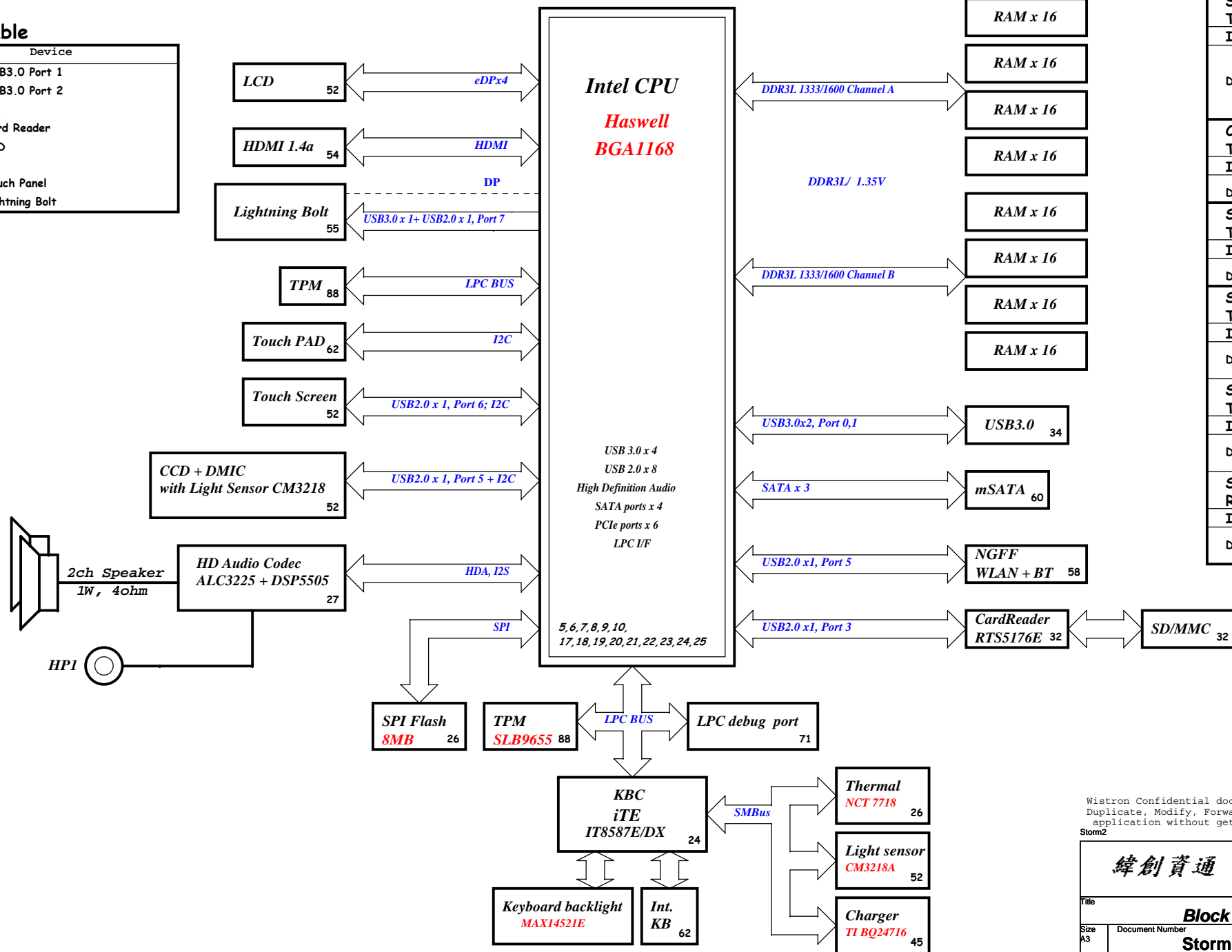
Sheet 1 of 102

Project code : 91.4LZ01.001
 PCB P/N : 12302-1
 Revision : 1

Storm 2 Block Diagram

USB Table

Pair	Device
0	USB3.0 Port 1
1	USB3.0 Port 2
2	NA
3	Card Reader
4	CCD
5	BT
6	Touch Panel
7	Lightning Bolt



CHARGER		BQ24737	44
INPUTS	OUTPUTS		
DCBATOUT	BT+		
SYSTEM DC/DC		TPS51285	45
INPUTS	OUTPUTS		
DCBATOUT	3D3V_DS _W , 3D3V_WLAN_50, MSATA_VDD, MSATA_VDD, 5V_DS _W , 5V_SS, USB30_VCC		
CPU DC/DC		TPS51622	46, 47
INPUTS	OUTPUTS		
DCBATOUT	VCC_CORE		
SYSTEM DC/DC		TPS51367	48
INPUTS	OUTPUTS		
DCBATOUT	1D05V_VTT		
SYSTEM DC/DC		TPS51367+TPS51206	49
INPUTS	OUTPUTS		
DCBATOUT	1D35V_S3, VDDQ_VREF, OD675V_S0		
SYSTEM DC/DC		TLV62065	51
INPUTS	OUTPUTS		
DCBATOUT	1d5V_S0		
SYSTEM DC/DC		RT9013	58
INPUTS	OUTPUTS		
DCBATOUT	1d8V_S0		

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Block Diagram	
Title	
Size A3	Document Number
Storm 2	
Date: Wednesday, March 13, 2013	Sheet 2 of 102
Rev	-1

5
4 3 2 1
SSID = CPU

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Storm2

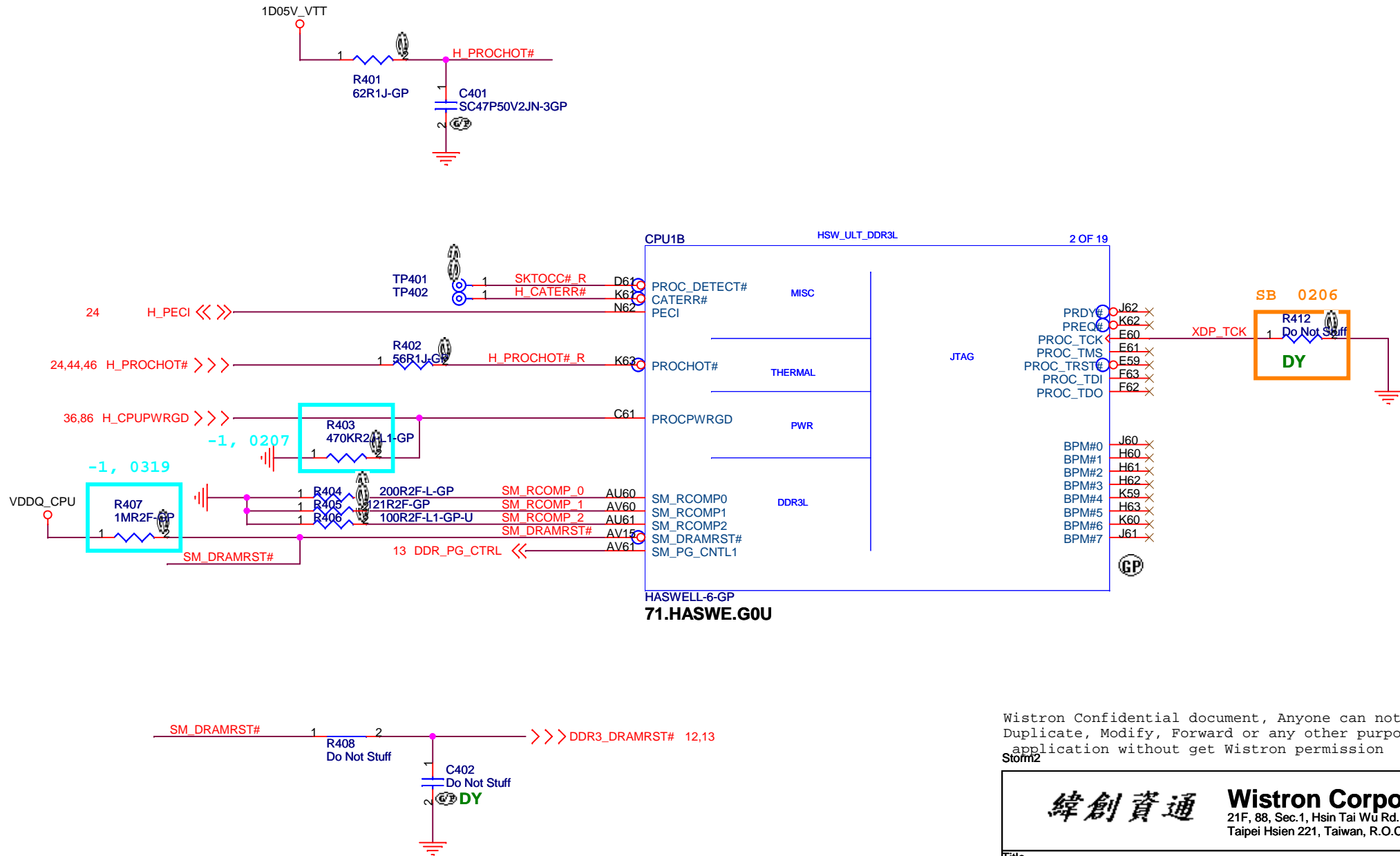
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Title **CPU (Reserved)**

Size A4	Document Number Storm 2	Rev -1
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Date: Friday, December 28, 2012 Sheet 3 of 102

SSID = CPU



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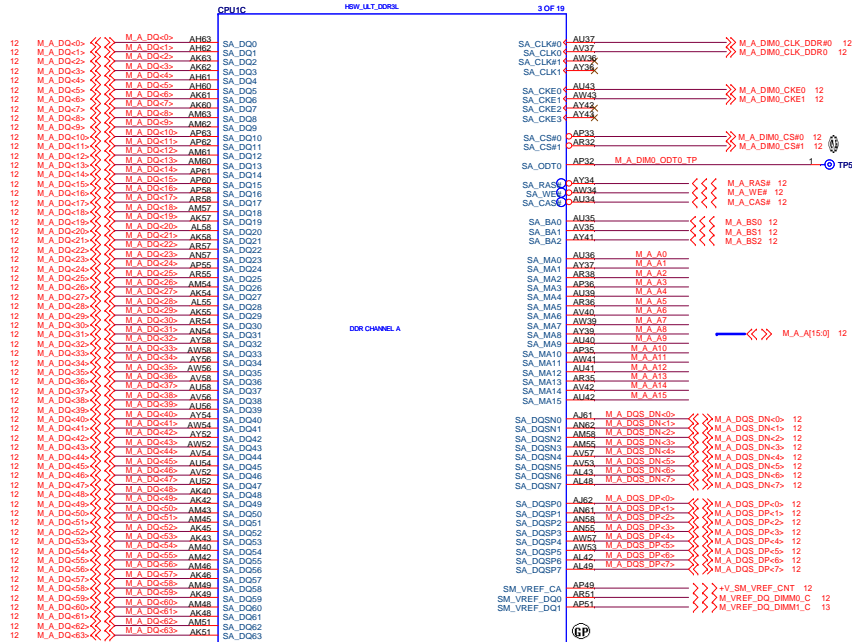

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Title **CPU (THERMAL/CLOCK/PM)**

Size A4 Document Number **Storm 2** Rev **-1**

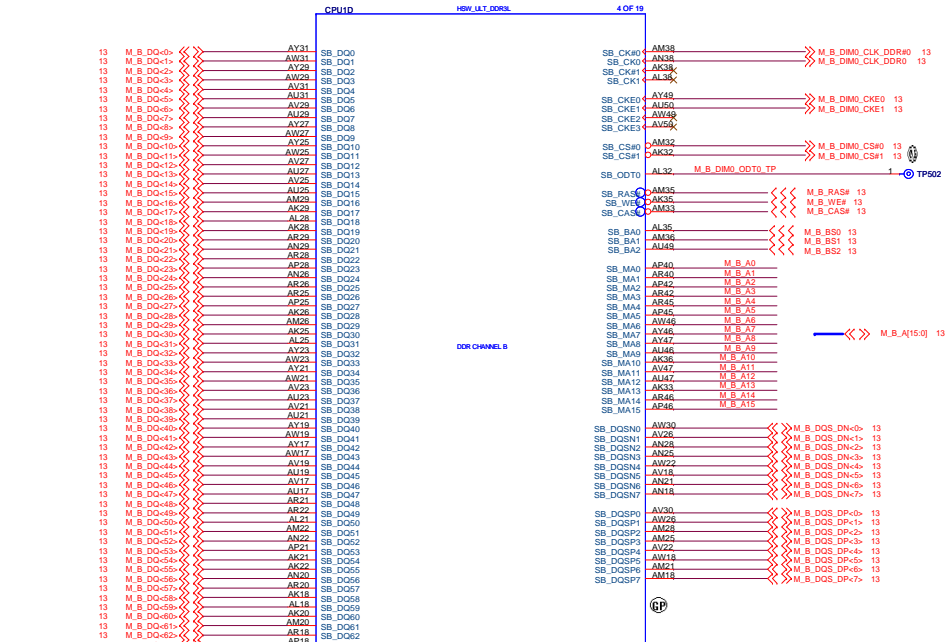
Date: Tuesday, April 02, 2013 Sheet 4 of 102

SSID = CPU



HASWELL-6-CP

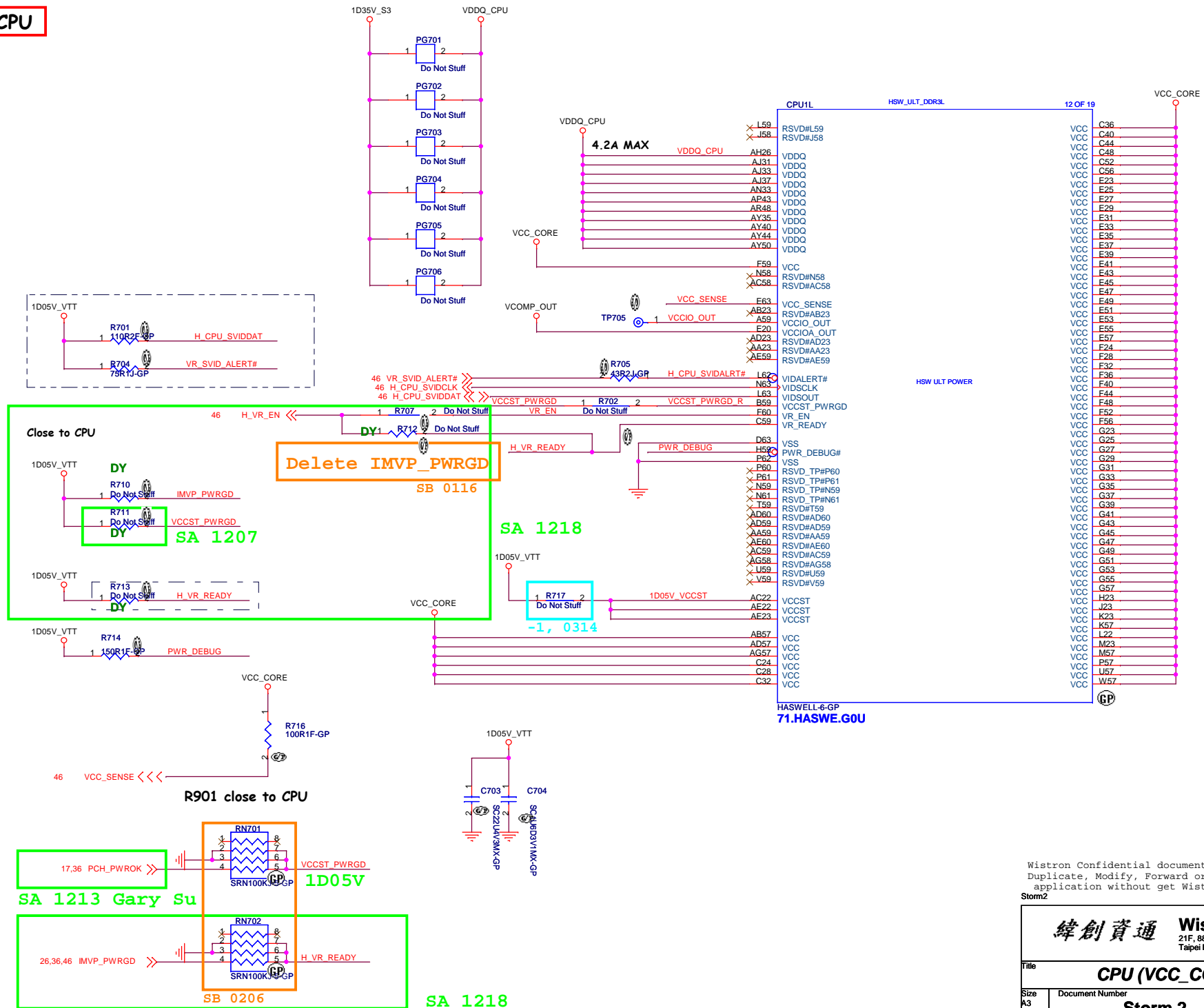
71.HASWELL.G00



HASWELL-6-CP

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SSID = CPU



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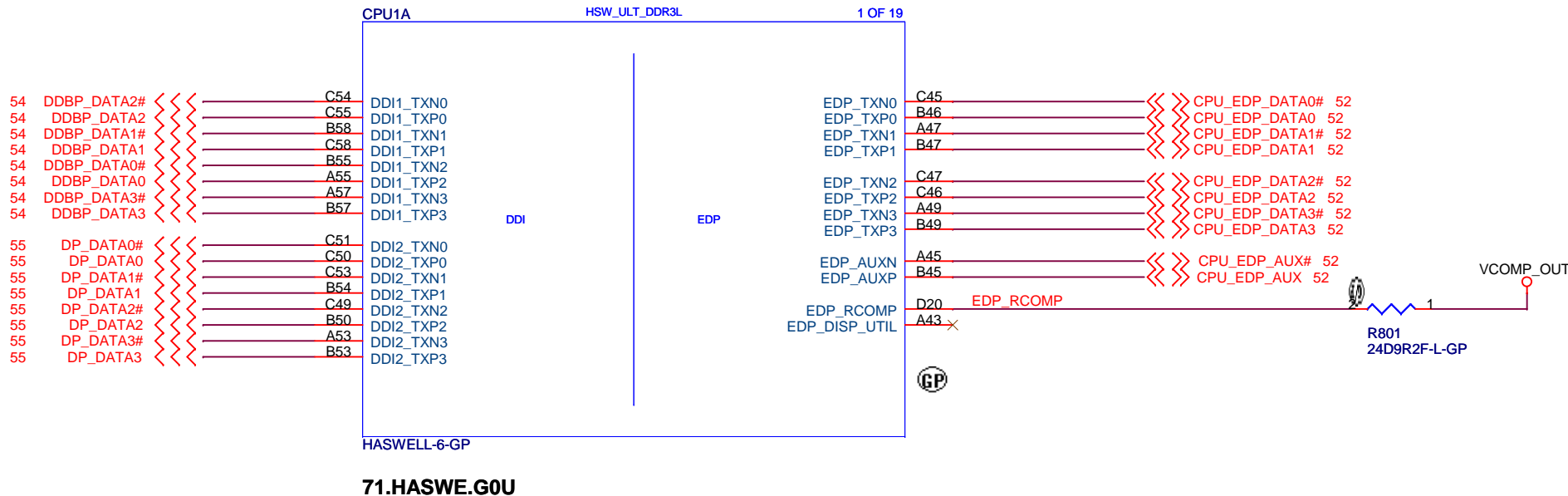
Title: **CPU (VCC_CORE)**

Size A3	Document Number	Rev
	Storm 2	-1
Date: Tuesday, April 02, 2013	Sheet 7 of 102	

SSID = CPU


HDMI

Lightning Bolt

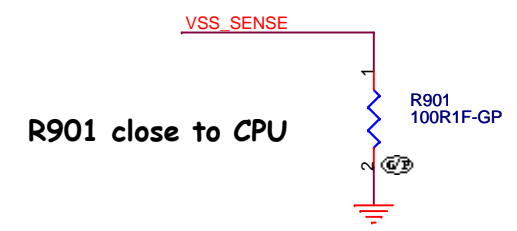
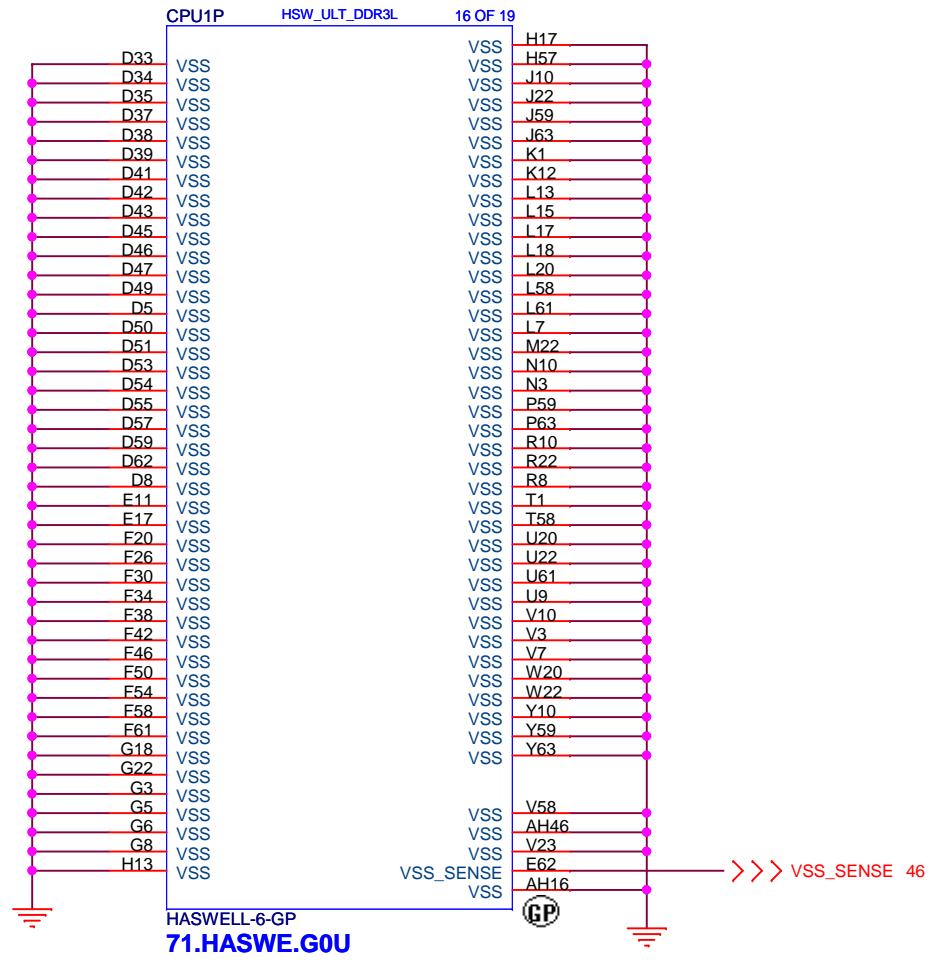


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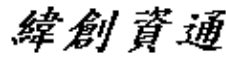
Storm2

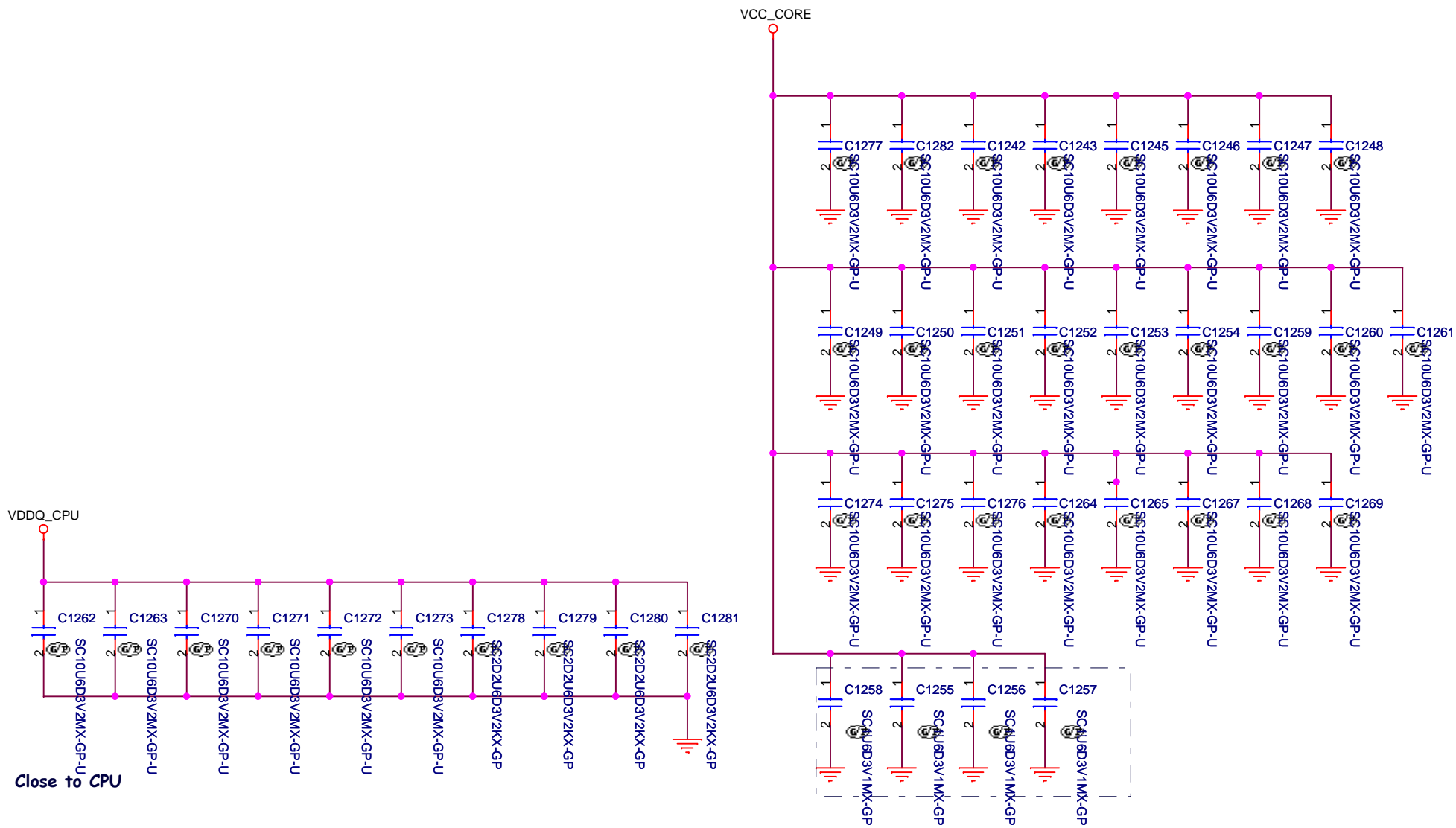
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CPU (DDI/EDP)		
Size A4	Document Number Storm 2	Rev -1
Date: Tuesday, April 02, 2013		Sheet 8 of 102

SSID = CPU

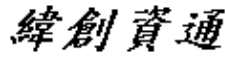


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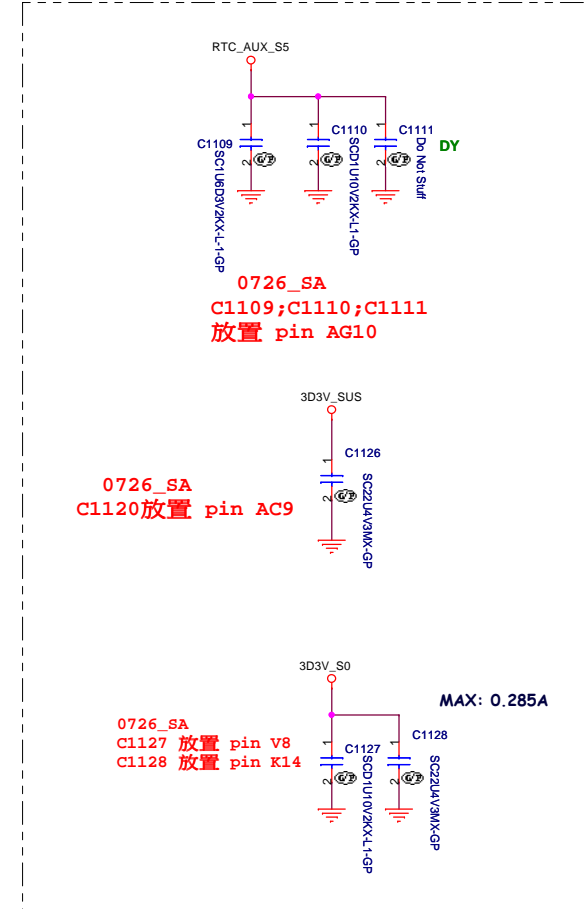
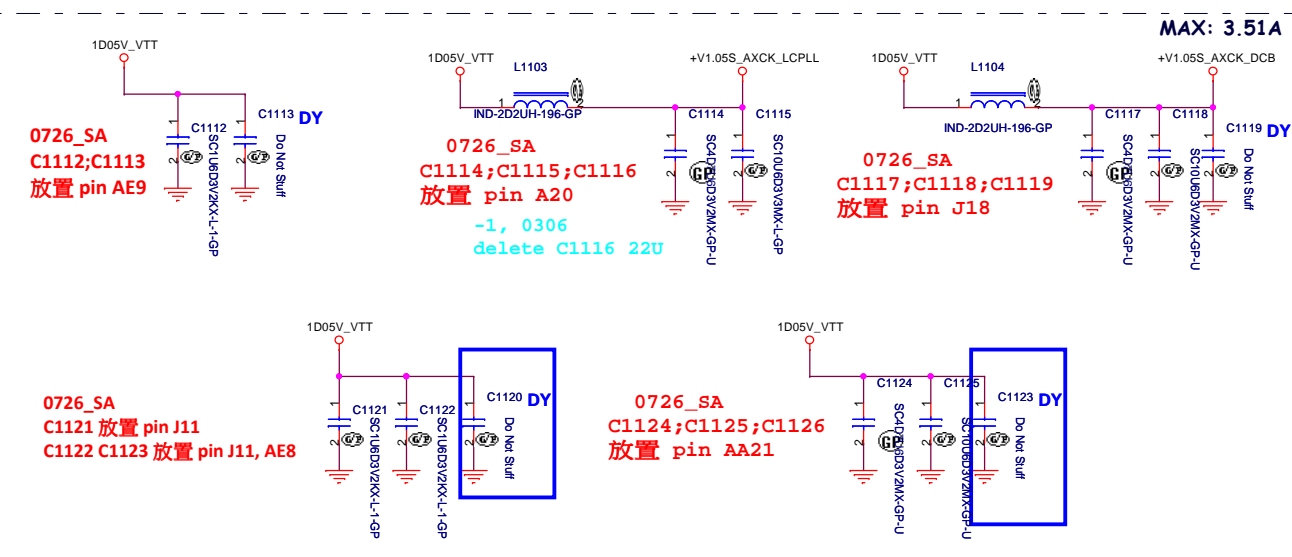
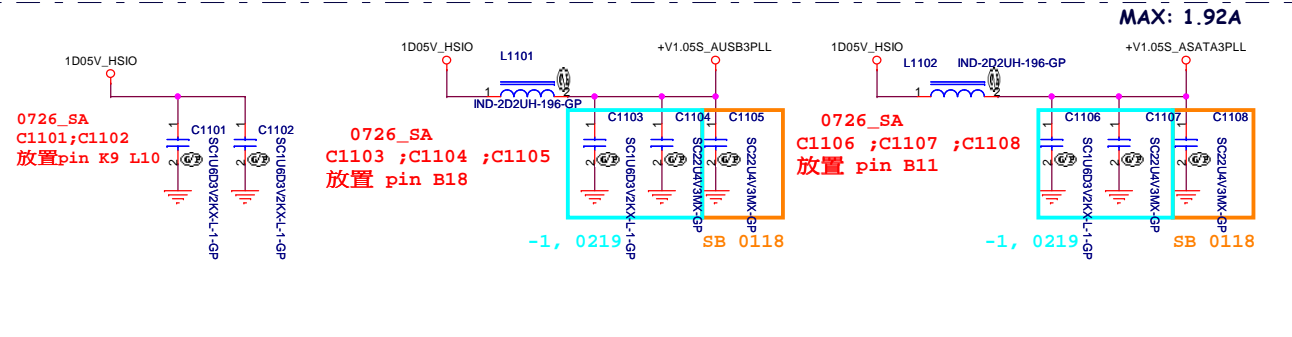
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CPU (VSS)		
Size A4	Document Number Storm 2	Rev -1
Date: Tuesday, April 02, 2013		Sheet 9 of 102



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CPU (Power CAP1)		
Size A4	Document Number	Rev -1
Date: Monday, February 04, 2013	Sheet 10 of 102	

0726_SA 擺放電容的位置請參考Page 21
每個位置如下



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<p>緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>Title PCH (Power CAP2)</p>	
<p>Size A3</p>	<p>Document Number Storm 2</p>
<p>Date: Wednesday, March 06, 2013</p>	<p>Rev -1</p>
<p>Sheet 11 of 102</p>	

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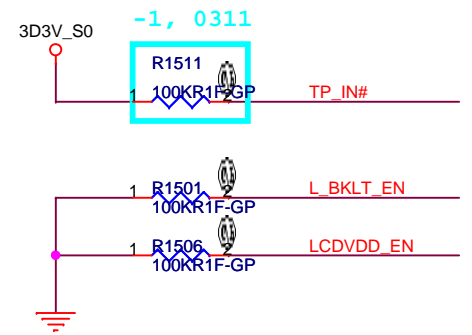
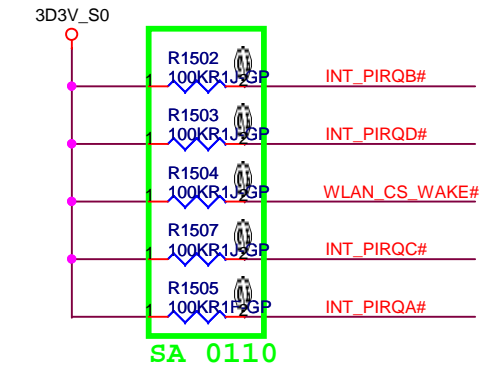
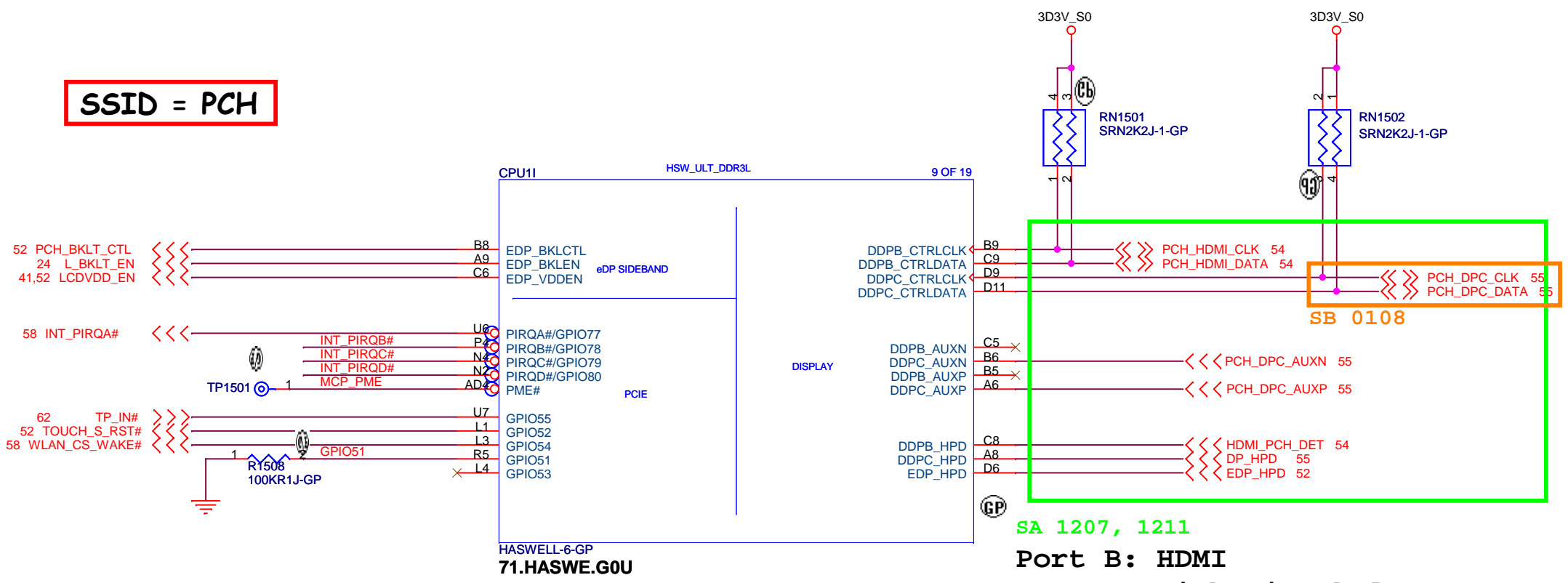
Storm2

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Title **SODIMM3_SODIMM4 (Reserved)**

Size A4	Document Number Storm 2	Rev -1
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SSID = PCH



SA 1207, 1211
 Port B: HDMI
 Port C: Lightning bolt

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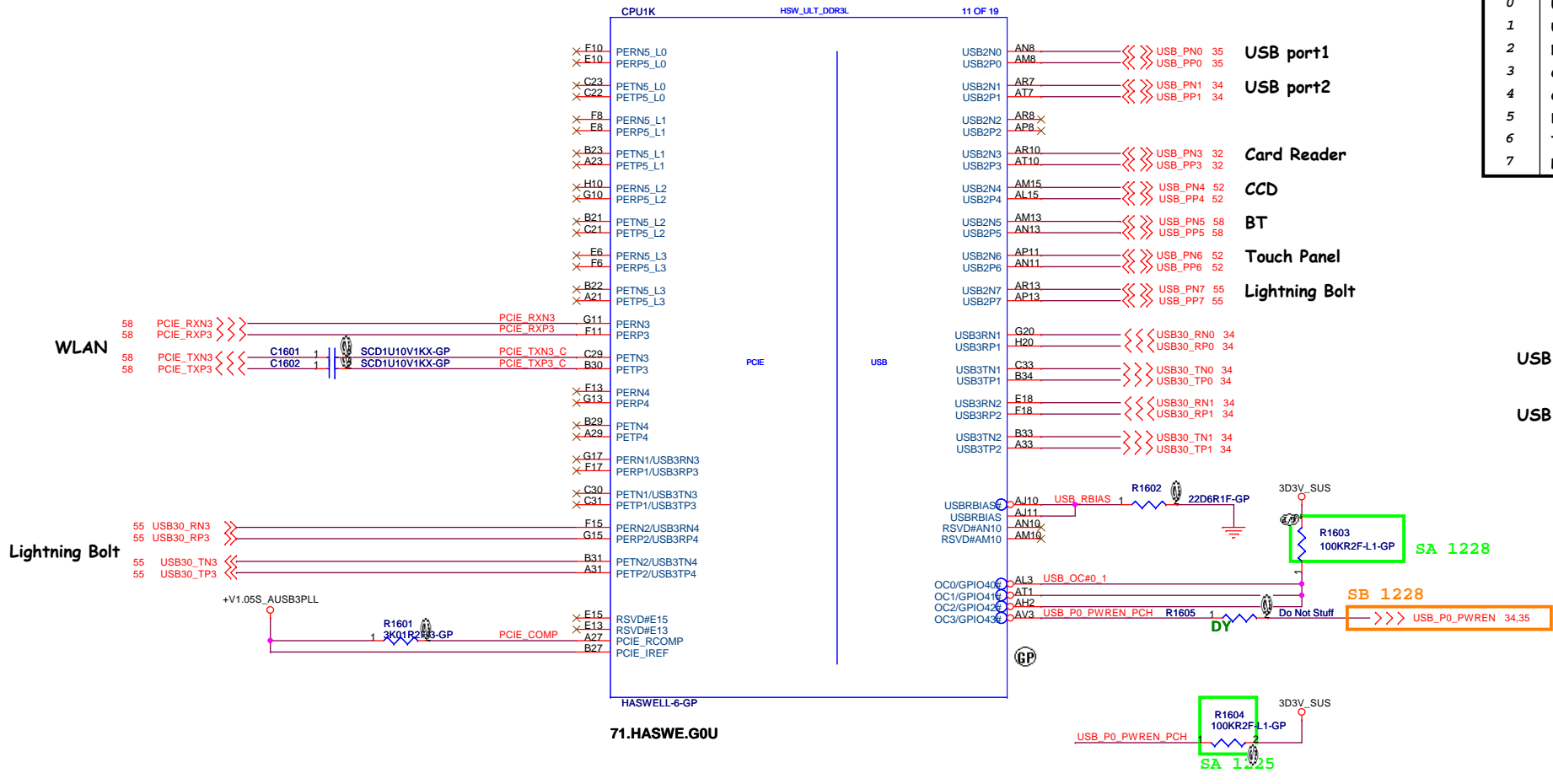
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title PCH (DDI)		
Size A4	Document Number Storm 2	Rev -1
Date: Tuesday, April 02, 2013	Sheet 15	of 102

SSID = PCH

USB Table

Pair	Device
0	USB3.0 Port 1
1	USB3.0 Port 2
2	NA
3	Card Reader
4	CCD
5	BT
6	Touch Panel
7	Lightning Bolt

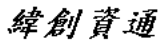


USB port1
USB port2

SA 1228
SB 1228
Do Not Stuff
USB_P0_PWREN 34,35

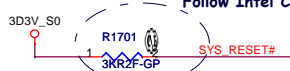
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CPU (PCI/USB)	
Title	
Size A3	Document Number
Date: Tuesday, April 02, 2013	Storm 2
Sheet 16 of 102	Rev -1

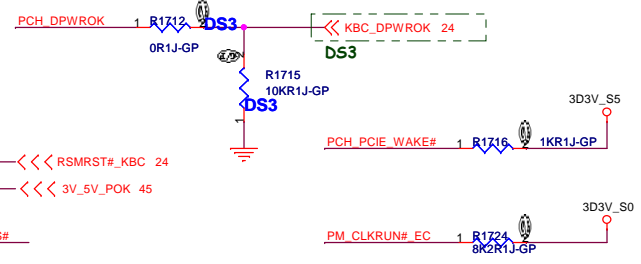
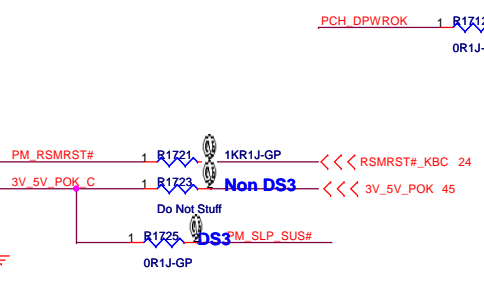
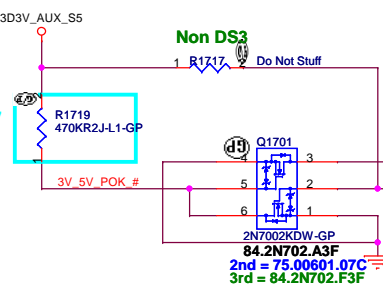
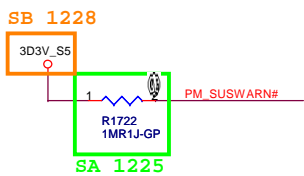
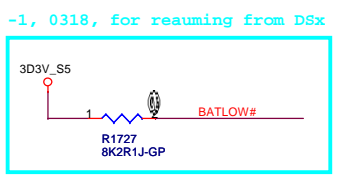
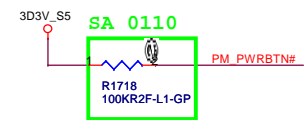
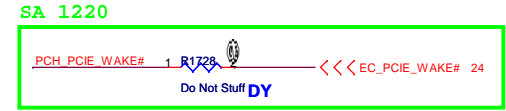
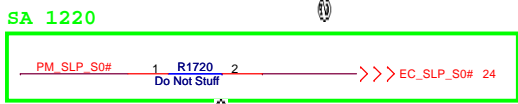
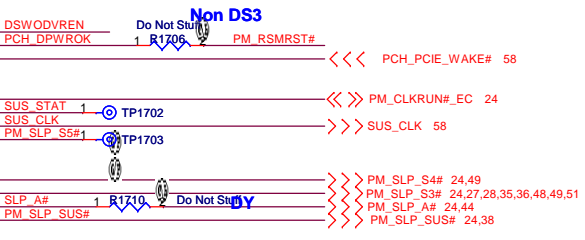
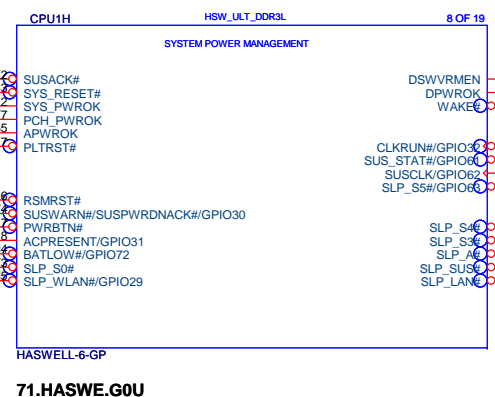
SSID = PCH

Follow Intel CRB



DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

SA 1214 Delete IMVP_PWRGD



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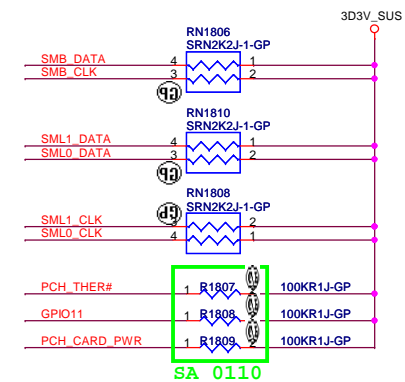
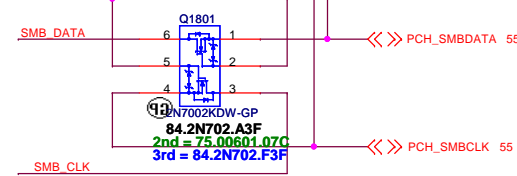
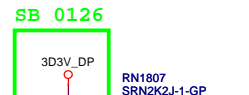
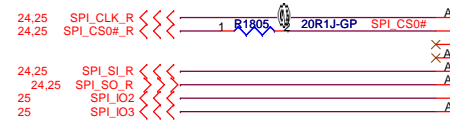
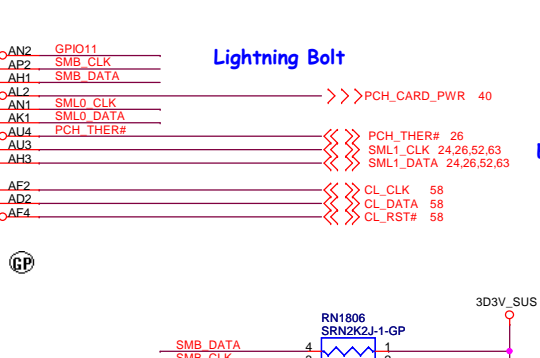
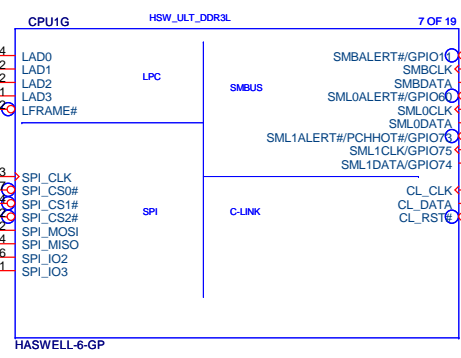
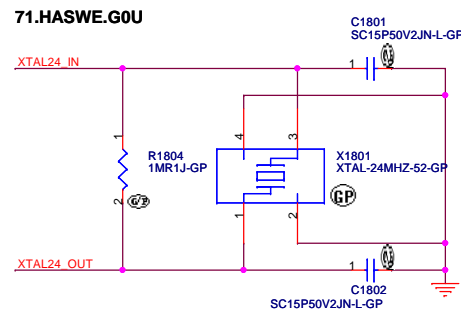
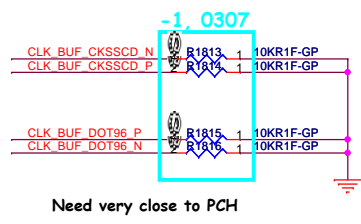
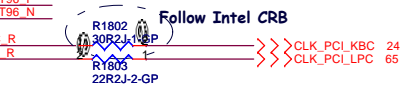
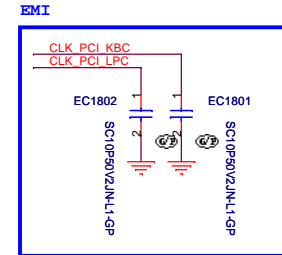
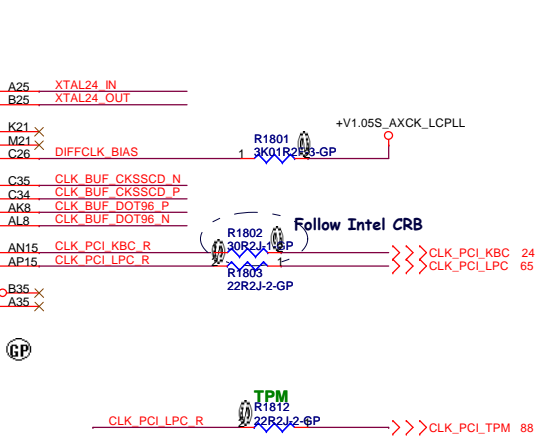
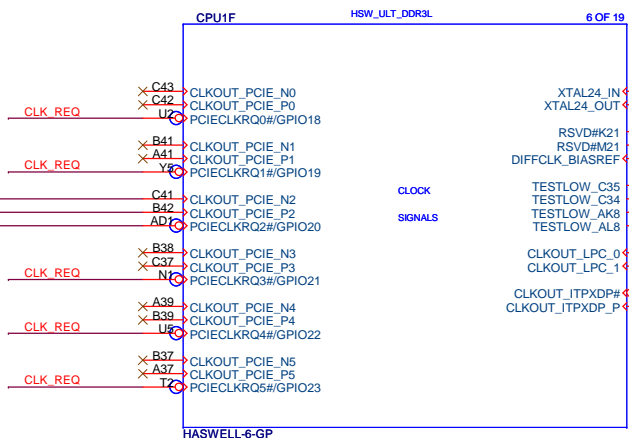
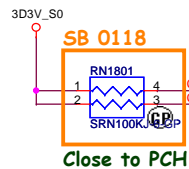
Storm2

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Title	PCH (PM)	
Size	Document Number	Rev
A3	Storm 2	-1
Date:	Wednesday, April 03, 2013	Sheet 17 of 102

SSID = PCH

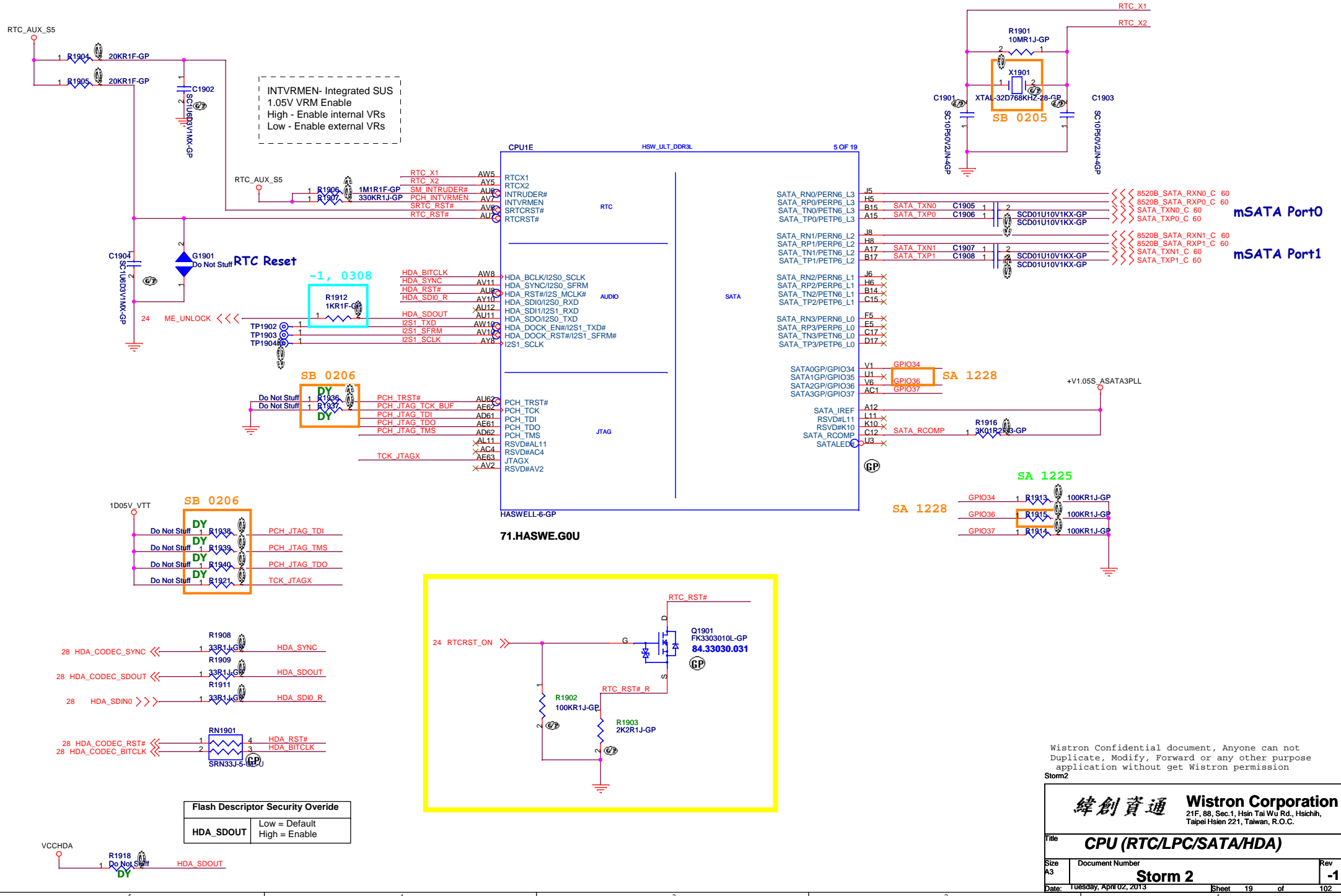
WLAN



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PCH (PCI-E/SMBUS/CLOCK/CL)	
Title	Rev
Storm 2	
Size A3	-1
Date: Tuesday, April 02, 2013	Sheet 18 of 102

SSID = PCH



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Storm2

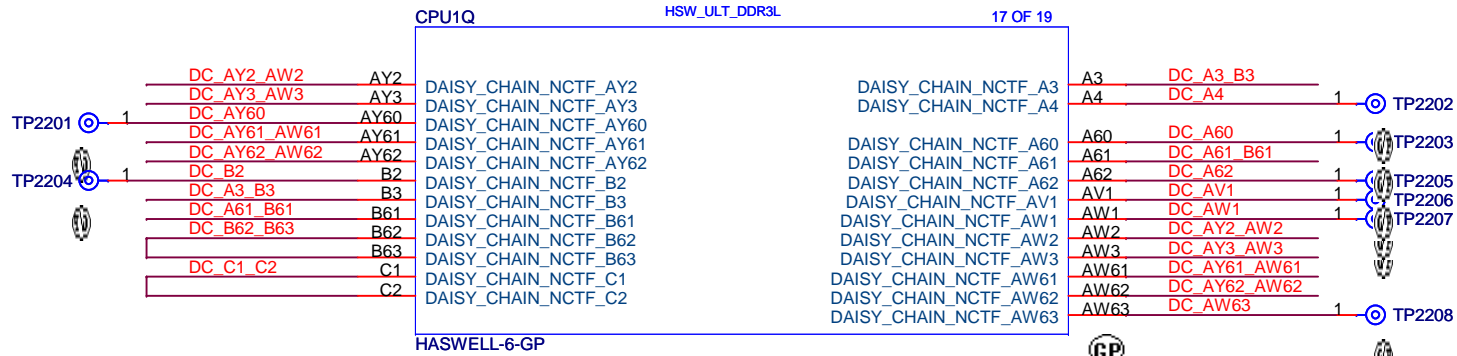
緯創資通 Wistron Corporation
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Title: **CPU (RTC/LPC/SATA/HDA)**

Size A3 Document Number: **Storm 2** Rev: **-1**

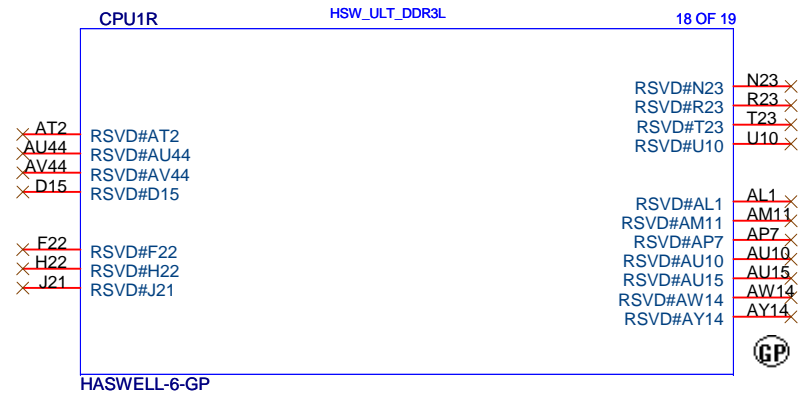
Date: Tuesday, April 02, 2013 Sheet 19 of 102

SSID = CPU



HASWELL-6-GP

71.HASWE.G0U




HASWELL-6-GP

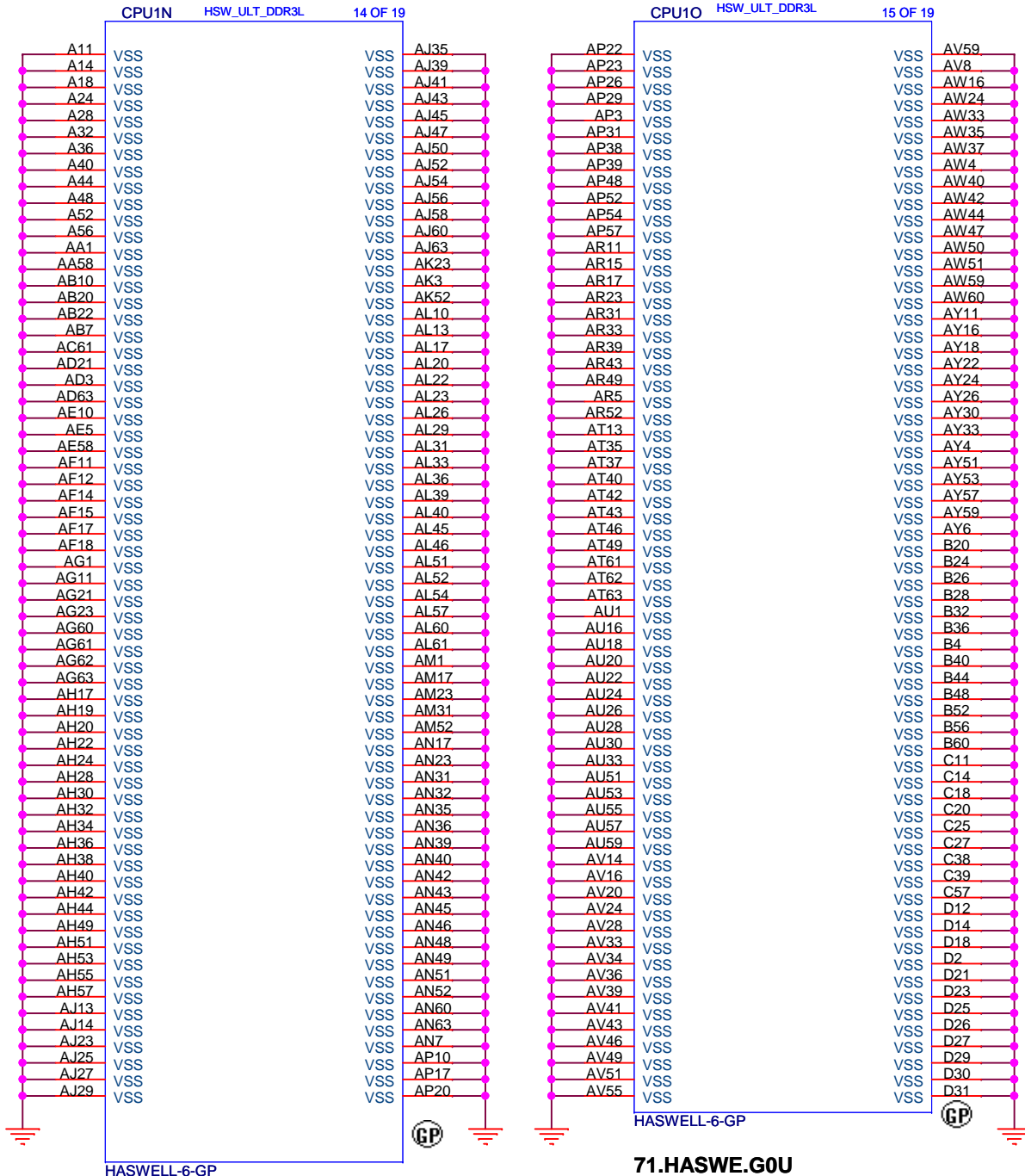
71.HASWE.G0U

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Title CPU (RSVD)		
Size A4	Document Number Storm 2	Rev -1
Date: Friday, February 01, 2013		Sheet 22 of 102

SSID = PCH



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Title **PCH (VSS)**

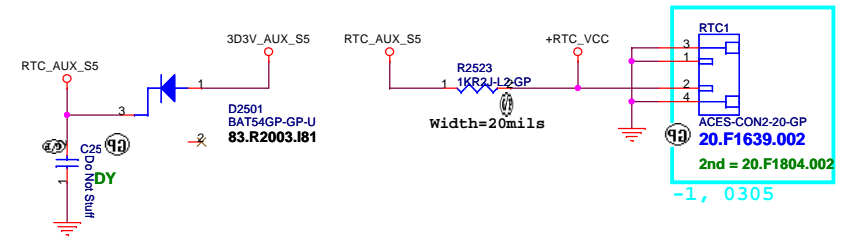
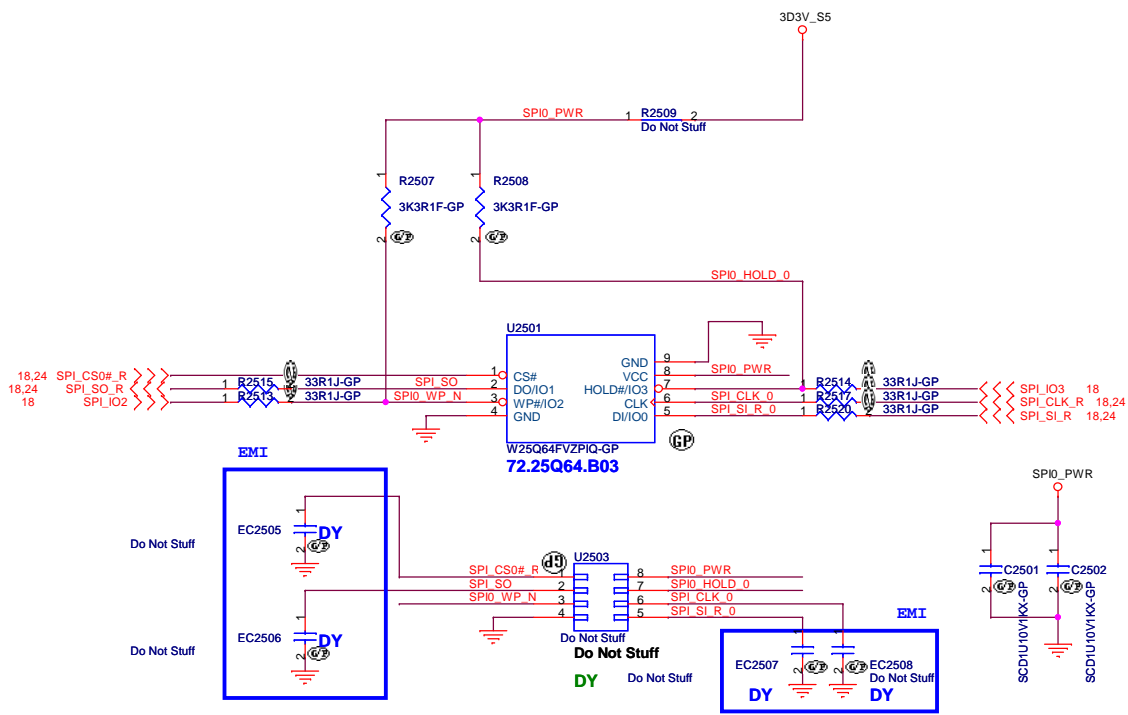
Size A4	Document Number Storm 2	Rev -1
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SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH

SSID = RBAT

SPI ROM Equal length need to less than 500mil

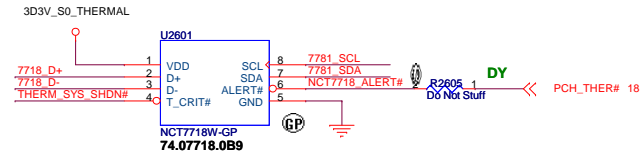
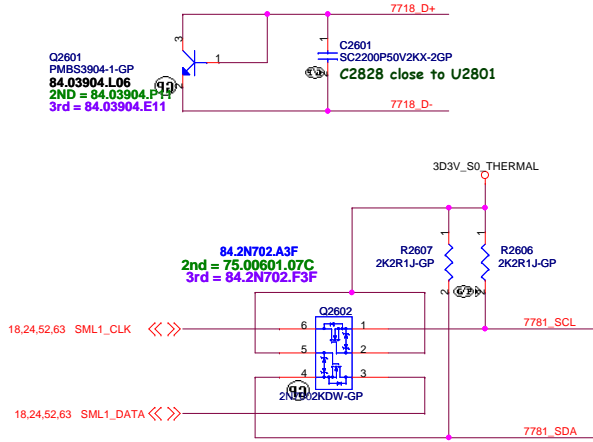


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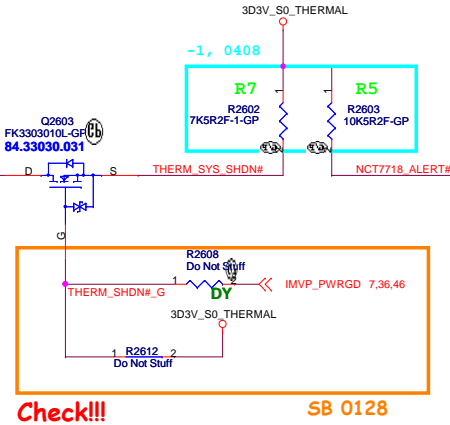
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Flash/RTC			
Title	Document Number		Rev
	Storm 2		-1
Date: Tuesday, April 02, 2013	Sheet	25	of 102

SSID = Thermal



- Layout notice :
- * Put the C1 2200pF to close the nct7718W
 - * Add ground shielding for D+ and D- traces
 - * D+/D- route has to be away from the high noise area
 - * The recommended traces width and ground shielding spacing are 10mils



Check!!! SB 0128

Setting 91°C

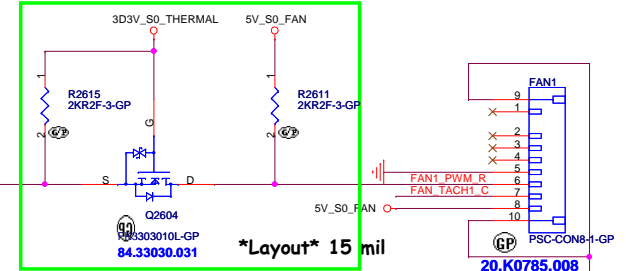
R7

The default value is trapping after power up 100ms by different pull-up resistors of T_CRIT# and ALERT# pin:

TEMPERATURE (°C)	T_CRIT#					
	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ	
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

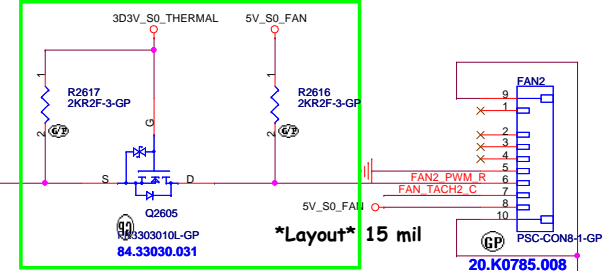
R5

SA 1222



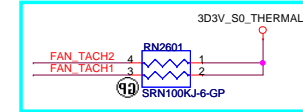
Layout 15 mil

SA 1222



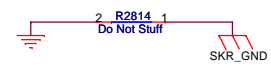
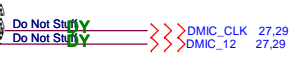
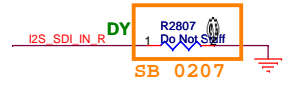
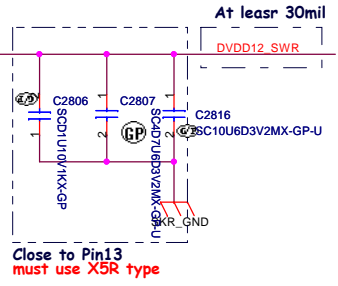
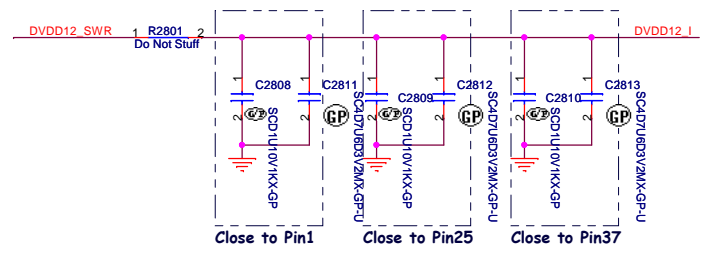
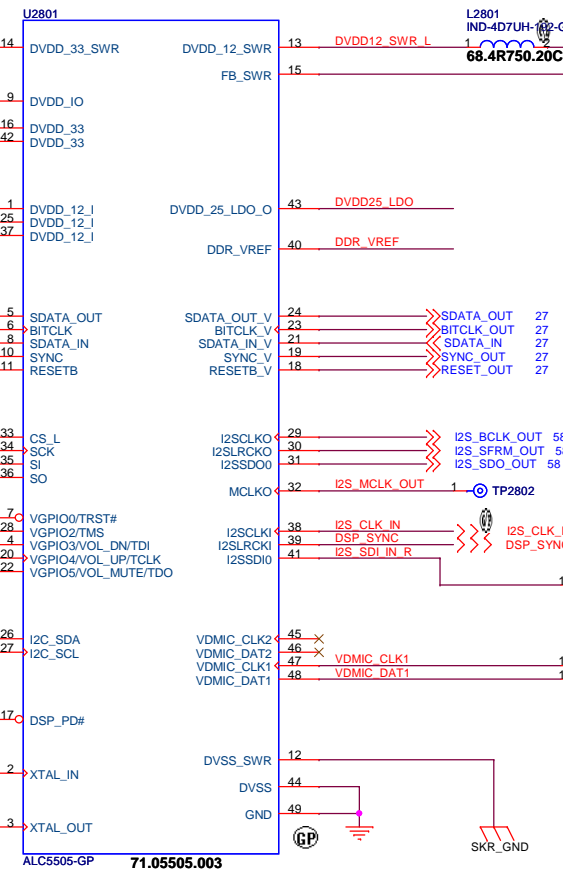
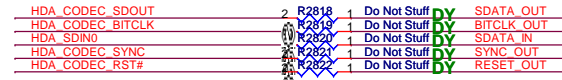
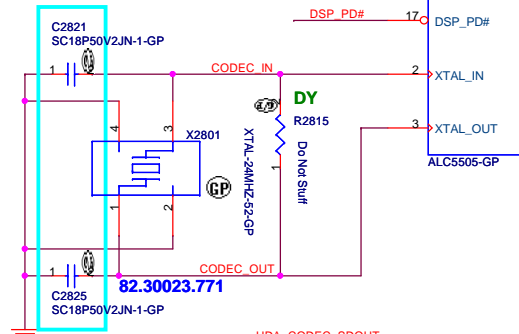
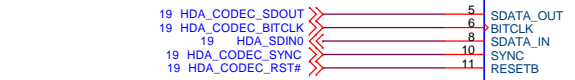
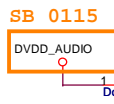
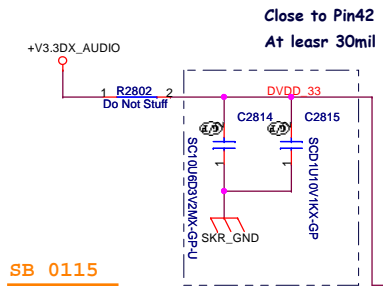
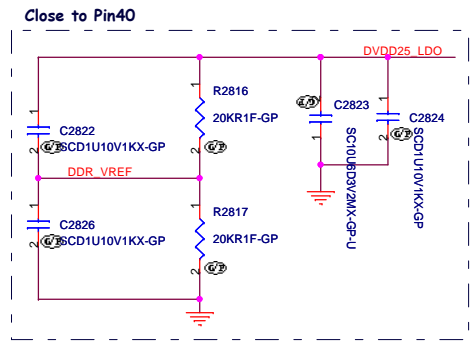
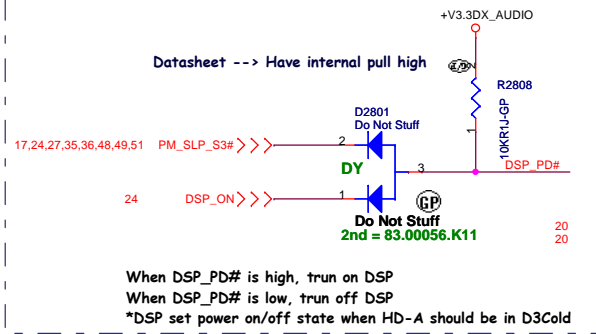
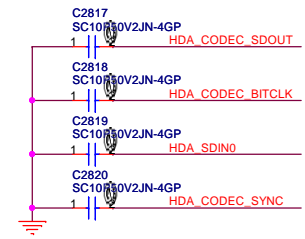
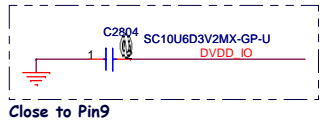
Layout 15 mil

-1, 0206



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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsein 221, Taiwan, R.O.C.
Title	NUVOTON_NCT7718W	
Size	Document Number	Rev
Custom	Storm 2	-1
Date:	Monday, April 08, 2013	Sheet 26 of 102



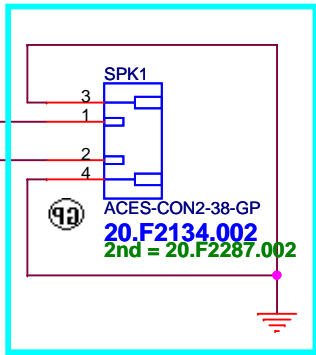
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AUDIO_DSP5505 (Reserved)			
Title	Document Number		
Size A3	Storm 2		Rev -1
Date: Tuesday, April 02, 2013	Sheet 28	of 102	

SSID = AUDIO

Speaker

27 AUD_SPK_L- >>>
27 AUD_SPK_L+ >>>

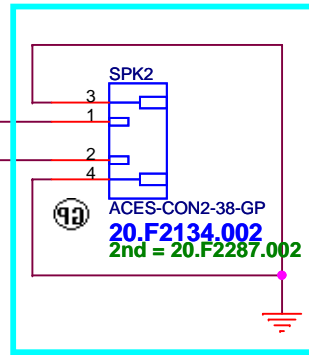


Layout Note:

Trace width=40mil

-1, 0305

27 AUD_SPK_R- >>>
27 AUD_SPK_R+ >>>



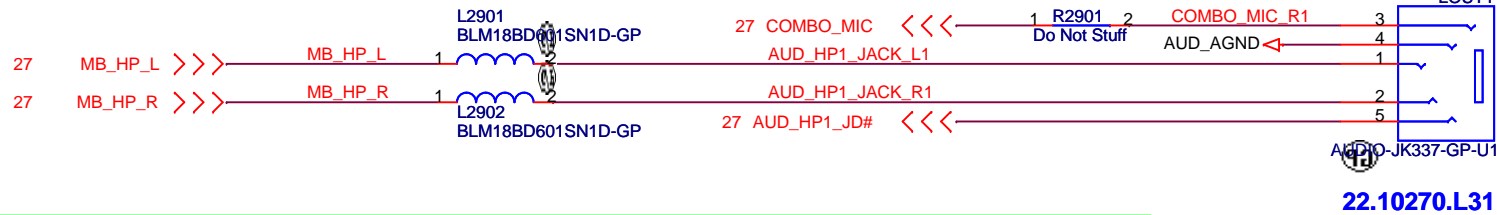
Layout Note:

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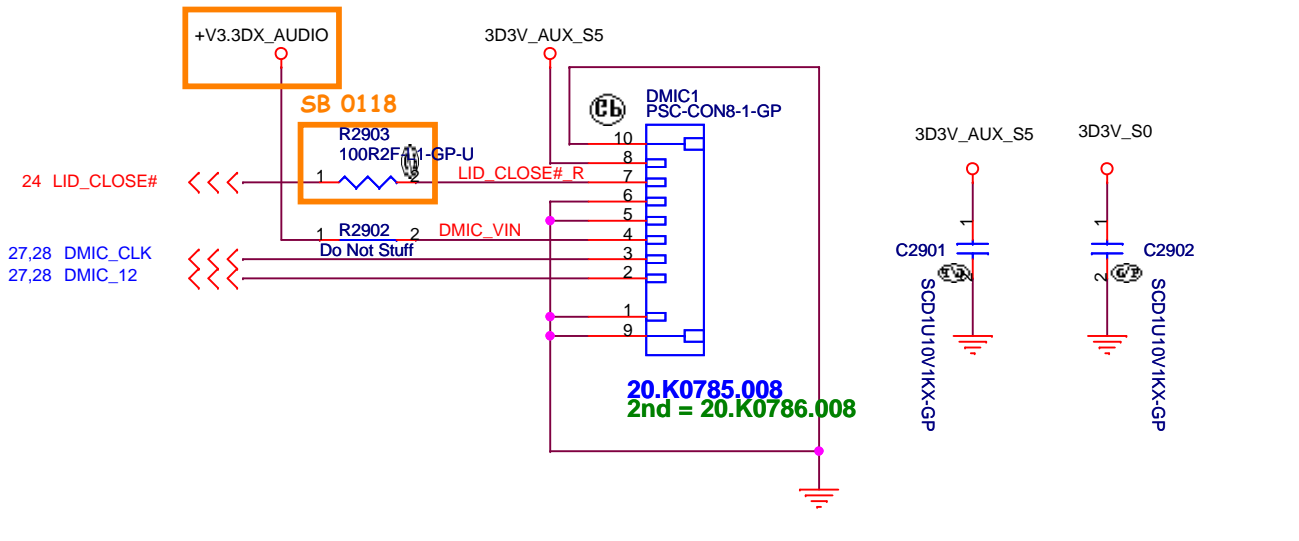
-1, 0305

Combo Jack

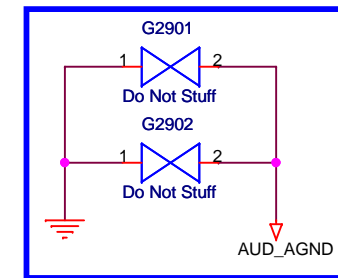
600ohm 100MHz
200mA 0.5ohm DC



DMIC & Hall Sensor



EMI



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Title **Audio Jack & Hall Sensor**

Size A4 Document Number **Storm 2** Rev **-1**

Date: Tuesday, April 02, 2013 Sheet 29 of 102

SSID = User.Interface

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Title **LAN (Reserved)**

Size A4	Document Number Storm 2	Rev -1
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Date: Friday, December 28, 2012 Sheet 30 of 102

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Title

RJ45 + Transformer (Reserved)

Size

Document Number

Rev

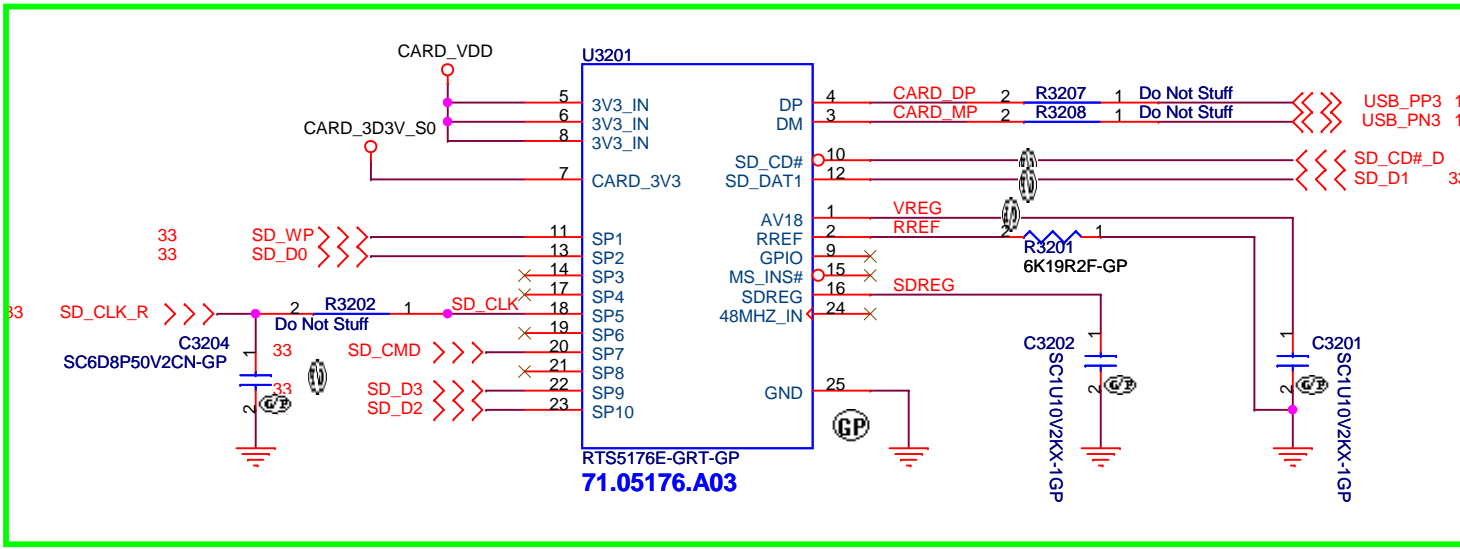
A

Storm 2

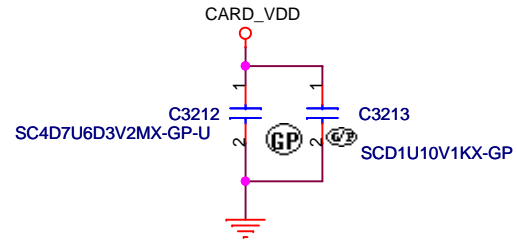
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Date: Friday, December 28, 2012

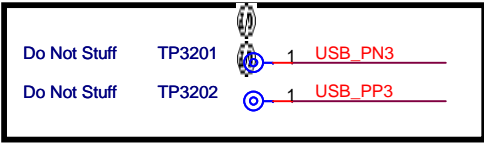
Sheet 31 of 102



SA 0104



FOR SIV, PLS near U3201



Pin#	Name	I/O Type	Description
1	AV18	O	Internal regulator for Analog blocks. An external capacitor should be connected
2	RREF	I	Connect external resistor (6.2K ± 1%) to reference ground
3	DM	I/O	USB2.0 D- signal
4	DP	I/O	USB2.0 D+ signal
5	3V3_IN	I	3.3V power input
6	3V3_IN	I	3.3V power input
7	CARD_3V3	O	3.3V power supplied for all media cards
8	3V3_IN	I	3.3V power input
9	GPIO	I/O	General purpose input/output. Now it's used for LED blinking
10	SD_CD#	I	SD Card Detect pin
11	SP1	I/O	SD Write Protect pin and MS Data 1
12	SD_DAT1	I/O	SD/MMC Data 1
13	SP2	I/O	SD/MMC Data 0 and MS Data 5
14	SP3	I/O	MMC Data 7 and MS Data 4
15	MS_INS#	I	MS Card Detect pin
16	SDREG	O	Internal regulator for SD card. An external capacitor should be connected
17	SP4	I/O	MMC Data 6 and MS Data 0
18	SP5	I/O	SD/MMC Clock pin and MS Data 2
19	SP6	I/O	MMC Data 5 and MS Data 6
20	SP7	I/O	SD/MMC Command pin and MS Data 3
21	SP8	I/O	MMC Data 4 and MS Data 7
22	SP9	I/O	SD/MMC Data 3 and MS Clock pin
23	SP10	I/O	SD/MMC Data 2 and MS BS pin
24	48MHz_In	I	48MHz clock input
	Exposed PAD		The Exposed PAD must be connected to the reference ground

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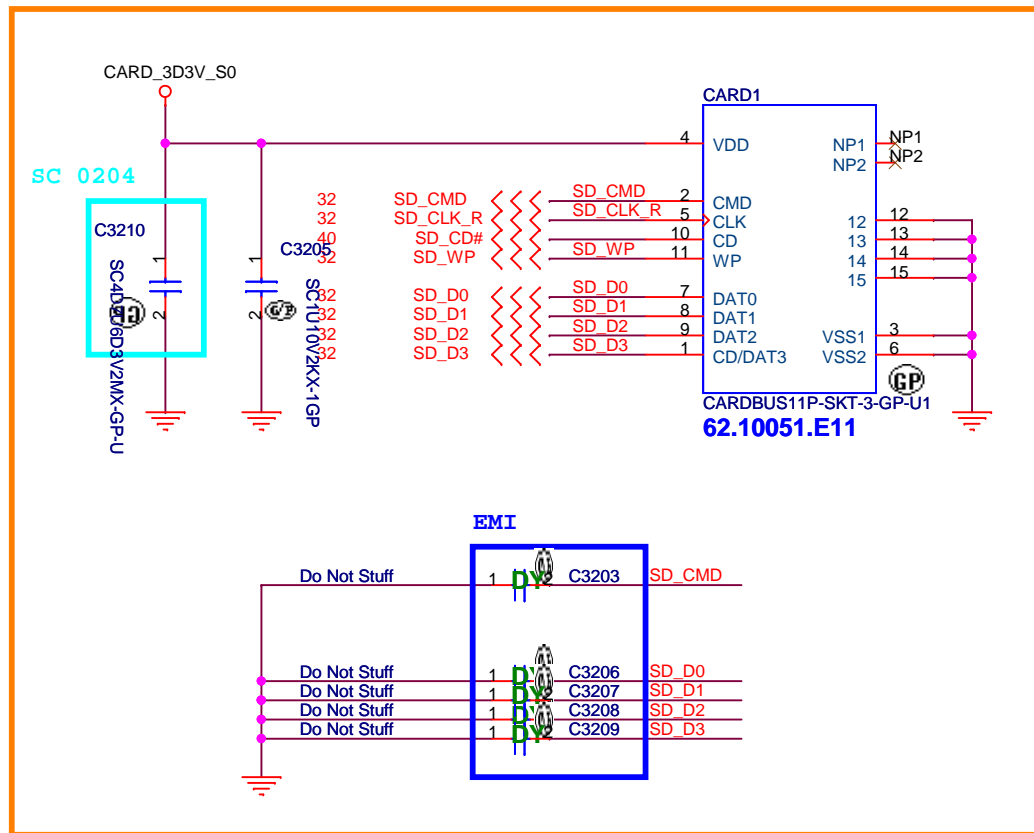
Title: **CARD READER_RTS5176E**

Size: A4 Document Number: **Storm 2** Rev: **-1**

Date: Tuesday, April 02, 2013 Sheet 32 of 102

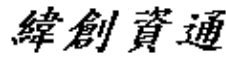
SD Card Reader CONN.

SB 1228



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Storm2

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Title CARD Reader CONN.	
Size A4	Document Number Storm 2
Date: Tuesday, April 02, 2013	Rev -1
Sheet 33 of 102	

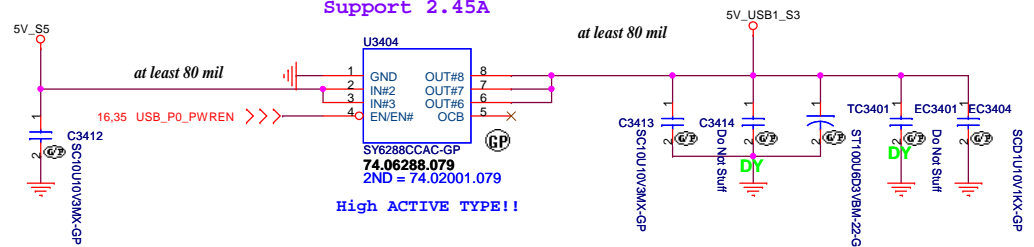
SSID = USB

JE40 modify

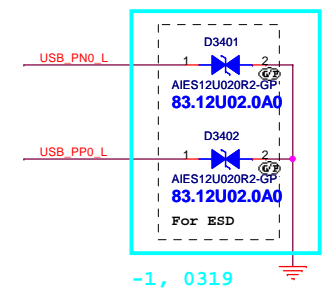
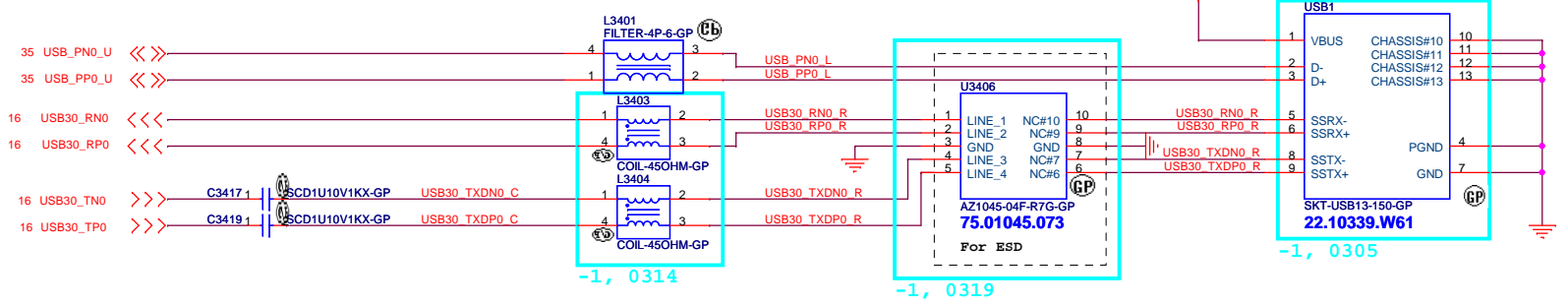
USB 3.0 Connector Pin definition

1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX-
6	StdA_SSRX+
7	GND
8	StdA_SSTX-
9	StdA_SSTX+

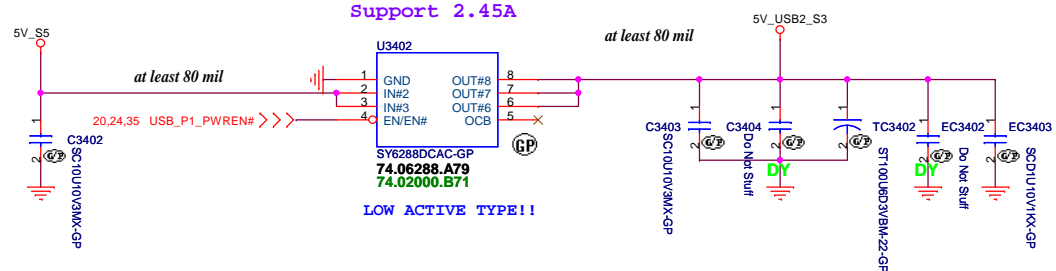
Change Main source Support 2.45A



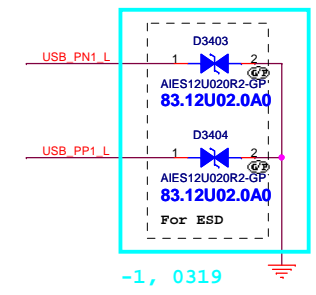
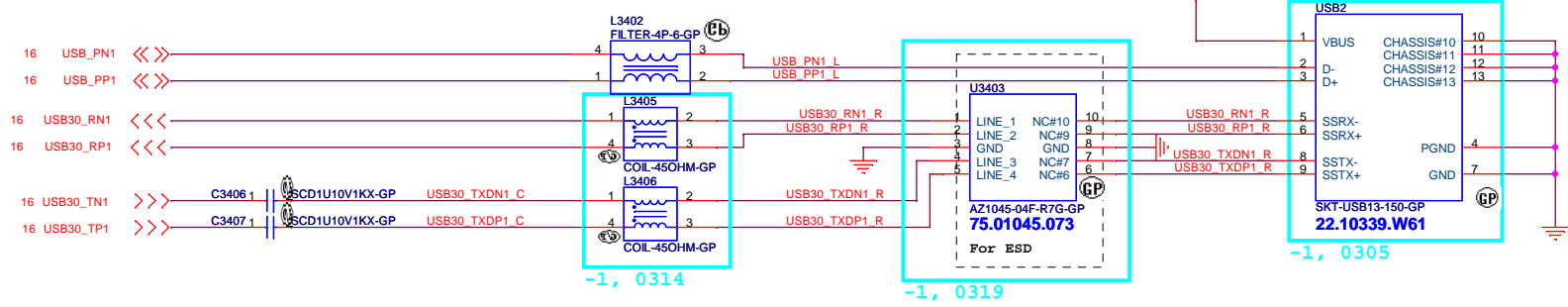
USB Charger Port USB3.0 Port1



Change Main source Support 2.45A



USB3.0 Port2

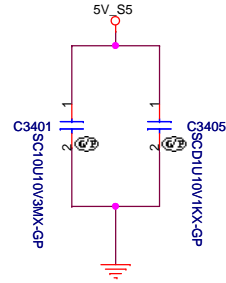


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Title			USB 3.0 Port
Size A3	Document Number	Rev	-1
Date: Tuesday, April 02, 2013			Sheet 34 of 102

USB Charger



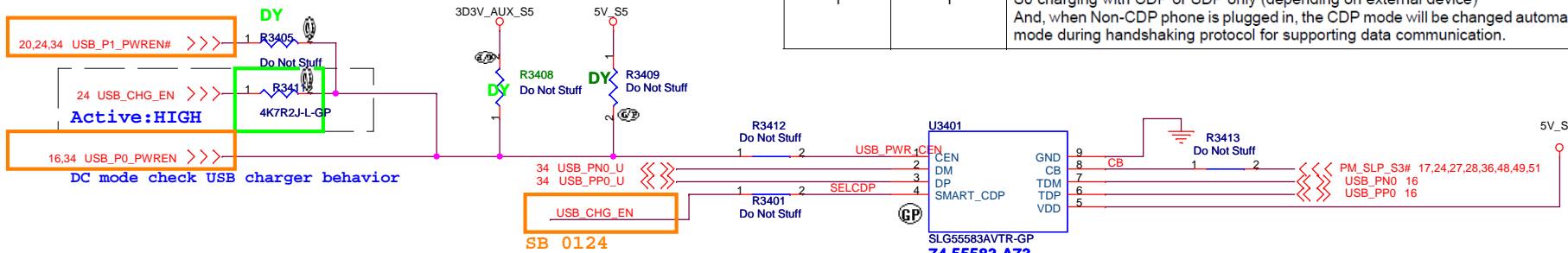
Pin Description - SLG55583A

Pin Define The symbol by pin number.

Pin #	Name	Type	Description
1	CEN	Output	N-FET Open Drain Output. Current Limit Switch (CLS) Control Output. CB changes from 0 to 1 or 1 to 0. CEN will be low for 2 seconds (typ)
2	DM	Input/Output	USB Connector D-
3	DP	Input/Output	USB Connector D+
4	SMART-CDP	Input	Input Control logic (see truth table)
5	VDD	PWR	Power Supply. Connect a 0.1μF capacitor between VDD and GND as close as possible to the device.
6	TDP	Input/Output	Host USB Transceiver D+ Connection
7	TDM	Input/Output	Host USB Transceiver D- Connection
8	CB	Input	Switch Control Bit 0 = autodetection charger identification active 1 = charging downstream port with active USB2.0 data communication mode with 1.5A support
9	Thermal Pad	GND	Ground

Truth Table

CB	SMART-CDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device) And, when Non-CDP phone is plugged in, the CDP mode will be changed automatically to SDP mode during handshaking protocol for supporting data communication.

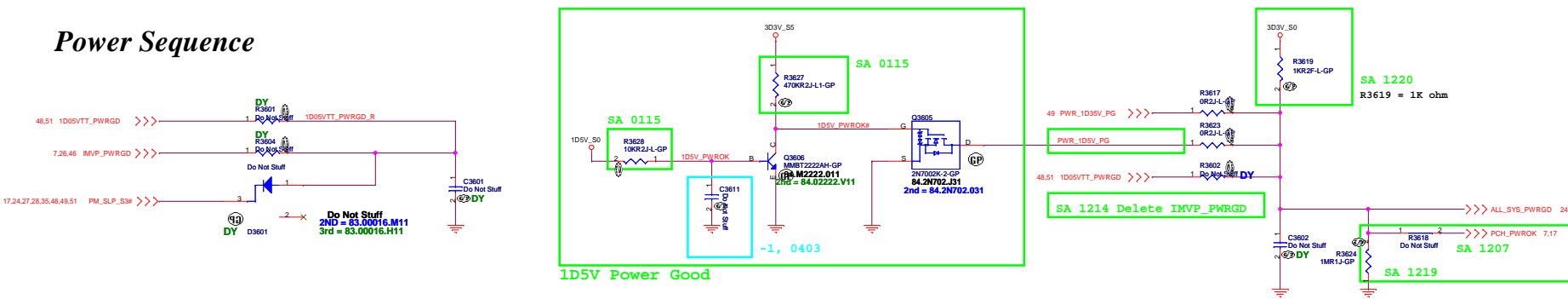


SB 1228

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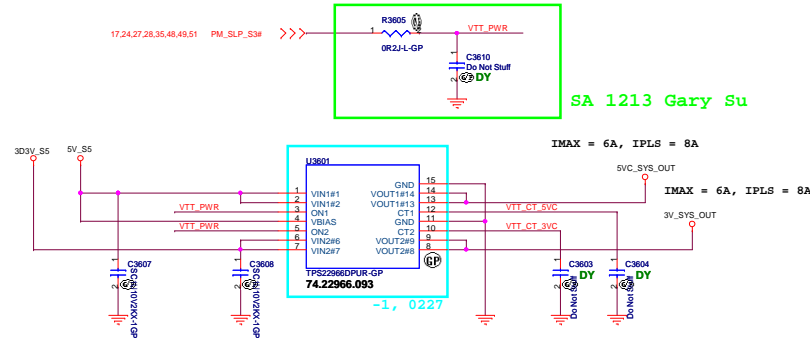
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USB Charger (reserved)	
Title Document Number Storm 2	Rev -1
Date: Tuesday, April 02, 2013	Sheet 35 of 102

Power Sequence

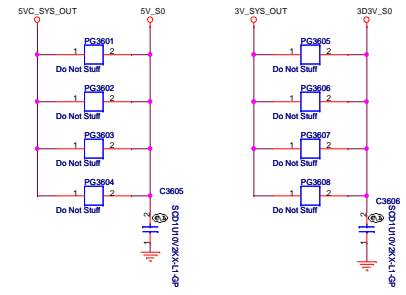


1D5V Power Good

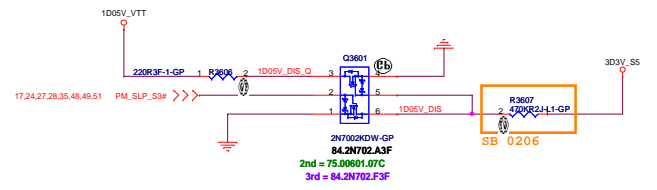
ANNIE Run Power



SA 1213 Gary Su

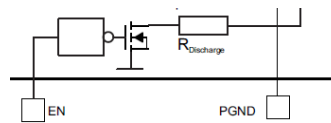


Discharge circuit



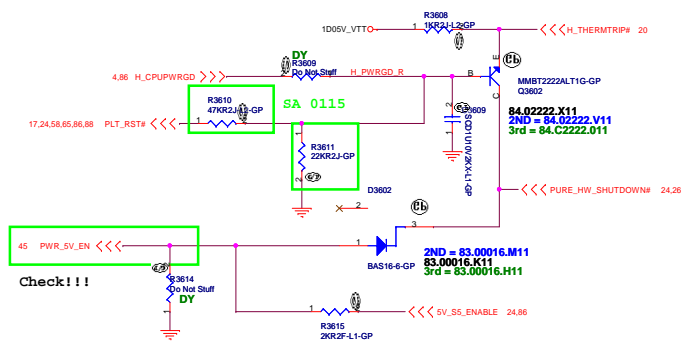
U5101: TLV26065 (1D5V) supports output discharge

$R_{(Discharge)}$	Internal discharge resistor	Activated with EN = GND, $2.9V \leq V_{IN} \leq 5.5V$, $0.8 \leq V_{OUT} \leq 3.6V$
-------------------	-----------------------------	--



U3601: TPS22966 supports output discharge

In the TPS22966, a 220-Ω on-chip load resistor is added for quick output discharge (QOD) when the switch is turned off. The rise time of the device is internally controlled in order to avoid in-rush current and can be adjusted using a ceramic capacitor on the CTx pins.



Check!!!

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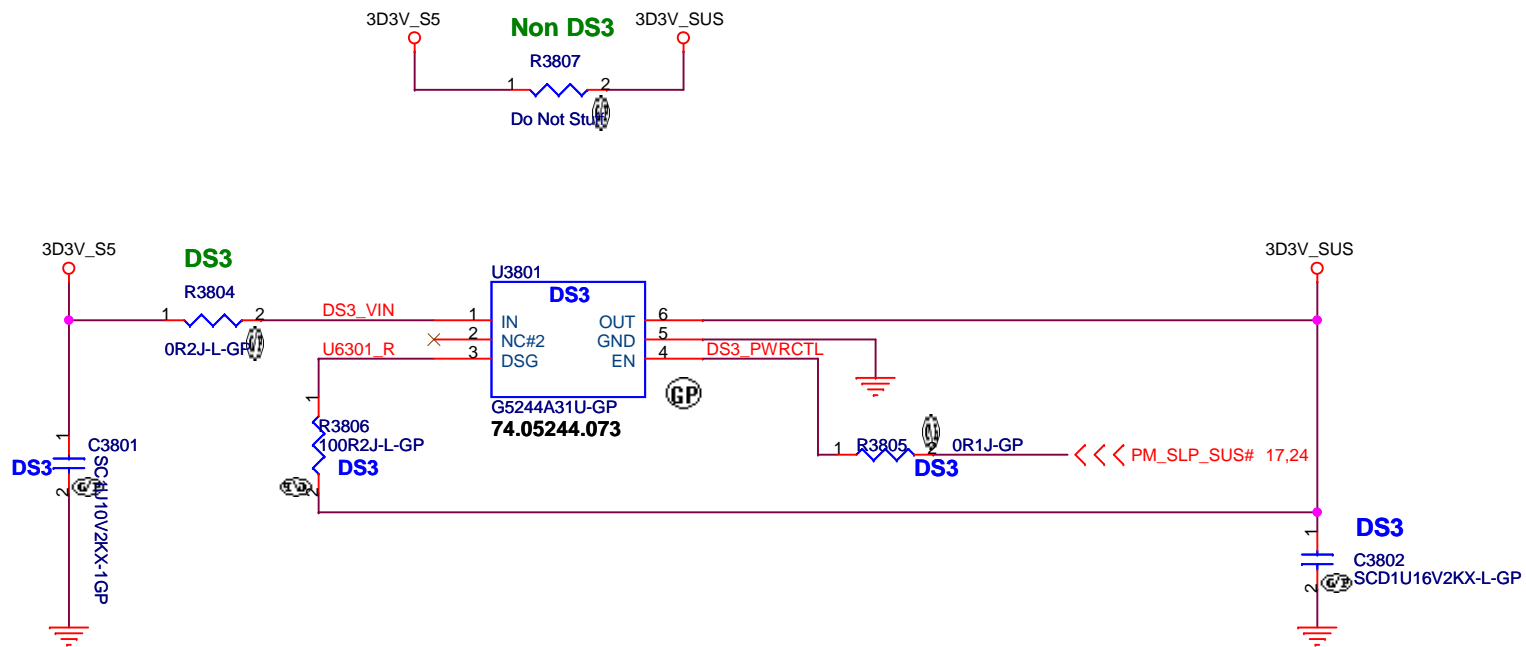
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Title
ADAPTER OCP / S3 reduction

Size A4	Document Number Storm 2	Rev -1
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Title			DS3
Size	Document Number	Rev	
A4	Storm 2	-1	
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Title

1D05M (Reserved)

Size

Document Number

Rev

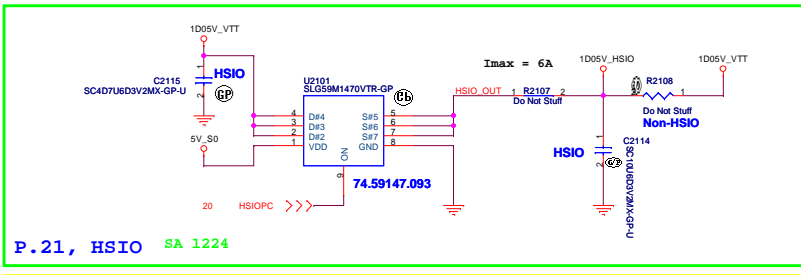
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Storm 2

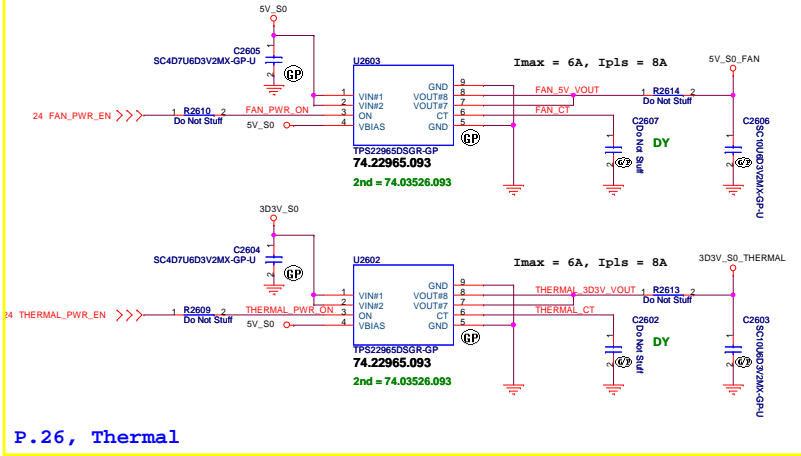
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Date: Friday, December 28, 2012

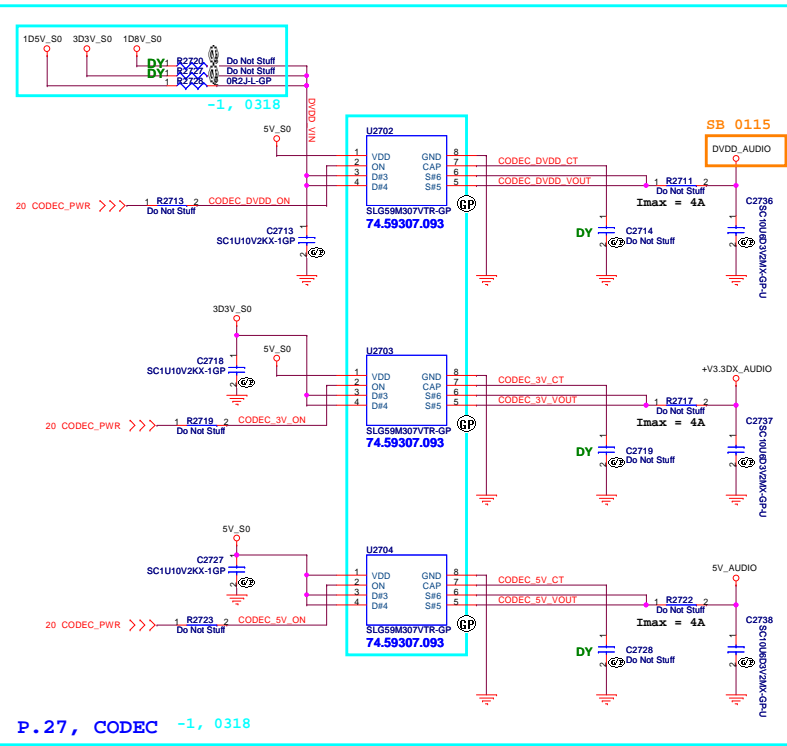
Sheet 39 of 102



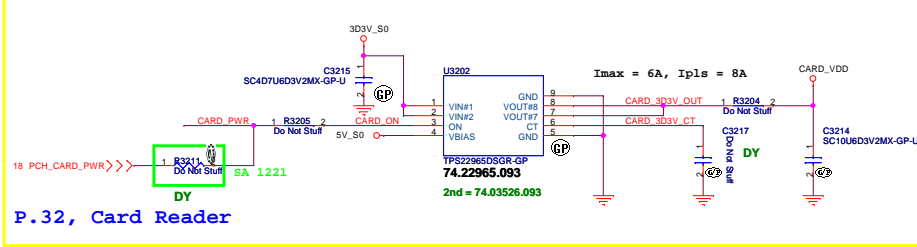
P.21, HSI0 SA 1224



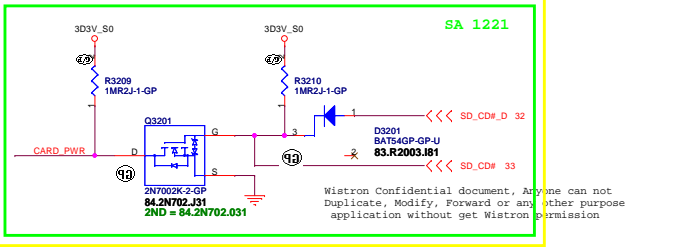
P.26, Thermal



P.27, CODEC -1, 0318



P.32, Card Reader



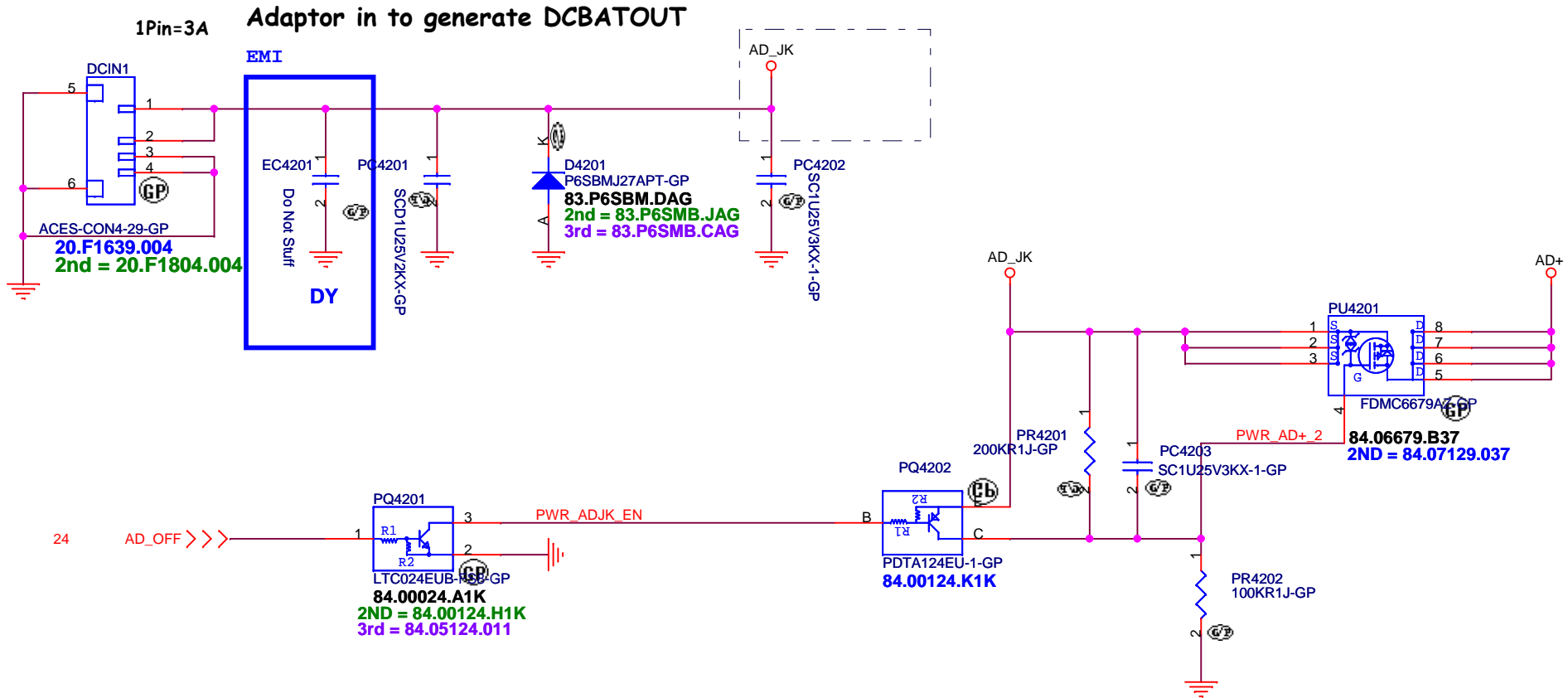
SA 1221

Storm2

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File		
Size		
Document Number	Storm 2	Rev
Date	Monday, April 08, 2013	Sheet 40 of 102

ANNIE solution

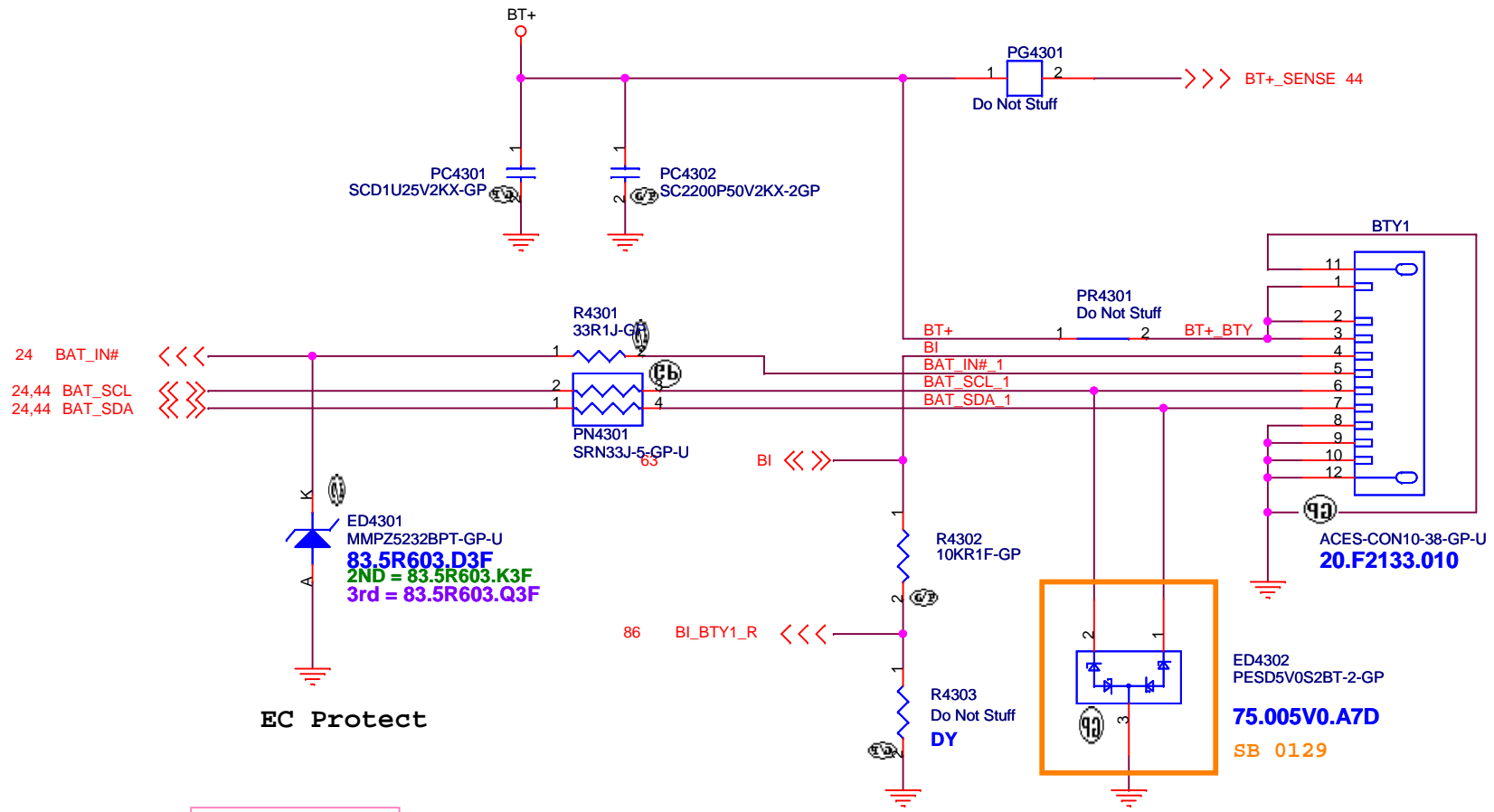


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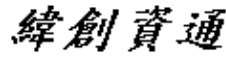
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Title			
DCIN JACK			
Size A4	Document Number Storm 2		Rev -1
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BATTERY CONNECTOR



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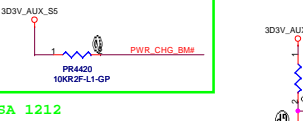
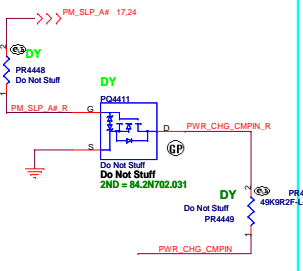

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Title		
BATT CONN		
Size A4	Document Number Storm 2	Rev -1
Date: Tuesday, April 02, 2013		
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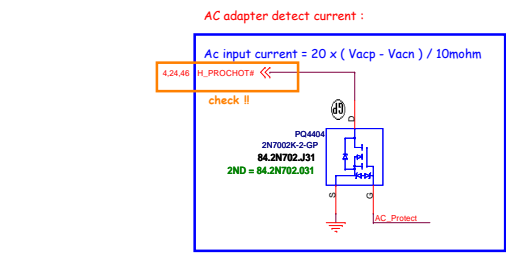
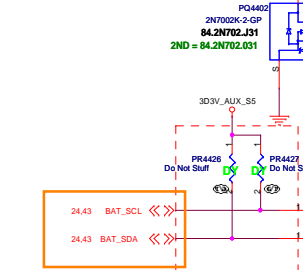
SSID = Charger

AD+ total power	R1	R2
45w	56K	100K
65w	1.06K	100K

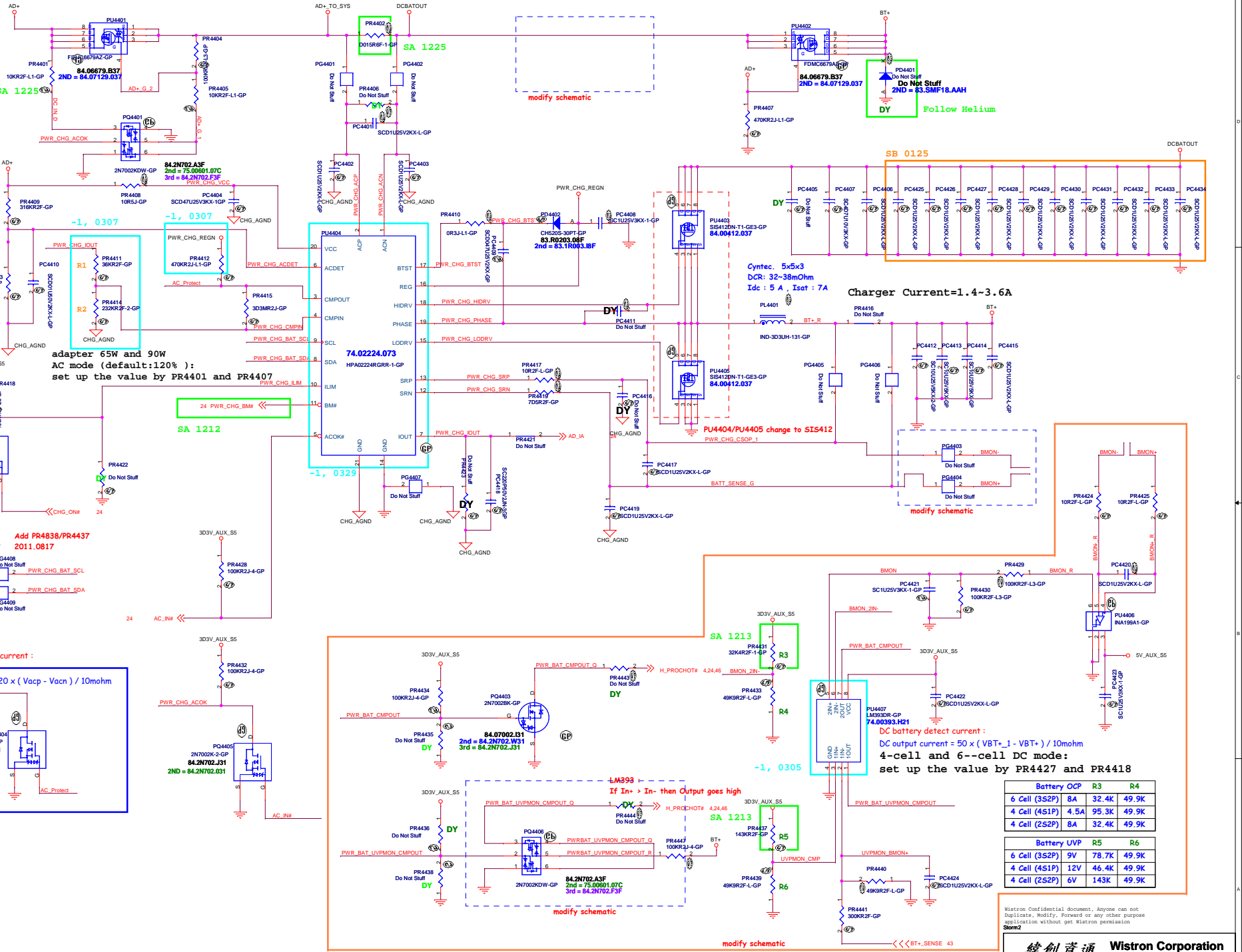
-1, 0307



SA 1212



SA 1213



adapter 65W and 90W
AC mode (default:120%):
set up the value by PR4401 and PR4407

Cyntec. 5x5x3
DCR: 32~38mOhm
I_{dc} : 5 A , I_{sat} : 7 A

Charger Current=1.4~3.6A

DC battery detect current:
DC output current = $50 \times (V_{BT+1} - V_{BT-}) / 10\text{mohm}$
4-cell and 6--cell DC mode:
set up the value by PR4427 and PR4418

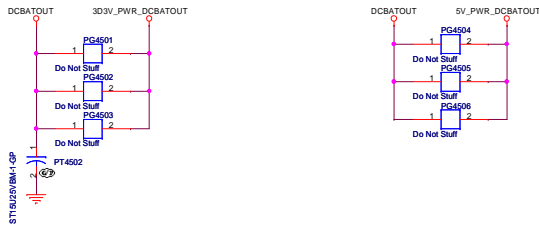
Battery OCP	R3	R4
6 Cell (3S2P)	8A	32.4K
4 Cell (4S1P)	4.5A	95.3K
4 Cell (2S2P)	8A	32.4K

Battery UVP	R5	R6
6 Cell (3S2P)	9V	78.7K
4 Cell (4S1P)	12V	46.4K
4 Cell (2S2P)	6V	143K

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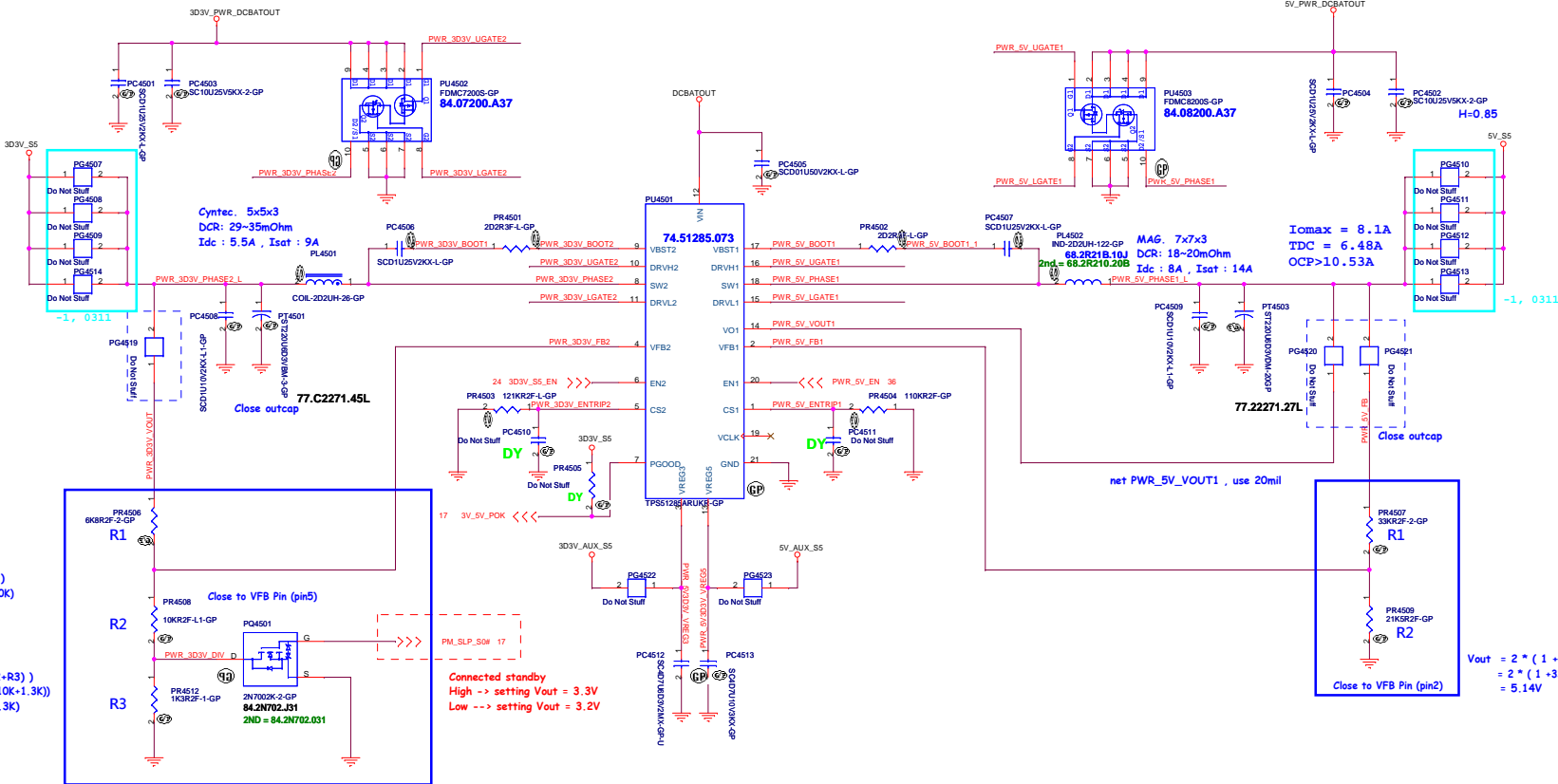
SSID = PWR.Plane.Regulator_3p3v5v



I_{omax} = 5.686A
 TDC = 4.548A
 OCP > 7.39A

Cyntec 5x5x3
 DCR: 29~35mOhm
 I_{dc}: 5.5A, I_{sat}: 9A

I_{omax} = 8.1A
 TDC = 6.48A
 OCP > 10.53A



PQ4501 Pin G , High
 $V_{out} = 2 * (1 + R1/R2)$
 $= 2 * (1 + 6.8K / 10K)$
 $= 3.36V$

PQ4501 Pin G , Low
 $V_{out} = 2 * (1 + R1/(R2+R3))$
 $= 2 * (1 + 6.8K / (10K+1.3K))$
 $= 2 * (1 + 6.8K/11.3K)$
 $= 3.203V$

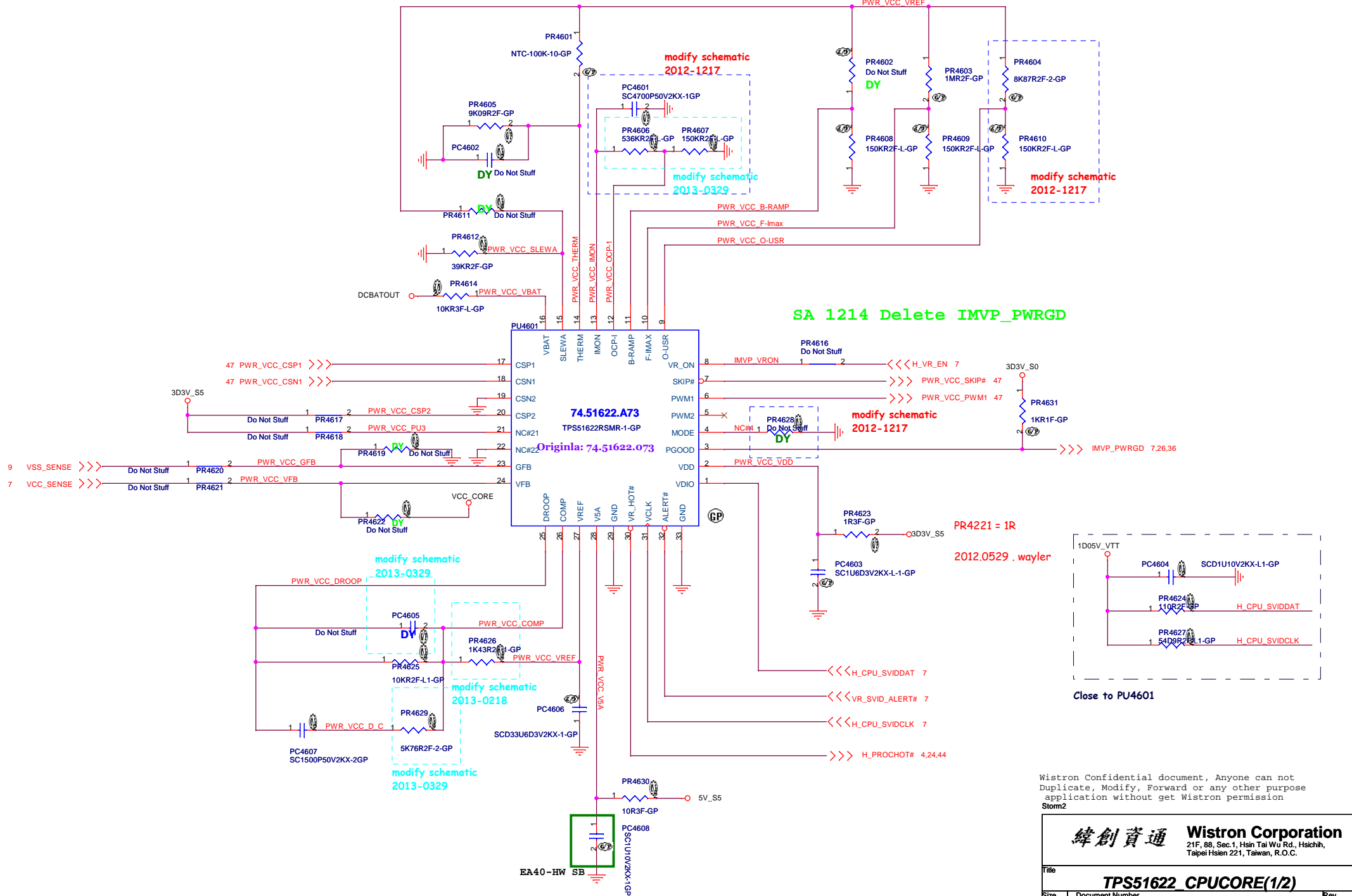
Connected standby
 High -> setting V_{out} = 3.3V
 Low -> setting V_{out} = 3.2V

$V_{out} = 2 * (1 + R1/R2)$
 $= 2 * (1 + 33K / 21K)$
 $= 5.14V$

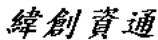
Wistron Confidential document. Anyone can not Duplicate, Modify, Forward or any other purpose without get Wistron permission

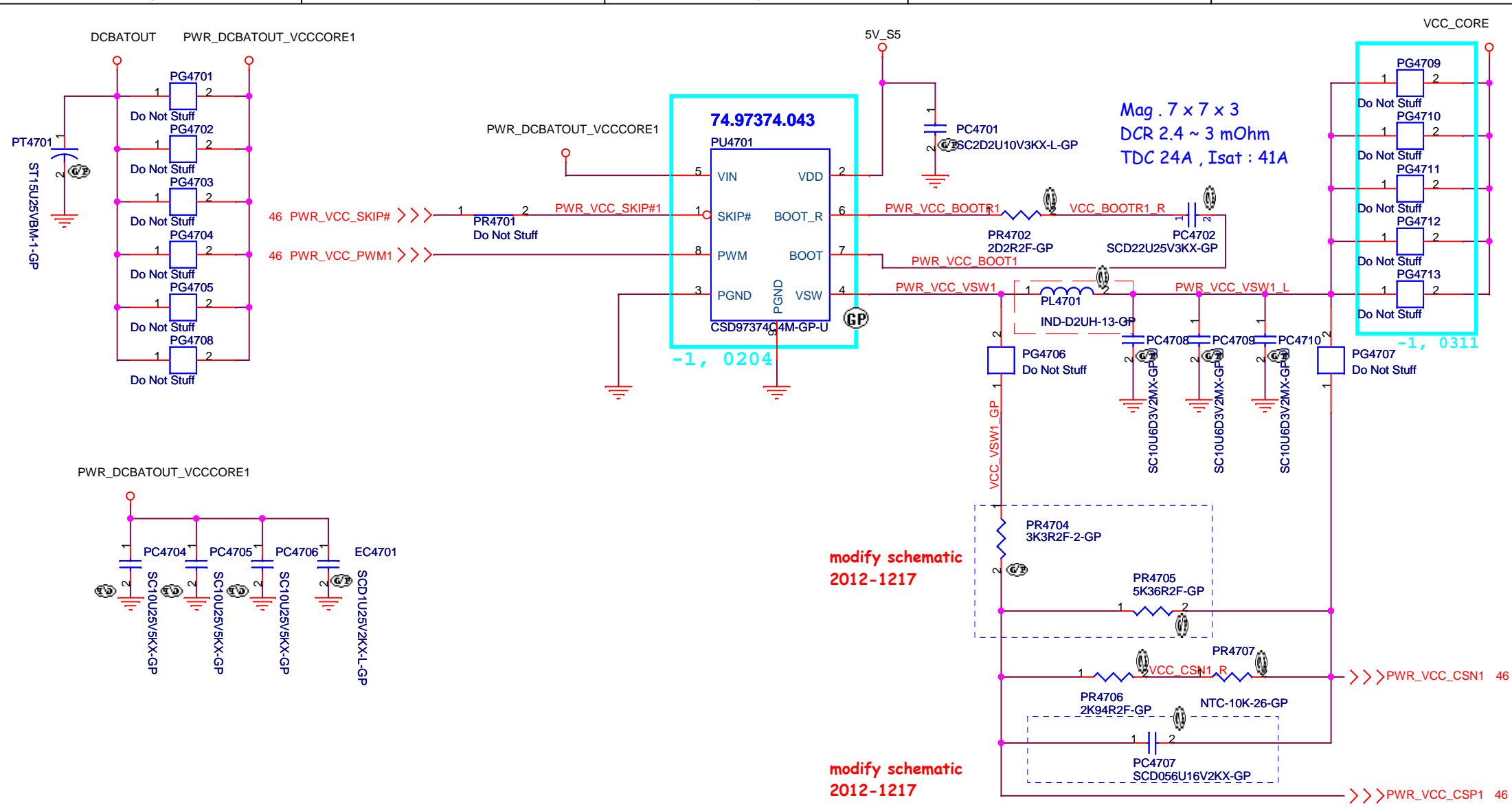
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.
File	TPS51285 5V/3D3V	
Size	Document Number	Rev
Custom	Storm 2	-1
Date	Tuesday, April 02, 2013	Sheet 45 of 100

SSID = CPU.Regulator



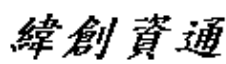
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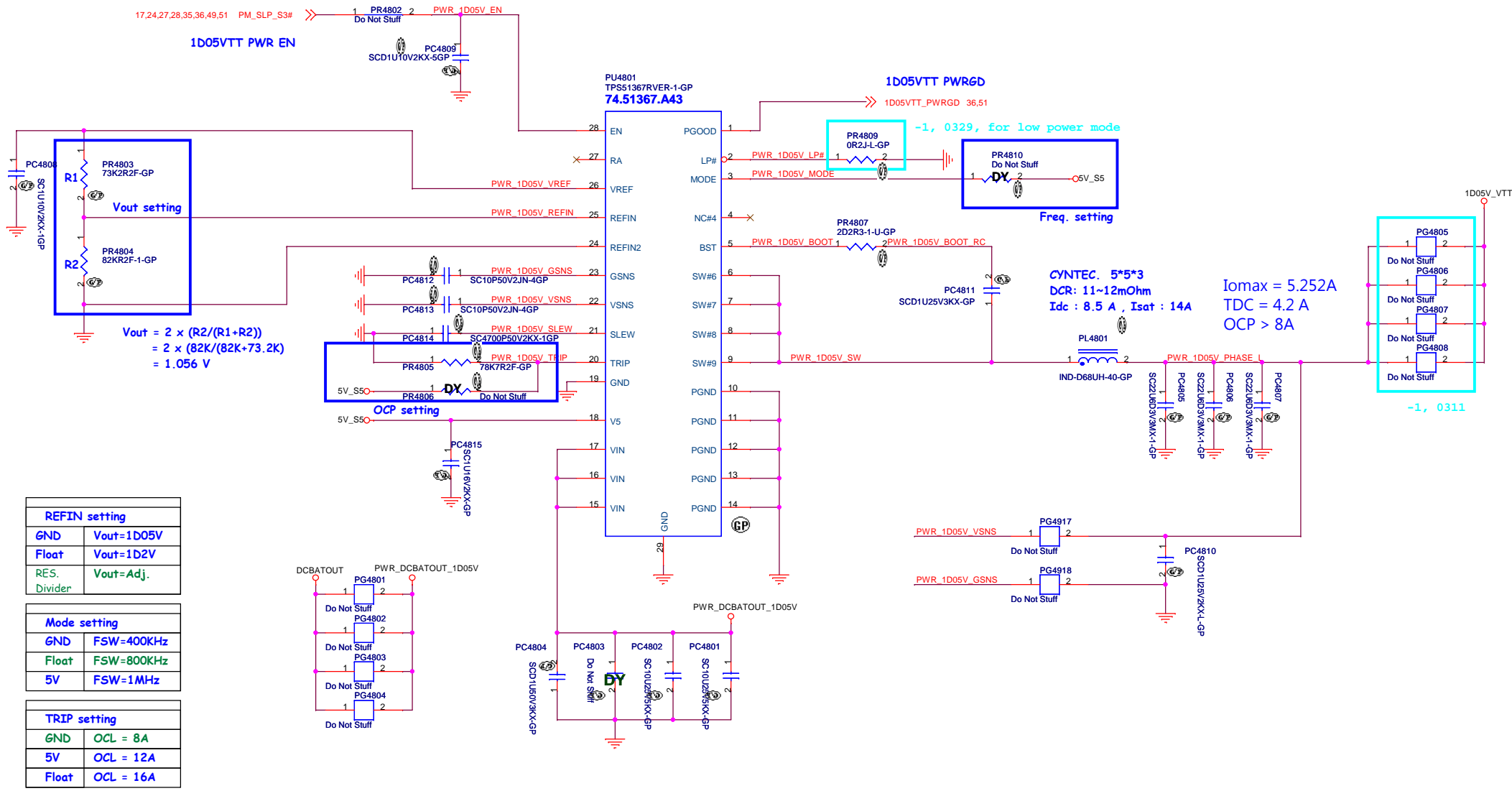
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
TPS51622 CPUCORE(1/2)	
Title	
Size A3	Document Number
Storm 2	
Date: Monday, April 08, 2013	Sheet 46 of 102
Rev	-1



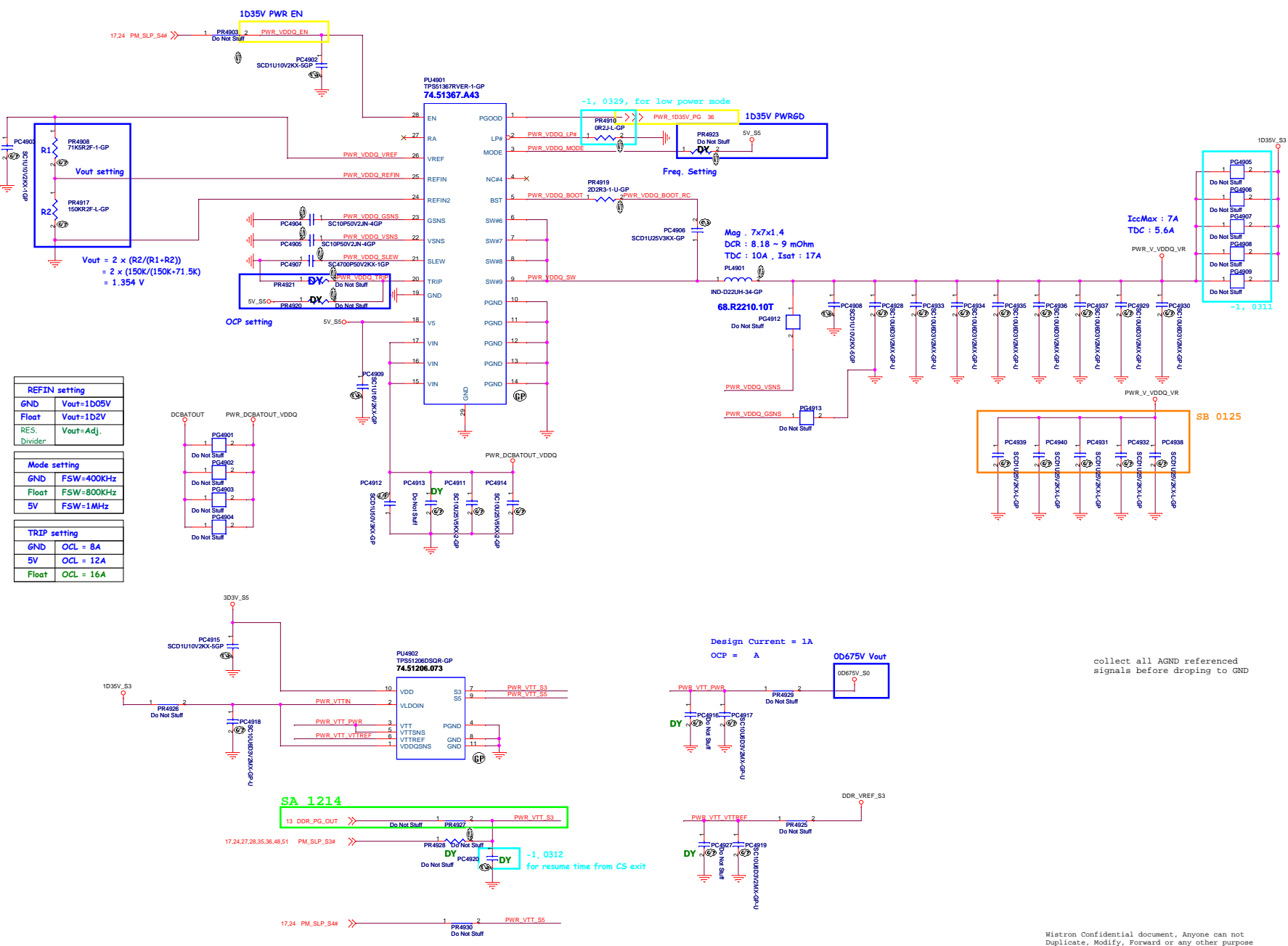
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Title TPS51622 CPU CORE(2/2)		
Size A4	Document Number Storm 2	Rev -1
Date: Tuesday, April 02, 2013	Sheet 47	of 102



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 Storm2



REFIN setting	
GND	Vout=1D05V
Float	Vout=1D2V
RES. Divider	Vout=Adj.

Mode setting	
GND	FSW=400KHz
Float	FSW=800KHz
5V	FSW=1MHz

TRIP setting	
GND	OCL = 8A
5V	OCL = 12A
Float	OCL = 16A

SA 1214	
13 DDR_PG_OUT	Do Not Stuff
17,24,27,28,35,36,48,51 PM_SLP_S3#	Do Not Stuff
17,24 PM_SLP_S4#	Do Not Stuff

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Title

1D8V S0 (Reserved)

Size

A4

Document Number

Storm 2

Rev

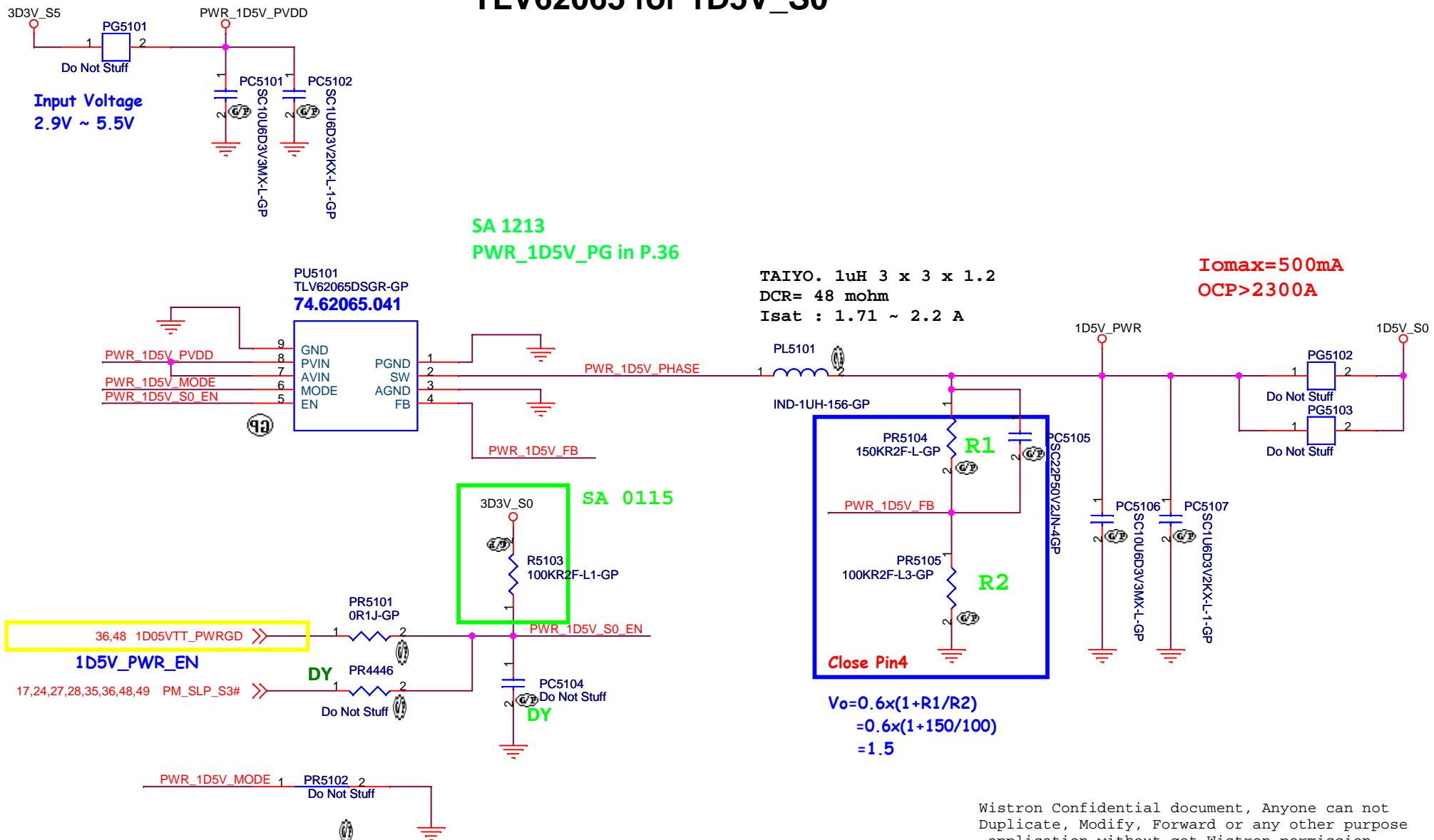
-1

Date: Friday, December 28, 2012

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102

TLV62065 for 1D5V_S0



MODE pin	Function
High	Fixed Freq. PWM mode
Low	Power Save Mode with automatic transition from PFM mode to fixed freq. PWM mode

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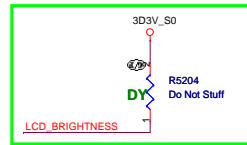
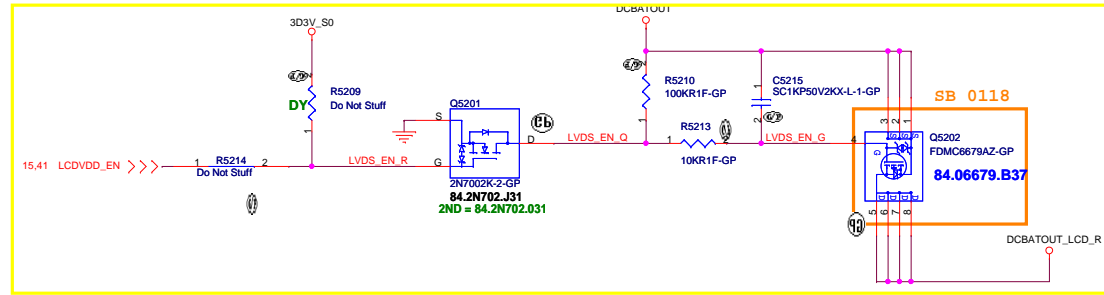
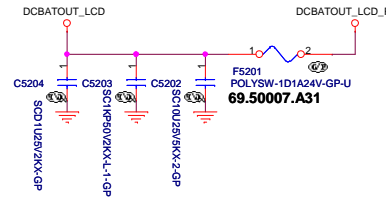
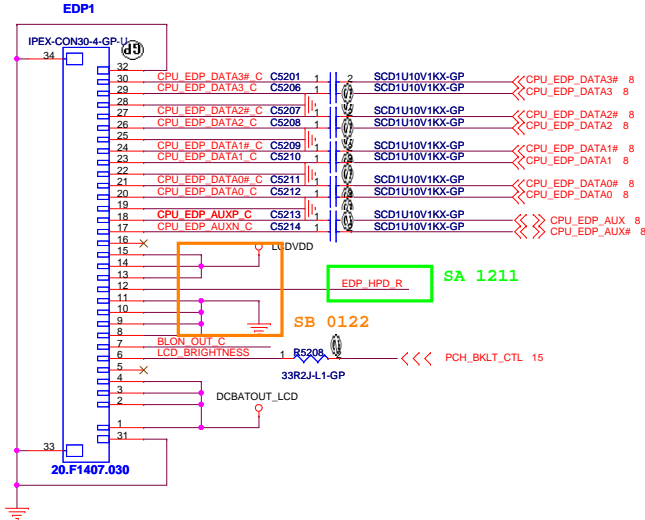
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title 1D5V S0 TLV62065	
Size A4	Document Number Storm 2
Date: Tuesday, April 02, 2013	Rev -1
Sheet 51 of 102	

SSID = VIDEO

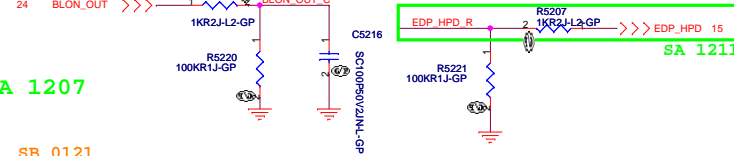
output turn-On Rising Time:1.3ms~2.7ms
current limit:2~3.3A

EDP CONNECTOR

Previous parts(74.05285.07F)rise time:1.5ms ~5ms
current limit:1.5ms~ 3.5ms

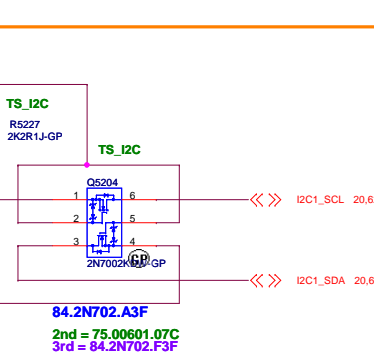
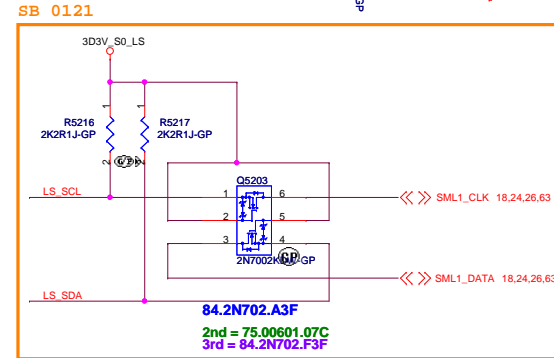
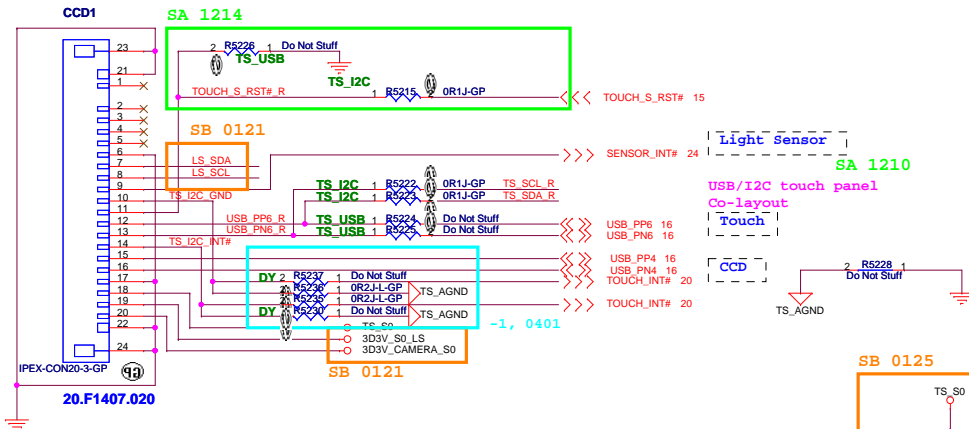


SA 1207



SA 1211

CCD/TS/LS CONNECTOR



Storm / Helium / MA50 /
Petra / MA40 / Husk / MA52

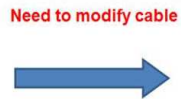
Storm2 / Helium2 / Angel

USB interface pin define

USB / I2C interface pin define

Pin	Assignment
1	VBus
2	USB_dm
3	USB_DP
4	GND
5	GND
6	INT

pin	define	pin	I2C(compatible) Define
1	VUSB_5V	1	+3.3V touch panel
2	USB_DM	2	SCL
3	USB_DP	3	SDA
4	UA_PA4	4	INT
5	GND	5	RESET
6	GND	6	GND



Need to rework component
to switch USB and I2C I/F on PCBa

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Title

Reserved

Size
A4

Document Number

Storm 2

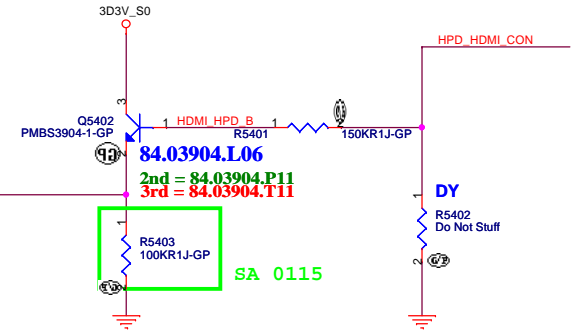
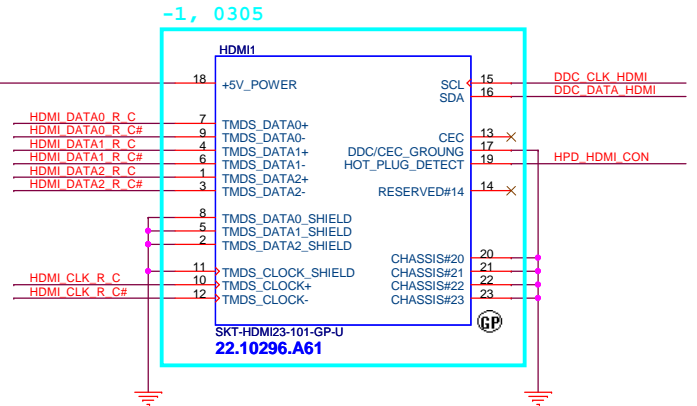
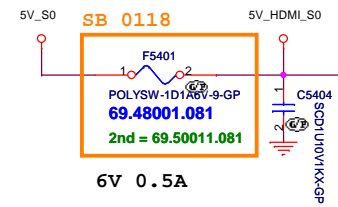
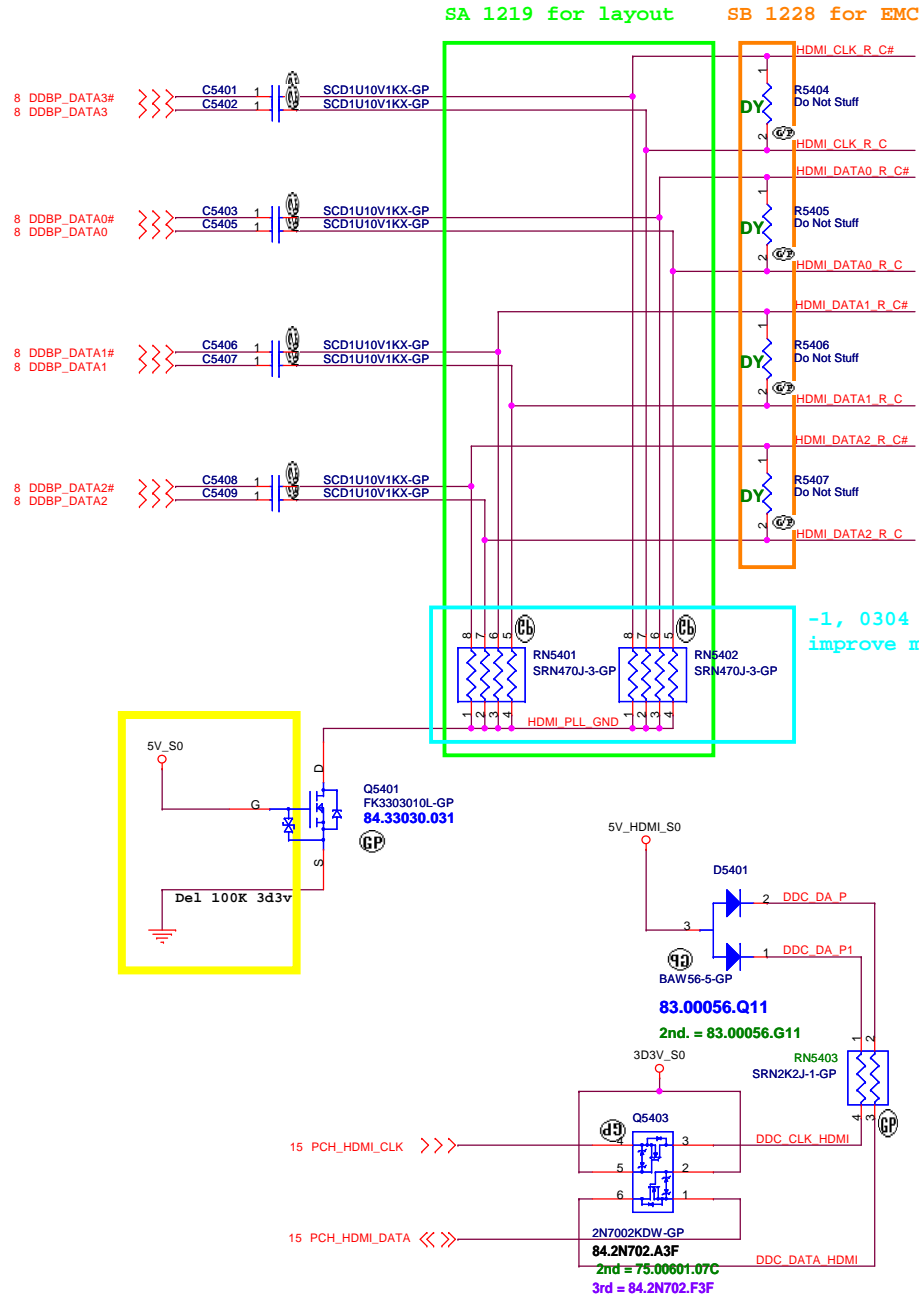
Rev
-1

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SSID = VIDEO

HDMI CONN.



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HDMI Level Shifter/Connector			
Title	Document Number		Rev
Size A3	Storm 2		-1
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Title **NGFF_SSD (Reserved)**

Size A4	Document Number Storm 2	Rev -1
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Title **Reserved**

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5 4 3 2 1

SSID = Wireless

NGFF Conn(WWAN) Reserved

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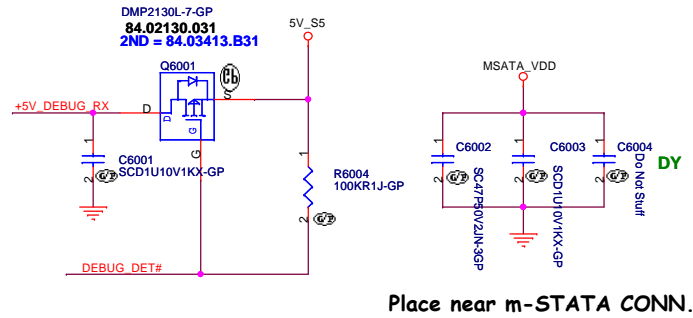
Title **reserved**

Size A4	Document Number Storm 2	Rev -1
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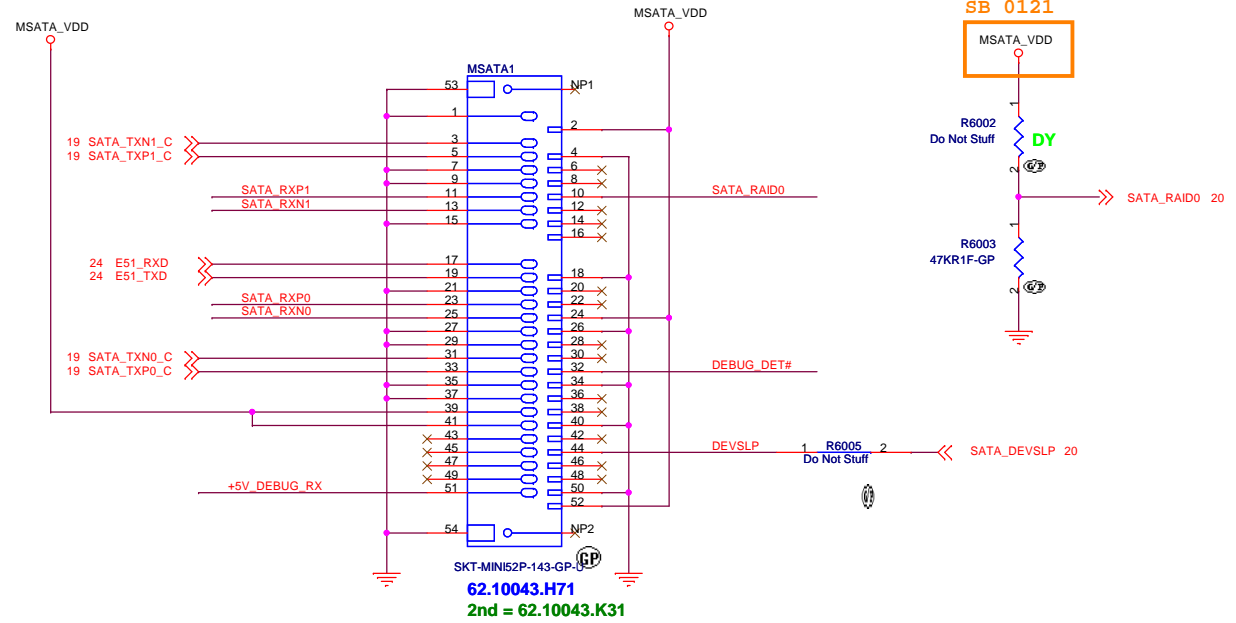
Date: Friday, December 28, 2012 Sheet 59 of 102

SSID = mSATA

Mini Card Connector(mSATA)

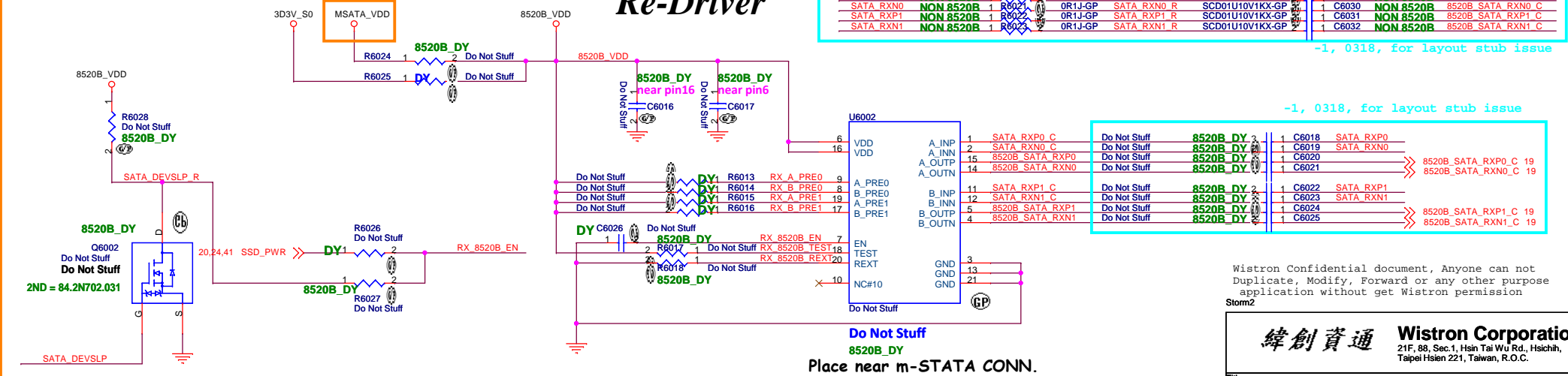


Place near m-STATA CONN.



SB 0130

Re-Driver



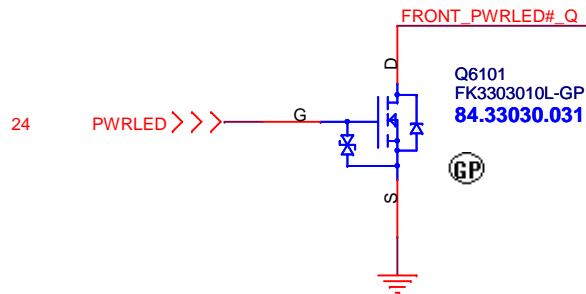
Place near m-STATA CONN.

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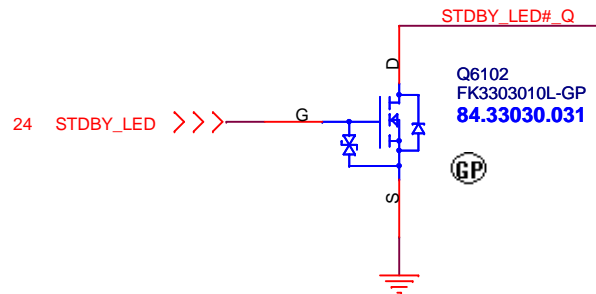
緯創資通 Wistron Corporation
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SSID = User.Interface

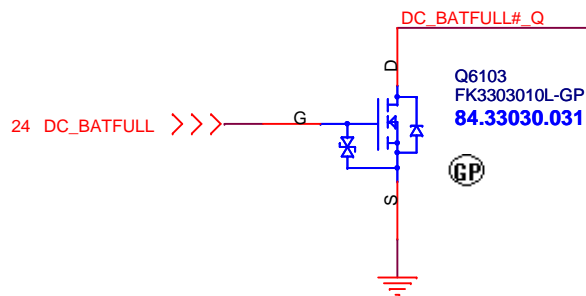
Power button LED



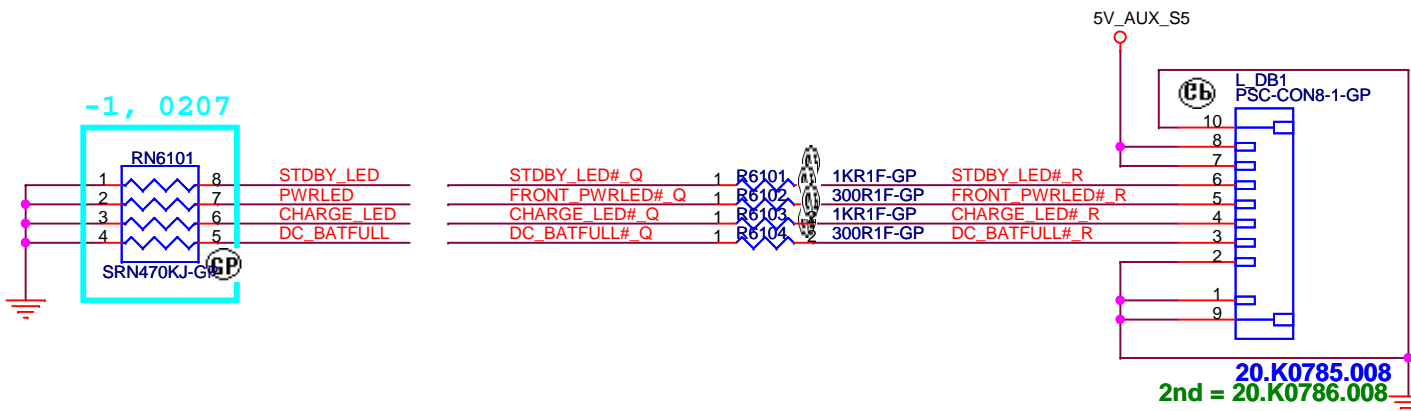
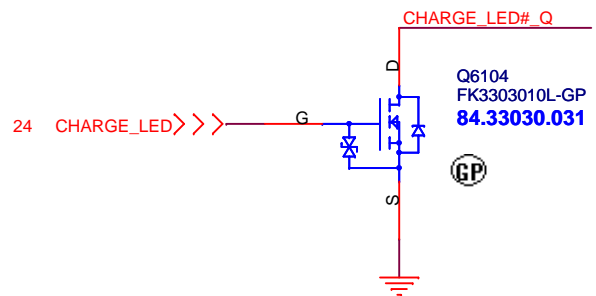
Power STDBY_LED



Battery LED2(DC_BATFULL)



Battery LED1(CHARGE)



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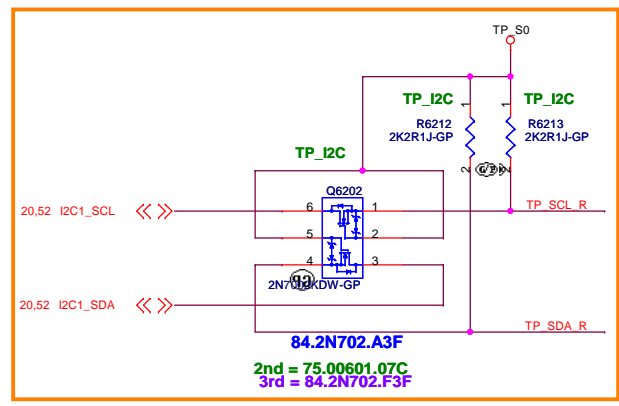
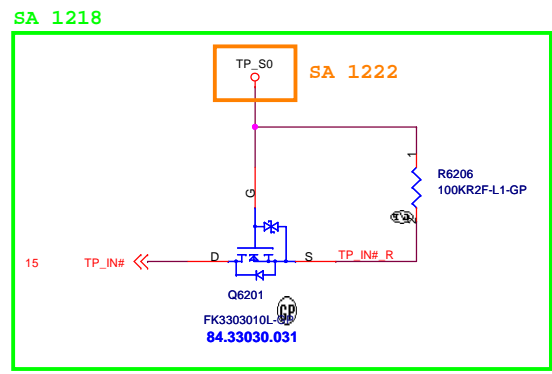
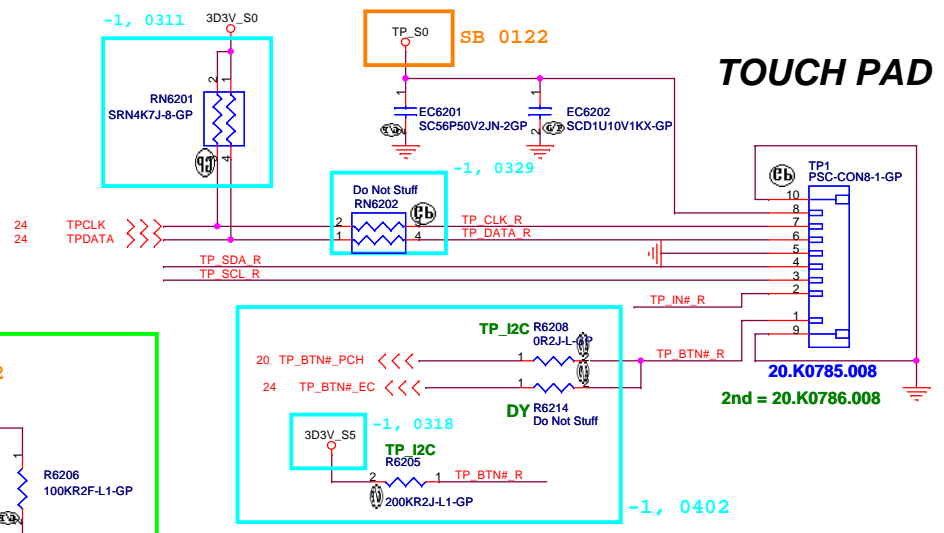
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Title			LED Board/Power Button		
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Pin Assignment and Description			
Pin#	Signal	I/O	Description
1	VCC	VCC	VCC, 3.3V +/-5%. Power ripple: 100 mVpp max. Power sequence: See section 4.6.
2	NC		Not connected
3	NC		Not connected
4	GND	GND	Ground
5	I ² C_SDA	I/O	I ² C data. I _{Drive} or I _{Sink} : 8 mA max.
6	I ² C_SCL	I/O	I ² C clock I _{Drive} or I _{Sink} : 8 mA max.
7	/INT	O	Reserved for SMBUS application. Indicates touchpad likes to send data to system (host). Low active.
8	/Button		Low active, pulled to VCC through a 200K Ω resistor inside touchpad when touchpad is powered. Suggest pulled to VCC through a suitable resistor in system side when touchpad is powered off. Low when button is pressed.

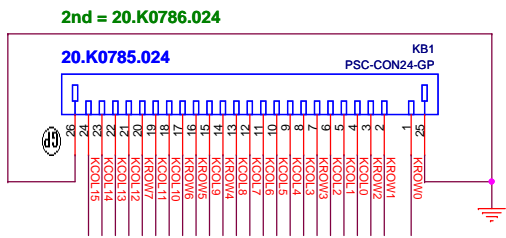
Pin number	Pin Define
1	VDD(3.3V)
2	PCClk
3	PCDt
4	DGND
5	NC*(SDA)
6	NC*(SCL)
7	NC*(/INT)
8	NC

Note: Reserve for SMBus

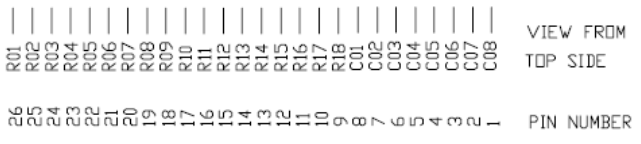
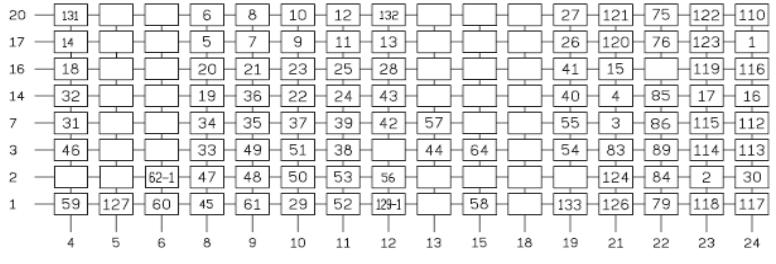


I2C Addr. = 0X20H (Synaptics)

Internal Keyboard Connector



0.5 pitch

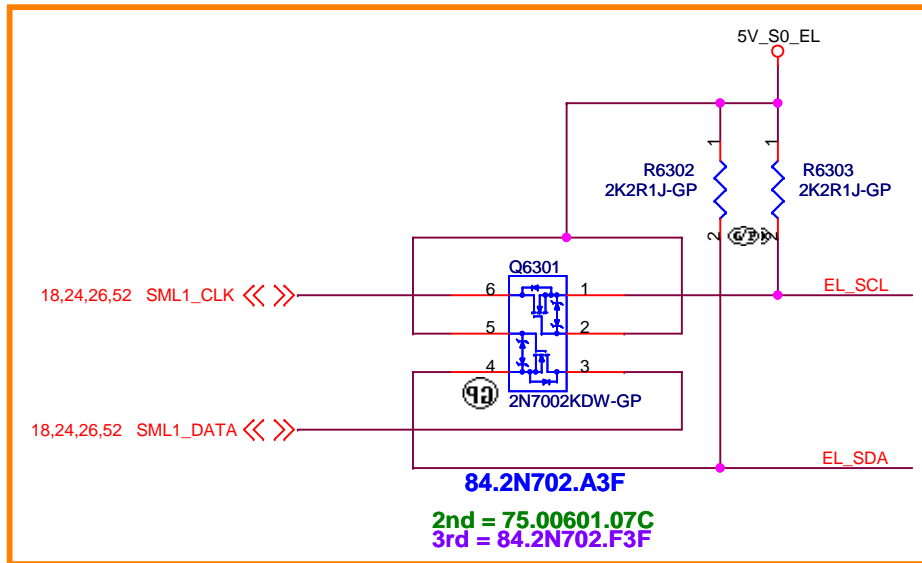


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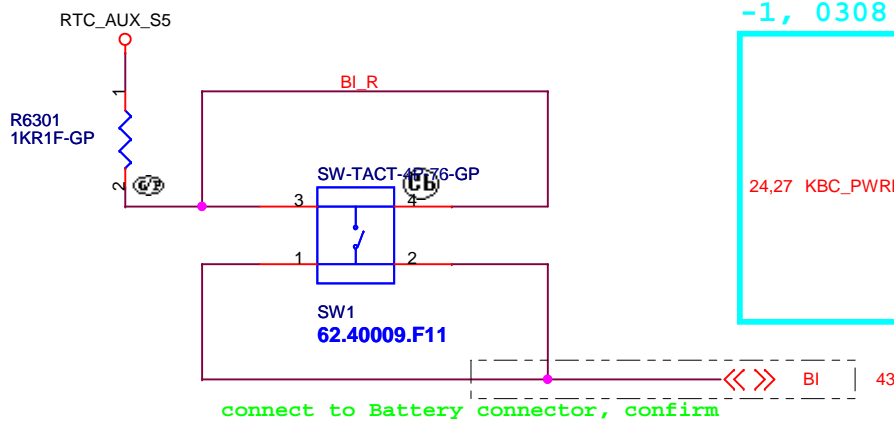
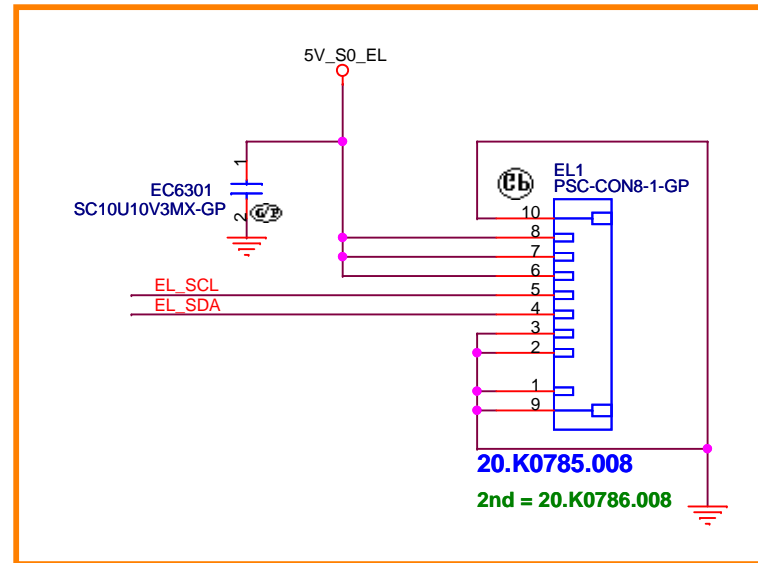
緯創資通		Wistron Corporation	
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Key Board/Touch Pad			
Size A3	Document Number	Rev	
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EL Backlight

SB 0121



SB 1228



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Title

IO Board Connector

Size A4 Document Number Rev

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Title

Hall Sensor (Reserved)

Size
A4

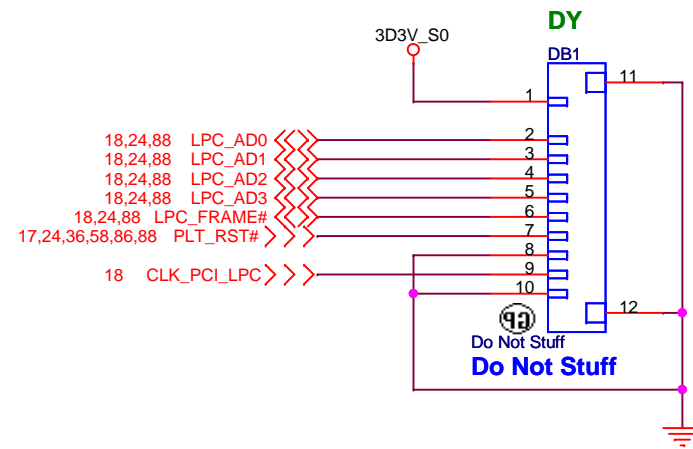
Document Number

Storm 2

Rev
-1

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Title

Dubug connector

Size
A4

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Title **Sensor Hub**

Size A4 Document Number **Storm 2** Rev **-1**

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Title

G Sensor (Reserved)

Size

Document Number

Rev

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Title **Thunderbolt 1/5 (Reserved)**

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Title **Thunderbolt 2/5 (Reserved)**

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Title **Thunderbolt 3/5 (Reserved)**

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Title **Thunderbolt 4/5 (Reserved)**

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Title **Thunderbolt 5/5 (Reserved)**

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5

4

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Title
GPU PEG (Reserved)

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5

4

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B

B

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GPU DIGIOUT (Reserved)

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GPU VRAM I/F (Reserved)

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Title

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VGA Power (Reserved)

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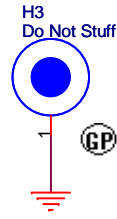
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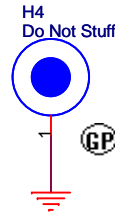
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Do Not Stuff



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SB 0118

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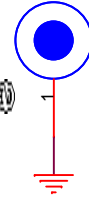
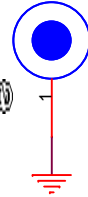
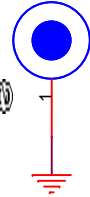
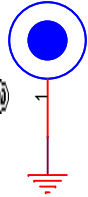
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HS2

HS3

HS4

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SPRING-115-GP



S2

SPRING-115-GP



S3

SPRING-115-GP



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S4

SPRING-115-GP



S5

SPRING-115-GP



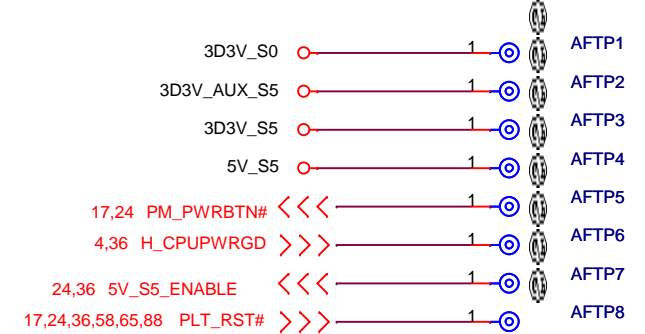
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SB 0123

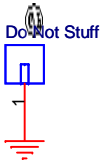
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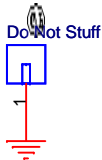
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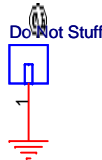
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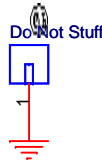
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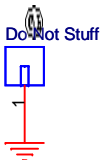
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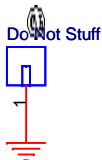
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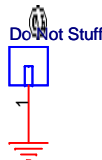
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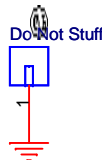
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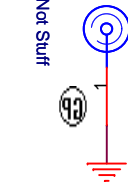
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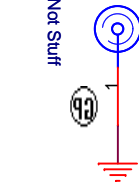
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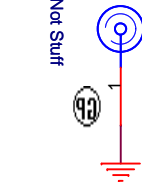
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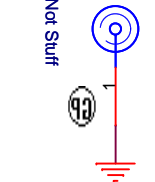
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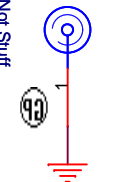
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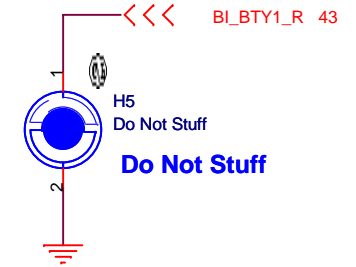
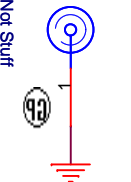
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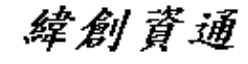
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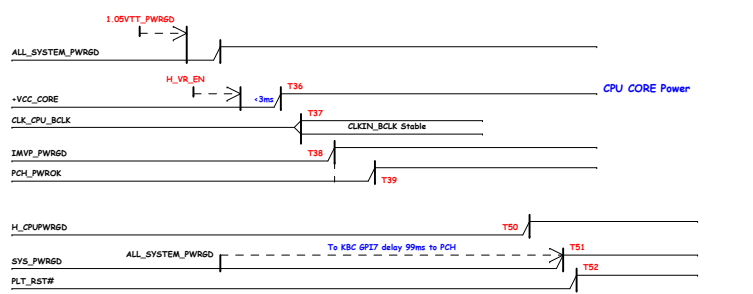
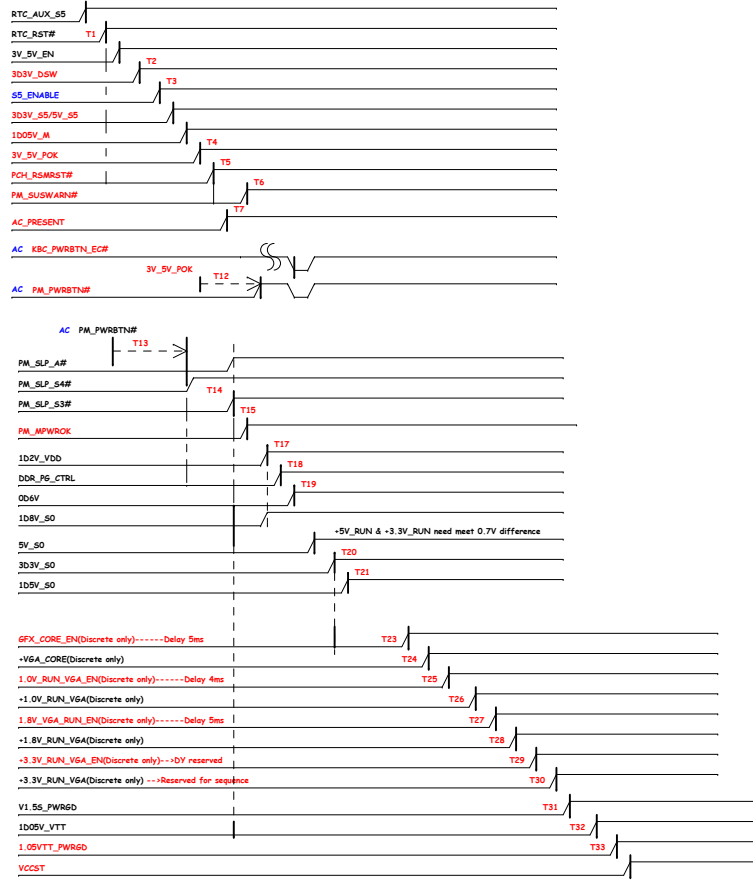
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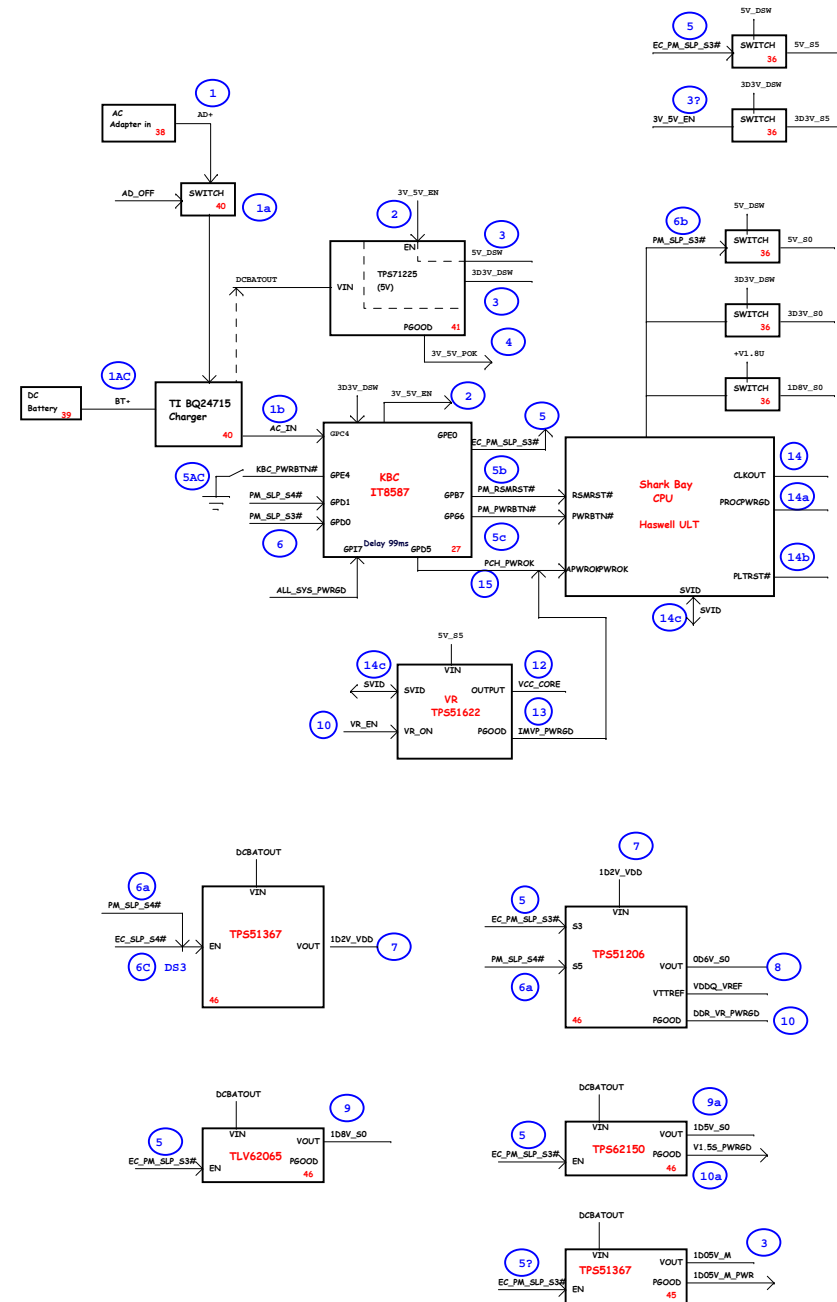
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Intel-Power Up Sequence

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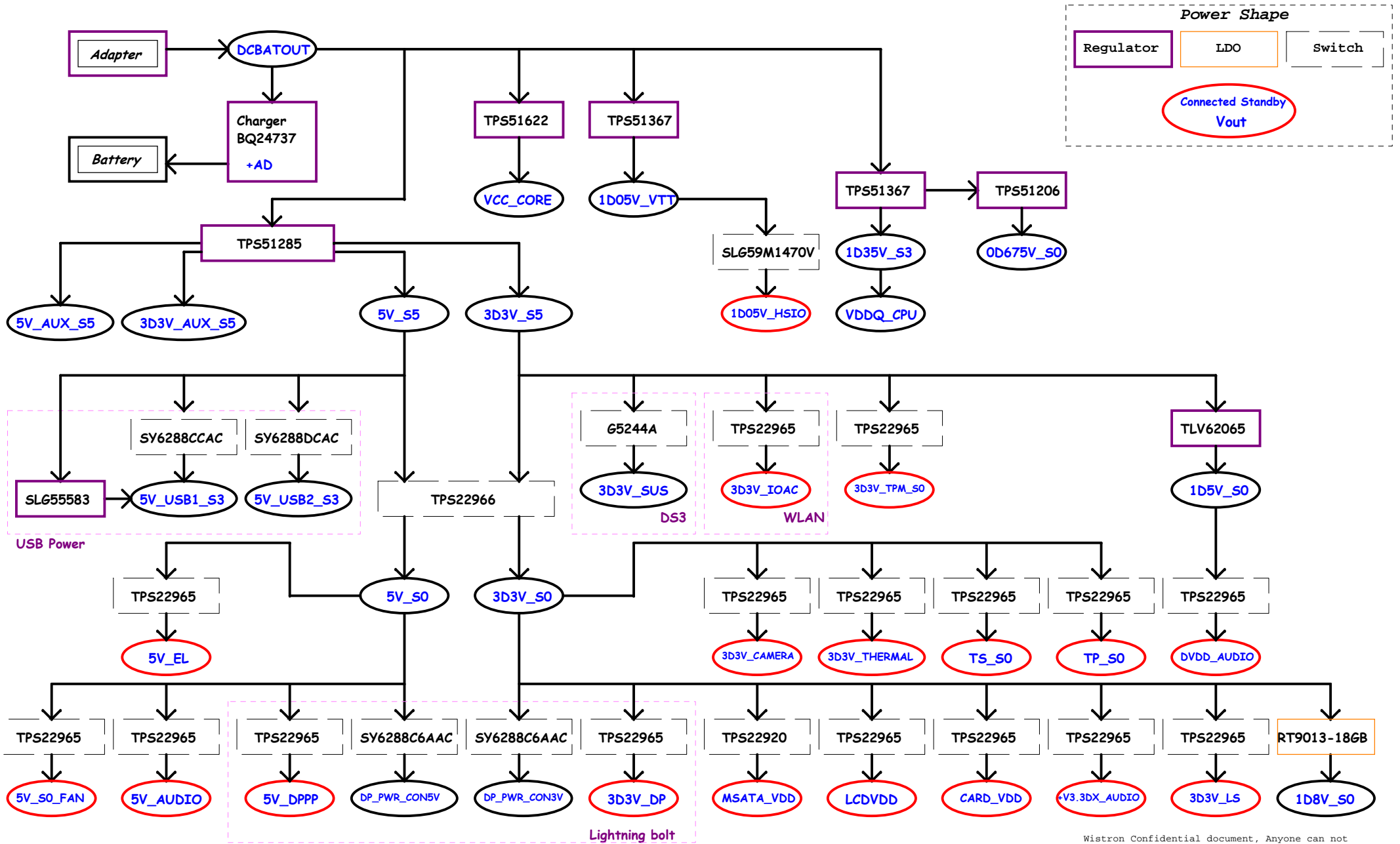


SHARK BAY POWER UP SEQUENCE DIAGRAM



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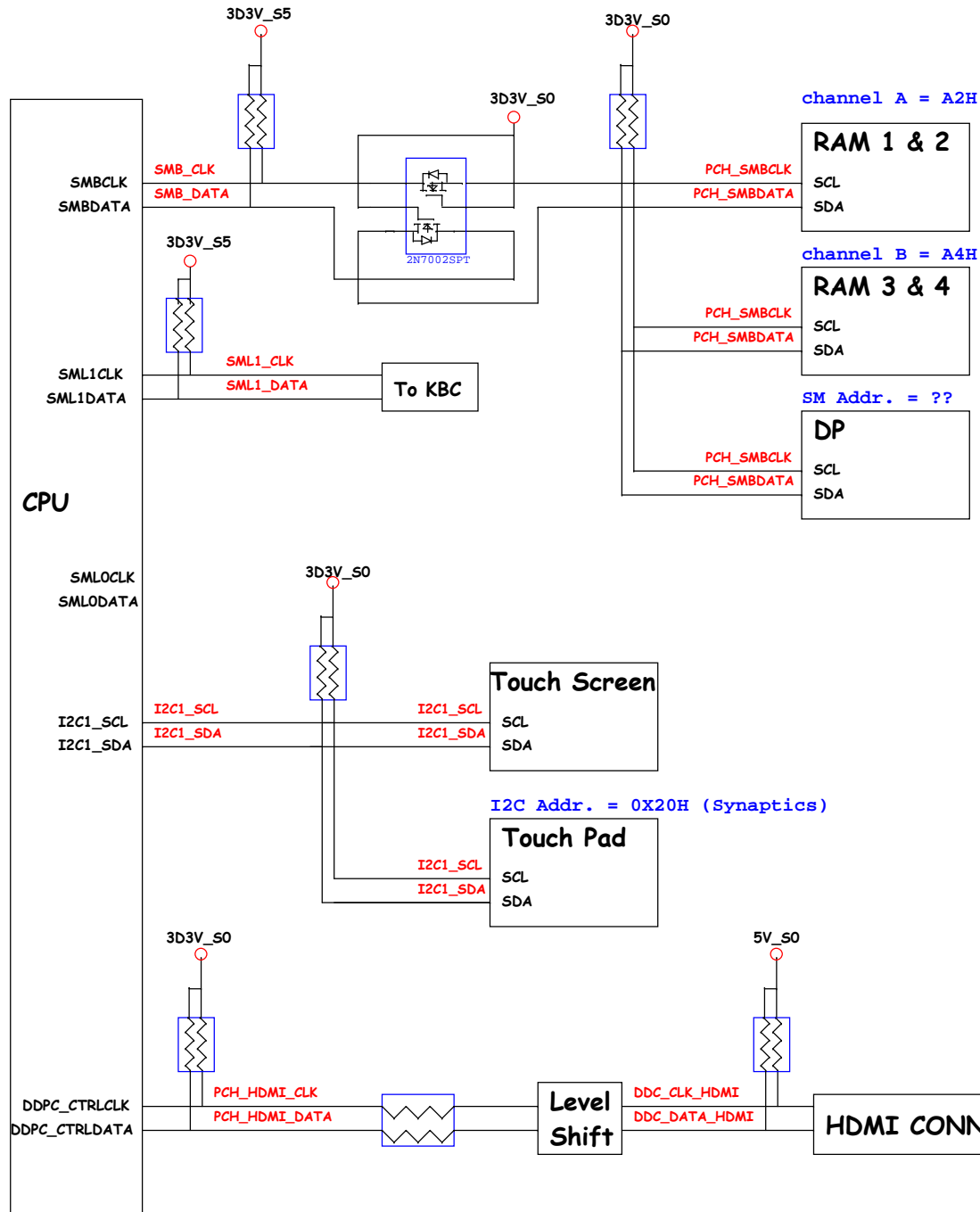
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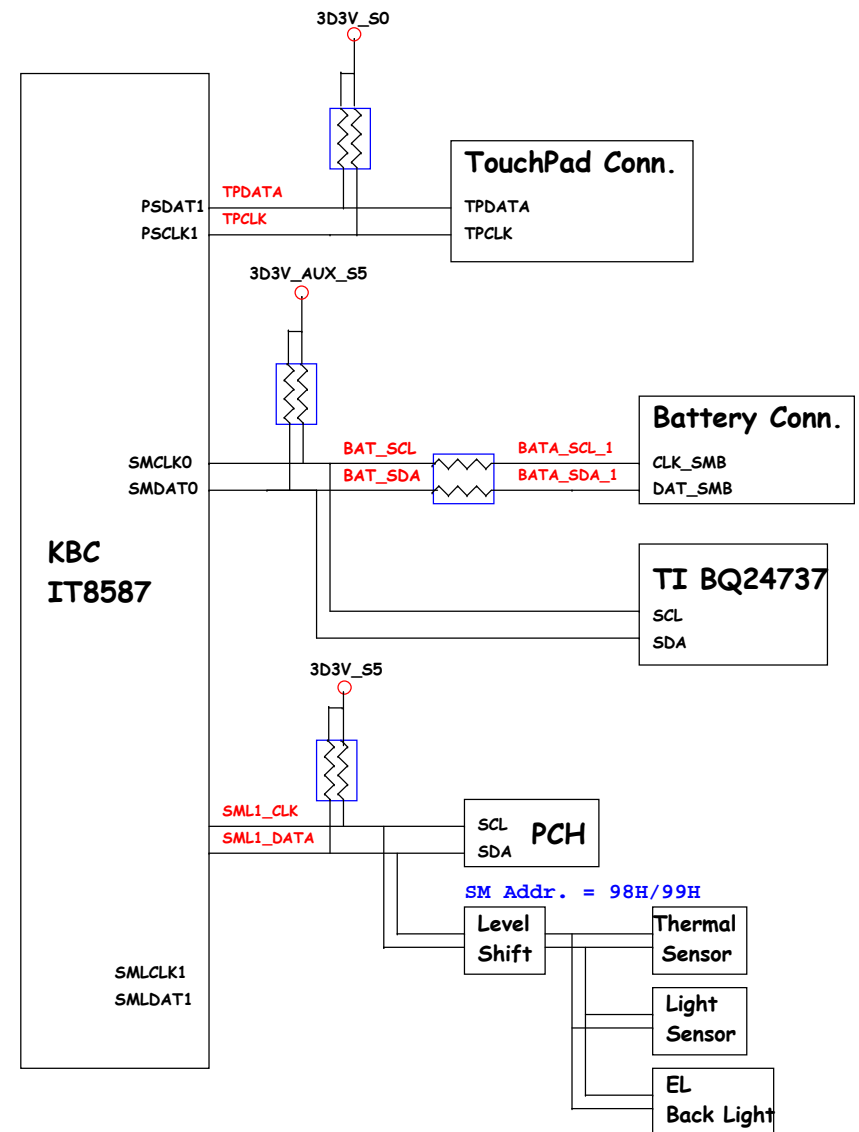
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CPU SMBus Block Diagram

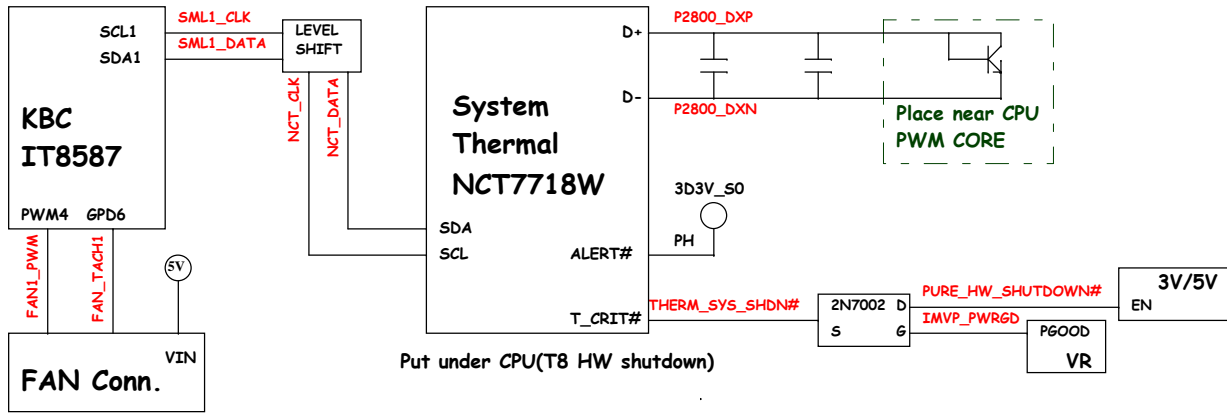


KBC SMBus Block Diagram

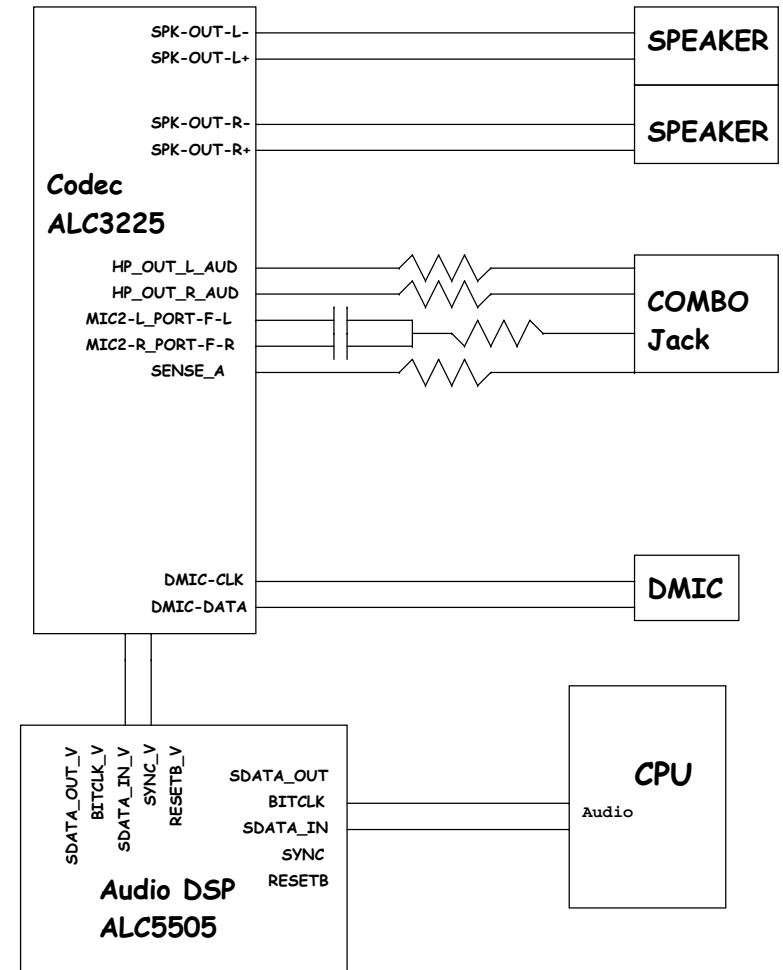


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Thermal Block Diagram



Audio Block Diagram



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