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HSF Property: ROHS or Halogen-Free(5L3?)

LUXOR10FG

2011.08.02

DATE	CHANGE NO.	REV
21-OCT-2009		

DESIGNER	EE	DATE	POWER	DATE	INVENTEC														
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SIZE	CODE	DOC NUMBER	REV																
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MODEL	PROJECT	FUNCTION																	
Everest	Main Board																		
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TITLE			
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NVIDIA
W/ OPTIMUS

N13P-GL
29X 29 MM

IVY BRIDGE
DC 35W
SOCKET-RPGA989
37.5 X 37.5 X 5 mm

DDR3@1.5/0.75V
(1333/1600 MHZ)
204-PIN SODIMM0

DDR3@1.5/0.75V
(1333/1600 MHZ)
204-PIN SODIMM1

HDMI

CRT

LCM

PCH
PANTHER POINT
25 X 25 X 2.3 mm

AUDIO CODEC
REA_ALC269Q_VB6

INTERNAL MIC IN

EXT MIC IN

HEADPHONE

USB_0: USB CONN
USB_2: USB CONN
USB_5: MINICARD WLAN
USB_8: CARD READER
USB_10: WEBCAM

SLEEP & CHARGE

USB_1: USB3.0 CONN

USB_8: CARD READER
REA_RTS5129

SATA0: ESATA
SATA1: HDD
SATA6: ODD

RJ45

PCIE_1: LAN
ATHEROS_AR8161/8162

PCIE_2: WLAN

PCIE_3: USB3.0

EC WINDBOND
NPCE885LA0DX

SPI FLASH 8MB
MXIC_MX25L3206EM21

KEYBOARD

TOUCH PAD

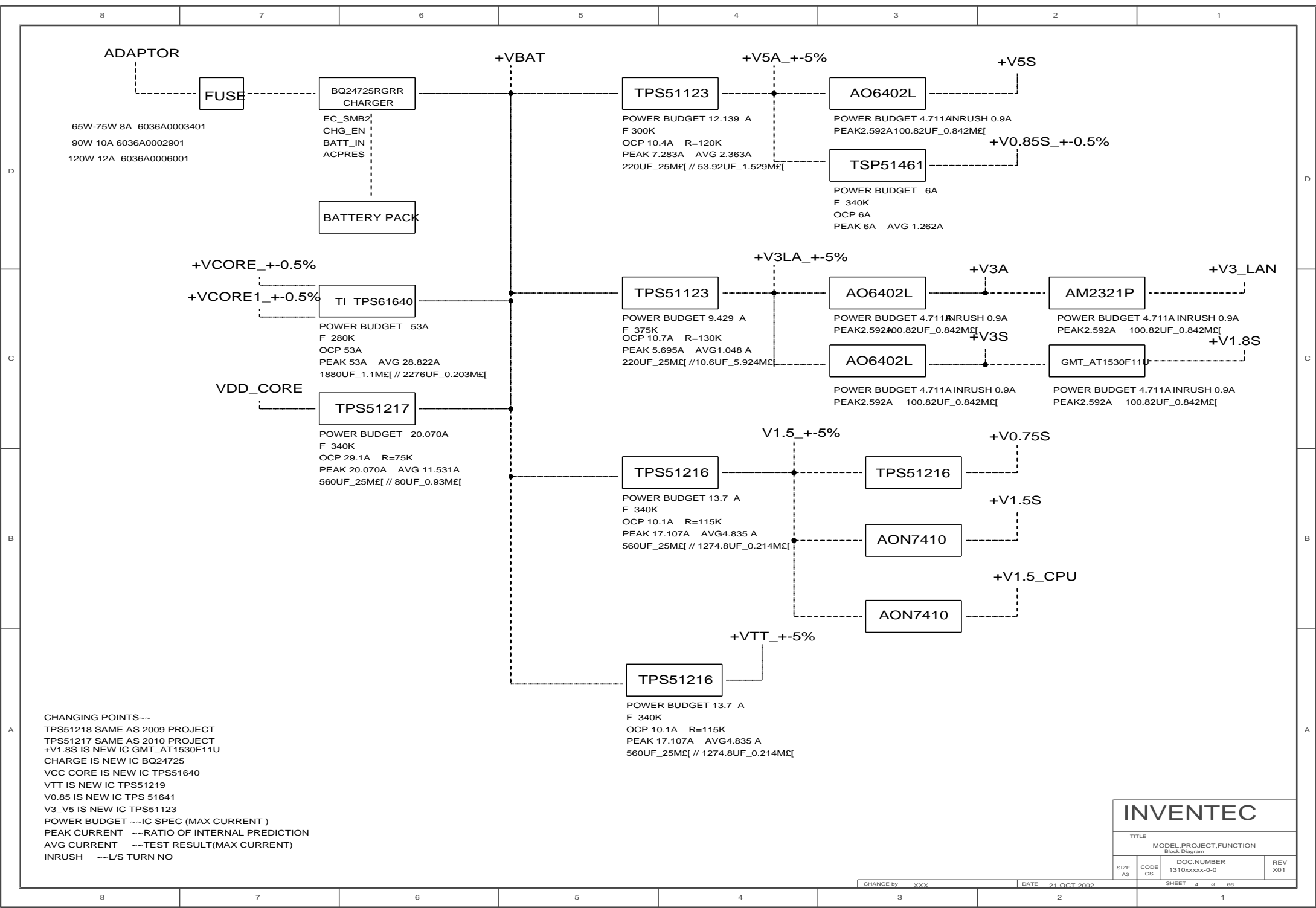
ENE-P2809A
THERMAL SENSOR

BATTERY CHARGER &
DC/DC & IMVP 7

LI-ION BATTERY
6-Cell

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TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
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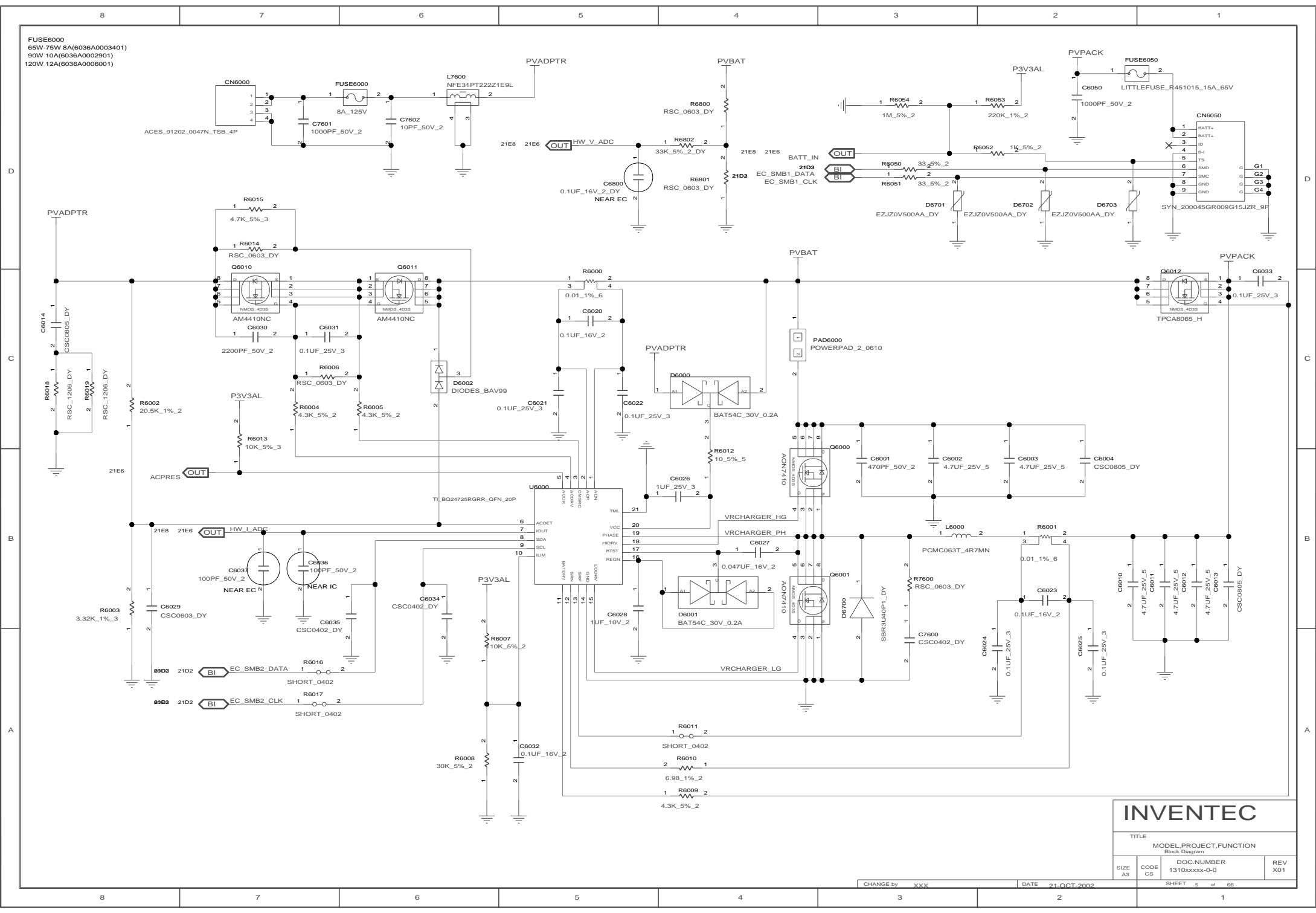
CHANGING POINTS--

TPS51218 SAME AS 2009 PROJECT
TPS51217 SAME AS 2010 PROJECT
+V1.8S IS NEW IC GMT_AT1530F11U
CHARGE IS NEW IC BQ24725
VCC CORE IS NEW IC TPS51640
VTT IS NEW IC TPS51219
V0.85 IS NEW IC TPS 51641
V3_V5 IS NEW IC TPS51123
POWER BUDGET --IC SPEC (MAX CURRENT)
PEAK CURRENT --RATIO OF INTERNAL PREDICTION
AVG CURRENT --TEST RESULT(MAX CURRENT)
INRUSH --L/S TURN NO

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FUSE6000
 65W-75W 8A(6036A0003401)
 90W 10A(6036A0002901)
 120W 12A(6036A0006001)

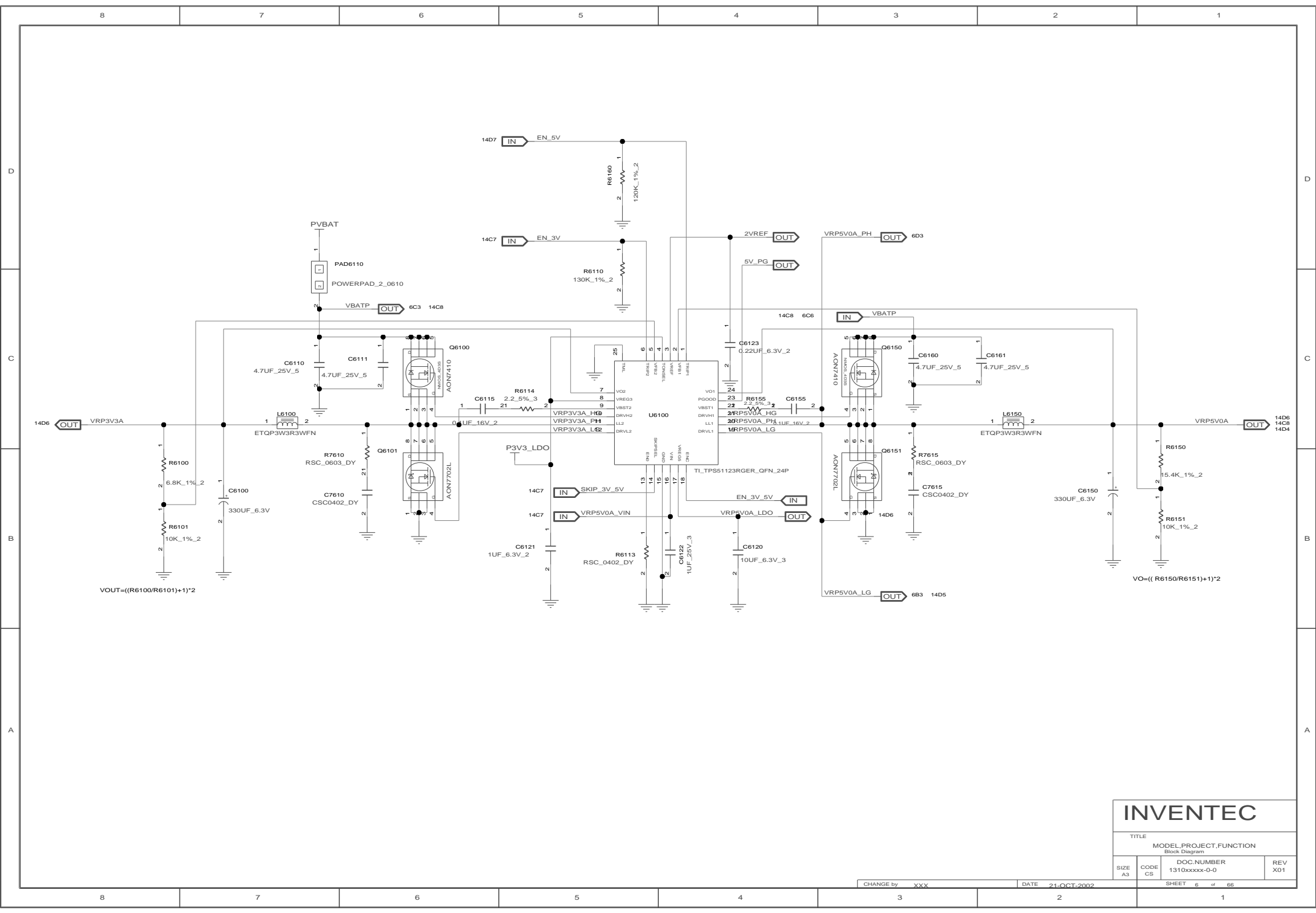


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TITLE
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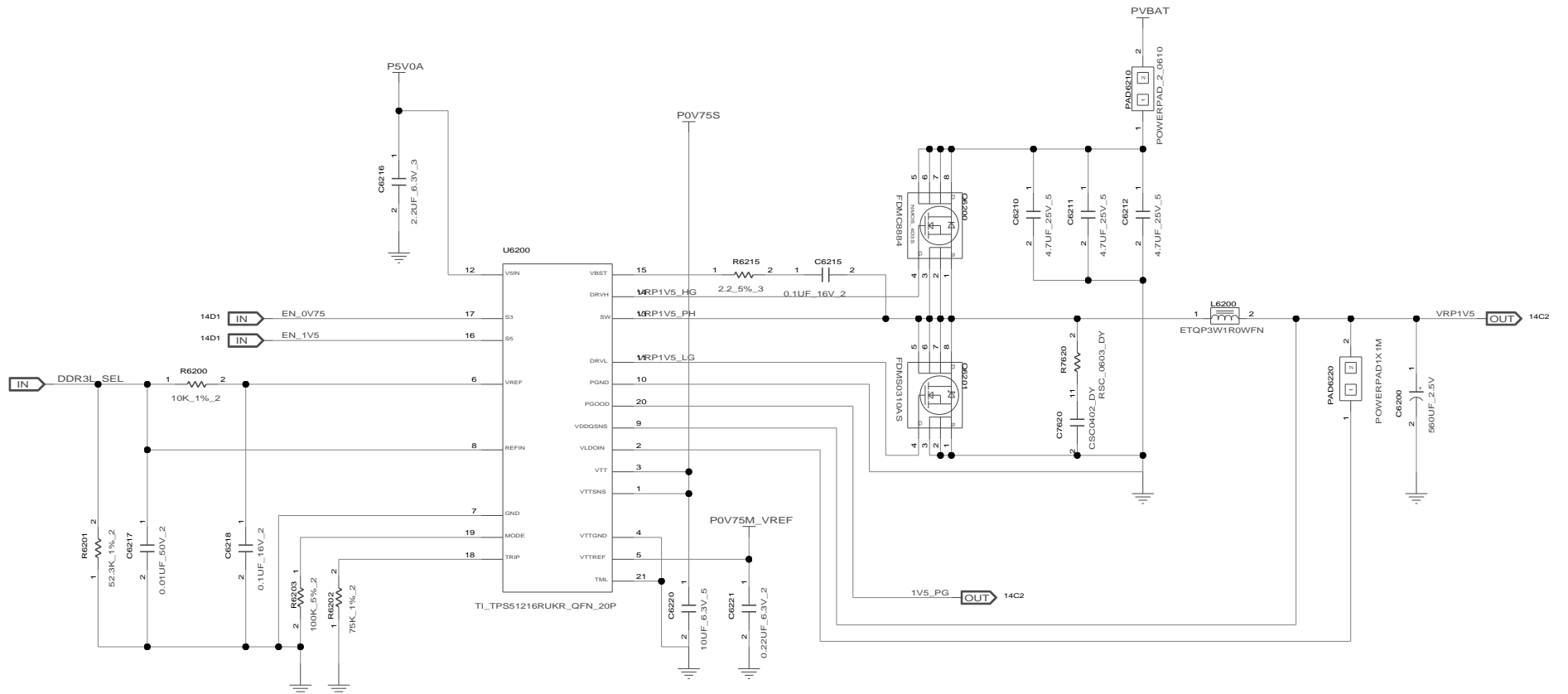
$$VOUT = ((R6100/R6101) + 1) \cdot 2$$

$$VO = ((R6150/R6151) + 1) \cdot 2$$

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$V_{OUT} = V_{REFIN} = 1.8 \cdot (R_{6201} / (R_{6200} + R_{6201}))$

MODE=100KOHM:TRACKING DISCHARGE

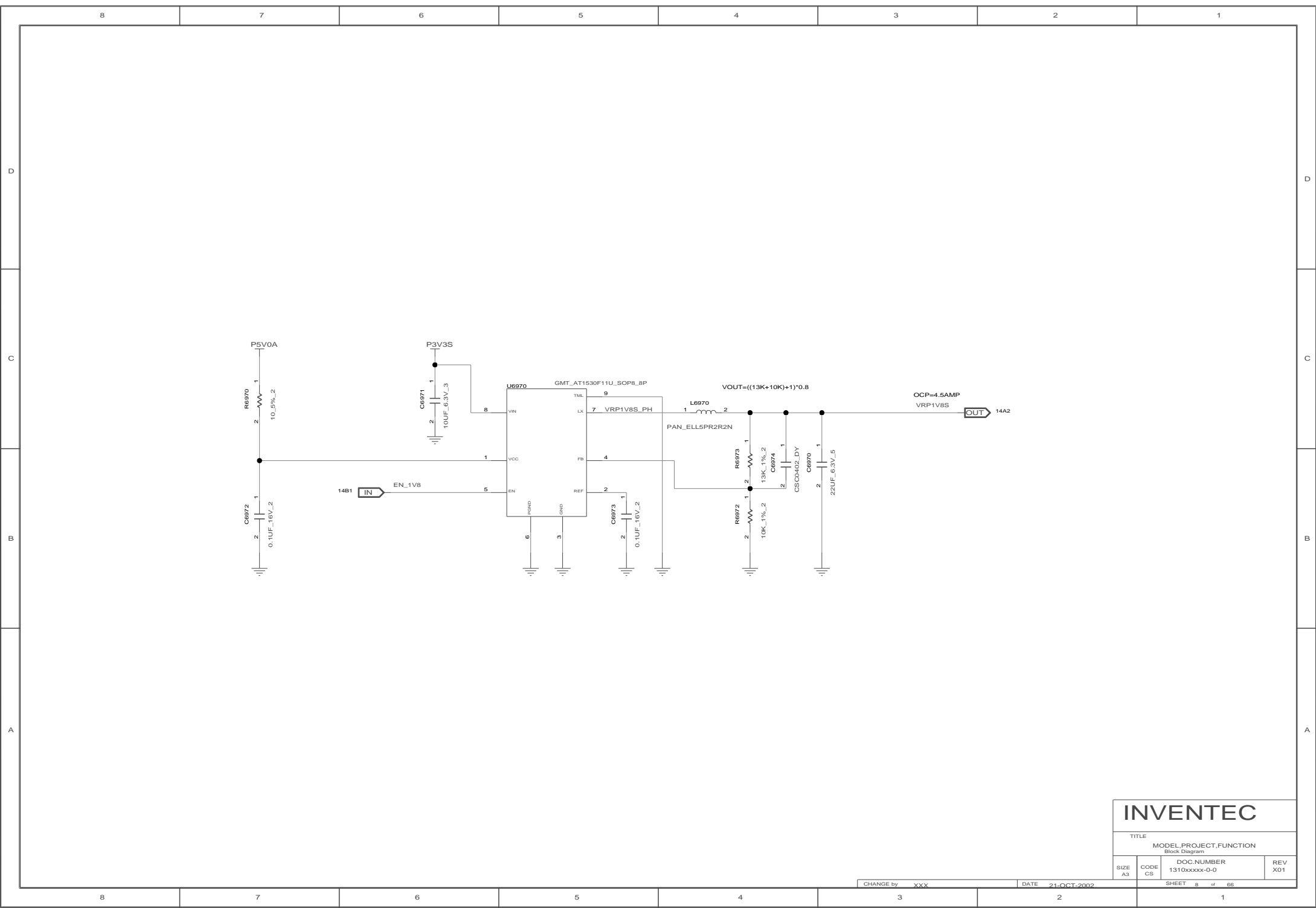
STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)

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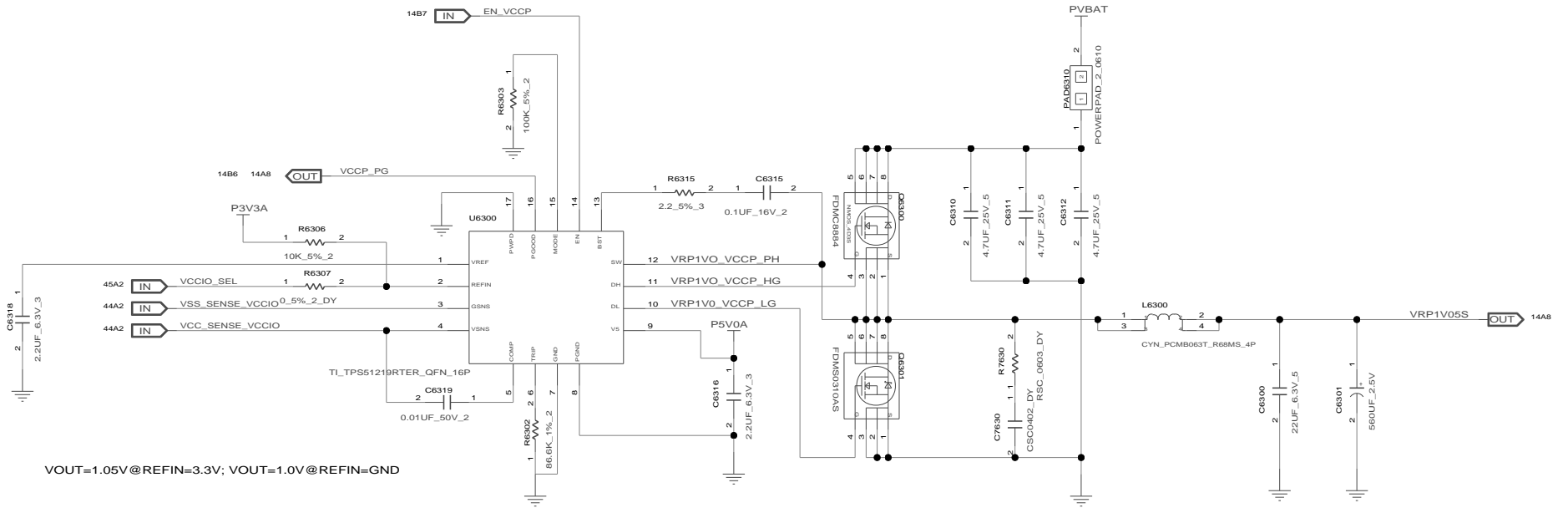
INVENTEC

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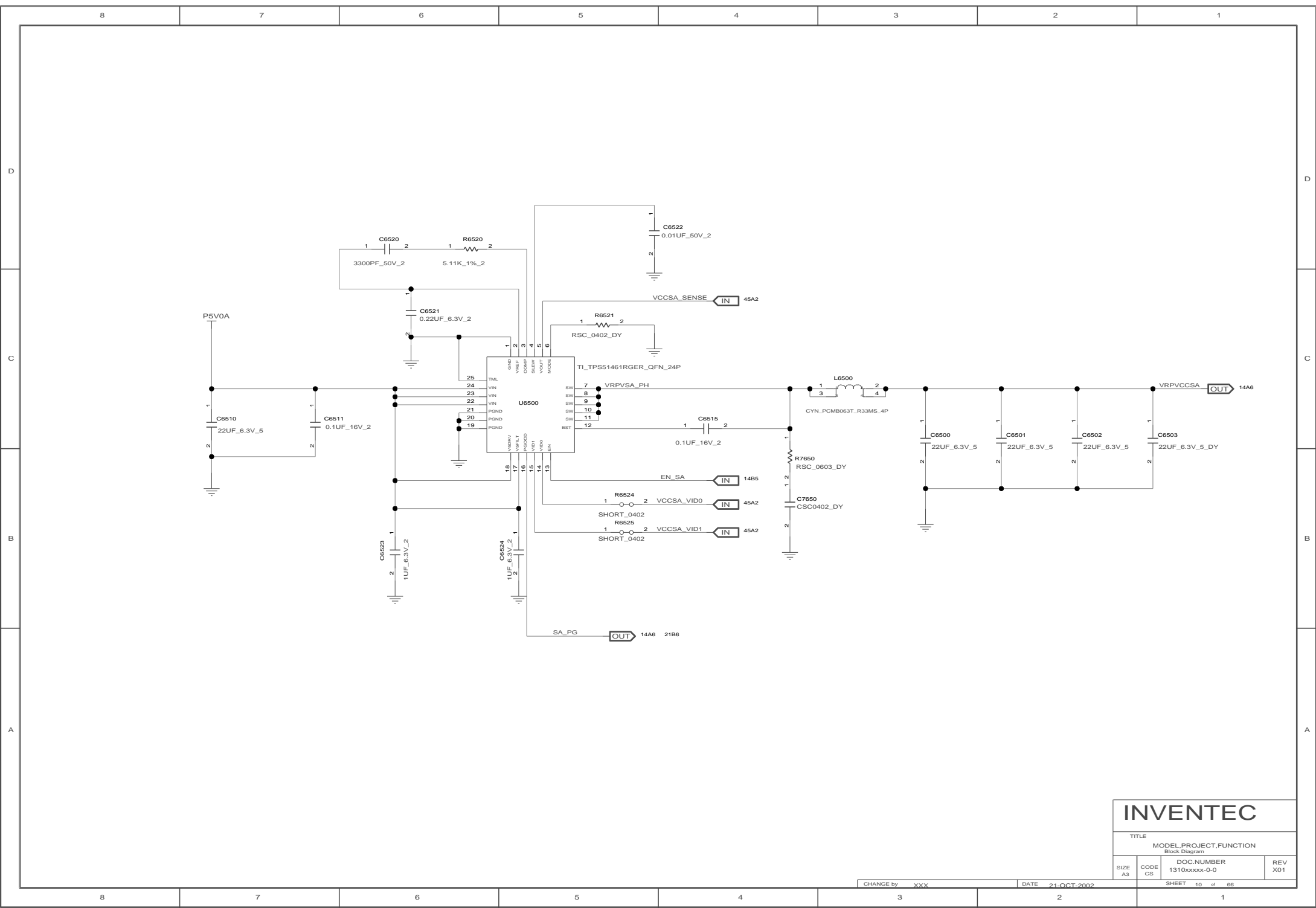
SHEET 8 of 66



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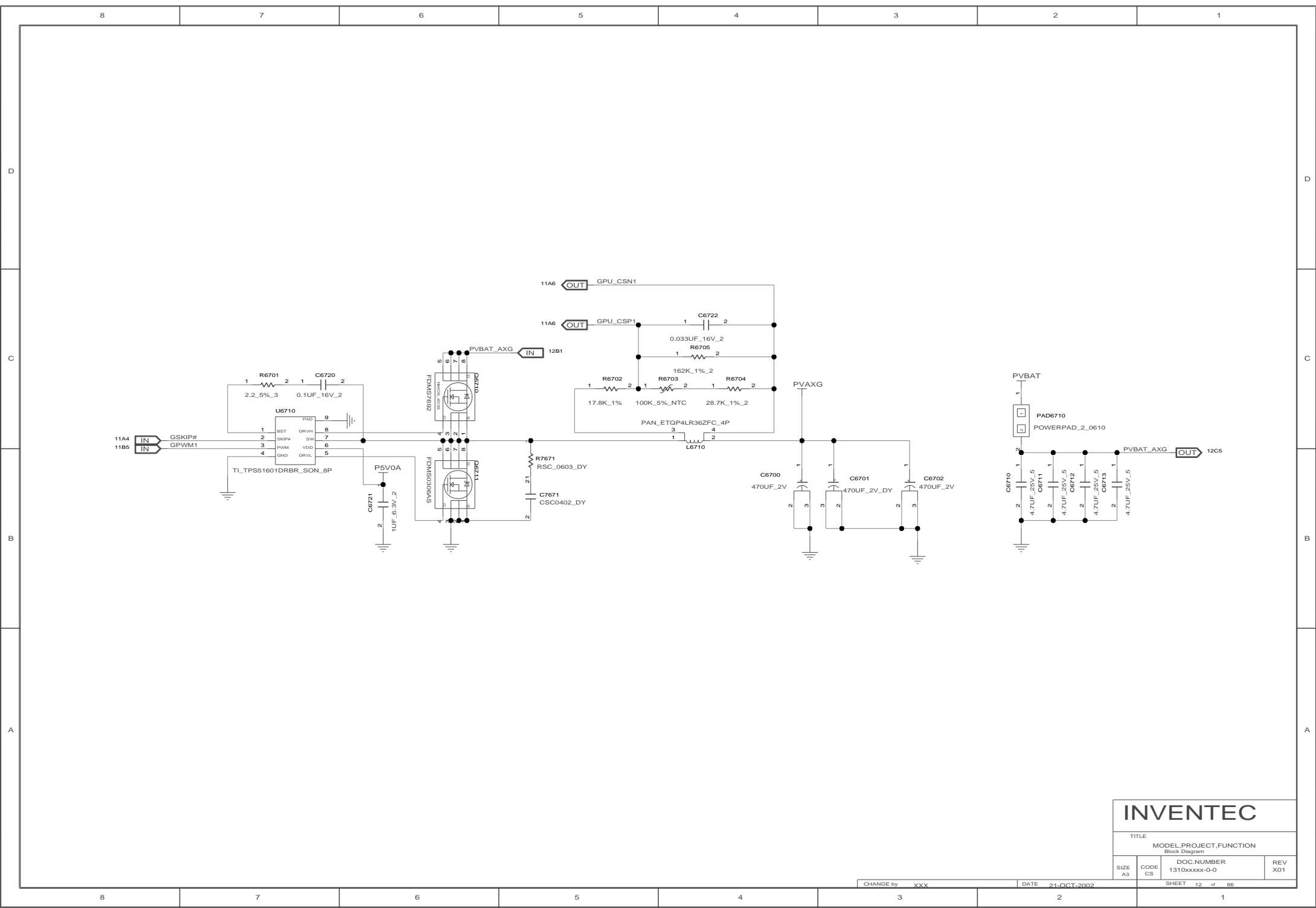
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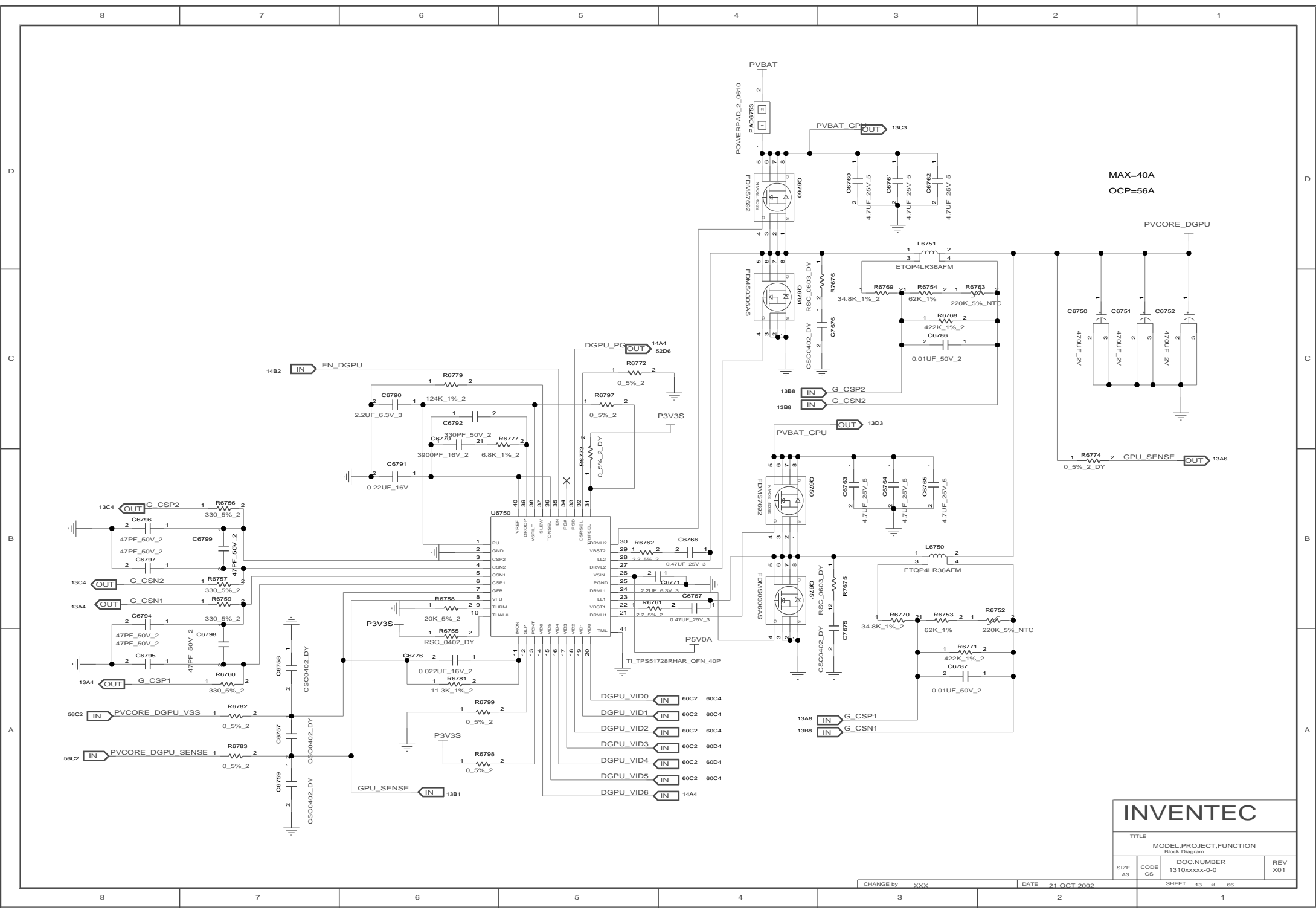
SIZE CODE DOC. NUMBER REV
A3 CS 1310xxxx-0-0 X01



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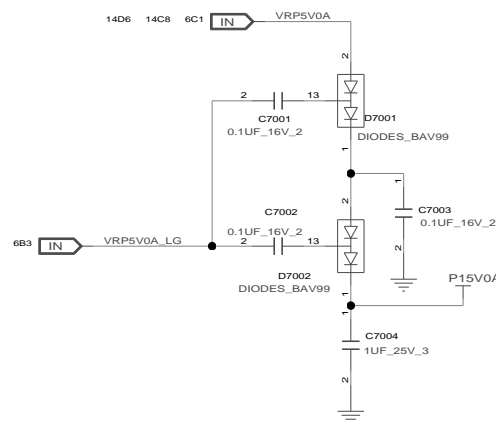
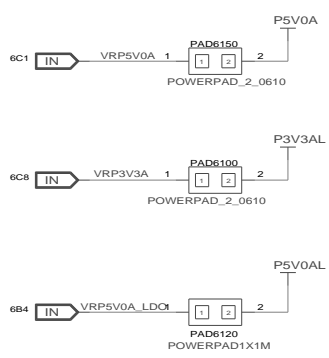
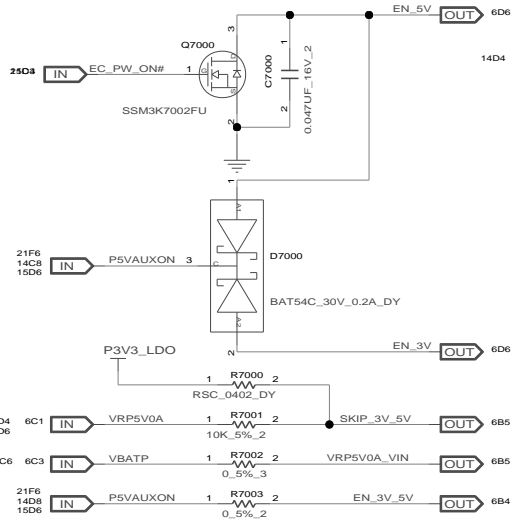
MAX=40A
OCP=56A

INVENTEC

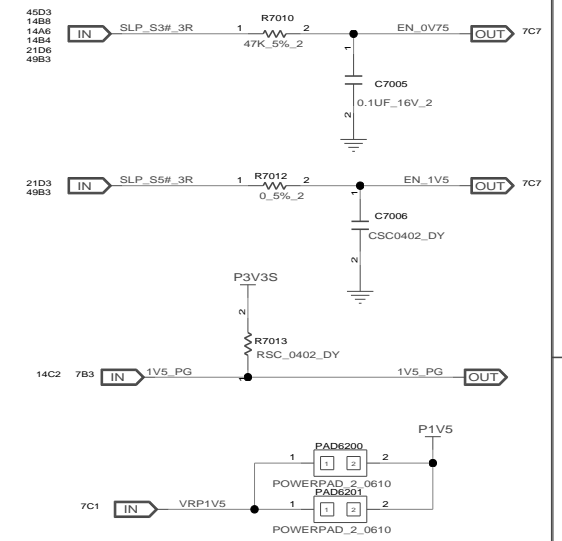
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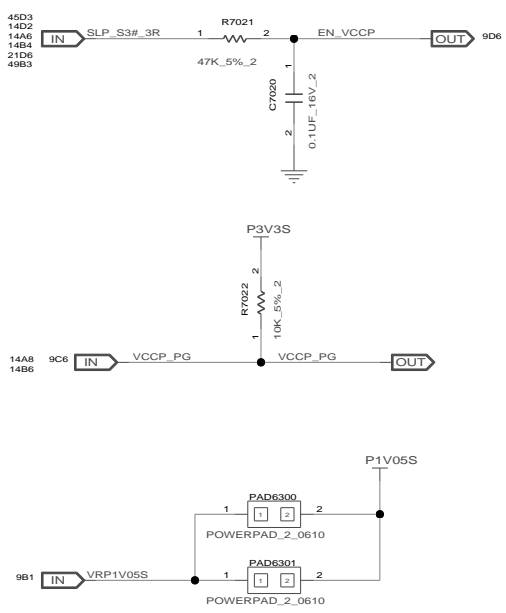
3V & 5V



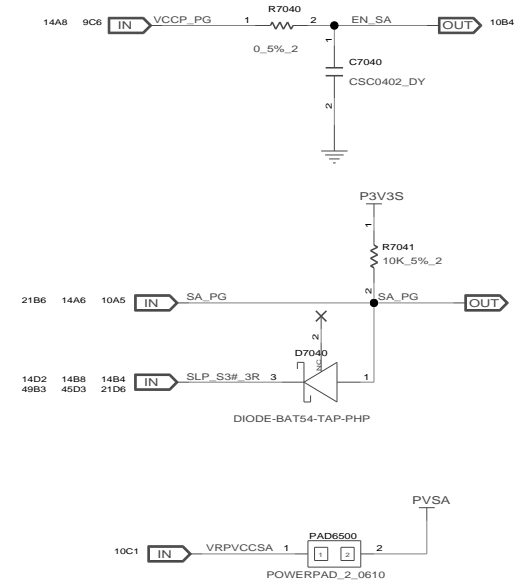
DDR_P1V5



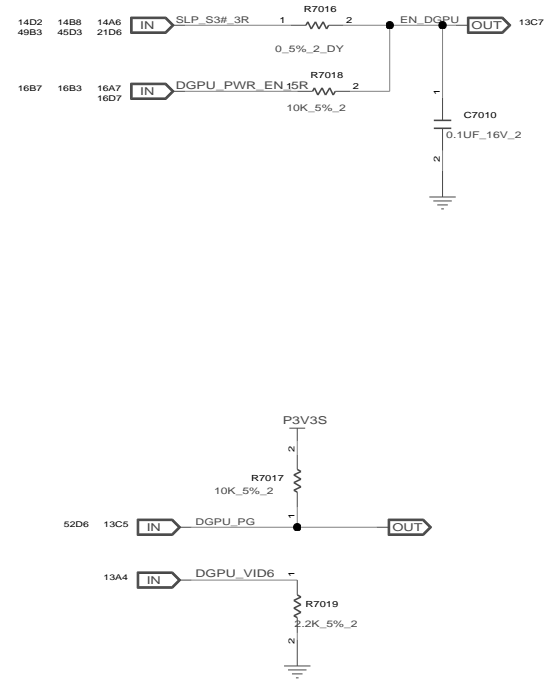
VCCIO



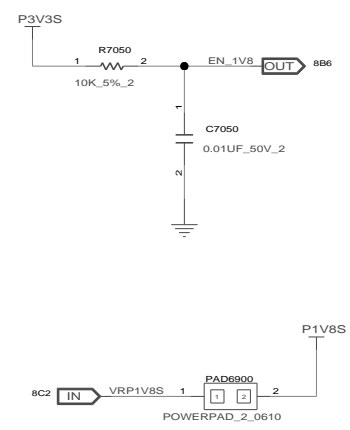
VCCSA



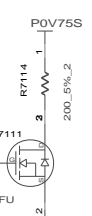
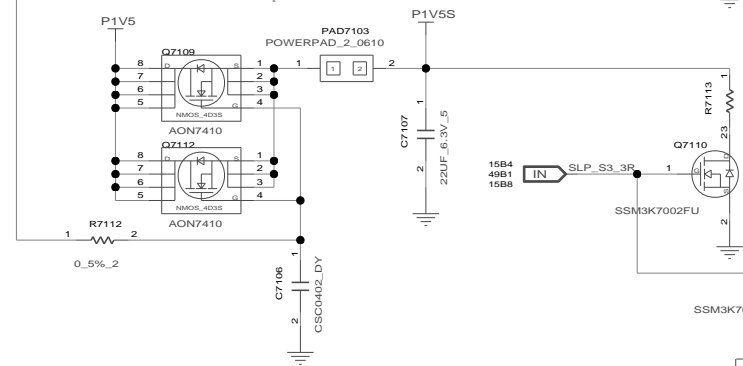
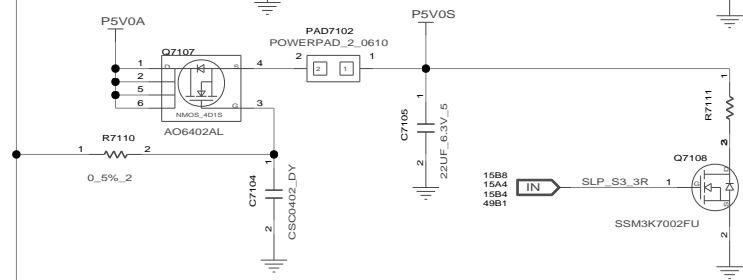
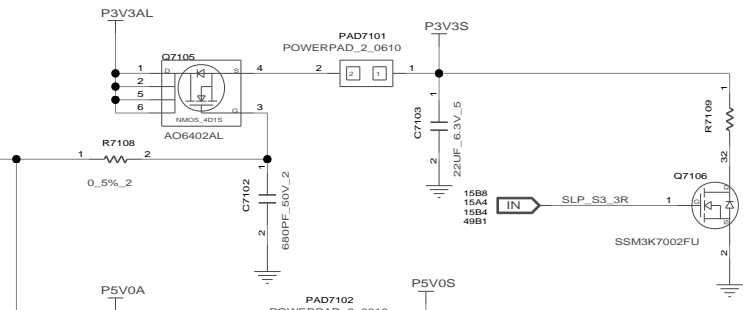
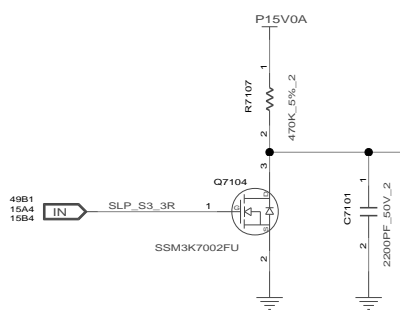
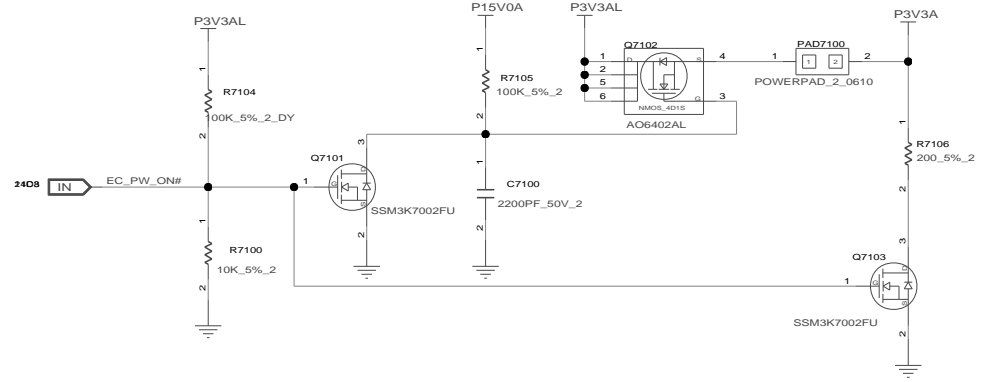
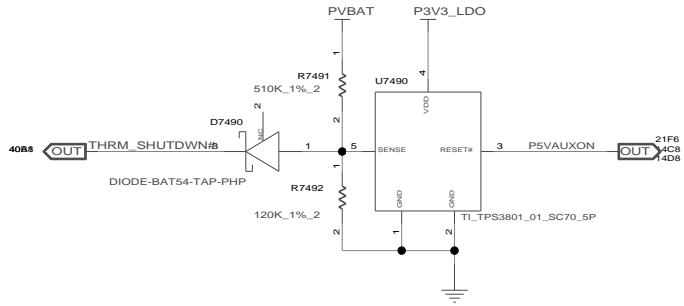
DGPU



P1V8S



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D

C

B

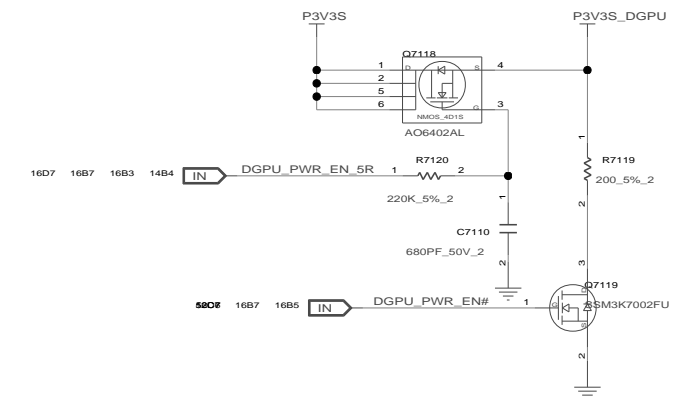
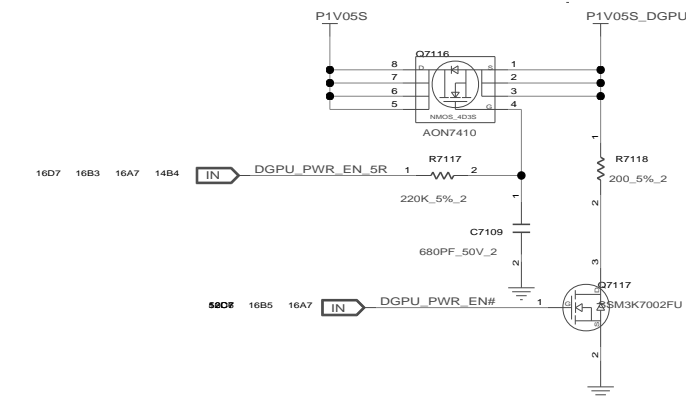
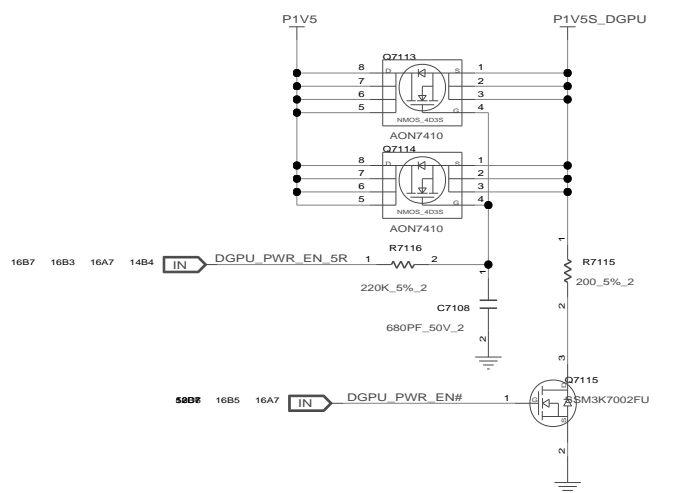
A

D

C

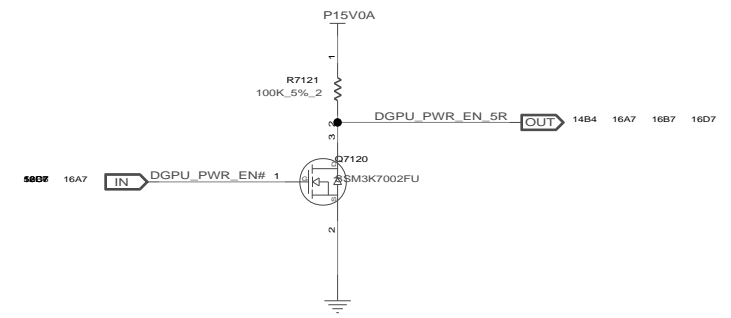
B

A



NVIDIA OPTIMUS

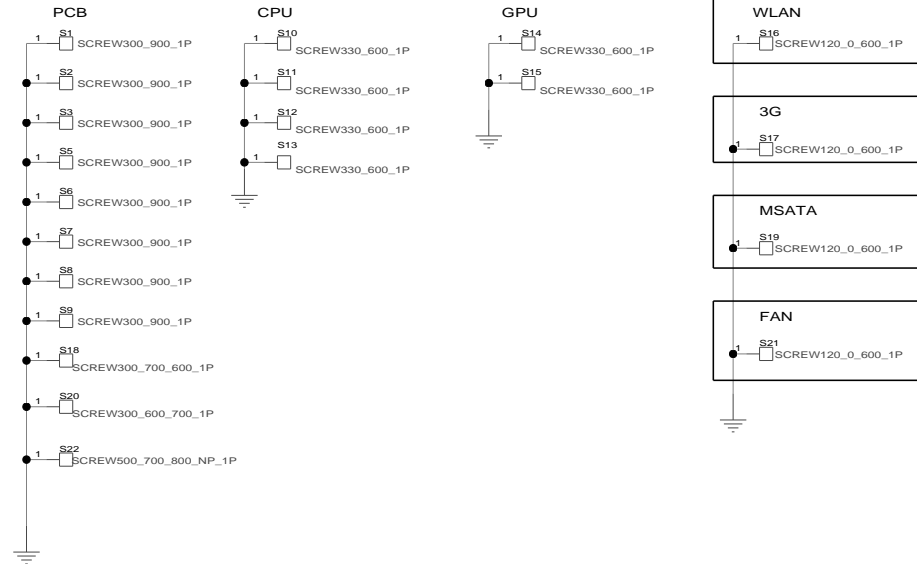
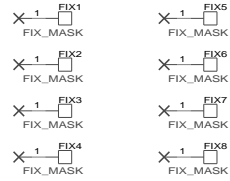
	DURING RESET	AFTER RESET	
DGPU_PWR_EN#	HIGH	HIGH	0 : DGPU POWER SWITCH TURNED ON 1 : POWER SWITCH TURNED OFF
DGPU_PG			0 : DGPU POWER IS NOT STABLE 1 : DGPU POWER IS STABLE
DGPU_HOLD_RST#	LOW	LOW	0 : KEEP DGPU IN RESET 1 : RESET IS RELEASED



INVENTEC

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MODEL,PROJECT,FUNCTION			
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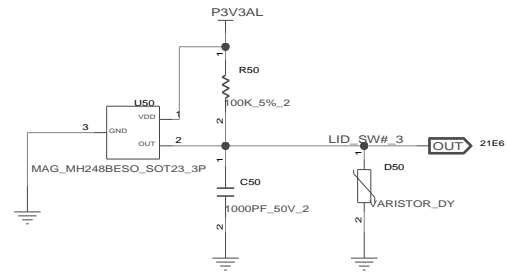
REFERENCE 0~49(PCB SCREW)



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REFERENCE 50-99(HALL SENSOR)



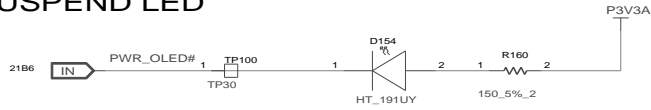
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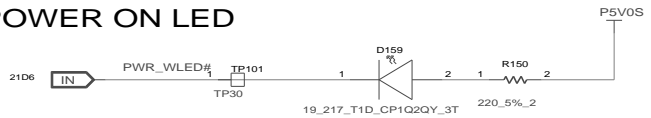
SUSPEND LED



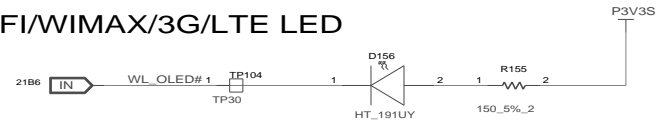
BATTERY LED

CHARGE:BRIGHT

POWER ON LED

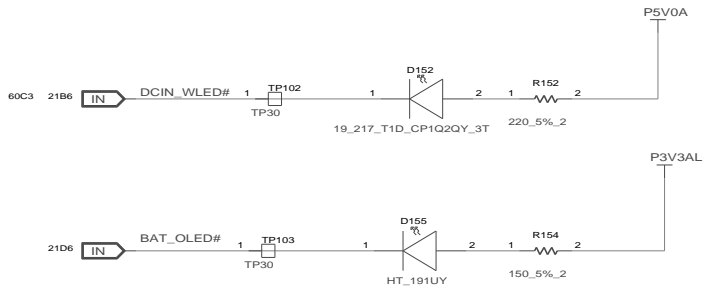


WIFI/WIMAX/3G/LTE LED



DC IN / BATTERY CHARGE LED

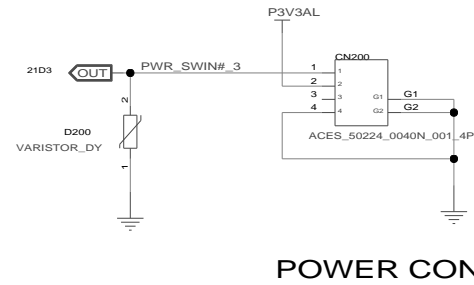
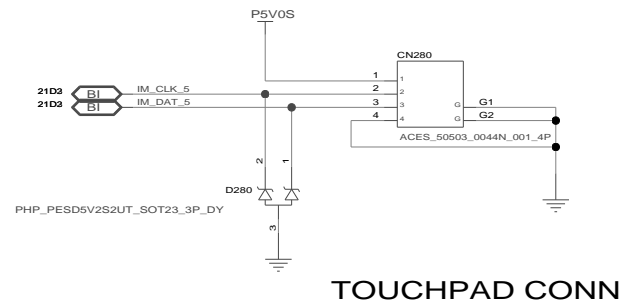
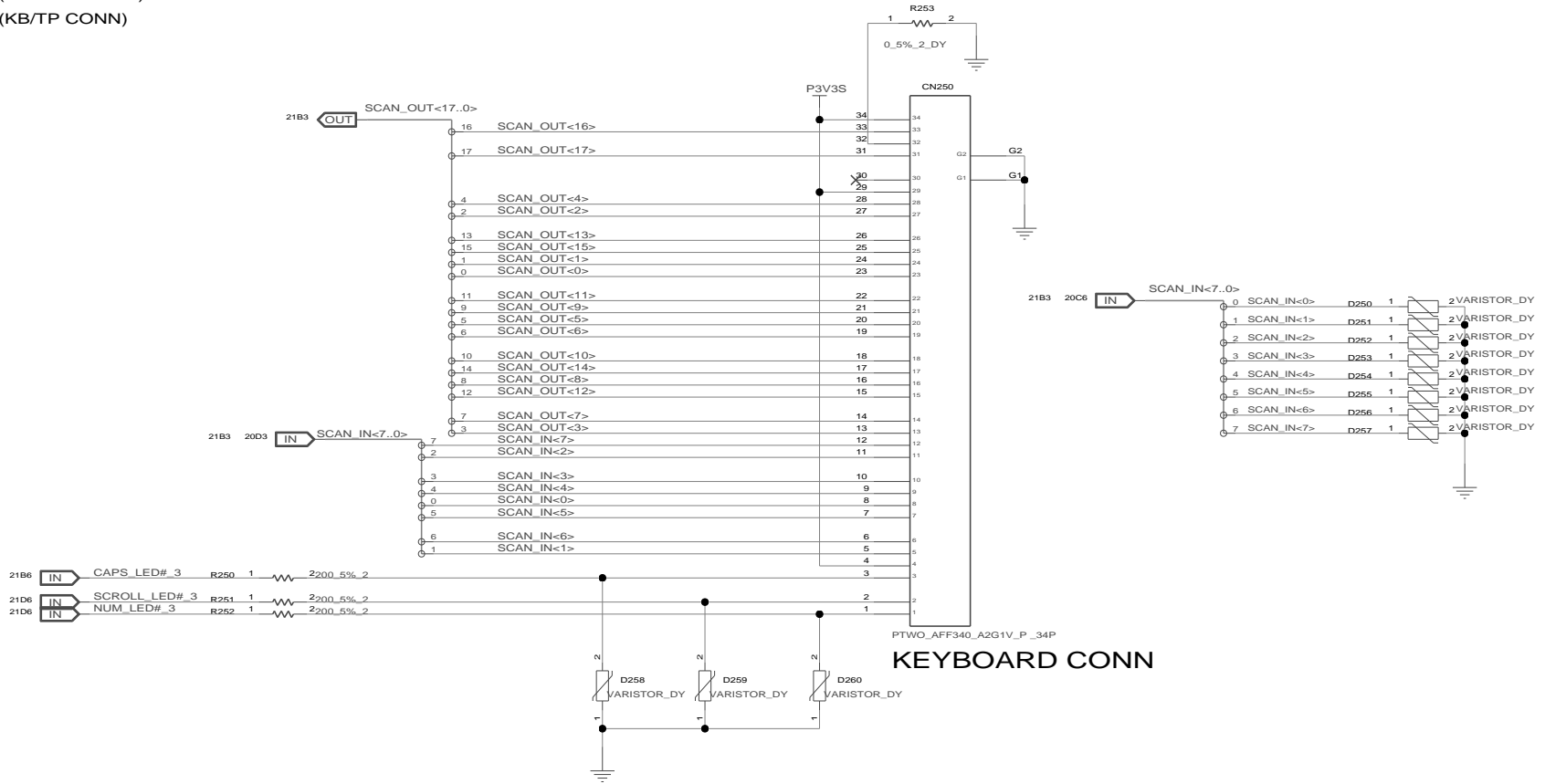
D152 BRIGHT:BOTH AC-ADAPTER IS PLUGGED IN AND BATTERY IS FULL CHARGED
 D155 BRIGHT:WHILE CHARGING BATTERY FROM AC-ADAPTER
 BLINK:LOW BATTERY



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REFERENCE 200~249(POWER CONN)
 REFERENCE 250~299(KB/TP CONN)



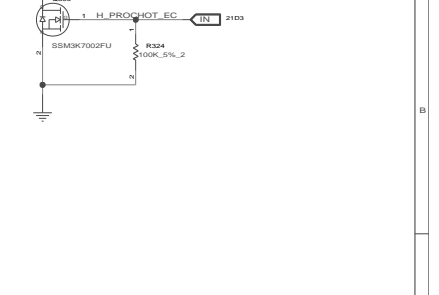
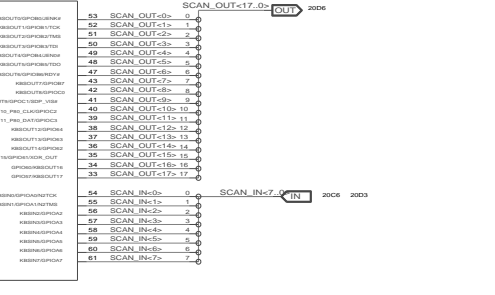
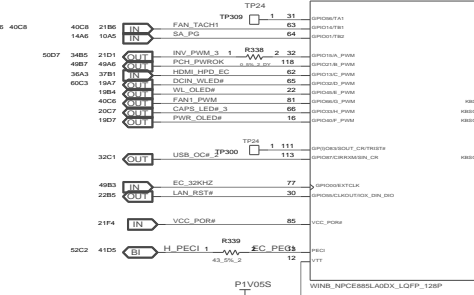
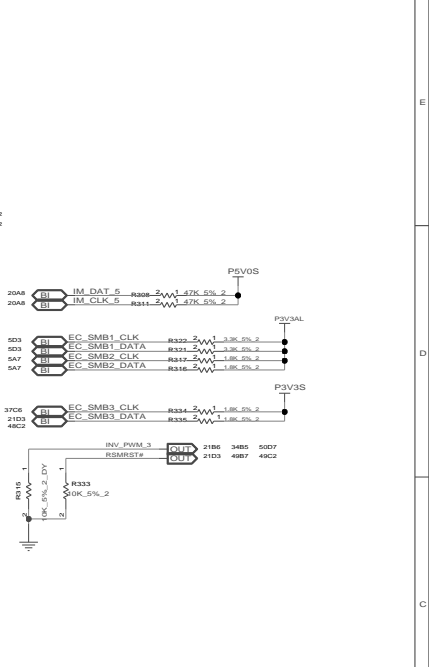
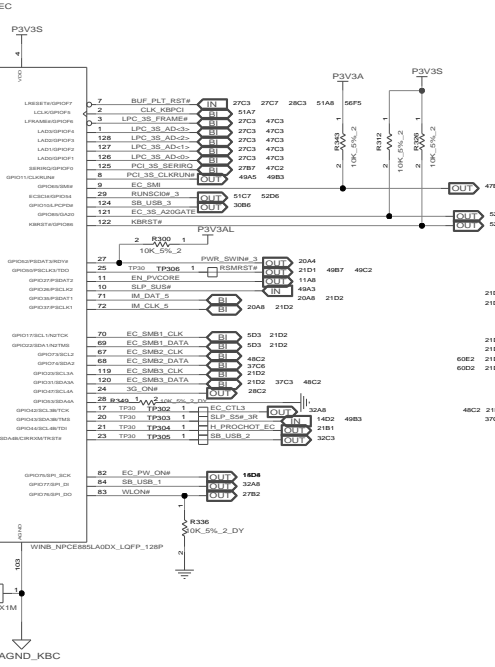
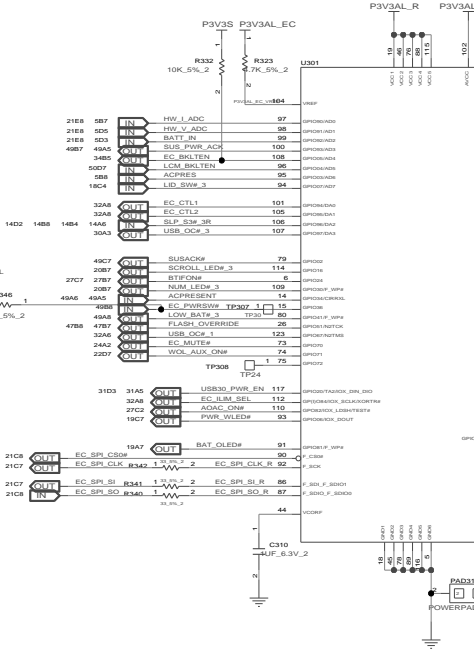
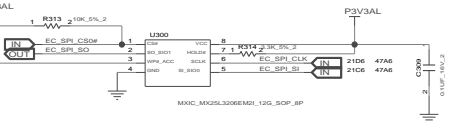
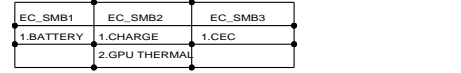
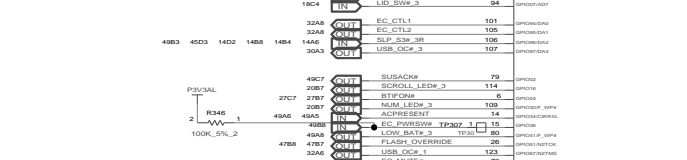
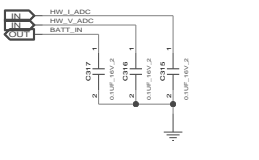
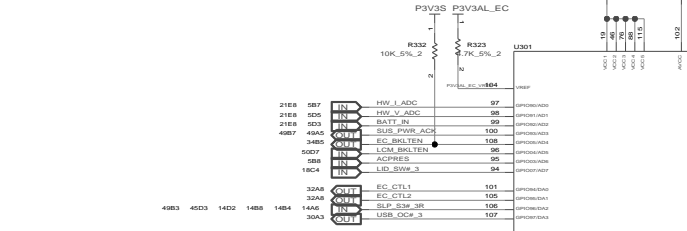
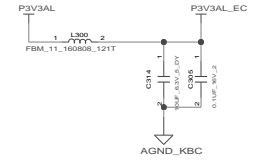
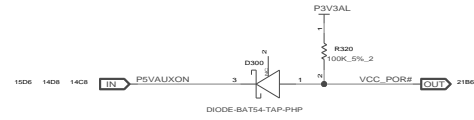
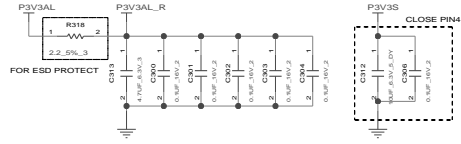
INVENTEC

TITLE
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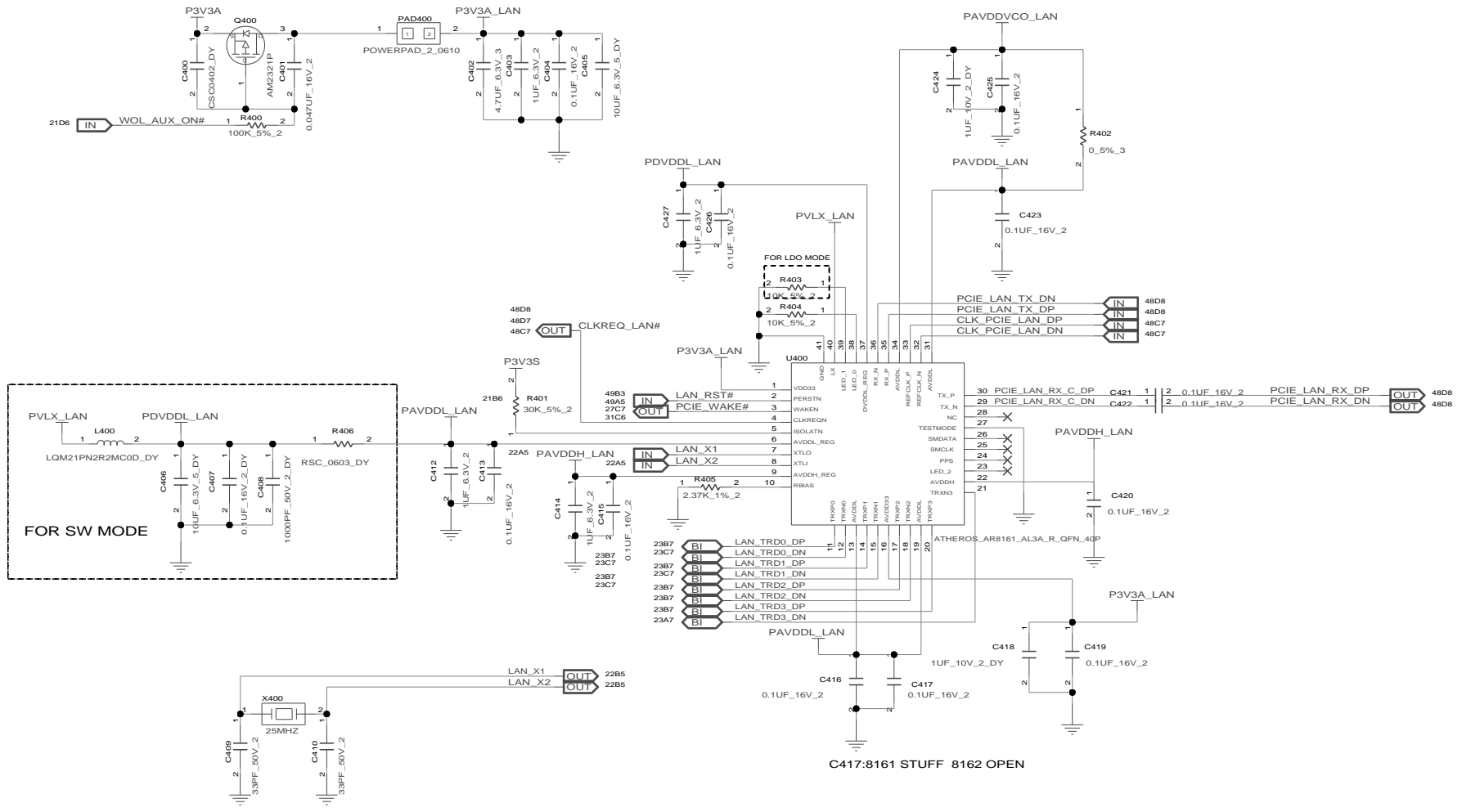
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REFERENCE 300-389(KBC)



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REFERENCE 400~499(LAN)

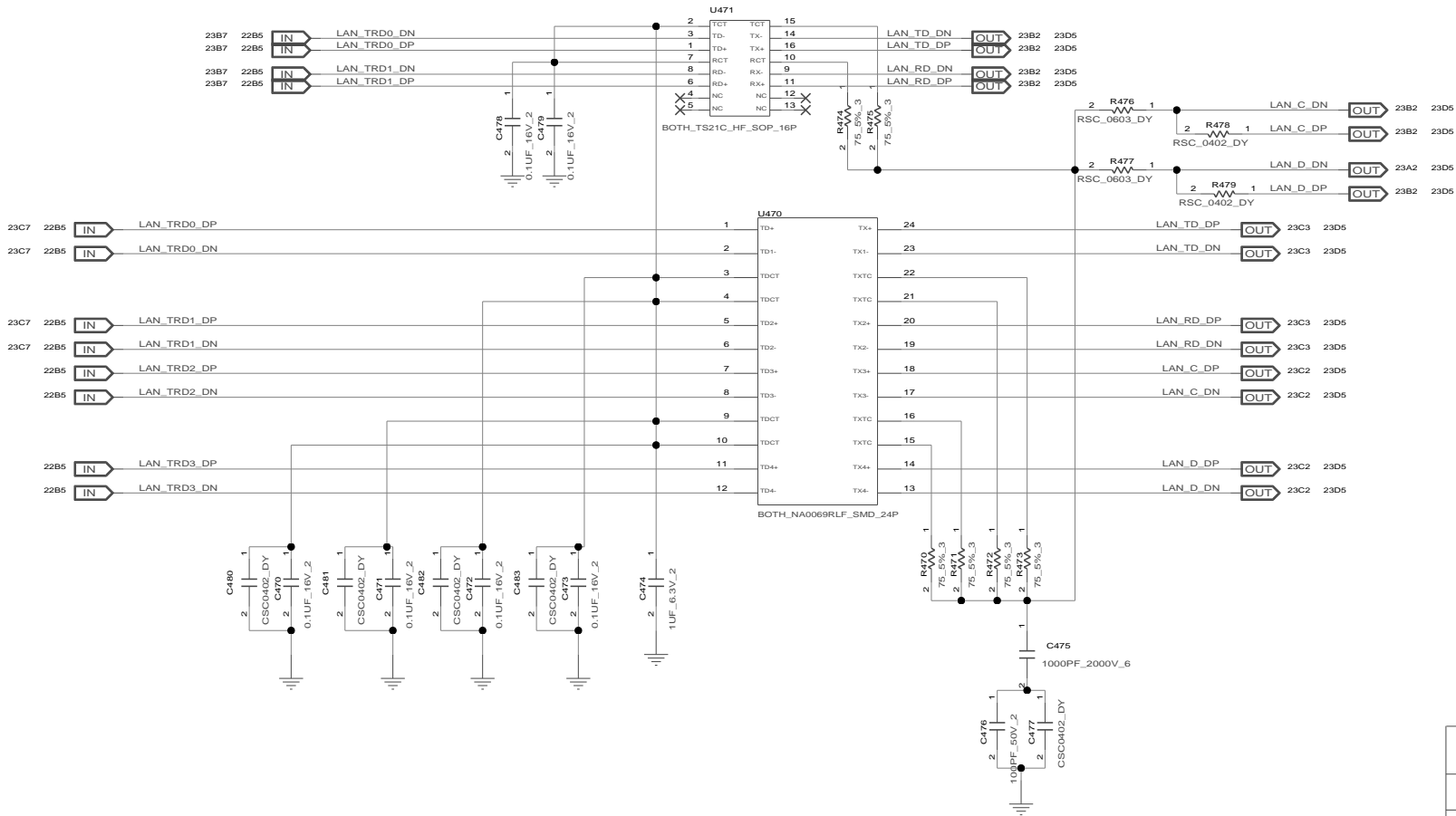
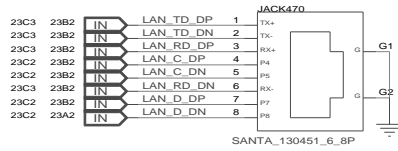


C417:8161 STUFF 8162 OPEN

INVENTEC

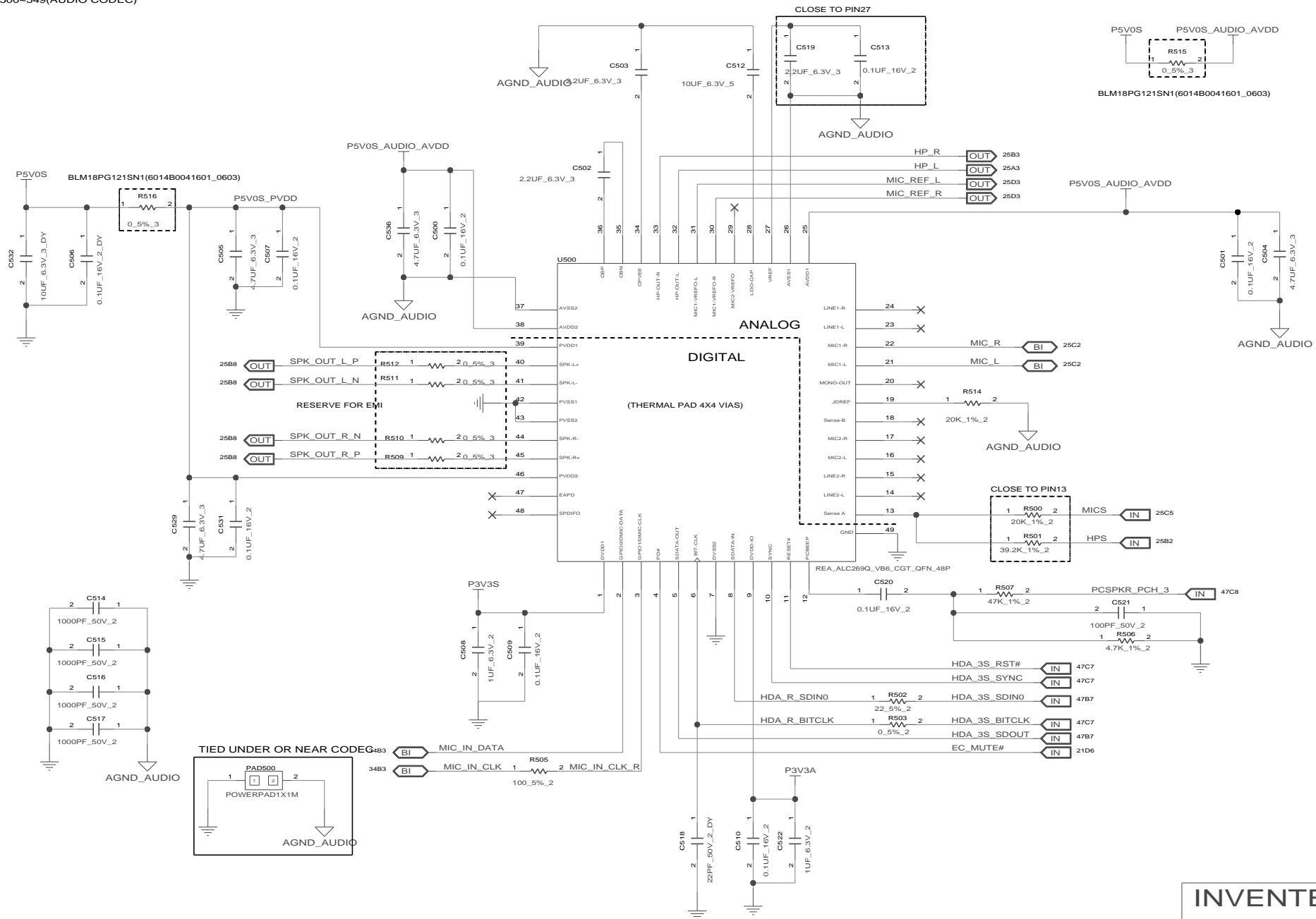
TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 22 of 66

REFERENCE 400~499(LAN)



INVENTEC			
TITLE MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01

REFERENCE 500-549(AUDIO CODEC)



INVENTEC

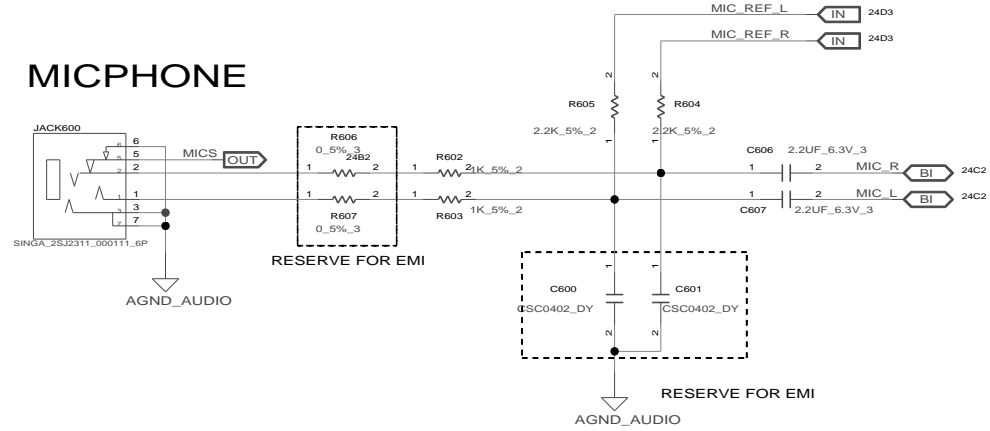
TITLE
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
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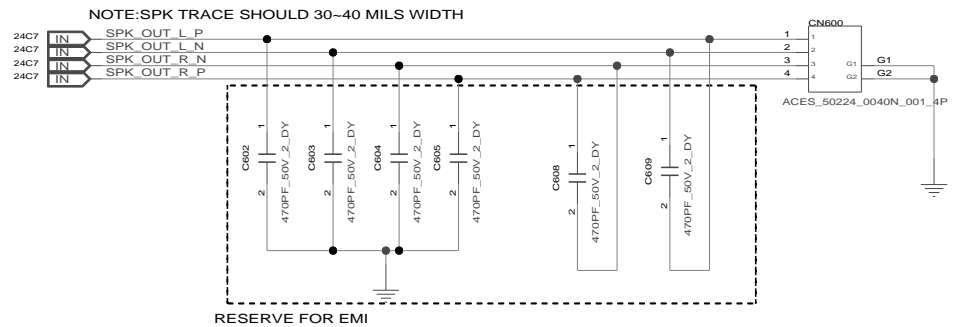
CHANGE by XXX DATE 21-OCT-2002 SHEET 24 of 66

AUDIO JACKS

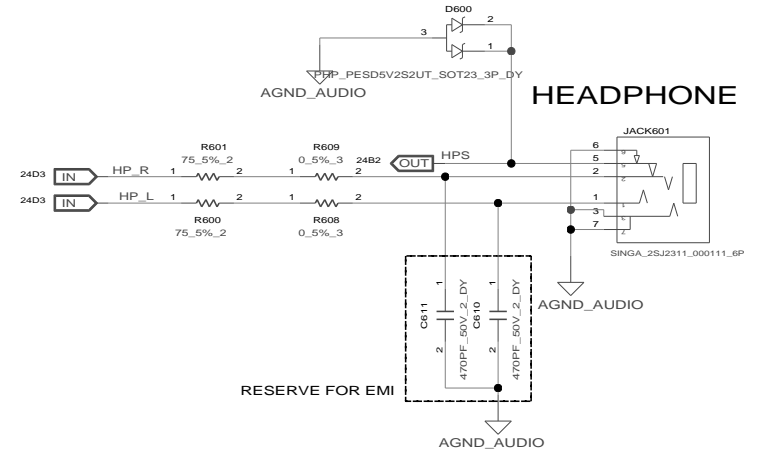
MICPHONE



INTERNAL SPEAKERS



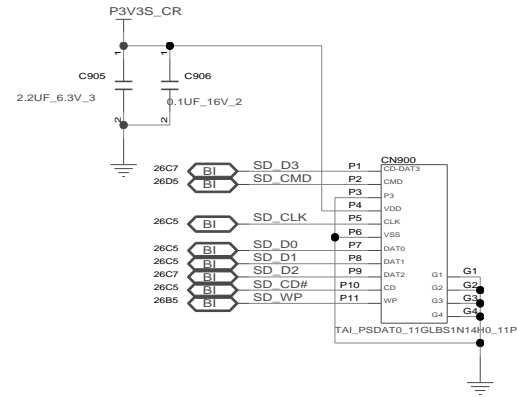
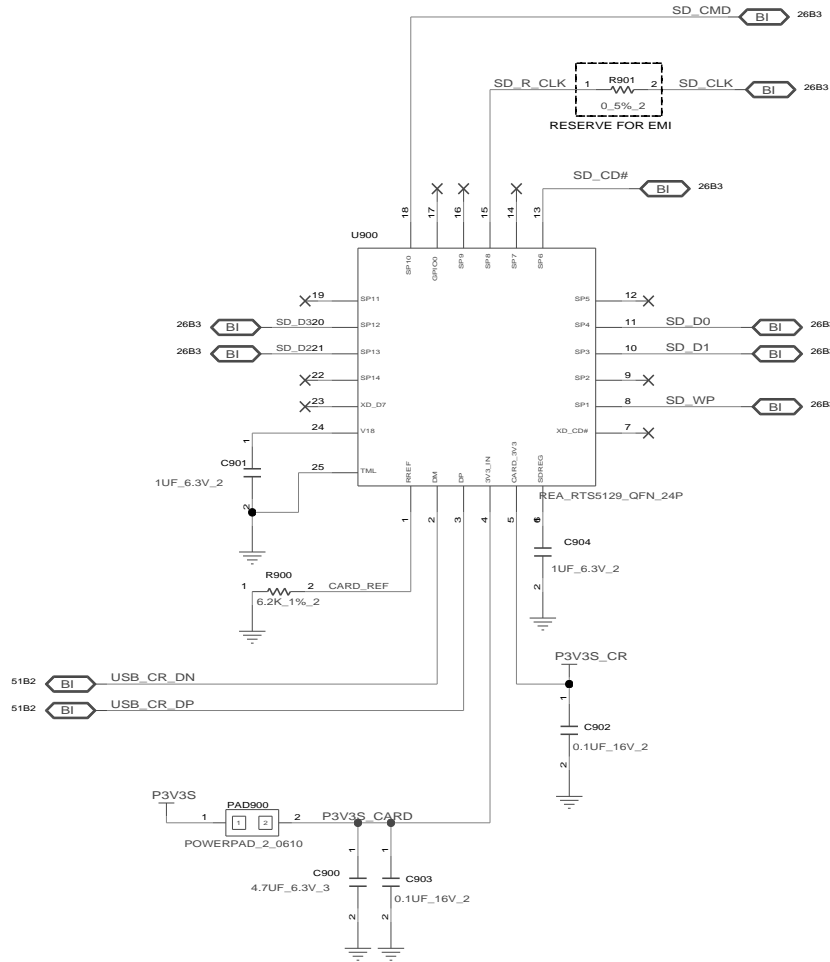
HEADPHONE



INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 25 of 66

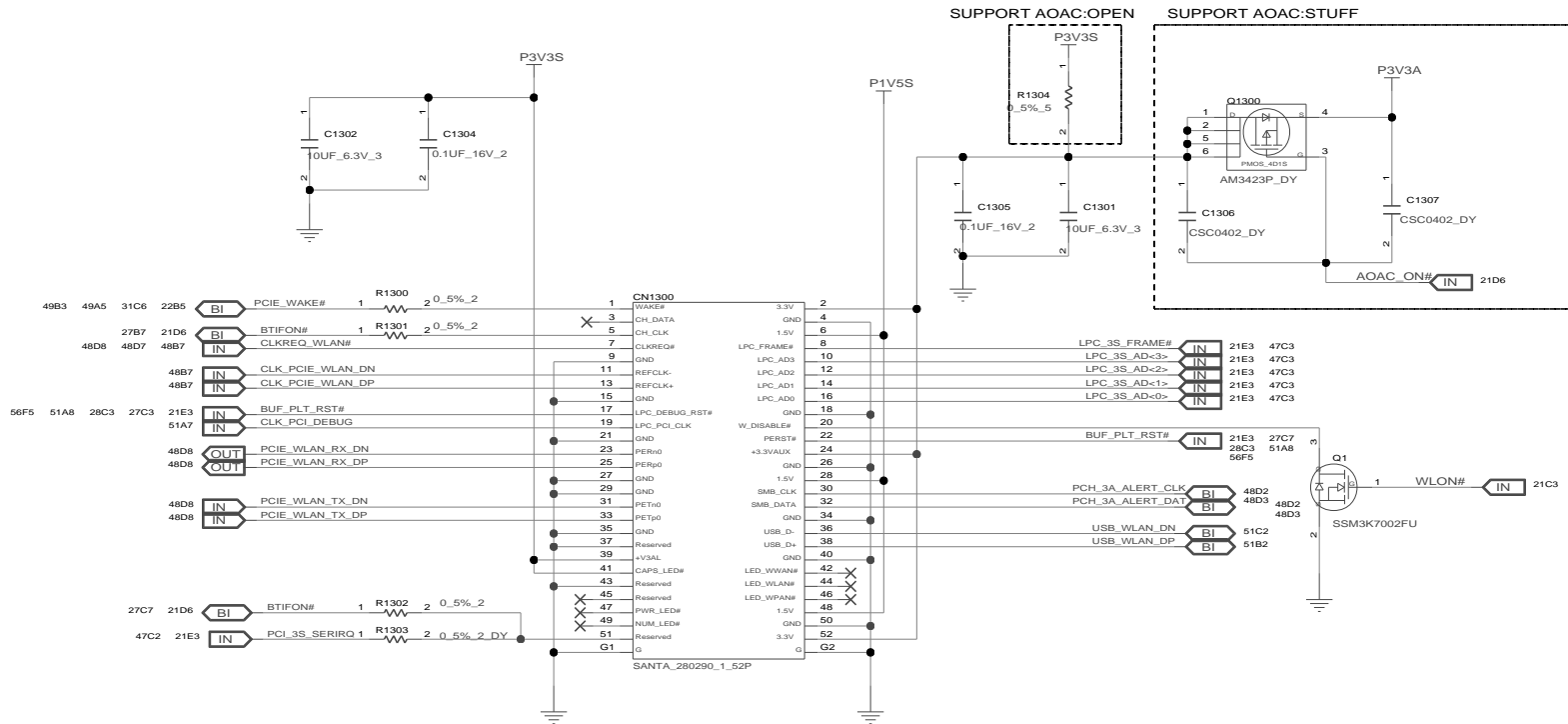
REFERENCE 900~999(CARDREADER)



INVENTEC

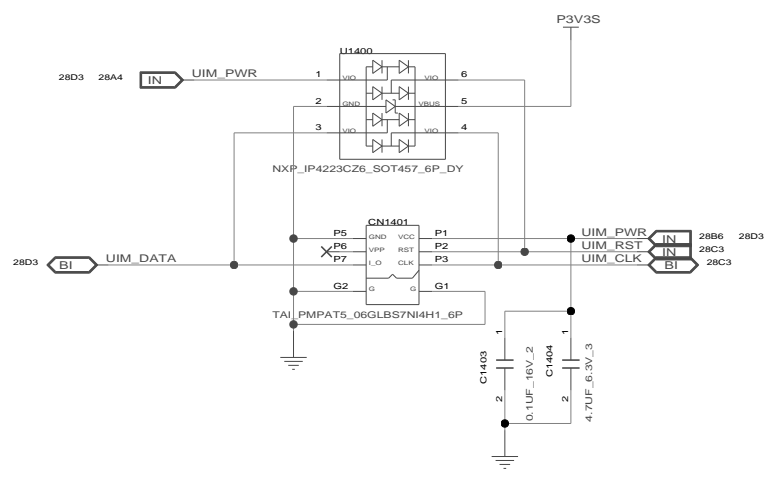
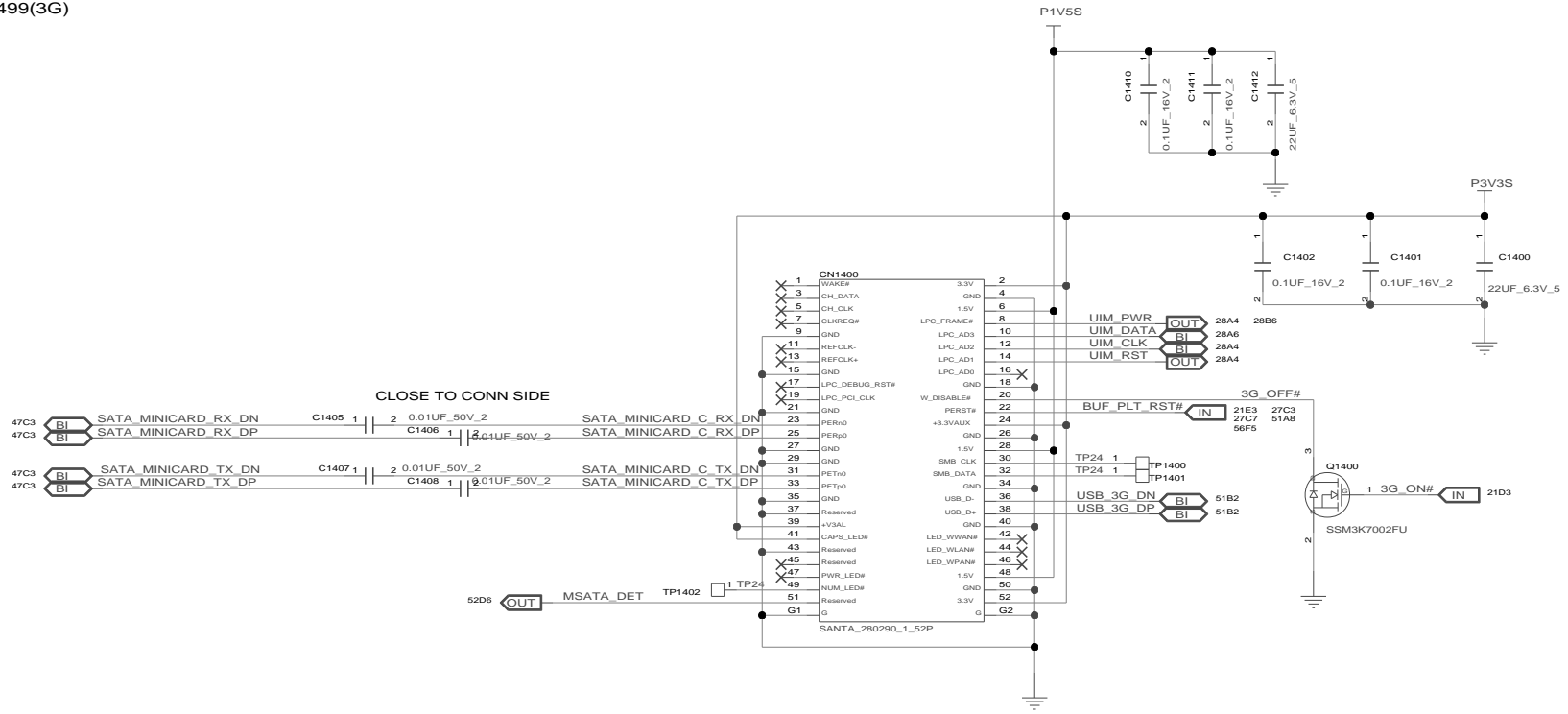
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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MINI CARD 1(WLAN)

INVENTEC			
TITLE MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 27 of 66



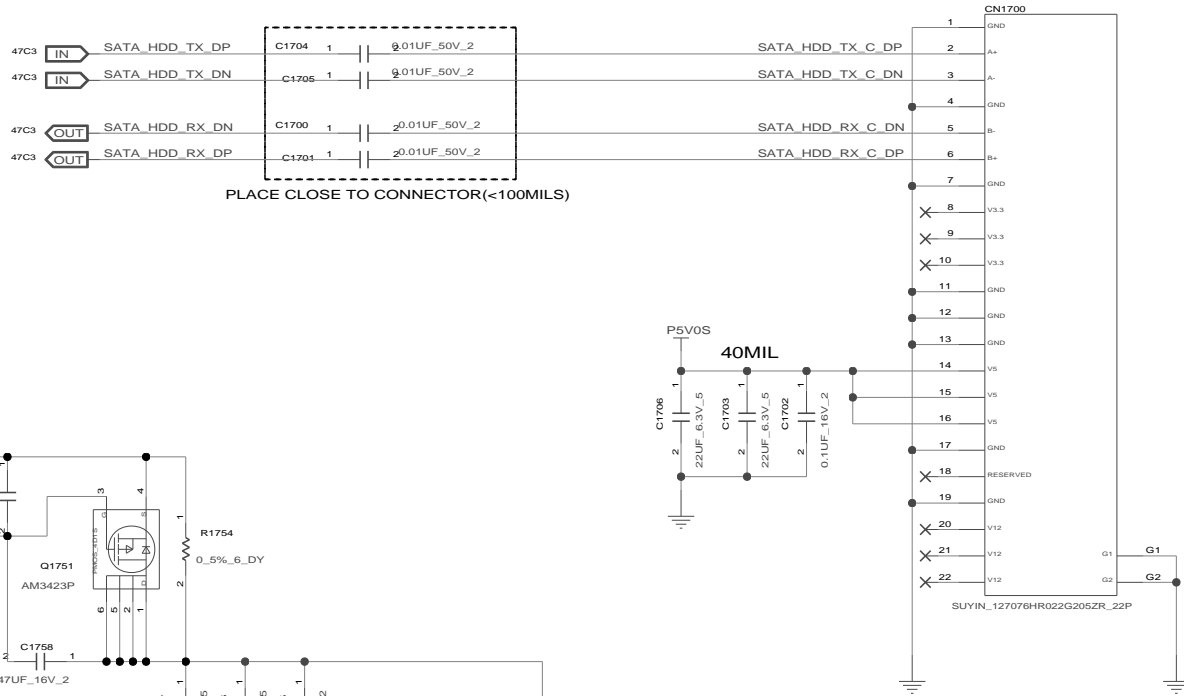
INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

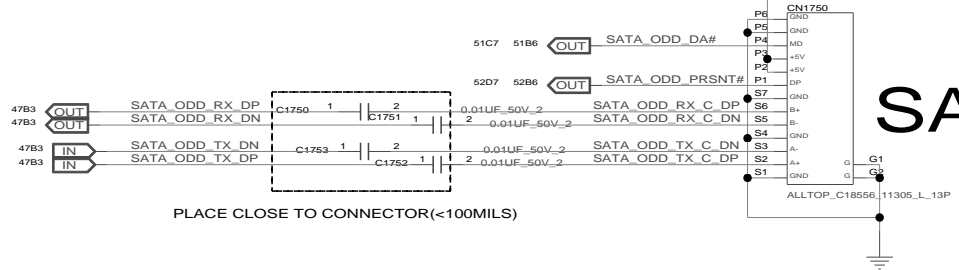
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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REFERENCE 1700~1749(HDD)
 REFERENCE 1750~1799(ODD)

SATA HDD



SATA ODD

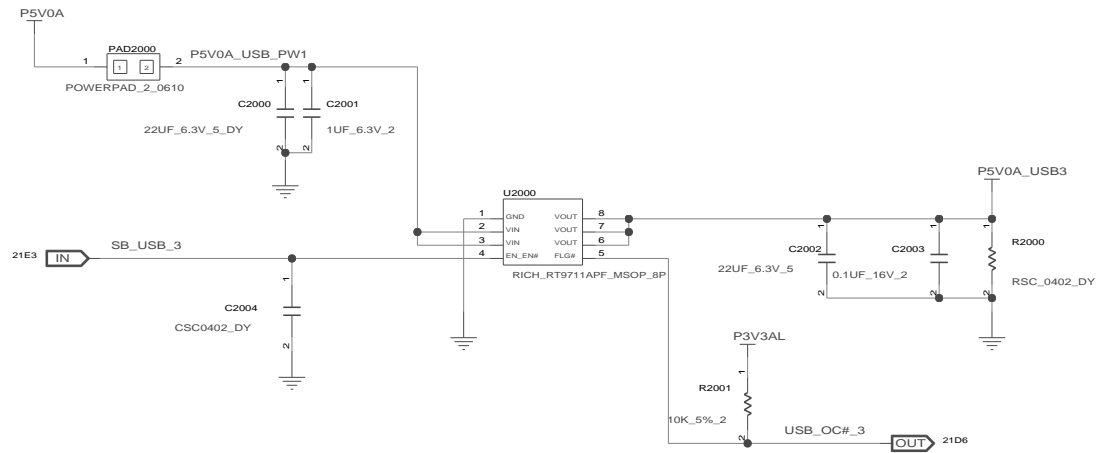
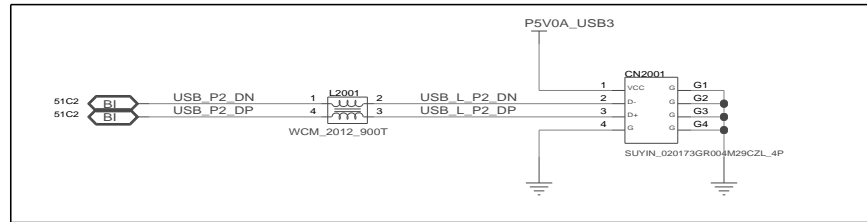


INVENTEC

TITLE
 MODEL,PROJECT,FUNCTION
 Block Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
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PLACEMENT @LEFT SIDE

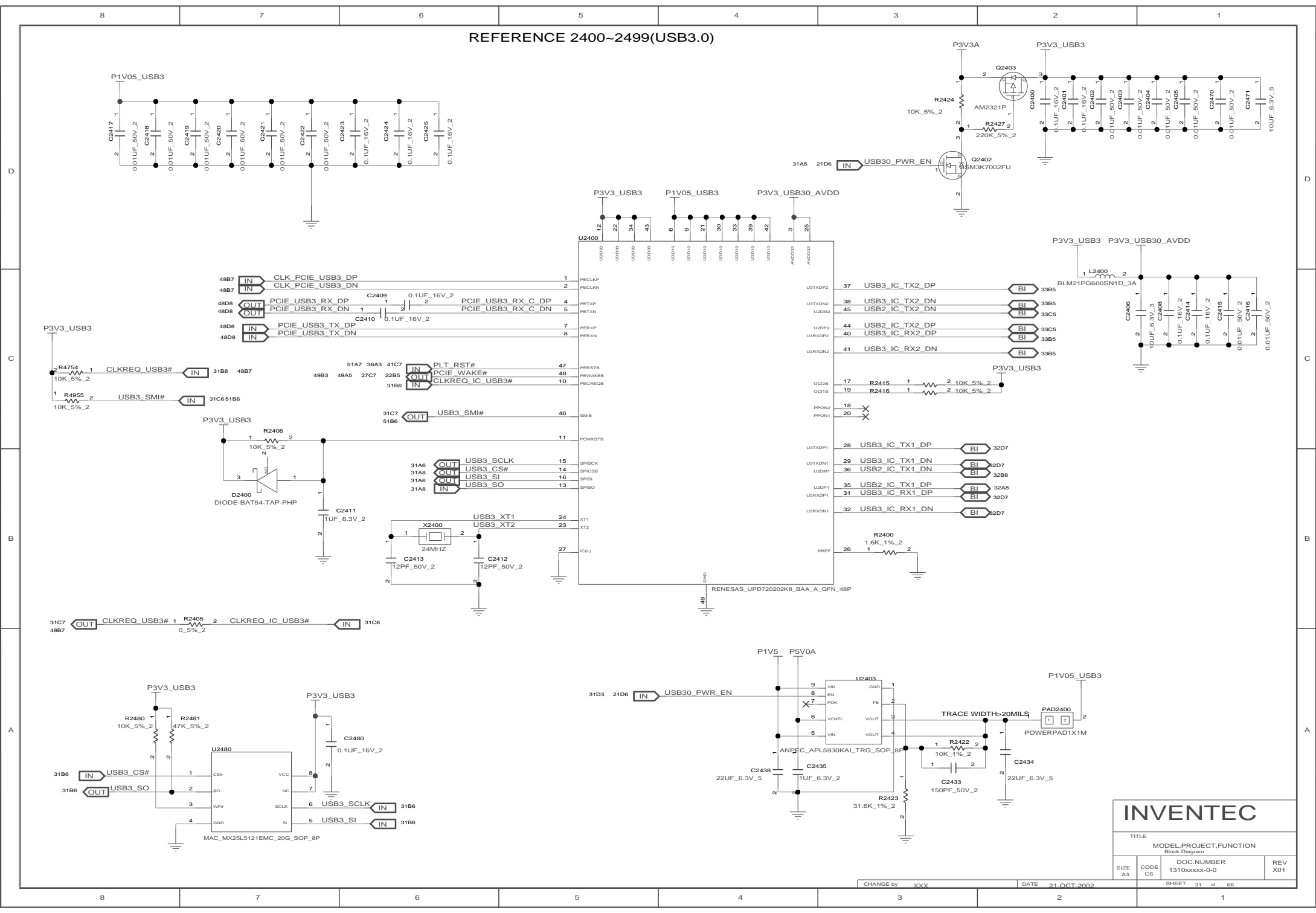


INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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REFERENCE 2400~2499(USB3.0)

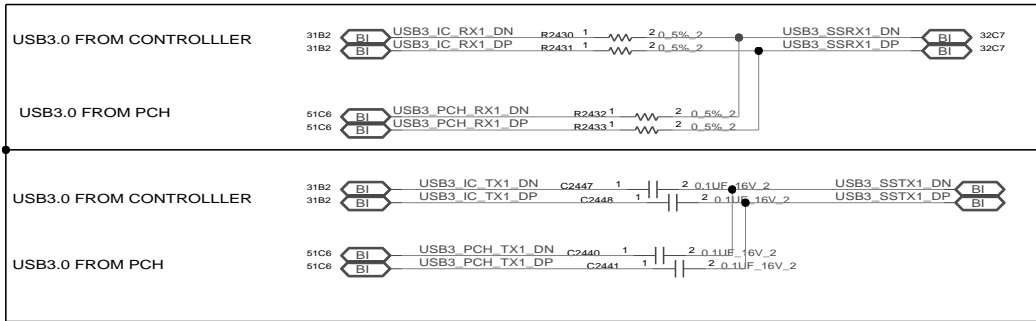


INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

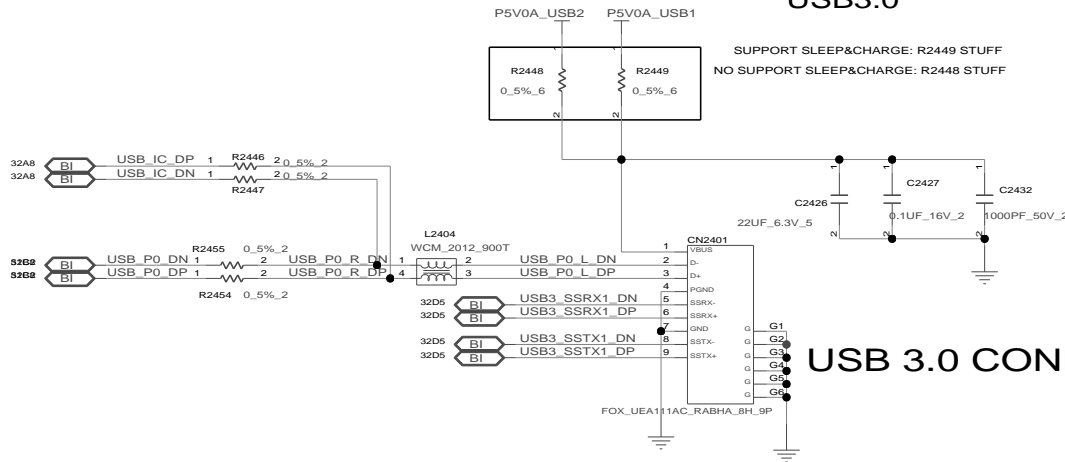
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
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CHANGE by XXX DATE 21-OCT-2002 SHEET 31 of 66

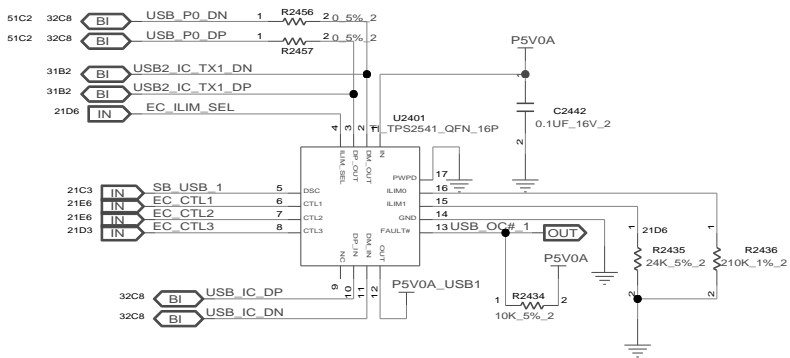
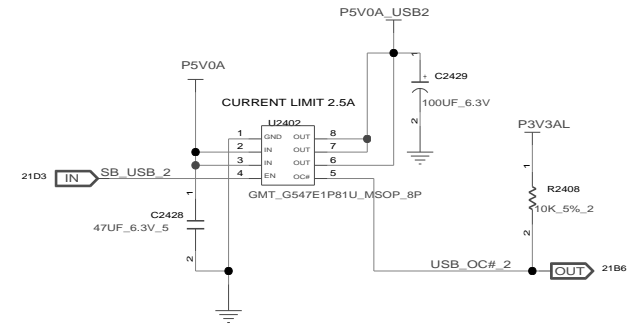


USB3.0

SUPPORT SLEEP&CHARGE: R2449 STUFF
NO SUPPORT SLEEP&CHARGE: R2448 STUFF



USB 3.0 CONNECTOR



CTL1	CTL2	CTL3	Mode
0	0	X	Dedicated Charging Port, Auto-detect
0	1	X	Dedicated Charging Port, BC Specification 1.1 Only
1	0	X	Dedicated Charging Port, Apple Only
1	1	0	Standard Downstream Port, USB 2.0 Mode
1	1	1	Charging Downstream Port, BC Specification 1.1

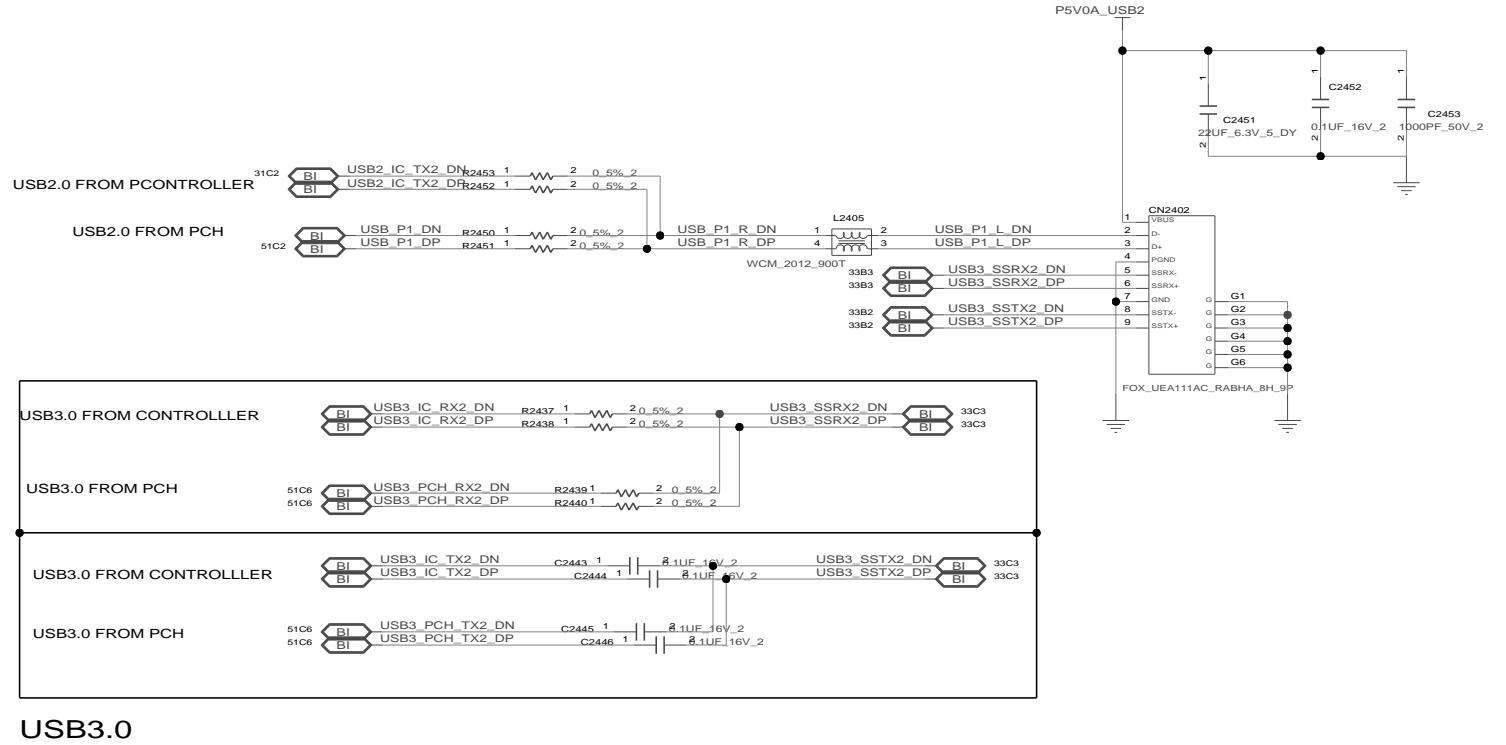
Table 3 - TPS2541 Control Truth Table

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
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USB 3.0 CONNECTOR

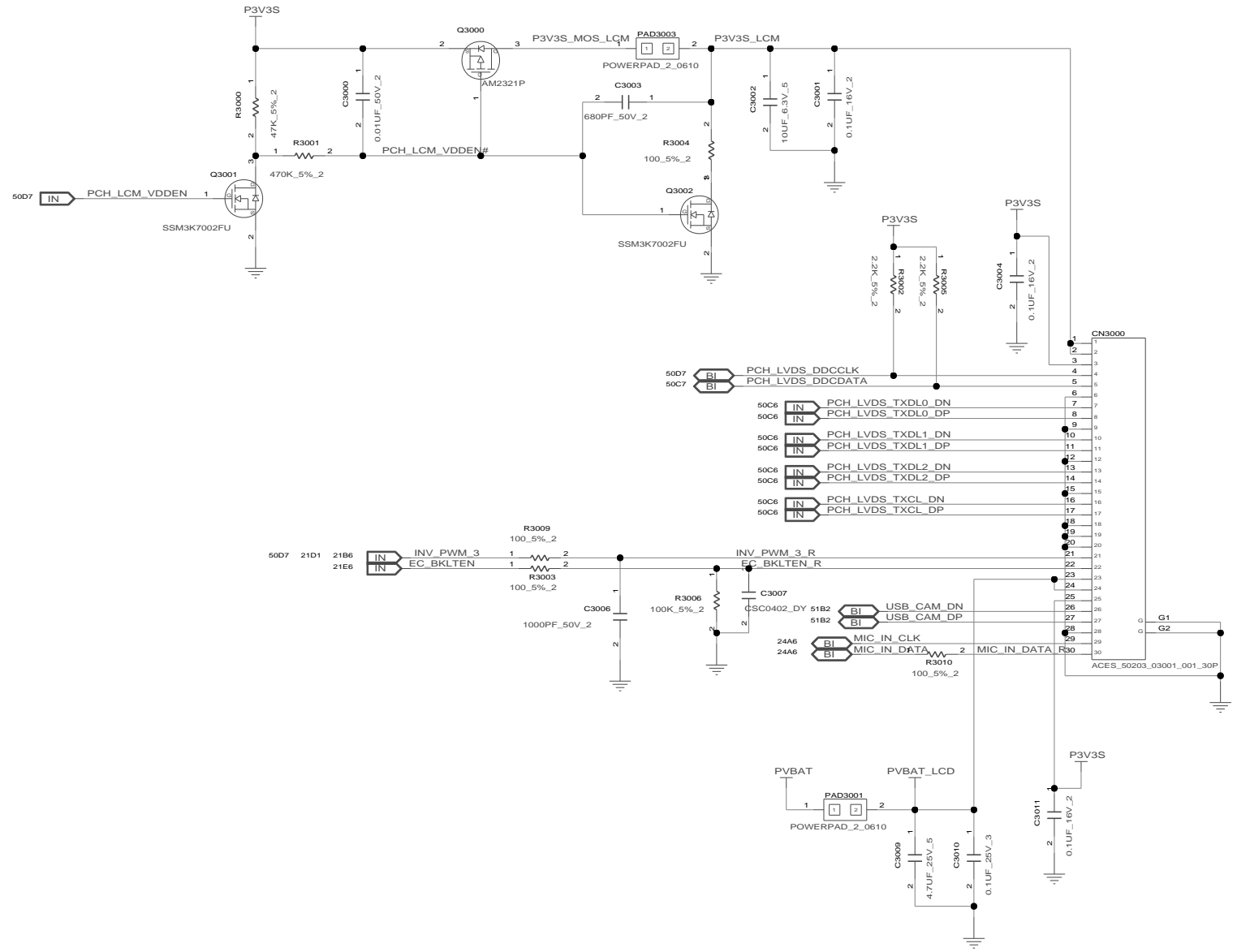


INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
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REFERENCE 3000-3049(LCM)



INVENTEC

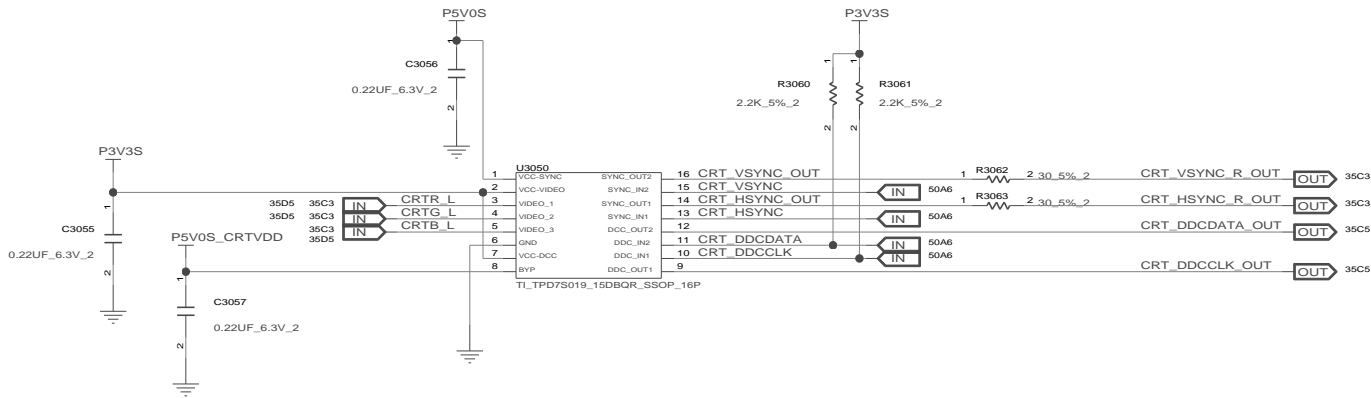
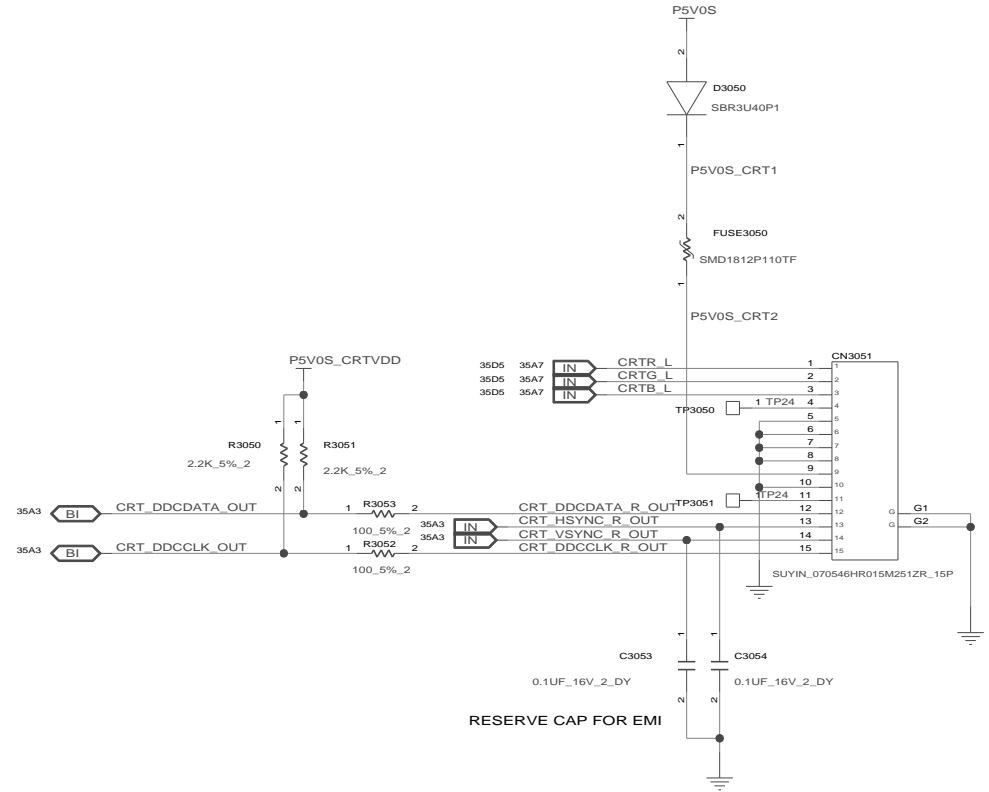
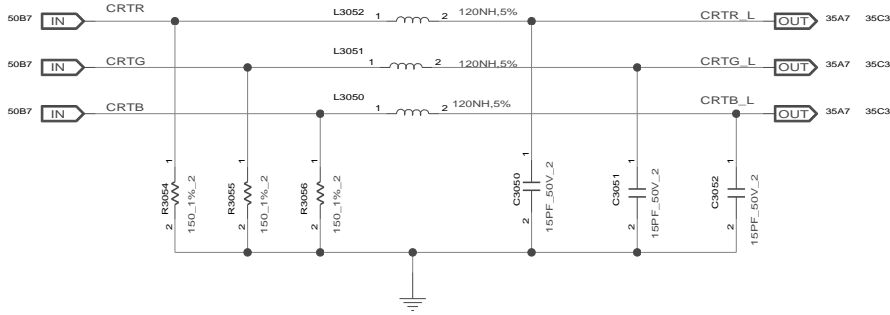
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
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CHANGE by: XXX DATE: 21-OCT-2002

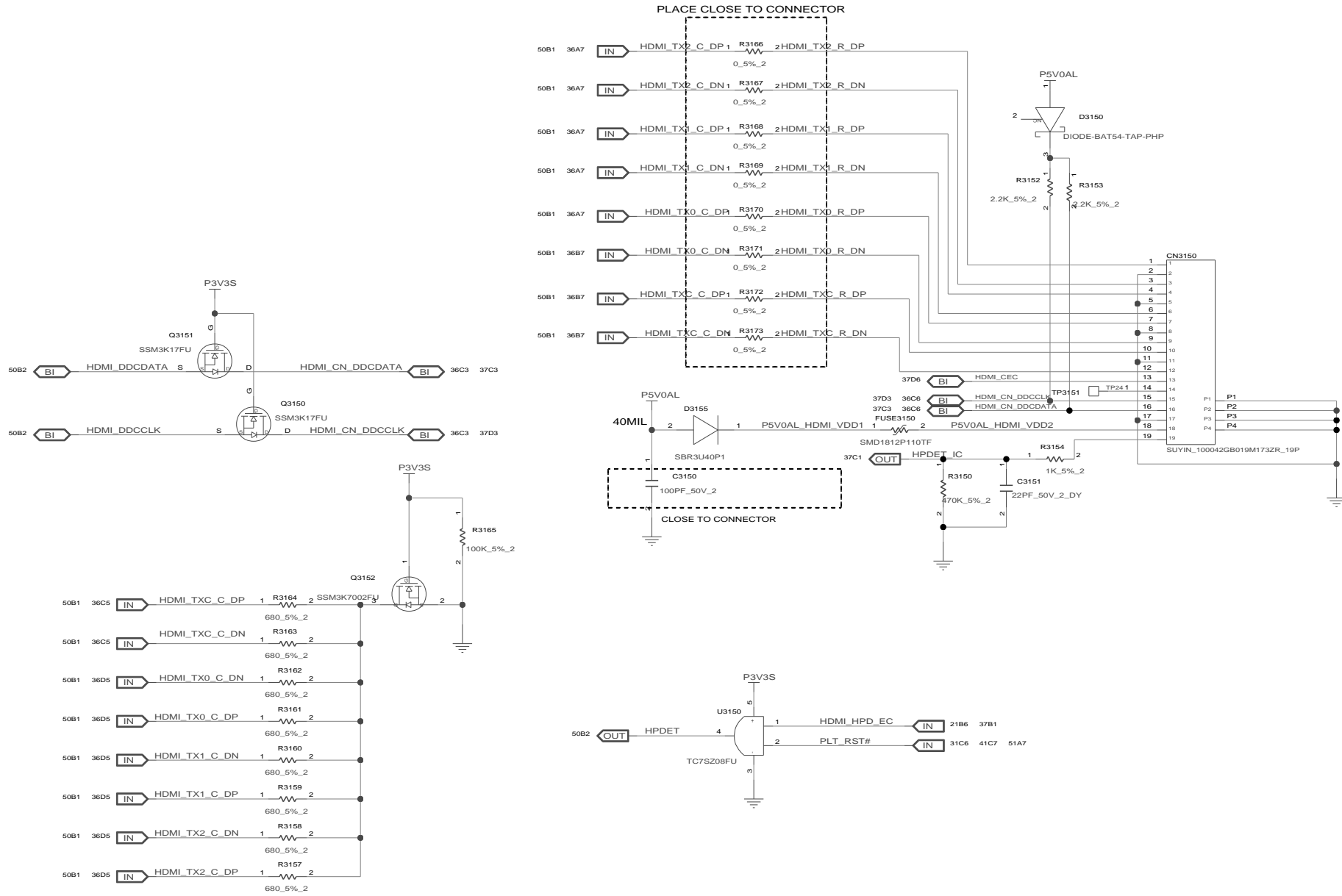
SHEET 34 of 66

REFERENCE 3050-3099(CRT)

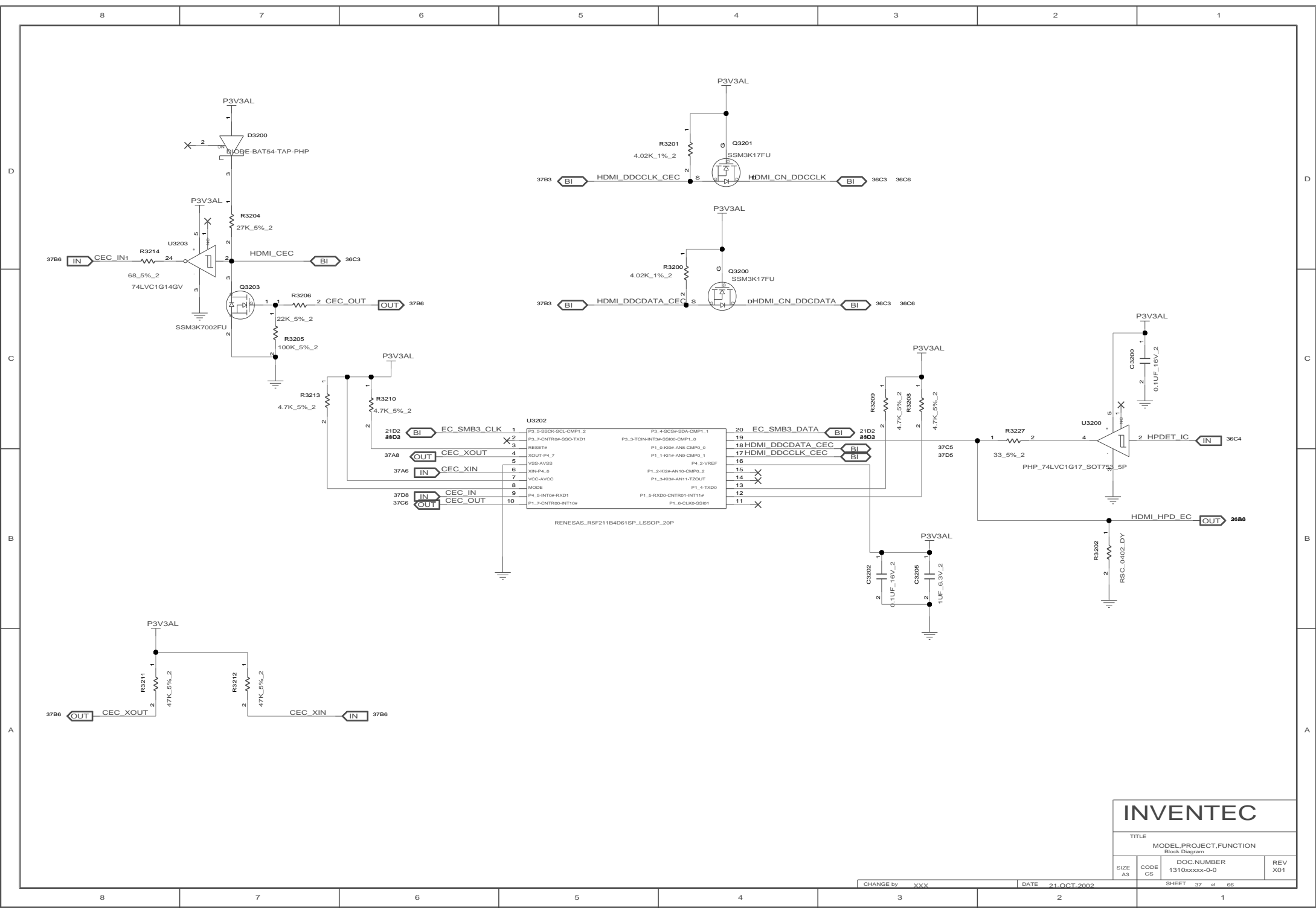


INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 35 of 66

REFERENCE 3150~3199(HDMI)



INVENTEC			
TITLE MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 36 of 66



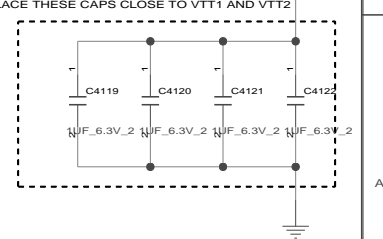
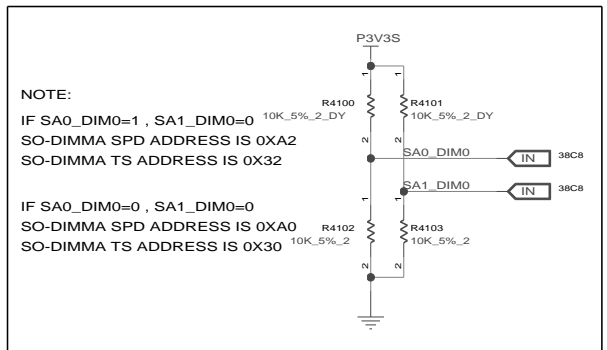
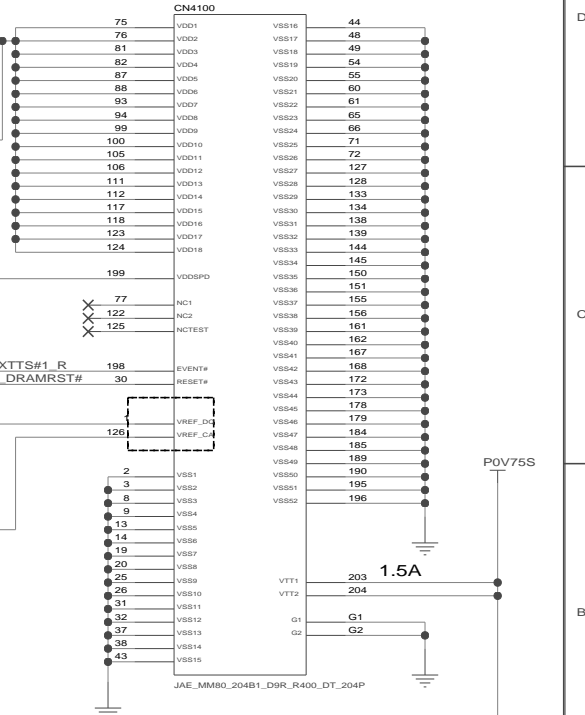
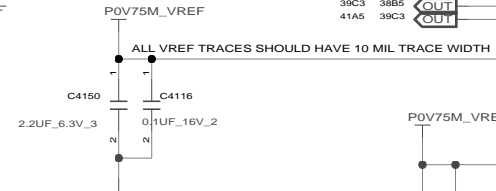
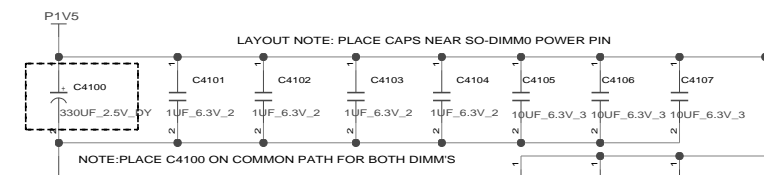
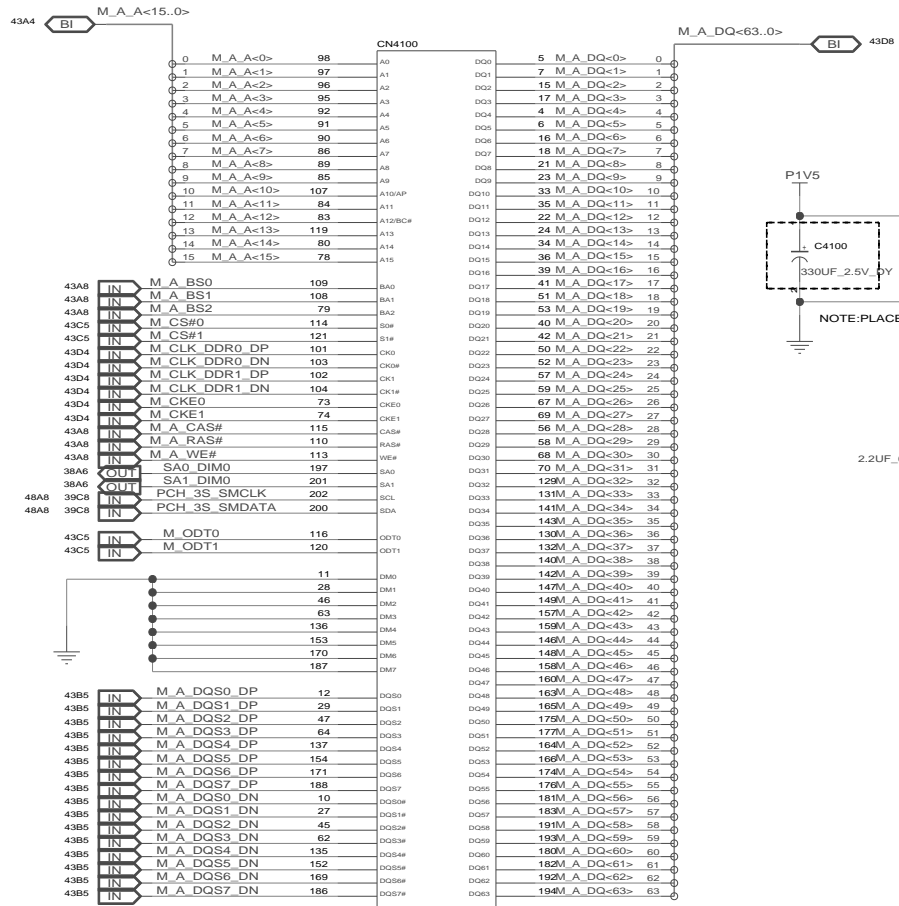
INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
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CHA

REFERENCE 4100~4299(DDR)



INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 38 of 66

CHB

D

D

C

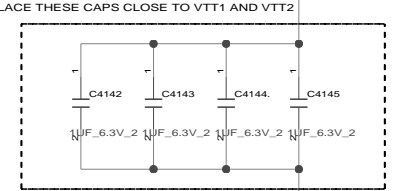
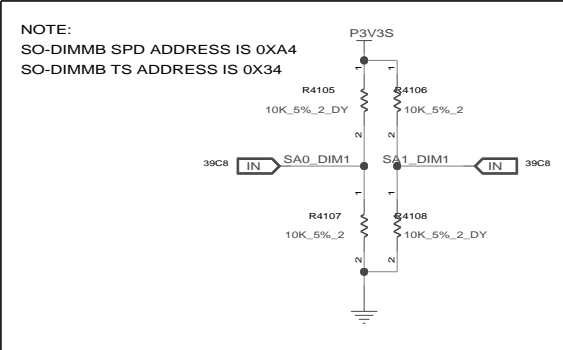
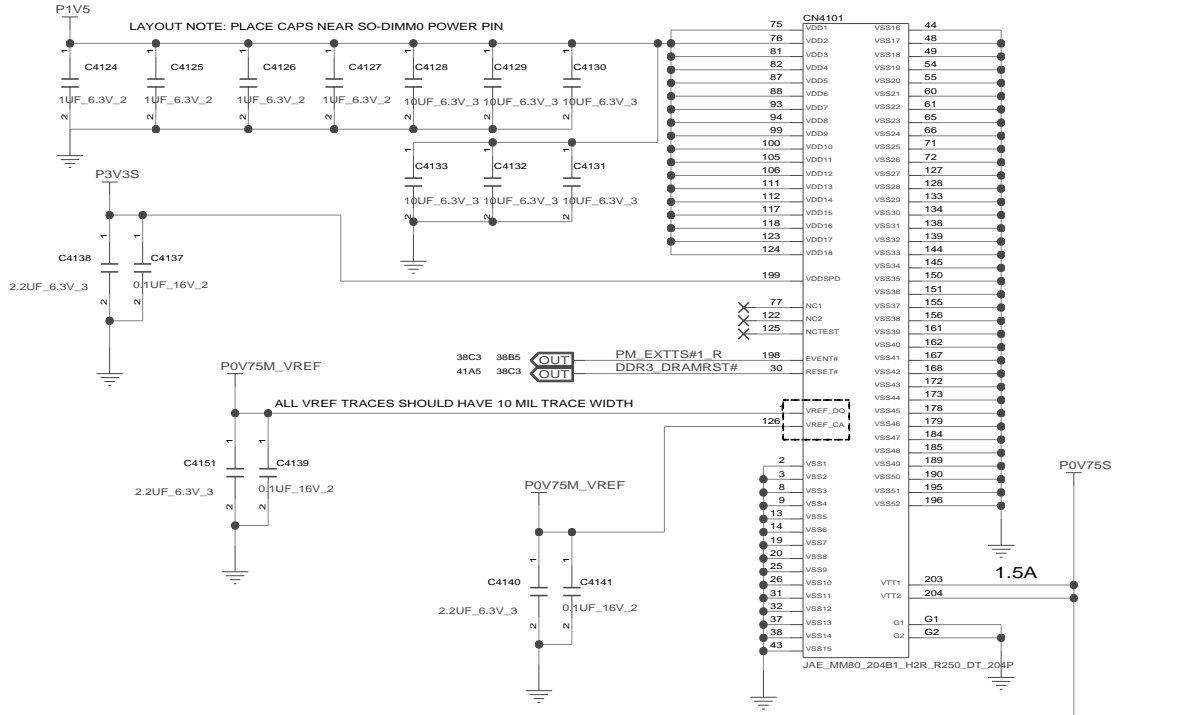
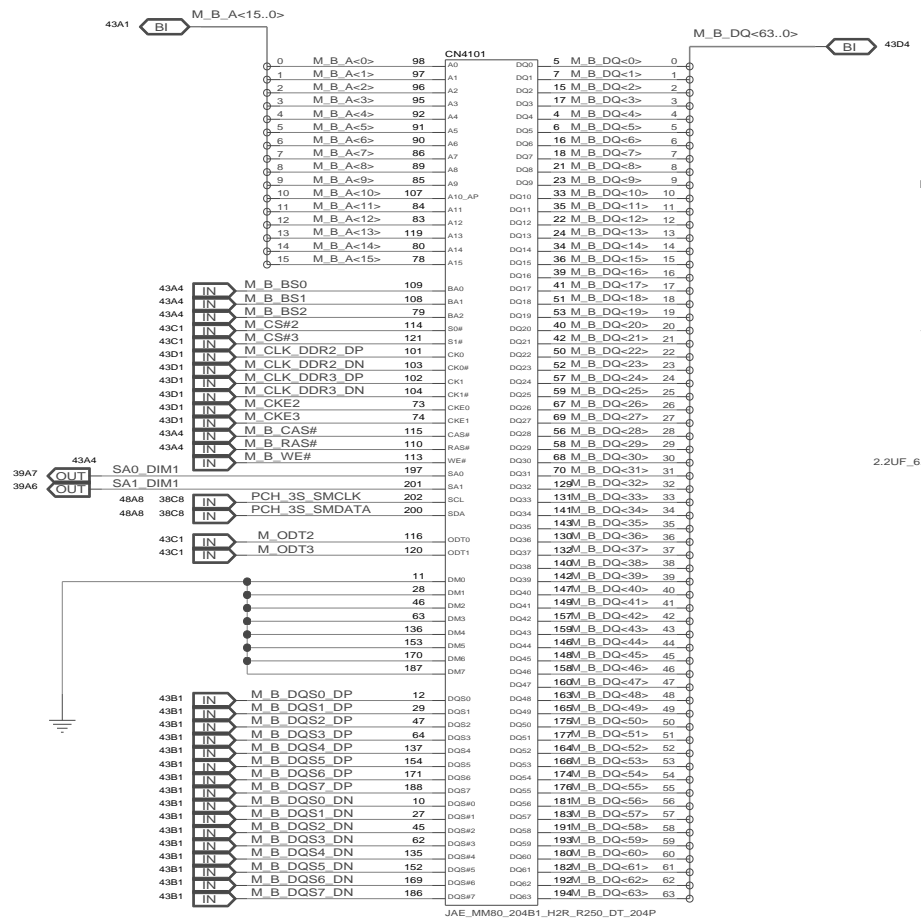
C

B

B

A

A

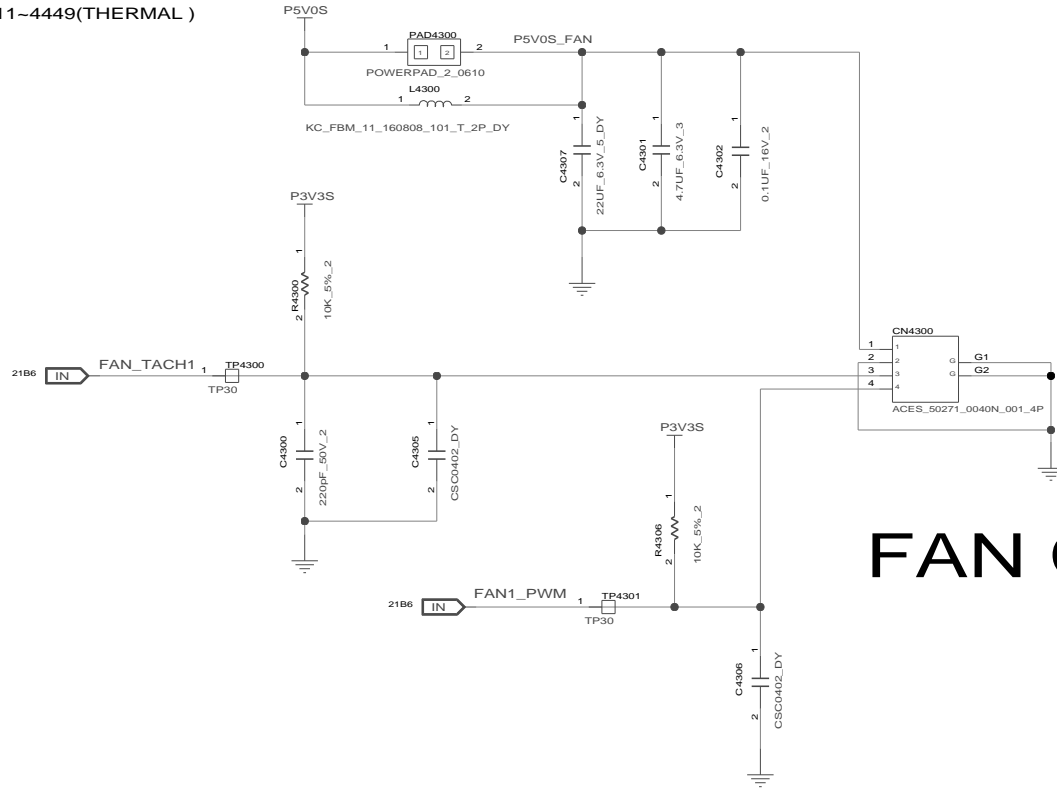


INVENTEC

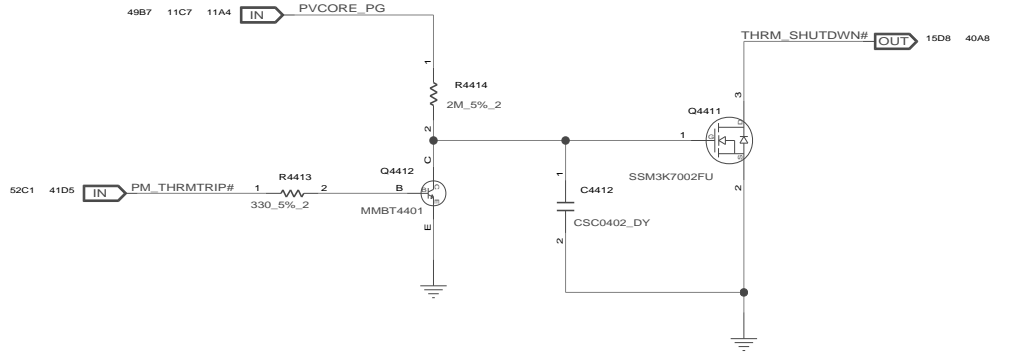
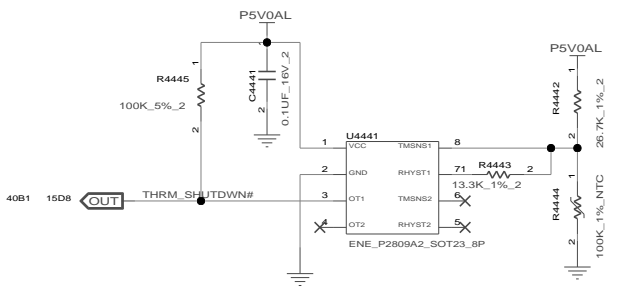
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
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REFERENCE 4300~4349(FAN)
 REFERENCE 4411~4449(THERMAL)



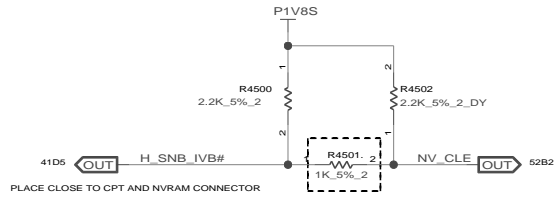
FAN CN



INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET		40 of 66	

REFERENCE 4500-4699(CPU)

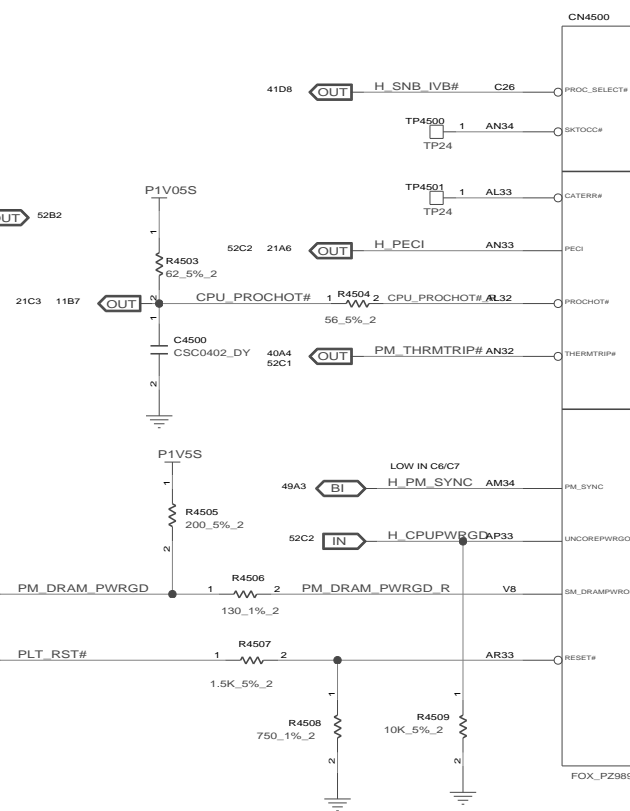


PROCESS STRAP SETTING

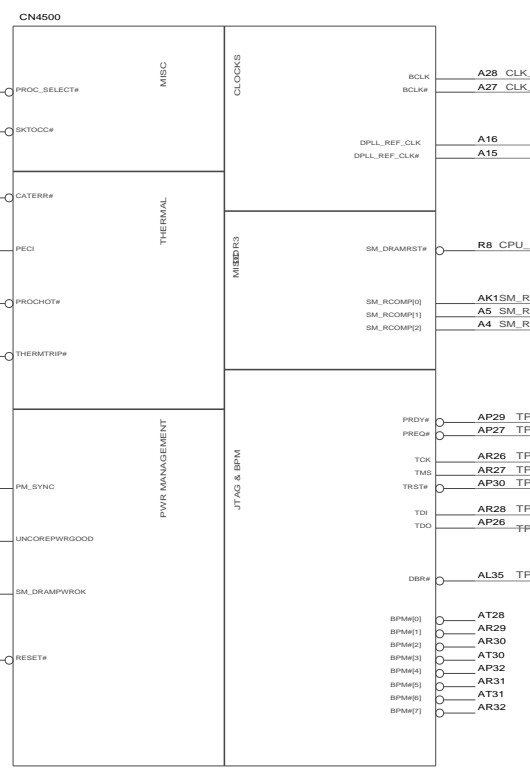
SANDY BRIDGE ONLY	STUFF R4502
SANDY BRIDGE/IVY BRIDGE	STUFF R4500/R4501

DMI&FDI TERMINATIONVOLTAGE

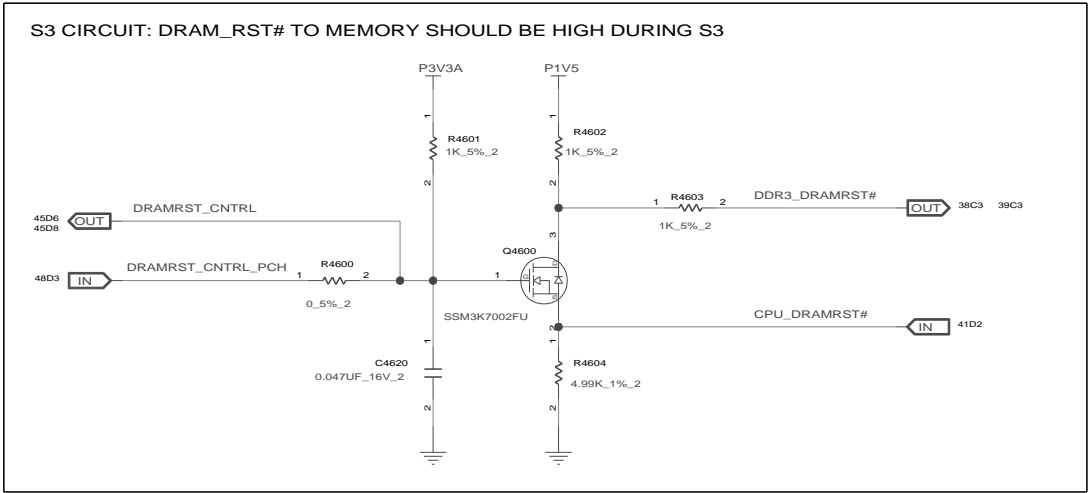
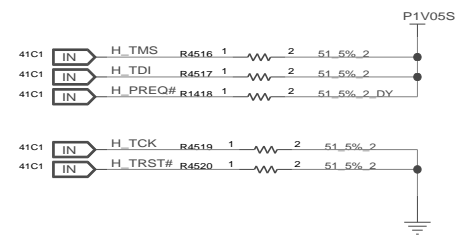
NV_CLE	SET TOVSS WHEN LOW(DEFAULT) SET TOVCC WHEN HIGH
--------	--



FOX_PZ98927_3641_41F_HURONRIVER_989P_CHIEFRIVER



CAD NOTE: ALL DDR_COMP SIGNALS SHOULD BE ROUTED SUCH TAHT
 - MAX LENGTH = 500 MILS
 - TRACE WIDTH = 15MILS AND
 - MB TRACE IMPEDANCE < 68 MOHMS
 (WORST CASE RESISTANCE)



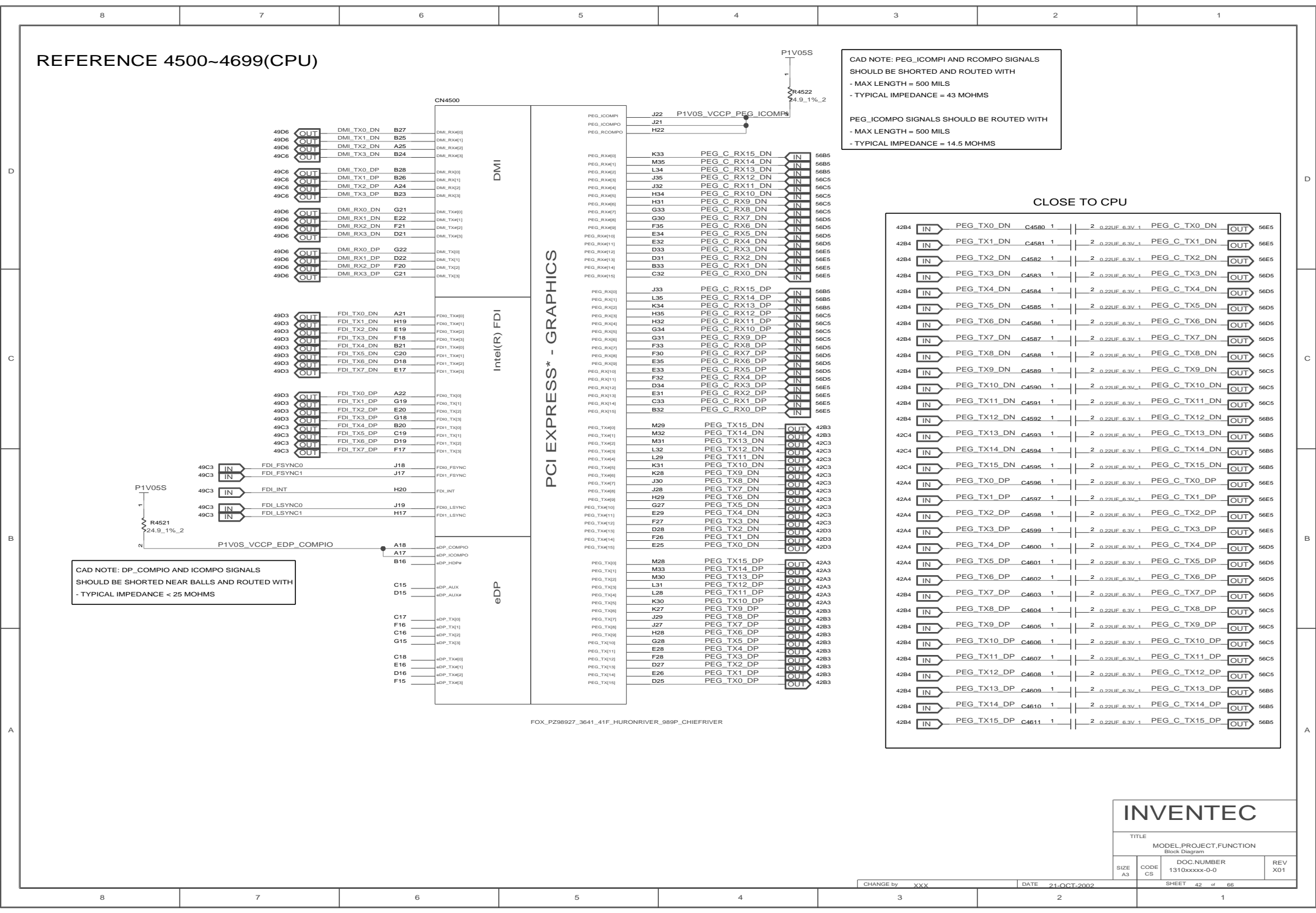
INVENTEC

TITLE Block Diagram			
MODEL,PROJECT,FUNCTION 1310xxxx-0-0		REV X01	
SIZE A3	CODE CS	DATE 21-OCT-2002	SHEET 41 of 66

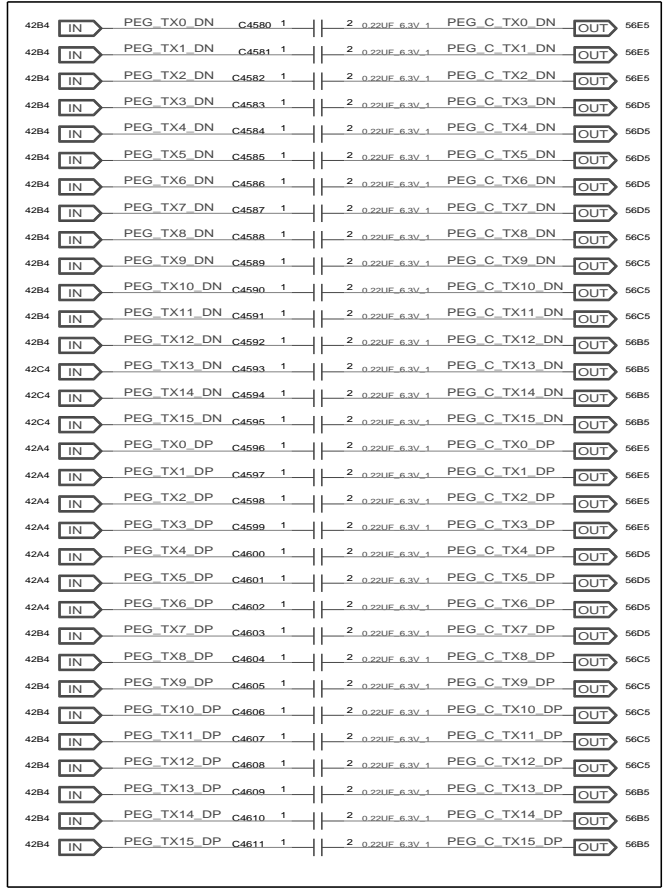
REFERENCE 4500~4699(CPU)

CAD NOTE: PEG_ICOMPI AND RCOMPO SIGNALS SHOULD BE SHORTED AND ROUTED WITH
 - MAX LENGTH = 500 MILS
 - TYPICAL IMPEDANCE = 43 MOHMS

PEG_ICOMPO SIGNALS SHOULD BE ROUTED WITH
 - MAX LENGTH = 500 MILS
 - TYPICAL IMPEDANCE = 14.5 MOHMS



CLOSE TO CPU



FOX_PZ98927_3641_41F_HURONRIVER_989P_CHIEFRIVER

INVENTEC

TITLE
 MODEL,PROJECT,FUNCTION
 Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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REFERENCE 4500~4699(CPU)

SOCKET,CPU,989P,TIN,3.0MM,STR,SMD,TR

CN4500

38D5 BI M A DQ<63.0>

- 0 M A DQ<0> C5 SA,DQ0
- 1 M A DQ<1> D5 SA,DQ1
- 2 M A DQ<2> D3 SA,DQ2
- 3 M A DQ<3> D2 SA,DQ3
- 4 M A DQ<4> D6 SA,DQ4
- 5 M A DQ<5> C6 SA,DQ5
- 6 M A DQ<6> C2 SA,DQ6
- 7 M A DQ<7> C3 SA,DQ7
- 8 M A DQ<8> F10 SA,DQ8
- 9 M A DQ<9> F8 SA,DQ9
- 10 M A DQ<10> G10 SA,DQ10
- 11 M A DQ<11> G9 SA,DQ11
- 12 M A DQ<12> F9 SA,DQ12
- 13 M A DQ<13> F7 SA,DQ13
- 14 M A DQ<14> G8 SA,DQ14
- 15 M A DQ<15> G7 SA,DQ15
- 16 M A DQ<16> K4 SA,DQ16
- 17 M A DQ<17> K5 SA,DQ17
- 18 M A DQ<18> K1 SA,DQ18
- 19 M A DQ<19> J1 SA,DQ19
- 20 M A DQ<20> J5 SA,DQ20
- 21 M A DQ<21> J4 SA,DQ21
- 22 M A DQ<22> J2 SA,DQ22
- 23 M A DQ<23> K2 SA,DQ23
- 24 M A DQ<24> M8 SA,DQ24
- 25 M A DQ<25> N10 SA,DQ25
- 26 M A DQ<26> N8 SA,DQ26
- 27 M A DQ<27> N7 SA,DQ27
- 28 M A DQ<28> M10 SA,DQ28
- 29 M A DQ<29> M9 SA,DQ29
- 30 M A DQ<30> N9 SA,DQ30
- 31 M A DQ<31> M7 SA,DQ31
- 32 M A DQ<32> AG6 SA,DQ32
- 33 M A DQ<33> AG5 SA,DQ33
- 34 M A DQ<34> AK6 SA,DQ34
- 35 M A DQ<35> AK5 SA,DQ35
- 36 M A DQ<36> AH5 SA,DQ36
- 37 M A DQ<37> AH6 SA,DQ37
- 38 M A DQ<38> AJ5 SA,DQ38
- 39 M A DQ<39> AJ6 SA,DQ39
- 40 M A DQ<40> AJ8 SA,DQ40
- 41 M A DQ<41> AK8 SA,DQ41
- 42 M A DQ<42> AJ9 SA,DQ42
- 43 M A DQ<43> AK9 SA,DQ43
- 44 M A DQ<44> AH8 SA,DQ44
- 45 M A DQ<45> AH9 SA,DQ45
- 46 M A DQ<46> AL9 SA,DQ46
- 47 M A DQ<47> AL8 SA,DQ47
- 48 M A DQ<48> AP11 SA,DQ48
- 49 M A DQ<49> AN11 SA,DQ49
- 50 M A DQ<50> AL12 SA,DQ50
- 51 M A DQ<51> AM12 SA,DQ51
- 52 M A DQ<52> AM11 SA,DQ52
- 53 M A DQ<53> AL11 SA,DQ53
- 54 M A DQ<54> AP12 SA,DQ54
- 55 M A DQ<55> AN12 SA,DQ55
- 56 M A DQ<56> AJ14 SA,DQ56
- 57 M A DQ<57> AH14 SA,DQ57
- 58 M A DQ<58> AL15 SA,DQ58
- 59 M A DQ<59> AK15 SA,DQ59
- 60 M A DQ<60> AL14 SA,DQ60
- 61 M A DQ<61> AK14 SA,DQ61
- 62 M A DQ<62> AJ15 SA,DQ62
- 63 M A DQ<63> AH15 SA,DQ63

- 38D8 M A BS0 AE10 SA,BS0
- 38D8 M A BS1 AP10 SA,BS1
- 38D8 M A BS2 V6 SA,BS2

- 38C8 M A CAS# AEB SA,CAS#
- 38C8 M A RAS# AD9 SA,RAS#
- 38C8 M A WE# AF9 SA,WE#

DDR SYSTEM MEMORY A

- SA,CLK0 AB6 M CLK DDR0 DP OUT 38C8
- SA,CLK0 SA,CLK0 AB6 M CLK DDR0 DN OUT 38C8
- SA,CKE0 V9 M_CKE0 OUT 38C8
- SA,CLK1 AA5 M CLK DDR1 DP OUT 38C8
- SA,CLK1 SA,CLK1 AA5 M CLK DDR1 DN OUT 38C8
- SA,CKE1 V10 M_CKE1 OUT 38C8
- RSVD_TF11 AB4
- RSVD_TF11 AA4
- RSVD_TF11 W9
- RSVD_TF11 AB3
- RSVD_TF11 AA3
- RSVD_TF11 W10
- SA,CB#0 AK3 M_CS#0 OUT 38D8
- SA,CB#1 AL3 M_CS#1 OUT 38C8
- RSVD_TF17 AG1
- RSVD_TF18 AH1
- SA,ODT0 AH3 M_ODT0 OUT 38C8
- SA,ODT1 AG3 M_ODT1 OUT 38C8
- RSVD_TF19 AG2
- RSVD_TF19 AH2
- SA,DQS0 C4 M A DQS0 DN OUT 38B8
- SA,DQS1 G6 M A DQS1 DN OUT 38B8
- SA,DQS2 J3 M A DQS2 DN OUT 38B8
- SA,DQS3 M6 M A DQS3 DN OUT 38B8
- SA,DQS4 AL6 M A DQS4 DN OUT 38B8
- SA,DQS5 AM6 M A DQS5 DN OUT 38B8
- SA,DQS6 AR12M A DQS6 DN OUT 38B8
- SA,DQS7 AM19M A DQS7 DN OUT 38B8
- SA,DQS8 D4 M A DQS0 DP OUT 38B8
- SA,DQS9 F6 M A DQS1 DP OUT 38B8
- SA,DQS10 K3 M A DQS2 DP OUT 38B8
- SA,DQS11 N6 M A DQS3 DP OUT 38B8
- SA,DQS12 AL5 M A DQS4 DP OUT 38B8
- SA,DQS13 AM9 M A DQS5 DP OUT 38B8
- SA,DQS14 AR11M A DQS6 DP OUT 38B8
- SA,DQS15 AM14M A DQS7 DP OUT 38B8
- SA,MA0 AD10 M A A<0> 0
- SA,MA1 W1 M A A<1> 1
- SA,MA2 W2 M A A<2> 2
- SA,MA3 W7 M A A<3> 3
- SA,MA4 V3 M A A<4> 4
- SA,MA5 V2 M A A<5> 5
- SA,MA6 W3 M A A<6> 6
- SA,MA7 W6 M A A<7> 7
- SA,MA8 V1 M A A<8> 8
- SA,MA9 V5 M A A<9> 9
- SA,MA10 AD8 M A A<10> 10
- SA,MA11 V4 M A A<11> 11
- SA,MA12 W4 M A A<12> 12
- SA,MA13 AF8 M A A<13> 13
- SA,MA14 V5 M A A<14> 14
- SA,MA15 V7 M A A<15> 15

M A A<15.0> OUT 38D8

- 38D8 M B BS0 AA9 SA,BS0
- 38D8 M B BS1 AA7 SA,BS1
- 38C8 M B BS2 R6 SA,BS2

- 38C8 M B CAS#AA10 SA,CAS#
- 38C8 M B RAS# AB8 SA,RAS#
- 38C8 M B WE# AB9 SA,WE#

38D5 BI M B DQ<63.0>

- 0 M B DQ<0> C9 SA,DQ0
- 1 M B DQ<1> A7 SA,DQ1
- 2 M B DQ<2> D10 SA,DQ2
- 3 M B DQ<3> C8 SA,DQ3
- 4 M B DQ<4> A9 SA,DQ4
- 5 M B DQ<5> A8 SA,DQ5
- 6 M B DQ<6> D9 SA,DQ6
- 7 M B DQ<7> D8 SA,DQ7
- 8 M B DQ<8> G4 SA,DQ8
- 9 M B DQ<9> F4 SA,DQ9
- 10 M B DQ<10> F1 SA,DQ10
- 11 M B DQ<11> G1 SA,DQ11
- 12 M B DQ<12> G5 SA,DQ12
- 13 M B DQ<13> F5 SA,DQ13
- 14 M B DQ<14> F2 SA,DQ14
- 15 M B DQ<15> G2 SA,DQ15
- 16 M B DQ<16> J7 SA,DQ16
- 17 M B DQ<17> J8 SA,DQ17
- 18 M B DQ<18> K10 SA,DQ18
- 19 M B DQ<19> K9 SA,DQ19
- 20 M B DQ<20> J9 SA,DQ20
- 21 M B DQ<21> J10 SA,DQ21
- 22 M B DQ<22> K8 SA,DQ22
- 23 M B DQ<23> K7 SA,DQ23
- 24 M B DQ<24> M5 SA,DQ24
- 25 M B DQ<25> N4 SA,DQ25
- 26 M B DQ<26> N2 SA,DQ26
- 27 M B DQ<27> N1 SA,DQ27
- 28 M B DQ<28> M4 SA,DQ28
- 29 M B DQ<29> N5 SA,DQ29
- 30 M B DQ<30> M2 SA,DQ30
- 31 M B DQ<31> M1 SA,DQ31
- 32 M B DQ<32> M5 SA,DQ32
- 33 M B DQ<33> M6 SA,DQ33
- 34 M B DQ<34> AR3 SA,DQ34
- 35 M B DQ<35> AP3 SA,DQ35
- 36 M B DQ<36> AN3 SA,DQ36
- 37 M B DQ<37> AN2 SA,DQ37
- 38 M B DQ<38> SA11 SA,DQ38
- 39 M B DQ<39> AP2 SA,DQ39
- 40 M B DQ<40> AP5 SA,DQ40
- 41 M B DQ<41> AN9 SA,DQ41
- 42 M B DQ<42> AT5 SA,DQ42
- 43 M B DQ<43> AT6 SA,DQ43
- 44 M B DQ<44> AP6 SA,DQ44
- 45 M B DQ<45> AN8 SA,DQ45
- 46 M B DQ<46> AR6 SA,DQ46
- 47 M B DQ<47> AR5 SA,DQ47
- 48 M B DQ<48> AR9 SA,DQ48
- 49 M B DQ<49> AH11 SA,DQ49
- 50 M B DQ<50> AT8 SA,DQ50
- 51 M B DQ<51> AT9 SA,DQ51
- 52 M B DQ<52> AH11 SA,DQ52
- 53 M B DQ<53> AR8 SA,DQ53
- 54 M B DQ<54> AH12 SA,DQ54
- 55 M B DQ<55> AH12 SA,DQ55
- 56 M B DQ<56> AH11 SA,DQ56
- 57 M B DQ<57> SA14 SA,DQ57
- 58 M B DQ<58> AR14 SA,DQ58
- 59 M B DQ<59> AP14 SA,DQ59
- 60 M B DQ<60> AT12 SA,DQ60
- 61 M B DQ<61> AN15 SA,DQ61
- 62 M B DQ<62> SA15 SA,DQ62
- 63 M B DQ<63> AT15 SA,DQ63

CN4500

DDR SYSTEM MEMORY B

- SB,CLK0 AE2 M CLK DDR2 DP OUT 39C8
- SB,CLK0 SB,CLK0 AD2 M CLK DDR2 DN OUT 39C8
- SB,CKE0 R9 M_CKE2 OUT 39C8
- SB,CLK1 AE1 M CLK DDR3 DP OUT 39C8
- SB,CLK1 SB,CLK1 AD1 M CLK DDR3 DN OUT 39C8
- SB,CKE1 R10 M_CKE3 OUT 39C8
- RSVD_TF11 AB2
- RSVD_TF12 AA2
- RSVD_TF13 T9
- RSVD_TF14 AA1
- RSVD_TF15 AB1
- RSVD_TF16 T10
- SB,CB#0 AD3 M_CS#2 OUT 39C8
- SB,CB#1 AE3 M_CS#3 OUT 39C8
- RSVD_TF17 AD6
- RSVD_TF18 AE6
- SB,ODT0 AE4 M_ODT2 OUT 39C8
- SB,ODT1 AD4 M_ODT3 OUT 39C8
- RSVD_TF19 AD5
- RSVD_TF20 AE5
- SB,DQS0 D7 M B DQS0 DN OUT 39B8
- SB,DQS1 F3 M B DQS1 DP OUT 39B8
- SB,DQS2 K6 M B DQS2 DN OUT 39B8
- SB,DQS3 N3 M B DQS3 DN OUT 39B8
- SB,DQS4 AN5 M B DQS4 DN OUT 39B8
- SB,DQS5 AP9 M B DQS5 DN OUT 39B8
- SB,DQS6 AK12 M B DQS6 DN OUT 39B8
- SB,DQS7 AP15 M B DQS7 DN OUT 39B8
- SB,DQS8 C7 M B DQS0 DP OUT 39B8
- SB,DQS9 G3 M B DQS1 DP OUT 39B8
- SB,DQS10 J6 M B DQS2 DP OUT 39B8
- SB,DQS11 M3 M B DQS3 DP OUT 39B8
- SB,DQS12 AN6 M B DQS4 DP OUT 39B8
- SB,DQS13 AP8 M B DQS5 DP OUT 39B8
- SB,DQS14 AK11 M B DQS6 DP OUT 39B8
- SB,DQS15 AP14 M B DQS7 DP OUT 39B8
- SB,MA0 AA8 M B A<0> 0
- SB,MA1 T7 M B A<1> 1
- SB,MA2 R7 M B A<2> 2
- SB,MA3 T6 M B A<3> 3
- SB,MA4 T2 M B A<4> 4
- SB,MA5 T4 M B A<5> 5
- SB,MA6 T3 M B A<6> 6
- SB,MA7 R2 M B A<7> 7
- SB,MA8 T5 M B A<8> 8
- SB,MA9 R3 M B A<9> 9
- SB,MA10 AB7 M B A<10> 10
- SB,MA11 R1 M B A<11> 11
- SB,MA12 T1 M B A<12> 12
- SB,MA13 AB10 M B A<13> 13
- SB,MA14 R5 M B A<14> 14
- SB,MA15 R4 M B A<15> 15

M B A<15.0> OUT

FOX_PZ98927_3641_41F_HURONRIVER_989P_CHIEFRIVER

FOX_PZ98927_3641_41F_HURONRIVER_989P_CHIEFRIVER

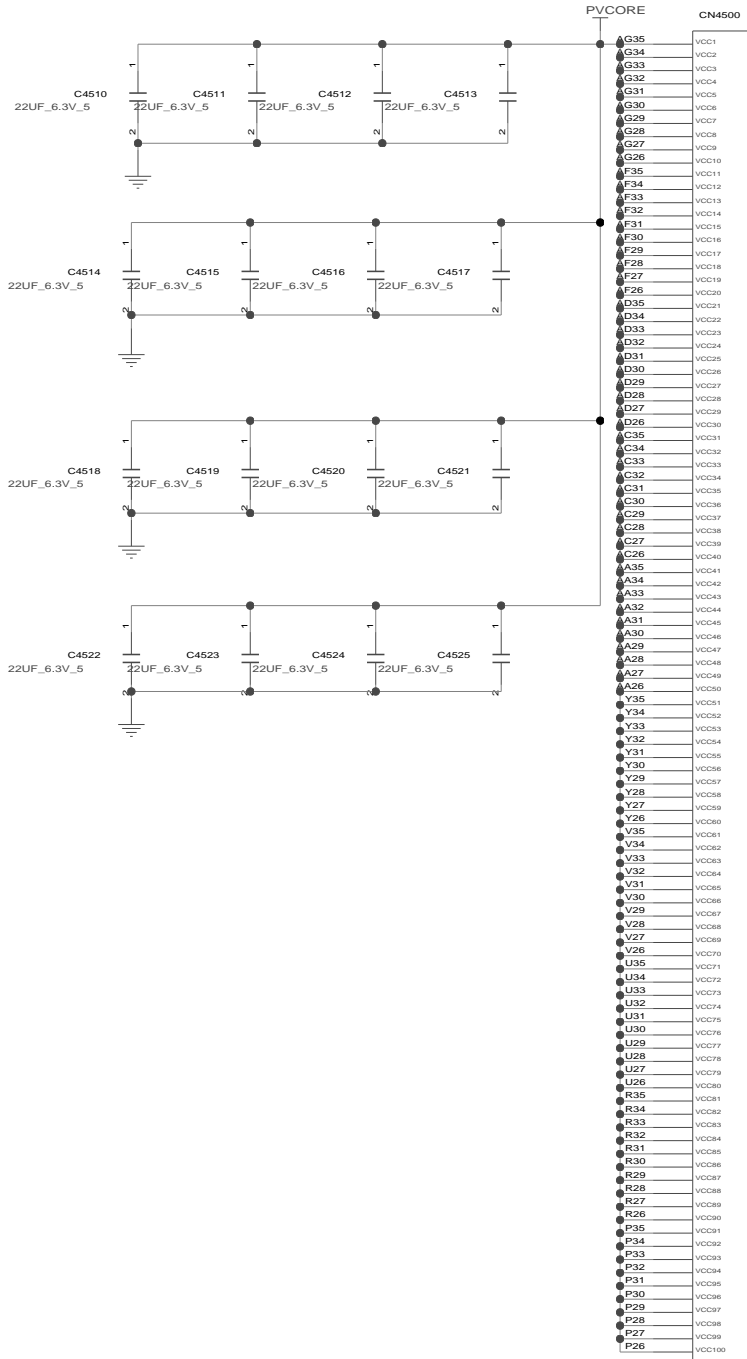
INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
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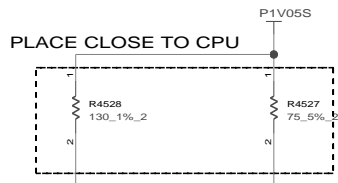
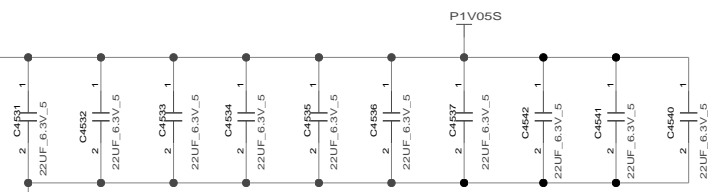
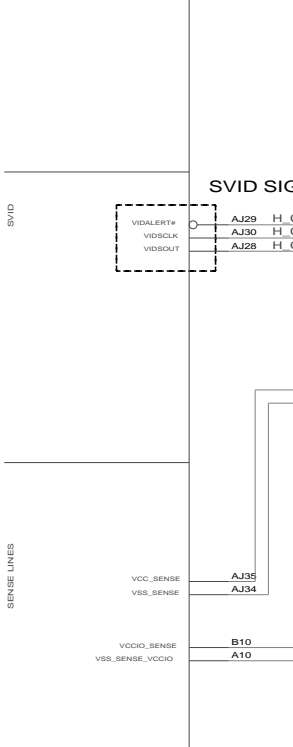
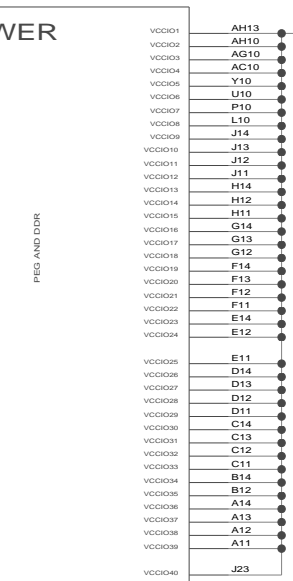
CHANGE by XXX DATE 21-OCT-2002 SHEET 43 of 66

REFERENCE 4500~4699(CPU)

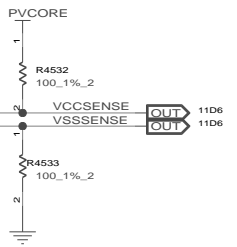


POWER

CORE SUPPLY



SVID SIGNAL TO VR

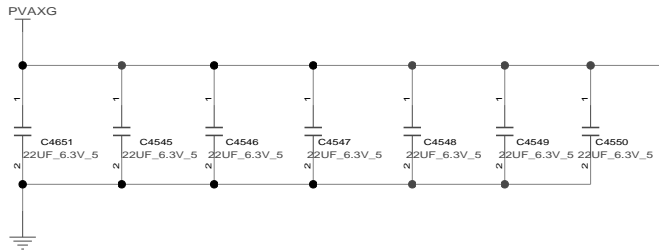


INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

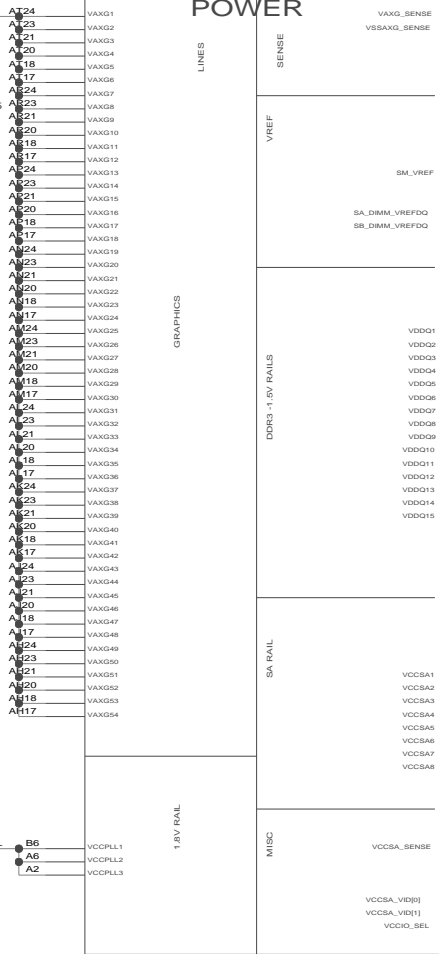
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
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PROCESSOR DRIVEN VREF PATH WAS STUFFED BY DEFAULT:
ROUTE WITH MIN. TRACE WIDTH OF 10 MILS



CN4500
FOX_PZ98927_3641_41F_HURONRIVER_989P_CHIEFRIVER

POWER



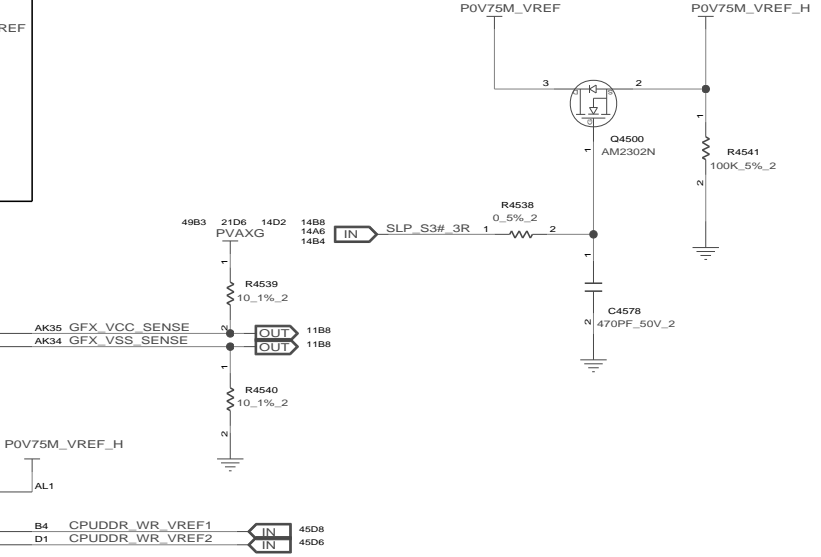
LINES

GRAPHICS

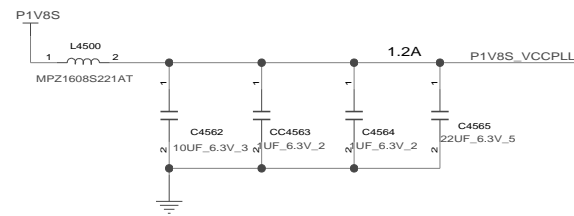
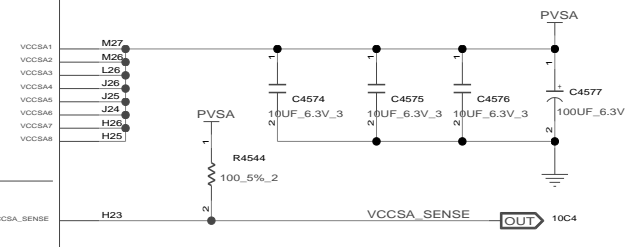
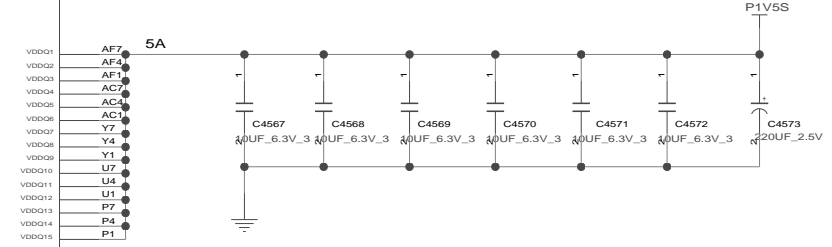
SA RAIL

MISC

1.8V RAIL

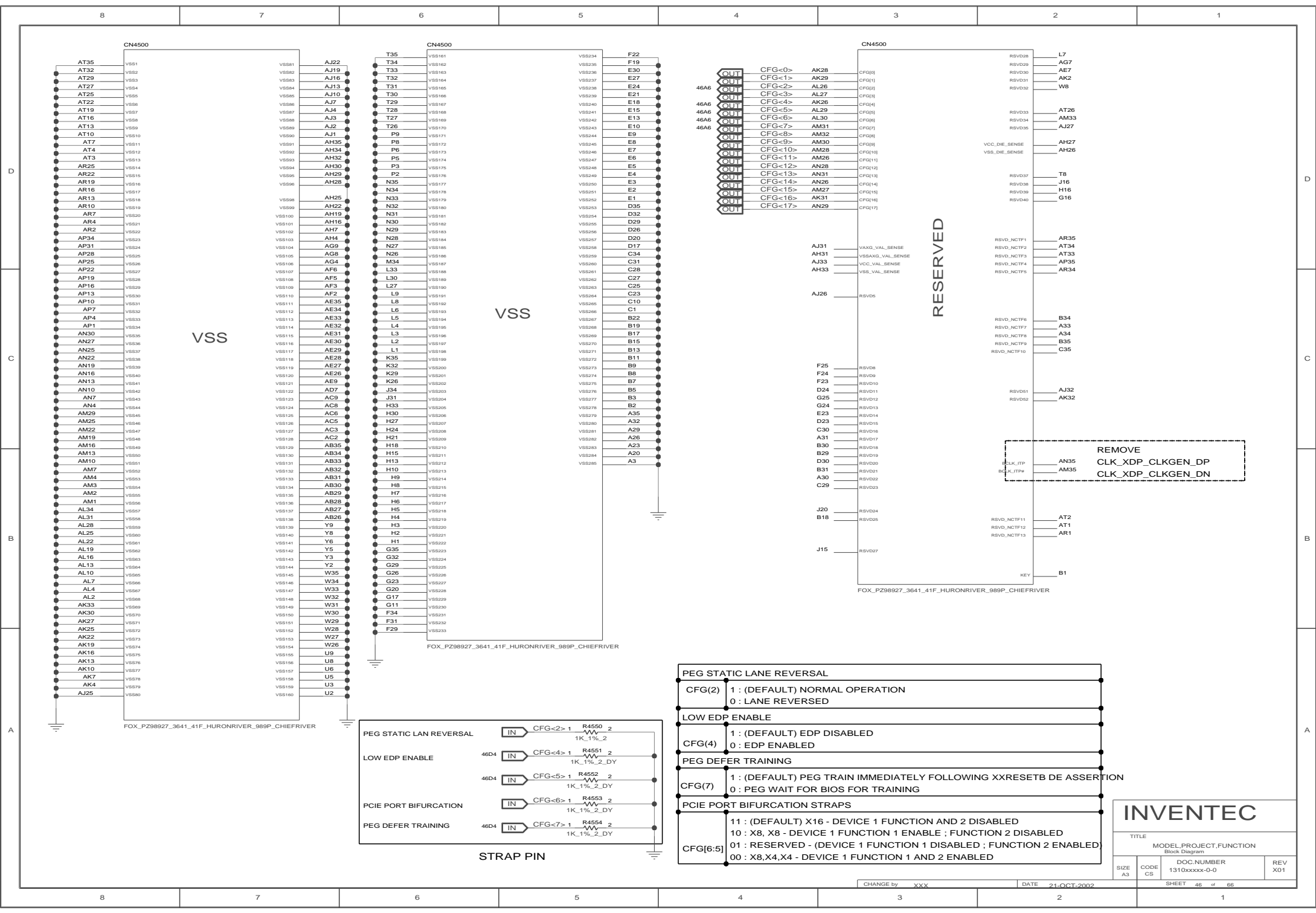


NOTE : DDR_WR_VREF SHOULD HAVE 20/20 MIL WHEREVER POSSIBLE



INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
SHEET		45 of 66	



CN4500

AT35	V5S1	AJ22	V5S191
AT32	V5S2	AJ19	V5S188
AT29	V5S3	AJ16	V5S185
AT27	V5S4	AJ13	V5S182
AT25	V5S5	AJ10	V5S179
AT22	V5S6	AJ7	V5S176
AT19	V5S7	AJ4	V5S173
AT16	V5S8	AJ3	V5S172
AT13	V5S9	AJ2	V5S171
AT10	V5S10	AJ1	V5S170
AT7	V5S11	AH35	V5S167
AT4	V5S12	AH34	V5S166
AT3	V5S13	AH32	V5S165
AR25	V5S14	AH30	V5S164
AR22	V5S15	AH29	V5S163
AR19	V5S16	AH28	V5S162
AR16	V5S17	AH25	V5S159
AR13	V5S18	AH22	V5S156
AR10	V5S19	AH19	V5S153
AR7	V5S20	AH16	V5S150
AR4	V5S21	AH7	V5S147
AR2	V5S22	AH4	V5S144
AP34	V5S23	AG9	V5S141
AP31	V5S24	AG8	V5S140
AP28	V5S25	AG4	V5S137
AP25	V5S26	AF6	V5S134
AP22	V5S27	AF5	V5S133
AP19	V5S28	AF3	V5S130
AP16	V5S29	AF2	V5S129
AP13	V5S30	AE35	V5S126
AP10	V5S31	AE34	V5S125
AP7	V5S32	AE33	V5S124
AP4	V5S33	AE32	V5S123
AP1	V5S34	AE31	V5S122
AN30	V5S35	AE30	V5S121
AN27	V5S36	AE29	V5S120
AN25	V5S37	AE28	V5S119
AN22	V5S38	AE27	V5S118
AN19	V5S39	AE26	V5S117
AN16	V5S40	AE9	V5S114
AN13	V5S41	AD7	V5S111
AN10	V5S42	AC9	V5S108
AN7	V5S43	AC8	V5S107
AN4	V5S44	AC6	V5S104
AM29	V5S45	AC5	V5S103
AM25	V5S46	AC3	V5S100
AM22	V5S47	AB35	V5S97
AM19	V5S48	AB34	V5S96
AM16	V5S49	AB33	V5S95
AM13	V5S50	AB32	V5S94
AM10	V5S51	AB31	V5S93
AM7	V5S52	AB30	V5S92
AM4	V5S53	AB29	V5S91
AM3	V5S54	AB28	V5S90
AM2	V5S55	AB27	V5S89
AM1	V5S56	AB26	V5S88
AL34	V5S57	Y9	V5S85
AL31	V5S58	Y8	V5S84
AL28	V5S59	Y6	V5S81
AL25	V5S60	Y5	V5S80
AL22	V5S61	Y3	V5S77
AL19	V5S62	Y2	V5S76
AL16	V5S63	W35	V5S73
AL13	V5S64	W34	V5S72
AL10	V5S65	W33	V5S71
AL7	V5S66	W32	V5S70
AL4	V5S67	W31	V5S69
AL2	V5S68	W30	V5S68
AK33	V5S69	W29	V5S67
AK30	V5S70	W28	V5S66
AK27	V5S71	W27	V5S65
AK25	V5S72	W26	V5S64
AK22	V5S73	W25	V5S63
AK19	V5S74	U9	V5S60
AK16	V5S75	U8	V5S59
AK13	V5S76	U6	V5S57
AK10	V5S77	U5	V5S56
AK7	V5S78	U3	V5S54
AK4	V5S79	U2	V5S53
AJ25	V5S80		

CN4500

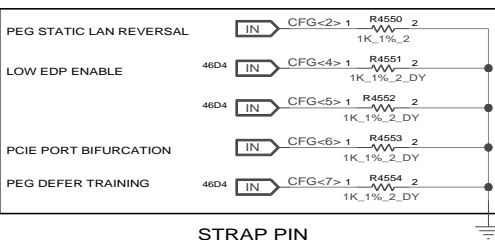
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T34	V5S162	F19	V5S233
T33	V5S163	E30	V5S232
T32	V5S164	E27	V5S231
T31	V5S165	E24	V5S230
T30	V5S166	E21	V5S229
T29	V5S167	E18	V5S228
T28	V5S168	E15	V5S227
T27	V5S169	E13	V5S226
T26	V5S170	E10	V5S225
P9	V5S171	E9	V5S224
P8	V5S172	E8	V5S223
P5	V5S173	E7	V5S222
P5	V5S174	E6	V5S221
P3	V5S175	E5	V5S220
P2	V5S176	E4	V5S219
N35	V5S177	E3	V5S218
N34	V5S178	E2	V5S217
N33	V5S179	E1	V5S216
N32	V5S180	D35	V5S215
N31	V5S181	D32	V5S214
N30	V5S182	D29	V5S213
N29	V5S183	D26	V5S212
N28	V5S184	D20	V5S209
N27	V5S185	D17	V5S206
N26	V5S186	C34	V5S203
N34	V5S187	C31	V5S200
L33	V5S188	C28	V5S197
L30	V5S189	C27	V5S196
L27	V5S190	C25	V5S193
L9	V5S191	C23	V5S192
LB	V5S192	C10	V5S189
L6	V5S193	C1	V5S186
L5	V5S194	B22	V5S183
L4	V5S195	B19	V5S180
L3	V5S196	B17	V5S177
L2	V5S197	B15	V5S174
L1	V5S198	B13	V5S171
K35	V5S199	B11	V5S168
K32	V5S200	B9	V5S165
K29	V5S201	B8	V5S162
K26	V5S202	B7	V5S159
J34	V5S203	B5	V5S156
J31	V5S204	B3	V5S153
H33	V5S205	B2	V5S150
H30	V5S206	A35	V5S147
H27	V5S207	A32	V5S144
H24	V5S208	A29	V5S141
H21	V5S209	A26	V5S138
H18	V5S210	A23	V5S135
H15	V5S211	A20	V5S132
H13	V5S212	A3	V5S129
H10	V5S213		
H9	V5S214		
H8	V5S215		
H7	V5S216		
H6	V5S217		
H5	V5S218		
H4	V5S219		
H3	V5S220		
H2	V5S221		
H1	V5S222		
G35	V5S223		
G32	V5S224		
G29	V5S225		
G26	V5S226		
G23	V5S227		
G20	V5S228		
G17	V5S229		
G11	V5S230		
F34	V5S231		
F31	V5S232		
F29	V5S233		

CN4500

CFG<0>	AK28	CFG(0)
CFG<1>	AK29	CFG(1)
CFG<2>	AL26	CFG(2)
CFG<3>	AL27	CFG(3)
CFG<4>	AK26	CFG(4)
CFG<5>	AL29	CFG(5)
CFG<6>	AL30	CFG(6)
CFG<7>	AM31	CFG(7)
CFG<8>	AM32	CFG(8)
CFG<9>	AM30	CFG(9)
CFG<10>	AM28	CFG(10)
CFG<11>	AM26	CFG(11)
CFG<12>	AN28	CFG(12)
CFG<13>	AN31	CFG(13)
CFG<14>	AN26	CFG(14)
CFG<15>	AM27	CFG(15)
CFG<16>	AK31	CFG(16)
CFG<17>	AN29	CFG(17)

CN4500

RSVD28	L7
RSVD29	AG7
RSVD30	AE7
RSVD31	AK2
RSVD32	W8
RSVD33	AT26
RSVD34	AM33
RSVD35	AJ27
RSVD37	T8
RSVD38	J16
RSVD39	H16
RSVD40	G16
RSVD_NCTF1	AR35
RSVD_NCTF2	AT34
RSVD_NCTF3	AT33
RSVD_NCTF4	AP35
RSVD_NCTF5	AR34
RSVD_NCTF6	B34
RSVD_NCTF7	A33
RSVD_NCTF8	A34
RSVD_NCTF9	B35
RSVD_NCTF10	C35
RSVD01	AJ32
RSVD02	AK32
RSVD_NCTF11	AT2
RSVD_NCTF12	AT1
RSVD_NCTF13	AR1
KEY	B1



PEG STATIC LANE REVERSAL

CFG(2) 1 : (DEFAULT) NORMAL OPERATION
0 : LANE REVERSED

LOW EDP ENABLE

CFG(4) 1 : (DEFAULT) EDP DISABLED
0 : EDP ENABLED

PEG DEFER TRAINING

CFG(7) 1 : (DEFAULT) PEG TRAIN IMMEDIATELY FOLLOWING XRESSETB DE ASSERTION
0 : PEG WAIT FOR BIOS FOR TRAINING

PCIe PORT BIFURCATION STRAPS

CFG[6:5] 11 : (DEFAULT) X16 - DEVICE 1 FUNCTION 1 AND 2 DISABLED
10 : X8, X8 - DEVICE 1 FUNCTION 1 ENABLE ; FUNCTION 2 DISABLED
01 : RESERVED - (DEVICE 1 FUNCTION 1 DISABLED ; FUNCTION 2 ENABLED)
00 : X8,X4,X4 - DEVICE 1 FUNCTION 1 AND 2 ENABLED

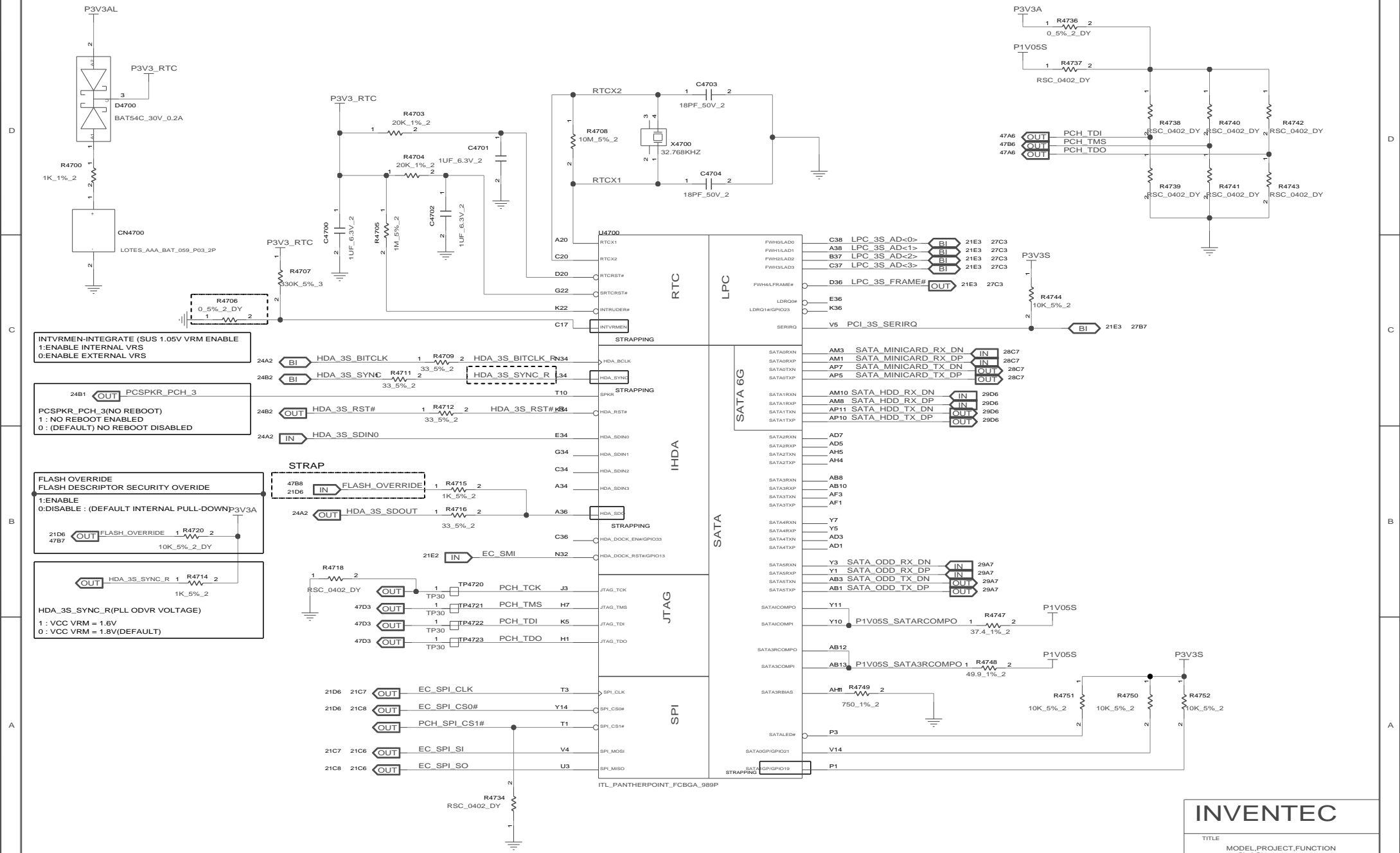
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
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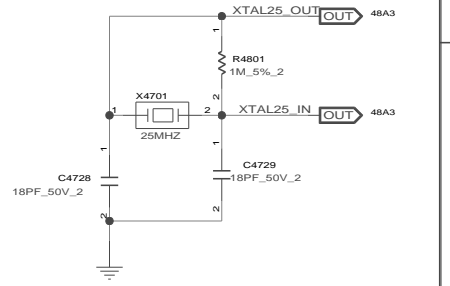
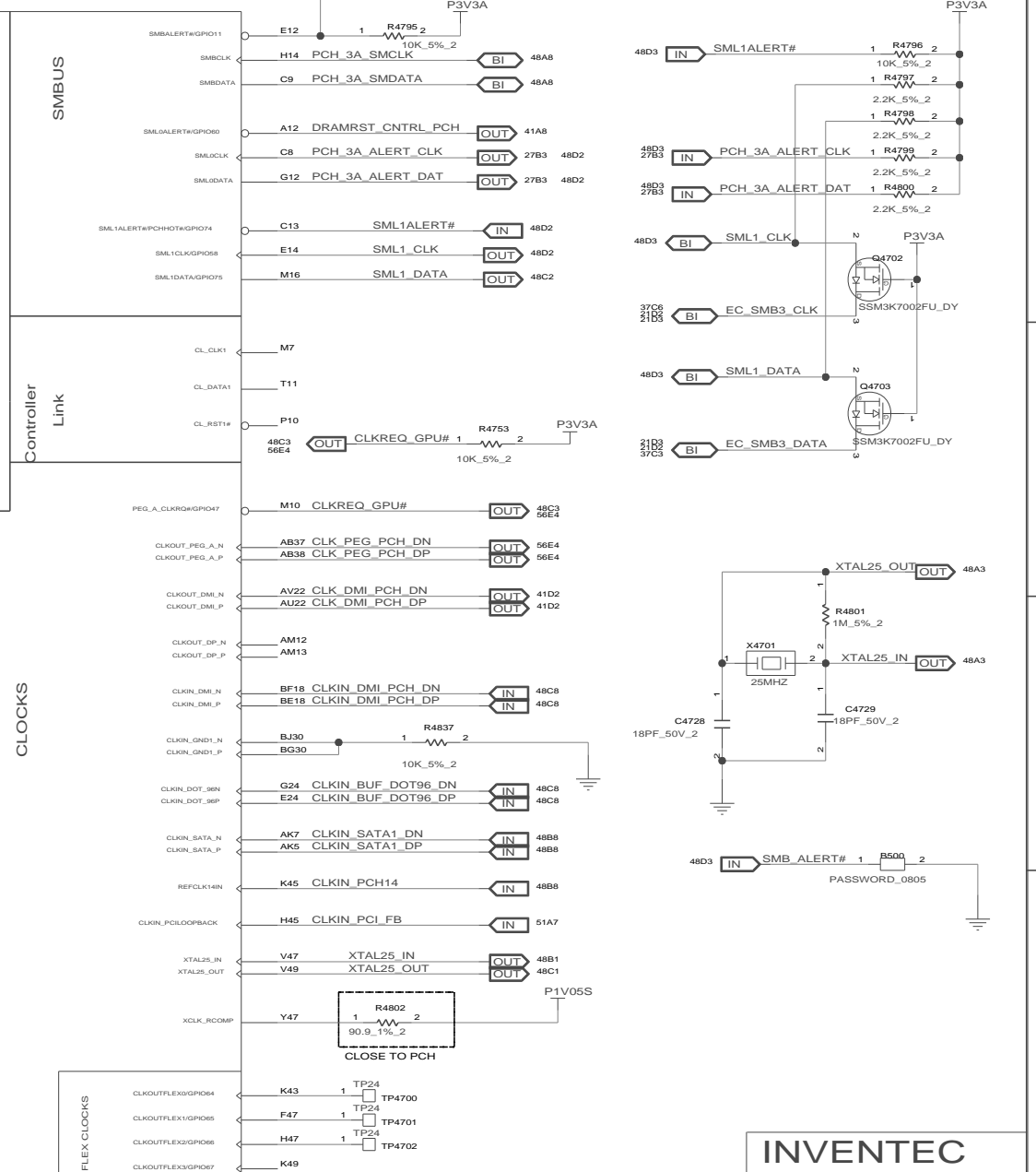
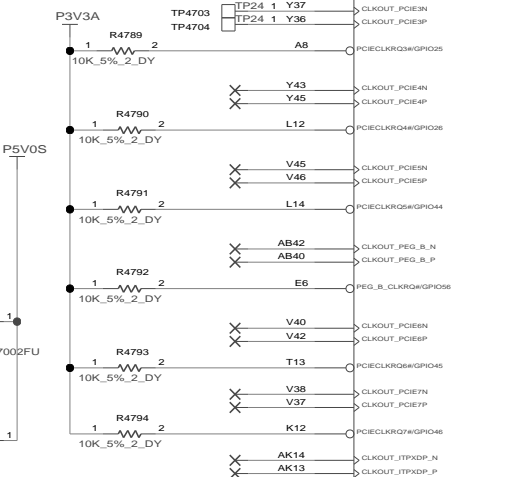
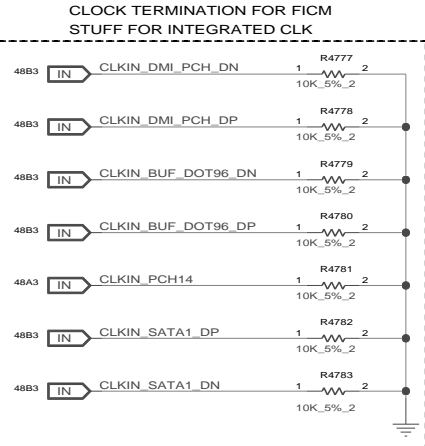
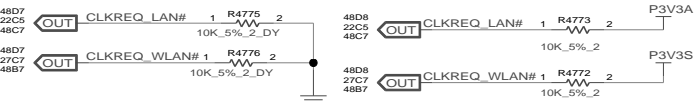
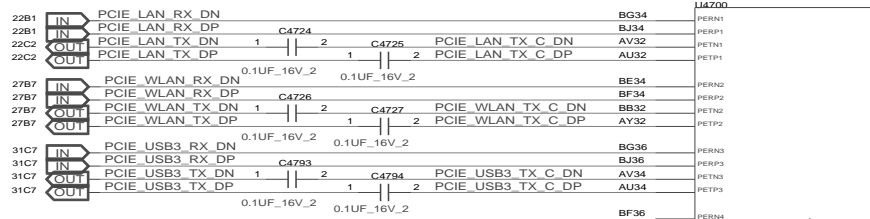
CHANGE by: XXX DATE: 21-OCT-2002 SHEET 46 of 66

REFERENCE 4700~4949(PCH)

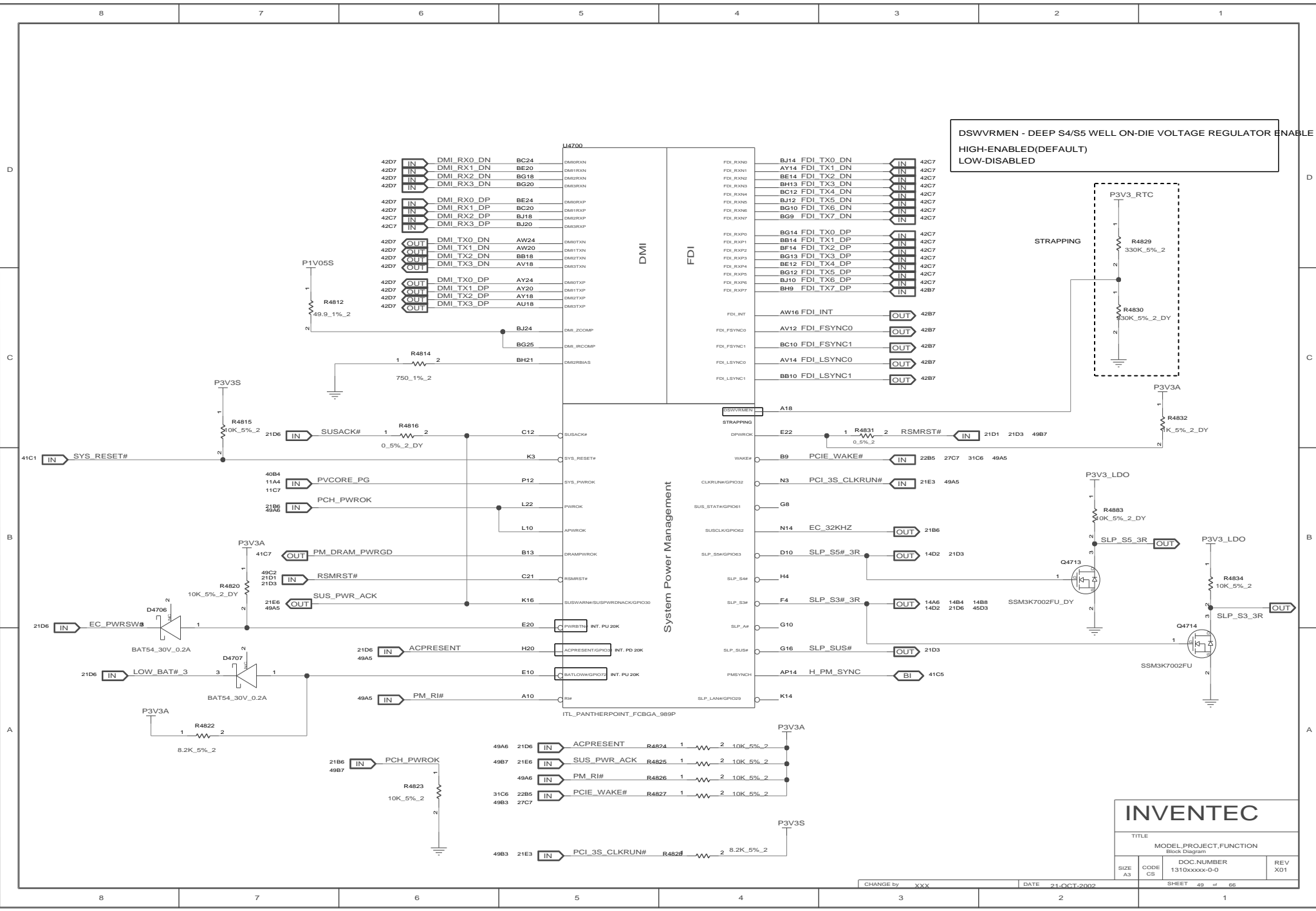


INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 47 of 66

REFERENCE 4700-4949(PCH)



INVENTEC			
TITLE Block Diagram			
MODEL,PROJECT,FUNCTION			
REV X01			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01



DSWVRMEN - DEEP S4/S5 WELL ON-DIE VOLTAGE REGULATOR ENABLE
 HIGH-ENABLED(DEFAULT)
 LOW-DISABLED

INVENTEC			
TITLE			
MODEL_PROJECT.FUNCTION			
Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
CHANGE by xxx		DATE 21-OCT-2002	
SHEET 49 of 66		2	

D

C

B

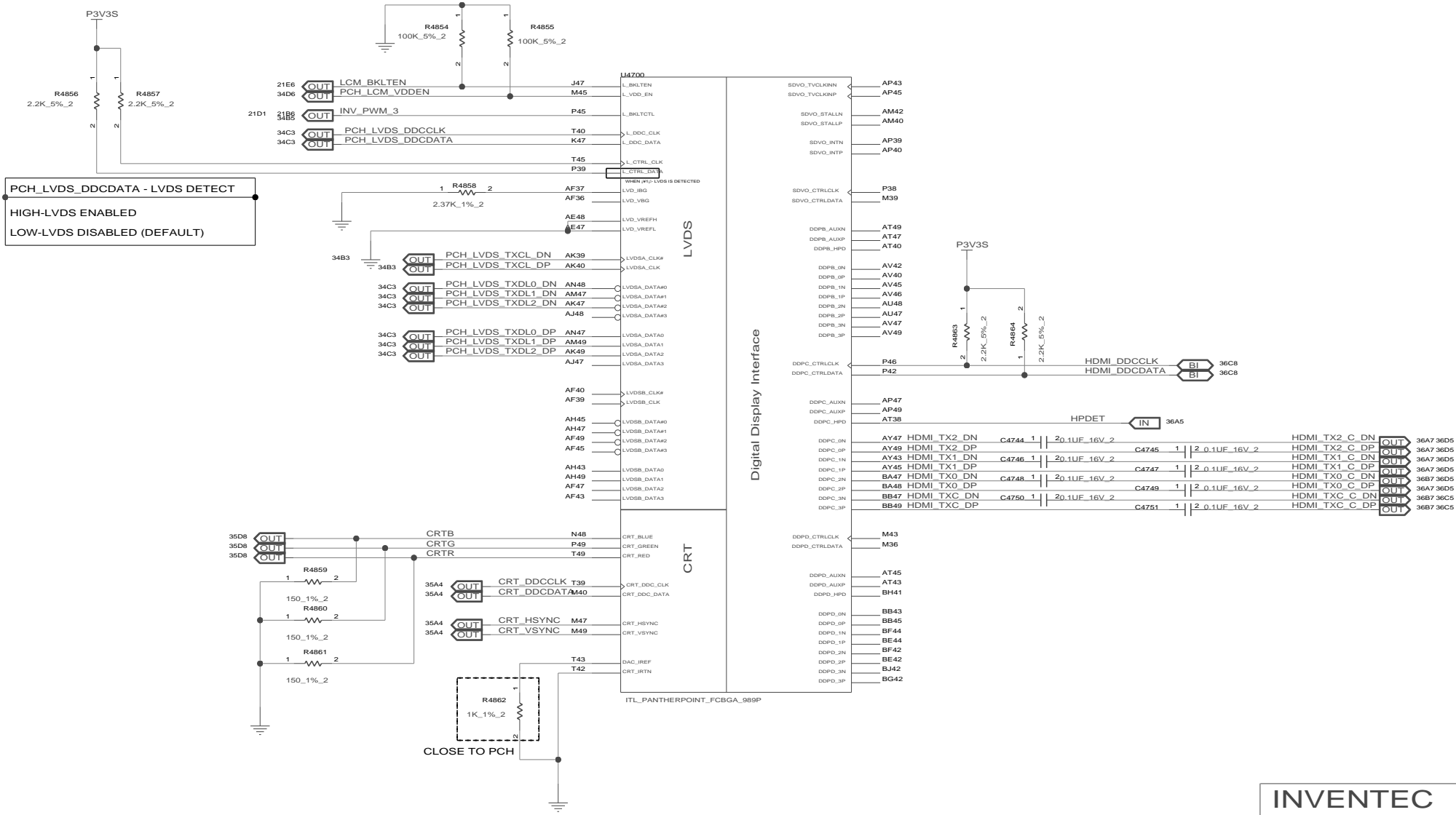
A

D

C

B

A



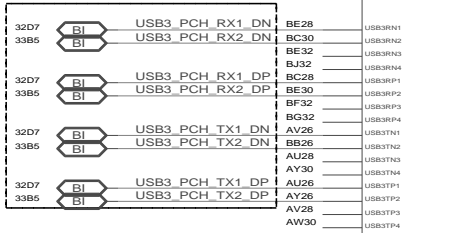
INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE A3	CODE CS	DOC. NUMBER 1310xxxx-0-0	REV X01

REFERENCE 4700-4949(PCH)

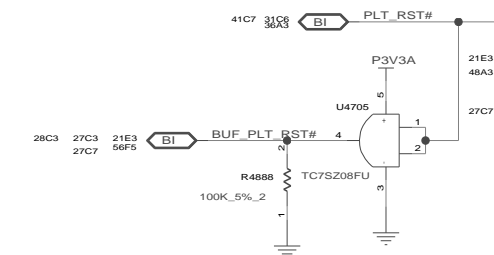
GPIO51 BBS_BIT1	GPIO19 BBS_BIT0	BOOT BIOS DESTINATION
0	1	RESERVED(NAND)
1	0	-----
1	1	SPI (DEFAULT)
0	0	LPC



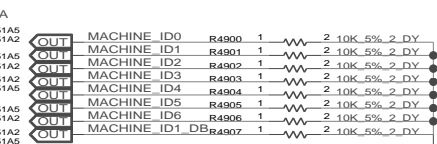
ROUTE WITH 90 OHMS IMPEDANCE
TOTAL LENGTH NO LONGER THAN 11 INCHES



LOW=A16 SWAP OVERRIDE
STP_A16OVR
TOP-BLOCK SWAP OVERRIDE
HIGH=DEFAULT



NOTE:10K_5%(60130B1030ZT)



NOTE:10K_5%(60130B1030ZT)



NVRAM

DEBUG PORT

USB

PCI

P3V3A

NOTE:
USB2.0/3.0 COMBO-USB2.0 PORT 0,1 MAPPED USB3.0 PORT 1,2

P0,P1 RESERVER FOR USB3.0

WLAN

CARD READER

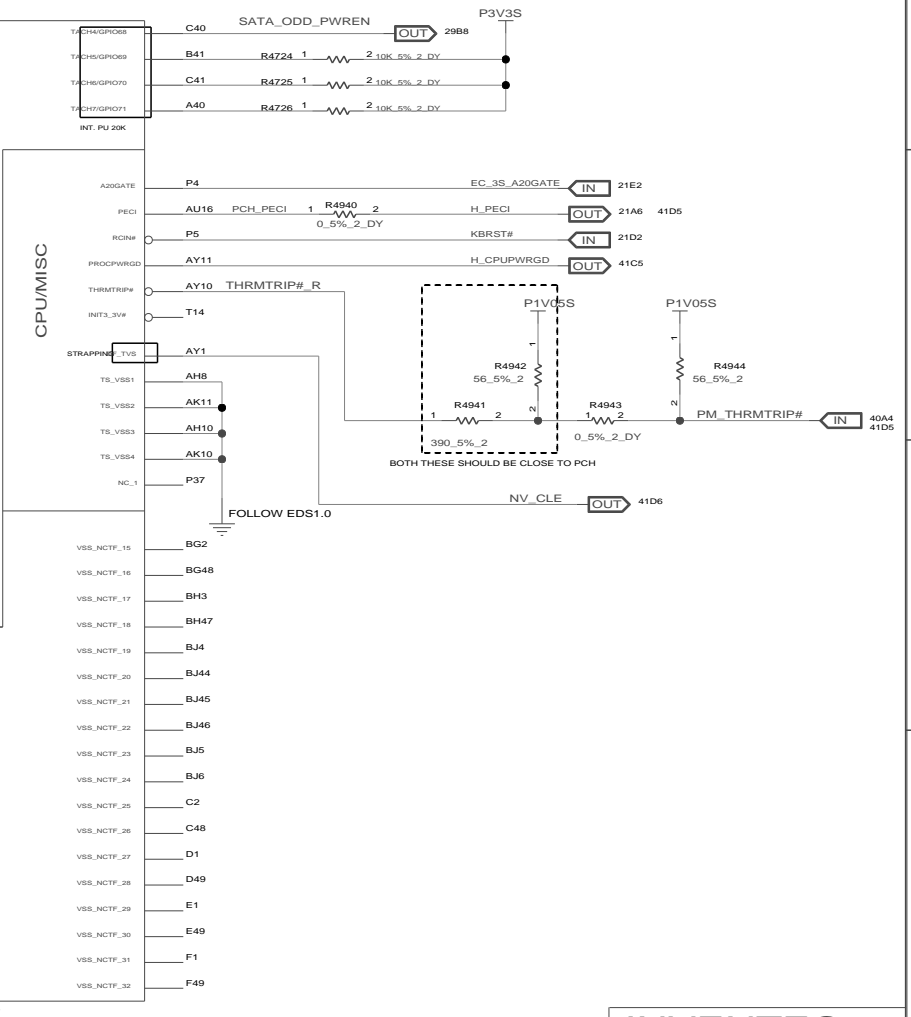
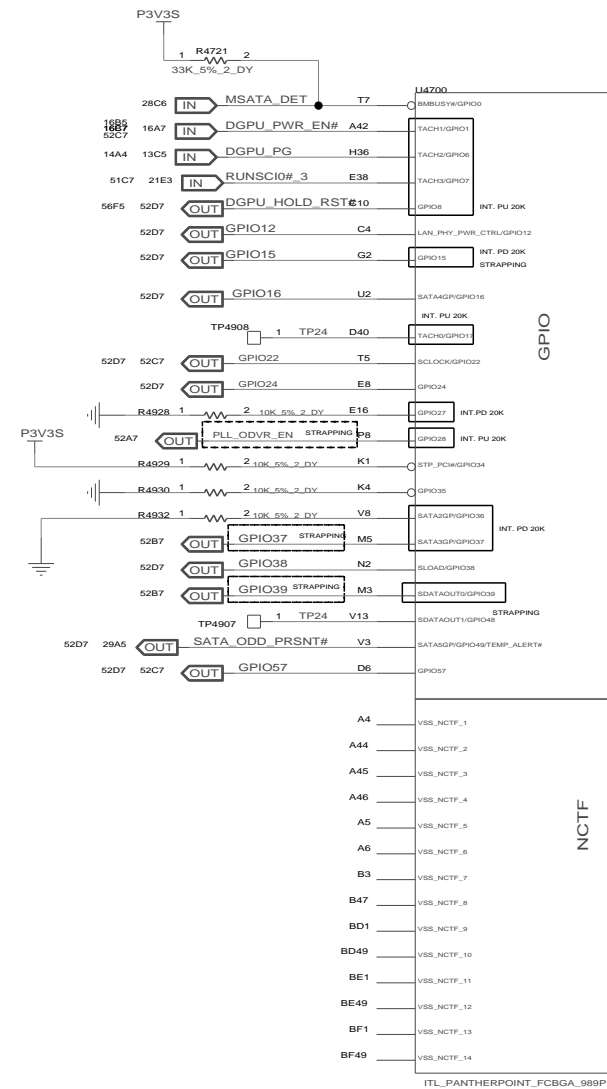
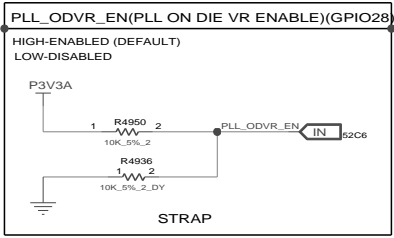
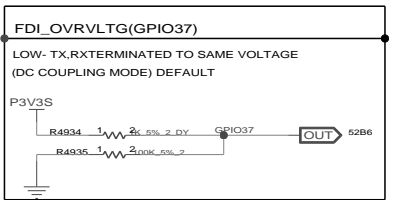
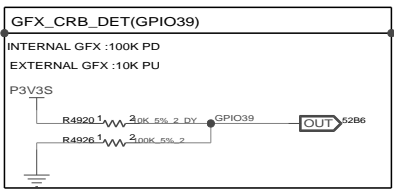
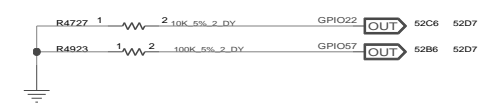
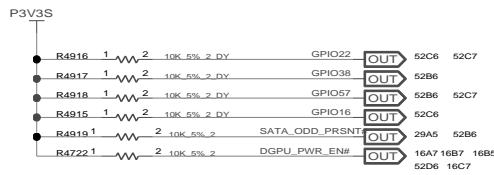
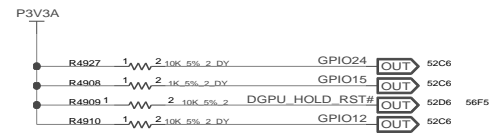
WEBCAM

3G

INVENTEC

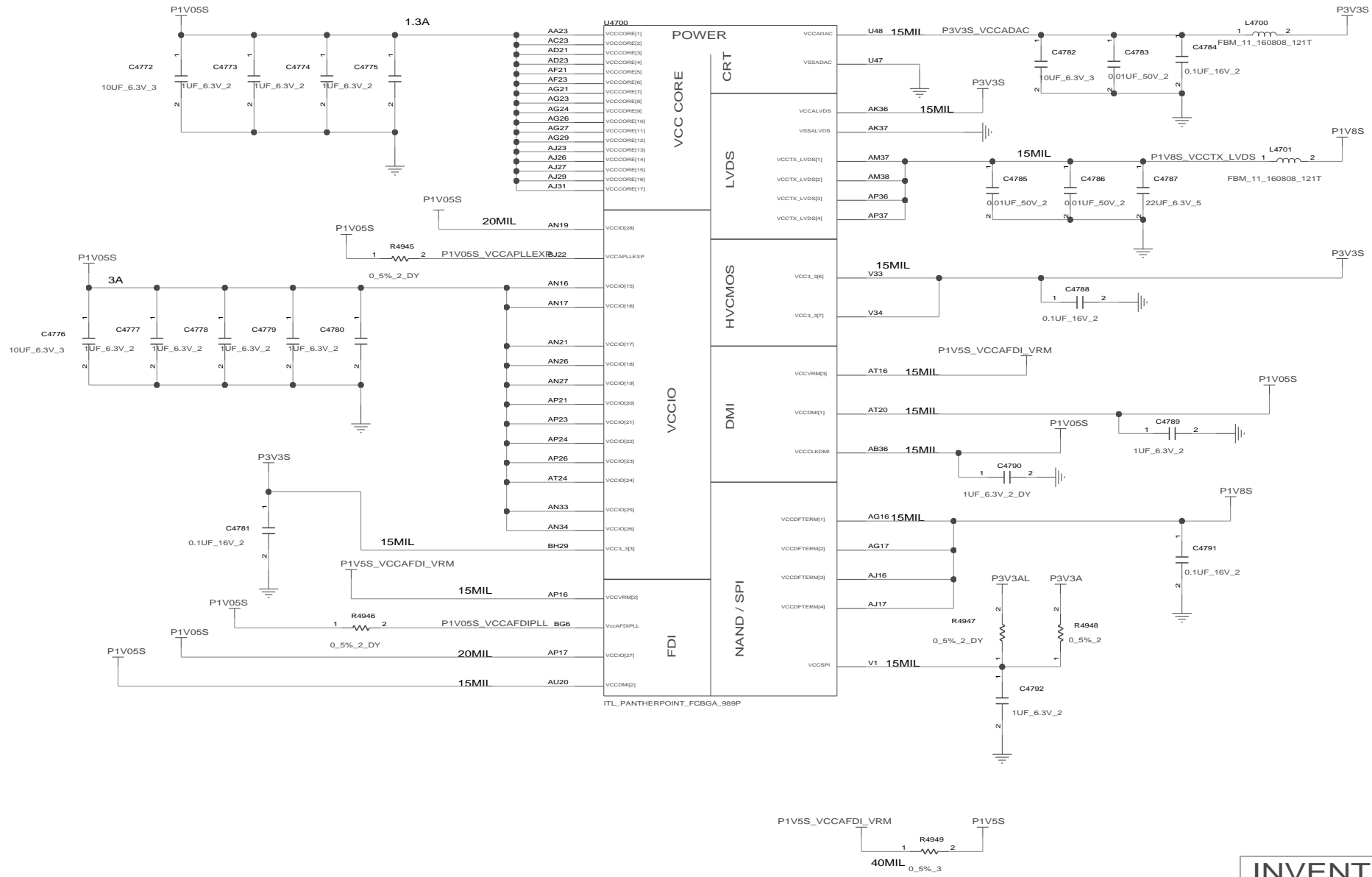
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3 CODE CS DOC.NUMBER 1310xxxx-0-0 REV X01



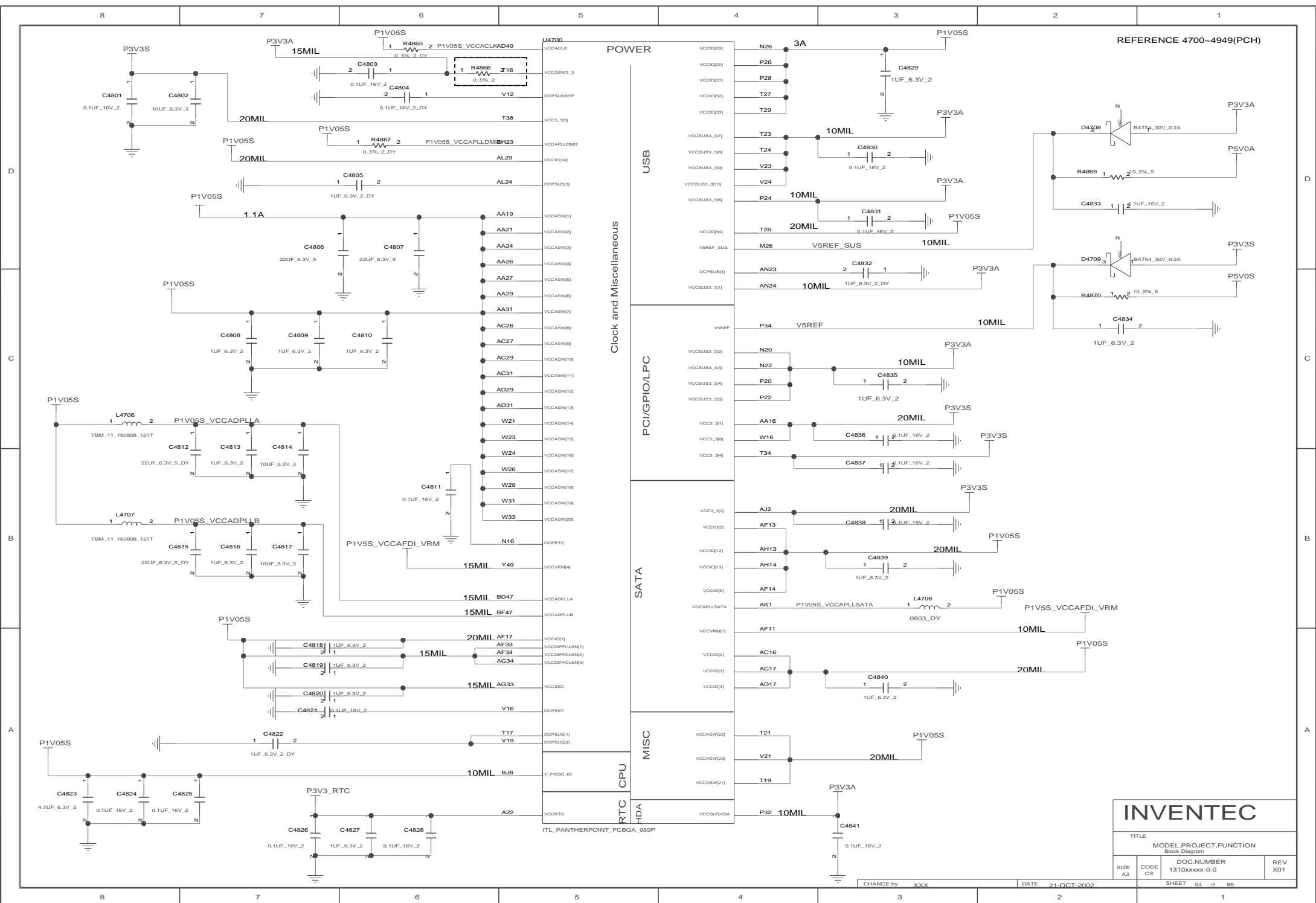
INVENTEC			
TITLE MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by xxx		DATE 21-OCT-2002	SHEET 52 of 66

REFERENCE 4700~4949(PCH)



INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET		53 of 66	

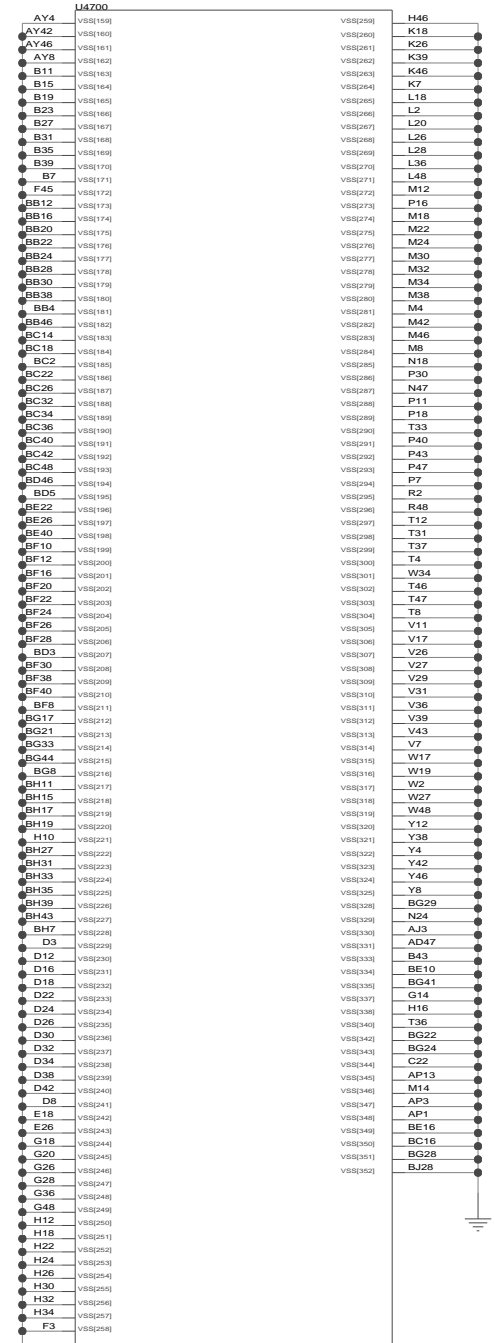
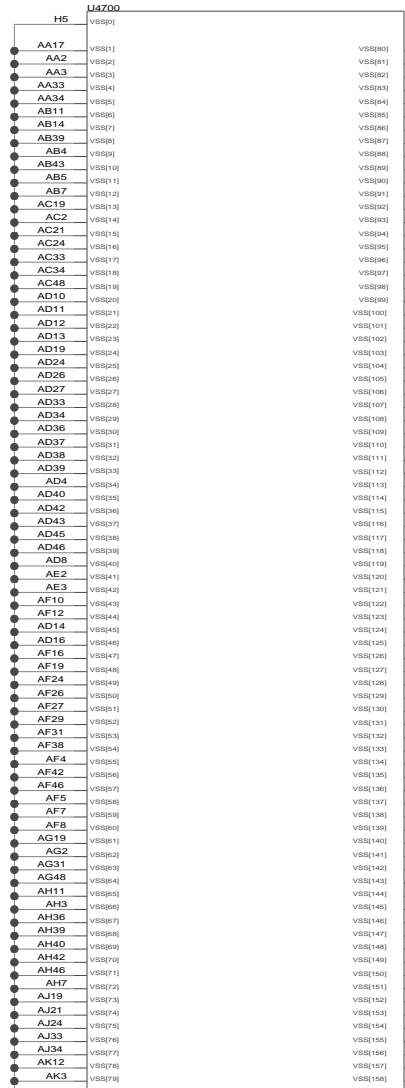


INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
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REFERENCE 4700-4949(PCH)

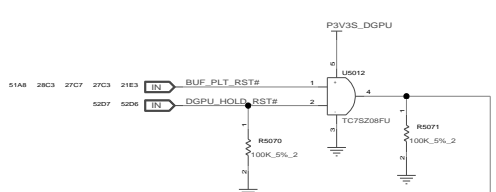
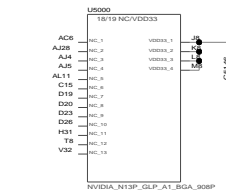


INVENTEC

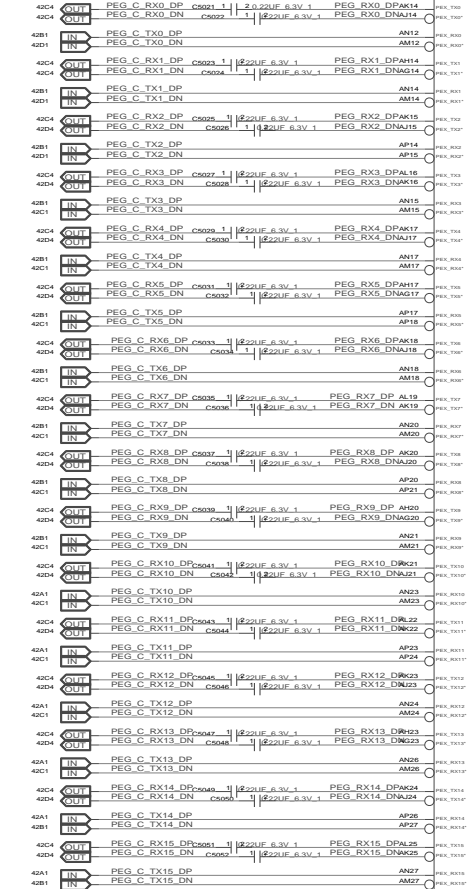
TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC. NUMBER 1310xxxx-0-0	REV X01
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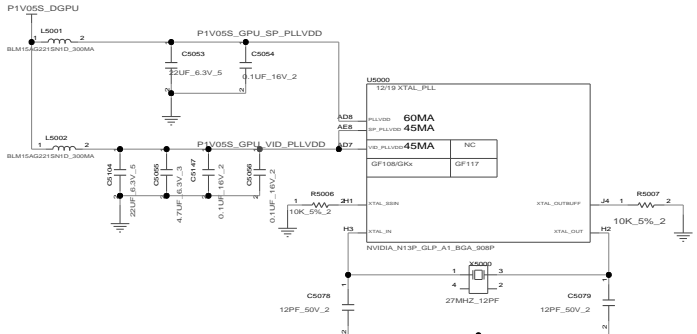
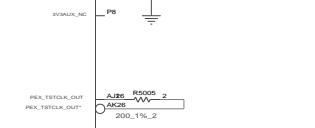
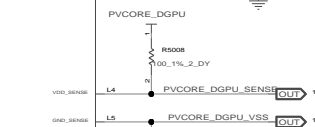
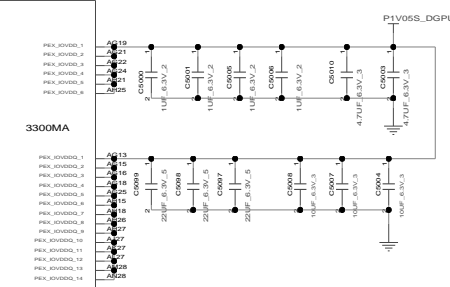
CHANGE by XXX DATE 21-OCT-2002 SHEET 55 of 66



CLOSE TO GPU

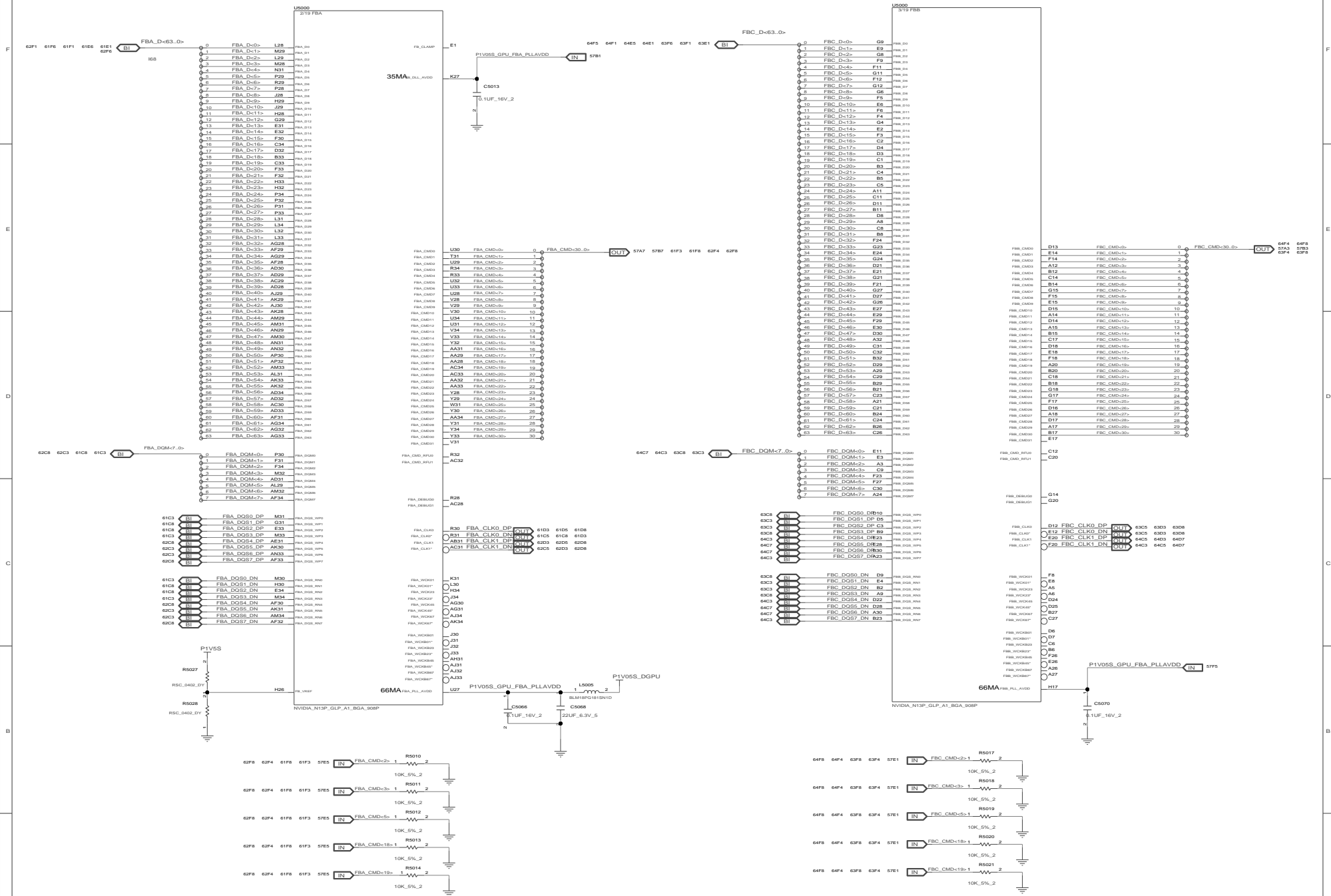


+1.05V POWER RAIL SHOULD HAVE 3500MA CAPABILITY AT LEAST



INVENTEC			
MODEL PROJECT.FUNCTION Risk Design			
SIZE	CODE	DOC NUMBER	REV
C	ES	1310xxxx-0-0	X01
CHANGE BY: xxx		DATE: 21/0CT/2002	
SHEET		96 of 96	

FB_CLAMP
N13P-PES/GL/PL: NC
N13P-GV/N13M-GS/N13P-GT-GL-PS: PL10K

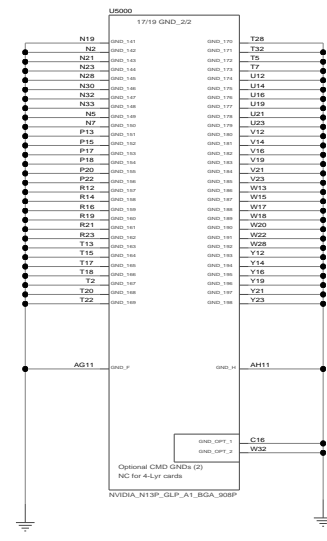
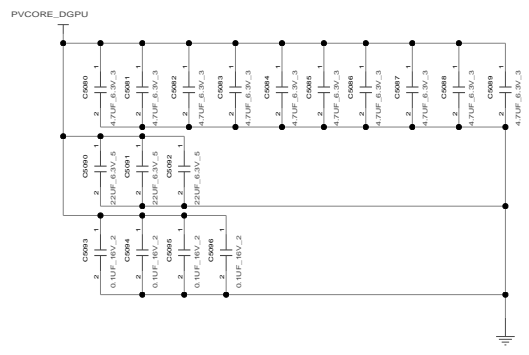
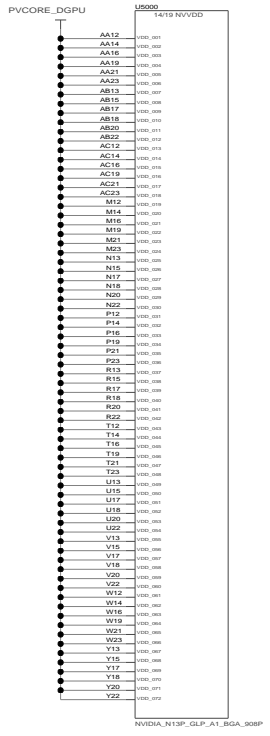
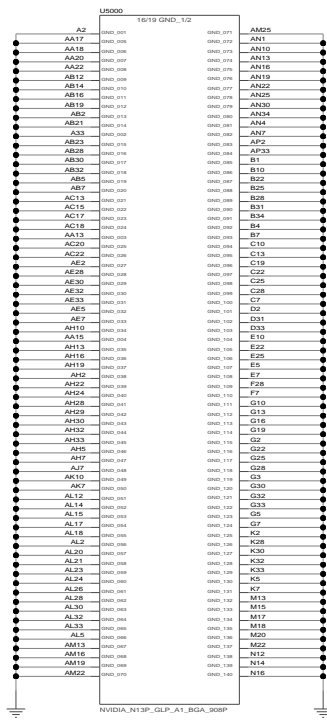


INVENTEC

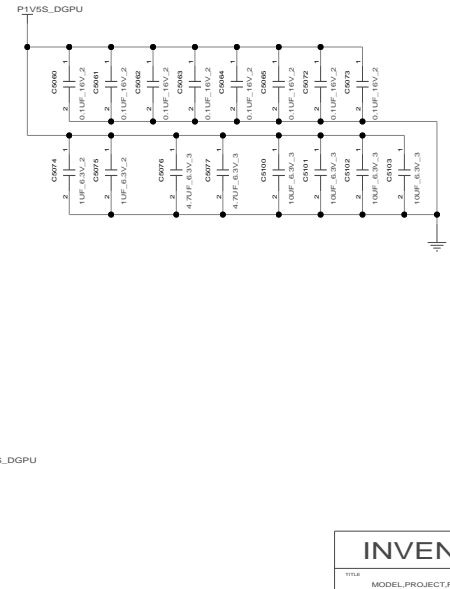
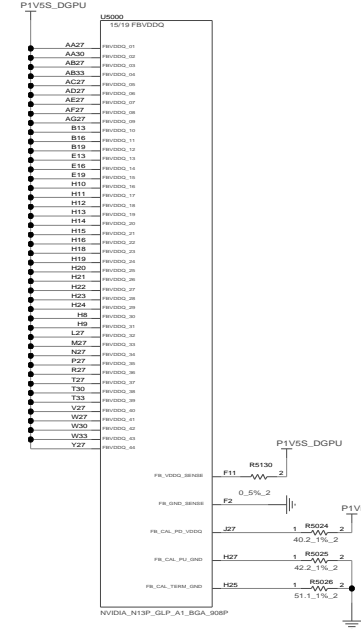
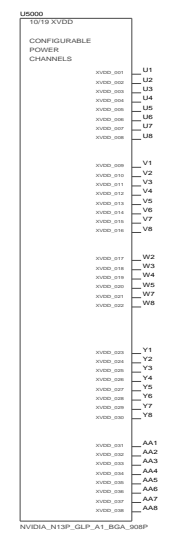
MODEL PROJECT.FUNCTION
Risk Drawing

SIZE	CODE	DOC NUMBER	REV
C	ES	1310xxxx-0-0	X01

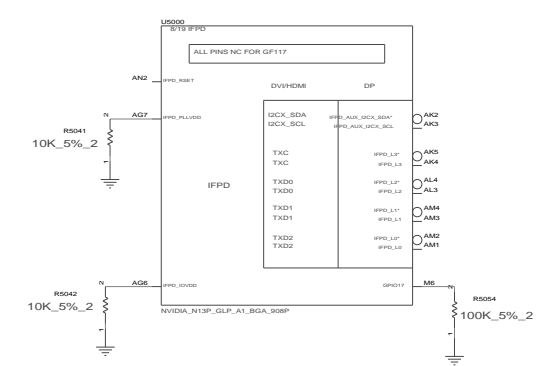
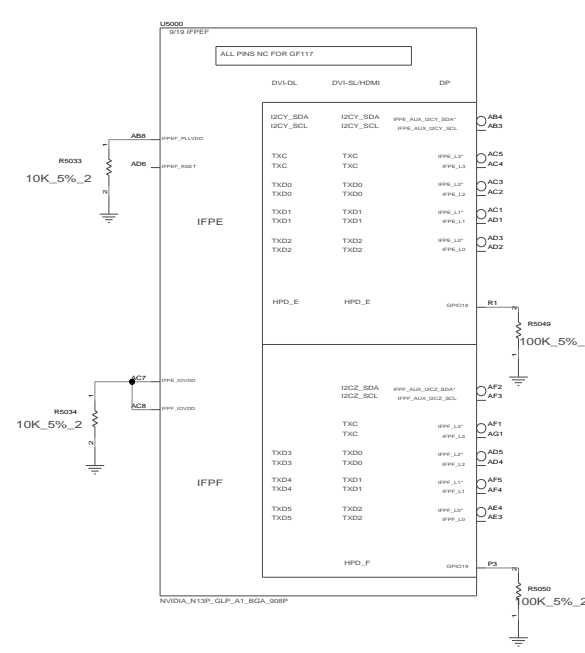
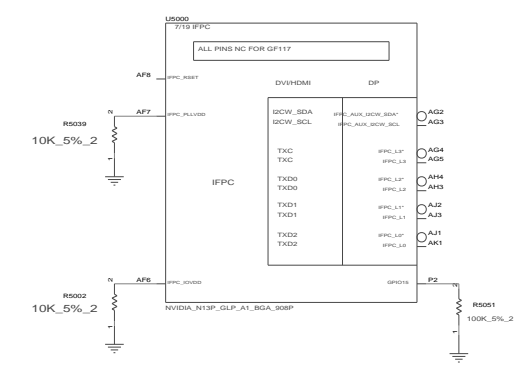
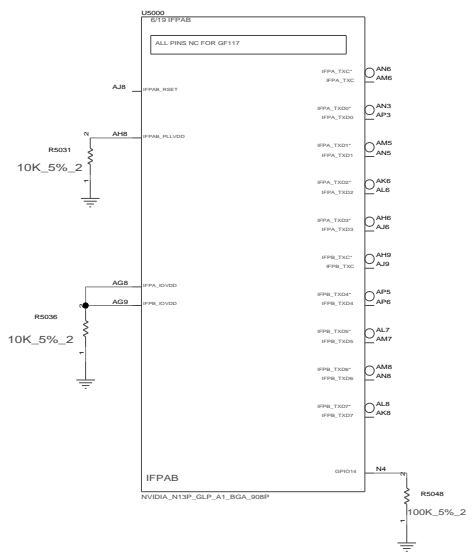
CHANGE BY: v.v.v. DATE: 21/02/2022
SHEET: 07 of 08



To be configured as needed on the PCB



TITLE			
MODEL.PROJECT.FUNCTION			
Risk Diagram			
SIZE	CODE	DOC NUMBER	REV
C	ES	1310xxxx-0-0	X01
SHEET 08 of 08			



INVENTEC			
TITLE MODEL PROJECT.FUNCTION Block Diagram			
SIZE C	CODE ES	DOC NUMBER 1310xxxx-0-0	REV X01
CHANGE BY: xxx		DATE: 21 OCT 2002	
SHEET 05		OF 05	

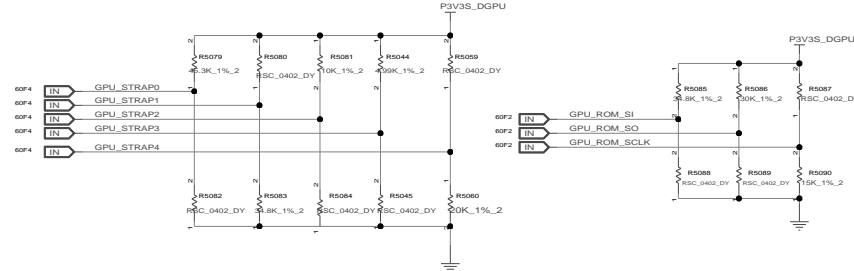
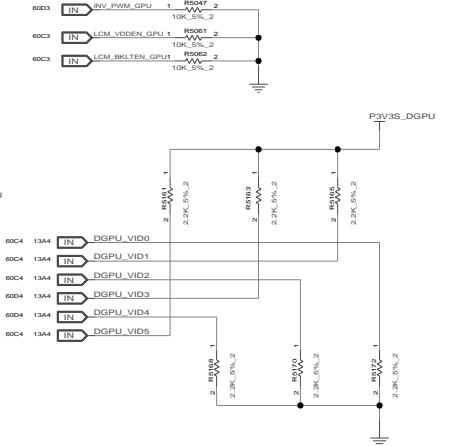
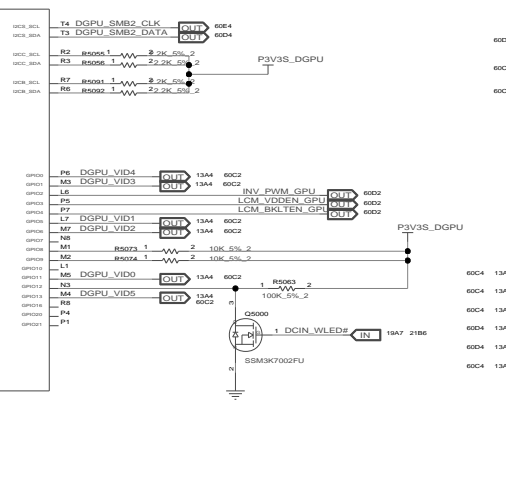
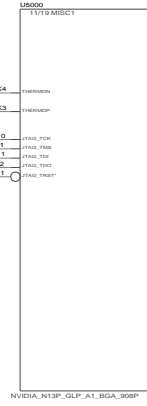
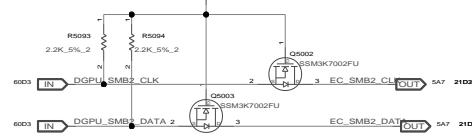
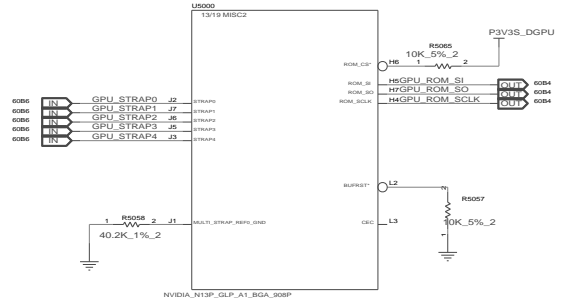
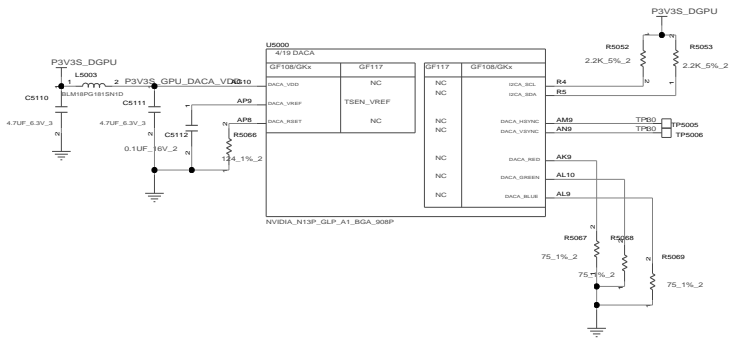
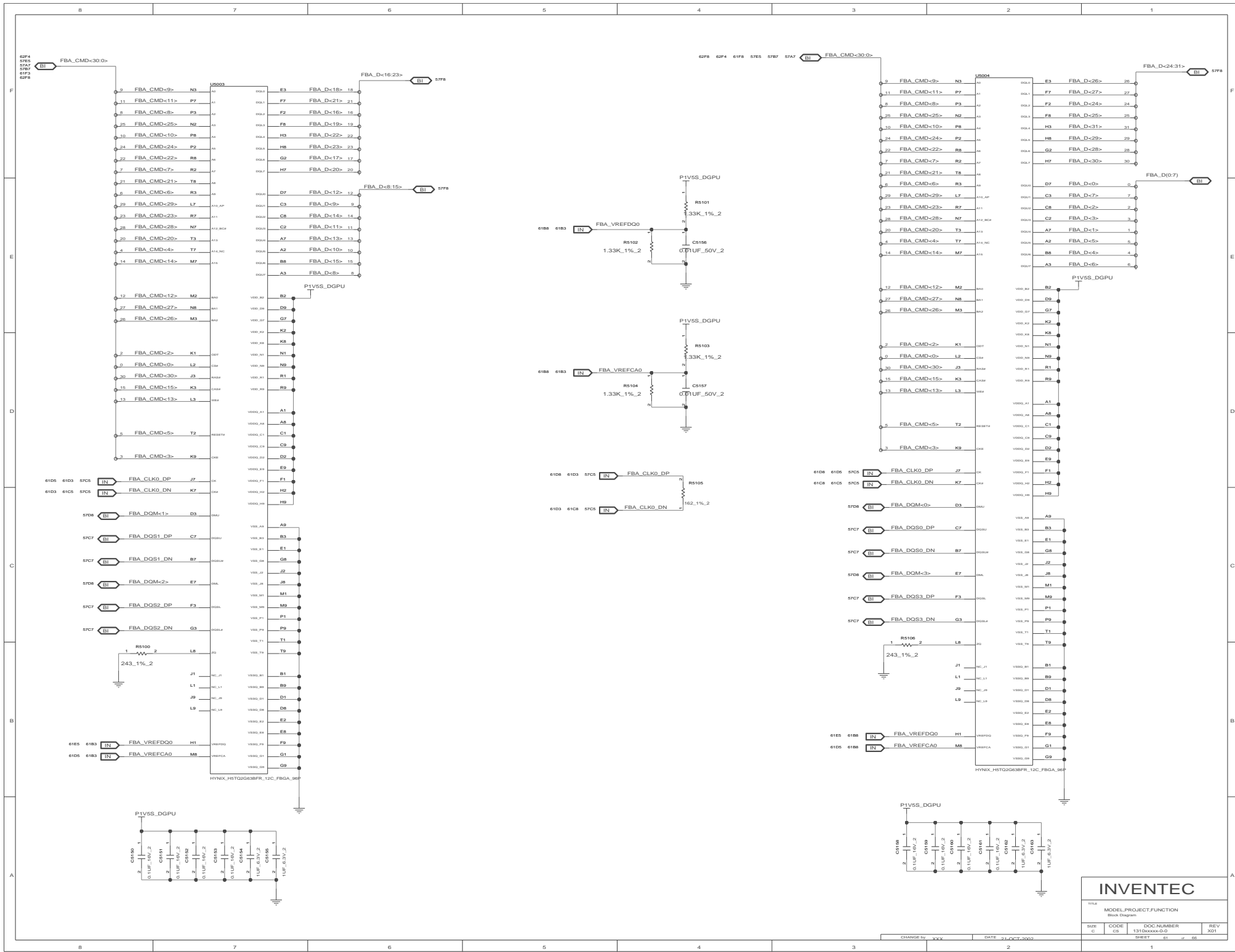
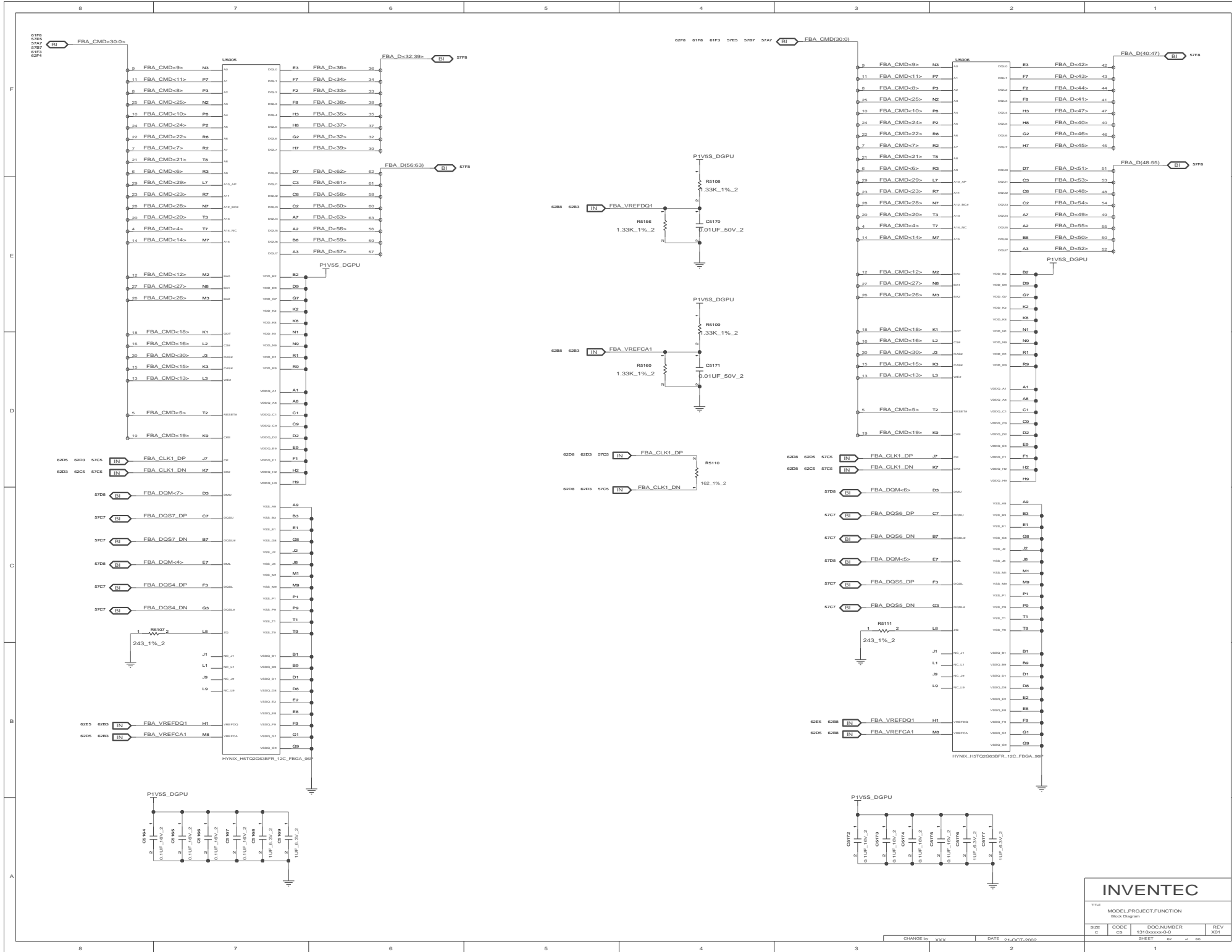


Table 5. VID Table

VID						V _{DAC} (V)
6	5	4	3	2	1	
0	1	0	1	0	1	0.9750

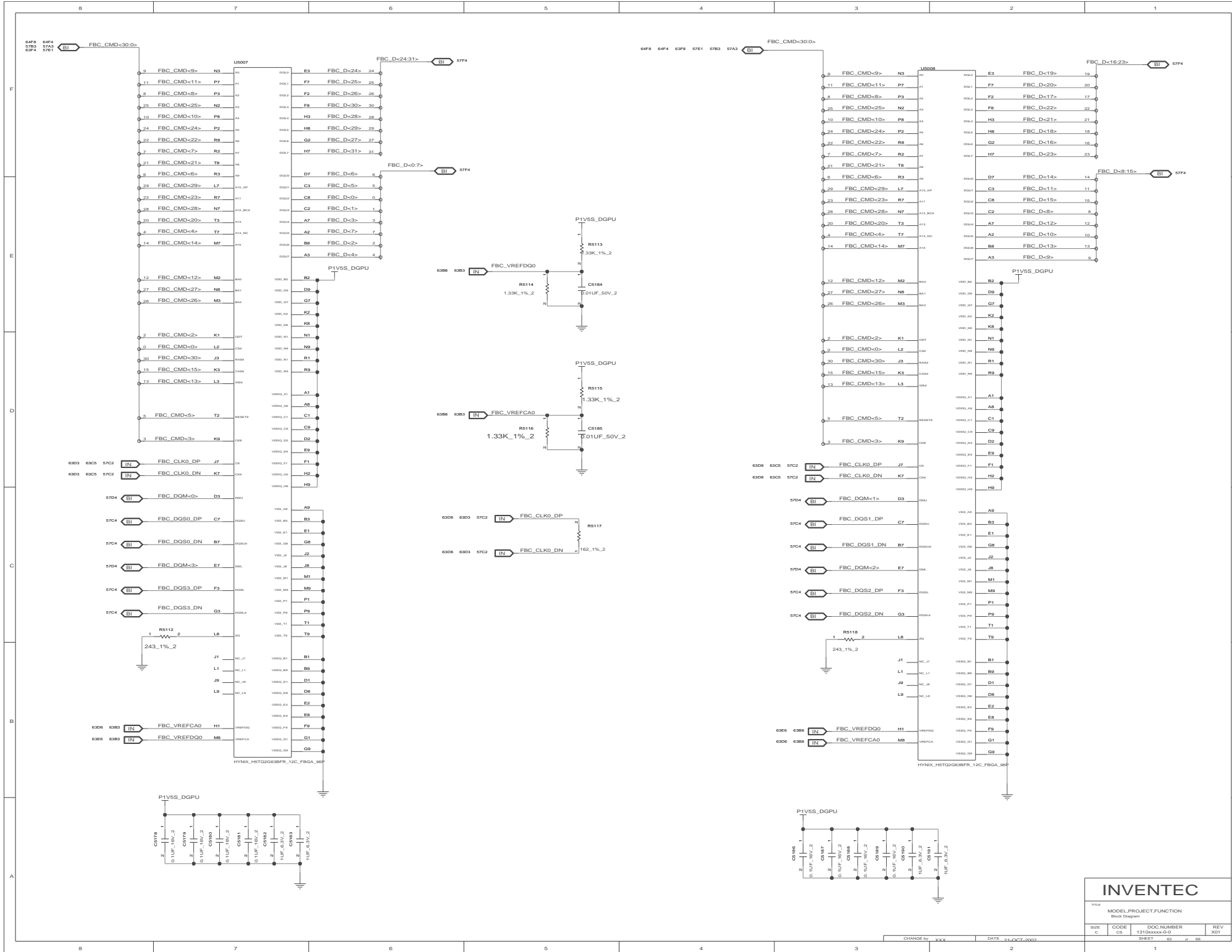


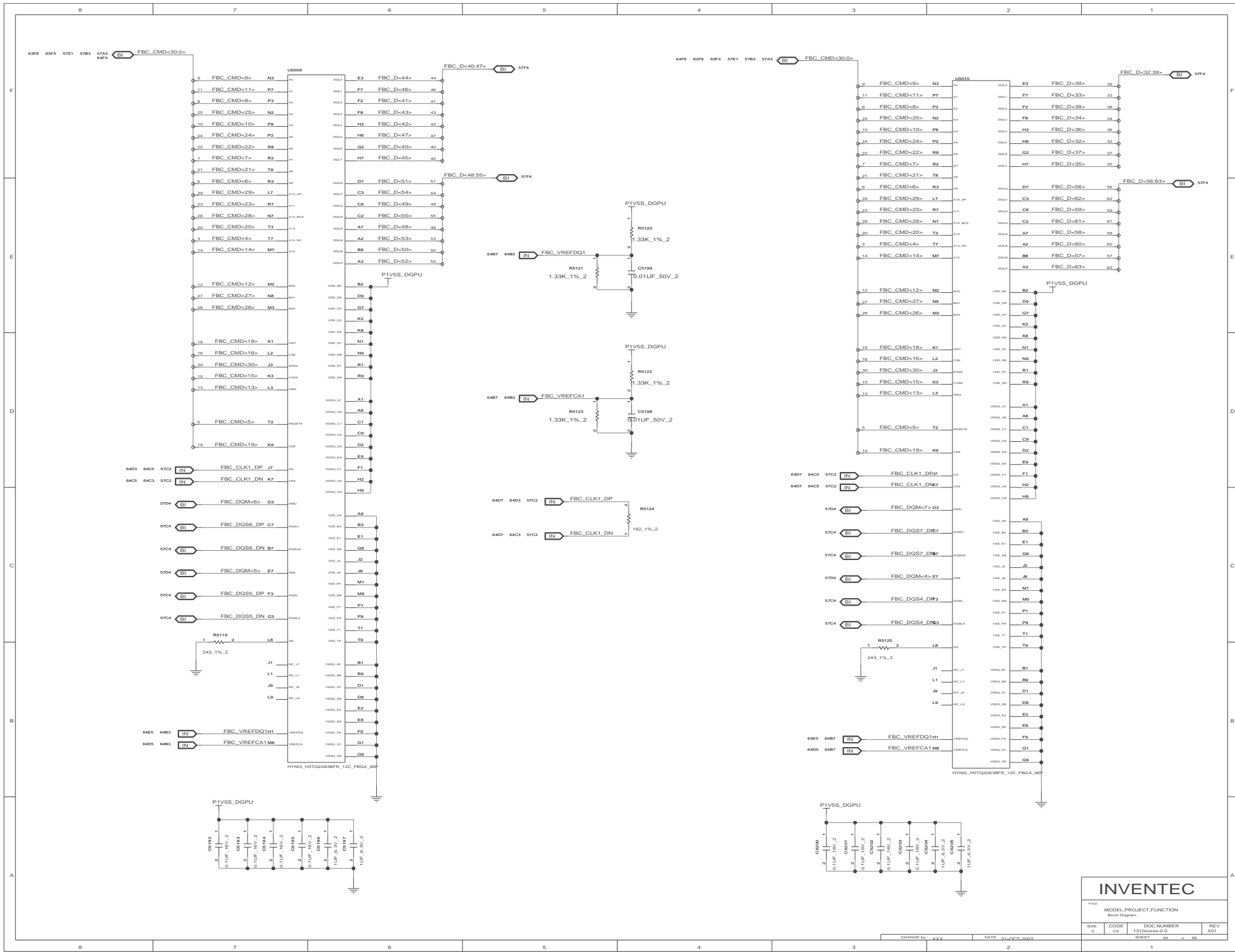
INVENTEC			
<small>TITLE</small>			
<small>MODEL PROJECT FUNCTION</small>			
<small>Block Diagram</small>			
<small>SIZE</small>	<small>CODE</small>	<small>DOC NUMBER</small>	<small>REV</small>
C	ES	1310xxxx-0-0	X01
<small>CHANGE by</small> xxx		<small>DATE</small> 21/0CT/2002	
<small>SHEET</small> 01		<small>of</small> 05	



INVENTEC			
MODEL PROJECT.FUNCTION Block Diagram			
SIZE	CODE	DOC NUMBER	REV
C	ES	1310xxxx-0-0	X01
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CHANGE by: xxx DATE: 21/0CT/2002





INVENTEC

TITLE MODEL PROJECT.FUNCTION
Block Diagram

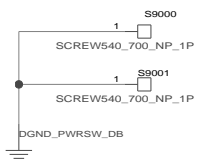
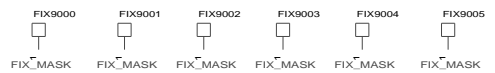
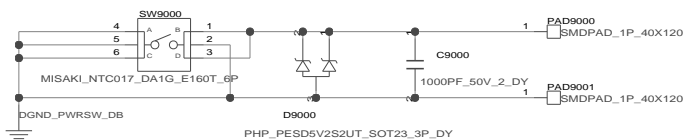
SIZE	CODE	DOC NUMBER	REV
C	ES	1310xxxx-0-0	X01

CHANGE by: xxx DATE: 21/OCT/2002

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REFERENCE 9000~9999(SMALL BOARD)

POWER BUTTON



INVENTEC			
TITLE MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 65 of 66

8 7 6 5 4 3 2 1

D

D

C

C

B

B

A

A

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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8 7 6 5 4 3 2 1