ZQP SYSTEM DIAGRAM

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

HDMI@ -----> HDMI option
SP@ -----> Board ID/Strap pin
H@ -----> 家電下鄉

UMA **REV:B**

AMD Smarter Choice

DDR3- SODIMM2 PAGE 7

DDR3- SODIMM1 PAGE 6

DDR3 Channel A

AMD Brazos
Zacate TDP~18W
19mmX19mm 413pin BGA
PAGE 3,4,5

CRT → CRT PAGE 13

LVDS → LVDS PAGE 13

TMDS → HDMI PAGE 14

CPU (PROCHOT)
E.C. (CPUFAN#)
32.768KHz 25MHz

PWM FAN SCH. PAGE 23

CPU THERMAL SENSOR (Reserve Only) PAGE 4

CPU SideBand TemperatureSense I2C

HT3 1.8GHz

AMD Hudson-M1
23mmX23mm, 605pin BGA
TDP~4.7W
PAGE 8,9,10,11,12

PCI-Express

P0 → **LAN** Atheros AR8158L rev.B (10/100) PAGE 15
25MHz
RJ45 PAGE 15

SATA - HDD PAGE 17 — SATA0 150MB 3 Gb/s

SATA - ODD PAGE 17 — SATA1 150MB 3 Gb/s

P0 → **USB2.0 Port** on board x1 PAGE 21

P9 → **Blue Tooth** PAGE 21

P13 → **Web-Camera** PAGE 13

FFC → **USB BOARD** USB2.0 Ports x2 PAGE 21

P4 → **Mini Card** (Wireless LAN) PAGE 16

P10 → **CardReader** AU6435 PAGE 18
12MHz

PCLK_DEBUG

LPC

Azalia

CLK_PCI_775

Winbond KBC NPCE791L PAGE 24

CPU SideBand TemperatureSense I2C

Audio CODEC Conexant CX20584-21Z PAGE 19

Keyboard TouchPad PAGE 23

SPI ROM PAGE 24

INT MIC PAGE 19

AUDIO CONN (H.P./ MIC) PAGE 20

Speaker CN PAGE 20

CHARGER (ISL88731A) PAGE 25

AMD CPU CORE (OZ8380) PAGE 27 — *CPU*

1V (G5602) PAGE 29 — *NB*

0.9V/DDR 1.5V(RT8207) PAGE 37

SYSTEM 5V/3V (RT8223M) PAGE 26

1.1V(G5602) PAGE 28

Discharge /Thermal protec PAGE 31

PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	Block Diagram	1A
Date: Tuesday, March 15, 2011	Sheet 1 of 32	

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PAGE#	DESCRIPTION	NOTE
1	BLOCK DIAGRAM	
2	SYSTEM INFORMATION	
3	ONTARIO MEM & PCIE I/F(1/3)	
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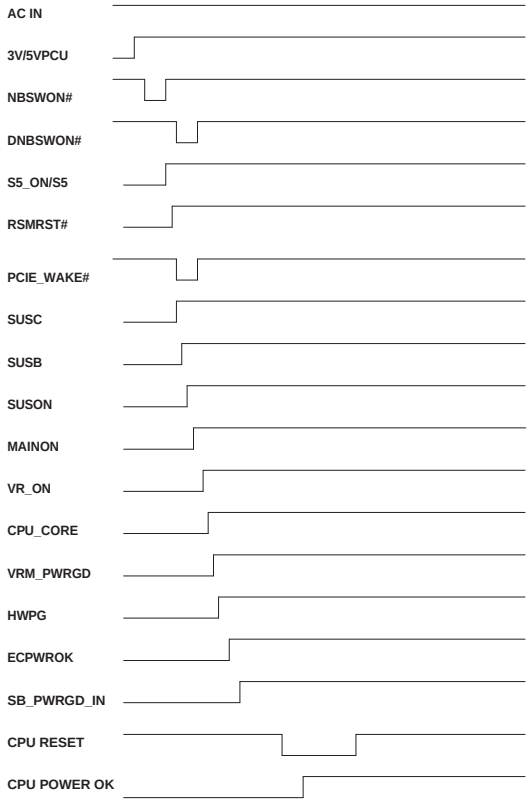
5	ONTARIO POWER & DECOUP(3/3)	
6	DDR3 SO-DIMM (STD=8)	
7	DDR3 SO-DIMM (STD=4)	
8	HUDSON PCIE/LPC/CPU IF(1/5)	
9	HUDSON ACPI/GPIO/USB(2/5)	
10	HUDSON SATA/BIDs(3/5)	
11	HUDSON PWR/GND(4/5)	
12	HUDSON STRAPS/PWRGD(5/5)	
13	CRT/LVDS/CCD	
14	HDMI	
15	LAN AR8152	
16	MINI PCI-E	
17	HDD /ODD	
18	CARD READER	
19	AUDIO - CONEXANT 20584	
20	AUDIO JACK CONN	
21	USB / BT /TP	
22	LED / NUT	
23	KB/FAN/TP	
24	WPCE791 /FLASH	
25	CHARGER (ISL88731A)	
26	SYSTEM 5V/3V (RT8223M)	
27	CPU CORE (OZ8380)	
28	VCCP 1.1V (G5602)	
29	+1V(G5602)	
30	DDR 1.5V (RT8207A)	
31	+1.8V/Discharge/Thermal Protection	
32	Change list	

Power Sequence



Hudson M1 SM BUS

SB820 SMBUS	Pin NO.	SMBUS Function Define
PCLK_SMB PDAT_SMB (+3V)	AD22 AE22	DDR / RFID
SB_SMBCLK1 SB_SMBDATA1 (+3V_S5)	F5 F4	not used
SB_SCLK2 SB_SDATA2 (+3V_S5)	D25 F23	not used
SB_SCLK3 SB_SDATA3 (+3V_S5)	B26 E26	not used
SB_SCLK3 SB_SDATA3 (+3V_S5)	B26 E26	not used

KBC(EC) SM BUS

KBC SMBUS	Pin NO.	SMBUS Function Define
MBCLK MBDATA (+3VPCU)	110 111	Battery
MBCLK_THRM MBDATA_THRM (+3VPCU)	115 116	Thermal

This page is different AMD Nile

U17E

ONTARIO (2.0)
PART 1 OF 5

MEMORY I/F

FT1_ONTARIO

U17A

ONTARIO (2.0)
PART 2 OF 5

PCIE I/F

UMI I/F

FT1_ONTARIO

Del PCIE TP 01/05

Del PCIE TP 01/05

Add R150/R153 for S3 issue
01/13

0902-- change value from 1uF to 1nF

PROJECT : ZQP	Quanta Computer Inc.
Size	Document Number: ONTARIO MEM & PCIE I/F(1/3) — Rev 1A
Date: Tuesday, March 15, 2011	Sheet 3 of 32

E350	AJ0E350VT01
C50	AJ00C50VT02

+1.8V 5,31
+3V 5,6,7,9,10,11,12,13,14,16,18,19,22,23,24,26,27,28,29,30,31

Add HDMI 01/18

ANALOG/DISPLAY/MISC

DIFFERENTIAL ROUTING

0831---follow AMD request for HDMI function

Can remove on MP------>LX

Modify 12/31

Modify 01/11

0830---add circuit

VID Override Circuit

for normal operation
open all switches

FT1_ONTARIO

SN74LVC2G07DCKR

PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	ONTATIO DISPLAY/CLK/MI(2/3)	1A
Date: Tuesday, March 15, 2011	Sheet 4 of 32	

This page is different AMD Nil

+1.5V_SUS 3,6,7,22,30
+1V 22,29
+1.8V 4,31
+3V 4,6,7,9,10,11,12,13,14,16,18,19,22,23,24,26,27,28,29,30,31
+VCORE 22,27
+NBCORE 22,27
VDD_10 3

U17C
FT1_ONTARIO
ONTARIO (2.0) PART 4 OF 5
POWER

+VCORE
11A 440mil viax22
E5 E6 F5 F7 G6 G8 H5 H7 J6 J8 L7 M6 M8 N7 R8

+NBCORE
10A 400mil viax20
E8 E11 E13 F9 F12 G11 G13 H9 H12 K11 K13 L10 L12 L14 M11 M12 M13 N10 N12 N14 P11 P13

+1.5V_SUS
2A 80mil viax4
G16 G19 E17 J16 L16 L19 N16 R16 R19 W18 U16

VDD_18
2A 80mil viax4
U8 W8 U6 U9 W6 T7 V7
1u/6.3V_4 C134
C135 10u/6.3V_8 C175 C544
0.1u/10V_4 C149 C148
1u/6.3V_4 C127
R371 0_8 +1.8V

VDDAN_18_DAC
150mA 10mil viax1
W9
C18
C674 10u/6.3V_8
C537 10u/6.3V_8
C188 1u/6.3V_4
L58 BLM18PG221SN1D(220_1.4A)_6 +1.8V
C19

VDDPL_10
200mA 10mil viax1
T49 +1V
U11
R103 0_6
0.1u/10V_4 C534
C192 C191
10u/6.3V_8 1u/6.3V_4

0901-- change R7037 P/N and footprint add R

VDD_10
5.5A 220mil viax11
U13 W13 V12 T12
10u/6.3V_8 C579
C280 0.1u/10V_4 C237 C236 C238 C235
10u/6.3V_8 1u/6.3V_4 1u/6.3V_4
R149 0_8 R144 0_8 +1V

+3V
500mA 20mil viax1
A4
C528 1u/6.3V_4

+VCORE
10u/6.3V_8 C501 C170 C498 C499 C500 C141 C206 10u/6.3V_8
10u/6.3V_8 10u/6.3V_8 10u/6.3V_8

+VCORE
0.1u/10V_4 C131 C166 C168 C136 C130 C164 C169 C132 C167 0.1u/10V_4
0.1u/10V_4 0.1u/10V_4 0.1u/10V_4 0.1u/10V_4

+VCORE
1u/6.3V_4 C163 C138 C165 C129 1u/6.3V_4
1u/6.3V_4 1u/6.3V_4

+NBCORE
10u/6.3V_8 C155 C259 C147 C266 C231 10u/6.3V_8
10u/6.3V_8 10u/6.3V_8

+NBCORE
1u/6.3V_4 C195 C198 C233 C154 C197 1u/6.3V_4
1u/6.3V_4 1u/6.3V_4 1u/6.3V_4

+NBCORE
0.1u/10V_4 C194 C181 C203 C199 C247 C251 C250 C214 C252 0.1u/10V_4
0.1u/10V_4 0.1u/10V_4 0.1u/10V_4 0.1u/10V_4

+1.5V_SUS
1u/6.3V_4 C269 C289 C321 C315 1u/6.3V_4
1u/6.3V_4

+1.5V_SUS
C351 10u/6.3V_8 C352 10u/6.3V_8

+1.5V_SUS
0.1u/10V_4 C272 C275 C311 C273 C271 C296 C319 C316 C350 0.1u/10V_4
0.1u/10V_4 0.1u/10V_4 0.1u/10V_4 0.1u/10V_4

U17D
GROUND
ONTARIO (2.0) PART 5 OF 5
FT1_ONTARIO
A7 B7 B11 B17 B22 C4 D5 D7 D9 D11 D14 B15 D17 D19 E7 E9 E12 E20 F8 F11 F13 G4 G5 G7 G9 G12 G20 G22 H6 H11 H13 J4 J5 J7 J20 K10 K14 L4 L6 L8 L11 L13 L20 L22 M7 N4 N6 N8 N11
N13 N20 N22 P10 P14 R4 R7 R20 T6 T9 T11 T13 U4 U5 U7 U12 U20 U22 V8 V9 V11 V13 W1 W2 W4 W5 W7 W12 W20 Y5 Y7 Y9 Y11 Y13 Y15 Y17 Y19 AA4 AA22 AB2 AB5 AB9 AB13 AB17 AB21 AC5 AC9 AC13 A11

place capacitors under BGA
EMC CAPS
+1.5V_SUS C270 180P/50V_4 C303 180P/50V_4
+VCORE 180P/50V_4 C133 C128 180P/50V_4
+NBCORE C196 180P/50V_4 C232 180P/50V_4
+1.5V_SUS 0.1u/10V_4 C274 C320 0.1u/10V_4
VDD_18 C174 180P/50V_4 C153 180P/50V_4
VDDAN_18_DAC C187 180P/50V_4
VDD_10 C234 180P/50V_4
VDDPL_10 C190 180P/50V_4
+3V C521 0.1u/10V_4

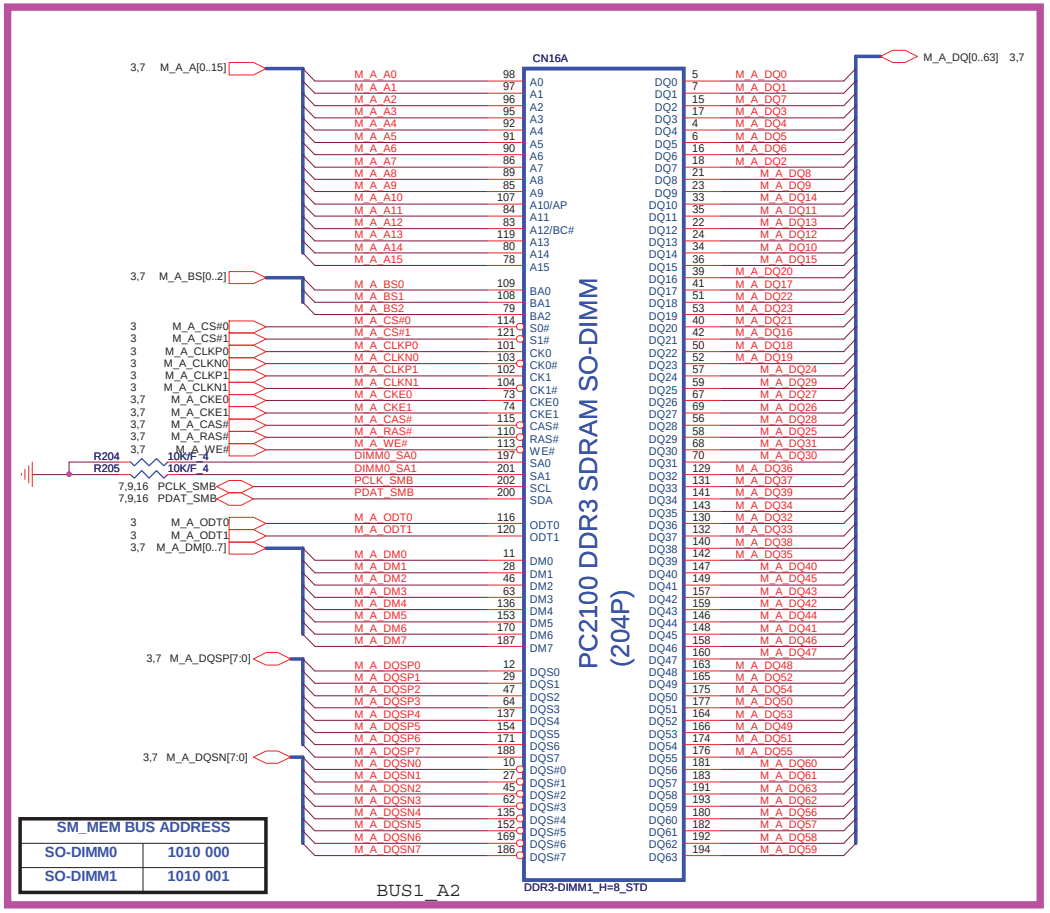
PROJECT : ZQP
Quanta Computer Inc.
Size | Document Number: ONTARIO POWER&DECOUP(3/3) | Rev 1A
Date: Tuesday, March 15, 2011 | Sheet 5 of 32

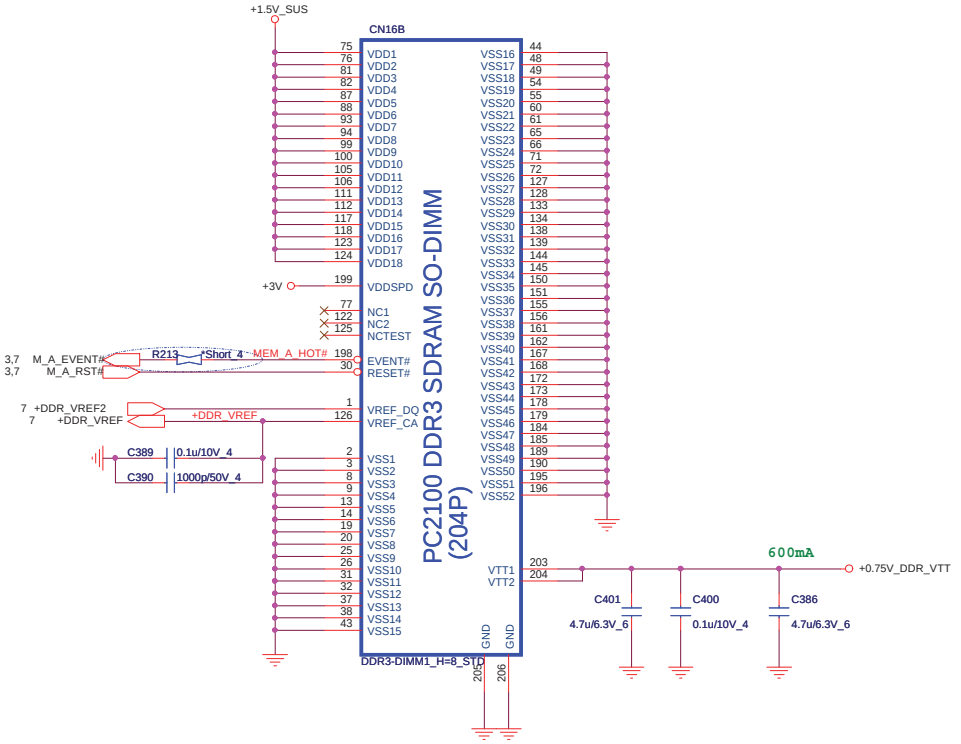
0830--P/N and footprint are follow ZR7B

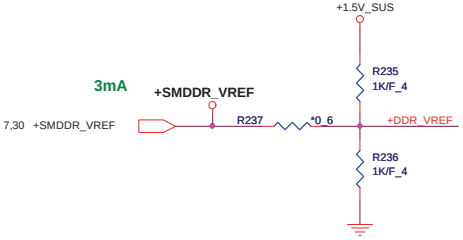
+1.5V_SUS 3,5,7,22,30

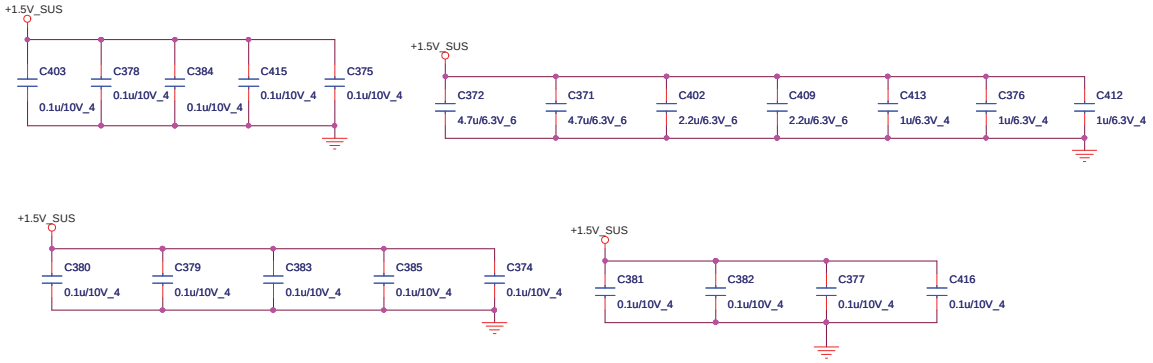
+0.75V_DDR_VTT 7,30

+3V 4,5,7,9,10,11,12,13,14,16,18,19,22,23,24,26,27,28,29,30,31









PROJECT : ZQP	Quanta Computer Inc.
Size	Document Number: DDR3 SO-DIMM (STD) — Rev 1A
Date: Tuesday, March 15, 2011	Sheet 6 of 32

0830--P/N and footprint are follow ZR7B

07

+1.5V_SUS 3,5,6,22,30
+0.75V_DDR_VTT 6,30
+3V 4,5,6,9,10,11,12,13,14,16,18,19,22,23,24,26,27,28,29,30,31

CN20A

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0_H=4_Standard

SM_MEM BUS ADDRESS	
SO-DIMM0	1010 000
SO-DIMM1	1010 001

BUS1_A2

CN20B

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0_H=4_Standard

3mA

+SMDDR_VREF

R244 *0_6

R245 1K/F_4

R246 1K/F_4

C423 4.7u/6.3V_6
C434 4.7u/6.3V_6
C410 2.2u/6.3V_6
C439 2.2u/6.3V_6
C417 1u/6.3V_4
C435 1u/6.3V_4
C420 1u/6.3V_4

C433 0.1u/10V_4
C426 0.1u/10V_4
C428 0.1u/10V_4
C429 0.1u/10V_4

C411 0.1u/10V_4
C430 0.1u/10V_4
C424 0.1u/10V_4
C414 0.1u/10V_4
C418 0.1u/10V_4

C436 0.1u/10V_4
C427 0.1u/10V_4
C425 0.1u/10V_4
C438 0.1u/10V_4
C404 0.1u/10V_4

C421 4.7u/6.3V_6
C419 0.1u/10V_4
C437 4.7u/6.3V_6

C432 0.1u/10V_4
C431 1000p/50V_4

R251 *Short_4

PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	DDR3 SO-DIMM (STD)	1A
Date: Tuesday, March 15, 2011	Sheet 7 of 32	

This page is different AMD Nile expect RTC circuit

PCIE_VDDR 11
+3V_S5 9,10,11,12,15,21,22,26
+3VPCU 13,22,23,24,25,26,31
+5VPCU 26,27,28,31

RTC

PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U41

Hudson M1 Part 1 of 5

STRAP Function To EC

Debug STRAPs

All the PCI bus has build-in Pull-UP/Down resistors

Del Q33,R434,R435,R444 from BOMs, ZQE no support RTC charge circuits.

CR2032 (Non-Chargeable)
AHL03003014
AHL030M0009

RTC_CLK must ready refore RSMRST#

INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).

To LAN Controller

To WLAN Controller

To STRAPs Page

Add C606,C614,C619 for strong clock
02/15 REV:B

BG625000486

PROJECT : ZQP
Quanta Computer Inc.

Size | Document Number: HUDSON PCIE/LPC/CPU IF(1/5) | Rev 1A
Date: Tuesday, March 15, 2011 | Sheet 8 of 32

This page is different AMD Nile

SCL0/SDATA0 is 3V tolerance
AMD datasheet define it
Clock gen/Robson/TV tuner /DDR3/DDR3 thermal/Accelerometer

+3V R125 2.2K_4 PCLK_SMB
+3V R131 2.2K_4 PDAT_SMB

+3V R179 *10K/F_4 SUS_STAT#
+3V R133 4.7K_4 NB_PWRGD

+3V_S5 R175 10K/F_4 CPU_THERMTRIP#

SB/ PWR_GOOD / VDDIO_33_S

+3V_S5 R437 *10K/F_4 SYS_RST#
+3V R120 *10K/F_4 SIO_A20GATE
By AMD confirm

+3V_S5
R436 *10K/F_4 DNBSWON#
R189 10K/F_4 PCIE_WAKE#
R352 10K/F_4 SB_SCLK3
R353 10K/F_4 SB_SDATA3
R193 10K/F_4 SB_PWRGD_IN
R116 2.2K_4 SB_SCLK4
R102 2.2K_4 SB_SDATA4

+3V, +3V_S5 4,5,6,7,10,11,12,13,14,16,18,19,22,23,24,26,27,28,29,30,31 / 8,10,11,12,15,21,22,26

U18D
Hudson M1
Part 4 of 5

3 APU_MEMHOT# J2
T163 R# K1
T157 SPI_CS3# D3
24 SUSB# F1
24 SUSC# H1
24 DNBSWON# F2
SB_PWRGD_IN H5
SUS_STAT# G6
SB_TEST0 B3
T155 SB_TEST1 C4
T97 SB_TEST2 F6
T82 SIO_A20GATE AD21
24 SIO_A20GATE AE21
24 SIO_RCIN# K2
24 SIO_EXT_SCI# J29
24 SIO_EXT_SMI# H2
T166 SYS_RST# J1
15,24 PCIE_WAKE# H6
C346 100p/50V_4 F3
T169 CPU_THERMTRIP# J6
4 CPU_THERMTRIP# NB_PWRGD AC19
24 ICH_RSMRST# G1

PCI_PME#/GEVENT4#
R#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/GEVENT23#
GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
NB_PWRGD
RSMRST#

ACPI / WAKE UP EVENTS

USBCLK/14M_25M_48M_OSC A10 T144
USB_RCOMP G19 USB_RCOMP_SB R139 11.8K/F_4

USB 1.1 USB MISC

USB_FSD1P/GPIO186 J10 T69
USB_FSD1N H11 T70
USB_FSD0P/GPIO185 H9 T76
USB_FSD0N J8 T85

USB_HSD13P B12 A12
USB_HSD13N
USB_HSD12P F11 E11 T192 T194
USB_HSD12N
USB_HSD11P E14 E12
USB_HSD11N
USB_HSD10P J12 J14
USB_HSD10N
USB_HSD9P A13 B13
USB_HSD9N
USB_HSD8P D13 C13
USB_HSD8N
USB_HSD7P G12 G14
USB_HSD7N
USB_HSD6P G16 G18
USB_HSD6N
USB_HSD5P D16 C16
USB_HSD5N
USB_HSD4P B14 A14
USB_HSD4N
USB_HSD3P E18 E16 T195 T196
USB_HSD3N
USB_HSD2P J16 J18
USB_HSD2N
USB_HSD1P B17 A17
USB_HSD1N
USB_HSD0P A16 B16
USB_HSD0N

USB 2.0

Add TP 01/11
Add TP 01/11

DEL MINI CARD 12/31
USBP9+ 16 / USBP9- 16 WL1
USBP8+ 21 / USBP8- 21 EXT BLUETOOTH
USBP7+ 21 / USBP7- 21 BLUETOOTH
USBP6+ 18 / USBP6- 18 4 IN 1 CARD READER (MMC)
USBP5+ 21 / USBP5- 21 USB3 Connector (Daughter)
USBP2+ 13 / USBP2- 13 CCD
USBP1+ 21 / USBP1- 21 USB2 Connector (Daughter)
USBP0+ 21 / USBP0- 21 USB1 Connector (MB Side)

8 SB_GPIO_RST# PCIE_REQ_LAN# R AC18
15 PCIE_REQ_LAN# R140 *Short_4 dGPU_PWR_EN AF20
Modify 12/31 T86 AE19
T61 AF19
19 SPKR AD22
6,7,16 PCLK_SMB PCLK_SMB
6,7,16 PDAT_SMB PDAT_SMB AE22
+3V_S5 R184 10K/F_4 SB_SMBCLK1 F5
R185 10K/F_4 SB_SMBDATA1 F4
Modify 12/31 T183 PCIE_REQ_WLAN2# R AH21
16 PCIE_REQ_WLAN1# R142 *Short_4 PCIE_REQ_WLAN1# R AB18
ACCLED_EN E1
T168 AJ21
T142 H4
T159 D5
T90 D7
T81 G5
T91 K3
T165 AA20
T59

CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#
GBE_LED0/GPIO183
GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN

GPIO

T164 CPU_MEMHOT#_IN H3
+3V_S5 R187 *10K/F_4 21 OC_6# D1
21 OC_4# E4
D4
E8
T77 F7
T84 E7
T83 F8
T78

BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/TRST#/GEVENT12#

USB OC

SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it

SCL2/GPIO193 D25 SB_SCLK2 R360 10K/F_4 +3V_S5
SDA2/GPIO194 F23 SB_SDATA2 R362 10K/F_4
SCL3_LV/GPIO195 B26 SB_SCLK3 4
SDA3_LV/GPIO196 E26 SB_SDATA3 SB_SDATA3 4
EC_PWM0/EC_TIMER0/GPIO197 F25
EC_PWM1/EC_TIMER1/GPIO198 T53 E22
EC_PWM2/EC_TIMER2/GPIO199 T125 F22 SB_GPIO199 R132 *2.2K_4
EC_PWM3/EC_TIMER3/GPIO200 E21 SB_GPIO200 R134 2.2K_4

has checked with AMD FAE already--Allen

GPIO200	GPIO199
H,H = Reserved	
H,L = SPI ROM (DEFAULT)	
L,H = LPC ROM	
L,L = FWH ROM	

EMBEDDED CTRL

KSI_0/GPIO201 G24
KSI_1/GPIO202 G25
KSI_2/GPIO203 E28
KSI_3/GPIO204 E29
KSI_4/GPIO205 D29
KSI_5/GPIO206 D28
KSI_6/GPIO207 C29
KSI_7/GPIO208 C28

KSO_0/GPIO209 B28
KSO_1/GPIO210 A27
KSO_2/GPIO211 B27
KSO_3/GPIO212 D26
KSO_4/GPIO213 A26
KSO_5/GPIO214 C26
KSO_6/GPIO215 A24
KSO_7/GPIO216 B25
KSO_8/GPIO217 A25
KSO_9/GPIO218 D24
KSO_10/GPIO219 B24
KSO_11/GPIO220 C24
KSO_12/GPIO221 B23
KSO_13/GPIO222 A23
KSO_14/GPIO223 D22
KSO_15/GPIO224 C22
KSO_16/GPIO225 A22
KSO_17/GPIO226 B22

To Azalia
HD audio interface is 3.3S voltage

for EMI
19 ACZ_BITCLK_AUDIO C607 *10p/50V_4 R424 33_4 R412 *10K_4 ACZ_BITCLK_R M3
12 ACZ_SDOUT ACZ_SDOUT N1
19 ACZ_SDOUT_AUDIO R425 33_4 L2
C608 *10p/50V_4 M2
19 ACZ_SDIN0 C604 *10p/50V_4 R411 *10K_4 M1
R414 33_4 ACZ_SYNC_R M4
19 ACZ_SYNC_AUDIO R416 33_4 ACZ_RST#_R N2
19 ACZ_RESET#_AUDIO C605 *10p/50V_4 P2

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#

HD AUDIO

R417 10K/F_4 GBE_COL T1
R428 10K/F_4 GBE_CRS T4
L6
+3V_S5 R171 10K/F_4 GBE_MDIO L5
T9
U1
U3
T2
U2
T5
R169 10K/F_4 GBE_RXERR V5
P5
M5
P9
T7
P7
M7
P4
M9
+3V_S5 R161 10K/F_4 GBE_PHY_INTR V7

GBE_COL
GBE_CRS
GBE_MDCK
GBE_MDIO
GBE_RXCLK
GBE_RXD3
GBE_RXD2
GBE_RXD1
GBE_RXD0
GBE_RXCTL/RXDV
GBE_RXERR
GBE_TXCLK
GBE_TXD3
GBE_TXD2
GBE_TXD1
GBE_TXD0
GBE_TXCTL/TXEN
GBE_PHY_PD
GBE_PHY_RST#
GBE_PHY_INTR

GBE LAN

Modify 12/31 T172 SB_SDATA4 E23
T171 SB_SCLK4 E24
T58 SB_GPIO166 F21
T114 SB_GPIO160 G29

PS2_DAT/SDA4/GPIO187
PS2_CLK/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
FC_RST#/GPIO160

T116 AC_OK D27
T115 BAT_INT# F28
F29
E27

PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192

EMBEDDED CTRL

HudsonM1

System PWR_OK(CLG)

+3V_S5
C349 *0.1u/10V_4
U8
T193 SB_PWRGD_IN 4
Modify 12/31
2
1 PWROK_EC
CPU_COREPG 27
PWROK_EC 24
TC7SH08FU
R194 100K_4

PROJECT : ZQP
Quanta Computer Inc.
Size | Document Number: HUDSON ACPI/GPIO/USB(2/5) | Rev 1A
Date: Tuesday, March 15, 2011 | Sheet 9 of 32

SATA PORT 0,1,2,3 can support AHCI mode

PLACE SATA AC COUPLING CAPS CLOSE TO Hudson M1

AVDD_SATA 11
+3V 4,5,6,7,9,11,12,13,14,16,18,19,22,23,24,26,27,28,29,30,31
+3V_S5 8,9,11,12,15,21,22,26

This page is different AMD Nile

SATA HDD

17 SATA_TXP0 — C592 .01U/16V/X7R_4 — SATA_TXP0_C — AH9 — SATA_TX0P
17 SATA_TXN0 — C590 .01U/16V/X7R_4 — SATA_TXN0_C — AJ9 — SATA_TX0N
17 SATA_RXN0 — AJ8 — SATA_RX0N
17 SATA_RXP0 — AH8 — SATA_RX0P

SATA ODD

17 SATA_TXP1 — C588 .01U/16V/X7R_4 — SATA_TXP1_C — AH10 — SATA_TX1P
17 SATA_TXN1 — C585 .01U/16V/X7R_4 — SATA_TXN1_C — AJ10 — SATA_TX1N
17 SATA_RXN1 — AG10 — SATA_RX1N
17 SATA_RXP1 — AF10 — SATA_RX1P

AG12 — AF12 — SATA_TX2P / SATA_TX2N
AJ12 — AH12 — SATA_RX2N / SATA_RX2P
AH14 — AJ14 — SATA_TX3P / SATA_TX3N
AG14 — AF14 — SATA_RX3N / SATA_RX3P
AG17 — AF17 — SATA_TX4P / SATA_TX4N
AJ17 — AH17 — SATA_RX4N / SATA_RX4P
AJ18 — AH18 — SATA_TX5P / SATA_TX5N
AH19 — AJ19 — SATA_RX5N / SATA_RX5P

PLACE SATA_CAL RES VERY CLOSE TO BALL OF Hudson M1

XTLVDD_SATA-- SATA crystal power

PLVDD_SATA-- SATA PLL POWER

AVDD_SATA — R147 1K/F_4 — R143 931/F_4 — SATA_CALRP — SATA_CALRN — AB14 — AA14 — SATA_CALRP / SATA_CALRN

22 SATA_LED# — AD11 — SATA_ACT#/GPIO67

C575 *22p/50V_4 — Y4 *25MHz_30PPM — R381 *1M/F_4 — C582 *22p/50V_4 — SATA_X1 AD16 — SATA_X2 AC16

T89 SPI_DI J5
T96 SPI_DO E2
T160 SPI_CLK K4
T79 SPI_CS1# K9
T162 ROM_RST# G2
SPI_DI/GPIO164 / SPI_DO/GPIO163 / SPI_CLK/GPIO162 / SPI_CS1#/GPIO165 / ROM_RST#/GPIO161

U18B

Hudson M1

Part 2 of 5

SERIAL ATA / FLASH / HW MONITOR / SPI ROM

FC_CLK AH28 — T123
FC_FBCLKOUT AG28 — T124
FC_FBCLKIN AF26 — T47

FC_OE#/GPIOD145 AF28 — T121
FC_AVD#/GPIOD146 AG29 — T122
FC_WE#/GPIOD148 AG26 — T128
FC_CE1#/GPIOD149 AF27 — T119
FC_CE2#/GPIOD150 AE29 — T118
FC_INT1/GPIOD144 AF29 — T120
FC_INT2/GPIOD147 AH27 — T129

FC_ADQ0/GPIOD128 AJ27 — T126
FC_ADQ1/GPIOD129 AJ26 — T133
FC_ADQ2/GPIOD130 AH25 — T132
FC_ADQ3/GPIOD131 AH24 — T137
FC_ADQ4/GPIOD132 AG23 — T135
FC_ADQ5/GPIOD133 AH23 — T134
FC_ADQ6/GPIOD134 AJ22 — T138
FC_ADQ7/GPIOD135 AG21 — T143
FC_ADQ8/GPIOD136 AF21 — T139
FC_ADQ9/GPIOD137 AH22 — T140
FC_ADQ10/GPIOD138 AJ23 — T141
FC_ADQ11/GPIOD139 AF23 — T131
FC_ADQ12/GPIOD140 AJ24 — T136
FC_ADQ13/GPIOD141 AJ25 — T130
FC_ADQ14/GPIOD142 AG25 — T46
FC_ADQ15/GPIOD143 AH26 — T127

FANOUT0/GPIO52 W5 — BOARD_ID0
FANOUT1/GPIO53 W6 — BOARD_ID1
FANOUT2/GPIO54 Y9 — SB_PROCHOT#
FANIN0/GPIO56 W7 — BOARD_ID2
FANIN1/GPIO57 V9 — BOARD_ID3
FANIN2/GPIO58 W8 — BOARD_ID4

0831--modify location

TEMPIN0/GPIO171 B6 — TEMPIN0
TEMPIN1/GPIO172 A6 — TEMPIN1
TEMPIN2/GPIO173 A5 — TEMPIN2
TEMPIN3/TALERT#/GPIO174 B5 — SB_TALERT#
TEMP_COMM C7 — SB_TALERT# 4

VIN0/GPIO175 A3 — CPU_TYPE
VIN1/GPIO176 B4 — SB_HOLE_TIME
VIN2/GPIO177 A4 — CPU_SENSOR
VIN3/GPIO178 C5 — VIN2 — R390 10K_4
VIN4/GPIO179 A7 — VIN3 — R387 10K_4
VIN5/GPIO180 B7 — VIN4 — R386 10K_4
VIN6/GBE_STAT3/GPIO181 B8 — VIN5 — R383 10K_4
VIN7/GBE_LED3/GPIO182 A8 — BOARD_ID5

NC1 G27
NC2 Y2

4,8,24 H_PROCHOT# — H_PROCHOT# — D6 RB500V-40 — SB_PROCHOT#

0831--add circuit

AMD recommand : TEMPIN0 / TEMPIN1 / TEMPIN2 can not maintain on floating stages when without usage. Do not care pull high or pull down.

TEMPIN2 — R388 10K_4
TEMPIN1 — R389 10K_4
TEMPIN0 — R391 10K_4

MB ID

CPU THERMAL	GPIO52
External	1
SB-TSI	0

	GPIO57
(Dis) SW	1
UMA	0

SB8XX Hold Time	GPIO53
1.2V	1
1.1V	0

	GPIO58
With HDMI	1
Without HDMI	0

DU1/MK2	GPIO56
MK2.0 AMD	1
DU1.0 AMD	0

	GPIO182
PX4.0	1
PX3.0	0

+3V

GPIO52: R182 10K_4 BOARD_ID0 R192 *10K_4
GPIO53: R181 10K_4 BOARD_ID1 R191 *10K_4
GPIO56: R180 10K_4 BOARD_ID2 R190 *10K_4
GPIO57: R158 10K_4 BOARD_ID3 R157 *SP@10K_4
GPIO58: R418 *SP@10K_4 BOARD_ID4 R429 SP@10K_4

GPIO 58 define to HDMI strap pin
02/11 REV:B

+3V_S5

GPIO182: R385 *SP@10K_4 BOARD_ID5 R384 10K_4
R400 *10K/F_4 CPU_TYPE R399 10K/F_4
R395 *10K/F_4 CPU_SENSOR R394 10K/F_4
R398 *10K/F_4 SB_HOLE_TIME R397 10K/F_4

Modify 01/14

PROJECT : ZQP
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Size	Document Number	Rev
	HUDSON SATA/BIDs(3/5)	1A
Date: Tuesday, March 15, 2011	Sheet 10 of 32	

+3V 4,5,6,7,9,10,12,13,14,16,18,19,22,23,24,26,27,28,29,30,31
+1.1V 22,28,31
+3V_S5 8,9,10,12,15,21,22,26
+1.1V_S5 28
AVDD_SATA 10
VDDIO_AZ 12

This page is different AMD Nile

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

GPIOD Interface Not Implemented connected to GND through a 0-Ω resistor

U18C Hudson M1 Part 3 of 5

POWER

42mA
150mA 10mil viax1
22mA
1115mA 50mil viax3
15mA 5mil vaix1
1354mA 60mil viax3
534mA 25mil viax2
88mA
790mA 35mil viax2
382mA 20mil viax1
165mA 10mil viax1
49mA
15mA
58mA
46mA
65mA
16mA
12mA
5mA

U18E Hudson M1 GROUND Part 5 of 5

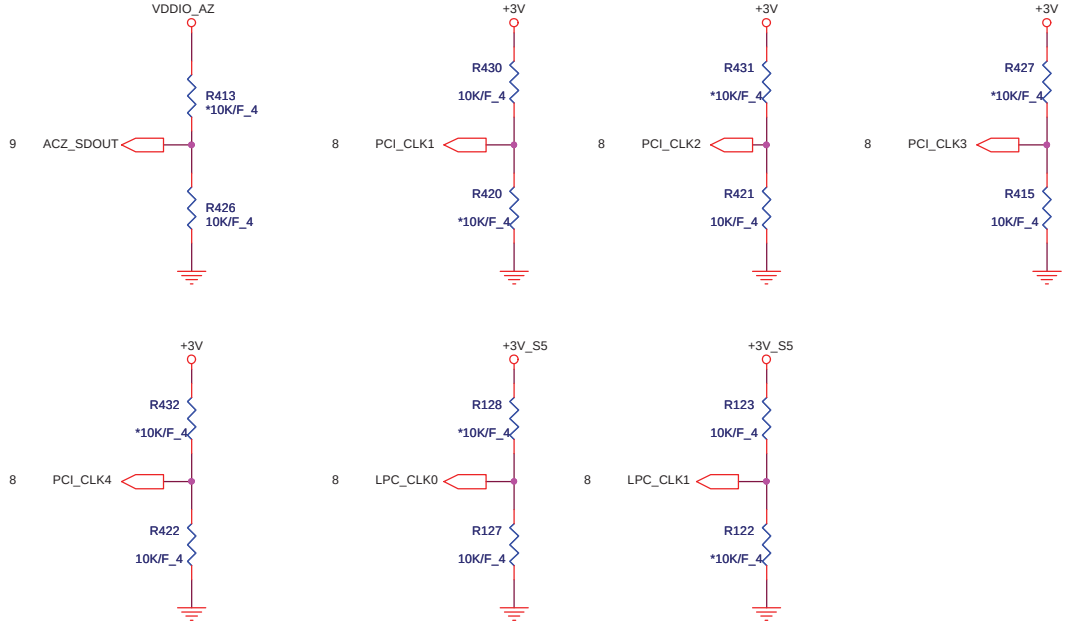
PROJECT : ZQP
Quanta Computer Inc.
Size | Document Number: HUDSON PWR/GND(4/5) | Rev 1A
Date: Tuesday, March 15, 2011 | Sheet 11 of 32

VDDIO_AZ 11
+3V 4,5,6,7,9,10,11,13,14,16,18,19,22,23,24,26,27,28,29,30,31
+3V_S5 8,9,10,11,15,21,22,26

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

intermal have pull
Hi 10K , confirm AMD
ward this pull Hi
not need

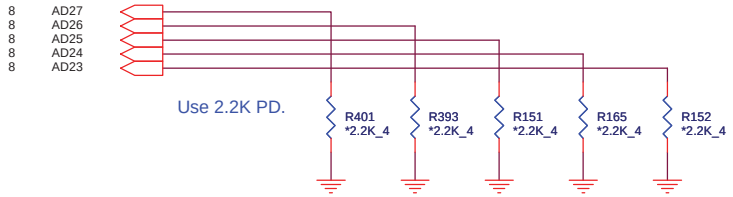
REQUIRED STRAPS



PCI_CLK4 CPU/NB HT Clock Selection
0 V - Reserved.
3.3 V - Required setting for integrated clock mode.
This strap is not used if the strap CLKGEN is
configured for external clock generator mode.

DEBUG STRAPS

HUDSON-M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM (Default)
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM L,L = FWH ROM

PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	HUDSON STRAPS/PWRGD(5/5)	1A
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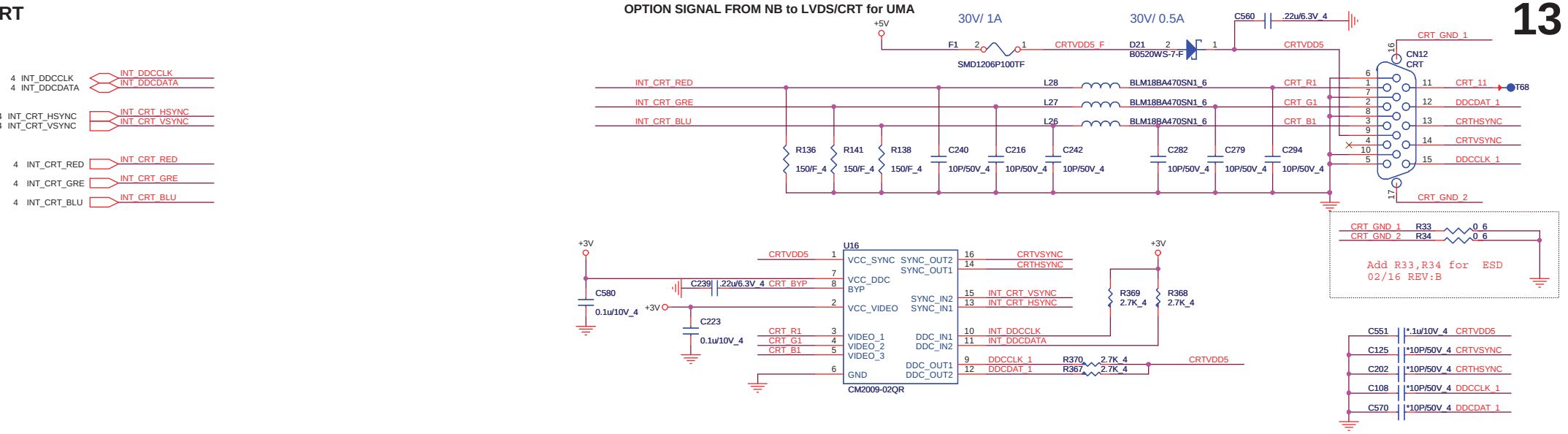
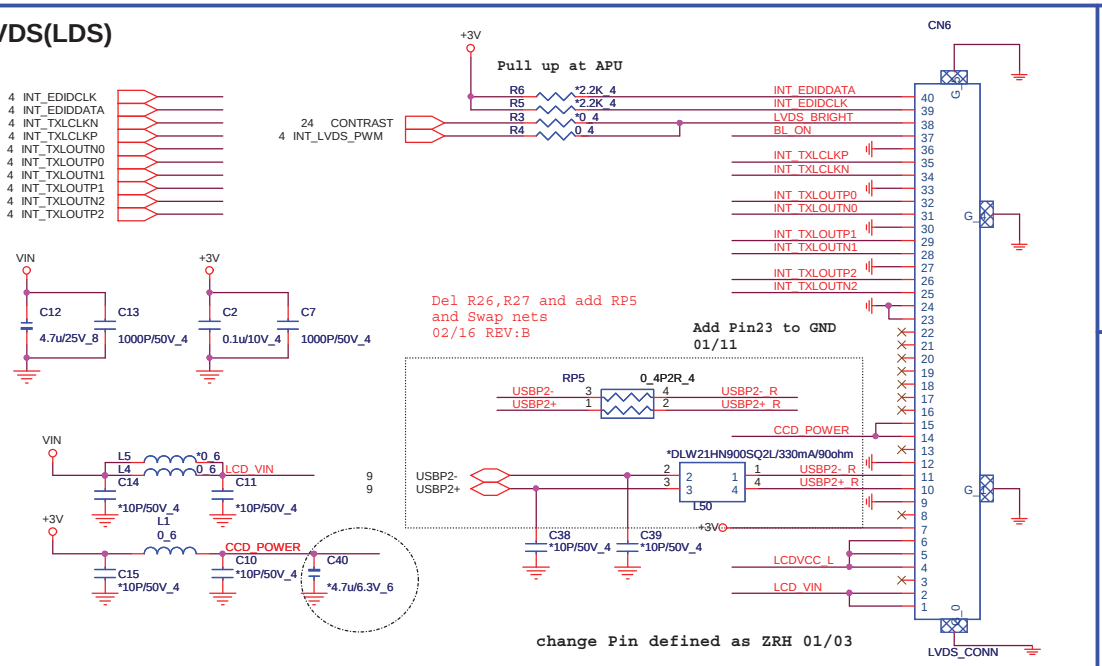
CRT

OPTION SIGNAL FROM NB to LVDS/CRT for UMA

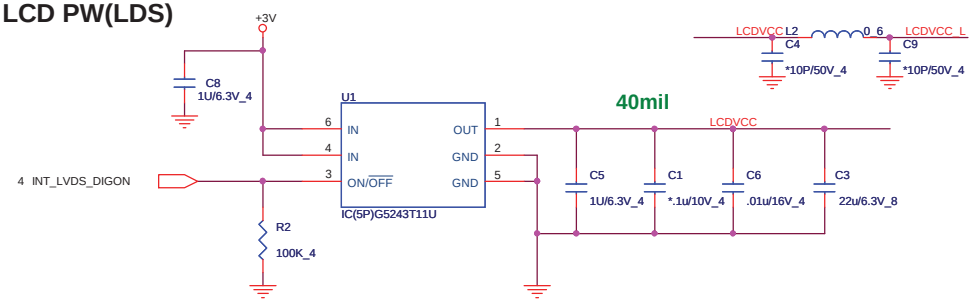
13



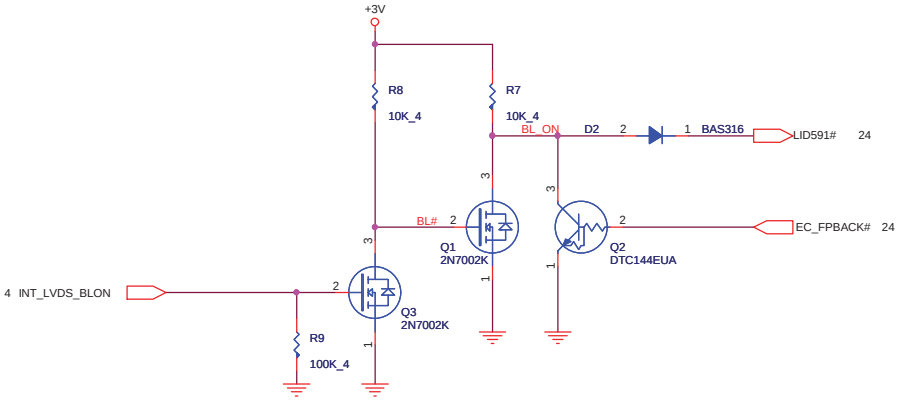
LVDS(LDS)



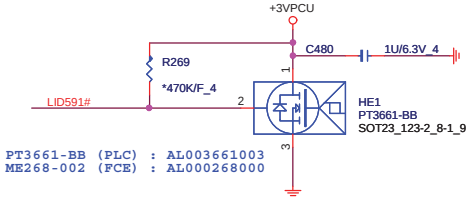
LCD PW(LDS)



Backlight Control(LDS)



Lid Switch (HSR)



PT3661-BB (PLC) : AL003661003
ME268-002 (FCE) : AL000268000

http://hobi-elektronika.net

PROJECT : ZQP
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Size	Document Number	Rev
	CRT/LVDS/LID	1A
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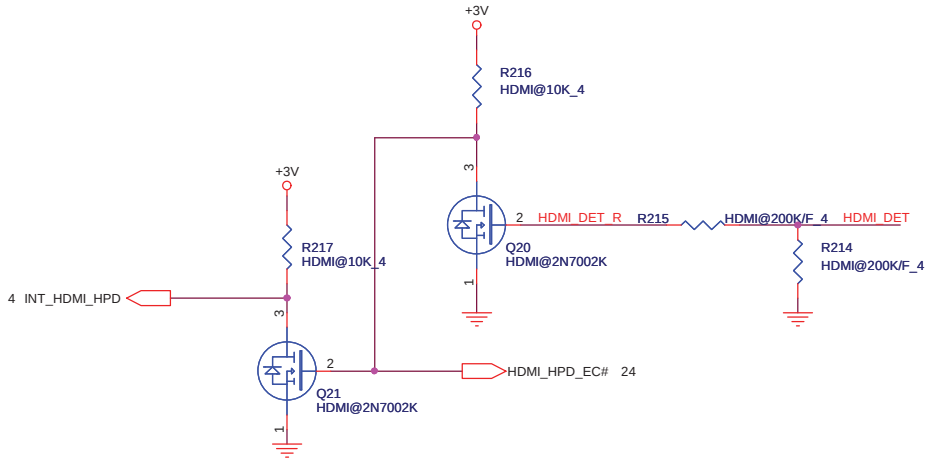
HDMI SDVO I2C Control

4 HDMI_DDCDATA
4 HDMI_DDCCLK
HDMI_DDCDATA
HDMI_DDCCLK

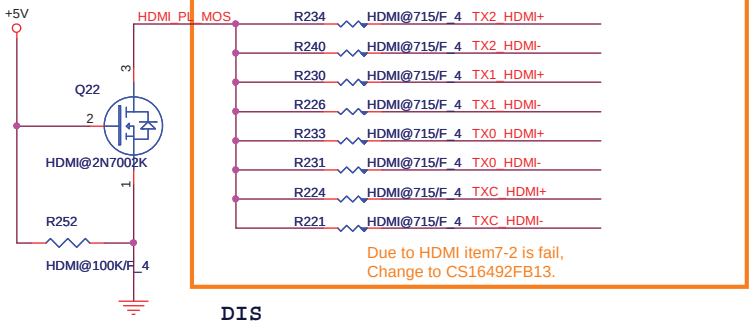
HDMI HPD SENSE (HDM)

UMA use +3V for the detect pin
Dis use +3V_DELAY for the detect pin



HDMI (HDM)

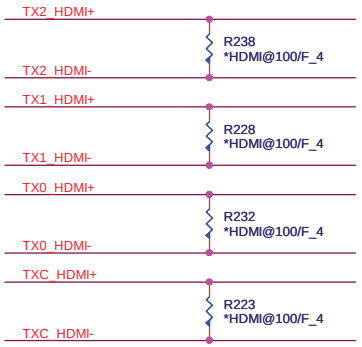
Close to HDMI Connector



DIS
Stuff 499 ohm CS14992FB24

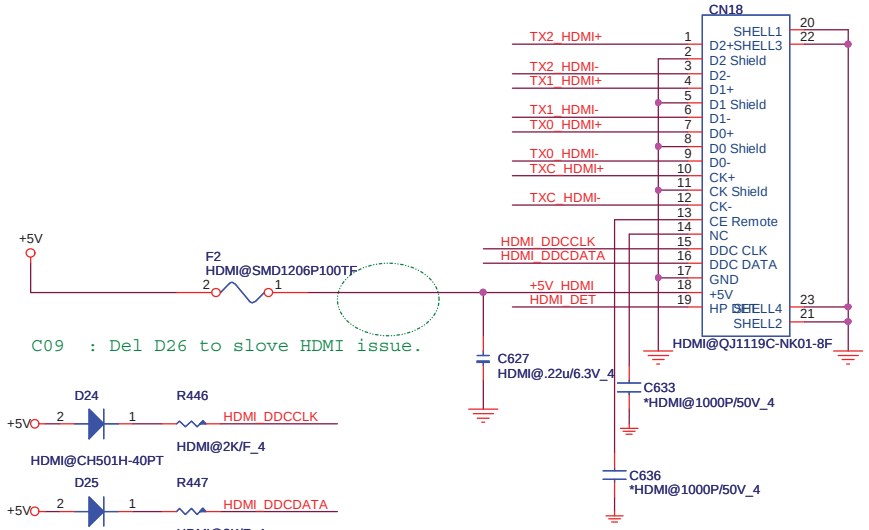
EMI reserve for HDMI(EMC)

Close connector



Added HDMI function
01/19 REV:B

HDMI PORT (HDM)



C09 : Del D26 to slove HDMI issue.

PROJECT : ZQP
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Size	Document Number	Rev
	HDMI	1A
Date: Tuesday, March 15, 2011	Sheet 14 of 32	

LAN (LAN)

<BOM note>
If center tap power come from internal switch regulator
=>Stuff 52SWR@ (Default)
If center tap power come from internal LDO
=>Stuff 52LDO@

<Layout note>
Close to Pin1

If use LDO mode L55 no stuff

L55 4.7uH/1A DCR:0.15ohm
C615 0.1U/16V_4
C616 10U/10V_8
Modify 01/06
VDDCT
VDDCT_REG R35 *52LDO@0/J_6
C37 0.1U/16V_4
C48 *52LDO@1U/10V_4

C365 33P/50V_4
C364 33P/50V_4
Y2 25MHz-LAN
XTLO_LAN
XTLI_LAN

BG625000486

Add R28/D4 for 家電下鄉
01/13

U4 *H@UCLAMP2512T.TCT
U5 *H@UCLAMP2512T.TCT
X-TX1N X-TX1P X-TX0N X-TX0P
TX1N TX1P TX0N TX0P

* Why does Pin17 CLKREQn connect to Pin16(LED2) and Pin30(DVDDL)?

Power Sequence:
VDD33 to PERSTn >= 100ms

76.1mA ; 30mil
<Layout note>
Close to Pin2
+3V_S5 +3V_LAN
R195 0/J_6
C353 10U/10V_8
C366 1U/10V_4
C361 0.1U/16V_4
* Int. PU in SB

U9 AR8158 4X4mm 32Pin QFN
AR8158-BL1A-RL

LX 40mil
8,16,18,24 PLTRST#
9,24 PCIE_WAKE#
VDDCT_REG 20mil
VDDCT 20mil
AVDDL 20mil
AVDDH 20mil
XTLO_LAN XTLI_LAN
R203 2.37K/F_4 RBIAS
TX0P TX0N TX1P TX1N
PCIE_REQ_LAN# R506 *0/J_4

C373 0.1U/16V_4
C618 1U/10V_4
C624 0.1U/16V_4
C368 1U/10V_4
C367 0.1U/16V_4

<Layout note>
Close to LAN Chip
1nF reserved for EMI
RN2 49.9/F_4P2R
RN1 49.9/F_4P2R
C29 0.1U/16V_4
C33 *1000P/50V_4
C66 0.1U/16V_4
C35 *1000P/50V_4

PU in CLK Gen.
CLKREQn R485 0/J_4 R505 *0/J_4 DVDDL PCIE_REQ_LAN# 9
SMCLK SMBUS for debug only
SMDATA
TESTMODE
C406 0.1U/16V_4
NC
TX_N PCIE_RXN0 C407 .1U/10V_4 PCIE_RXN0_LAN 8
TX_P PCIE_RXP0 C408 .1U/10V_4 PCIE_RXP0_LAN 8
AVDDL
REFCLK_N CLK_PCIE_LANN 8
REFCLK_P CLK_PCIE_LANP 8
C621 0.1U/16V_4
RX_P PCIE_TXP0_LAN 8
RX_N PCIE_TXN0_LAN 8
C622 0.1U/16V_4
DVDDL_REG DVDDL 20mil
LED[0] LAN_ACTLED
LED[1] Del LED
GND1
C397 0.1U/16V_4
C393 1U/10V_4

Add R29
01/13
R29 5.1K/J_8 LAN_ACTLED
Active LED Pin:
Non-overclocking=>active high

+3V_S5 → VDD33 (2)
+1.1V analog power → AVDDL (24/27)
+1.7V analog power → VDDCT (6)

ATHEROS AR8158

AVDDL_REG (7) +1.1V regulator output (For all the analog 1.1V supply pins)
AVDDH_REG (10) +2.7V regulator output
DVDDL_REG (30) +1.1V regulator output (For all the digital 1.1V supply pins)
VDDCT_REG (5) +1.8V regulator output (For VDDCT when LDO mode)
LX (1) +1.7V Switching regulator (For VDDCT when switching mode)

TRANSFORMER (LAN)

exchange pair 0/1
0110

U22 NS0014LF_Bothhand
VDDCT L54 0/J_6 CX8EG601000: 0.5A/600ohm_6
AVDD_CEN
C613 0.1U/16V_4
C363 *1000P/50V_4
C394 0.1U/16V_4
C357 *1000P/50V_4
C356 *1U/6.3V_4
1nF reserved for EMI
TX1N TX1P TX0N TX0P
X-TX1N X-TX1P TERM0 TERM1 X-TX0N X-TX0P
R28 *H@1M_8
*H@B88069X9231T2032
D4
R199 75/F_8
R196 75/F_8
C354 220P/3KV_1808
TERM9

Add R28/D4 for 家電下鄉
01/13

change C354 to CH122GK1I10 for EMI
02/16 REV:B

TX0P EC38 6.8p/50V_4
TX0N EC40 6.8p/50V_4
TX1P EC43 6.8p/50V_4
TX1N EC46 6.8p/50V_4

Add EC38,EC40,EC43,EC46 for EMI
02/16 REV:B

Del 0110

RJ45 Connector (LAN)

Del LAN LED 01/05

CN15 RJ45
YELLOW_N YELLOW_P GREEN_N GREEN_P
X-TX0P X-TX0N X-TX1P TERM9 X-TX1N TERM9
GND2 GND1
LAN_GND_2 R31 V-PORT-0603-220K
LAN_GND_1 R32 V-PORT-0603-220K
chenge to ESD
01/18 REV:B

change RJ45 connector without LED
03/02

We will change RJ45 connector

http://hobi-elektronika.net

PROJECT : ZQP
Quanta Computer Inc.

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	LAN AR8158L	1A
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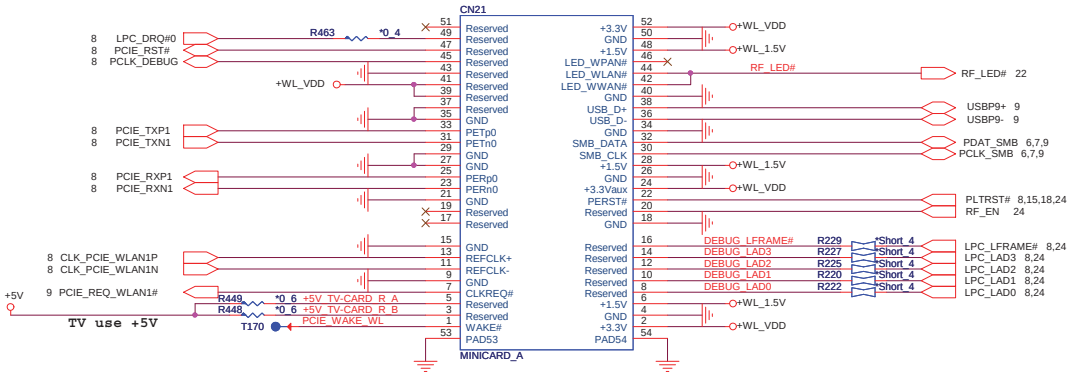
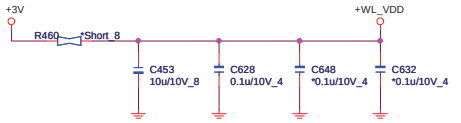
MINI-CARD WLAN(MPC)

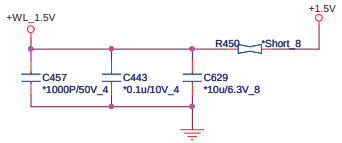
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

Check LED signal. (active high or low)



Debug



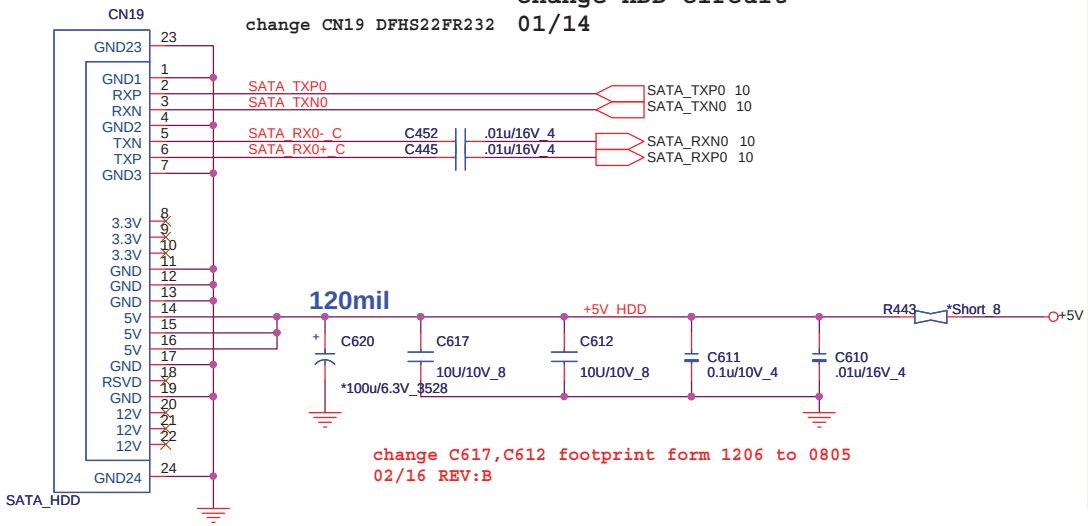


PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	MINI PCI-E card	1A
Date: Tuesday, March 15, 2011	Sheet 16 of 32	

SATA HDD

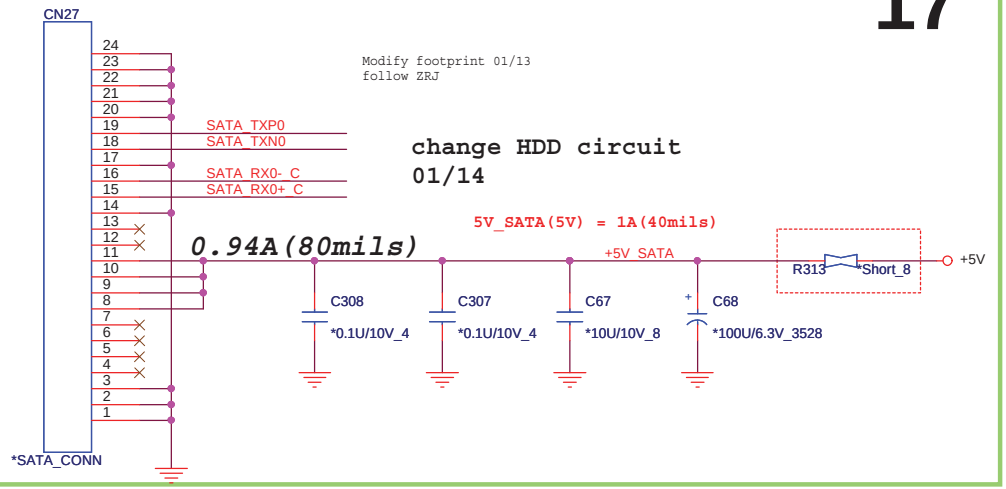
change HDD circuit
change CN19 DFHS22FR232 01/14



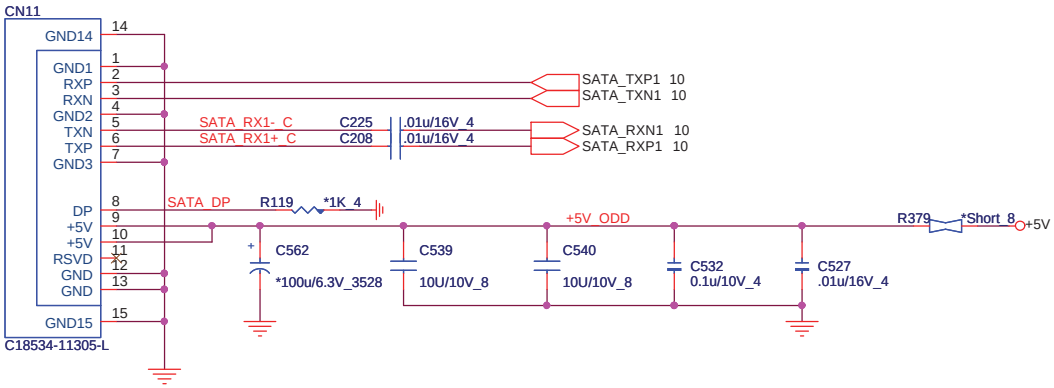
change C617,C612 footprint form 1206 to 0805
02/16 REV:B

SATA HDD(HDD)

17



SATA ODD



change C539,C540 footprint form 1206 to 0805
02/16 REV:B

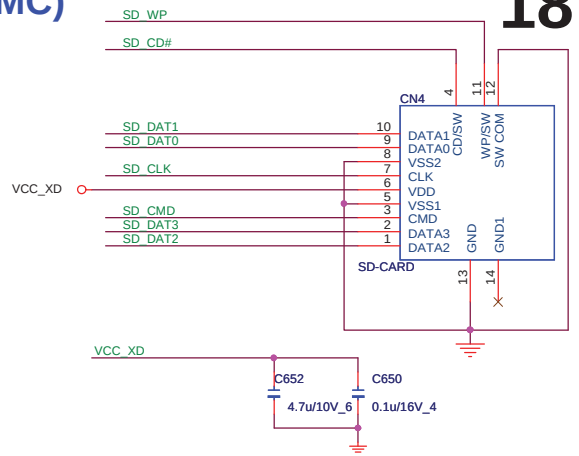
PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	SATA-HDD/ODD/HOLE	1A
Date: Tuesday, March 15, 2011	Sheet 17 of 32	

CARD READER Controller
AU6435-GDL

2 IN 1 CARD READER (SD/MMC)

Main	DFHS11FR011
Second	DFHS11FR033



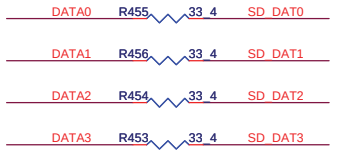
Close to CN14 pin 14 & pin23
4.7u CAP close to pin23

PIN45=Clock input selection
'1' for 48MHz input [Default,Internal PU]
'0' for 12MHz input

PIN43=Power saving mode enable.
'1' for enable [Default]
'0' for disable

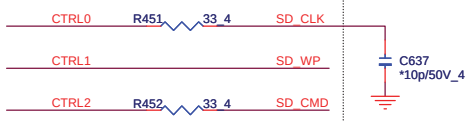
CTRL0, CRTL 1 trace length shorter , and surround with GND.

The trace length difference for each card interfaces should be smaller than 500 mil

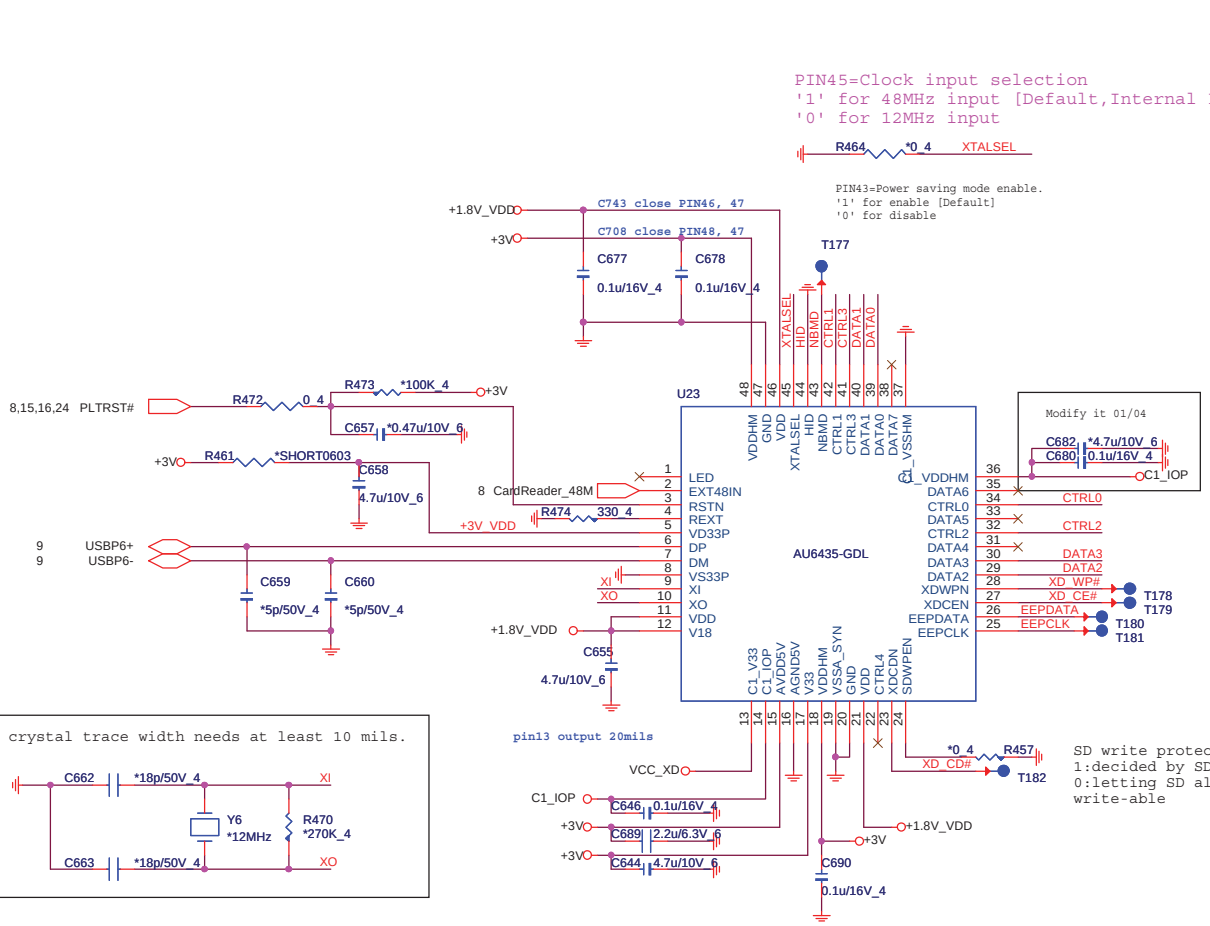


Close to connector

CLK length should be as short as possible. Shorter than 1200 mil is good.



change R452 from CTRL1 to CTRL2
01/13



PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	AU6435 CardReader	1A
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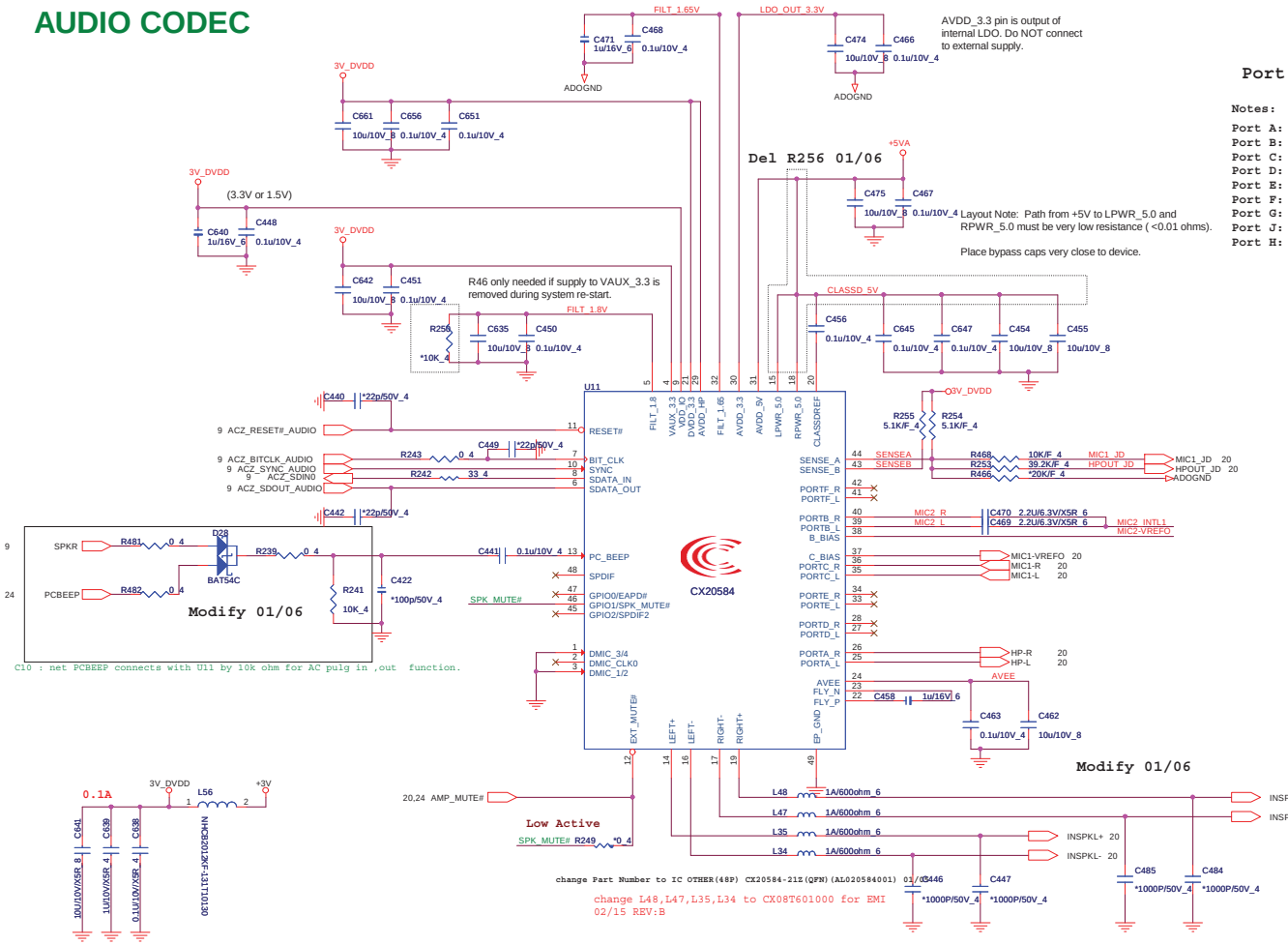
AUDIO CODEC



1. The VDD_IO and VAUX_3.3 pins should be connected to same power supply domain as HDA bus controller so that the HDA controller and codec bus interface will power-up at the same time. This will avoid bus leakage issues if using HDA controller with bus pull-up strap options. See other FET option on this page if these supplies are not on same domain as HDA controler.

2. To support Wake-on-Jack, the codec VAUX_3.3 pin must be powered from a Standby supply.

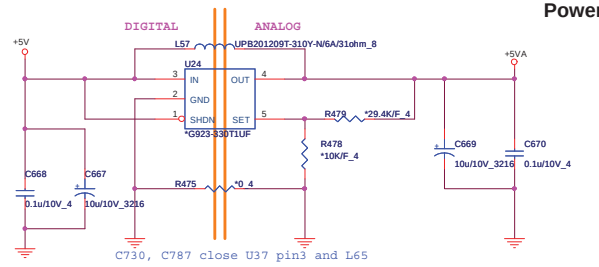
3. C309, C310, C311 are optional.
Do not install unless needed for EMI/SI.

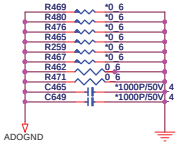
Port Configuration

Notes:

Port A: Headphone jack (jack shared with S/PDIF)
Port B: Internal MIC (mono or stereo)
Port C: Microphone/LI/LO jack
Port D: Line Out jack (Optional)
Port E: Line In jack (Optional)
Port F: Not used.
Port G: Internal stereo speakers
Port J: Internal stereo digital mic (Optional)
Port H: S/PDIF (jack shared with headphone)

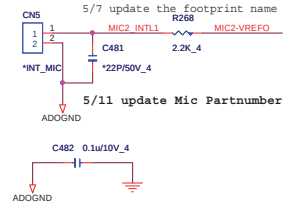
Power (ADO)





Tied at one point only under the codec or near the codec

INT MIC array



cap place close to MIC-connector

PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	CONEXANT 20584	1A
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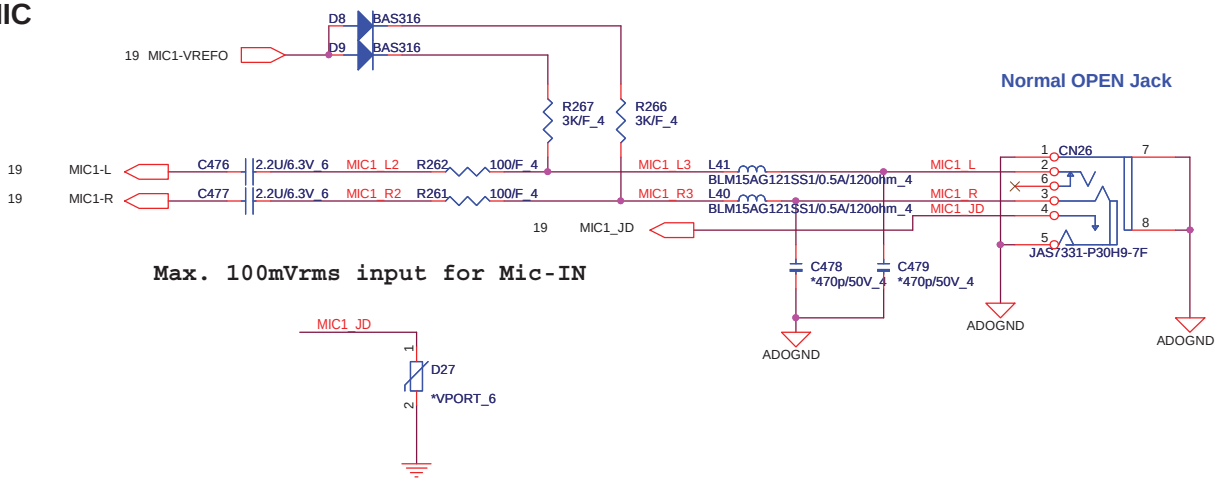
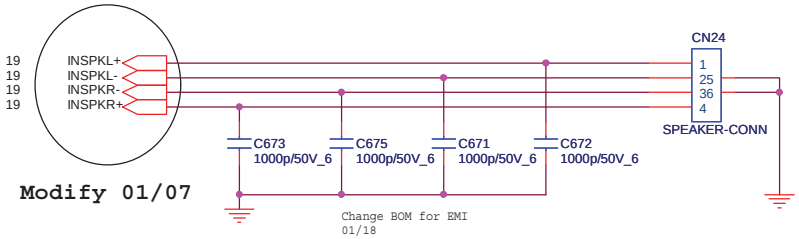
MIC

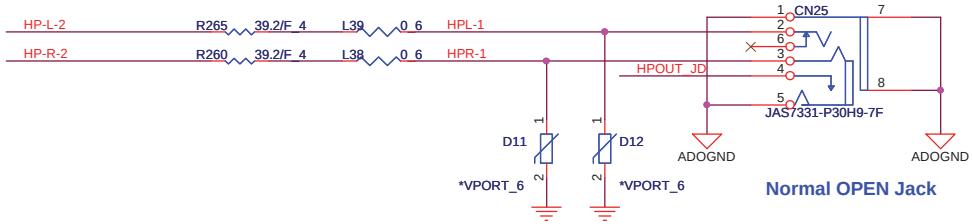


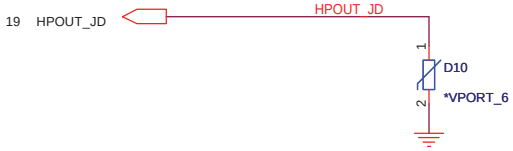
Internal Speaker

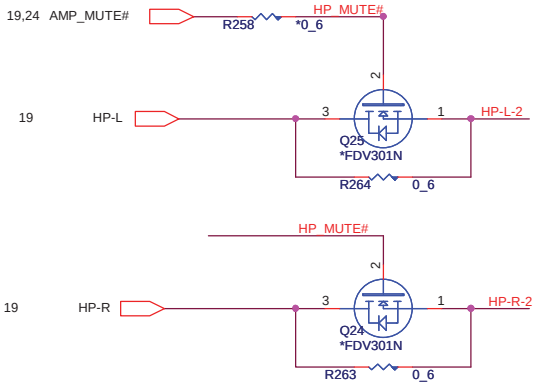


change C673,C675,C671,C672 for EMI
02/15 REV:B

HP







PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	AUDIO JACK CONN	1A
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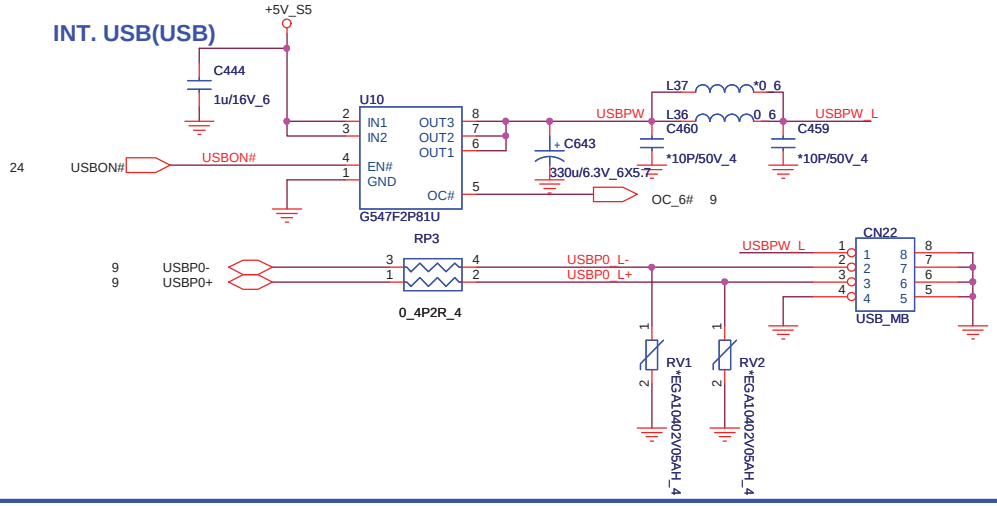
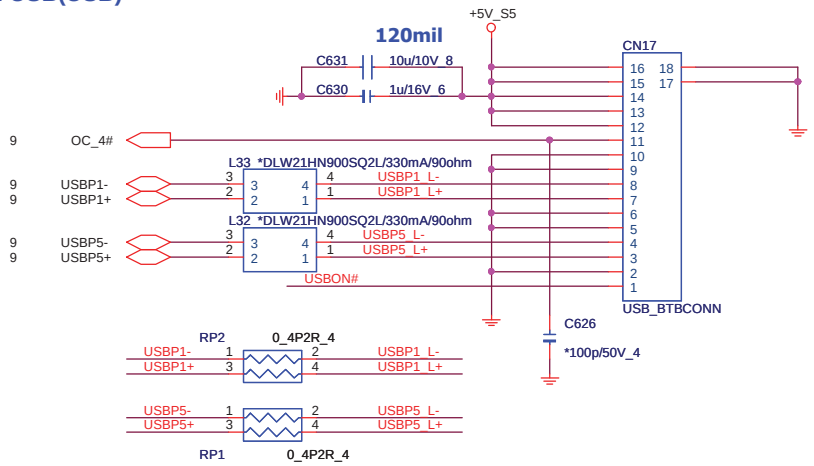
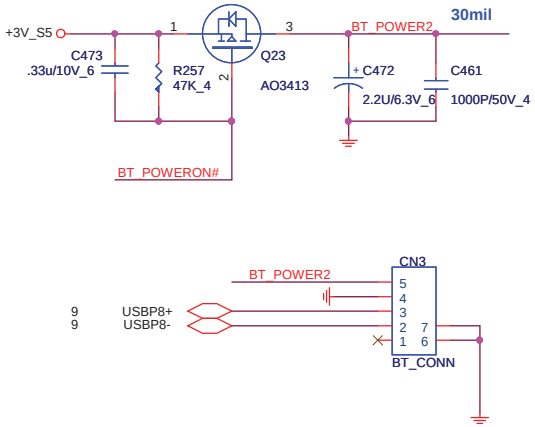
INT. USB(USB)



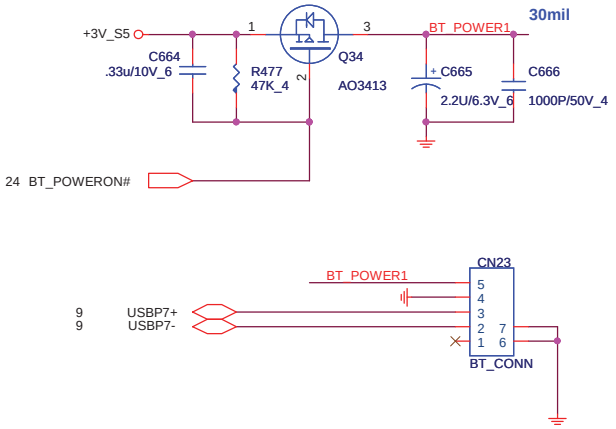
EXT. USB(USB)



BLUETOOTH V2.1 CONN(BTM)

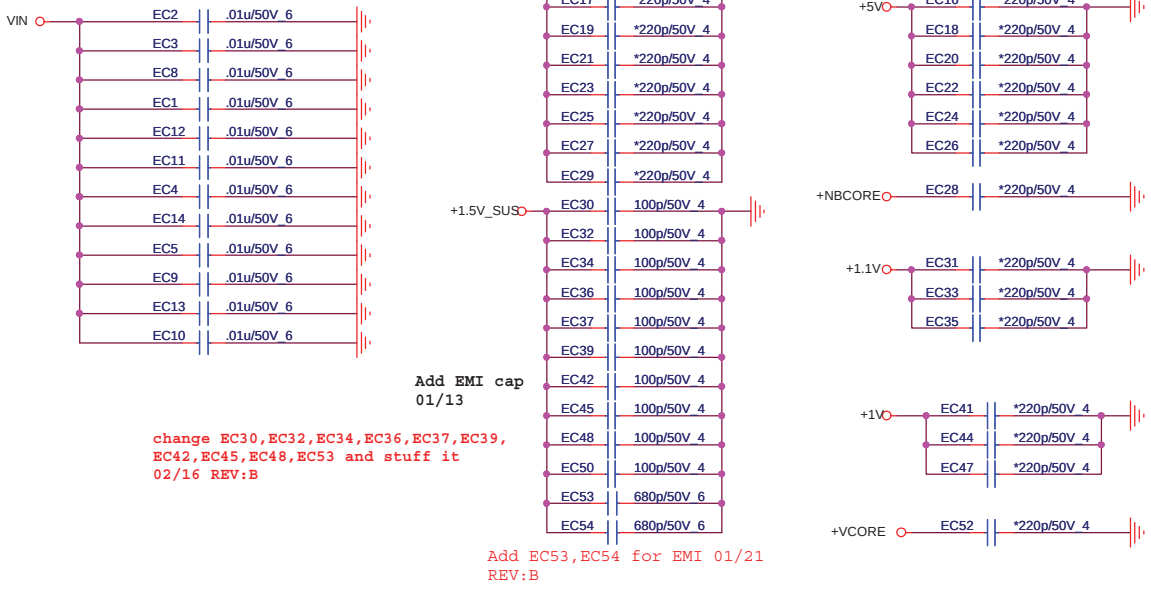


BLUETOOTH V3.0 CONN(BTM)



PROJECT : ZQP Quanta Computer Inc.		
Size	Document Number **USB/BT**	Rev 1A
Date: Tuesday, March 15, 2011	Sheet 21 of 32	

EE RETURN-PATH CAPACITORS(EMC)



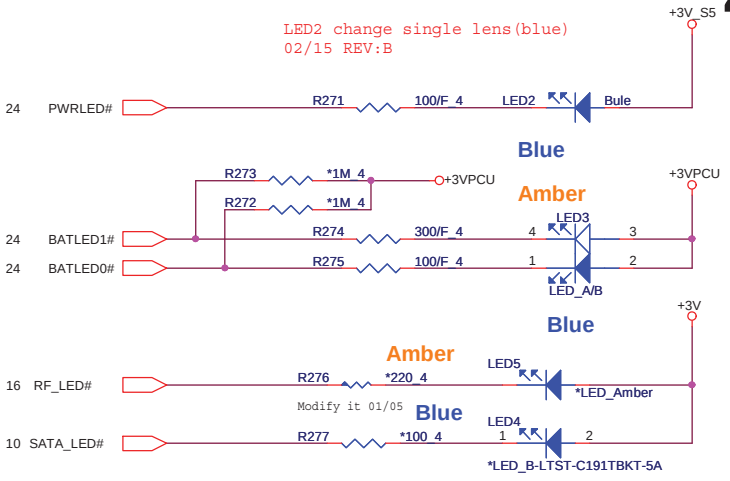
Add EMI cap
01/13

change EC30,EC32,EC34,EC36,EC37,EC39,
EC42,EC45,EC48,EC53 and stuff it
02/16 REV:B

Add EC53,EC54 for EMI 01/21
REV:B

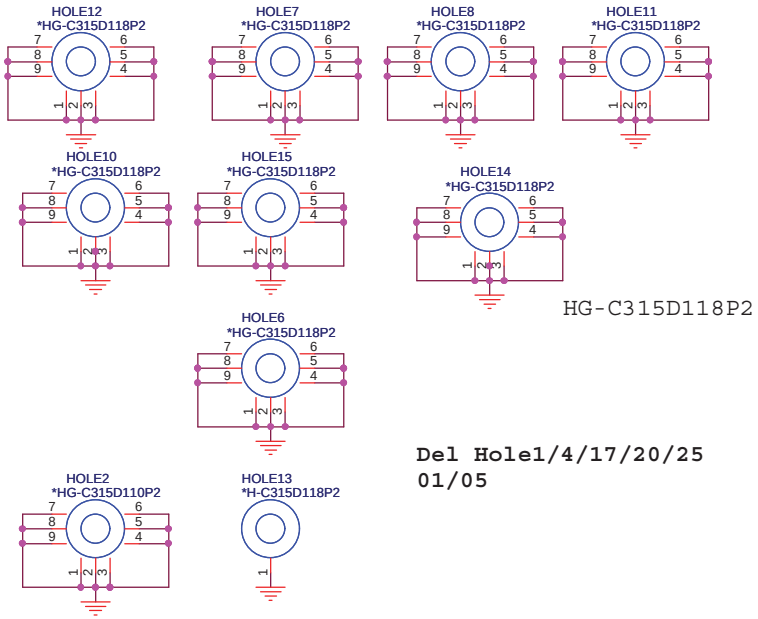
LED(UIF)

LED2 change single lens(blue)
02/15 REV:B



Del it 01/05

HOLE(OTH)

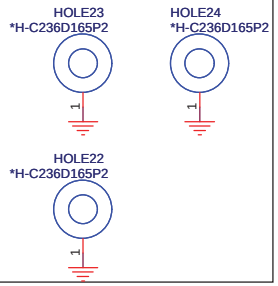


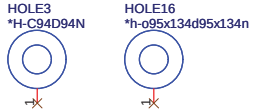
HG-C315D118P2

Del Hole1/4/17/20/25
01/05

mini PCI

cpu





No stuff HOLE9
REV:B 02/17

CPU nut PN : FBBU1001010 x 3 @ SHOLE1~3

PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	LED/ EMI/ Screw Hole& Nut	1A
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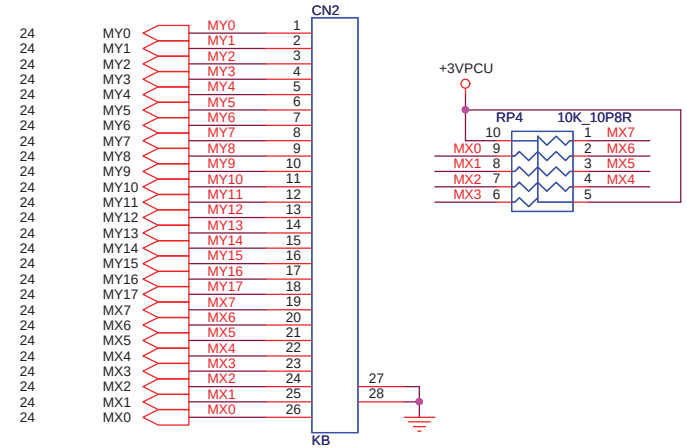
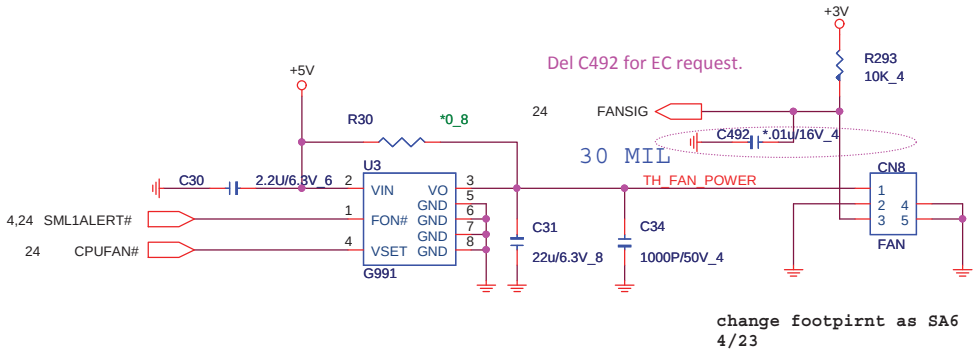
K/B(KBC)

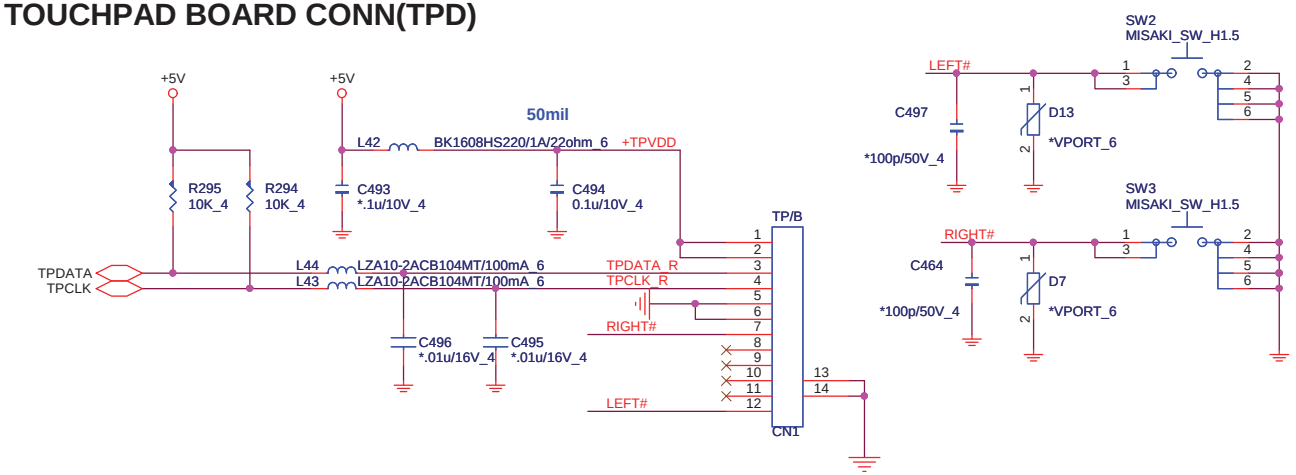


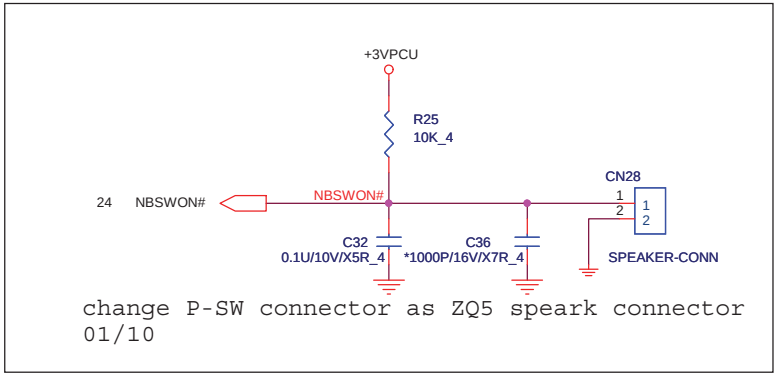
CPU FAN(THM)



change footpirnt as SA6
4/23

TOUCHPAD BOARD CONN(TPD)





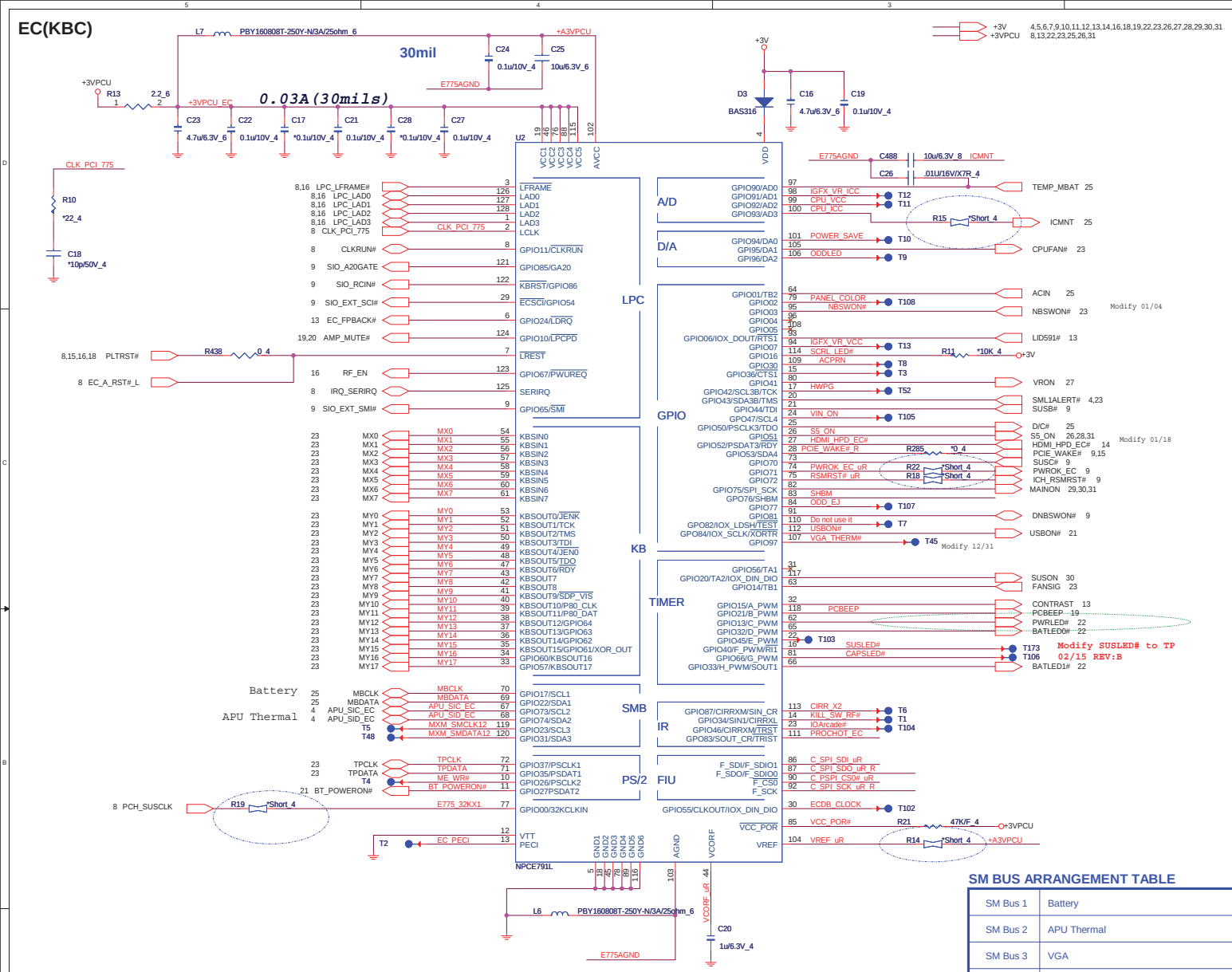
change P-SW connector as ZQ5 speark connector
01/10

DFFC12FR234 will be EOL by PDC , so change PN to DFFC12FR026

PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	KB/TP/FAN	1A
Date: Tuesday, March 15, 2011	Sheet 23 of 32	

EC(KBC)



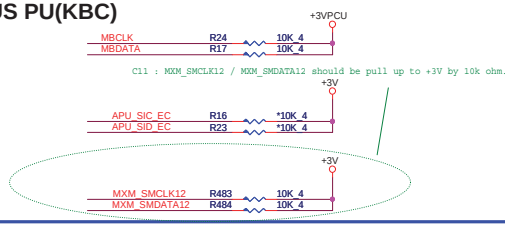
SM BUS ARRANGEMENT TABLE

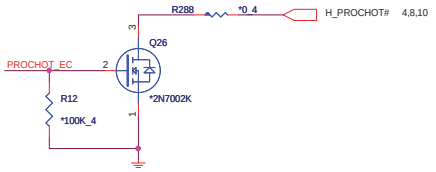
SM Bus 1	Battery
SM Bus 2	APU Thermal
SM Bus 3	VGA

I/O ADDRESS SETTING(KBC)

Disable (non share SPI ROM) : no external PU resistor
enable (share SPI ROM) : 10Kohm external PD resistor

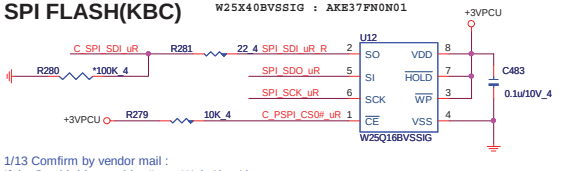
SM BUS PU(KBC)





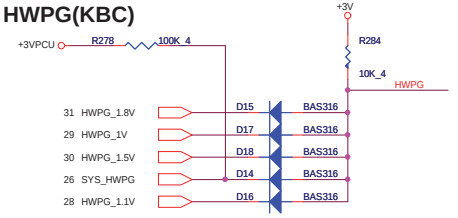
SPI FLASH(KBC)

socket : DG008000031
W25X40BVSSIG : AKE37FN0N01

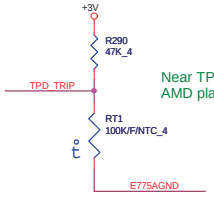


1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by
default, the flash device should be 50MHz (or faster)

HWPG(KBC)



PALM REST THERMAL SENSOR (THM)



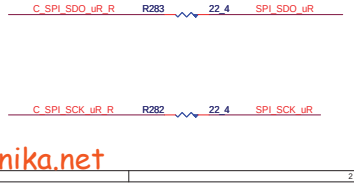
Near TP on TOP side and only for
AMD platform Palm Rest use.

(02/25)
Per QSMC SMT request, change to
Mitsubishi.
Main: CU4100B0000
Second: CU410000Z07 (MIT)

POWER-ON SWITCH (KBC)

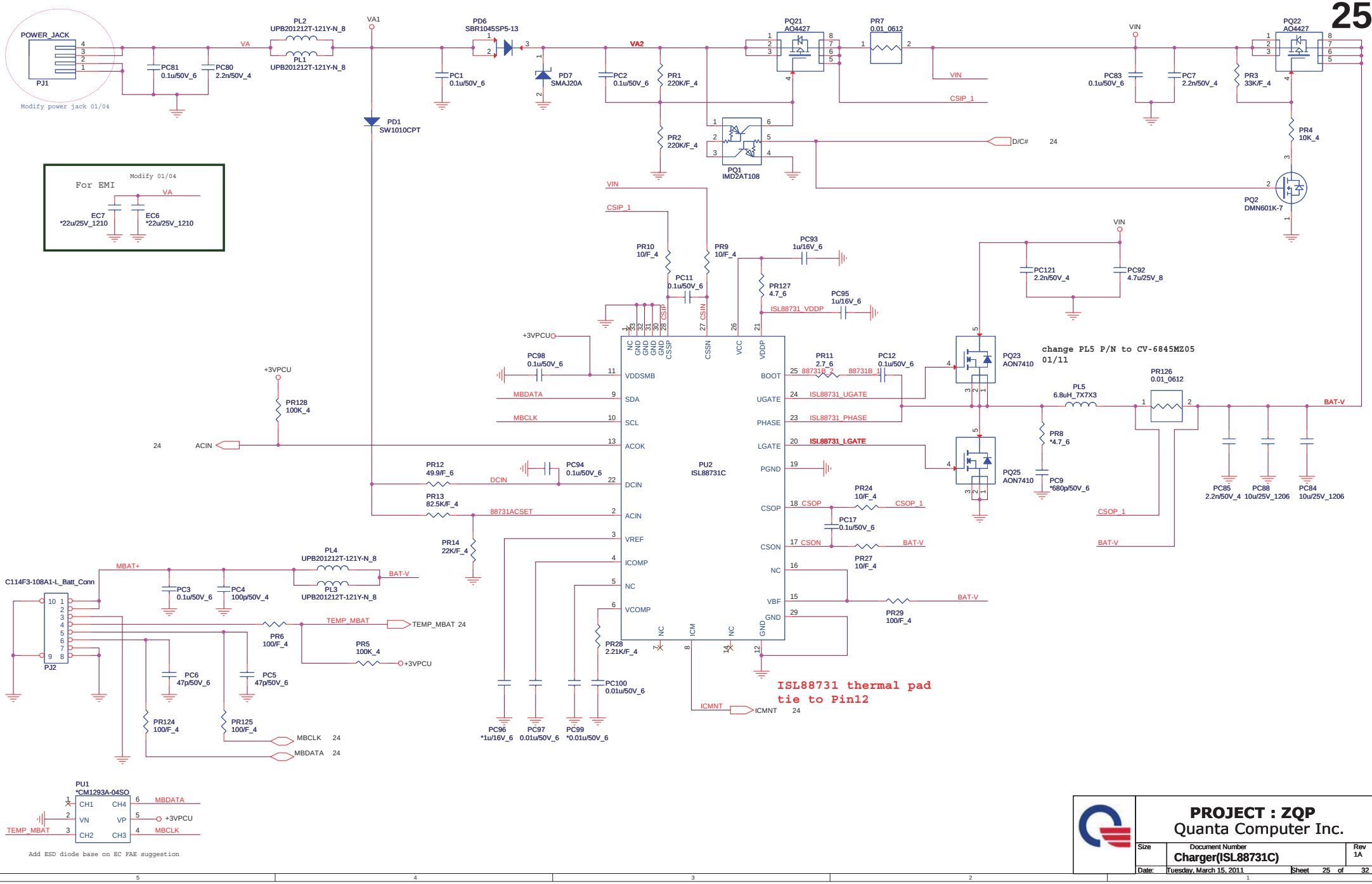
Del SW1,stuff D1
02/15 REV:B

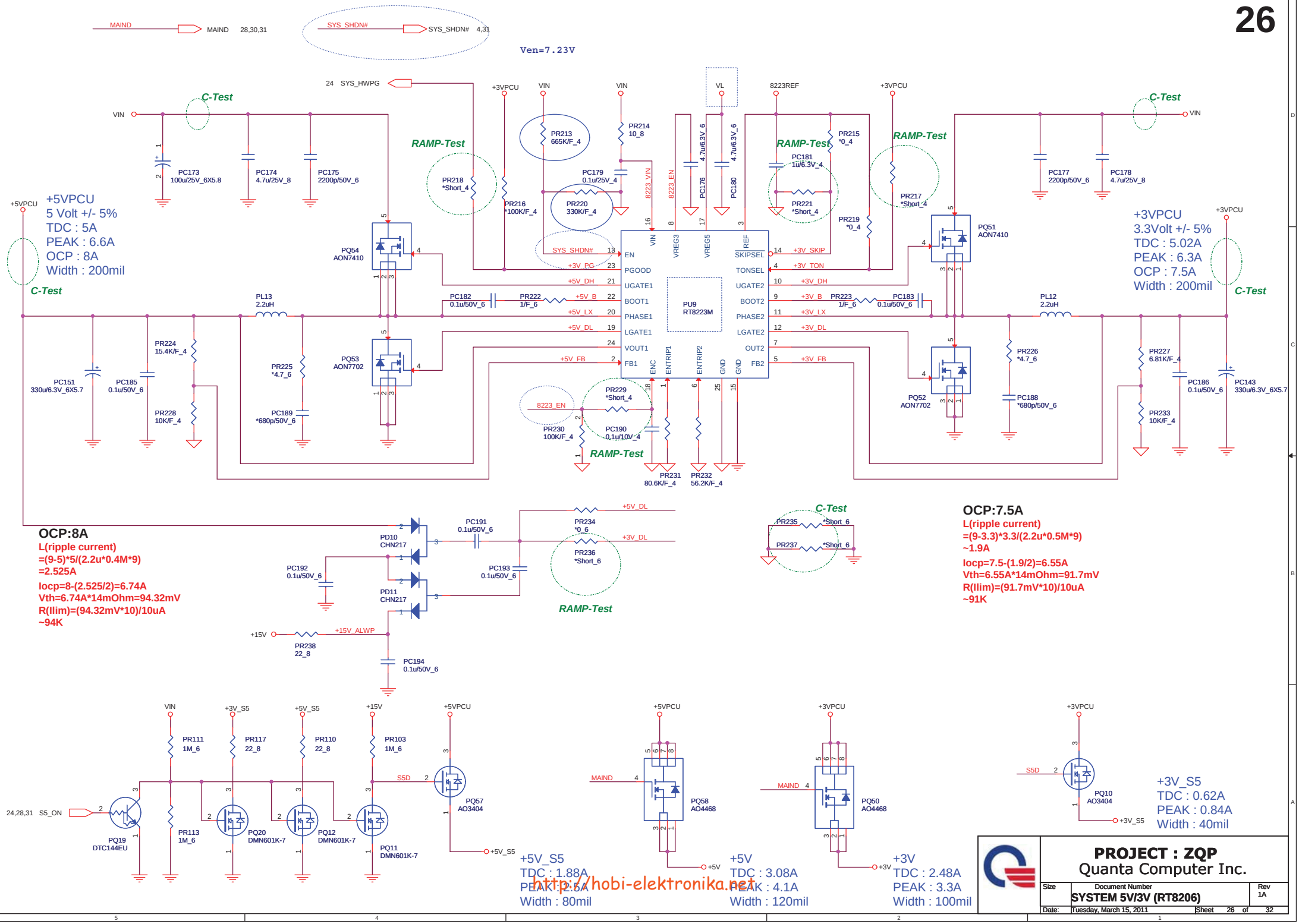
Add D5 for ESD
02/15 REV:B



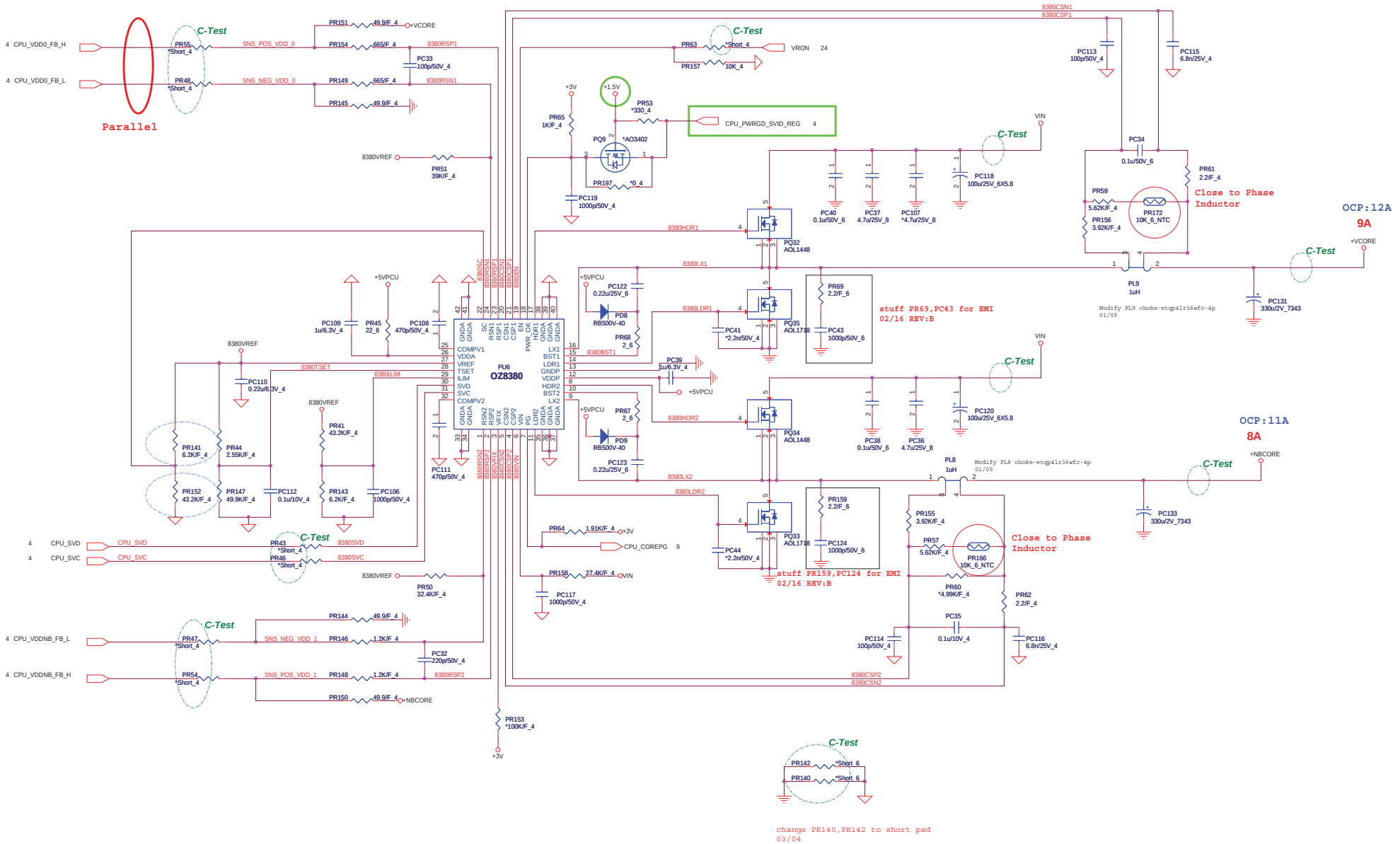
PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	WPCE791 & FLASH	1A
Date: Tuesday, March 15, 2011	Sheet 24 of 32	





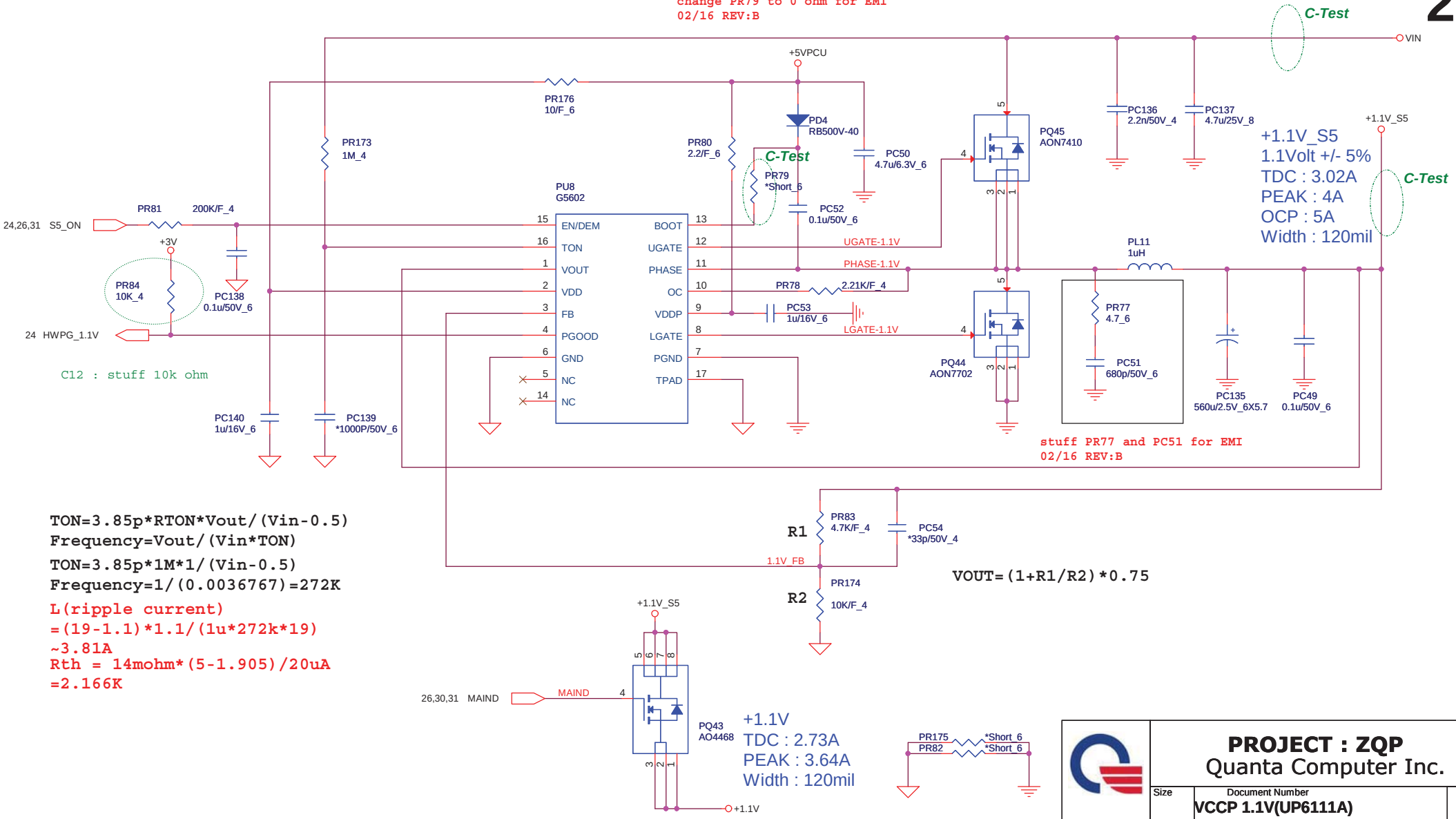
PROJECT : ZQP		
Quanta Computer Inc.		
Size	Document Number: SYSTEM 5V/3V (RT8206)	Rev: 1A
Date: Tuesday, March 15, 2011	Sheet 26 of 32	



http://hobi-elektronika.net

	PROJECT : ZQP Quanta Computer Inc.	
Size	Document Number CPU Core (OZ8380)	Rev 1A
Date: Tuesday, March 15, 2011	Sheet 27 of 32	

change PR79 to 0 ohm for EMI
02/16 REV:B



TON=3.85p*RTON*Vout/(Vin-0.5)
Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)
Frequency=1/(0.0036767)=272K

L(ripple current)
=(19-1.1)*1.1/(1u*272k*19)
~3.81A
Rth = 14mohm*(5-1.905)/20uA
=2.166K

PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	VCCP 1.1V(UP6111A)	1A
Date: Tuesday, March 15, 2011	Sheet 28 of 32	

change PR76 to 0 ohm for EMI
02/16 REV:B

C13

change PR169 PN from 0ohm to 430kohm for timing issue

C14 : stuff 10k ohm

C-Test

+1V
1Volt +/- 5%
TDC : 4.3A
PEAK : 5.7A
OCP : 7A
Width : 180mil

stuff PR164,PC126 for EMI
02/16 REV:B

VOUT=(1+R1/R2)*0.75

C15 : change PR75 value from 3.57k to 3.65k
PR75-->4.02K for
1333MHz,1.05V

TON=3.85p*RTON*Vout/(Vin-0.5)
Frequency=Vout/(Vin*TON)
TON=3.85p*1M*1/(Vin-0.5)
Frequency=1/(0.0036767)=272K

L(ripple current)
=(19-1)*1/(1u*272k*19)
~3.483A
Rth=14mohm*(10-1.741)/20uA
=3.68Kohm

PROJECT : ZQP Quanta Computer Inc.		
Size	Document Number +1V(G5602)	Rev 1A
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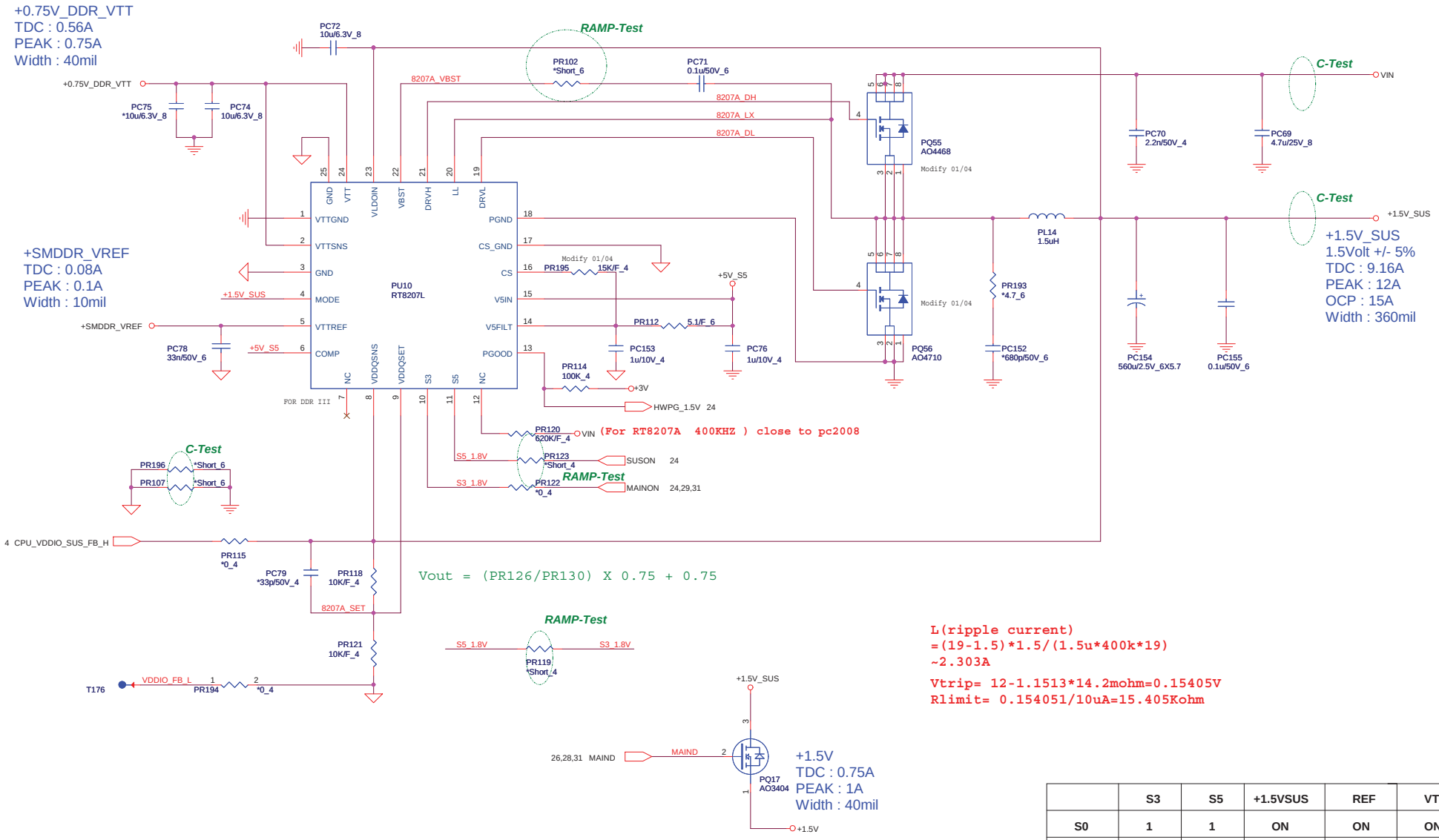

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A
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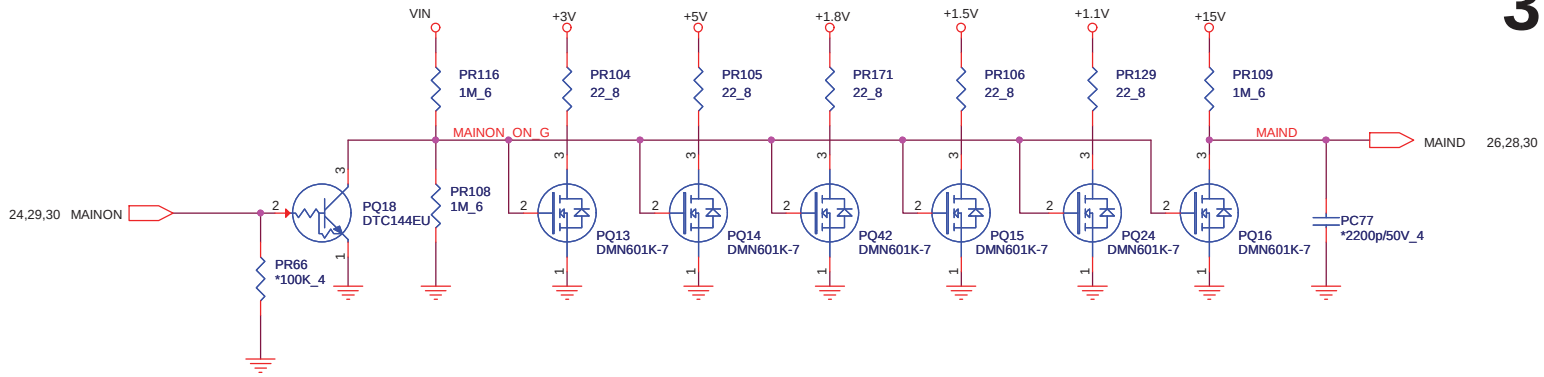
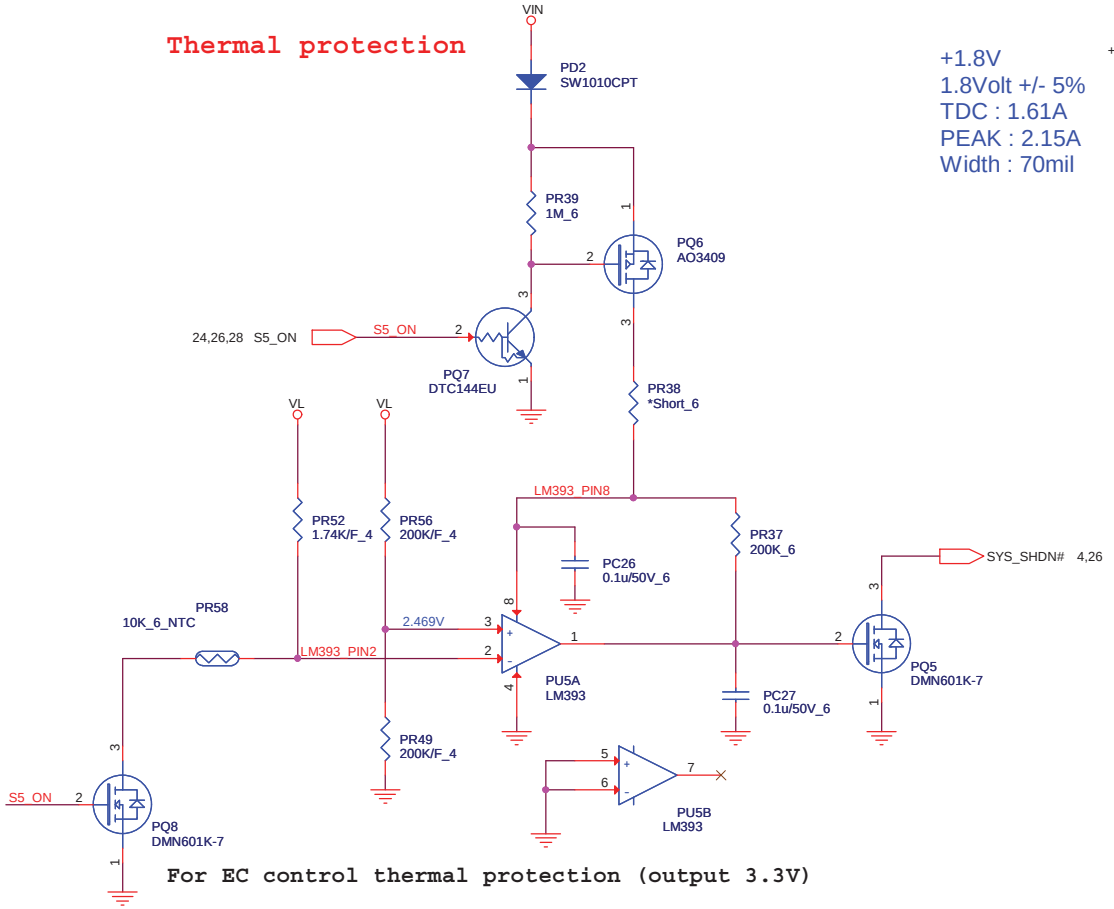
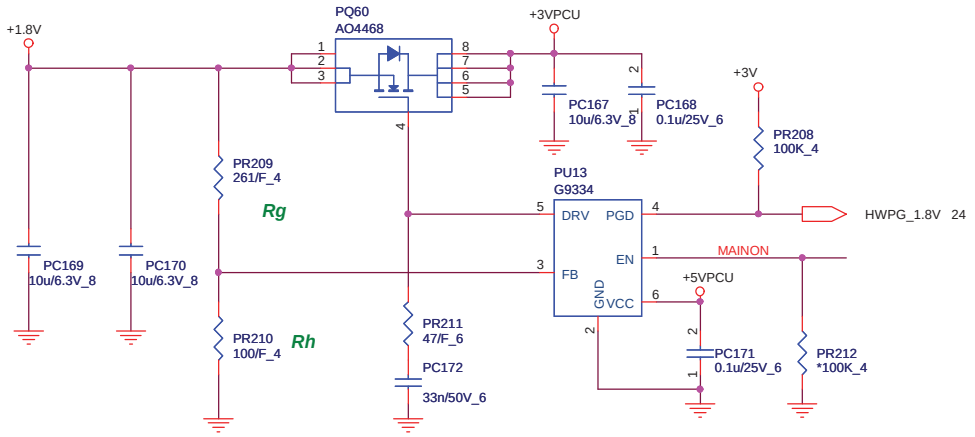


Thermal protection



For EC control thermal protection (output 3.3V)

+1.8V
1.8Volt +/- 5%
TDC : 1.61A
PEAK : 2.15A
Width : 70mil



*Vout1 = (1+Rg/Rh)*0.5*

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	Discharge /Thermal protection	1A
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MODEL	REV	CHANGE LIST
ZQP/Q M/B	A	First Release
	B	01.P14: Add HDMI function 02.P22: Add EC53,EC54 for EMI 03.P20: Stuff C673/C675/C671/C672 for EMI 04.P15: Stuff ESD protector at R31/R32 for EMI 05.P10: GPIO 58 define to HDMI strap pin 06.P08: Add C606,C614,C619 for strong clock 07.P20:change C673,C675,C671,C672 for EMI 08.P19:change L48,L47,L35,L34 to CX08T601000 for EMI 09.P24:No stuff SW1,stuff D1 10.P24:Add D5 on S5_ON for ESD 11.P22:LED2 change single lens(blue) 12.P08:Del C623 13.P24:Del SW1 14.P13:Del R26,R27 and add RP5 for EMI 15.P15:Add EC38,EC40,EC43,EC46 for EMI 16.P28:change PR79 to 0 ohm and stuff PR77 and PC51 for EMI 17.P29:change PR76 to 0 ohm and stuff PR164,PC126 for EMI 18.P27:stuff PR69,PC43 for EMI 19.P17:change C617,C612,C539,C540 footprint form 1206 to 0805 20.P13:Swap USB nets between L50 and PR5 21.P13:Add R33,R34 for ESD 22.P15:change C354 to CH122GK1I10 for EMI 23.P22:change EC30,EC32,EC34,EC36,EC37,EC39,EC42,EC45,EC48,EC53 and stuff it for EMI 24.P26:Remove JP20,JP21,JP22,JP23 and change to short pad PR235,PR237 25.P27:Remove JP10,JP9,JP6,JP8 and change to short pad PR55,PR48,PR43,PR46,PR47,PR54,PR63,PR142,PR140 26.P28:Remove JP24,JP25 27.P29:Remove JP16,JP17 and change to short pad PR70,PR72 28.P30:Remove JP18,JP19 and change to short pad PR196,PR107 29.P22:No stuff HOLE9
	C	01.P15:change RJ45 connector without LED 02.P27:change PR140,PR142 to short pad 03.P30:change PR119,PR123,PR102 to short pad 04.P26:change PR217,PR218,PR221,PR229,PR236 to short pad 05.P29:change PR76 to short pad 06.P28:change PR79 to short pad

Model	ZQE/G M/B BOARD	
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8	1A	3A
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	CHANGE LIST - 3A	1A
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	APPROVED BY : Andy Lin	CHECK BY : JC Huang	DRAWING BY : Andy Chen	DATE :10/18/2010	SHEET 1