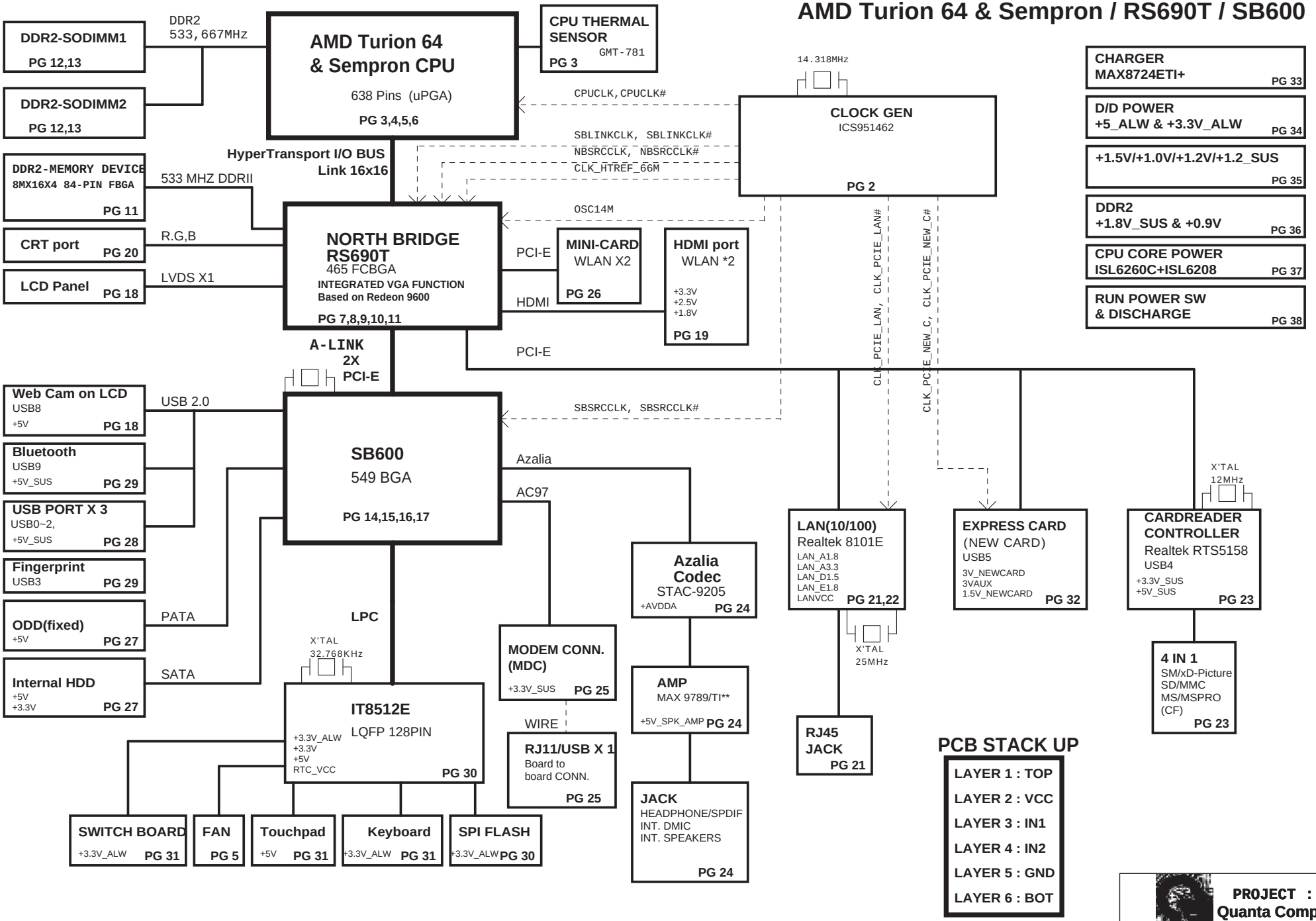
SA1A BLOCK DIAGRAM

AMD Turion 64 & Sempron / RS690T / SB600



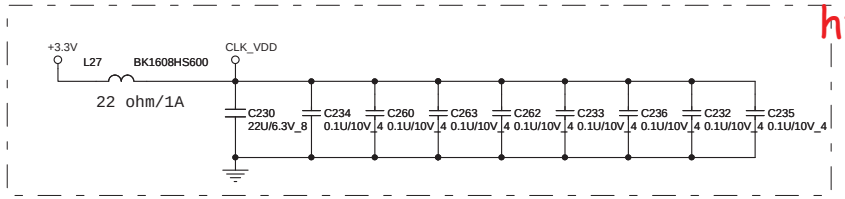
PCB STACK UP

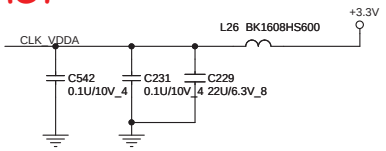
- LAYER 1 : TOP
- LAYER 2 : VCC
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : GND
- LAYER 6 : BOT

PROJECT : SA1A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	3A

Date: Thursday, January 31, 2008 Sheet 1 of 39



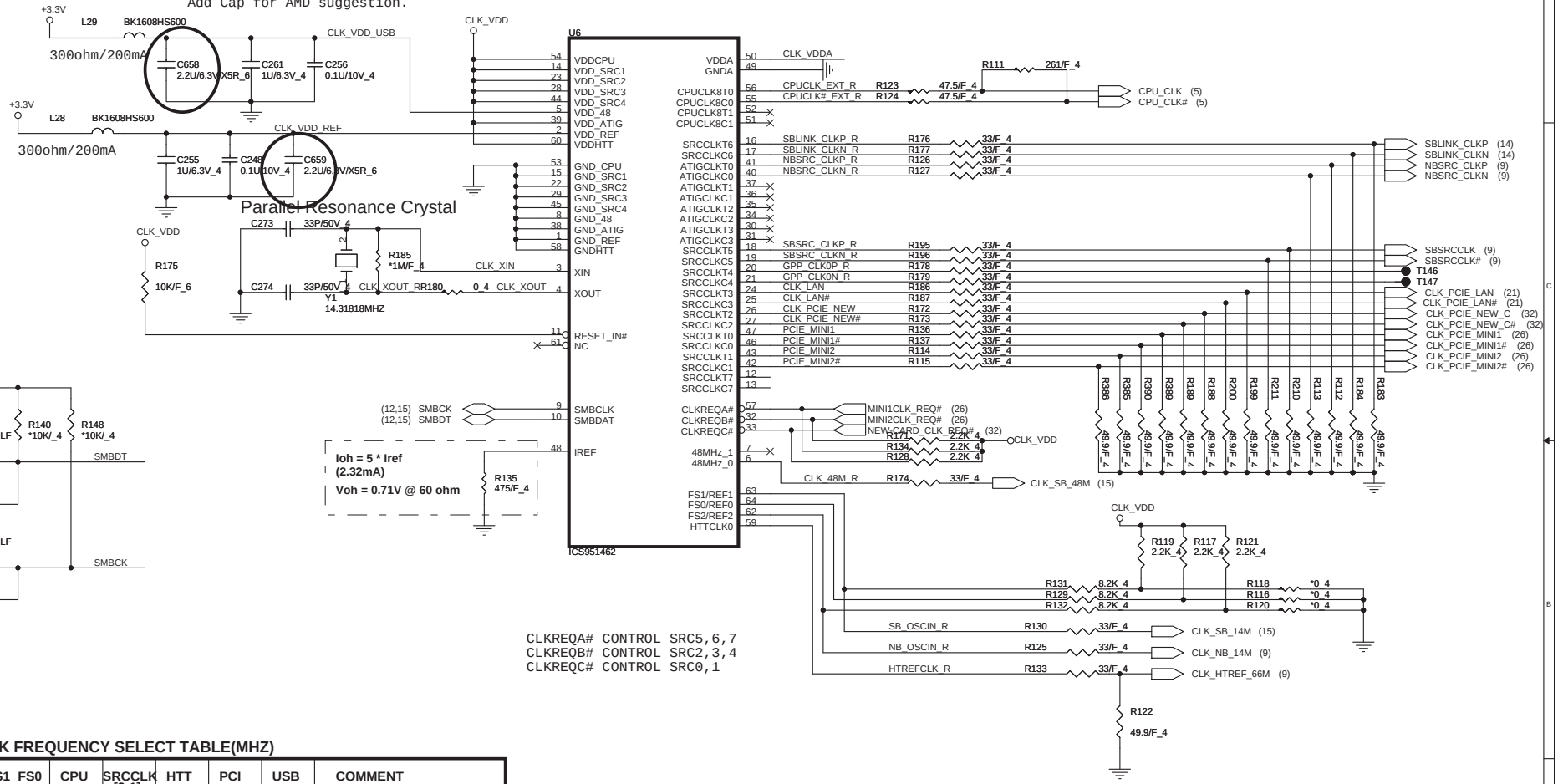


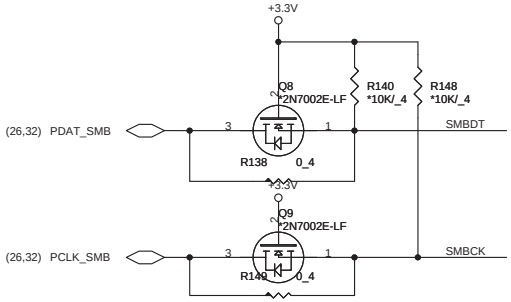
B01

Add Cap for AMD suggestion.

1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO U800

2- PUT DECOUPLING CAPS CLOSE TO Clock Gen.POWER PIN





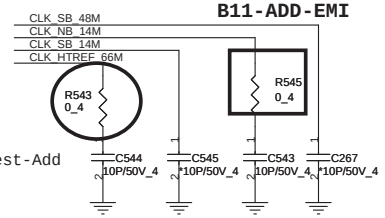
CLKREQA# CONTROL SRC5,6,7
CLKREQB# CONTROL SRC2,3,4
CLKREQC# CONTROL SRC0,1

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Normal ATHLON64 operation
1	1	1	200.00	100.00	66.66	33.33	48.00	Reserved

Check AMD clock

B11-ADD-EMI

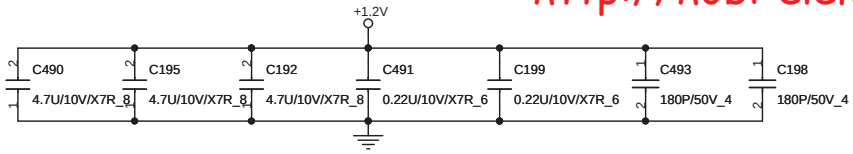


A01

C-test-Add

PROJECT : SA1A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK GENERATOR	3A
Date: Tuesday, February 05, 2008	Sheet 2 of 39	

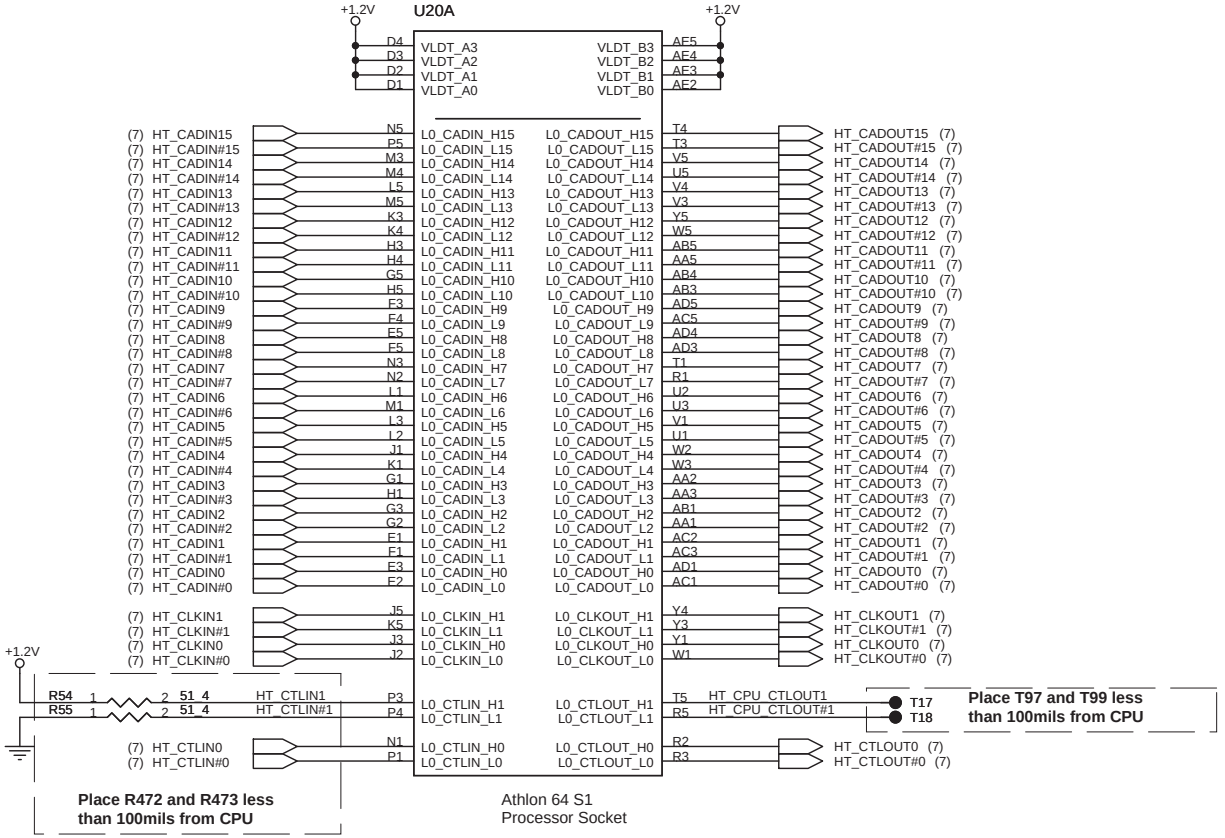


LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS

PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



PROJECT : SA1A
Quanta Computer Inc.

Size	Document Number	Rev
B	ATHLON64 HT I/F	3A

Date: Thursday, January 31, 2008 Sheet 3 of 39

Notes for the SODIMM locations:
DIMMA = Far = Bottom
DIMMB = Near = Top

Processor DDR2 Memory Interface

VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

+1.8V_SUS

C67 0.1U/10V/X7R_4
R48 1K/F_6

CPU_VTT_SUS_SENSE should be routed as 10mils and 10mils spacing from any adjacent signals in X, Y, Z directions.

+0.9V_CPU_M_VREF_SUS

C76 0.1U/10V/X7R_4
C73 1000P/50V_4
R47 1K/F_6

for +0.9V_DDR_VTT feedback

Place Capacitors for +0.9V_CPU_M_VREF_SUS < 1" from the RS690.
+0.9V_CPU_M_VREF_SUS trace length < 6", trace width > 15mils and 20mils spacing from any adjacent signals in X, Y, Z directions.

+1.8V_SUS

R351 39.2/F_4
R352 39.2/F_4

KEEP TRACE TO RESISTORS LESS THAN 1.5" FROM CPU PIN

U20B

+0.9V_DDR_VTT

(36) CPU_VTT_SENSE

U20B		
W17	MEMVREF	
Y10	VTT_SENSE	
AE10	MEMZN	M_ZN
AF10	MEMZP	M_ZP
D10	VTT1	
C10	VTT2	
B10	VTT3	
AD10	VTT4	
W10	VTT5	
AC10	VTT6	
AB10	VTT7	
AA10	VTT8	
A10	VTT9	
V19	PMA0_CS_L3	T16 DDR_CS3_DIMMA#
J22	PMA0_CS_L2	T32 DDR_CS2_DIMMA#
V22	PMA0_CS_L1	(12,13) DDR_CS1_DIMMA#
T19	PMA0_CS_L0	(12,13) DDR_CS0_DIMMA#
Y26	PMB0_CS_L3	T14 DDR_CS3_DIMMB#
J24	PMB0_CS_L2	T33 DDR_CS2_DIMMB#
W24	PMB0_CS_L1	(12,13) DDR_CS1_DIMMB#
U23	PMB0_CS_L0	(12,13) DDR_CS0_DIMMB#
H26	MB_CKE1	(12,13) DDR_CKE1_DIMMB
J23	MB_CKE0	(12,13) DDR_CKE0_DIMMB
J20	MA_CKE1	(12,13) DDR_CKE1_DIMMA
J21	MA_CKE0	(12,13) DDR_CKE0_DIMMA
Y16	MA0_CLK_H2	M_CLK_DDR1 (12,13)
AA16	MA0_CLK_L2	M_CLK_DDR#1 (12,13)
E16	MA0_CLK_H1	M_CLK_DDR0 (12,13)
F16	MA0_CLK_L1	M_CLK_DDR#0 (12,13)
AF18	MB0_CLK_H2	M_CLK_DDR3 (12,13)
AE17	MB0_CLK_L2	M_CLK_DDR#3 (12,13)
A17	MB0_CLK_H1	M_CLK_DDR2 (12,13)
A18	MB0_CLK_L1	M_CLK_DDR#2 (12,13)
W23	MB0_ODT1	M_ODT3 (12,13)
W26	MB0_ODT0	M_ODT2 (12,13)
V20	MA0_ODT1	M_ODT1 (12,13)
U19	MA0_ODT0	M_ODT0 (12,13)

(12,13) DDR_A_MA[0..15]

DDR_A_MA15	K19	MA_ADD15	MB_ADD15
DDR_A_MA14	K20	MA_ADD14	MB_ADD14
DDR_A_MA13	V24	MA_ADD13	MB_ADD13
DDR_A_MA12	K24	MA_ADD12	MB_ADD12
DDR_A_MA11	L20	MA_ADD11	MB_ADD11
DDR_A_MA10	R19	MA_ADD10	MB_ADD10
DDR_A_MA9	L19	MA_ADD9	MB_ADD9
DDR_A_MA8	L22	MA_ADD8	MB_ADD8
DDR_A_MA7	L21	MA_ADD7	MB_ADD7
DDR_A_MA6	M19	MA_ADD6	MB_ADD6
DDR_A_MA5	M20	MA_ADD5	MB_ADD5
DDR_A_MA4	M24	MA_ADD4	MB_ADD4
DDR_A_MA3	M22	MA_ADD3	MB_ADD3
DDR_A_MA2	N22	MA_ADD2	MB_ADD2
DDR_A_MA1	N21	MA_ADD1	MB_ADD1
DDR_A_MA0	R21	MA_ADD0	MB_ADD0

J25	DDR_B_MA15		DDR_B_MA[0..15] (12,13)
J26	DDR_B_MA14		
W25	DDR_B_MA13		
L23	DDR_B_MA12		
L25	DDR_B_MA11		
U25	DDR_B_MA10		
L24	DDR_B_MA9		
M26	DDR_B_MA8		
L26	DDR_B_MA7		
N23	DDR_B_MA6		
N24	DDR_B_MA5		
N25	DDR_B_MA4		
N26	DDR_B_MA3		
P24	DDR_B_MA2		
P26	DDR_B_MA1		
T24	DDR_B_MA0		

(12,13) DDR_A_BS2	K22	MA_BANK2	MB_BANK2 K26 DDR_B_BS2 (12,13)
(12,13) DDR_A_BS1	R20	MA_BANK1	MB_BANK1 T26 DDR_B_BS1 (12,13)
(12,13) DDR_A_BS0	T22	MA_BANK0	MB_BANK0 U26 DDR_B_BS0 (12,13)
(12,13) DDR_A_RAS#	T20	MA_RAS_L	MB_RAS_L U24 DDR_B_RAS# (12,13)
(12,13) DDR_A_CAS#	U20	MA_CAS_L	MB_CAS_L V26 DDR_B_CAS# (12,13)
(12,13) DDR_A_WE#	U21	MA_WE_L	MB_WE_L U22 DDR_B_WE# (12,13)

DDR II: CMD/CTRL/CLK

Athlon 64 S1
Processor Socket

U20C

(12) DDR_B_D[0..63]

DDR_B_D63	AD11	MB_DATA63	MA_DATA63
DDR_B_D62	AE11	MB_DATA62	MA_DATA62
DDR_B_D61	AE14	MB_DATA61	MA_DATA61
DDR_B_D60	AE14	MB_DATA60	MA_DATA60
DDR_B_D59	Y11	MB_DATA59	MA_DATA59
DDR_B_D58	AB11	MB_DATA58	MA_DATA58
DDR_B_D57	AC12	MB_DATA57	MA_DATA57
DDR_B_D56	AE13	MB_DATA56	MA_DATA56
DDR_B_D55	AE15	MB_DATA55	MA_DATA55
DDR_B_D54	AF16	MB_DATA54	MA_DATA54
DDR_B_D53	AC18	MB_DATA53	MA_DATA53
DDR_B_D52	AF19	MB_DATA52	MA_DATA52
DDR_B_D51	AD14	MB_DATA51	MA_DATA51
DDR_B_D50	AC14	MB_DATA50	MA_DATA50
DDR_B_D49	AE18	MB_DATA49	MA_DATA49
DDR_B_D48	AD18	MB_DATA48	MA_DATA48
DDR_B_D47	AD20	MB_DATA47	MA_DATA47
DDR_B_D46	AC20	MB_DATA46	MA_DATA46
DDR_B_D45	AF23	MB_DATA45	MA_DATA45
DDR_B_D44	AF24	MB_DATA44	MA_DATA44
DDR_B_D43	AF20	MB_DATA43	MA_DATA43
DDR_B_D42	AE20	MB_DATA42	MA_DATA42
DDR_B_D41	AD22	MB_DATA41	MA_DATA41
DDR_B_D40	AC22	MB_DATA40	MA_DATA40
DDR_B_D39	AE25	MB_DATA39	MA_DATA39
DDR_B_D38	AD26	MB_DATA38	MA_DATA38
DDR_B_D37	AA25	MB_DATA37	MA_DATA37
DDR_B_D36	AA26	MB_DATA36	MA_DATA36
DDR_B_D35	AE24	MB_DATA35	MA_DATA35
DDR_B_D34	AD24	MB_DATA34	MA_DATA34
DDR_B_D33	AA23	MB_DATA33	MA_DATA33
DDR_B_D32	AA24	MB_DATA32	MA_DATA32
DDR_B_D31	G24	MB_DATA31	MA_DATA31
DDR_B_D30	G23	MB_DATA30	MA_DATA30
DDR_B_D29	D26	MB_DATA29	MA_DATA29
DDR_B_D28	C26	MB_DATA28	MA_DATA28
DDR_B_D27	G26	MB_DATA27	MA_DATA27
DDR_B_D26	G25	MB_DATA26	MA_DATA26
DDR_B_D25	E24	MB_DATA25	MA_DATA25
DDR_B_D24	E23	MB_DATA24	MA_DATA24
DDR_B_D23	C24	MB_DATA23	MA_DATA23
DDR_B_D22	B24	MB_DATA22	MA_DATA22
DDR_B_D21	C20	MB_DATA21	MA_DATA21
DDR_B_D20	B20	MB_DATA20	MA_DATA20
DDR_B_D19	C25	MB_DATA19	MA_DATA19
DDR_B_D18	D24	MB_DATA18	MA_DATA18
DDR_B_D17	A21	MB_DATA17	MA_DATA17
DDR_B_D16	D20	MB_DATA16	MA_DATA16
DDR_B_D15	D18	MB_DATA15	MA_DATA15
DDR_B_D14	C18	MB_DATA14	MA_DATA14
DDR_B_D13	D14	MB_DATA13	MA_DATA13
DDR_B_D12	C14	MB_DATA12	MA_DATA12
DDR_B_D11	A20	MB_DATA11	MA_DATA11
DDR_B_D10	A19	MB_DATA10	MA_DATA10
DDR_B_D9	A16	MB_DATA9	MA_DATA9
DDR_B_D8	A15	MB_DATA8	MA_DATA8
DDR_B_D7	A13	MB_DATA7	MA_DATA7
DDR_B_D6	D12	MB_DATA6	MA_DATA6
DDR_B_D5	E11	MB_DATA5	MA_DATA5
DDR_B_D4	G11	MB_DATA4	MA_DATA4
DDR_B_D3	B14	MB_DATA3	MA_DATA3
DDR_B_D2	A14	MB_DATA2	MA_DATA2
DDR_B_D1	A11	MB_DATA1	MA_DATA1
DDR_B_D0	C11	MB_DATA0	MA_DATA0

(12) DDR_B_DM[0..7]

DDR_B_DM7	AD12	MB_DM7	MA_DM7
DDR_B_DM6	AC16	MB_DM6	MA_DM6
DDR_B_DM5	AF22	MB_DM5	MA_DM5
DDR_B_DM4	AB26	MB_DM4	MA_DM4
DDR_B_DM3	E25	MB_DM3	MA_DM3
DDR_B_DM2	A22	MB_DM2	MA_DM2
DDR_B_DM1	B16	MB_DM1	MA_DM1
DDR_B_DM0	A12	MB_DM0	MA_DM0

(12) DDR_B_DQS[0..7]

DDR_B_DQS7	AE12	MB_DQS_H7	MA_DQS_H7
DDR_B_DQS#7	AE12	MB_DQS_L7	MA_DQS_L7
DDR_B_DQS6	AE16	MB_DQS_H6	MA_DQS_H6
DDR_B_DQS#6	AD16	MB_DQS_L6	MA_DQS_L6
DDR_B_DQS5	AF21	MB_DQS_H5	MA_DQS_H5
DDR_B_DQS#5	AF22	MB_DQS_L5	MA_DQS_L5
DDR_B_DQS4	AC25	MB_DQS_H4	MA_DQS_H4
DDR_B_DQS#4	AC26	MB_DQS_L4	MA_DQS_L4
DDR_B_DQS3	F26	MB_DQS_H3	MA_DQS_H3
DDR_B_DQS#3	F26	MB_DQS_L3	MA_DQS_L3
DDR_B_DQS2	A24	MB_DQS_H2	MA_DQS_H2
DDR_B_DQS#2	A23	MB_DQS_L2	MA_DQS_L2
DDR_B_DQS1	D16	MB_DQS_H1	MA_DQS_H1
DDR_B_DQS#1	C16	MB_DQS_L1	MA_DQS_L1
DDR_B_DQS0	C12	MB_DQS_H0	MA_DQS_H0
DDR_B_DQS#0	B12	MB_DQS_L0	MA_DQS_L0

DDR DATA

Athlon 64 S1
Processor Socket

Y13	DDR_A_DM7		DDR_A_DM[0..7] (12)
AB16	DDR_A_DM6		
Y19	DDR_A_DM5		
AC24	DDR_A_DM4		
F24	DDR_A_DM3		
F19	DDR_A_DM2		
C15	DDR_A_DM1		
E12	DDR_A_DM0		
W12	DDR_A_DQS7		DDR_A_DQS[0..7] (12)
W13	DDR_A_DQS#7		
Y15	DDR_A_DQS6		
W15	DDR_A_DQS#6		
AB19	DDR_A_DQS5		
AB20	DDR_A_DQS#5		
AD23	DDR_A_DQS4		
AC23	DDR_A_DQS#4		
G22	DDR_A_DQS3		
G21	DDR_A_DQS#3		
C22	DDR_A_DQS2		
C21	DDR_A_DQS#2		
G16	DDR_A_DQS1		
G15	DDR_A_DQS#1		
G13	DDR_A_DQS0		
H13	DDR_A_DQS#0		

To SODIMM socket B (Near/TOP)

To SODIMM socket A (Far/Bottom)

DDR_B_DQS0 DDR_B_DQS1 DDR_B_DQS2 DDR_B_DQS3 DDR_B_DQS4 DDR_B_DQS5 DDR_B_DQS6 DDR_B_DQS7
(12) DDR_B_DQS[0..7]

DDR_B_DQS#0 DDR_B_DQS#1 DDR_B_DQS#2 DDR_B_DQS#3 DDR_B_DQS#4 DDR_B_DQS#5 DDR_B_DQS#6 DDR_B_DQS#7
(12) DDR_B_DQS#[0..7]

DDR_A_DQS0 DDR_A_DQS1 DDR_A_DQS2 DDR_A_DQS3 DDR_A_DQS4 DDR_A_DQS5 DDR_A_DQS6 DDR_A_DQS7
(12) DDR_A_DQS[0..7]

DDR_A_DQS#0 DDR_A_DQS#1 DDR_A_DQS#2 DDR_A_DQS#3 DDR_A_DQS#4 DDR_A_DQS#5 DDR_A_DQS#6 DDR_A_DQS#7
(12) DDR_A_DQS#[0..7]

PROJECT : SA1A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ATHLON64 DDRII MEMORY	3A

Date: Thursday, January 31, 2008 Sheet 4 of 39

SB600 ONLY

(14) CPU_PWRGD — R376 680_4 — C210 *1000P/16V/X7R_4 — CPU_PWRGD — R91 1 2 0_4 — LDT_STOP_R#

A02 C-test-Del

A03 C-test-Change

+1.8V — R99 *0_4 — +1.8V_SUS — R97 *0_4

D4 *SDMK0340L-7-F

(9,14) LDT_STOP# — R98 *10K/F_4 — U4 *NL17SZ17DFT2G — R96 680_4

R100 *680_4 — C221 *0.1U/16V_4 — C217 *47P/50V_4

NOTE: R7516 and C7598 close to JCPU pin F10

A03 C-test-Change

(14) LDT_RST# — R377 680 — C540 *1000P/16V/X7R_4 — LDT_RST#

NOTE: Place R7090 on the top of the board that is iaccessible, and that shorting across this resistor will toggle the hyper Transport reset signal.

A02 C-test-Del

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG. This trace should be kept at least 20 mils away from all other signals.

+2.5V_CPU_VDDA_RUN

L65 ferrite bead with an approximate impedance of 33 , a maximum DC resistance of 0.025 ohm , and a current rating of at least 3000mA.

+2.5V — L25 <Size> BLM18PG330SN1D — +2.5V_CPU_VDDA_RUN — +2.5V_CPU_VDDA_RUN

C532 100U/6.3V_3528 — C224 4.7U/10V_8 — C223 0.22U/10V_6 — C218 3300P/X7R/_4

If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300-Ω (±5%) pulldown to VSS.

Place R78 and R77 < 1.5". Route CPU_HTREF1/0 with 5mils trace width and 10mils spacing from other signals in X, Y, Z directions

The AMD SI feature has errata, and will not be plemented.

+1.2V — R353 300_4 CPU_SIC — R354 *0_4 CPU_SID — R361 44.2/F_4 CPU_HTREF1 — R358 44.2/F_4 CPU_HTREF0

To Power (37) CPU_VDD_RUN_FB_H — (37) CPU_VDD_RUN_FB_L — T42 — T49

(36) VDDIO_FB_H — (36) VDDIO_FB_L

T15 VDDIO_FB_H — T13 VDDIO_FB_L — T58 CPU_CLK — T59 CPU_CLK# — T47 CPU_TEST29_H_FBCLKOUT_P — T46 CPU_TEST29_L_FBCLKOUT_N

U20D

F8 VDDA2 — F9 VDDA1

B7 RESET_L — A7 PWROK — E10 LDTSTOP_L

AE4 SIC — AE5 SID

P6 HT_REF1 — R6 HT_REF0

F6 VDD_FB_H — E6 VDD_FB_L

W9 VDDIO_FB_H — Y9 VDDIO_FB_L

A9 CPU_CLKIN_SC_P — A8 CPU_CLKIN_SC_N — CLKIN_H — CLKIN_L

G10 DBRDY

AA9 TMS — AC9 TCK — AD9 TRST_L — AF9 TDI

LDT_RST# — CPU_PWRGD — LDT_STOP_R#

CPU_DBRDY — CPU_TMS — CPU_TCK — CPU_TRST# — CPU_TDI

THERMTRIP_L — PROCHOT_L — AE6 THERMTRIP# — AC7 CPU_PROCHOT# — H_THERMTRIP# (15)

+3.3V_ALW — +1.8V_SUS — R38 10K_4 — R34 *4.7K — R41 300_4 — R22 300_4 — R104 300_4 — THERM_B1

Q1 MMST3904 — C49 0.1U/16V_4

VID5 A5 — VID4 C6 — VID3 A6 — VID2 A4 — VID1 C5 — VID0 B5 — VID5 (37) — VID4 (37) — VID3 (37) — VID2 (37) — VID1 (37) — VID0 (37)

CPU_PRESENT_L — AC6 CPU_PRESENT# — PSI_L A3 — CPU_PSI# (37) — T51

PSI_L is a Power Status Indicator signal. This signal is asserted when the processor is in a low powerstate. PSI_L should be connected to the power supply controller, if the controller supports "skipmode, or diode emulation mode". PSI_L is asserted by the processor during the C3 and S1 states.

DBREQ_L F10 CPU_DBREQ# — TDO AE9 CPU_TDO

TEST29_H C9 CPU_TEST29_H_FBCLKOUT_P — TEST29_L C8 CPU_TEST29_L_FBCLKOUT_N — R89 2 1 80.6/F_4

ROUTE AS 80 Ohm DIFFERENTIAL PAIR PLACE IT CLOSE TO CPU WITHIN 1"

T41 CPU_TEST25_H_BYPASSCLK_H — T44 CPU_TEST25_L_BYPASSCLK_L — T38 CPU_TEST19_PLLTEST0 — T35 CPU_TEST18_PLLTEST1

T45 CPU_TEST17_BP3 — T43 CPU_TEST16_BP2 — T139 CPU_TEST15_BP1 — T54 CPU_TEST14_BP0 — T9 CPU_TEST12_SCANSHIFTENB

E9 TEST25_H — E8 TEST25_L — G9 TEST19 — H10 TEST18 — AA7 TEST13 — C2 TEST9 — D7 TEST17 — E7 TEST16 — F7 TEST15 — C7 TEST14 — AC8 TEST12

TEST24 AE7 CPU_TEST24_SCANCLK1 — T4
TEST23 AD7 CPU_TEST23_TSTUPD — T6
TEST22 AE8 CPU_TEST22_SCANSHIFTEN — T8
TEST21 AB8 CPU_TEST21_SCANEN — T10
TEST20 AE7 CPU_TEST20_SCANCLK2 — T3

TEST28_H J7 — TEST28_L H8 — TEST27 AF8 CPU_TEST27_SINGLECHAIN — T5 — TEST26 AF6 CPU_TEST26_BURNIN# — T7 — TEST10 K8 — TEST8 C4

H_THERMDC — H_THERMDA — C3 — AA2 — W7 — W8 — Y8 — AB8 — TEST7 — TEST6 — TEST5 — TEST4 — TEST3 — TEST2

T26 CPU_RSVD_MA0_CLK3_P — T25 CPU_RSVD_MA0_CLK3_N — T29 CPU_RSVD_MA0_CLK0_P — T28 CPU_RSVD_MA0_CLK0_N

P20 RSVD0 — P19 RSVD1 — N20 RSVD2 — N19 RSVD3

RSVD8 H16 CPU_MA_RESET# — T39
RSVD9 B18 CPU_MB_RESET# — T50
RSVD10 R3 CPU_RSVD_VIDSTRB1 — T138
RSVD11 C1 CPU_RSVD_VIDSTRB0 — T137
RSVD12 H6 CPU_RSVD_VDDNB_FB_P — T34
RSVD13 G6 CPU_RSVD_VDDNB_FB_N — T40
RSVD14 D5 CPU_RSVD_CORE_TYPE — T48
RSVD15 R24 CPU_RSVD_15 — T21
RSVD16 W18 CPU_RSVD_16 — T12
RSVD17 R23 CPU_RSVD_17 — T20
RSVD18 AA8 CPU_RSVD_18 — T11
RSVD19 H18 CPU_RSVD_19 — T36
RSVD20 H19 CPU_RSVD_20 — T37

T23 CPU_RSVD_MB0_CLK3_P — T22 CPU_RSVD_MB0_CLK3_N — T27 CPU_RSVD_MB0_CLK0_P — T19 CPU_RSVD_MB0_CLK0_N

R26 RSVD4 — R25 RSVD5 — P22 RSVD6 — R22 RSVD7

MISC

AMD NPT S1 SOCKET
Processor Socket

(2) CPU_CLK — C529 3900P/50V_4 — CPU_CLKIN_SC_P — CPU_CLKIN_SC_N — R373 169/F_4 — (2) CPU_CLK# — C528 3900P/50V_4

1.KEEP TRACE TO RESISTOR LESS THAN 600MILS FROM CPU PIN AND TRACE TO AC CAPS LESS THAN 1250MILS.

2. CPUCLK and CPUCLK# mismatch < 35 mils.

+1.8V_SUS

CPU_TEST27_SINGLECHAIN — R347 *300_4
CPU_TEST26_BURNIN# — R346 300_4
CPU_PRESENT# — R44 1K/F_4
CPU_TEST25_H_BYPASSCLK_H — R90 510/F_4

CPU_TEST21_SCANEN — R26 300_4
CPU_TEST20_SCANCLK2 — R45 *300_4
CPU_TEST24_SCANCLK1 — R349 *300_4
CPU_TEST22_SCANSHIFTEN — R350 *300_4
CPU_TEST12_SCANSHIFTENB — R27 *300_4
CPU_TEST15_BP1 — R94 *300_4
CPU_TEST14_BP0 — R93 *300_4
CPU_TEST25_L_BYPASSCLK_L — R95 510/F_4
CPU_TEST19_PLLTEST0 — R64 300_4
CPU_TEST18_PLLTEST1 — R65 300_4

If no use which Net need pull-up or down

+1.8V_SUS — R40 *10K_4 — +3.3V — R42 *4.7K_4 — Q2 *MMBT3904 — CPU_PROCHOT# — SB_CPU_PROCHOT# (16) — VR_TT# (37)

HDT CONNECTOR

+1.8V_SUS — R32 *220_4 — R31 *220_4 — R28 *220_4 — R29 *220_4 — R30 *220_4 — R33 *220_4 — R48 *220_4 — R29 *220_4

JHDT1 *HDT conn

CPU_DBREQ# — CPU_DBRDY — CPU_TCK — CPU_TMS — CPU_TDI — CPU_TRST# — CPU_TDO

1 GND — 3 Resreved1 — 5 Resreved2 — 7 DBREQ_L — 9 DBRDY — 11 TCK — 13 TMS — 15 TDI — 17 TRST_L — 19 TDO — 21 VDDIO1 — 23 VDDIO2 — 25 RESET_L — GND

+1.8V_SUS — C671 0.1U/10V/X7R_4 — C672 0.1U/10V/X7R_4 — C673 0.1U/10V/X7R_4 — C674 0.1U/10V/X7R_4 — C675 0.1U/10V/X7R_4 — C670 0.1U/10V/X7R_4 — C689 0.1U/10V/X7R_4

EC C-01

NOTE:HDT TERMINATION IS REQUIRED FOR REV.Ax SILICON ONLY.

+3.3V — R379 4.7K_4 — +1.8V — R381 4.7K_4 — CPU_RESET# — Q37 MMBT3904 — LDT_RST#

R380 *100K_4

CPU Thermal monitor

+3.3V — Q4 2N7002W-7-F — (30) ABCLK — ABCLK — THCLK_SMB

Q6 2N7002W-7-F — (30) ABDATA — ABDATA — THDAT_SMB

(16) THERM_ALERT# — R85 *0_4

Q7 2N7002W-7-F — (34) SYS_SHDN# — 6648OVERT#

R88 220_6 — 6648VCC — C207 0.1U/10V/X5R_4

R82 10K_4 — R83 10K_4 — R84 10K_4 — R87 *10K_4

U3 G781P8 ADDRESS: 98H

SCLK — SDA — ALERT# — OVERT# — VCC — DXP — DXN — GND

H_THERMDA — C208 2200P/50V_6 — H_THERMDC

+5V — 30 mil — U21 G993P1U — VEN VIN VO SET — GND GND GND GND

(30) PWM_FAN1 — R378 0_4 — +5V_FAN — C534 *0.1U/10V/X5R_4

EC C-02

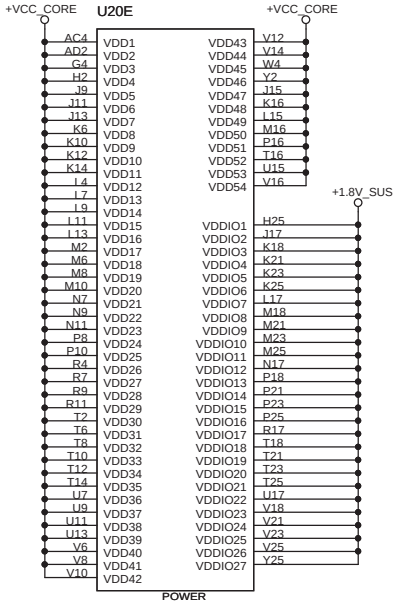
C539 1U/10V/X5R_6 — C536 0.1U/10V/X5R_4 — C537 10U/10V/X5R_8 — C548 1000P/16V/X7R_4

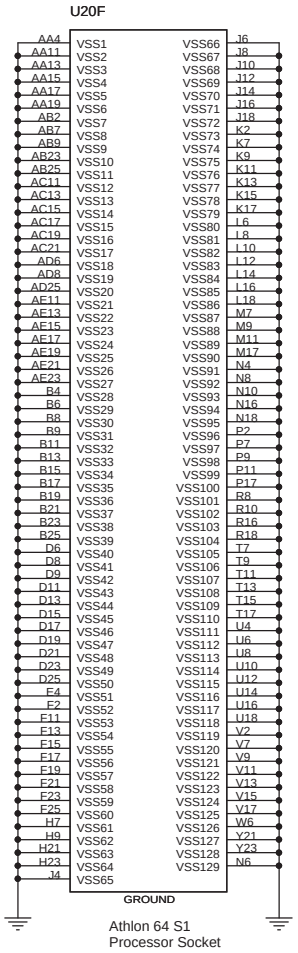
30 mil — +5V_FAN — CN21 FAN

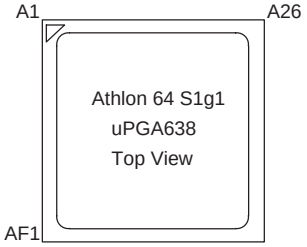
+3.3V — Q39 PDTA124EU — (30) FANSIG1 — R409 100K_4

PROJECT : SA1A		
Quanta Computer Inc.		
Size: Custom	Document Number: ATHLON64 CTRL & DEBUG	Rev: 3A
Date: Thursday, January 31, 2008	Sheet 5 of 39	

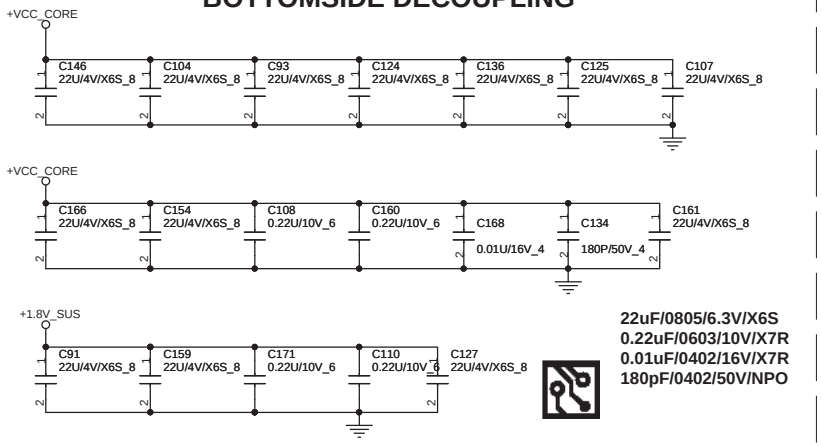
Layout Note:
Layout Note:Routing 10:10 mils and away from noise source with ground gard



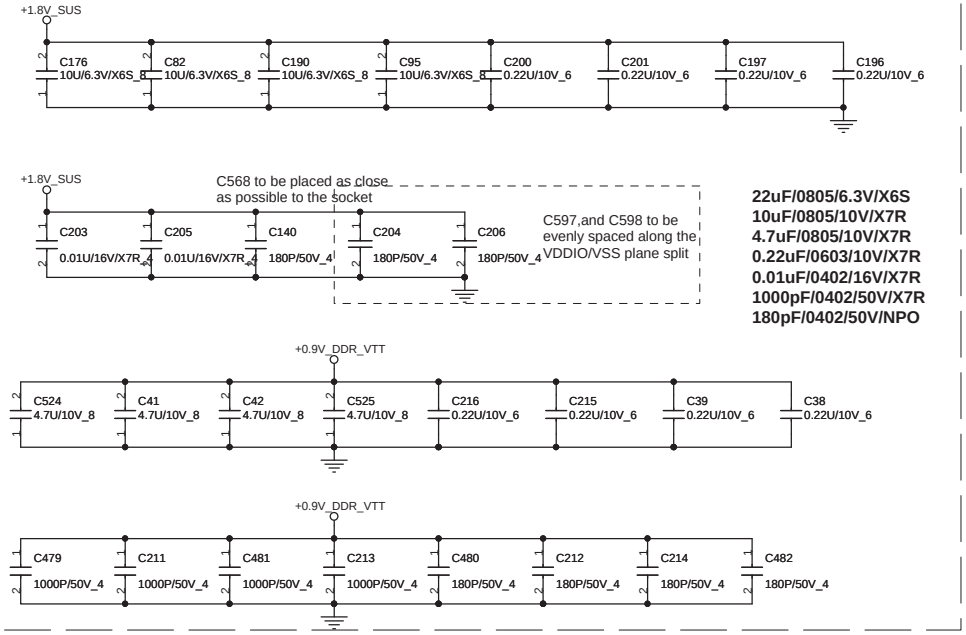




BOTTOMSIDE DECOUPLING



DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE



PROCESSOR POWER AND GROUND

PROJECT : SA1A
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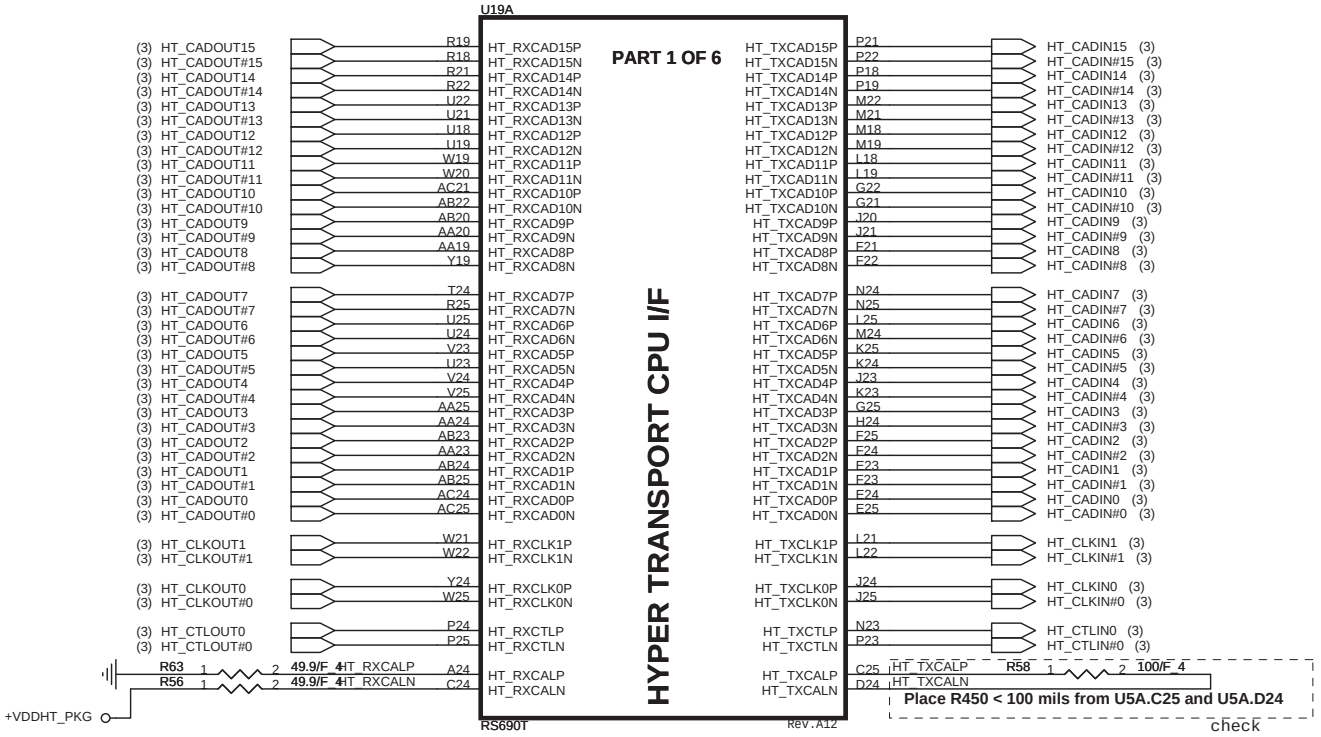
Size	Document Number	Rev
Custom	ATHLON64 PWR & GND	3A
Date: Thursday, January 31, 2008	Sheet 6 of 39	

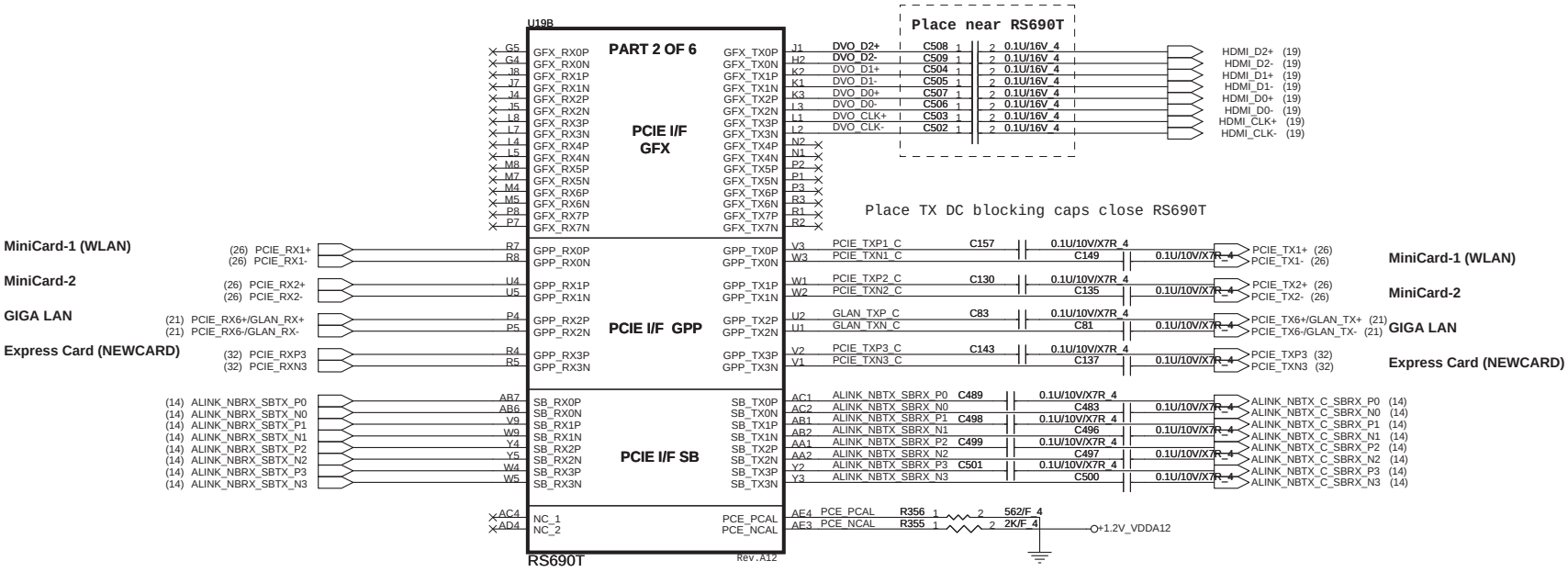
Change Part Number



PROJECT : SA1A
Quanta Computer Inc.

Size	Document Number	Rev
B	RS690T-HT LINK0 I/F	3A

Date: Thursday, January 31, 2008 Sheet 7 of 39



PROJECT : SA1A
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Size	Document Number	Rev
Custom	RS690T-PCIE LINK I/F	3A

Date: Thursday, January 31, 2008 Sheet 8 of 39

+1.8V L53 BLM15AG221SN1D +1.8V_AVDDQ C523 *10U/10V_8 C181 2.2U/10V_6
+1.8V L52 BLM15AG221SN1D +1.8V_PLLVDD C522 *10U/10V_8 C518 2.2U/10V_6
+1.8V L51 BLM15AG221SN1D +1.8V_HTPVDD C514 *10U/10V_8 C517 4.7U_6.3V_6 C513 1U/6.3V_4

+3.3V L54 BLM18PG330SN1D +3.3V_AVDD C521 2.2U/10V_6 — 20mil Width
+1.8V R366 0_4 +1.8V_RUN_AVDDDI C520 2.2U/10V_6 — 20mil Width
+1.8V_AVDDQ — 20mil Width

U19C — RS690T — PART 3 OF 6

CRT/TVOUT: AVDD1 AVDD2 AVSSN1 AVSSN2 AVDDDI AVSSDI AVDDQ AVSSQ C_R Y_G COMP_B RED GREEN BLUE DACVSYNC DACHSYNC RSET DACSCL DACSDA
PLL PWR: PLLVDD18(PLLVDD) PLLVSS HTPVDD HTPVSS VDDPLL_1(VDDA12) VDDPLL_2(VDDA12) VSSPLL_1(VSSA12) VSSPLL_2(VSSA12)
PM: SYSRESET# POWERGOOD LDTSTOP# ALLOW_LDTSTOP#
CLOCKs: HTTSTCLK HTREFCLK TVCLKIN OSCIN PLLVDD12(OSCOUT) GFX_CLKP GFX_CLKN SB_CLKP SB_CLKN
MIS.: BMREQb I2C_CLK I2C_DATA THERMALDIODE_P THERMALDIODE_N TMDS_HPD DDC_DATA TESTMODE STRP_DATA

R446,R455,R461 CLOSE TO NB
(20) INT_CRT_RED (20) INT_CRT_GRN (20) INT_CRT_BLU
R59 150_4 R53 150_4 R51 150_4
(20) INT_VSYNC (20) INT_HSYNC
R60 715/F
(20) INT_CRT_DDCCLK (20) INT_CRT_DDCDAT
+1.8V_PLLVDD — 20mil Width
+1.8V_HTPVDD — 20mil Width

+1.2V_VDDA12 L15 BLM21PG221SN1D <Imax> <Size> +1.2V_VDDPLL C116 4.7U_6.3V_0603 C123 1U — 30mil Width
RS690: 220 Ohm 2A FB

(14,20,21,26,27,32) PLTRST# R73 0_4
(30) NB_PWRGD R62 0_4
(14) ALLOW_LDTSTOP
LDT_STOP# NB

AC Term closely clock pin for length: 50 mils
(2) CLK_HTREF_66M R61 *22 C156 *22P
R362 10K_4
(15,30) SUS_STAT# R360 0_4
(2) CLK_NB_14M R66 33 C177 22P
+1.2V_PLLVDD12
AC Term closely clock pin for length: 50 mils

(2) NBSRC_CLKP (2) NBSRC_CLKN
(2) SBSRCCLK (2) SBSRCCLK#
BMREQ# D
(18) INT_LVDS_EDIDCLK (18) INT_LVDS_EDIDDATA
NB_THERMDA NB_THERMDC
TMDS_HPD DDC_DATA
(35) NB_VCORE_CNTRL R364 4.7K

+1.8V R371 4.7K +3.3V R372 10K_4 Q36 MMBT3904
(5,14) LDT_STOP# LDT_STOP#_NB

+1.2V_VDDA12 L20 BLM15AG221SN1D +1.2V_PLLVDD12 C179 2.2U/10V_6
+3.3V R359 4.7K_4 SUS_STAT#

+3.3V R363 10K_4 D25 *SDMK0340L-7-F R365 *0_4 C512 *15P/50V_4
(14) BMREQ# BMREQ# D
B2-USB performance
Add R363 and Del R365

A04
C-test-For HDMI Hot Plug
R79 and R86 Change to 0 ohm
Del-C193 and R80 and D3
(19) HDMI_DET R79 0_4 EC C-13 R86 0_4 TMDS_HPD
C193 *0.01U R80 100K_4 D3 *UDZ2.4B-TE-17

+3.3V U2 *AT24C04N-10SU-2.7 R77 *10K_4 R68 *2K_4 C188 *0.1U/16V_4 R78 *2K_4
NC VCC A1 WP A2 SCL VSS SDA
INT_LVDS_EDIDCLK NB_VCORE_CNTRL

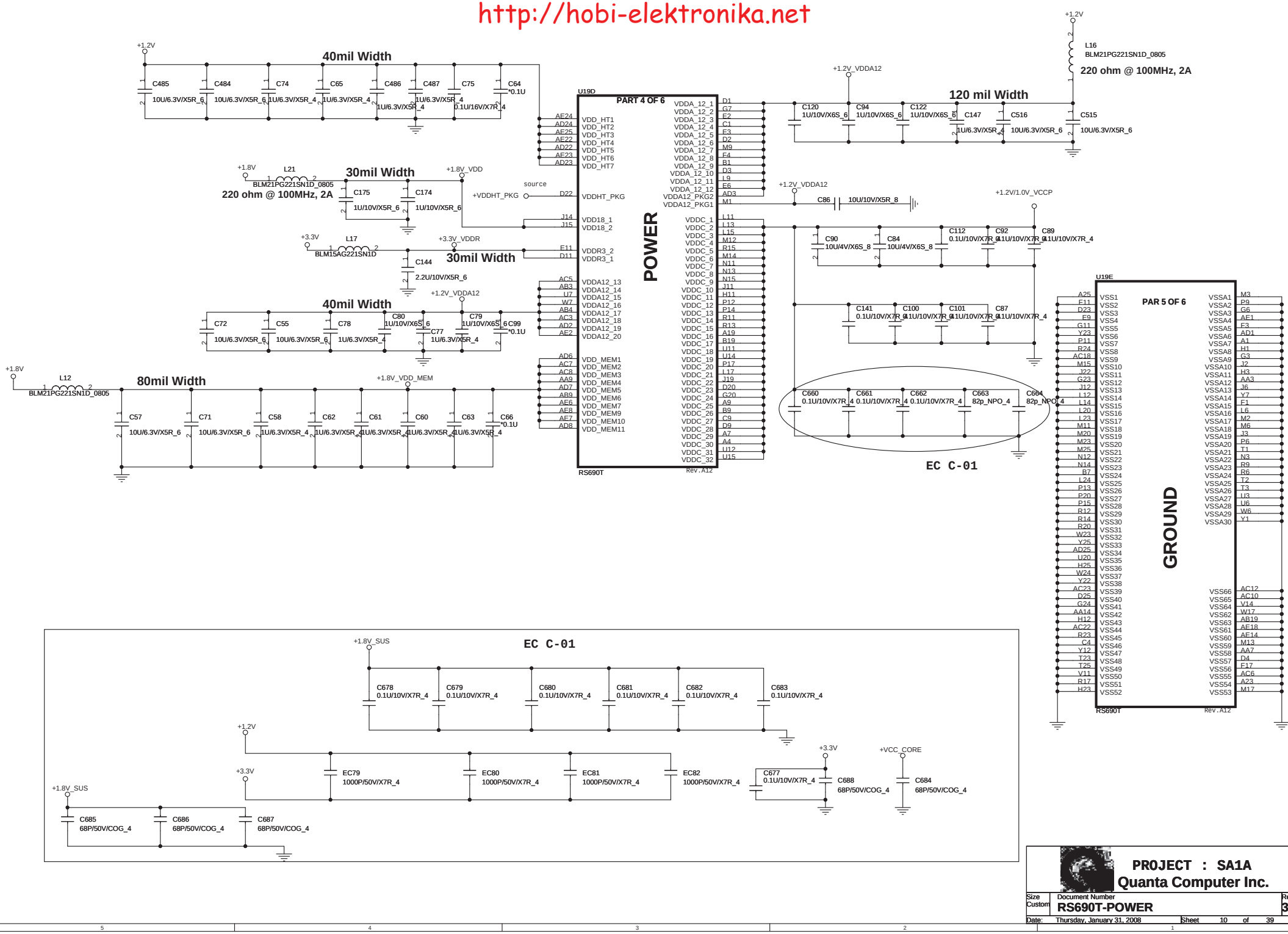
B3
Change P/N
+3.3V R69 39K INT_LVDS_EDIDCLK Q3 FDV301N +5V R67 15K/F_4 HDMI_CTRLCLK HDMI_CTRLCLK (19)
+3.3V R368 39K R369 39K INT_LVDS_EDIDDATA R370 *0_4 R367 0_4 DDC_DATA Q5 FDV301N +5V R81 15K/F_4 HDMI_CTRLDATA HDMI_CTRLDATA (19)

TXOUT_L0P TXOUT_L0N TXOUT_L1P TXOUT_L1N TXOUT_L2P TXOUT_L2N TXOUT_L3P TXOUT_L3N
TXLOUT0+ (18) TXLOUT0- (18) TXLOUT1+ (18) TXLOUT1- (18) TXLOUT2+ (18) TXLOUT2- (18)
TXOUT_U0P TXOUT_U0N TXOUT_U1P TXOUT_U1N TXOUT_U2P TXOUT_U2N TXOUT_U3P TXOUT_U3N
TXUOUT0+ (18) TXUOUT0- (18) TXUOUT1+ (18) TXUOUT1- (18) TXUOUT2+ (18) TXUOUT2- (18)
TXCLK_LP TXCLK_LN TXCLK_UP TXCLK_UN
TXLCLKOUT+ (18) TXLCLKOUT- (18) TXUCLKOUT+ (18) TXUCLKOUT- (18)
LPVDD LPVSS +LPVDD C129 0.1U/10V/X7R C519 2.2U/10V_6 — L55 BLM15AG221SN1D 20mil Width
LVDDR18D_1 LVDDR18D_2 LVDDR33A_1 LVDDR33A_2 +LVDDR18D +LVDDR33A — L19 BLM15AG221SN1D 30mil Width — L18 BLM15AG221SN1D 30mil Width
LVSSR1 LVSSR3 LVSSR5 LVSSR6 LVSSR7 LVSSR8 LVSSR12 LVSSR13
C158 0.1U/10V/X7R C167 2.2U/10V_6 C145 0.1U/10V/X7R C180 4.7U_6.3V_0603
LVDS_DIGON LVDS_BLON LVDS_BLEN
INT_LVDS_DIGON (18) INT__BKLT_CTRL (18) INT_LVDS_BLON (18)
R52 100K_4
EC C-03 R76 10K
DFT_GPIO0 LOAD_ROM# DFT_GPIO2 DFT_GPIO3 DFT_GPIO4 DFT_GPIO5
R71 R57 R72 R74 R75 R70 *3K

	PU by internal	PD by external
DFT_GPIO0	Side-Port Memory Disable	Side-Port Memory Enable (Default)
DFT_GPIO1	Bypassing EEPROM, use default values (Default)	Using EEPROM Strapping
DFT_GPIO[4:2]	Set PCI-E GPP mode to Conf. E	Select PCI-E GPP mode
DFT_GPIO5	Use default values (Default)	Use the memory data bus for debug bus output

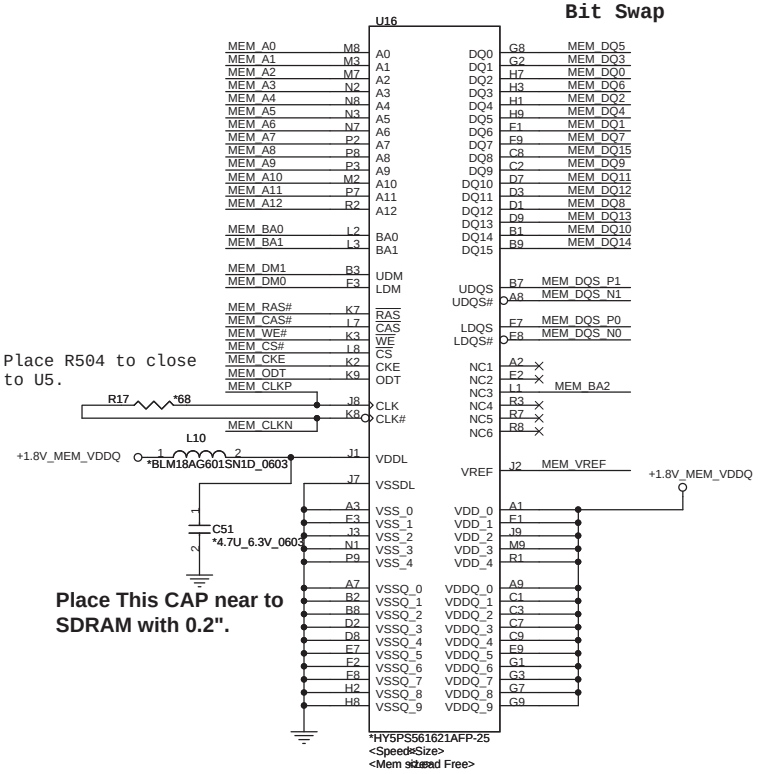
NOTE: ACCESS TO STRAP_DATA and I2C_CLK PINS IS MANDATORY.

PROJECT : SA1A
Quanta Computer Inc.
Size: Custom | Document Number: RS690T-LVDS | Rev: 3A
Date: Thursday, January 31, 2008 | Sheet 9 of 39

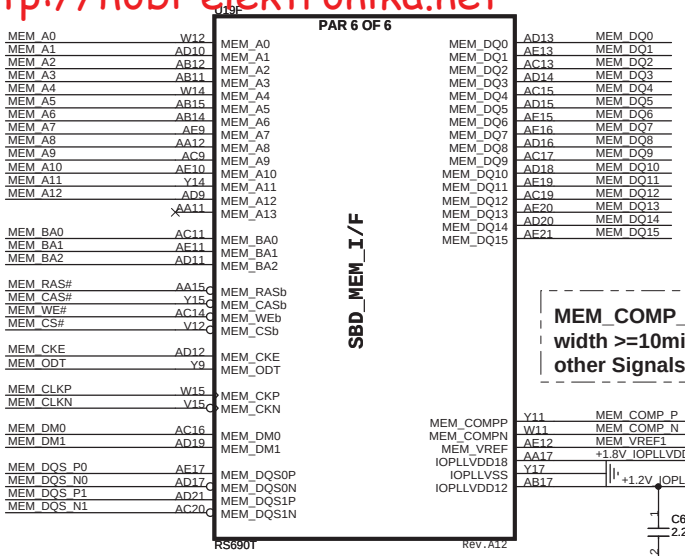


PROJECT : SA1A		
Quanta Computer Inc.		
Size: Custom	Document Number: RS690T-POWER	Rev: 3A
Date: Thursday, January 31, 2008	Sheet 10 of 39	

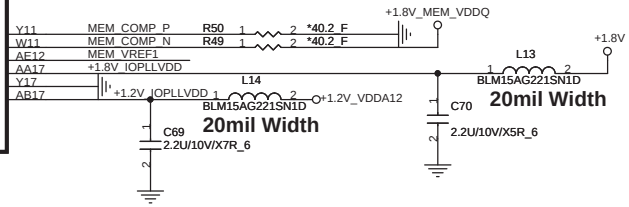
Bit Swap

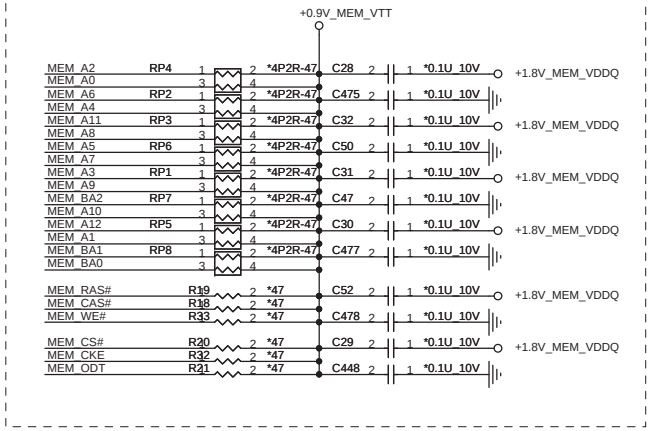


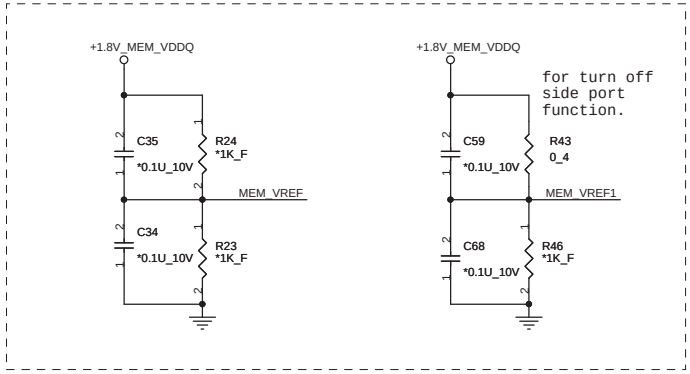
256-Mbit DDR2 16Mbit*16(4bank)

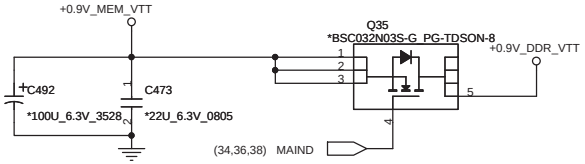


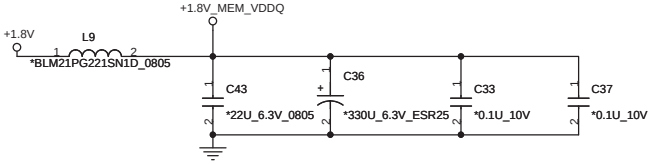
MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions





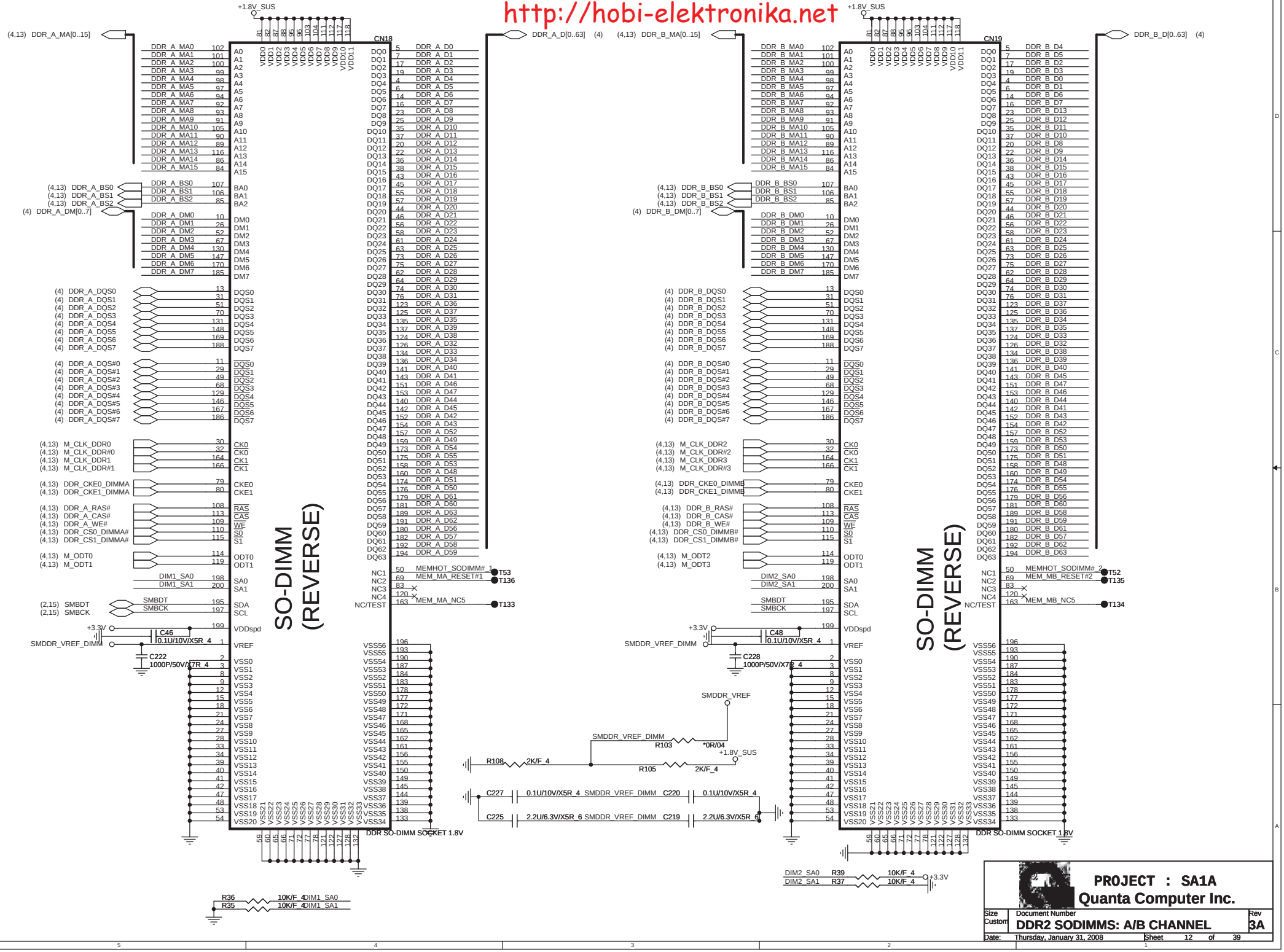






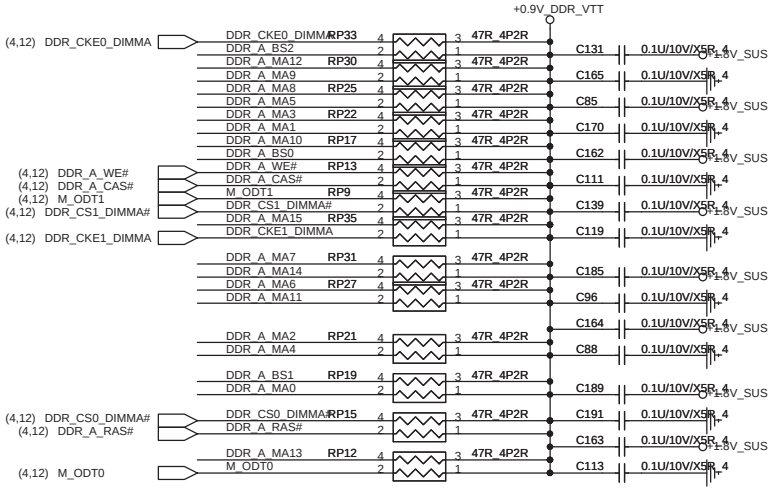
Local Frame Buffer(64MB) DDRII Power

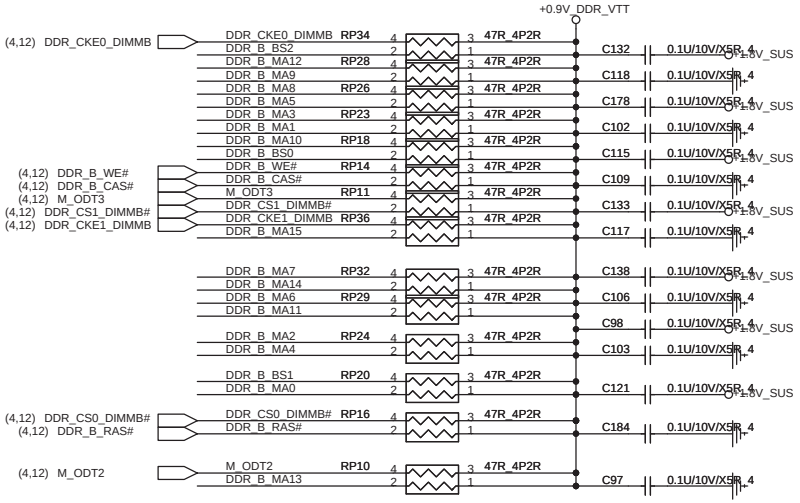
PROJECT : SA1A Quanta Computer Inc.		
Size: Custom	Document Number: RS690T-SIDE PORT I/O	Rev: 3A
Date: Thursday, January 31, 2008	Sheet 11 of 39	

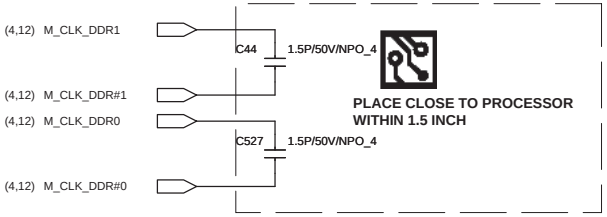


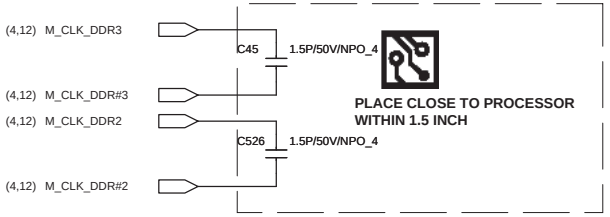
(4,12) DDR_A_MA[0..15] — DDR_A_MA[0..15]
(4,12) DDR_A_BS[0..2] — DDR_A_BS[0..2]

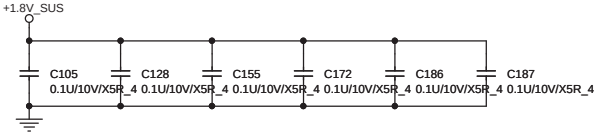
(4,12) DDR_B_MA[0..15] — MEM_MB_ADD[0..15]
(4,12) DDR_B_BS[0..2] — DDR_B_BS[0..2]

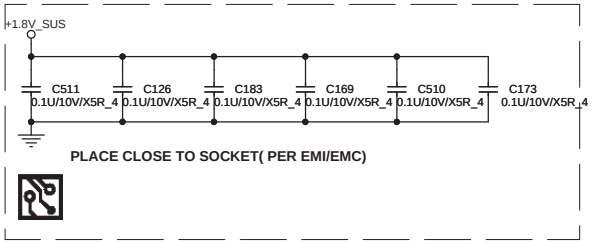












PROJECT : SA1A Quanta Computer Inc.		
Size: Custom	Document Number: DDR2 SODIMMS TERMINATIONS	Rev: 3A
Date: Thursday, January 31, 2008	Sheet 13 of 39	

SB600 SB 27x27mm
Part 1 of 4

PCI EXPRESS INTERFACE
PCI INTERFACE
PCI CLKS
XTAL
LPC
CPU
RTC

Place R346,R348,R344
< 100mils from pins E27,E28,E29

20mil Width

PCIE Power

50mil Width

NOTE: Nopop L68. Keep in case ATI provides a fixed SB600. Can pop L68 and Nopop L74 and the +1.2V_PCIE_PVDD switch circuit for cost savings.

ATi Recommend
Vendor: NSK
Part Number: NXG 32.768KAE12FUD 16 PPM.

EC C-03

EC C-04

H_DPSLP# should be put down , reserve R592 for verifing

EC C-16

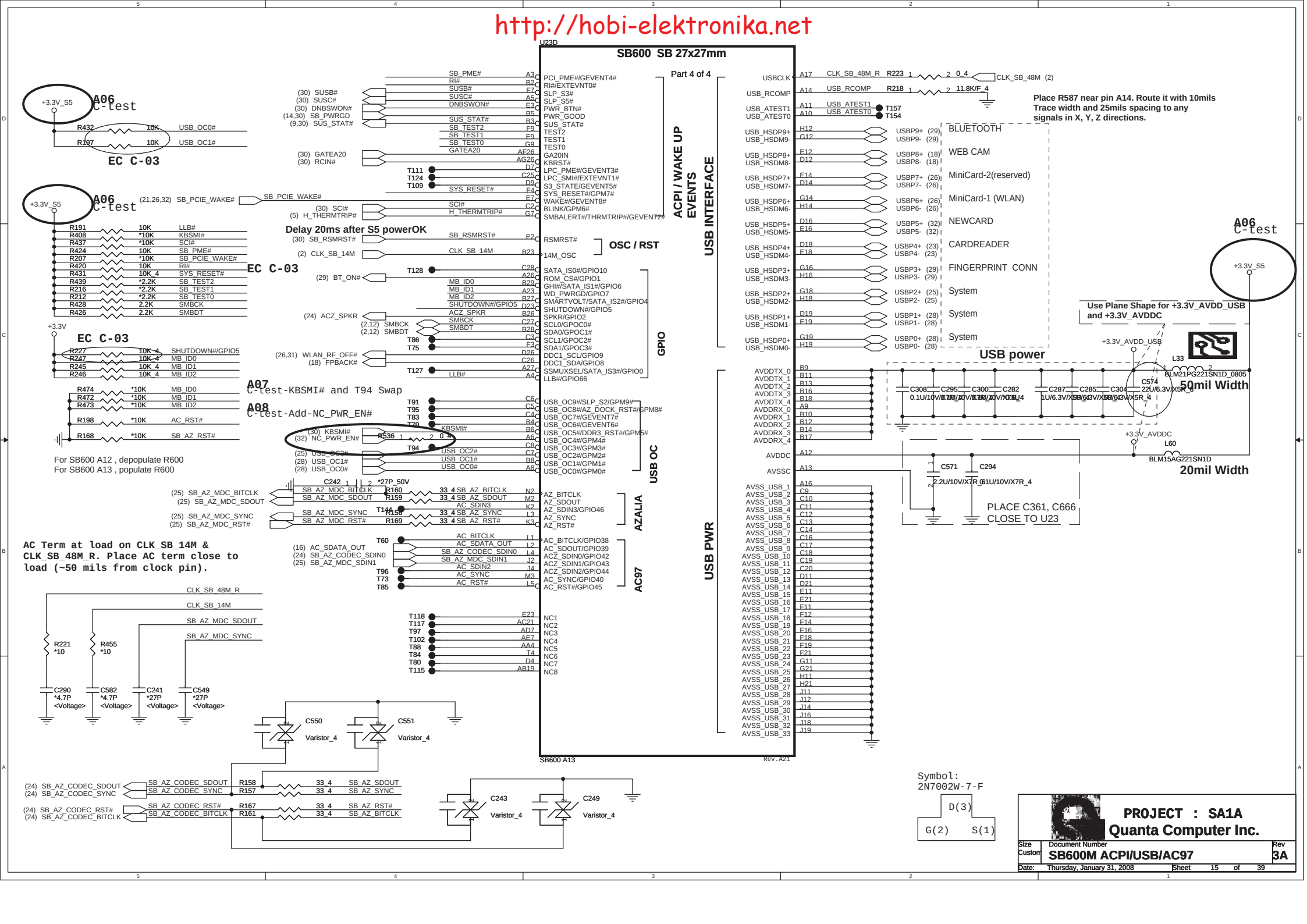
Option to "Disable" clkrun. Pulling it down will keep the clocks running.

RTC

A05
C-test-Pin define

SB600 A13
Rev.A21

PROJECT : SA1A			
Quanta Computer Inc.			
Size: Custom	Document Number: SB600M-PCIE/PCI/LPC		Rev: 3A
Date: Thursday, January 31, 2008	Sheet 14 of 39		



SB600 SB 27x27mm

Part 2 of 4

U23B

SATA clock

C292 27P/50V/NPO_4 — Y5 25MHZ — R224 10M_4 — C323 27P/50V/NPO_4

SATA_X1 / SATA_X2

SATA Power

+3.3V — L31 BLM15AG221SN1D — C305 1U/10V/X6S_6 — C311 *0.1U

CAP CLOSE TO THE BALL OF SB600

+1.2V — L32 BLM15AG221SN1D — C289 1U/6.3V/X5R_4 — C296 *0.1U — C280 22U/6.3V/X5R_8

+1.2V — L34 BLM21PG221SN1D <Size> — C328 22U/6.3V/X5R_8 — C314 1U/6.3V/X5R_4 — C320 1U/6.3V/X5R_4 — C318 0.1U/10V/X7R_4 — C312 0.1U/10V/X7R_4

+1.2V_AVDD_SATA — C324 *0.1U — C298 *0.1U — C301 *0.1U

SERIAL ATA

(27) SATA_TX0+	C586 0.01U/16V/X7R_4 SATA_TX0+_C — AH21 SATA_TX0+
(27) SATA_TX0-	C584 0.01U/16V/X7R_4 SATA_TX0-_C — AJ21 SATA_TX0-
(27) SATA_RX0-	SATA_RX0- — AH20 SATA_RX0-
(27) SATA_RX0+	SATA_RX0+ — AJ20 SATA_RX0+
	T167 — AH18 SATA_TX1+
	T163 — AJ18 SATA_TX1-
	T162 — AH17 SATA_RX1-
	T161 — AJ17 SATA_RX1+
	T114 — AH13 SATA_TX2+
	T112 — AH14 SATA_TX2-
	T113 — AH16 SATA_RX2-
	T160 — AJ16 SATA_RX2+
	T156 — AJ11 SATA_TX3+
	T155 — AH11 SATA_TX3-
	T158 — AH12 SATA_RX3-
	T159 — AJ13 SATA_RX3+

+5V — R206 4.7K_4 — +3.3V — R192 4.7K_4 — R215 1K/F_4 <Tolerance> — SATA_CAL — AF12 SATA_CAL

SATA_X1 — AD16 SATA_X1

SATA_X2 — AD18 SATA_X2

(31) SATA_LED# — Q13 MMBT3904 — SATA_ACT# — AC12 SATA_ACT#/GPIO67

+1.2V_PLLVDD_SATA — AD14 PLLVDD_SATA_1 / AJ10 PLLVDD_SATA_2

+3.3V_XTLVDD_SATA — AC16 XTLVDD_SATA

+1.2V_AVDD_SATA — AE14 AVDD_SATA_1 / AE16 AVDD_SATA_2 / AE18 AVDD_SATA_3 / AE19 AVDD_SATA_4 / AE19 AVDD_SATA_5 / AE21 AVDD_SATA_6 / AG22 AVDD_SATA_7 / AG23 AVDD_SATA_8 / AH22 AVDD_SATA_9 / AH23 AVDD_SATA_10 / AJ12 AVDD_SATA_11 / AJ14 AVDD_SATA_12 / AJ19 AVDD_SATA_13 / AJ22 AVDD_SATA_14 / AJ23 AVDD_SATA_15

AVSS_SATA_1 AB14 / AVSS_SATA_2 AB16 / AVSS_SATA_3 AB18 / AVSS_SATA_4 AC14 / AVSS_SATA_5 AC18 / AVSS_SATA_6 AC19 / AVSS_SATA_7 AD12 / AVSS_SATA_8 AD19 / AVSS_SATA_9 AD21 / AVSS_SATA_10 AE12 / AVSS_SATA_11 AE21 / AVSS_SATA_12 AE11 / AVSS_SATA_13 AE14 / AVSS_SATA_14 AE16 / AVSS_SATA_15 AE18 / AVSS_SATA_16 AG11 / AVSS_SATA_17 AG12 / AVSS_SATA_18 AG13 / AVSS_SATA_19 AG14 / AVSS_SATA_20 AG16 / AVSS_SATA_21 AG17 / AVSS_SATA_22 AG18 / AVSS_SATA_23 AG19 / AVSS_SATA_24 AG20 / AVSS_SATA_25 AG21 / AVSS_SATA_26 AH10 / AVSS_SATA_27 AH19

SERIAL ATA POWER

SB600 A13

ATA 66/100

IDE_IORDY	AB29 IDE_DIORDY (27)
IDE_IRQ	AA28 IDE_IRQ (27)
IDE_A0	AA29 IDE_DA0 (27)
IDE_A1	AB27 IDE_DA1 (27)
IDE_A2	Y28 IDE_DA2 (27)
IDE_DACK#	AB28 IDE_DDACK# (27)
IDE_DRQ	AC27 IDE_DDREQ (27)
IDE_IOR#	AC29 IDE_DIOR# (27)
IDE_IOW#	AC28 IDE_DIOW# (27)
IDE_CS1#	W28 IDE_DCS1# (27)
IDE_CS3#	W27 IDE_DCS3# (27)
	IDE_DD[0..15] (27)
IDE_D0/GPIO15	AD28 IDE_DD0
IDE_D1/GPIO16	AD26 IDE_DD1
IDE_D2/GPIO17	AE29 IDE_DD2
IDE_D3/GPIO18	AE27 IDE_DD3
IDE_D4/GPIO19	AG29 IDE_DD4
IDE_D5/GPIO20	AH28 IDE_DD5
IDE_D6/GPIO21	AJ28 IDE_DD6
IDE_D7/GPIO22	AJ27 IDE_DD7
IDE_D8/GPIO23	AH27 IDE_DD8
IDE_D9/GPIO24	AG27 IDE_DD9
IDE_D10/GPIO25	AG28 IDE_DD10
IDE_D11/GPIO26	AE28 IDE_DD11
IDE_D12/GPIO27	AF29 IDE_DD12
IDE_D13/GPIO28	AE28 IDE_DD13
IDE_D14/GPIO29	AD25 IDE_DD14
IDE_D15/GPIO30	AD29 IDE_DD15

A10 C-test-Change

SPI ROM

SPI_DI/GPIO12	J3 — T87
SPI_DO/GPIO11	J6 — T63
SPI_CLK/GPIO47	G3 — T76
SPI_HOLD#/GPIO31	G2 — T67
SPI_CS#/GPIO32	G6 — T100
LAN_RST#/GPIO13	C23 — T168
ROM_RST#/GPIO14	G5 — T99

HW MONITOR

FANOUT0/GPIO3	M4 — T103
FANOUT1/GPIO48	T3
FANOUT2/GPIO49	V4
FANIN0/GPIO50	N3 — T77
FANIN1/GPIO51	P2 — T72
FANIN2/GPIO52	W4 — T82
TEMP_COMM	P5 — R429 0_4
TEMPIN0/GPIO61	P7 — T71
TEMPIN1/GPIO62	P8 — T105
TEMPIN2/GPIO63	T8 — T107
TEMPIN3/TALERT#/GPIO64	T7 — R163 0_4 SB_CPU_PROCHOT# — SB_CPU_PROCHOT# (5)
VIN0/GPIO53	V5 — THERM_ALERT# (5)
VIN1/GPIO54	L7 — LAN_DISABLE# (21)
VIN2/GPIO55	M8 LOM_PCIE_RST# — T110
VIN3/GPIO56	V6 NC_GPIO56 — T98
VIN4/GPIO57	M6 LBF_ID0
VIN5/GPIO58	P4 LBF_ID1
VIN6/GPIO59	M7 LBF_ID2
VIN7/GPIO60	V7

BIOS should not enable the internal GPIO pull up resistor

+3.3V_AVDD_HWM — L30 BLM15AG221SN1D — +3.3V

AVDD N1 — 20mil Width — C265 2.2U/10V/X5R_6 — C270 0.1U/10V/X7R_4 — L65 *BLM15AG221SN1D — +3.3V_S5

AVSS M1

HWM_AGND — R166 0_4 — Close to SB600

HWM_AGND TRACE AT LEAST 10MIL WIDE

B04 Requirement from AMD.

REQUIRED STRAPS

15K internal PU for RTC_CLK
,External PU/PD is not required.
SB600 has 15K internal PD for AC_SDOUT

+3.3V — R145 *2.2K — R397 *10K — R396 10K_4 — R194 *10K_4 — R146 10K

(15) AC_SDATA_OUT
(14) CLK_PCI_DOCK
(14,26) PCLK_LPC_DEBUG
(14) PCI_CLK0
(14) PCI_CLK1

A09 C-test-Del — A09 C-test-Add

R398 10K_4 — R182 10K — R147 *10K_4

A09 C-test-Add — A09 C-test-Del

Net Name	AC_SDOUT	CLK_PCI_DOCK	CLK_PCI_PCCARD	PCI_CLK0 PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 Default	H, H = PCI ROM Default H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM
PULL LOW	IGNORE DEBUG STRAPS Default	USE EXT. 48MHZ Default	CPU IF=P4	

+3.3V — R144 *10K — R155 *10K — R152 *10K

R143 10K_4 — LBF_ID0
R154 10K_4 — LBF_ID1
R153 10K_4 — LBF_ID2

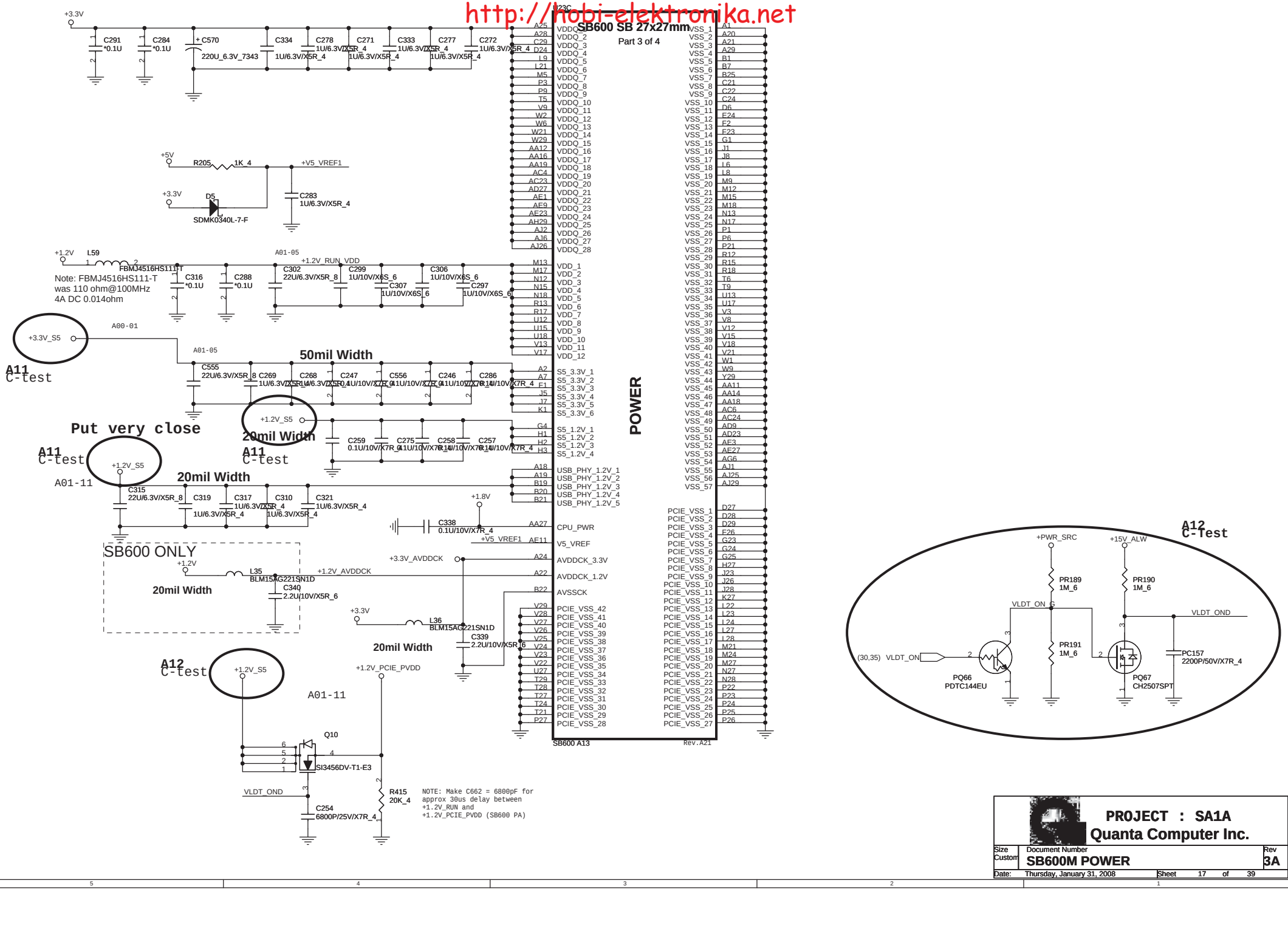
Memory Vendor	LBF_ID2	LBF_ID1	LBF_ID0
Hynix	0	0	0
Qimonda	0	0	1
Samsung	0	1	0

NC_GPIO56	R162	*20K
THERM_ALERT#	R202	*20K
LAN_DISABLE#	R208	*20K
LOM_PCIE_RST#	R214	*20K

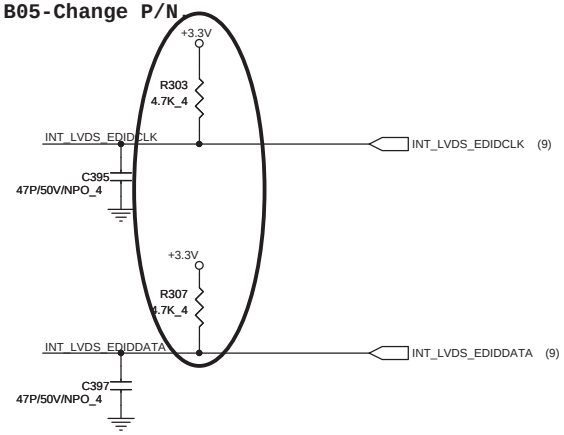
PROJECT : SA1A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB600M HDD/POWER	3A

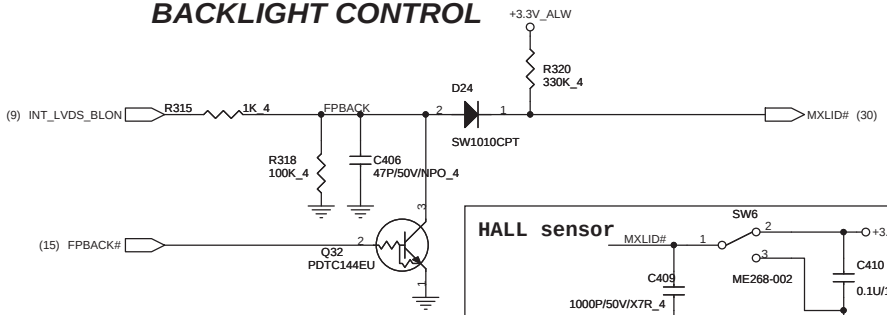
Date: Thursday, January 31, 2008 Sheet 16 of 39



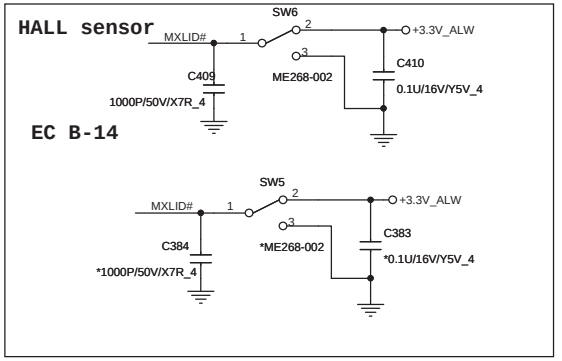
B05-Change P/N



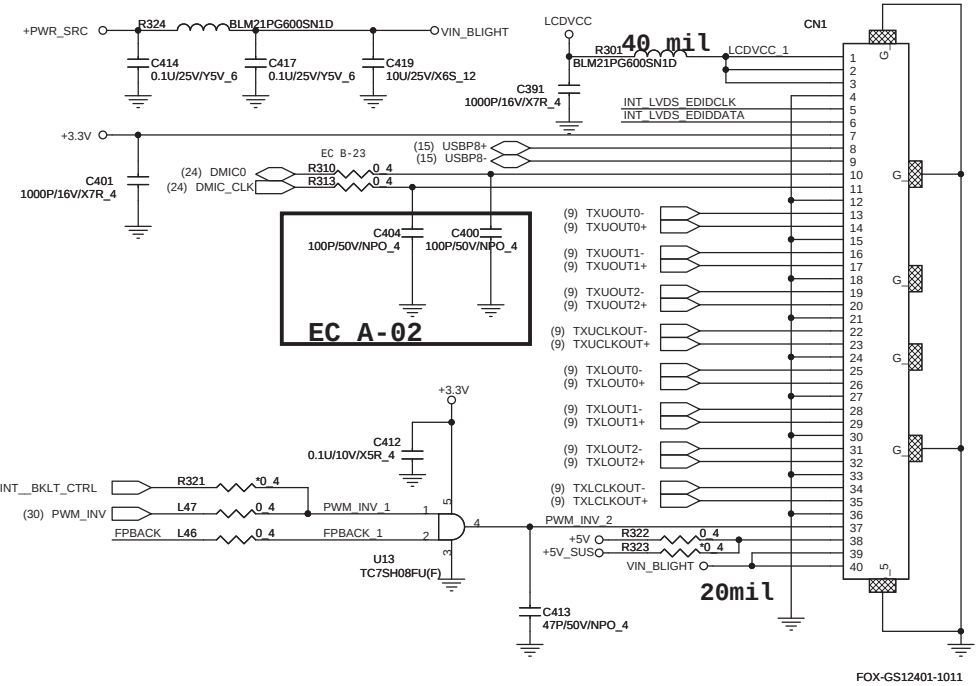
BACKLIGHT CONTROL



HALL sensor

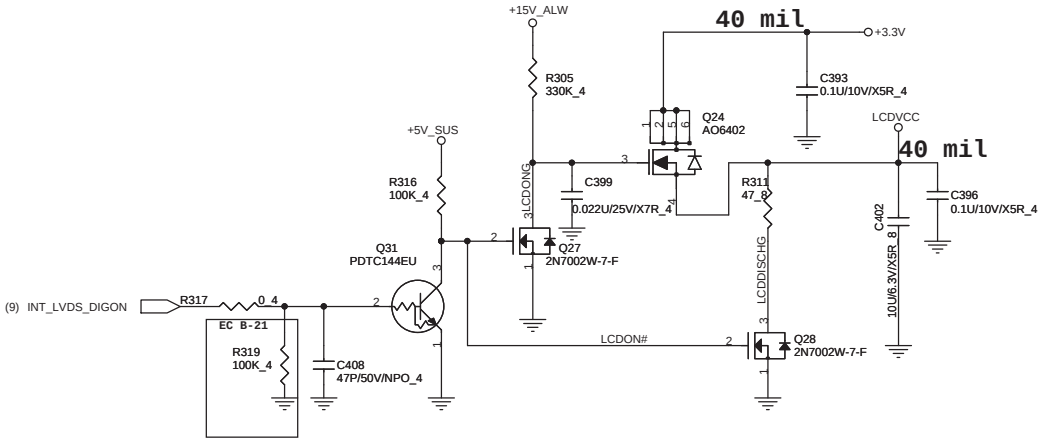


LCD CONNECTOR(Include WEB CAM function)

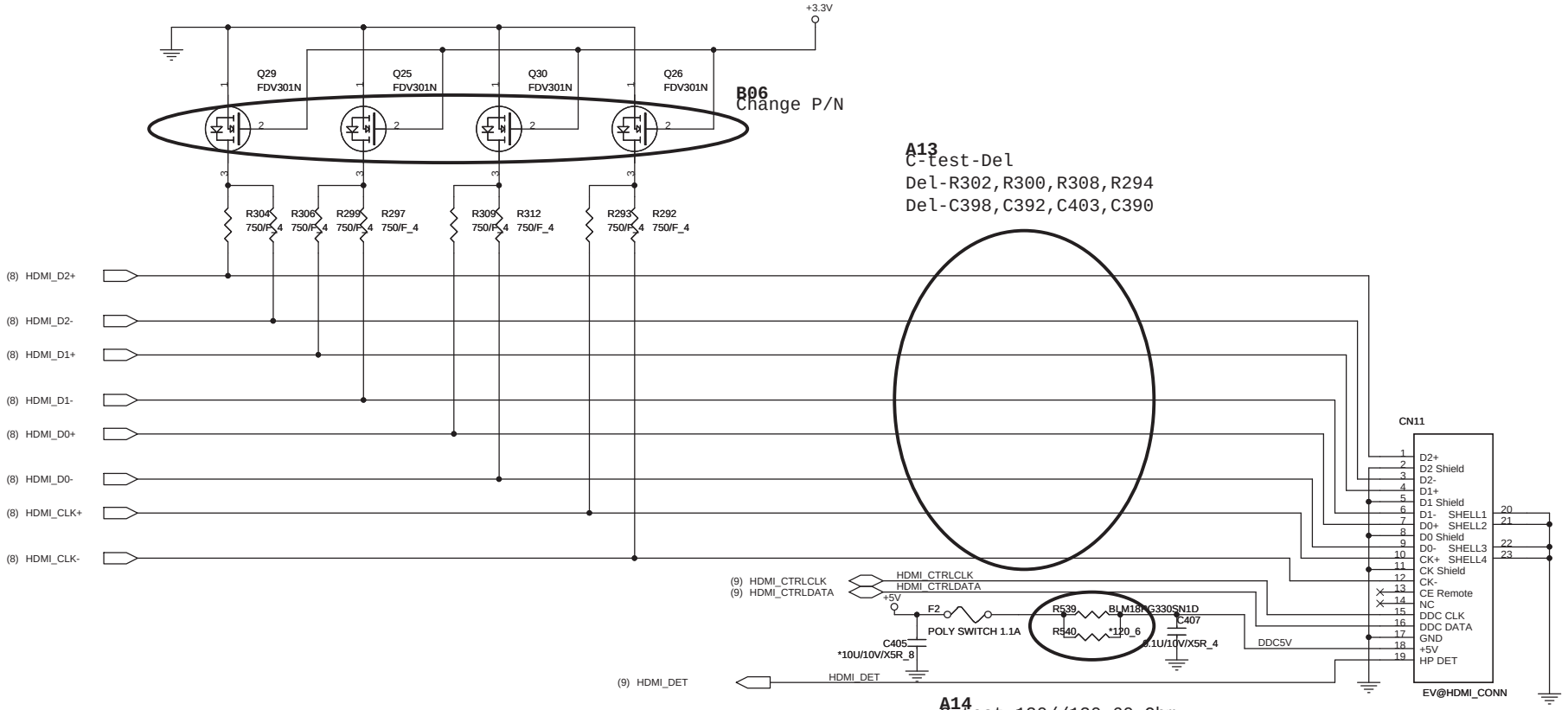


TO PANEAL

PANEL VCC CONTROL



Quanta Computer Inc.	PROJECT : SA1A	
Size: Custom	Document Number: LVDS/LCD CONN/LID/WEB CAM	Rev: 3A
Date: Thursday, January 31, 2008	Sheet 18 of 39	



LANCELOT

PROJECT : SA1A Quanta Computer Inc.		
Size: Custom	Document Number: HDMI CONNECTOR	Rev: 3A
Date: Thursday, January 31, 2008	Sheet 19 of 39	

CRT PORT

EC C-05

+3.3V R296 4.7K_4

(9) INT_CRT_DDCCLK

Q22 2N7002E

+5V

C394 0.1U/16V/Y5V_4

(9) INT_VSYNC

Q20 RHU002N06

DDCCLK

CRT_VS_1

(9) INT_HSYNC

Q23 RHU002N06

CRT_HS_1

DDCDAT

(9,14,21,26,27,32) PLTRST#

U12 TC7SH08FU(F)

+5V R298 *2.2K_4

+3.3V R295 4.7K_4

(9) INT_CRT_DDCDAT

Q21 2N7002E

EC C-05

D22 EC10QS04

F1 POLY SWITCH 1.1A

CRTVDD2

L45 PBY201209T-330Y-N

CRTVDD_5V

C387 0.1U/10V/X7R_4

CN9 CRT_CONN

(9) INT_CRT_RED

(9) INT_CRT_GRN

(9) INT_CRT_BLU

L4 BK1608LL300 CRT_R_1

L5 BK1608LL300 CRT_G_1

L6 BK1608LL300 CRT_B_1

CRT_SENSE#

T1

C5 *180P

T2

R5 150/F_4

R6 150/F_4

R7 150/F_4

C7 *5.6P/50V_4

C8 *5.6P/50V_4

C9 *5.6P/50V_4

C2 5.6P/50V_4

C1 5.6P/50V_4

C3 5.6P/50V_4

CRTVDD_5V

D20 RB501H

EC C-06

R1 6.8K_4 DDCCLK

R4 6.8K_4 DDCDAT

DDCCLK L2 BK1608HM121 DDCCLK_2

CRT_VS1 L1 BK1608HM121 CRT_VS_2

CRT_HS1 L3 BK1608HM121 CRT_HS_2

DDCDAT L7 BK1608HM121 DDCDAT_2

C389 *33P

C388 *33P

C6 *33P

C4 *33P

CRTVDD_5V

C10 0.1U/10V/X7R_4

R291 1K_4

U10 AHCT1G125DCH

CRT_VS_1

CRT_VS0 R2 10_4 CRT_VS1

CRT_HS_1

CRT_HS0 R3 10_4 CRT_HS1

U11 AHCT1G125DCH

Layout Note:
Place near U < 200 mil

ESD PORTECTION

CRTVDD_5V +3.3V

D16 *BC000204Z21 CRT_R_1

D17 *BC000204Z21 CRT_G_1

D18 *BC000204Z21 CRT_B_1

D15 *BC000204Z21 CRT_VS_2

D19 *BC000204Z21 CRT_HS_2

D23 *BC000204Z21 DDCCLK_2

D21 *BC000204Z21 DDCDAT_2

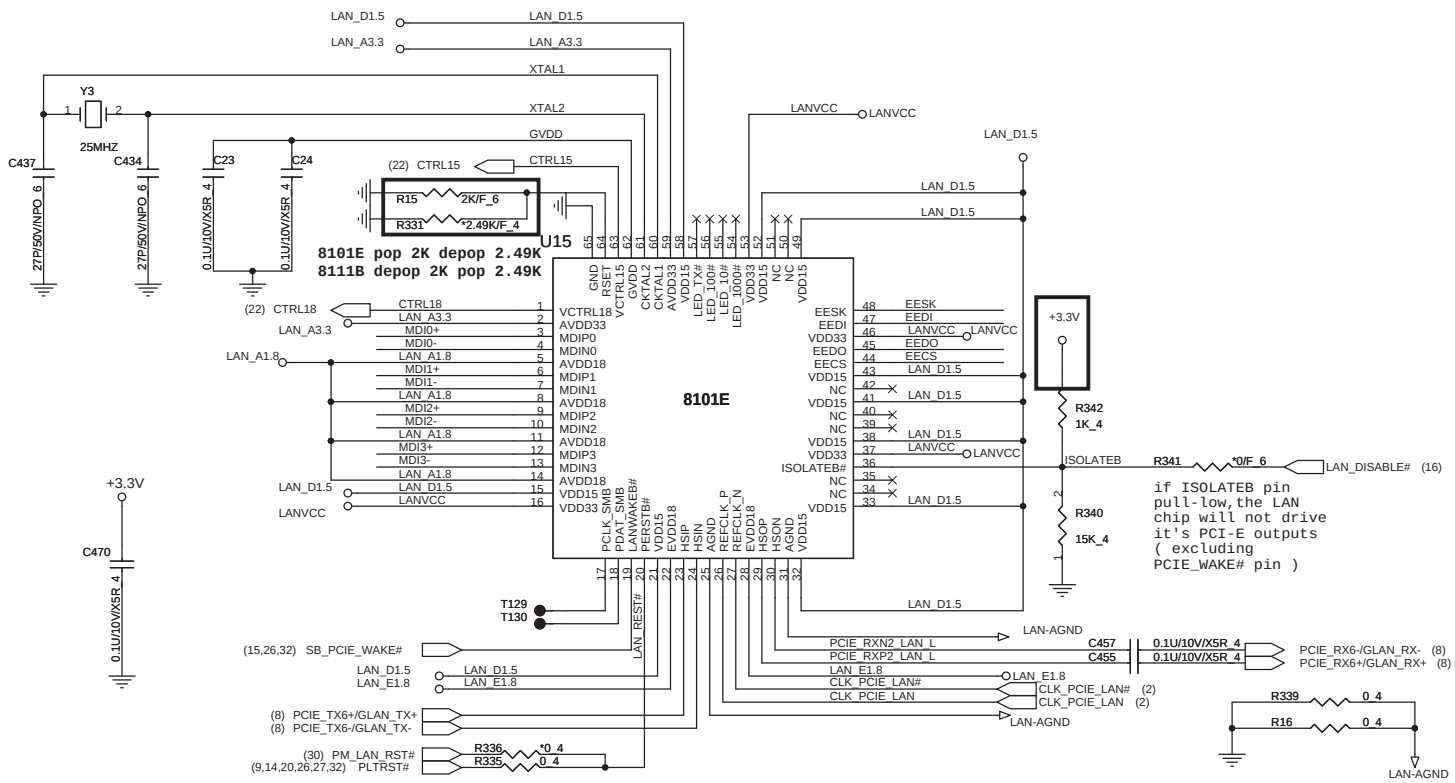
PROJECT : SA1A

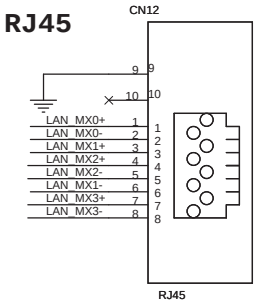
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT PORT	3A

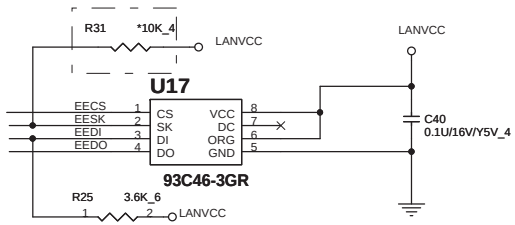
Date: Thursday, January 31, 2008 Sheet 20 of 39

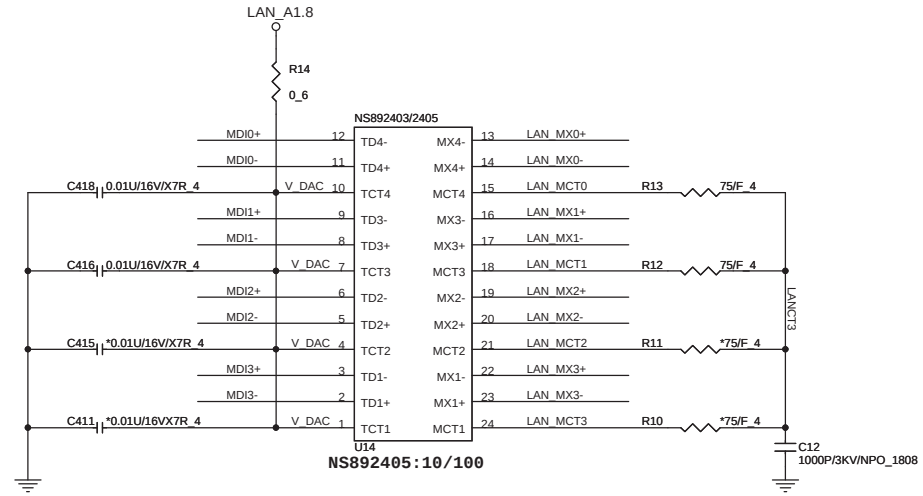
E : Stuffed for 8101E(10/100)



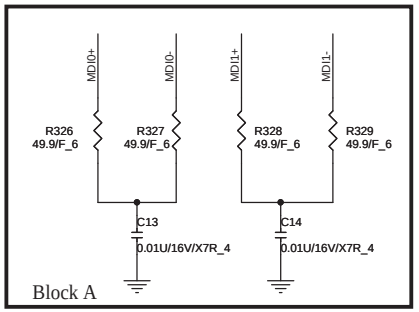


for 93C56 used. NC if 93C46 is used.





BLOCK A is only for RTL8101E application.



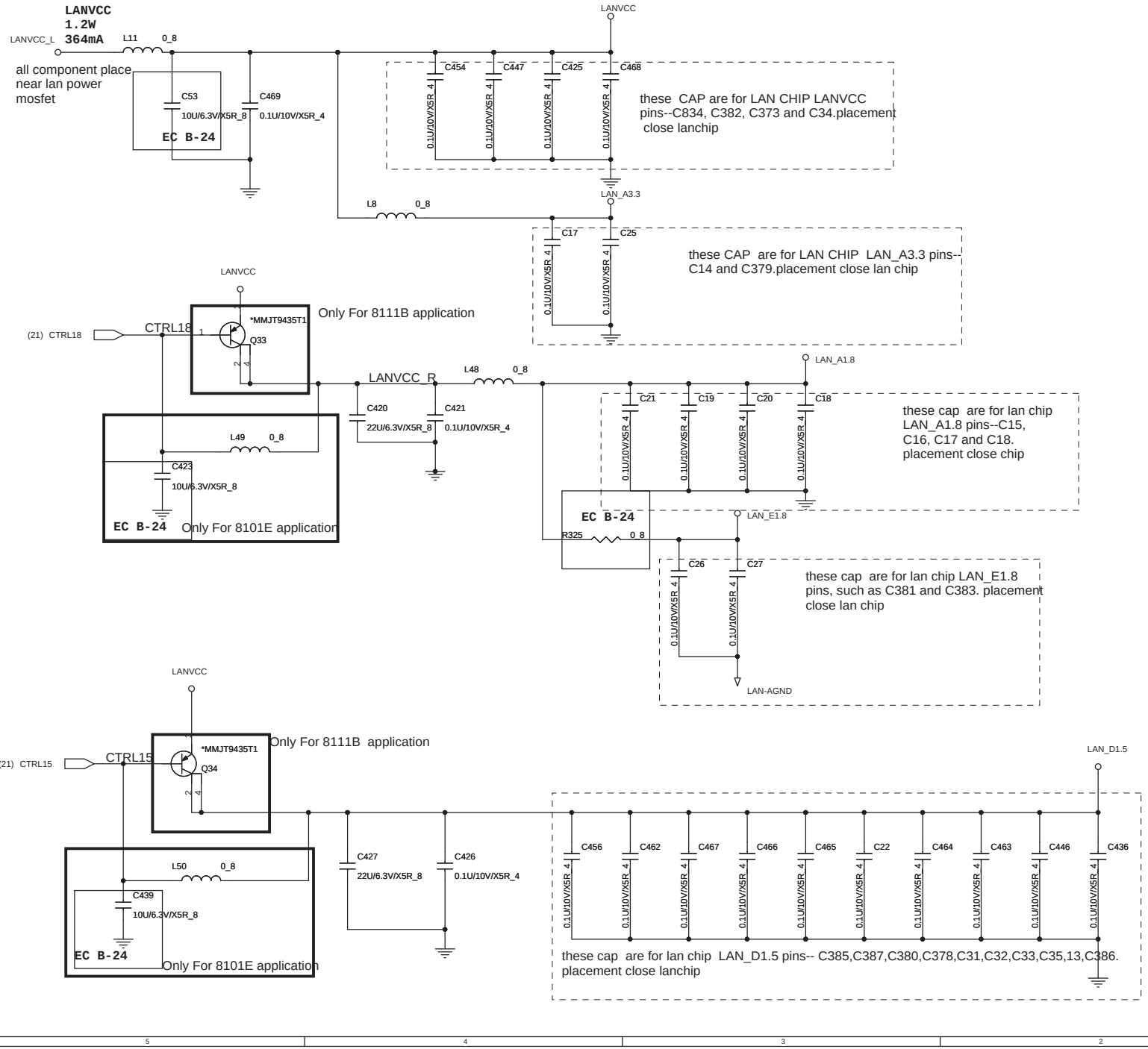
	10/100M	1G
R14 R15 R16 R17	ASM	NoASM

PROJECT : SA1A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN(REALTEK 8101E)	3A
Date: Thursday, January 31, 2008	Sheet 21 of 39	

T : Stuffed for RTL8111B(10/100/1000)

E : Stuffed for 8101E(10/100)



Power domain chart

	RTL8111B / RTL8101E
LANVCC	*3.3V*
LAN_D1.8	*1.8V*
LAN_A1.8	*1.8V*
LAN_D1.5	*1.5V*

	Q23	Q24
RTL8111B	*Need*	*Need*
RTL8101E	*N/A*	*N/A*

PROJECT : SA1A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN POWER	3A
Date: Thursday, January 31, 2008	Sheet 22 of 39	

Note:

	SD/MMC	MS	XD
SP0			
SP1	SD_WP		XD_CD#
SP2			
SP3	SD_CD#		
SP4			XD_D4
SP5		MS_BS	XD_D5
SP6	SD_DAT1	MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14			XD_R/B#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

U9

Realtek RTS5158

A15
C-test-Change

A16
C-test-Del R230 and Add new one

7 IN1 CARD-READER (PUSH-PUSH)

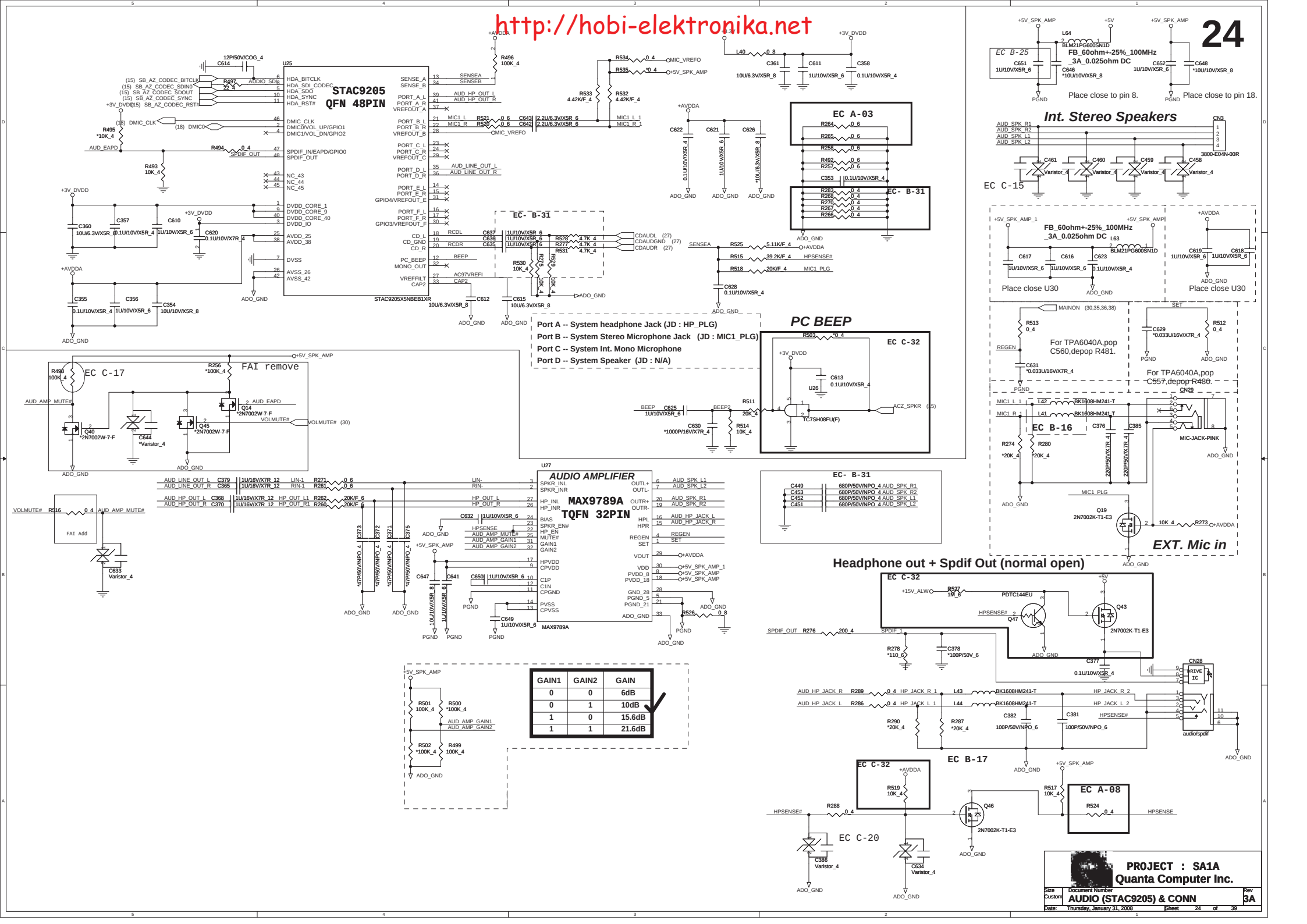
Support SD/MS/xD/SM/RS-MMC/MMC/miniSD Cards

SP0	R233	56_4	SM_CD#
SP1	R190	56_4	XD_CD#
SP2	R181	56_4	SD_WP
SP3	R170	56_4	SD_CD#
SP4	R213	56_4	XD_D4
SP5	R220	56_4	XD_D5/MS_BS
SP6	R222	56_4	SD_DAT1/XD_D3/MS_D1
SP7	R209	56_4	SD_DAT0/XD_D6/MS_D0
SP8	R225	56_4	SD_DAT7/XD_D2/MS_D2
SP9	R228	56_4	MS_INS#
SP10	R204	56_4	MS_D3/SD_DAT6/XD_D7
SP11	R219	56_4	XD_D1/SD_CLK/MS_SCLK
SP12	R237	56_4	SD_DAT5/XD_D0
SP13	R240	56_4	SD_DAT4/XD_WP#
SP14	R248	56_4	XD_R/B#
SP15	R231	56_4	SD_DAT3/XD_WE#
SP16	R235	56_4	SD_DAT2/XD_RE#
SP17	R241	56_4	XD_ALE
SP18	R243	56_4	XD_CE#
SP19	R242	56_4	XD_CLE

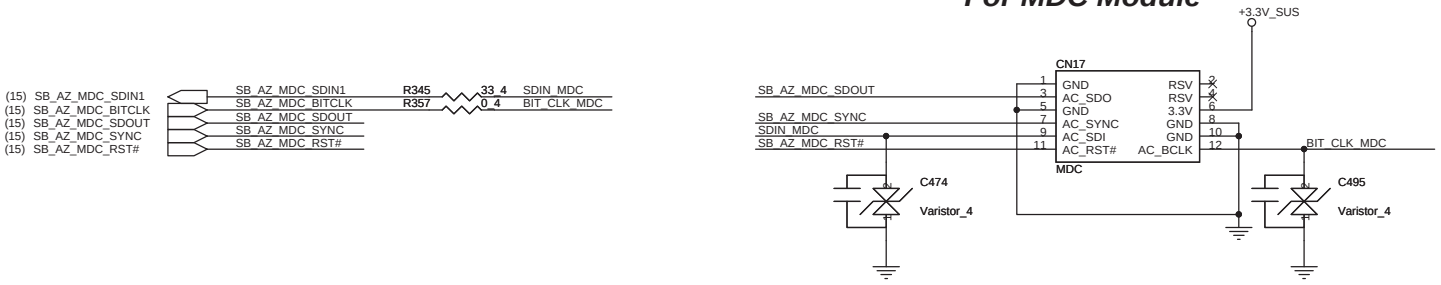
CN8

R015-212-LM

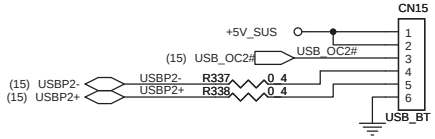
Project	PROJECT : SA1A
Company	Quanta Computer Inc.
Size	Custom
Document Number	REALTEK RTS5158
Rev	3A
Date:	Thursday, January 31, 2008
Sheet	23 of 39



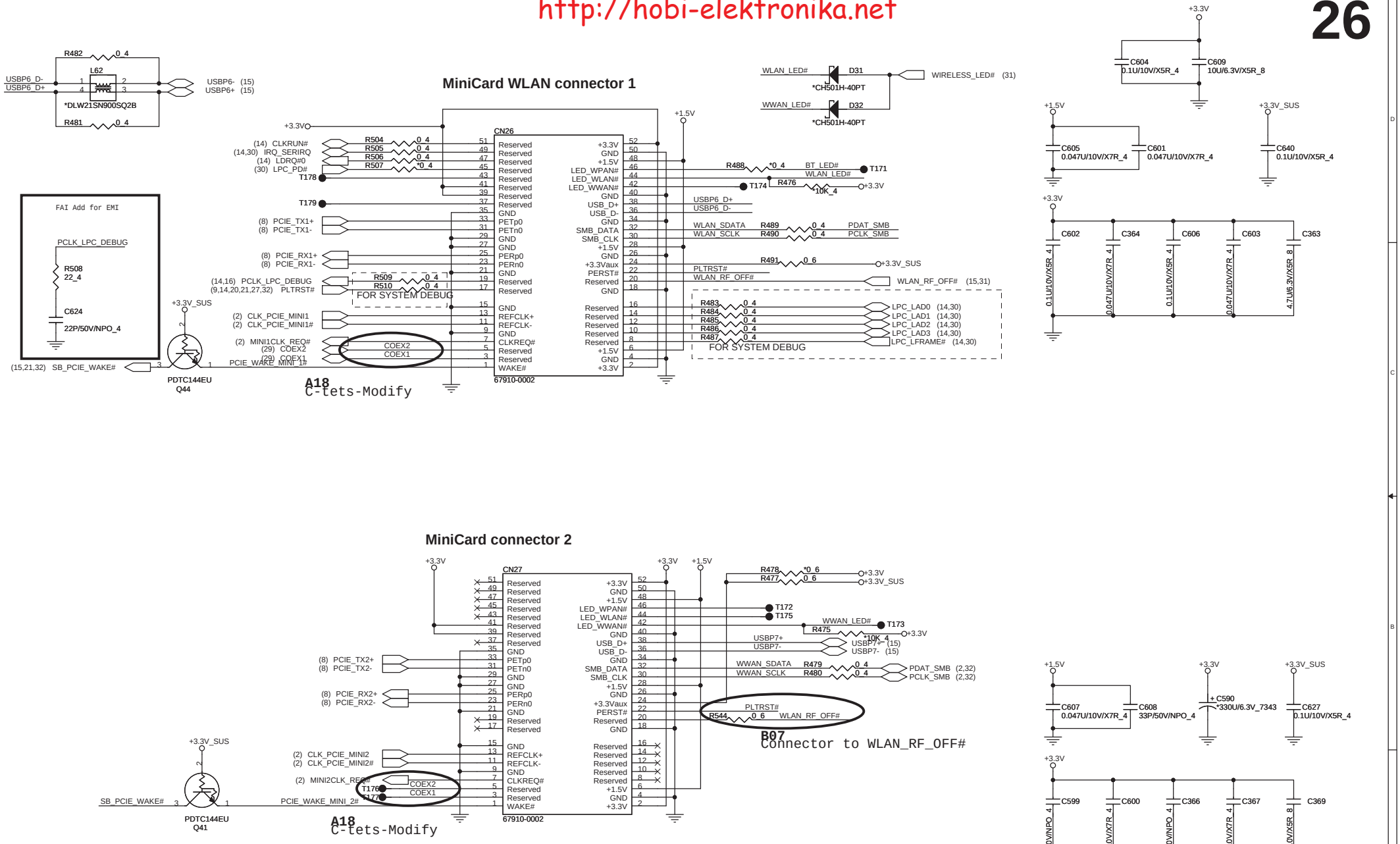
For MDC Module

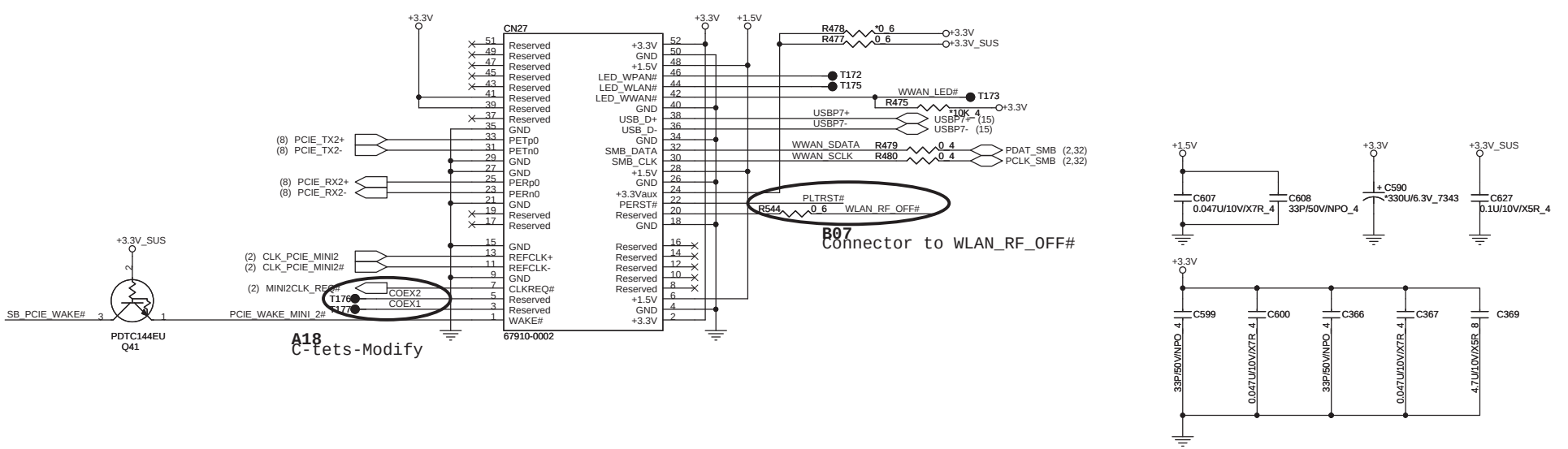


TO RJ11/USB PORT



	PROJECT : SA1A Quanta Computer Inc.	
Size: Custom	Document Number: MODEM(MDC)/RJ11 BOARD	Rev: 3A
Date: Thursday, January 31, 2008	Sheet 25 of 39	



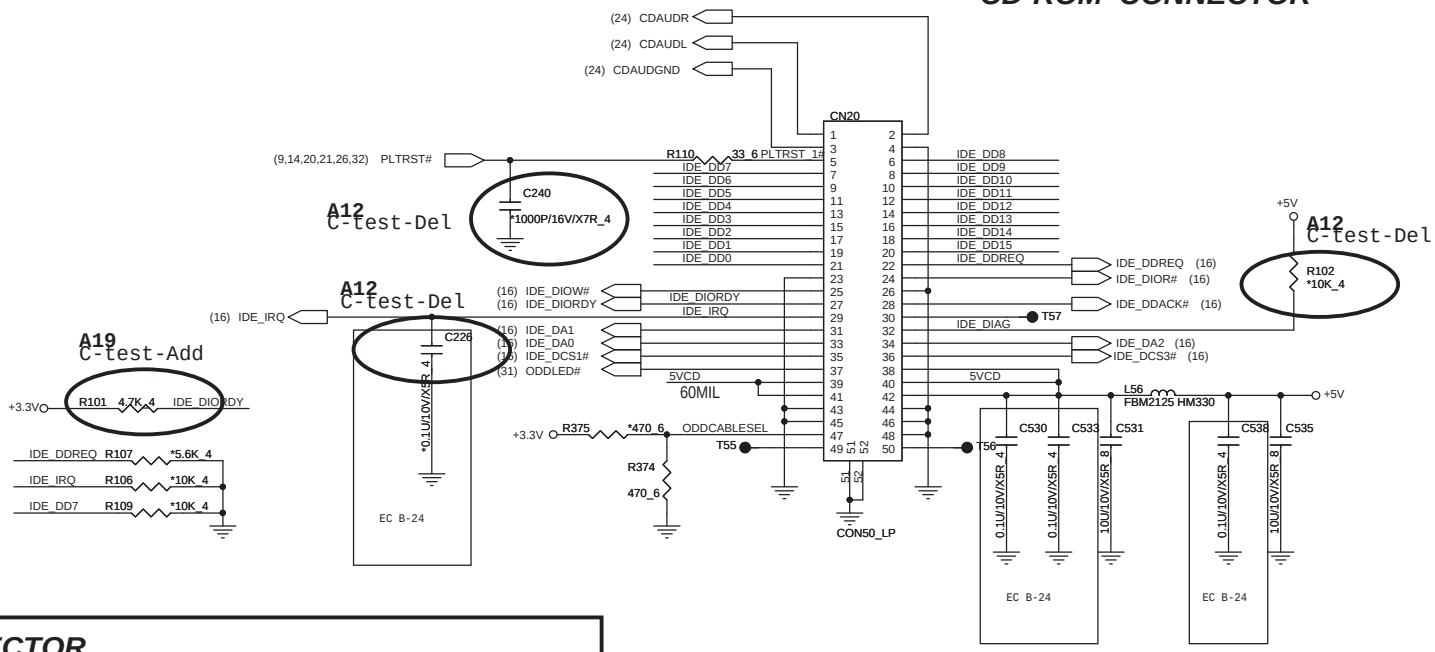


	PROJECT : SA1A Quanta Computer Inc.	
Size: Custom	Document Number: MINI PCI-E Card	Rev: 3A
Date: Thursday, January 31, 2008	Sheet 26 of 39	

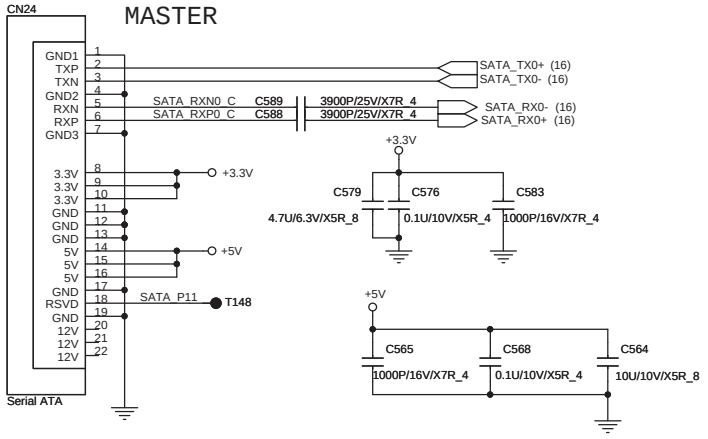
(16) IDE_DD[0..15] IDE_DD[0..15]

For fix ODD

CD-ROM CONNECTOR



SATA CONNECTOR



PROJECT : SA1A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA HDD,ODD	3A
Date: Thursday, January 31, 2008	Sheet 27 of 39	

NB SCREW HOLE

HOLE12 H-C236D142P2

HOLE17 H-C236D142P2

MINI PCI-E SCREW HOLE 2

HOLE21 H-C236D142P2

HOLE24 H-C236D142P2

MINI PCI-E SCREW HOLE 1

HOLE23 H-C236D142P2

HOLE22 H-C236D142P2

MDC SCREW HOLE

HOLE11 H-C236D142P2

HOLE7 H-TC236BS4D142P2

CPU SCREW HOLE

HOLE10 *h-ts315bs256d169p2

HOLE15 *h-ts315bs256d169p2

HOLE9 *h-ts315bs256d169p2

HOLE14 *h-ts315bs256d169p2

USB-0

60MIL

(14,18,23,25,34,37,38) +5V_SUS

+5V_SUS

U18 CM3512-04SN

VCC, OUT1, OUT2, EN1, EN2, GND, OC1, OC2

USB0PWR C476 4.7U/10V/Y5V_8

USB1PWR C494 4.7U/10V/Y5V_8

USB_OC0# (15)

USB_OC1# (15)

USB0PWR

C56 Varistor_4

C54 0.1U/10V/X5R_4

C488 100U/6.3V/TAN_6

USBP_0-

USBP_0+

CN16 USB_CONN_straddle

C471 Clamp-Diode_4

C472 Clamp-Diode_4

EC E-33

FAI Change to 0402

USB-1

(15) USBP0-

(15) USBP0+

(15) USBP1-

(15) USBP1+

R343 0_4 USBP_0-

R344 0_4 USBP_0+

R330 0_4 USBP_1-

R334 0_4 USBP_1+

EC B-08

USB1PWR

C15 Varistor_4

C16 0.1U/10V/X5R_4

C422 100U/6.3V/TAN_6

USBP_1-

USBP_1+

CN14 USB_CONN_straddle

C424 Clamp-Diode_4

C435 Clamp-Diode_4

EC E-33

FAI Change to 0402

EMI Use

EC A-01

+3.3V

EC33 EC62 EC50 EC9 EC7 0.1U/10V/X5R_4

EC32 EC34 EC35 EC28 0.1U/10V/X5R_4 SI Use

EC20 0.1U/10V/X5R_4

EC21 EC61 EC29 *0.1U/10V_4

EC24 EC27 0.1U/10V/X5R_4

+5V_SUS

EC17 EC19 EC66 EC18 EC48 EC51 EC60 EC58 EC57 0.1U/10V/X5R_4

EC22 0.1U/10V/X5R_4

+1.8V

EC15 EC16 EC13 0.1U/10V/X5R_4

EC59 *0.1U/10V_4

EC12 *0.1U/10V_4

+1.8V_AN_A1.8

EC6 EC8 EC53 0.1U/10V/X5R_4

EC54 *0.1U/10V_4

EC3 *0.1U/10V_4

+PWR_SRC

EC B-30

EC63 EC4 EC56 EC55 EC46 EC45 EC52 EC5 EC64 EC10 1000P/50V/X7R_4

+3.3V_ALW

EC2 EC44 EC65 EC1 EC23 EC43 EC14 EC11 0.1U/10V/X5R_4

+15V_ALW

EC67 EC26 EC37 EC47 EC41 EC42 EC38 EC49 0.1U/25V/X5R_4

EC B-30

+PWR_SRC

EC40 EC39 EC36 EC30 EC31 1000P/50V/X7R_4

HOLE1 *h-ts4bs8d110p2

HOLE2 *h-ts8bs8d110p2

HOLE8 *h-ts1-be354x354d110p2

HOLE6 *h-ts7bs8d110p2

HOLE16 *H-TS354BC280D110P2

HOLE3 *h-c118d118n

HOLE5 *H-C98D98N

HOLE26 *H-TS314BS1D110P2

HOLE27 *h-te433bs354d110p2

HOLE25 *H-TC276BC354D110P2

HOLE4 *h-ts5bs6d110p2

HOLE13 *h-bb355x453d197x295p2

HOLE18 *h-ts2bs2d110p2

C-test-Modify

HOLE28 *H-C236D110P2

ADO_GND

HOLE20 *h-ts314bs354d119p2

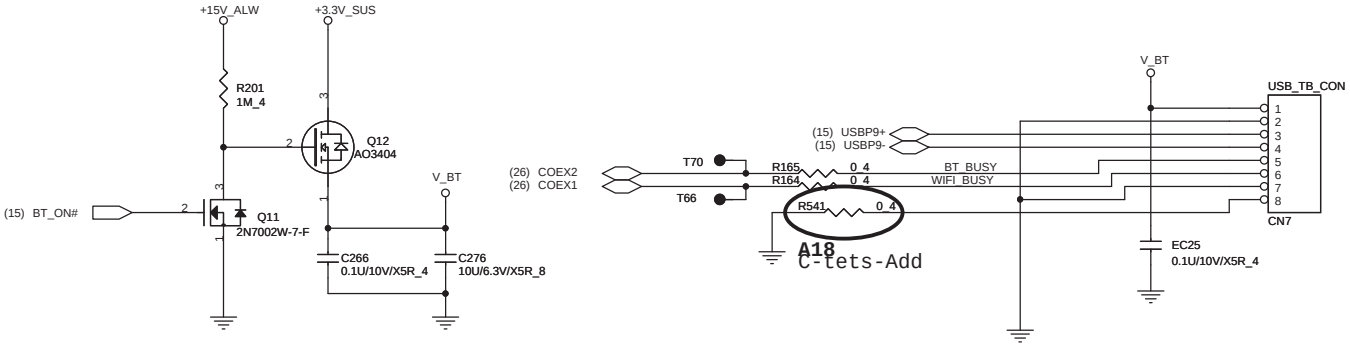
HOLE19 *H-TC276TD110RB

PROJECT : SA1A

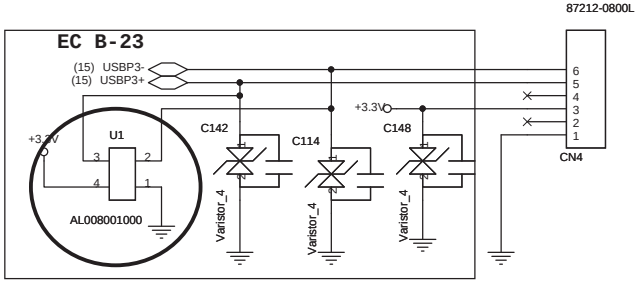
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB CONN & HOLE	3A
Date: Thursday, January 31, 2008	Sheet 28 of 39	

BLUETOOTH CONNECTOR



FINGERPRINT CONNECTOR



PROJECT : SA1A Quanta Computer Inc.		
Size: Custom	Document Number: BT/FG/CONNECTOR	Rev: 3A
Date: Thursday, January 31, 2008	Sheet 29 of 39	

IT8512

POWER SWITCH

A21 C-test-Swap

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

TMKBC Function	
High	Enable
Low	Disable

R3444	FLASH TYPE SELECT
High	LPC/FWH FLASH ROM
Low	SPI FLASH ROM (Default)

Layout Note:
Place all capacitors close to IT8512.

Layout Note:
net "3VPCU" and "RTC_VCC" minimum trace width 12mils.

(For PLL Power)

Layout Note:
Place R428,R416,R420 within 500 mils from SPI Flash.

Please reserve this connector for serial debug port & KBS download usage.

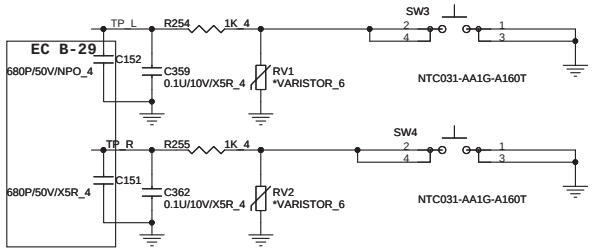
Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

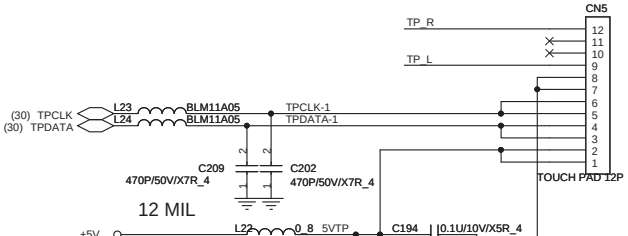
RF ON/OFF SLIDE SWITCH

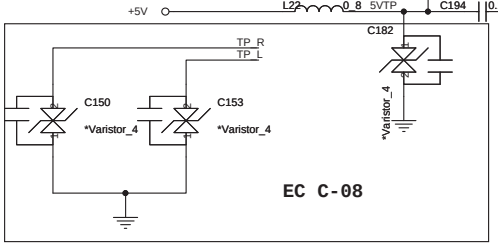
8Mbit (1M Byte), SPI

PROJECT :	SA1A
Quanta Computer Inc.	
Size: Custom	Document Number: KBC-IT8502
Rev:	3A
Date: Thursday, January 31, 2008	Sheet 30 of 39

TOUCHPAD SWITCH CONN

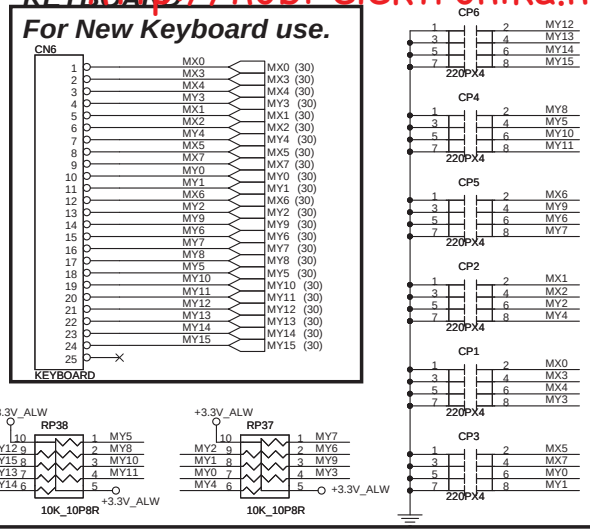




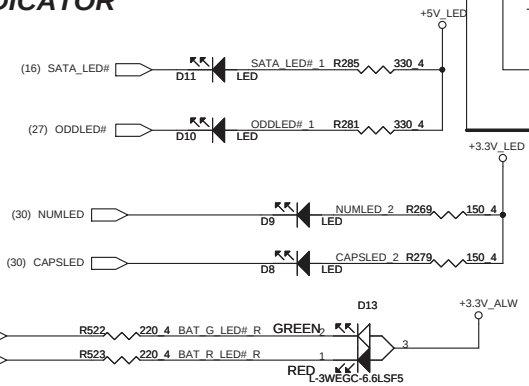


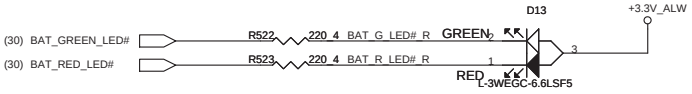
KEYBOARD

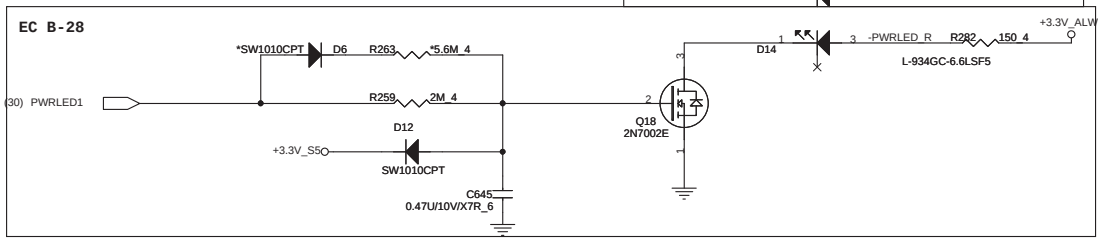
For New Keyboard use.

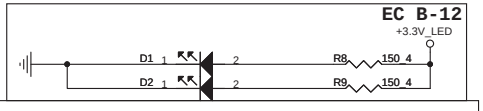


LED INDICATOR

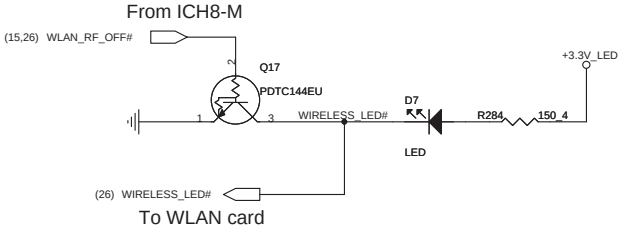


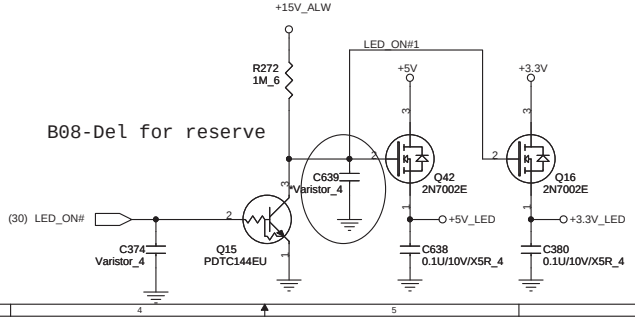


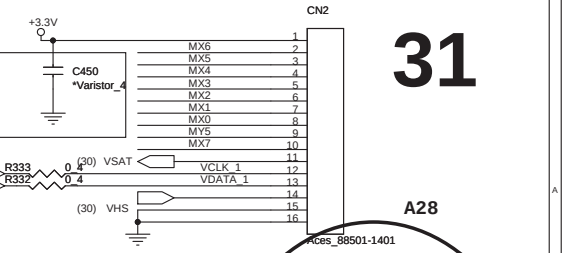


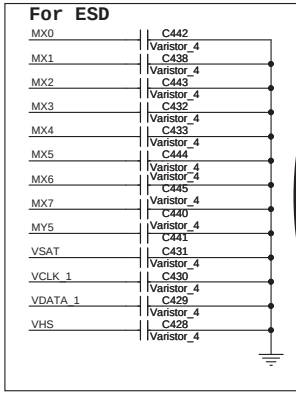


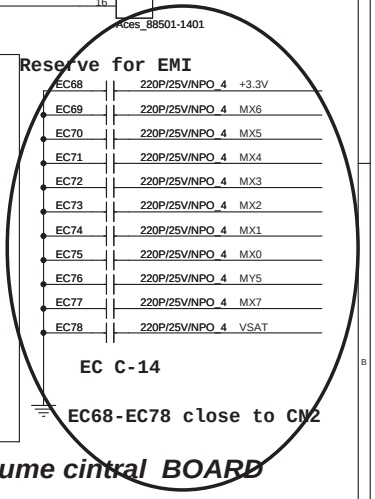
WIRELESS LED











SWITCH/Volume cintral BOARD

PROJECT : SA1A		
Quanta Computer Inc.		
Size: Custom	Document Number: TP/KB/LED/SW. BOARD	Rev: 3A
Date: Thursday, January 31, 2008	Sheet 31 of 39	

NEWCARD

(15) USBP5-
(15) USBP5+
R445 0_4 USBCONP5-
R444 0_4 USBCONP5+

+3.3V
CPUSB# R151 10K_4
CPPE# R393 *10K_4
2231_SHDN# R141 10K_4
2231_STBY# R139 10K_4

A08
C-test-Del

A08
C-test-Add

(15) NC_PWR_EN#
R538 0_4
R537 0_4
T64 *PAD
T62 *PAD
R150 *10K_4
R142 *0_4

U7
R5538
+3.3V_SUS
3VAUX
2231_STBY# → STBY#
CP_RST# → AUXIN
CPPE# → AUXOUT
CPUSB# → SYSRST#
PERST# → CPPE#
2231_SHDN# → CPUSB#
RCLKEN → PERST#
OC# → 2231_SHDN#
GND → RCLKEN
3.3VIN → OC#
3.3VIN → GND
AUXOUT
1.5VIN
1.5VIN
3.3VOUT
3.3VOUT
1.5VOUT
1.5VOUT
+3.3V
+1.5V
3V_NEWCARD **1.35A need 60 mil**
1.5V_NEWCARD **0.75A need 30~40 mil**

1.35A need 60 mil
3V_NEWCARD

A08
C-test-Change

(2,26) PCLK_SMB
(2,26) PDAT_SMB
0.75A need 30~40 mil
1.5V_NEWCARD
(15,21,26) SB_PCIE_WAKE#
3VAUX
PERST#

A08
C-test-Change

(2) NEW-CARD_CLK_REQ#
R239 0_4 CLK_NEW_OE#
NC_PWR_EN#
(2) CLK_PCIE_NEW_C#
(2) CLK_PCIE_NEW_C
(8) PCIE_RXN3
(8) PCIE_RXP3
(8) PCIE_TXN3
(8) PCIE_TXP3

CN23
USBCONP5-
USBCONP5+
NC_PWR_EN#
RESERVED2
RESERVED1
SMB_CLK
SMB_DATA
+1.5V2
+1.5V1
WAKE#
+3.3VAUX
PERST#
+3.3V2
+3.3V1
CLKREQ#
CPPE#
REFCLK-
REFCLK+
GND3
PERn0
PERp0
PETn0
PETp0
GND4
USB_D-
USB_D+
CPUSB#
GND2
GND1
SHIELD6
SHIELD5
SHIELD4
SHIELD3
SHIELD2
SHIELD1
331-1CX43201-ZG-X2_NEW_CARD

+3.3V_SUS
C239 0.1U/10V/X5R_4
(9,14,20,21,26,27) PLTRST#
U5
TC7SH08FU(F)
CP_RST#

3V_NEWCARD
3VAUX
1.5V_NEWCARD
C237 0.1U/10V/X5R_4
C238 0.1U/10V/X5R_4
C253 0.1U/10V/X5R_4
C252 0.1U/10V/X5R_4
C251 0.1U/10V/X5R_4
C250 0.1U/10V/X5R_4

EC B-24

PROJECT : SA1A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NEW CARD	3A
Date: Thursday, January 31, 2008	Sheet 32 of 39	

BATTERY CHARGER

A24
10/29 Change to 65W

TOP DC_JACK 65W
CN10 DC-JACK 65W-BLK
PC59 .1U/50V/X7R_6
HI0805R800R/5A_8 PL2
HI0805R800R/5A_8 PL3
PC58 .1U/50V/X7R_6
PD7 PDS1040-13
A25 C-Test
PD14 PASMAJ20A
EC C-09
PR96 RL3720WT-R020
R1
CSIP 1P
CSIN 2P

C1
12/28 Change footprint to
DCJK-2DC-G213X200-V-SA7

PR1 *0_4
PR2 *200K/F_6
PR3 *200K/F_6
PC1 *0.1U/50V/X7R_6
PR4 *0_4
PQ2 *IMD2
D/C#
PR97 *0_4
PQ24 SUD45P03-15
PC60 1U/25V/X7R_8
PQ1 DTA124EU
PC2 0.1U/50V/X7R_6
PR98 10K/F_6
ACOK_IN
PR11 *33.2K/F_6
PR5 *10K/F_6
PR10 *0_4
PQ3 *2N7002K-T1-E3
PR12 200K/F_6
PR6 100K/F_6
PQ25 SI4425BDY-T1-E3
Place close to EC,
PL5 HI0805R800R/5A_8
PL4 HI0805R800R/5A_8
BAT_CONN
BATT+
CN13
PR173 100K/F_6
MBATV
PR172 14K/F_6
PC129 0.01U/50V/X7R_6
PR9 330/F_4
PR8 330/F_4
PR7 10K/F_4
PC3 .01U/16V/X7R_4
TEMP_MBAT (30)
MBDATA (30)
MBCLK
PD2 UDZS5.6BTE-17
PD1 UDZS5.6BTE-17

Place these CAPs close to FETs
B09-ADD-EMI
PC73 1U/50V/X7R_4
PC72 .1U/50V/X7R_6
PC67 10U/25V/X6S_12
PC68 10U/25V/X6S_12
R546 2.2_8
C653 1500P/50V/X7R_4
PQ33 Si4800BDY
PQ32 Si4800BDY
PC16 1500P/50V/X7R_4
PL6 SIL104R-100PF/10UH/4.4A
6251LR
PR104 RL3720WT-R020
R2
PC74 10U/25V/X6S_12
PC75 10U/25V/X6S_12
PC76 .01U/50V/X7R_4

PR117 20_6
PC81 0.047U/10V/X5R_4
A25 C-Test
PR113 20_6
PR146 0_6
PC91 .1U/50V/X7R_6
CH501H-40PT PD11
PC82 .1U/50V/X7R_6
PC78 1U/6.3V/X5R_4
PR107 4.7_6
PC88 4.7U/6.3V/X5R_6
PR128 2_6
PR124 20_6
PR129 2_6
ISL6251_VDD
ISL6251_VDDP
ISL6251_UGATE
ISL6251_PHASE
ISL6251_LGATE

A25 C-Test
PD9 SW1010CPT
PR106 10_6
PC79 1U/25V/X5R_8
PR110 100K/F_4
PR108 12.4K/F_4
Setting the Vin min to 12V
For ACSET 1.26V
DCIN
6251ACIN
6251EN
PR112 150K/F_4
PR115 10K/F_4
Setting the Vin min to 17V
For EN = 1.06V

CSOP
CSON
ACOK#
ACPRN
DCIN
ACSET
EN
CELLS
ICOMP
VCOMP
ICM
VFREE
CHLIM
BOOT
UGATE
PHASE
LGATE
PGND
GND
VADJ
ACLIM

A23
PR143 178K/F_4 Rhigh
PR144 *100K/F_4
PR142 29.4K/F_4 Rlow
PR145 *100K/F_4
6251VREF
VADJ =
VERF >> 4.2V +5%
Float >> 4.2V
GND >> 4.2 -5%
A25 C-Test

PU5 ISL6251A
A25 C-Test
PC84 6800P/25V/X7R_4
6251VREF
VREF = 2.39V
PR139 0_4
CC_SET (30)
V ACLIM = VREF * (Rlow // 152K) / (Rhigh // 152K + Rlow// 152K)
Iin_max = (1/R1)((0.05/Vref) * Vaclim + 0.05)
PC21 100P/50V/X7R_4
PR140 *100K/F_4
Charging Curret setting =>
Ichg = 165mV / R2 * (Vchlim / 3.3V)
PR130 10K/F_4
PR136 100/F_4
SYS_I
PC89 3300P/50V/X7R_4
PC19 100P/50V/X7R_4
PC86 0.1U/16V/X7R_4
Input Current monitor
V icm = 19.9 * (Vcsip - Vcsin)

ACOK
ISL6251_VDD
PR122 10K/F_4
PQ34 DTA124EU
(30) ACIN
PR127 15K/F_4
6251ACIN
PC83 1U/25V/X5R_8
ACOK#
CH2507SPT PQ36
PD10 SW1010CPT
PR138 1M_4

A25 C-Test
Ec C-10
PR123 100K/F_4
PR118 100K/F_4
6251CELLS
(30) CELL_SLT
CH2507SPT PQ5

CELL_SLT = 1 -- 3 S (Cells = GND 3S)
CELL_SLT = 0 -- 4 S (Cells = VDD 4S)

ADP TYPE	PR143	P/N
65W	178K/F_4	CS41782FB11
90W	11K/F_4	CS31102FB11

A22
Ramp-PQ4 P/N Change to PQ7

A22
Ramp-PC18-Del
PC15 *1U/25V/X5R_6
PC18 *1N/50V/X7R_4
PR28 475K/F_6
PR27 332K/F_6
PC17 *1N/50V/X7R_4
PD3 SW1010CPT
PQ4 CH2507SPT
Battery Low 7.5V
A22
Ramp-PC17-Del
PU2 G1331
PR36 10K/F_4
PR35 10K/F_4
PR37 *0_4
PQ7 2N7002K-T1-E3
D/C# (30)
BL/C# (30)
PD4 SW1010CPT
A22 C-Test
PR34 100K/F_4
PQ6 2N7002K-T1-E3

TON: 5V / 3.3V
GND = 400 / 500KHz
REF = 400 / 300KHz
VCC = 200 / 300KHz

A25 Del 10/29

Place these CAPs close to FETs

+5Volt +/- 5%
Countinue current:7.5A
OCP minimum:10A

Vout=0.7(Ra+Rb)/Rb

Rb around 49.9k

I_lim*MOSFET(RDSON)=V_ILIM(mV)/10
V_ILIM(mV)=5uA*R_ILIM

Rds(on) 15m ohm

A25 C-Test

+3.3Volt +/- 5%
Countinue current:7.5A
OCP minimum:10A

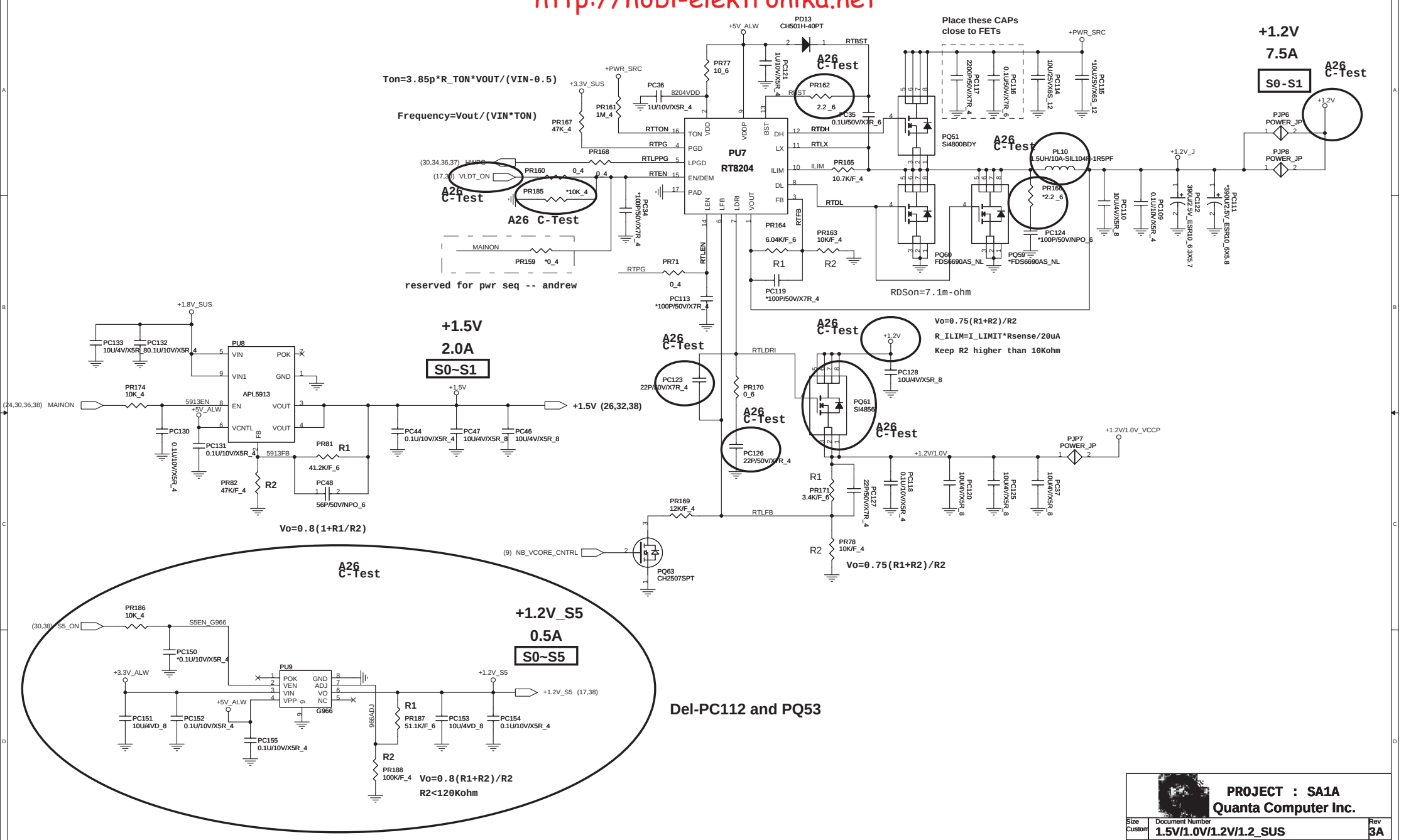
C3 Change Part for SMT

+5V 5A S0-S1

+5VSUS 4A S0-S3

+3V 5.76A S0-S1

PROJECT : SA1A	Quanta Computer Inc.
Size: Custom	Document Number: 3V/5V/10V /15V
Rev: 3A	
Date: Thursday, January 31, 2008	Sheet 34 of 39



Quanta Computer Inc.	PROJECT : SA1A		
Size: Custom	Document Number: 1.5V/1.0V/1.2V/1.2_SUS		Rev: 3A
Date: Thursday, January 31, 2008	Sheet 35 of 39		

+1.8VSUS
18A
S0~S3

+PWR_SRC

PC61 100U/25V_6.3X7.7
PC94 100U/25V_6.3X7.7
PC25 *10U/25V/X6S_12
PC102 10U/25V/X6S_12

Place these CAPs close to FETs

PC100 0.1U/50V/X7R_6
PC101 2200P/50V/X7R_4

Ra=(Vout-0.75)/0.75*Rb

Rb value from 100K to 300K ohm

+1.8V_SUS

PJP3 POWER_JP
PJP4 POWER_JP
PJP5 POWER_JP

+1.8V_SUS_J

PC106 390U/2.5V_ESR10_6.3X5.7
PC105 390U/2.5V_ESR10_6.3X5.7
PC107 0.1U/10V/X5R_4
PC96 *100P/50V/X7R_4

PL9 MPO104-1R5/1.5U/20A

PR46 *2.2_8
PC26 *100P/50V/NPO_6

PQ40 SI7686DP
PQ41 SI7636DP
PQ8 *SI7636DP

A25 C-Test

Ra
PR150 *2K/F_4
PR152 0_4

Rb
PR39 *10K/F_4
PR154 *0_4
PR24 *0_4

VDDIO_FB_H (5)
Differential Pair
VDDIO_FB_L (5)

Rds(on) 7.25m ohm

Fix 1.8V Output
PR40 0_4
51116_V5FILT

I_lim(Valley)=10uA*R_ILIM/RDS_ON
For OCP set.

+5V_ALW
PR156 10_6
51116_V5FILT
PC98 2.2U/6.3V/X5R_6
PC22 1U/10V/X5R_4
+3.3V_SUS
PR38 *10K_4
PC104 0.1U/50V/X7R_6 2.2_6
PR157
51116_BST
PR43 7.15K/F_6
PR153 0_4
HWPG (30,34,35,37)

PU6 TI51116
VBST
V5IN
V5FILT
CS
PGOOD
DRVH
LL
S5
S3
VLDOIN
DRVL
VTTGND
MODE
VDDQSNS
VDDQSET
VTT
VTTSNS
COMP
NC
NC
VTTREF
CS_GND
PGND
PAD GND

1.8V_DH
1.8V_LX
1.8V_DL
1.8V_OUT
1.8V_FB
COMP

S5SON
S3SON
PR149 0_4
PR151 0_4
SUSON (30,38)

+1.8V_SUS_J
PC103 1U/10V/X5R_4
PC99 10U/4V/X5R_8
PC24 10U/4V/X5R_8
+0.9V_DDR_VTT
+0.9V_DDR_VTT (4,6,11,13,38)
VTTSNS
PR45 0_4
PR42 *0_4
CPU_VTT_SENSE (4)
PR44 0_4
MODE
+1.8V_SUS_J

PR41 0_4
51116_V5FILT
SMDDR_VREF
PR155 0_6
PC97 0.033U/25V/X7R_6

+0.9V
1.53A
S0~S3

+2.5V
0.25A
S0~S1

Close to CPU
SI power

(24,30,35,38) MAINON
PR51 10K_4
+3.3V_ALW
PC30 0.1U/10V/X5R_4
PC29 1U/10V/X5R_4

PU3 G913C
SHDN
VIN
GND
VOUT
SET

R1 PR56 100K/F_4
R2 PR57 100K/F_4
PC32 4.7U/6.3V/X5R_6
+2.5V

Vout=1.25(1+R1/R2)

(11,34,38) MAIND
PQ35 SI4856

+1.8V
6A
S0~S1

+1.8V_SUS
+1.8V
+1.8V (5,9,10,11,14,17,28,38)
PC80 10U/4V/X5R_8
PC156 10U/4V/X5R_8

A25 C-Test

PROJECT : SA1A
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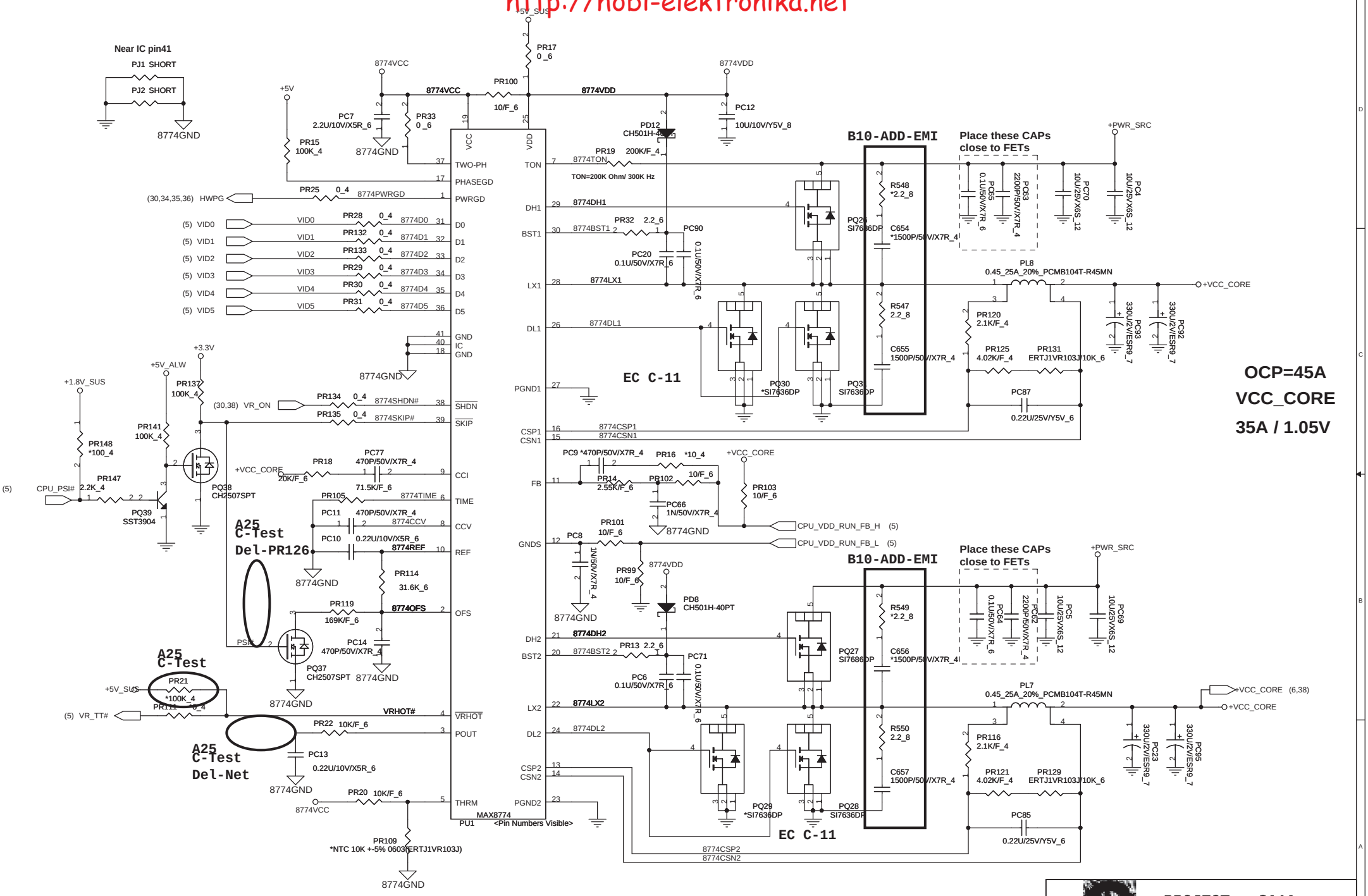
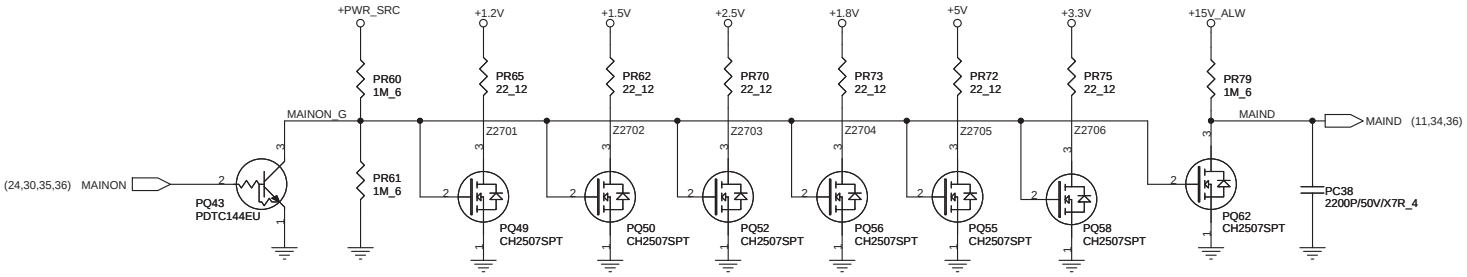
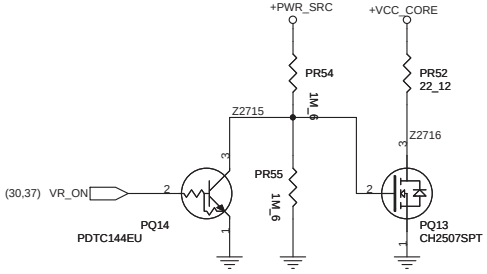
Size	Document Number	Rev
Custom	1.8V_SUS/1.8V/2.5V	3A
Date: Thursday, January 31, 2008	Sheet 36 of 39	

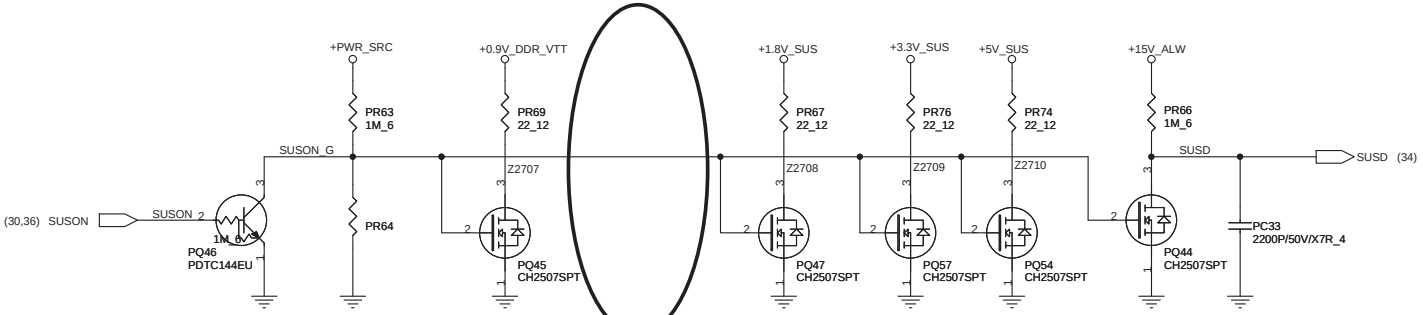


PROJECT : SA1A		
Quanta Computer Inc.		
Size: Custom	Document Number: CPU VCC CORE	Rev: 3A
Date: Tuesday, February 05, 2008	Sheet 37 of 39	

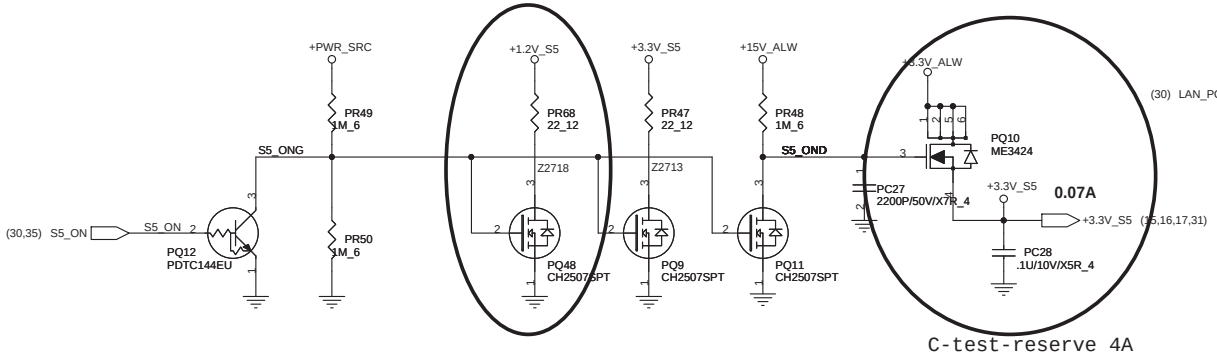


C-test-Del +1.2V_SUS

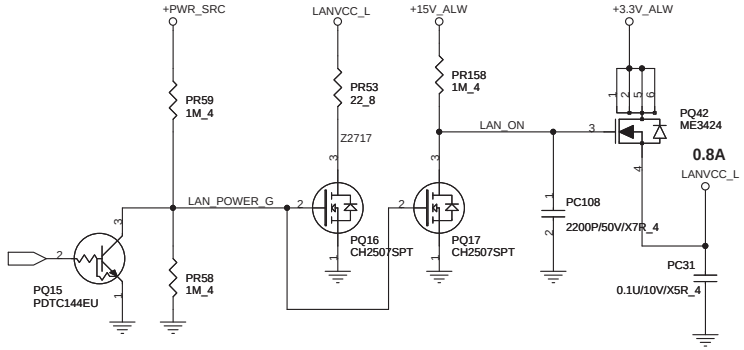




A27
C-test-Add +1.2V_S5



C-test-reserve 4A



PROJECT : SA1A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DISCHARGE	3A

Date: Thursday, January 31, 2008 Sheet 38 of 39

A01. For EMI reserve but no stuff.
A02. Reference AMD demo circuit don`t add capacitor.
A03. ADM suggest by pass directly, for single core and dure core start-up issue.
A04. ADM suggest by pass HDMI_DET directly for TMDS directly.
A05. Change CN22 Pin connection.
A06. Change Power rail.
A07. Change KBSMI# to new GPIO for S/W request.
A08. Add New-Card power controll Pin.
A09. Modify STRAP Pin setting.
A10. Solve Start-up "FF" issue.
A11. Change Power rail.
A12. Use +15V let Q10 turn-on fully.
A13. Base on AMD suggest and Demo circuit don`t connection those parts.
A14. AMD suggest use 60 Ohm Res , so we use 120//120=60 Ohm.
A15. Modify by Realtek suggestion for power saving.
A16. Change Power soucer by Realtek suggestion.
A17. Del capacitor by Realtek suggestion for signal loading capacitor.
A18. Modify Pin define for common design.
A19. Solve some ODD can't detection issue.
A20. Change ESD component P/N.
A21. Change EC net to correct function.
A22. Del PC17, PC18 and change PR35 ,PR36 to slove battery learnning can`t discharge issue.
A23. Change Resistor 65W charge setting.
A24. Modify P/N for common design.
A25. Change by Power for fine tune some part's volume or footprint.
A26. Change power circuit for power budget and slove leakge issue.
A27. Change Power rail.
A28. For EMI reserve.

B-01 / Page 2 / Add Cap for AMD suggestion.
B-02 / Page 9 / USB performance
B-03 / Page 9 / Change Value for AMD suggestion to PASS HDMI test.
B-04 / Page 16 / Requirement from AMD.
B-05 / Page 18 / Change value to solve HDMI issue.
B-06 / Page 19 / Change to FDV301N to solve HDMI issue.
B-07 / Page 26 / Connector to WLAN_RF_OFF#.
B-08 / Page 31 / Delete.
B-09 / Page 33 / Add for EMI suggestion.
B-10 / Page 37 / Add for EMI suggestion.
B-11 / Page 2 / Reserve for EMI suggestion.

EC C-01 / Page 5,10 / ADD EMI solution
EC C-02 / Page 5 / The PWM output do not need a series 100K and a 0.1u cap. So R378 change to 0 ohm , C534 remove Cap.
EC C-03 / Page 9,14,15 / Insert 10K resistor for ESD.
EC C-04 / Page 14 / Change to non-insert.
EC C-05 / Page 20 / Change Resistor from 2.2K to 4.7K.
EC C-06 / Page 20 / Change Resistor from 2.2K to 6.8K.
EC C-07 / Page 20 / Change to non-insert.
EC C-08 / Page 31 / Change to non-insert for ESD.
EC C-09 / Page 33 / Add PD14 for Power plug issue.
EC C-10 / Page 33 / Insert 100K for Battery charger issue.
EC C-11 / Page 37 / PQ29 Change TO PQ28 , PQ30 Change TO PQ31 for EMI.
EC C-12 / Page 19 / Base on AMD requirement we will change R539 to CX8PG330007 , Change R540 to non-insert.(Change FAI stage).
EC C-13 / Page 09 / Insert 100K for HDMI hot plug issue(Change FAI stage).
EC C-14 / Page 31 / Change Capacitor from 0.1U to 220P for EMI(Change FAI stage).
EC C-15 / Page 24 / C461,C460,C459,C458 change to ASM(Change FAI stage).
EC C-16 / Page 14 / R391 change to ASM(Change FAI stage).
EC C-17 / Page 24 / R498 change to ASM(Change FAI stage).

PROJECT : SA1A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Change Notice	3A

Date: Thursday, January 31, 2008 Sheet 39 of 39