

Compal Confidential

Model Name :
File Name : LA-8671P

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TN-Note Schematic Document

2012-10-04

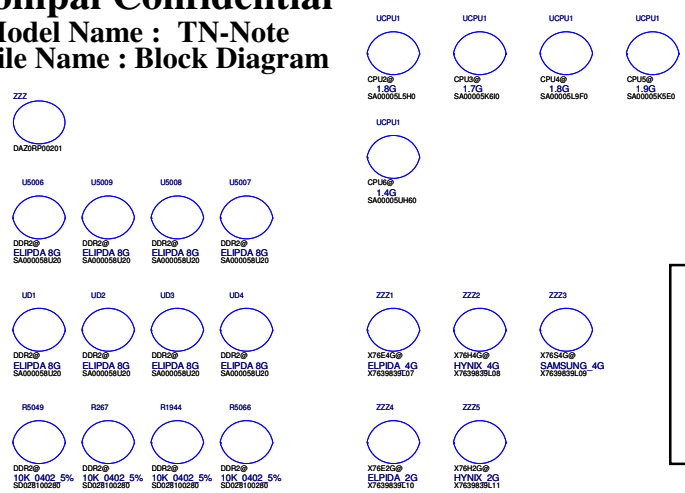
REV:1A_1004A

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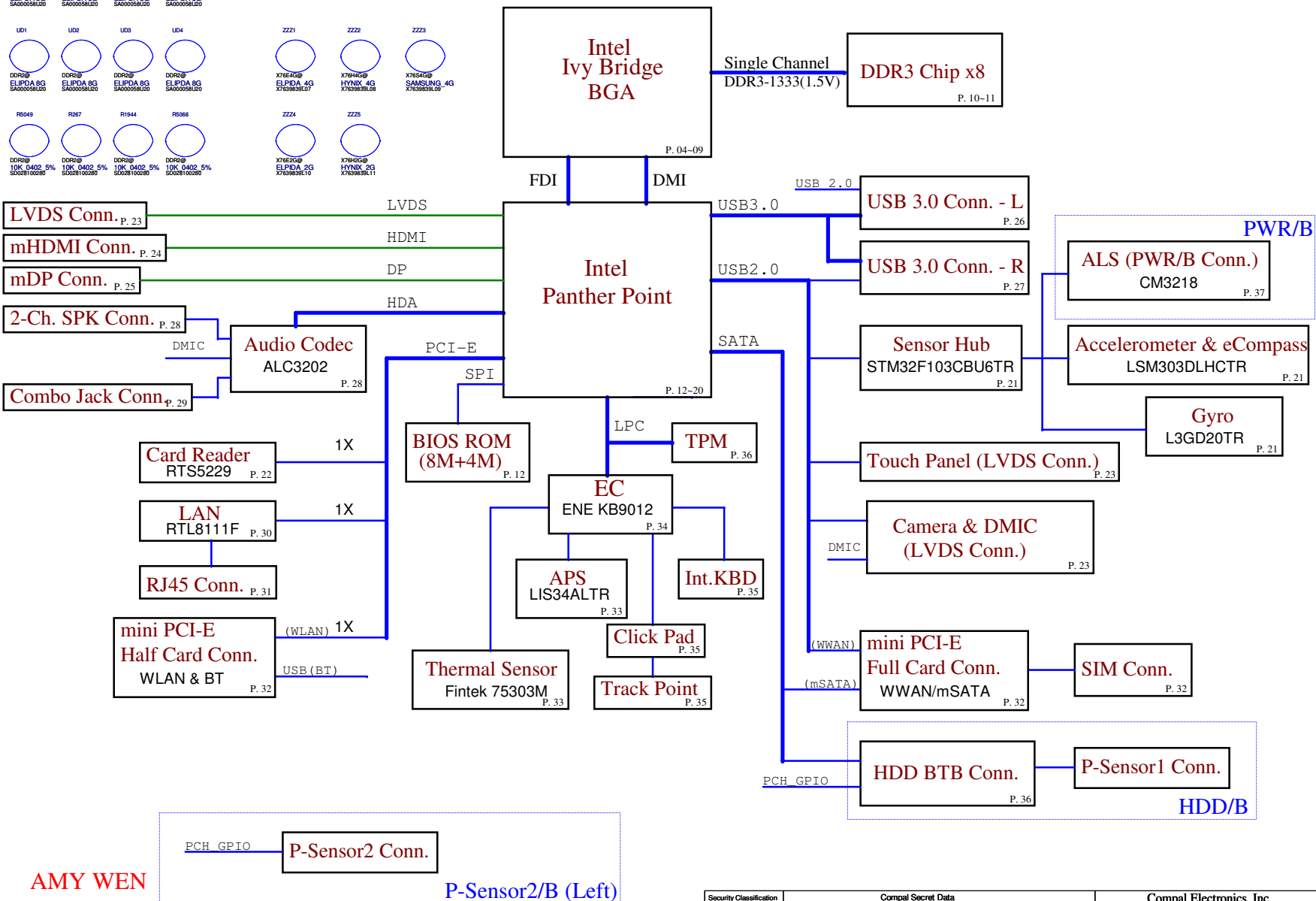
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Model Name : TN-Note
File Name : Block Diagram



CPU2B	SA00005L5H0	S IC AV8063801058401 SR0N9 L1 1.8G A39!
CPU3B	SA00005K610	S IC AV8063801058002 SR0N8 L1 1.7G A39!
CPU4B	SA00005L9F0	S IC AV8063801057801 SR0N7 L1 1.8G A39!
CPU5B	SA00005K5E0	S IC AV8063801057605 SR0N6 L1 1.9G A39!
CPU6B	SA00005UH60	S IC AV8062701313000 SR0U3 J1 1.4G A39!

- Sub-board**
1. PWR Board (LS-8671P)
 2. HDD Board (LS-8672P)
 3. P-Sensor1 Board (LS-8673P)
 4. P-Sensor2 Board (LS-8674P)



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P-Sensor2/B (Left)

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Voltage Rails

Power plane / State	+B	+5VALW +3VALW	+1.5V	+3VM +1.05VM	+5VS +3VS +1.8VS +1.5VS +1.05VS +VCC_GFXCORE_AXG +CPU_CORE +VCCSA +0.75VS
S0	○	○	○	○	○
S3	○	○	○	○	✗
M3	○	○	○	○	✗
S4/S5 - AC	○	○	✗	✗	✗
S4/S5 - BATT ONLY	○	✗	✗	✗	✗
S4/S5 - NO AC & BATT	✗	✗	✗	✗	✗

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	
6	
7	

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS
Full ON		H	H	H	ON	ON	ON
S3 (Suspend to RAM)		L	H	H	ON	ON	OFF
S4 (Suspend to Disk)		L	L	H	ON	OFF	OFF
S5 (Soft OFF)		L	L	L	ON	OFF	OFF

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001-011xb	16H
Charger	0001-0010b	12H

EC SM Bus2 address

Device	Address	HEX
Thermal sensor	1001-101xb	9AH
PCH (SML1DATA / GPIO75)	1001-0110 b	96H

SM Bus Controller

Device	Address	HEX
Security Rom	1010-100xb	A8 H
DDR DIMMO	1010-000xb	A0 H

BOM Structure

	SDV	FVT	SIT	SVT	SOVP
@ : No Stuff					
ME@ : ME components					
CPUx@ : CPU SKU	√	√	√	√	√
DDRx@ : RAM SKU	√	√	√	√	√
SBA@ : SBA	√	√	√	√	√
NOSBA@ : NO SBA					
ID4@ : Intel Deep S4	√				
AOAC@ : AOAC	√	√	√	√	√
TPM@ : TPM		√	√	√	√
Short@ : 0ohm short pad					

SM Bus Controller 0

Device	Address	HEX
No-use	No-use	No-use

Sensor HUB

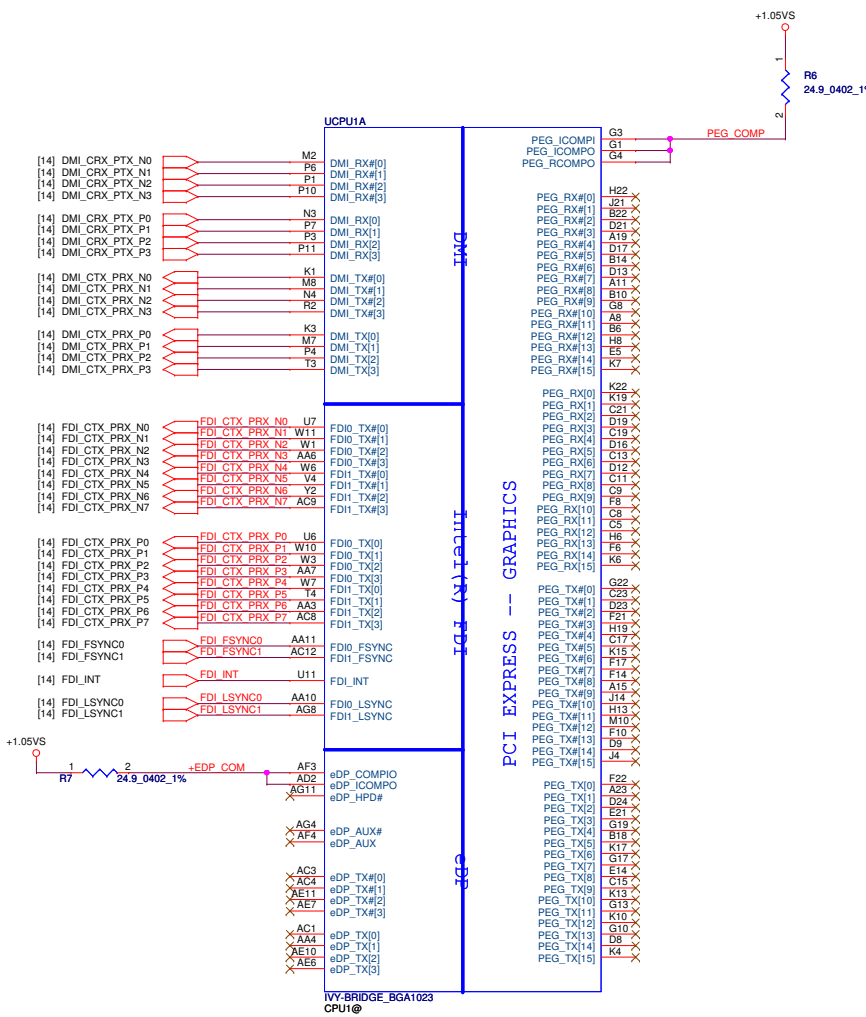
Device	Address	HEX
ALS	0100-100xb	48h
APS	0011-001xb	32h
Gyroscope	0110-101xb	6Ah
e-Compass	0011-110xb	3Ch

USB3.0	USB2.0	NOTE
1	0	
2	1*	USB3.0/2.0 Conn
3	2	USB3.0/2.0 Conn
4	3	
	4	Sensor Hub
	5	USB Camera
	6	✗
	7	✗
	8	Touch Panel
	9*	WWAN
	10	WLAN
	11	Finger Printer**
	12	
	13	Bluetooth**

* Debug Port
** Not Use

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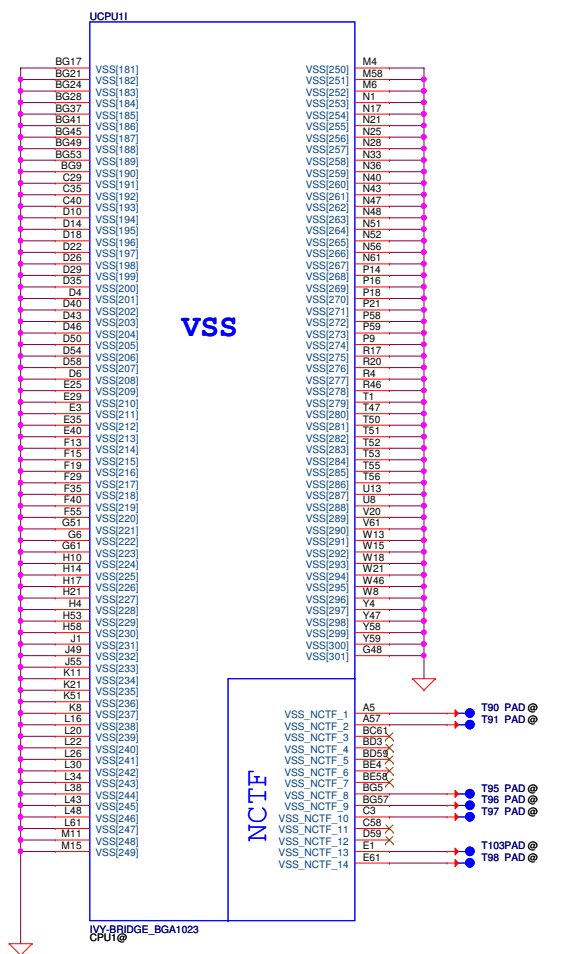
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PEG_ICOMPI and RCOMP signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
 PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

PEG Static Lane Reversal - CFG2 is for the 16x

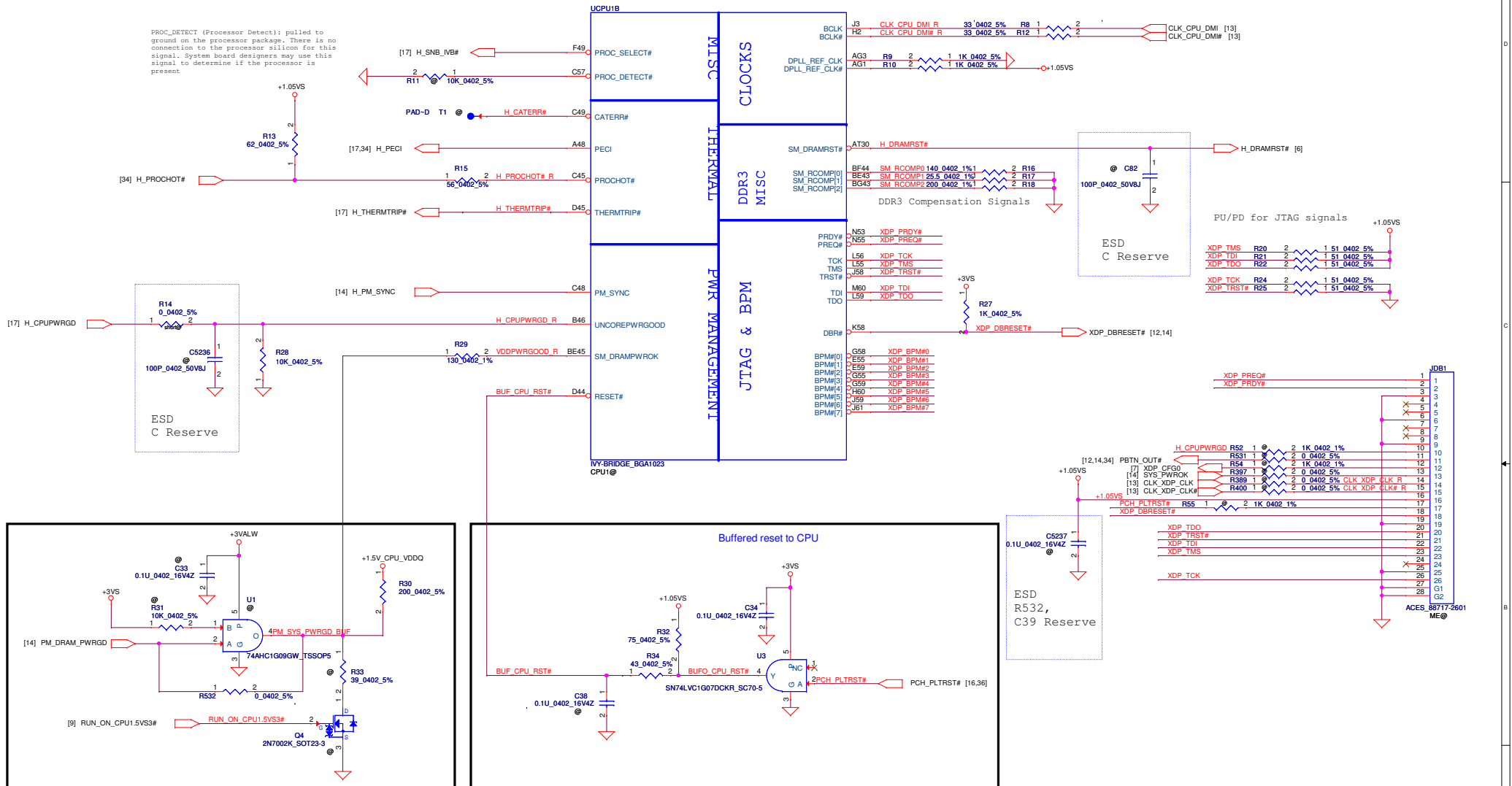
CFG2 * 1: Normal Operation; Lane # definition matches socket pin map definition
 0: Lane Reversed



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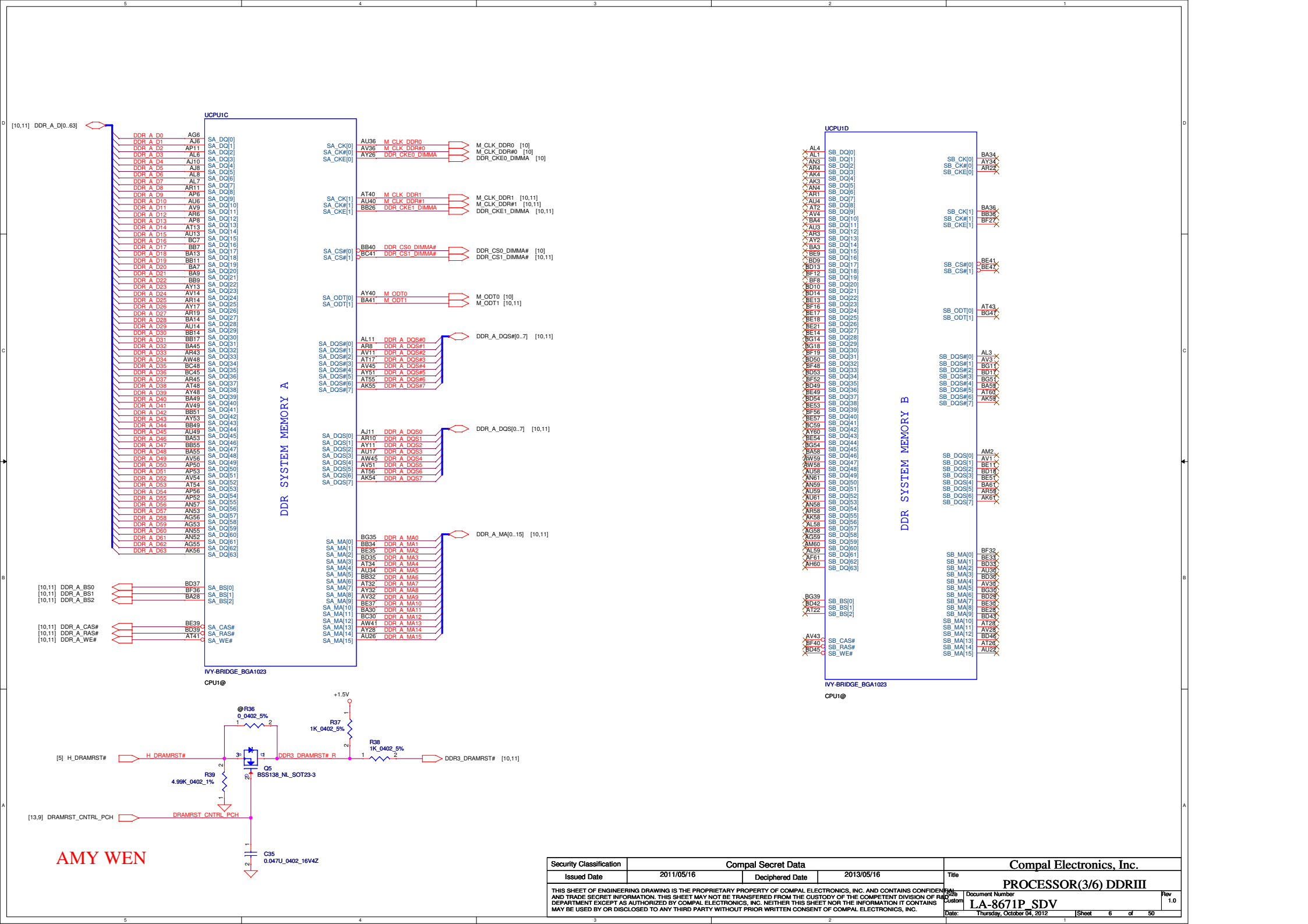
Security Classification		Compal Secret Data		Title		Compal Electronics, Inc.	
Issued Date	2011/05/16	Deciphered Date	2013/05/16	Processor (1/6) DMI, FDI, PEG		Size	Document Number
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PROC_DETECT (Processor Detect): pulled to ground on the processor package. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present.



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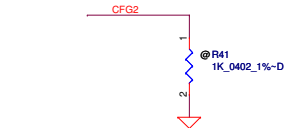
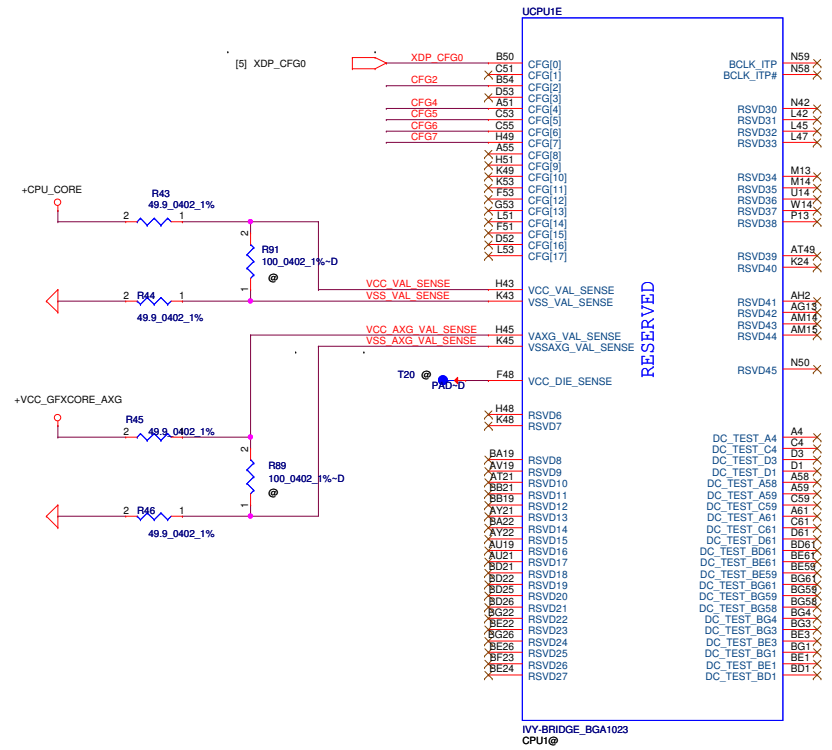
DDR SYSTEM MEMORY A

DDR SYSTEM MEMORY B

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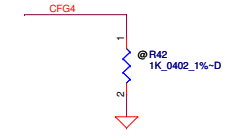
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CFG Straps for Processor



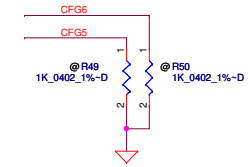
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	*1: (Default) Normal Operation; Lane # definition matches socket pin map 0: Lane Reversed
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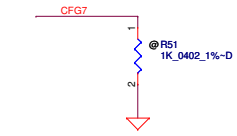
Display Port Presence Strap

CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port
------	--



PCIe Port Bifurcation Straps

CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
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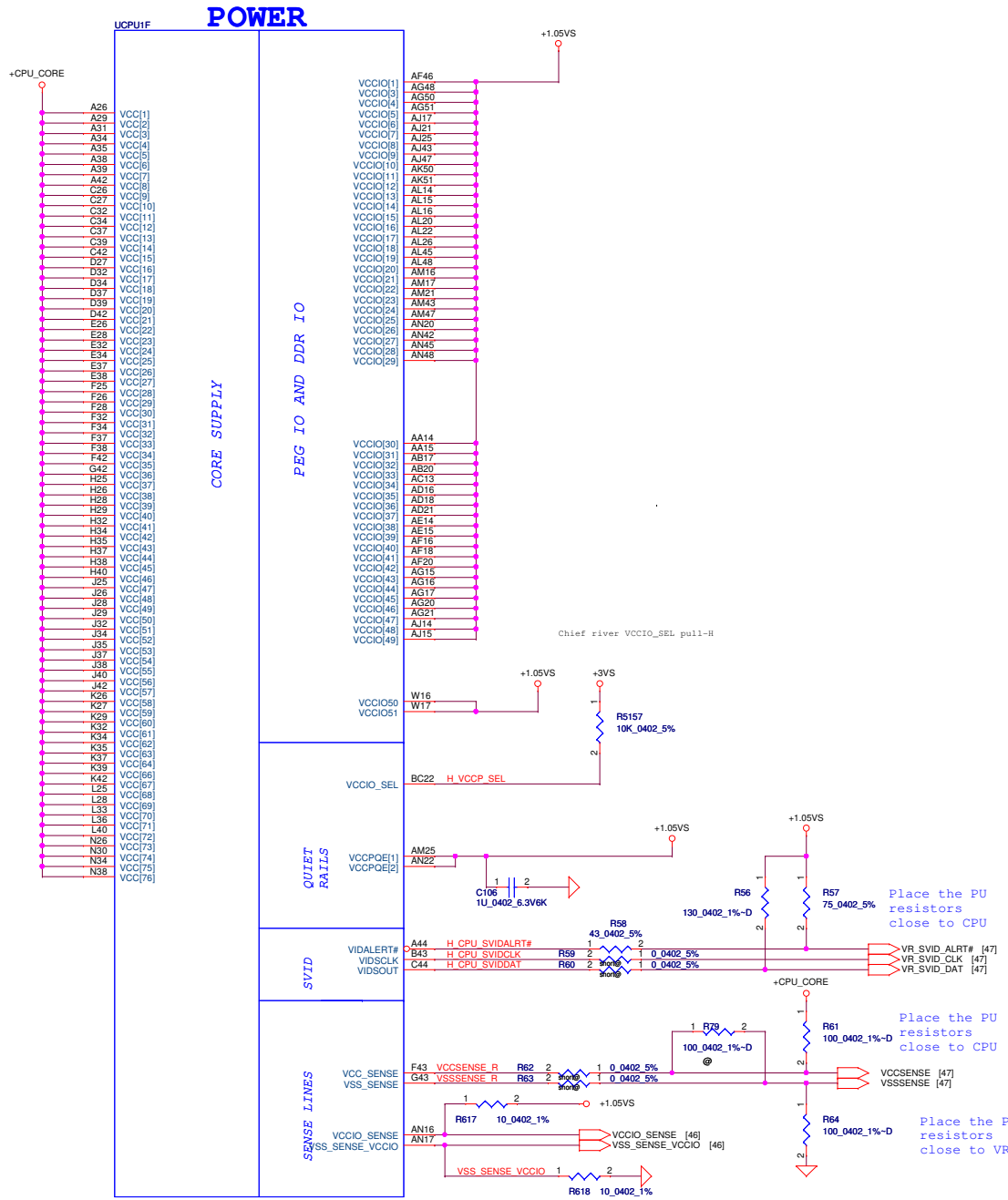
PEG DEFER TRAINING

CFG7	*1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training
------	--

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CPU_CORE
 GFX_CORE
 VCCP1.05

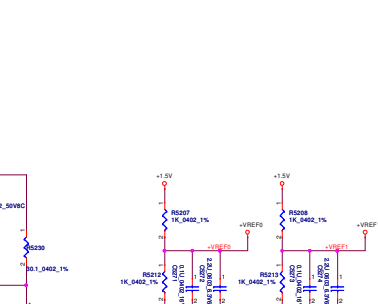
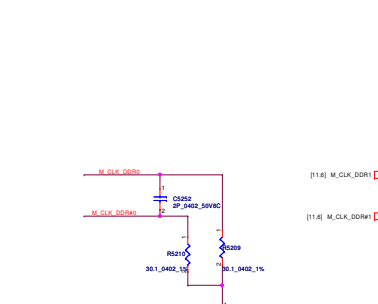
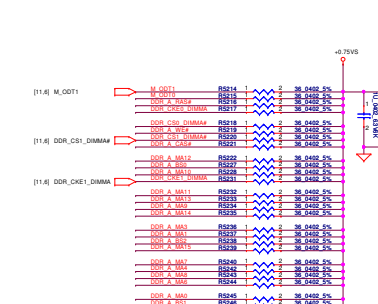
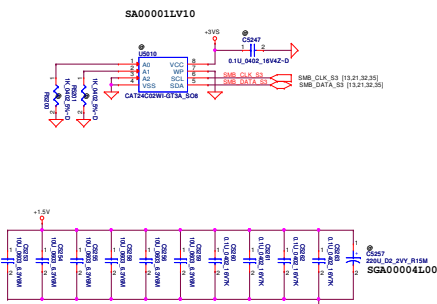
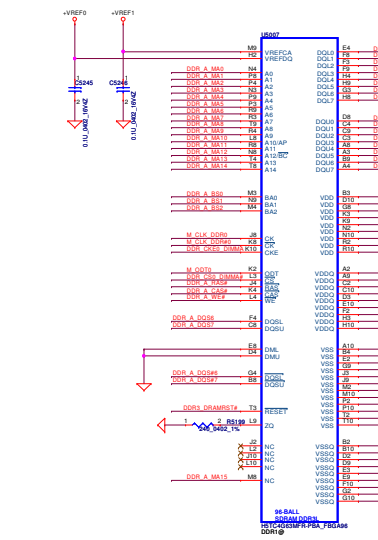
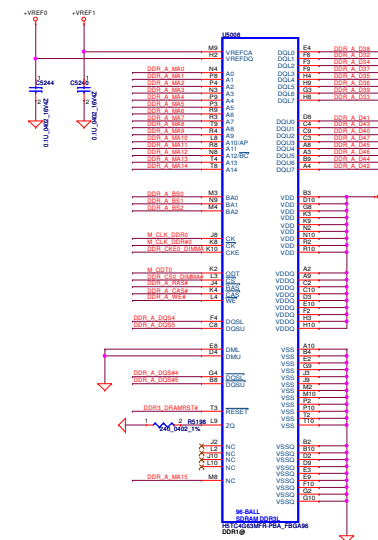
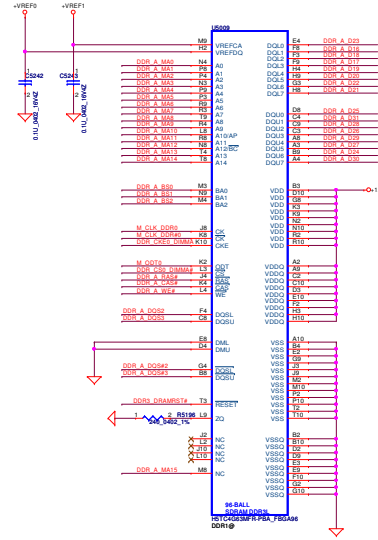
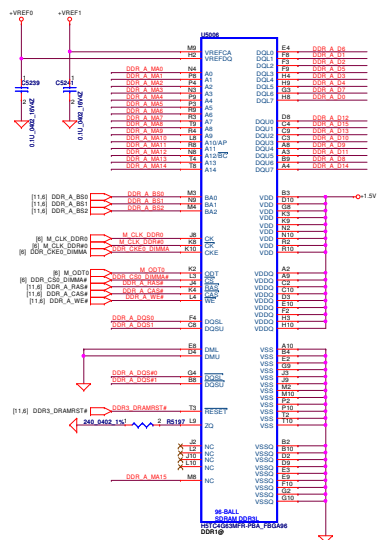
 VGA_CORE
 All Capacitor place on Power side.



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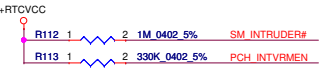
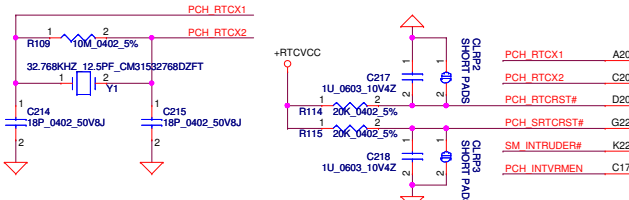
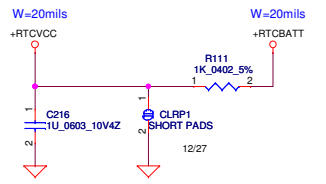
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- [1:4] DDR_A_M0:15
- [1:4] DDR_A_D0540:7
- [1:4] DDR_A_D0550:7
- [1:4] DDR_A_D0560:7
- [1:4] DDR_A_D0570:7
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- [1:4] DDR_A_D231:7
- [1:4] DDR_A_D232:7
- [1:4] DDR_A_D233:7
- [1:4] DDR_A_D234:7
- [1:4] DDR_A_D235:7
- [1:4] DDR_A_D236:7
- [1:4] DDR_A_D237:7
- [1:4] DDR_A_D238:7
- [1:4] DDR_A_D239:7
- [1:4] DDR_A_D240:7
- [1:4] DDR_A_D241:7
- [1:4] DDR_A_D242:7
- [1:4] DDR_A_D243:7
- [1:4] DDR_A_D244:7
- [1:4] DDR_A_D245:7
- [1:4] DDR_A_D246:7
- [1:4] DDR_A_D247:7
- [1:4] DDR_A_D248:7
- [1:4] DDR_A_D249:7
- [1:4] DDR_A_D250:7
- [1:4] DDR_A_D251:7
- [1:4] DDR_A_D252:7
- [1:4] DDR_A_D253:7
- [1:4] DDR_A_D254:7
- [1:4] DDR_A_D255:7

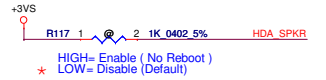


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Doc No	LA-8671P SDV	1A
Date	Thursday, October 24, 2013	Sheet 10 of 30

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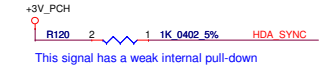
INTVRMEN(DCP_SUS)
 * H : Integrated VRM enable
 L : Integrated VRM disable
 (INTVRMEN should always be pull high.)



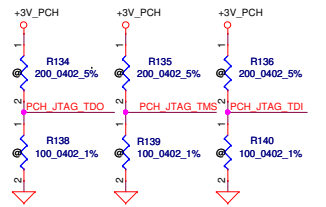
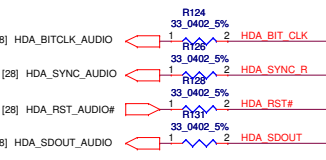
HIGH= Enable (No Reboot)
 * LOW= Disable (Default)



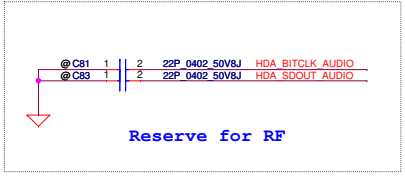
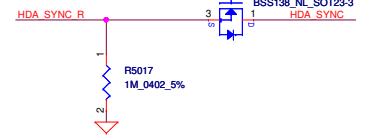
* Low = Disabled (Default)
 High = Enabled [Flash Descriptor Security Override]



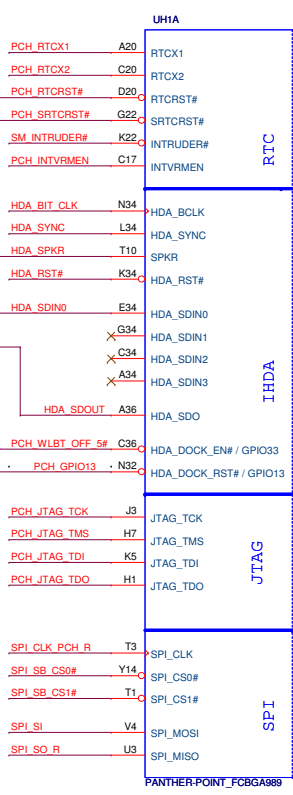
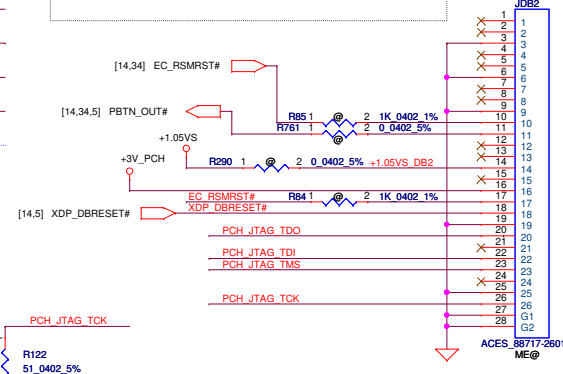
This signal has a weak internal pull-down
 * On Die PLL VR Select is supplied by 1.5V when sampled high
 1.8V when sampled low
 Needs to be pulled High for Huron River platform



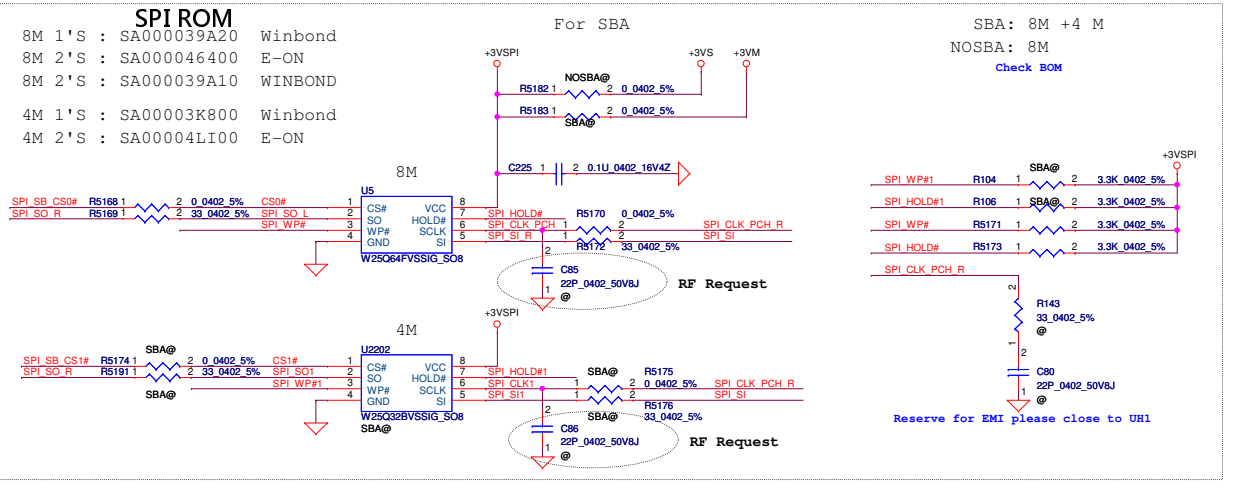
CMOS



Reserve for RF



SA00004N970

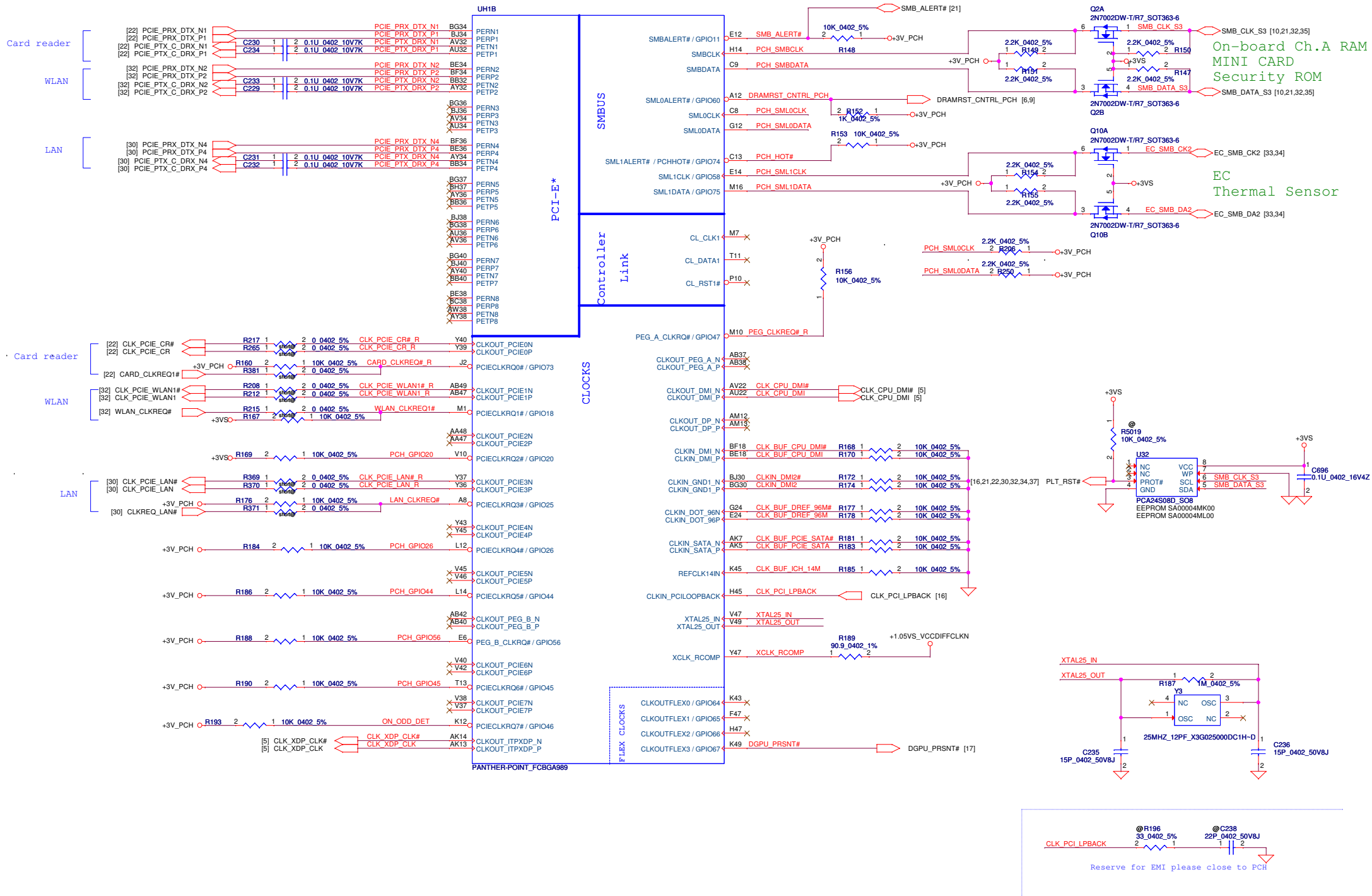


Boot BIOS Strap bit1 BBS1

GPIO51	GPIO19	Boot BIOS	Destination
Bit11	Bit10		
0	1	Reserved	
1	0	Reserved	
1	1	* SPI (Default)	
0	0	LPC	

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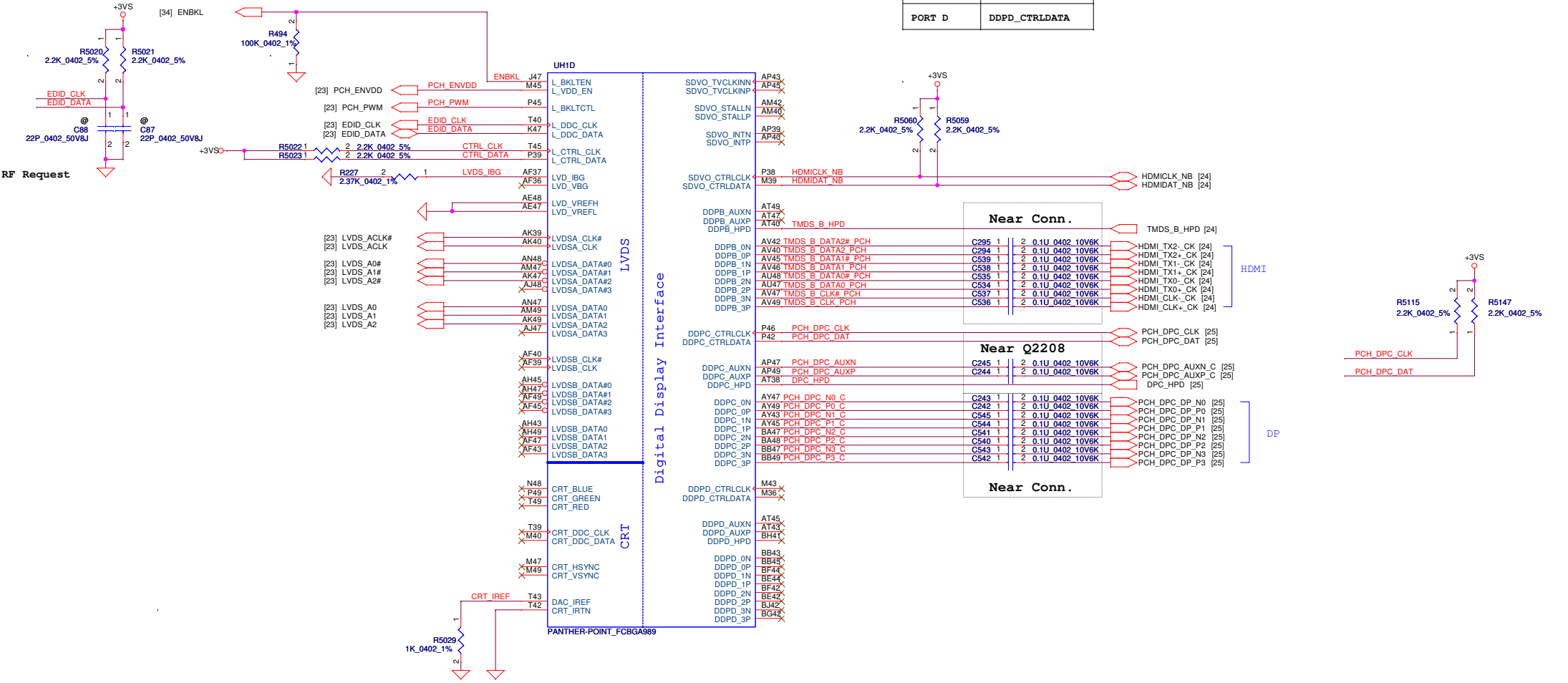
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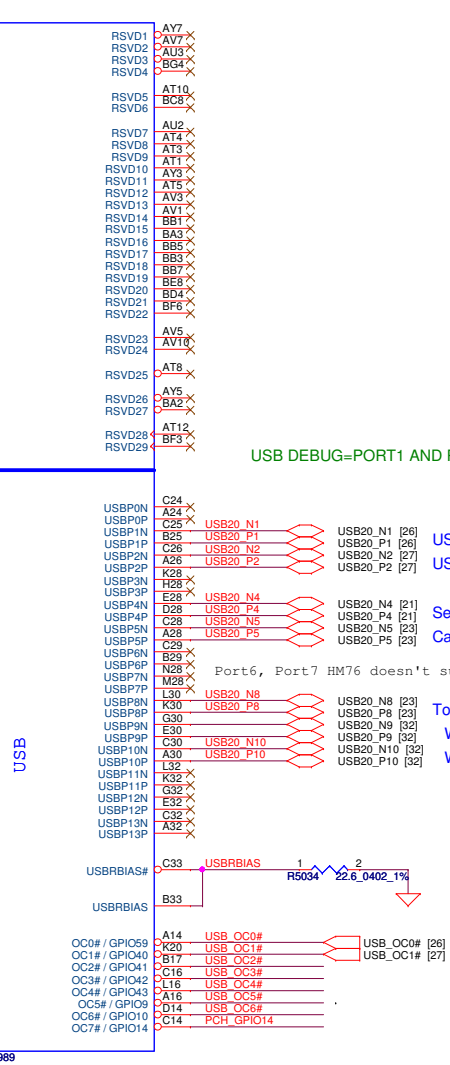
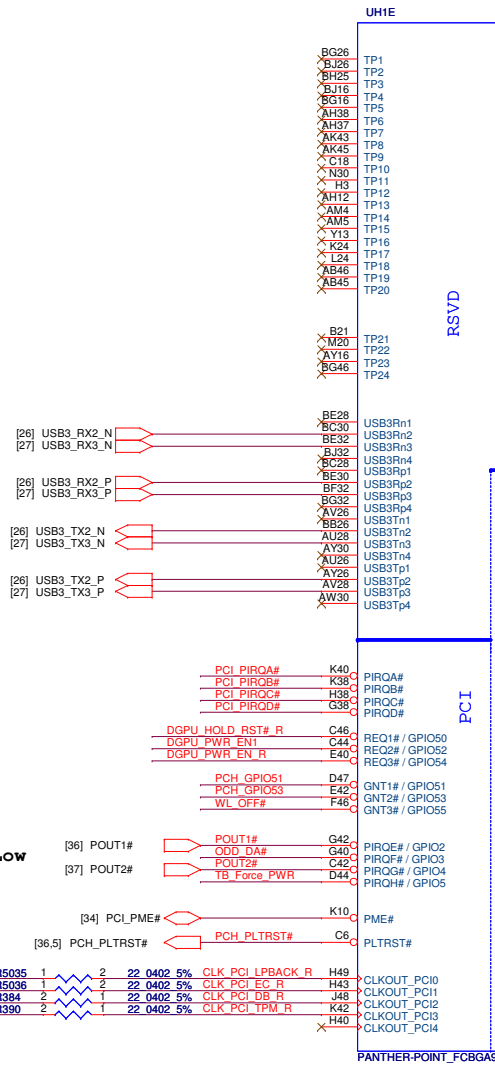
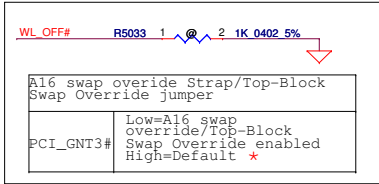
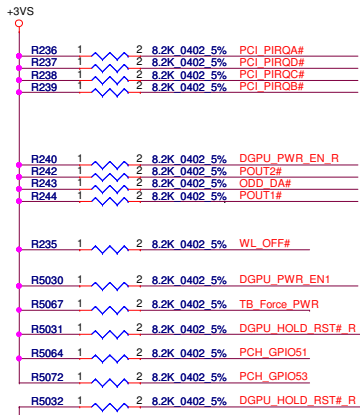
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PORT	STRAP
LVDS	L_DDC_DATA
PORT B	SDVO_CTRLDATA
PORT C	DDPC_CTRLDATA
PORT D	DDPD_CTRLDATA

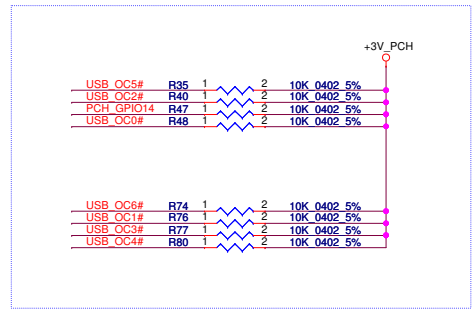
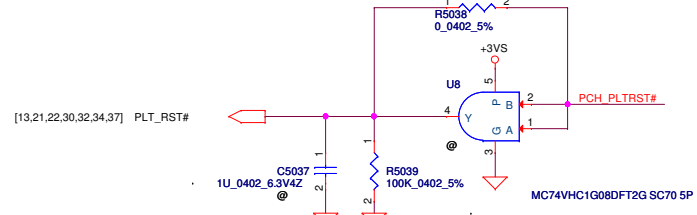
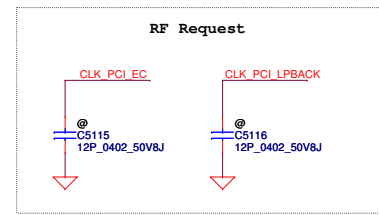


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Default: Active Low

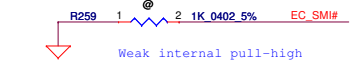


USB3.0	USB2.0	NOTE
1	0	
2	1*	USB3.0/2.0 Conn
3	2	USB3.0/2.0 Conn
4	3	
	4	Sensor Hub
	5	USB Camera
	6	X
	7	X
	8	Touch Panel
	9*	WWAN
	10	WWAN
	11	WLAN
	12	Finger Printer**
	13	Bluetooth**

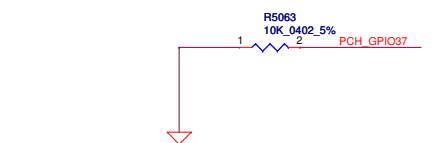
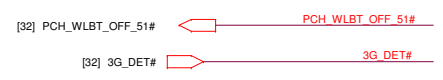
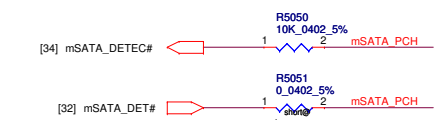
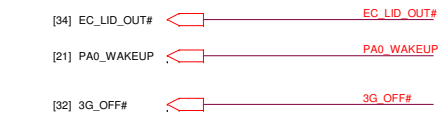
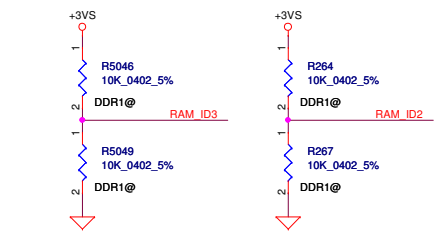
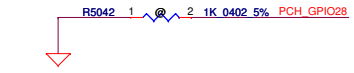
* Debug Port
** Not Use

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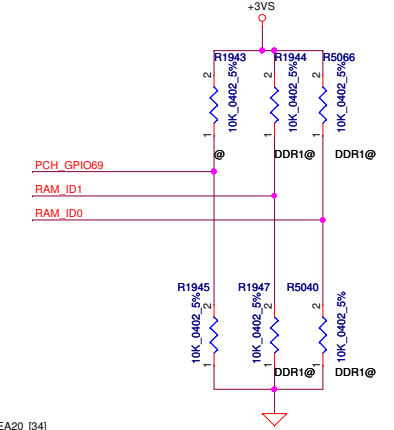
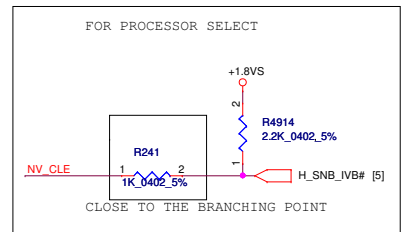
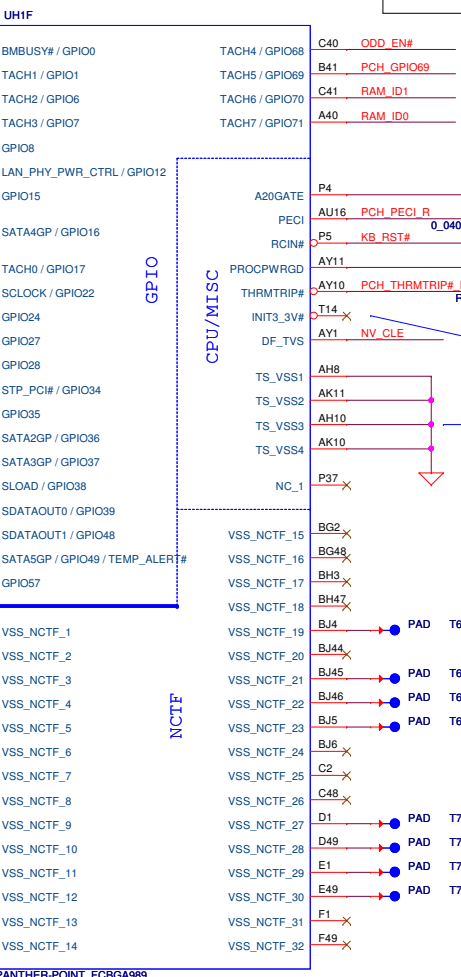
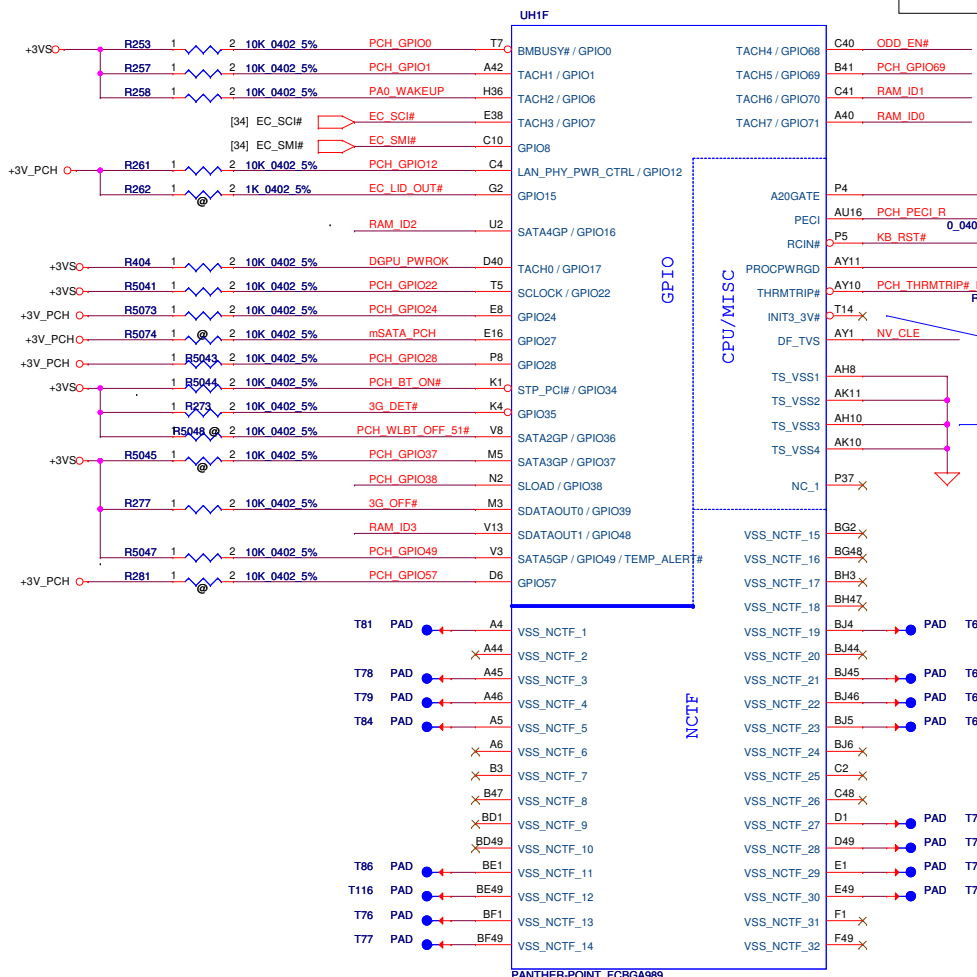
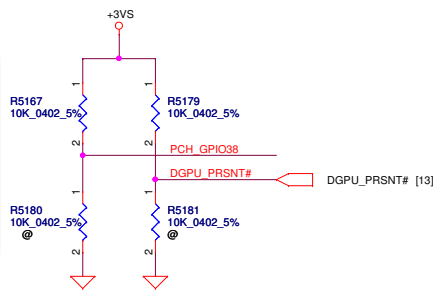
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GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable



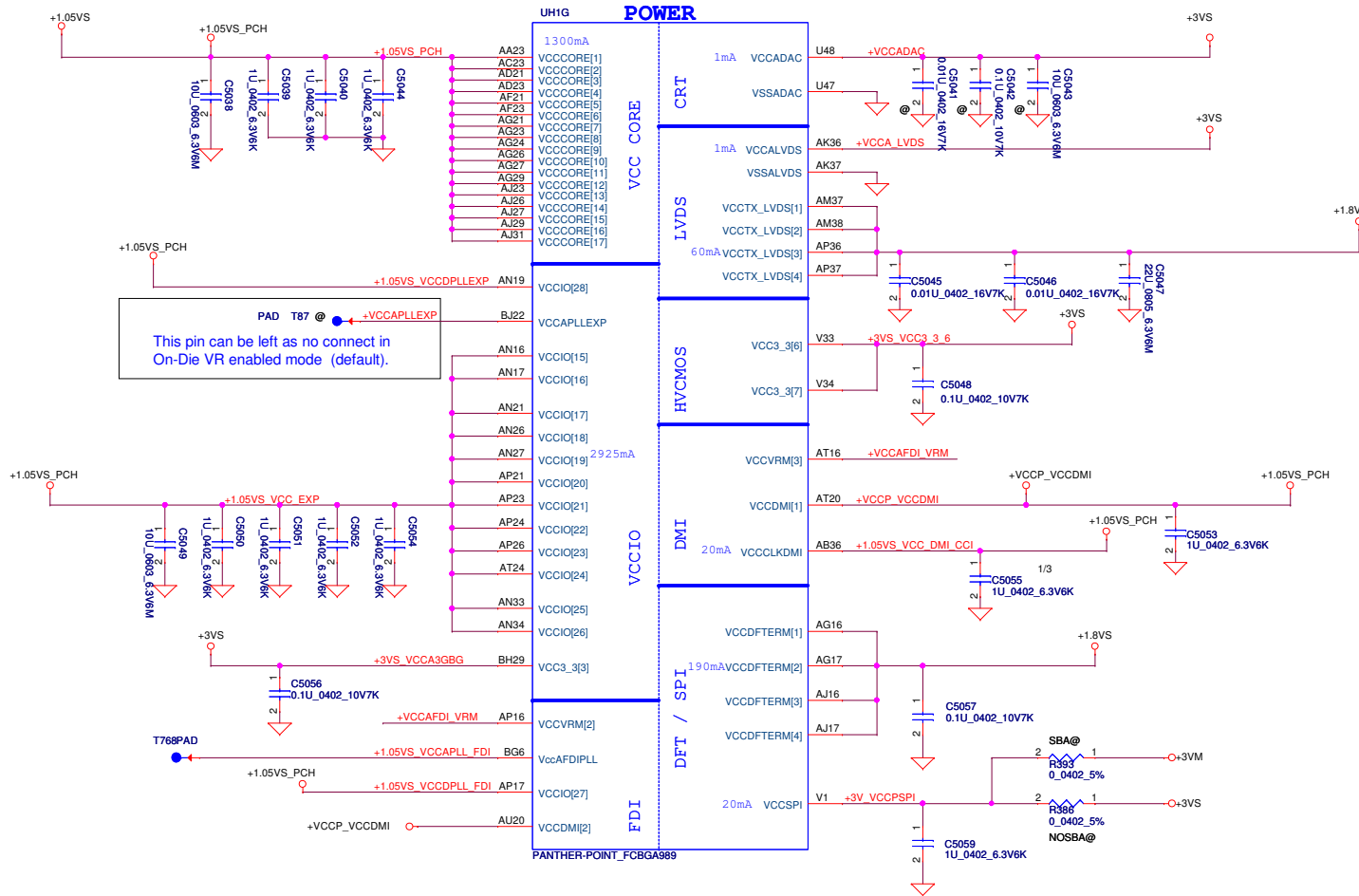
PCH_GPIO69	PCH_GPIO38	PCH_GPIO67	Function	GPU_ID
0	0	0	PX4.0	0
0	0	1	Reserved	1
0	1	0	DIS	2
0	1	1	UMA	3



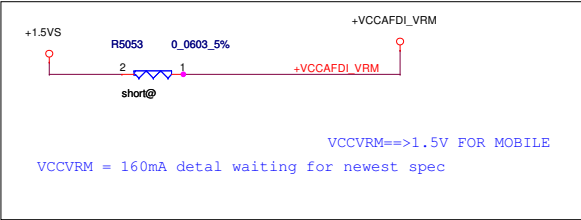
FOR PROCESSOR SELECT
NV_CLE
CLOSE TO THE BRANCHING POINT
H_SNB_IVB# [5]
R4914 2.2K 0402 5%
R260 10K 0402 5%
+3VS

INIT3_3V
This signal has weak internal PU, can't pull low
Intel schematic revieve recommend.

RAM_ID3	RAM_ID2	RAM_ID1	RAM_ID0	RAM
GPIO48	GPIO16	GPIO70	GPIO71	
0	0	0	0	ELPIDA 4GB
0	0	0	1	SAMSUNG 4GB
0	0	1	0	HYNIX 4GB
0	0	1	1	ELPIDA 8GB
0	1	0	0	SAMSUNG 8GB
0	1	0	1	HYNIX 8GB
0	1	1	0	ELPIDA 2GB
0	1	1	1	SAMSUNG 2GB
1	0	0	0	HYNIX 2GB
1	0	0	1	TBD
1	0	1	0	TBD
1	0	1	1	TBD
1	1	0	0	TBD
1	1	0	1	TBD
1	1	1	0	TBD
1	1	1	1	TBD

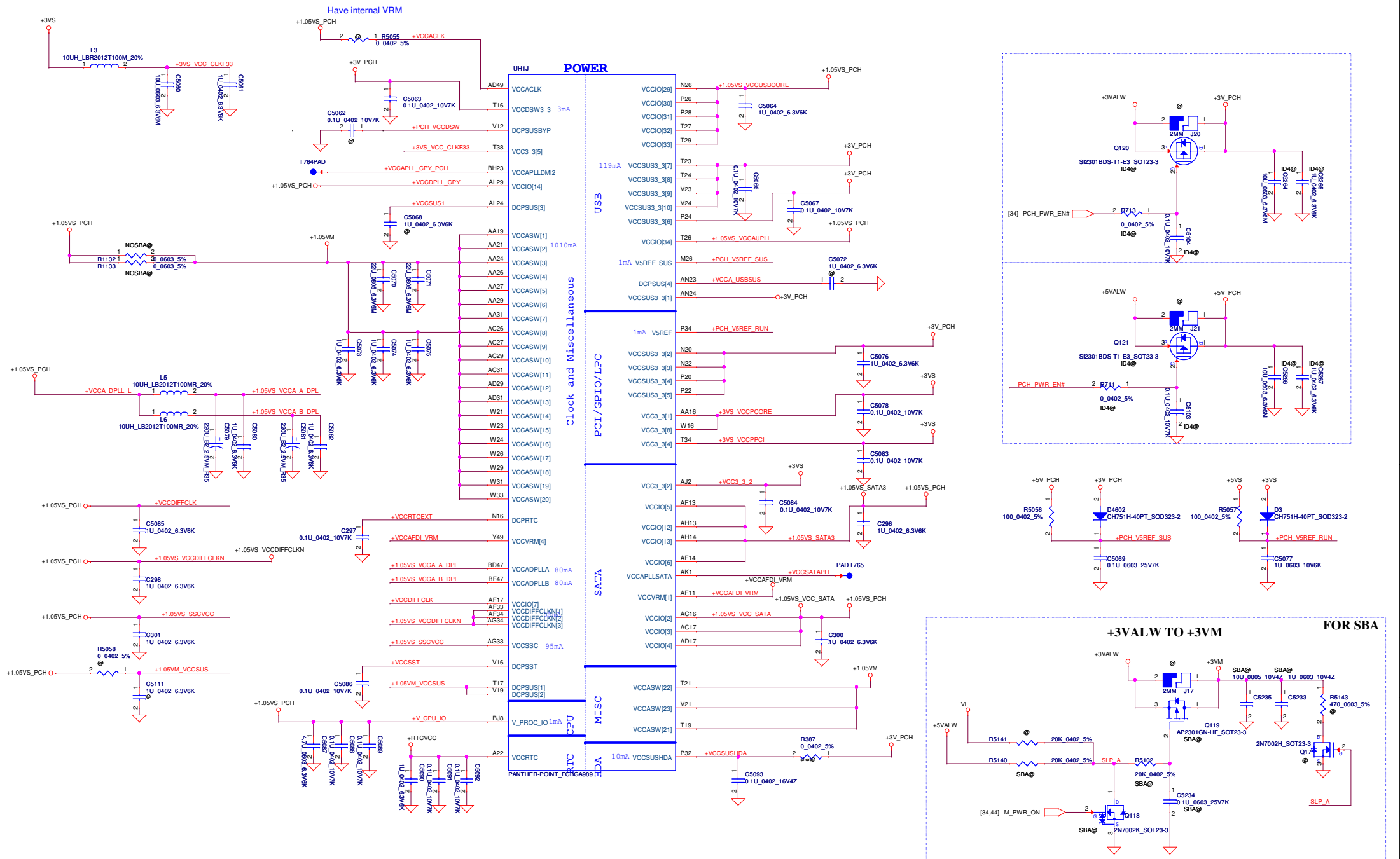


PAD T87 @ \leftarrow -VCCAPLLEXP
 This pin can be left as no connect in On-Die VR enabled mode (default).



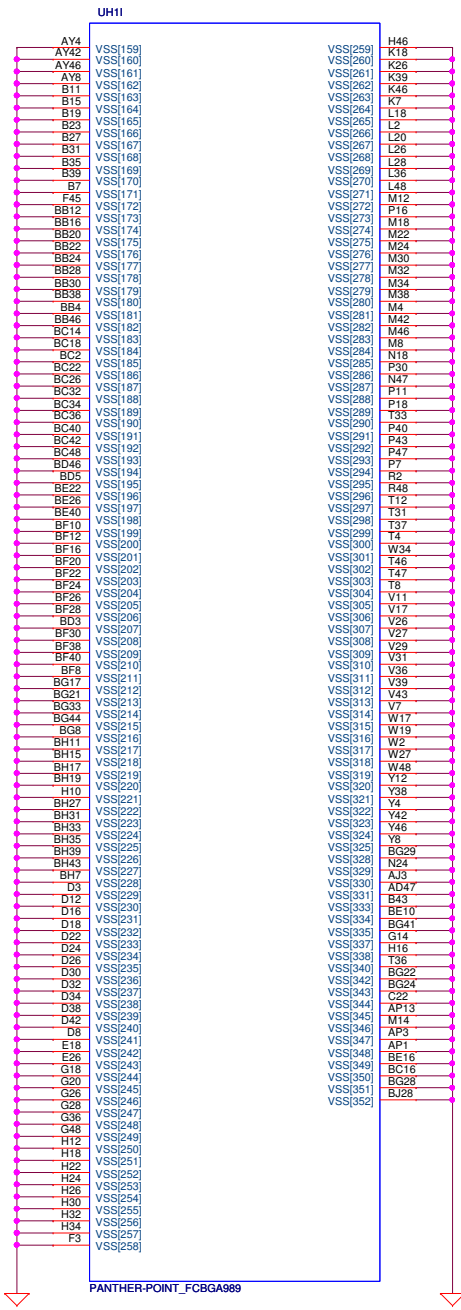
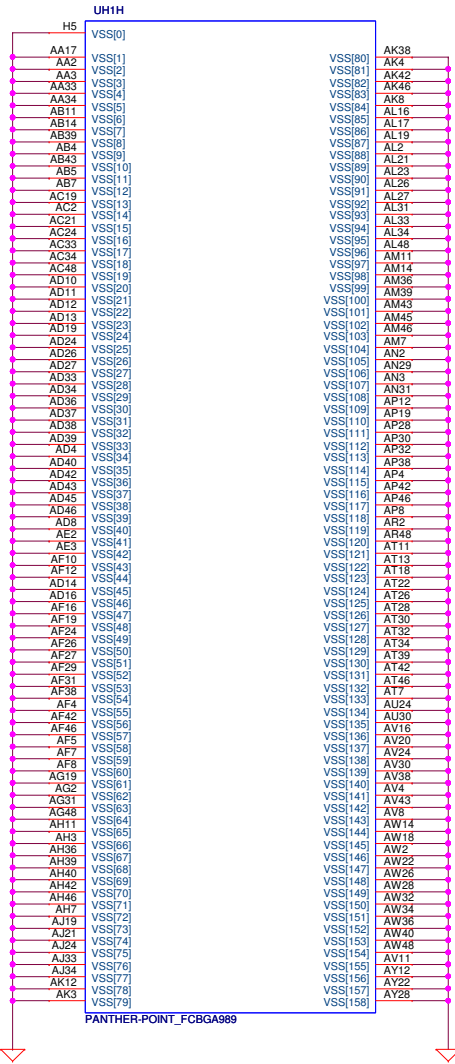
PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccLVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

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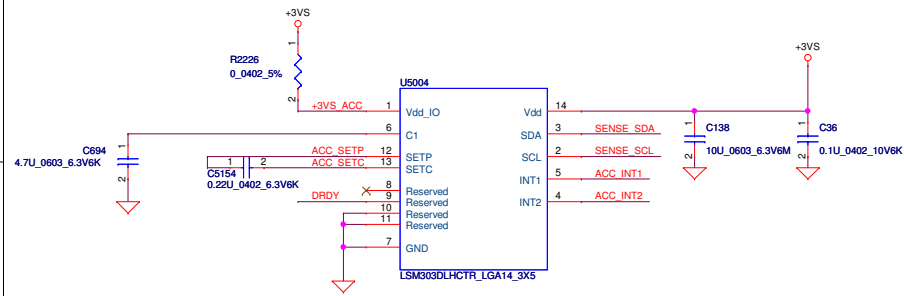
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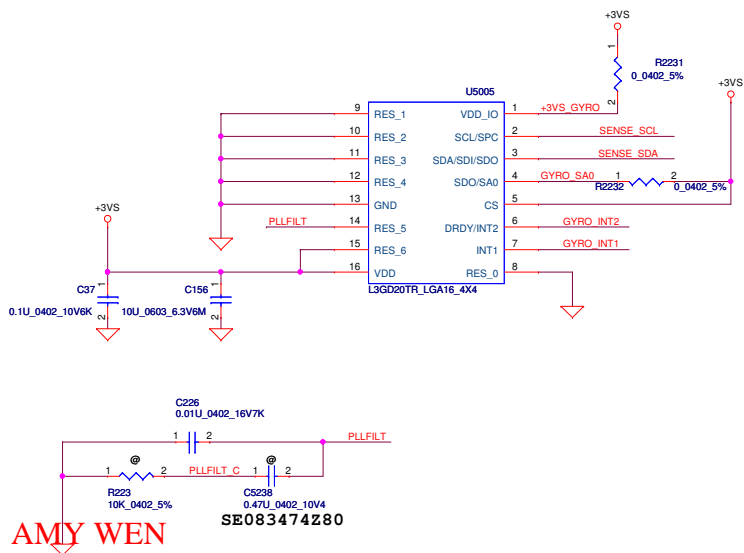
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Accelerometer + eCompass



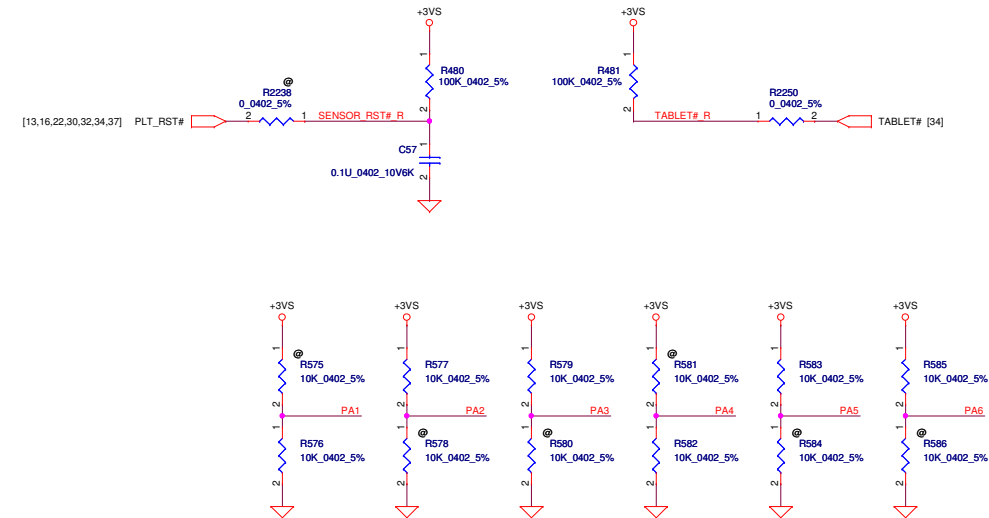
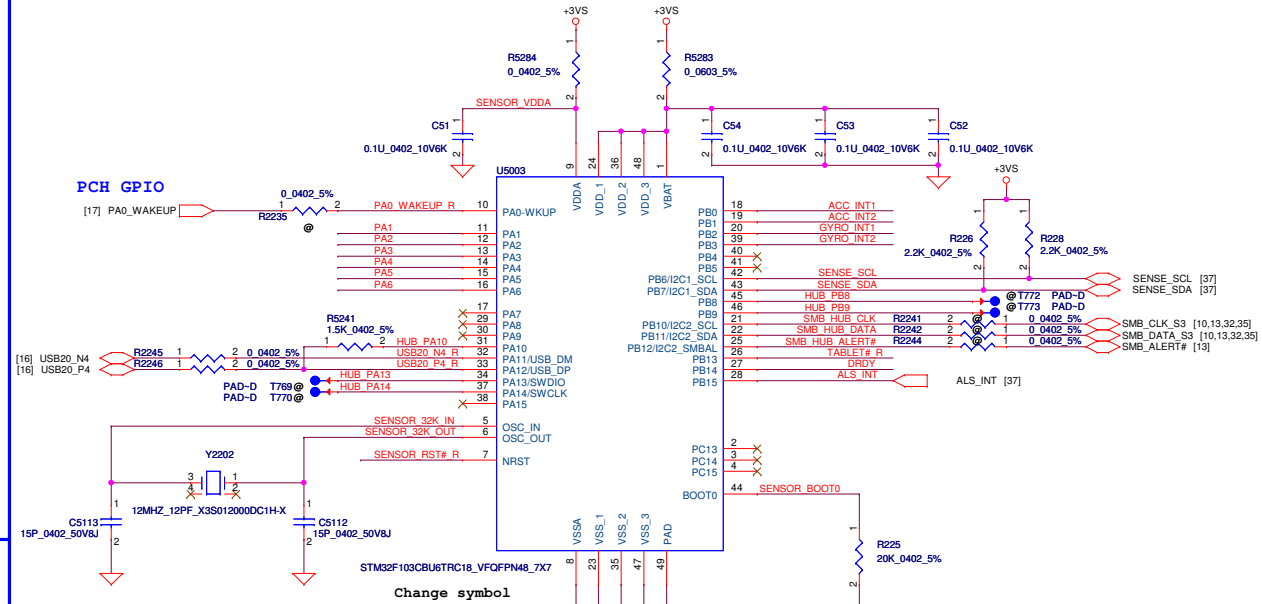
Gyro



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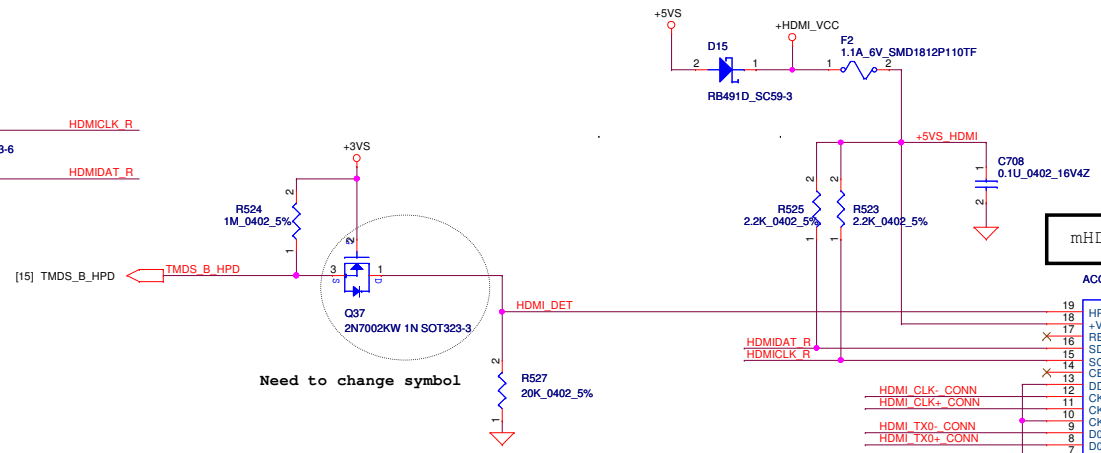
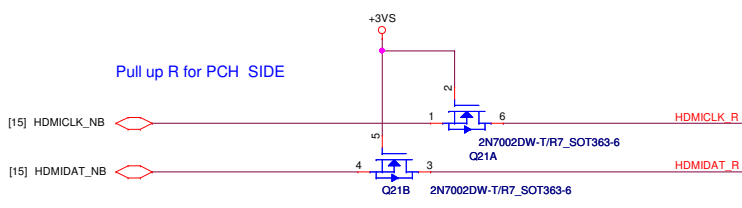
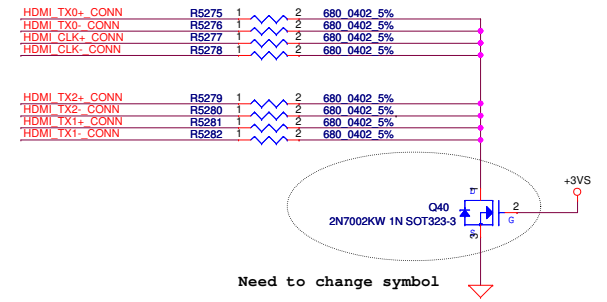
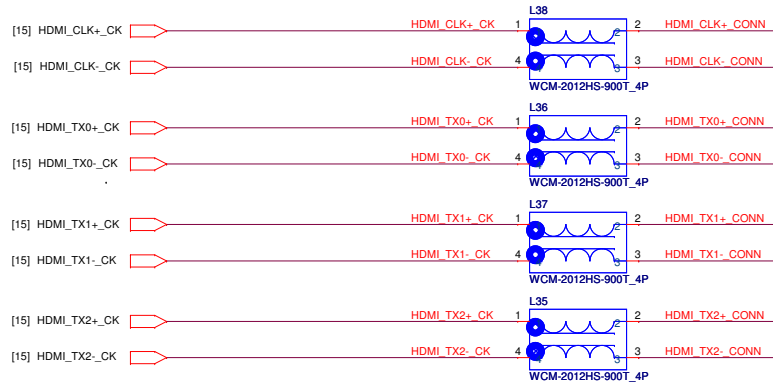
SE083474280

Sensor Hub

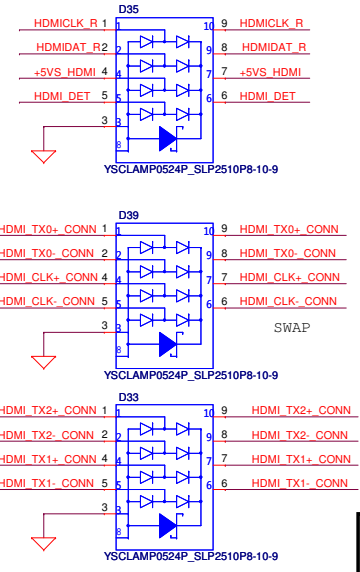


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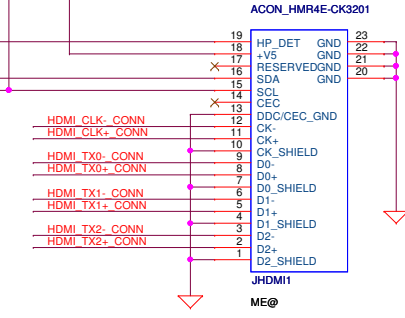
PN:SM070001S00x 4



Type-C
mHDMI PN:SP060005H00



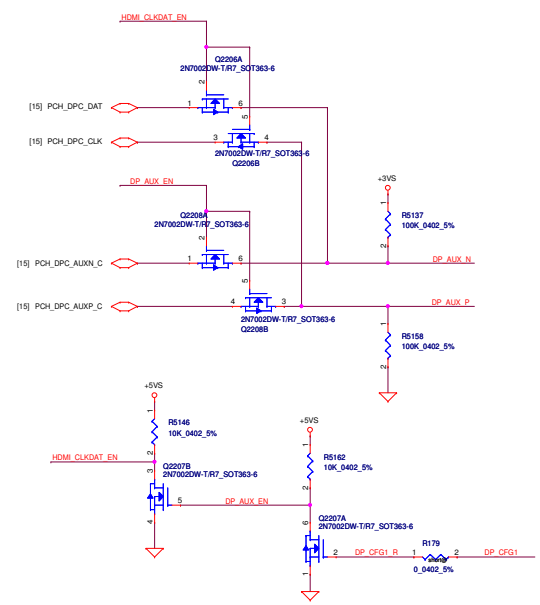
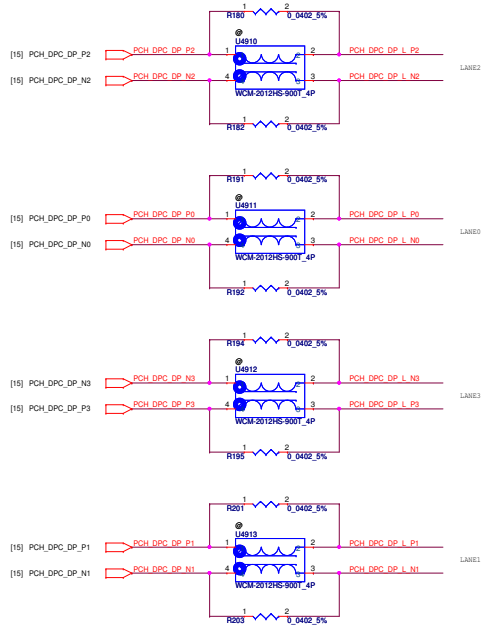
1'SPN: SC300001Y00
2'SPN: SC300002800



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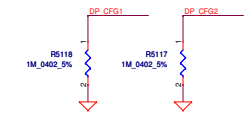
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Close to JmDP1

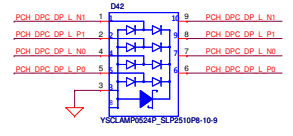
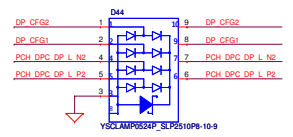
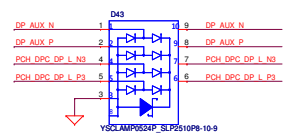
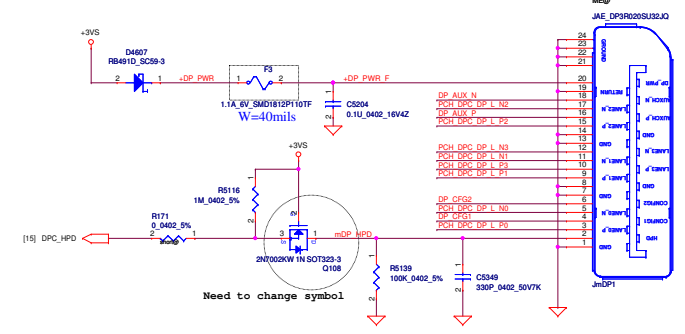


TBT, HDMI, DP mode table

HPD	CFG1	CFG2	LSRX	Mode
1	0	0	X	DP
1	1	X	X	HDMI
0	0	1	1	TBT



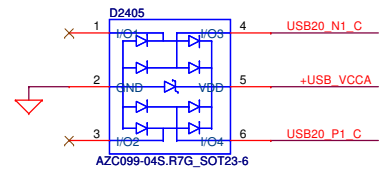
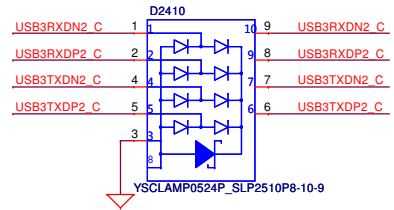
mini DP type



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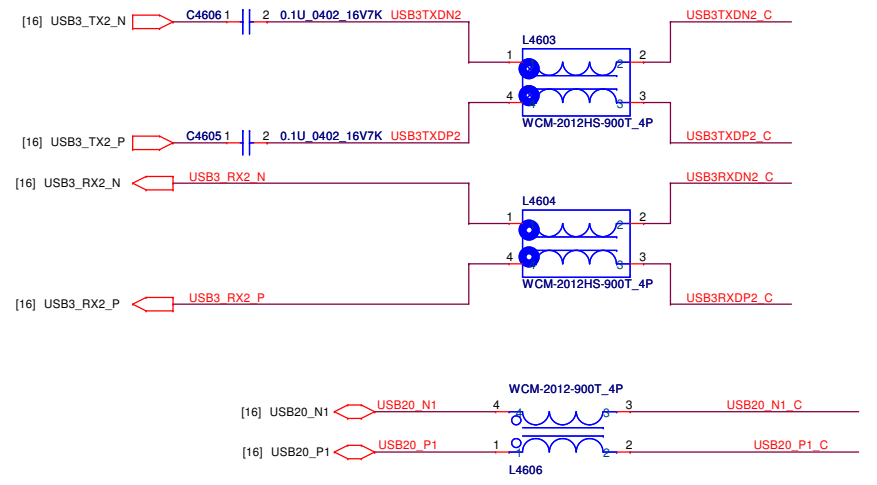
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			mDP Connector		
			Size	Document Number	Rev
			Custom	LA-8671P_SDV	1.0
			Date:	Thursday, October 04, 2012	Sheet 28 of 80

1'SPN: SC300001Y00
2'SPN: SC300002800

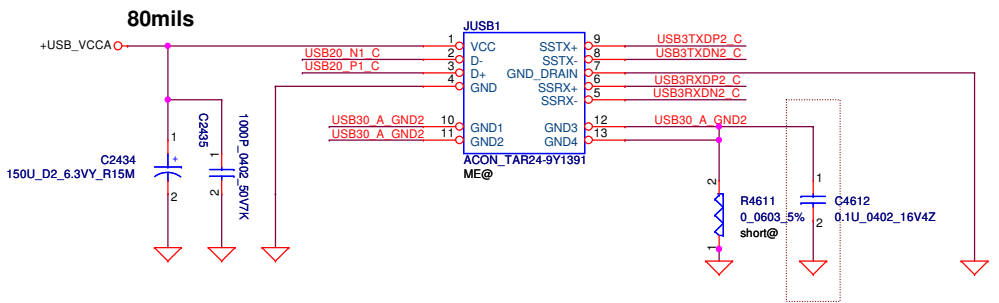
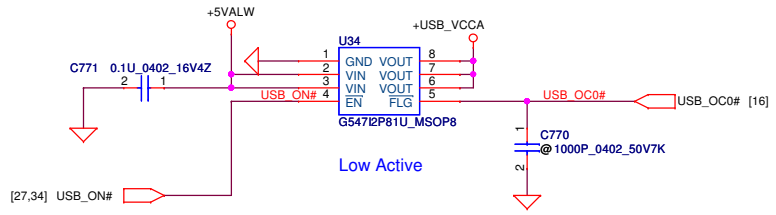


1'S PN: SC300001G00
2'S PN: SC300002E00

JUSB1USB3.0/USB2.0



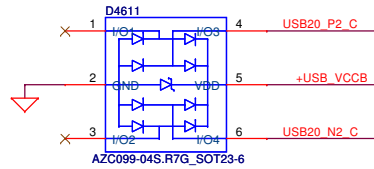
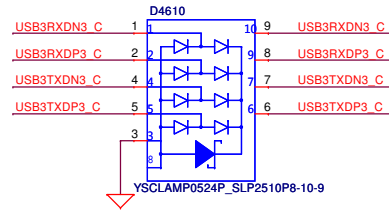
DC23300A410



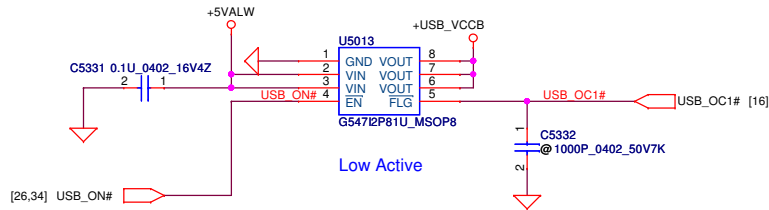
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Size	Custom	Document Number	LA-8671P_SDV	Rev	1.0
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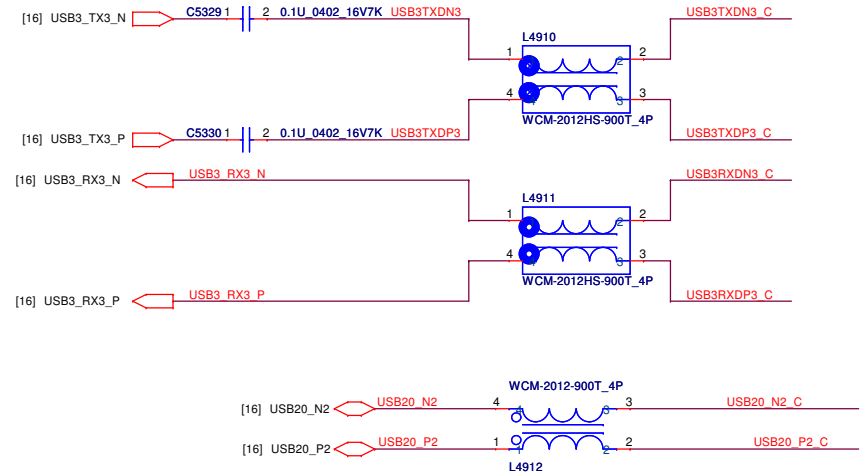
1'SPN: SC300001Y00
2'SPN: SC300002800



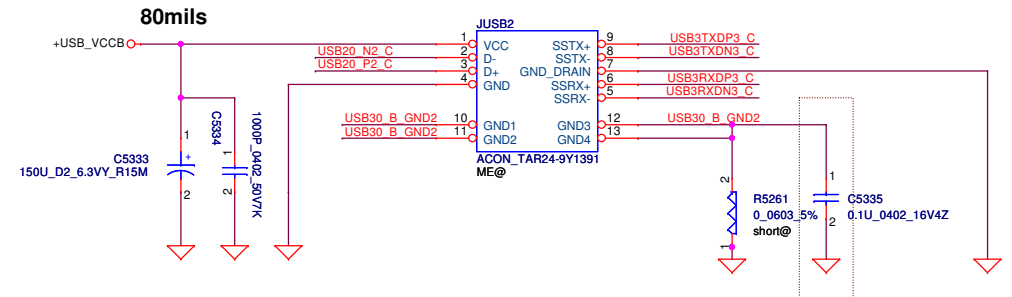
1'S PN: SC300001G00
2'S PN: SC300002E00



JUSB1USB3.0/USB2.0



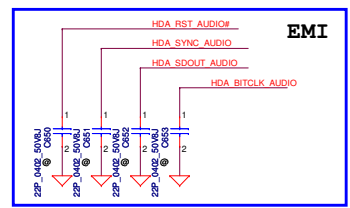
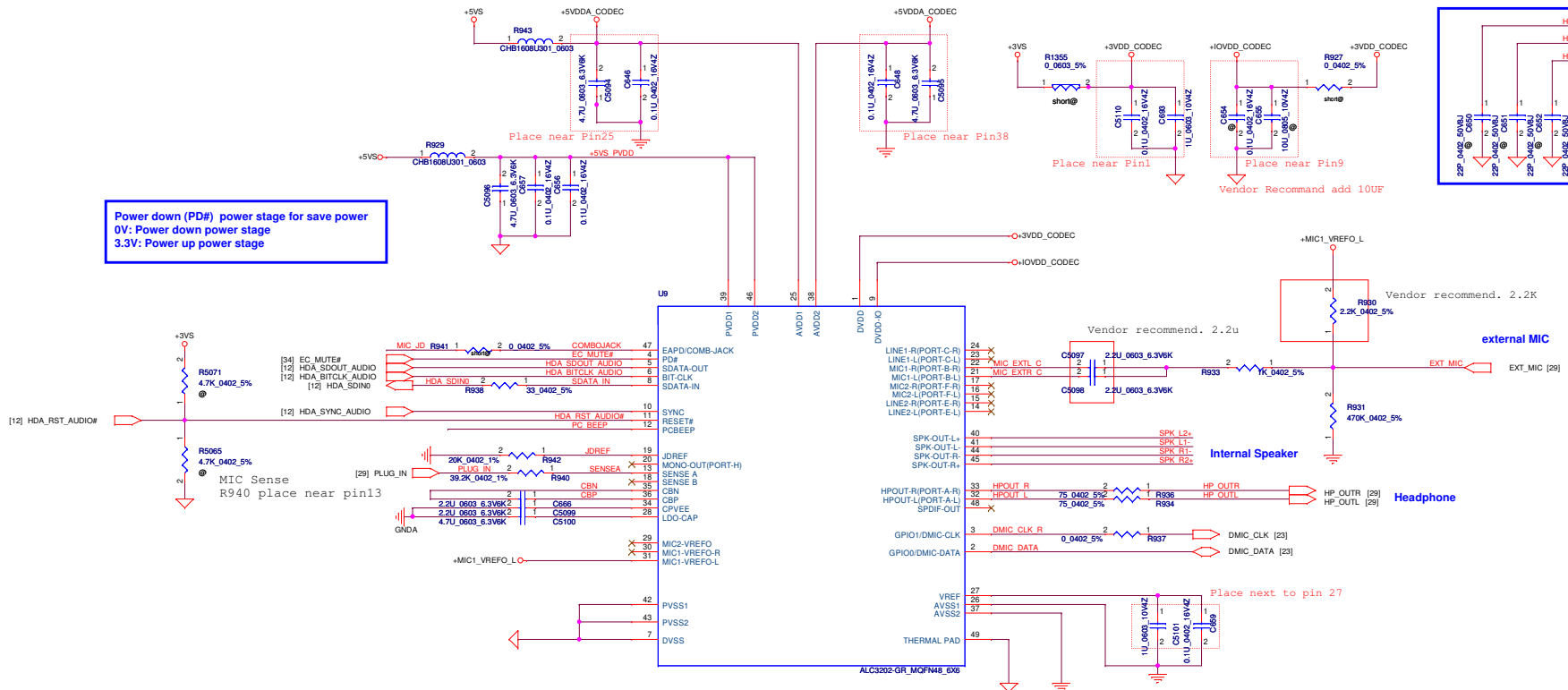
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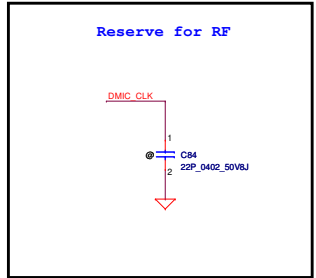
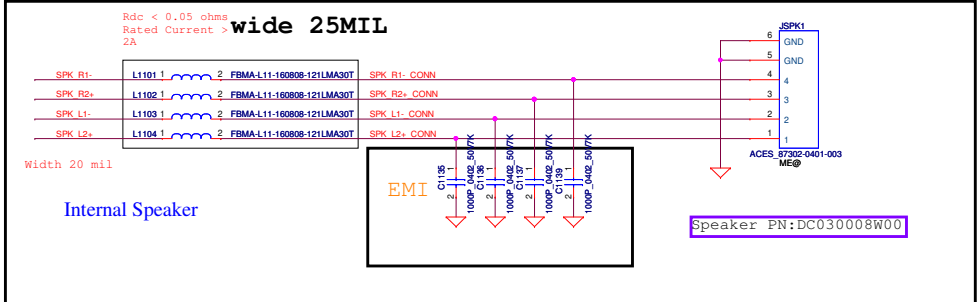
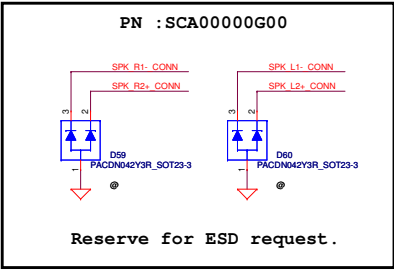
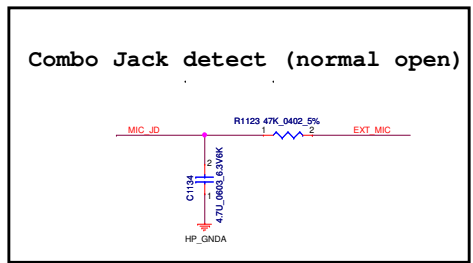
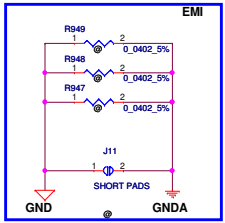
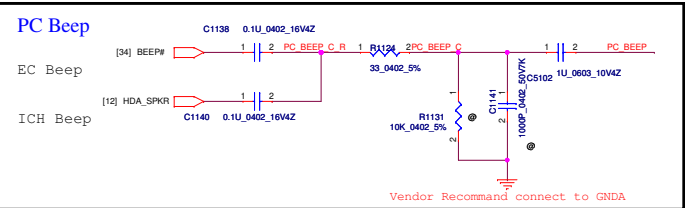
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Issued Date	2011/05/16	Deciphered Date	2013/05/16	Title	
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Size	Custom	Document Number	LA-8671P_SDV	Rev	1.0
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Power down (PD#) power stage for save power
 0V: Power down power stage
 3.3V: Power up power stage



SA00058310
 Change symbol

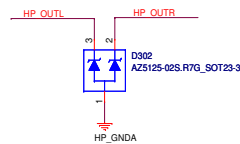
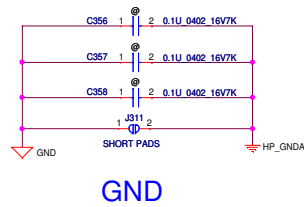
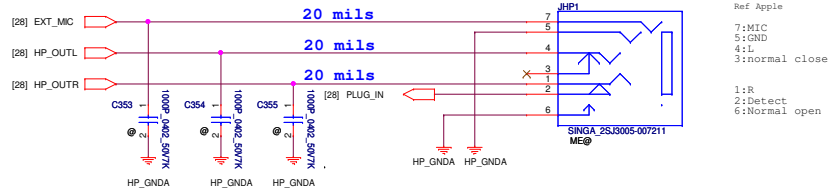
Pin Assignment	Location	Function
SPK-OUT (Pin40/41/44/45)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
MIC1 (Pin21/22)	External	Mic in



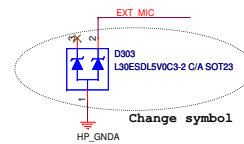
AMY WEN

PN:DC230008E00

Choose normal-open type!



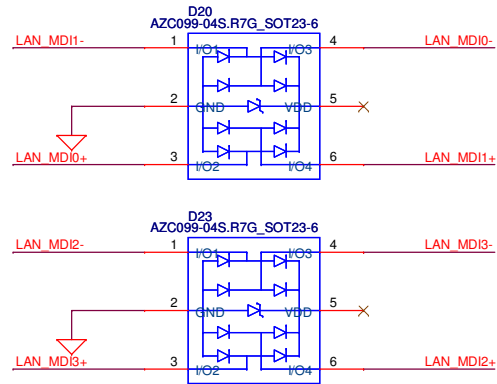
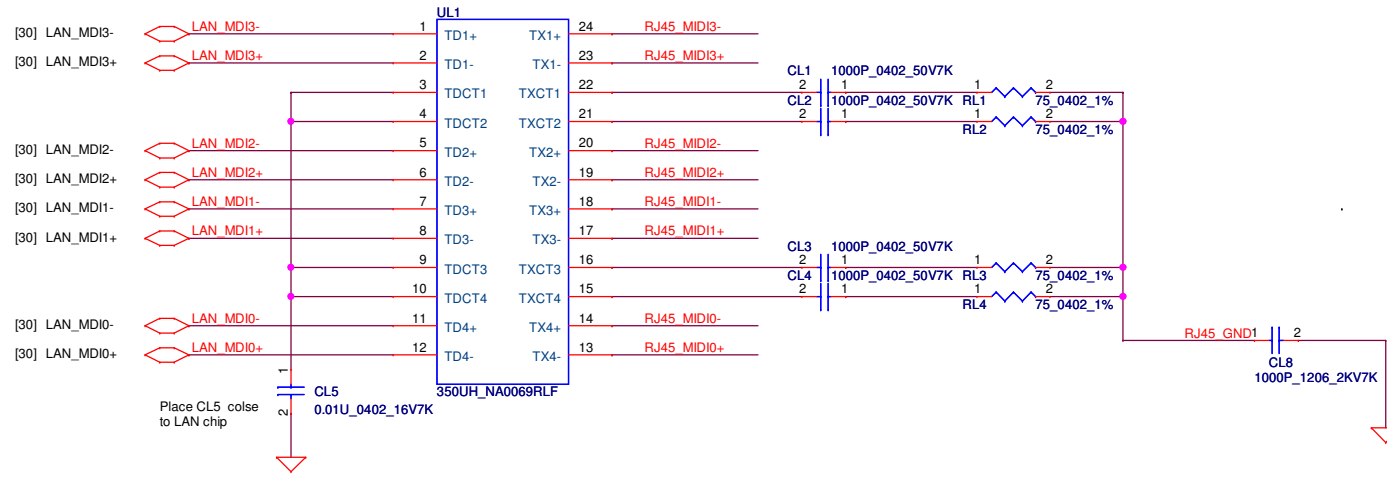
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PN: SCA00001L00

AMY WEN

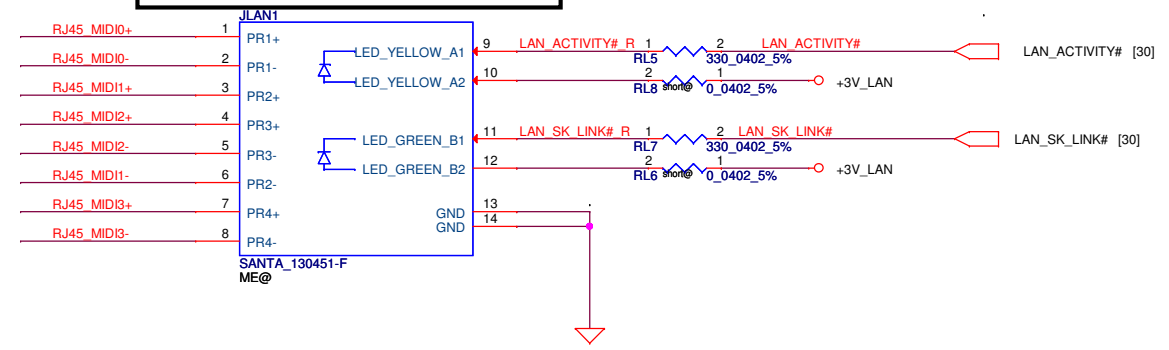
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Issued Date	2011/05/16	Deciphered Date	2013/05/16	Title
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				LA-8671P_SDV
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				Date: Thursday, October 04, 2012 Sheet 29 of 50



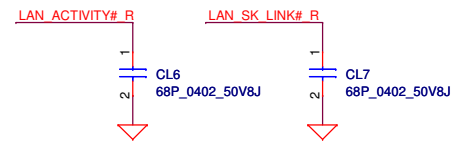
D20/D23
 1'S PN:SC300001G00
 2'S PN:SC300002E00

DC234005300
LAN Conn.

RL5,RL7 Vendor recommend 510 ohm

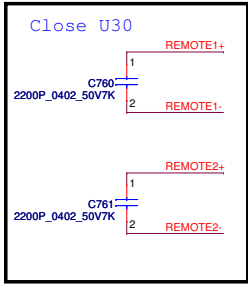


For EMI's request

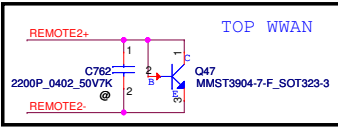
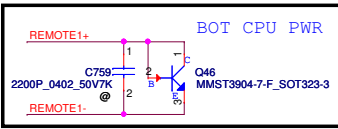
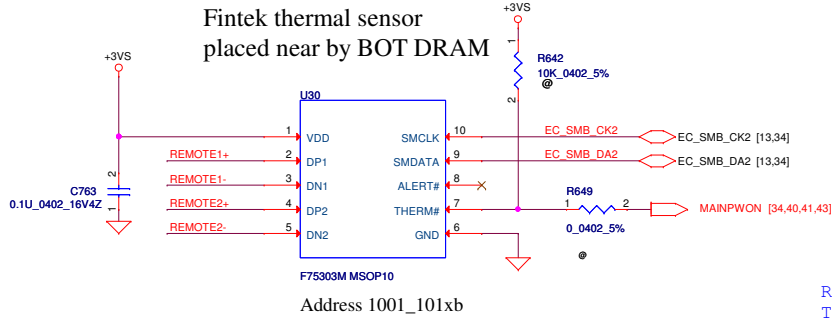


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Size	Document Number	Rev		1.0	
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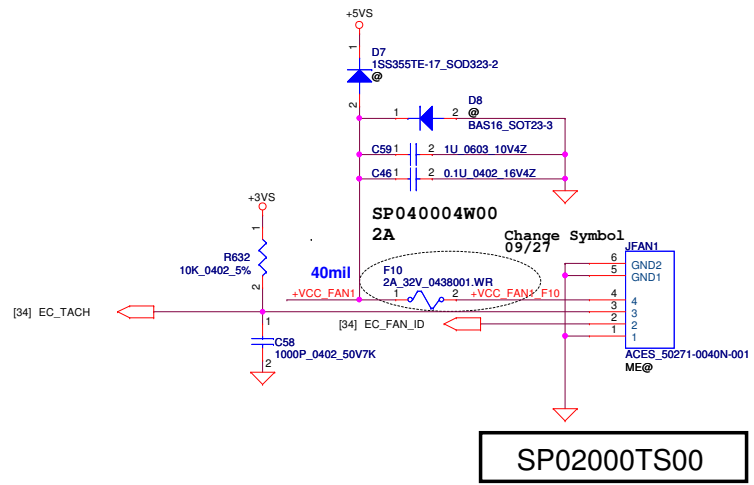
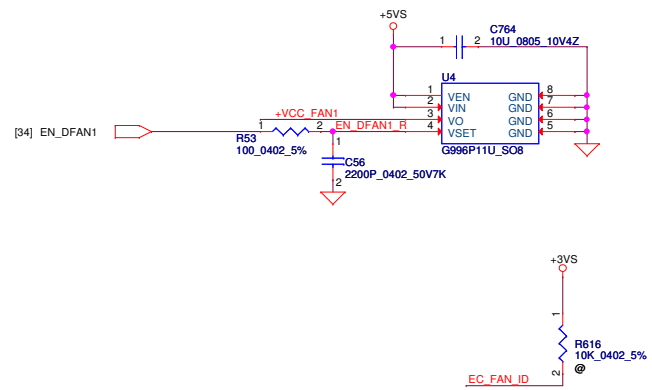


Fintek thermal sensor placed near by BOT DRAM

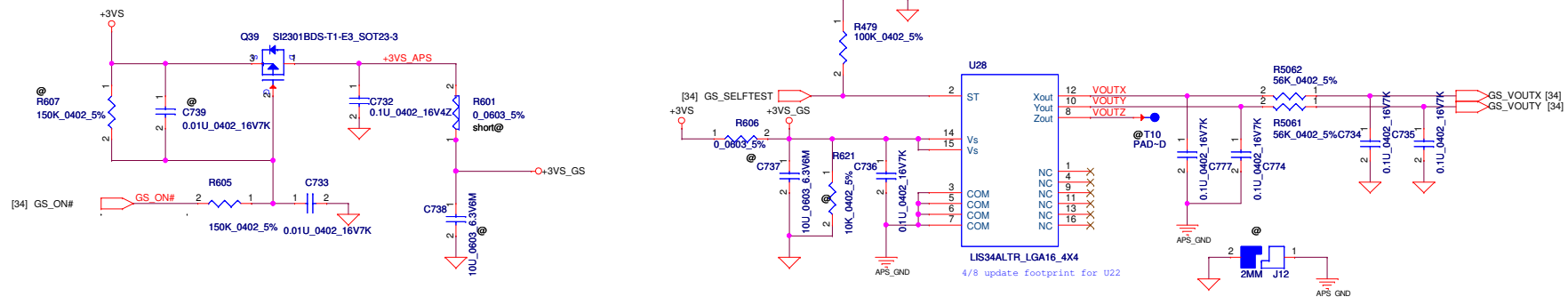


REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN +5VS DROOP



APS G-Sensor



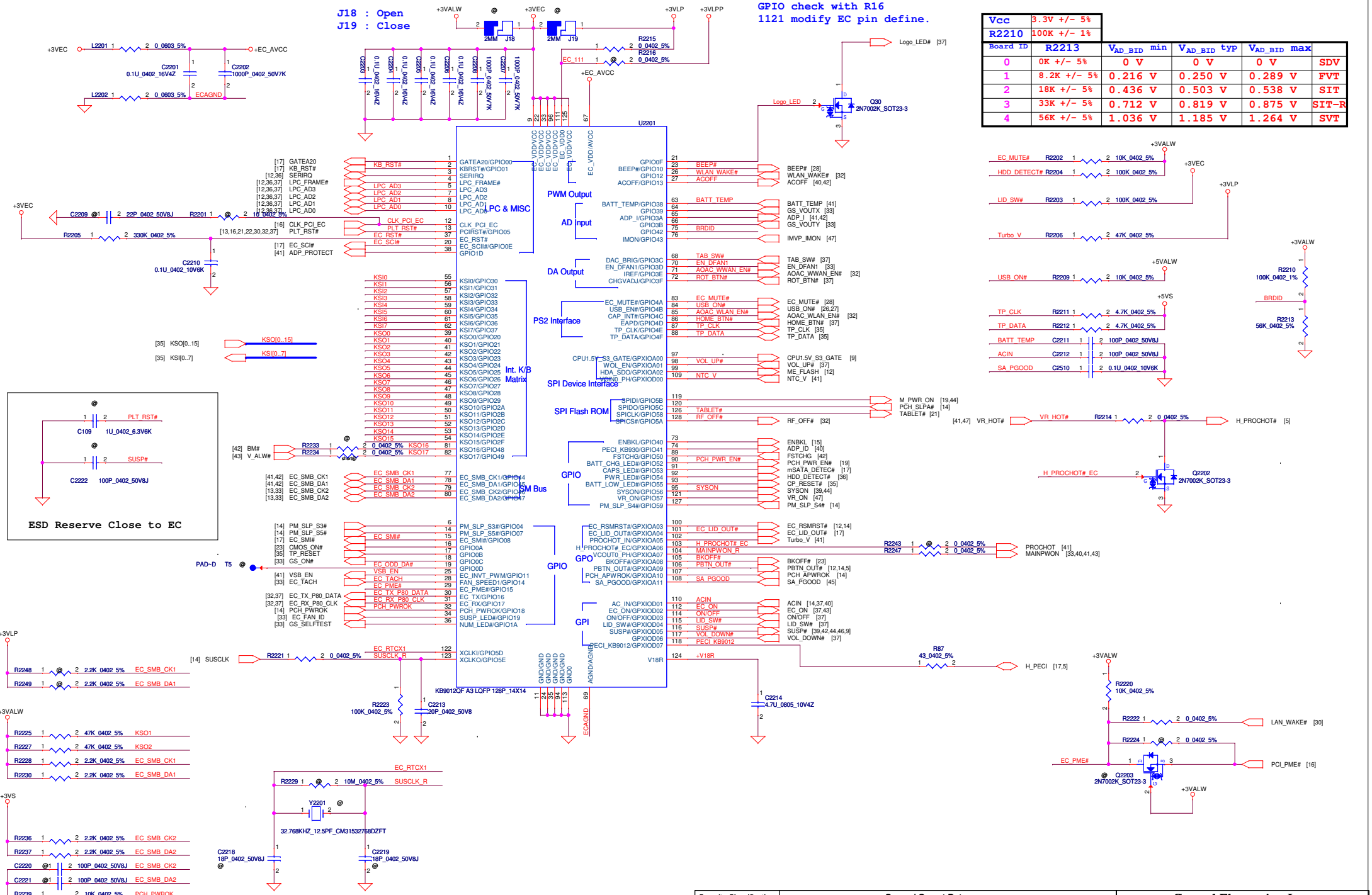
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				FintekF57303_Thermal sensor/FAN
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J18 : Open
J19 : Close

GPIO check with R16
I121 modify EC pin define.

Vcc		3.3V +/- 5%		R2210		100K +/- 1%	
Board ID	R2213	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max			
0	0K +/- 5%	0 V	0 V	0 V	SDV		
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	FVT		
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	SIT		
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	SIT-R		
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	SVT		

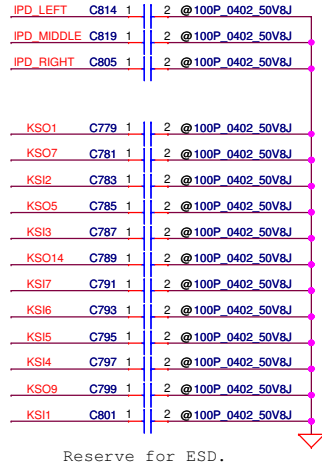
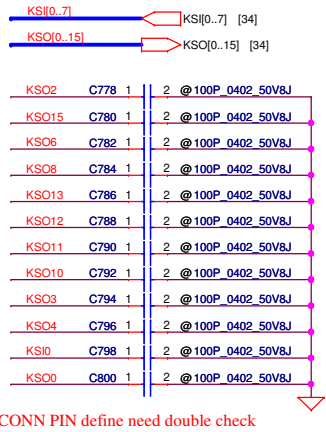


ESD Reserve Close to EC

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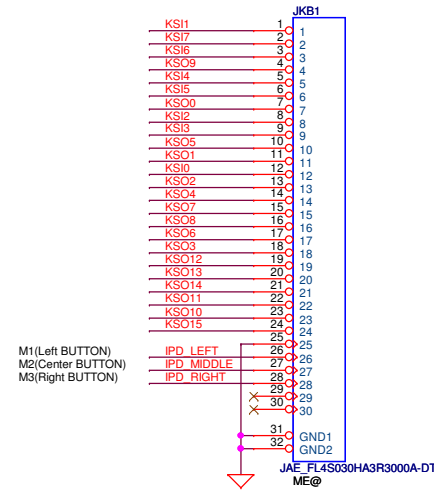
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Size	Document Number	Flow		
Custom	LA-8671P_SDV	1.0		
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INT_KBD Conn.



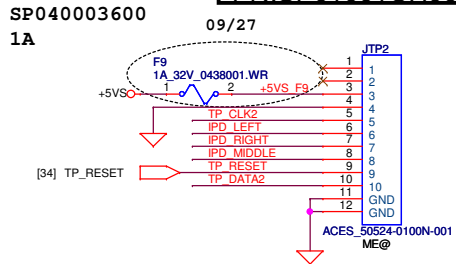
INT_KBD Conn.

PN:SP01000YH00



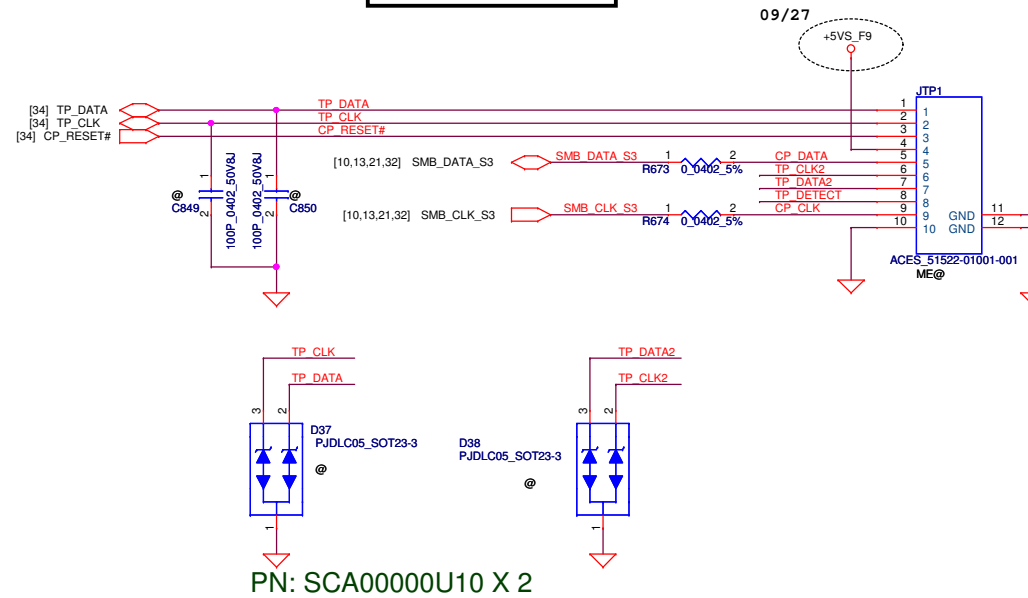
Track point

PN:SP01001CH00



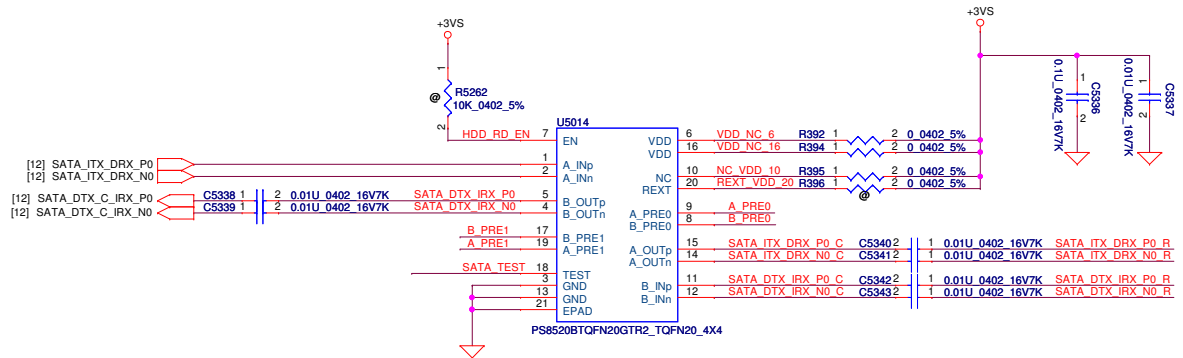
Click pad 10PIN

SP01001AL00

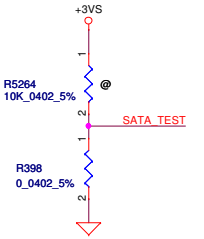
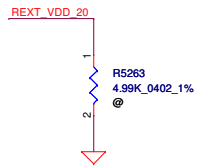


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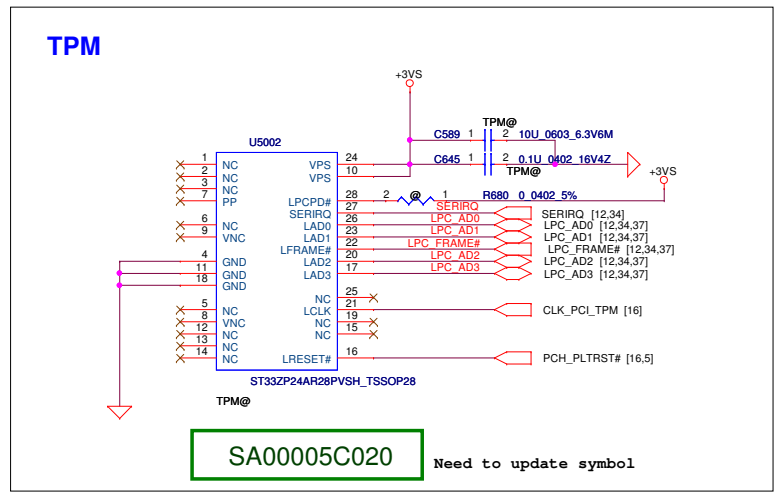


	TEST (Internal Low)
Normal Mode (Default)	LOW
Test Mode	HIGH



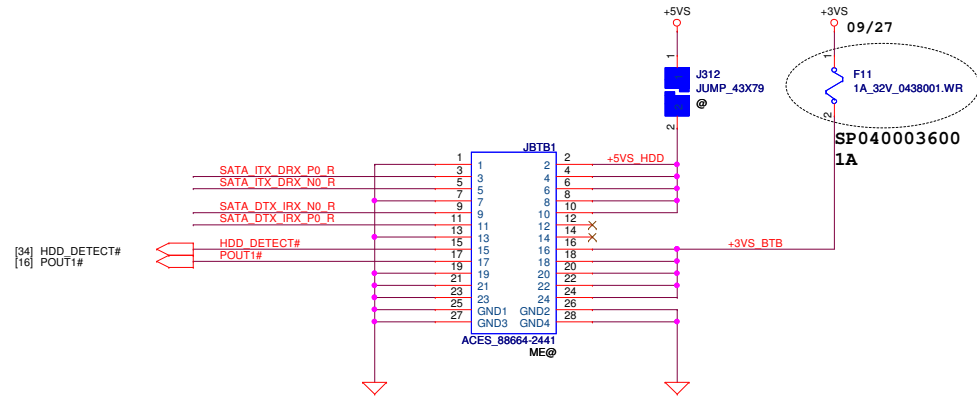
Remove pull-low

	A_PRE1/B_PRE1 (Internal pull Low)	A_PRE0/B_PRE0 (Internal pull Low)
0dB, no pre-emphasis	Low	Low
1.5dB pre-emphasis is selected	Low	High
2.5dB pre-emphasis is selected	High	Low
3.5dB pre-emphasis is selected	High	High



SA00005C020

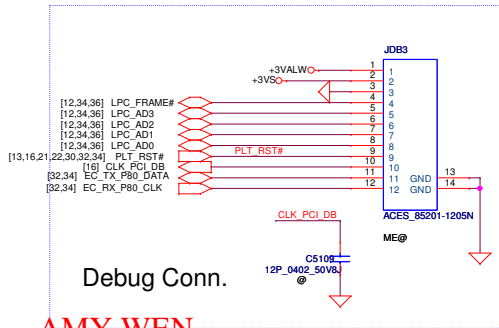
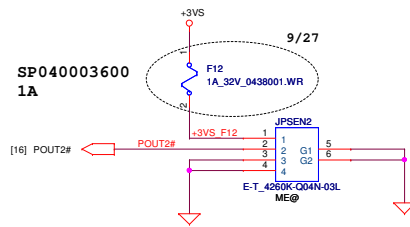
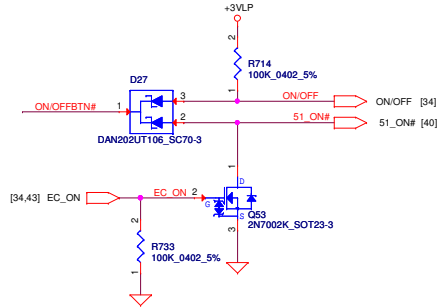
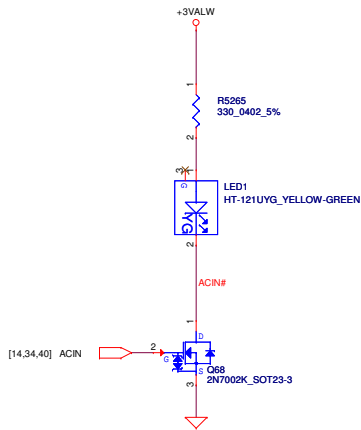
Need to update symbol



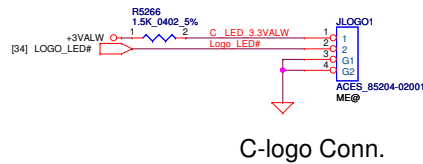
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Size	Document Number	Customer	Rev	1.0
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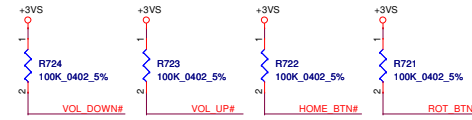
AC-IN LED (Color : Green)



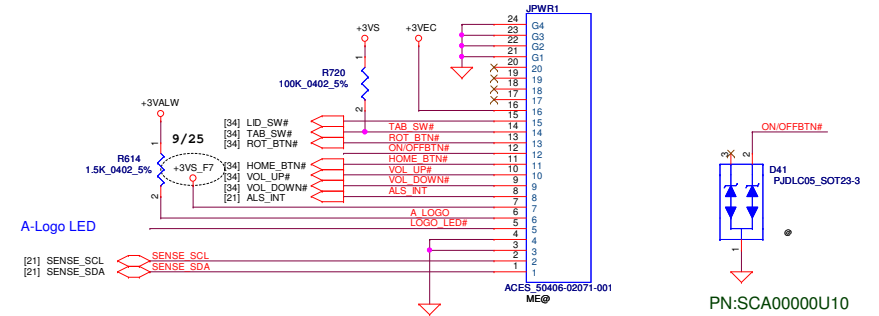
AMY WEN



C-logo Conn.



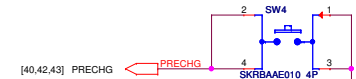
SP010016L00



Power Board connector

PN:SCA0000U10

BOTTOM SIDE
SN111005800 by ME drawing

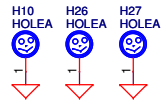


For Power Reset

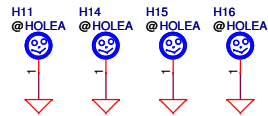
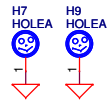
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Size	Document Number	Rev	1A	
Custom	LA-8671P_SDV	Date:	Thursday, October 04, 2012	Sheet 37 of 50

PT-H 20 SCREW HOLE

H_2P3



H_3P3



H_6P0



NON-PT-H 1 SCREW HOLE

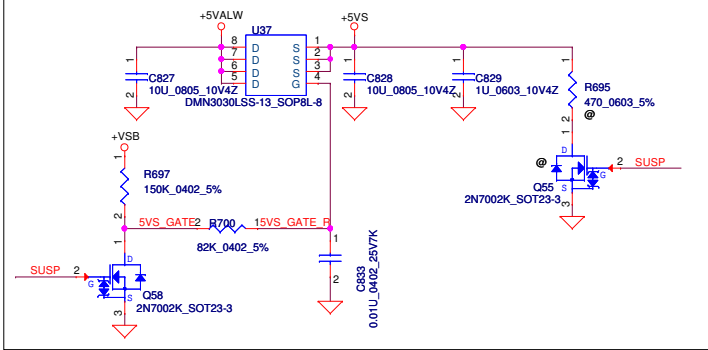
H_2P4N



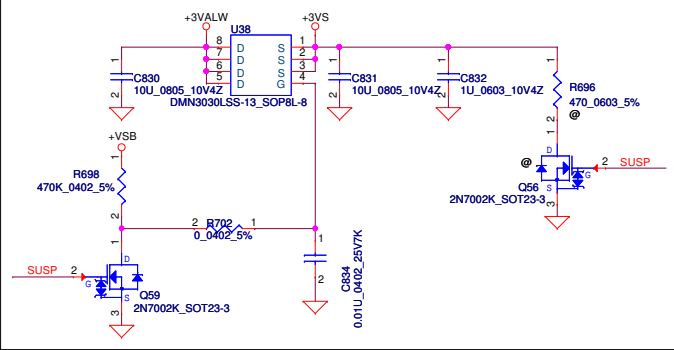
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			LA-8671P_SDV	1.0
Date:			Thursday, October 04, 2012	Sheet 38 of 50

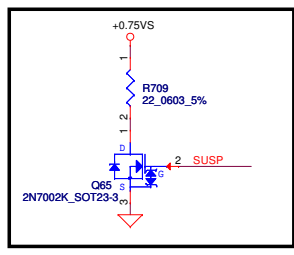
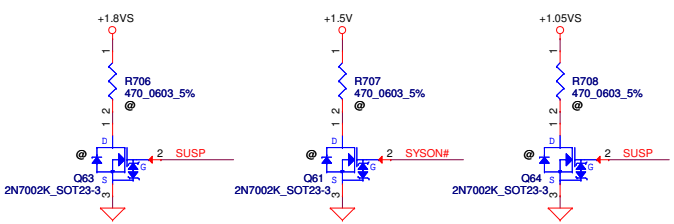
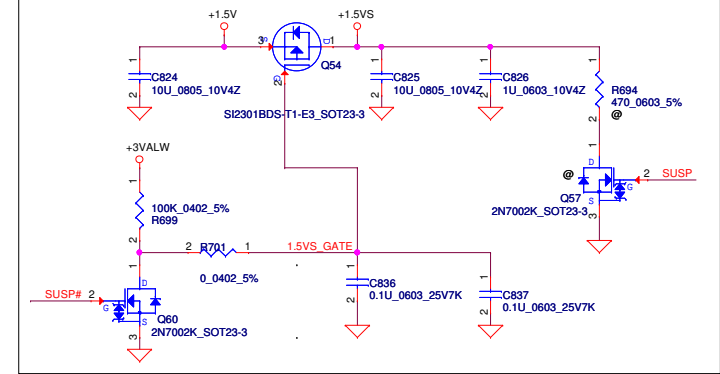
+5VALW TO +5VS



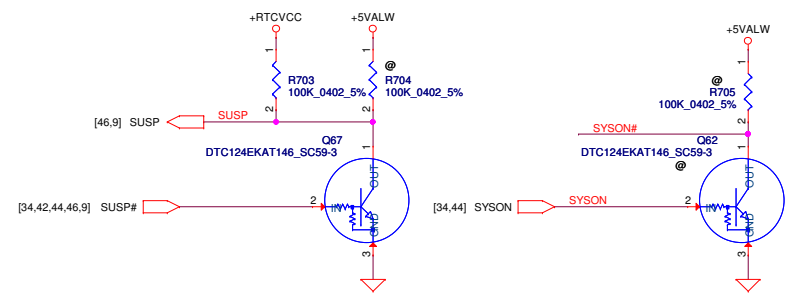
+3VALW TO +3VS



+1.5V to +1.5VS



For Intel S3 Power Reduction.

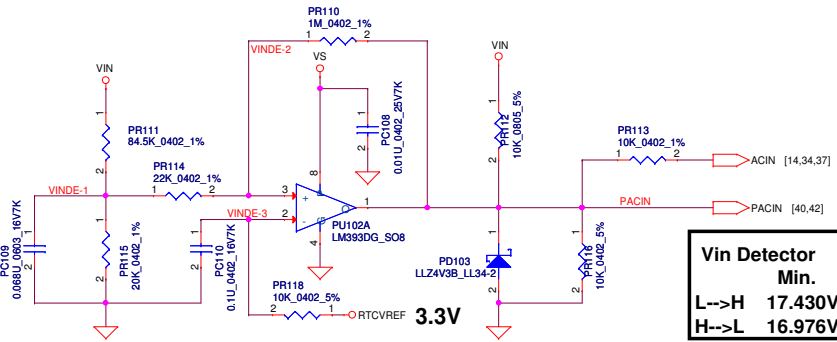
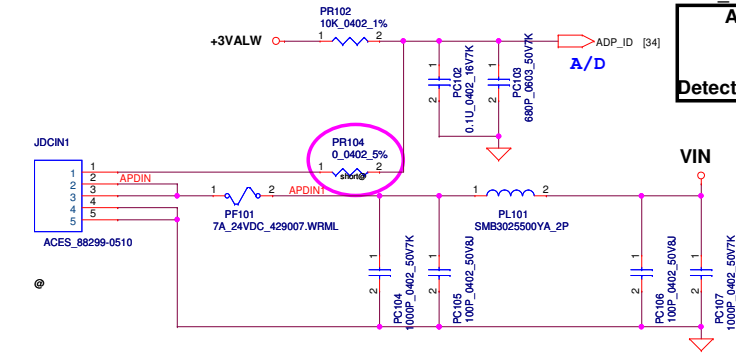


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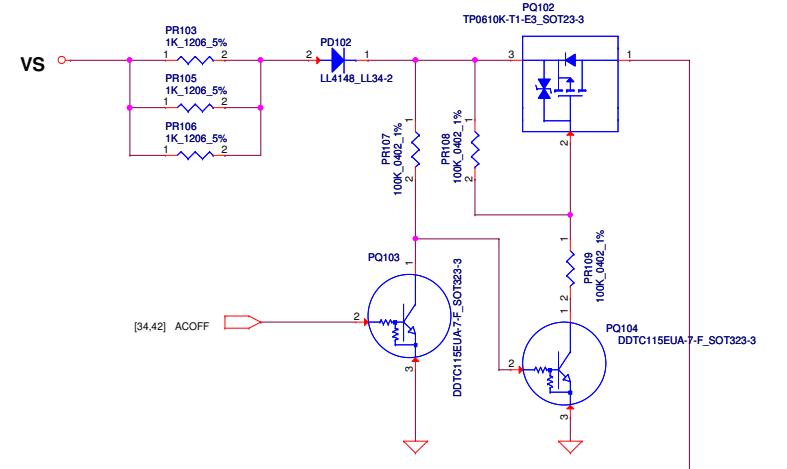
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/08/25	Deciphered Date	2012/08/25	Title	
				DC Interface	
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				Custom	1.0
				Date: Thursday, October 04, 2012	
				Sheet 39 of 50	

ADP_ID			
AC Adapter	90W	65W	
R(K ohm)	open	10	
ADP_ID(V)	3.3	1.65	
Detection voltage	>2.64	1.32~1.98	

**Precharge detector
15.97V/14.84V FOR
ADAPTOR**

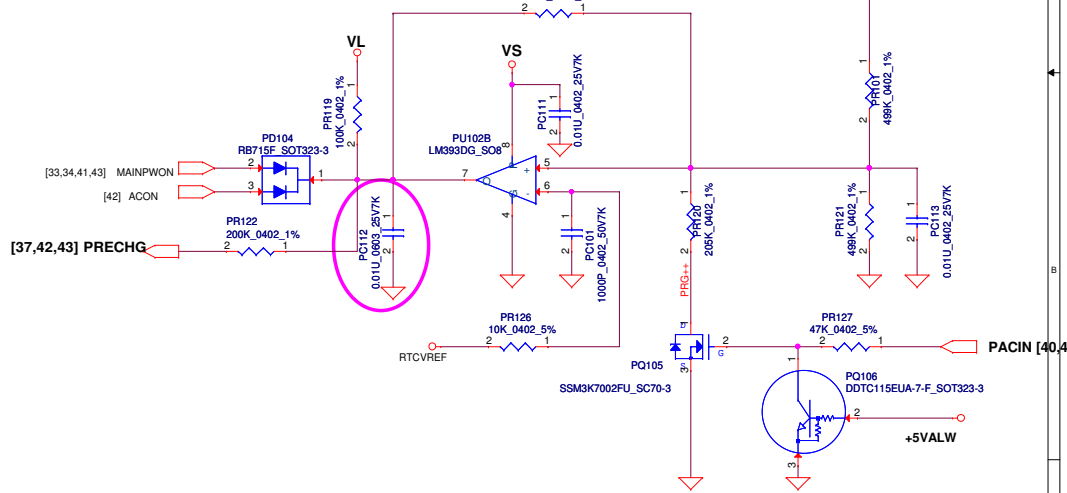
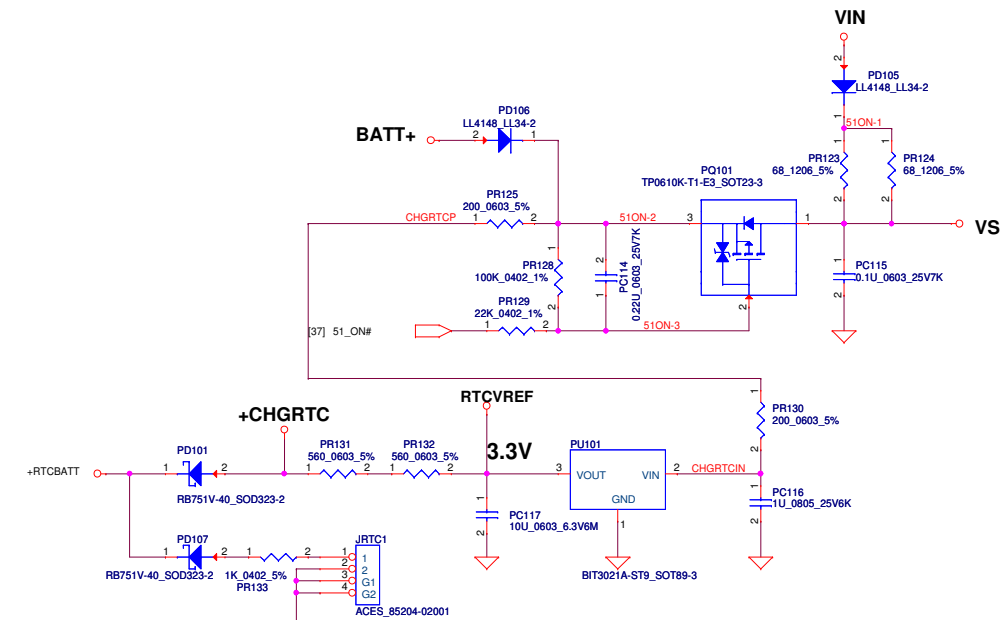


Vin Detector			
	Min.	typ.	Max.
L-->H	17.430V	17.901V	18.384V
H-->L	16.976V	17.262V	17.728V



ACIN			
Precharge detector			
	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

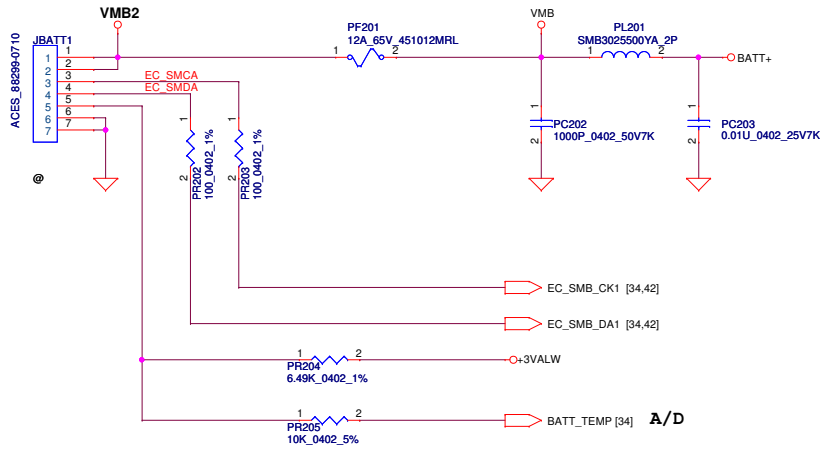
BATT ONLY			
Precharge detector			
	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V



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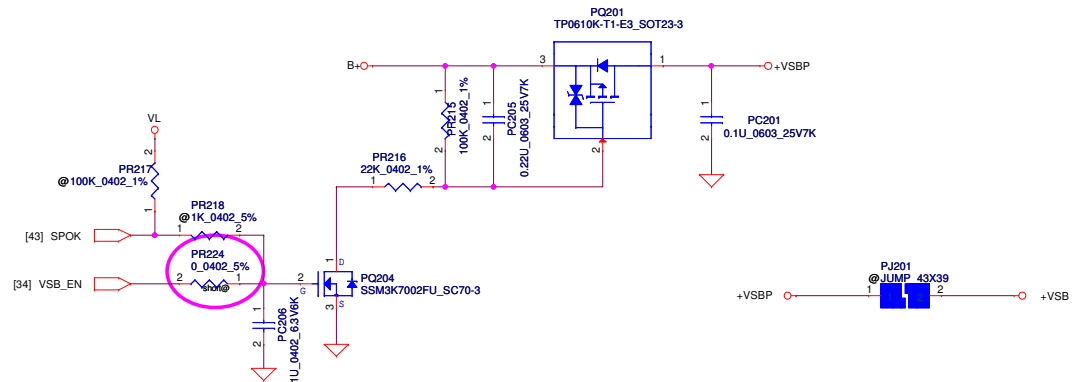
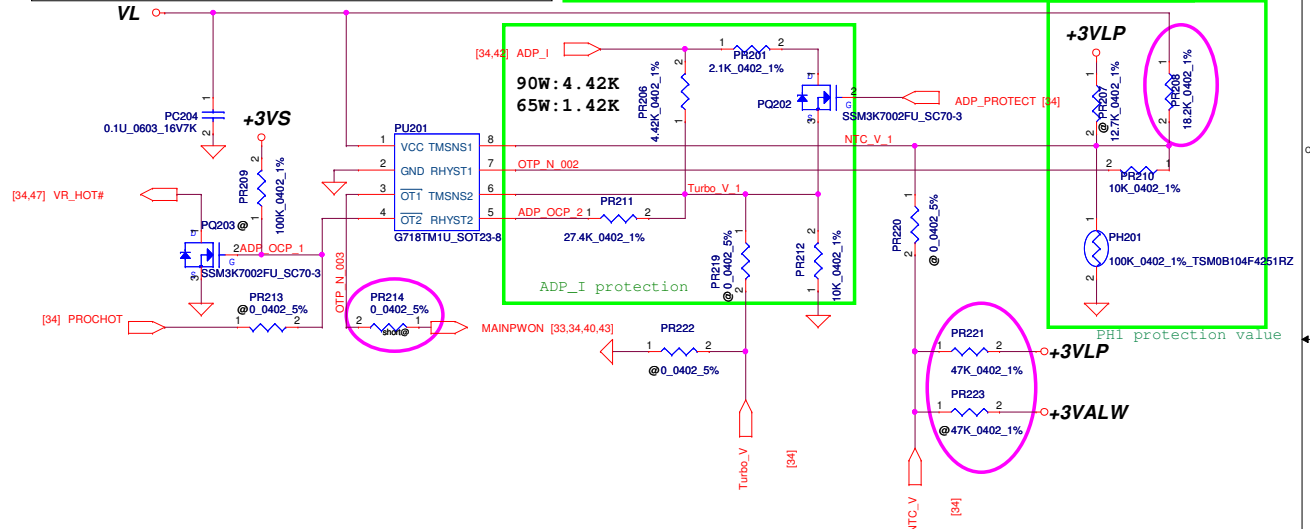
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31
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Compal Electronics, Inc.			
PWR DCIN / Vin Detector /Pre-charge			
Size	Document Number	Rev	
Custom	C38 Chief River Schematic	0.4	
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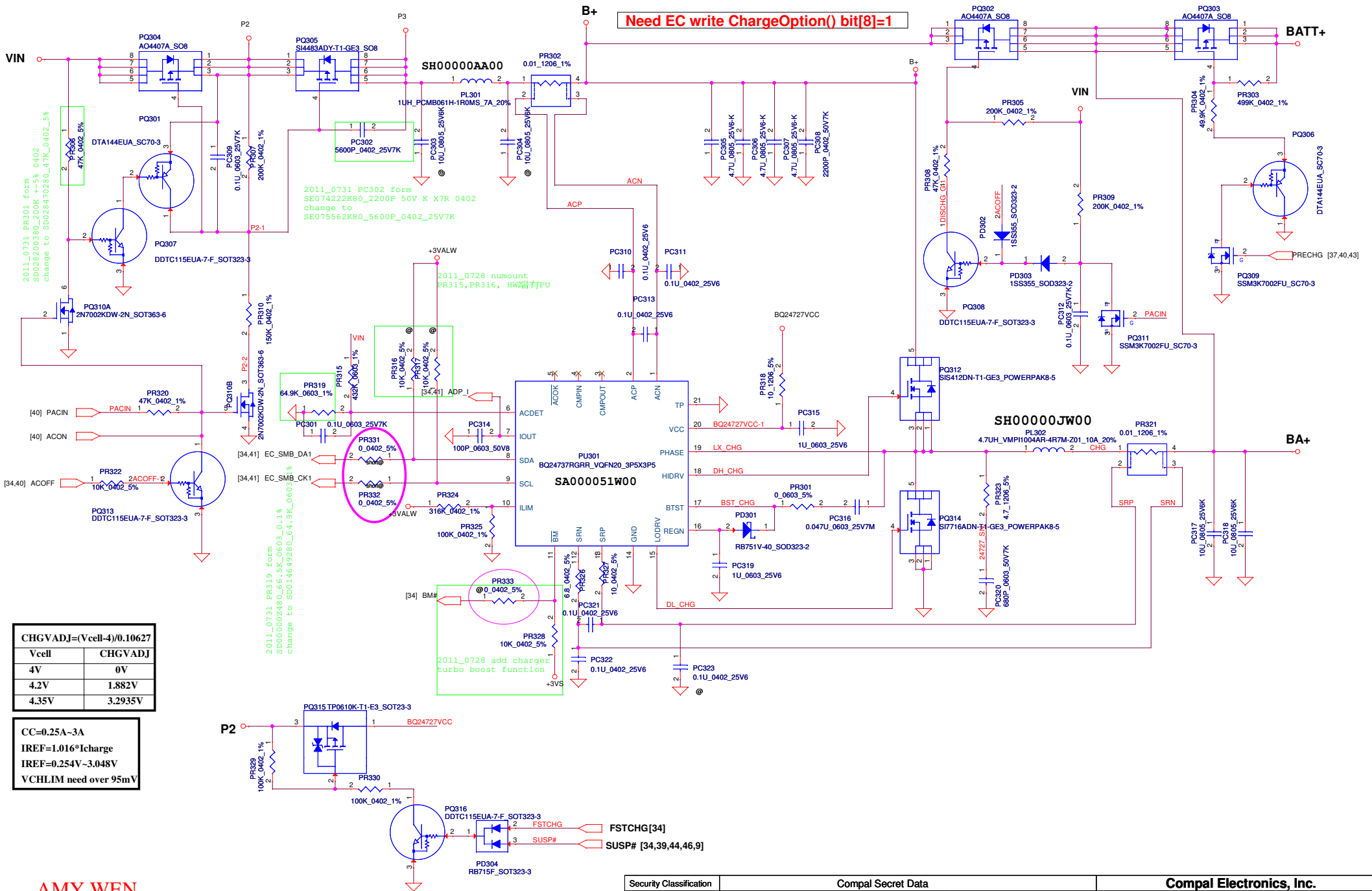
PH1 under CPU bottom side :
CPU thermal protection at 93 +3 degree C
Recovery at 56 +3 degree C

For KB930 --> Keep PU201 circuit
(Vth = 1.25V)
For KB9012 (Red square) --> Remove PU201 circuit, but keep PR206
PH201, PR205, PR211, PQ201, PR208, PR212



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				Rev 1.0



CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

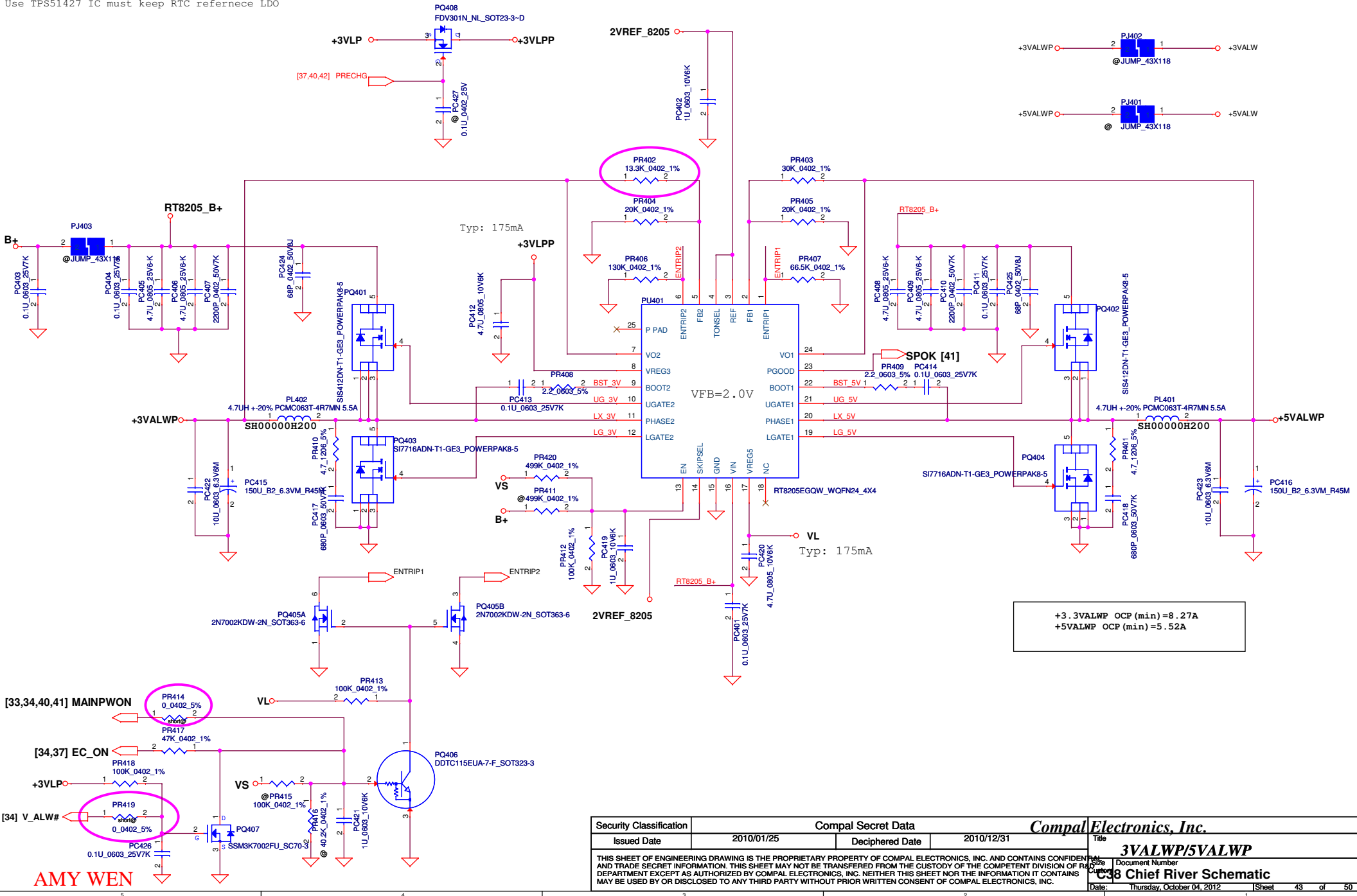
CC=0.25A-3A	
IREF=1.016*Icharge	
IREF=0.254V-3.048V	
VCHLIM need over 95mV	

Need EC write ChargeOption() bit[8]=1

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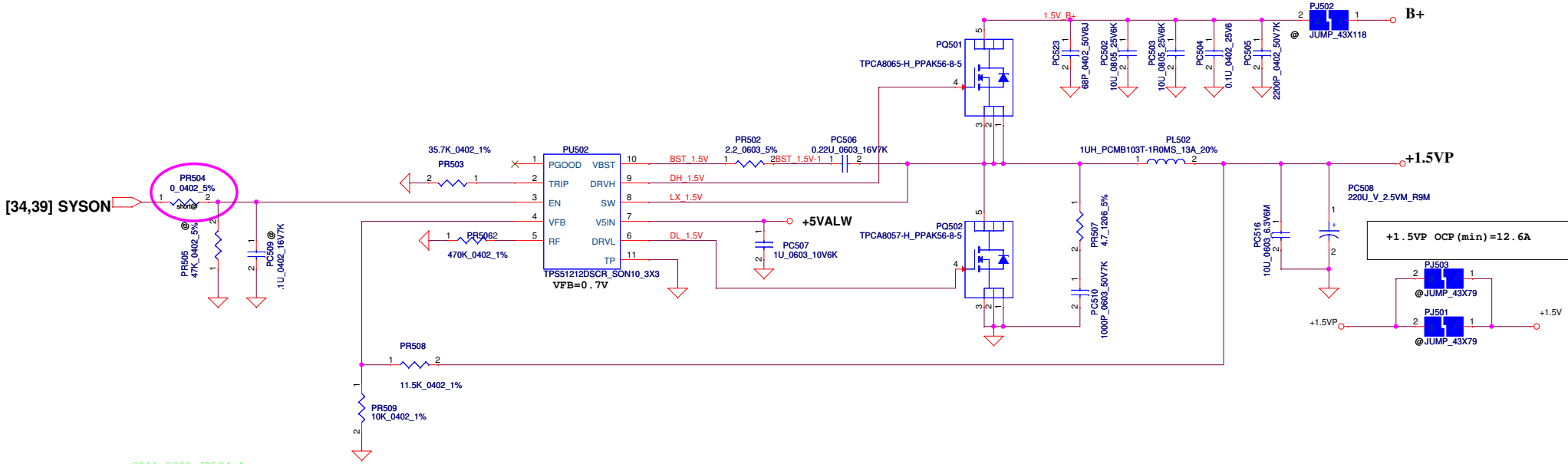
CHARGER
C29 Chief River Schematic

Note:
 Use TPS51125 IC can remove RTC refernece LDO
 Use TPS51427 IC must keep RTC refernece LDO



Security Classification	Compal Secret Data		Compal Electronics, Inc. Title: 3VALWP/5VALWP Document Number: C38 Chief River Schematic Date: Thursday, October 04, 2012 Sheet 43 of 50
Issued Date	2010/01/25	Deciphered Date	
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Rev	1.0		

[34,39] SYSON

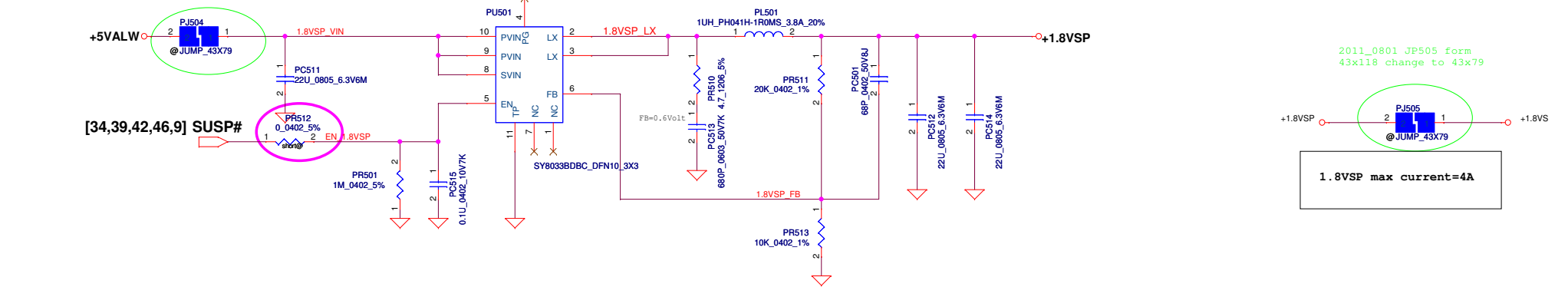


+1.5VP OCP (min)=12.6A

2011_0801 JP504 form
43x118 change to 43x79

+5VALW

[34,39,42,46,9] SUSP#



2011_0801 JP505 form
43x118 change to 43x79

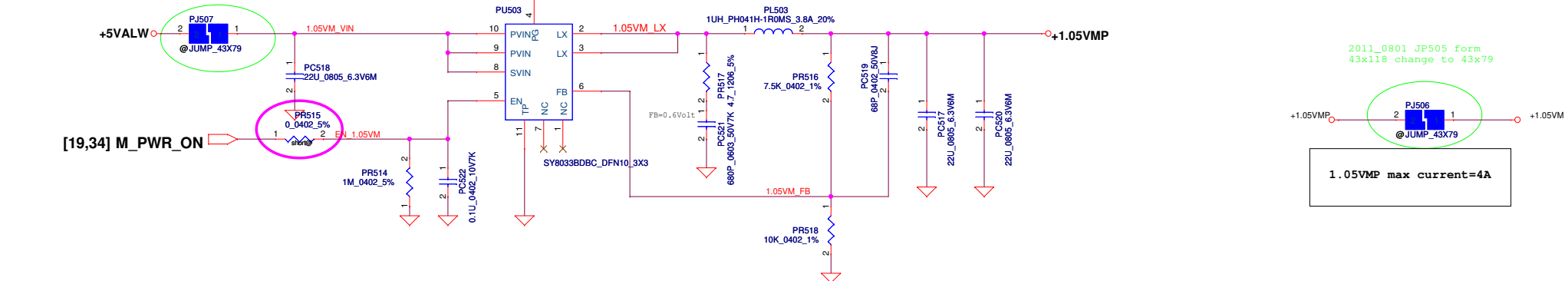
+1.8VSP

1.8VSP max current=4A

2011_0801 JP504 form
43x118 change to 43x79

+5VALW

[19,34] M_PWR_ON



2011_0801 JP505 form
43x118 change to 43x79

+1.05VMP

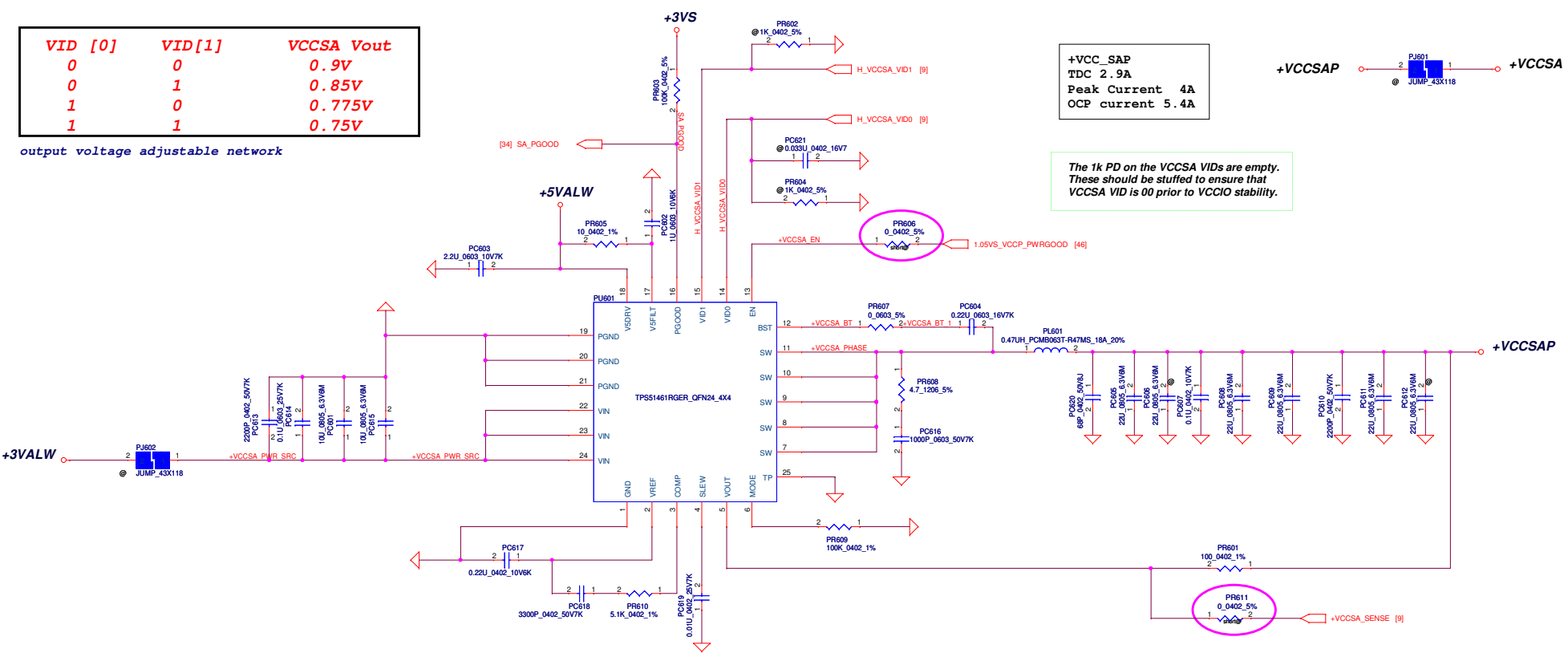
1.05VMP max current=4A

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Issued Date	2010/01/25	Deciphered Date	2010/12/31	Title	PWR-+1.5VP/+1.8VSP
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VID [0]	VID [1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

output voltage adjustable network



+VCC_SAP
TDC 2.9A
Peak Current 4A
OCP current 5.4A

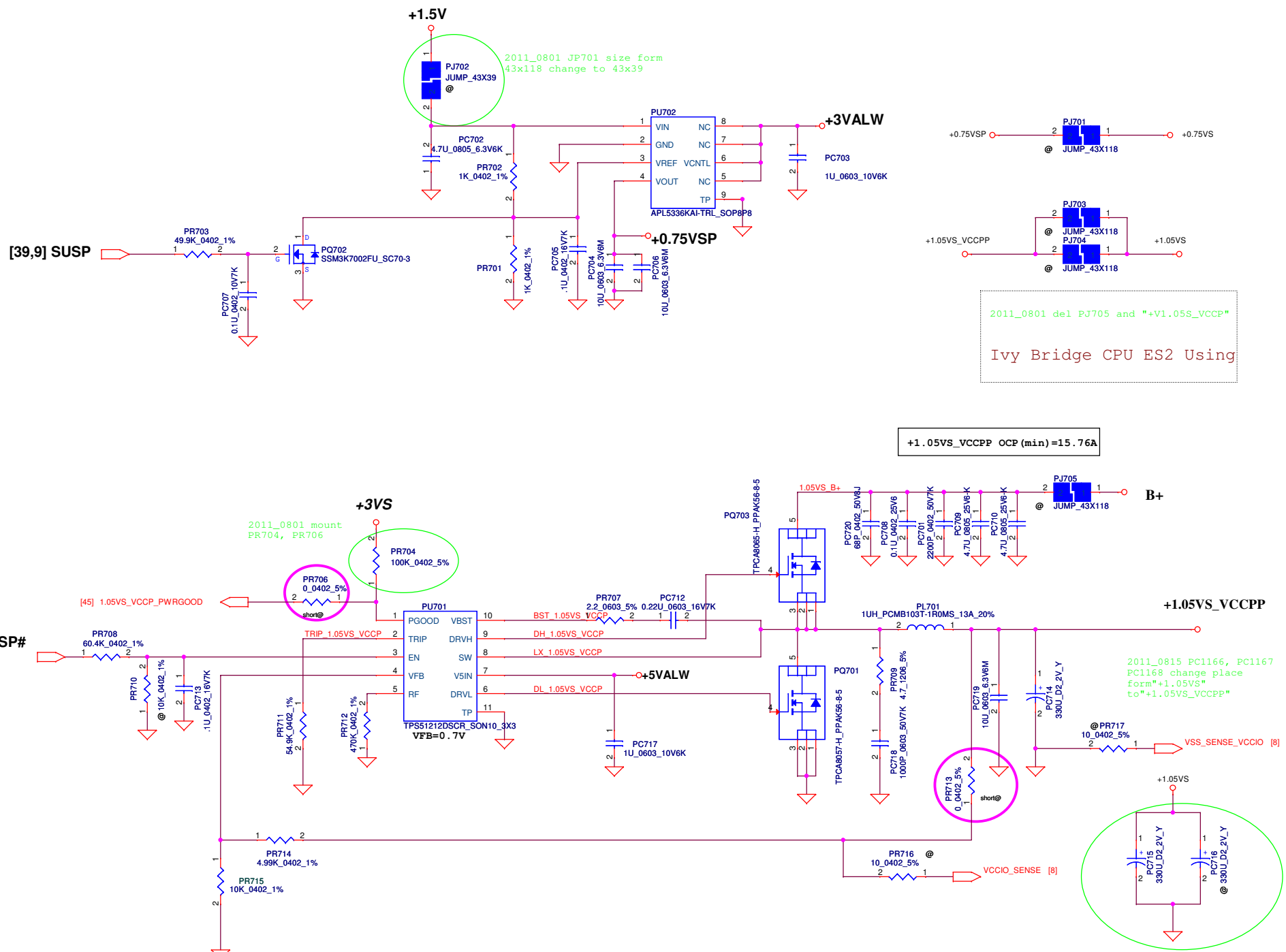
+VCCSAP +VCCSA

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



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				C38 Chief River Schematic
				Rev 1.0
				Date: Thursday, October 04, 2012 Sheet 45 of 50

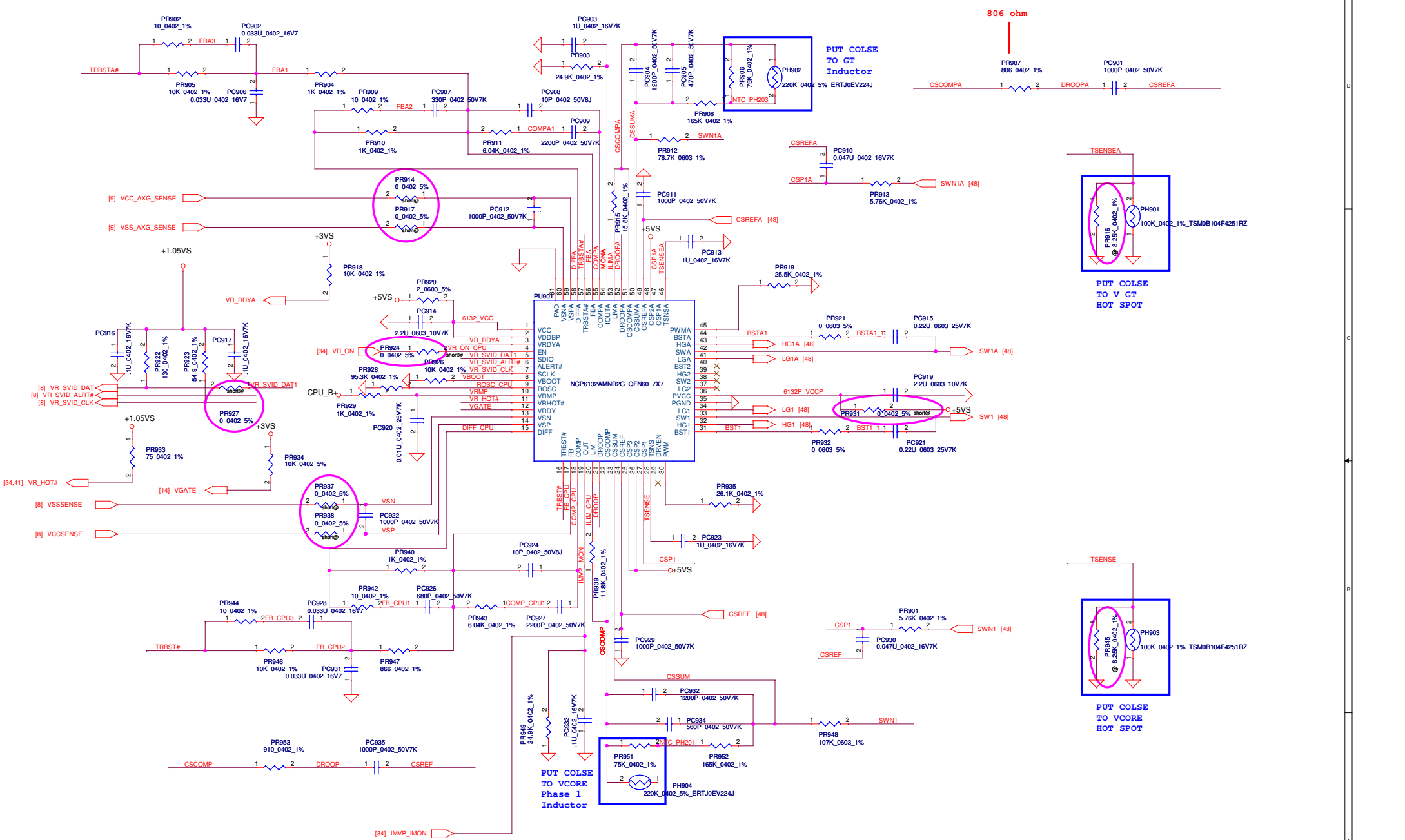


2011_0801 del PJ705 and "+V1.05S_VCCPP"
 Ivy Bridge CPU ES2 Using

+1.05VS_VCCPP OCP (min) = 15.76A

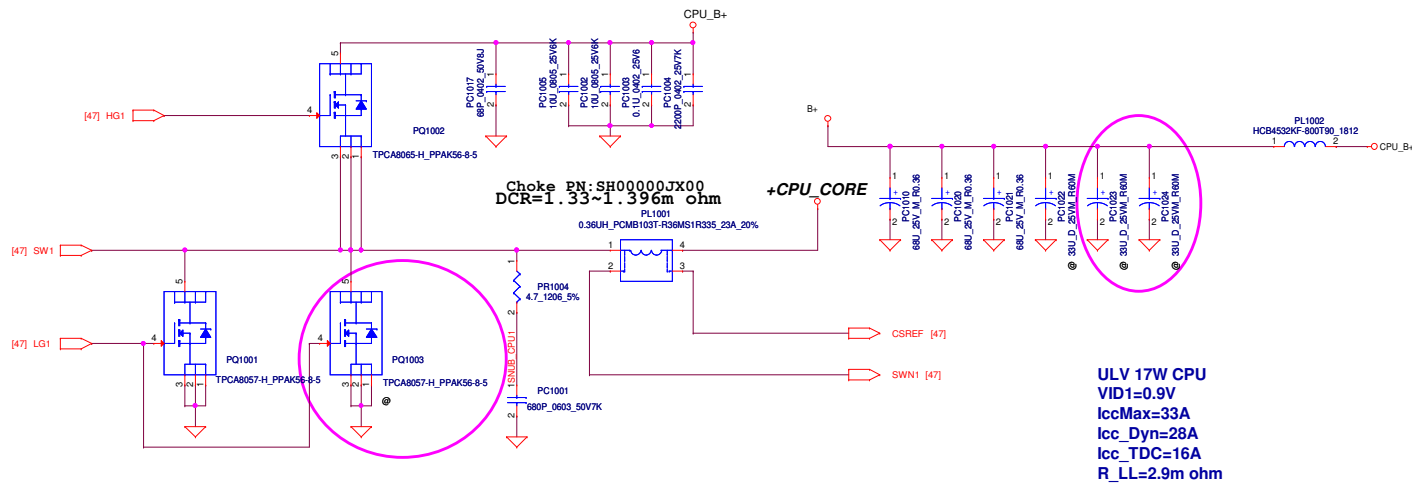
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Issued Date	2010/01/25	Deciphered Date	2010/12/31	Title	PWR +1.05VS_VCCPP/+0.75VSP
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Date:	Thursday, October 04, 2012	Sheet	46	of	50

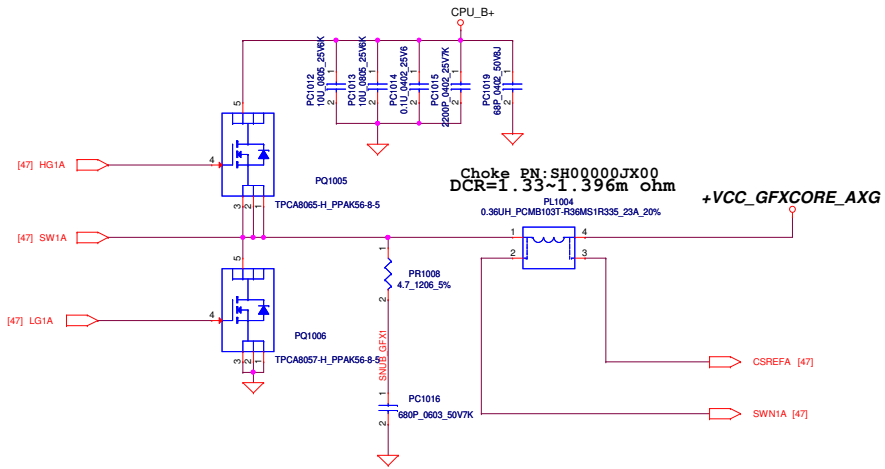


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				Rev 1.0
Date: Thursday, October 04, 2012				Sheet 47 of 50



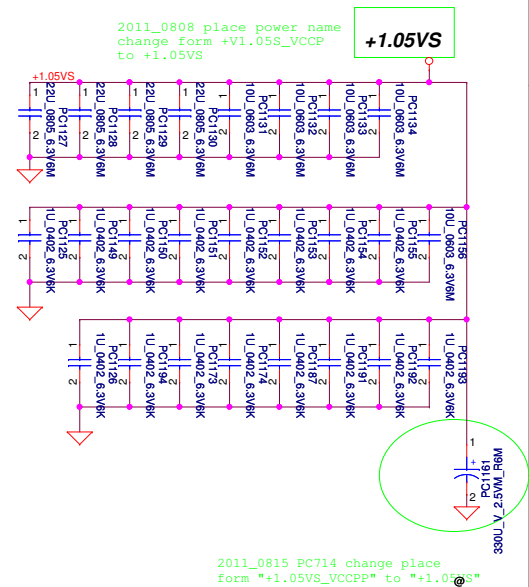
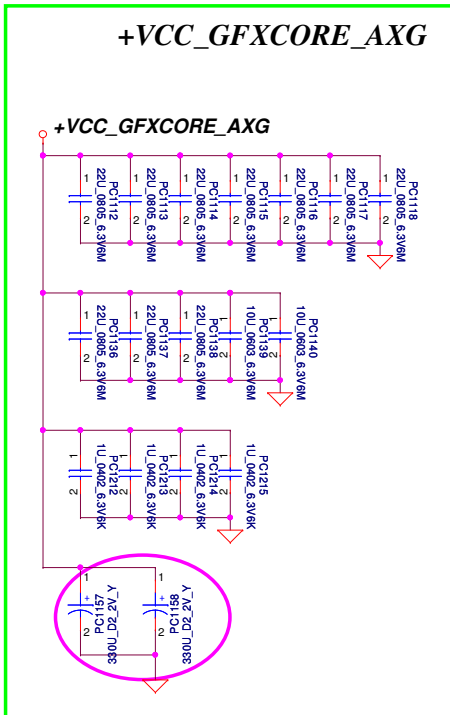
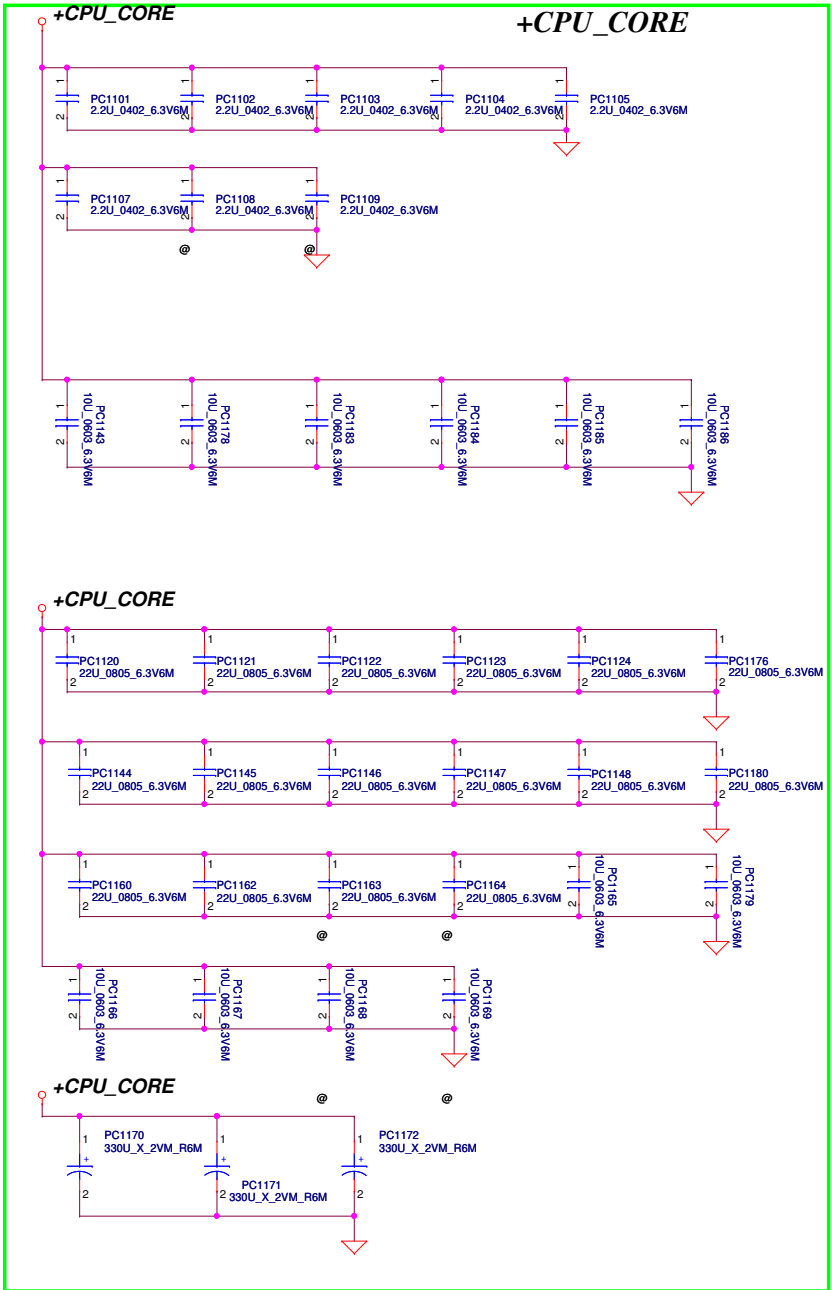
ULV 17W CPU
 VID1=0.9V
 IccMax=33A
 Icc_Dyn=28A
 Icc_TDC=16A
 R_LL=2.9m ohm



ULV GT2
 VID1=1.23V
 IccMax=33A
 Icc_Dyn=20.2A
 Icc_TDC=21.5A
 R_LL=3.9m ohm

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Date:	Thursday, October 04, 2012	Sheet	48	of 50



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Date:	Thursday, October 04, 2012	Sheet	49	of 50

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	NCP6132A update SPEC	P47	Remove PR916, PR945	2012/06/05	
2	Thermal verify PH1 setting point	P41	Change PR208 value to 18.2K	2012/06/08	
3	ME demand : Keyboard assembly issue	P44	Change PL401, PL402 to High=2.4mm (SH00000H200)	2012/06/08	
4	Noise is PASS, Don't need 33u CAP	P48	Remove PC1023, PC1024	2012/06/08	
5					
6					
7					
8					
9					
10					
11					
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13					
14					
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16					
17					

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				Custom	1.0
				Date:	Thursday, October 04, 2012
				Sheet	50 of 50