

# COMPAL CONFIDENTIAL

MODEL NAME : *PAL51/53*

PCB NO : *LA-6592P (DAA00001V10)*

BOM P/N : *43192931L01*

GPIO MAP: E3 Master GPIO Map10102010.xlsx

## E3 MACALLAN 14" SG

rPGA Sandy Bridge +  
FCBGA PCH Cougar Point-M

2011-1-13

REV : 1.0(A00)

@ : Nopop Component

CONN@ : ME control and stuff by default

MB Type	BOM P/N		
TPM EN/ TCM DIS	43192931L01	1@	3@
TPM DIS/ TCM EN	43192931L02	2@	4@
TPM DIS/ TCM DIS	43192931L03	2@	3@
ATG TPM EN/ TCM DIS	43192931L11	1@	3@
ATG TPM DIS/ TCM EN	43192931L12	2@	4@
ATG TPM DIS/ TCM DIS	43192931L13	2@	3@

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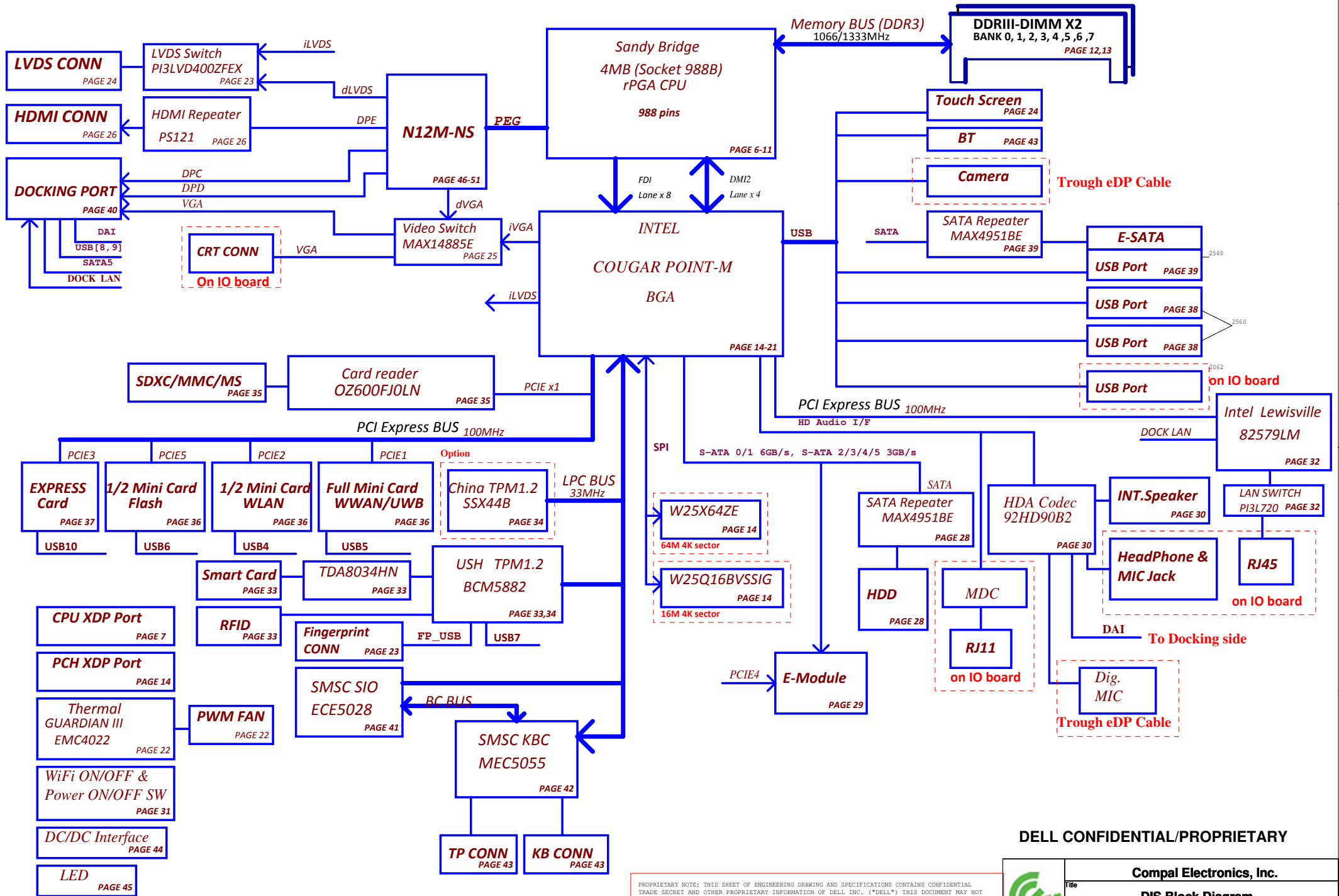
Title			
Cover Sheet			
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Part Number	Description
DAA00001V10	PCB OFE LA-6592P REV0 M/8 DIS

Block Diagram *Compal confidential* Model: PAL51/53



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<b>DIS Block Diagram</b>			
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# POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

# PM TABLE

State \ power plane	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

SATA	DESTINATION
SATA 0	HDD
SATA 1	ODD/ E3 Module Bay
SATA 2	NA
SATA 3	NA
SATA 4	ESATA
SATA 5	Dock

need to update Power Status and PM Table

PCH	USB PORT#	DESTINATION
	0	JUSB2 (Right side 1)
	1	JUSB3 (Right side 2)
	2	JESA1 (Right Side ESATA)
	3	JESA1 (Ext Left Side )
	4	WLAN
	5	WWAN
	6	JMINI3(Flash)
	7	USH->BIO
	8	DOCKING
	9	DOCKING
	10	Express card
	11	Bluetooth
	12	Camera
13	LCD Touch	

USH	0	BIO
	1	NA

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Express card
Lane 4	E3 Module Bay (USB3)
Lane 5	1/2vMINI CARD-3 PCIE
Lane 6	MMI
Lane 7	10/100/1G LOM
Lane 8	None

DSC DP/HDMI Port	Connetion
Port C	Dock DP port 2
Port D	Dock DP port 1
Port E	MB HDMI Conn

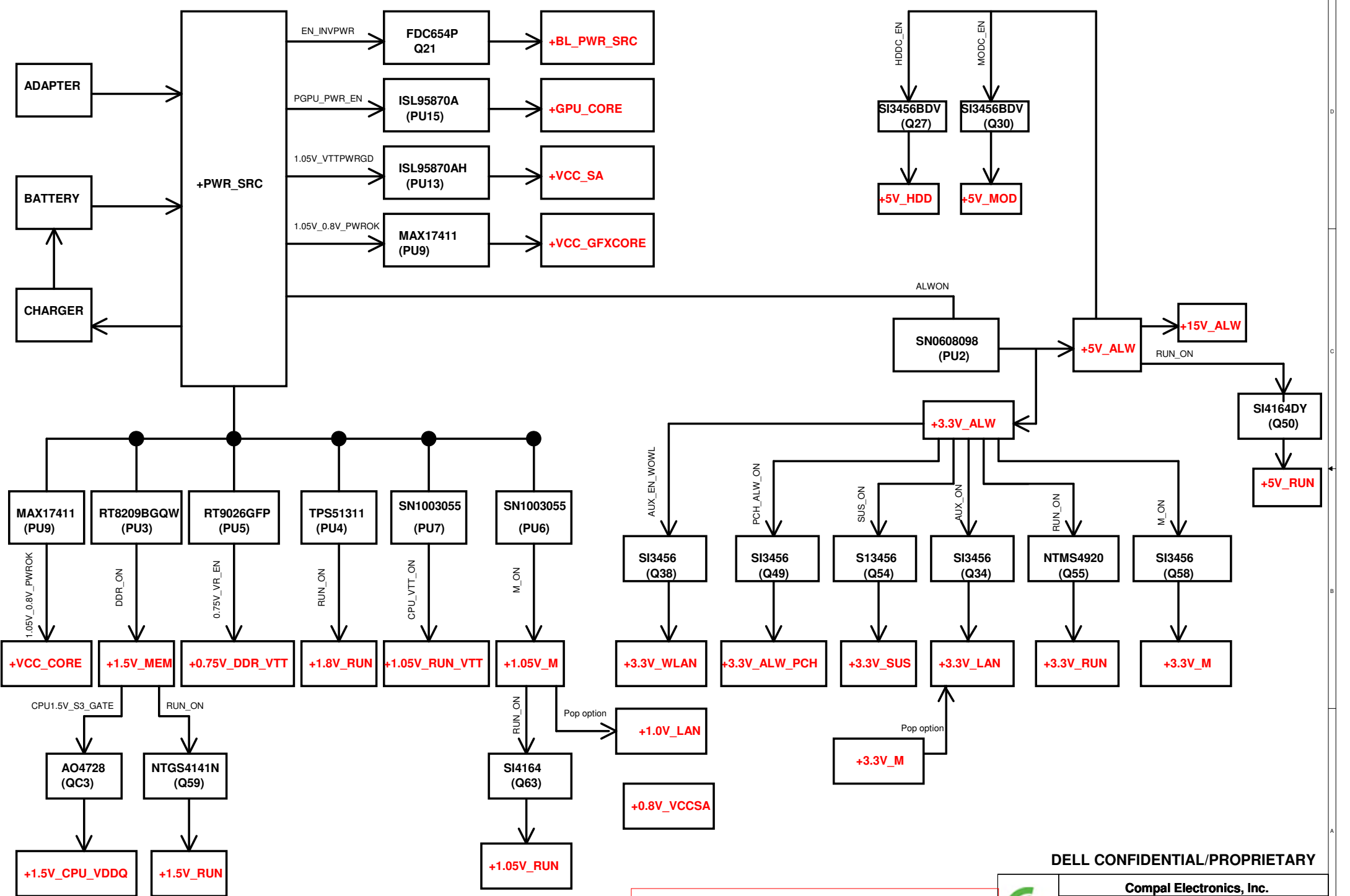
Layer No.	Name	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
		SolderMask	min 0.4	0.50000
		Add Plating		1.45000
1	Top	Copper foil	0.5oz(0.68)	0.65000
		Prepreg	1080	2.75000
2	GND1	Copper foil	1oz(1.35)	1.35000
		Core	4mil	3.89000
3	IN 1	Copper foil	1oz(1.35)	1.35000
		Prepreg	1506	5.50000
4	GND2	Copper foil	1oz(1.35)	1.35000
		Core	3mil	3.09000
5	IN 2	Copper foil	1oz(1.35)	1.35000
		Prepreg	1506*2	11.50000
6	IN 3	Copper foil	1oz(1.35)	1.35000
		Core	3mil	3.09000
7	VCC	Copper foil	1oz(1.35)	1.35000
		Prepreg	1506	5.50000
8	IN 4	Copper foil	1oz(1.35)	1.35000
		Core	4mil	3.89000
9	GND 3	Copper foil	1oz(1.35)	1.30000
		Prepreg	1080	2.75000
10	Bottom	Copper foil	0.5oz(0.68)	0.65000
		Add Plating		1.45000
		SolderMask	min 0.4	0.50000
	Overall Thickness (1.45mm ± 10%)			57.91000

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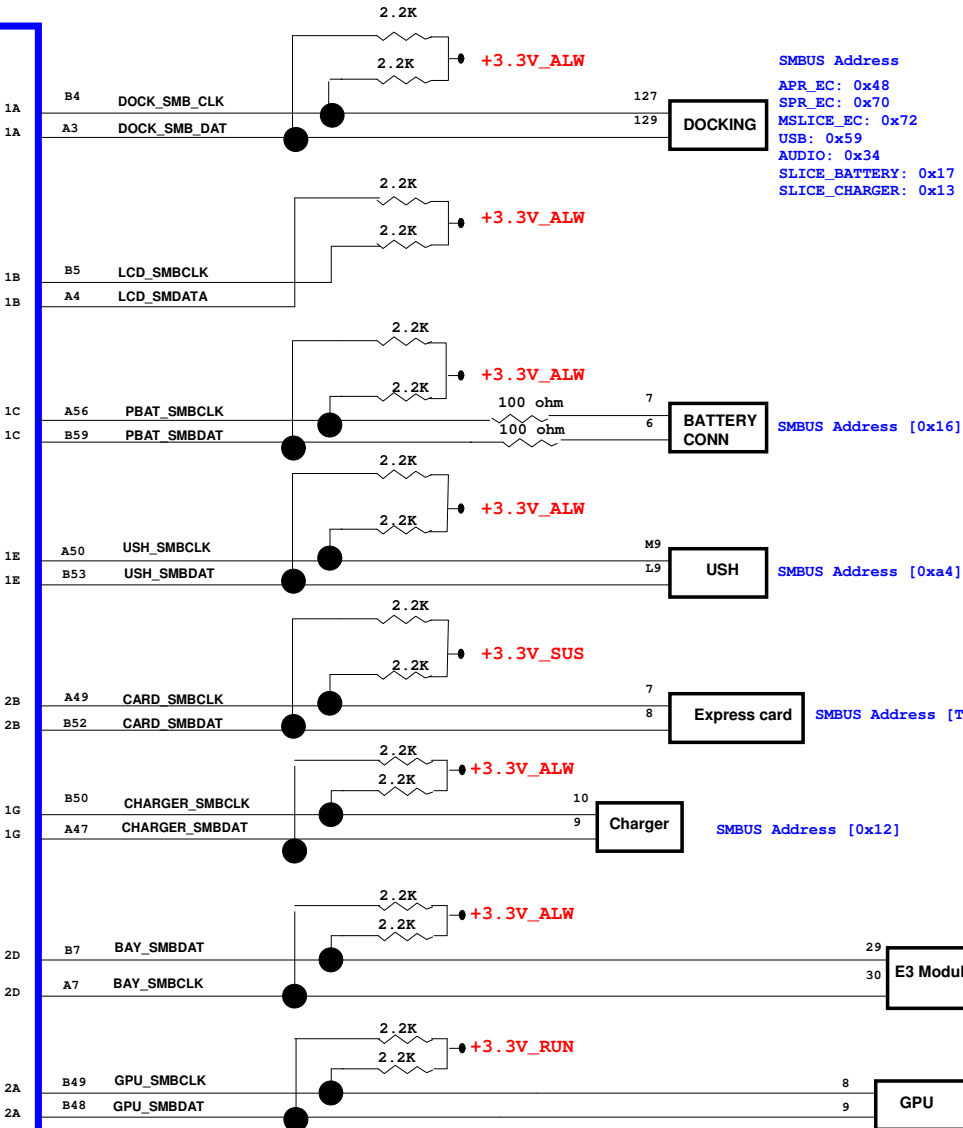
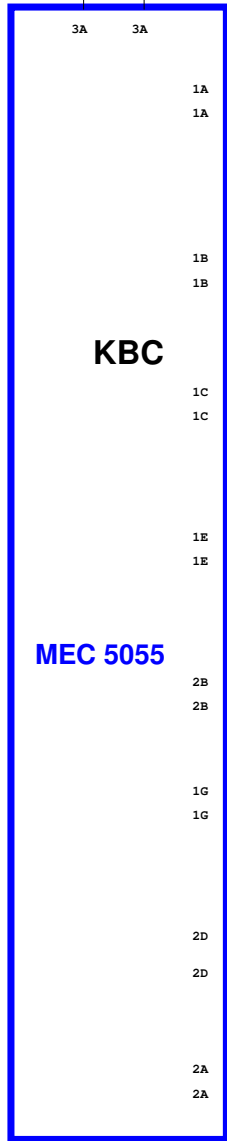
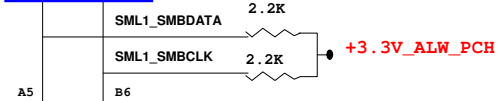
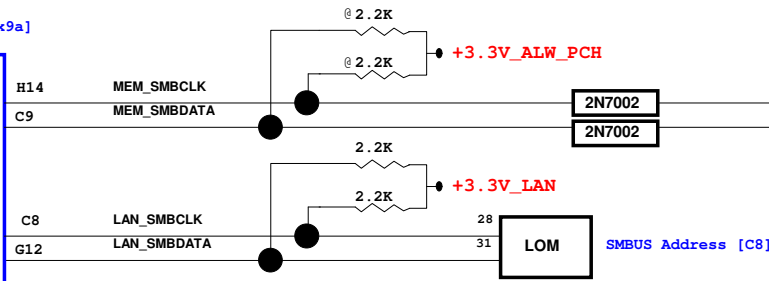
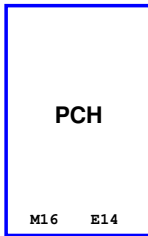


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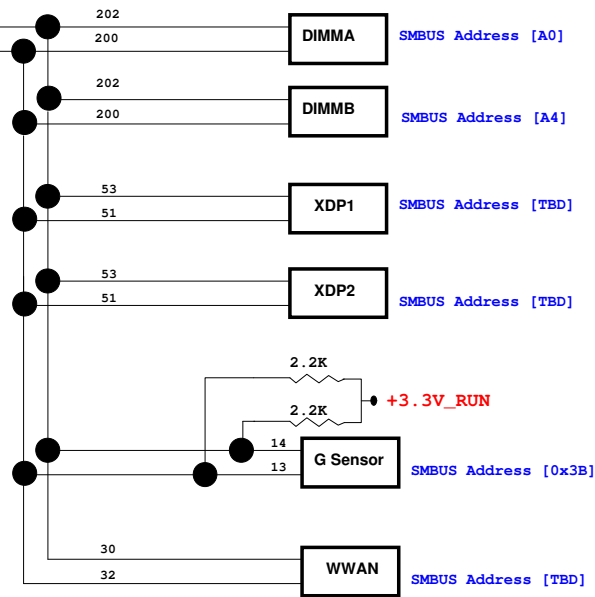
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<b>Compal Electronics, Inc.</b>			
<b>Power Rail</b>			
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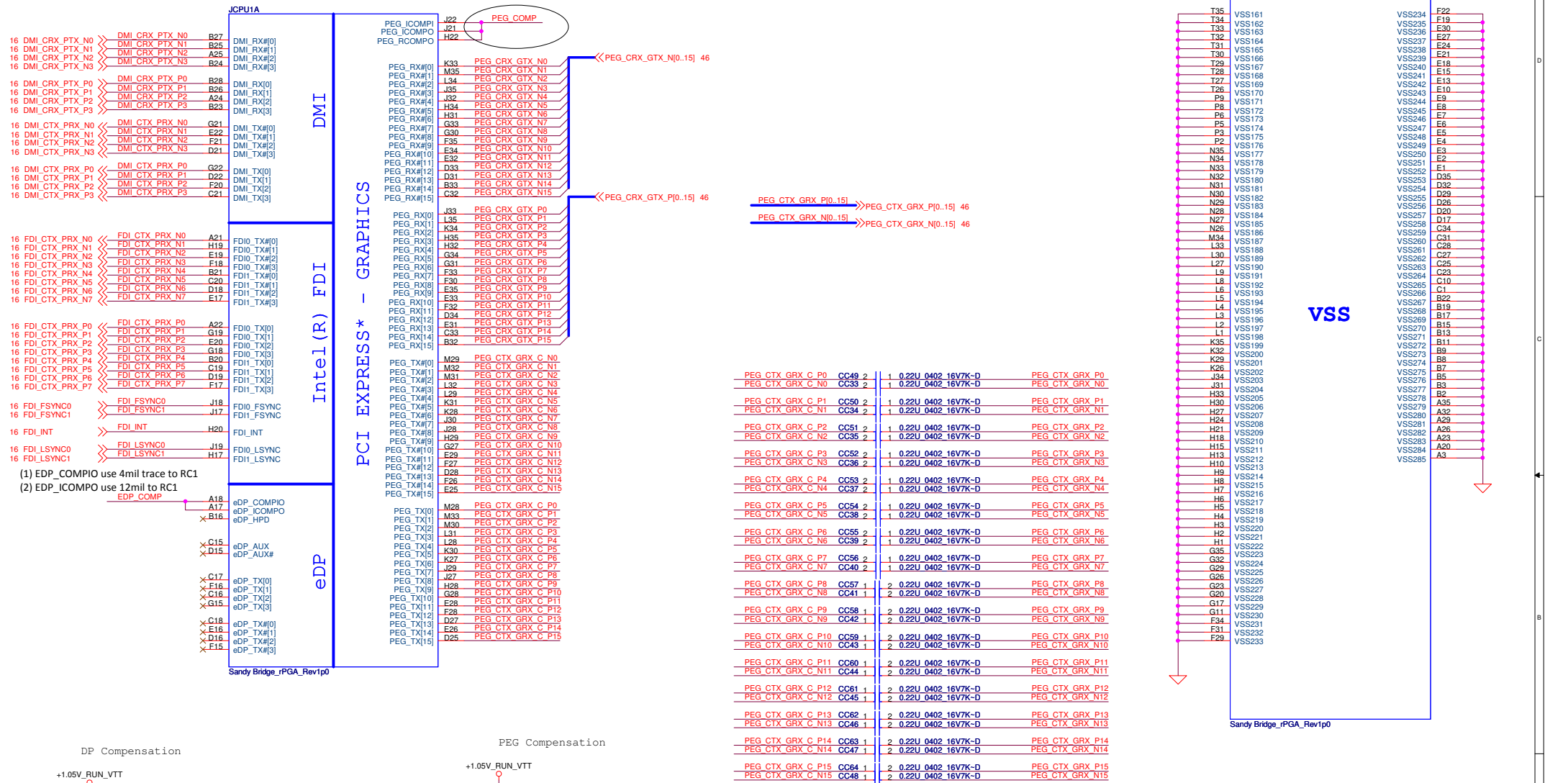
SMBUS Address [0x9a]



SMBUS Address  
APR\_EC: 0x48  
SPR\_EC: 0x70  
MSLICE\_EC: 0x72  
USB: 0x59  
AUDIO: 0x34  
SLICE\_BATTERY: 0x17  
SLICE\_CHARGER: 0x13



(1) PEG\_RCOPMO (H22) use 4mil connect to PEG\_ICOMPI, then use 4mil connect to RC2.  
 (2) PEG\_ICOMPO use 12mil connect to RC2



eDP\_COMP and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG\_ICOMPI and RCOPMO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms  
 PEG\_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

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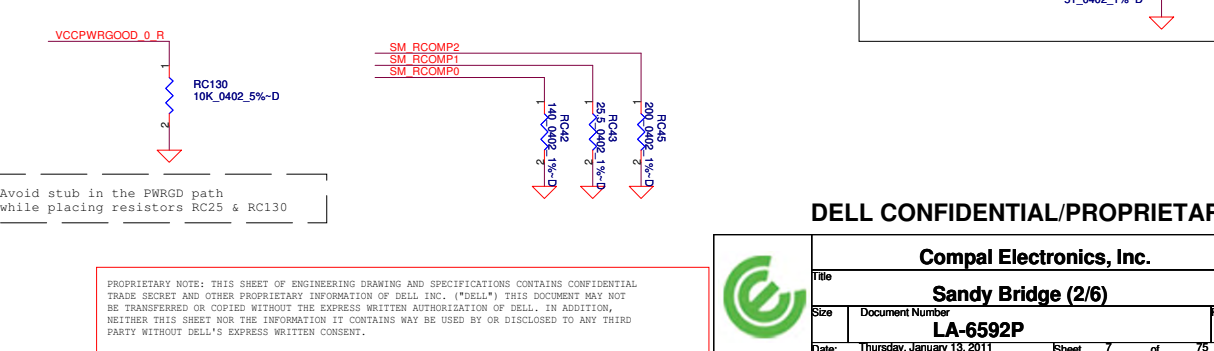
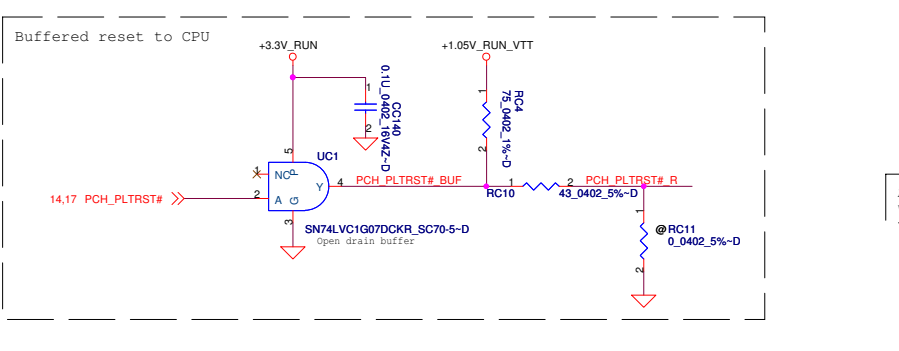
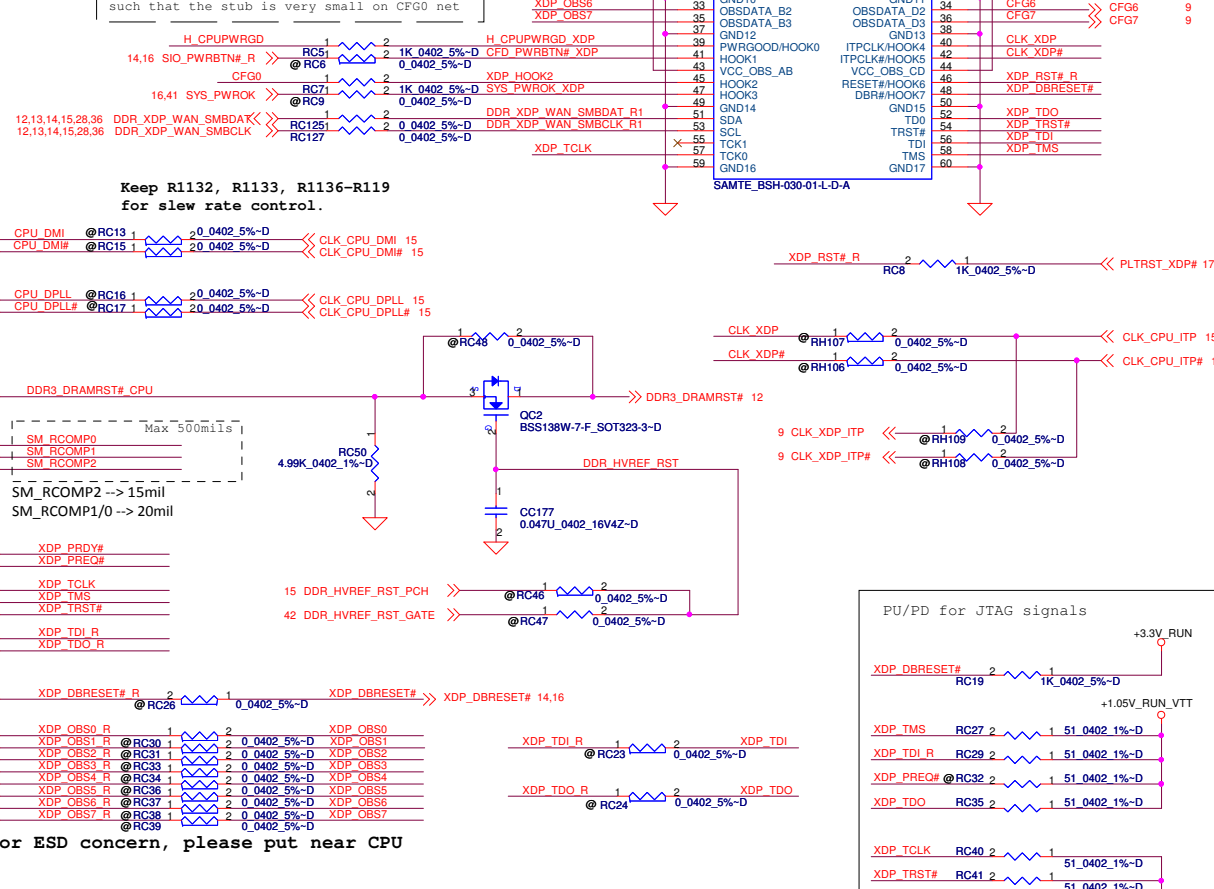
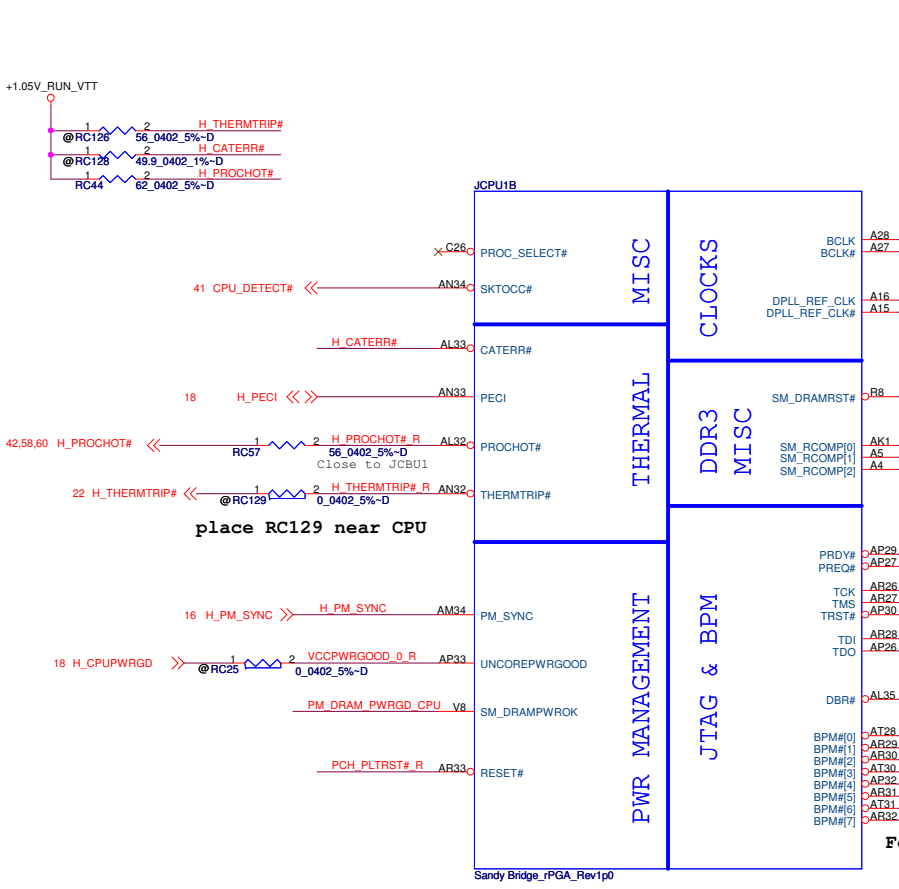
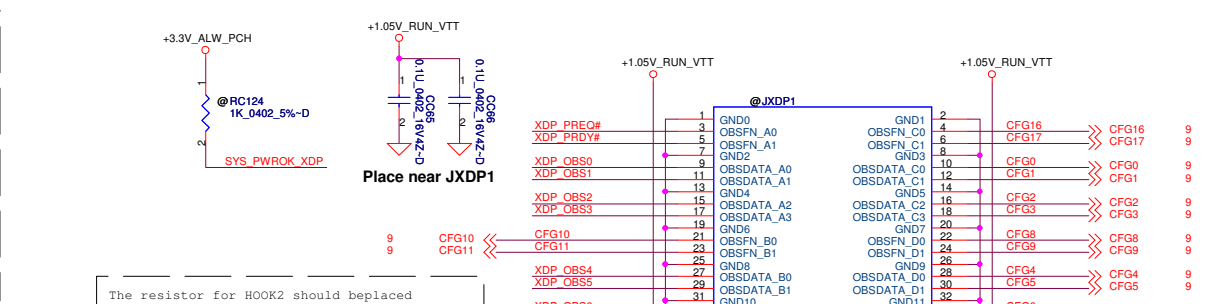
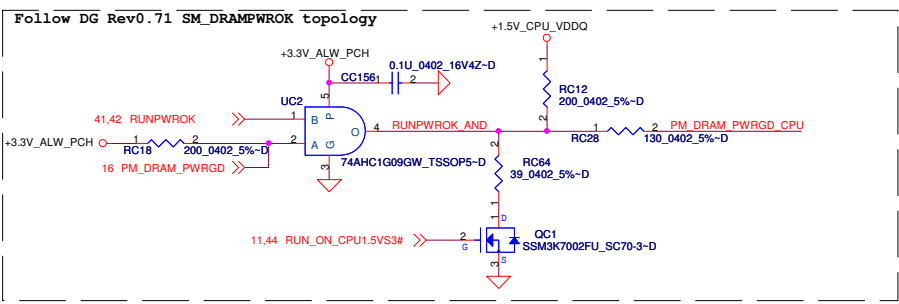
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**Sandy Bridge (1/6)**

**LA-6592P**

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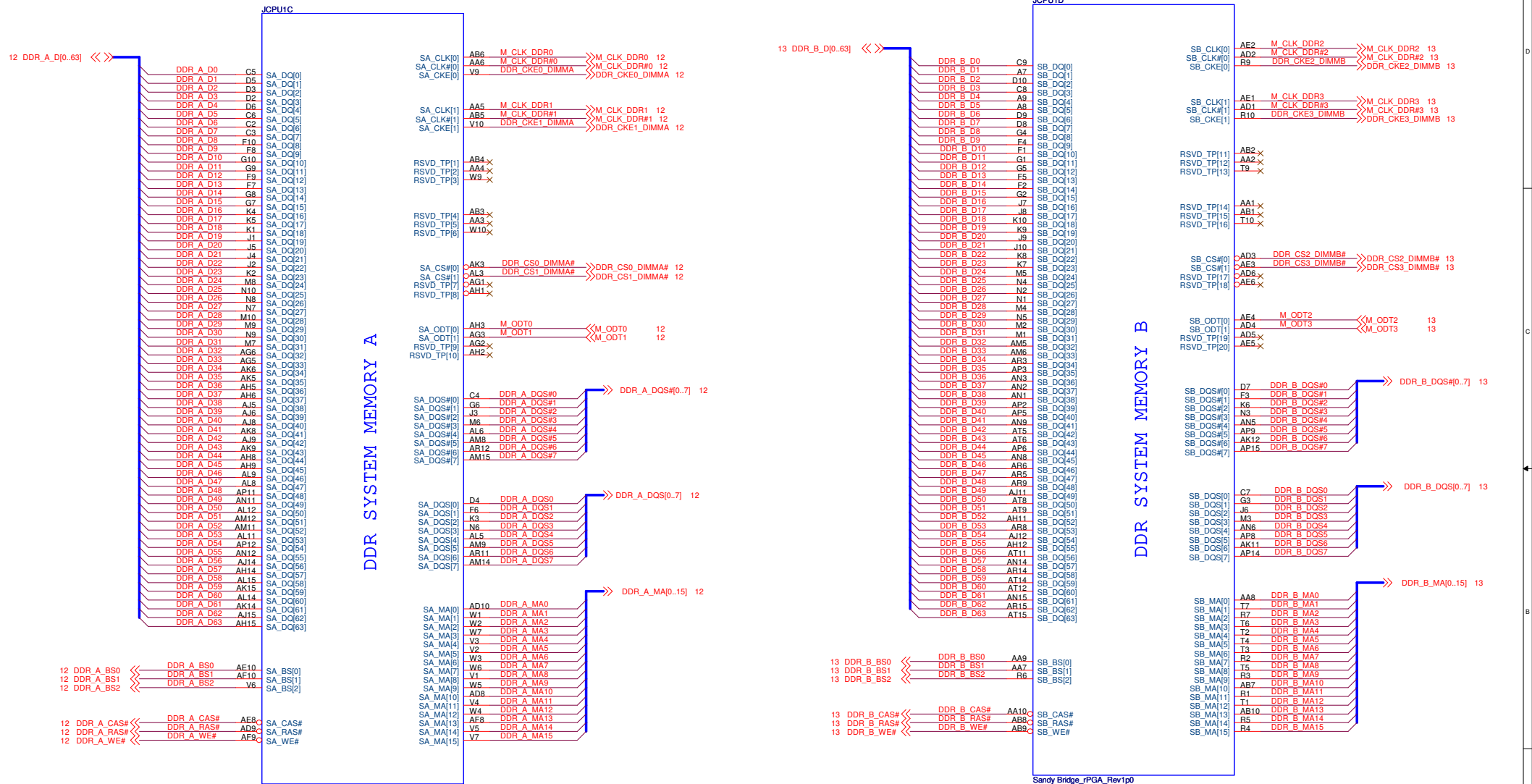
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**Sandy Bridge (2/6)**  
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Sandy Bridge\_rPGA\_Rev1p0

Sandy Bridge\_rPGA\_Rev1p0

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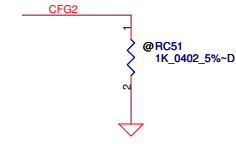
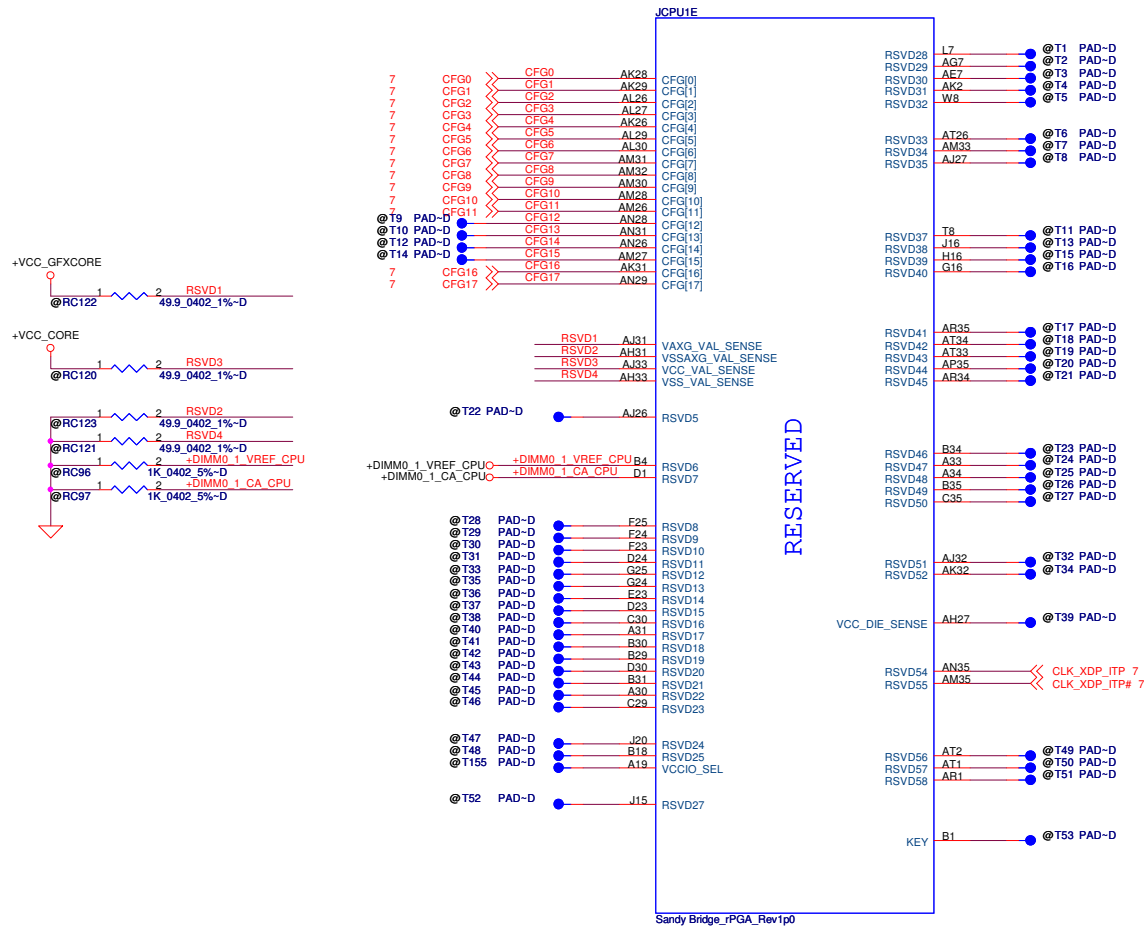


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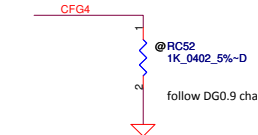
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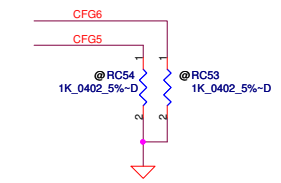
# CFG Straps for Processor



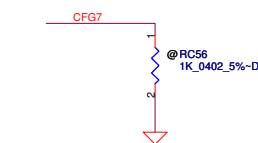
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

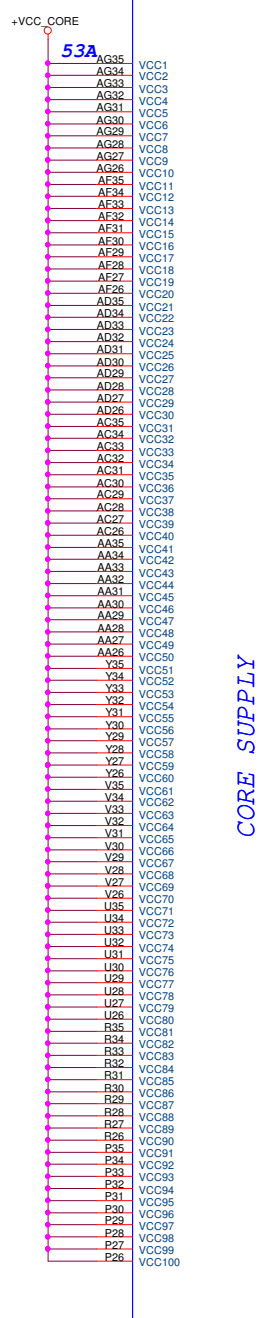
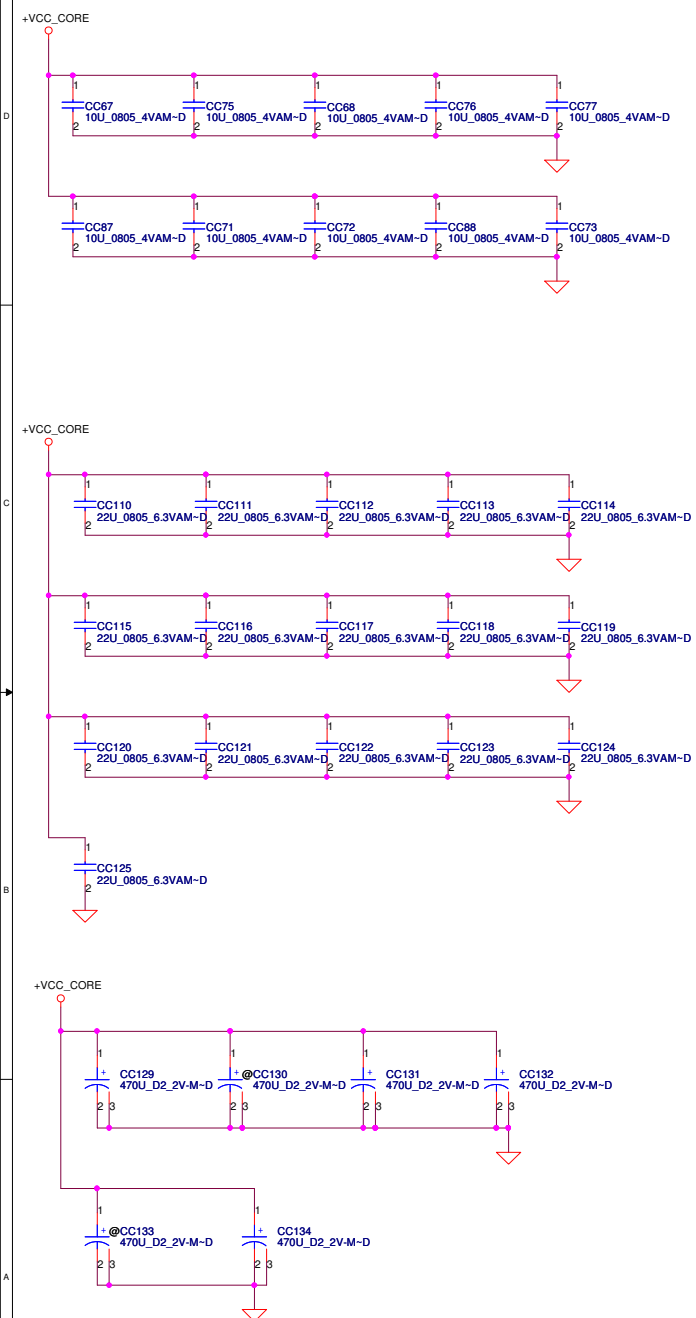
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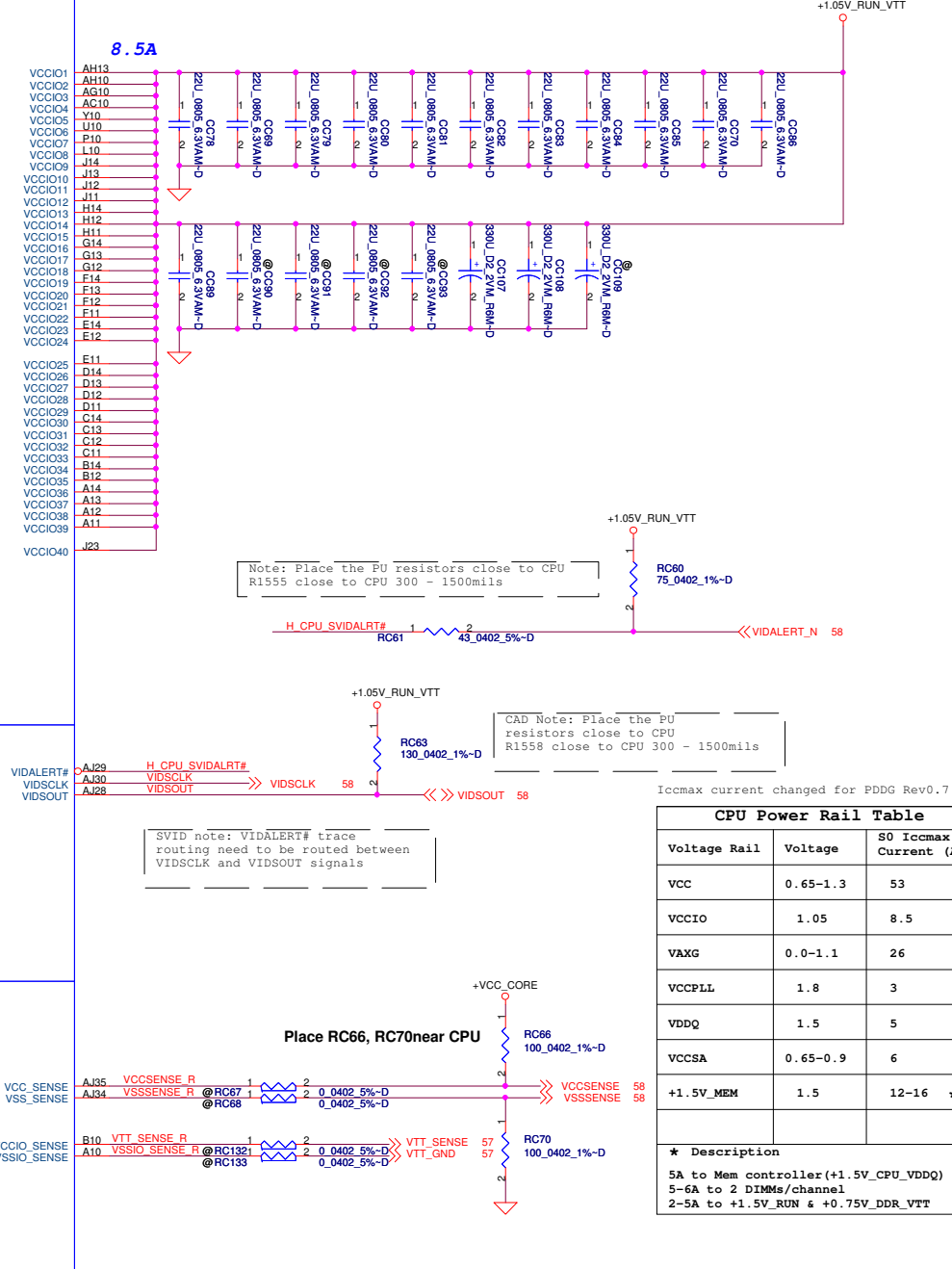
# POWER



PEG AND DDR

CORE SUPPLY

SENSE LINES



Note: Place the PU resistors close to CPU R1555 close to CPU 300 - 1500mils

CAD Note: Place the PU resistors close to CPU R1558 close to CPU 300 - 1500mils

SVID note: VIDALERT# trace routing need to be routed between VIDSCLK and VIDSOUT signals

Place RC66, RC70 near CPU

Iccmax current changed for PDDG Rev0.7

CPU Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	0.65-1.3	53
VCCIO	1.05	8.5
VAXG	0.0-1.1	26
VCCPLL	1.8	3
VDDQ	1.5	5
VCCSA	0.65-0.9	6
+1.5V_MEM	1.5	12-16 *

\* Description  
 5A to Mem controller(+1.5V\_CPU\_VDDQ)  
 5-6A to 2 DIMMs/channel  
 2-5A to +1.5V\_RUN & +0.75V\_DDR\_VTT

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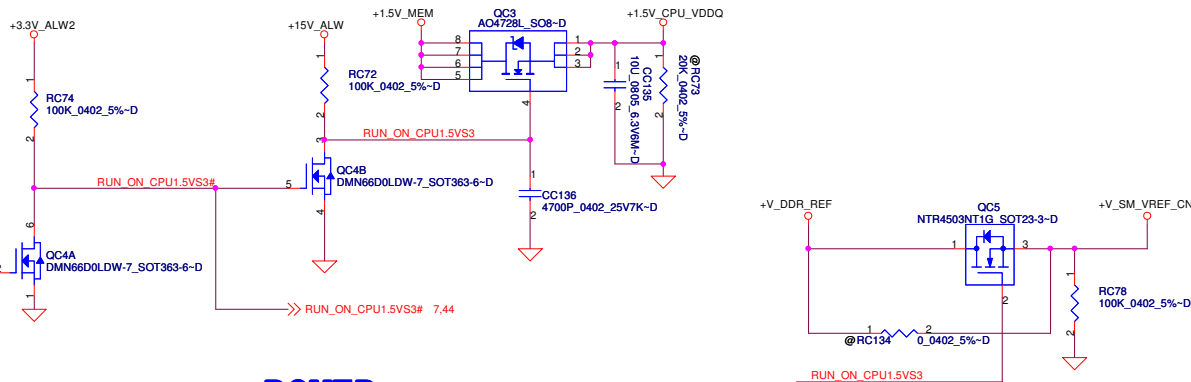
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Sandy Bridge (5/6)

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**+1.5V\_CPU\_VDDQ Source**



JCPU1H		
AT35	VSS1	AJ22
AT32	VSS2	AJ19
VSS3	VSS3	VSS3
AT17	VSS4	VSS4
AT25	VSS5	VSS5
AT22	VSS6	VSS6
AT19	VSS7	VSS7
AT16	VSS8	AJ3
AT13	VSS9	AJ2
AT10	VSS10	AJ1
AT7	VSS11	AH35
AT4	VSS12	VSS12
AT3	VSS13	VSS13
AR25	VSS14	VSS14
AR22	VSS15	VSS15
AR19	VSS16	AH28
AR16	VSS17	AH26
AR13	VSS18	AH25
AR10	VSS19	AH22
AR7	VSS20	VSS20
AR4	VSS21	VSS21
AR2	VSS22	VSS22
AP34	VSS23	VSS23
AP31	VSS24	VSS24
AP28	VSS25	VSS25
AP25	VSS26	VSS26
AP22	VSS27	VSS27
AP19	VSS28	VSS28
AP16	VSS29	AH22
AP13	VSS30	VSS30
AP10	VSS31	VSS31
AP7	VSS32	VSS32
AP4	VSS33	VSS33
AN30	VSS34	VSS34
AN27	VSS35	VSS35
AN25	VSS36	VSS36
AN22	VSS37	VSS37
AN19	VSS38	VSS38
AN16	VSS39	VSS39
AN13	VSS40	VSS40
AN10	VSS41	VSS41
AN7	VSS42	VSS42
AN4	VSS43	VSS43
AM29	VSS44	VSS44
AM25	VSS45	VSS45
AM22	VSS46	VSS46
AM19	VSS47	VSS47
AM16	VSS48	VSS48
AM13	VSS49	VSS49
AM10	VSS50	VSS50
AM7	VSS51	VSS51
AM4	VSS52	VSS52
AM1	VSS53	VSS53
AL34	VSS54	VSS54
AL31	VSS55	VSS55
AL28	VSS56	VSS56
AL25	VSS57	VSS57
AL22	VSS58	VSS58
AL19	VSS59	VSS59
AL16	VSS60	VSS60
AL13	VSS61	VSS61
AL10	VSS62	VSS62
AL7	VSS63	VSS63
AL4	VSS64	VSS64
AL2	VSS65	VSS65
AK33	VSS66	VSS66
AK30	VSS67	VSS67
AK27	VSS68	VSS68
AK25	VSS69	VSS69
AK22	VSS70	VSS70
AK19	VSS71	VSS71
AK16	VSS72	VSS72
AK13	VSS73	VSS73
AK10	VSS74	VSS74
AK7	VSS75	VSS75
AK4	VSS76	VSS76
AJ25	VSS77	VSS77
	VSS78	VSS78
	VSS79	VSS79
	VSS80	VSS80
	VSS81	VSS81
	VSS82	VSS82
	VSS83	VSS83
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	VSS164	VSS164
	VSS165	VSS165
	VSS166	VSS166
	VSS167	VSS167
	VSS168	VSS168
	VSS169	VSS169
	VSS170	VSS170
	VSS171	VSS171
	VSS172	VSS172
	VSS173	VSS173
	VSS174	VSS174
	VSS175	VSS175
	VSS176	VSS176
	VSS177	VSS177
	VSS178	VSS178
	VSS179	VSS179
	VSS180	VSS180

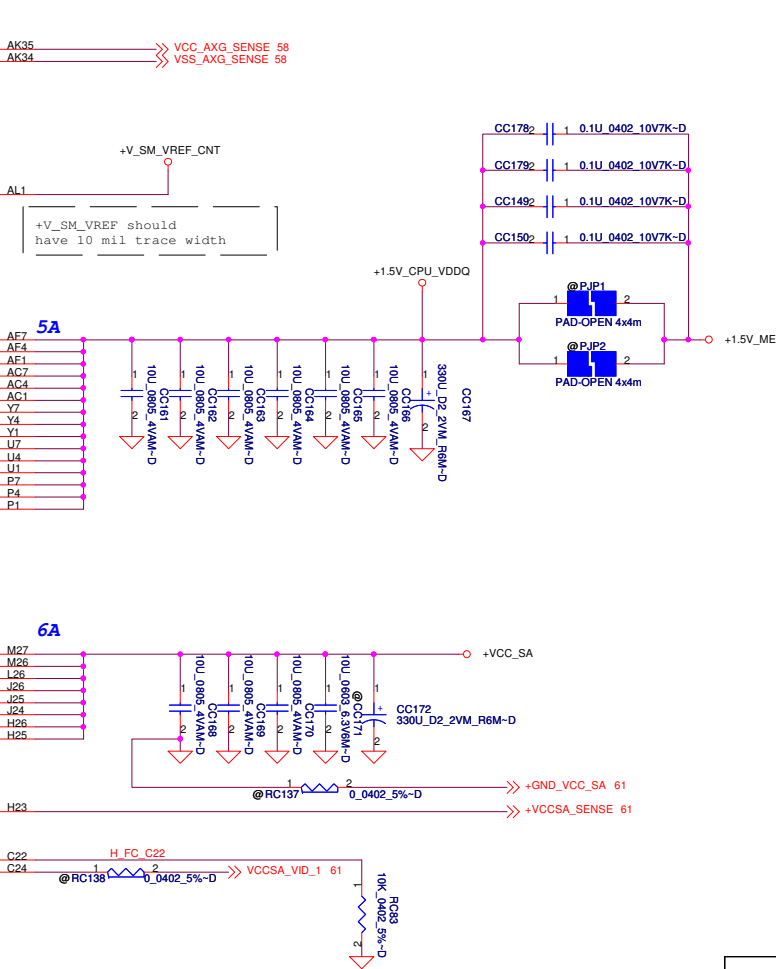
**POWER**

**GRAPHICS**

**SA RAIL**

**MISC**

JCPU1G	JCPU1H
AT24	VAXG1
AT23	VAXG2
AT21	VAXG3
AT20	VAXG4
AT18	VAXG5
AT17	VAXG6
AR24	VAXG7
AR23	VAXG8
AR21	VAXG9
AR20	VAXG10
AR17	VAXG11
AP24	VAXG12
AP23	VAXG13
AP21	VAXG14
AP20	VAXG15
AP18	VAXG16
AP17	VAXG17
AN24	VAXG18
AN23	VAXG19
AN21	VAXG20
AN20	VAXG21
AN18	VAXG22
AN17	VAXG23
AM24	VAXG24
AM23	VAXG25
AM21	VAXG26
AM20	VAXG27
AM18	VAXG28
AM17	VAXG29
AL24	VAXG30
AL23	VAXG31
AL21	VAXG32
AL20	VAXG33
AL18	VAXG34
AL17	VAXG35
AK24	VAXG36
AK23	VAXG37
AK21	VAXG38
AK20	VAXG39
AK18	VAXG40
AK17	VAXG41
AJ24	VAXG42
AJ23	VAXG43
AJ20	VAXG44
AJ18	VAXG45
AJ17	VAXG46
AH24	VAXG47
AH23	VAXG48
AH21	VAXG49
AH20	VAXG50
AH18	VAXG51
AH17	VAXG52
	VAXG53
	VAXG54



**VSS**

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**Sandy Bridge (6/6)**

**LA-6592P**

Title	Sandy Bridge (6/6)		
Size	Document Number	Rev	1.0
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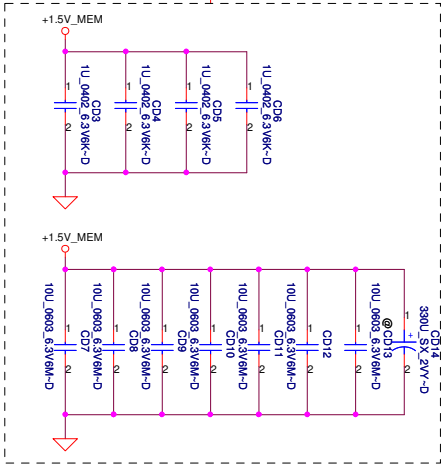
Note:  
Check voltage tolerance of  
VREF\_DQ at the DIMM socket

- 8 DDR\_A\_DQS#0[0.7] <<>
- 8 DDR\_A\_D[0.63] <<>
- 8 DDR\_A\_DQS#0[0.7] <<>
- 8 DDR\_A\_MA[0.15] <<>

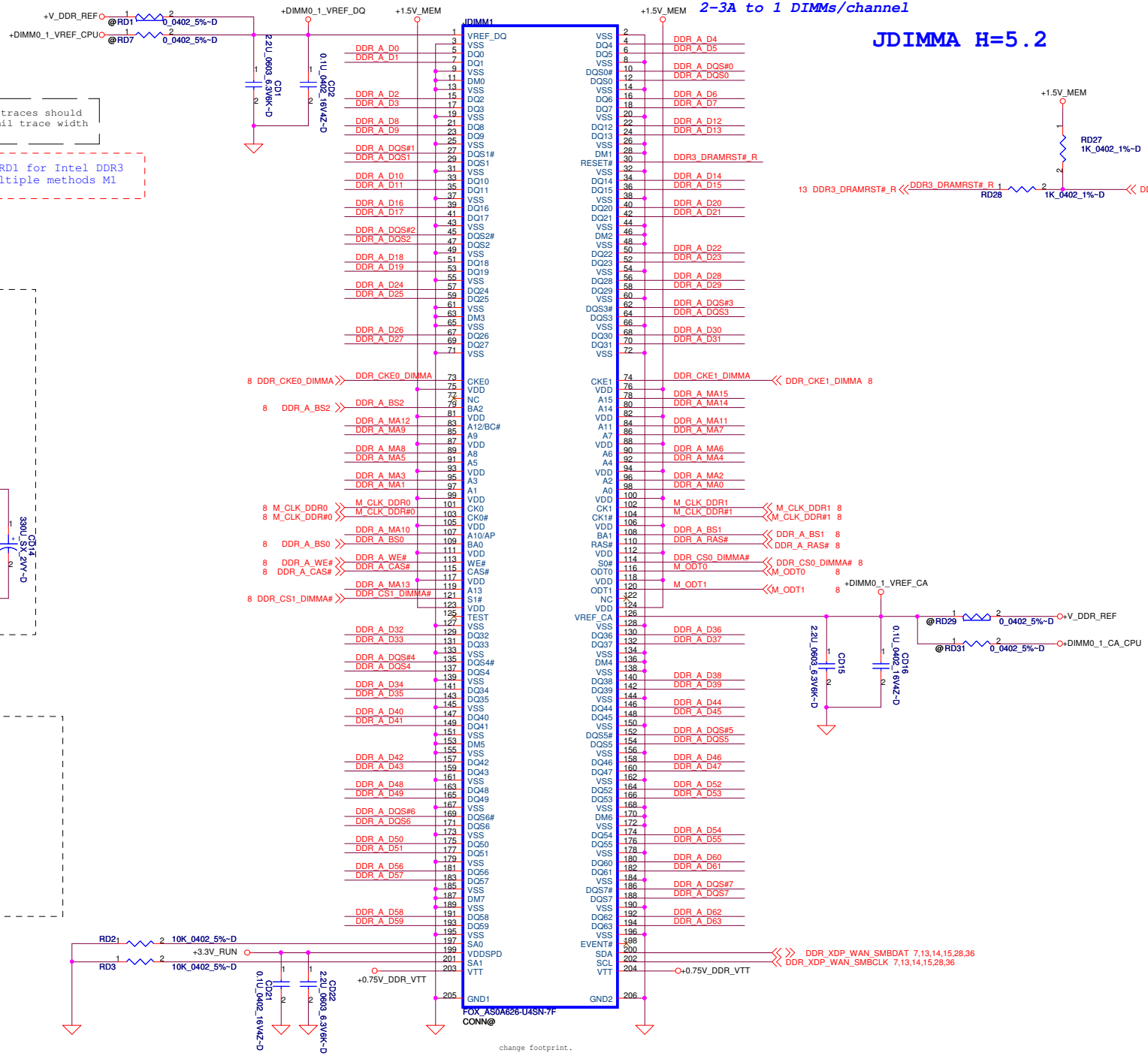
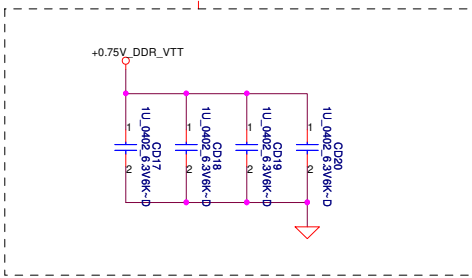
All VREF traces should  
have 10 mil trace width

Populate RD1 for Intel DDR3  
VREFDQ multiple methods M1

Layout Note:  
Place near JDIMMA



Layout Note:  
Place near JDIMMA.203,204



### JDIMMA H=5.2

1	VREF_DQ	2	+1.5V_MEM
3	VSS	4	DDR A D4
5	DQ0	5	DDR A D5
7	DQ1	6	DDR A D6
9	VSS	7	DDR A D7
11	DM0	8	DDR A DQS#0
13	VSS	9	DDR A DQS#0
15	DQ2	10	DDR A D8
17	DQ3	11	DDR A D9
19	VSS	12	DDR A D10
21	DQ8	13	DDR A D11
23	DQ9	14	DDR A D12
25	VSS	15	DDR A D13
27	DQS1#	16	DDR3_DRAMRST#_R
29	DQS1	17	DDR A D14
31	VSS	18	DDR A D15
33	DDR A D10	19	DDR A D20
35	DDR A D11	20	DDR A D21
37	VSS	21	DDR A D22
39	DDR A D16	22	DDR A D23
41	DDR A D17	23	DDR A D28
43	VSS	24	DDR A D29
45	DDR A DQS#2	25	DDR A DQS#3
47	DDR A DQS2	26	DDR A DQS3
49	VSS	27	DDR A D30
51	DDR A D18	28	DDR A D31
53	DDR A D19	29	VSS
55	VSS	30	VSS
57	DDR A D24	31	VSS
59	DDR A D25	32	VSS
61	VSS	33	VSS
63	DM3	34	VSS
65	VSS	35	VSS
67	DDR A D26	36	VSS
69	DDR A D27	37	VSS
71	VSS	38	VSS
73	DDR_CKE0_DIMMA	39	VSS
75	VDD	40	VSS
77	NC	41	VSS
81	VDD	42	VSS
83	DDR A MA12	43	VSS
85	DDR A MA9	44	VSS
87	A9	45	VSS
89	VDD	46	VSS
91	DDR A MA5	47	VSS
93	VDD	48	VSS
95	DDR A MA3	49	VSS
97	DDR A MA1	50	VSS
99	VDD	51	VSS
101	M_CLK_DDR0	52	VSS
103	M_CLK_DDR#0	53	VSS
105	VDD	54	VSS
107	DDR A MA10	55	VSS
109	DDR A BS0	56	VSS
111	VDD	57	VSS
113	DDR A WE#	58	VSS
115	DDR A CAS#	59	VSS
117	VDD	60	VSS
119	DDR A MA13	61	VSS
121	DDR CS1_DIMMA#	62	VSS
123	VDD	63	VSS
125	TEST	64	VSS
127	VSS	65	VSS
129	DQ32	66	VSS
131	DQ33	67	VSS
133	VSS	68	VSS
135	DDR A DQS#4	69	VSS
137	DDR A DQS4	70	VSS
139	VSS	71	VSS
141	DDR A D34	72	VSS
143	DDR A D35	73	VSS
145	VSS	74	VSS
147	DDR A D40	75	VSS
149	DDR A D41	76	VSS
151	VSS	77	VSS
153	DM5	78	VSS
155	VSS	79	VSS
157	DDR A D42	80	VSS
159	DDR A D43	81	VSS
161	VSS	82	VSS
163	DDR A D48	83	VSS
165	DDR A D49	84	VSS
167	VSS	85	VSS
169	DDR A DQS#6	86	VSS
171	DDR A DQS6	87	VSS
173	VSS	88	VSS
175	DDR A D50	89	VSS
177	DDR A D51	90	VSS
179	VSS	91	VSS
181	DDR A D56	92	VSS
183	DDR A D57	93	VSS
185	VSS	94	VSS
187	DM7	95	VSS
189	VSS	96	VSS
191	DQ68	97	VSS
193	DQ69	98	VSS
195	VSS	99	VSS
197	VSS	100	VSS
199	VDDSPD	101	VSS
201	SA1	102	VSS
203	VTT	103	VSS
205	GND1	104	VSS
206	GND2	105	VSS
207	VSS	106	VSS
208	VSS	107	VSS
209	VSS	108	VSS
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277	VSS	176	VSS
278	VSS	177	VSS
279	VSS	178	VSS
280	VSS	179	VSS
281	VSS	180	VSS
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300	VSS	199	VSS
301	VSS	200	VSS
302	VSS	201	VSS
303	VSS	202	VSS
304	VSS	203	VSS
305	VSS	204	VSS

change footprint.

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Title			
DDRIII-SODIMM SLOT1			
Size			
Document Number			
LA-6592P			
Rev			
1.0			
Date:	Thursday, January 13, 2011	Sheet	12 of 75

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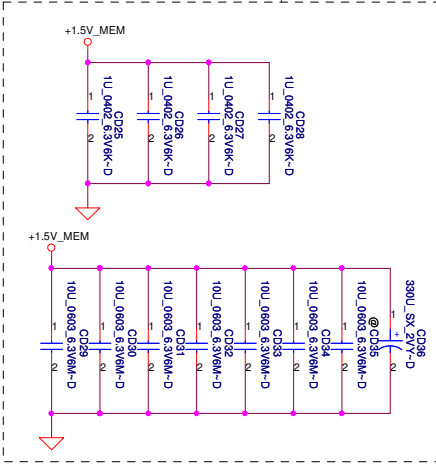
All VREF traces should have 10 mil trace width



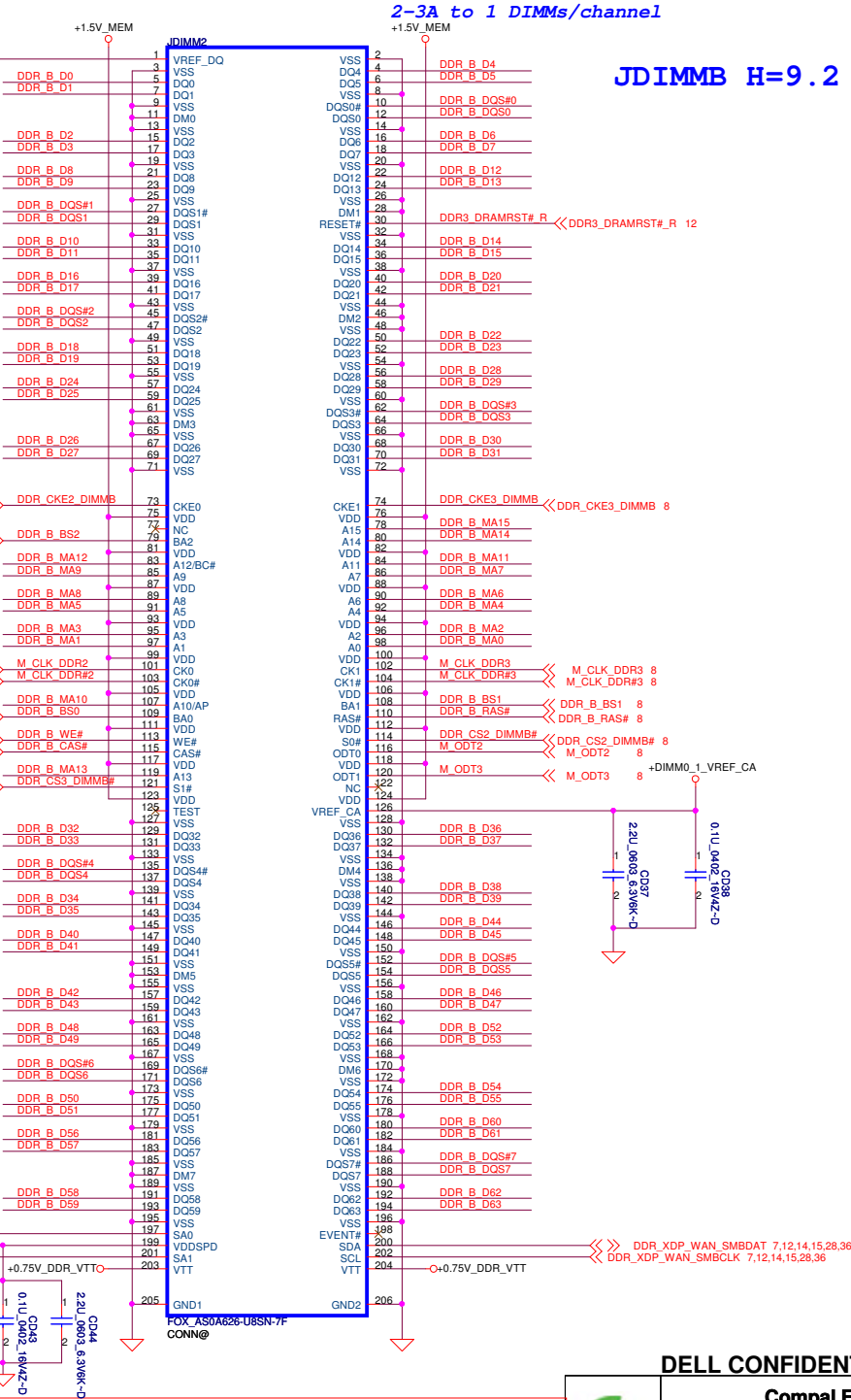
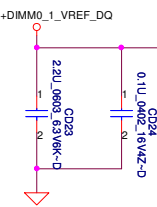
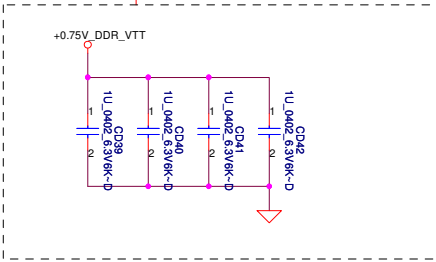
Populate RD4 for Intel DDR3 VREFDQ multiple methods M1

Note:  
Check voltage tolerance of VREF\_DQ at the DIMM socket

Layout Note:  
Place near JDIMMB



Layout Note:  
Place near JDIMMB.203,204



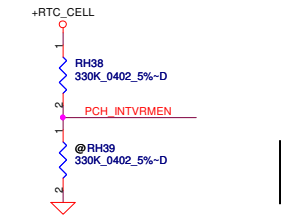
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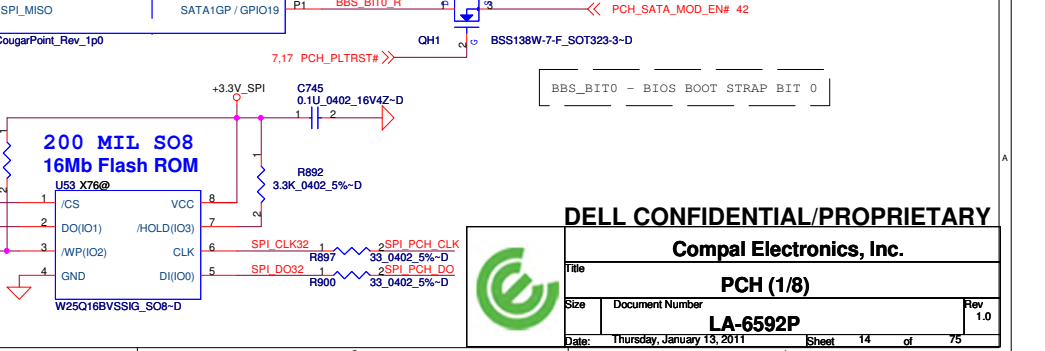
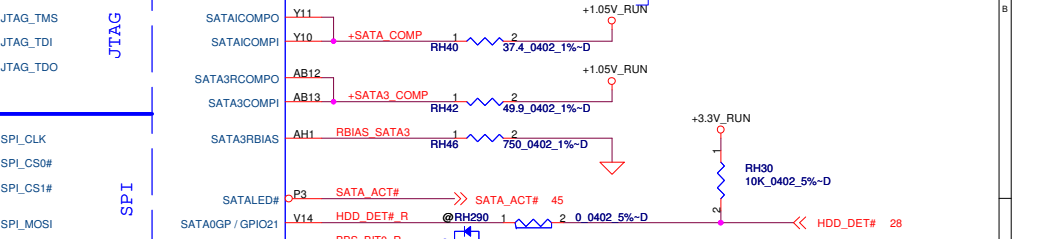
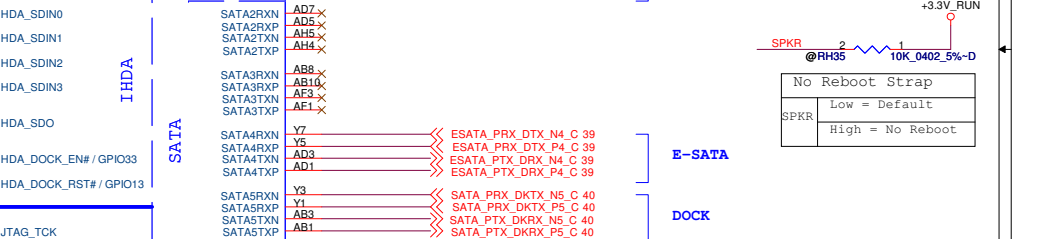
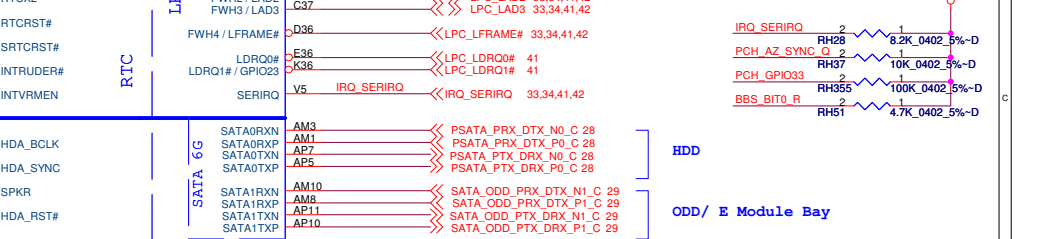
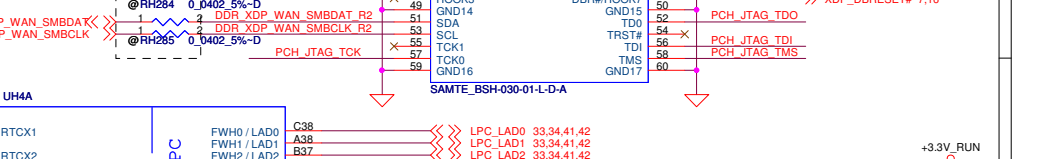
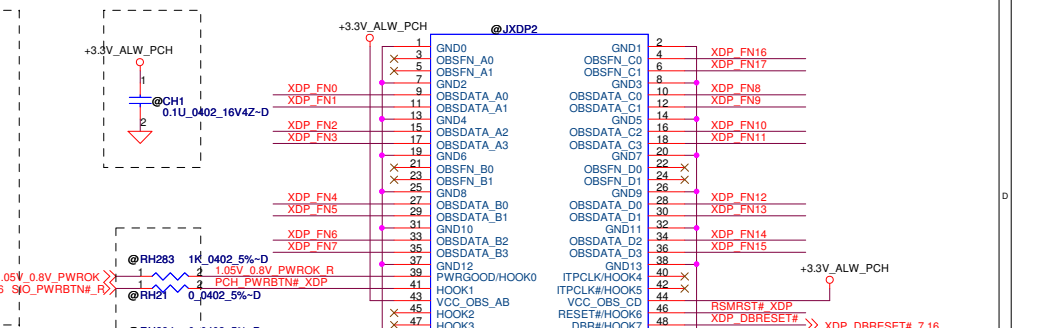
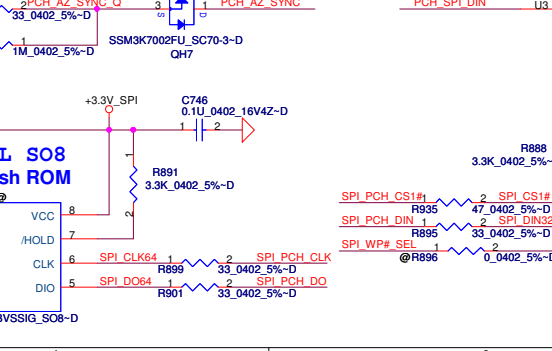
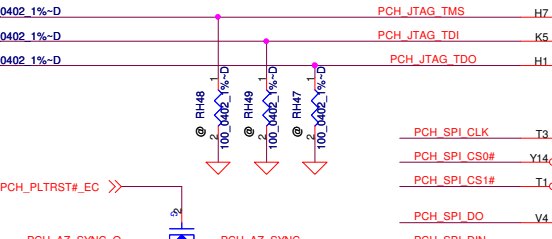
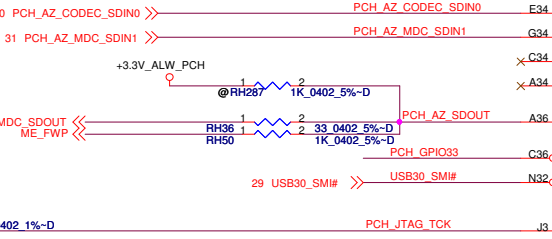
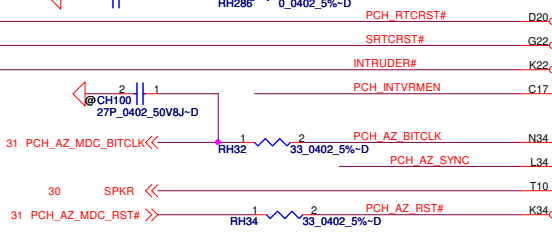
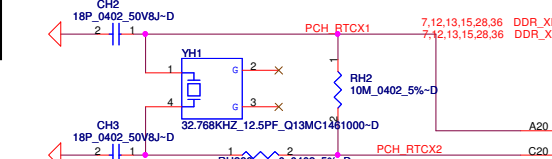
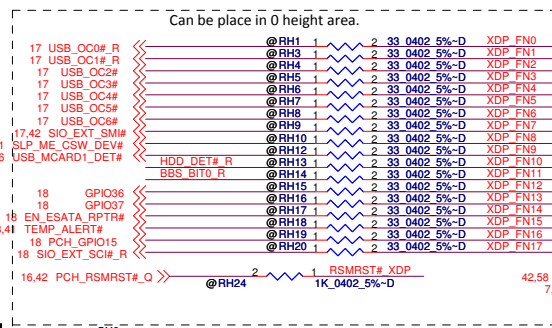
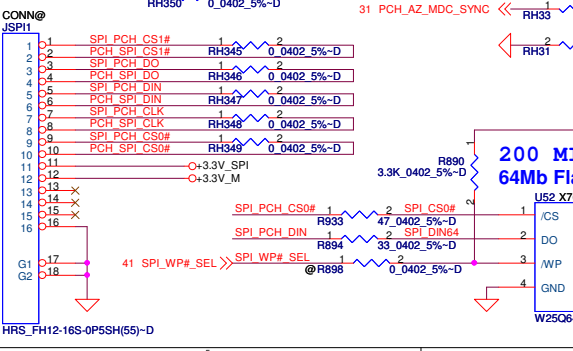
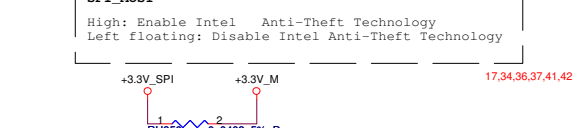
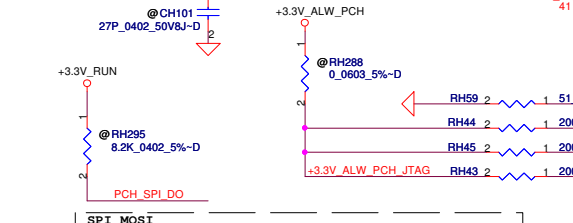
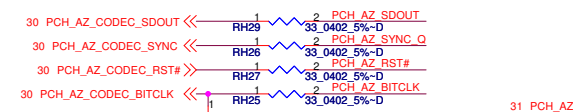
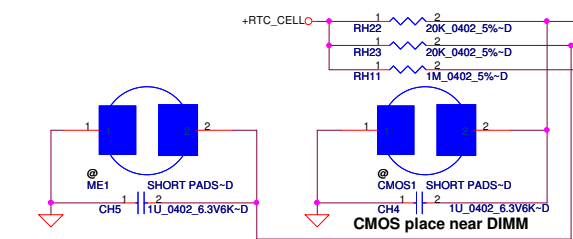
CMOS CLR1		CMOS setting	
Shunt	Clear CMOS	Open	Keep CMOS

ME CLR1		TPM setting	
Shunt	Clear ME RTC Registers	Open	Keep ME RTC Registers

PCH\_AZ\_SYNC is sampled at the rising edge of RSMRST# pin. So signal should be PU to the ALWAYS rail.



**INTVTRMEN- Integrated SUS**  
 1.1V VRM Enable  
 High - Enable Internal VRs  
 Low - Enable External VRs



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**PCH (1/8)**

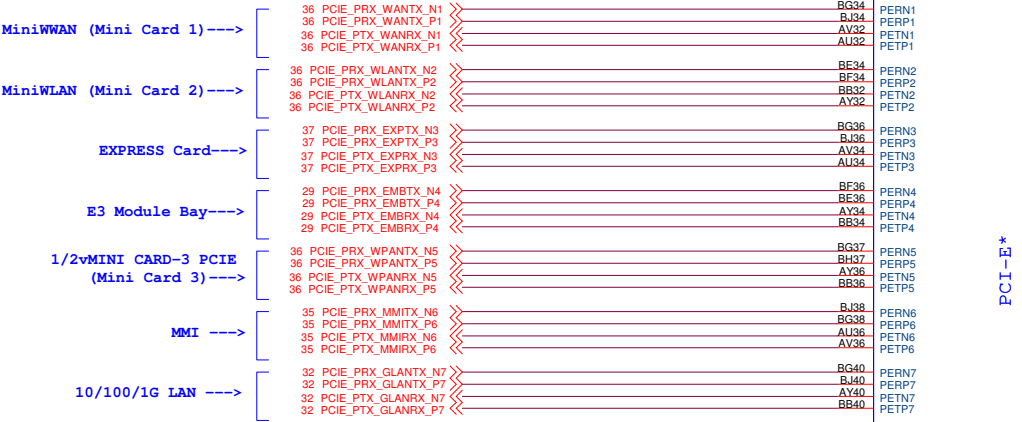
Title: PCH (1/8)

Size: Document Number: LA-6592P

Date: Thursday, January 13, 2011 Sheet 14 of 75

Rev 1.0

Follow DG0.9 Device down & Express/Mini card topology

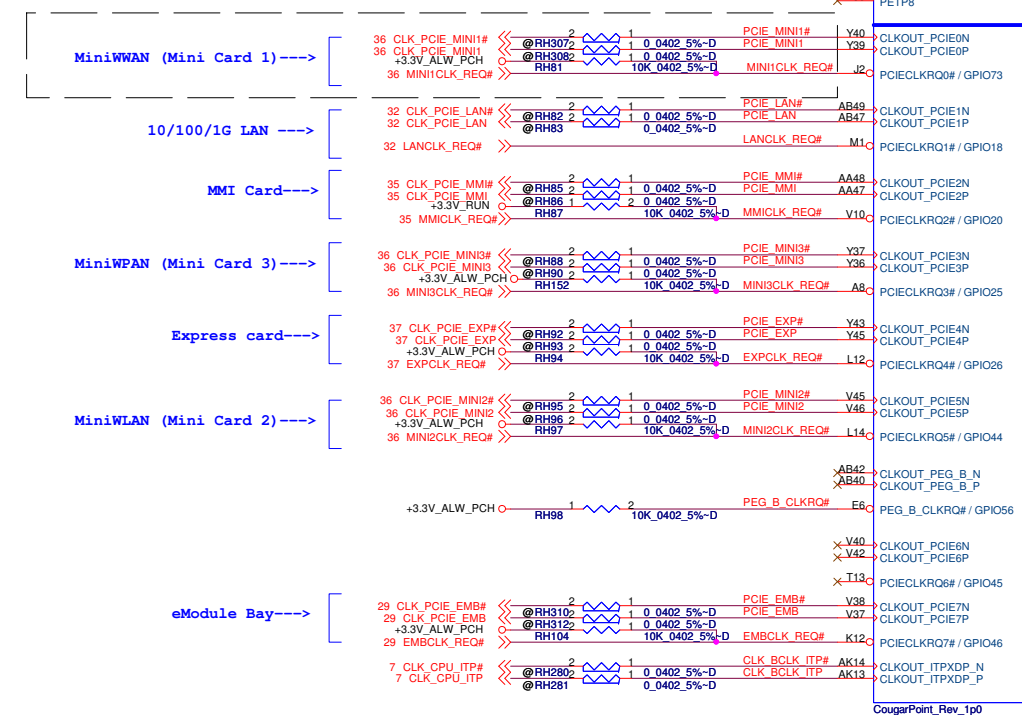


UH4B

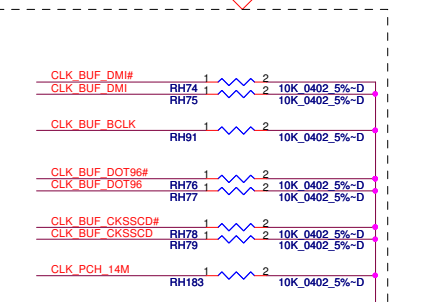
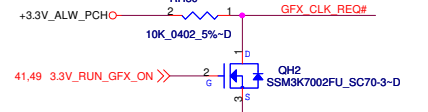
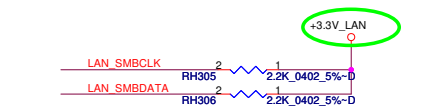
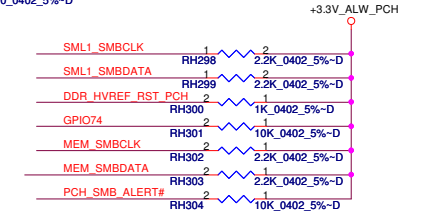
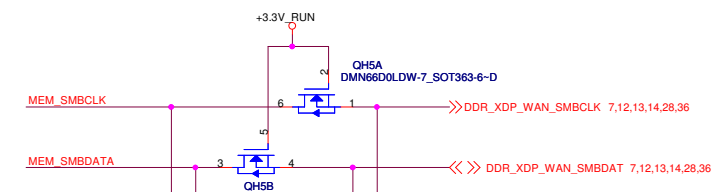
SMBUS  
Controller Link  
PCI-E\*

CLOCKS

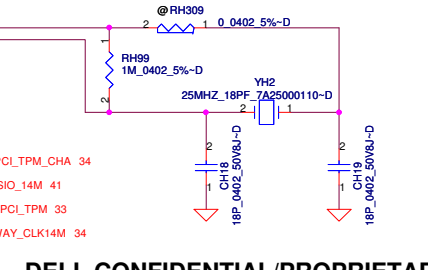
FLEX CLOCKS



CougarPoint\_Rev\_1p0



CLOCK TERMINATION for FCIM and need close to PCH



PCIE REQ power rail:  
suspend: 0 3 4 5 6 7  
core: 1 2

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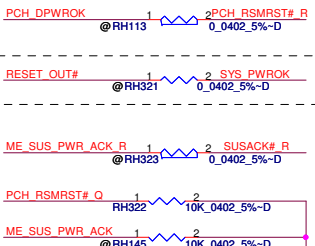
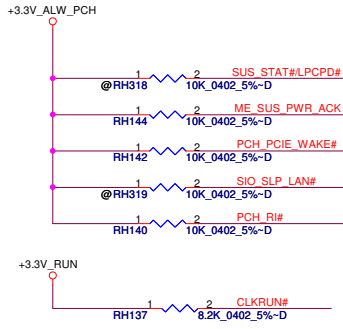


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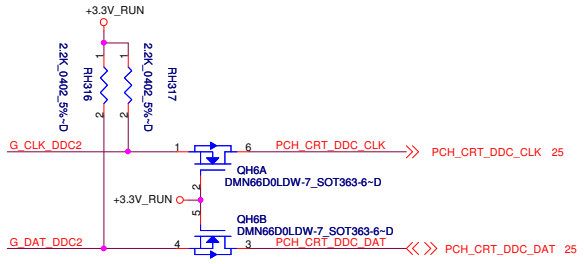
Compal Electronics, Inc.

Title: PCH (2/8)

Size: Document Number LA-6592P Rev 1.0  
Date: Tuesday, January 18, 2011 Sheet 15 of 75



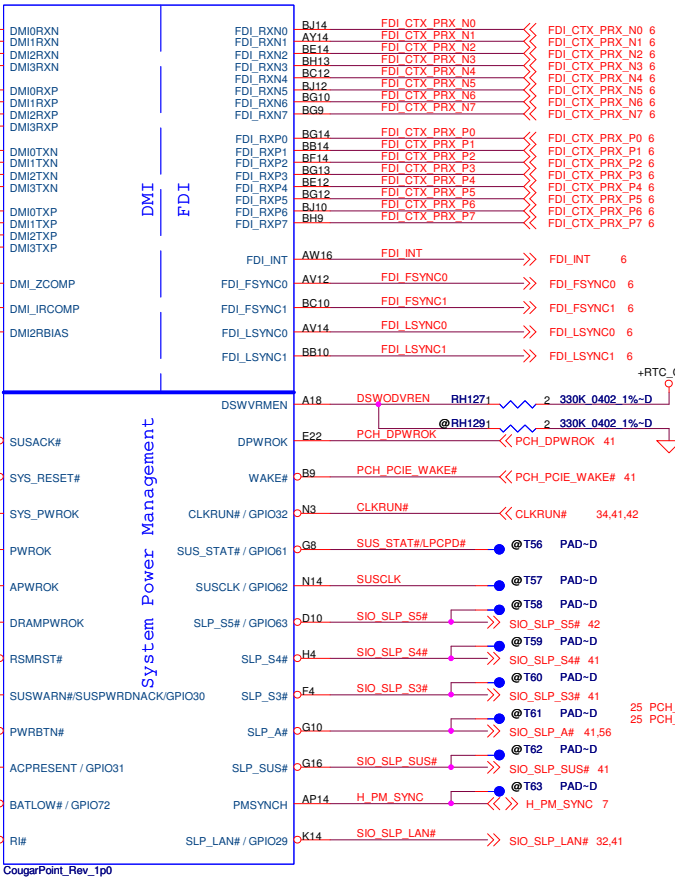
DSWODVREN - On Die DSW VR Enable  
 Enabled (DEFAULT)  
 HIGH: R221 STUFFED,  
 R222 UNSTUFFED  
 Disabled  
 LOW: R221 STUFFED,  
 R222 UNSTUFFED



L_DDC_DATA - LVDS Detected	
1	LVDS is detected
0	LVDS is not detected

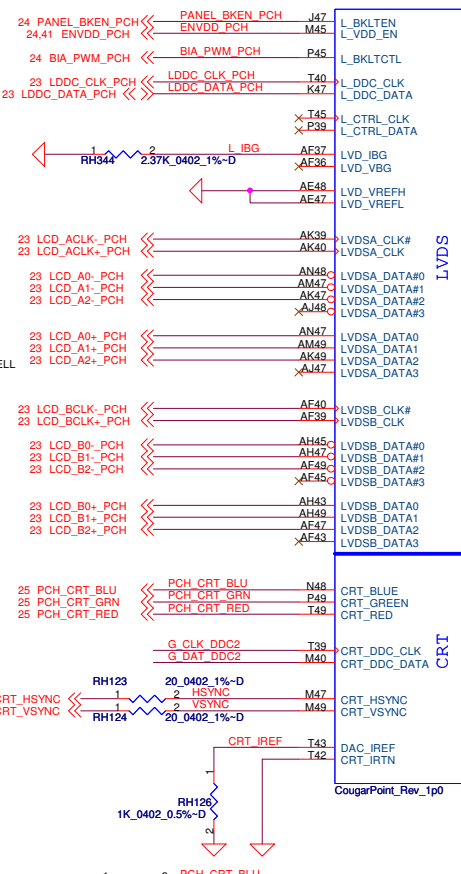
Intel request DDPB can not support eDP

UH4C

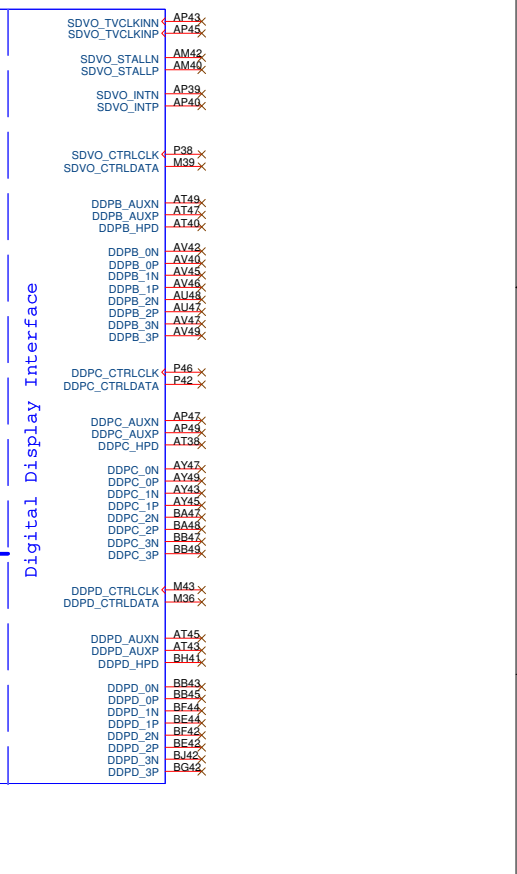


CougarPoint\_Rev\_1p0

UH4D



CougarPoint\_Rev\_1p0



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**PCH (3/8)**

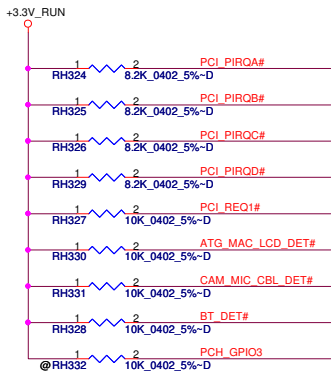
LA-6592P

Thursday, January 13, 2011

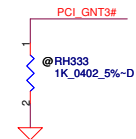
Sheet 16 of 75



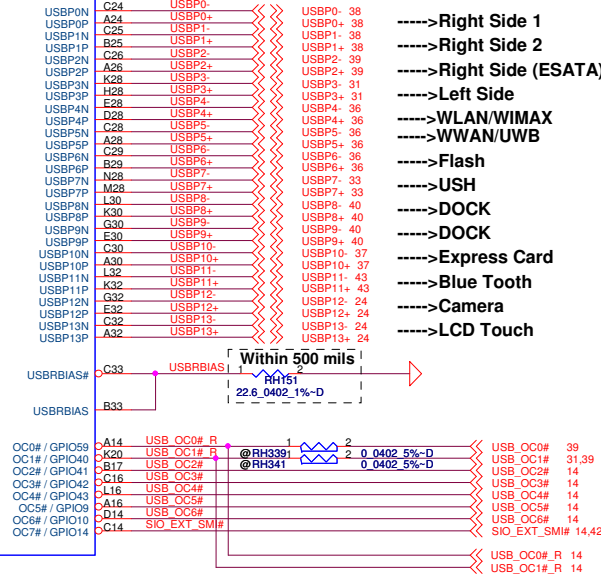
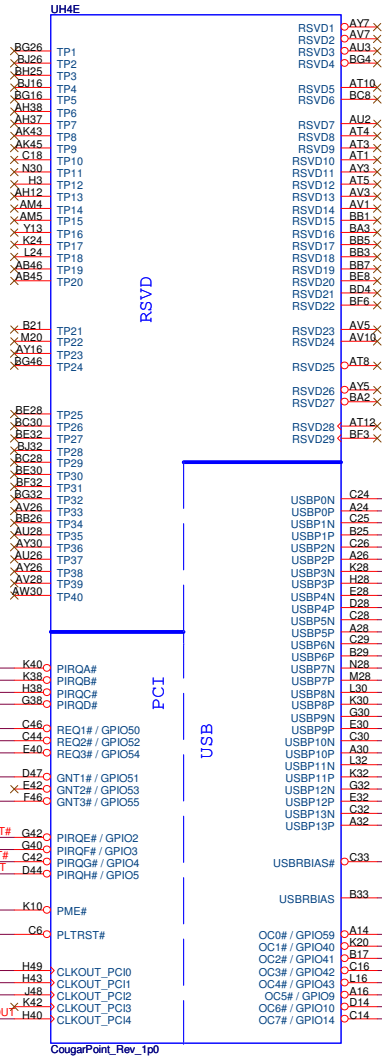
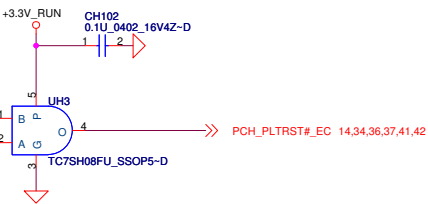
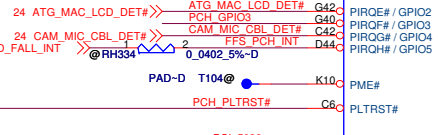
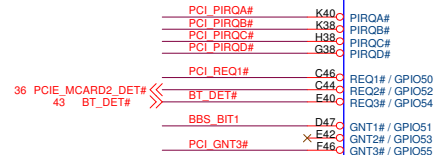
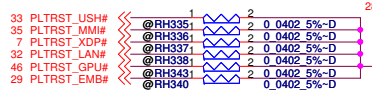




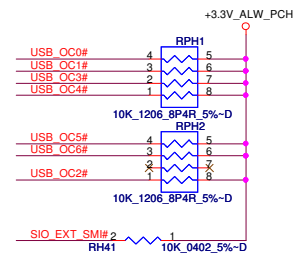
LVDS_CBL_ID	High : Normal type panel
	Low : High contrast ratio brightness



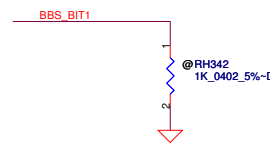
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default



- >Right Side 1
- >Right Side 2
- >Right Side (ESATA)
- >Left Side
- >WLAN/WIMAX
- >WWAN/UWB
- >Flash
- >USH
- >DOCK
- >DOCK
- >Express Card
- >Blue Tooth
- >Camera
- >LCD Touch



BBS_BIT1	SATA_SLPD (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



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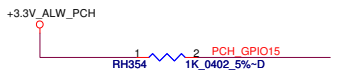
**Compal Electronics, Inc.**

**PCH (4/8)**

**LA-6592P**

Size: \_\_\_\_\_ Document Number: \_\_\_\_\_ Rev: 1.0

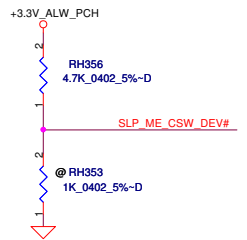
Date: Thursday, January 13, 2011 Sheet 17 of 75



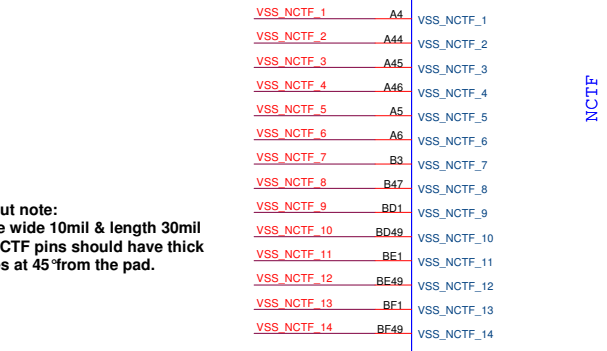
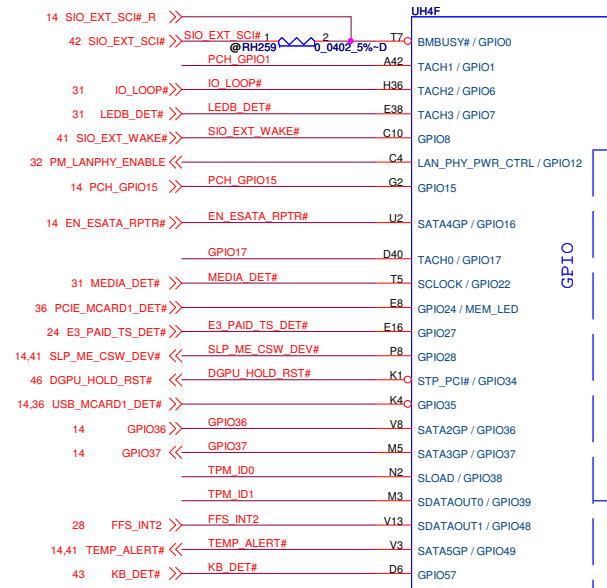
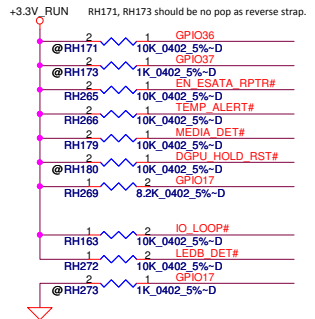
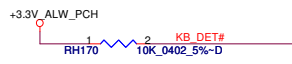
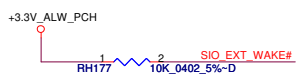
PCH\_GPIO15 TLS Confidentiality

Low = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality

High = Intel ME Crypto TLS cipher suite with confidentiality



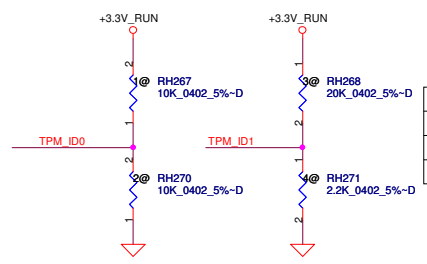
Note: PCH has internal pull up 20k ohm on E3\_PAID\_TS\_DET# (GPIO27)



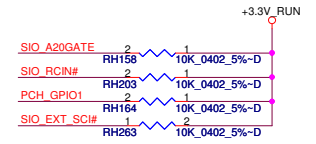
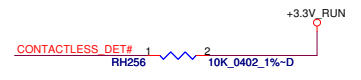
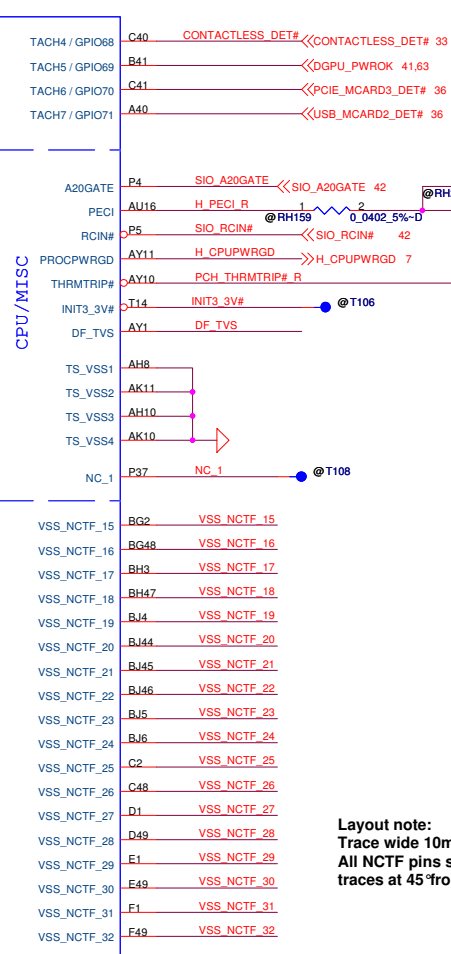
CougarPoint\_Rev\_1p0

Layout note:  
Trace wide 10mil & length 30mil  
All NCTF pins should have thick traces at 45° from the pad.

Layout note:  
Trace wide 10mil & length 30mil  
All NCTF pins should have thick traces at 45° from the pad.



	TPM_ID0	TPM_ID1
China TPM	0	0
No TPM, No China TPM	0	1
USH2.0	1	1



PLACE RH150 CLOSE TO THE BRANCHING POINT ( TO CPU and NVRAM CONNECTOR)

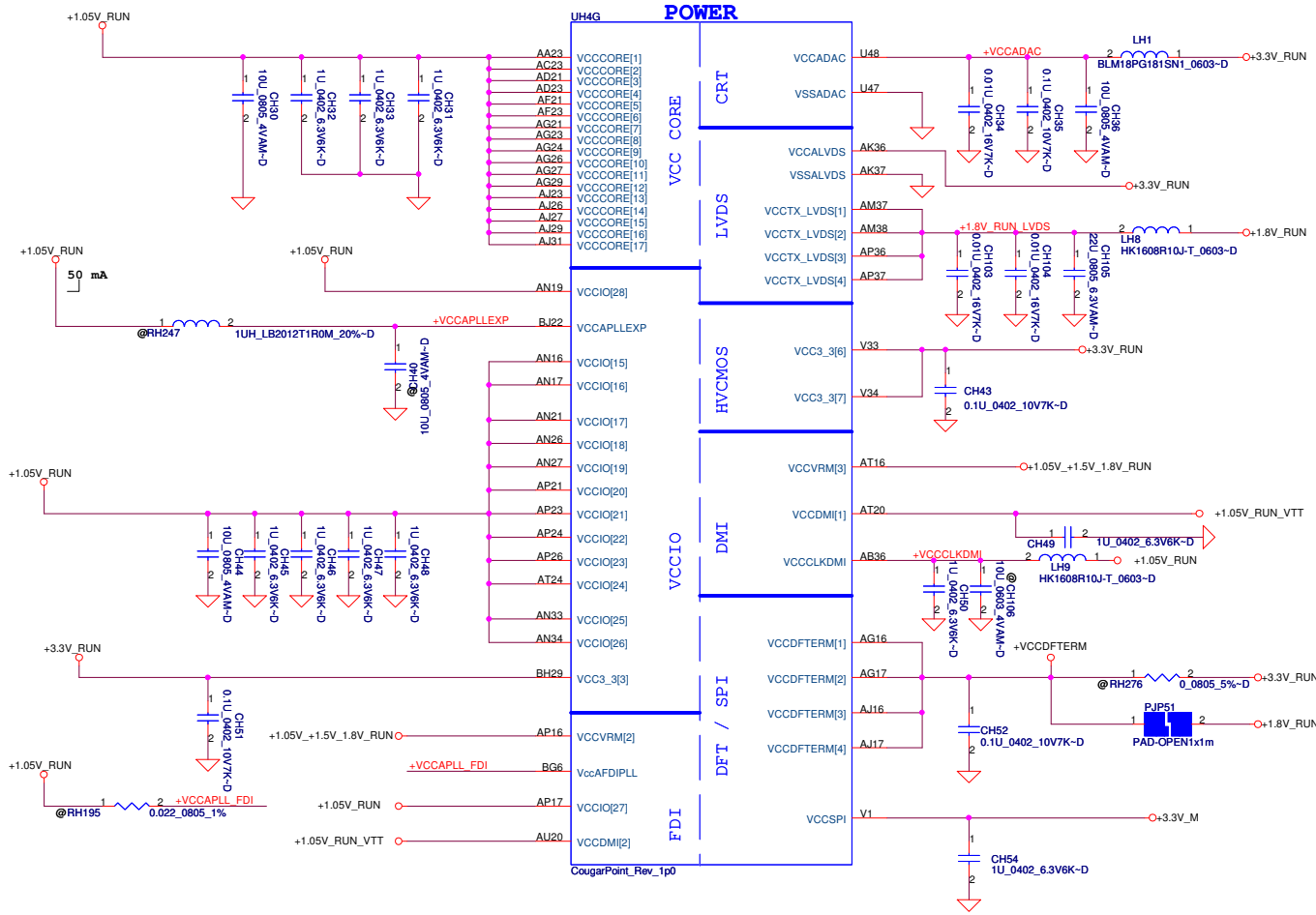
DF\_TVS R<sub>1</sub>

DMI & FDI Termination Voltage	
DF_TVS	Set to Vss when LOW Set to Vcc when HIGH

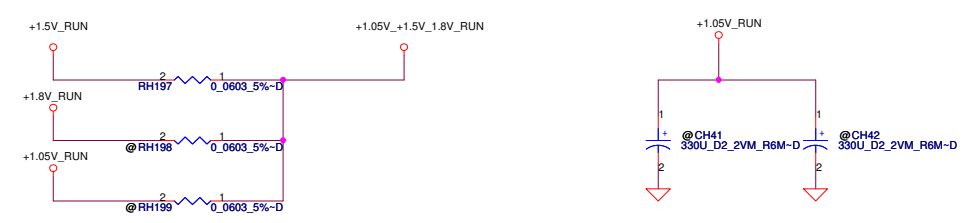


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Title <b>PCH (5/8)</b>		
Size	Document Number <b>LA-6592P</b>	Rev 1.0
Date: Thursday, January 13, 2011	Sheet 18	of 75



PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.020
VccDSW3_3	3.3	0.003
VCCDFTERM	1.8	0.19
VccRTC	3.3	2 (mA)
VccSus3_3	3.3	0.119
VccSusHDA	3.3	0.01
VccVRM	1.8 / 1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06



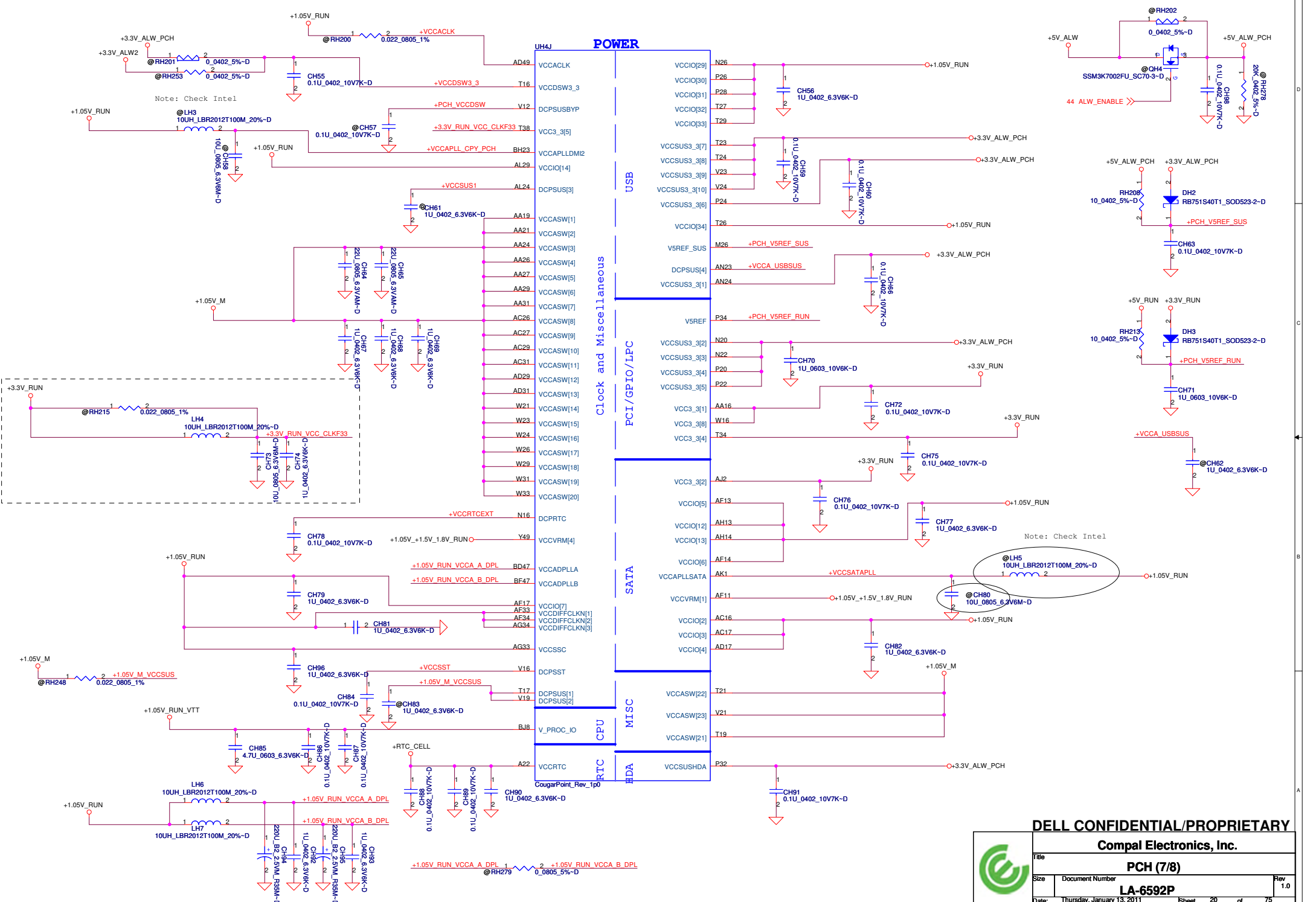
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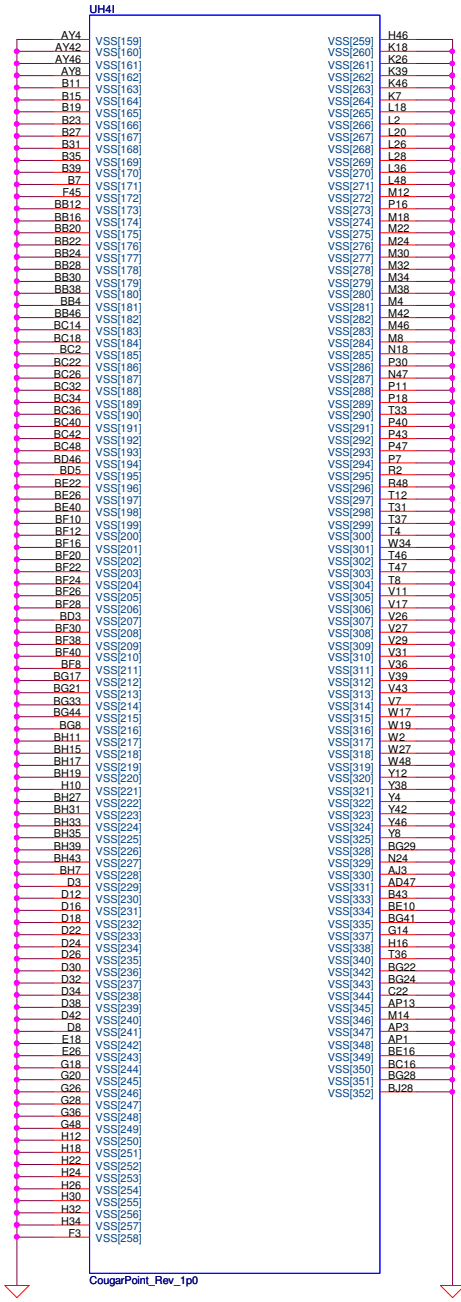
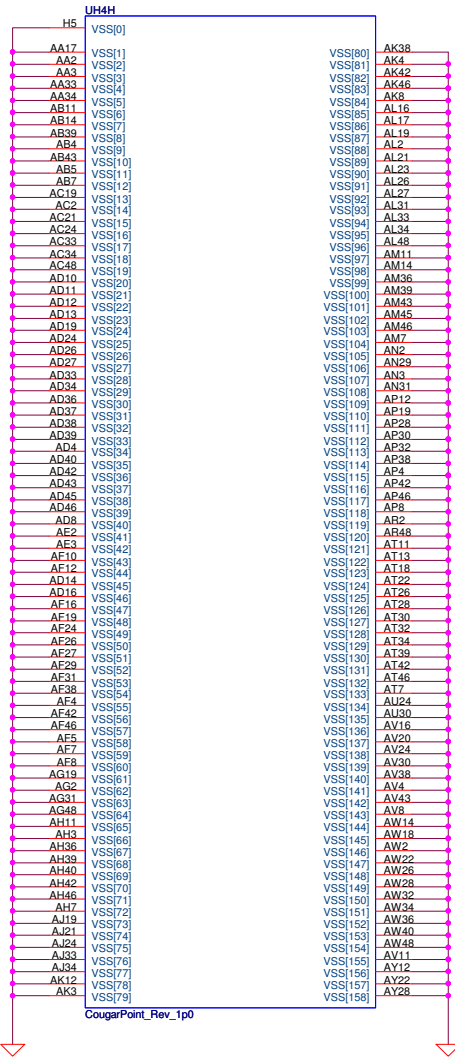
Title			PCH (6/8)		
Size	Document Number	Rev			
	LA-6592P	1.0			
Date:	Thursday, January 13, 2011	Sheet	19	of	75



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Compal Electronics, Inc.		
PCH (7/8)		
LA-6592P	Rev 1.0	
Thursday, January 13, 2011	Sheet 20 of 75	



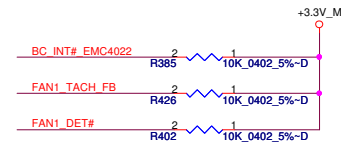
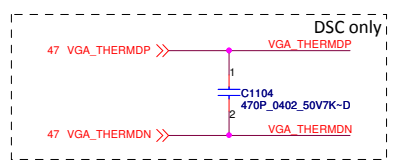
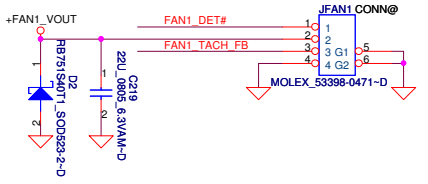
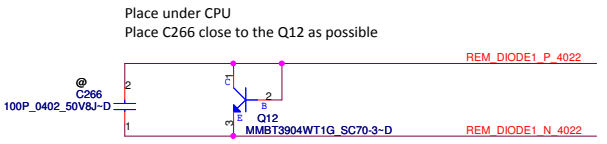
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**Compal Electronics, Inc.**

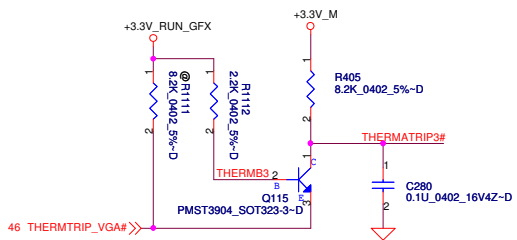
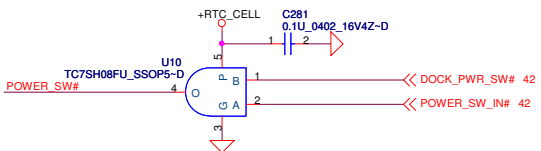
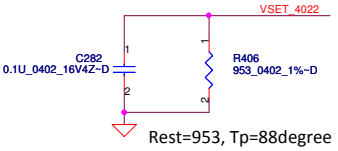
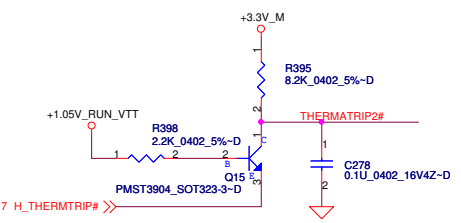
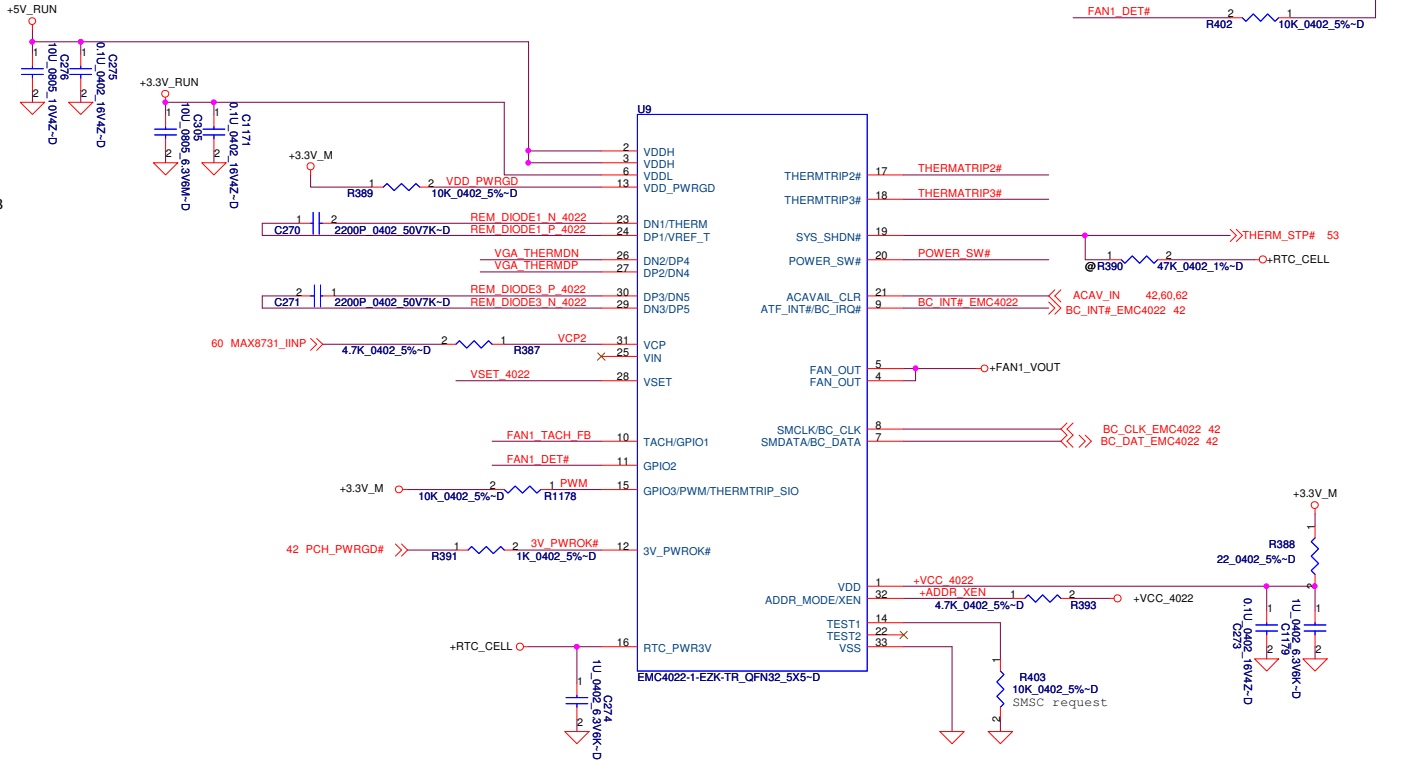
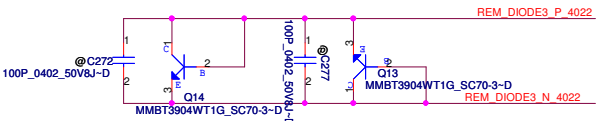
Title: **PCH (8/8)**

Size: **LA-6592P**

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- DP3/DN3 for SODIMM on Q14, place Q14 close to SODIMM and C272 close to Q14
- DP5/DN5 for Skin on Q13, place Q13 close to JMINI1 for WWAN and C277 close Q13

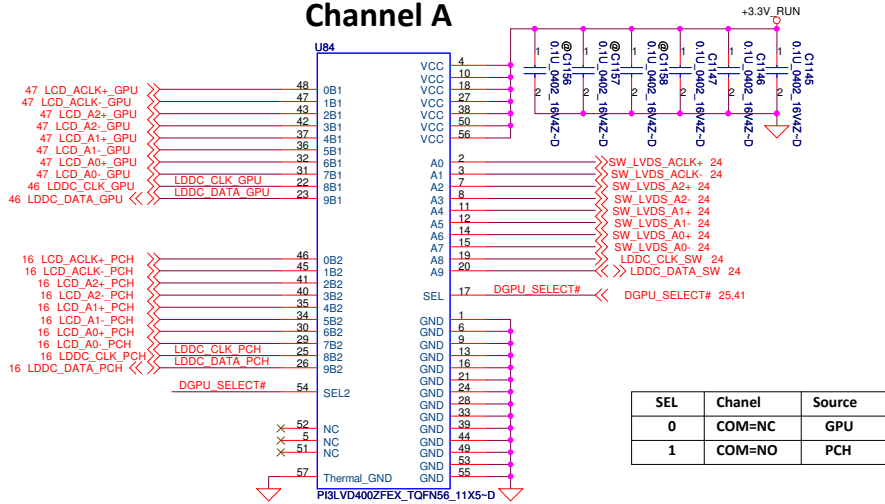


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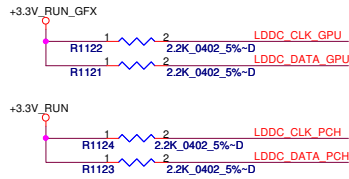
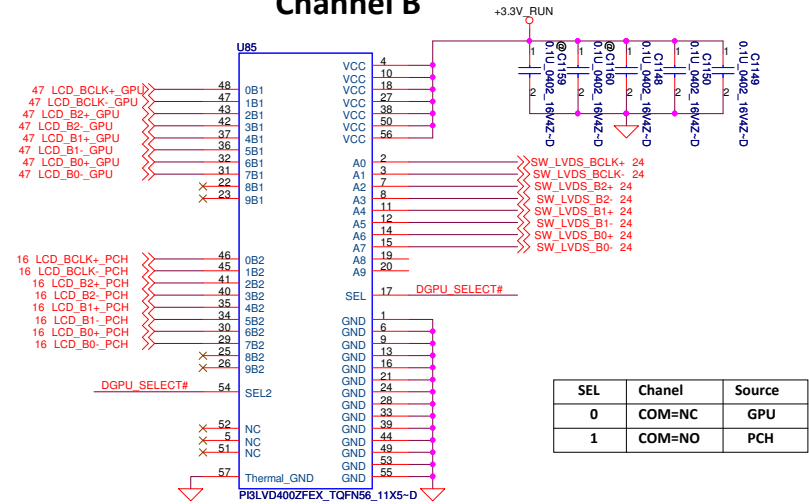
		<b>Compal Electronics, Inc.</b>		
		<b>FAN &amp; Thermal Sensor</b>		
Size	Document Number	Rev		
	<b>LA-6592P</b>	<b>1.0</b>		
Date:	Thursday, January 13, 2011	Sheet	22 of 75	

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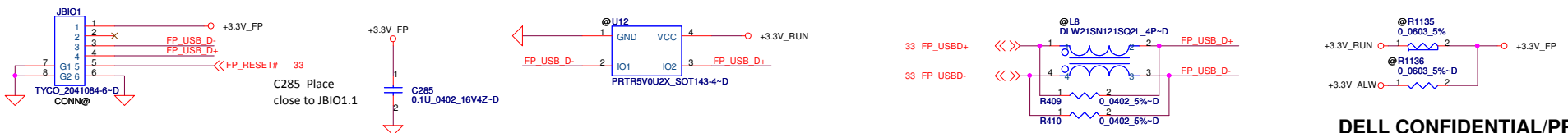
### Channel A



### Channel B



### Fingerprint CONN.



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**LA-6592P**

LA-6592P

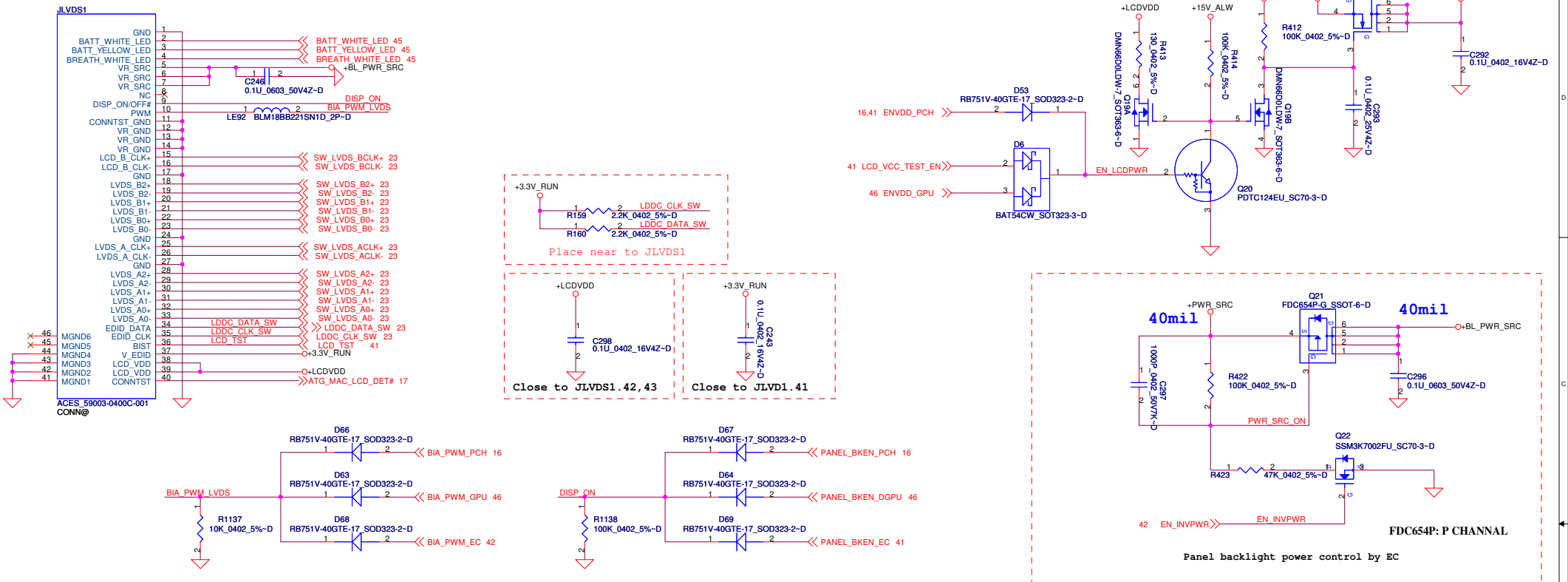
1.0

Tuesday, January 18, 2011

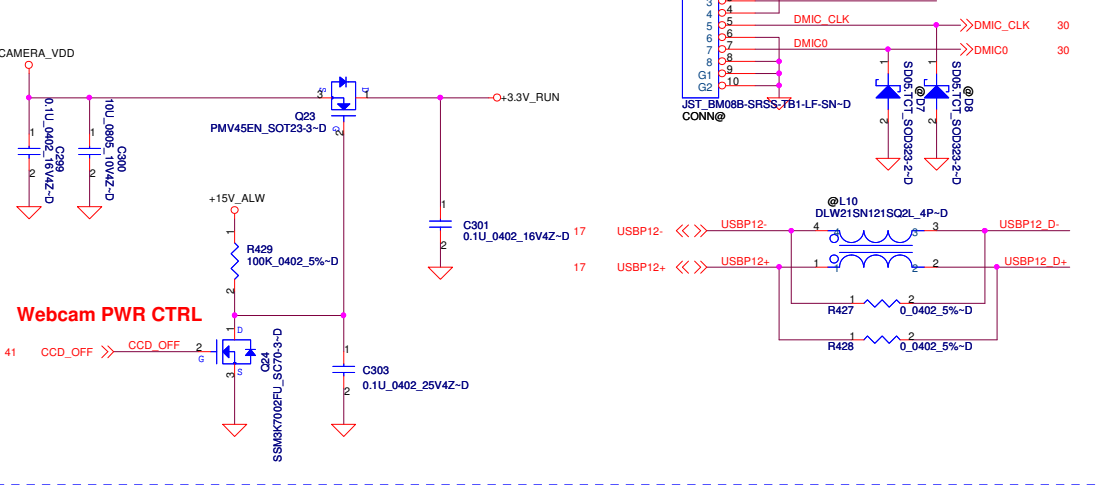
Sheet 23 of 75

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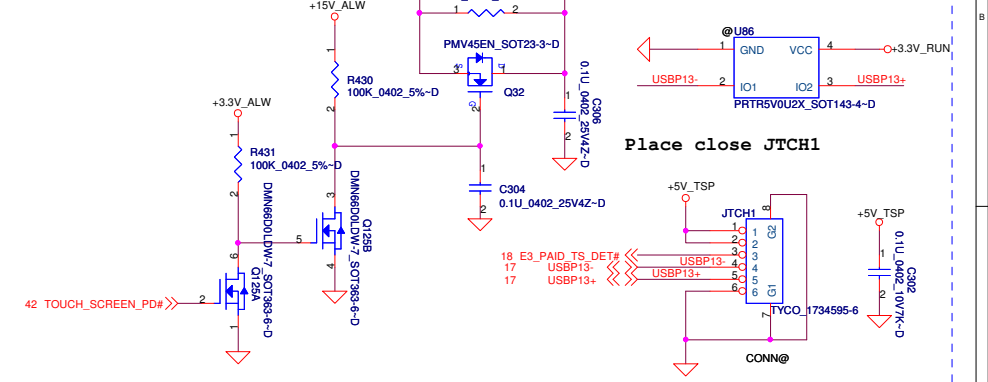
### LCD Power



### For Webcam



### Touch Screen Connector



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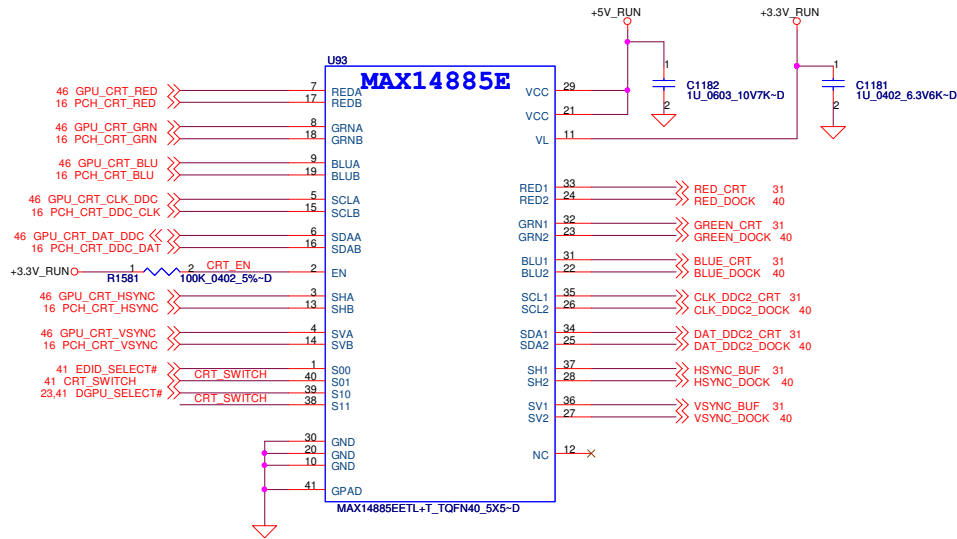
<b>Compal Electronics, Inc.</b>			
<b>eDP &amp; CAM &amp; TS Conn</b>			
<b>LA-6592P</b>			
Date:	Thursday, January 13, 2011	Sheet	24 of 75
Size:	Document Number	Rev	1.0

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Channel A --> GPU

Channel B --> PCH



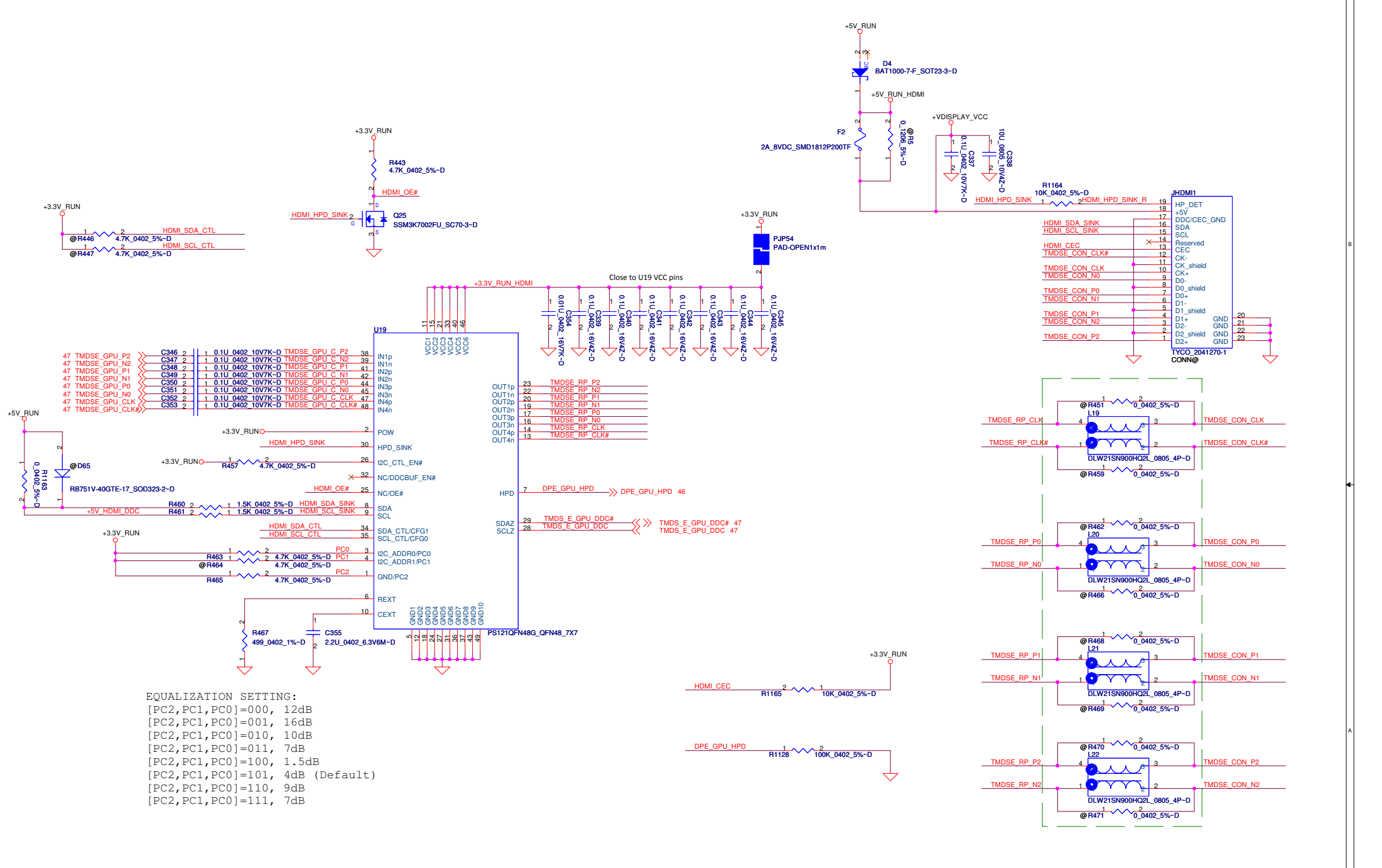
CRT_SWITCH	0	0	1	1
DGPU_SELECT#	0	1	0	1
EDID_SELECT#	0	1	0	1
	A --> Port 1	B --> Port 1	A --> Port 2	B --> Port 2

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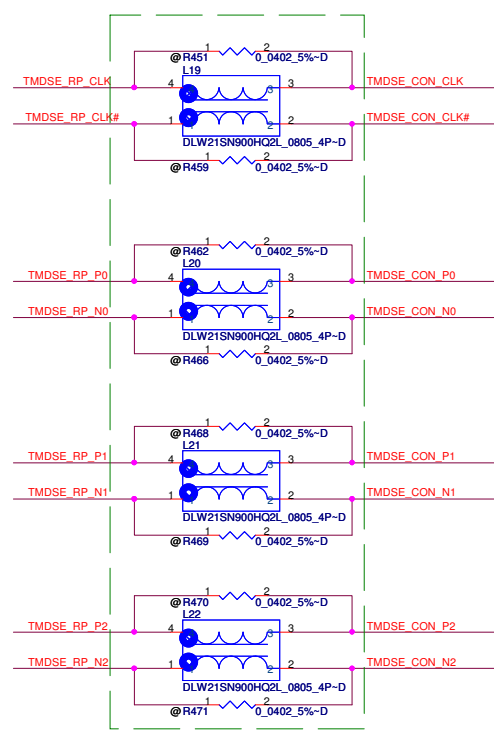
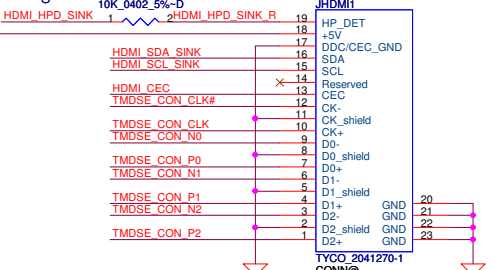


Compal Electronics, Inc.			
Title <b>CRT/Video switch</b>			
Size	Document Number <b>LA-6592P</b>	Rev <b>1.0</b>	
Date: Thursday, January 13, 2011	Sheet 25	of 75	

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EQUALIZATION SETTING:  
 [PC2,PC1,PC0]=000, 12dB  
 [PC2,PC1,PC0]=001, 16dB  
 [PC2,PC1,PC0]=010, 10dB  
 [PC2,PC1,PC0]=011, 7dB  
 [PC2,PC1,PC0]=100, 1.5dB  
 [PC2,PC1,PC0]=101, 4dB (Default)  
 [PC2,PC1,PC0]=110, 9dB  
 [PC2,PC1,PC0]=111, 7dB



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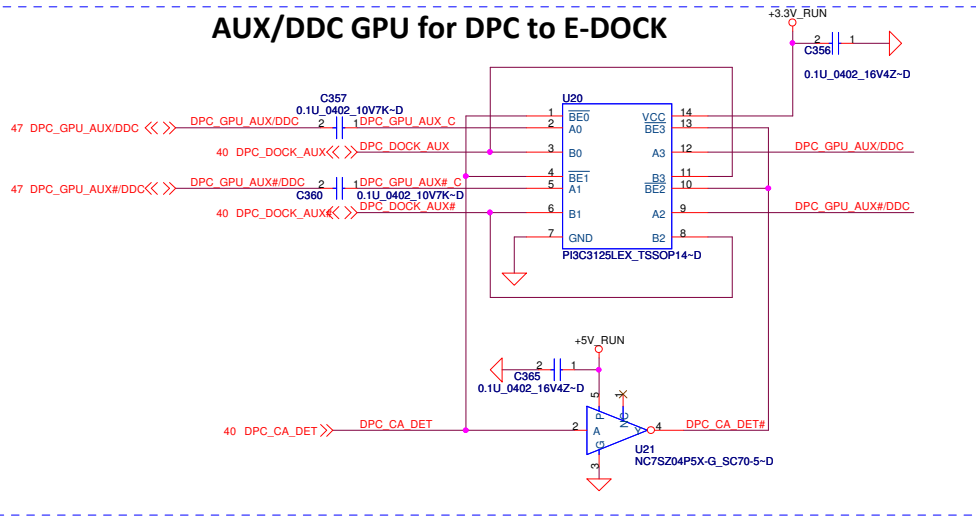
Title: **HDMI port**

Size: Document Number **LA-6592P** Rev: 1.0

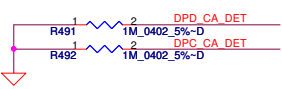
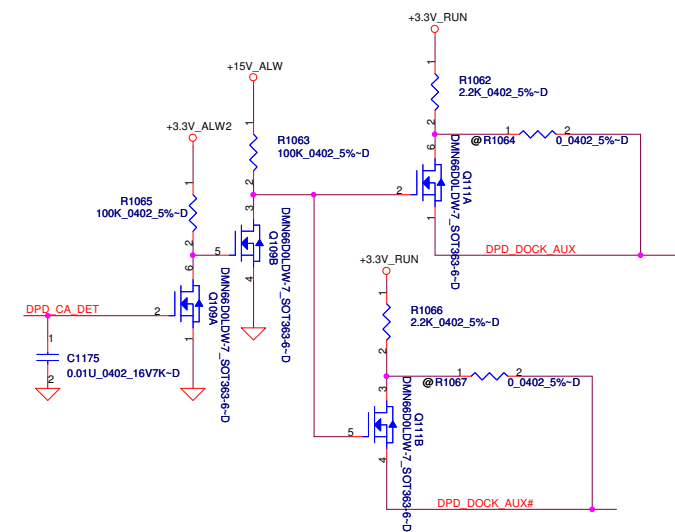
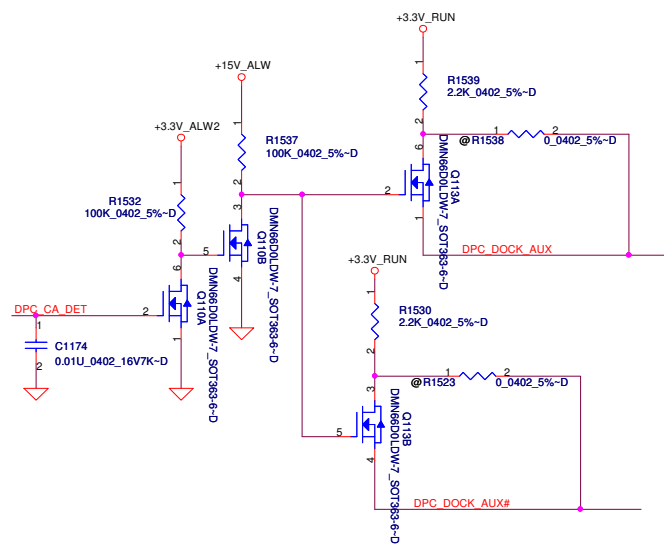
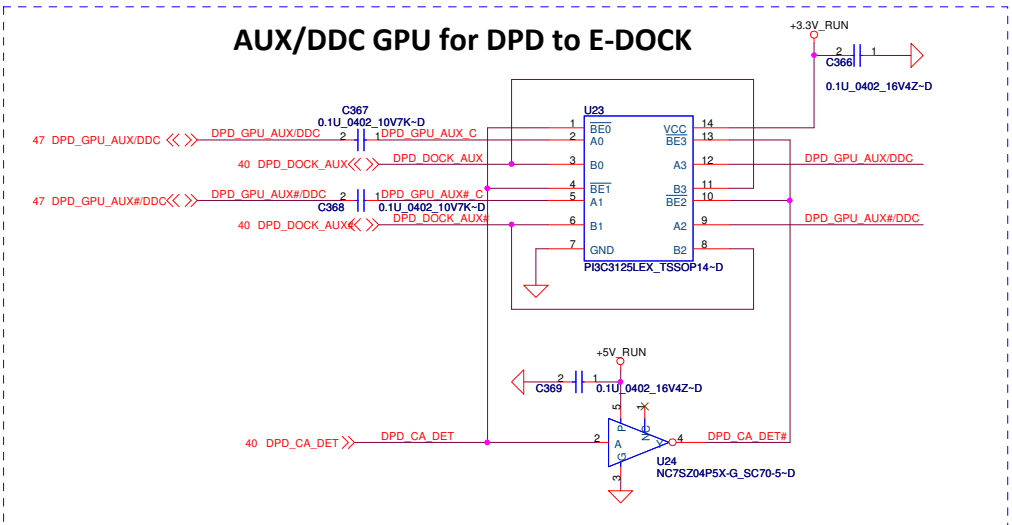
Date: Tuesday, January 18, 2011 Sheet: 26 of 75

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### AUX/DDC GPU for DPC to E-DOCK



### AUX/DDC GPU for DPD to E-DOCK

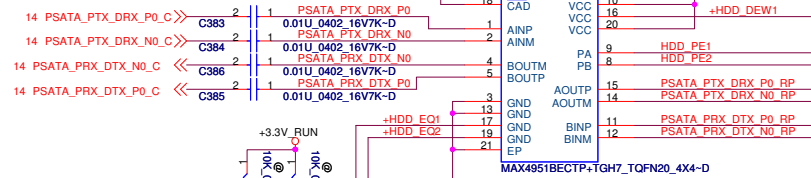


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		<b>Compal Electronics, Inc.</b>	
		<b>DP AUX SW</b>	
Size	Document Number	Rev	
	<b>LA-6592P</b>	<b>1.0</b>	
Date:	Thursday, January 13, 2011	Esheet	27 of 75

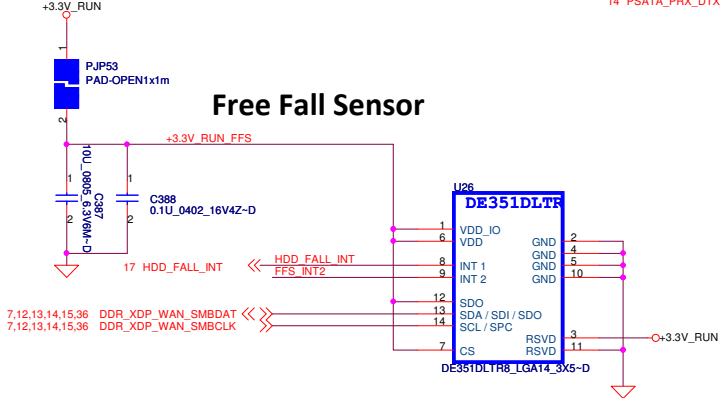
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## HDD Repeater

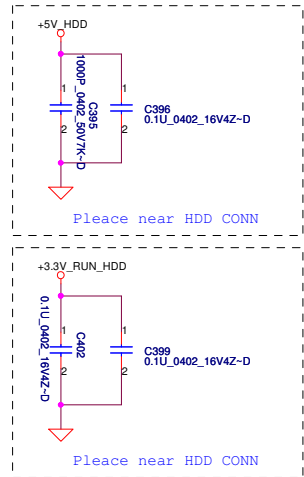
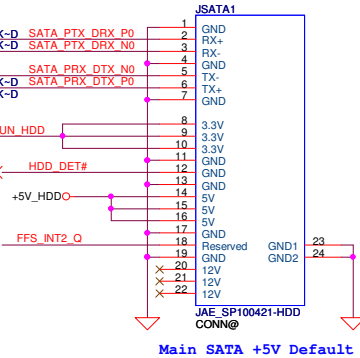
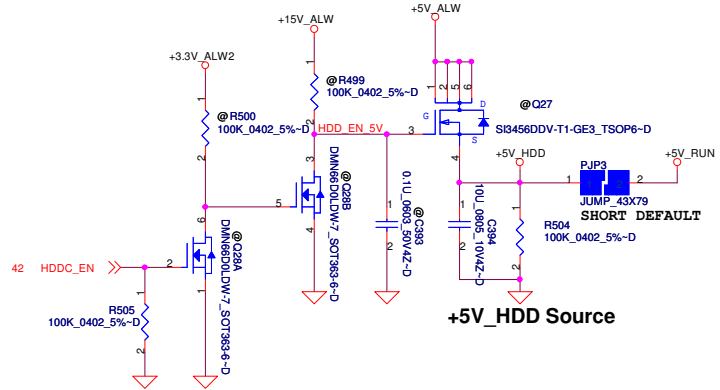


Note: +HDD\_DEW1, +HDD\_DEW2, +HDD\_EQ1, +HDD\_EQ2 need to route 10 mils and R1169, R1171, R1174, R1176 need to change to 10k and no stuff R1174, R1176 to support TI SN75LVCP601

## Free Fall Sensor



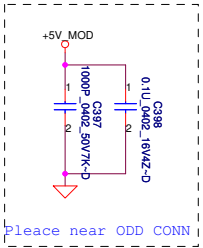
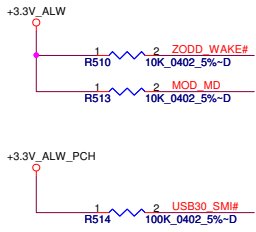
## HDD PWR



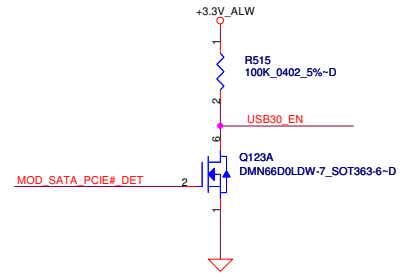
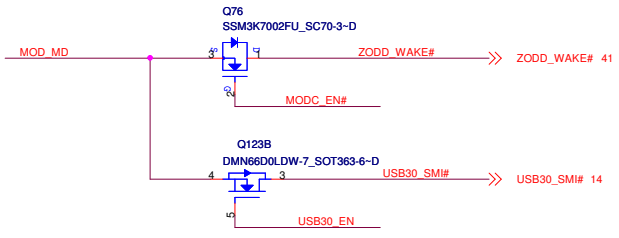
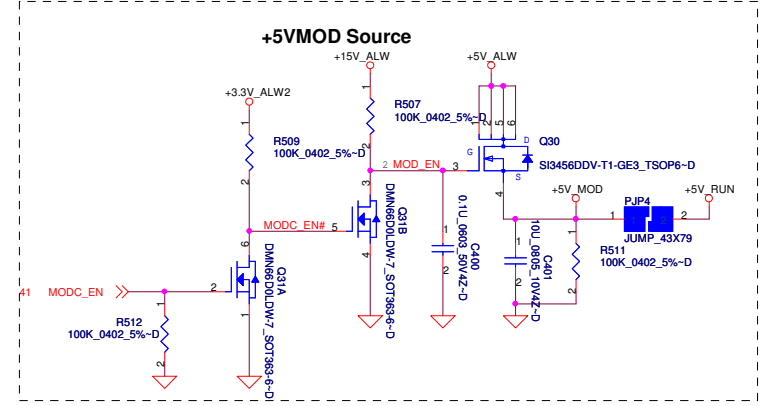
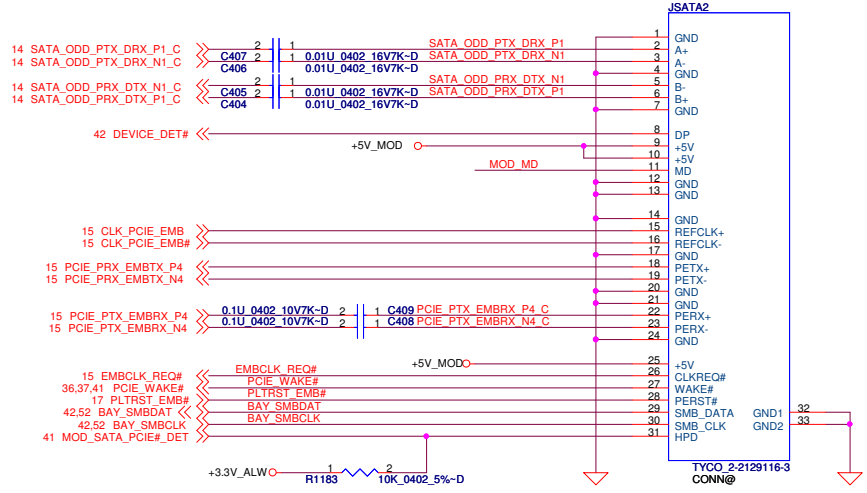
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<b>HDD CONNECTOR</b>		
Size	Document Number	Rev
	<b>LA-6592P</b>	1.0
Date:	Thursday, January 13, 2011	Sheet 28 of 75



**For ODD**



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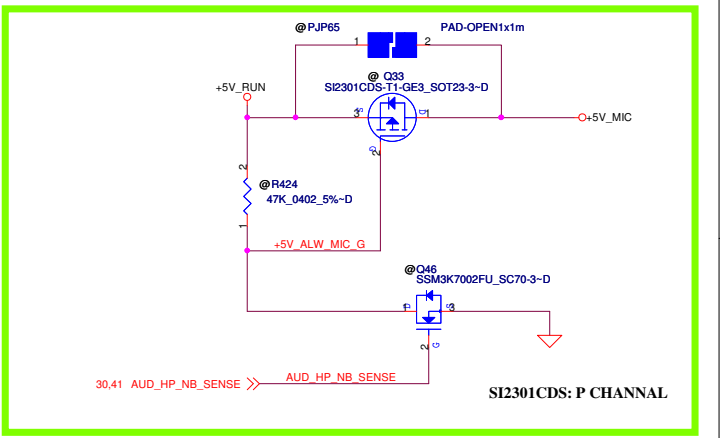
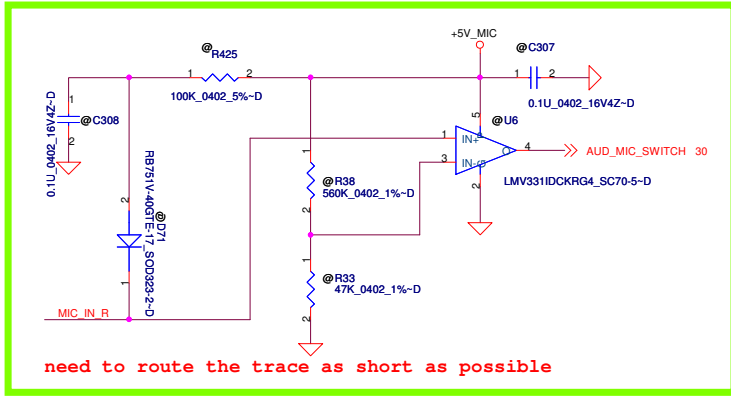
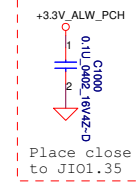
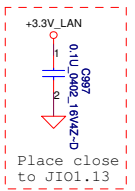
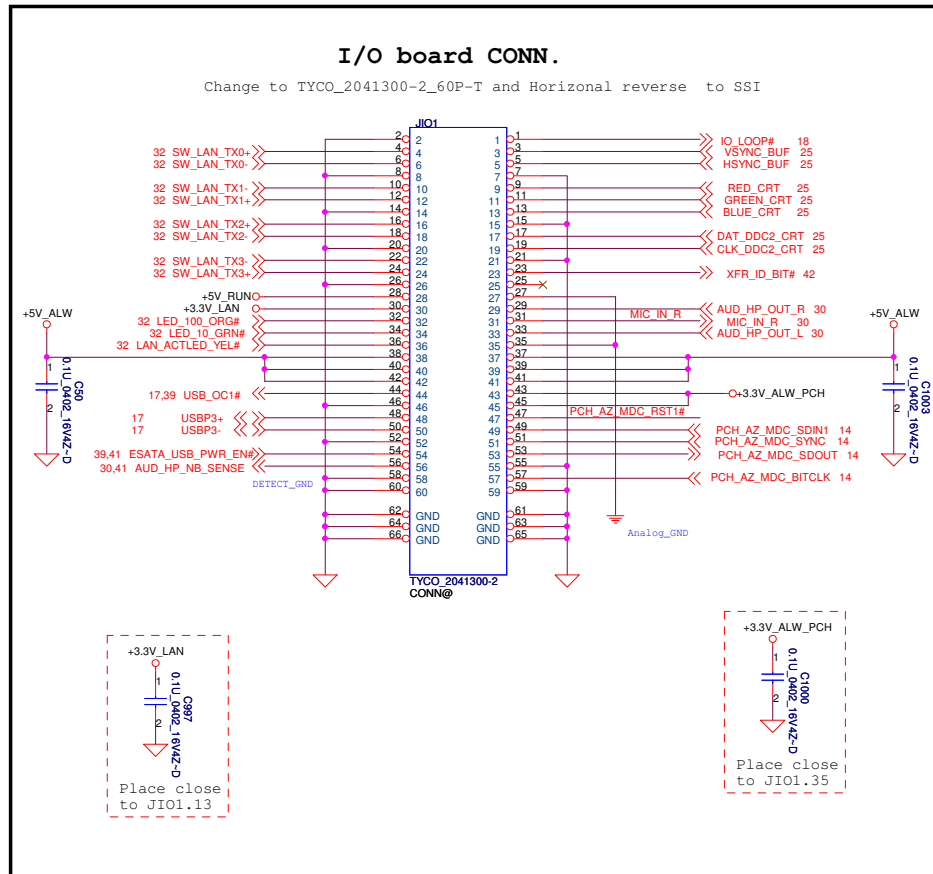
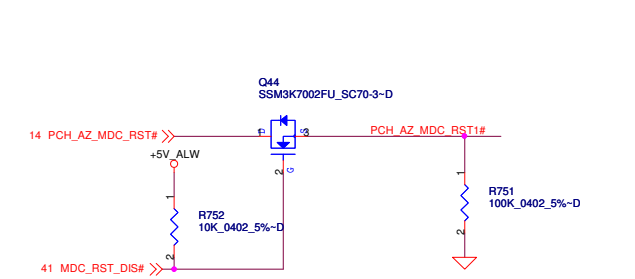
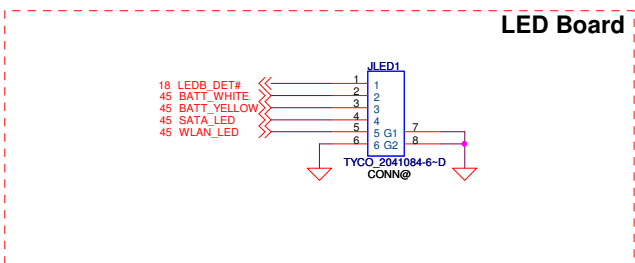
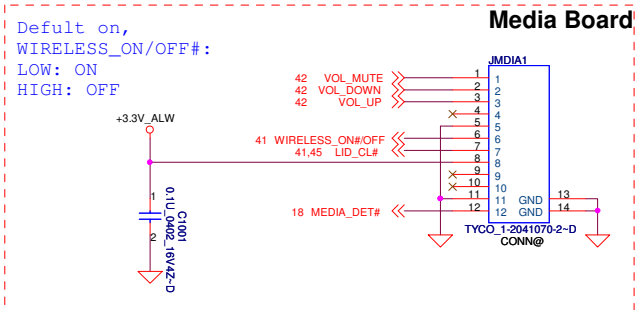
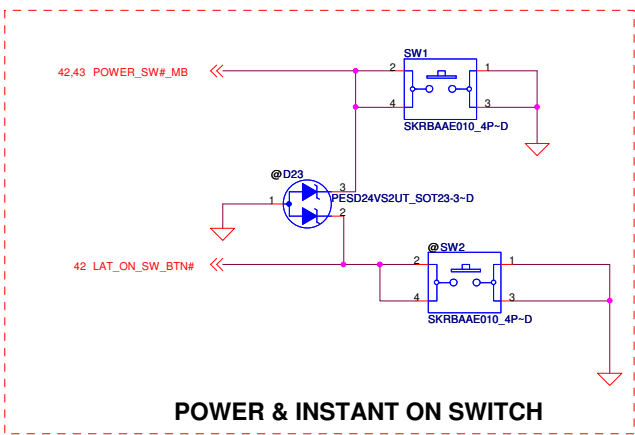
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Title			
ODD CONNECTOR			
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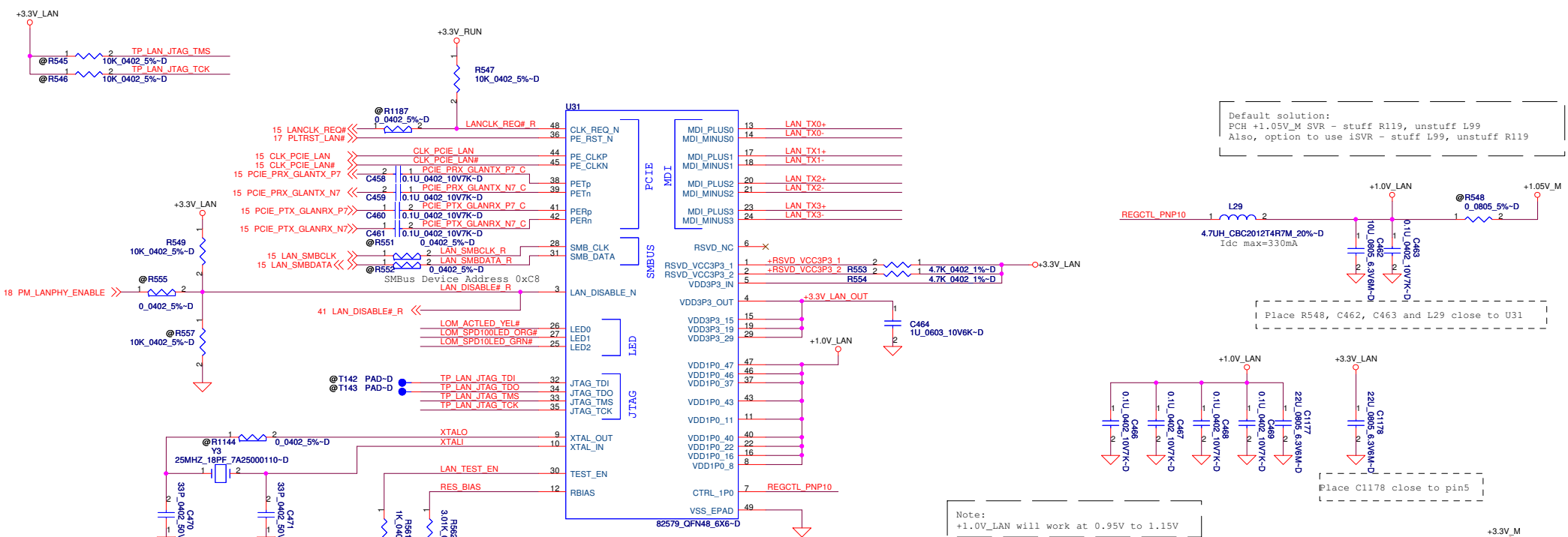


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Compal Electronics, Inc.			
Title <b>PWR SW/Sub-board Connector</b>			
Size	Document Number	Rev 1.0	
LA-6592P			
Date:	Thursday, January 13, 2011	Sheet	31 of 75

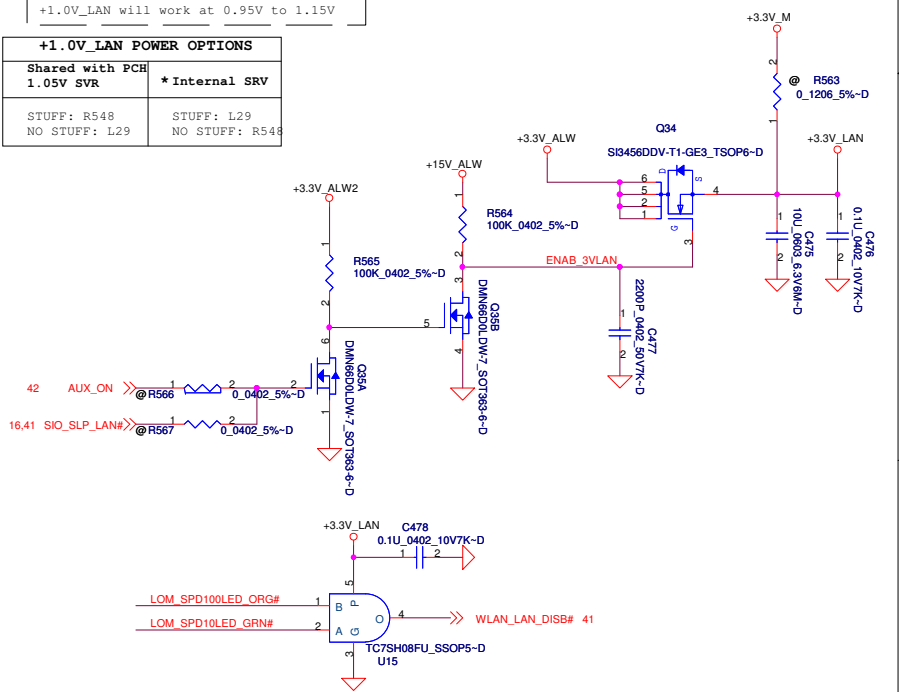
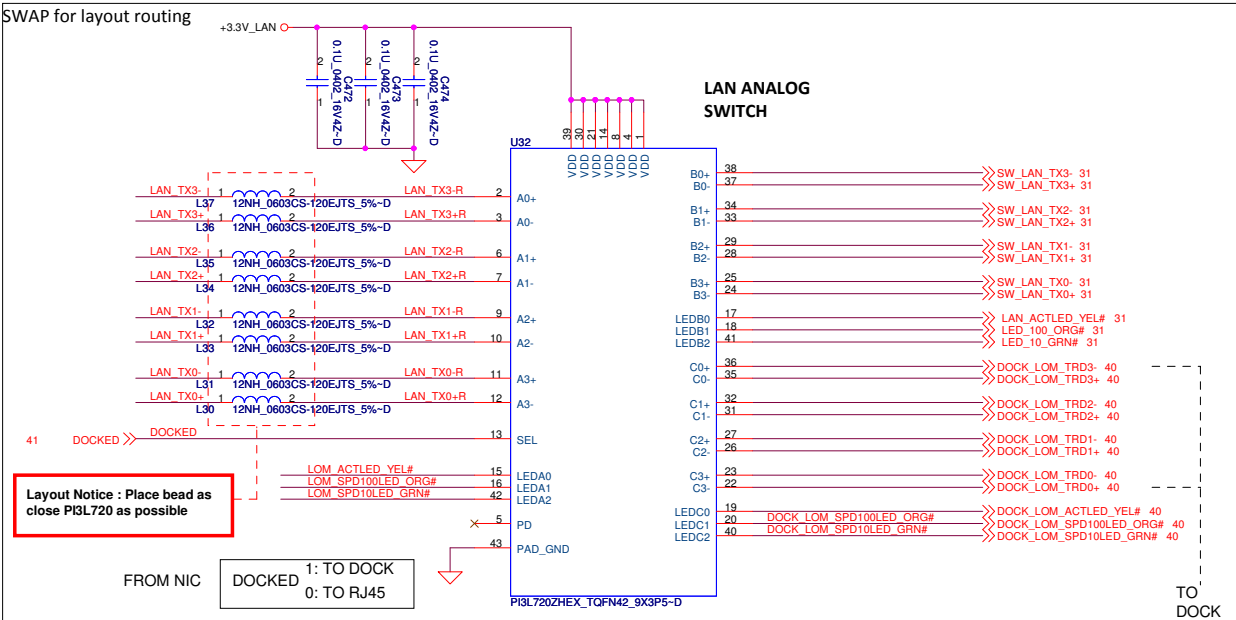
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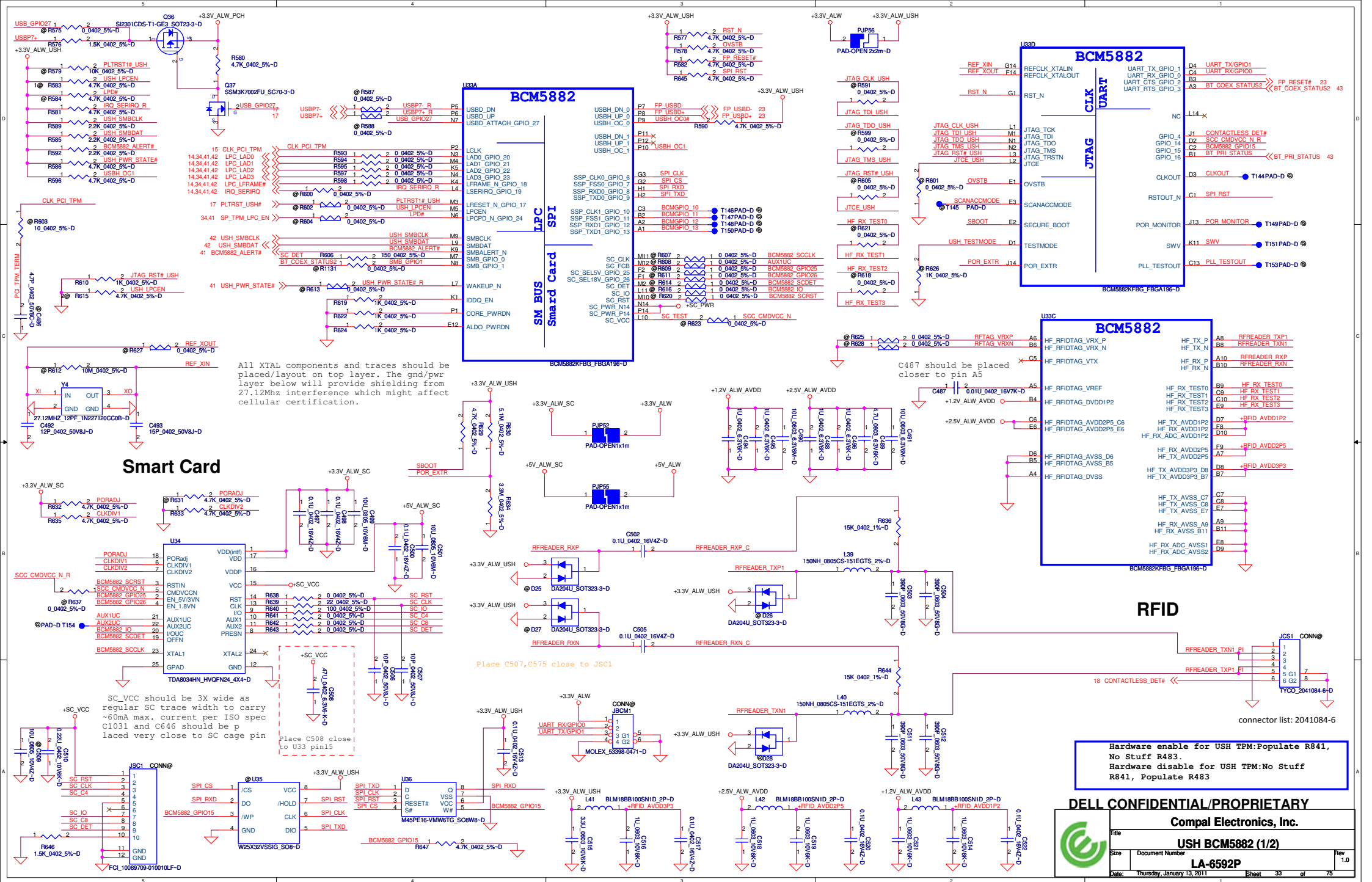
Need to verify A3 silicon drive power before removing C427  
KDS crystal vender verify driving level in A3

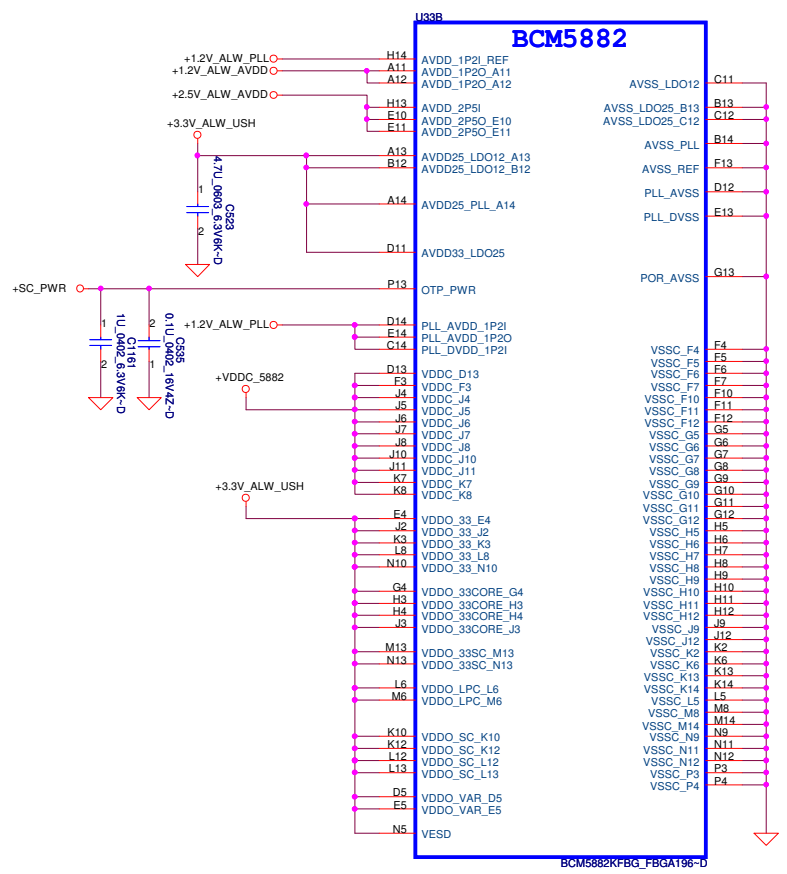
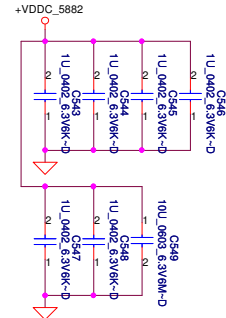
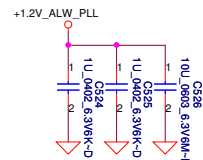
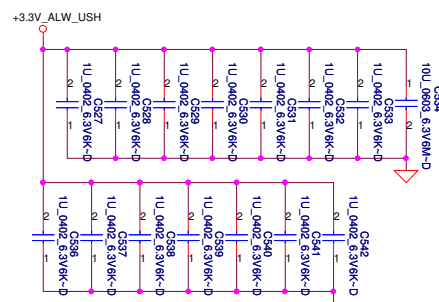
R1200 Resistor Value:  
3.01 kohm for Hanksville-M LOM  
2.37 kohm for Hanksville-D LOM

+1.0V_LAN POWER OPTIONS	
Shared with PCH 1.05V SVR	* Internal SRV
STUFF: R548	STUFF: L29
NO STUFF: L29	NO STUFF: R548



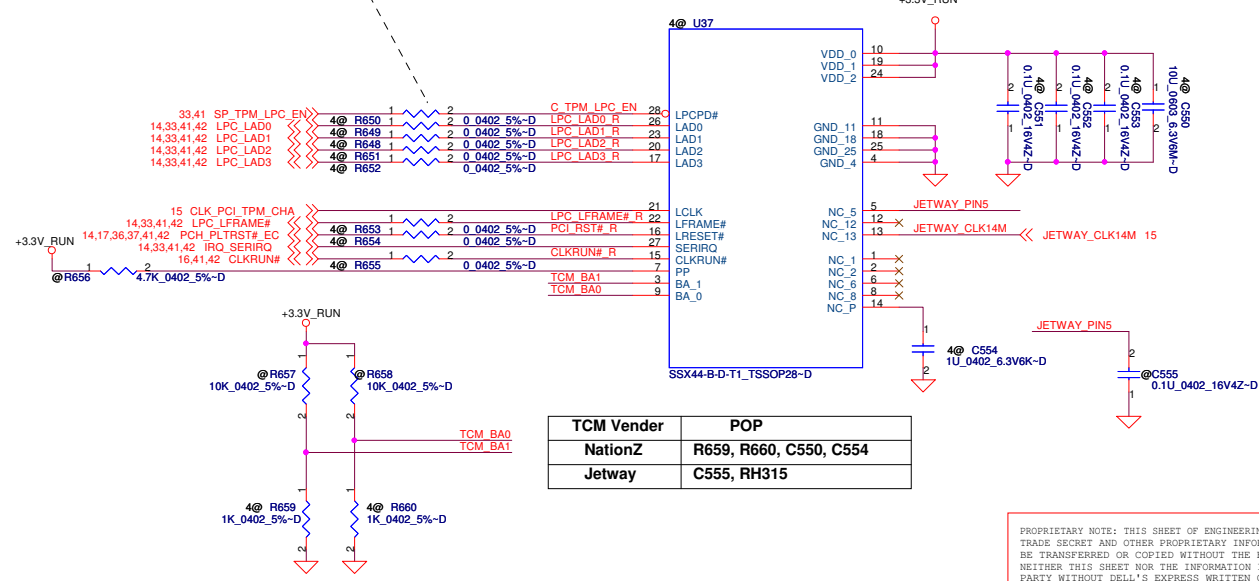






LOW: Power Down Mode  
High: Working Mode

### China TCM: NationZ & Jetway co-lay



TCM Vender	POP
NationZ	R659, R660, C550, C554
Jetway	C555, RH315

USH BCM5882 and China TCM Z8H172T Option				
PART/PIN	Ref Des	TCM Enable	TPM Enable	ALL TPM/TCM Disable
TCM circuit	All 4@	POP	@	@
USH_LPCEN	PU R583 PD R615	@ POP	POP @	@ @
SIO 5028 ->SP_TPM_LPC_EN	PU R772	@	@	@
PCH GPIO39 ->TPM_ID1	PU RH268 PD RH271	@ POP	POP @	POP @
PCH GPIO38 ->TPM_ID0	PU RH267 PD RH270	@ POP	POP @	POP POP

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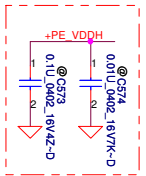
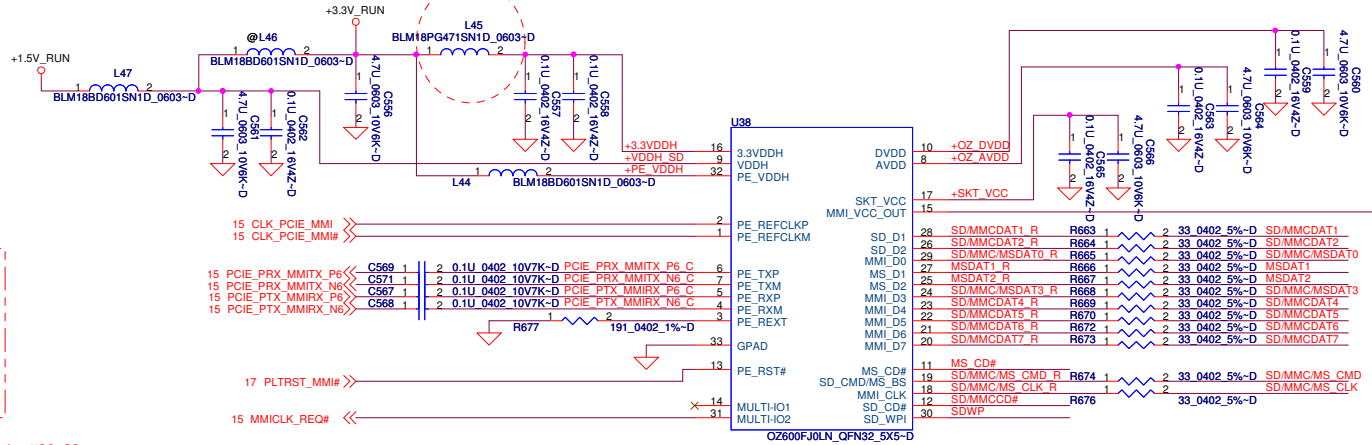
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Title			USH BCM5882 (2/2)		
Size	Document Number	Rev			1.0
Date: Thursday, January 13, 2011		Sheet: 34		of 75	

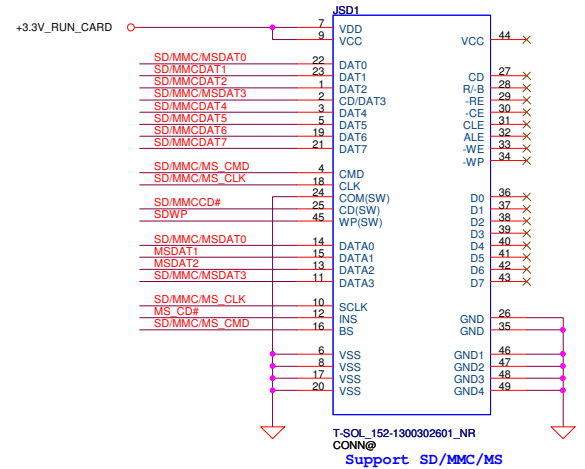
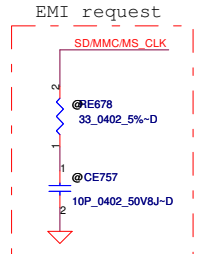
LA-6592P

need to apply CIS symbol.



place close to pin U38.32

Note: The trace need to route as daisy-chain and the trace of SD signals need to route as short as possible



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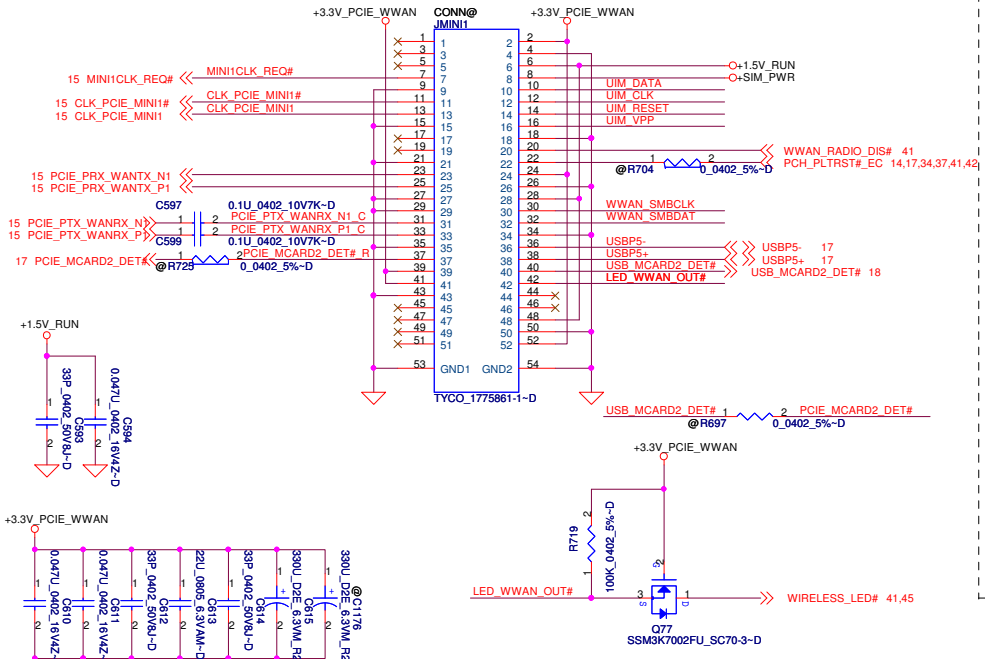


Title			Card Reader OZ600FJ0		
Size			Document Number		
Date			Thursday, January 13, 2011		
Sheet			35 of 75		
Rev			1.0		

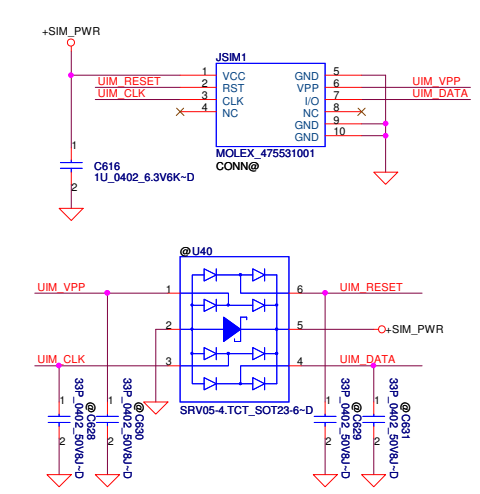
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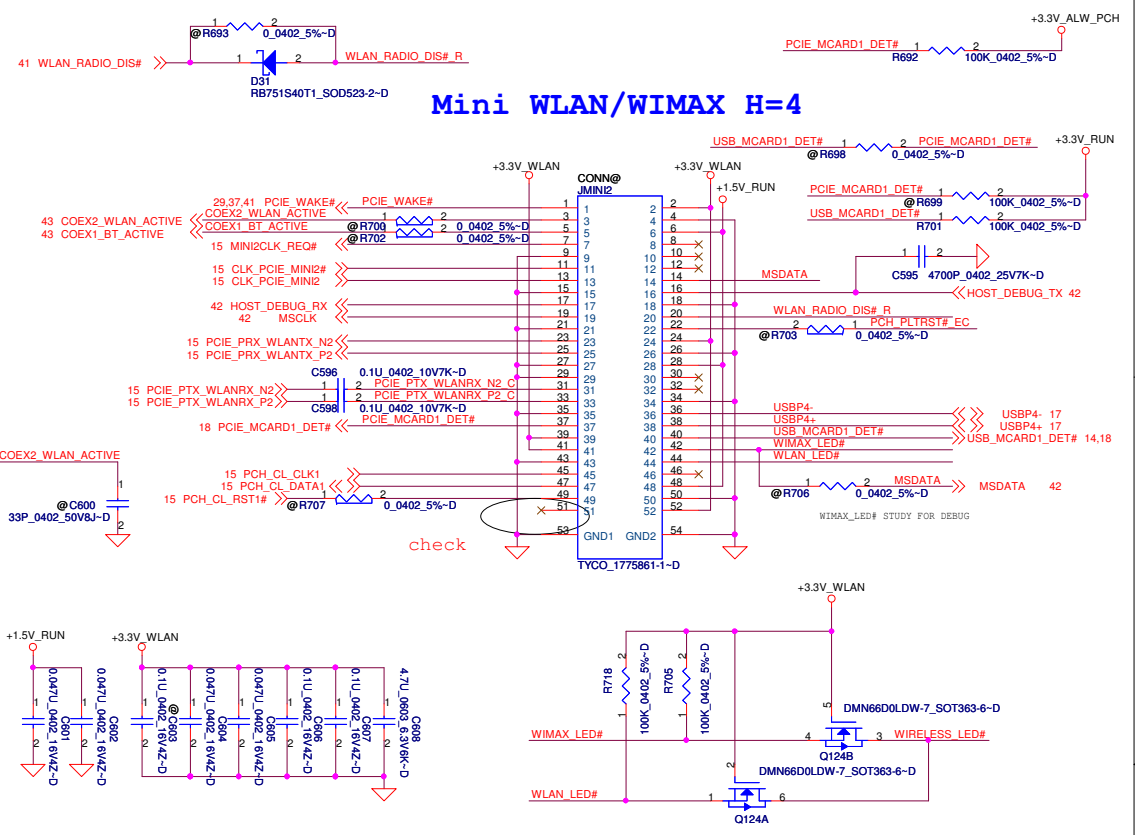
### Mini WWAN/GPS/LTE/UWB H=5.2



### SIM Card Push-Push

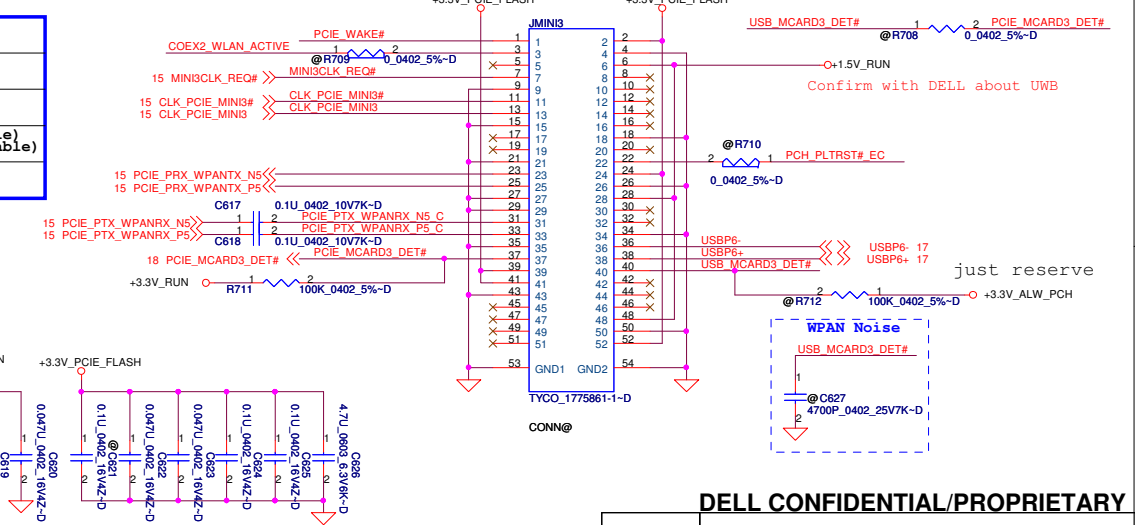


PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+9%	1000	750	
+3.3Vaux	+9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+5%	500	375	NA



### Mini WLAN/WIMAX H=4

### 1/2 Minicard Flash Card H=4

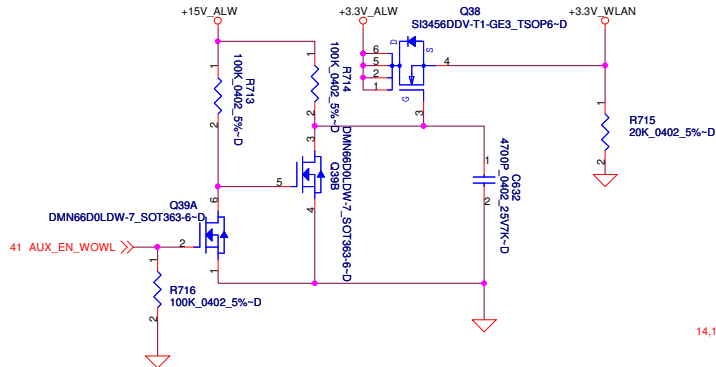


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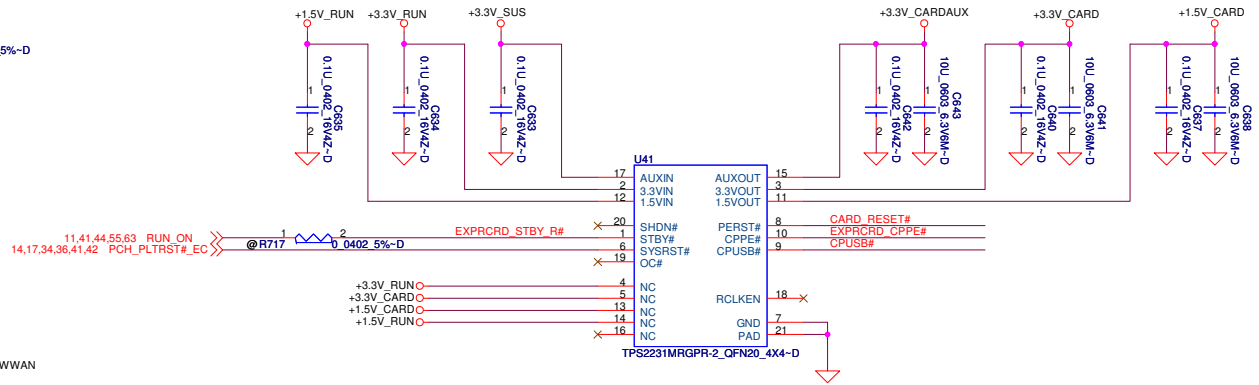
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Title: **Mini Card**  
 Size: **LA-6592P**  
 Date: Thursday, January 13, 2011 Sheet 36 of 75

### Power Control for Mini card2

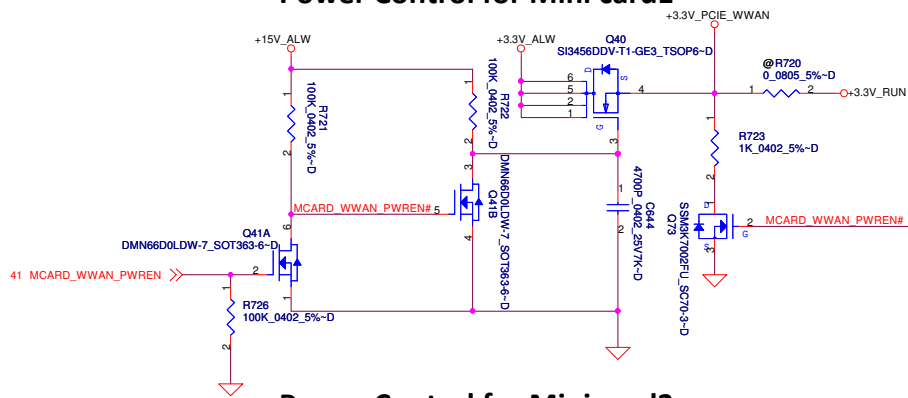


### Express Card PWR S/W

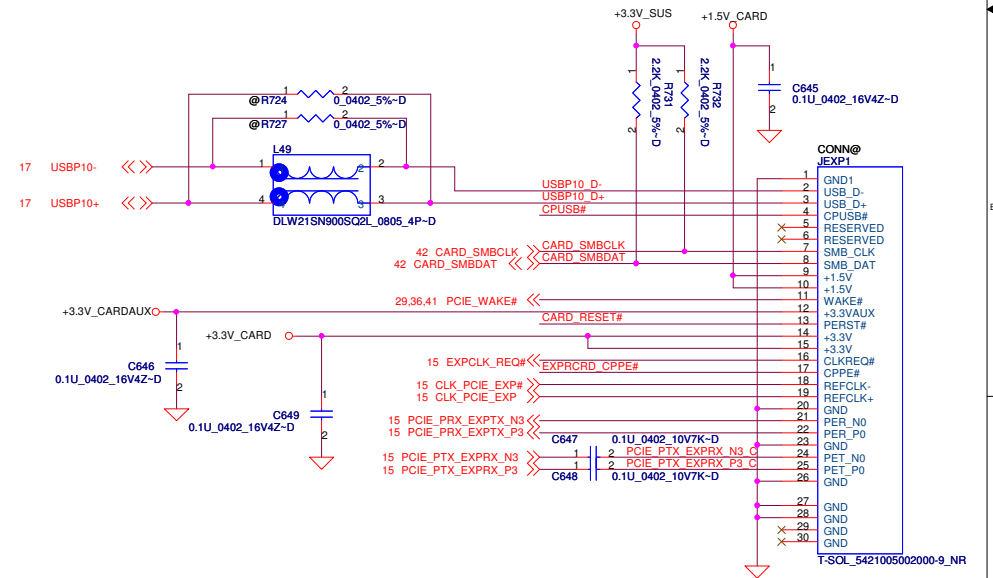


[ Note: Add connection on pin4, pin5, pin13 and pin14 to support GMT 2nd source part ]

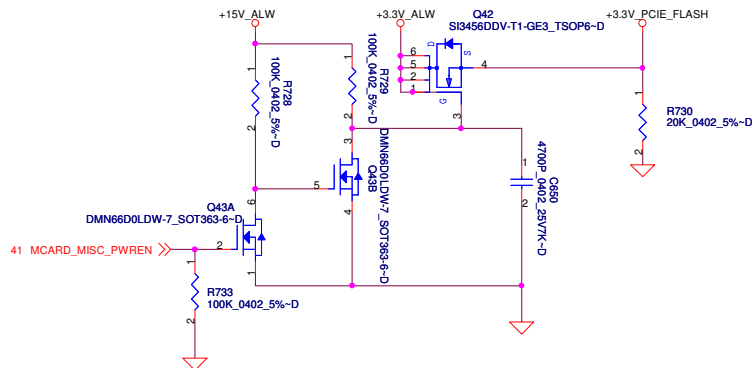
### Power Control for Mini card1



### Express Card Conn.



### Power Control for Mini card3



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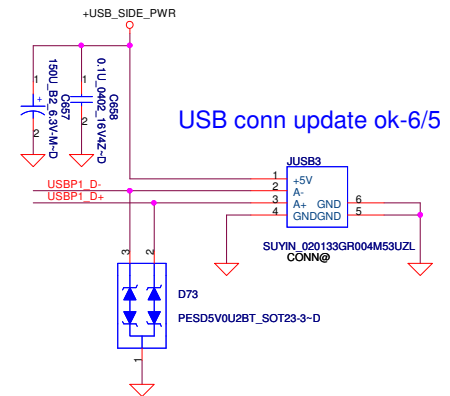
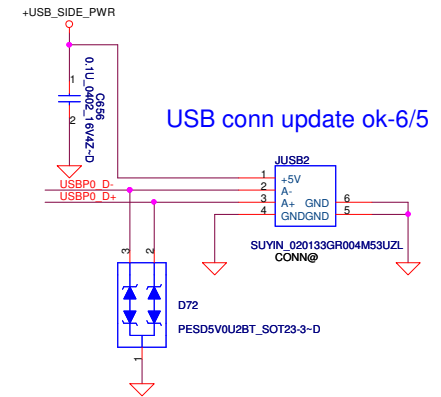
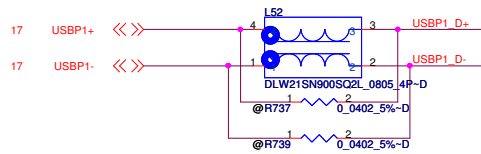
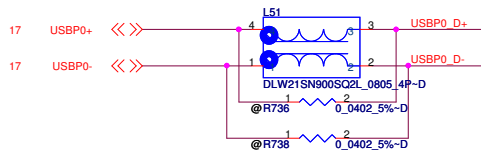
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Title: **PCIe-SATA SW / PCIe PWR**

Size: Document Number **LA-6592P** Rev 1.0

Date: Tuesday, January 18, 2011 Sheet 37 of 75

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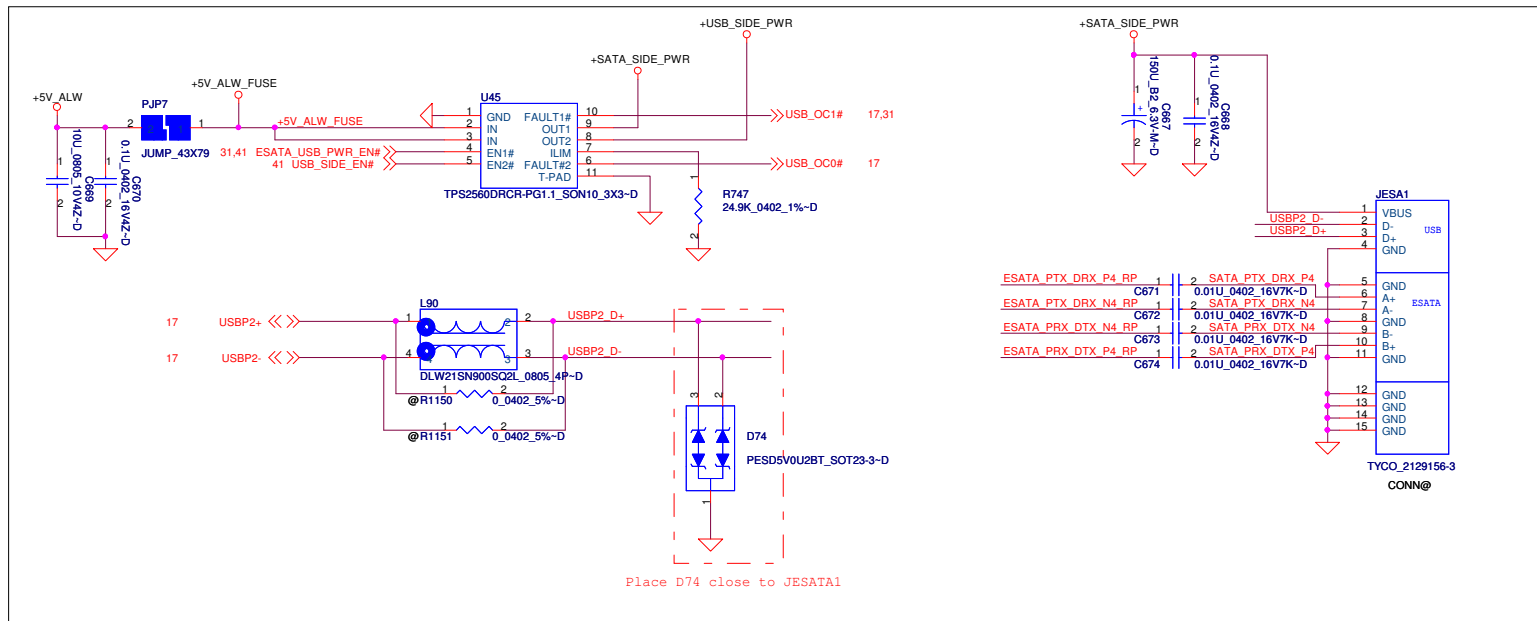
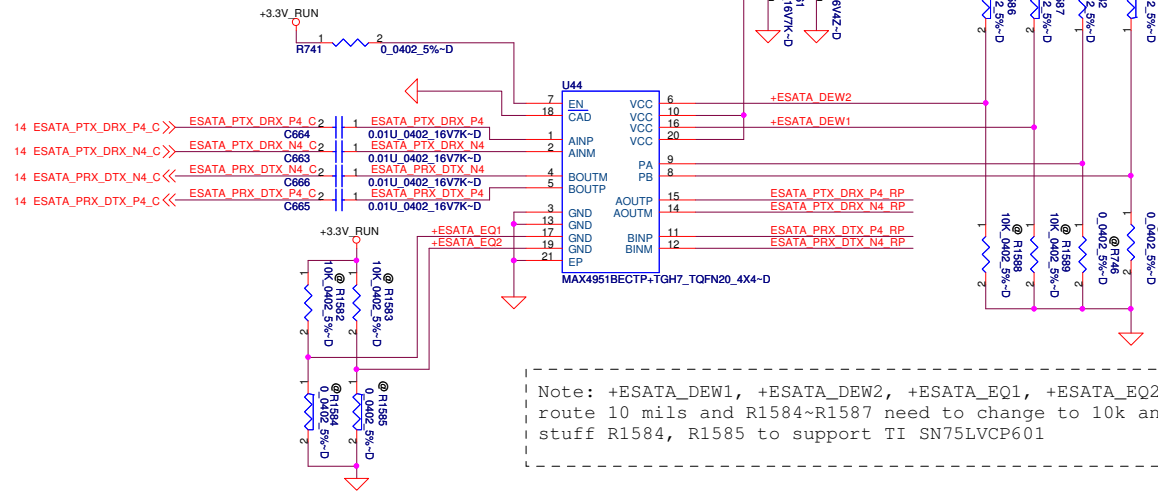


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Title			USB x2	
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# ESATA Repeater



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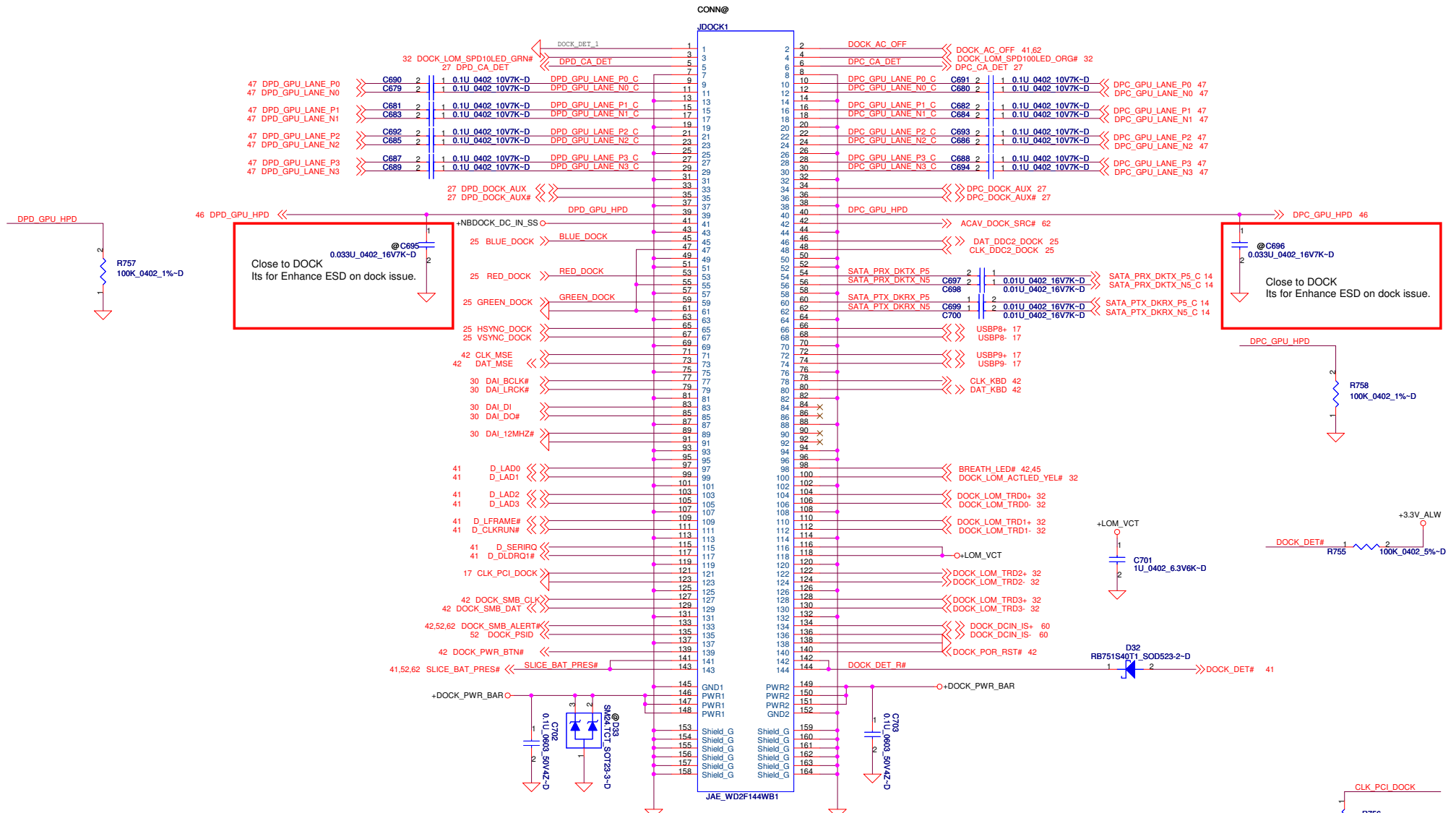
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**USB/ESATA/IO/MDC**

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Date: Tuesday, January 18, 2011 Sheet 39 of 75

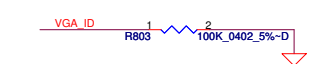
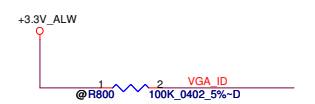
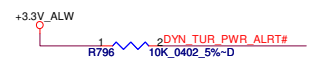
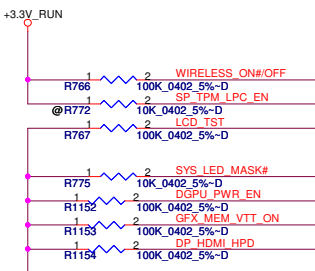
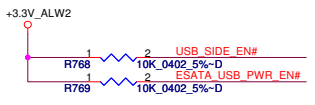
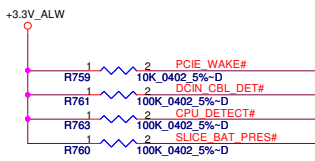


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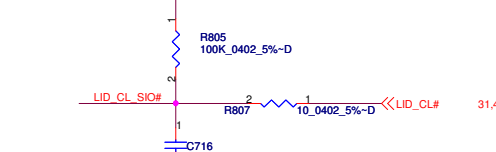
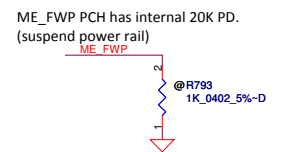
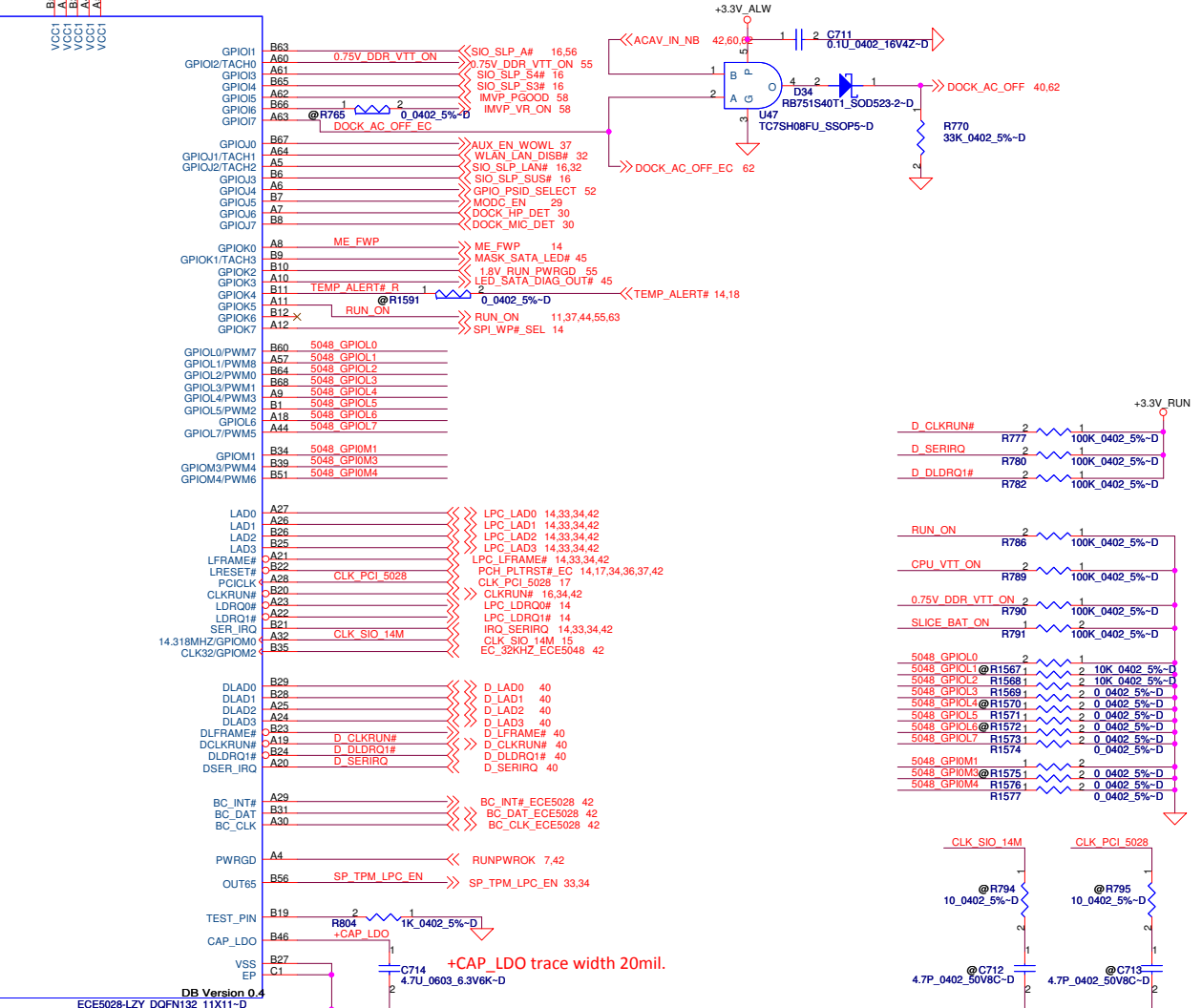
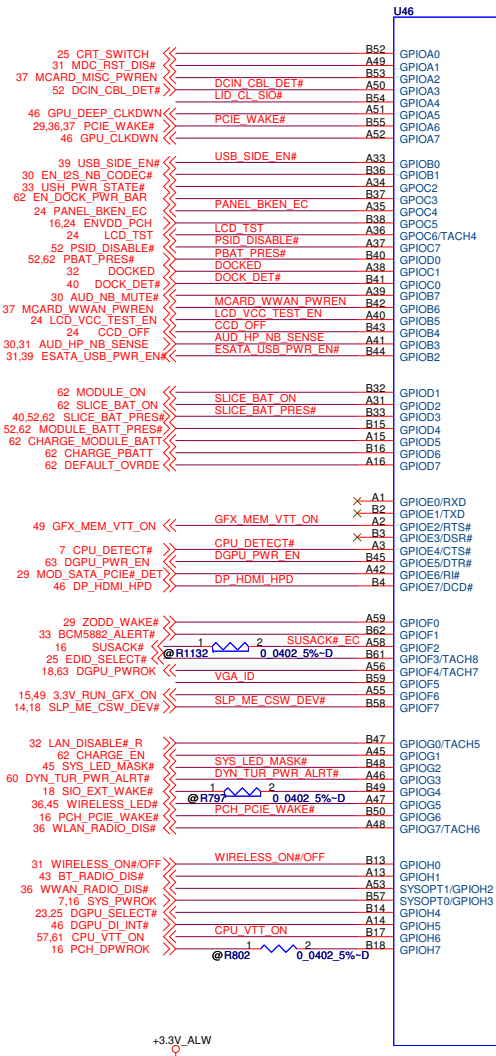
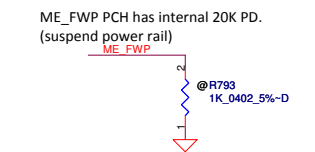
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<b>DOCKING CONN</b>			
<b>LA-6592P</b>			
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	VGA_ID
Discrete	0
UMA	1



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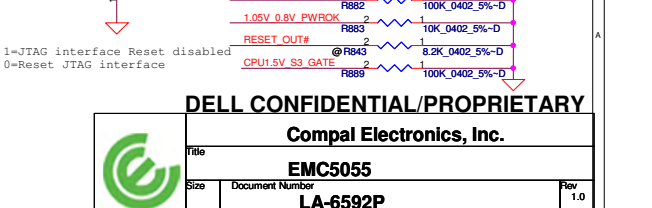
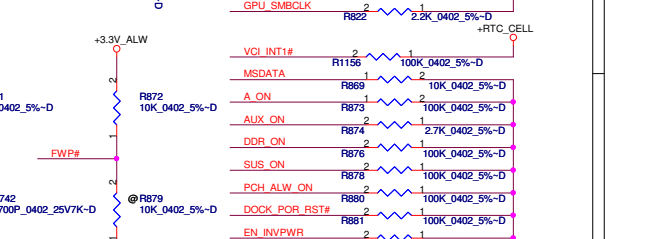
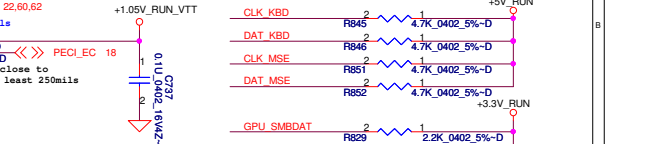
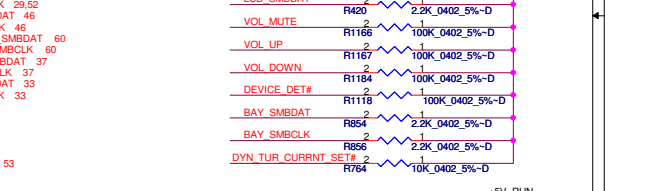
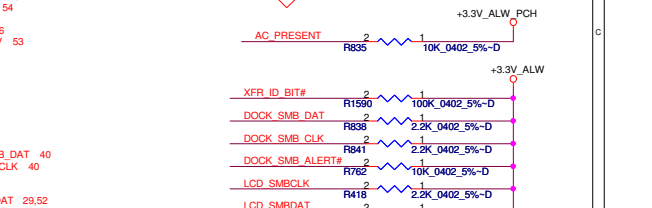
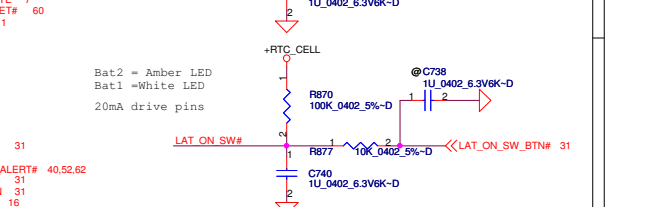
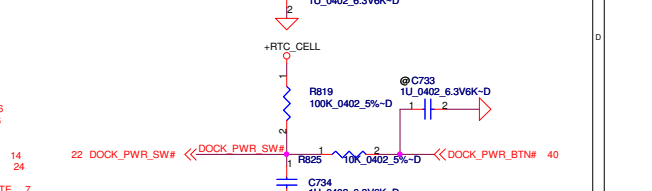
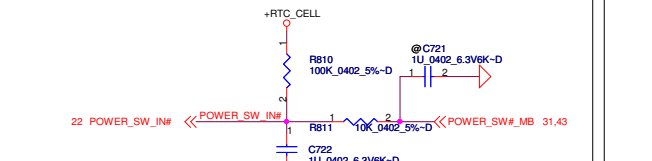
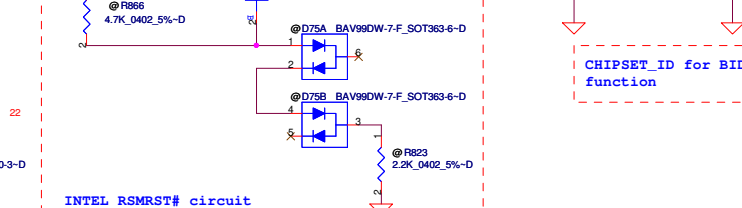
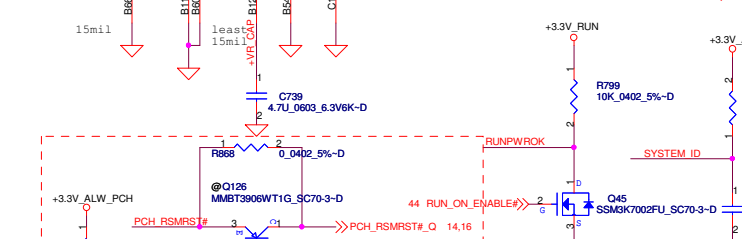
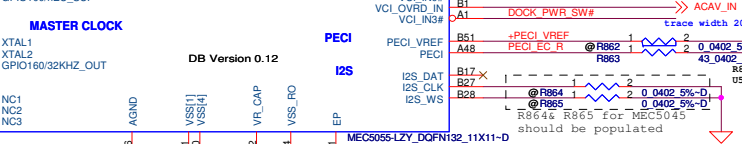
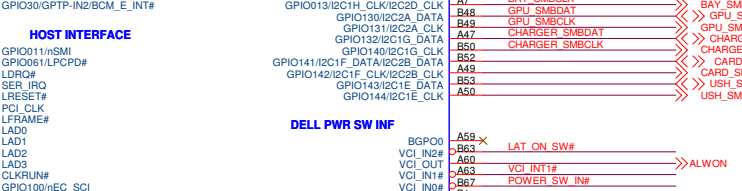
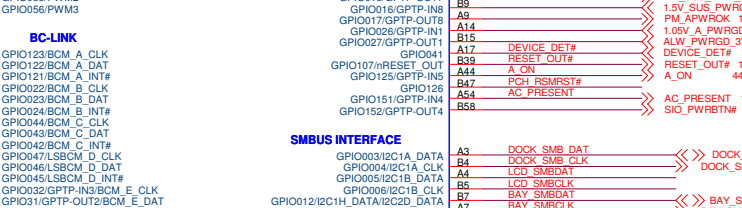
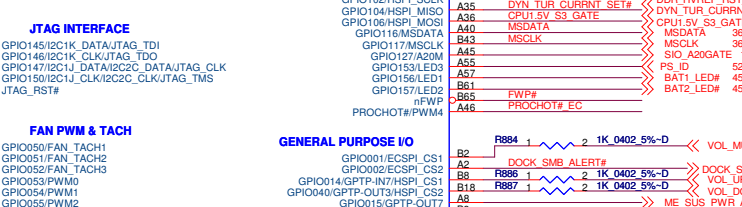
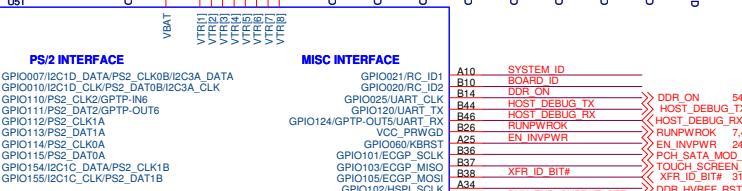
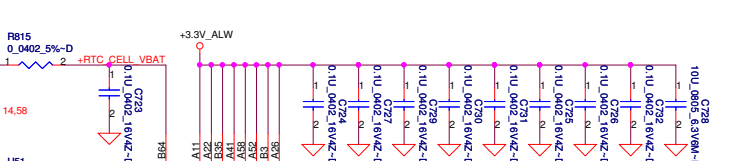
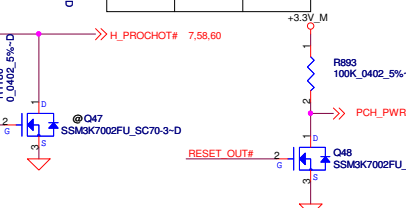
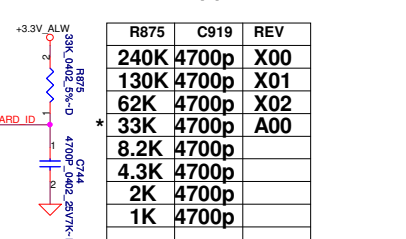
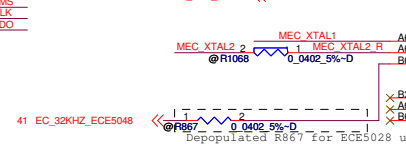
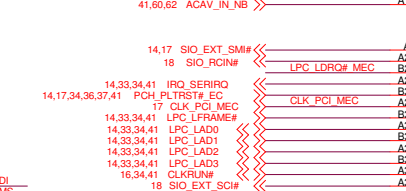
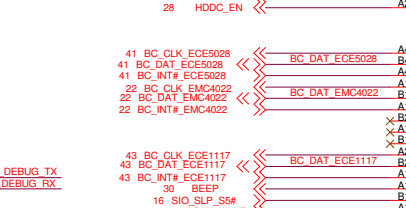
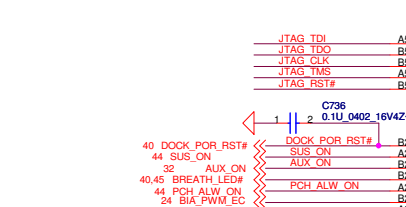
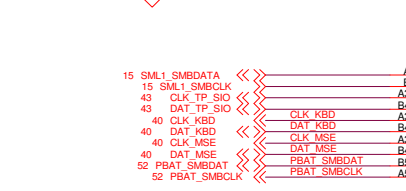
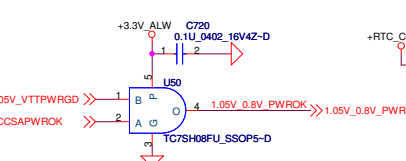
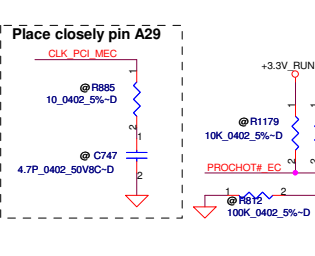
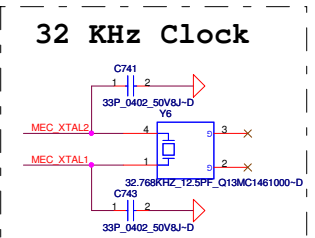
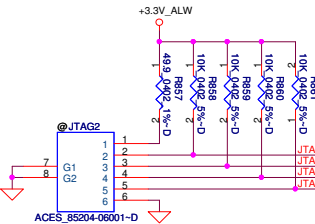
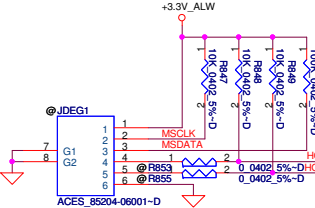
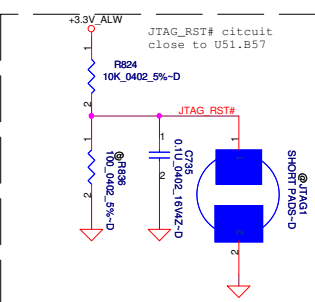
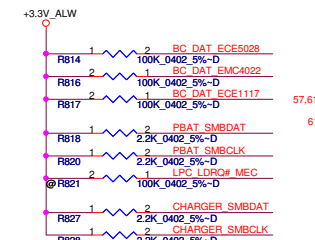
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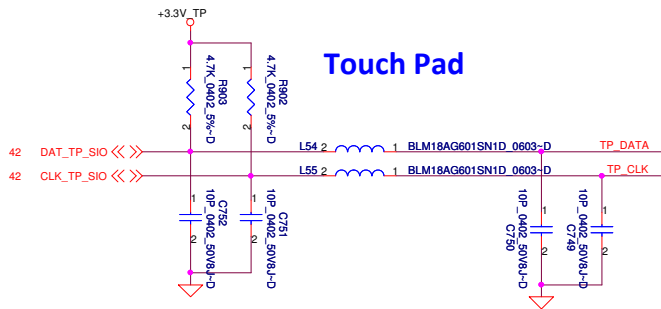
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Size: **LA-6592P**

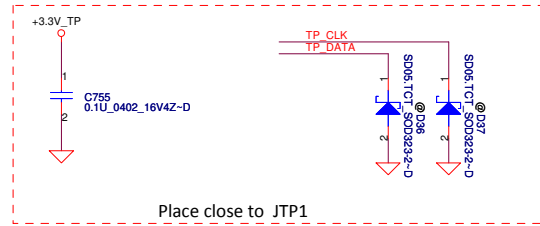
Date: Thursday, January 13, 2011 Sheet 41 of 75 Rev 1.0



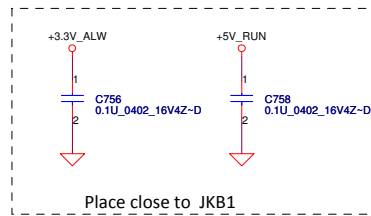
R875	C919	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	A00
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	



### Touch Pad



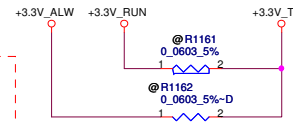
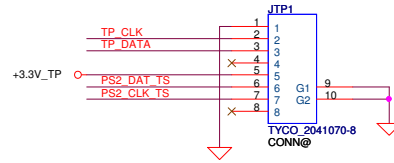
Place close to JTP1



Place close to JKB1

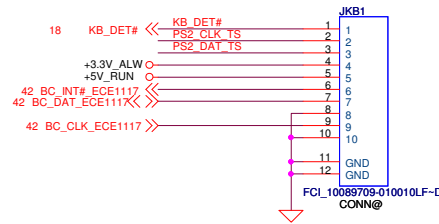
Pin reverse for PT

### Touch Pad Conn. Pitch=0.5mm



Change KB connector to same as JSC1

### KB Conn. Pitch=1.0mm



#### @LVDS cable

Part Number	Description
DC020003Y0L	H-COON SET 2LX MB-LCD 14 WXGA(+1ch)

#### @RTC BATT

Part Number	Description
GC20323M000	BATT CR2032 3V 220MAH MAXELL

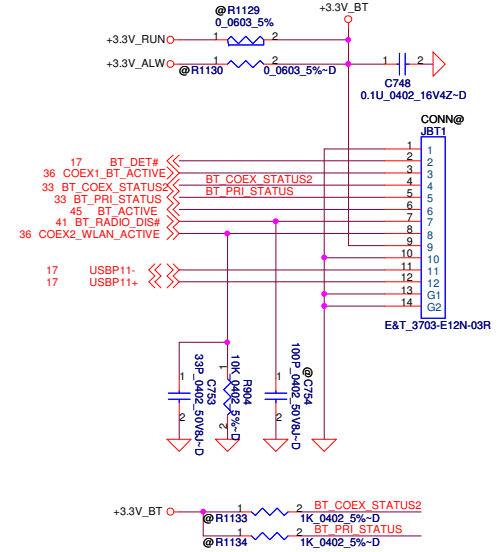
#### @FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

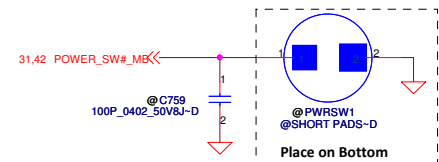
#### @Speak

Part Number	Description
PK230003Q0L	SPK PACK 2LX 2.0W 4 OHM FG

### BlueTooth



### Power Switch for debug



Place on Bottom

#### @LED Board FFC

Part Number	Description
NBX0000RFP0L	FFC 6P H P1 PAD=0.7 87.4MM MB-LED/B OFD

#### @MEDIA Board FFC

Part Number	Description
NBX0000RS0L	FFC 12P G P.5 PAD.3 75MM MB-VOLUME/B OFD

#### @LVDS cable

Part Number	Description
DC02C00180L	H-COON SET OFD MB-LCD CAM LED 2CHANNEL

#### @SG DC IN wire cable

Part Number	Description
DC30100B00L	CONN SET OFE DCJACK-MB WDM-DCE30002-DF

#### @Battery bridge cable

Part Number	Description
DC020014210	H-COON SET OFD M/B-BATTERY 9PIN

#### @MDC wire set cable

Part Number	Description
DC30100BL0L	CONN SET OFD MDC-RJ11

#### @T/P FFC

Part Number	Description
NBX0000RR0L	FFC 8P F P0.5 PAD=0.3 136MM MB-TP/B OFD

#### @KB FFC

Part Number	Description
SP070007V0L	S SOCKET TYCO 1770551-1 10P H5.9 SMART

#### @BT wire cable

Part Number	Description
DC020014Y0L	H-COON SET OFD MB-BT

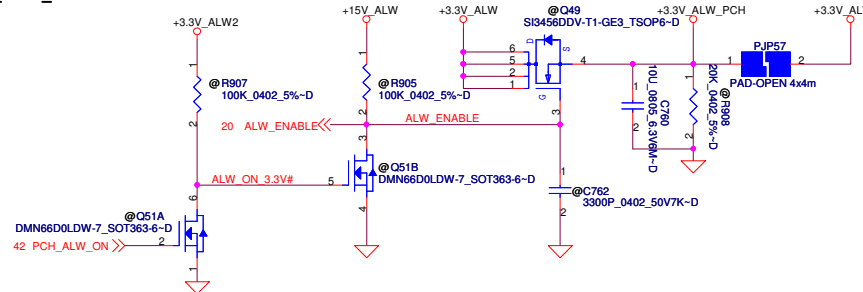
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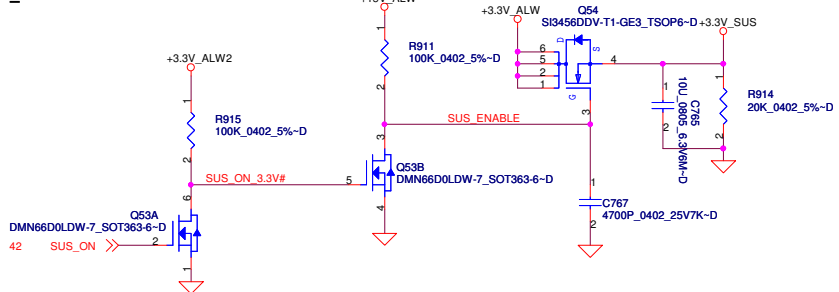
Title			
Touch Pad/Int KB/BT			
Size	Document Number	Rev	
	LA-6592P	1.0	
Date:	Thursday, January 13, 2011	Sheet	43 of 75

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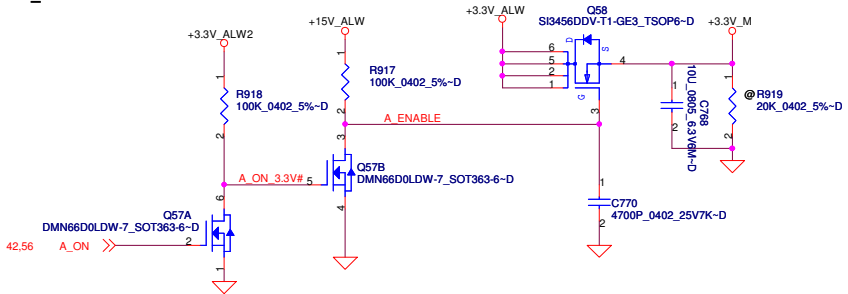
**+3.3V\_ALW\_PCH Source**



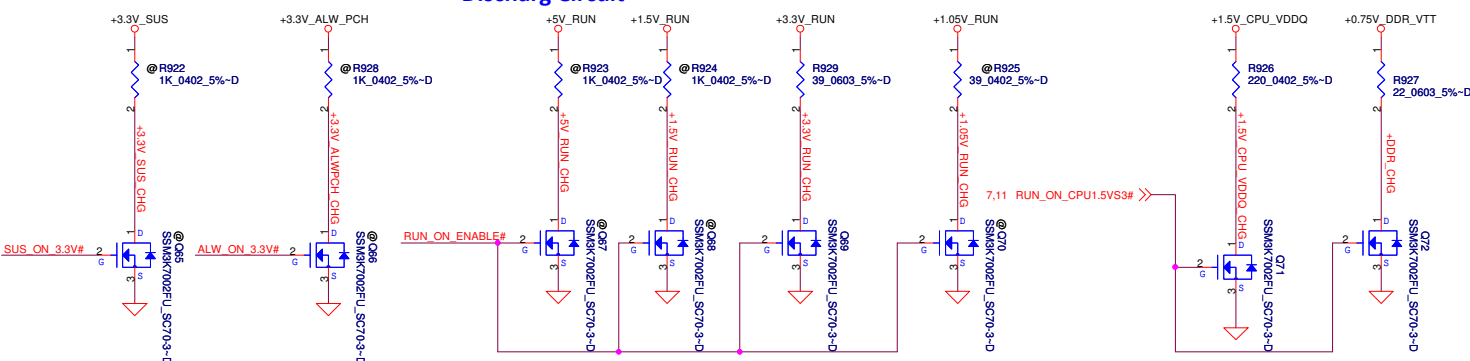
**+3.3V\_SUS Source**



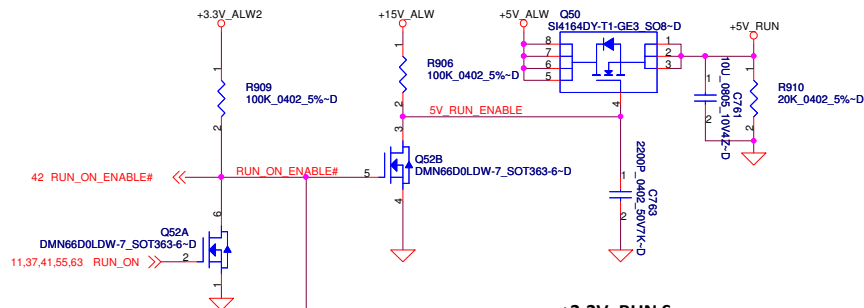
**+3.3V\_M Source**



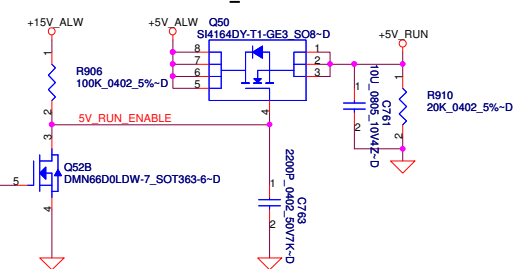
**Discharg Circuit**



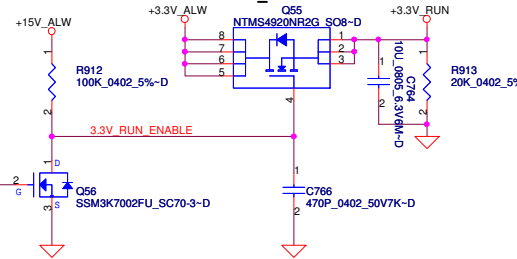
**DC/DC Interface**



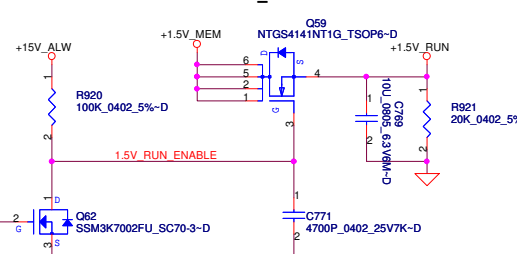
**+5V\_RUN Source**



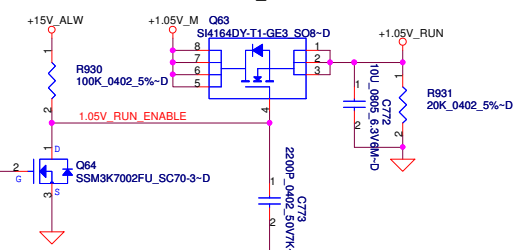
**+3.3V\_RUN Source**



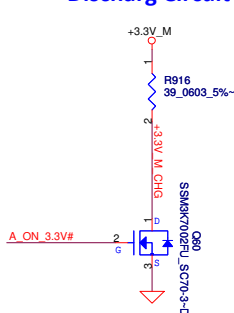
**+1.5V\_RUN Source**



**+1.05V\_RUN Source**



**Discharg Circuit**



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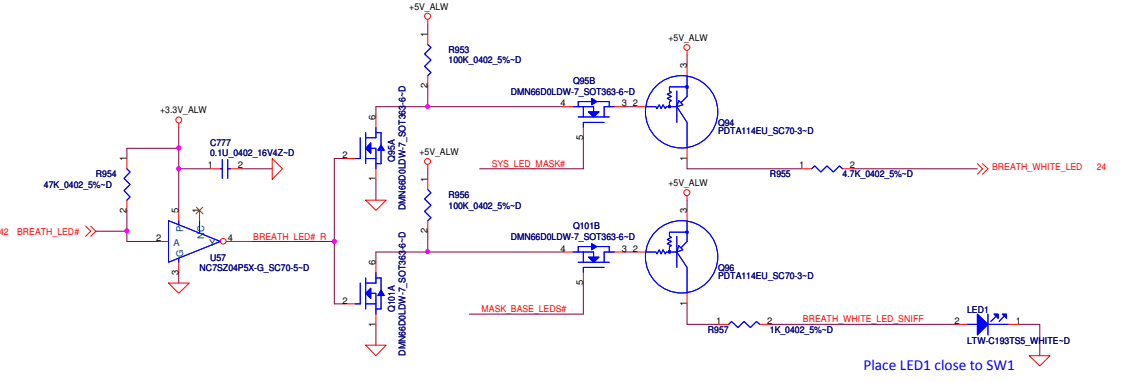
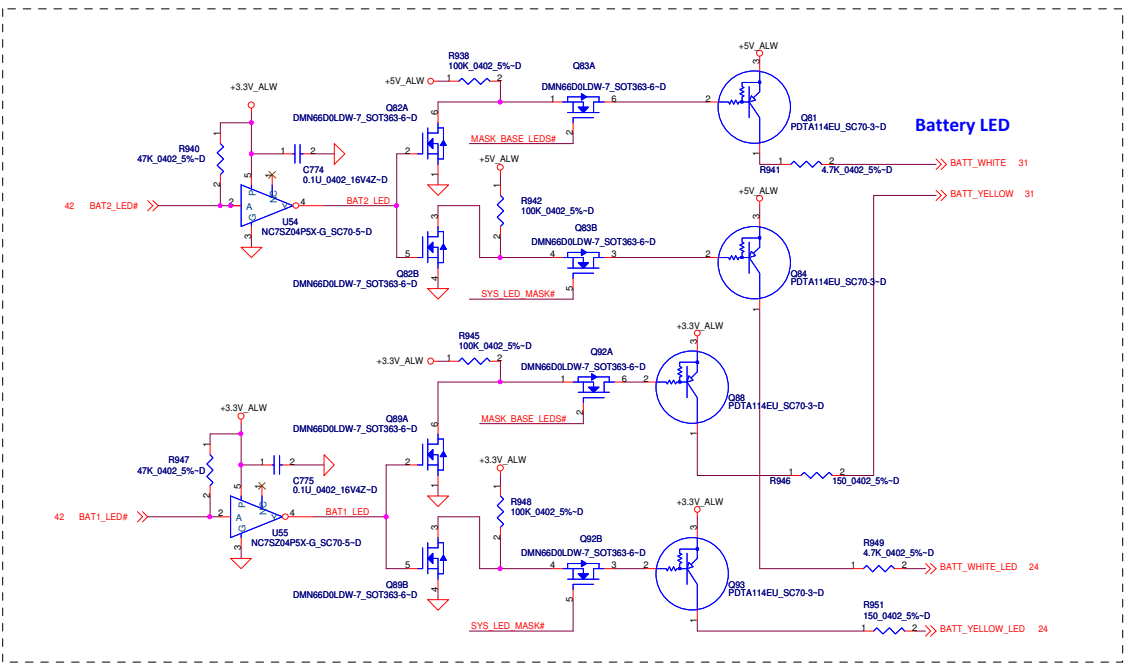
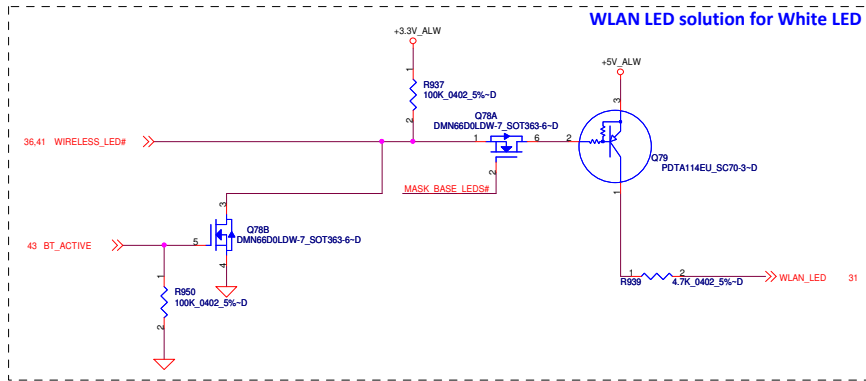
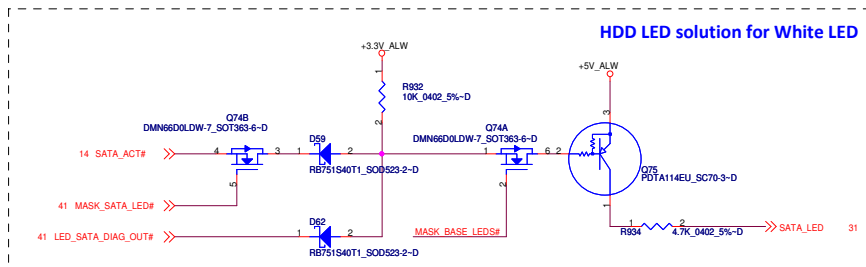
**Compal Electronics, Inc.**

**POWER CONTROL**

**LA-6592P**

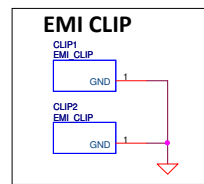
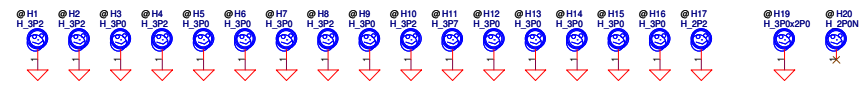
Size	Document Number	Rev
	LA-6592P	1.0
Date:	Thursday, January 13, 2011	Sheet 44 of 75

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- Fiducial Mark**
- FD1
  - FIDUCIAL MARK-D
  - FD2
  - FIDUCIAL MARK-D
  - FD3
  - FIDUCIAL MARK-D
  - FD4
  - FIDUCIAL MARK-D

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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**PAD and Standoff**

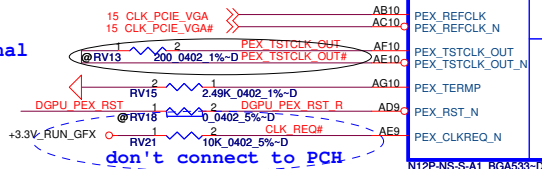
LA-6592P

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- 6 PEG\_CTX\_GRX\_P0.[15] >>> PEG\_CTX\_GRX\_P0.[15]
- 6 PEG\_CTX\_GRX\_N0.[15] >>> PEG\_CTX\_GRX\_N0.[15]
- 6 PEG\_CRX\_GTX\_P0.[15] <<< PEG\_CRX\_GTX\_P0.[15]
- 6 PEG\_CRX\_GTX\_N0.[15] <<< PEG\_CRX\_GTX\_N0.[15]

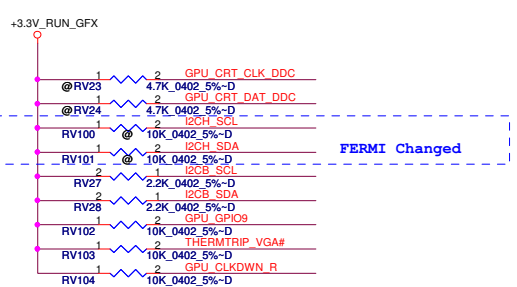
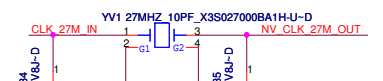
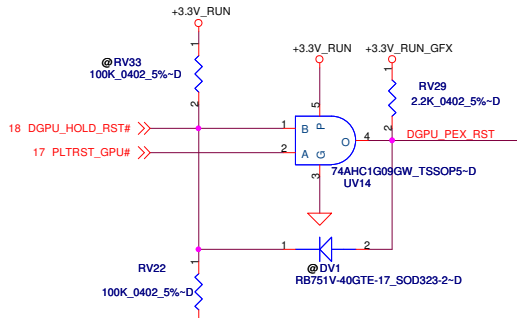
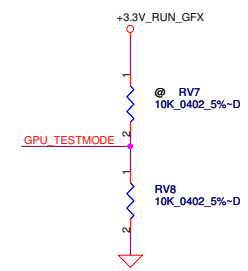
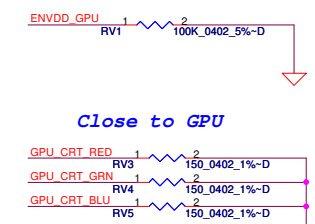
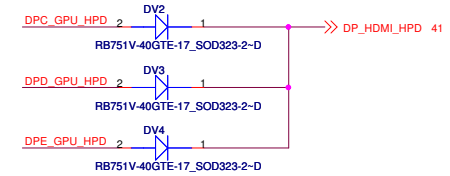
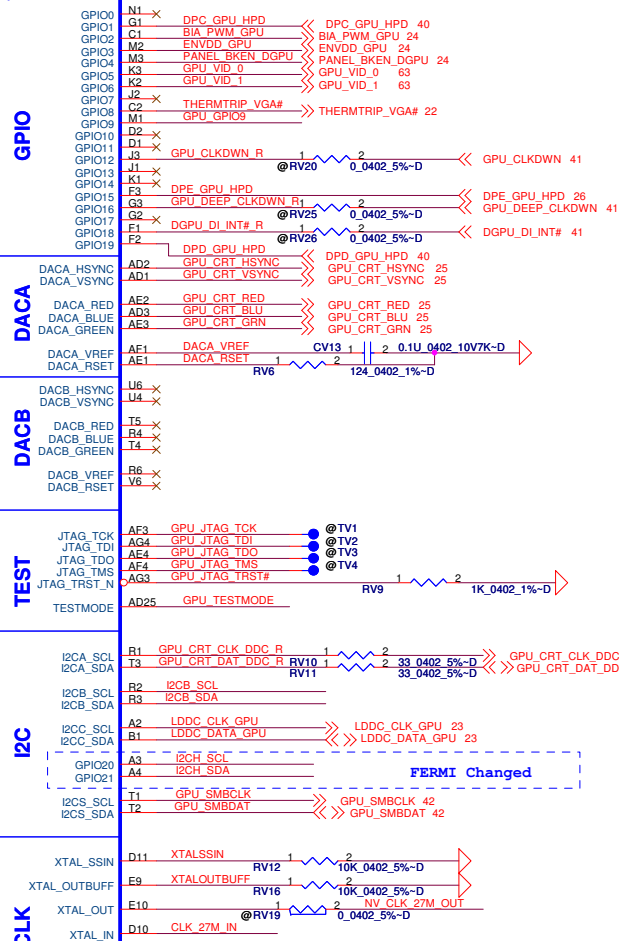
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PEG_CRX_GTX_P1	CV4	2	1	0.22u	0402	16V7K-D	PEG_CRX_GTX_C_P1
PEG_CRX_GTX_N1	CV3	2	1	0.22u	0402	16V7K-D	PEG_CRX_GTX_C_N1
PEG_CRX_GTX_P2	CV5	2	1	0.22u	0402	16V7K-D	PEG_CRX_GTX_C_P2
PEG_CRX_GTX_N2	CV6	2	1	0.22u	0402	16V7K-D	PEG_CRX_GTX_C_N2
PEG_CRX_GTX_P3	CV7	2	1	0.22u	0402	16V7K-D	PEG_CRX_GTX_C_P3
PEG_CRX_GTX_N3	CV8	2	1	0.22u	0402	16V7K-D	PEG_CRX_GTX_C_N3
PEG_CRX_GTX_P4	CV9	2	1	0.22u	0402	16V7K-D	PEG_CRX_GTX_C_P4
PEG_CRX_GTX_N4	CV10	2	1	0.22u	0402	16V7K-D	PEG_CRX_GTX_C_N4
PEG_CRX_GTX_P5	CV11	2	1	0.22u	0402	16V7K-D	PEG_CRX_GTX_C_P5
PEG_CRX_GTX_N5	CV12	2	1	0.22u	0402	16V7K-D	PEG_CRX_GTX_C_N5
PEG_CRX_GTX_P6	CV14	2	1	0.22u	0402	16V7K-D	PEG_CRX_GTX_C_P6
PEG_CRX_GTX_N6	CV15	2	1	0.22u	0402	16V7K-D	PEG_CRX_GTX_C_N6
PEG_CRX_GTX_P7	CV16	2	1	0.22u	0402	16V7K-D	PEG_CRX_GTX_C_P7
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PEG_CRX_GTX_P8	CV18	2	1	0.22u	0402	16V7K-D	PEG_CRX_GTX_C_P8
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PEG_CRX_GTX_P9	CV20	2	1	0.22u	0402	16V7K-D	PEG_CRX_GTX_C_P9
PEG_CRX_GTX_N9	CV21	2	1	0.22u	0402	16V7K-D	PEG_CRX_GTX_C_N9
PEG_CRX_GTX_P10	CV22	2	1	0.22u	0402	16V7K-D	PEG_CRX_GTX_C_P10
PEG_CRX_GTX_N10	CV23	2	1	0.22u	0402	16V7K-D	PEG_CRX_GTX_C_N10
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PEG_CRX_GTX_P14	CV30	2	1	0.22u	0402	16V7K-D	PEG_CRX_GTX_C_P14
PEG_CRX_GTX_N14	CV31	2	1	0.22u	0402	16V7K-D	PEG_CRX_GTX_C_N14
PEG_CRX_GTX_P15	CV32	2	1	0.22u	0402	16V7K-D	PEG_CRX_GTX_C_P15
PEG_CRX_GTX_N15	CV33	2	1	0.22u	0402	16V7K-D	PEG_CRX_GTX_C_N15

Differential signal



UV1A Part 1 of 5

PEG_CTX_GRX_P0	AE12	PEG_CTX_GRX_P1	AE12
PEG_CTX_GRX_N1	AG19	PEG_CTX_GRX_P2	AE13
PEG_CTX_GRX_P3	AE14	PEG_CTX_GRX_N2	AE15
PEG_CTX_GRX_N3	AF15	PEG_CTX_GRX_P4	AG15
PEG_CTX_GRX_P5	AG16	PEG_CTX_GRX_N4	AE16
PEG_CTX_GRX_N5	AE16	PEG_CTX_GRX_P6	AE18
PEG_CTX_GRX_P7	AE19	PEG_CTX_GRX_N6	AE19
PEG_CTX_GRX_N7	AG19	PEG_CTX_GRX_P8	AE19
PEG_CTX_GRX_P8	AE19	PEG_CTX_GRX_N8	AE21
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PEG_CTX_GRX_P11	AE22	PEG_CTX_GRX_N11	AE22
PEG_CTX_GRX_P12	AE24	PEG_CTX_GRX_N12	AE24
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PEG_CTX_GRX_P14	AG25	PEG_CTX_GRX_N14	AG26
PEG_CTX_GRX_P15	AE27	PEG_CTX_GRX_N15	AE27
PEG_CRX_GTX_C_P0	AD10	PEG_CRX_GTX_C_N0	AD11
PEG_CRX_GTX_C_P1	AD12	PEG_CRX_GTX_C_N1	AC12
PEG_CRX_GTX_C_P2	AB11	PEG_CRX_GTX_C_N2	AB12
PEG_CRX_GTX_C_P3	AD13	PEG_CRX_GTX_C_N3	AD14
PEG_CRX_GTX_C_P4	AD15	PEG_CRX_GTX_C_N4	AC15
PEG_CRX_GTX_C_P5	AB14	PEG_CRX_GTX_C_N5	AB15
PEG_CRX_GTX_C_P6	AC16	PEG_CRX_GTX_C_N6	AD16
PEG_CRX_GTX_C_P7	AD17	PEG_CRX_GTX_C_N7	AD18
PEG_CRX_GTX_C_P8	AC18	PEG_CRX_GTX_C_N8	AB18
PEG_CRX_GTX_C_P9	AB19	PEG_CRX_GTX_C_N9	AC20
PEG_CRX_GTX_C_P10	AD19	PEG_CRX_GTX_C_N10	AD20
PEG_CRX_GTX_C_P11	AD21	PEG_CRX_GTX_C_N11	AC21
PEG_CRX_GTX_C_P12	AB21	PEG_CRX_GTX_C_N12	AB22
PEG_CRX_GTX_C_P13	AC22	PEG_CRX_GTX_C_N13	AD22
PEG_CRX_GTX_C_P14	AD23	PEG_CRX_GTX_C_N14	AD24
PEG_CRX_GTX_C_P15	AE25	PEG_CRX_GTX_C_N15	AE26
PEG_CRX_GTX_C_N15	AE26		



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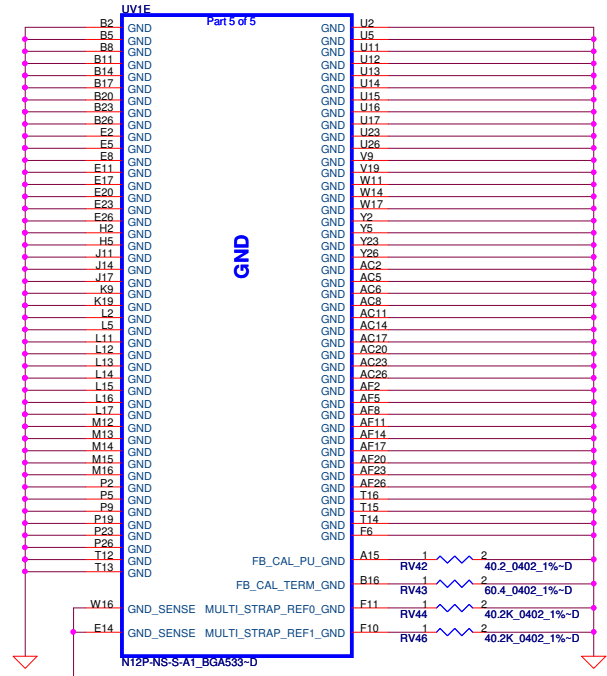
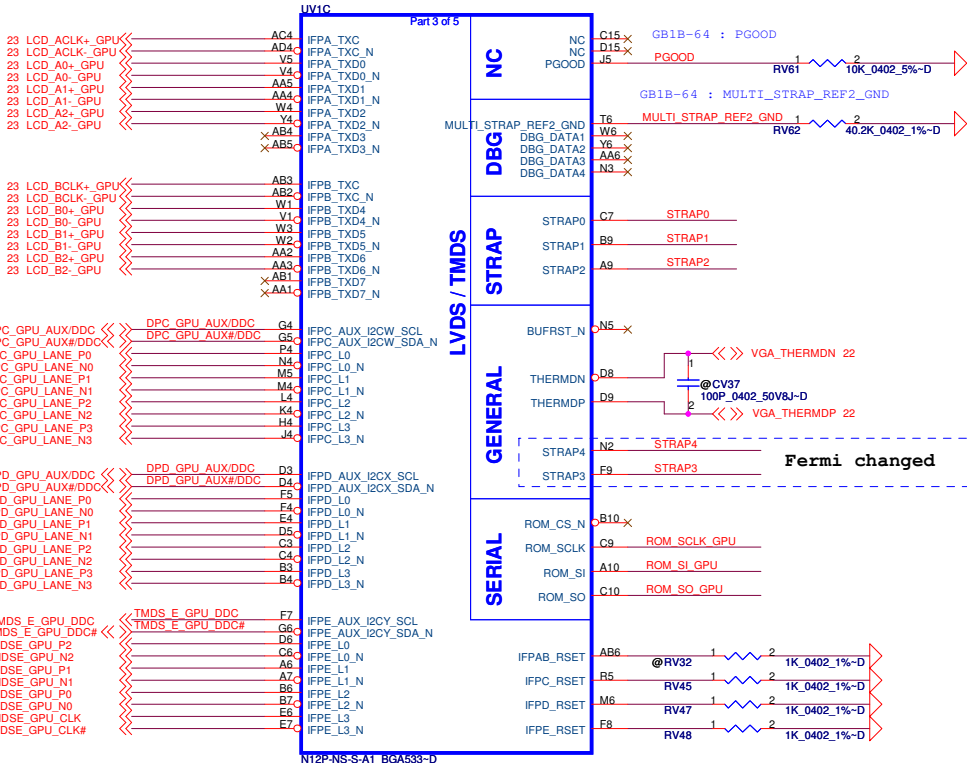
**Compal Electronics, Inc.**

**N12P PCIE,I2C,DAC,GPIO**

**LA-6592P**

Thursday, January 13, 2011

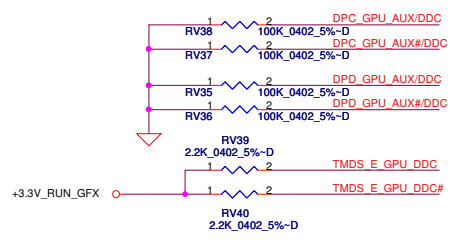
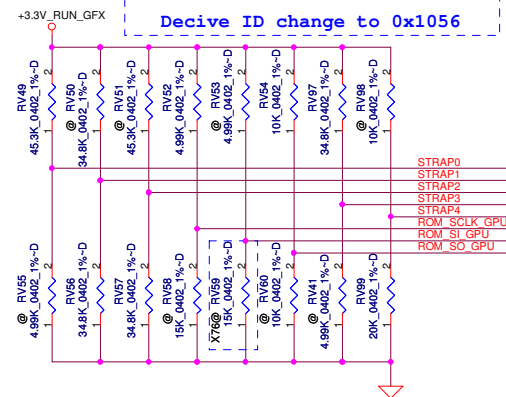
Size	Document Number	Rev
	LA-6592P	1.0
Date:	Thursday, January 13, 2011	Sheet 46 of 75



TO DOCKING

TO DOCKING

TO MB HDMI



Resistor Values	Pull-up to +3V	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

**\*\* Hynix 64Mx16 DDR3 part stuff RV59=15K  
Samsung 64Mx16 DDR3 part stuff RV59=20K  
Hynix 128Mx16 DDR3 part stuff RV59=35K  
Samsung 128Mx16 DDR3 part stuff RV59=45.3K**

ROM_SCLK	PCIDEVID_EXT, SUB_VENDOR, SLOT_CLK, PEX_PLL_EN
ROM_SI	RAM_CFG[3:0]
ROM_SO	XCLK_417, FB_0_BAR_SIZE, ALT_ADOOR, VGA_DEVICE

STRAP0	USER[3:0]
STRAP1	3GIO_PADCFG_LUT_ADR[3:0]
STRAP2	PCI_DEVID[3:0]

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**Compal Electronics, Inc.**

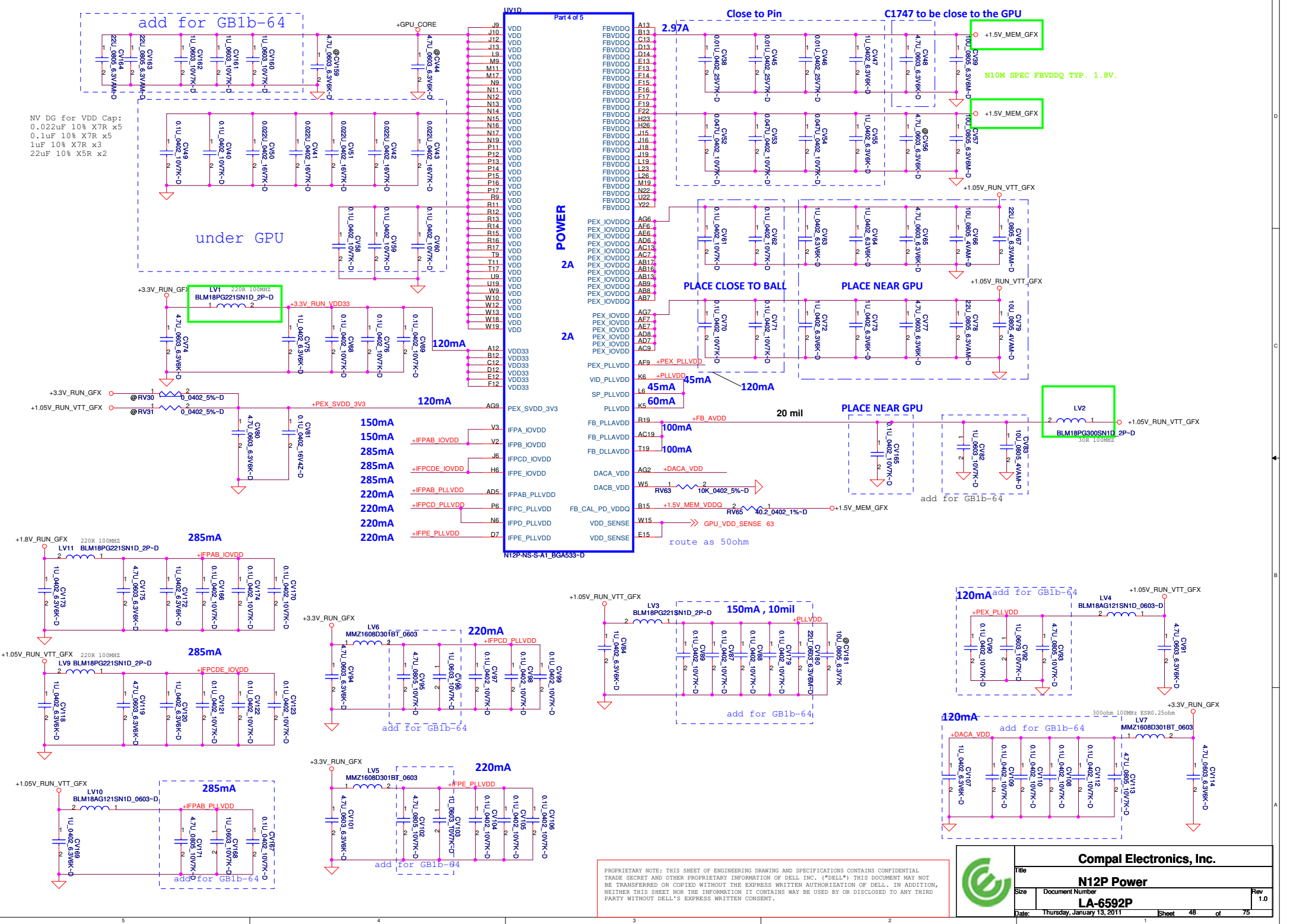
Title: **N12P DP, STRAP, GND**

Size: **LA-6592P**

Date: **Thursday, January 13, 2011**

Rev: **1.0**

Sheet: **47** of **75**



NV DG for VDD Cap:  
 0.022uF 10% X7R x5  
 0.1uF 10% X7R x5  
 1uF 10% X7R x3  
 22uF 10% X5R x2

+3.3V\_RUN\_GFX  
 +1.05V\_RUN\_VTT\_GFX

+1.8V\_RUN\_GFX  
 +1.05V\_RUN\_VTT\_GFX

+1.05V\_RUN\_VTT\_GFX

+1.05V\_RUN\_VTT\_GFX

+1.05V\_RUN\_VTT\_GFX

+1.05V\_RUN\_VTT\_GFX

POWER  
 2A  
 2A

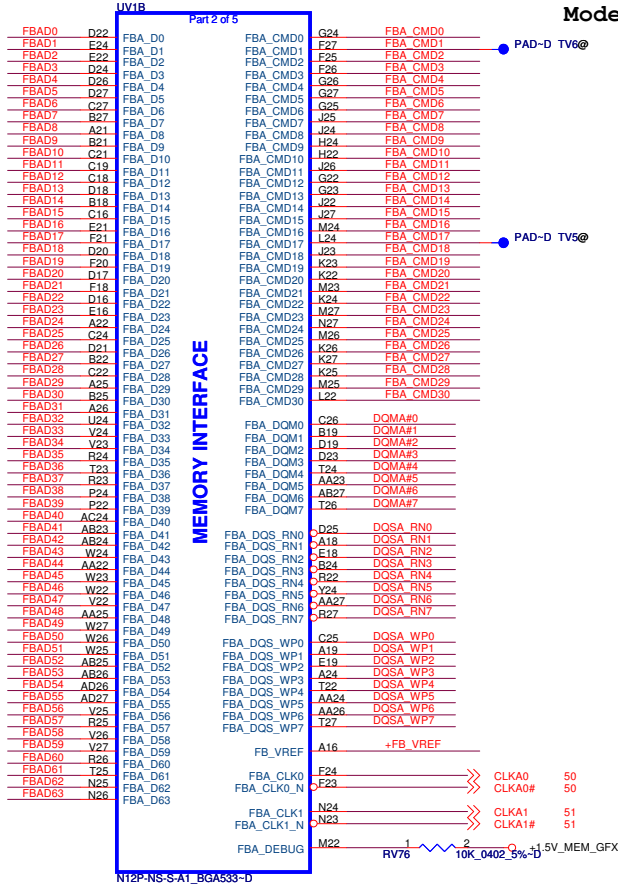
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<b>Compal Electronics, Inc.</b>				
				<b>N12P Power</b>
Title	Document Number <b>LA-6592P</b>	Date Thursday, January 13, 2011	Sheet 48	Rev 1.0

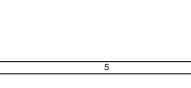
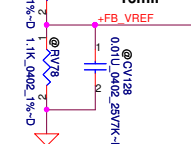
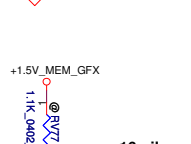
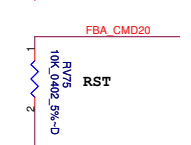
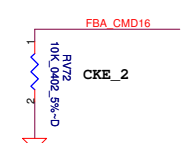
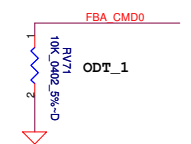
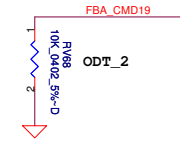
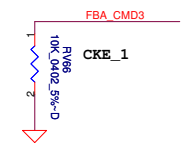
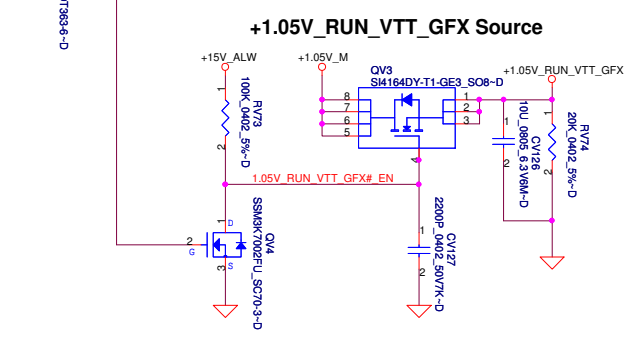
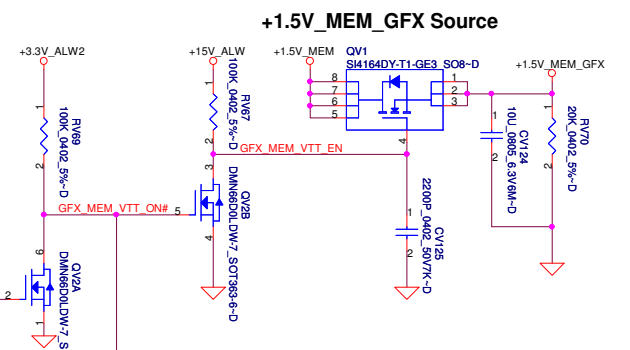
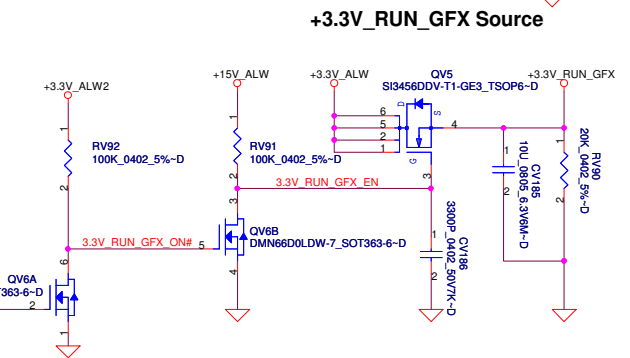
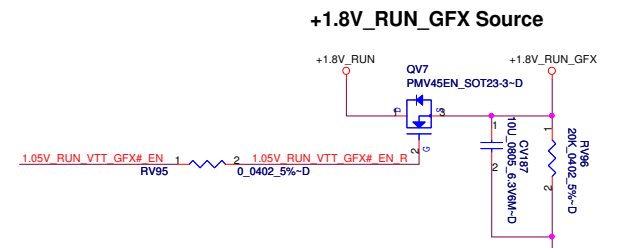


FBAD[0..63] <<> FBAD[0..63] 50.51  
 FBA\_CMD[0..30] <<> FBA\_CMD[0..30] 50.51  
 DQMA#[0..7] <<> DQMA#[0..7] 50.51  
 DQSA\_RN[0..7] <<> DQSA\_RN[0..7] 50.51  
 DQSA\_WP[0..7] <<> DQSA\_WP[0..7] 50.51

### Mode E - Mirror Mode Mapping



Address	DATA Bus
CMD0	ODT_L
CMD1	CS1#_L
CMD2	CS0#_L
CMD3	CKE_L
CMD4	A9
CMD5	A6
CMD6	A3
CMD7	A0
CMD8	A8
CMD9	A12
CMD10	A1
CMD11	RAS#
CMD12	A13
CMD13	BA1
CMD14	A14
CMD15	CAS#
CMD16	CKE_H
CMD17	CS1#_H
CMD18	CS0#_H
CMD19	ODT_H
CMD20	RST
CMD21	A7
CMD22	A4
CMD23	A11
CMD24	A2
CMD25	A10
CMD26	A5
CMD27	BA2
CMD28	WE#
CMD29	BA0
CMD30	A15
CMD31	BA2



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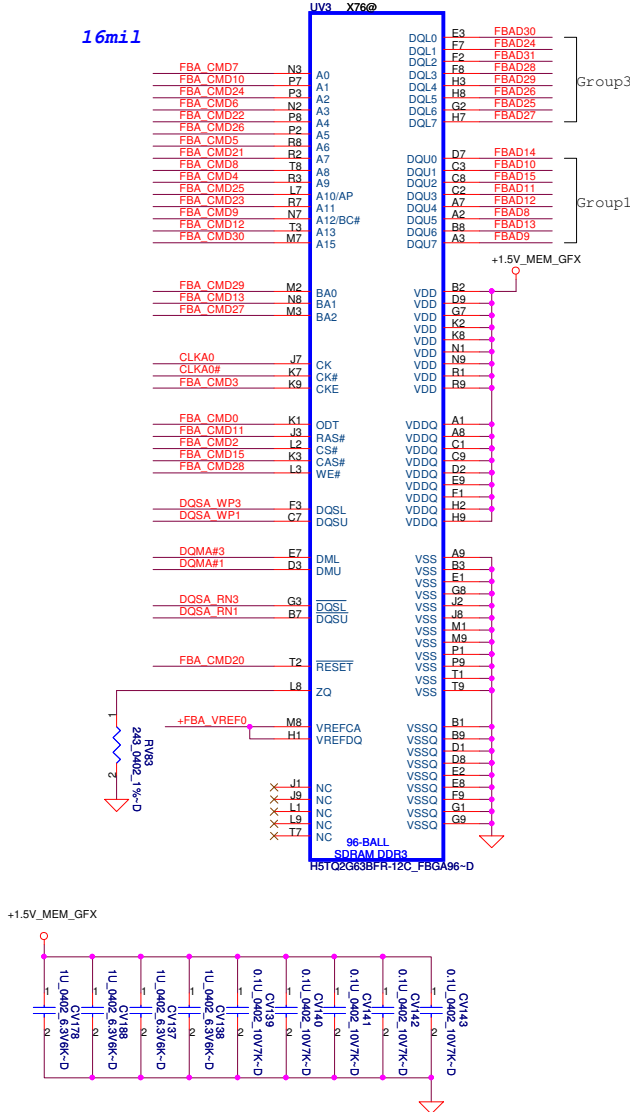
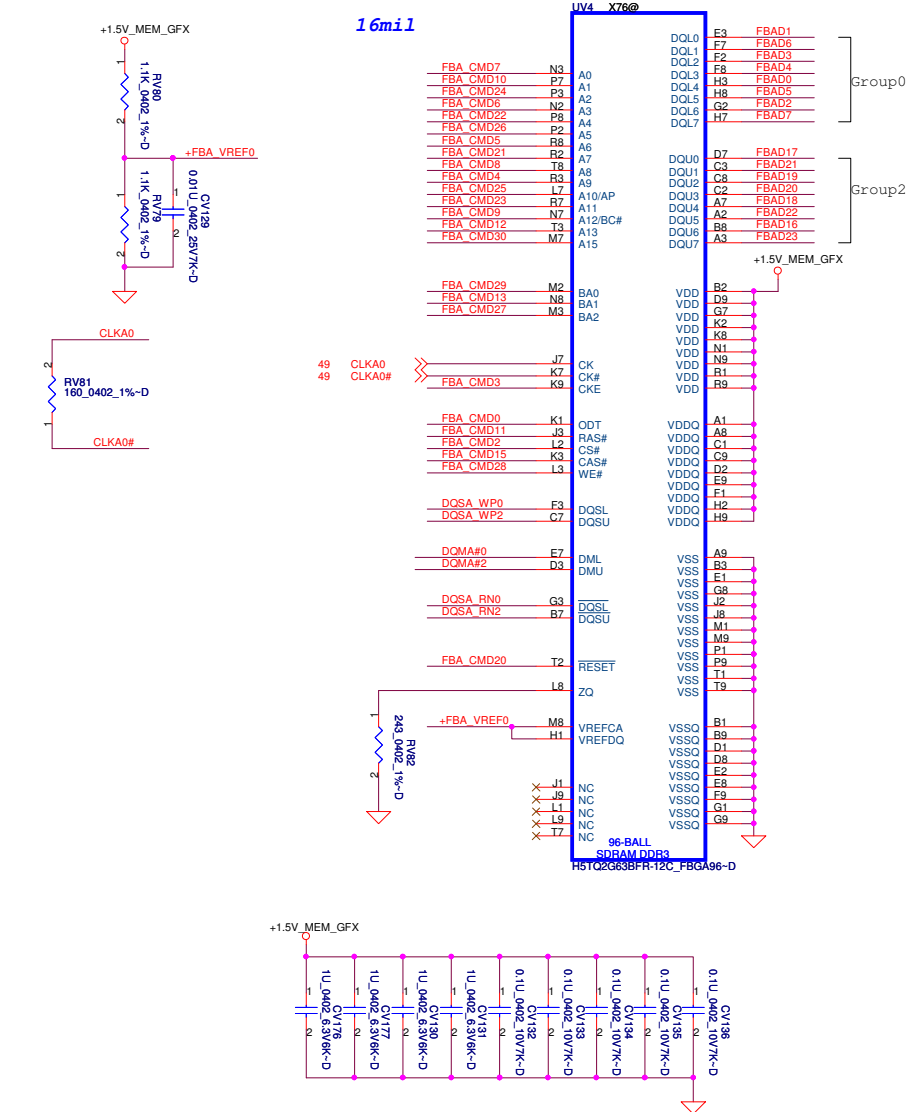
**N12P Memory**

**LA-6592P**

Date: Thursday, January 13, 2011 Sheet 49 of 75

Memory Partition A - Lower 32 bits

change to Hynix




- FBA\_CMD[0..30] <<< FBA\_CMD[0..30] 49.51
- FBAD[0..63] <<<>> FBAD[0..63] 49.51
- DOMA#[0..7] <<<>> DOMA#[0..7] 49.51
- DQSA\_RN[0..7] <<<>> DQSA\_RN[0..7] 49.51
- DQSA\_WP[0..7] <<<>> DQSA\_WP[0..7] 49.51

Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD0	ODT_L	
CMD1	CS1#_L	
CMD2	CS0#_L	
CMD3	CKE_L	
CMD4	A9	A11
CMD5	A6	A7
CMD6	A3	BA1
CMD7	A0	A12
CMD8	A8	A8
CMD9	A12	A0
CMD10	A1	A2
CMD11	RAS#	RAS#
CMD12	A13	A14
CMD13	BA1	A3
CMD14	A14	A13
CMD15	CAS#	CAS#
CMD16		CKE_H
CMD17		CS1#_H
CMD18		CS0#_H
CMD19		ODT_H
CMD20	RST	RST
CMD21	A7	A6
CMD22	A4	A5
CMD23	A11	A9
CMD24	A2	A1
CMD25	A10	WE#
CMD26	A5	A4
CMD27	BA2	A15
CMD28	WE#	A10
CMD29	BA0	BA0
CMD30	A15	BA2

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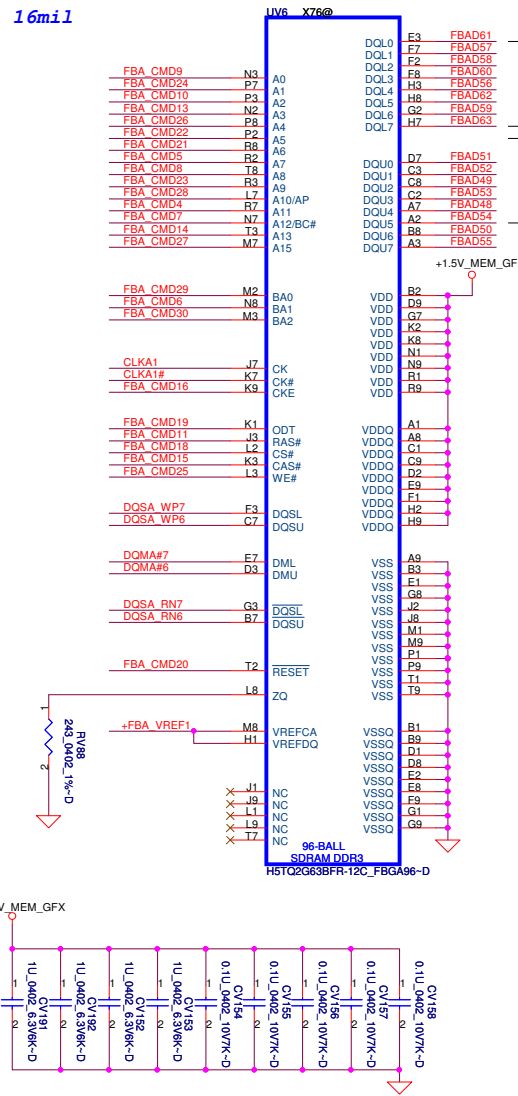
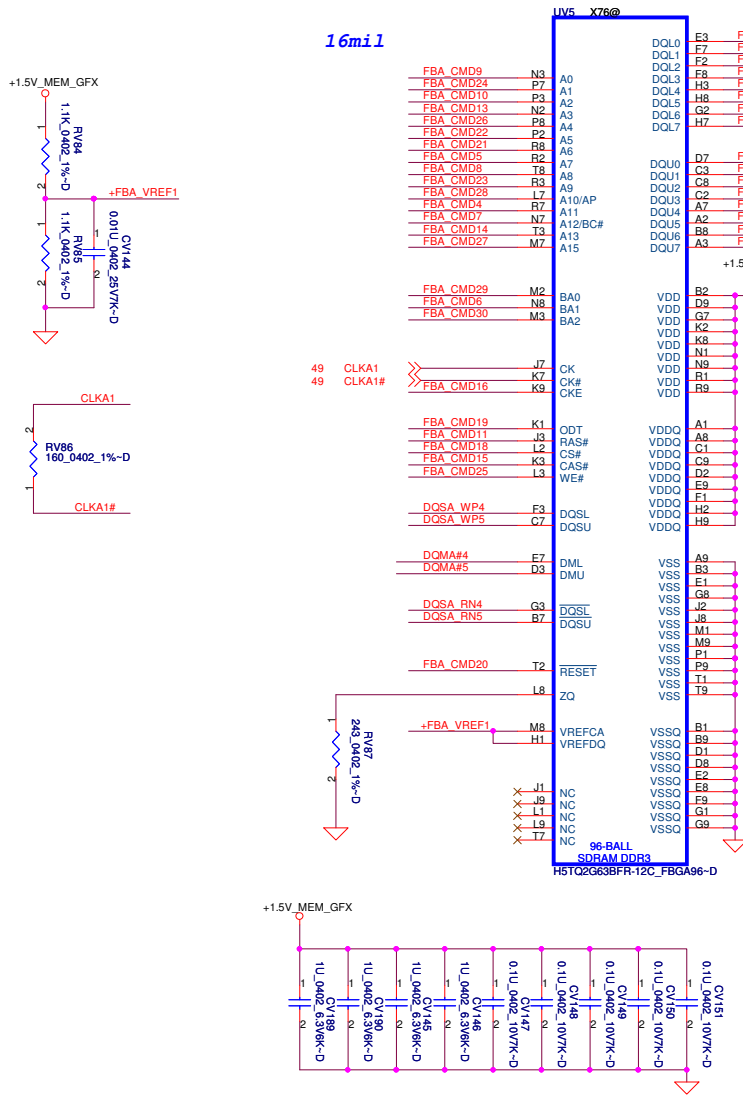
Title: **VRAM A Lower**

Size: **LA-6592P**

Date: Thursday, January 13, 2011 Sheet 50 of 75 Rev 1.0

# Memory Partition A - Upper 32 bits

FBAD[0..63] <<>> FBAD[0..63] 49.50  
 FBA\_CMD[0..30] <<>> FBA\_CMD[0..30] 49.50  
 DOMA#[0..7] <<>> DOMA#[0..7] 49.50  
 DQSA RN[0..7] <<>> DQSA\_RN[0..7] 49.50  
 DQSA WP[0..7] <<>> DQSA\_WP[0..7] 49.50



## Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD0	ODT_L	
CMD1	CS1#_L	
CMD2	CS0#_L	
CMD3	CKE_L	
CMD4	A9	A11
CMD5	A6	A7
CMD6	A3	BA1
CMD7	A0	A12
CMD8	A8	A8
CMD9	A12	A0
CMD10	A1	A2
CMD11	RAS#	RAS#
CMD12	A13	A14
CMD13	BA1	A3
CMD14	A14	A13
CMD15	CAS#	CAS#
CMD16		CKE_H
CMD17		CS1#_H
CMD18		CS0#_H
CMD19		ODT_H
CMD20	RST	RST
CMD21	A7	A6
CMD22	A4	A5
CMD23	A11	A9
CMD24	A2	A1
CMD25	A10	WE#
CMD26	A5	A4
CMD27	BA2	A15
CMD28	WE#	A10
CMD29	BA0	BA0
CMD30	A15	BA2

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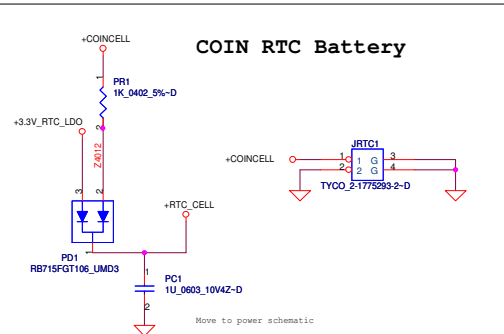
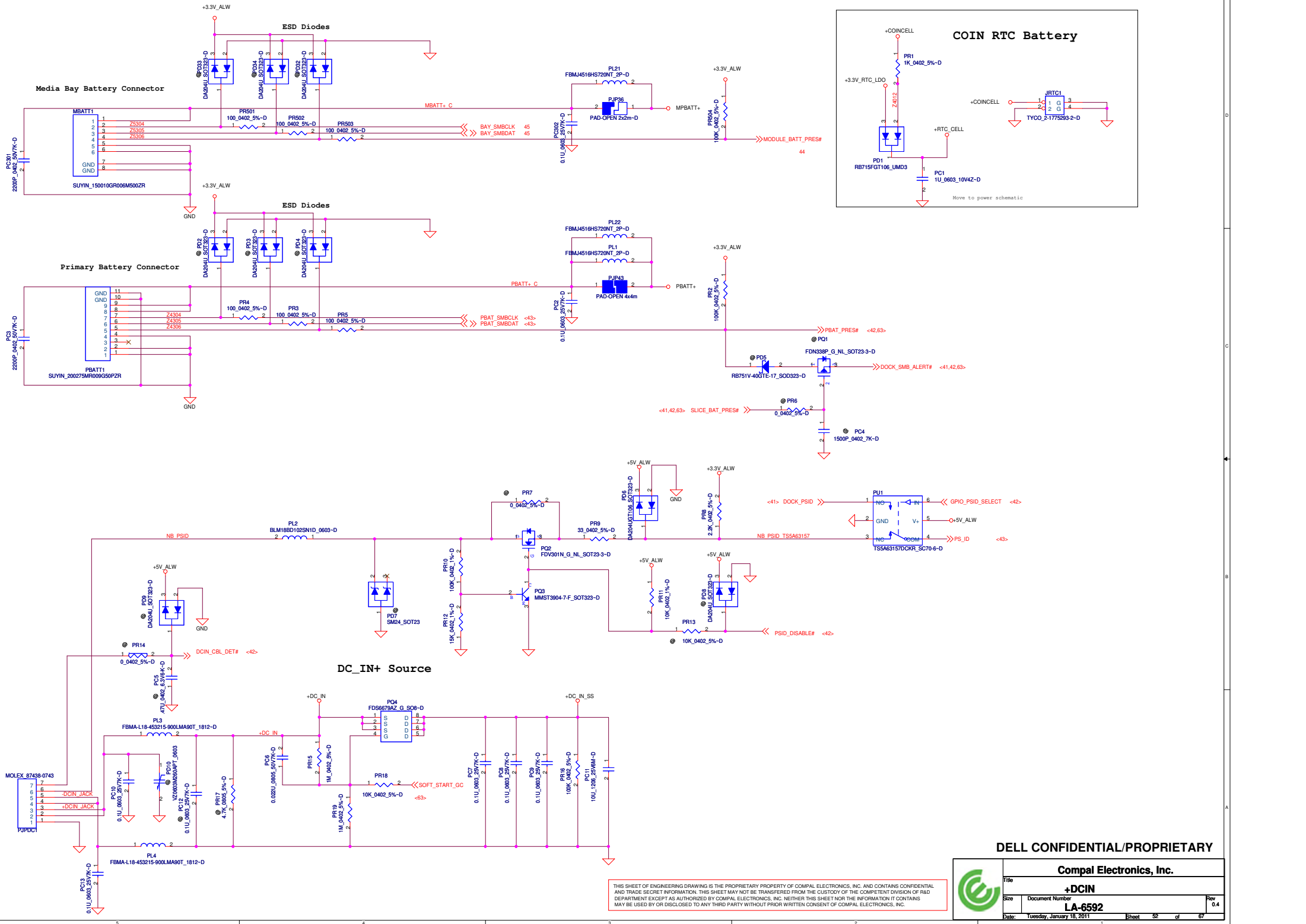
**Compal Electronics, Inc.**

Title: **VRAM A Upper**

Size: **LA-6592P**

Date: Thursday, January 13, 2011

Document Number	Rev	
<b>LA-6592P</b>	<b>1.0</b>	
Date: Thursday, January 13, 2011		Sheet 51 of 75



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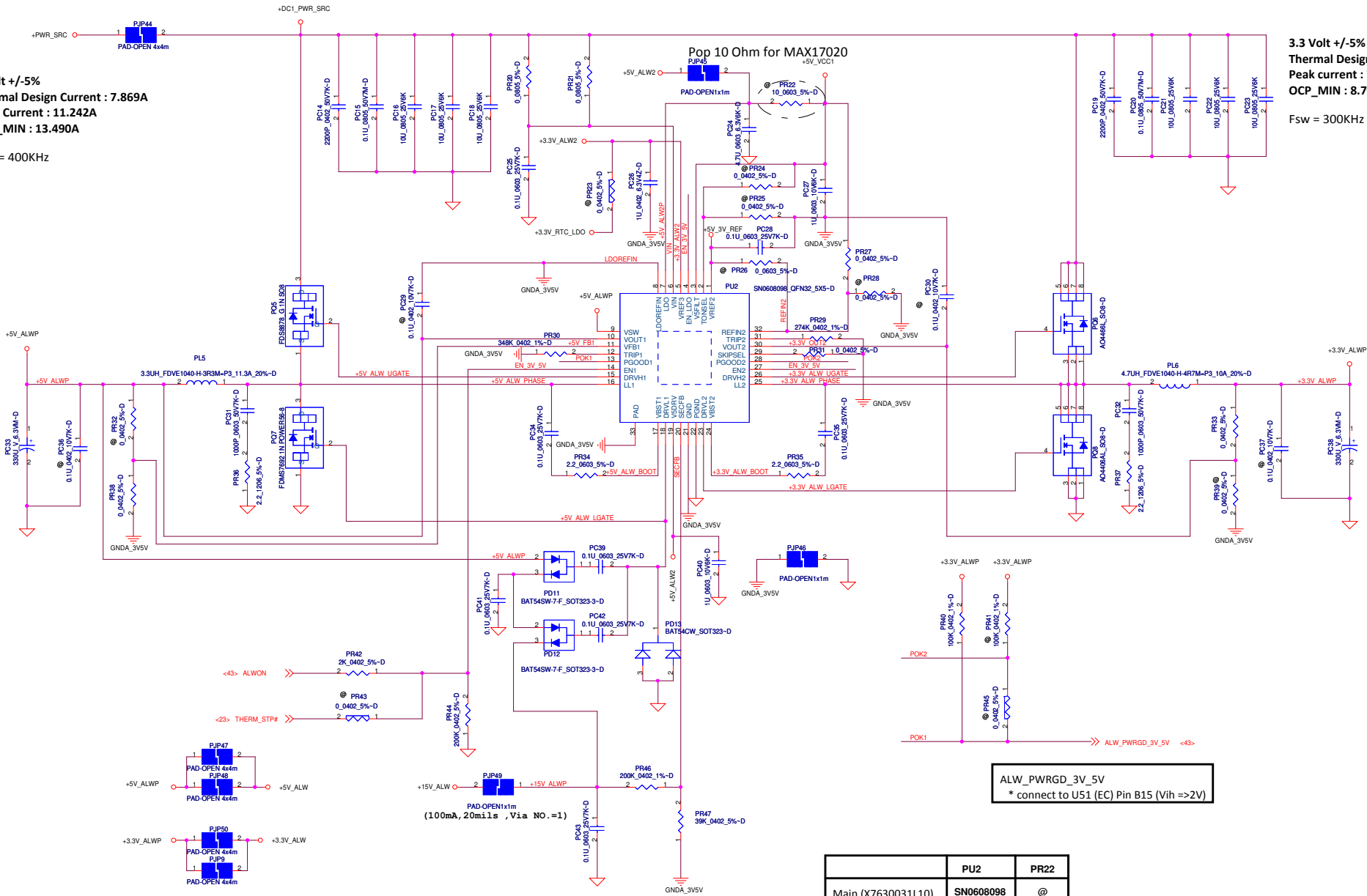
		<b>Compal Electronics, Inc.</b>	
		<b>+DCIN</b>	
Size	Document Number	LA-6592	Rev
Date:	Tuesday, January 18, 2011	Sheet	52 of 67

**+3.3V\_ALWP / +5V\_ALWP / +5V\_ALW2 / +15V\_ALWP / +3.3V\_RTC\_LDO**

**5 Volt +/-5%**  
**Thermal Design Current : 7.869A**  
**Peak Current : 11.242A**  
**OCP\_MIN : 13.490A**

Fsw = 400KHz

**3.3 Volt +/-5%**  
**Thermal Design Current : 5.079A**  
**Peak current : 7.256A**  
**OCP\_MIN : 8.707A**  
  
 Fsw = 300KHz



ALW\_PWRGD\_3V\_5V  
 \* connect to U51 (EC) Pin B15 (Vih =>2V)

	PU2	PR22
Main (X7630031L10)	SN0608098	@
2nd (X7630031L11)	MAX17020	10 Ohm

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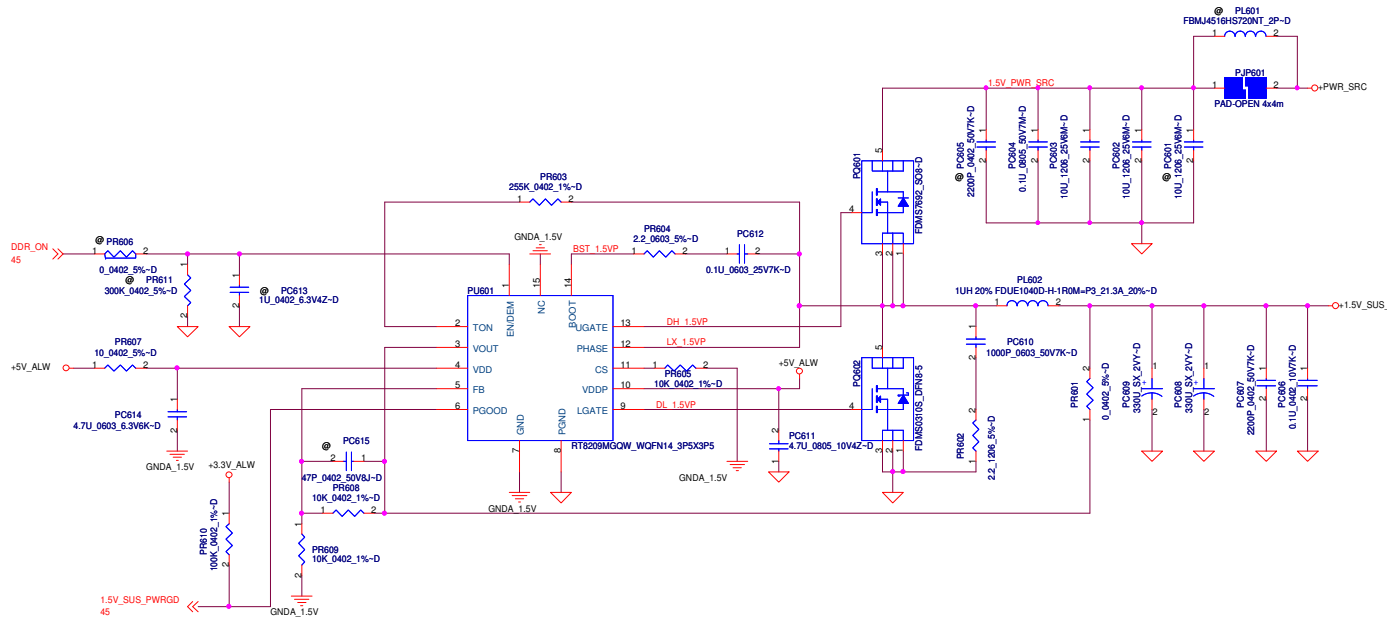
**Title DC/DC +3V/ +5V**

Size Document Number **LA-6592** Rev 0.4

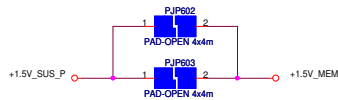
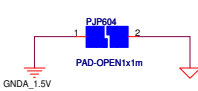
Date: Tuesday, January 18, 2011 Sheet 53 of 67

+1.5V\_SUS\_P

1.5 Volt +/-5%  
 Thermal Design Current: 12.275A  
 Peak current: 17.535A  
 OCP\_MIN: 21.042A



1.5V\_SUS\_PWRGD  
 \* connect to U51 (EC) Pin B9 (Vih => 2V)



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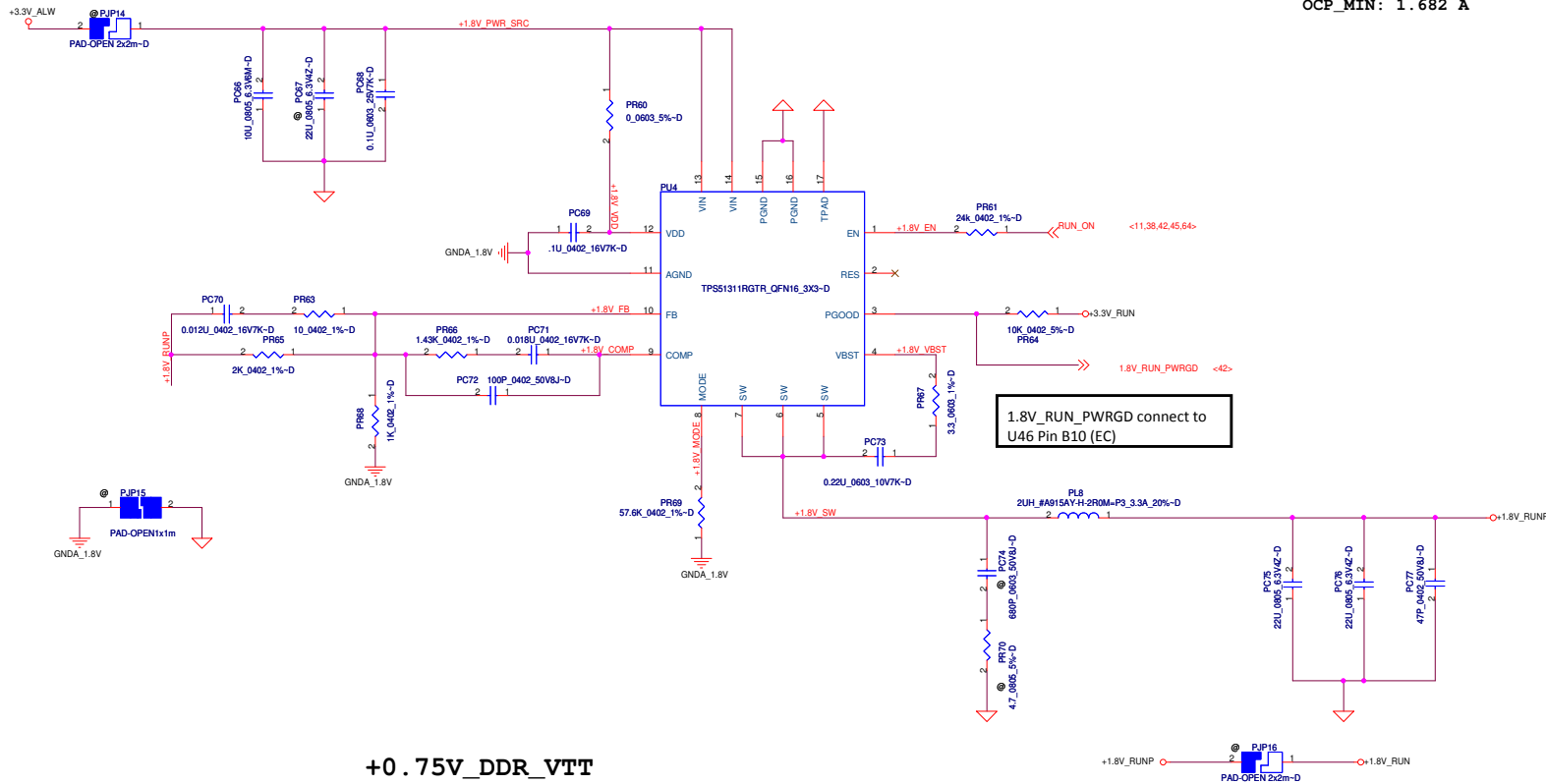
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title		<b>+1.5V MEM</b>	
Size	Document Number	Rev	
	<b>LA-6592</b>	<b>0.4</b>	
Date:	Tuesday, January 18, 2011	Sheet	54 of 67

### +1.8V\_RUNP

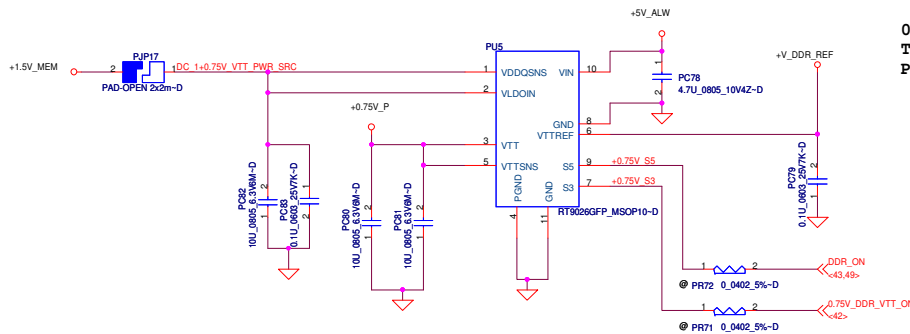
1.8 Volt +/-5%  
 Thermal Design Current: 0.981 A  
 Peak current: 1.402 A  
 OCP\_MIN: 1.682 A



### +0.75V\_DDR\_VTT

DDR3 Termination

0.75V Volt +/-5%  
 Thermal Design Current: 0.525A  
 Peak current: 0.75A



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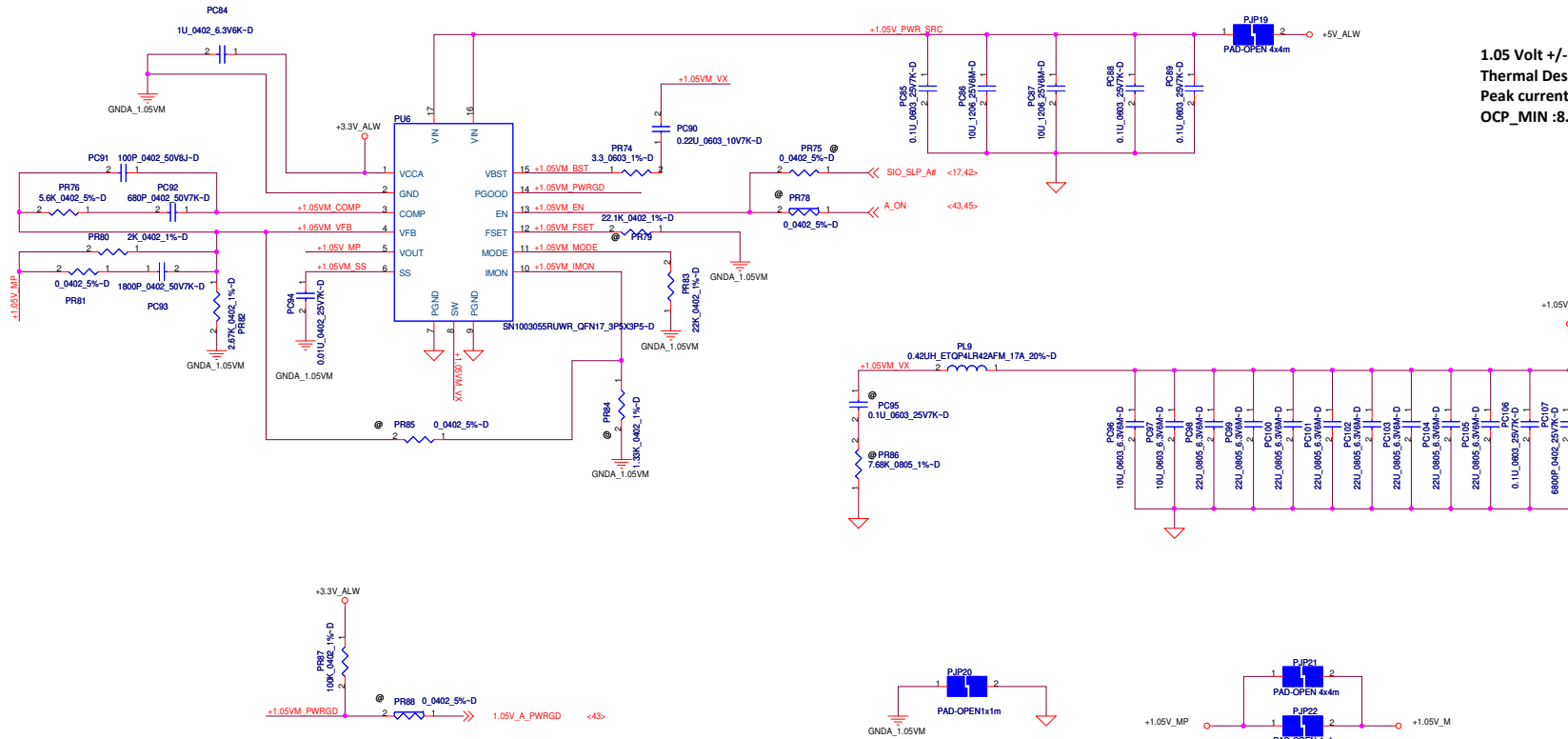
Compal Electronics, Inc.

+0.75V DDR VT/+1.8V RUN

Title	+0.75V DDR VT/+1.8V RUN		Rev	0.4
Size	Document Number	LA-6592		
Date:	Tuesday, January 18, 2011	Sheet	55	of 67

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+1.05V\_M



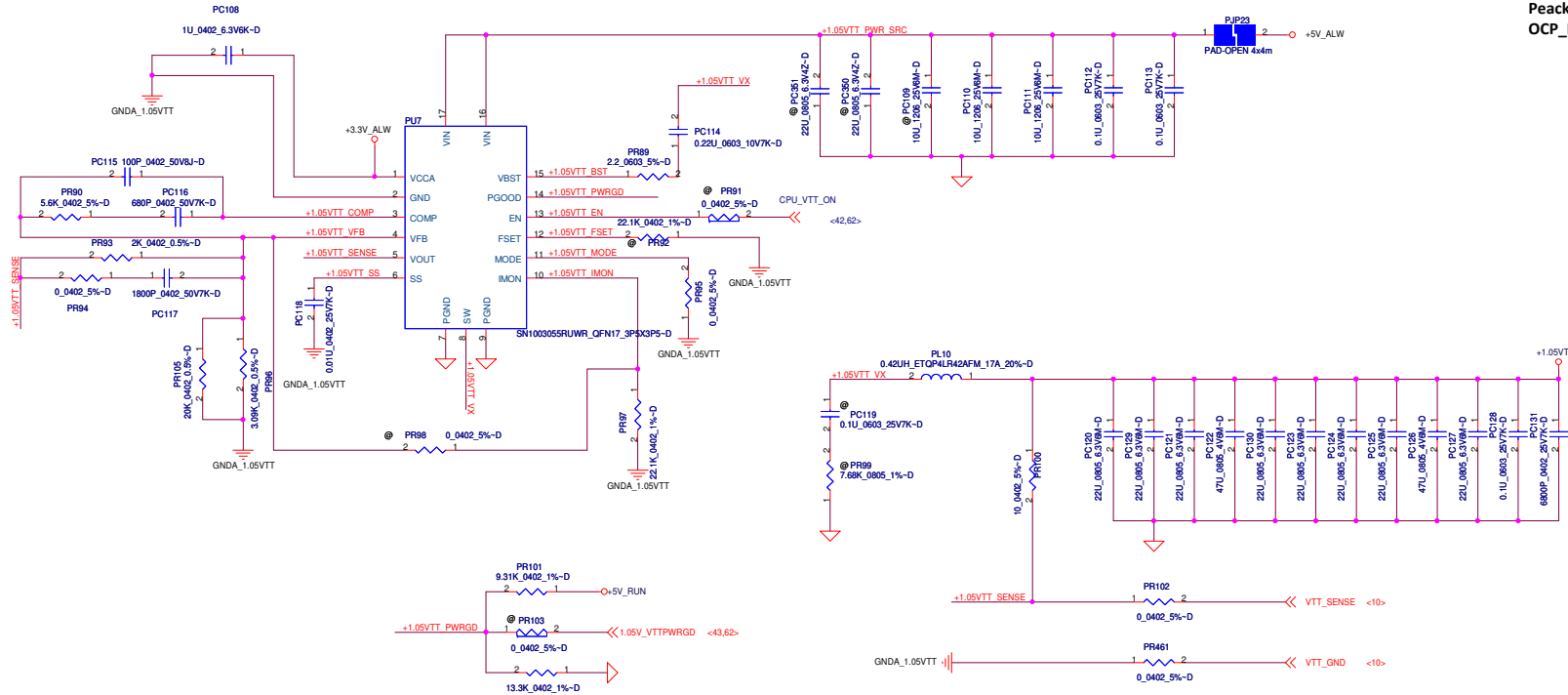
1.05 Volt +/-5%  
 Thermal Design Current : 4.782A  
 Peak current : 6.832A  
 OCP\_MIN :8.198A

1.05V\_A\_PWRGD  
 \* connect to U51 (EC) Pin A14 (Vih => 2V)

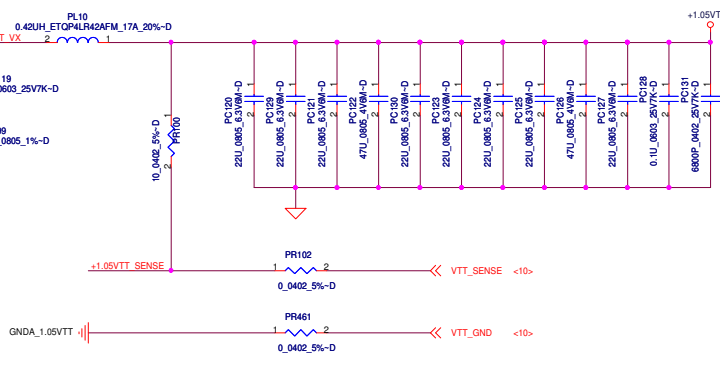
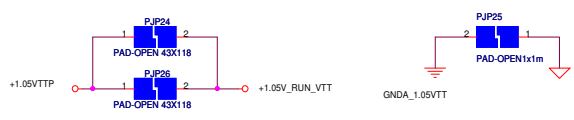


**+1.05VTT**

**1.05Volt**  
 => (+/- 5% AC + DC +Ripple)  
 => (+/- 2% DC + Ripple)  
**Thermal Design Current : 5.980A**  
**Peack current : 8.970A**  
**OCP\_MIN : 10.764A**



**1.05V\_VTTPWRGD**  
 \* connect to PU13 Pin 15 (Vih => 2V)  
 \* connect to U50 Pin 1 (Vih => 2.31V)



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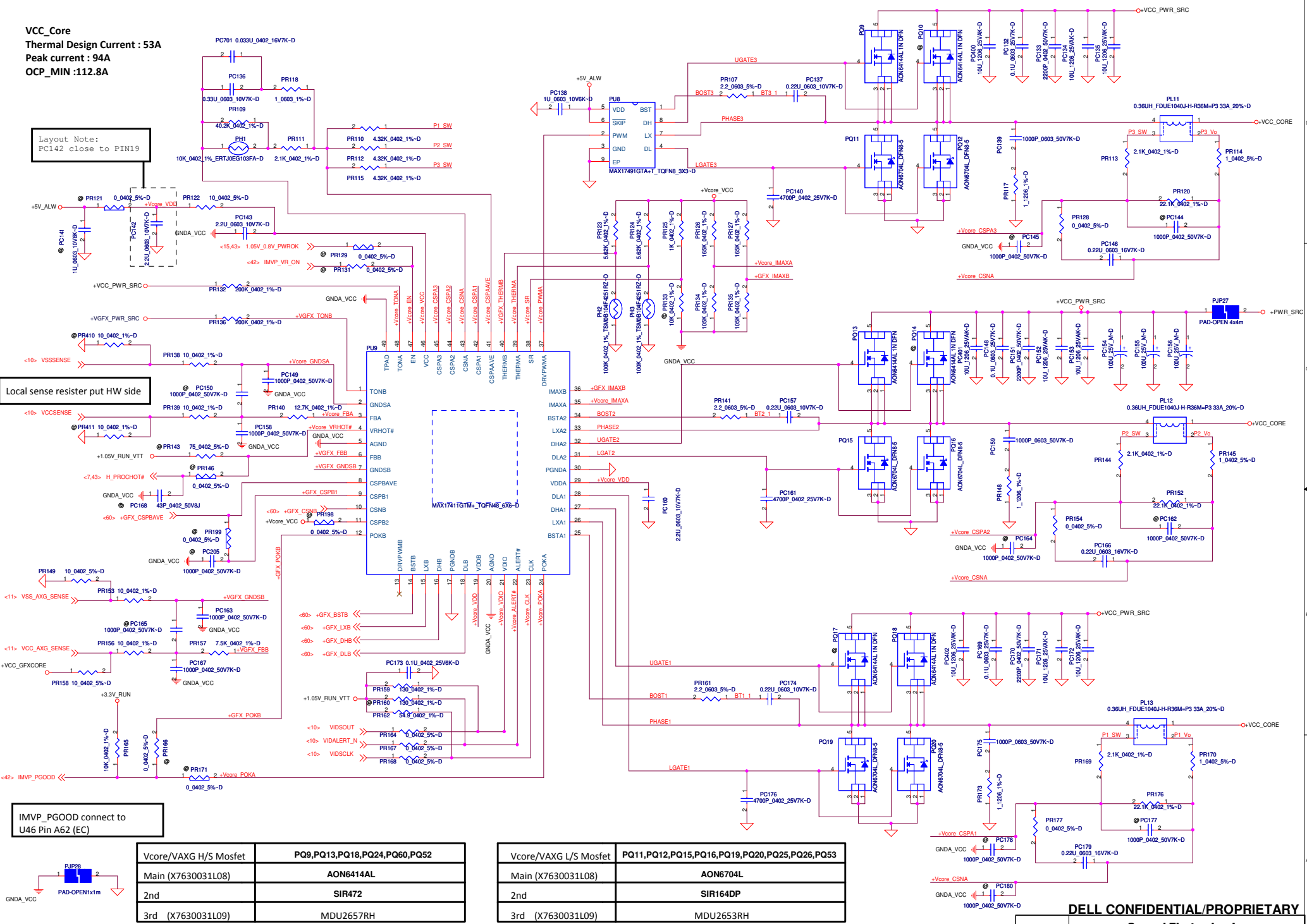
**Compal Electronics, Inc.**

Title		<b>ISL95870A +1.05V RUN VTT</b>	
Size	Document Number	Rev	
	<b>LA-6592</b>	<b>0.4</b>	
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VCC\_Core  
 Thermal Design Current : 53A  
 Peak current : 94A  
 OCP\_MIN :112.8A

Layout Note:  
 PC142 close to PIN19



Local sense resistor put HW side

IMVP\_PGOOD connect to U46 Pin A62 (EC)

Vcore/VAXG H/S Mosfet	PQ9,PQ13,PQ18,PQ24,PQ60,PQ52
Main (X7630031L08)	AON6414AL
2nd	SIR472
3rd (X7630031L09)	MDU2657RH

Vcore/VAXG L/S Mosfet	PQ11,PQ12,PQ15,PQ16,PQ19,PQ20,PQ25,PQ26,PQ53
Main (X7630031L08)	AON6704L
2nd	SIR164DP
3rd (X7630031L09)	MDU2653RH

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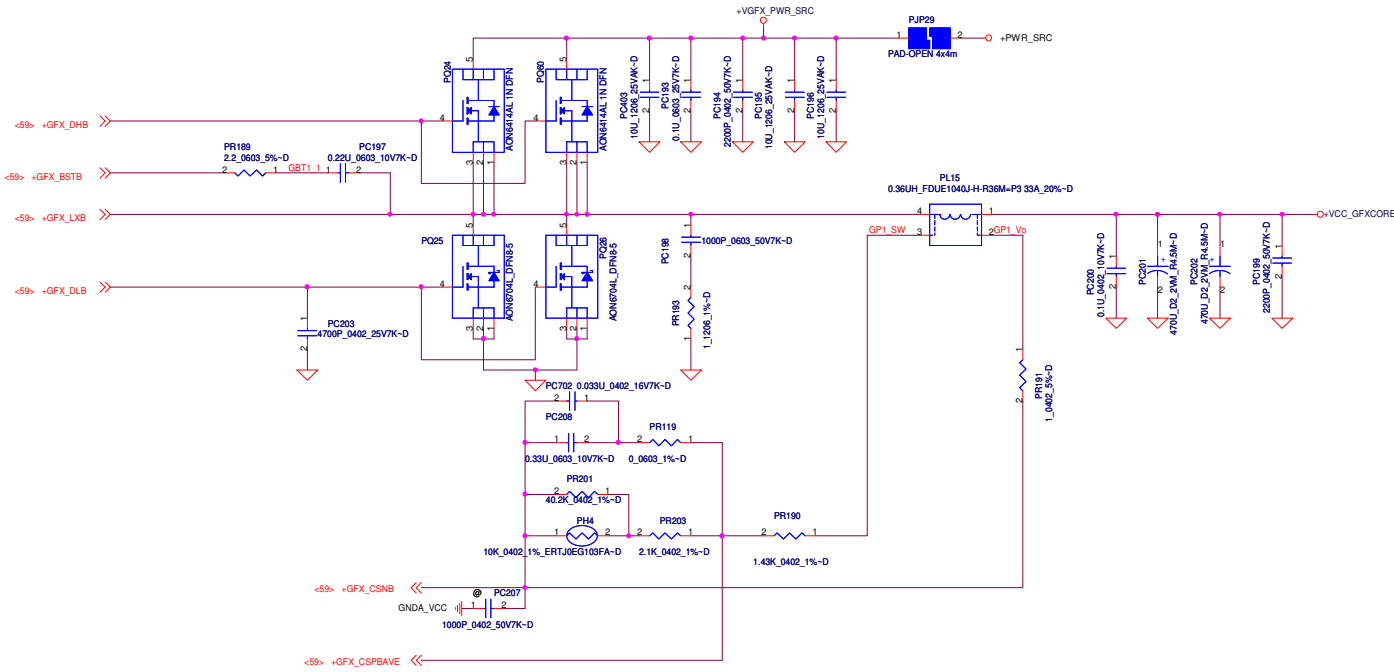
**Vcore**

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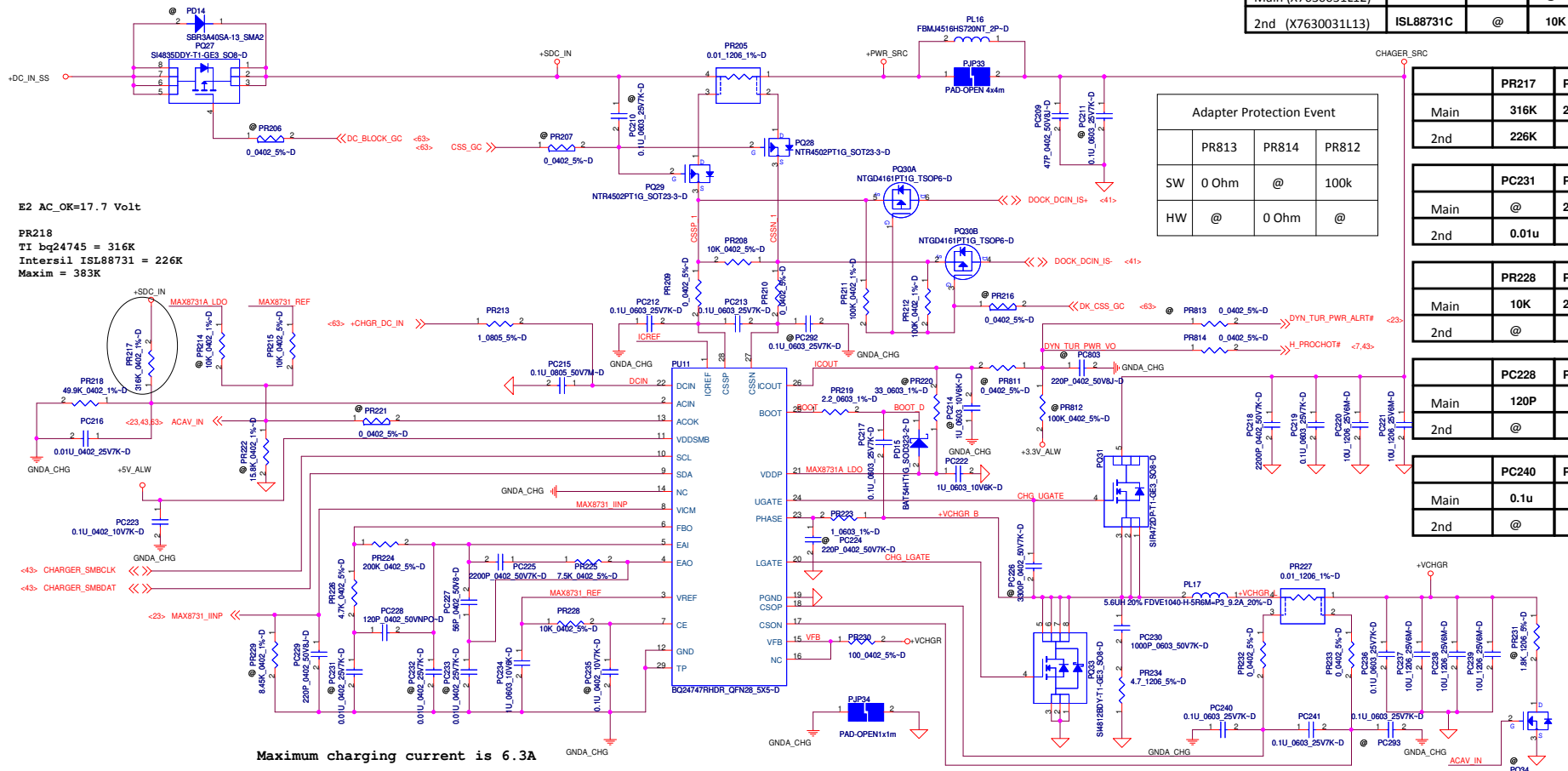
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VCC\_AXG  
 Thermal Design Current : 21.5A  
 Peak current : 33A  
 OCP\_MIN :39.6A



	PU11	PR215	PR214	PR222
Main (X7630031L12)	BQ24747	10K	@	@
2nd (X7630031L13)	ISL88731C	@	10K	15.8K



E2 AC\_OK=17.7 Volt  
 PR218  
 TI bq24745 = 316K  
 Intersil ISL88731 = 226K  
 Maxim = 383K

Adapter Protection Event			
	PR813	PR814	PR812
SW	0 Ohm	@	100k
HW	@	0 Ohm	@

	PR217	PC229	PR226
Main	316K	220P	4.7K
2nd	226K	@	2.2K

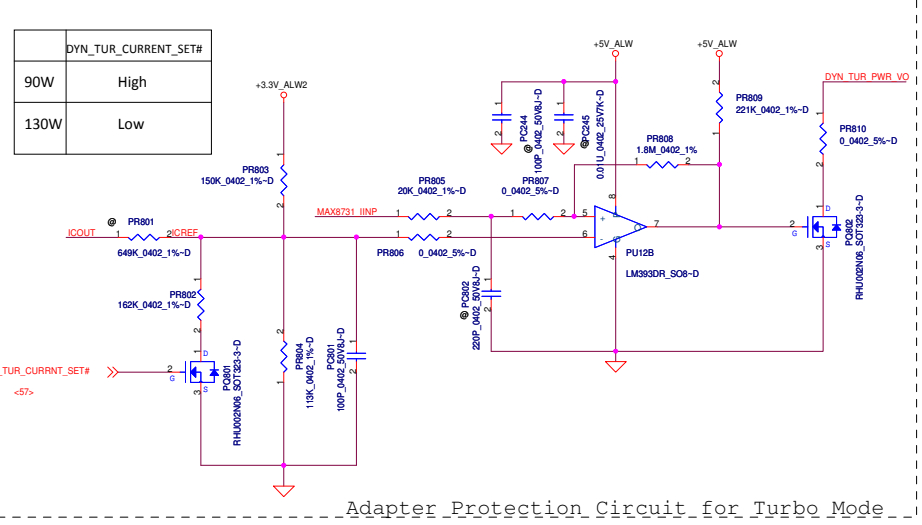
	PC231	PR224	PR225
Main	@	200K	7.5K
2nd	0.01u	@	@

	PR228	PC225	PC227
Main	10K	2200P	56P
2nd	@	@	@

	PC228	PC234	PC233
Main	120P	1u	@
2nd	@	@	0.01u

	PC240	PC241	PR232
Main	0.1u	0.1u	0 ohm
2nd	@	0.22u	10 ohm

Maximum charging current is 6.3A



DYN_TUR_CURRENT_SET#	
90W	High
130W	Low

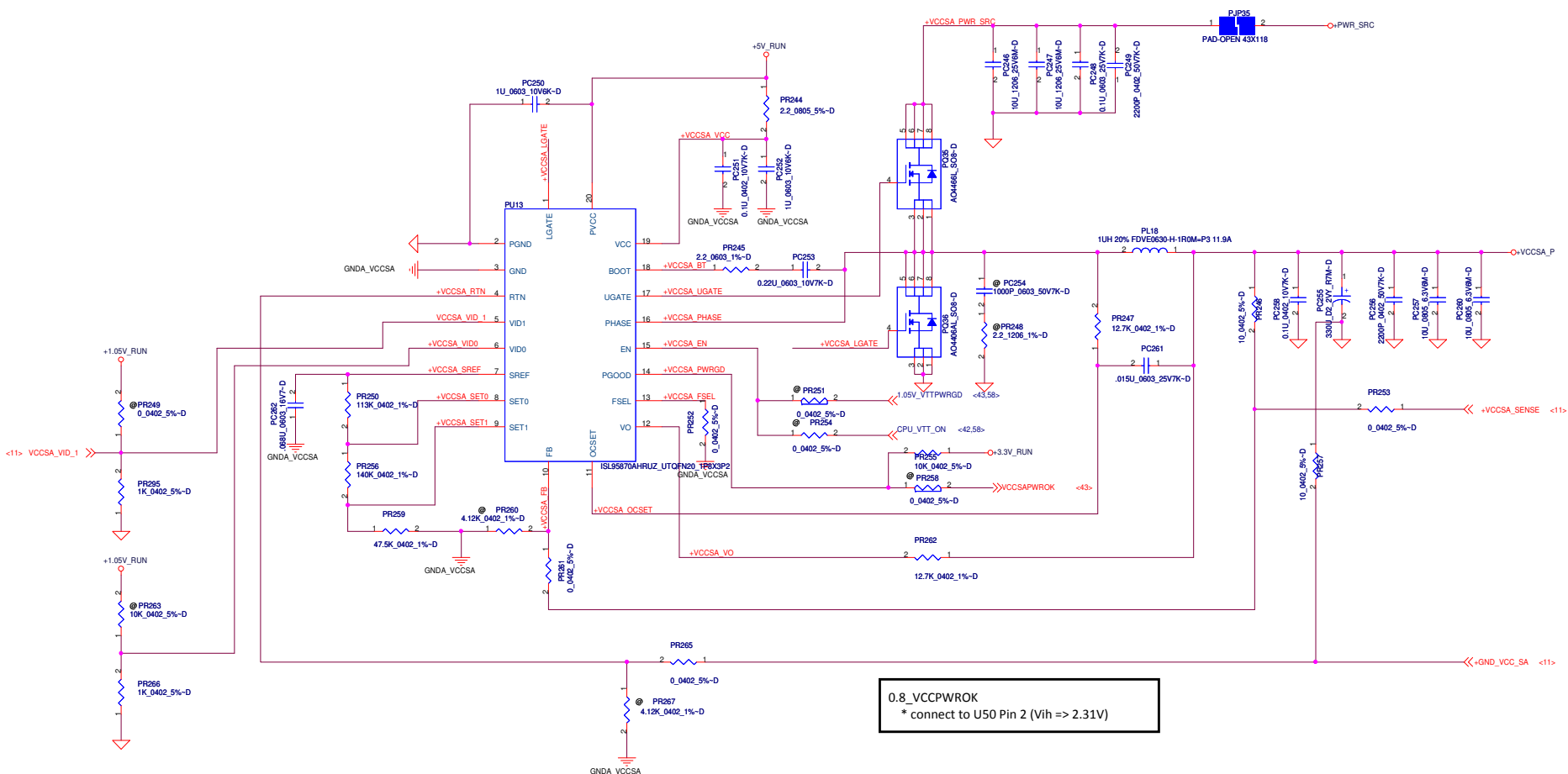
	PR223	PR220	PC214	PC292	PR209	PR210	PC213
Main	1 ohm	@	@	@	0 ohm	0 ohm	0.1u
2nd	0 ohm	4.7 ohm	1u	0.1u	10 ohm	10 ohm	0.047u

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	Charger		
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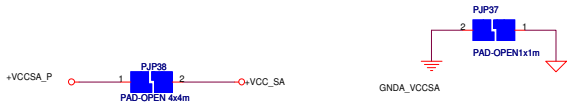
VCCSA  
 Thermal Design Current : 4.2A  
 Peak current : 6A  
 OCP\_MIN : 7.2A



0.8\_VCCPWROK  
 \* connect to U50 Pin 2 (Vih => 2.31V)

VCCSA_VID_1	0.9V	0.8V
	0	1

output voltage adjustable network



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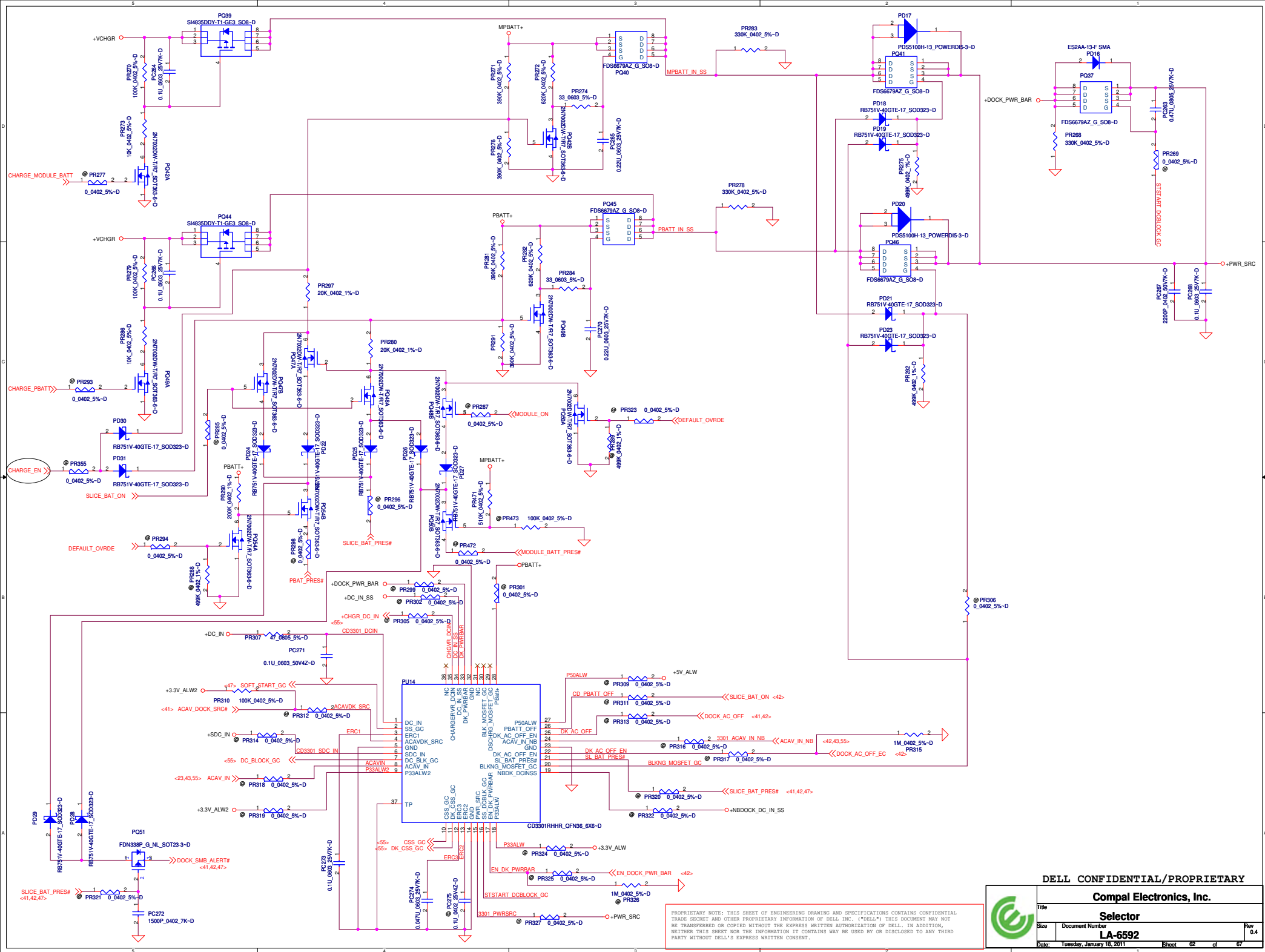
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**ISL95870A 0.8V VCC SA**

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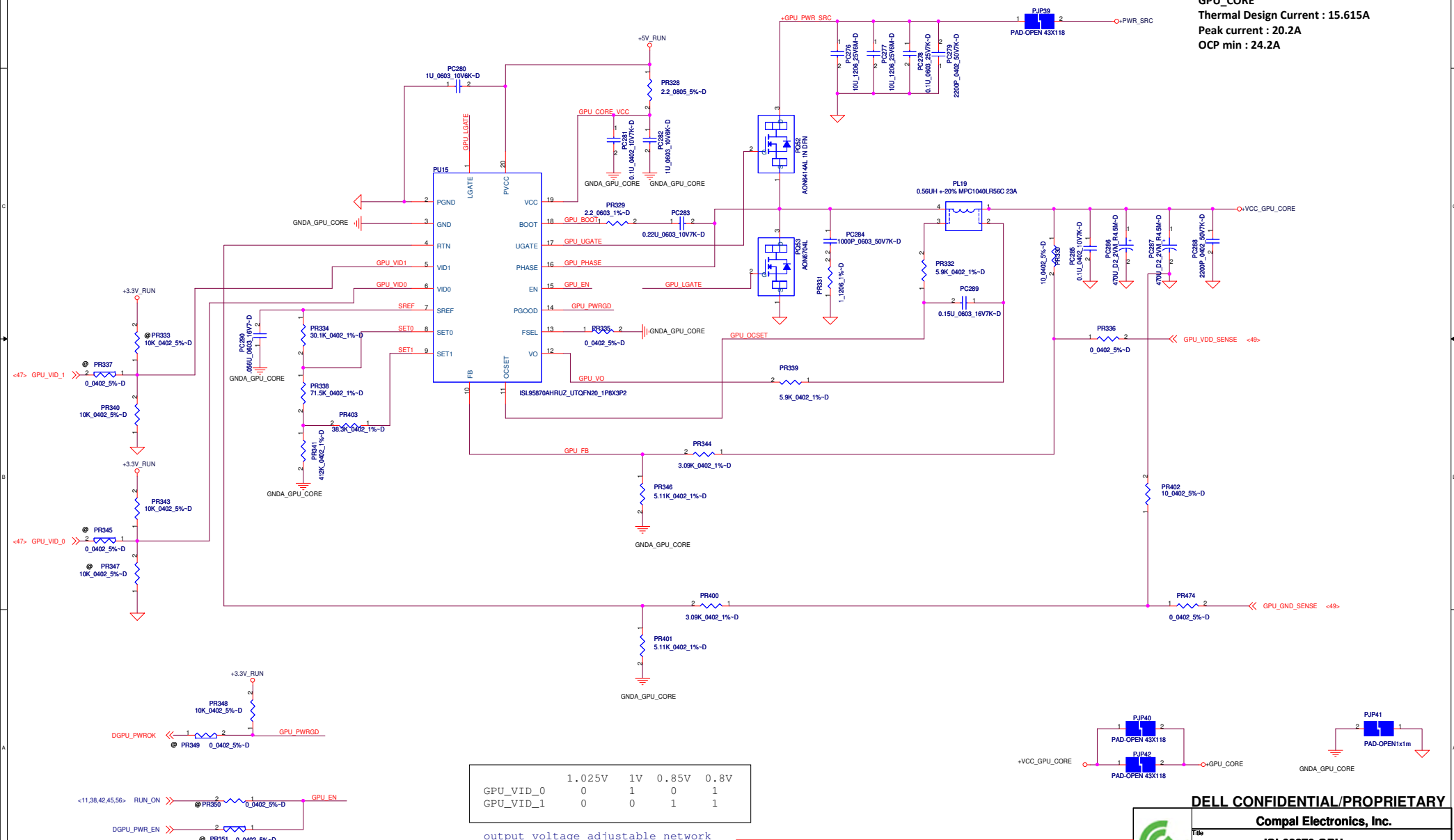
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**GPU\_CORE**  
**Thermal Design Current : 15.615A**  
**Peak current : 20.2A**  
**OCP min : 24.2A**



output voltage adjustable network

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<b>ISL62870 GPU core</b>			
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# Version Change List (P. I. R. List)


Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	61	VCCSA	6/30	Intersil	VCCSA spike issue	Delete PR264 Delete VCCSA_VID_0 net Connect VCCSA_VID_1 net to PIN5 Depop PR249, PR267 and PR260 Change PR261 and PR260 to 0 Ohm (SD02800008L) from 24.9k (SD03424918L) Change PR259 to 47.5k (SD03447528L) from 274k (SD03427438L) Change PR256 to 140k (SD03414038L) from 0 Ohm (SD02800008L) Change PR250 to 113k ( ) from 34k (SD03434028L) Add pull down PR295 10k(SD02810028L)	X01
2	61	VCCSA	6/30	Intel	Change VCCSA VID pull down resistor value	Change PR295 and PR266 to 1k (SD02810018L) from 10k (SD02810028L)	X01
3	53	3V/5V	7/15	Compal	3V/5V Bulk cap interfere with ME	Change PC33 and PC38 to 330U/25m/H1.9(SGA00001A8L) from 330U/25m/H2.8 (SGA1933131L)	X01
4	54	+1.5V_SUS	7/15	Compal	Vendor will not support this part	Change PC609 and PC608 to 330U/9m/2V (SGA20331E0L) from 330U/9m/2.5V (SGA19331D1L)	X01
5	52	DCIN	7/15	Compal	PL3 and PL4 current rating is not enough for 130W adapter	Change PL2 and PL3 to FBMA-L18-453215-900LMA90T (SM01002078L) from FBMJ4516HS720NT(SM010009C8L)	X01
6	52	DCIN	7/15	Compal	PL1 current rating is not enough for 9cell (3.0Ah 1C) discharge current	Change PL1 to FBMJ4516HS720NT(SM010009C8L) from FBMA-L18-453215-900LMA90T (SM01002078L) Add PL22 FBMJ4516HS720NT(SM010009C8L)	X01
7	53	3V/5V	7/16	Compal	10u/1206/X5R/25V will COS	Change PC16,PC17,PC18,PC21,PC22 and PC23 to 10u/0805/X5R (SE00000QK00) from 10u/1206/X5R (SE142106M8L)	X01
8	53	3V/5V	7/16	Compal	+3.3V phase node over Mosfet Vds rating	Change PQ6 AO4466L (SB00000CG8L) from SI4128DY (SB00000IR0L) Change PQ8 AO4712L (SB00000AJ1L) from SI4134DY(SB00000KB0L)	X01
9	53	3V/5V	7/16	Compal	PC24 down size to 0603 from 0805	Change PC24 to 4.7u/6.3V/0603 (SE107475K8L) from 4.7u/6.3V/0805 (SE093475K8L)	X01
10	61	VCCSA	7/16	Compal	VCCSA output voltage is not constant so change some net name	Change +0.8V_VCC net name to +VCCSA_P Change 0.8V_VCCPWROK net name to VCCSAPWROK Change +0.8V_VCC_SA net name to +VCC_SA	X01
11	54	1.5V_SUS	7/16	Richtek	Reserve Pull down resistor on EN pin for power consumption issue	Add 0402 resistor pad on EN pin	X01
12	60	Charger	7/18	Compal	PQ27 body diode can handle surge current when adapter plug in so depop PD14	Depop PD14 SBR3A40SA (SC100003J00)	X01
13	62	Selector	7/18	Compal	Leakage issue on PD16	Change PD16 to ES2AA (SC100005A0L) from SBR3A40SA (SC100003J00)	X01
14	58,59	Axg_core Vcore	7/20	MAXIM	Reserve 0402 cap pad for transient fine tune	Add PC701 and PC702 0402 cap pad	X01
15	60	Charger	7/20	Compal	Reserve adapter protection circuit for turbo mode	Change PU11 pin1 net name to ICREF from GNDA_CHG Change PU11 pin26 net name to ICOUT from VCC Reserve PR801,PR802,PR803,PR804,PR805,PR806,PR807,PR808,PR809,PR810,PR811,PR812 Reserve PC801,PC802,PC803	X01
16	61	VCCSA	7/20	Compal	VCCSA phase node over Mosfet Vds rating	Change PQ35 AO4466L (SB00000CG8L) from SI4128DY (SB00000IR0L) Change PQ36 AO4712L (SB00000AJ1L) from SI4172DY(SB00000HN0L)	X01

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17	58	Vcore VAXG_core	7/24	MAXIM	Fine tune OCP setting for Pass 2 IC	Change PR127 to 165K (SD03416530L) from 100K (SD03410038L) Change PR135 to 105K (SD03410538L) from 150K (SD03415038L) Change PR126 to 165K (SD03416530L) from 100K (SD03410038L) Change PR134 to 105K (SD03410538L) from 150K (SD03415038L)	X01
18	58,59	Vcore VAXG_core	7/24	MAXIM	Phase node switching waveform abnormal issue for Pass 2 IC	Change PR118 to 1 Ohm (SD014100B8L) from 2 Ohm (SD013200B8L) Change PR119 to 1 Ohm (SD014100B8L) from 2 Ohm (SD013200B8L)	X01
19	53	3V/5V	7/28	Comapl	Broad band issue in 700MHz	Pop PC32 1000P (SE025102K8L) Pop PR37 2.2 Ohm (SD011220B8L) Pop PC31 1000P (SE025102K8L) Pop PR36 2.2 Ohm (SD011220B8L) Change PR35 to 2.2 Ohm (SD013220B8L) from 1 Ohm (SD013100B8L) Change PR35 to 2.2 Ohm (SD013220B8L) from 1 Ohm (SD013100B8L)	X01
20	58	Vcore	7/28	Comapl	Bump noise in band of 700MHz	Pop PC139 470P (SE024471J8L) Pop PC159 470P (SE024471J8L) Pop PR117 2.2 Ohm (SD011220B8L) Pop PR148 2.2 Ohm (SD011220B8L)	X01
21	54,58 59,63 56	1.5V Vcore VGF_X_Core GPU_core 1.05VM	7/28	Comapl	Broad band in 800MHz and 900MHz	Pop PC610 1000P (SE025102K8L) Pop PR602 2.2 Ohm (SD011220B8L) Pop PC175 470P (SE024471J8L) Pop PR173 2.2 Ohm (SD011220B8L) Pop PC198 470P (SE024471J8L) Pop PR193 2.2 Ohm (SD011220B8L) Pop PC284 1000P (SE025102K8L) Pop PR331 2.2 Ohm (SD011220B8L) Pop PC85 0.1u (SE00000Q900)	X01
22	60	Charger	7/28	TI	Pop adapter protection component for turbo mode with TI solution	Pop PR803 100k (SD03410038L) Pop PR804 78.7k (SD03478728L) Pop PR802 115k (SD034111538L) Pop PR801 1.87M ( ) Pop PQ801 RHU002N06 (SB50206008L) Pop PR812 100K (SD02810038L) Pop PC801 100P (SE071101J8L)	X01
23	58,59	Vcore VAXG_core	7/28	Compal	Fine tune load line and transient for Vcore and VAXG_core	Change PR140 to 11.8k (SD03411828L) from 12.4k (SD00000AJ8L) Change PR157 to 8.25k (SD03482518L) from 8.66K(SD03486618L) Pop PC701 and PC702 0.033uF (SE076333K8L)	X01
24	56	Selector	9/2	Compal	Change parts to HF parts	Change PQ51 FDN338P_G (SB90338001L) from FDN338P (SB90338008L) Change PD18, PD19, PD21, PD22, PD23, PD24, PD25, PD26, PD27, PD28, PD29, PD30 and PD31 RB751V-40GTE-17 (SCS00004L0L) from RB751V (SC1B751V08L) Change PQ37, PQ40, PQ41, PQ45 and PQ46 FDS6679AZ_G (SB000009D1L) from FDS6679AZ (SB000009D8L)	X02
25	46	+DCIN	9/2	Compal	Change parts to HF parts	Change PD6 DA204UGT106 (SC60000170L) from DA204UT106 (SC1A204U00L) Change PQ4 FDS6679AZ_G (SB000009D1L) from FDS6679AZ (SB000009D8L) Change PD1 RB715FGT106 (SCSB715F010) from RB715F (SCSB715F08L) Change PQ2 FDV301N_G (SB503010020) from FDV301N (SB50301008L)	X02
26	47	+5V/3.3 /+15VALW	9/2	Compal	Change parts to HF parts	Change PQ5 FDS8878_G (SB00000BV1L) from FDS8878 (SB00000BV8L)	X02
27	54	Charger	9/2	Compal	Change parts to HF parts	Change PQ33 SI4812BDY-T1-GE3 (SB00000DI1L) from SI4812BDY-T1-E3 (SB00000DI0L) Change PL17 FDVE1040-H-5R6M=P3 (SH00000CH1L) from FDVE1040-5R6M=P3 (SH00000CH0L) Change PQ27 SI4835DDY-T1-GE3 (SB00000FF1L) from SI4835DDY-T1-E3 (SB00000FF0L)	X02
28	48	+1.5V_SUS	9/2	Compal	Change parts to HF parts	Change PL602 FDUE1040D-H-1R0M=P3 (SH000009U1L) from FDUE1040D-1R0M=P3 (SH000009U0L)	X02

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29	47	+5V/3.3 /+15VALW	9/2	TI	Fine tune OCP setting for +5V/+3.3V	Change PR29 to 274K (SD03427438L) from 220K (SD03422038L) Change PR30 to 348K (SD00000WW8L) from 243K (SD03424338L)	X02
30	56	Selector	9/13	Compal	Change parts to HF parts	Change PQ39 and PQ44 SI4835DDY-T1-GE3 (SB00000FF1L) from SI4835DDY-T1-E3 (SB00000FF0L)	X02
<del>31</del>	<del>60</del>	<del>charger</del>	9/13	<del>Compal</del>	<del>Fine tune adapter protection circuit for 2nd source and reserve H_PROCHOT#</del>	<del>Delete PQ802 and PR807 MAX8731_IINP signal connect change to inverting input from Non inverting input ICREF signal connect change to Non inverting input from inverting input Depop PR811 and PR813 0 Ohm (SD02800008L) Depop PR814</del>	X02
32	56	+1.05VM	9/14	TI	Fine tune OCP setting	Change PR83 to 22k (SD03422028L) from 10k (SD03410028L)	X02
33	56	+1.05VM	10/05	Compal	22u/1206/6.3V COS issue	Change PC98 ~ PC105 to 22u/0805 (SE00000110L) from 22u/1206 (SE077226M8L)	X02
34	57	+1.05VTT	10/05	Compal	22u/1206/6.3V COS issue	Change PC123 ~ PC125, PC121, PC127, PC120, PC129 and PC130 to 22u/0805 (SE00000110L) from 22u/1206 (SE077226M8L) Change PC122 and PC126 to 47u/0805 (SE00000G60L) from 22u/1206 (SE077226M8L)	X02
35	52	DCIN	10/05	Compal	6 ~ 7mA leakage current in slice	Change PR2 and PR504 to 100K (SD02810038L) from 10K (SD03410028L)	X02
36	61	VCCSA	10/14	Compal	Fine tune VCCSA OCP setting for 2nd and 3rd source choke	Change PR247 and PR262 to 12.7k (SD03412728L) from 11.5k (SD03411528L)	X02
37	<del>63</del>	<del>GPU_Core</del>	<del>10/14</del>	<del>nVidia</del>	<del>Fix output voltage to 0.9V for nVidia ES sample</del>	<del>Depop PR337 and PR345 0 Ohm (SD02800008L) Depop PR347 10K (SD02810028L) Depop PR343 10K (SD02810028L)</del>	<del>X02</del>
38	63	GPU_Core	10/14	Compal	Change OCP setting for new nVidia chip	Change PR332 and PR339 to 5.9k (SD03459018L) from 4.22k (SD03442218L)	X02
39	63	GPU_Core	11/09	nVidia	Change VID setting for new nVidia chip. Default set 1V.	Depop PR347 10K (SD02810028L) Pop PR343 10K (SD02810028L) Change PR344 and PR400 to 3.09k (SD00000J38L) from 3.57k (SD03435718L) Change PR341 to 412k (SD00000678L) from 402k (SD034402380) Change PR403 to 38.3k (SD03438328L) from 200k (SD03420038L) Change PR338 to 71.5k (SD03471528L) from 0 Ohm (SD02800008L) Change PR334 to 30.1k (SD03430128L) from 23.7k (SD03423728L)	X03
40	62	Selector	11/09	Compal	Fine tune main and media battery switching to slice battery transient time	Change PC270 and PC265 to 0.22uF (SE000005Z8L) from 1uF (SE00000698L)	X03
41	60	Charger	11/09	Compal	Change adapter protection circuit trip point. (Adapter rated current + 0.75A)	Change PR802 to 107k (SD03410738L) from 115k (SD03411538L) Change PR801 to 649K (SD03464938L) from 1.87M (SD00000WN0L) Change PR804 to 80.6K (SD03480628L) from 78.7k (SD03478728L)	X03
42	60	Charger	11/09	Compal	Change adapter protection event to HW from SW	Pop PR814 0 Ohm (SD02800008L) Depop PR813 0 Ohm (SD02800008L) Depop PR812 100k Ohm (SD02810038L)	X03
43	60	Charger	12/09	Compal	H_PROCHOT# can not pull high issue with external circuit at DC mode	Change PR803.1 net nam to +3.3V_ALW2 from MAX8731_REF Change PQ801.3, PR804.1 and PC801.2 net nam to PGND from GAND_CHG	X04
44	60	Charger	12/09	Compal	H_PROCHOT# pull low level can not meet Intel SPEC with TI solution at AC mode	Depop PR801 (SD03464938L) Change PR802 to 174k (SD03417438L) from 107k (SD03410738L) Change PR803 to 150k (SD03415038L) from 100k (SD03410038L) Change PR804 to 113k (SD03411338L) from 80.6K (SD03480628L) Pop PR806, PR807, PR810 0 Ohm (SD02800008L) Pop PQ802 RHU002N06 (SB50206008L) Pop PR809 221k (SD00000HX8L) Pop PR808 1.8M (SD00000K180) Pop PR805 20K (SD03420028L) Depop PR811 (SD02800008L)	X04

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45	58,59,63	+Vcore +VAXG +VGPU	12/10	Compal	Change sunbber valure for 3rd source MOSFET	Change PC139, PC159, PC175, PC198, PC284 to 1000P (SE025102K8L) from 470P (SE024471J8L) Change PR117, PR148, PR173, PR193, PR331 to 1 Ohm (SD012100B8L) from 2.2 Ohm (SD011220B8L)	X04
46	60	Charger	12/17	TI	H_PROCHOT# spike voltage issue when AC to DC transient	Pop PR208 10k (SD02810028L)	X04
47	58,59	+Vcore +VAXG	12/17	Compal	Fine tune VAXG and Vcore load line for 2nd source choke	Change PR157 to 7.5k (SD03475018L) from 8.25k(SD03482518L) Change PR140 to 12.7k (SD03412728L) from 11.8k (SD03411828L)	X04
48	59	+VAXG	12/17	MAXIM	Low side driver no signal when loading over 10A	Change PR119 to 0 Ohm (SD01400008L) from 1 Ohm (SD014100B8L)	X04
49	60	Charger	01/12	Compal	Adapter protection trip point for 2nd source	Change PR802 to 162k (SD03416238L) from 174k (SD03417438L)	A00
50	52 ~ 63	ALL	01/12	Compal	Remove debug resistor (0 Ohm)	Change PR14,PR23,PR43,PR45,PR71,PR72,PR78,PR88,PR91,PR103,PR121,PR129,PR146,PR171,PR198 PR199,PR206,PR207,PR216,PR221,PR240,PR251,PR258,PR269,PR277,PR285,PR287,PR293,PR294 PR296,PR298,PR299,PR301,PR302,PR305,PR309,PR311,PR312,PR313,PR314,PR316,PR317,PR318 PR319,PR321,PR322,PR323,PR324,PR325,PR337,PR345,PR349,PR351,PR355,PR472,PR606 footprint	A00

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	7	HW	6/15/2010	COMPAL	Boot issue	Change QC1 control from SUS_ON to RUN_ON_CPU1.5VS3#	X01
2	11	HW	6/15/2010	COMPAL	Modify net name	Change +0.8V_VCC_SA to +VCC_SA	X01
3		HW	6/15/2010	COMPAL	Follow PPM recommendation to change material	Change capacitors from 10uF_0805_10V Y5V to 10uF_0805_6.3V_X5R: C305,C387,C462,C705,C728,C760,C764,C765,C768,C769,C772,CC135,CH58,CH73,CH80,CV124,CV126,CV185,CV187 Change capacitors from 10uF_0805_6.3V to 10uF_0603_6.3V: C475,C638,C641,C643 Change resistors to 0402 size: RC134, RH201,RH253,RH208,RH213 Delete RH192 and add PJP51	X01
4	14	HW	6/15/2010	COMPAL	De-pop PCH XDP	De-pop RH1, RH3~RH10, RH12~RH21, RH24, RH283~RH285, CH1	X01
5	14	HW	6/15/2010	COMPAL	Change HDA_SYNC topology	Add QH7 and RH37	X01
6	17,29,42	HW	6/15/2010	COMPAL	Change ODD connector from 13 pin to 31 pin	Change ODD connector to 31 pin, add @R1189,RH340 and remove C1168, C1169,C1170,U87,U88,U89, R1188 and short R1188 pin1 and pin2 together	X01
7	18	HW	6/17/2010	COMPAL	Remove touch screen PAID pull down circuit	Remove RH241	X01
8	18	HW	6/17/2010	INTEL	Follow Intel Design Guide Rev1.0	Change RH149 to 1k and RH150 to 4.7k	X01
9	22	HW	6/17/2010	COMPAL	Change EMC4002 to EMC4022	Change U9 to EMC4022, remove R392,R394 R866,R404,C279	X01
10	25	HW	6/17/2010	COMPAL	Change CRT SW to MAX14885	Change CRT SW to MAX14885 and add C1181,C1182, R1581 remove C325~C336	X01
11	26	HW	6/17/2010	COMPAL	Safety request	Add no stuff D4 and co-lay with F2, change F2 to 2A_8V	X01
12	28, 39	HW	6/17/2010	COMPAL	Change SATA repeater to MAX4951BE	Chagne U25, U44 to MAX4591BE and change R1169,R1171,R1174,R1176 to 0 ohm and stuff R1174,R1176	X01
13	30	HW	6/17/2010	COMPAL	Change Codec to ZB version and speaker connector	Change JSPK1 to TYCO_1734595-6 and change U72 to ZB version and stuff C962	X01
14	33	HW	6/17/2010	COMPAL	Add Jumper for power consumption measurement	Add PJP52,PJP55	X01
15	33	HW	6/17/2010	COMPAL	Change SI2301BDS to C version	Change Q36 to SI2301CDS	X01
16	33	HW	6/17/2010	BRCOM	Change RFID capacitors for more popular	Change C502,C505 from 1uF to 0.1uF	X01
17	35	HW	6/17/2010	COMPAL	Link R677 to CIS	Link R677 to CIS to have the correct part number	X01
18	37	HW	6/17/2010	COMPAL	Change express card power SW to TPS2231MRGPR-2	Change U41 to TPS2231MRGPR-2 and remove C636,C639	X01
19	41	HW	6/17/2010	COMPAL	Add pull down on SLICE_BAT_ON	Add R791	X01
20	42	HW	6/17/2010	COMPAL	Board ID	Change R875 to 130K	X01
21	46	HW	6/17/2010	COMPAL	BIOS request	De-pop DV1, RV29 and pop U14	X01

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22	11, 14, 42	HW	6/18/2010	COMPAL	EOL concern	Change CC176 to SGA00005H0L, change YH1, Y6 to SJ132P7KWLL	X01
23	43	HW	6/18/2010	COMPAL	Change connector	Change JKB1 to same as JSC1	X01
24	43	HW	6/18/2010	COMPAL	Change TP pin definition	Reverse TP pin definition for PT	X01
25	41, 42	HW	6/18/2010	COMPAL	Add series resistor and pull up resistors on MIC_MUTE#, VOL_MUTE, VOL_UP, VOL_DOWN	Add R773, R806, R884, R886, R887, R1166, R1167, R1184	X01
26	24, 45	HW	6/18/2010	COMPAL	Correct net name for LED signal	Modify signal name BREATH_BLUE_LED to BREATH_WHITE_LED and BREATH_BLUE_LED_SNIFF to BREATH_WHITE_LED_SNIFF	X01
27	26, 40, 41, 46	HW	6/21/2010	NVIDIA	Add HPD circuit to inform system for NV request	Add DV2, DV3, DV4, R1154 and use ECE5028 GPIOE7/DCD# as HPD signal to inform system	X01
28	32	HW	6/21/2010	INTEL	Remove useless resistors	Remove R556, R558, R559, R560 and short the pin1 and pin2 together	X01
29	24, 28, 29, 32, 37, 44, 49	HW	6/22/2010	COMPAL	Change part for Halogen free	Change Q18, Q27, Q30, Q34, Q38, Q40, Q42, Q49, Q54, Q58, QV5 to HF part	X01
30	10	HW	6/22/2010	COMPAL	To have better return path	De-pop CC130 and pop CC134	X01
31	44	HW	6/23/2010	COMPAL	Solution +1.5V_RUN voltage drop issue	Change Q59 from SI3456BDV to NTGS4141NT1G	X01
32	41	HW	6/23/2010	COMPAL	Remove double pull high resistor	Remove R1177	X01
33	29	HW	6/23/2010	COMPAL	Remove useless resistor	Remove R1125, R1126	X01
34	44	HW	6/25/2010	COMPAL	NTMS4107NR2G EOL	Change Q55 to NTMS4920NR2G	X01
35	10	HW	6/25/2010	COMPAL	CC129~CC134 D2T LESR5M EOL	Change CC129~CC134 to SGA00004X0L	X01
36	24	HW	6/25/2010	COMPAL	Change LVDS connector to 40 pin	Change JLVDS1 to 40 pin	X01
37	31	HW	6/25/2010	COMPAL	Change I/O connector to TYCO	Change JIO1 vendor from Lotes to TYCO	X01
38	24	HW	6/25/2010	COMPAL	PT panel change touch screen pin definition	Change JTS1 pin definition for new TS pin define	X01
39	14, 29, 36, 42	HW	7/1/2010	COMPAL	Modify Module Bay circuit	1. Remove R1181, R1182, R1189. 2. Change BAY_SMBUS, DEVICE_DET# pull up power rail from +3.3V_RUN to +3.3V_ALW. 3. Change net name ODD_DET# to PCH_SATA_MOD_EN#. 4. Add Q123, Q76, R513, R514, R515 for USB_SMI# circuit. 5. De-pop C627, R712	X01
40	24	HW	7/1/2010	COMPAL	Stuff PWM pull down resistor for PT solution	Pop R1137	X01
41	7	HW	7/1/2010	COMPAL	For support XDP device	De-pop RC9	X01
42	15, 18, 41, 42	HW	7/1/2010	COMPAL	Base on GPIO map to modify	1. Move SLP_ME_CSW_DEV# from GPIO45 to GPIO28, add MCARD_PCIE_SATA# on 5028 GPIOE3. 2. Remove RH238, change RH80 from 1k to 10k. 3. Change SLICE_BAT_PRES# pull up power rail from +3.3V_ALW2 to +3.3V_ALW. 4. Add R889	X01

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43	24	HW	7/1/2010	COMPAL	PWM function	Remove R1139,R1140 and add D68,D69	X01
44	11	HW	7/1/2010	COMPAL	VCCSA VID circuit	Change VCCSA_VID_0 to VCCSA_VID_1 and pop RC138	X01
45	36,45	HW	7/2/2010	COMPAL	Modify LED circuit	Remove R1578,R1579,R1580,D42,D60,D61, add Q77,Q124,R705,R718,R719	X01
46	22	HW	7/2/2010	COMPAL	Modify thermal diode for thermal request	Remove C268,C269, use DP1/DN1 for CPU,DP2/DN2 for GPU, DP3/DN3 for DIMM, DN5/DP5 for WWAM	X01
47	15,32	HW	7/5/2010	COMPAL	EOL concern	Change Y3 and YH2 from 1Y725000CE1A to 7A25000110	X01
48	11,24,27,45	HW	7/7/2010	COMPAL	Change part for Halogen free part	Change QC5 to NTR4501NT1G, U21,U24,U54,U55,U57 change to NC7SZ04P5X-G, Q21 change to FDC654P-G	X01
49	29	HW	7/7/2010	COMPAL	USB30 SMI circuit	Stuff R513 due to this pin is OD type on USB30 module	X01
50	29	HW	7/8/2010	COMPAL	Link CIS symbol	Link JSATA2 CIS symbol	X01
51	35	HW	7/9/2010	O2-Mirco	Add discharge circuit for +3.3V_RUN_CARD	Add R826 on +3.3V_RUN_CARD	X01
52	15,29,32,35,36,37	HW	7/9/2010	COMPAL	Move PCIE TX AC coupling capacitors close to PCH	Move C408,C409,C460,C461,C567,C568,C596,C597,C598,C599,C617,C618,C647,C648 to page 15 to close to PCH	X01
53	14	HW	7/12/2010	COMPAL	To solve SPI EA	Add R933,R935 on SPI chip select signals	X01
54	24	HW	7/12/2010	COMPAL	Link CIS symbol	Link JLWDS1	X01
55	28	HW	7/12/2010	COMPAL	Meet EA result	Stuff R493,R494	X01
56	24,30,35,38,39	EMI	7/12/2010	COMPAL	EMI request to solve EMI issue	Add R678,C757,L92,L93, and stuff L51,L52,L90, de-pop R736~R739,R1150,R1151, and remove R1106	X01
57	31,41,45	HW	7/13/2010	Dell	Remove Mic mute function and LED	Remove R773,R806,R1108,R1061,Q105 and delete MIC_MUTE# signal	X01
58	28	HW	7/13/2010	COMPAL	Follow EA result	De-pop R493,R494 and pop R495,R496	X01
59	29	HW	7/13/2010	COMPAL	Modify zero ODD circuit	Change ZODD_WAKE#,MODC_EN#,MOD_SATA_PCIE#_DET,USB30_EN connection	X01
60	33	HW	7/14/2010	COMPAL	Change power rail for smart card	Change R632,R635 pull up power rail from +3.3V_ALW to +3.3V_ALW_SC	X01
61	22	HW	7/14/2010	COMPAL	Reserve capacitor for WWAN thermal diode	Add @C277	X01
62	14,17,18	HW	7/14/2010	COMPAL	To solve back drive issue	Move SIO_EXT_SMI# from PCH GPIO1 to GPIO14, remove RH254, and change RH164 pull up power rail from +3.3V_RUN to +3.3V_ALW_PCH	X01
63	45	HW	7/14/2010	COMPAL	Remove CLIP	Remove CLIP3,CLIP4,CLIP6~CLIP8	X01
64	38,39	HW	7/15/2010	COMPAL	Remove one TPS2560 for cost saving	Remove U43,C659,C660,R740,PJP6, and share with power source of U45	X01
65	31,41,45	HW	7/15/2010	COMPAL	Remove speaker LED	Remove Q119,Q102,R1109,R1059	X01

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66	17, 18	HW	7/15/2010	COMPAL	Add pull up for PCH GPIO1	Add RH41 and change reference RH164 to RH41	X01
67	24, 30, 35	HW	7/16/2010	COMPAL	Change part reference for EMI request	Change L92 to LE92, L93 to LE93, R678 to RE678, CE757 to CE757	X01
68	20, 44	HW	7/16/2010	COMPAL	For cost saving	Add PJP57, RH202, no stuff QH4, Q49, RH278, R908	X01
69	22	HW	7/16/2010	COMPAL	Modify current sense connection	Move MAX8731_IINP from U9.25 to U9.31	X01
70	41, 42	HW	7/16/2010	DELL	Follow GPIO 0713	Add DYN_TURB_PWR_ALRT#, DYN_TUR_CURRNT_SET#, and change R796 pull up power rail from +3.3V_RUN to +3.3V_ALW	X01
71	35	HW	7/16/2010	COMPAL	Follow vendor request	De-pop RE678, CE757	X01
72	28, 45	HW	7/19/2010	COMPAL	Part leverage select	Change D16, D59, D62 to SC100000S0L	X01
73	14	HW	7/19/2010	COMPAL	Follow Intel XDP design	Change RH43, RH44, RH45 to 200 ohm	X01
74	38, 39	HW	7/19/2010	COMPAL	Change power rail for layout limitation	Change U90, U91 power rail to +USB_SIDE_PWR, U92 power rail to +SATA_SIDE_PWR	X01
75	46	HW	7/19/2010	NV	NV request to add 10k pull on GPIO9	Add RV102	X01
76	23	HW	7/20/2010	SMSC	Follow SMSC review result	Add R403	X01
77	31	HW	7/20/2010	COMPAL	Change USB3 (on IO/B) enable signal	Change USB3 enable signal from USB_SIDE_EN# to ESATA_USB_PWR_EN#	X01
78	31	HW	7/20/2010	COMPAL	Change JIO1 for correct connector list	Change JIO1 to TYCO_2041300-2	X01
79	46	HW	7/20/2010	NV	Follow NV request	Add RV103, RV104, @RV20, @RV25, @RV26 and de-pop R1111	X01
80	26	HW	7/20/2010	Safety	Follow safety request	De-pop F2, pop D4 and add R5	X01
81	17, 30, 40	HW	7/20/2010	EMI	Follow EMI request	Add RE1098, RE1100, RE1101, RE1102, CE573, CE574, change RH103, R756 to 33 ohm, C704 to 12pF	X01
82	14	HW	7/20/2010	COMPAL	Change SPI chip select damping R	Change R933, R935 to 47 ohm	X01
83	24, 39	HW	7/20/2010	COMPAL	Change material for small size	Change C300, C669 from 1206 16V to 0805 10V	X01
84	24	HW	7/20/2010	COMPAL	Change U86 power rail for touch screen	Change U86.4 power rail from +3.3V_RUN to +5V_RUN	X01
85	38, 39	HW	7/20/2010	COMPAL	Remove useless capacitors	Remove C1151~C1154	X01
86	41	HW	7/20/2010	COMPAL	Follow GPIO map	Change R796 to 10k ohm, add R764	X01
87	44	HW	7/20/2010	COMPAL	Change PJP57 footprint	Change PJP57 footprint to 4x4m	X01
88	31	HW	7/21/2010	COMPAL	Modify HP & Mic circuit	Change JIO1 pin connection	X01
89	36	HW	7/21/2010	COMPAL	Add 0 ohm R on PCIE_MCARD2_DET#	Add R725	X01
90	40	HW	7/21/2010	COMPAL	Follow EA request	Change C704 to 6.8pF	X01

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91	35	HW	7/21/2010	COMPAL	Change JSD1 to support Memory Stick	Change R666,R667, change JSD1	X01
92	31, 42	HW	7/22/2010	COMPAL	GPIO MAP update.	add R1590	X01
93	39	HW	7/22/2010	COMPAL	Follow Vender request.	add R1582~R1585	X01
94	39	HW	7/23/2010	COMPAL	To compatible with SN75LVCP601	Add R1586~R1589	X01
95	41	HW	7/23/2010	COMPAL	Add 0 ohm R on TEMP_ALERT# for backup	Add R1591	X01
96	24, 42	HW	7/24/2010	COMPAL	Follow GPIO map to add touch screen power down control circuit	Add TOUCH_SCREEN_PD#, Q125,Q32,R430,R431,C304,C306, and change JTCH1 pin 1,pin2 from +5V_RUN to +5V_TSP	X01
97	24	HW	7/26/2010	COMPAL	Reserve a 0 ohm resistor for +5V_TSP	Add R1592	X01
98	45	HW	7/26/2010	COMPAL	Add pull down 100k on BT_ACTIVE	Add R950	X01
99	48	HW	7/27/2010	NV	Follow NV suggestion to modify BOM	De-pop CV184, and change CV183 to 1uF,CV182 to 4.7uF, CV109 to 470pF,CV110 to 4700pF, LV8 to 100nH	X01
100	37	HW	8/23/2010	COMPAL	Add connection for express card SW	Add connection of pin4,pin5,pin13 and pin 14	X01
101	18	HW	8/23/2010	Intel	Follow Intel design guide Rev1.2	Change RH149 to 2.2k and RH150 to 0 ohm	X01
102	46	HW	8/23/2010	COMPAL	De-pop pull up resistors	De-pop RV23,RV24	X01
103	14, 18, 30	HW	8/23/2010	DELL	Remove PAID function of RTC and speaker	Change speaker connector to 4 pin and remove RTC_DET# and SPEAKER_DET#	X01
104	17	HW	8/26/2010	Intel	Follow Intel check list rev1.2	Add @RH332	X01
105	14, 18	HW	8/26/2010	Intel	Follow Intel request	Add RH51 and RH356	X01
106	33	HW	8/27/2010	BRCOM	Follow BRCOM request	Change L39,L40 to rated current is 400mA	X01
107	45	HW	8/27/2010	COMPAL	Follow ME request	Change H17 to 2P2	X01
108	16	HW	8/27/2010	COMPAL	Reserve pull down R for ME_SUS_PWR_ACK	Add @RH145	X01
109	36	HW	9/2/2010	COMPAL	De-pop ESD diode	De-pop U40	X01
110	11	HW	9/2/2010	COMPAL	Change QC5 VGS to 20V part	Change QC5 to SB00000HK0L	X01
111	45	HW	9/3/2010	COMPAL	Follow ME request	Change H11 from 3P8 to 3P7	X01
112	26	HW	9/3/2010	COMPAL	Follow safety request	Pop F2 and de-pop R5	X01
113	46, 47, 48, 49	HW	9/6/2010	COMPAL	Change GPU to N12P FERMI	Change UV1 to N12P FERMI	X01
114	24, 26, 46	HW	9/8/2010	COMPAL	Change RB751V to HF part	Change D53,D63~D69,DV1~DV4 to SCS00004L0L	X01

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115	30, 31	HW	9/9/2010	IDT	To solve pop noise and detect issue	Add U6, Q33, Q46, D70, D71, R425, R33, R38, R424, R161, R352, R1088, C967, C307, C308	X01
116	35	HW	9/10/2010	O2	To solve RF noise issue	Add @C573, @C574, L45	X01
117	50, 51	HW	9/14/2010	COMPAL	Change VRAM to 800MHz	Change UV3~UV6 to SA00003VS0L	X01
118	30, 38, 39	HW	9/14/2010	COMPAL	For EMI request	Change C973~C976 to 680pF and pop, add L91~L94, D72~D74, remove U90~U92	X01
119	35	HW	9/14/2010	O2	Modify circuit	Remove R661, R662, add L46, L47, change L45 to SM01000GG0T	X01
120	17, 24	HW	9/15/2010	COMPAL	To support high contrast ratio brightness	Change net name from LVDS_CBL_DET# to LVDS_CBL_ID	X01
121	37, 38, 39	HW	9/16/2010	COMPAL	change materials	Change L49, L51, L52, L90 to SM070001E0L	X01
122	46, 48, 50, 51	HW	9/20/2010	Nvidia	Vender request	add CV89, CV176, CV177, CV178, CV188~CV192, RV30, RV31, change RV81/86 to 160ohm RV59 to 15K, CV80 to 4.7uF, CV40, CV58, CV59, CV60 to 0.1u, CV41, CV42, CV43, CV50, CV51 to 0.022u. CV160~CV162 to 1u, CV181 to 10u CV180 to 22u, pop RV99 and change it to 20K pop RV41 and change to 4.99K, de-pop RV50, pop RV56. Rename from I2CS_SCL/SDA to I2CH_SCL/SDA	X01
123	48	HW	9/28/2010	Nvidia	Vender request	Change LV3 to SM01000BE0L (220ohm)	X01
124	24	HW	9/28/2010	COMPAL	solve PWM leakage issue.	Change R1137 to 10Kohm	X01
125	46	HW	9/28/2010	COMPAL	solve system can't boot in UMA only mode.	correct from U14 to UV14 and change the PN to SA00003Y00L. pop RV29, <del>de-pop RV22</del>	X01
126	14	HW	10/01/2010	COMPAL	DG1.5 update.	add RH31	X01
127	32	HW	10/04/2010	COMPAL	GPIO MAP update.	add U15, C478.	X01
128	45	HW	10/04/2010	COMPAL	LED brightness test result	change R957 to 1K, R955, R941, R949, R939, R934 to 4.7K	X01
129	32	HW	10/07/2010	COMPAL	Solve LAN Package Lost Problem	change L30~L37 from 22NH to 12NH.	X01
130	9	HW	10/07/2010	COMPAL	DG1.5 update.	depop RC96, RC97	X01
131	30	HW	10/07/2010	COMPAL	change Codec to YA version.	change the PN from SA00003ZZ1L to SA00003ZZ2L	X01
132	17, 24, 41	HW	10/11/2010	COMPAL	Follow GPIO Map	Change LVDS_CBL_ID to ATG_MAC_LCD_DET#, remove R771	X02
133	31	HW	10/11/2010	DELL	Remove Latitude On button	Depop SW2	X02
134	28	HW	10/12/2010	DELL	Support SSD	Add PJP64, C399, C402	X02
135	31	HW	10/18/2010	IDT	Change GND reference	Change Mic detect circuit DGND to AGND	X02
<del>136</del>	<del>30</del>	<del>HW</del>	<del>10/19/2010</del>	<del>COMPAL</del>	<del>Change Mic detect to external detect</del>	<del>Remove R161 and add C1164</del>	<del>X02</del>
137	14, 18	HW	10/19/2010	COMPAL	Follow Intel debug port DG	Connect PCH_GPIO15 to PCH_XDP	X02

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# Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
138	42	HW	10/19/2010	COMPAL	Change board ID to X02	Change R875 to 62k	X02
139	30, 31	HW	10/21/2010	COMPAL	Modify Mic detect circuit	1. Add PJP65, 2. Change C307,C308 to 0402 size 3. Change C308 connection, 4. Change Mic detect power from +5V_ALW to +5V_RUN, 5. De-pop Q33,Q46,R424, 6. Move C1180 to +VREFOUT_R	X02
140	18	HW	10/22/2010	COMPAL	Follow check list rev1.0	Change RH177 to 10k	X02
141	31	HW	10/26/2010	COMPAL	Cost saving	Change C307,C308 to 0402 package	X02
142	34	HW	10/26/2010	COMPAL	Follow BRCOM request	Pop C1161	X02
143	14~21	HW	10/28/2010	Intel	Change PCH stepping	Change UH4 to B2 stepping	X02
144	30, 31	HW	10/28/2010	COMPAL	Use internal Mic detect circuit	De-pop D71,R425,R33,R38,C307,C308,U6, R352,R1088,C967	X02
145	47	HW	11/1/2010	NV	Solve HDMI audio issue	De-pop RV41, change RV97 to 34.8K and stuff it	X02
146	47	HW	11/1/2010	NV	Chagne Device ID to 0x1056	De-pop RV51,change RV57 to 34.8k and stuff	X02
147	47	HW	11/1/2010	NV	Follow NV request	De-pop RV60, change RV54 to 10k and stuff it, change RV52 to 4.99k	X02
148	15	HW	11/5/2010	COMPAL	To fix ME issue	De-pop RH296,RH297, pop QH5,RH302,RH303	X02
149	37	HW	11/16/2010	COMPAL	To fix soldering issue	Change express card connector JEXP1 to TAISOL 5-421005002000-9	X02
150	28	HW	11/17/2010	Intel	Follow Intel CRB design	Change R501,R502 to 10k	X02
151	12, 13	HW	11/18/2010	COMPAL	Follow part reference design rule	Change JDIMMA1 & JDIMMB1 to JDIMM1 & JDIMM2	X02
152	46, 47, 48, 49	HW	11/18/2010	NV	Change GPU to QS sample	Change UV1 to N12P-NS-S-A1	X02
153	28, 44	HW	11/19/2010	COMPAL	For cost saving	De-pop R499,R500,C393,Q28,R905,R907,C762,Q51	X02
154	31	HW	11/22/2010	COMPAL	Follow part reference design rule	Change JMEDIA1 to JMDIA1	X02
155	14	HW	11/22/2010	COMPAL	Change SPI ROM to version C	Change U52 to SA000039A1L, U53 to SA00003F01L	X02
156	46	HW	12/03/2010	COMPAL	Solve GPU reset timing issue	Add RV33 100Kohms pull up to +3.3V_RUN and de-pop RV22	X02
157	42	HW	12/03/2010	COMPAL	Follow INTEL DG1.5 RSMRST# timing cicuit	Just add RSMRST# circuit for backup. but de-pop	X02
158	46	HW	12/07/2010	COMPAL	Solve GPU reset timing issue	de-pop RV33 and pop RV22	X02
159	18	HW	12/07/2010	COMPAL	Audio MIC detect selection	de-pop RH269 and add RH273 1Kohms pull low	X02
160	33	HW	12/17/2010	COMPAL	Follow NXP design guide	Add @C575	A00

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
160	14	HW	12/17/2010	COMPAL	For cost saving	De-pop RH47, RH48, RH49, RH288	A00
161	42	HW	12/20/2010	COMPAL	Change Board ID	Change R875 to 33k	A00
162	42	HW	12/21/2010	COMPAL	To solve backdrive issue	Pop Q45	A00
163	33, 34	HW	12/24/2011	COMPAL	Change USH chip to CID7	Change U33 to SA00003AO1L	A00
164	34	HW	1/6/2011	COMPAL	update TPM/TCM pop option table	Correct pop option table	A00
165	ALL	HW	1/11/2011	COMPAL	For cost saving	Change 125pcs 0402 0 ohm resistors and 3pcs 0603 0 ohm footprint to new footprint which is short pin1 and pin2	A00

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