

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : SVCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : SGND1
LAYER 8 : BOT

Cable Docking

- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

PAGE 38

SYSTEM CHARGER ISL6251AHAZ- PAGE 39

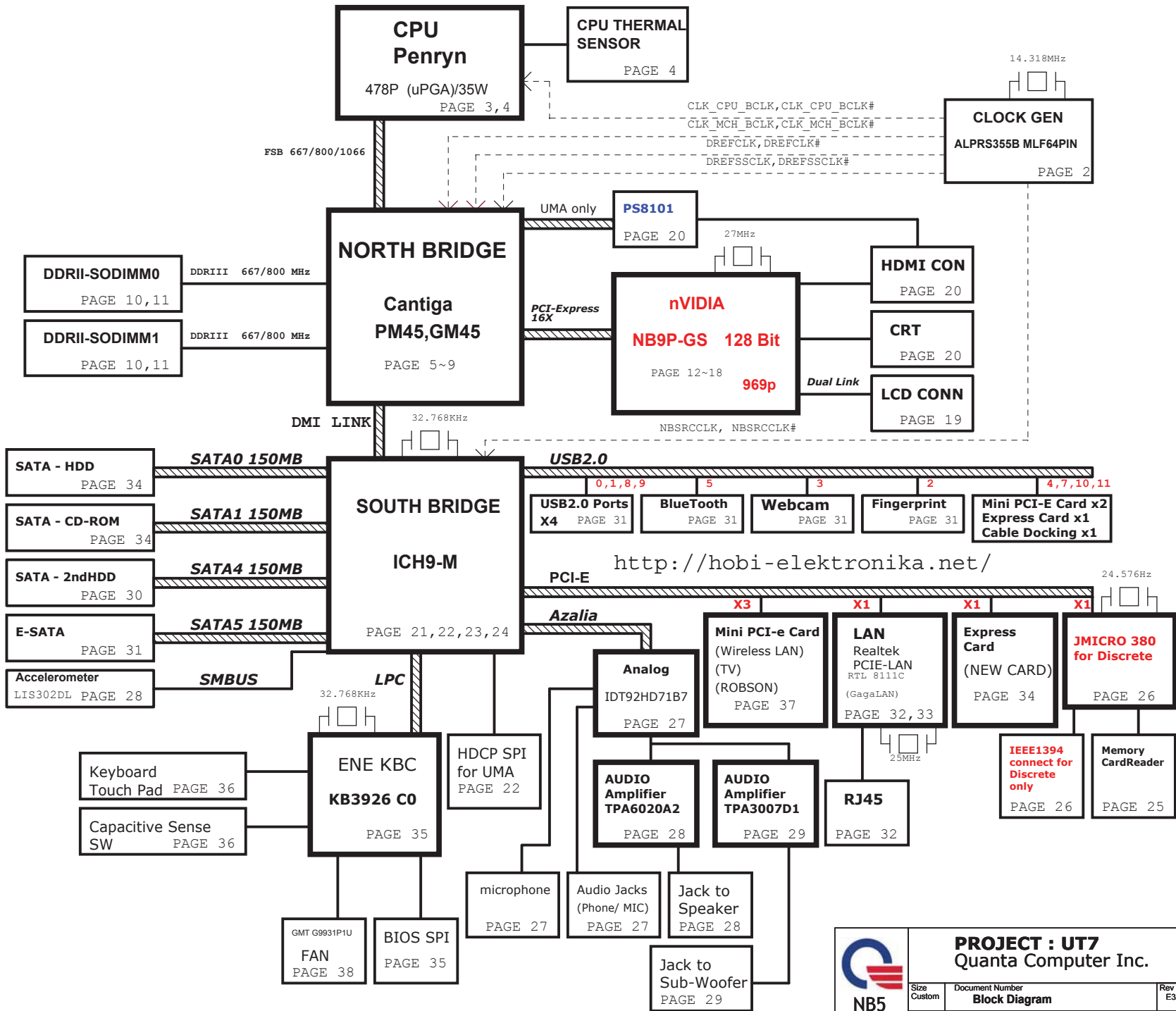
SYSTEM POWER ISL6237IRZ-T PAGE 40

DDR II SMDDR_VTERM 1.8V/1.8VSUS(TPS51116REGR) PAGE 44

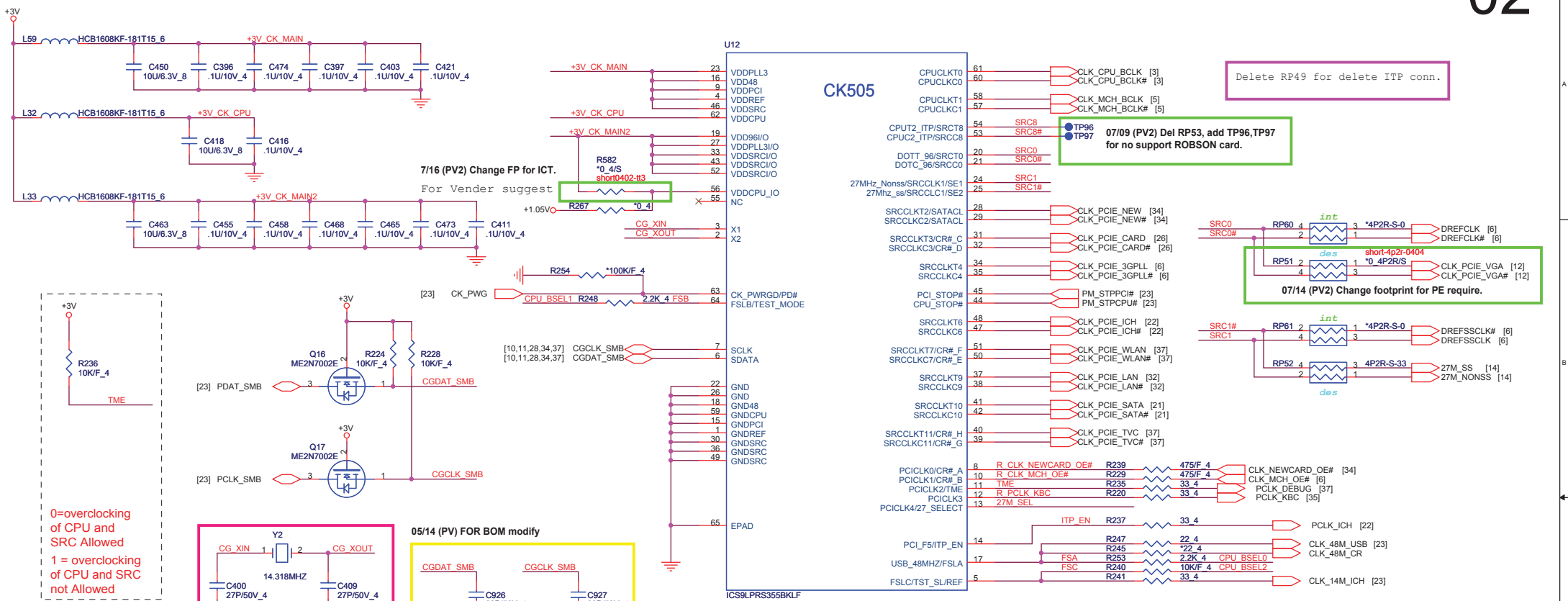
VCCP +1.5V AND GMCH 1.05V(RT8204) PAGE 44

VGACORE(1.025V)Oz8118 PAGE 43

CPU CORE ISL6266A PAGE 42



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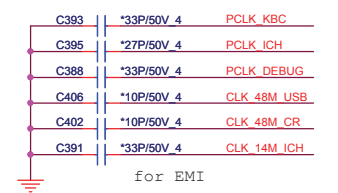
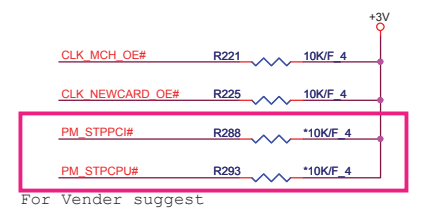
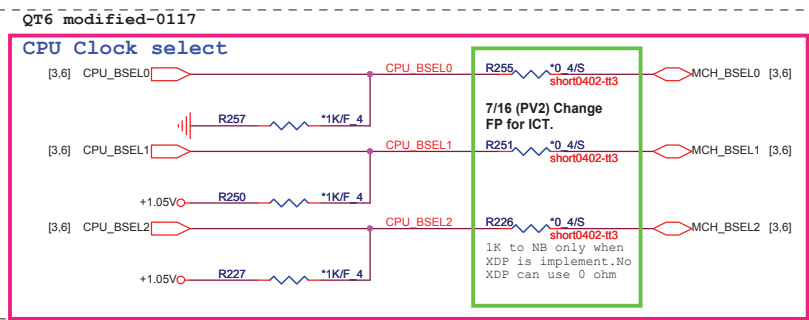
<http://hobi-elektronika.net/>

CK505 QFN64

ICS	ICS9LPRS355BKLF	ALPRS355000
Silego	SLG8SP513VTR	AL8SP513000
Realtek	RTM875N-606-VD-GR	AL000875000

27M_SEL PIN13	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

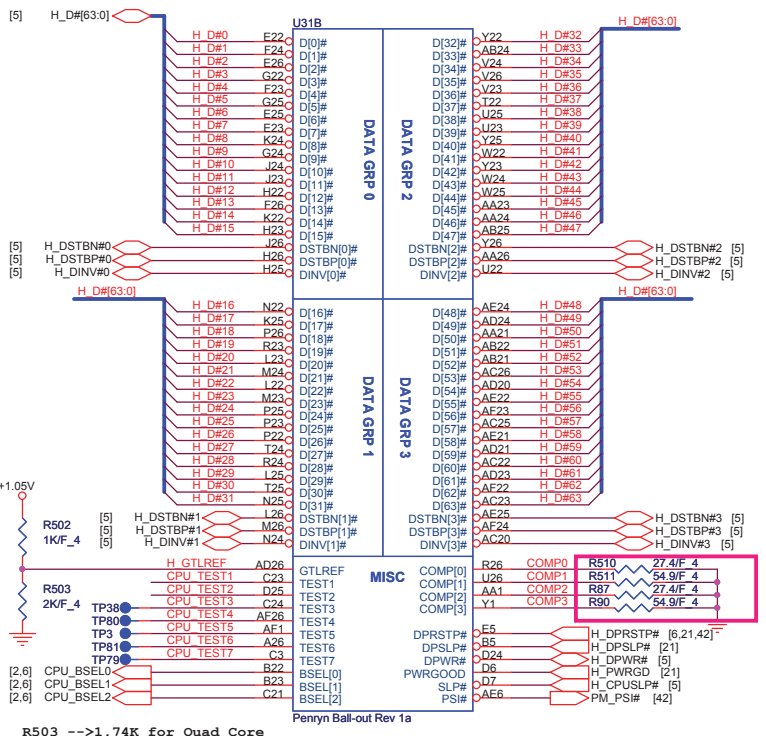
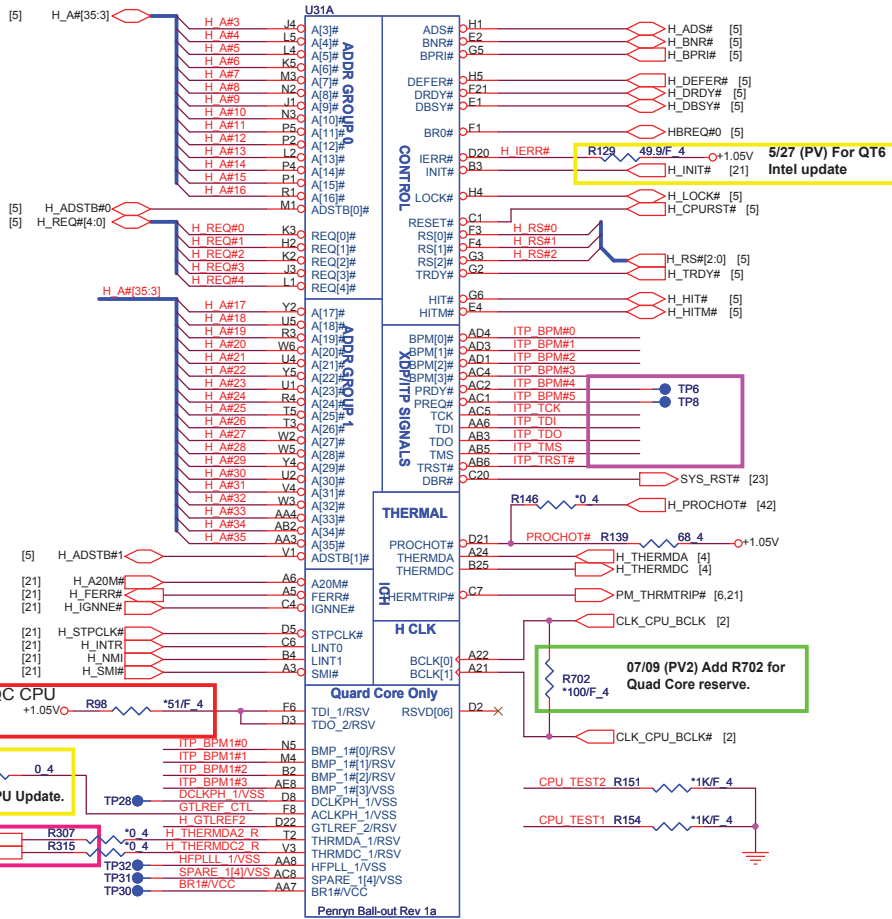


PROJECT : UT7
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NB5

Size Custom Document Number **Clock Generator** Rev E3A

Date: Friday, July 18, 2008 Sheet 2 of 46



	COMP0/2	COMP1/3
Dual Core	27.4 Ohm (CS02742FB19)	54.9 Ohm (CS05492FB19)
Quad Core	24.9 Ohm (CS02492FB29)	49.9 Ohm (CS04992FB31)

NI for Quad Core

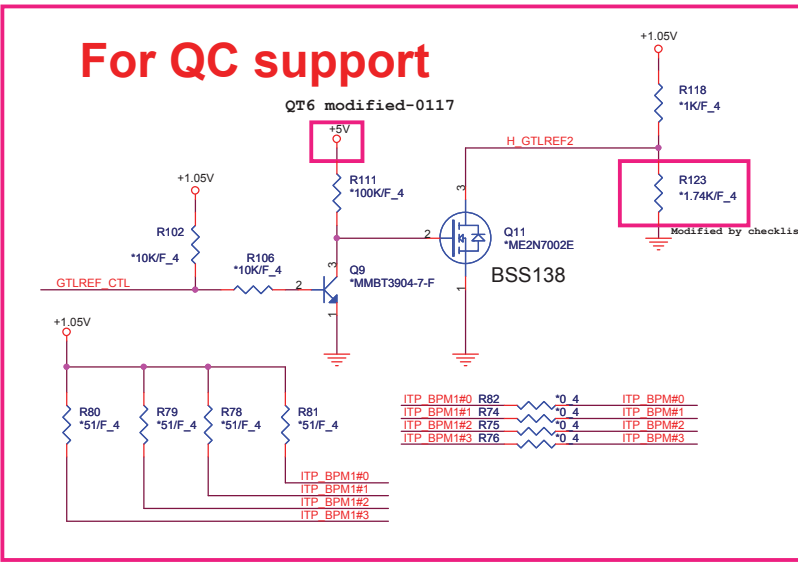
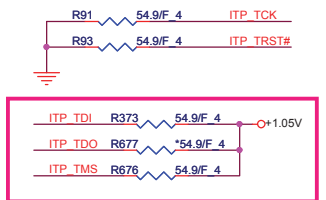
For QC CPU
+1.05V R98 *51/F_4

05/20 (PV) FOR INTEL CPU Update.

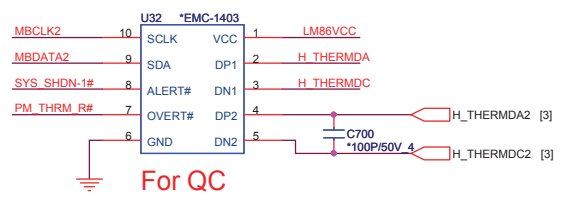
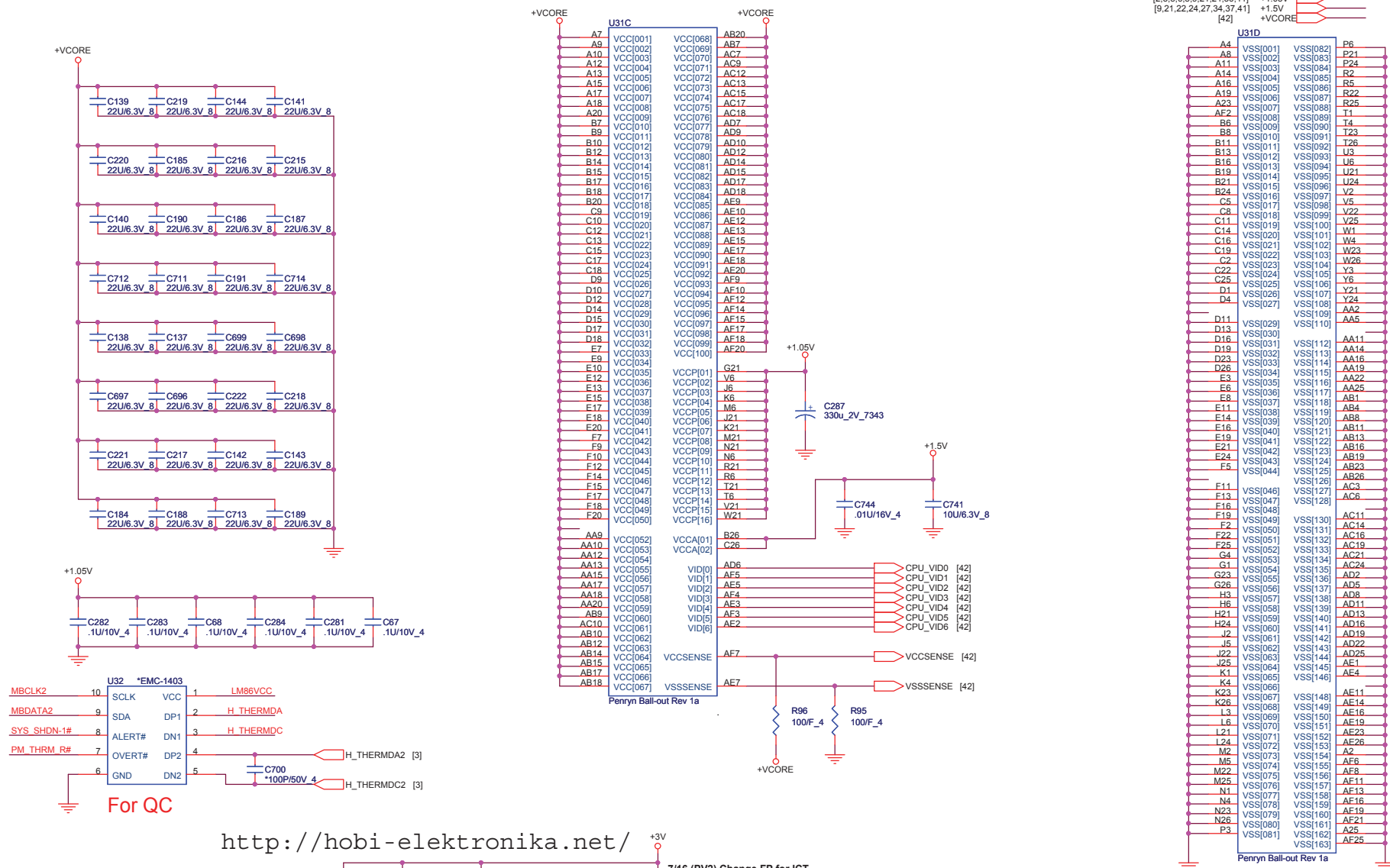
For QC CPU

MODEL	UT7 Quad Core	UT6 Dual Core
R696	*0_4	0_4

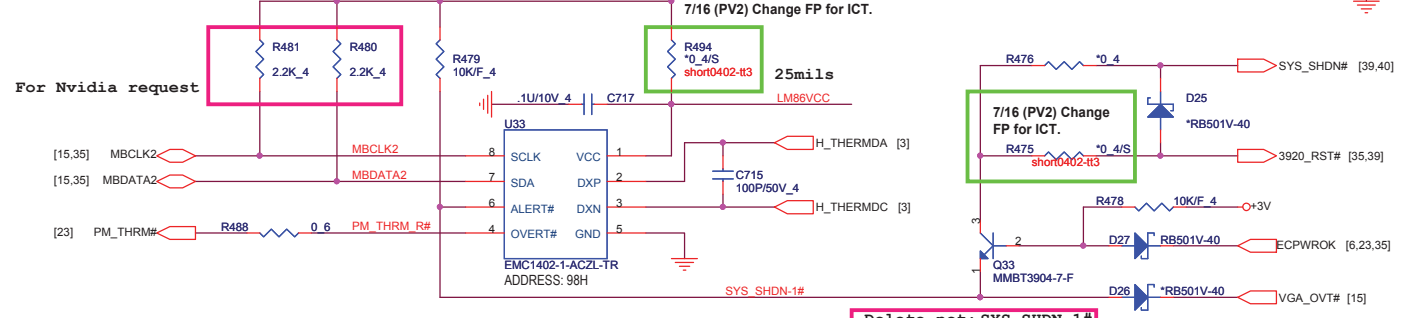
Populate ITP700Flex for bringup



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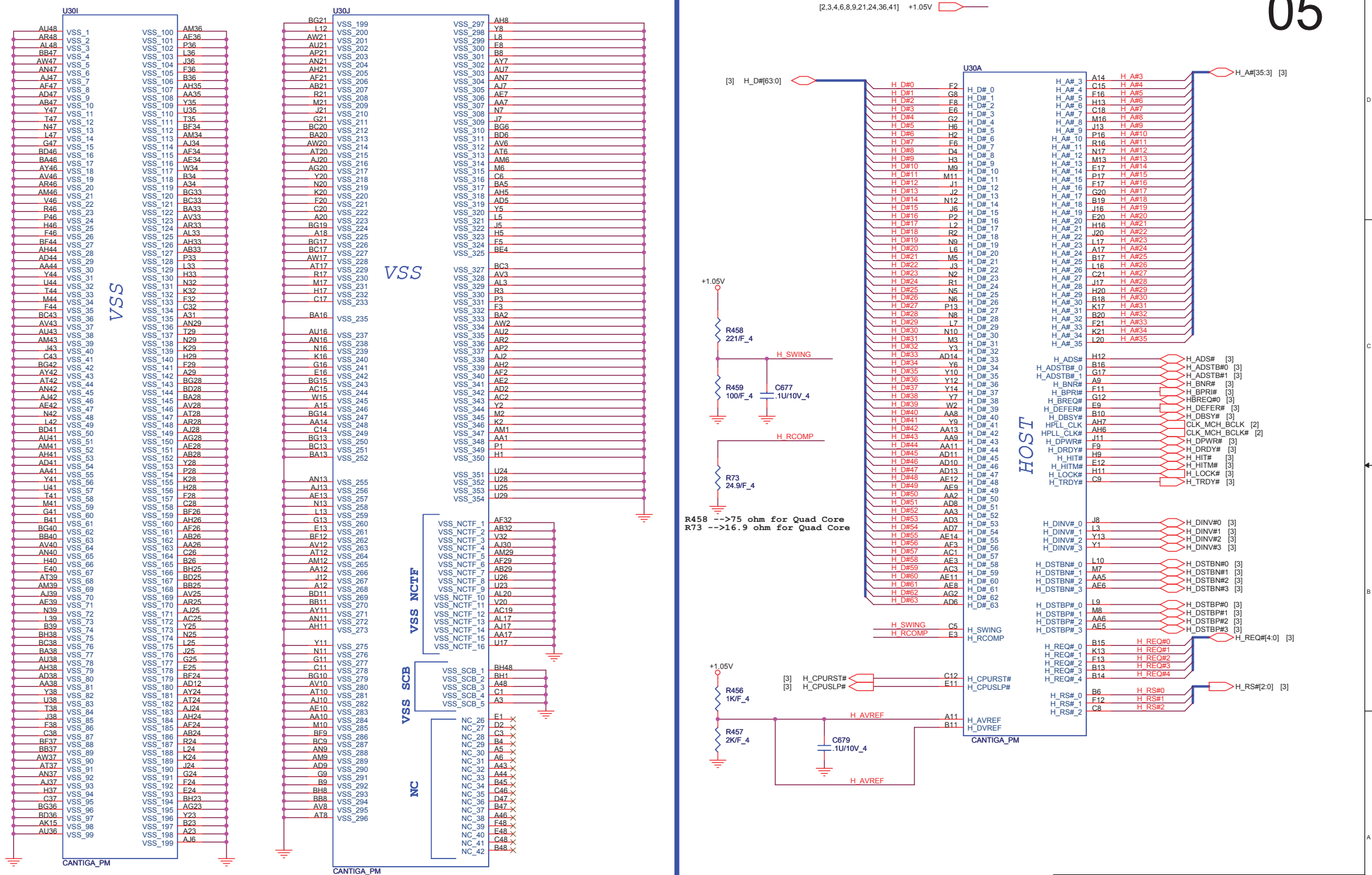
PROJECT : UT7
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NB5

Size Custom Document Number Penryn & TH Monitor 2/2 Rev E3A

Date: Friday, July 18, 2008 Sheet 4 of 46

[2,3,4,6,8,9,21,24,36,41] +1.05V



PROJECT : UT7
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NB5

Size Custom Document Number **Cantiga Host & VSS 1/5** Rev E3A

Date: Friday, July 18, 2008 Sheet 5 of 46

MCH_CFG_5 DMIx2 selection
 Low = DMI X2
 High = DMI X4 (Default)

MCH_CFG_16 FSB Dynamic ODT
 Low = Dynamic ODT disabled
 High = Dynamic ODT enabled (default)

MCH_CFG_9 PCI Express Graphic Lane
 Low = Reverse Lane
 High = Normal operation(Default)

MCH_CFG_19 DMI Lane Reversal
 Low = Normal operation (Default)
 High = Reverse Lanes

MCH_CFG_6 ITPM Host Interface
 Low = The ITPM Host Interface is enabled
 High = The ITPM Host Interface is disabled (default)

MCH_CFG_7 Intel(R) Management Engine Crypto
 Low = Intel(R) Management Engine Crypto
 TLS cipher suite with no confidentiality
 High = Intel(R) Management Engine Crypto
 TLS cipher suite with no confidentiality (Default)

MCH_CFG_10 PCIe Lookback Enable
 Low = Enabled
 High = Disabled (Default)

MCH_CFG_12/13 XOR/ALLZ/CLOCK Un-gating

MCH_CFG_13 MCH_CFG_12 Configuration

0	0	Reserved
0	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

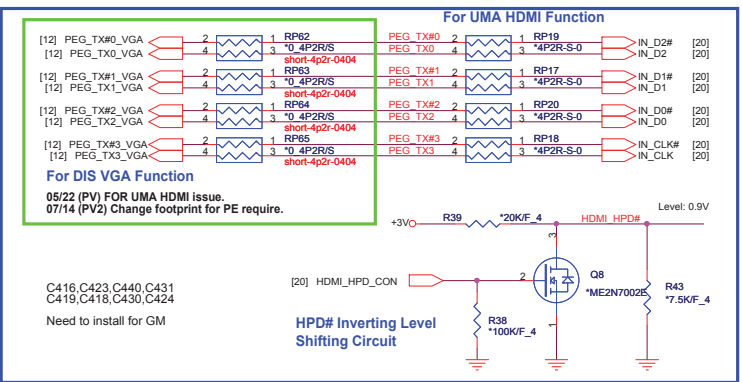
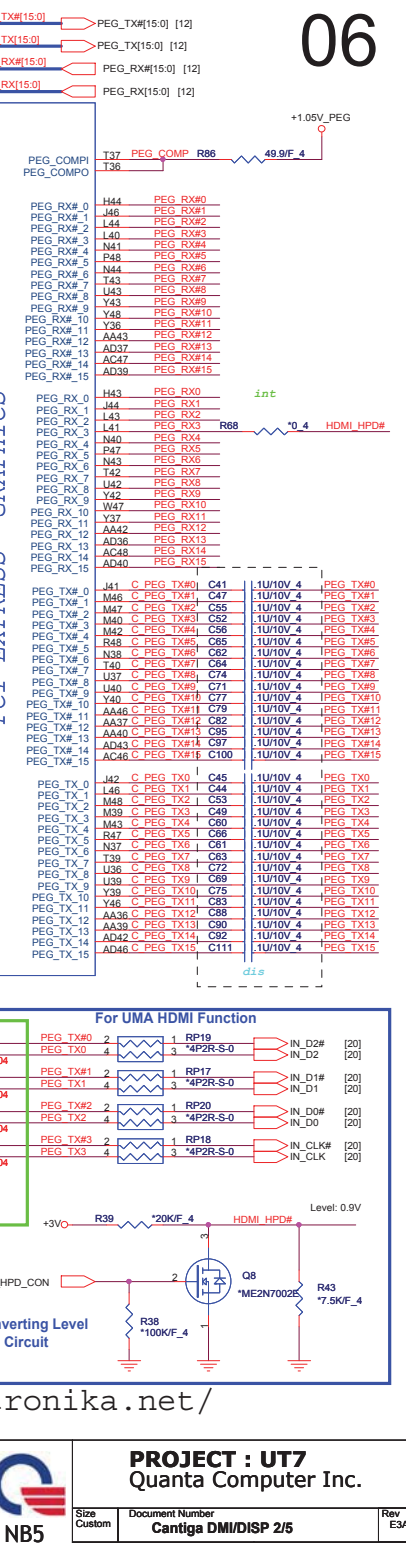
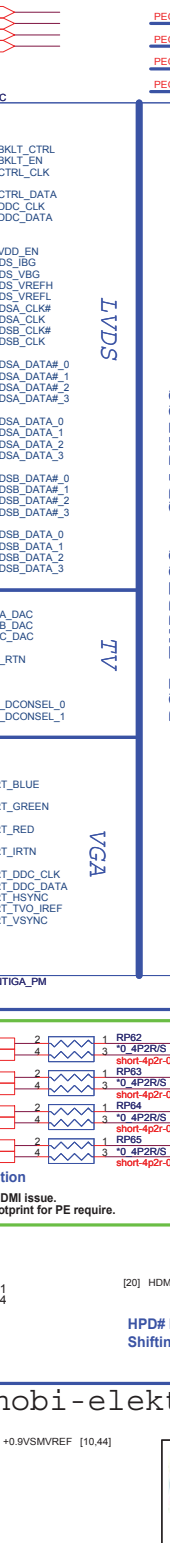
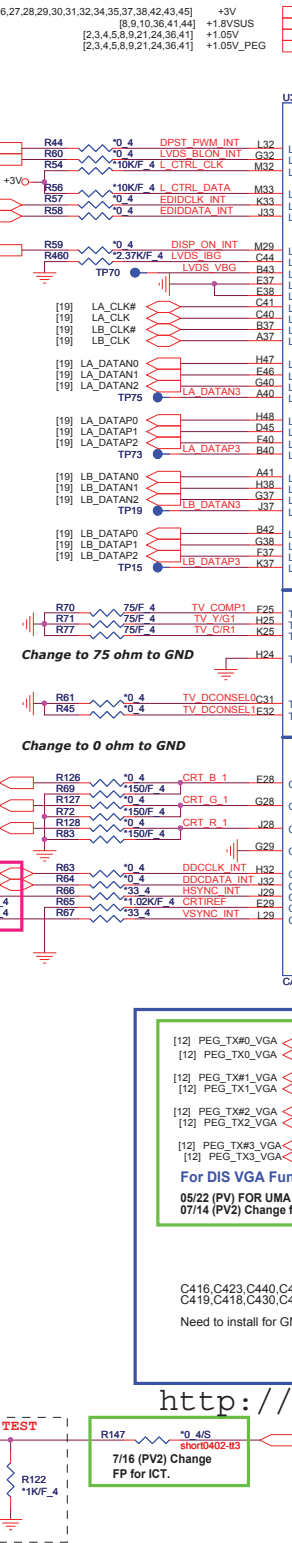
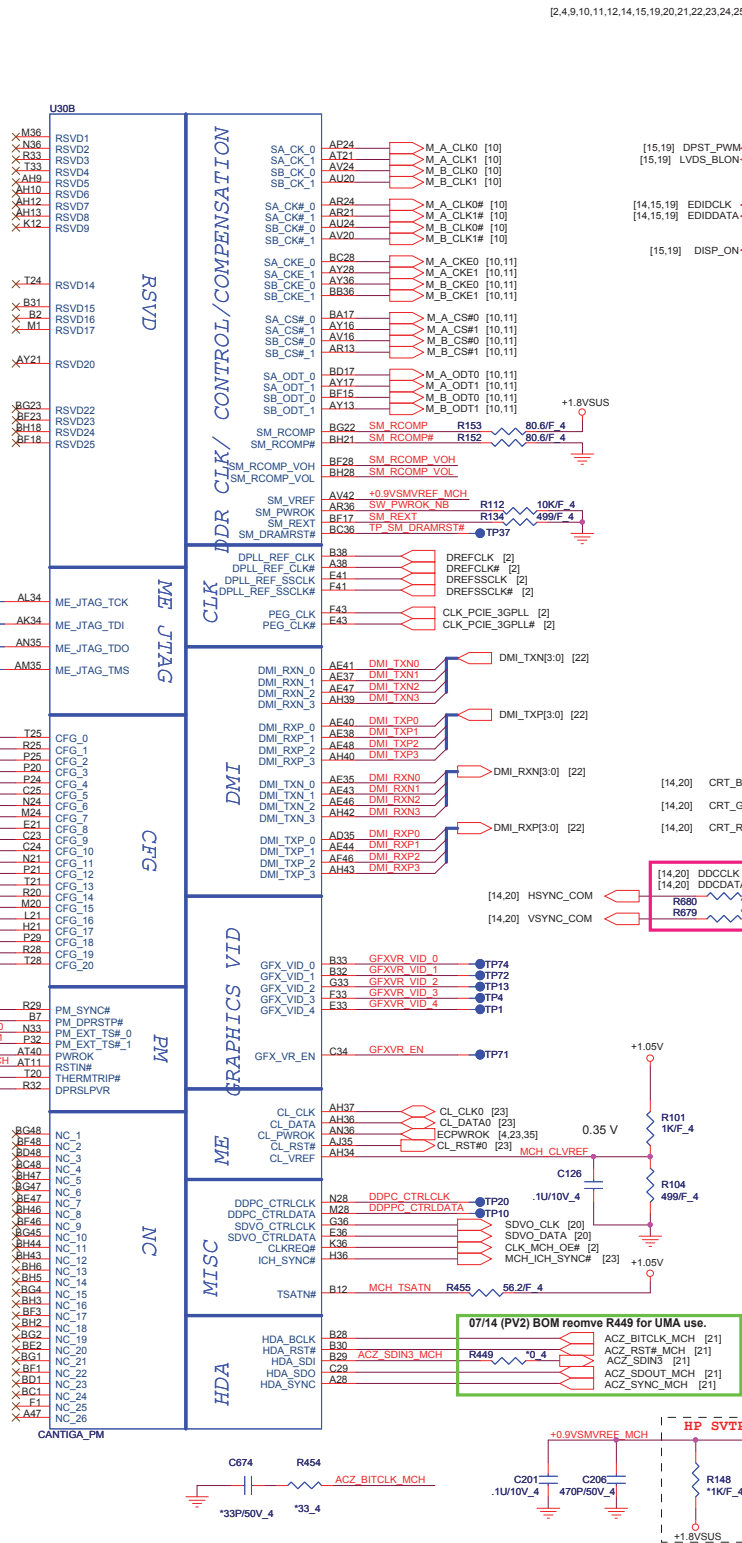
MCH_CFG_20

000	= FSB1066
010	= FSB800
011	= FSB667
Others	= Reserved

Digital Display Port (SDVO/DPI/HDMI) Concurrent with PCIE
 Low = Only digital display port (SDVO/DPI/HDMI) or PCIE is operational (default)
 High = Digital display port (SDVO/DPI/HDMI) and PCIE are operating simultaneously via the HPD port

MCH_CFG2:0

TP34	AL34	ME_JTAG_TCK
TP33	AK34	ME_JTAG_TDI
TP36	AN35	ME_JTAG_TDO
TP35	AM35	ME_JTAG_TMS

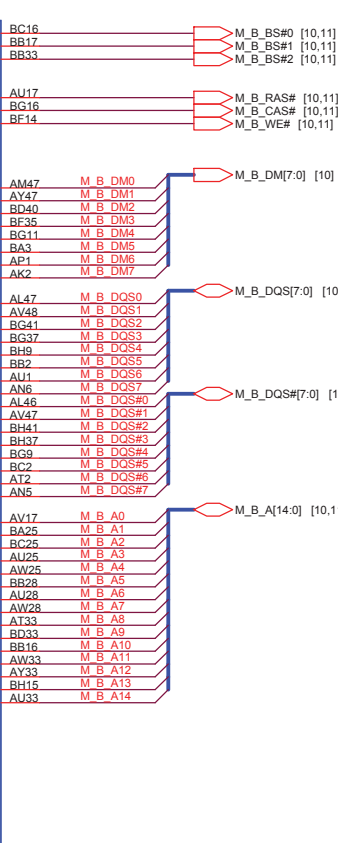
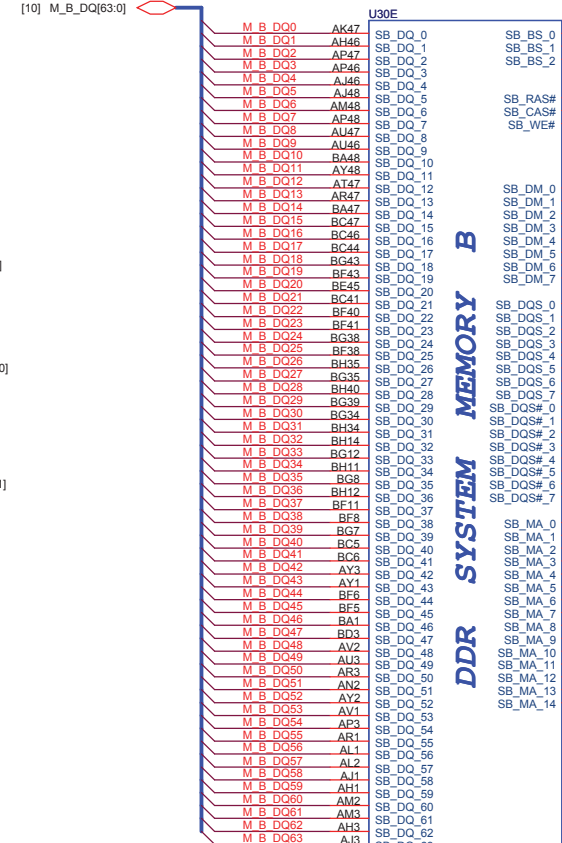
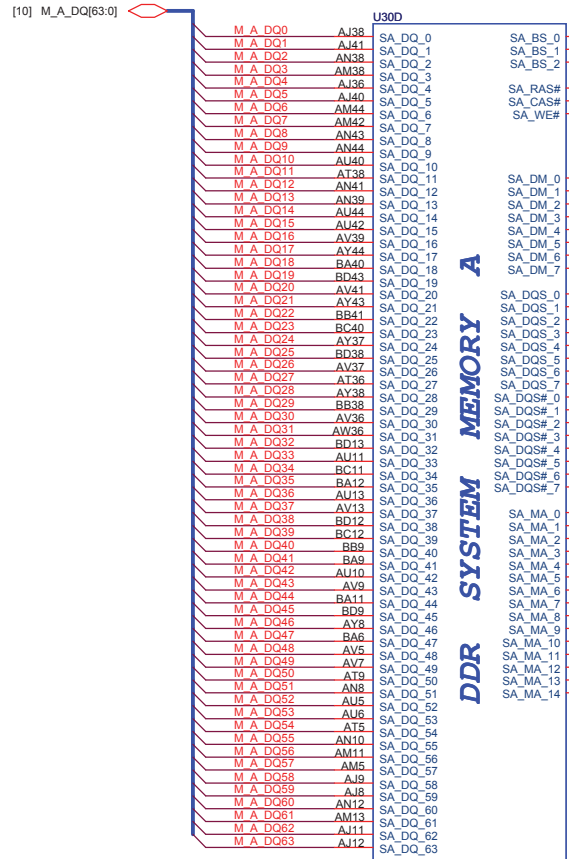


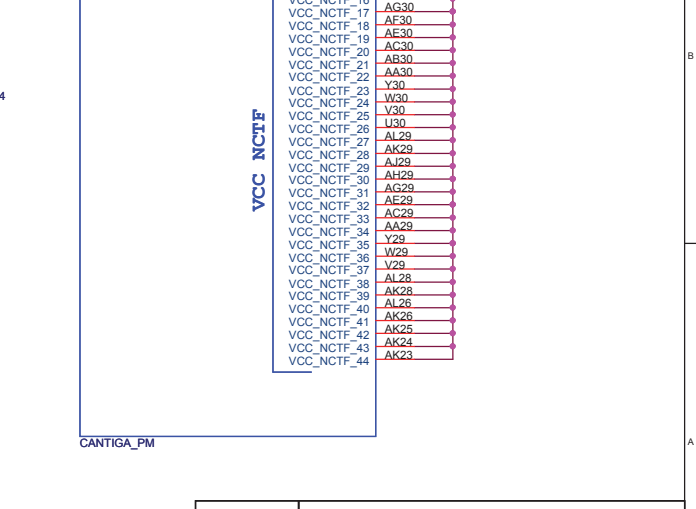
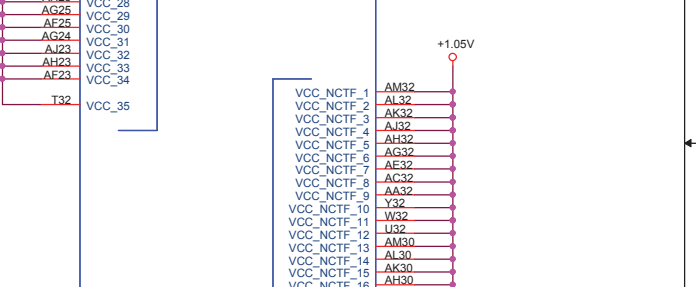
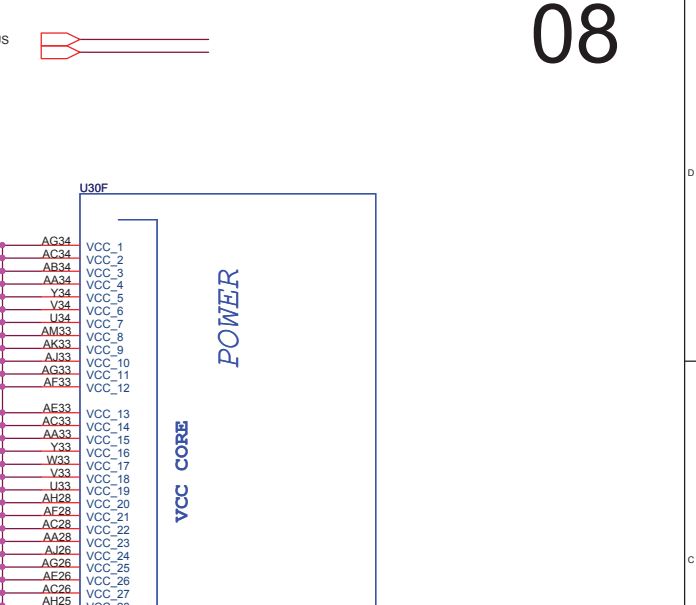
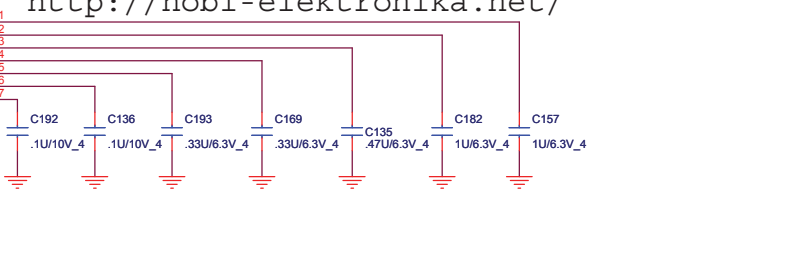
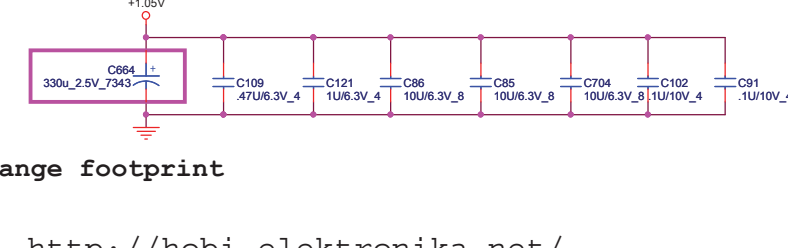
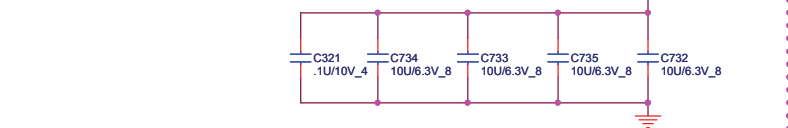
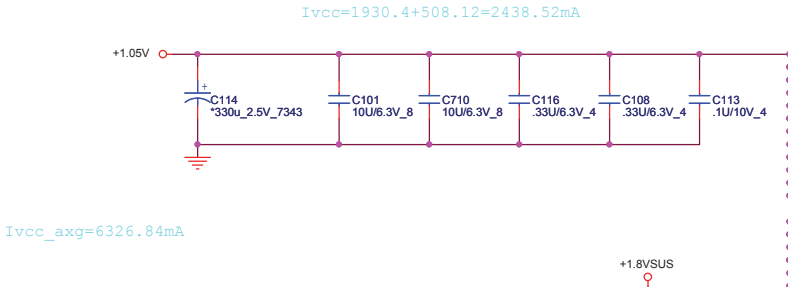
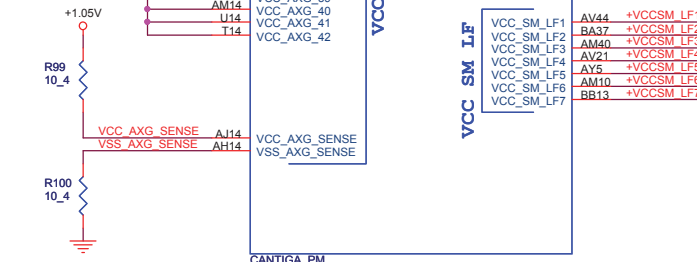
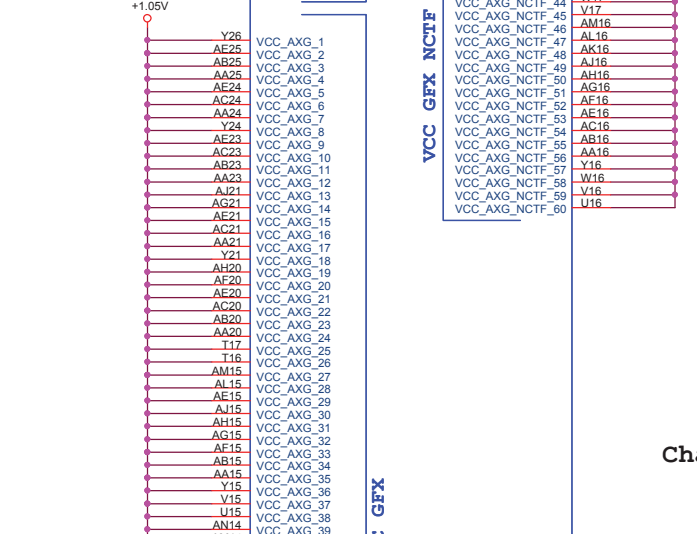
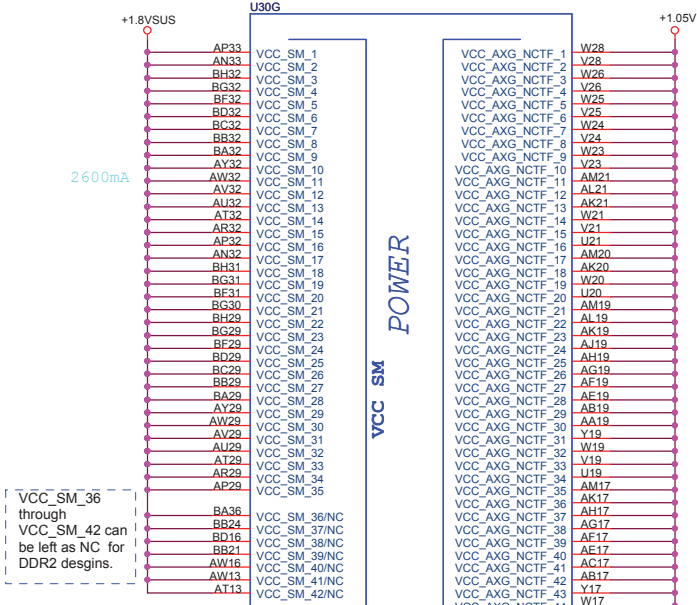
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PROJECT : UT7
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Size Custom Document Number
Cantiga DMI/DISP 2/5

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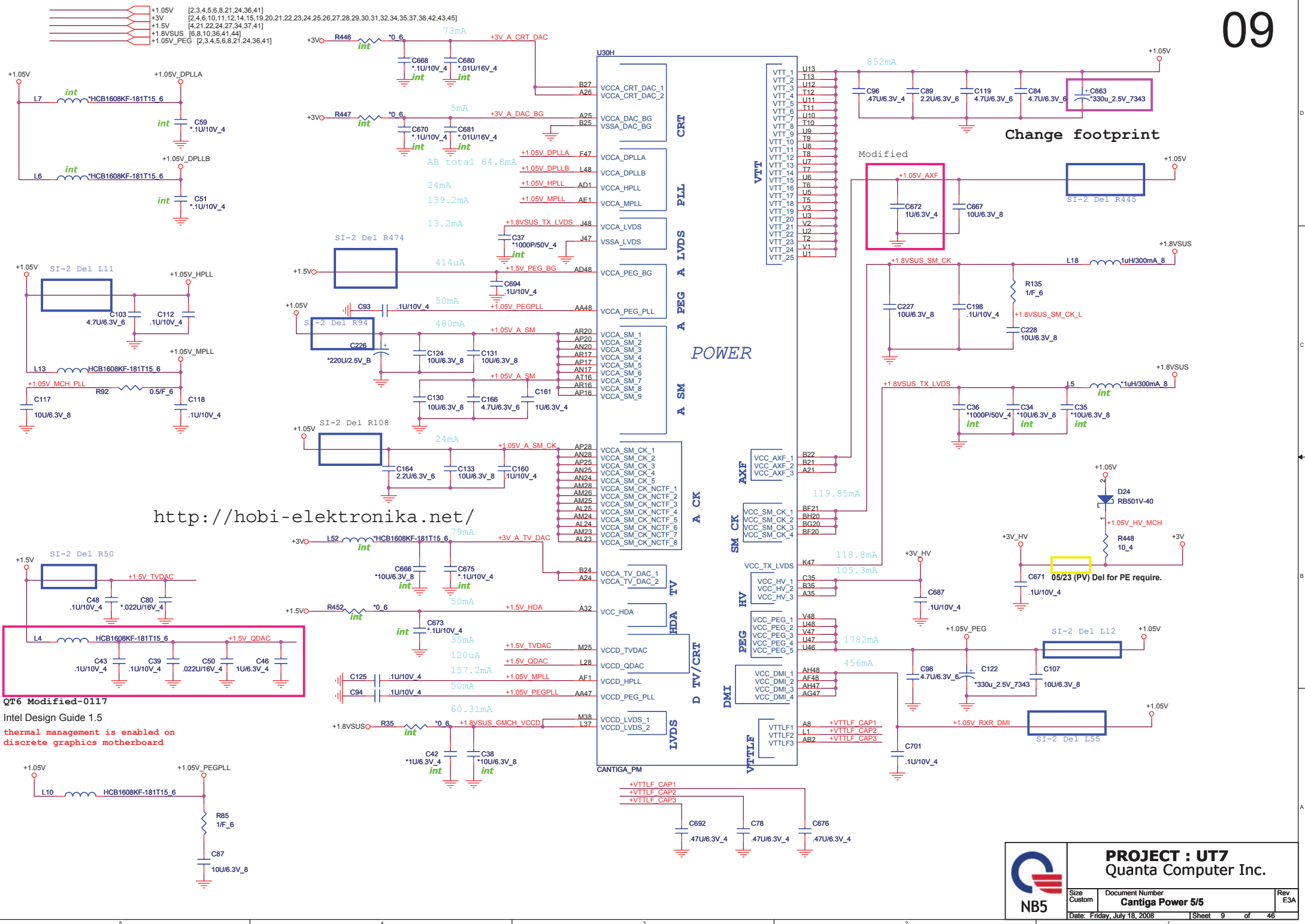
Change footprint

<http://hobi-elektronika.net/>

PROJECT : UT7
Quanta Computer Inc.

Size Custom Document Number Cantiga Vcc 4/5 Rev E3A

Date: Friday, July 18, 2008 Sheet 8 of 46

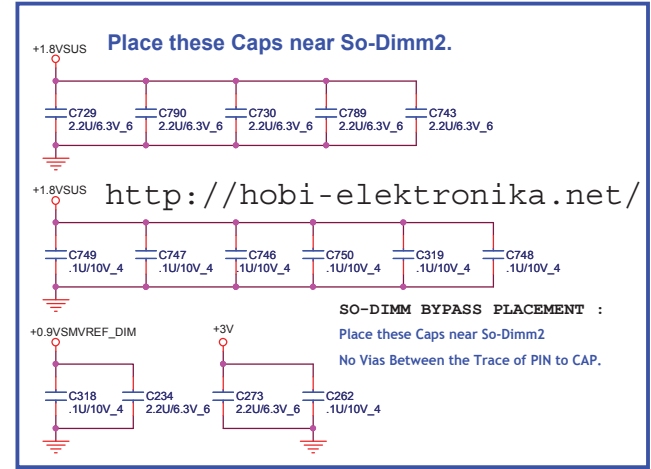
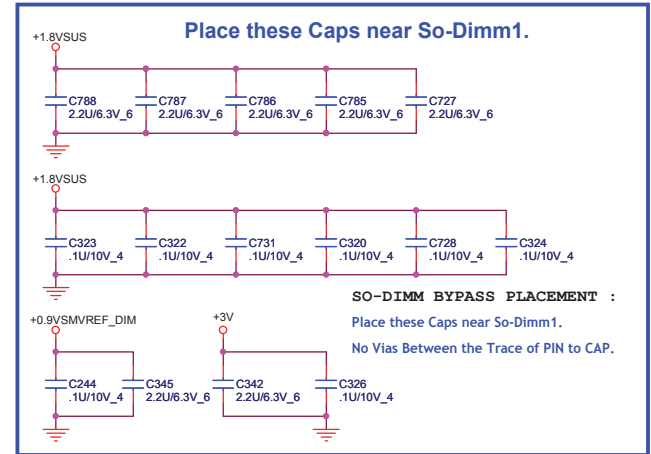
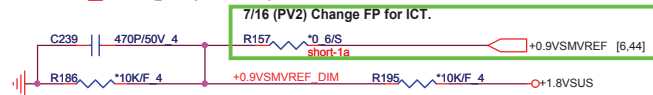
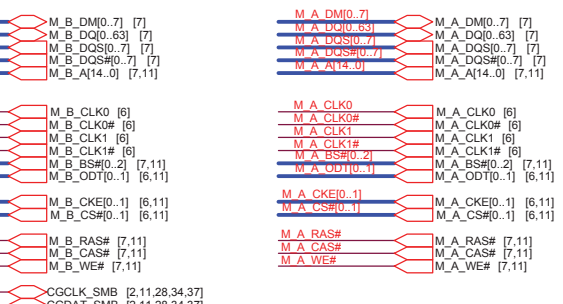
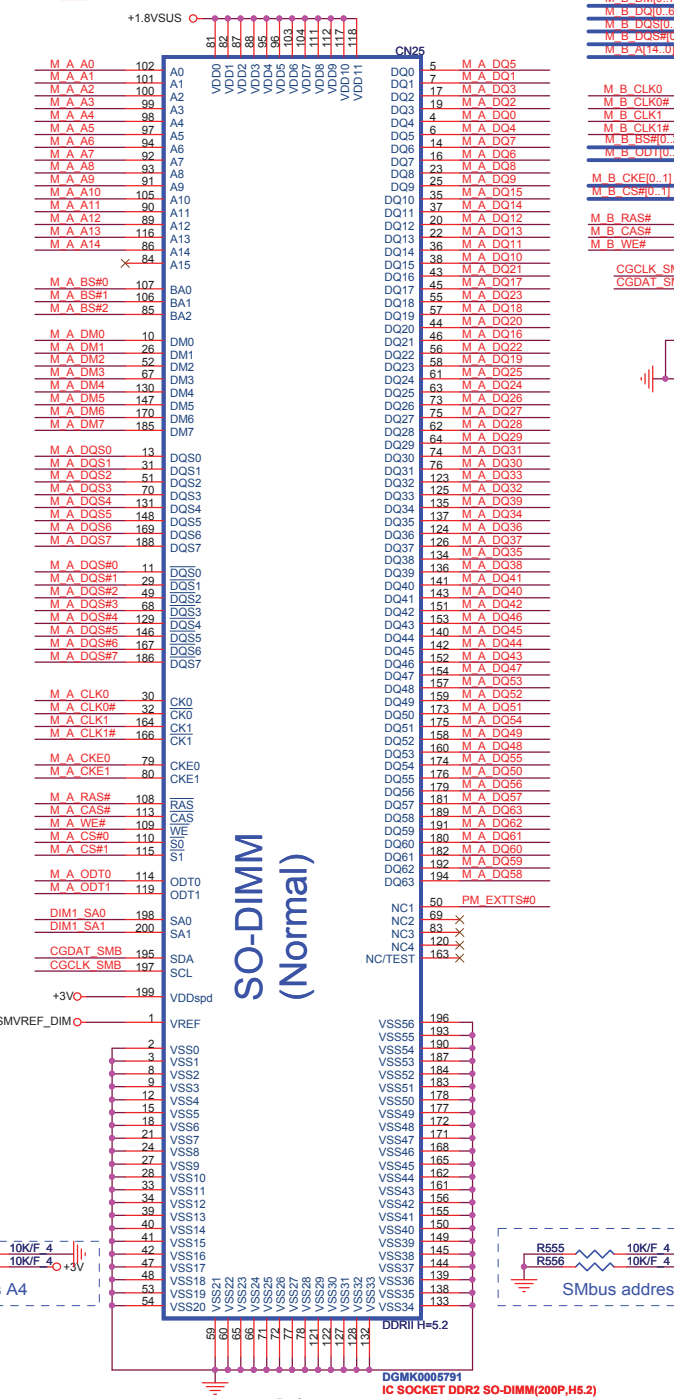
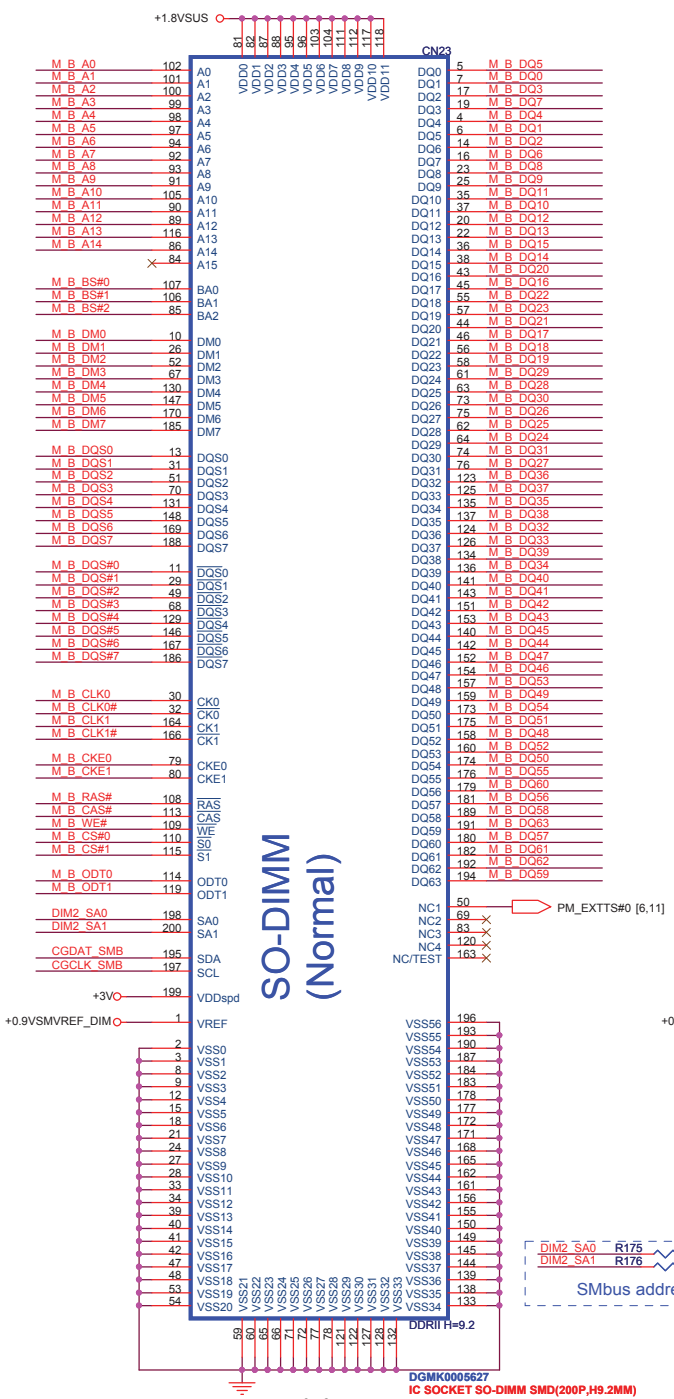


<http://hobi-elektronika.net/>

QT6 Modified-0117
 Intel Design Guide 1.5
 thermal management is enabled on
 discrete graphics motherboard

	PROJECT : UT7 Quanta Computer Inc.	
	Size Custom	Document Number Cantiga Power 5/5
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[2,4,6,9,11,12,14,15,19,20,21,22,23,24,25,26,27,28,29,30,31,32,34,35,37,38,42,43,45]



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SI modified
Footprint: "DDR-1-1734075-1-200P"

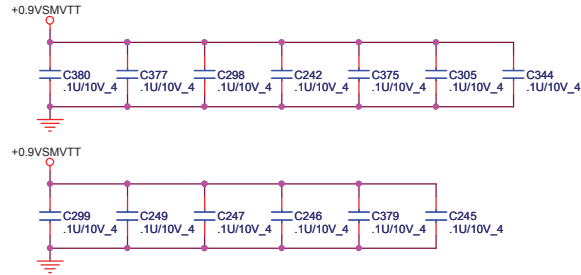
PROJECT : UT7
Quanta Computer Inc.

Size Custom Document Number **DDR2 DIMM** Rev E3A

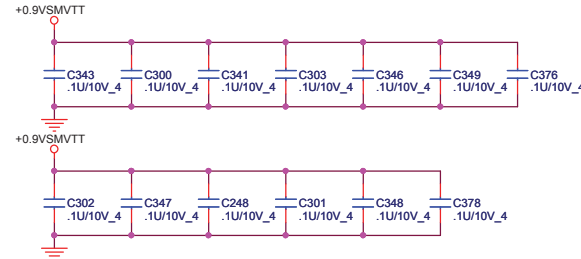
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DDRII DUAL CHANNEL A,B.

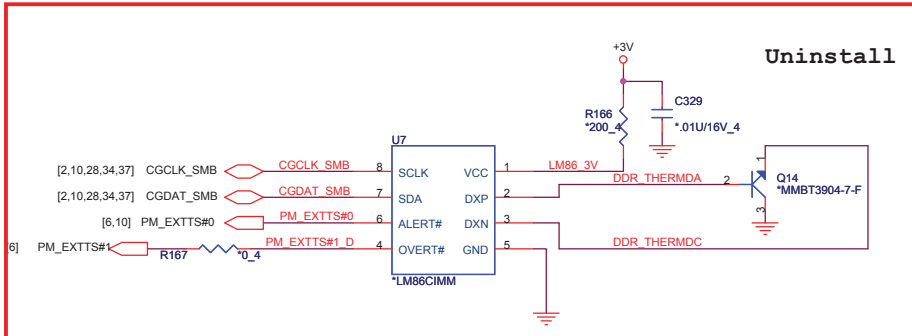
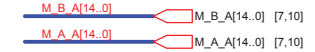
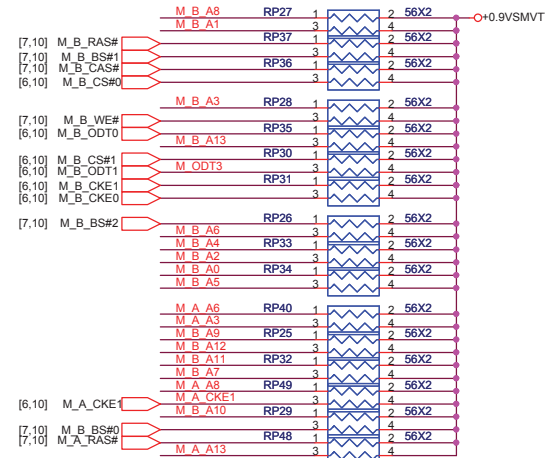
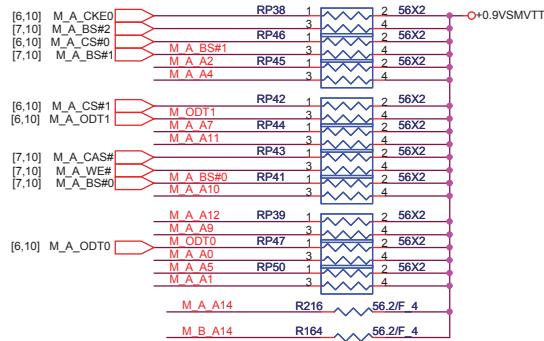
DDRII A CHANNEL



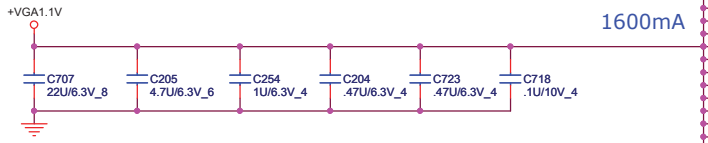
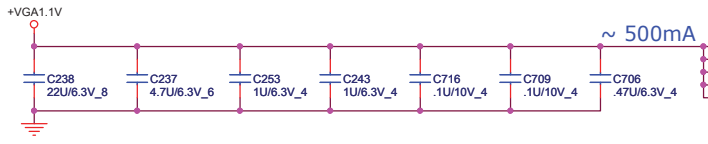
DDRII B CHANNEL



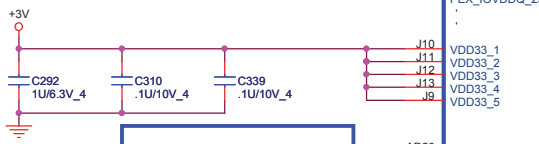
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM



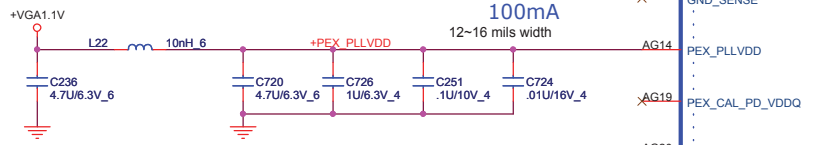
[2,4,6,9,10,11,14,15,19,20,21,22,23,24,25,26,27,28,29,30,31,32,34,35,37,38,42,43,45] +3V [13,14,44] +VGA1.1V



Near BGA



[43] VGA_SENSE
SI-2 4/10 For Nvidia recommend.

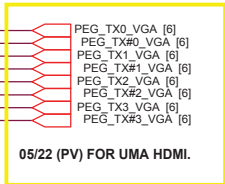


U35A
BG4969-NVIDIA-NB9P-GS
COMMON

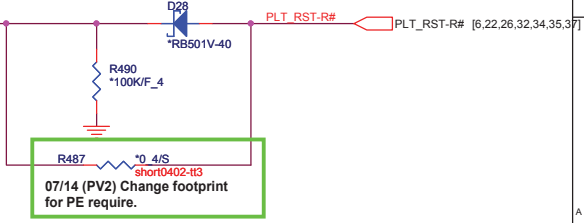
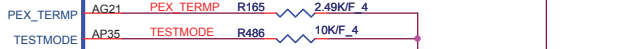
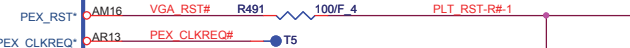
AK16	PEX_IOVDD_1	PEX_RX0	AP17	PEG_TX0_VGA
AK17	PEX_IOVDD_2	PEX_RX0*	AN17	PEG_TX#0_VGA
AK21	PEX_IOVDD_3	PEX_RX1	AN19	PEG_TX1_VGA
AK24	PEX_IOVDD_4	PEX_RX1*	AP19	PEG_TX#1_VGA
AK27	PEX_IOVDD_5	PEX_RX2	AR19	PEG_TX2_VGA
		PEX_RX2*	AR20	PEG_TX#2_VGA
		PEX_RX3	AN20	PEG_TX#3_VGA
		PEX_RX3*	AN22	PEG_TX4
AG11	PEX_IOVDDQ_1	PEX_RX4	AP22	PEG_TX#4
AG12	PEX_IOVDDQ_2	PEX_RX4*	AR22	PEG_TX#4
AG13	PEX_IOVDDQ_3	PEX_RX5	AR23	PEG_TX#5
AG15	PEX_IOVDDQ_4	PEX_RX5*	AP23	PEG_TX6
AG16	PEX_IOVDDQ_5	PEX_RX6	AN23	PEG_TX#6
AG17	PEX_IOVDDQ_6	PEX_RX6*	AN25	PEG_TX7
AG18	PEX_IOVDDQ_7	PEX_RX7	AP25	PEG_TX#7
AG22	PEX_IOVDDQ_8	PEX_RX7*	AR25	PEG_TX#8
AG23	PEX_IOVDDQ_9	PEX_RX8	AR26	PEG_TX#8
AG24	PEX_IOVDDQ_10	PEX_RX8*	AP26	PEG_TX9
AG25	PEX_IOVDDQ_11	PEX_RX9	AN26	PEG_TX#9
AG26	PEX_IOVDDQ_12	PEX_RX9*	AN28	PEG_TX10
AJ14	PEX_IOVDDQ_13	PEX_RX10	AP28	PEG_TX#10
AJ15	PEX_IOVDDQ_14	PEX_RX10*	AR28	PEG_TX11
AJ19	PEX_IOVDDQ_15	PEX_RX11	AN29	PEG_TX#11
AJ22	PEX_IOVDDQ_16	PEX_RX11*	AP29	PEG_TX12
AJ24	PEX_IOVDDQ_17	PEX_RX12	AN29	PEG_TX#12
AJ24	PEX_IOVDDQ_18	PEX_RX12*	AN31	PEG_TX13
AJ25	PEX_IOVDDQ_19	PEX_RX13	AR31	PEG_TX#13
AJ27	PEX_IOVDDQ_20	PEX_RX13*	AR31	PEG_TX14
AK18	PEX_IOVDDQ_21	PEX_RX14	AR32	PEG_TX#14
AK20	PEX_IOVDDQ_22	PEX_RX14*	AR34	PEG_TX15
AK23	PEX_IOVDDQ_23	PEX_RX15	AP34	PEG_TX#15
AK26	PEX_IOVDDQ_24	PEX_RX15*		
AL16	PEX_IOVDDQ_25			

PCI EXPRESS

PEX_TX0	AL17	C PEG_RX0	C171	.1U/10V_4	PEG_RX0 [6]
PEX_TX0*	AM17	C PEG_RX#0	C170	.1U/10V_4	PEG_RX#0 [6]
PEX_TX1	AM18	C PEG_RX1	C209	.1U/10V_4	PEG_RX1 [6]
PEX_TX1*	AM19	C PEG_RX#1	C210	.1U/10V_4	PEG_RX#1 [6]
PEX_TX2	AK19	C PEG_RX#2	C173	.1U/10V_4	PEG_RX#2 [6]
PEX_TX2*	AL20	C PEG_RX3	C145	.1U/10V_4	PEG_RX3 [6]
PEX_TX3	AM20	C PEG_RX#3	C146	.1U/10V_4	PEG_RX#3 [6]
PEX_TX3*	AM21	C PEG_RX4	C211	.1U/10V_4	PEG_RX#4 [6]
PEX_TX4	AM22	C PEG_RX#4	C212	.1U/10V_4	PEG_RX#4 [6]
PEX_TX4*	AL22	C PEG_RX5	C213	.1U/10V_4	PEG_RX#5 [6]
PEX_TX5	AK22	C PEG_RX#5	C214	.1U/10V_4	PEG_RX#5 [6]
PEX_TX5*	AL23	C PEG_RX6	C147	.1U/10V_4	PEG_RX#6 [6]
PEX_TX6	AM23	C PEG_RX#6	C148	.1U/10V_4	PEG_RX#6 [6]
PEX_TX6*	AM24	C PEG_RX7	C174	.1U/10V_4	PEG_RX#7 [6]
PEX_TX7	AM25	C PEG_RX#7	C175	.1U/10V_4	PEG_RX#7 [6]
PEX_TX7*	AL25	C PEG_RX8	C149	.1U/10V_4	PEG_RX#8 [6]
PEX_TX8	AK25	C PEG_RX#8	C150	.1U/10V_4	PEG_RX#8 [6]
PEX_TX8*	AL26	C PEG_RX9	C176	.1U/10V_4	PEG_RX#9 [6]
PEX_TX9	AM26	C PEG_RX#9	C177	.1U/10V_4	PEG_RX#9 [6]
PEX_TX9*	AM27	C PEG_RX10	C151	.1U/10V_4	PEG_RX#10 [6]
PEX_TX10	AM28	C PEG_RX#10	C152	.1U/10V_4	PEG_RX#10 [6]
PEX_TX10*	AL28	C PEG_RX11	C199	.1U/10V_4	PEG_RX#11 [6]
PEX_TX11	AK28	C PEG_RX#11	C200	.1U/10V_4	PEG_RX#11 [6]
PEX_TX11*	AK29	C PEG_RX12	C178	.1U/10V_4	PEG_RX#12 [6]
PEX_TX12	AL29	C PEG_RX#12	C179	.1U/10V_4	PEG_RX#12 [6]
PEX_TX12*	AM29	C PEG_RX13	C162	.1U/10V_4	PEG_RX#13 [6]
PEX_TX13	AM30	C PEG_RX#13	C163	.1U/10V_4	PEG_RX#13 [6]
PEX_TX13*	AM31	C PEG_RX14	C158	.1U/10V_4	PEG_RX#14 [6]
PEX_TX14	AM32	C PEG_RX#14	C158	.1U/10V_4	PEG_RX#14 [6]
PEX_TX14*	AN32	C PEG_RX15	C180	.1U/10V_4	PEG_RX#15 [6]
PEX_TX15	AP32	C PEG_RX#15	C181	.1U/10V_4	PEG_RX#15 [6]
PEX_TX15*					



05/22 (PV) FOR UMA HDMI.

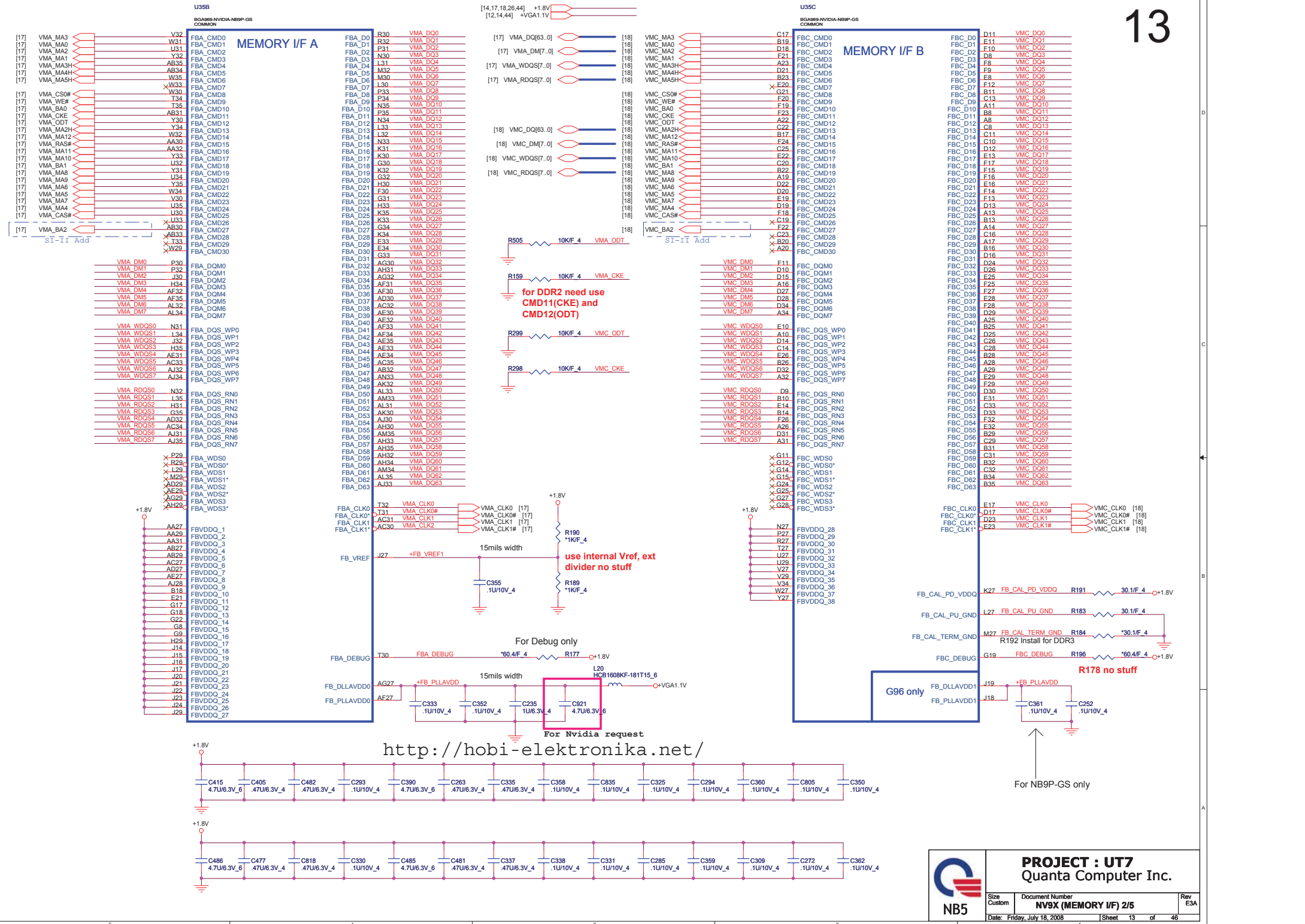


07/14 (PV2) Change footprint for PE require.

PROJECT : UT7
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Size Custom Document Number **NV9X (PCIE I/F) 1/5** Rev E3A

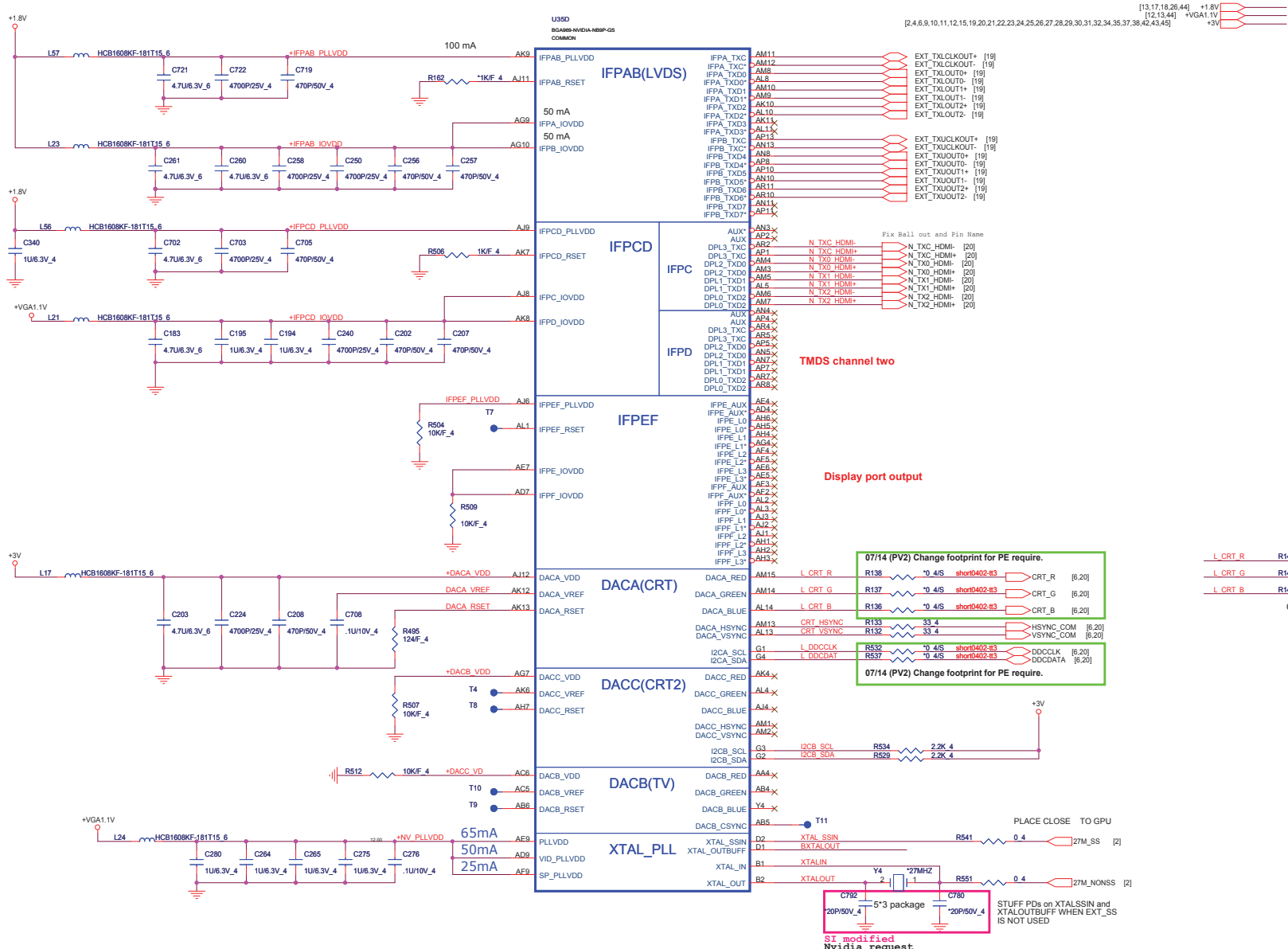
Date: Friday, July 18, 2008 Sheet 12 of 46



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[13,17,18,26,44] +1.8V
 [12,13,44] +VGA1.1V
 +3V

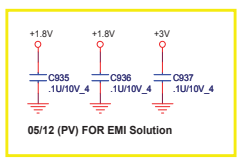
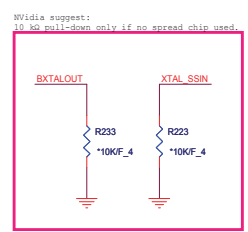
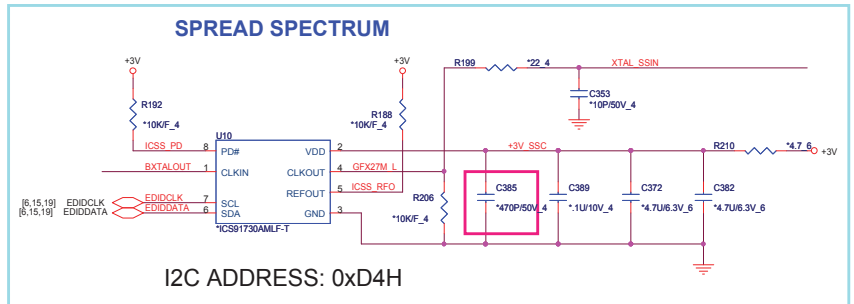
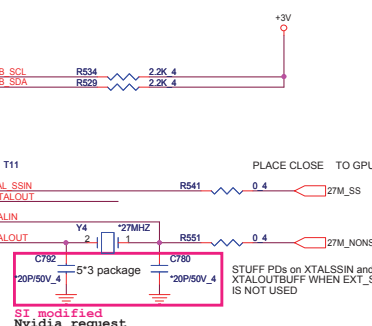
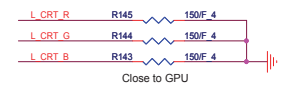
- AM11 EXT_TXCLKOUT+ [19]
- AM12 EXT_TXCLKOUT- [19]
- AM8 EXT_TXOUT0+ [19]
- AM9 EXT_TXOUT0- [19]
- AM10 EXT_TXOUT1+ [19]
- AM9 EXT_TXOUT1- [19]
- AK10 EXT_TXOUT2+ [19]
- AK10 EXT_TXOUT2- [19]
- AK14 EXT_TXCLKOUT+ [19]
- AK14 EXT_TXCLKOUT- [19]
- AN13 EXT_TXOUT0+ [19]
- AN13 EXT_TXOUT0- [19]
- AN8 EXT_TXOUT0+ [19]
- AN8 EXT_TXOUT0- [19]
- AP8 EXT_TXOUT0+ [19]
- AP10 EXT_TXOUT1+ [19]
- AN10 EXT_TXOUT1- [19]
- AR11 EXT_TXOUT2+ [19]
- AR10 EXT_TXOUT2- [19]
- AN11 EXT_TXOUT2+ [19]
- AP11 EXT_TXOUT2- [19]

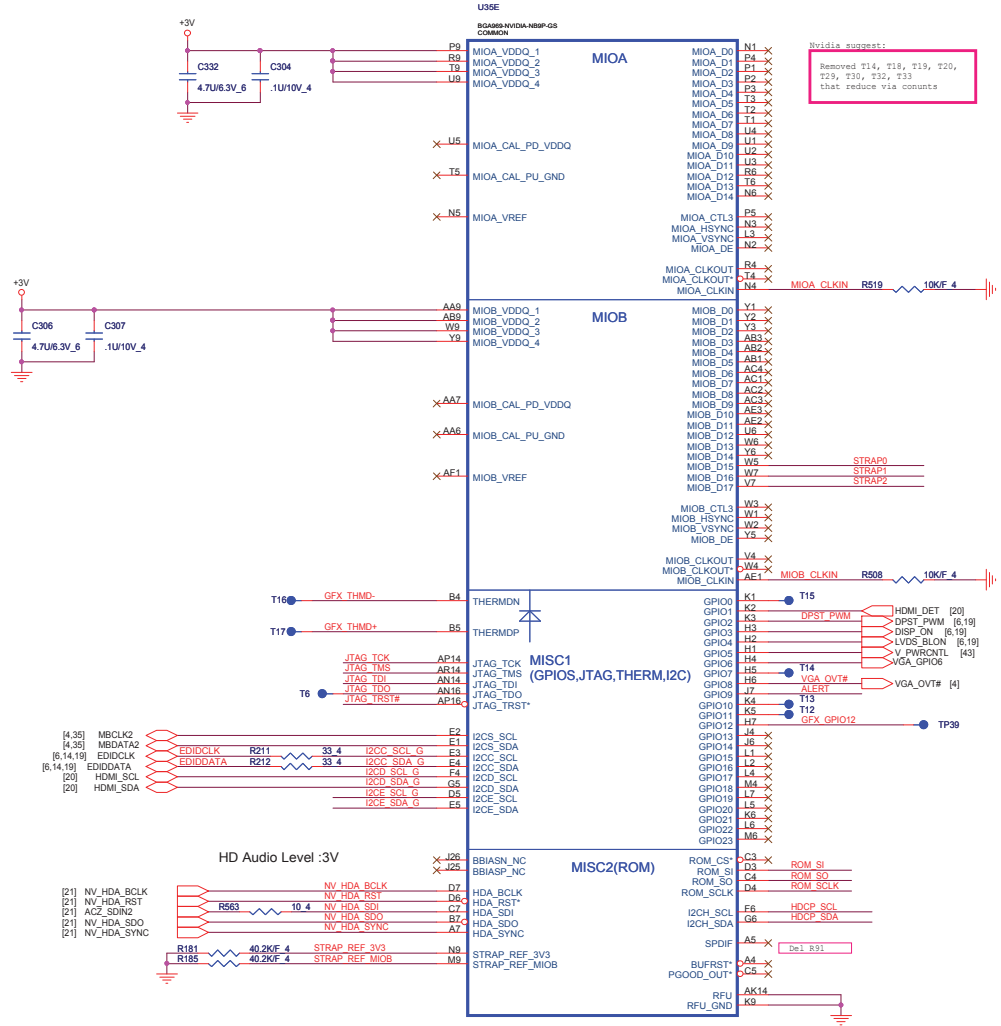
- Fix Ball out and Pin Name
- N_TXC_HDMI+ [20]
- N_TXC_HDMI- [20]
- N_TX0_HDMI+ [20]
- N_TX0_HDMI- [20]
- N_TX1_HDMI+ [20]
- N_TX1_HDMI- [20]
- N_TX2_HDMI+ [20]
- N_TX2_HDMI- [20]

TMD5 channel two

Display port output

- 07/14 (PV2) Change footprint for PE require.
- L CRT R R138 0.4S short0402-t3 CRT_R [6.20]
- L CRT G R137 0.4S short0402-t3 CRT_G [6.20]
- L CRT B R136 0.4S short0402-t3 CRT_B [6.20]
- CRT_HSYNC R133 33.4 HSYNC_COM [6.20]
- CRT_VSYNC R132 33.4 VSYNC_COM [6.20]
- DDCCCLK R532 0.4S short0402-t3 DDCCCLK [6.20]
- DDCCDAT R537 0.4S short0402-t3 DDCCDATA [6.20]
- 07/14 (PV2) Change footprint for PE require.

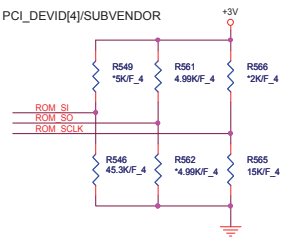




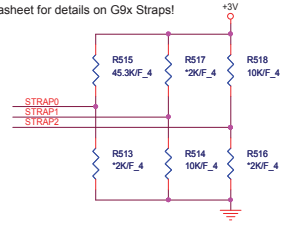
[2,4,6,9,10,11,12,14,19,20,21,22,23,24,25,26,27,28,29,30,31,32,34,35,37,38,42,43,45]

NB9P-GS (G96) Straps NB9M-GE (G98) Straps GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL



SEE Datasheet for details on G9x Straps!

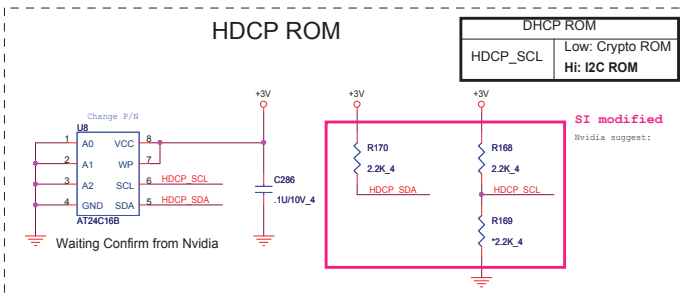


Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_277	TVMODE[2]	TVMODE[1]	TVMODE[0]	1000
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM100	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

Delete VGA thermal circuit



NB9X VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix HY5PS121621CFP-25
0110	DDR2 32Mx16x8, 128bit, 512MB	Qimonda HYB18T512161B2P-25
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung K4N51163QE-ZC25
0100	DDR2 32Mx16x8, 128bit, 512MB	Nanya/Elipida
0000	DDR2 64Mx16x8, 128bit, 1GB	Hynix
0001	DDR2 64Mx16x8, 128bit, 1GB	Samsung
0010	DDR2 64Mx16x8, 128bit, 1GB	Qimonda

CS33572FB13 RES CHIP 35.7K 1/16W +-1% (0402)

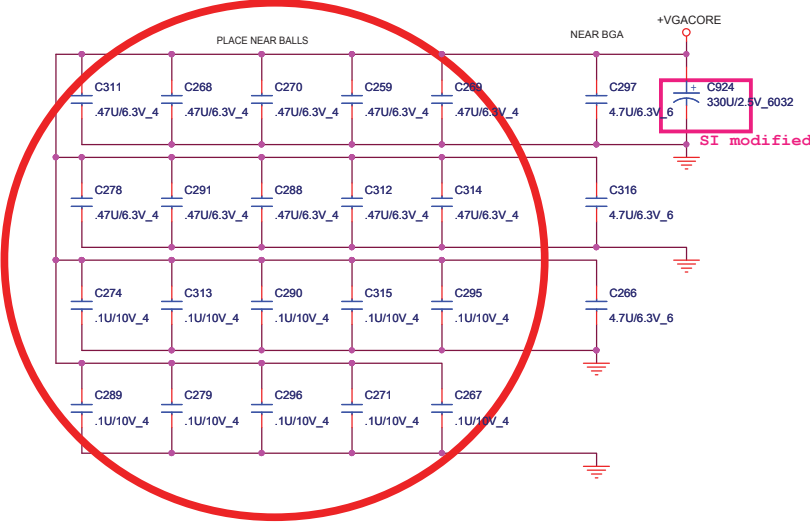
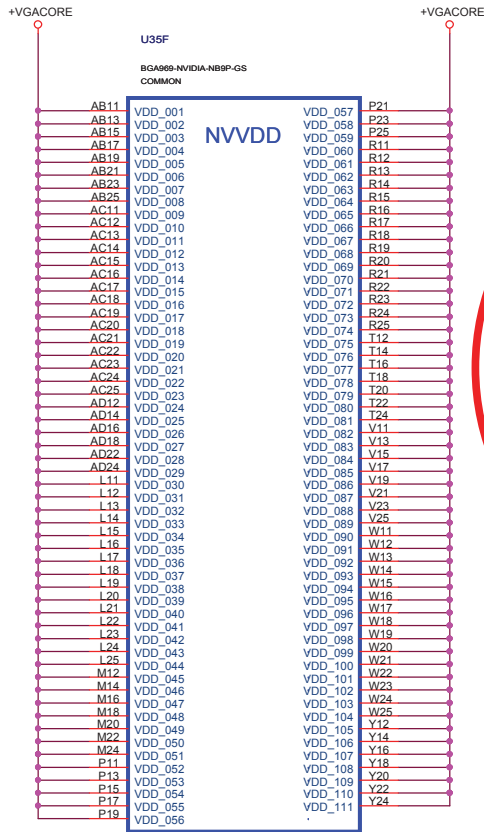
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NB5

Size C Document Number: **NV9X (GPIO & STRAPS) 4/5** Rev: ESA

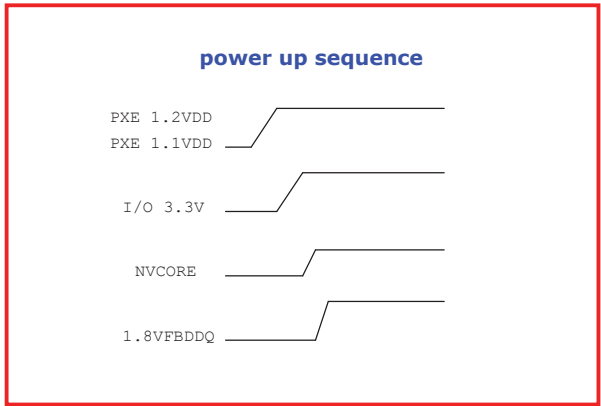
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NVVDD Decoupling

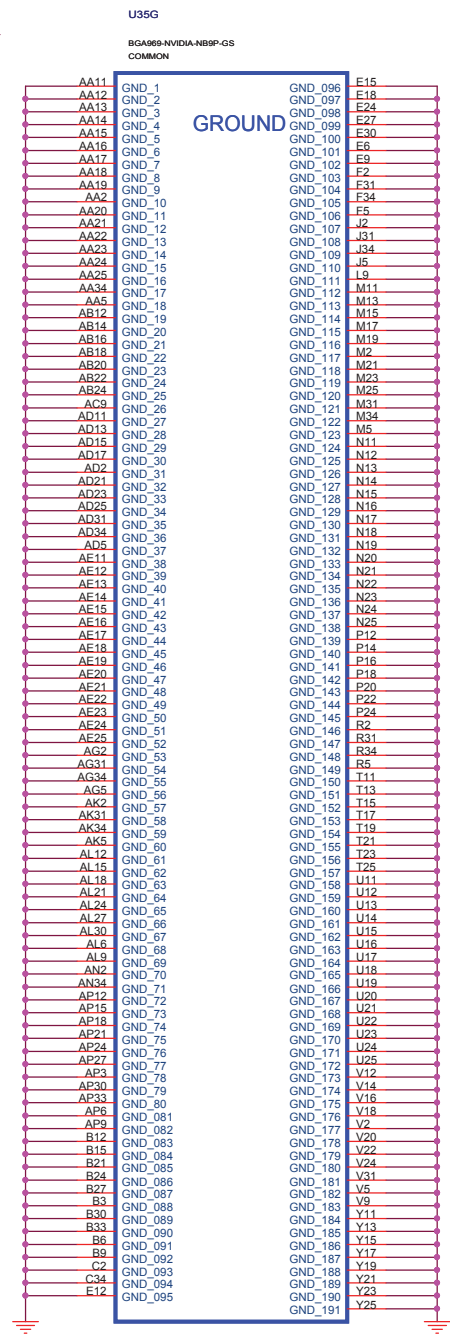


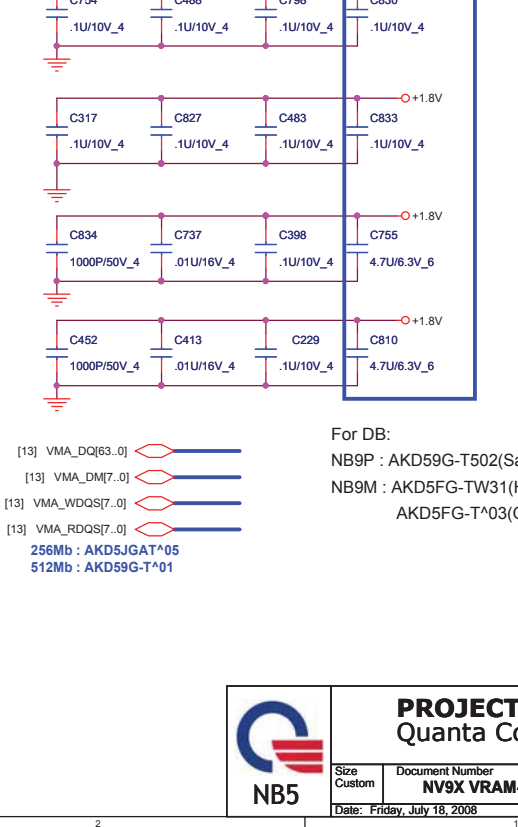
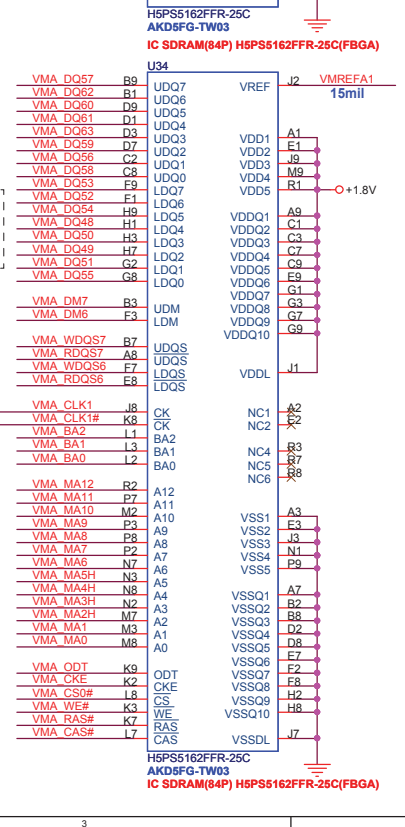
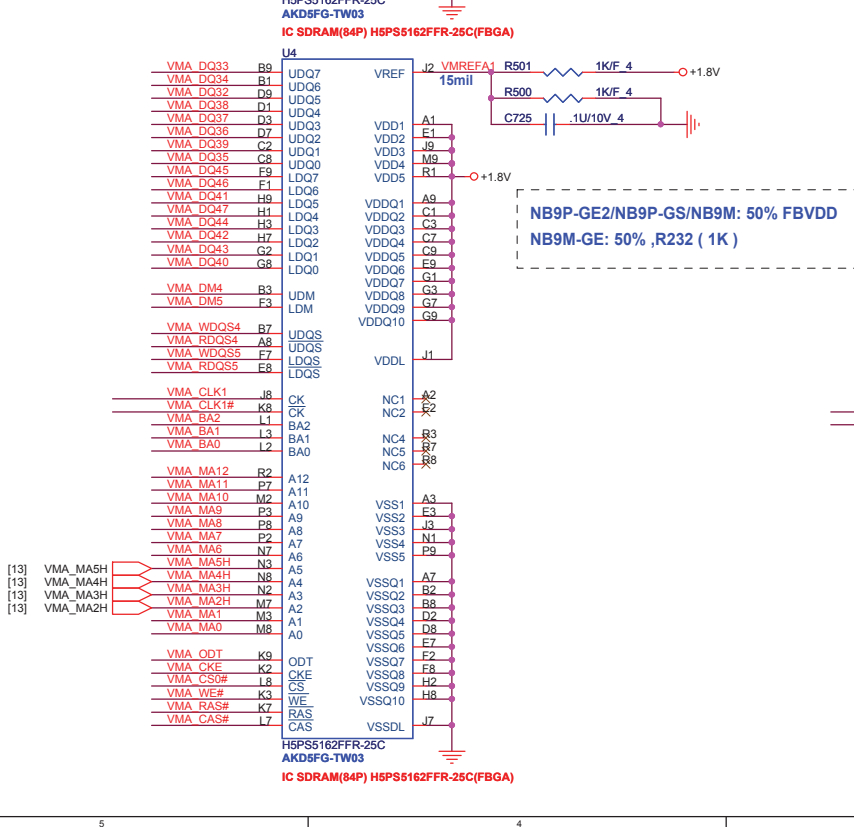
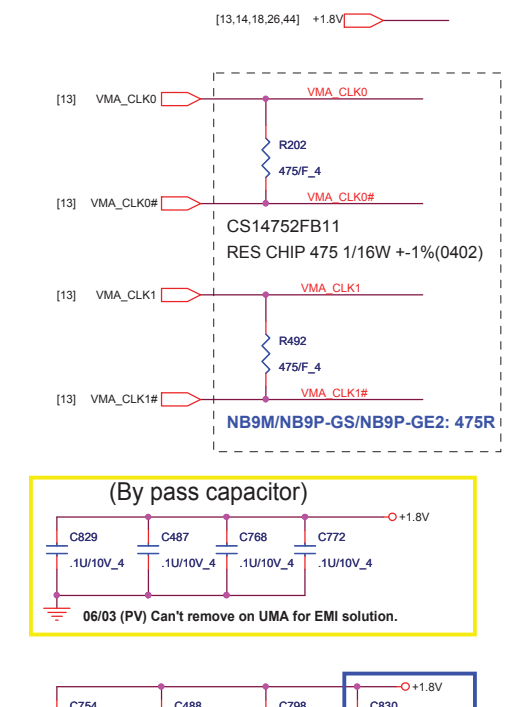
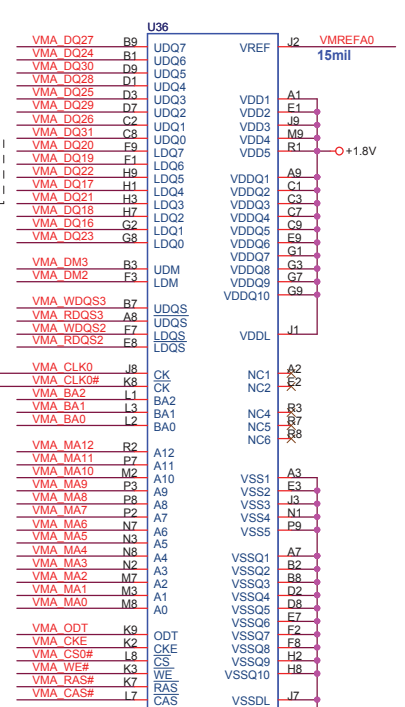
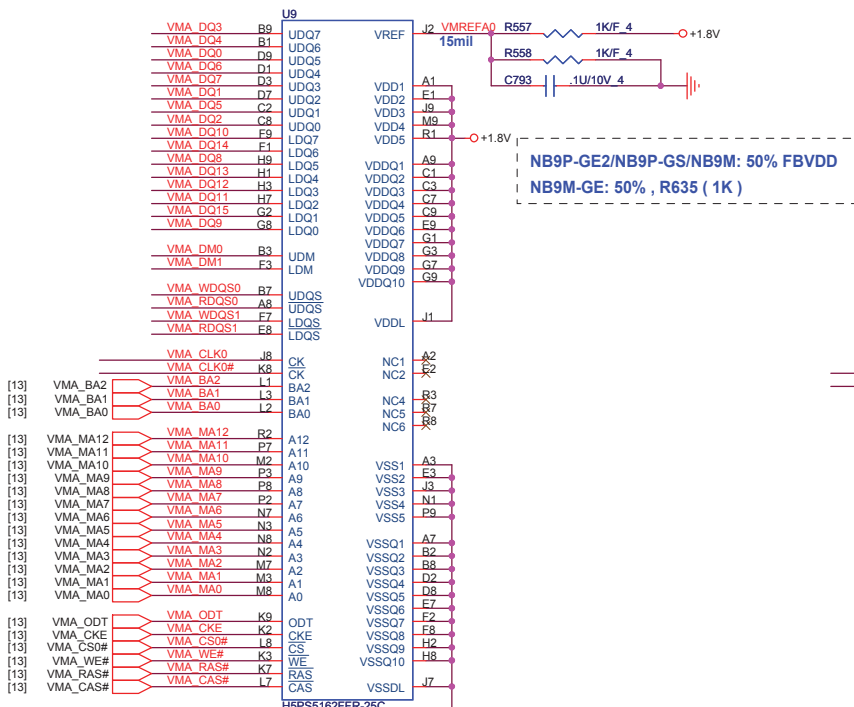
Follow Design Guide DG-03276-001 4.7uFx3 and 0.47x10 uF instead of 0.1uF x10

NB9M: VGACORE +0.90V (Normal) , +1.09V

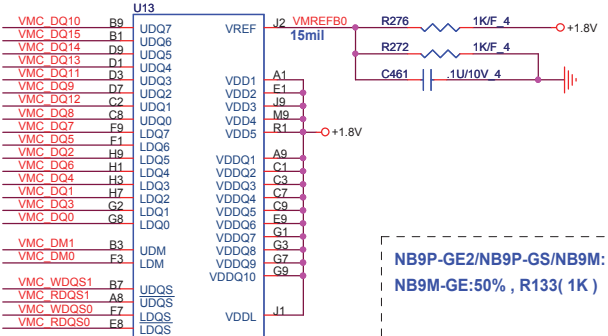


[43] +VGACORE

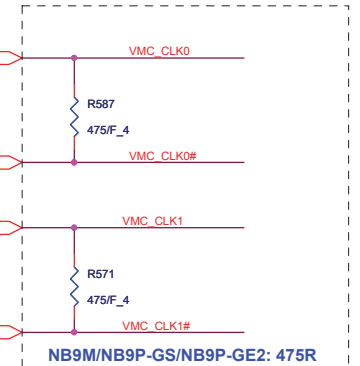
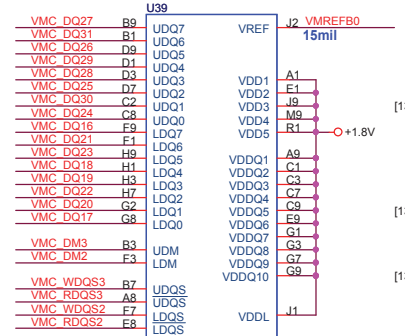




[13,14,17,26,44] +1.8V



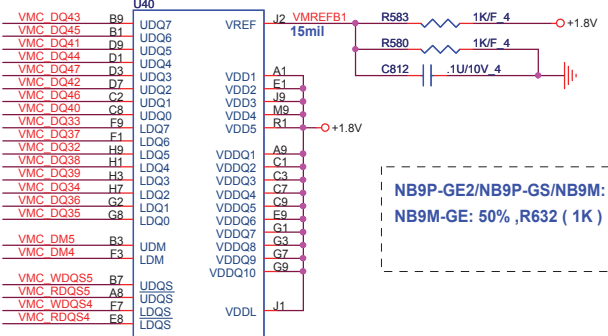
NB9P-GE2/NB9P-GS/NB9M: 50% FBVDD
NB9M-GE: 50%, R133(1K)



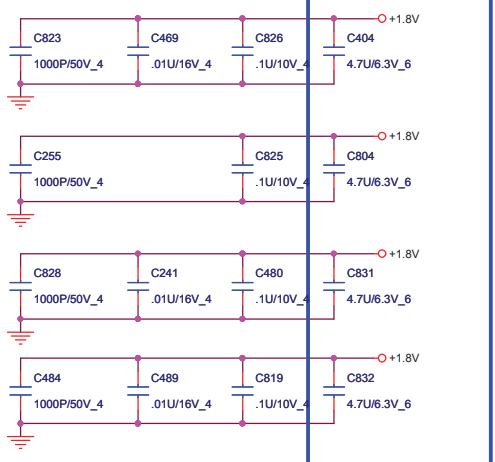
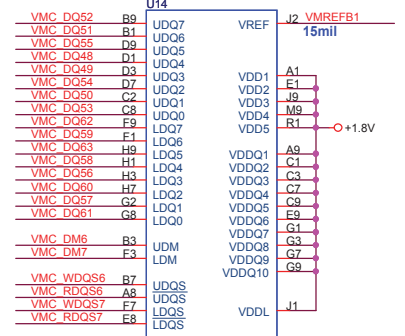
CS14752FB11 RES CHIP 475 1/16W +-1%(0402)

- [13] VMC_BA2
- [13] VMC_BA1
- [13] VMC_BA0
- [13] VMC_MA12
- [13] VMC_MA11
- [13] VMC_MA10
- [13] VMC_MA9
- [13] VMC_MA8
- [13] VMC_MA7
- [13] VMC_MA6
- [13] VMC_MA5
- [13] VMC_MA4
- [13] VMC_MA3
- [13] VMC_MA2
- [13] VMC_MA1
- [13] VMC_MA0
- [13] VMC_ODT
- [13] VMC_CKE
- [13] VMC_CS0#
- [13] VMC_WE#
- [13] VMC_RAS#
- [13] VMC_CAS#

- [13] VMC_BA2
- [13] VMC_BA1
- [13] VMC_BA0
- [13] VMC_MA12
- [13] VMC_MA11
- [13] VMC_MA10
- [13] VMC_MA9
- [13] VMC_MA8
- [13] VMC_MA7
- [13] VMC_MA6
- [13] VMC_MA5
- [13] VMC_MA4
- [13] VMC_MA3
- [13] VMC_MA2
- [13] VMC_MA1
- [13] VMC_MA0
- [13] VMC_ODT
- [13] VMC_CKE
- [13] VMC_CS0#
- [13] VMC_WE#
- [13] VMC_RAS#
- [13] VMC_CAS#



NB9P-GE2/NB9P-GS/NB9M: 50% FBVDD
NB9M-GE: 50%, R632 (1K)



- [13] VMC_MASH
- [13] VMC_MAH
- [13] VMC_MA3H
- [13] VMC_MA2H
- [13] VMC_MA1H
- [13] VMC_MA0H
- [13] VMC_ODT
- [13] VMC_CKE
- [13] VMC_CS0#
- [13] VMC_WE#
- [13] VMC_RAS#
- [13] VMC_CAS#

- [13] VMC_MASH
- [13] VMC_MAH
- [13] VMC_MA3H
- [13] VMC_MA2H
- [13] VMC_MA1H
- [13] VMC_MA0H
- [13] VMC_ODT
- [13] VMC_CKE
- [13] VMC_CS0#
- [13] VMC_WE#
- [13] VMC_RAS#
- [13] VMC_CAS#

VRAM Vendor

NB9M-GE	1	3
NB9P-GS	2	

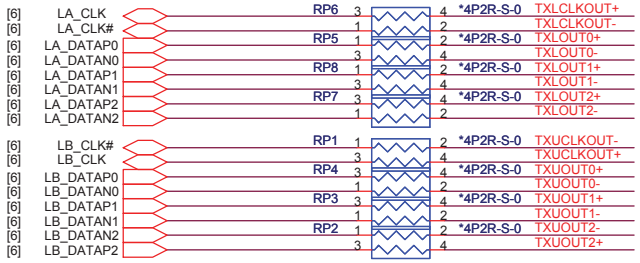
- 3 AKD5FG-T501 IC SDRAM(84P) K4N51163QG-HC25(FBGA) Samsung
- 2 AKD5FG-T*03 IC SDRAM(84P)HYB18T512161B2F-25(TFBGA) Qimonda
- 1 AKD5FG-TW31 IC SDRAM(84P) HY5PS121621CFP-25(FBGA) Hynix



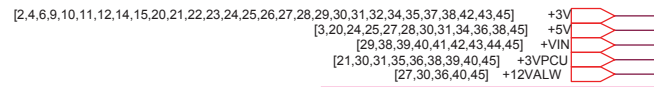
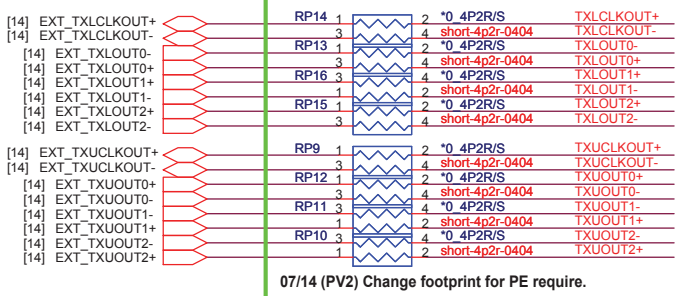
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1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

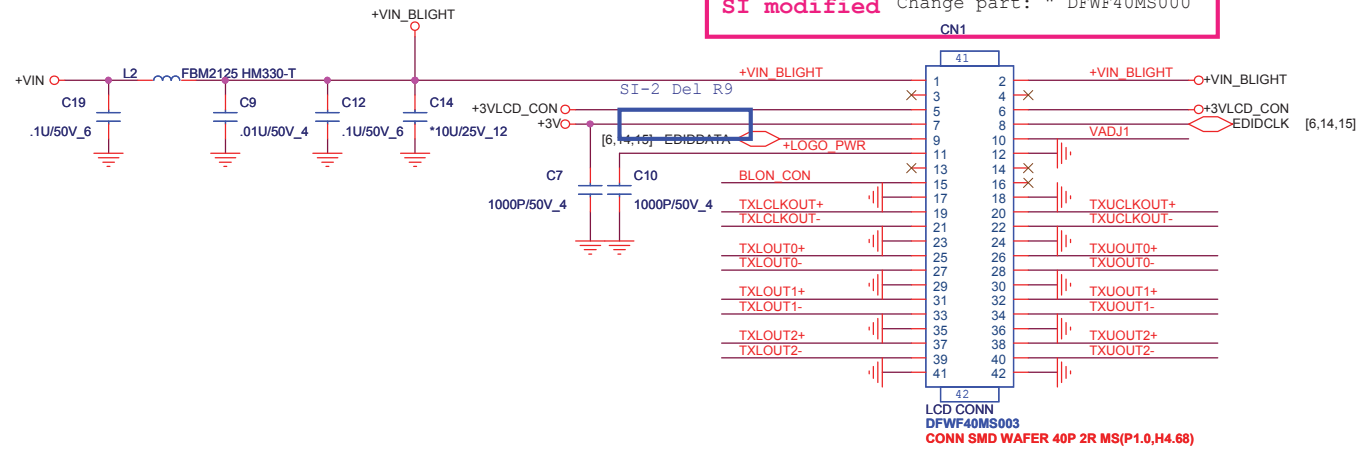
OPTION SIGNAL FROM NB FOR UMA VGA



OPTION SIGNAL FROM Nvidia to VGA

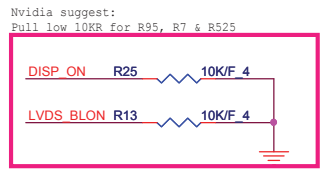
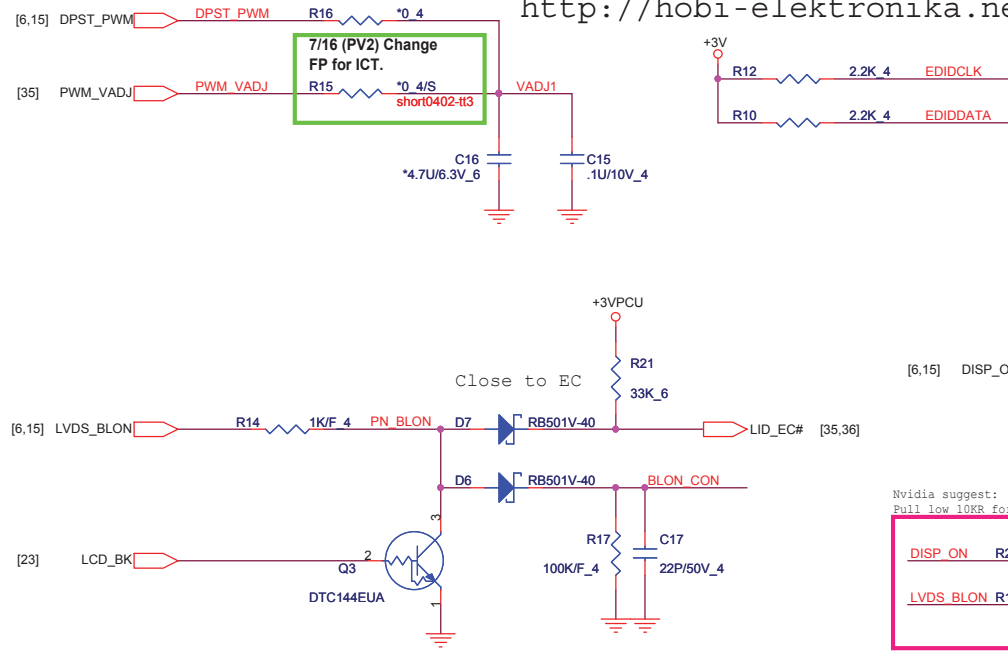


SI modified Change part: " DFWF40MS000

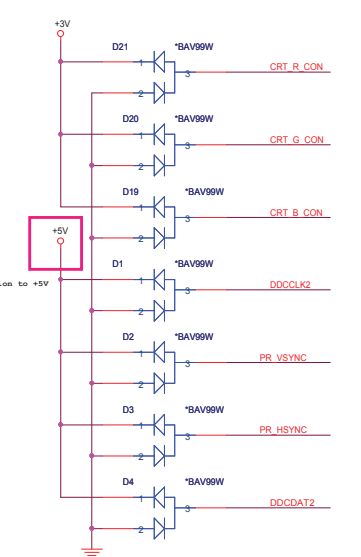
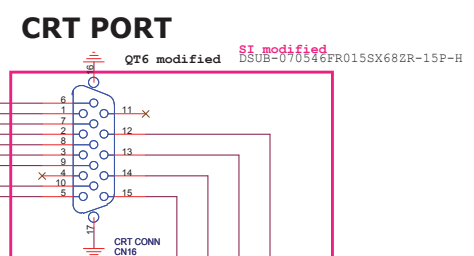
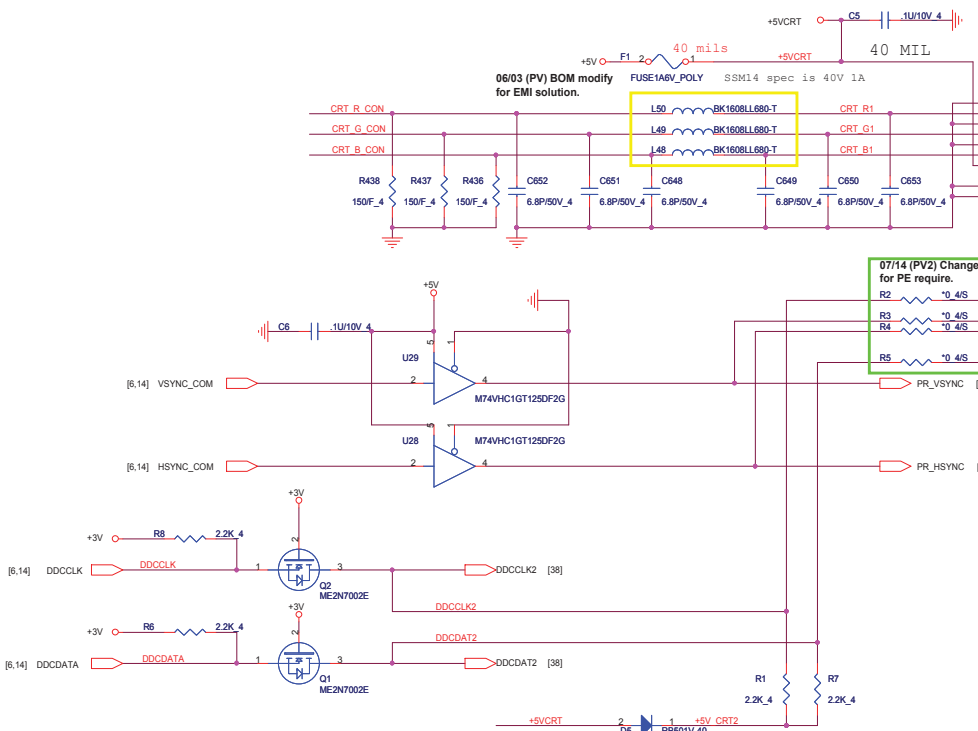


0090 use 100 ohm and must change back to 75ohm

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Size B	Document Number
LCD CONN/Lid function	
Date: Friday, July 18, 2008	Sheet 19 of 46
	Rev E3A

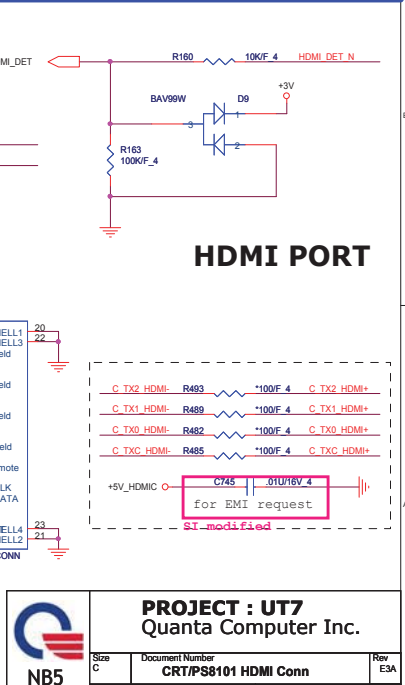
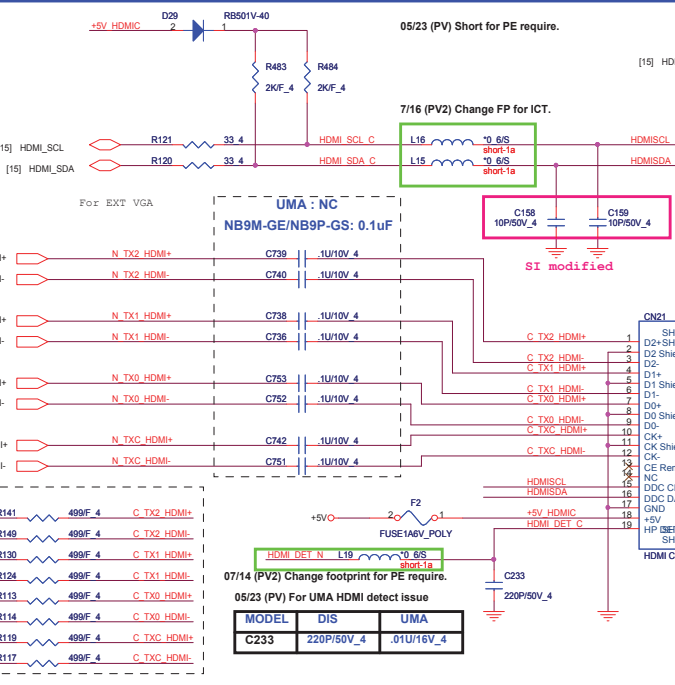
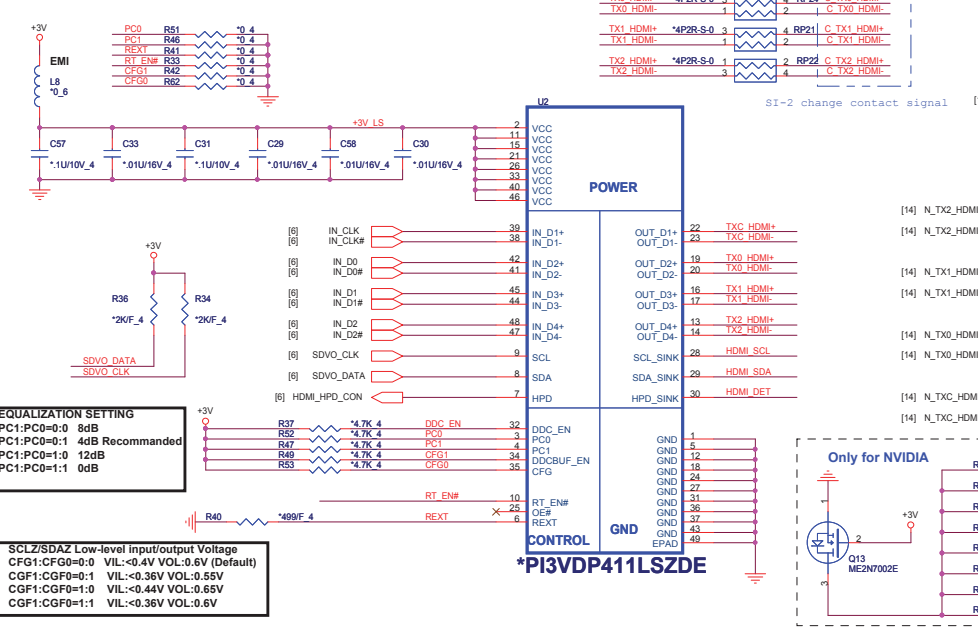


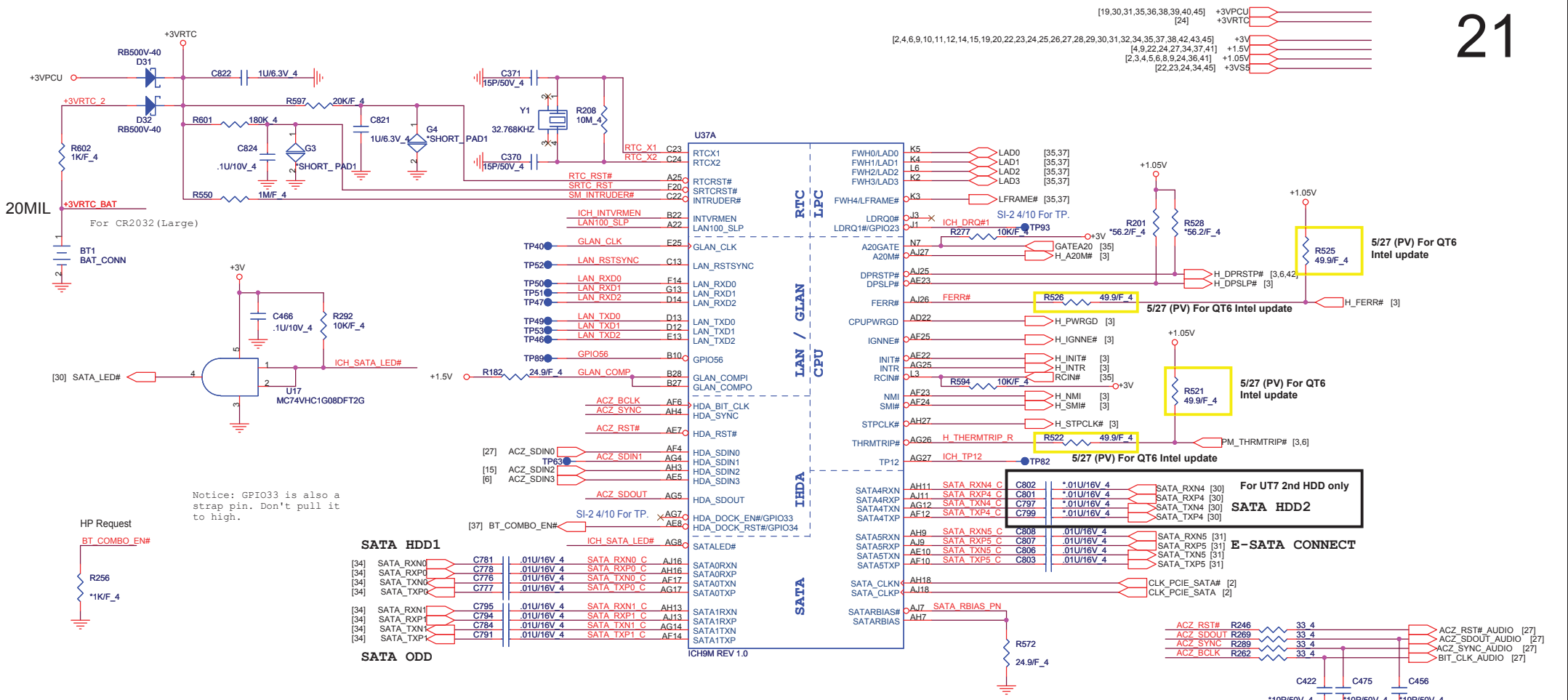
inputs	function
/E	L
SET	L
	L
	H
	X

function	inputs
Y - port 0	L
Y - port 1	H
Disconnect	X

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For UMA HDMI function





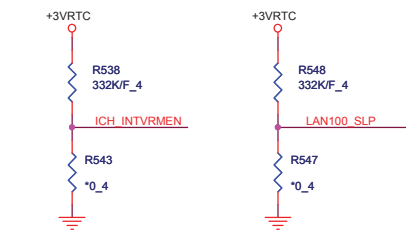
Notice: GPIO33 is also a strap pin. Don't pull it to high.

SB Strap

ICH9-M Internal VR Enable strap
(Internal VR for Vccs1_05, Vccs1_5 and VccCL1_5)

ICH9-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1_05)

Low = Internal VR enable(Default)
High = Internal VR enable(Default)



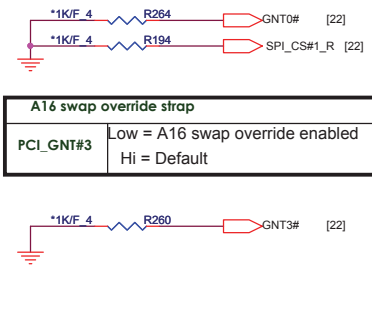
XOR Chain Entrance Strap

ICH_TP3	HDA_SDOOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1

ICH9 Boot BIOS select

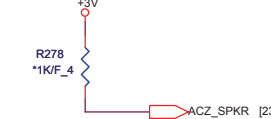
STRAP	PCI_GNT0#	SPL_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

(default)



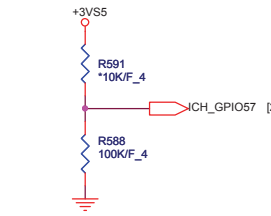
No Reboot Strap

ACZ_SPKR Low: Default
Hi: No reboot



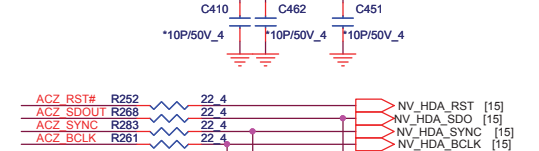
TPM physical presence

ICH_GPIO57 Low: Default



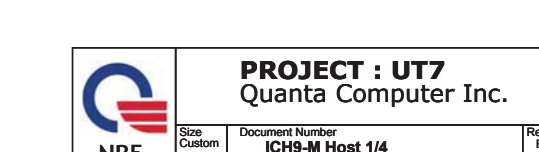
For GM UMA only

ACZ_RST# R242 *33_4
ACZ_SDOOUT R266 *33_4
ACZ_SYNC R274 *33_4
ACZ_BCLK R258 *33_4



Close to U45

ACZ_RST# R252 22_4
ACZ_SDOOUT R268 22_4
ACZ_SYNC R283 22_4
ACZ_BCLK R261 22_4



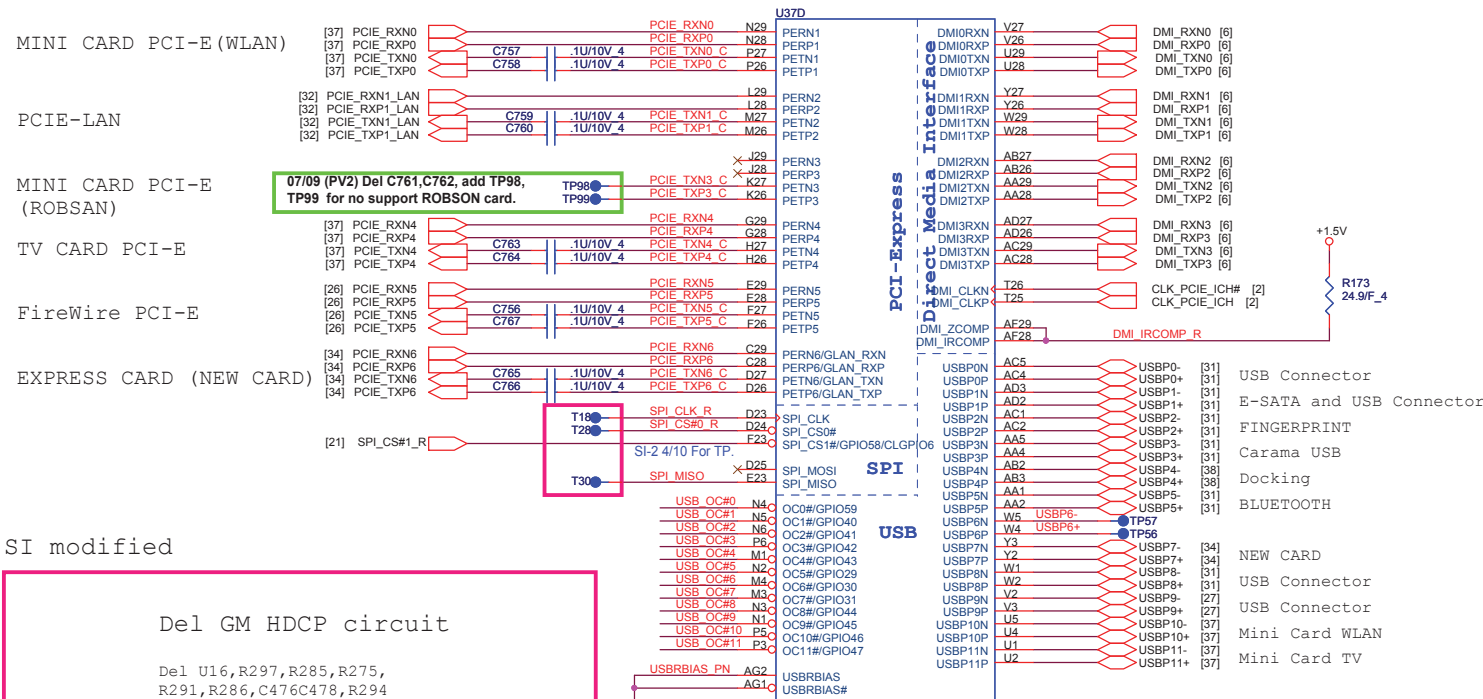
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Size Custom Document Number ICH9-M Host 1/4 Rev E3A

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SWAP PCIE PORT6 to PORT2 (Lan and New card swap) -->Rename the port name by function and port

[4,9,21,24,27,34,37,41] +1.5V
 [23,31,37,41,42,43,45] +3V
 [21,23,24,34,45] +3VS5

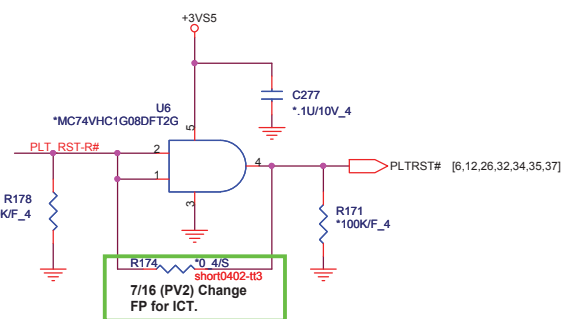
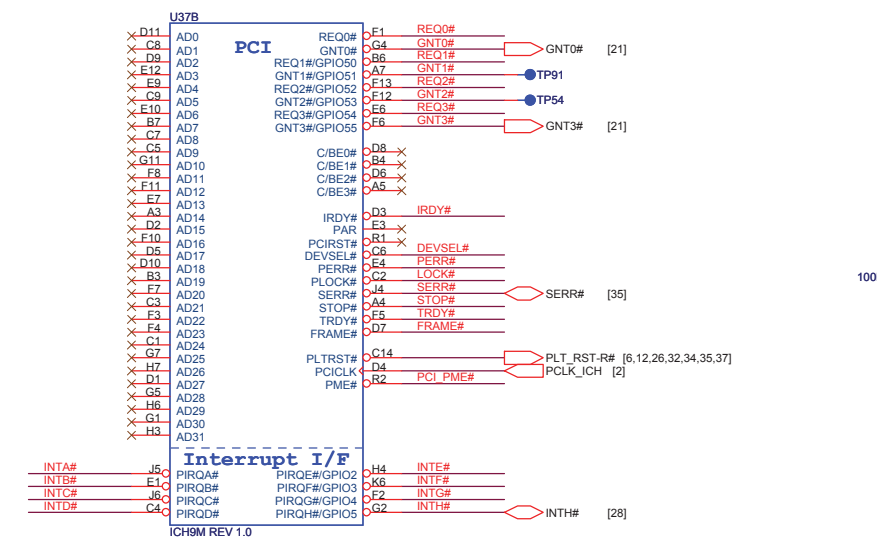
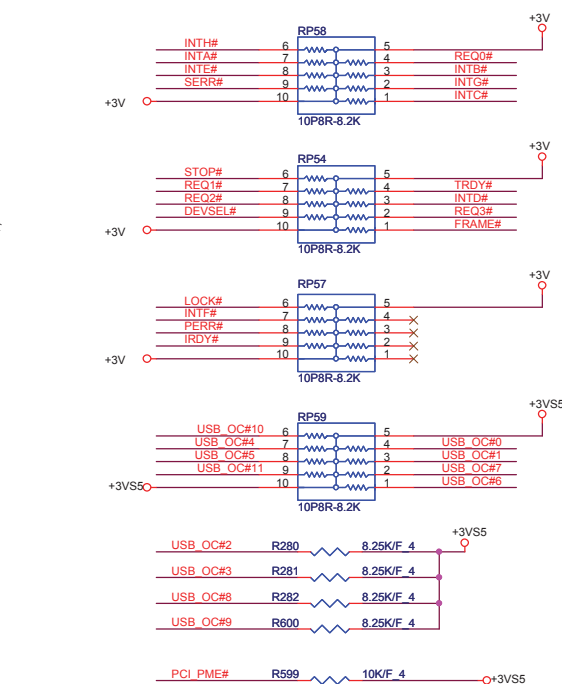


SI modified

Del GM HDCP circuit

Del U16, R297, R285, R275, R291, R286, C476C478, R294

512K byte SPI ROM
For HDCP only
For GM HDCP



R174 0.4S short0402-t13
7/16 (PV2) Change FP for ICT.

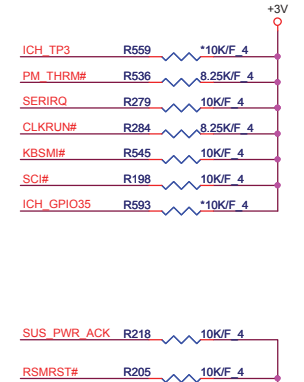
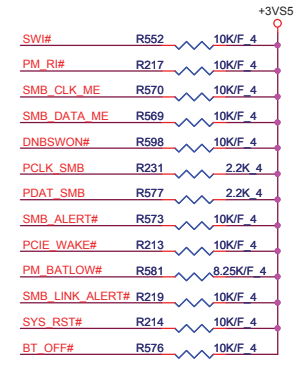
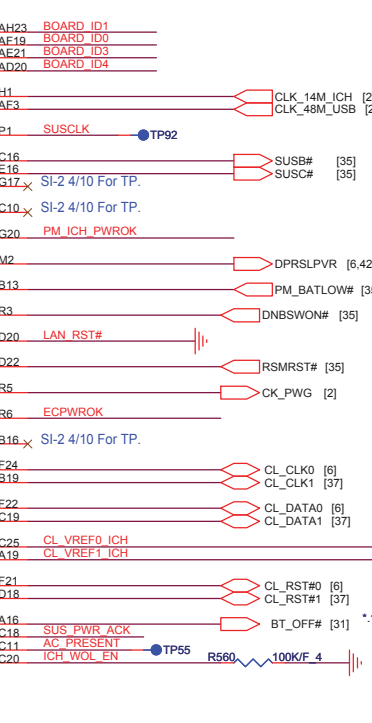
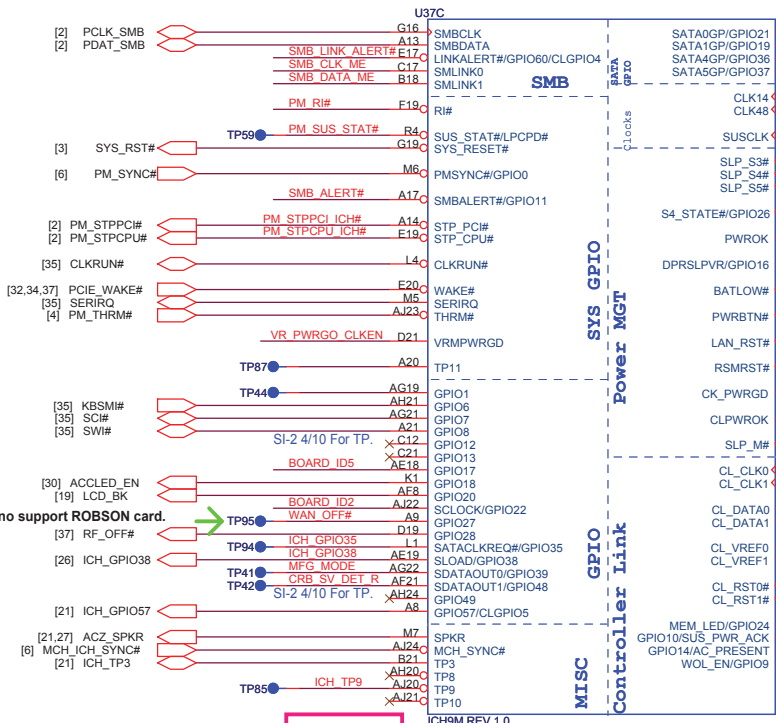
PROJECT : UT7
Quanta Computer Inc.

NB5

Size Custom Document Number ICH9-M PCIE 2/4 Rev E3A

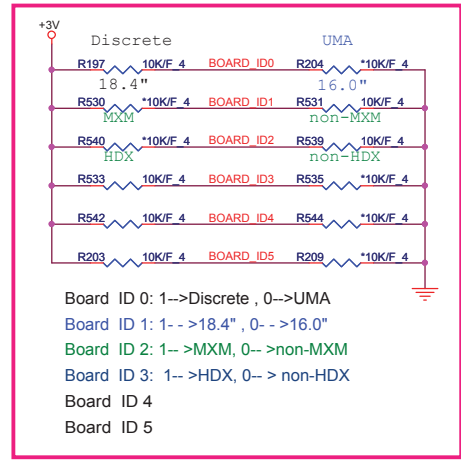
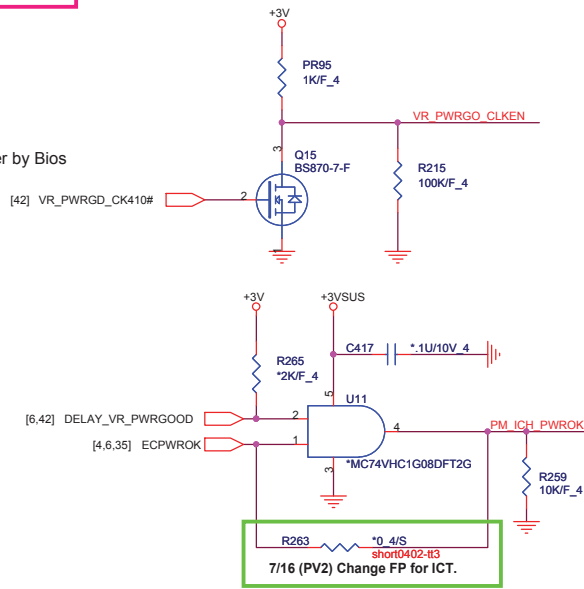
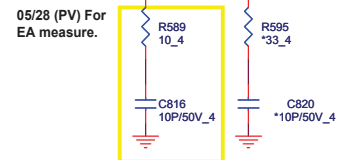
Date: Friday, July 18, 2008 Sheet 22 of 46

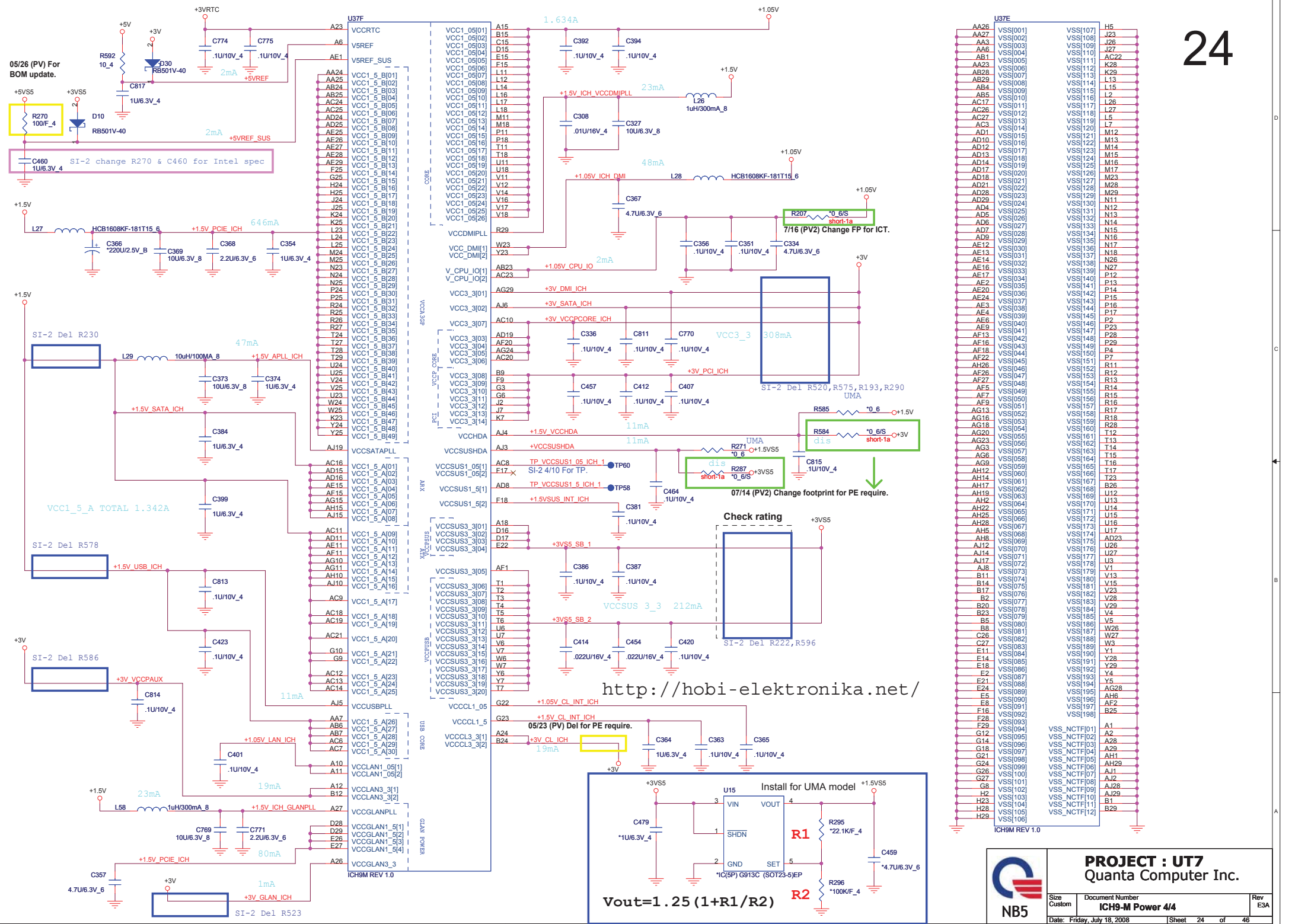
[2,4,6,9,10,11,12,14,15,19,20,21,22,24,25,26,27,28,29,30,31,32,34,35,37,38,42,43,45] +3V
 [21,22,24,34,45] +3VS5
 [31,37,41,42,43,45] +3VSUS



07/09 (PV2) Add TP95 for no support ROBSON card.

SI-2 Build
Delete R574,G2 as Bios_Rec can be cover by Bios





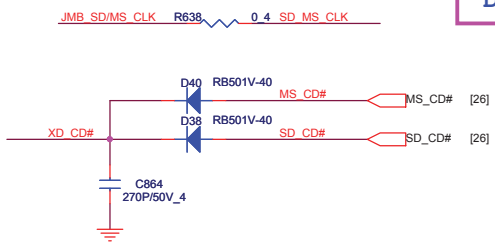
<http://hobi-elektronika.net/>

PROJECT : UT7
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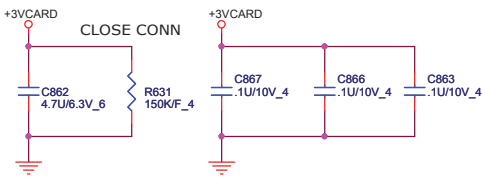
Size Custom Document Number ICH9-M Power 4/4 Rev E3A

Date: Friday, July 18, 2008 Sheet 24 of 46

Delete JMB 385

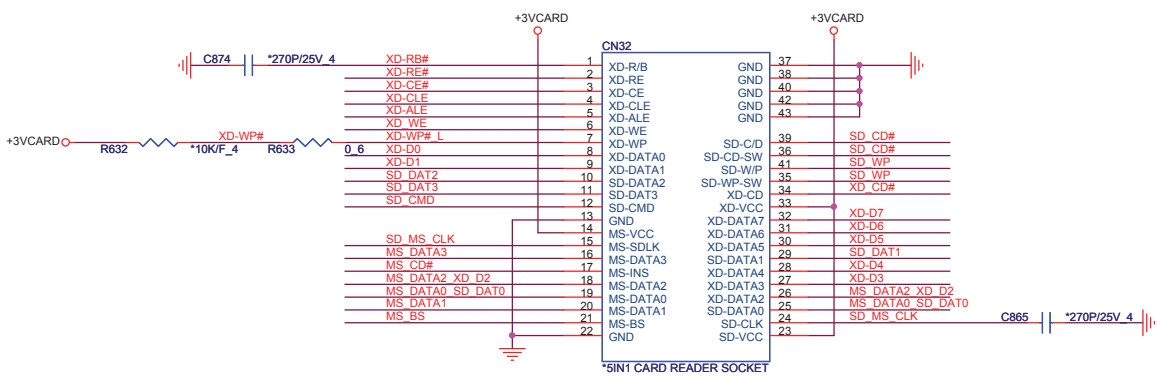


Close to CN34



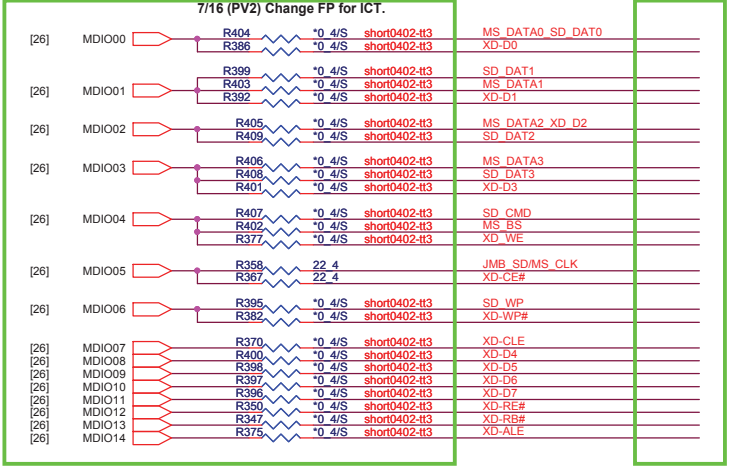
	SD/MMC	MS	XD
MDI00	SD DAT0	MS D0	XD D0
MDI01	SD DAT1	MS D1	XD D1
MDI02	SD DAT2	MS D2	XD D2
MDI03	SD DAT3	MS D3	XD D3
MDI04	SD CMD	MS BS	XD WE#
MDI05	SD CLK	MS SCLK	XD CE#
MDI06	SD WP		XD WP#
MDI07			XD CLE
MDI08	SD DAT4		XD D4
MDI09	SD DAT5		XD D5
MDI10	SD DAT6		XD D6
MDI11	SD DAT7		XD D7
MDI12			XD RE#
MDI13			XD RB#
MDI14			XD ALE
CR1 LEDN	SD1 LED#	MS1 LED#	XD LED#
CR1 PCTLN	SD1 PCTL#	MS1 PCTL#	XD1 PCTL#
CR1 CDO	SD1 CD#		XD CV#
CR1 CDT		MS1 CD#	XD CD#

5 IN1 CARD READER
XD, MMC/SD, MS/MSP

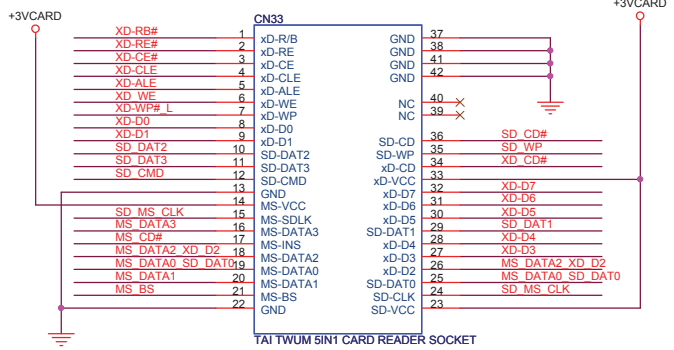


SI modified Footprint: "4in1-72700327123-43p-1"

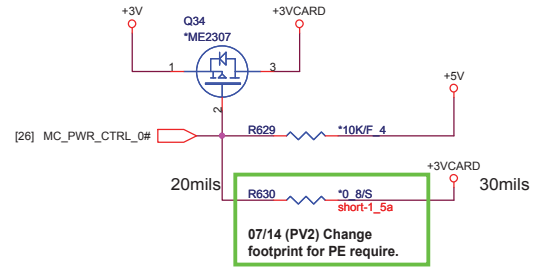
7/16 (PV2) Delete net for ICT.



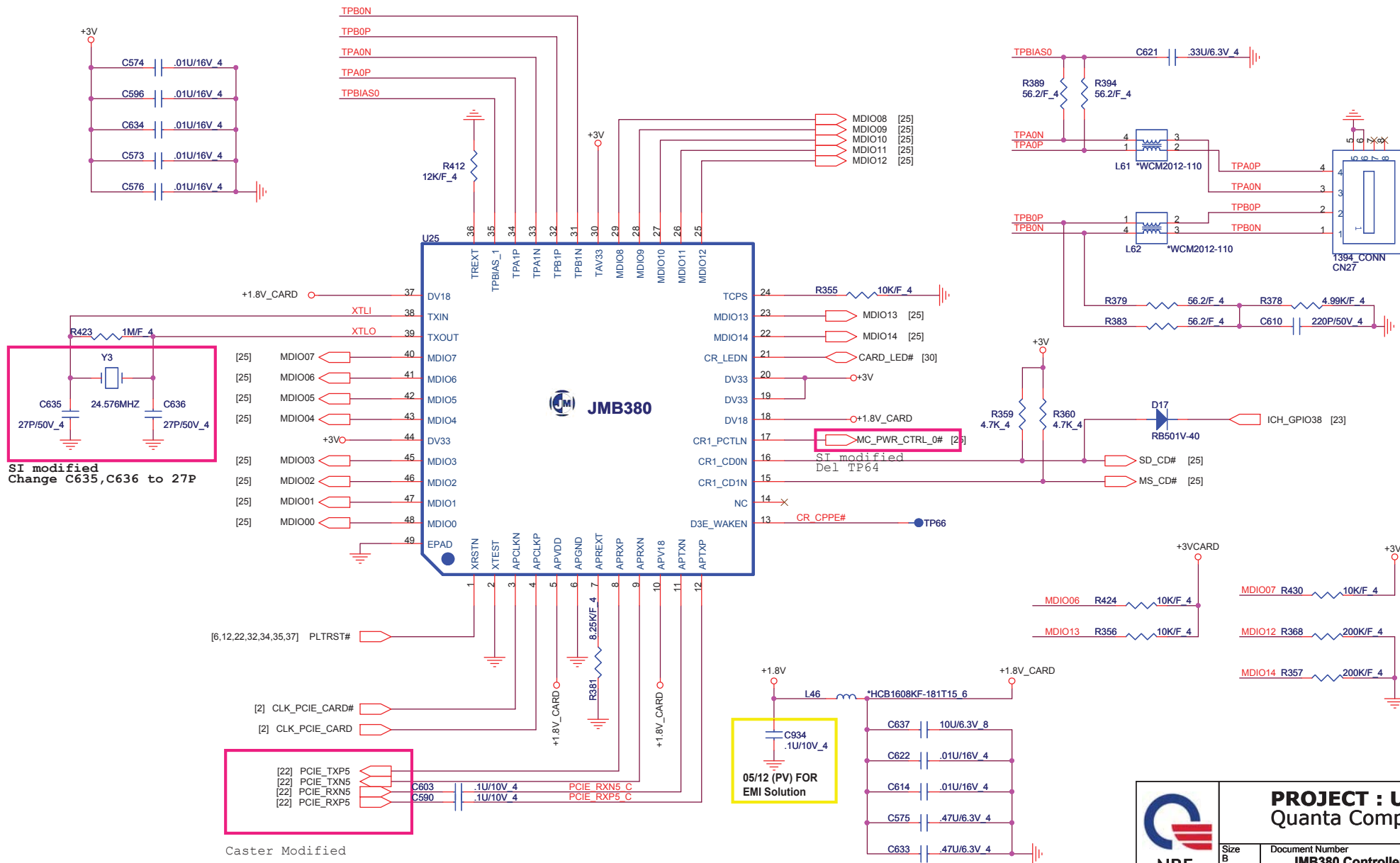
2ND SOURCE



SI modified Footprint: "7IN1-R015-B11-1M-42P-L"



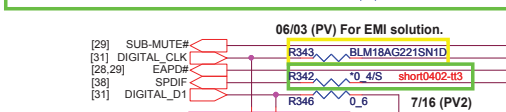
PROJECT : UT7
Quanta Computer Inc.



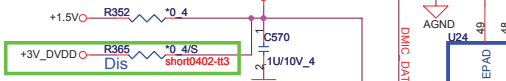
PROJECT : UT7
Quanta Computer Inc.

Size B	Document Number JMB380 Controller/1394	Rev E3A
Date: Friday, July 18, 2008	Sheet 26 of 46	

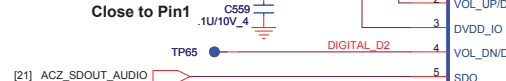
05/23 (PV) For IDT Dolby functionality.
07/14 (PV2) R697 change footprint for PE require.



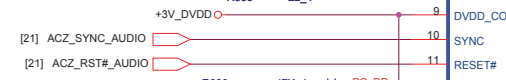
06/03 (PV) For EMI solution.
7/16 (PV2) Change FP for ICT.



07/14 (PV2) Change footprint for PE require.



05/12 (PV) FOR EMI Solution



07/14 (PV2) Change footprint for PE require.



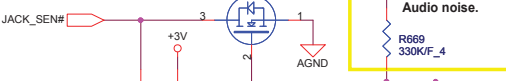
07/14 (PV2) Change footprint for PE require.



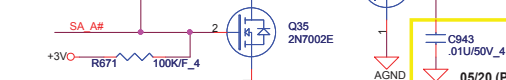
07/14 (PV2) Change footprint for PE require.



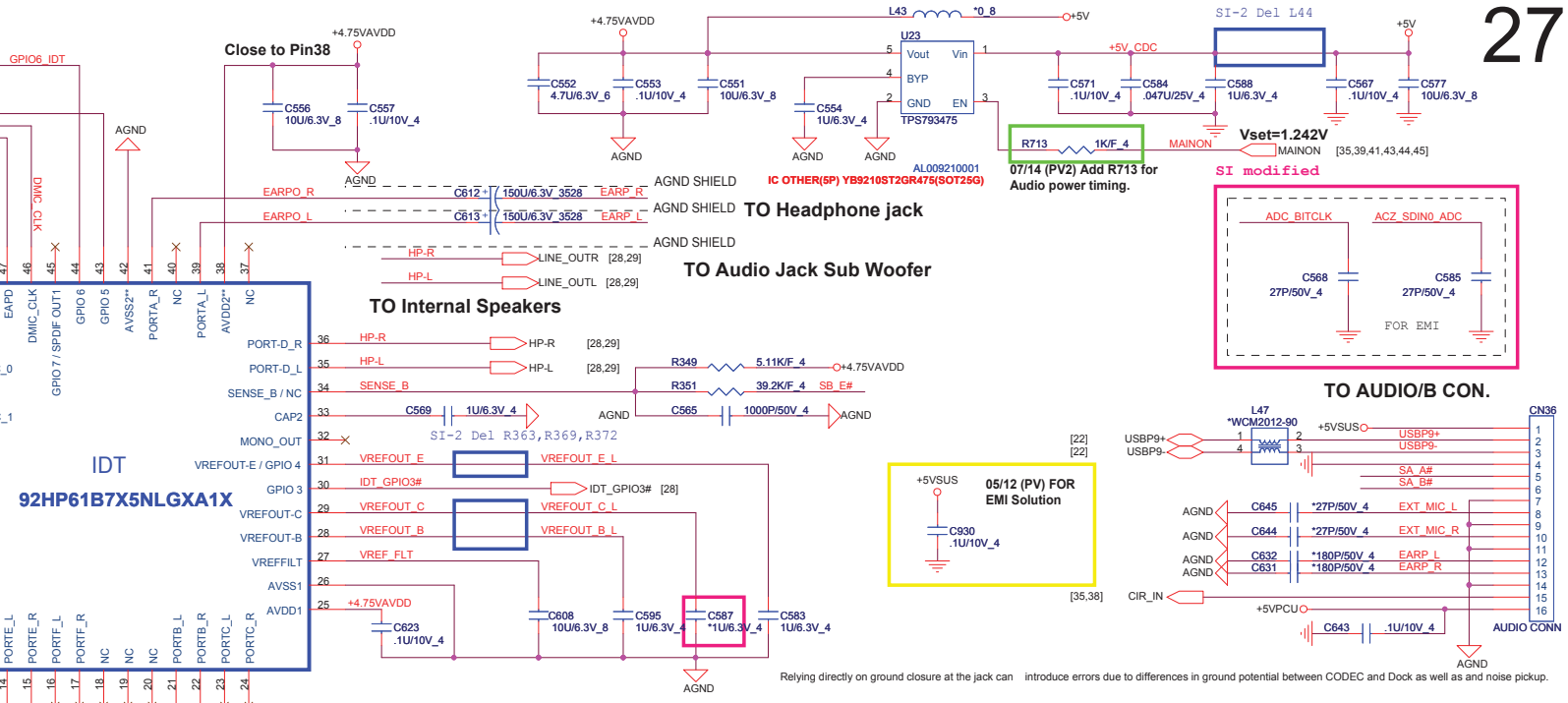
07/14 (PV2) Change footprint for PE require.



07/14 (PV2) Change footprint for PE require.

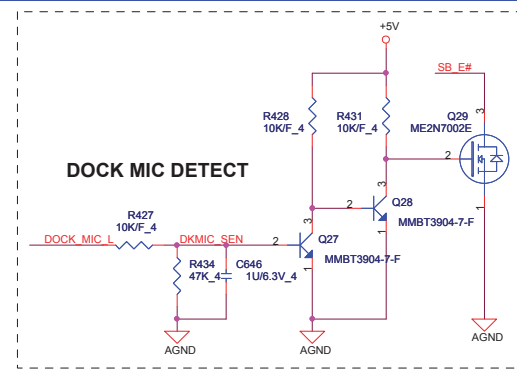
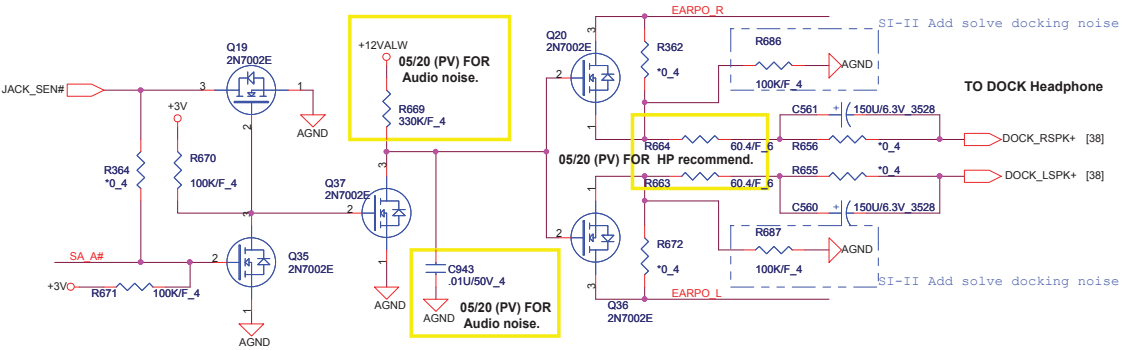
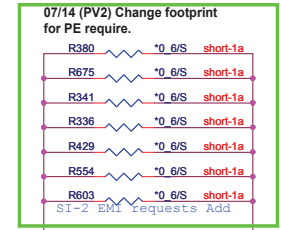


07/14 (PV2) Change footprint for PE require.



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PORT	PLACE TO
MONO_OUT	X
PORT A	HP OUT
PORT B	M/B MIC
PORT C	X
PORT D	Internal Speakers
PORT E	Docking MIC
PORT F	X
DM	DIGITAL MIC



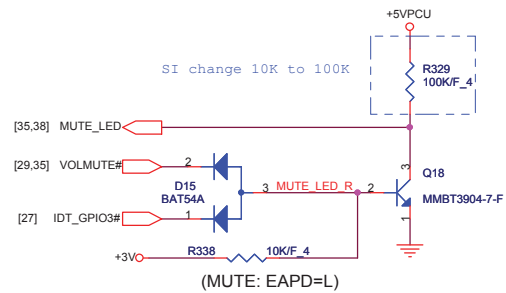
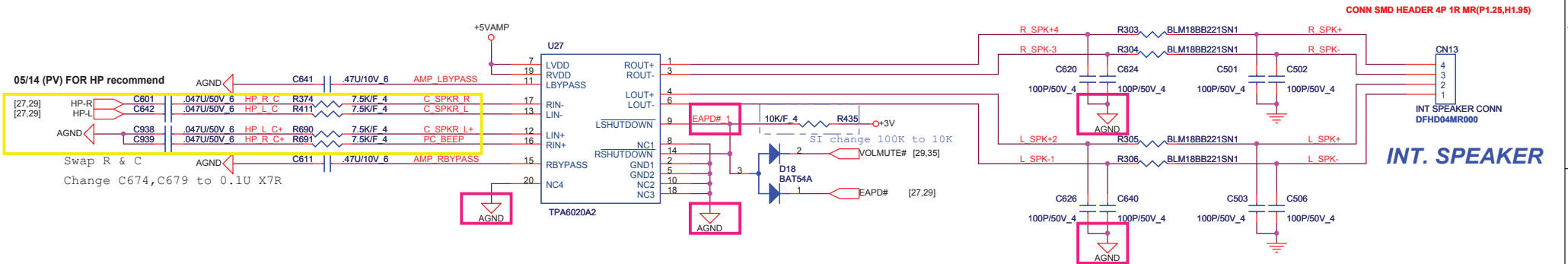
SA_A# -->EXT HP
SA_B# -->EXT MIC
SB_E#--> DOCK MIC
Audio JACK: Normal Open

PROJECT : UT7
Quanta Computer Inc.

NB5

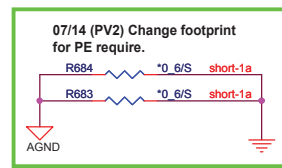
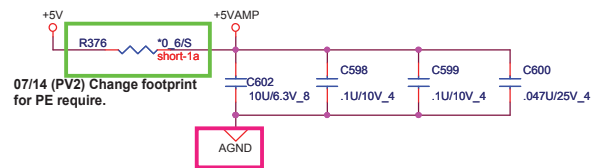
Size Custom Document Number Azalia IDT92HD71B7 Rev E3A
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AUDIO AMPLIFIER



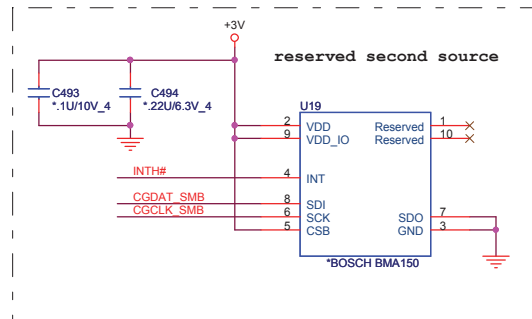
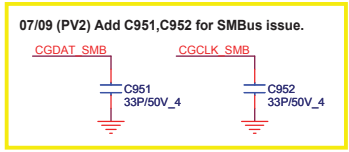
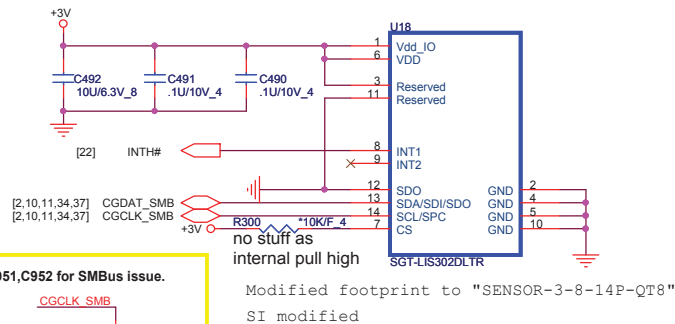
07/09 (PV2) Delete for 2ND FAN function.

Delete Gain set



Del R373, R677, R676
Del AMP_GND to AGND

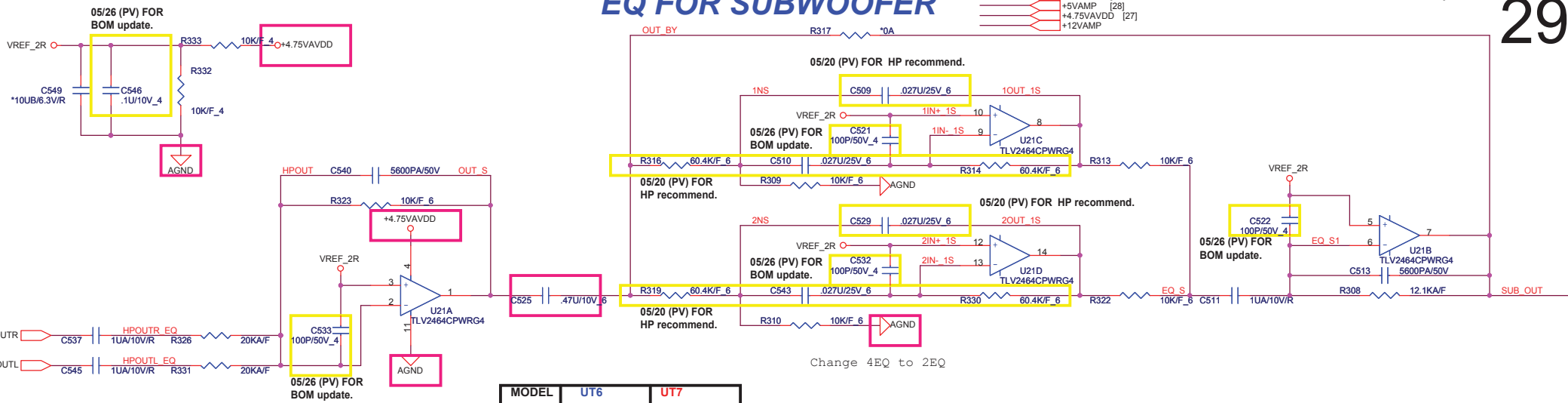
Accelerometer Sensor



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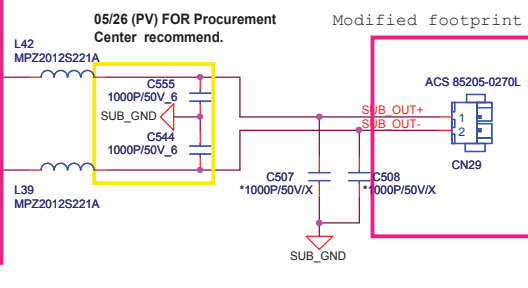
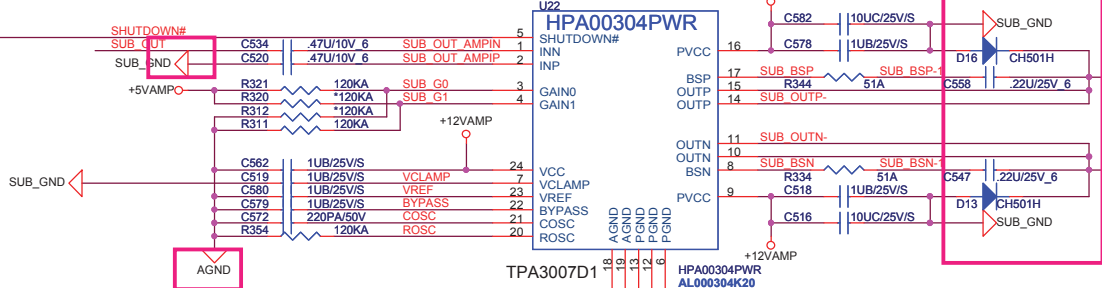
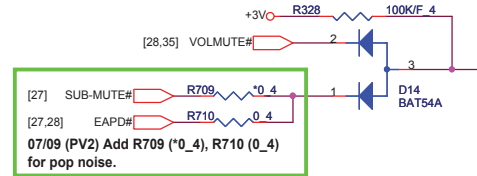
EQ FOR SUBWOOFER

[2,4,6,9,10,11,12,14,15,19,20,21,22,23,24,25,26,27,28,30,31,32,34,35,37,38,42,43,45]
 +3V [28]
 +5VAMP [27]
 +4.75VAVDD [27]
 +12VAMP

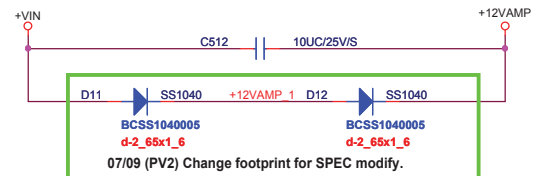


MODEL	UT6	UT7
R316	60.4K/F_6	40.2K/F_6
R319	60.4K/F_6	40.2K/F_6
R330	60.4K/F_6	80.6K/F_6
R314	60.4K/F_6	80.6K/F_6
C509	0.027U/25V_6	0.022U/50V_6
C510	0.027U/25V_6	0.022U/50V_6
C529	0.027U/25V_6	0.039U/16V_6
C543	0.027U/25V_6	0.039U/16V_6

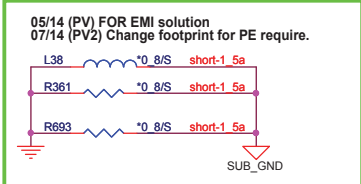
Change 4EQ to 2EQ



Sub-Woofer power



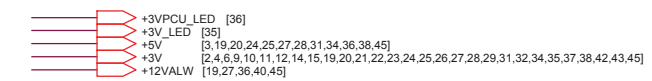
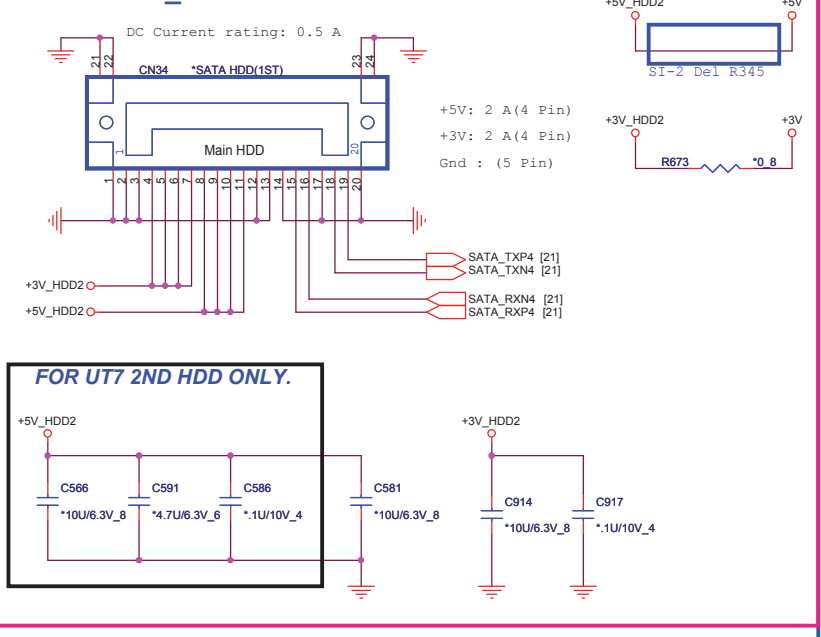
Del HP_GND to GND
 Del R307, R315
 Delete L1003



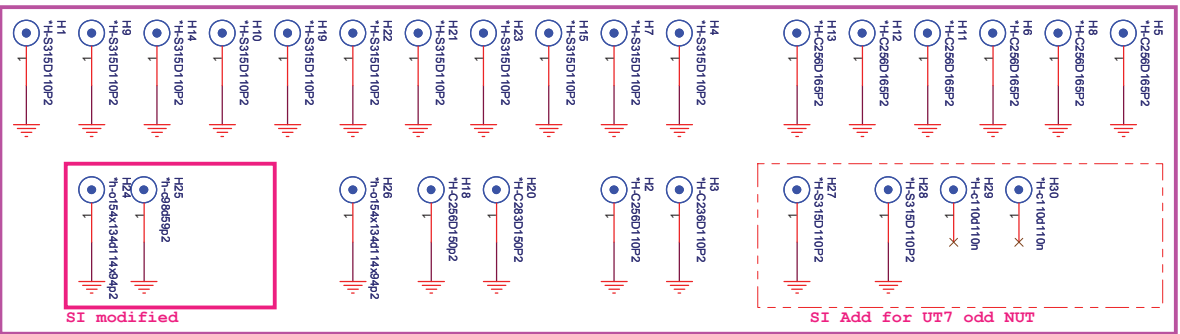
PROJECT : UT7
Quanta Computer Inc.

Size Custom	Document Number SUBWOOFER(EQ & AMP.)	Rev E3A
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SATA_2 CONNECTOR

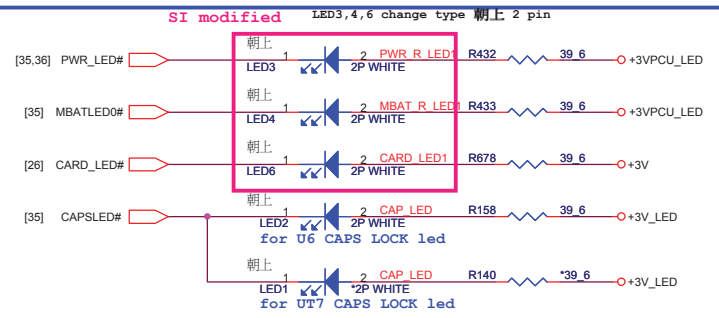
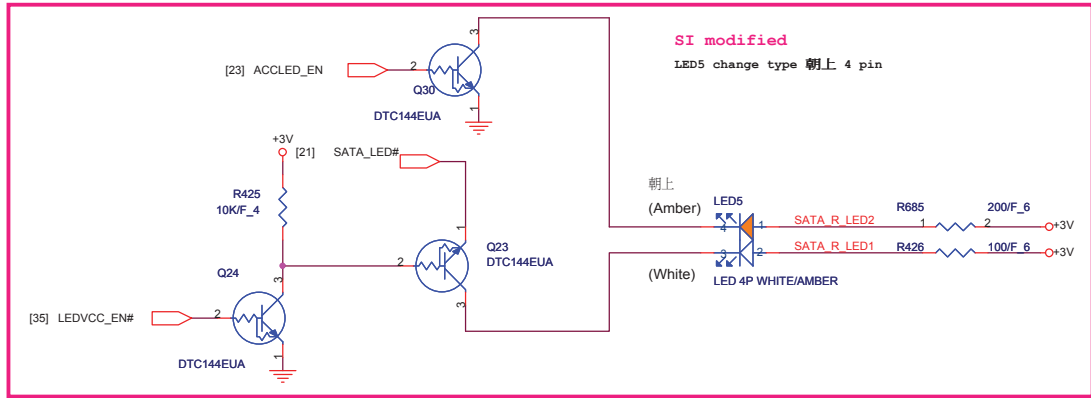
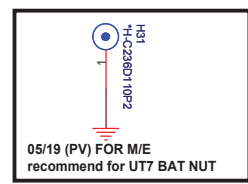
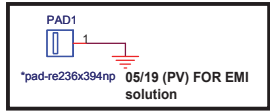


30

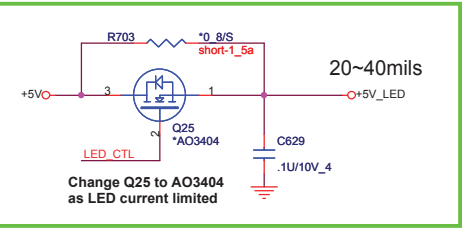
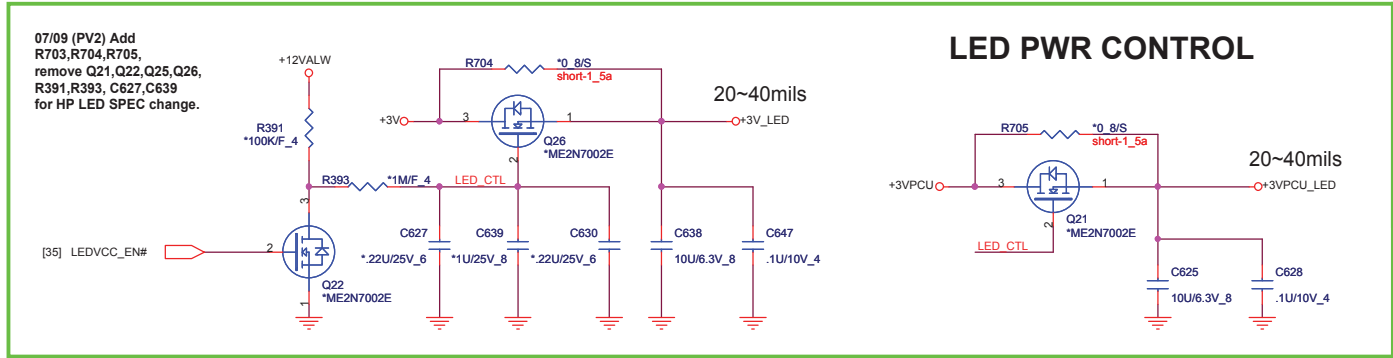


delete all PAD & change screw footprint

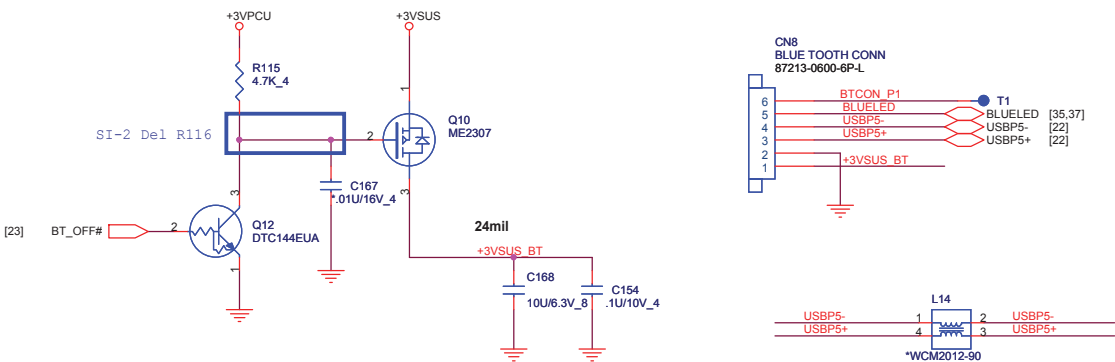
07/14 (PV2) Delete H16,H17 for no support ROBSON card.



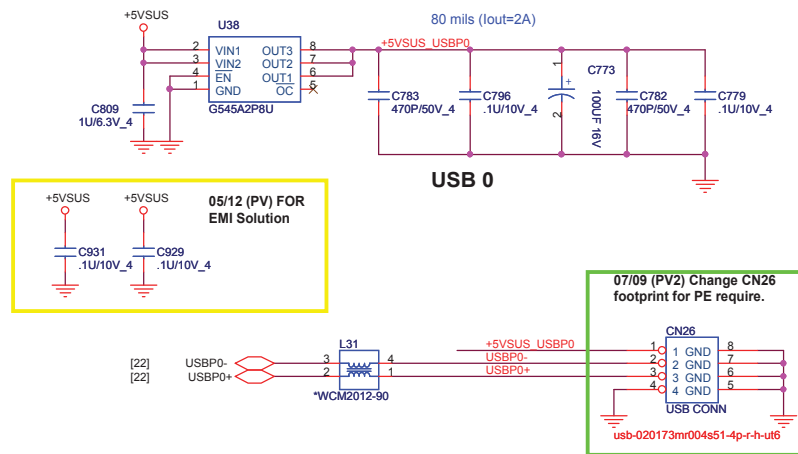
<http://hobi-elektronika.net/>



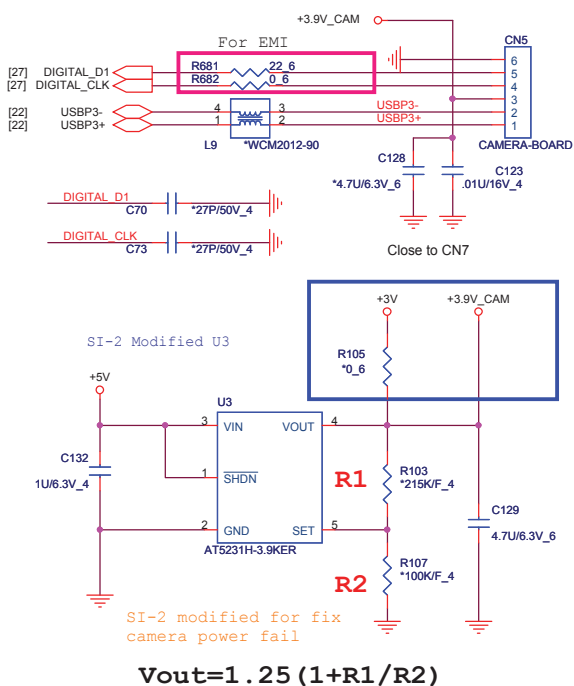
BLUETOOTH



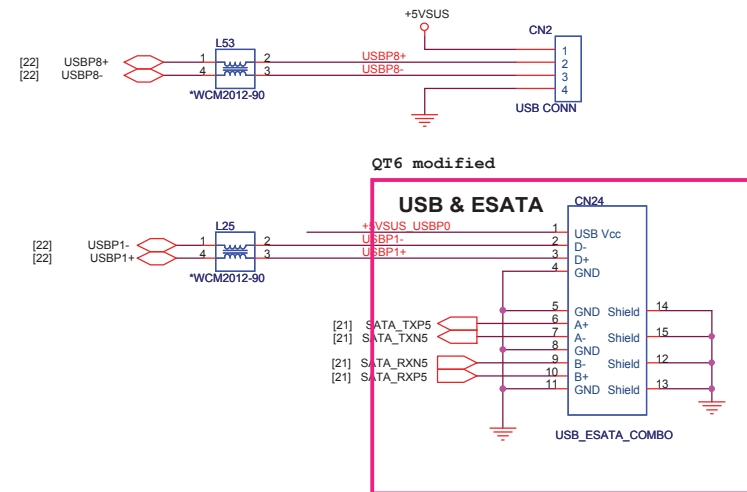
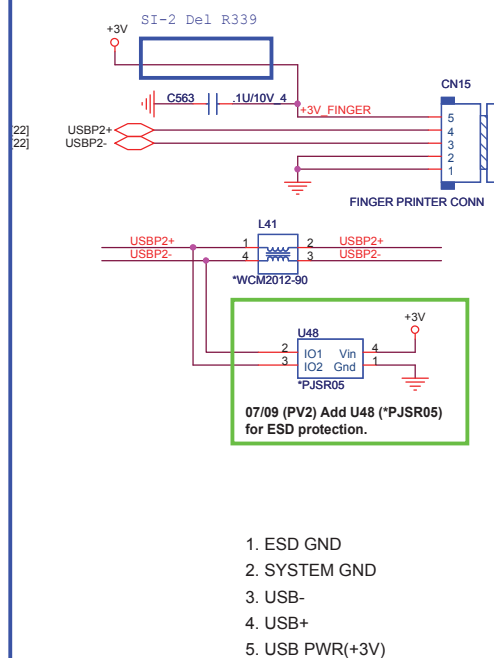
USB1 and E-SATA



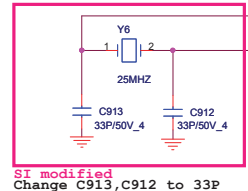
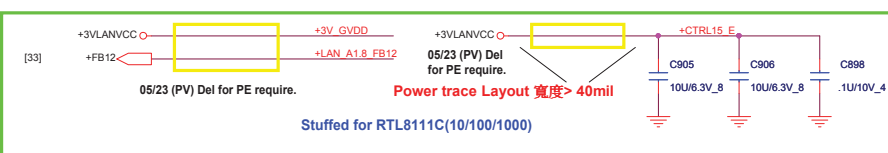
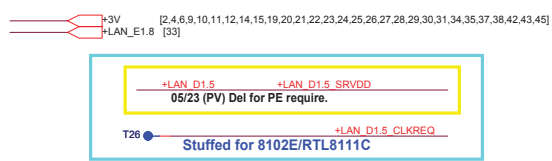
USB CAMERA /DIGITAL MIC CONNECT



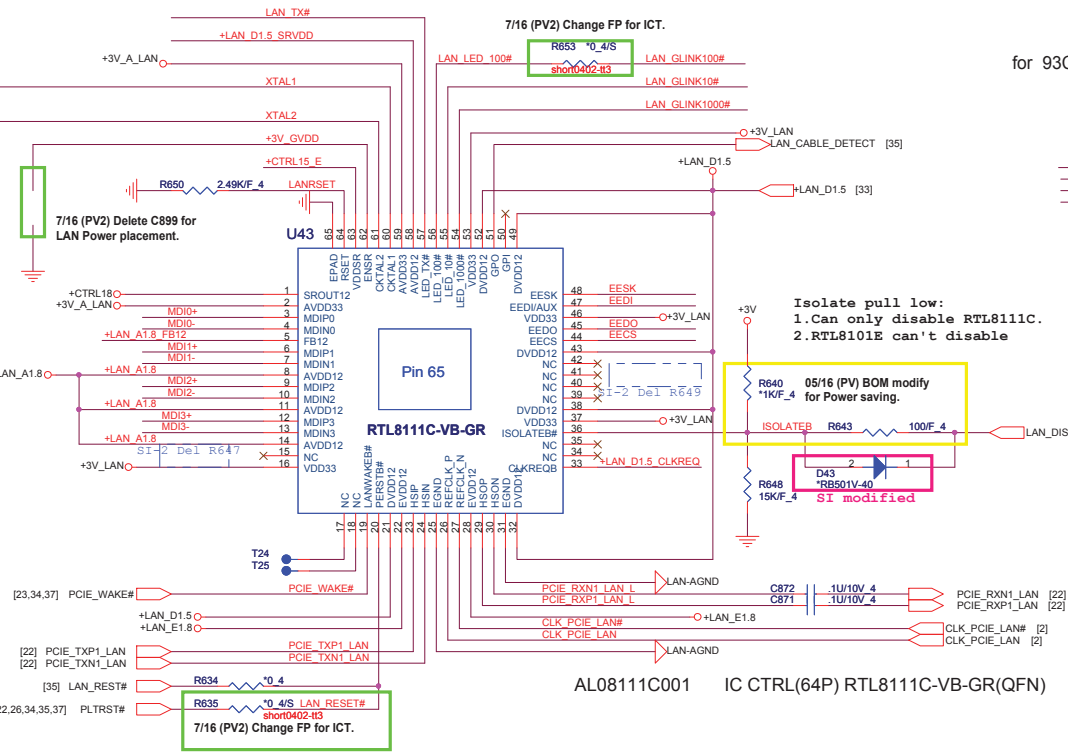
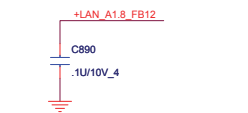
USB fingerprint CON



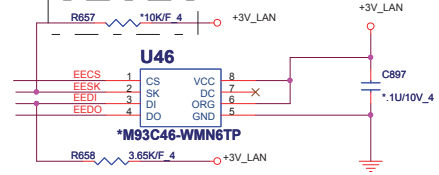
T : Stuffed for RTL8111C(10/100/1000)



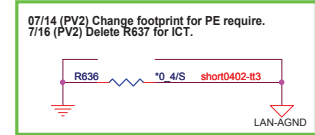
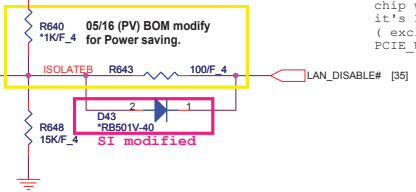
U18#63 wider than 40 mils
U18#1 wider than 60 mils



for 93C56 used. NC if 93C46 is used.

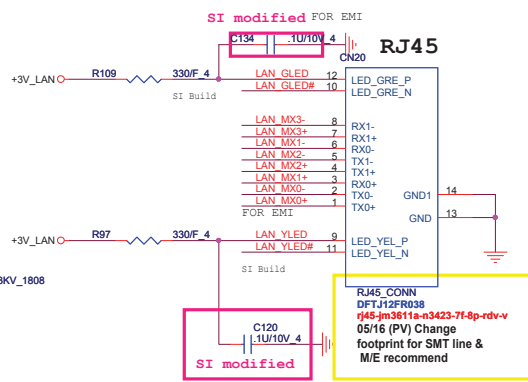
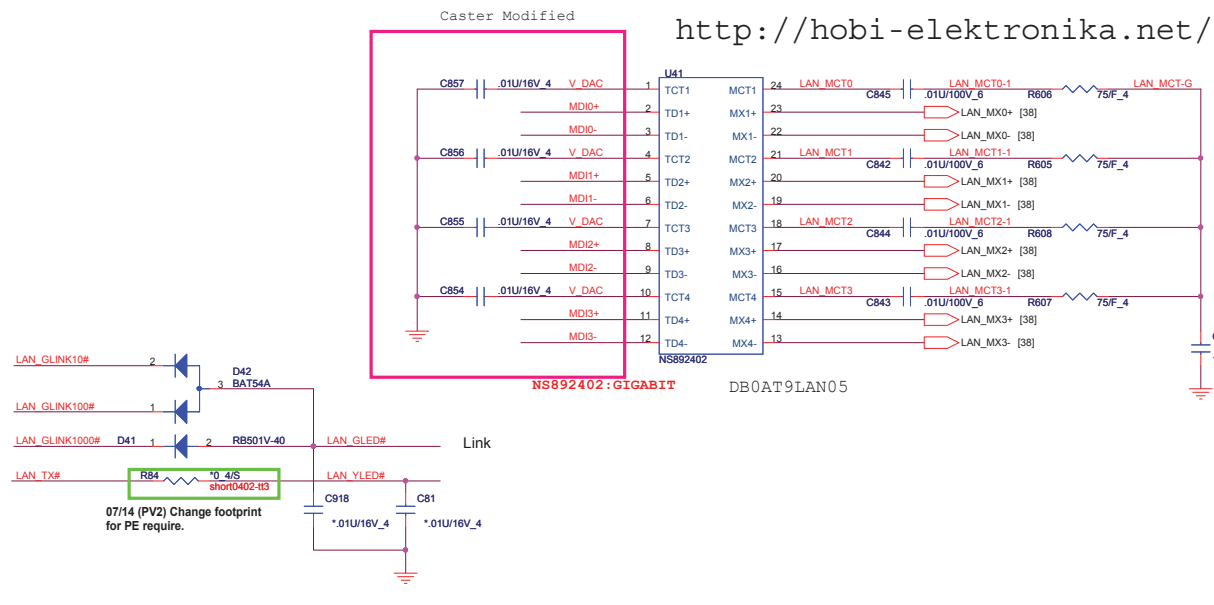


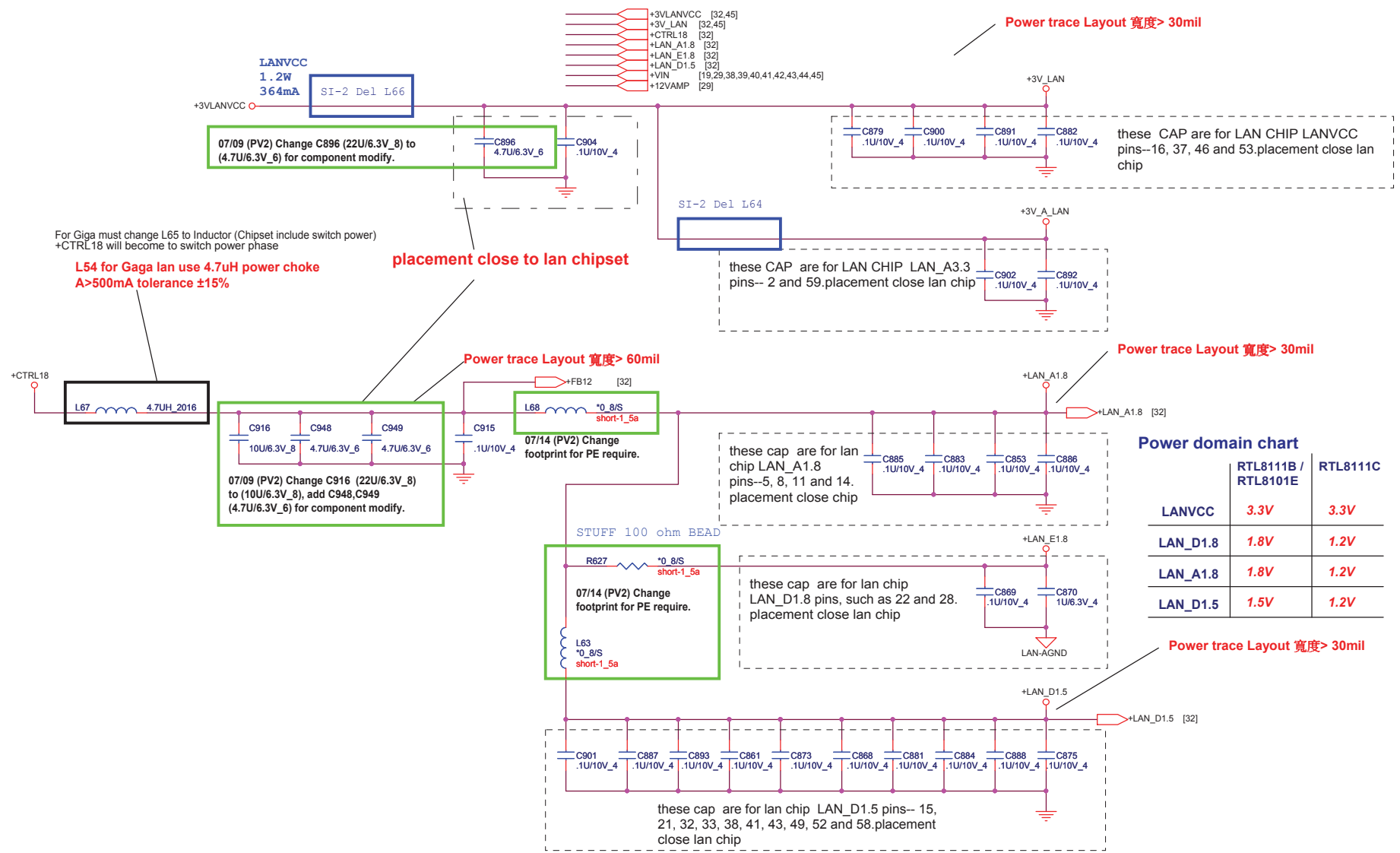
if ISOLATEB pin pull-low, the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)



AL08111C001 IC CTRL(64P) RTL8111C-VB-GR(QFN)

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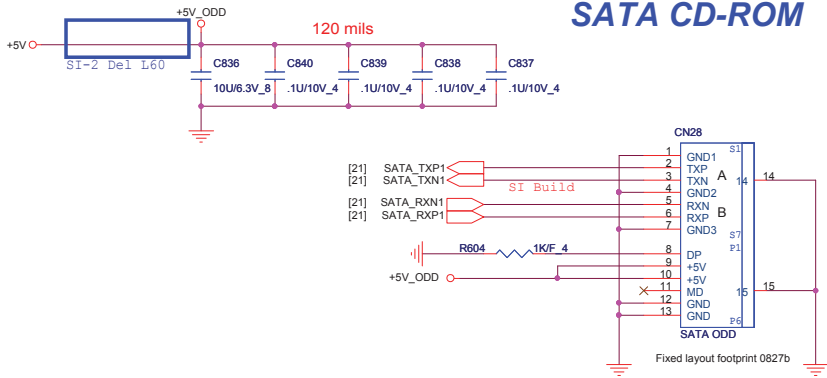




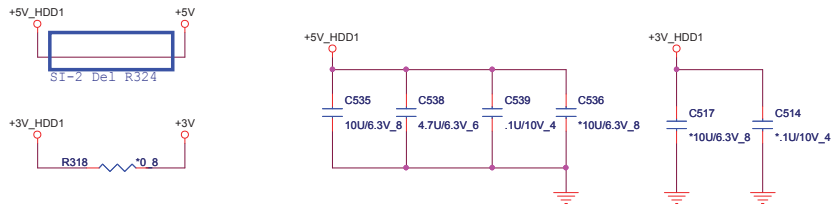
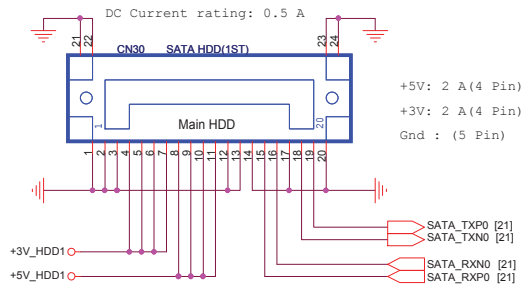
Power domain chart

	RTL8111B / RTL8101E	RTL8111C
LANVCC	3.3V	3.3V
LAN_D1.8	1.8V	1.2V
LAN_A1.8	1.8V	1.2V
LAN_D1.5	1.5V	1.2V

SATA CD-ROM

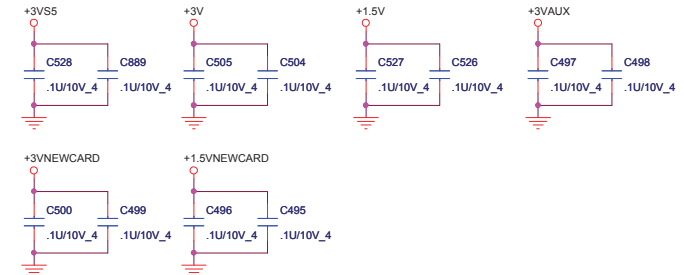
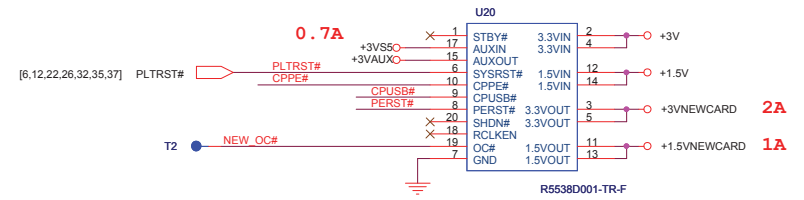
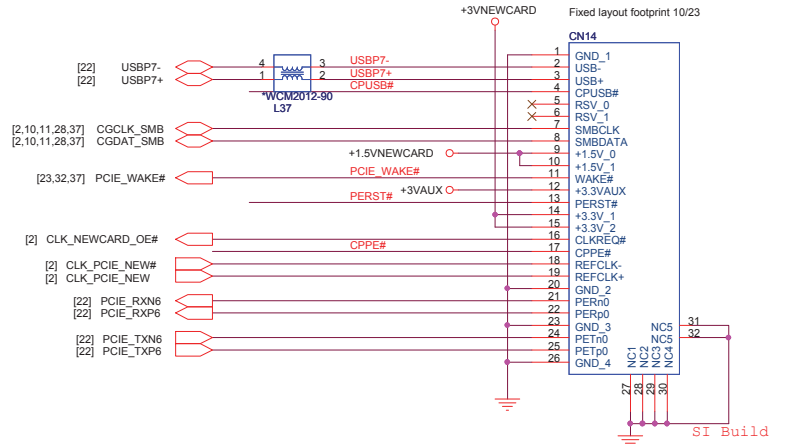


SATA_1 CONNECTOR

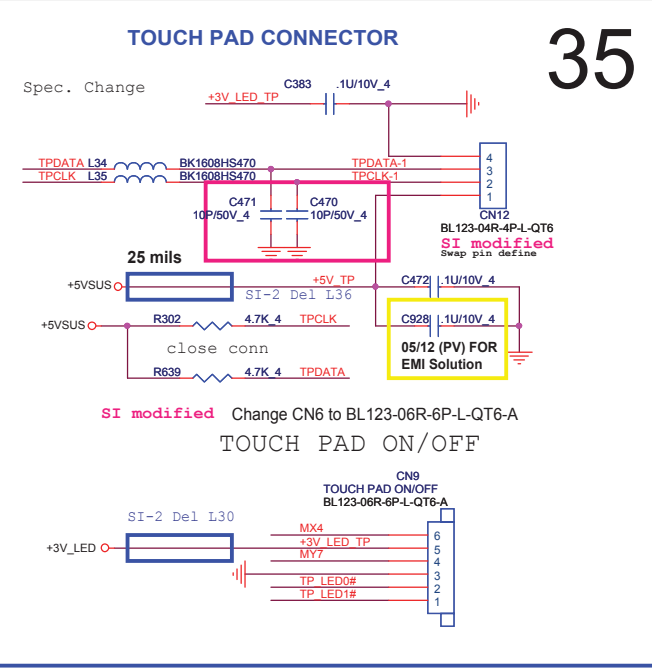
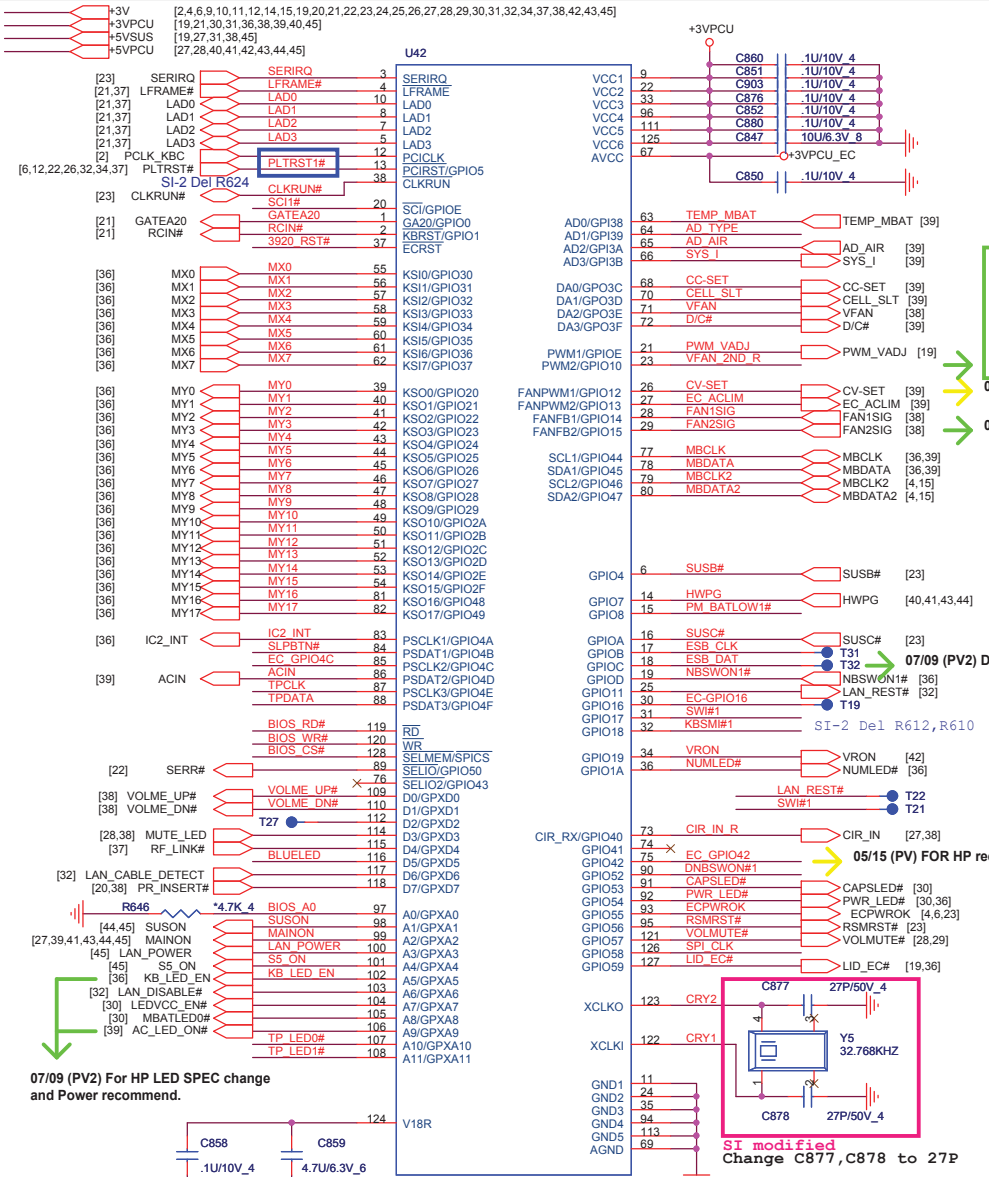


NEWCARD

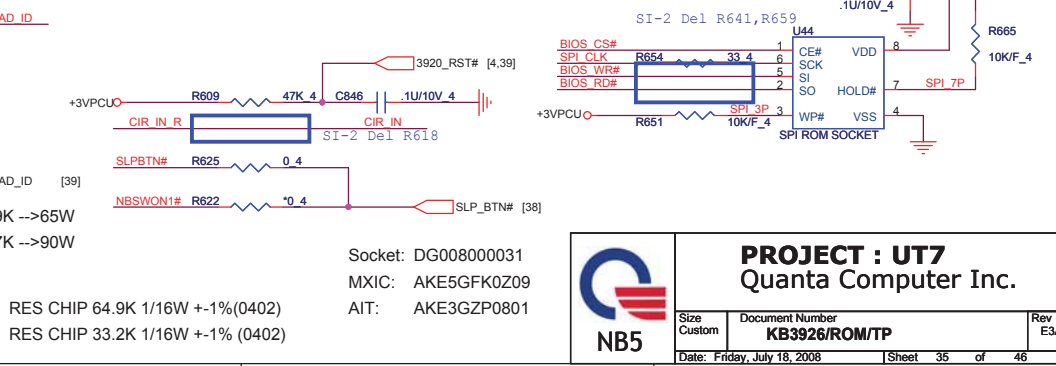
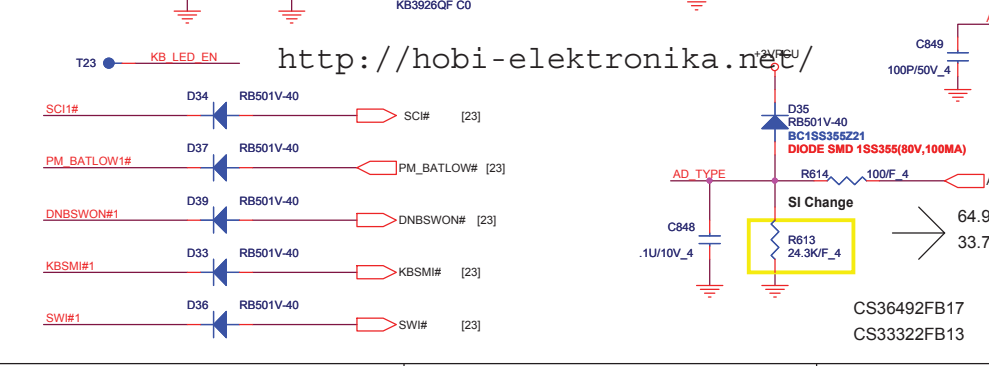
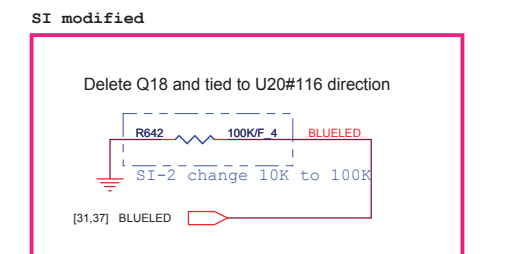
NEWCARD (PCIEXPRESS*1 + USB*1)



	<p>PROJECT : UT7 Quanta Computer Inc.</p>	
	<p>Size Custom</p>	<p>Document Number ODD/HDD/NEW CARD</p>
<p>Date: Friday, July 18, 2008</p>		<p>Sheet 34 of 46</p>



MODEL	UT7 120W (H)	UT6 90W (L)	UT6 65W (0.5V)
R694	8.25K/F_4	N/A	45.3K/F_4
R695	N/A	8.25K/F_4	8.25K/F_4

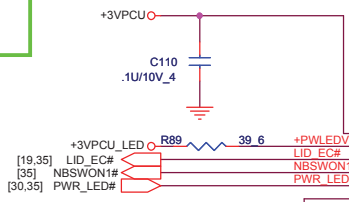
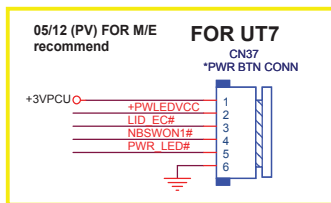
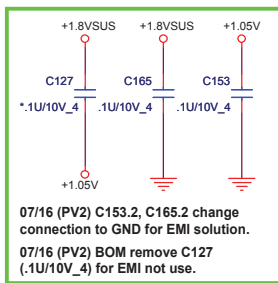


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Quanta Computer Inc.

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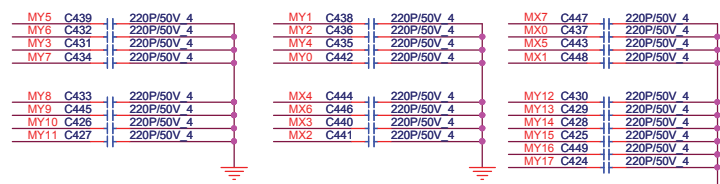
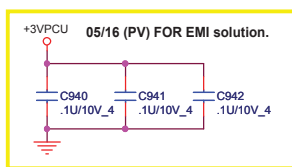
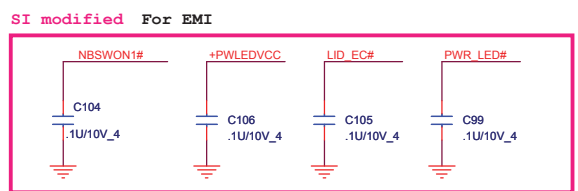
<http://hobi-elektronika.net/>



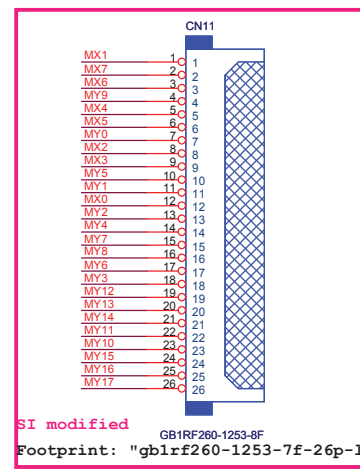
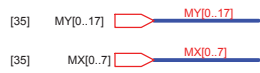
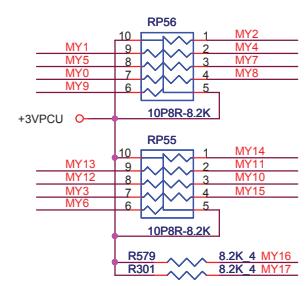
- FOR UT6**
1. +3VPCU(LIDSWITCH PWR)
 2. LEDVCC(+3VPCU)
 3. LIDSWITCH
 4. POWERON#
 5. PWLED#
 6. GND

SI modified Change CN6 to BL123-06R-6P-L-QT6-A

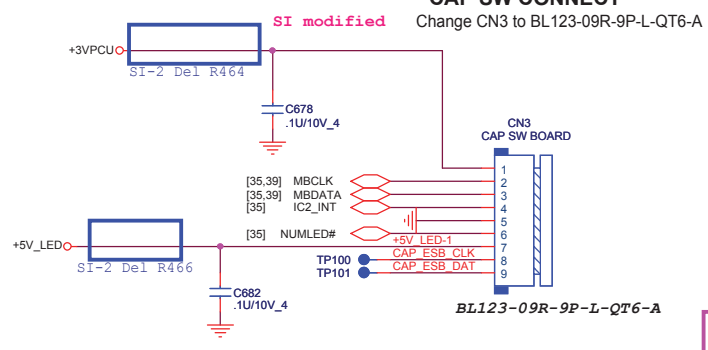
POWER BOTTOM CONNECT



KEYBOARD PULL-UP

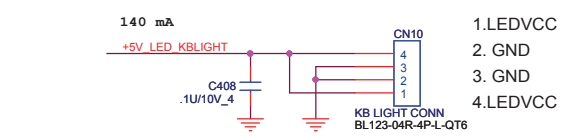
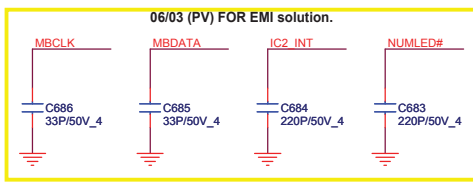


CAP SW CONNECT

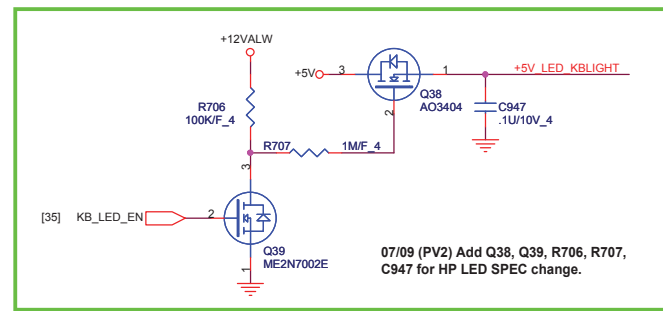


1. +3VPCU
2. MBCLK
3. MBDATA
4. CAP_INT
5. GND
6. NUM LOCK LED
7. +5V_LED
8. ESB_CLK
9. ESB_DAT

07/14 (PV2) Delete L69,L70,C922,C923 for EMI solution.



- 1.LEDVCC
2. GND
3. GND
- 4.LEDVCC

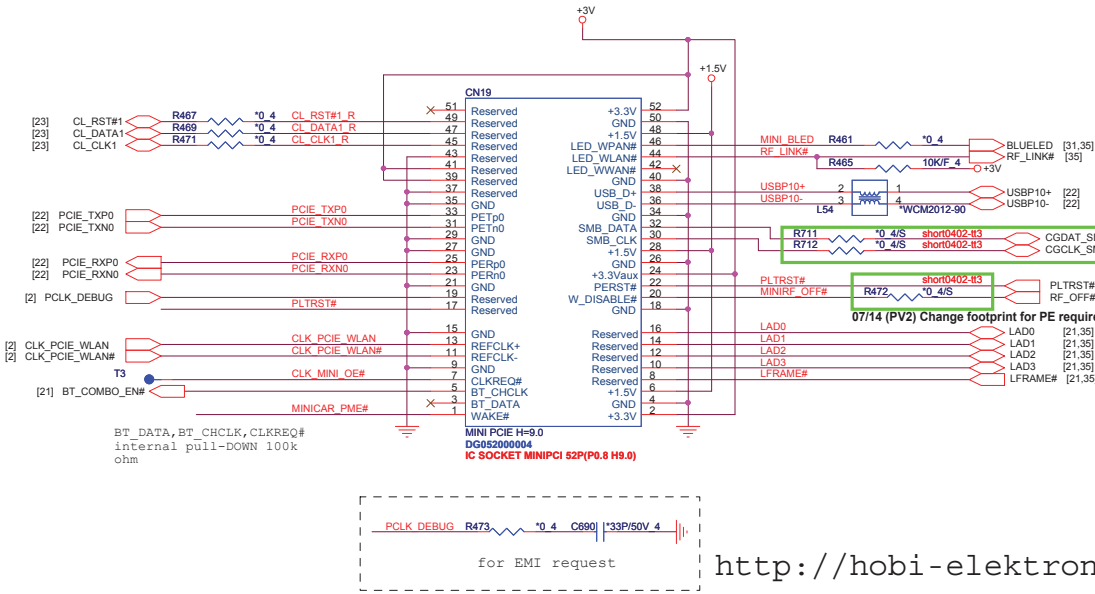


07/09 (PV2) Add Q38, Q39, R706, R707, C947 for HP LED SPEC change.

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Mini PCI-E Card 1 WLAN

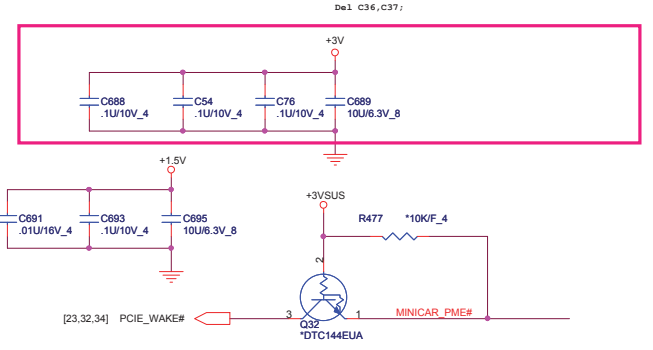
Delete R110,R78
+3V must have a 120mil plane
Each pin 25mil



07/09 (PV2) Add R711,R712 for SMBus issue.

07/14 (PV2) Change footprint for PE require.

INTEL WLAN CARD PIN 20 W_DISABLE# have internal pull-up 110k ohm

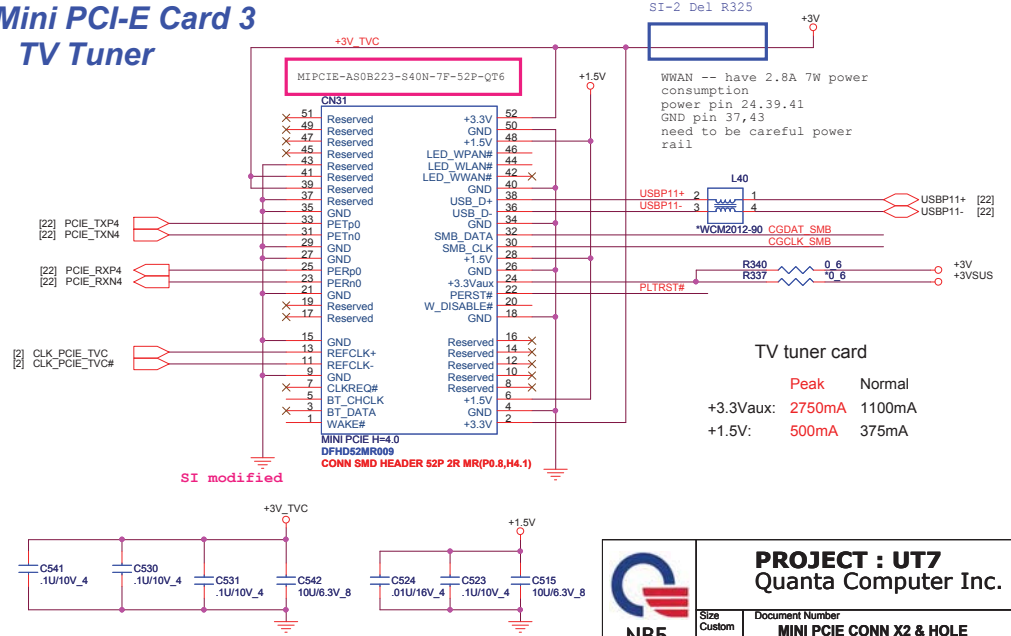


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Mini PCI-E Card 2 ROBSON

07/09 (PV2) Delete for no support ROBSON card.

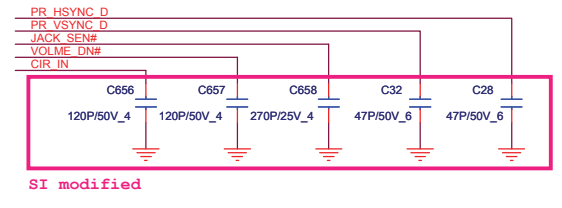
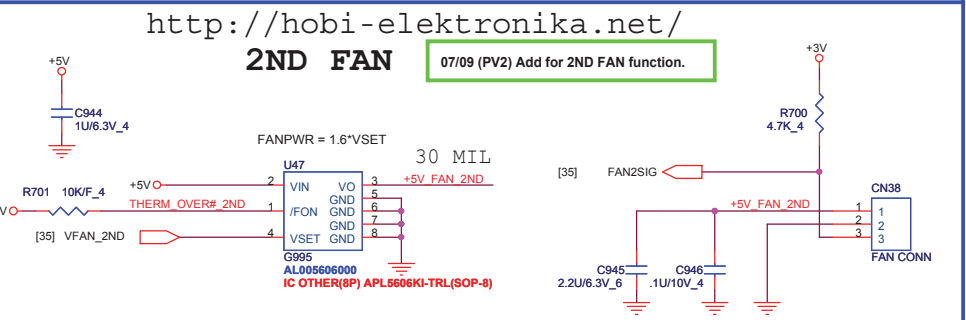
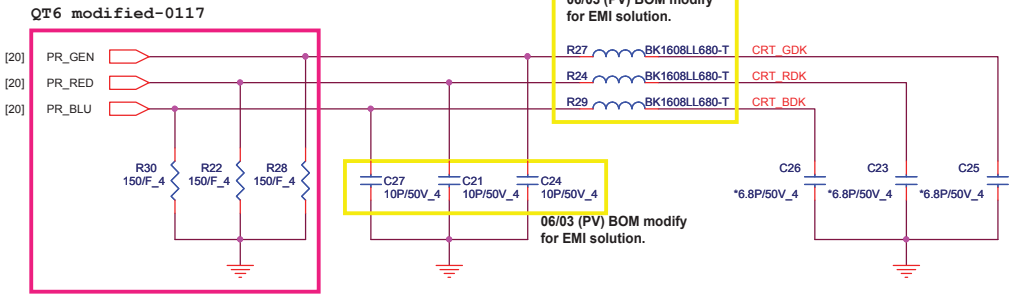
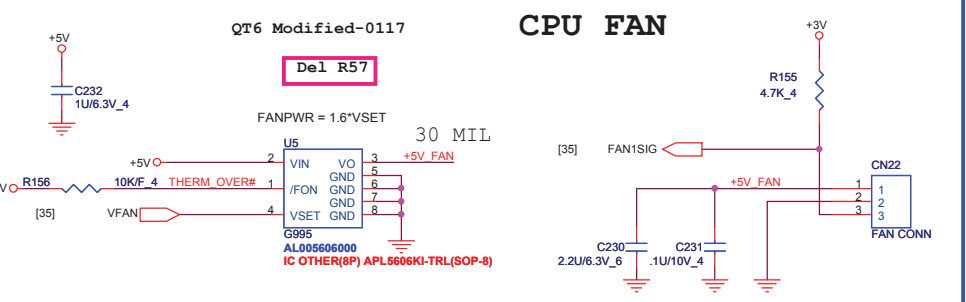
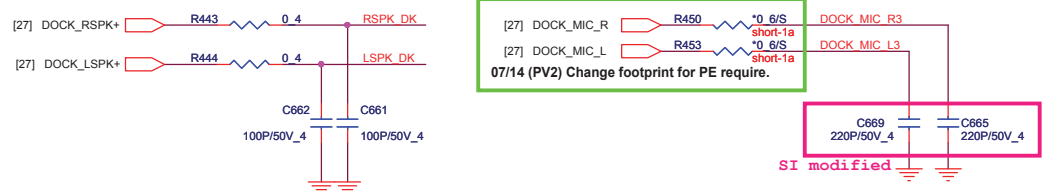
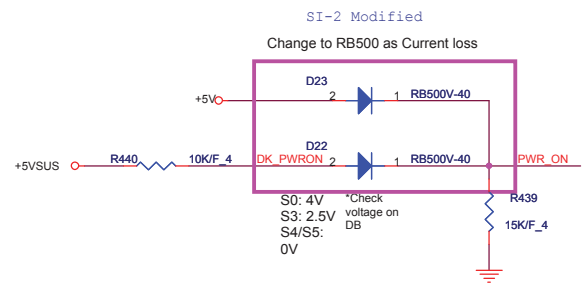
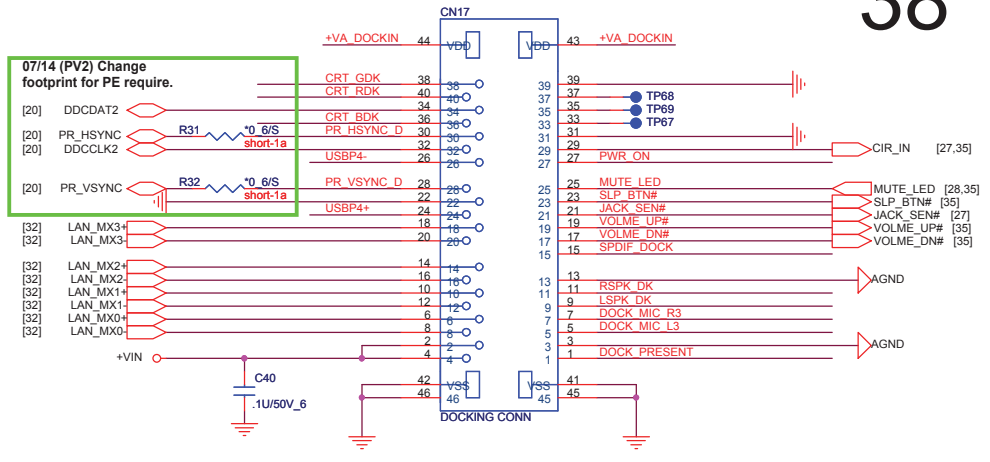
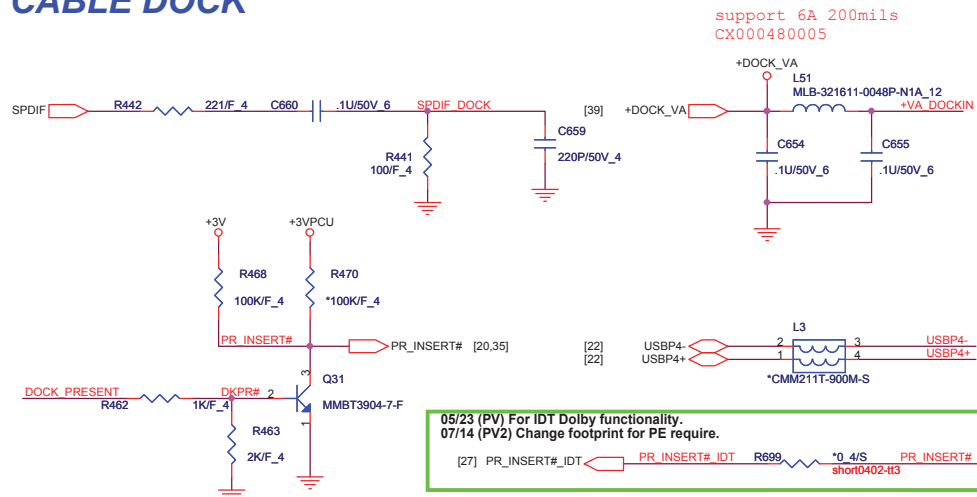
Mini PCI-E Card 3 TV Tuner



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Quanta Computer Inc.

Size Custom Document Number MINI PCI-E CONN X2 & HOLE Rev E3A

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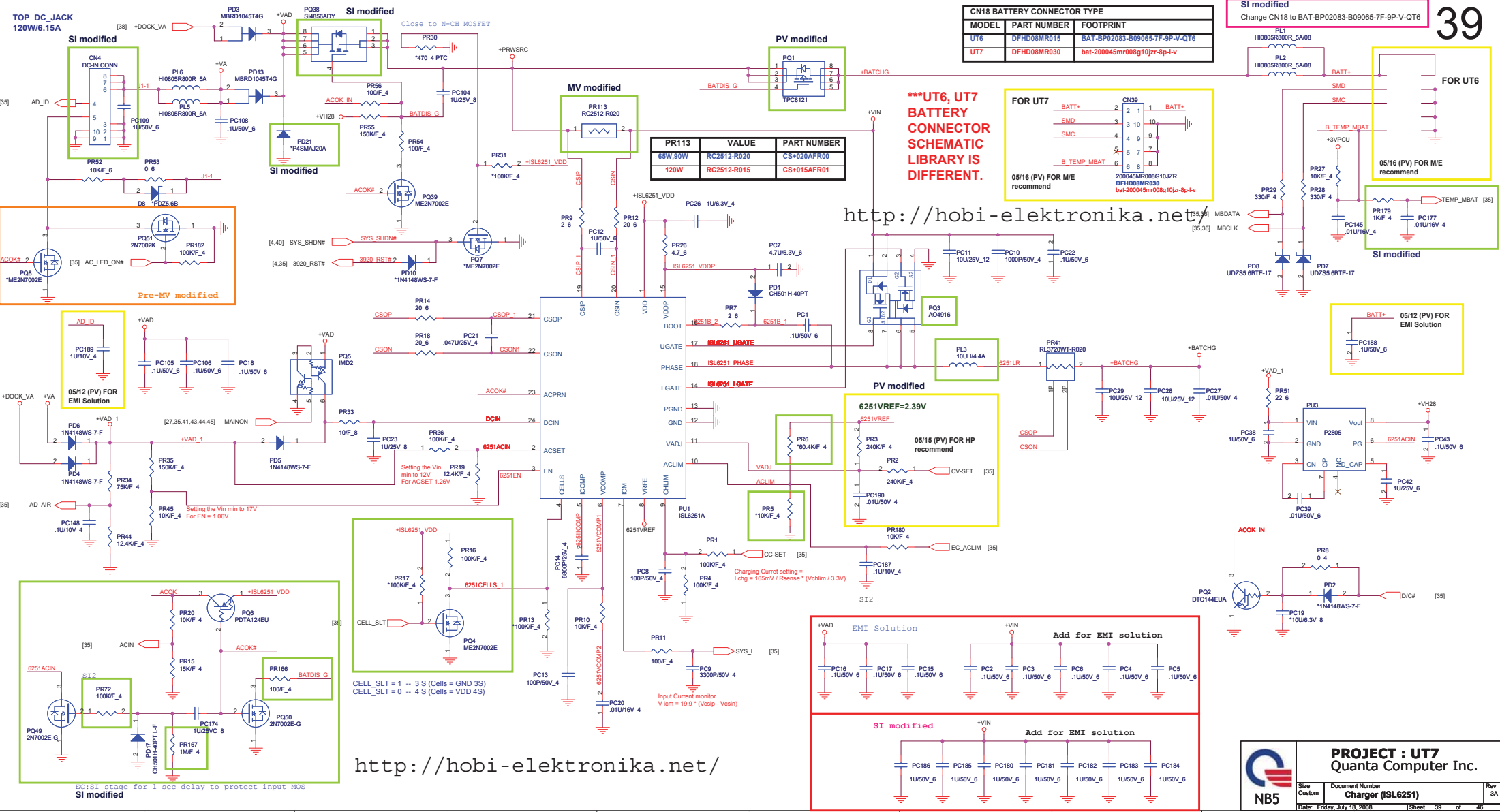
	PROJECT : UT7		Rev E3A
	Quanta Computer Inc.		
	Size Custom	Document Number CABLE DOCKING/FAN	
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TOP_DC_JACK
120W/6.15A

CN18 BATTERY CONNECTOR TYPE		
MODEL	PART NUMBER	FOOTPRINT
UT6	DFHD08MR015	BAT-8P02083-B09065-7F-9P-V-QT6
UT7	DFHD08MR030	bat-200045m009g10zr-8p-l-v

SI modified
Change CN18 to BAT-8P02083-B09065-7F-9P-V-QT6

39



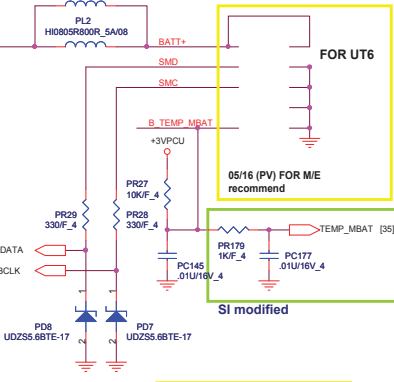
PR113	VALUE	PART NUMBER
65W,90W	RC2512-R020	CS*020AFR00
120W	RC2512-R015	CS*015AFR01

*****UT6, UT7 BATTERY CONNECTOR SCHEMATIC LIBRARY IS DIFFERENT.**

FOR UT7

BATT+ 2 2 1 1 BATT+
SMD 3 3 10 10
SMC 4 4 9 9
B_TEMP_MBAT 6 6 8 8

05/16 (PV) FOR M/E recommend
200045MR008G10ZR
DFHD08MR030
bat-200045m009g10zr-8p-l-v



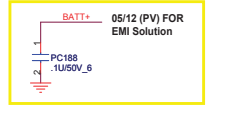
<http://hobi-elektronika.net/>

PV modified

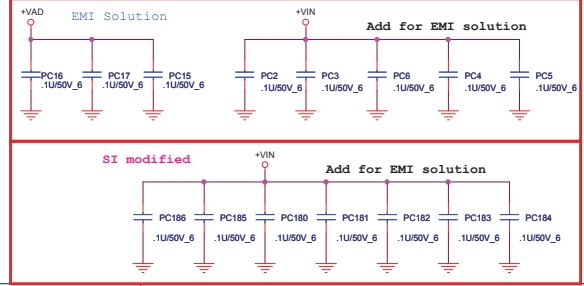
6251VREF=2.39V

05/15 (PV) FOR HP recommend

PR3 240KF_4
PR2 240KF_4
PC130 01U50V_4



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PROJECT : UT7 Quanta Computer Inc.

Charger (ISL6251)

Size Custom Document Number Rev 3A
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DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V ALW

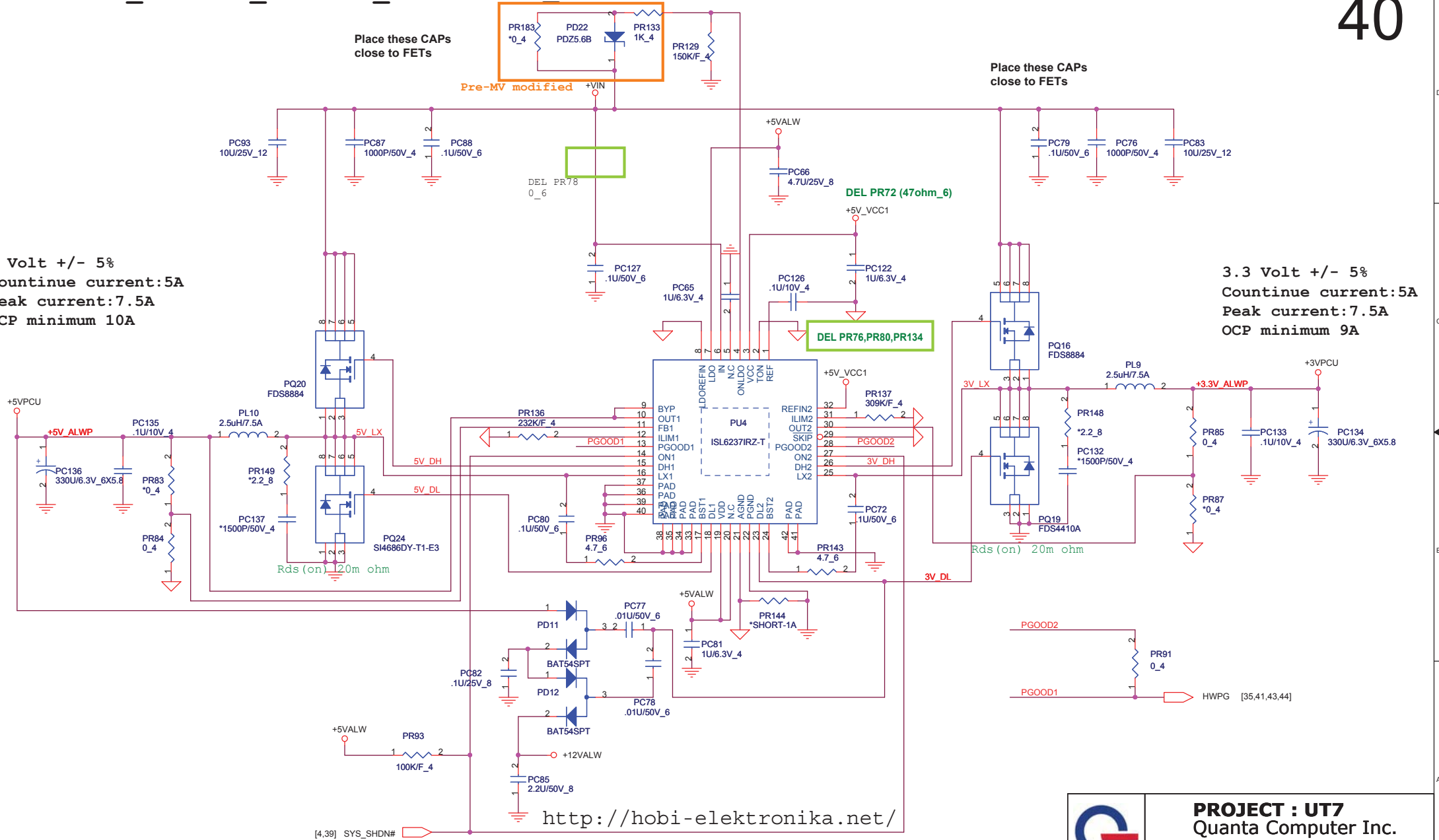
Place these CAPs close to FETs

Place these CAPs close to FETs

Pre-MV modified

5 Volt +/- 5%
Countinue current:5A
Peak current:7.5A
OCP minimum 10A

3.3 Volt +/- 5%
Countinue current:5A
Peak current:7.5A
OCP minimum 9A



<http://hobi-elektronika.net/>

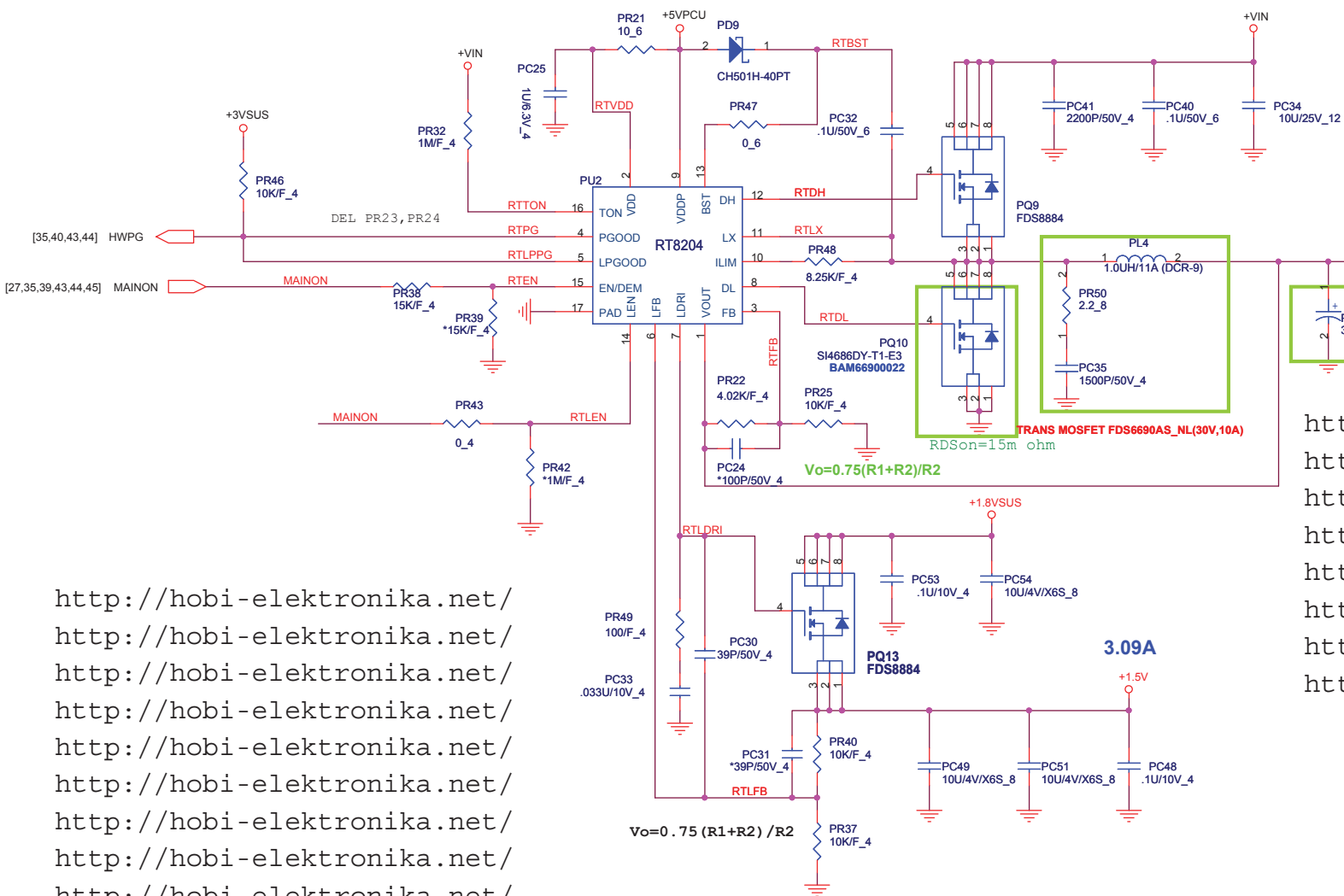
[4,39] SYS_SHDN#



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Quanta Computer Inc.

Size B	Document Number +5V/+3V (ISL6237)	Rev 3A
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VCCP1.05V & +1.5V




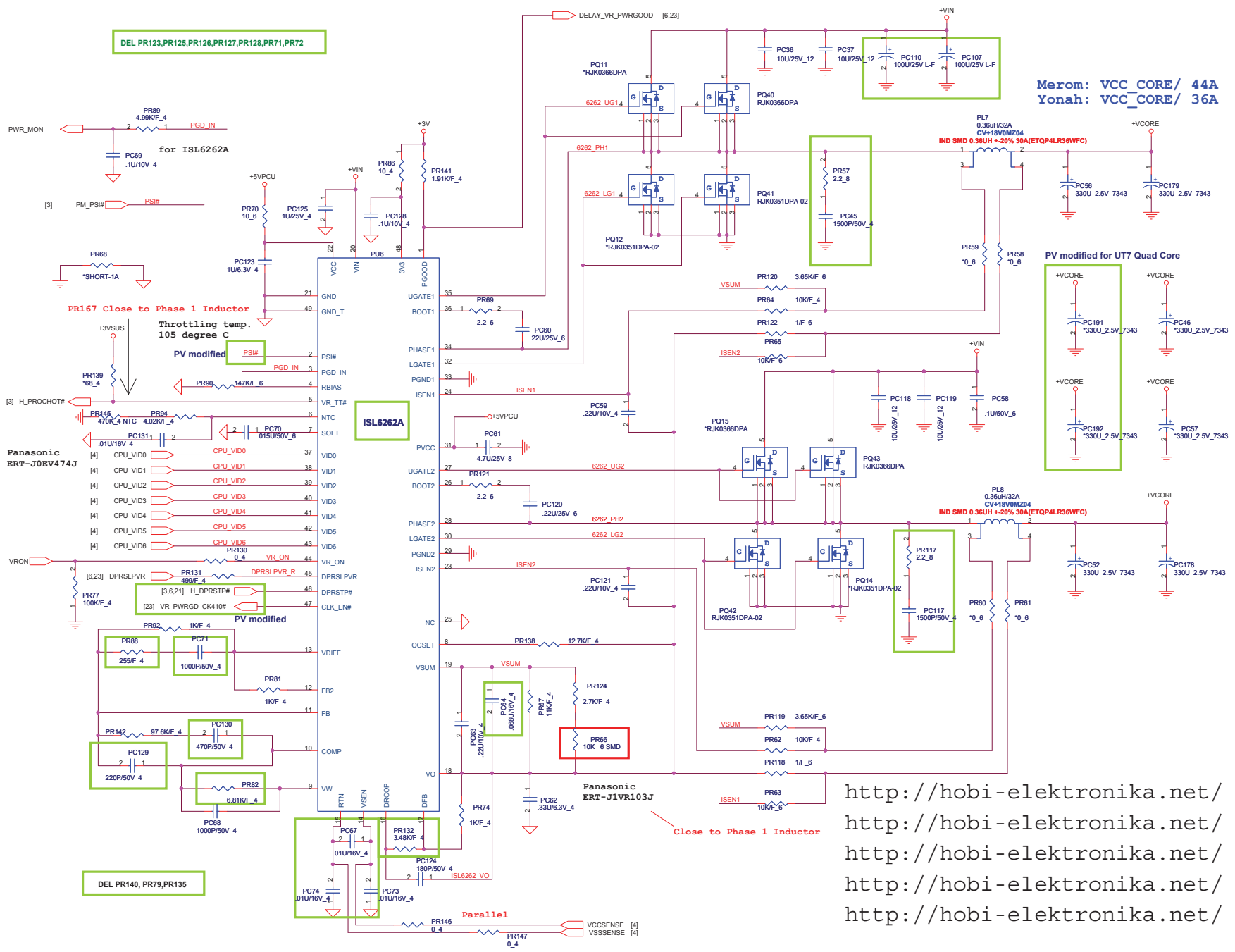
+1.05Volt +/- 5%
 Countinue current:7.5A
 Peak current:10A
 OCP minimum 15A

15A
600 mils

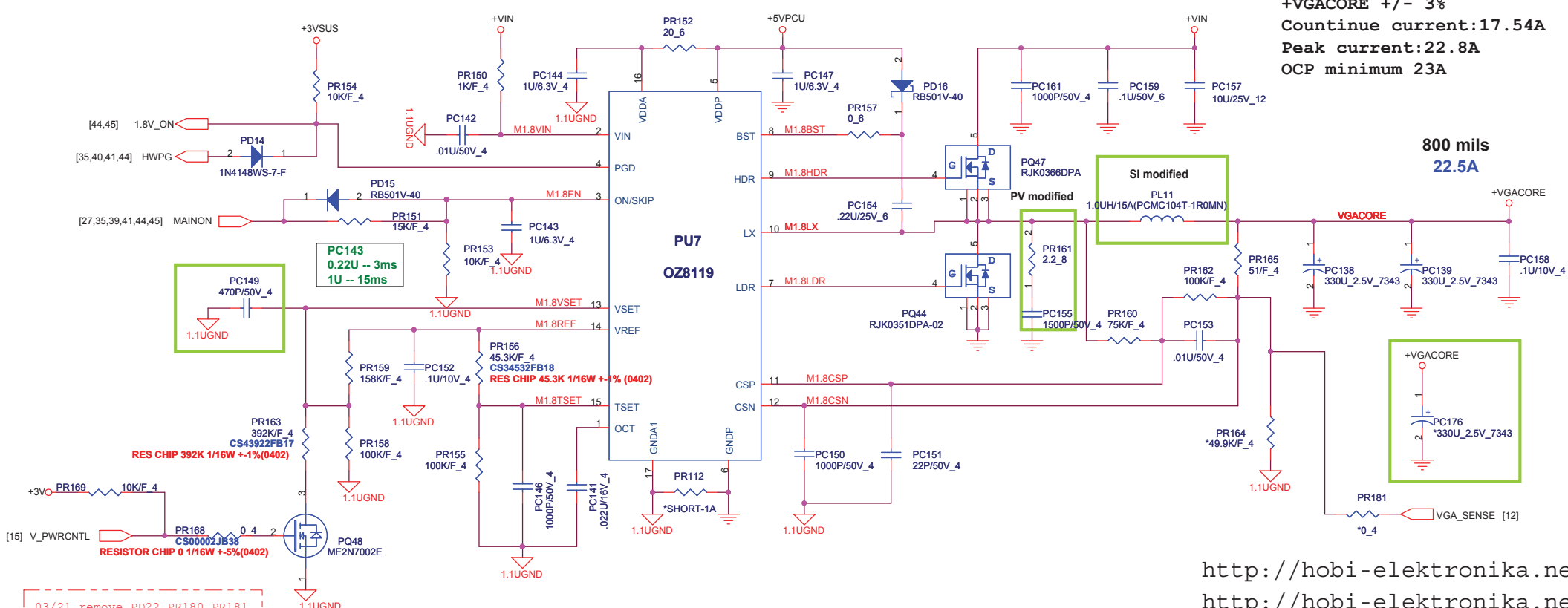
<http://hobi-elektronika.net/>
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		PROJECT : UT7	
		Quanta Computer Inc.	
Size B	Document Number	Rev 3A	
	+1.05V/+1.5V (RT8204)		
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+VGACORE +/- 3%
Continue current: 17.54A
Peak current: 22.8A
OCP minimum 23A

800 mils
22.5A

VREF=2.75V +/-1.5%

NB9P-GS: PR163=392Kohm
Output = 0.9V

NB9M-GE: PR203=590Kohm
 NB9P-GS: PR203=768Kohm

CS45902FB10 RES CHIP 590K 1/16W +/-1%(0402)
 CS47682FB10 RES CHIP 768K 1/16W +/-1%(0402)

03/21 remove PD22, PR180, PR181

V_PWRCNTL	NB9P-GS
GPIO5	1.05V
Low	1.05V
High	0.9V

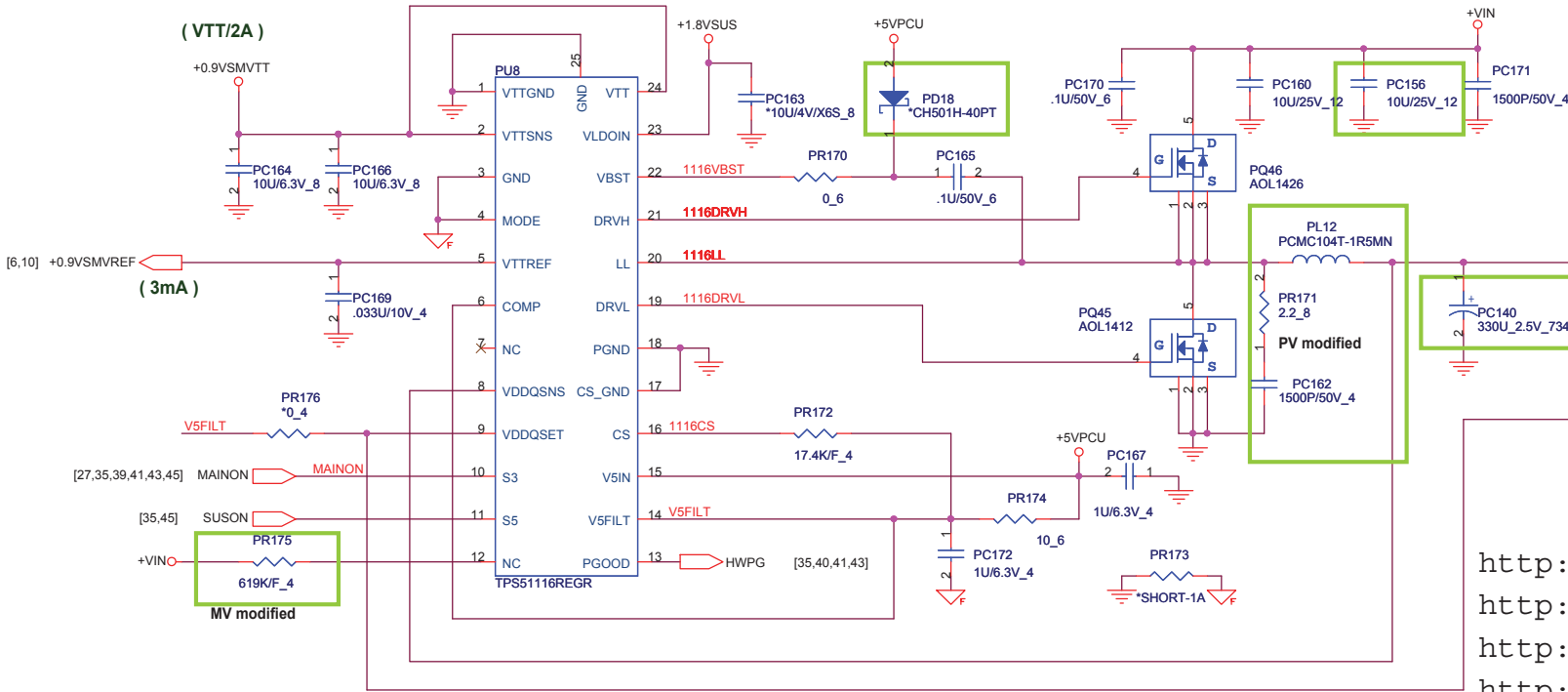
VGA_GPIO6	V_PWRCNTL		NB9P-GS	NB9M-GE
GPIO6	GPIO5			
Low	Low	MAX BAT	0.9V	0.9V
Low	High	SD DVD	0.9V	0.9V
High	Low	HD DVD	0.9V	0.9V
High	High	MAX PERF	1.05V	1.09V

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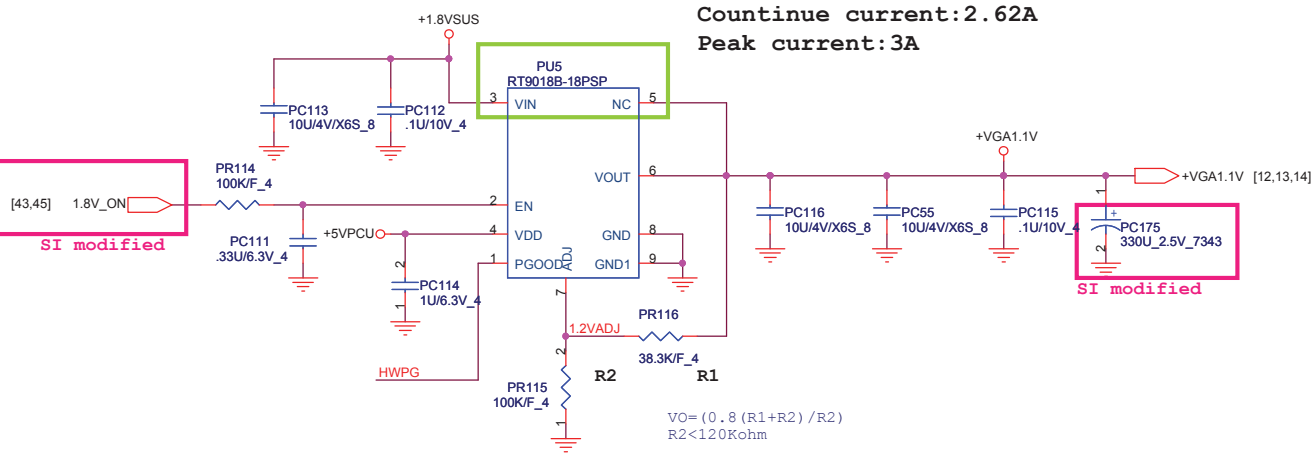
Size B	Document Number VGA CORE OZ8118	Rev 3A
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1.8 Volt +/- 5%
Countinue current:6A
Peak current:14A
OCp minimum 17A

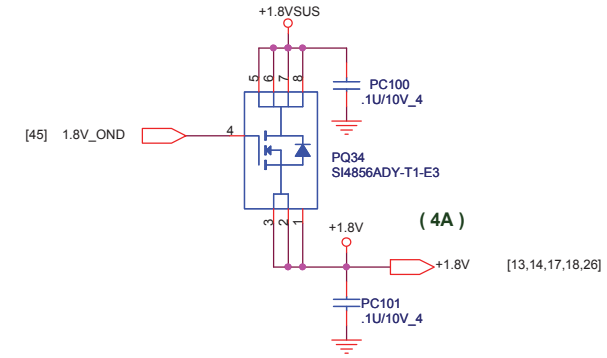
<http://hobi-elektronika.net/>
<http://hobi-elektronika.net/>
<http://hobi-elektronika.net/>
<http://hobi-elektronika.net/>
<http://hobi-elektronika.net/>

1.1 Volt +/- 5%
Countinue current:2.62A
Peak current:3A



$$VO = (0.8 (R1+R2) / R2)$$

$$R2 < 120Kohm$$

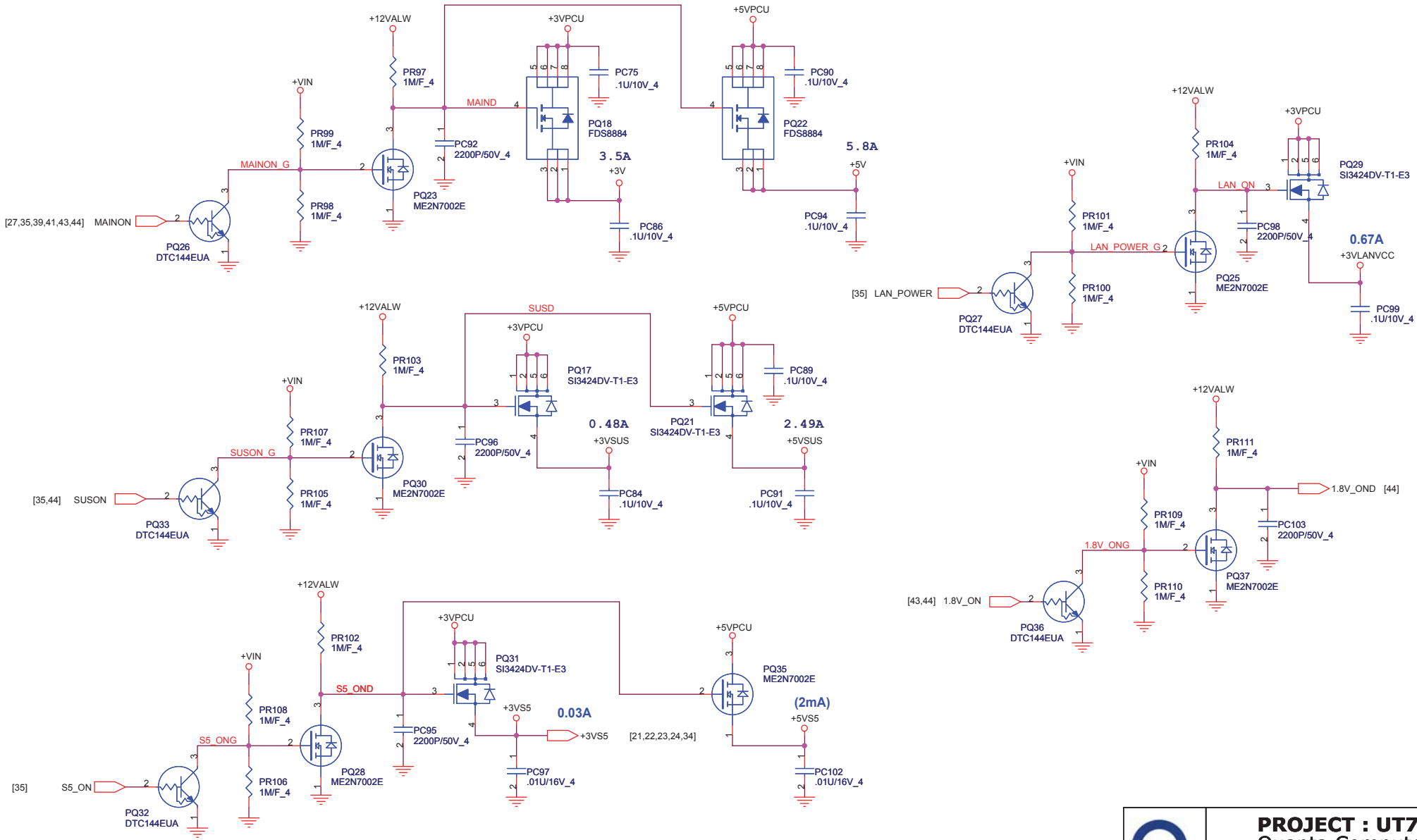


(4A)
 [13,14,17,18,26]



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Size B	Document Number 1.8V/DDR_VTER/+1.8v/+1.1V	Rev 3A
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Size B	Document Number DISCHARGE/3VS5/5VS5/LAN	Rev 3A
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	Voltage level	AC MODE				DC MODE			
		S0	S3	S4	S5	S0	S3	S4	S5
+3VPCU	3.3V +/- 5%	V	V	V	V	V	V	V	V
+5VPCU	5V +/- 5%	V	V	V	V	V	V	V	V
+3VRTC	3.3V +/- 5%	V	V	V	V	V	V	V	V
+3VS5	3.3V +/- 5%	V	V	V	V	V	V		
+5VS5	5V +/- 5%	V	V	V	V	V	V		
+3VSUS	3.3V +/- 5%	V	V			V	V		
+5VSUS	5V +/- 5%	V	V			V	V		
+1.8VSUS	1.8V +/- 5%	V	V			V	V		
+0.9VSMVTT	0.9V +/- 5%	V	V			V	V		
+1.5V	1.5V +/- 5%	V				V			
+1.05V	1.05V +/- 5%	V				V			
+VCORE	0.9~1.15V	V				V			
+VGA_CORE	0.9~1.2V	V				V			
+VGA1.1V	1.1V +/- 5%	V				V			
+1.8V	1.8V +/- 5%	V				V			
+3VLAVCC	3.3V +/- 5%	V				V			

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	Size Custom Date: Friday, July 18, 2008	Document Number Voltage Sheet 46 of 46