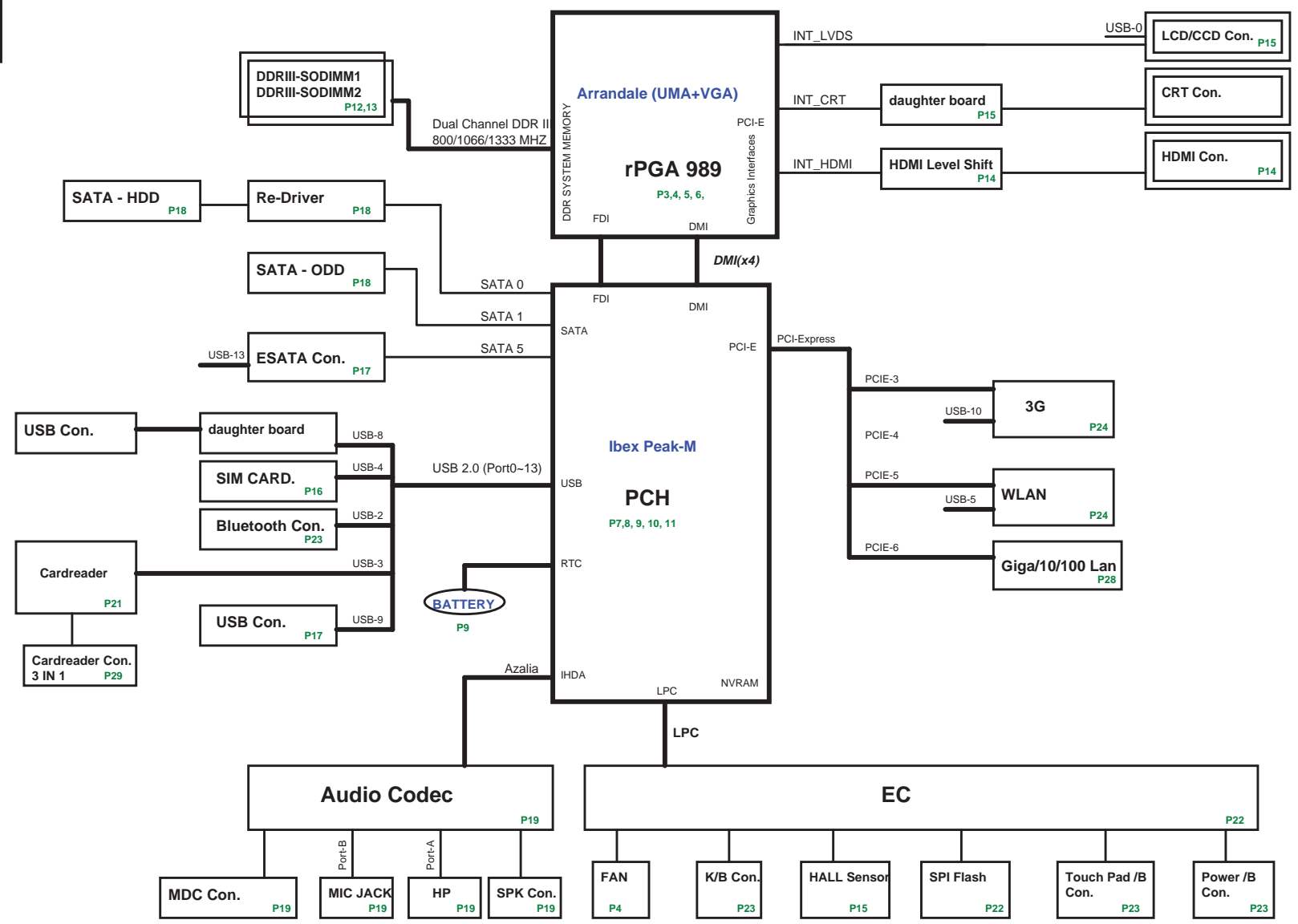


PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

TE2 Block Diagram

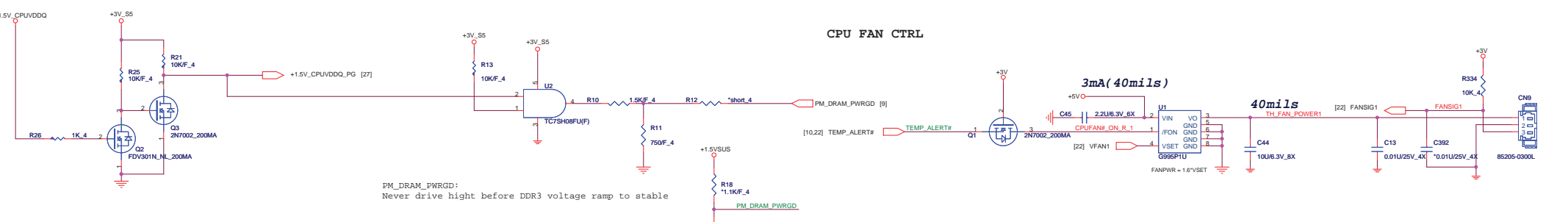
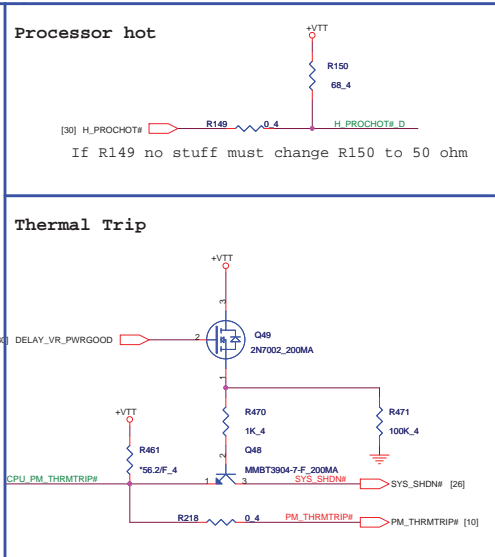
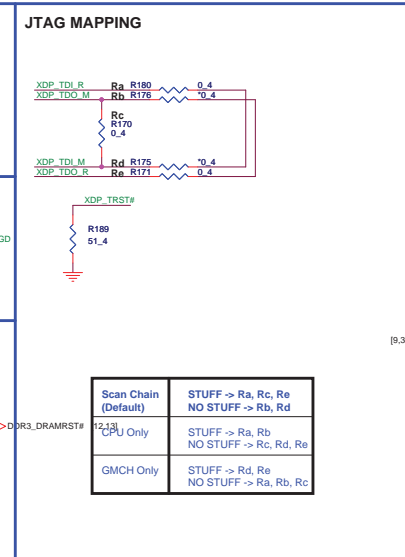
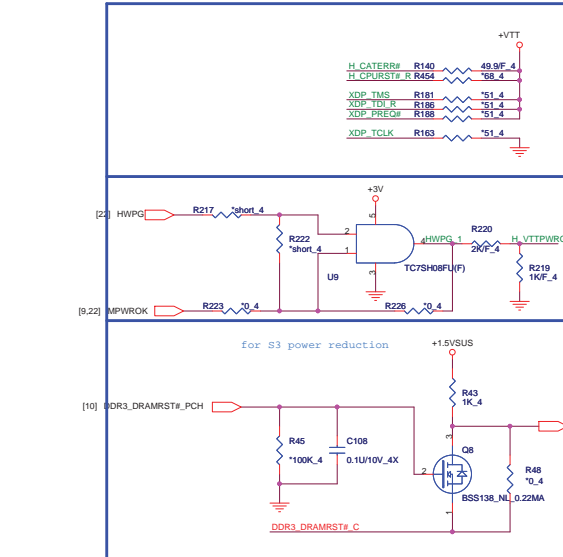
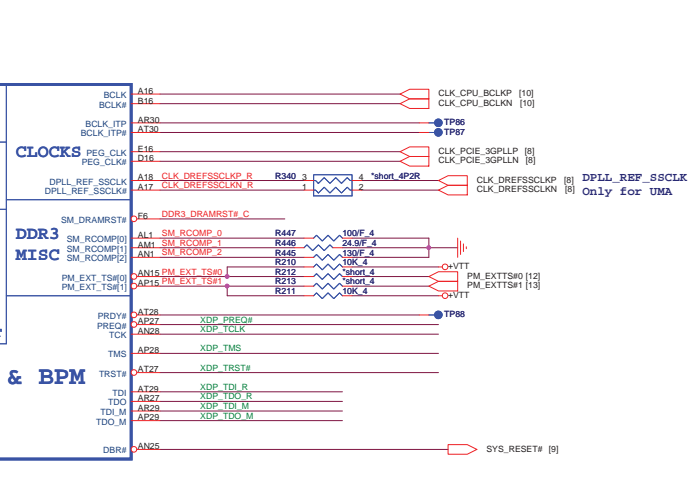
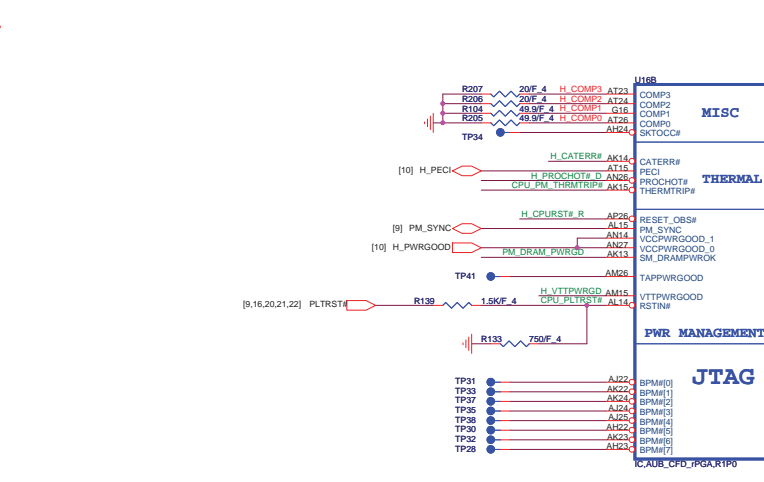
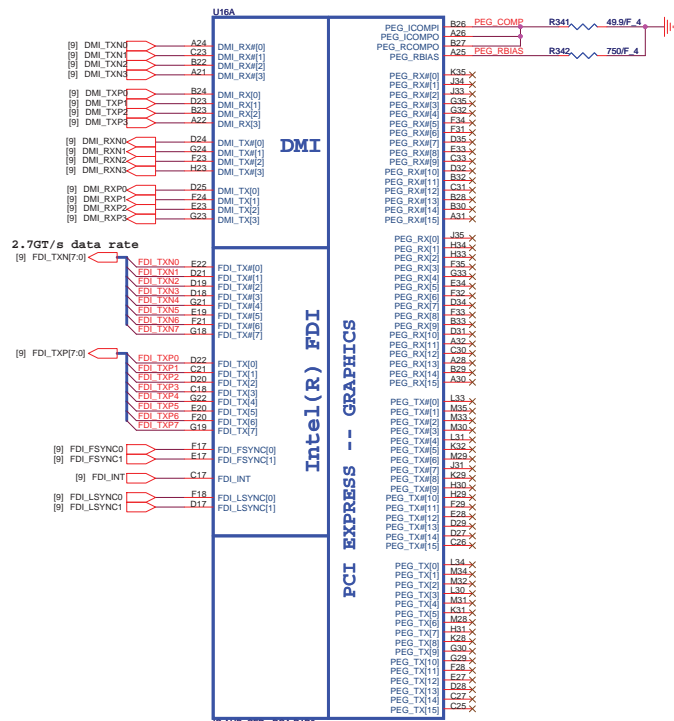


CK505
P2

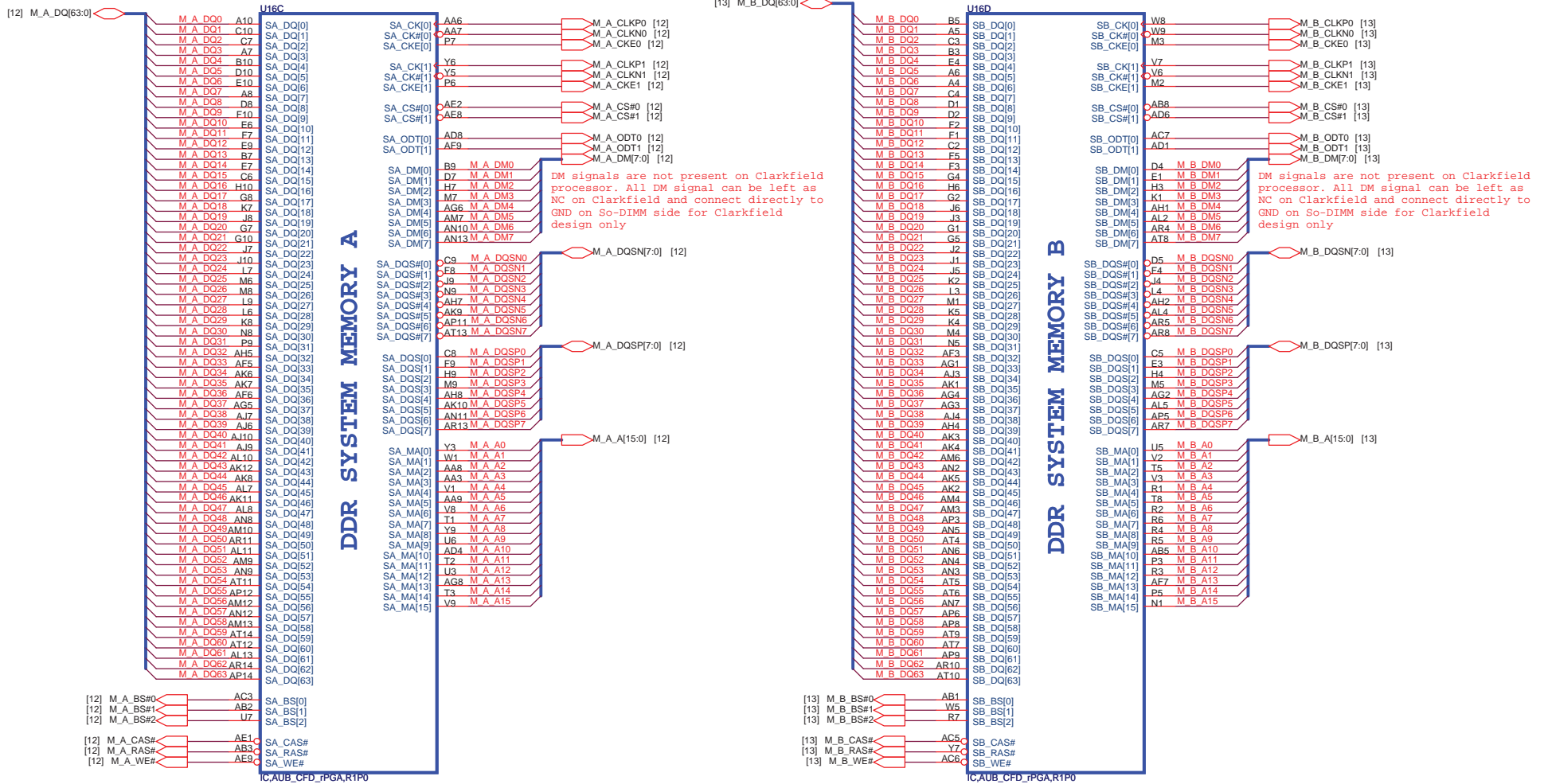
POWER SYSTEM

- ISL88731A P25
- RT8210B P26
- UP6163 P27
- UP6111A P28
- RT015A P29
- ISL62882C P30
- RT8152C P32

- +VCC_CORE
- +1.5V
+1.5VSUS
- +VTT
+1.05V
- +1.8V
- +1.5V_S5
+3VPCU
+3V_S5
+3V
+5VPCU
+5V_S5
+5V
+SMDDR_VTERM
+SMDDR_VREF

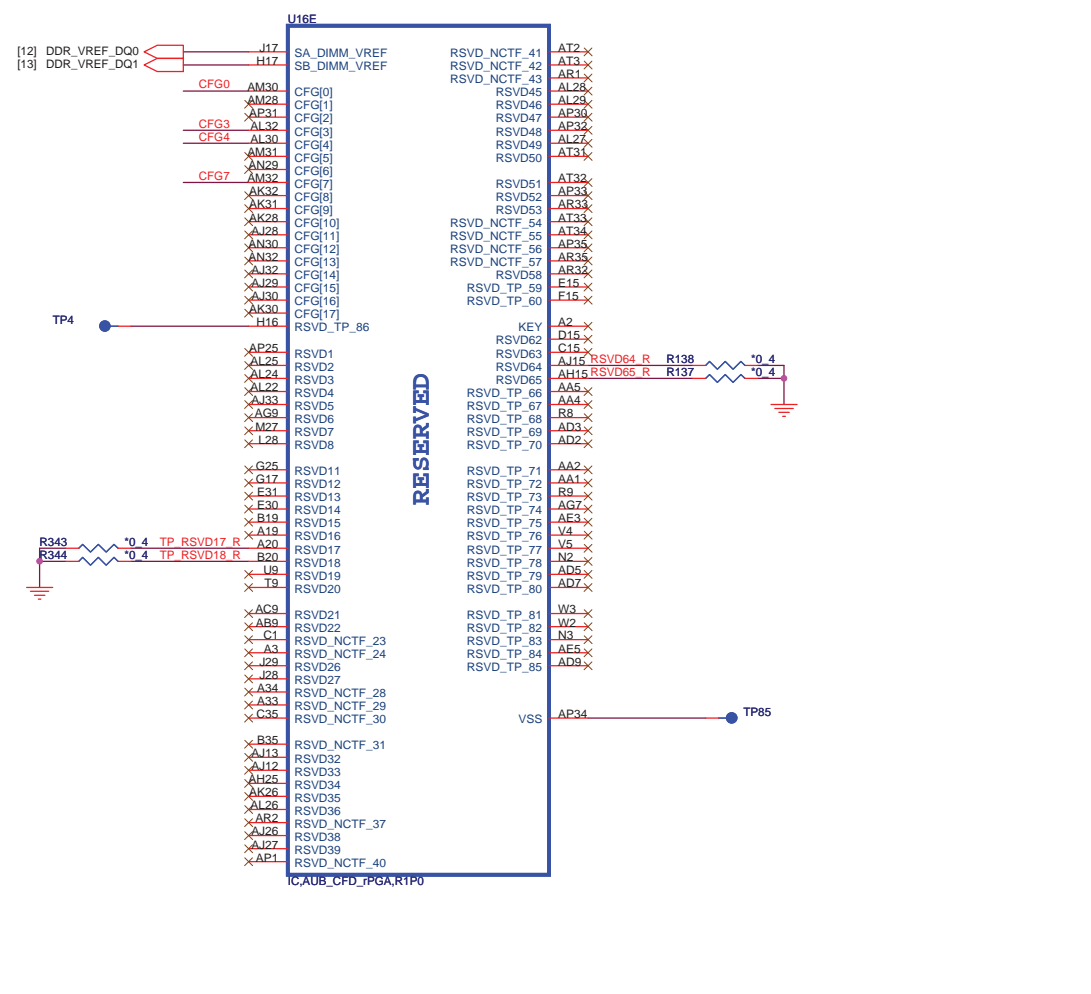
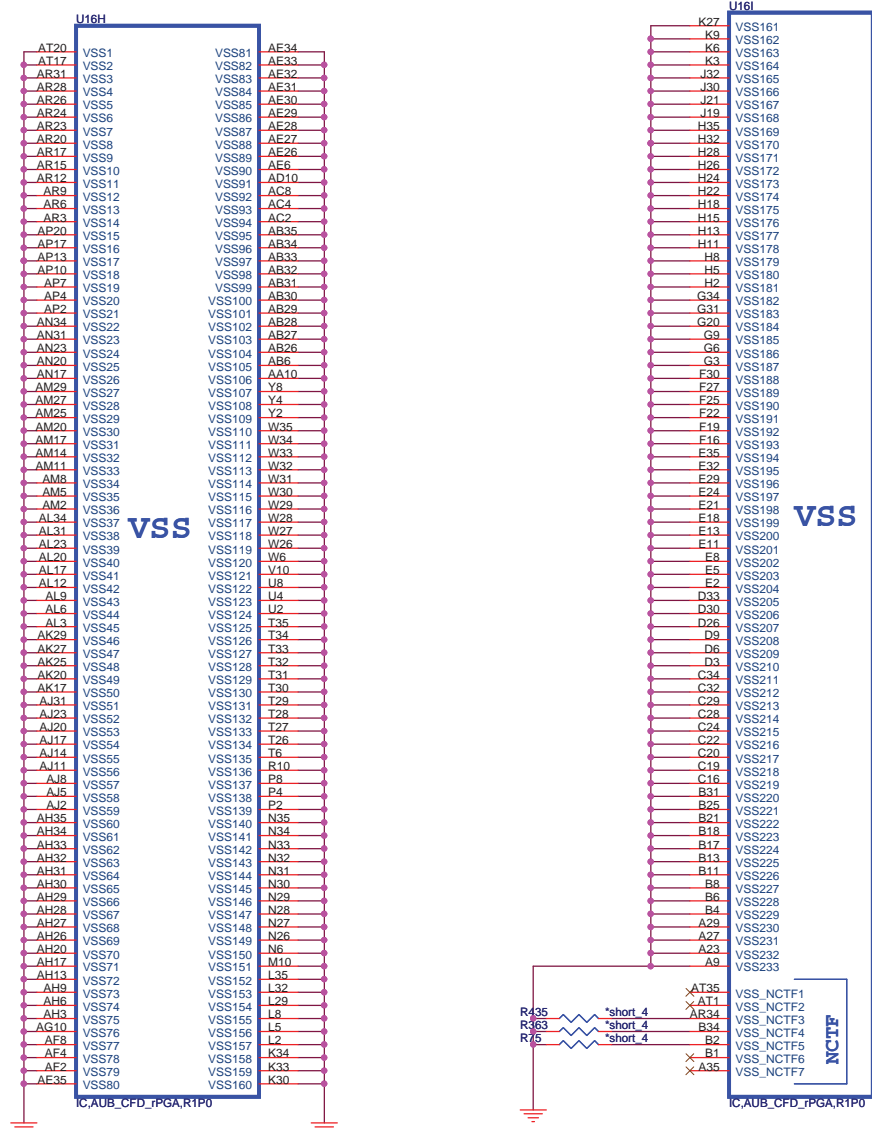


AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



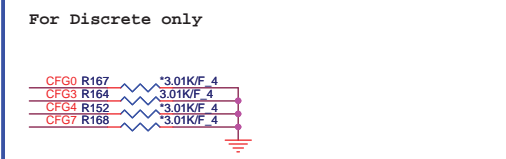
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0, 14 -> 1



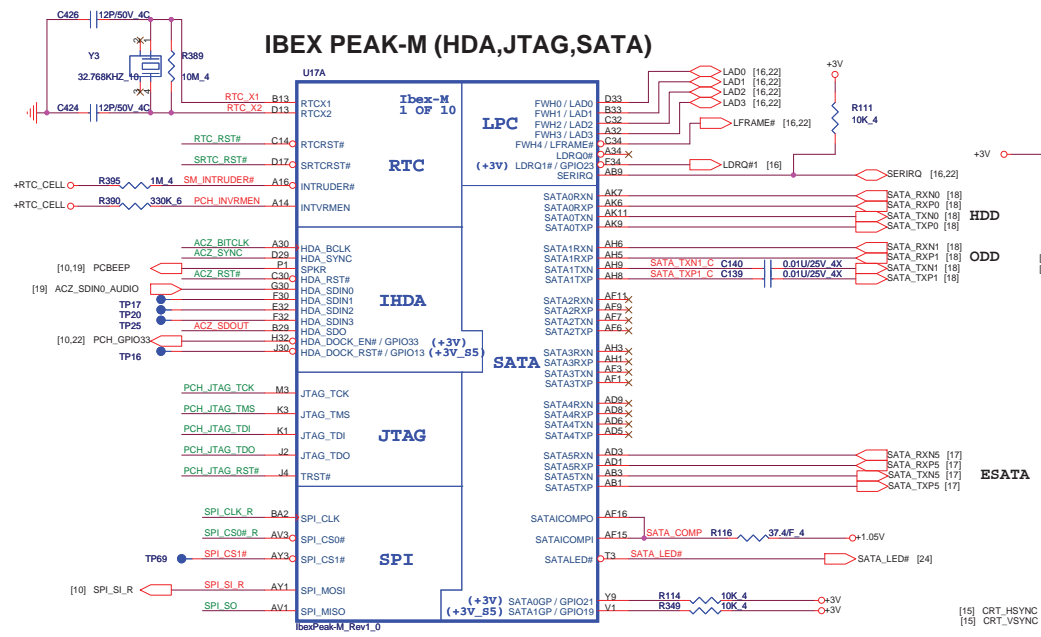
CFG[1:0] - PCI_Epress Configuration Select
 * 11= 1 x 16 PEG
 * 10= 2 x 8 PEG

Quanta Computer Inc.
PROJECT : TE2

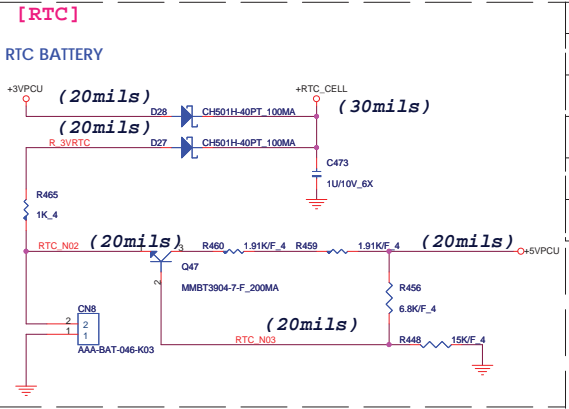
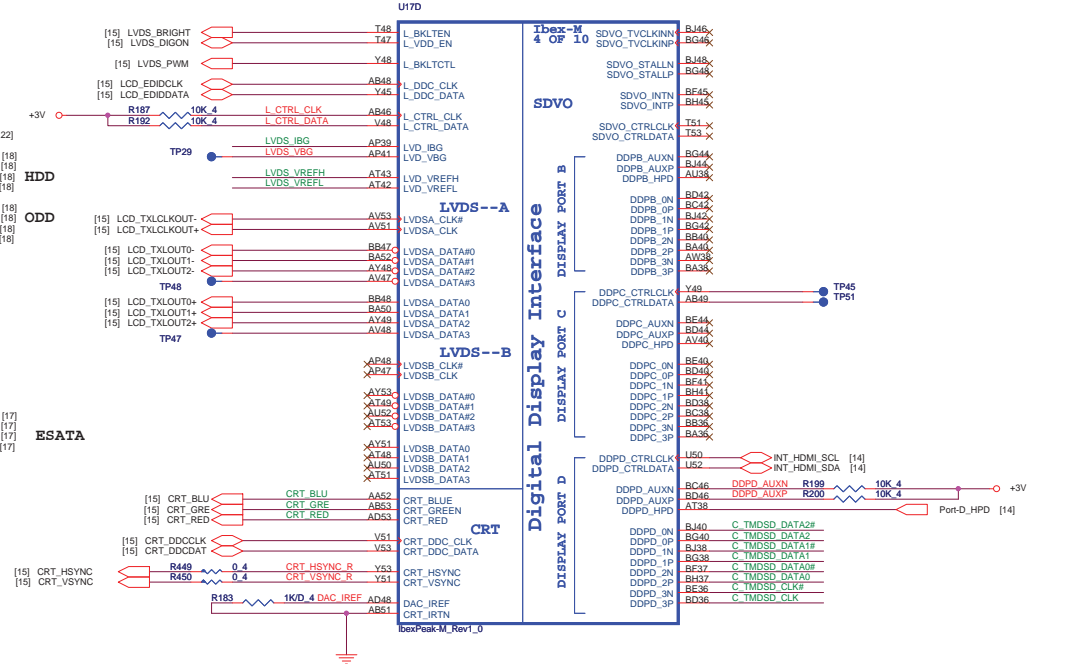
Size Document Number **PROCESSOR 4/4 (GND)** Rev 2A

Date: Tuesday, March 09, 2010 Sheet 6 of 35

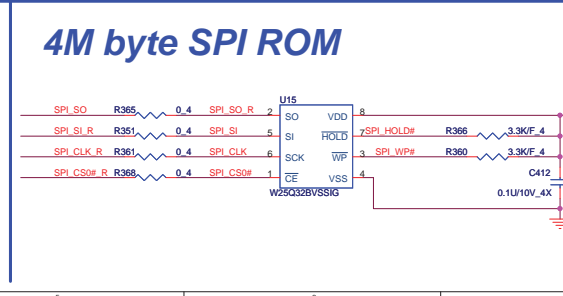
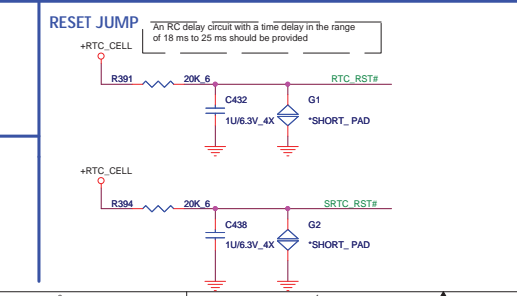
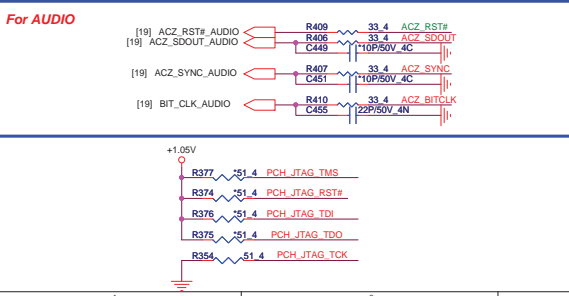
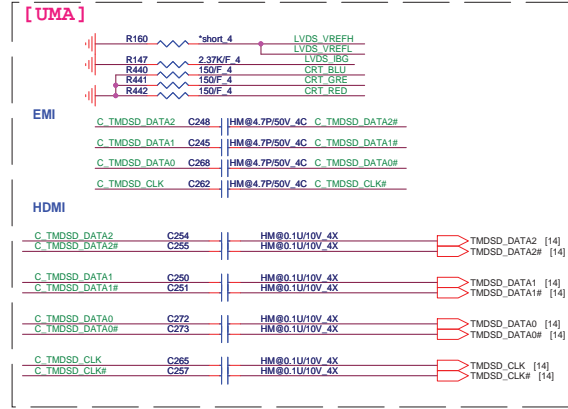
IBEX PEAK-M (HDA,JTAG,SATA)



IBEX PEAK-M (LVDS,DDI)



Port	Strap	How to enable Port?	How to disable Port?
Port A	LVDS	L_DDC_DATA	PU to 3.3V with 2.2k+/- 5%
Port B	SDVO	SDVO_CTRLDATA	PU to 3.3V with 2.2k+/- 5%
Port C	DDPC	DDPC_CTRLDATA	PU to 3.3V with 2.2k+/- 5%
Port D	DDPD	DDPD_CTRLDATA	PU to 3.3V with 2.2k+/- 5%
eDP	CFG[4]	PD to GND directly	NC

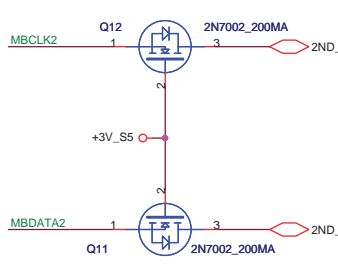
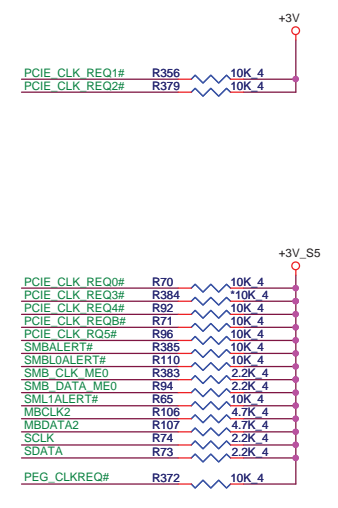
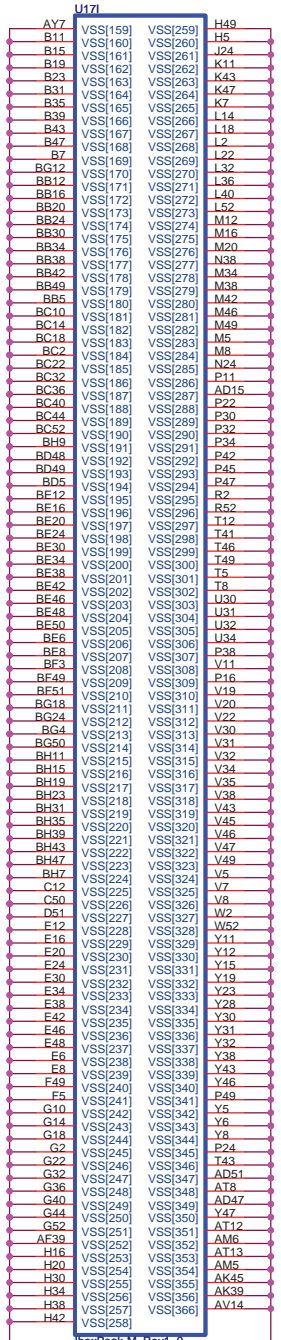


PCH	2MB	4MB	8MB
PM55	●		
HM55		●	
HM57/PM57		●	●
QM57/QS57			●

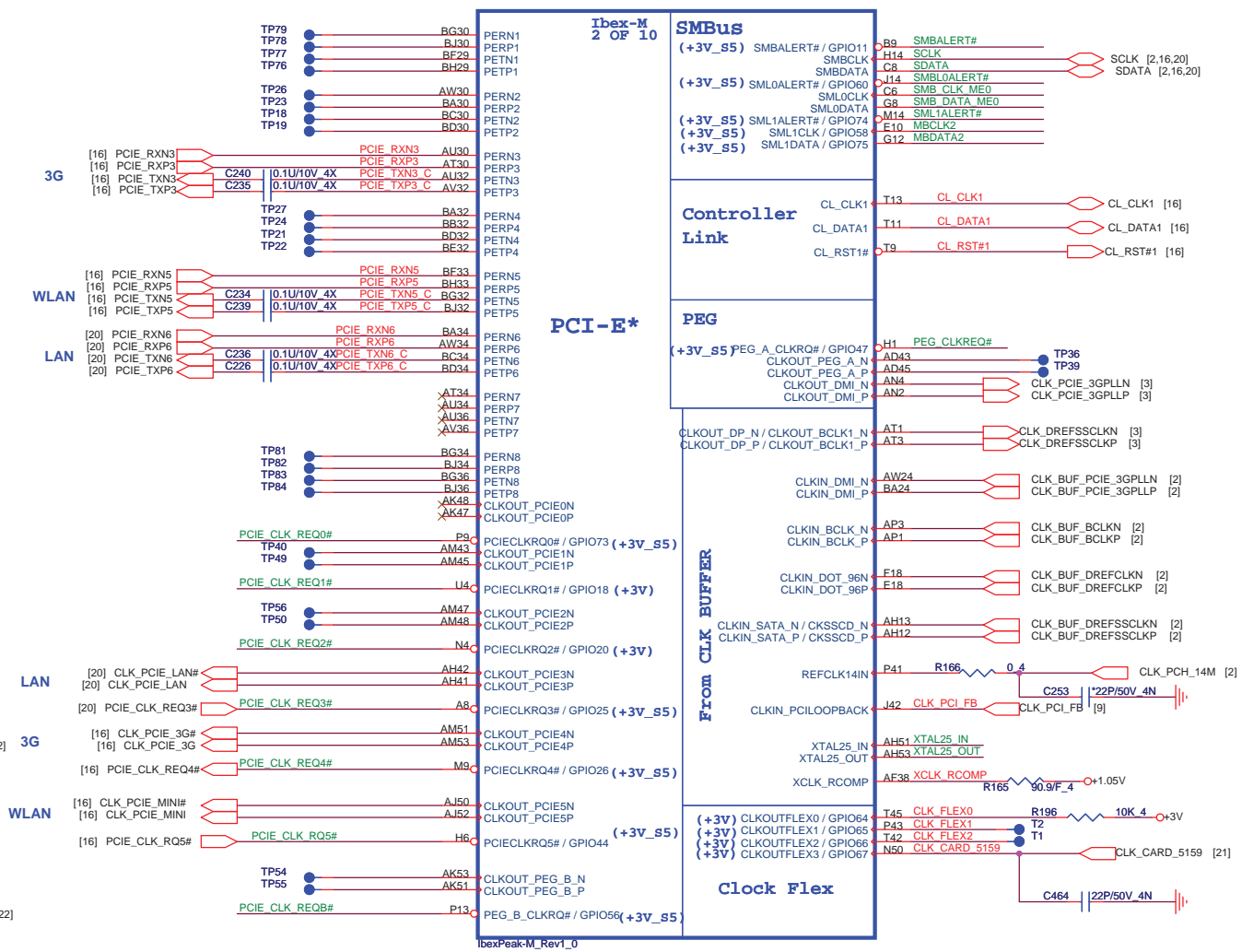
Quanta Computer Inc.
PROJECT : TE2

Size: Document Number: PCH 1/5 (SATA,HDA,LPC) Rev: 2A
Date: Wednesday, March 10, 2010 Sheet: 7 of 35

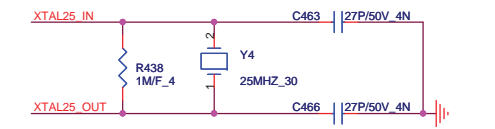
IBEX PEAK-M (GND)



IBEX PEAK-M (PCI-E, SMBUS, CLK)



Placement close

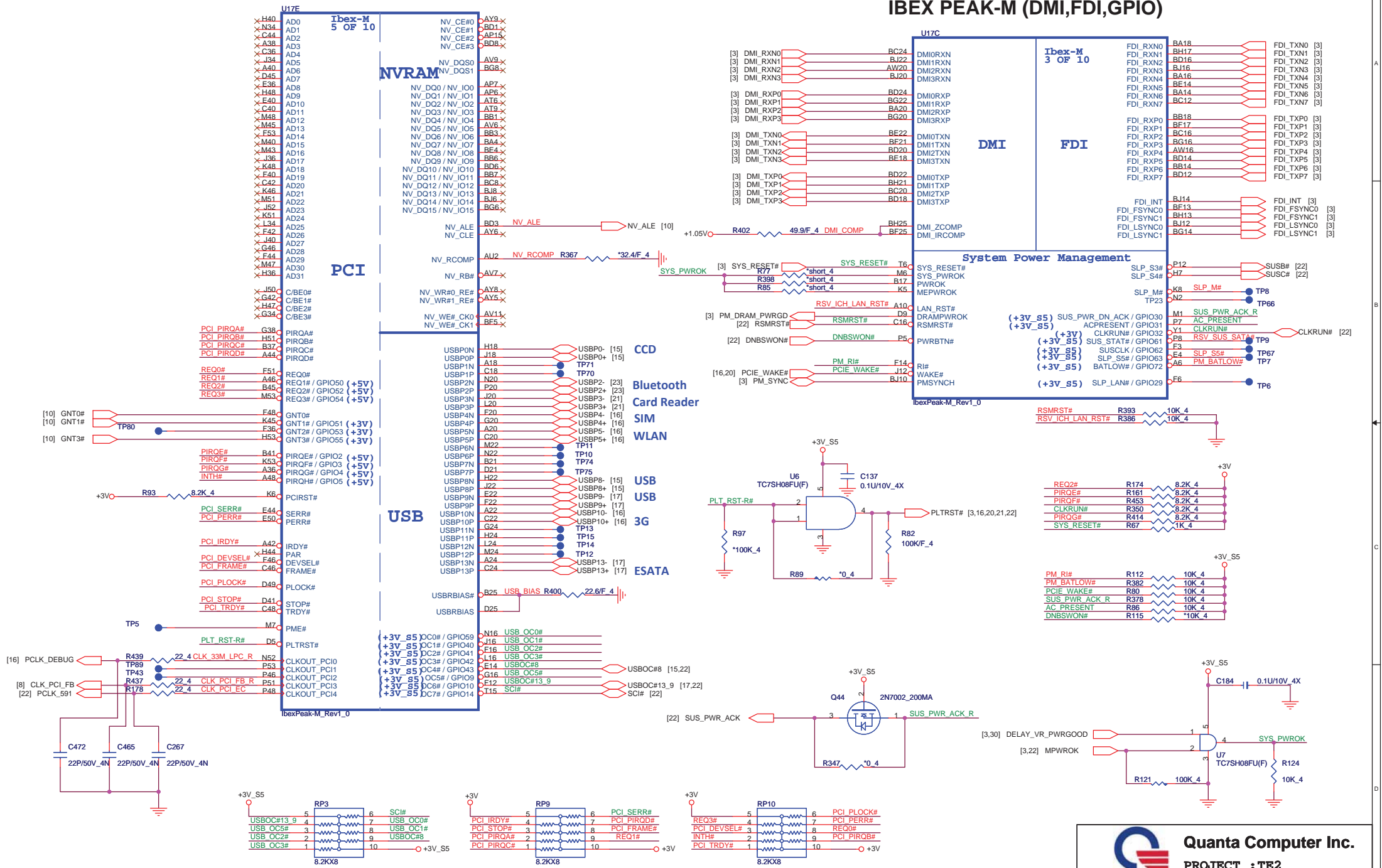


Quanta Computer Inc.
PROJECT : TE2

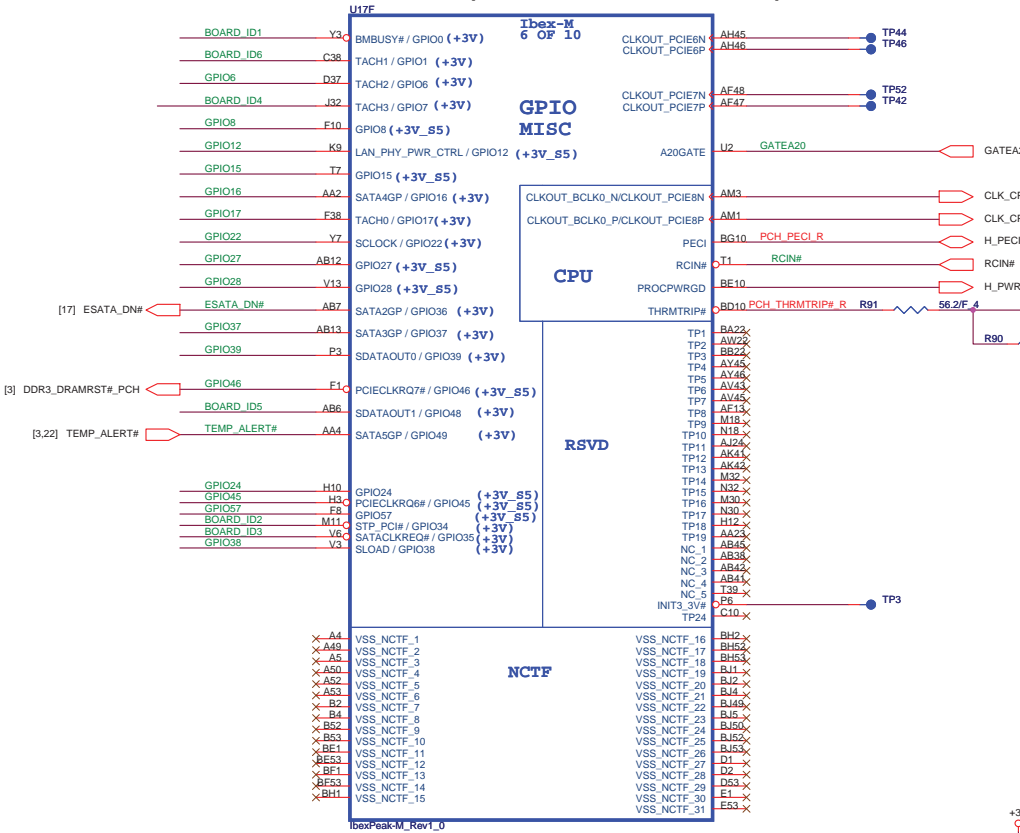
Size	Document Number	Rev
	PCH 2/5 (PCI-E, SMBUS, CK)	2A
Date:	Wednesday, March 10, 2010	Sheet 8 of 35

IBEX PEAK-M (PCI,USB,NVRAM)

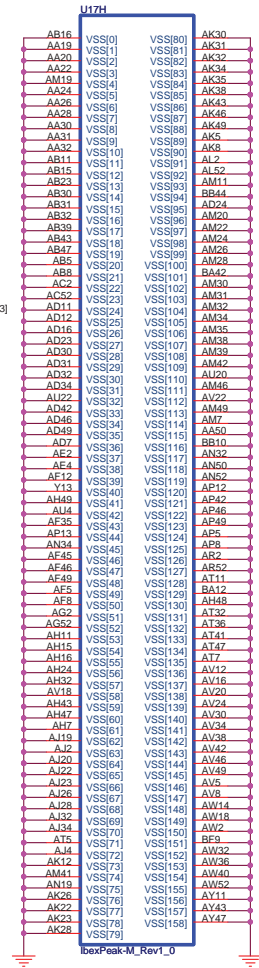
IBEX PEAK-M (DMI,FDI,GPIO)



IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



IBEX PEAK-M (GND)



PCH Strap Pin Configuration Table

SPKR

[7,19] PCBEEP *1K/F 4

0 = Default Mode (Internal weak Pull-down)
1 = No Reboot Mode with TCO Disabled

GNT3#/GPIO55

[9] GNT3# *10K/F 4

0 = Default Mode (Internal weak Pull-down)
1 = No Reboot Mode with TCO Disabled

HDA_DOCK_EN #GPIO33

[7,22] PCH_GPIO33 10K 4

0 = Top Block Swap Mode
1 = Default Mode (Internal pull-up)

GNT0#, GNT1#

[9] GNT0# *1K/F 4

[9] GNT1# *1K/F 4

Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

SPI_MOSI

[7] SPL_SLR *1K 4

NV_ALE

[9] NV_ALE *10K 4

1 = Enabled
0 = Disabled (Default)

GPIO8

GPIO8 *10K 4

This signal has a weak internal pull up.
NOTE: This signal should not be pulled low

GPIO15

GPIO15 1K 4

0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

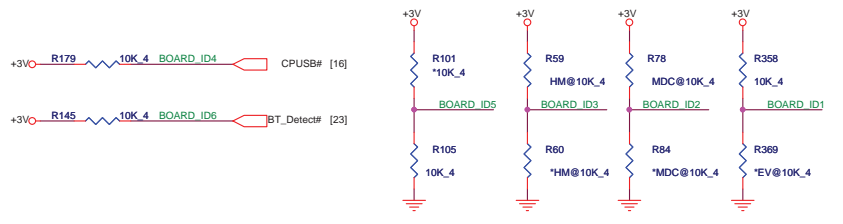
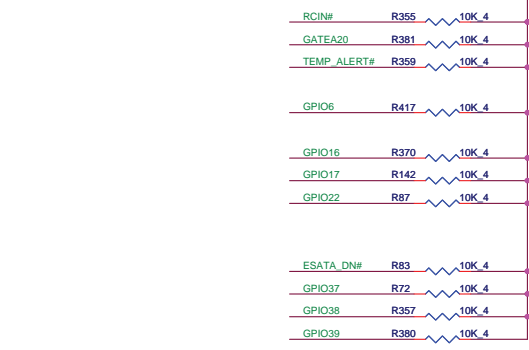
GPIO27

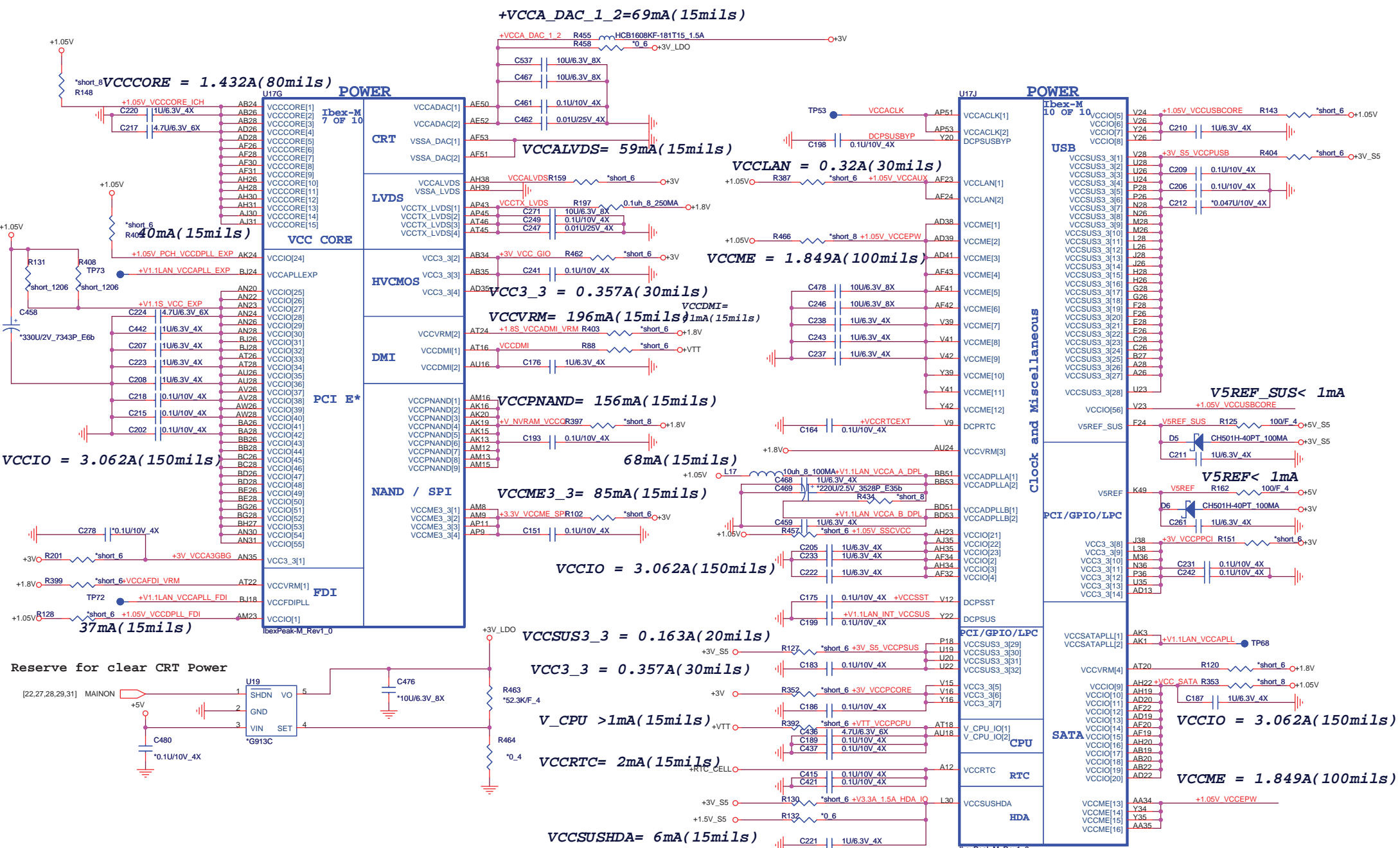
GPIO27 *10K 4

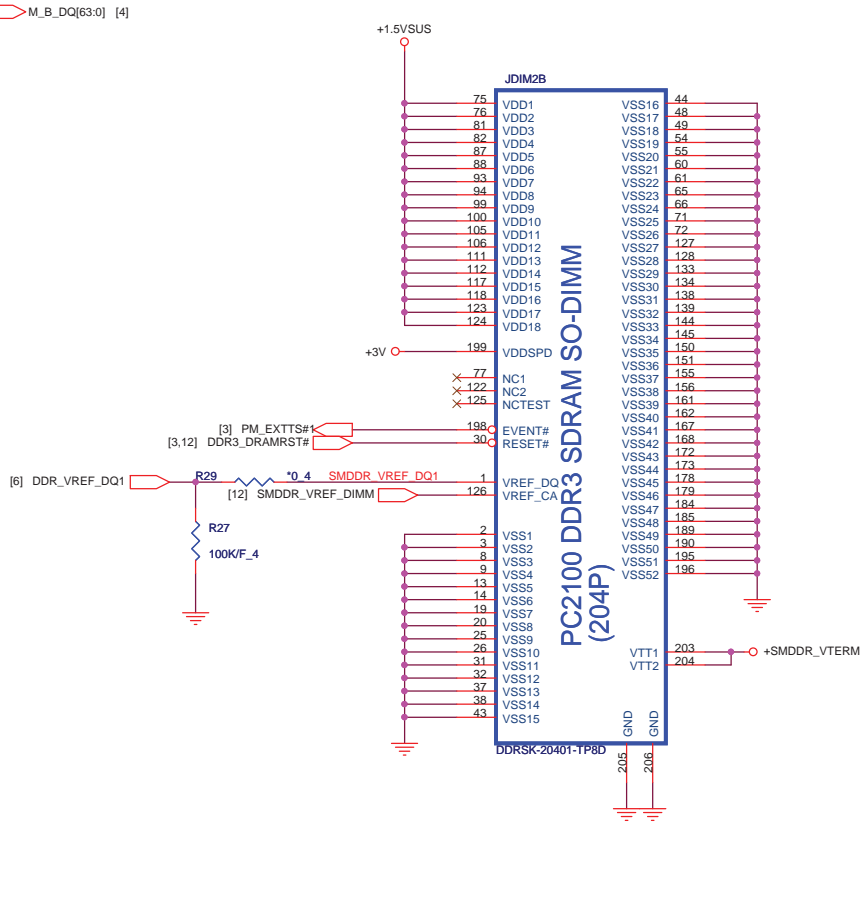
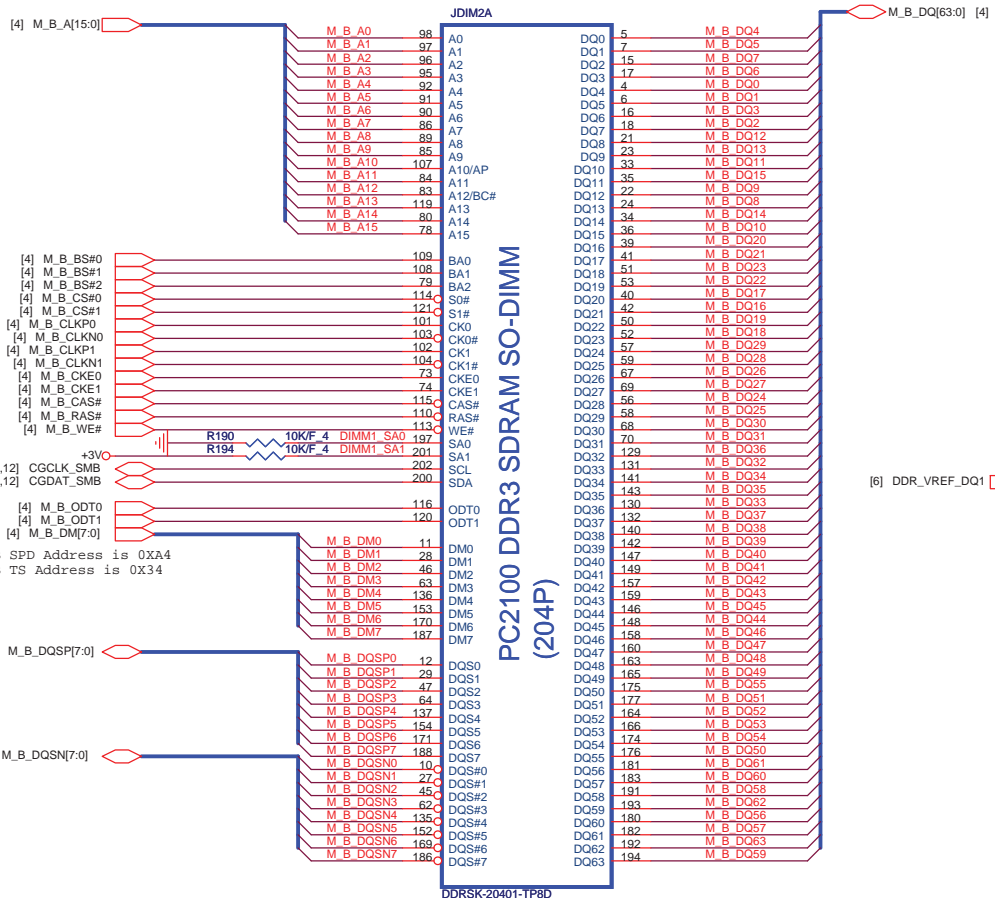
0 = Disables the VccVRM. Need to use on-board filter circuits for analog rails.
1 = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit.
This signal has a weak internal pull-up.

BOARD ID SETTING

Board ID	ID1	ID2	ID3	ID4	ID5	ID6
UMA SKU	H					
VGA SKU	L					
W/ MDC		H				
W/O MDC		L				
W/ HDMI			H			
W/O HDMI			L			
W/O 3G				H		
W/ 3G				L		
15"					H	
14"					L	
W/O BT						H
W/ BT						L

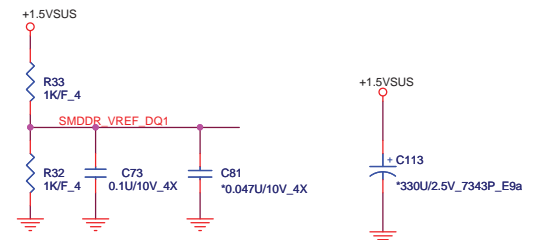
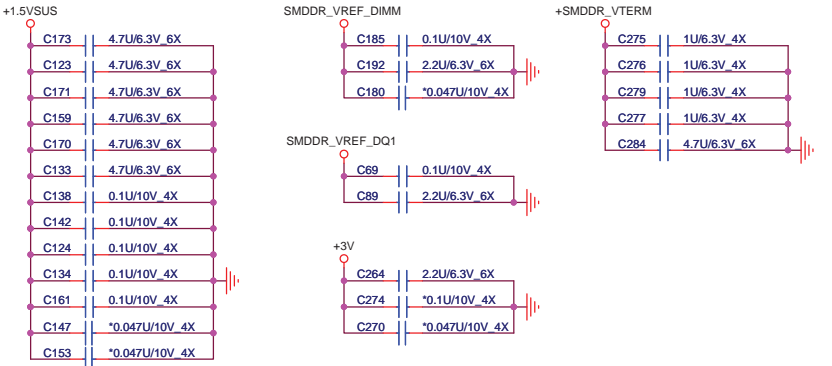






SO-DIMM SPD Address is 0XA4
SO-DIMM TS Address is 0X34

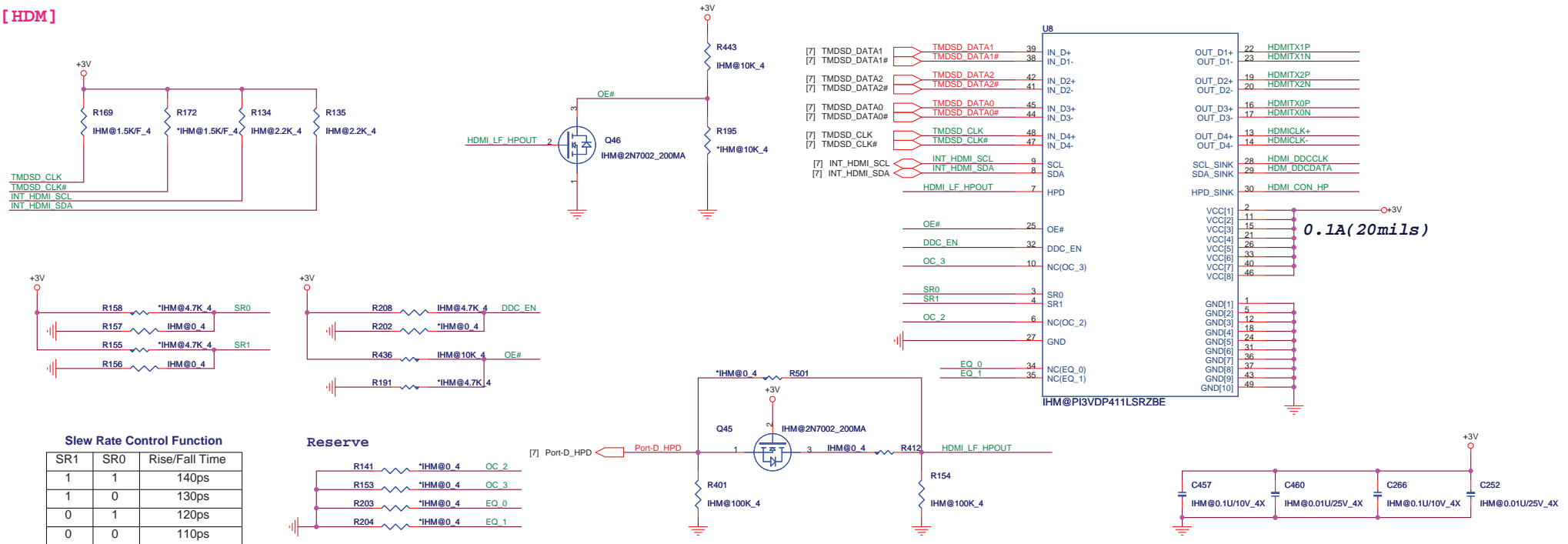
Place these Caps near So-Dimm1.
Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%



HDMI Conn

HDMI Level Shift UMA only

[HDM]

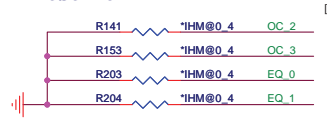


0.1A (20mils)

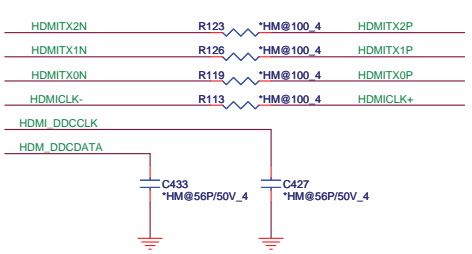
Slew Rate Control Function

SR1	SR0	Rise/Fall Time
1	1	140ps
1	0	130ps
0	1	120ps
0	0	110ps

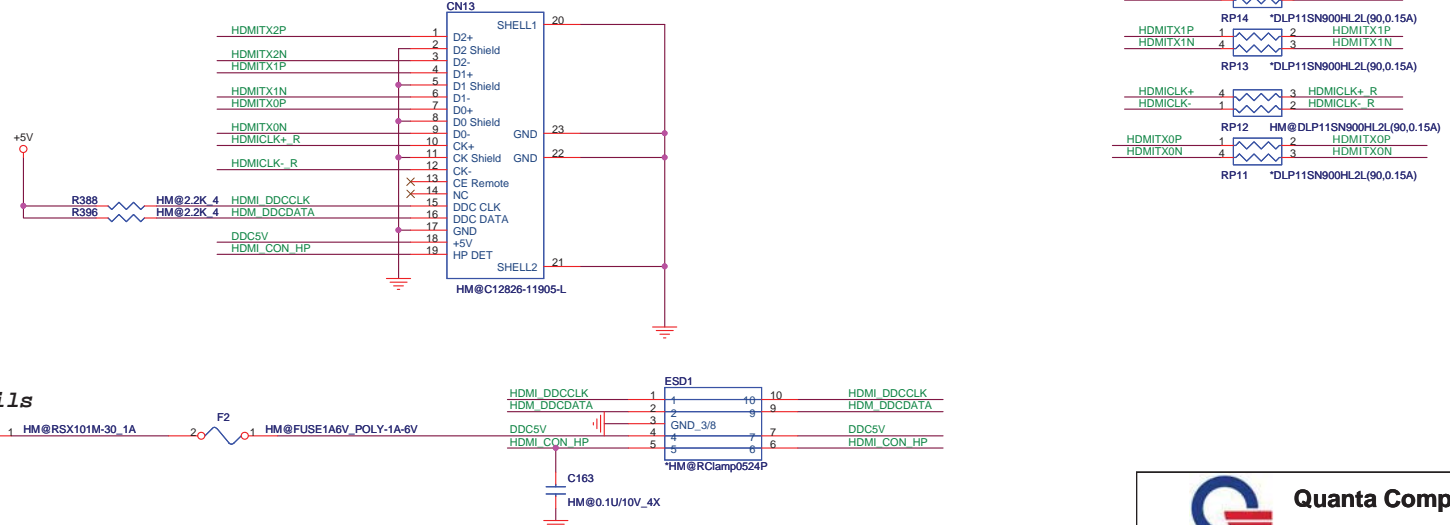
Reserve




For EMI close to connector



Close to HDMI CONN

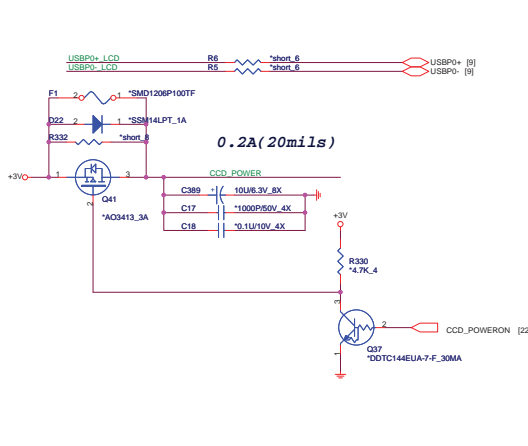




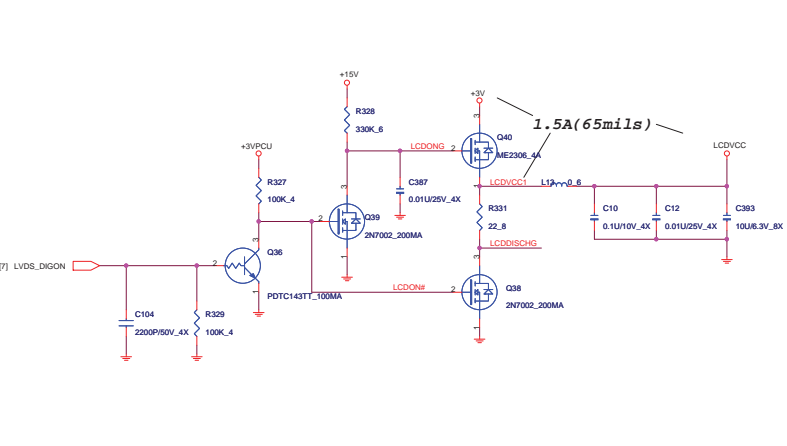
Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
HDMI CONN	HDMI CONN	2A
Date:	Wednesday, March 10, 2010	Sheet 14 of 35

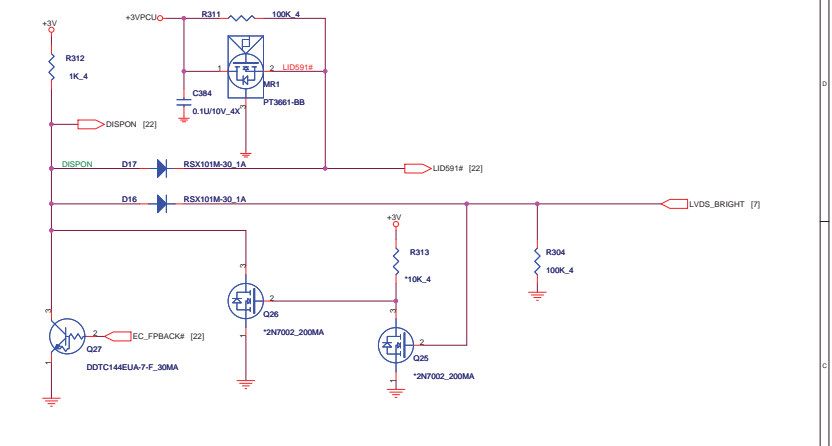
CCD [CCD]



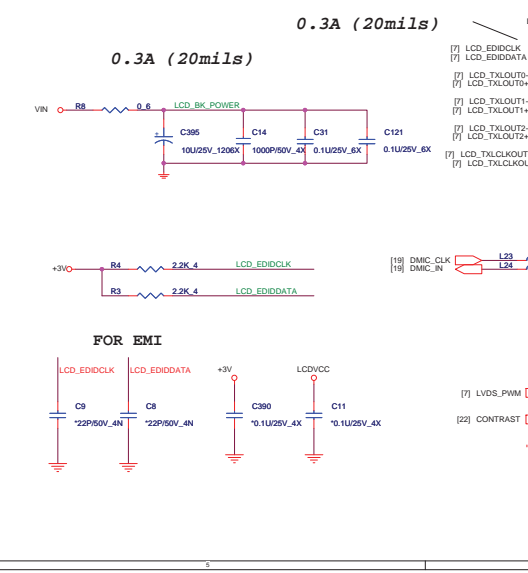
LCD POWER SWITCH [LDS]



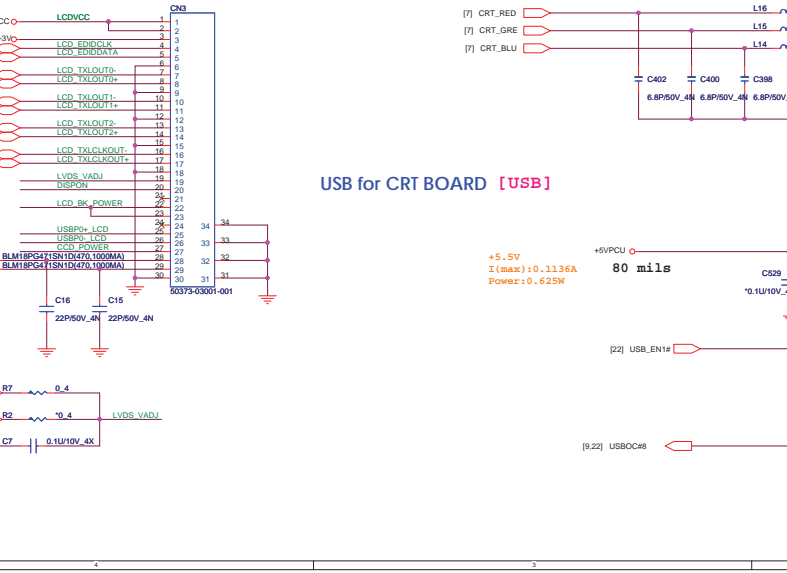
HALL SENSOR&BACK LIGHT SWITCH [HSR]



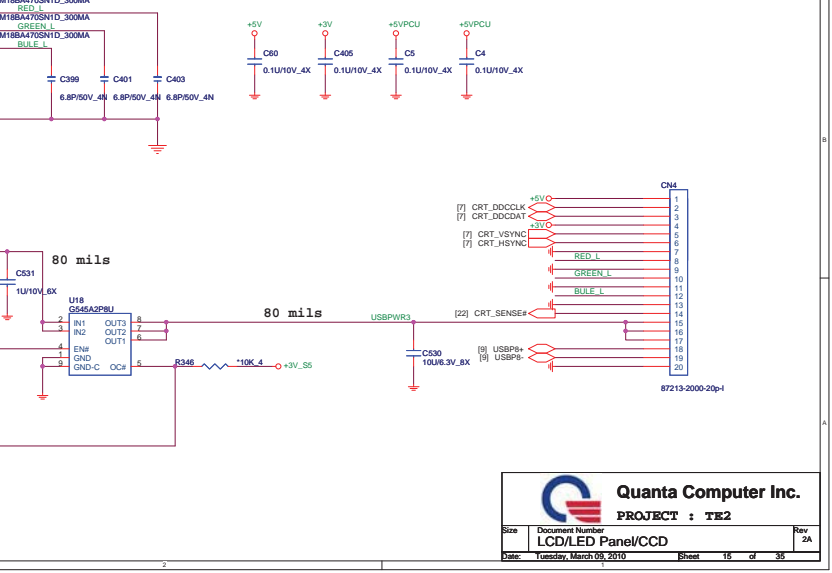
LCD Panel Module [LDS]



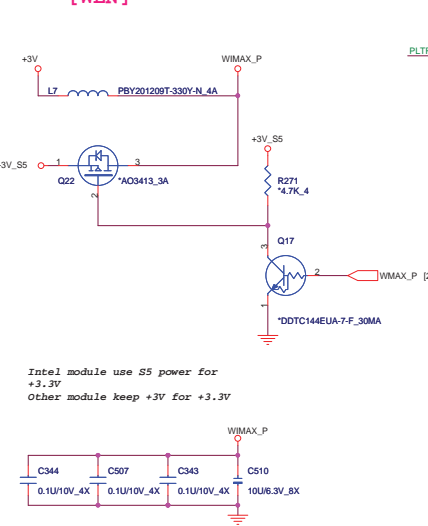
CRT [CRT]



USB for CRT BOARD [USB]

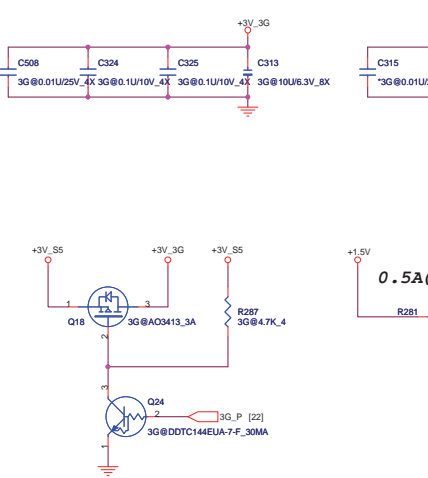


MINI Card Slot#1
(WiFi) [WLN]

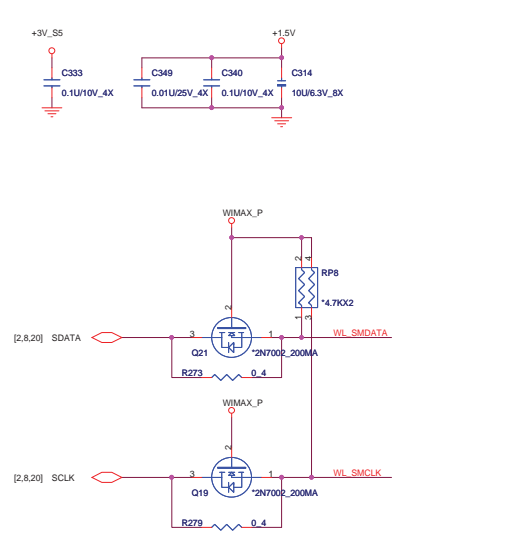
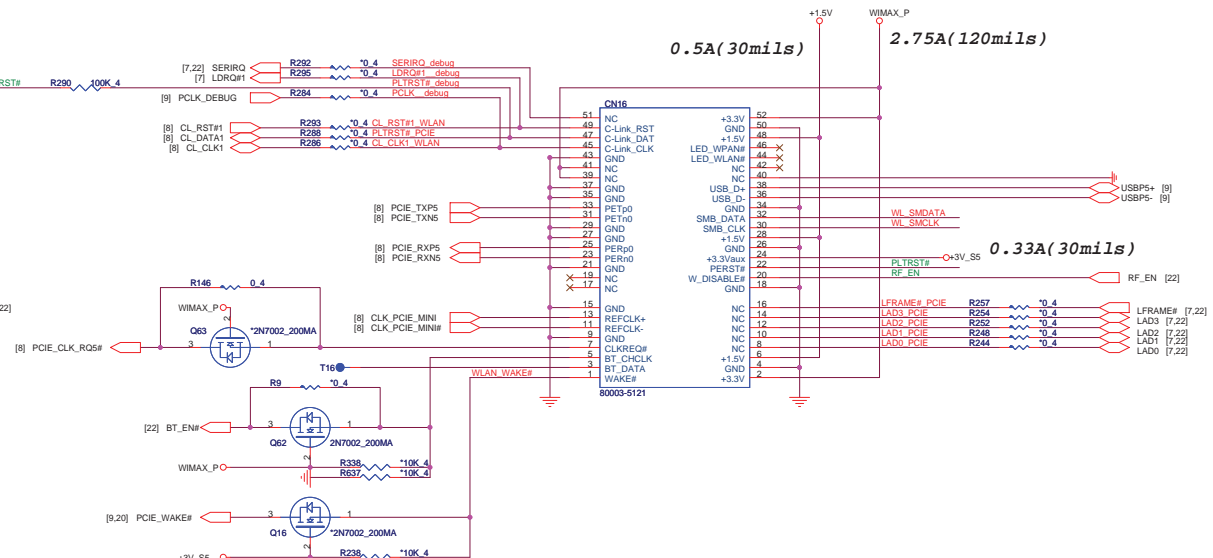


Intel module use S5 power for +3.3V
Other module keep +3V for +3.3V

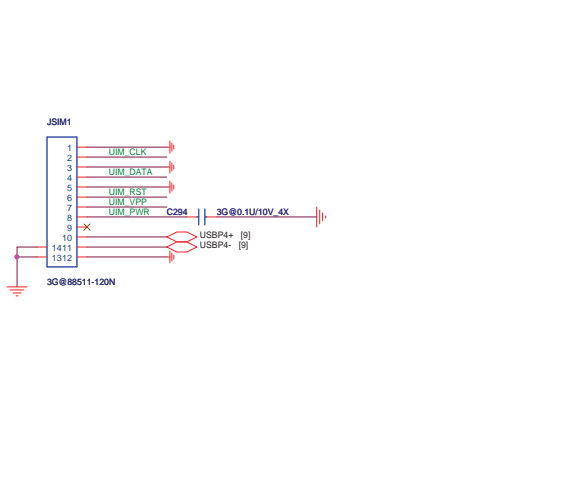
MINI Card Slot#2
3G [M3G]



0.5A (30mils)



SIM CARD

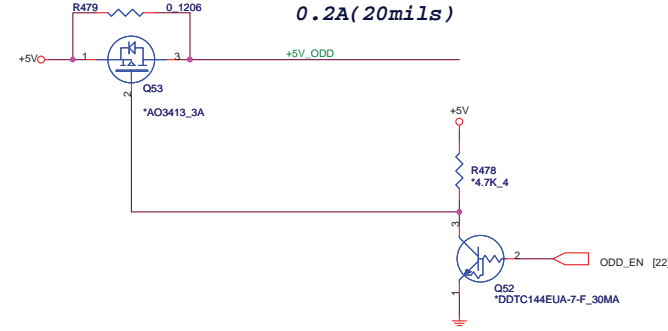
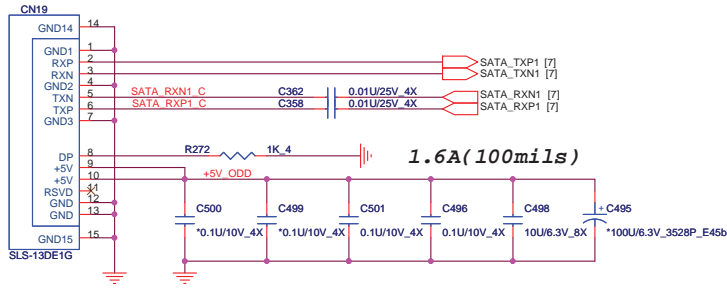


Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	MINI CARD(WLAN/3G/SIM Card)	2A
Date:	Friday, March 19, 2010	Sheet 16 of 35

SATA ODD

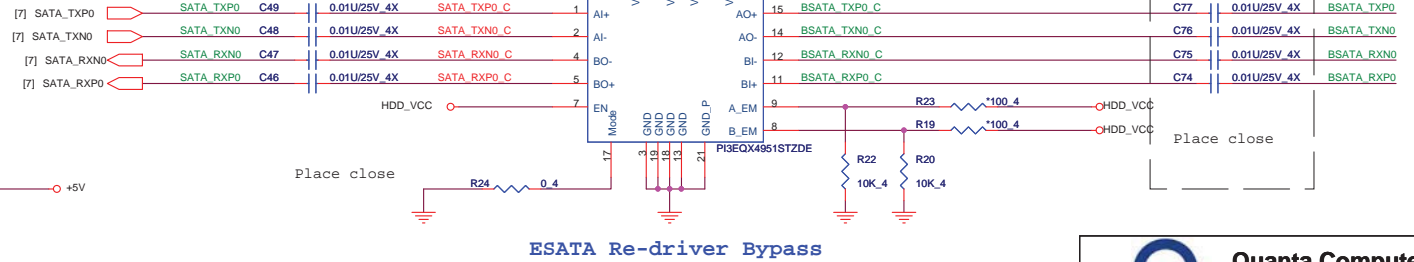
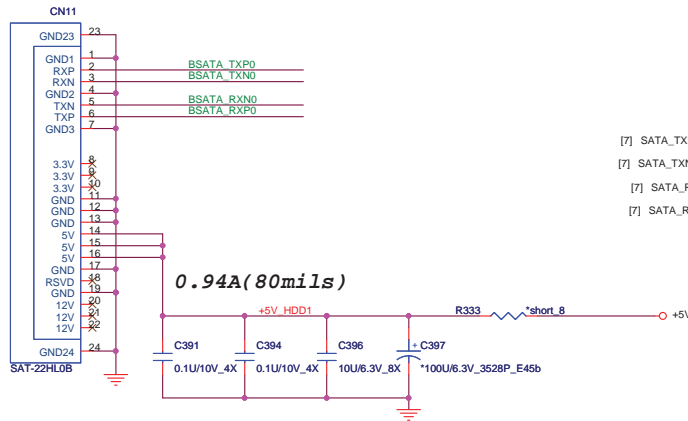
[ODD]




SATA HDD

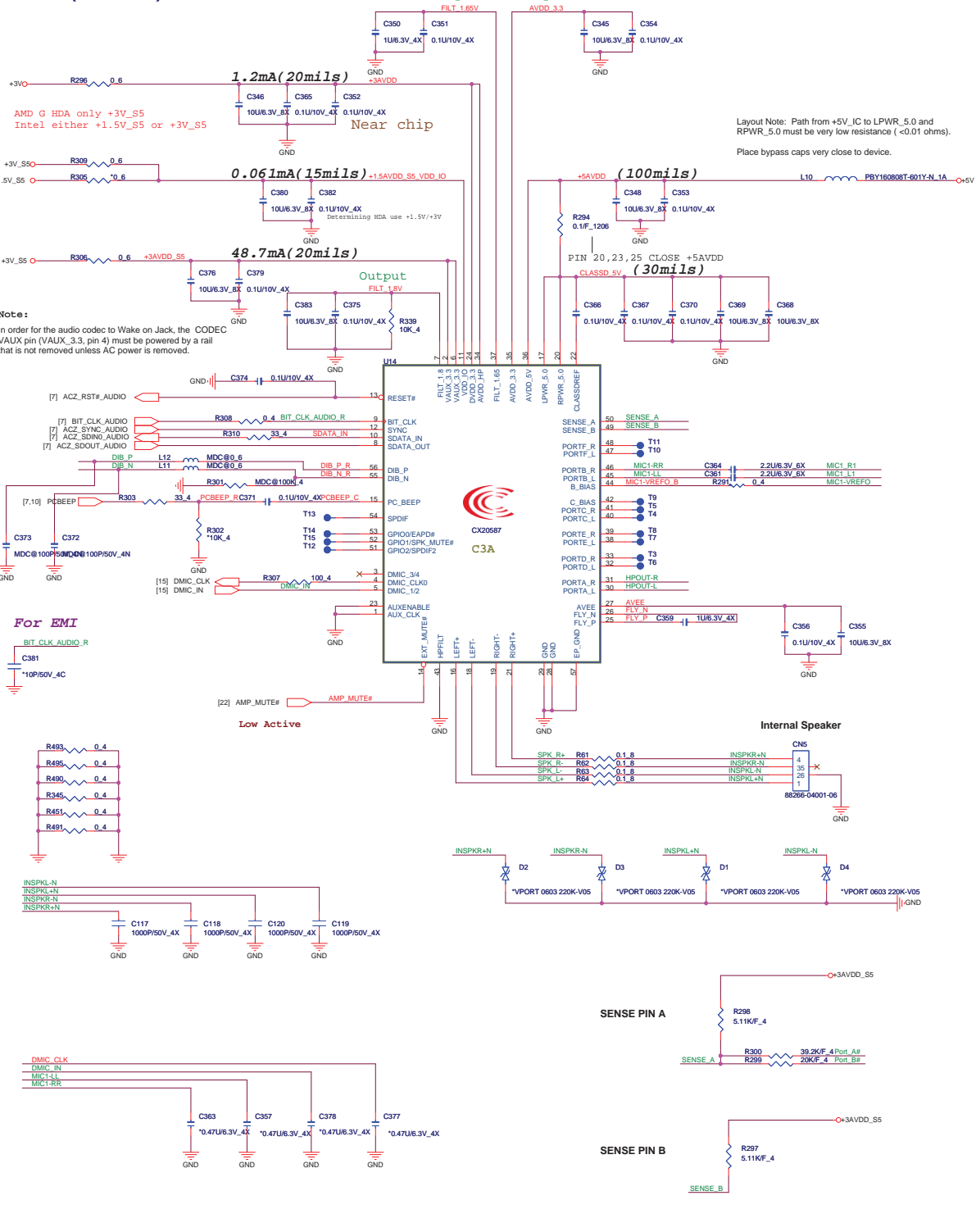
[HDD]

SATA HDD Re-driver IC

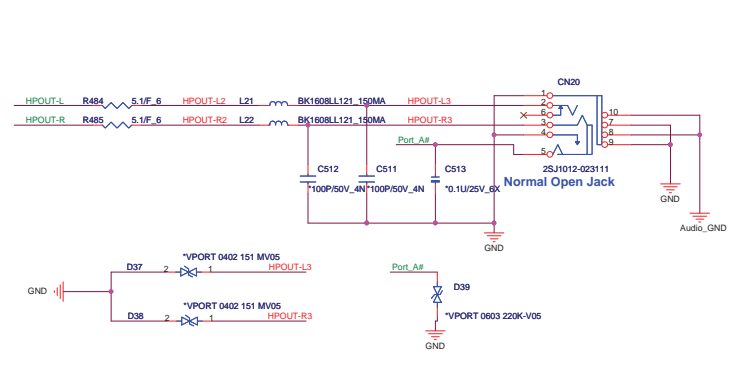


 Quanta Computer Inc. PROJECT : TE2			
			Size
	HDD/ODD/MDC		2A
Date:	Wednesday, March 10, 2010	Sheet	18 of 35

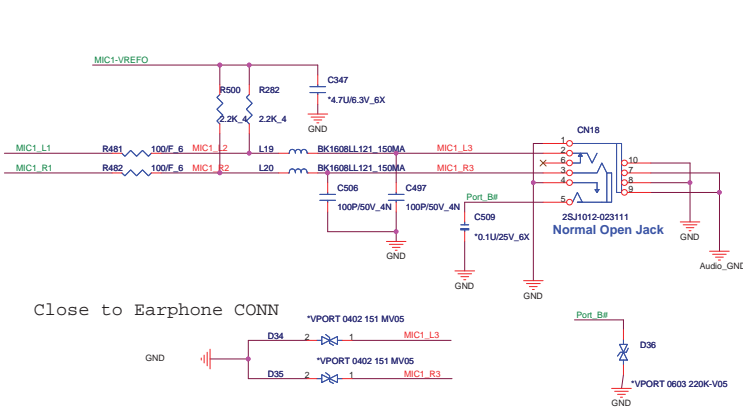
Codec (CX20583) [ADO]



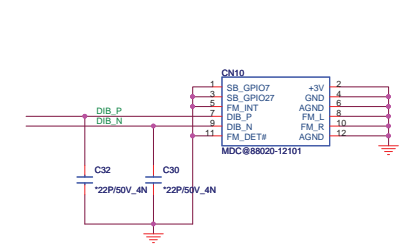
Earphone



External MIC



MDC

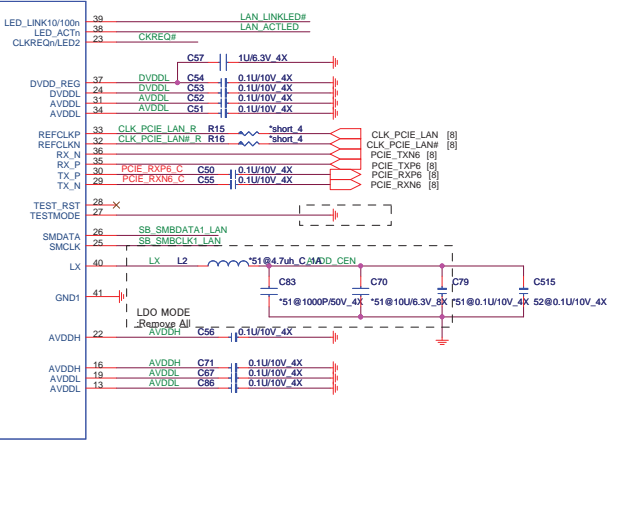
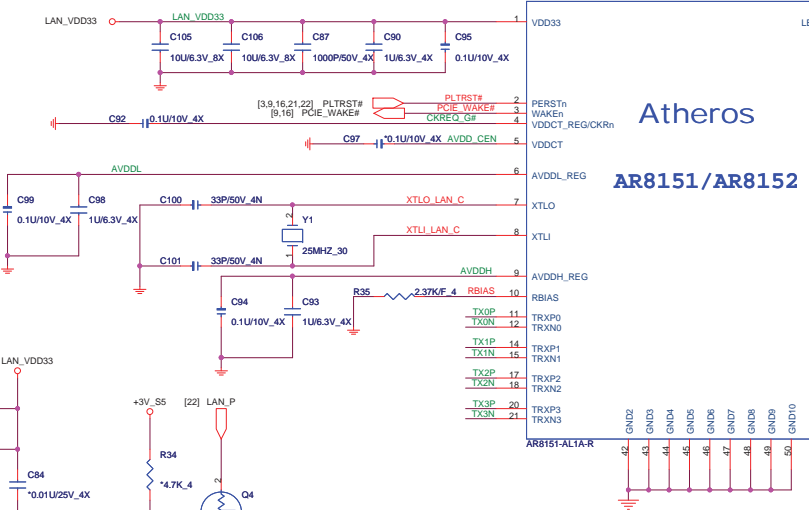
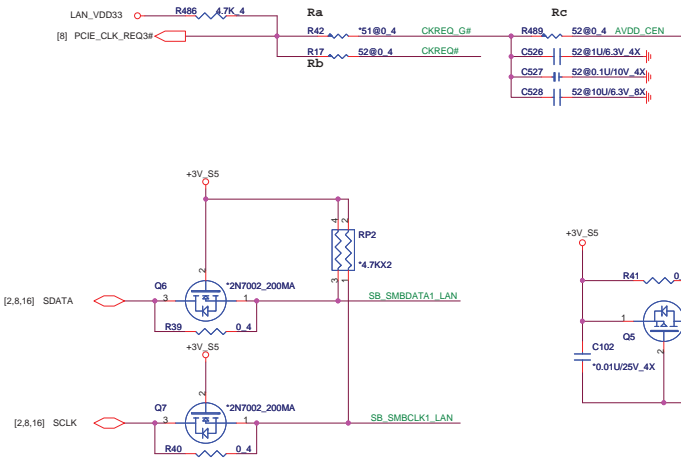


Quanta Computer Inc.
PROJECT : TE2

Size	Document Number	Rev
	Codec (CX20583)	2A
Date:	Friday, March 19, 2010	Sheet 19 of 35

Atheros Lan

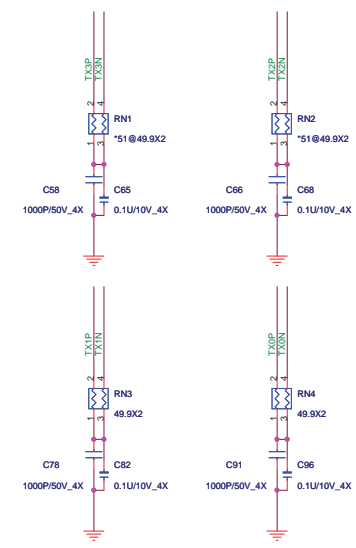
GIGA-STUFF
 Ra 10/100-STUFF
 Rb LDO MODE :STUFF
 Rc



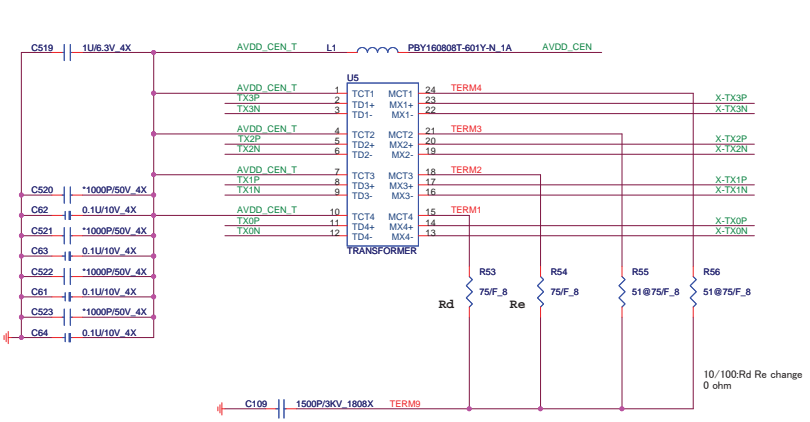
GIGA:AR8151-AL1A-R
 = AL008151001
 10/100:AR8152-AL1A-R
 = AL008152004

LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G#	1	Normal function
	0	ATE test mode

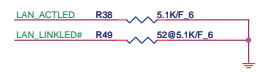
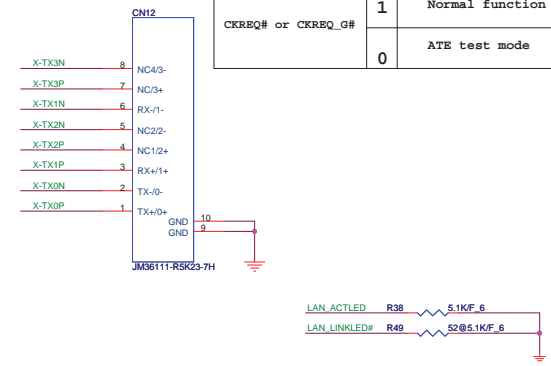
PLACE NEAR LAN IC SIDE



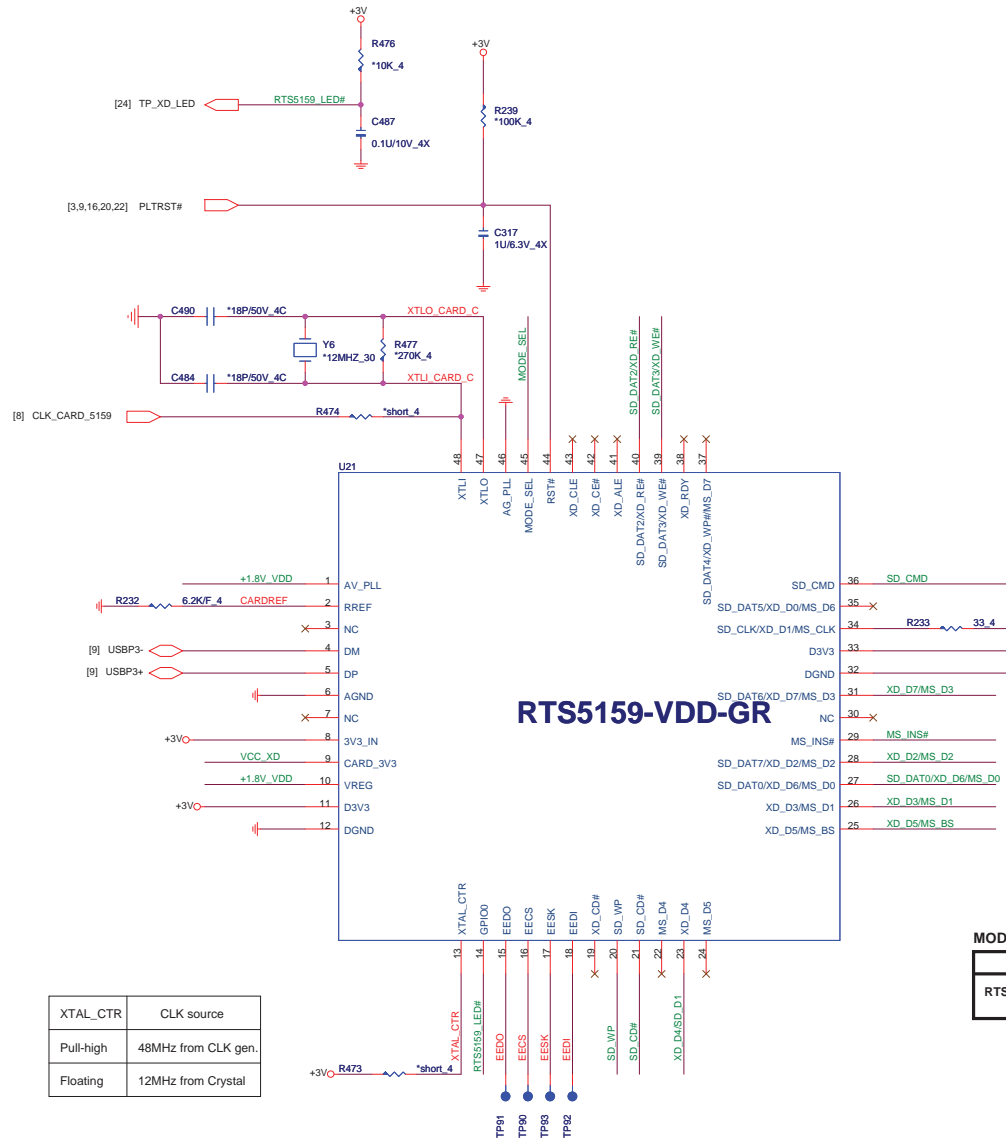
TRANSFORMER



RJ45



3 IN 1 CARD READER

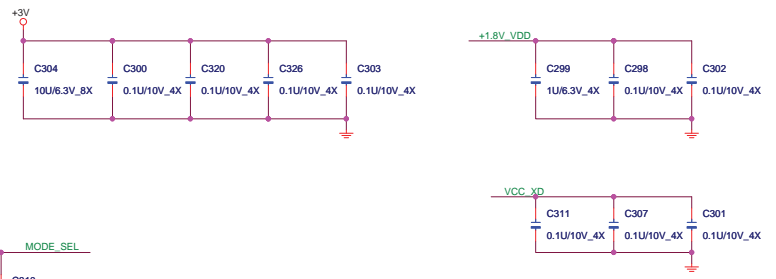
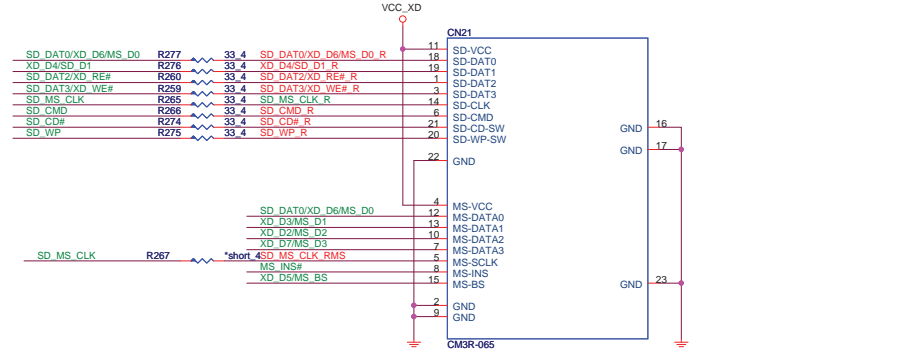


RTS5159-VDD-GR

MODE_SEL (Please refer to Realtek Application Notes for more detail description)

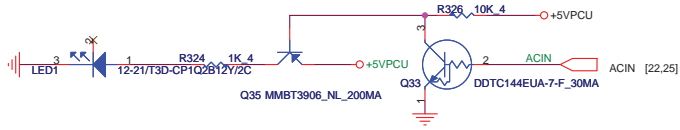
	R49	C73	Power mode
RTS 5159	0-ohm	NC	USB Auto De-link mode:

3 IN 1 CARD READER

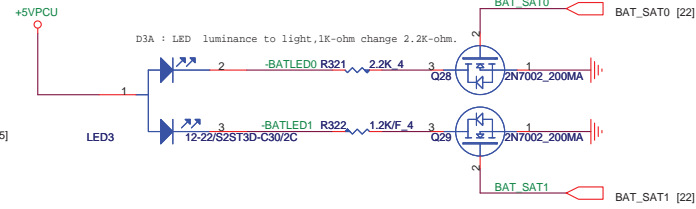


LED [LED]

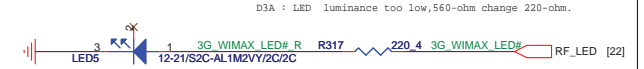
AC-IN



BATTERY

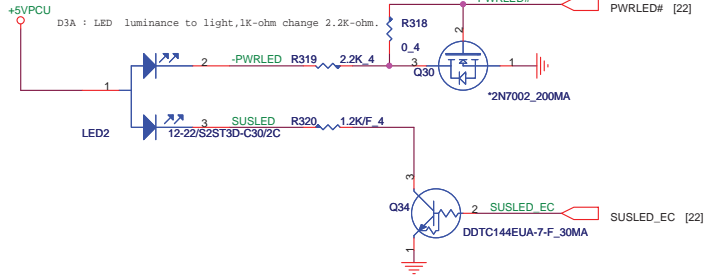


RF LED

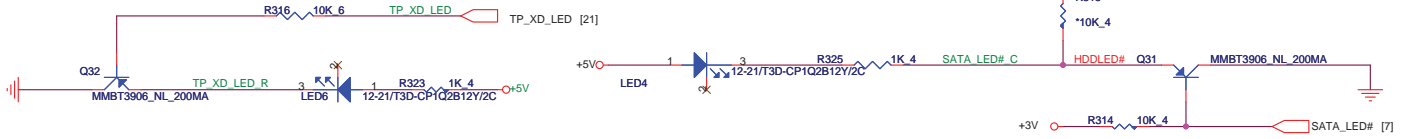


D3A : LED luminance too low,560-ohm change 220-ohm.

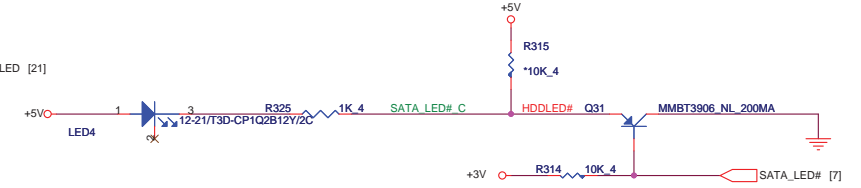
POWER



CARDREADER

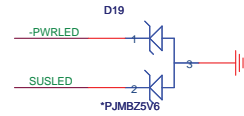


HDD/ODD

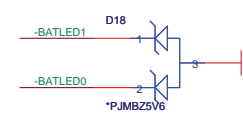


ESD Protect

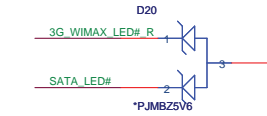
FOR POWER LED



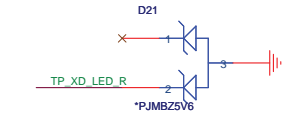
FOR BATTERY LED



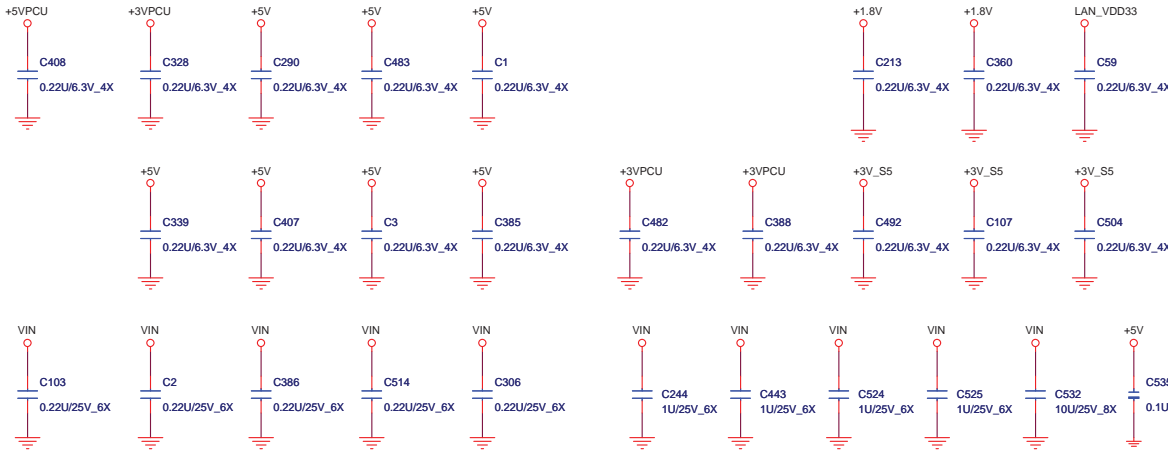
FOR HDD/W-LAN LED



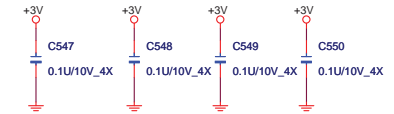
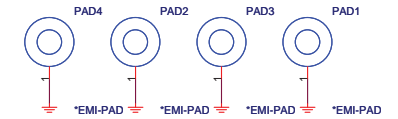
FOR 3G/CARDREADER LED



EMI

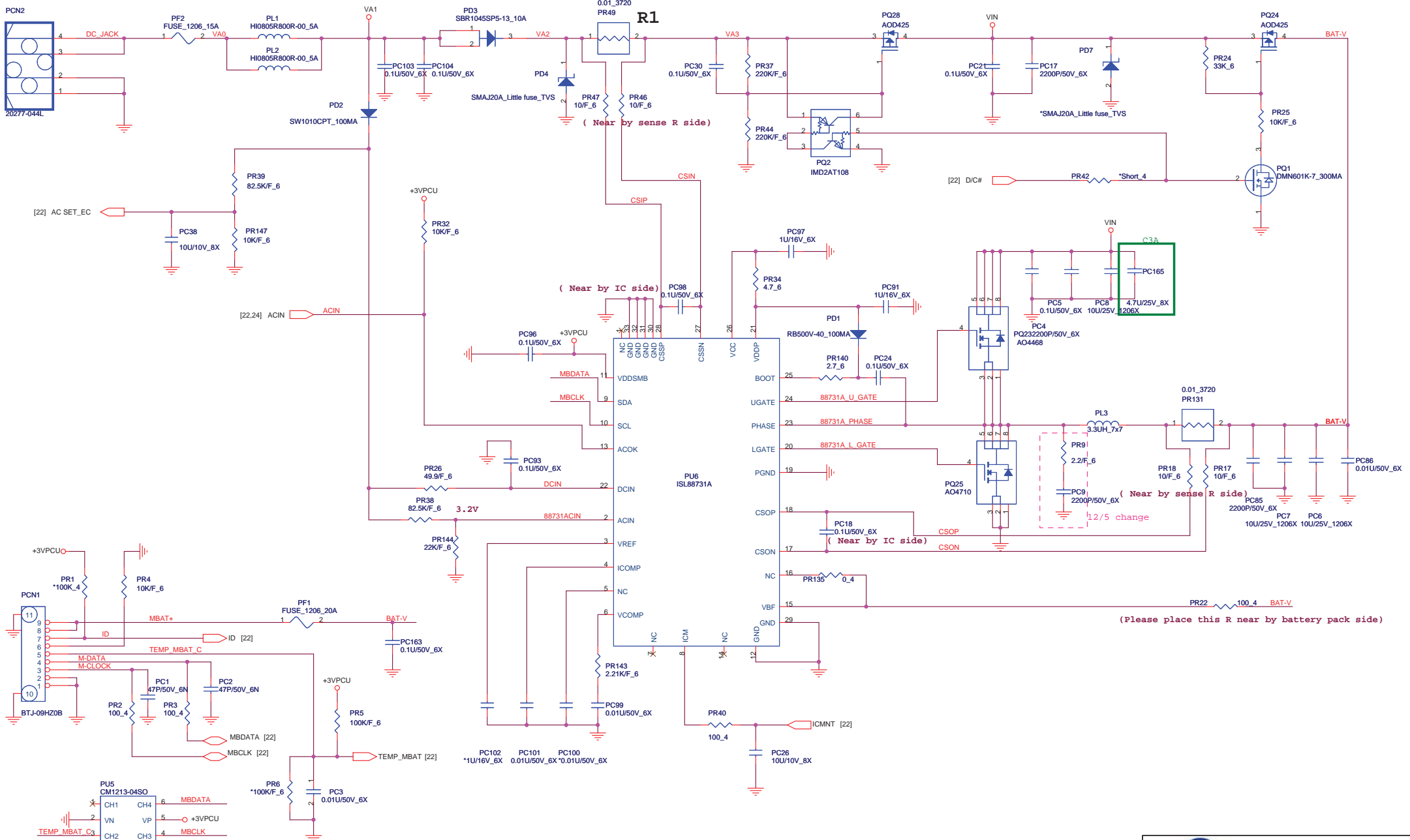


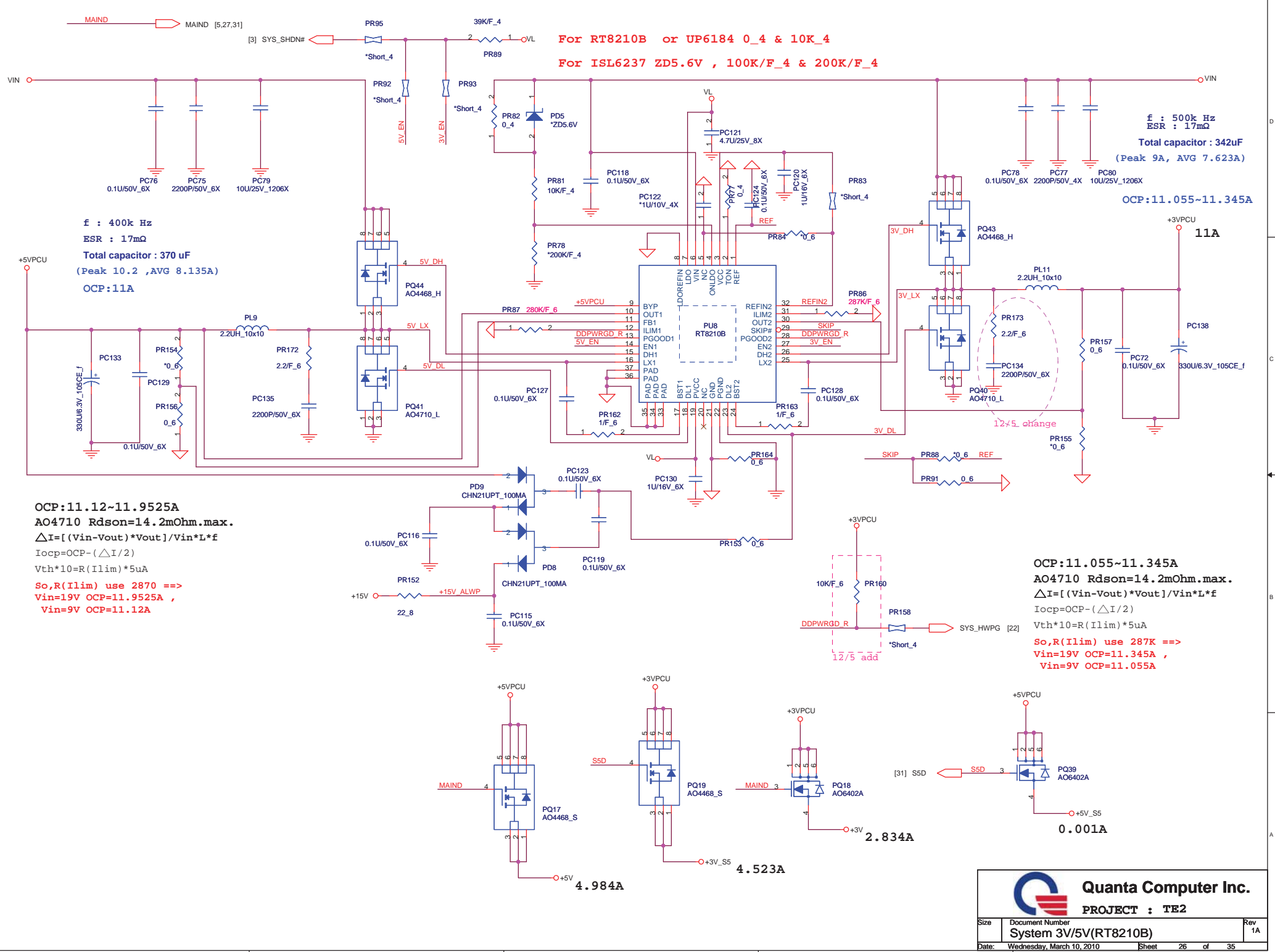
EMI PAD

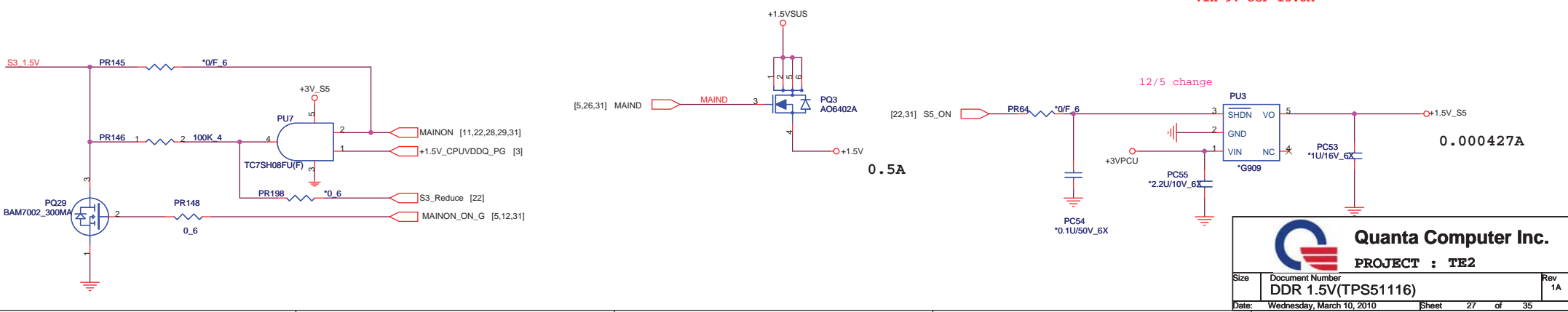
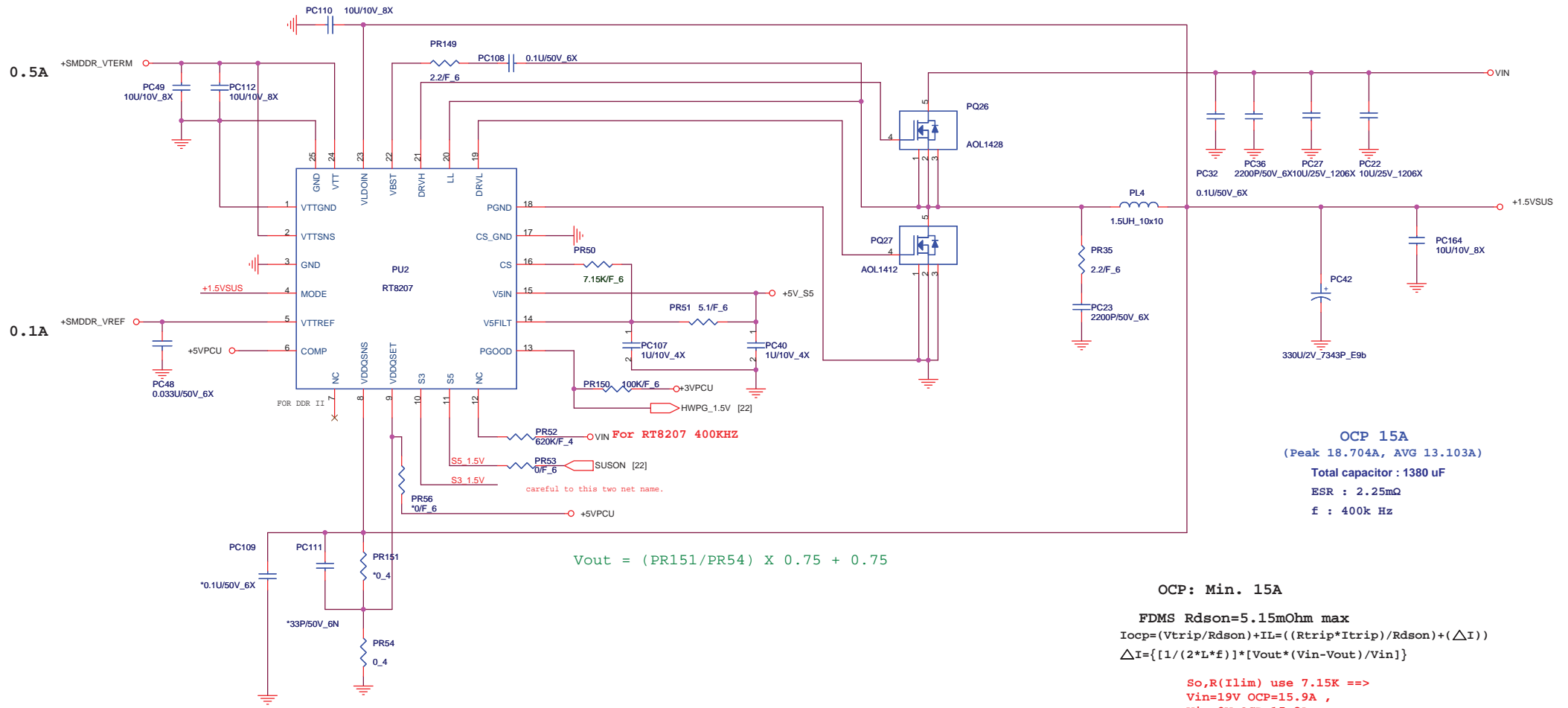


D3A : Add C547,C548,C549,C550 0.1u Cap for EMI issue.

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	LED/HOLE	2A
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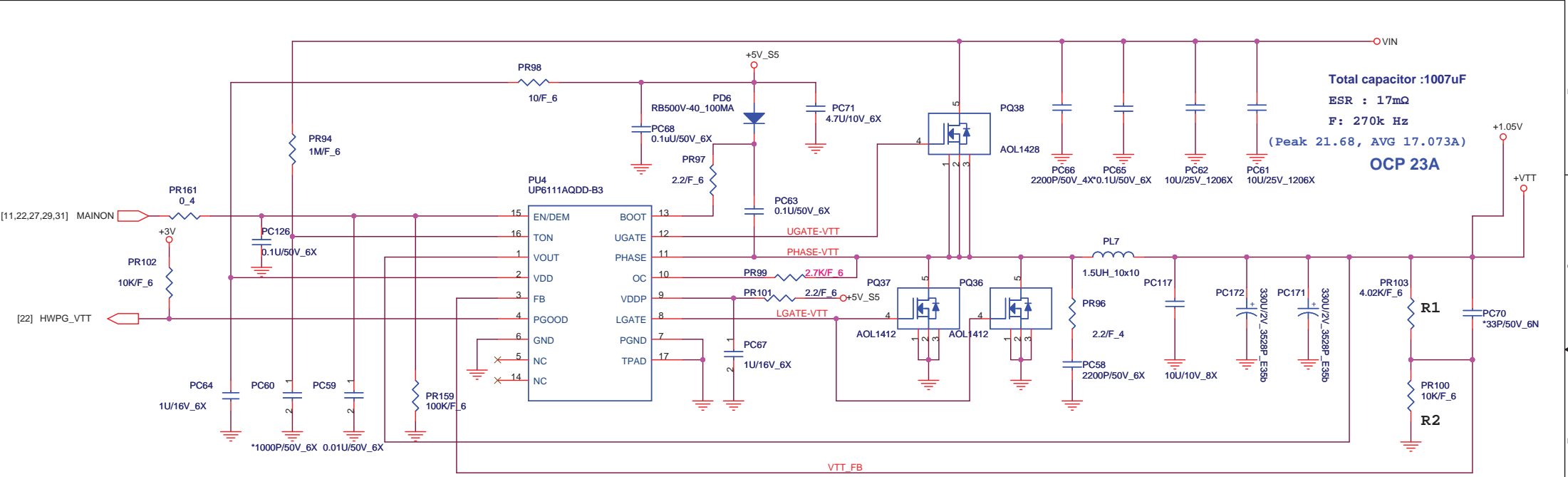






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	DDR 1.5V(TPS51116)	1A
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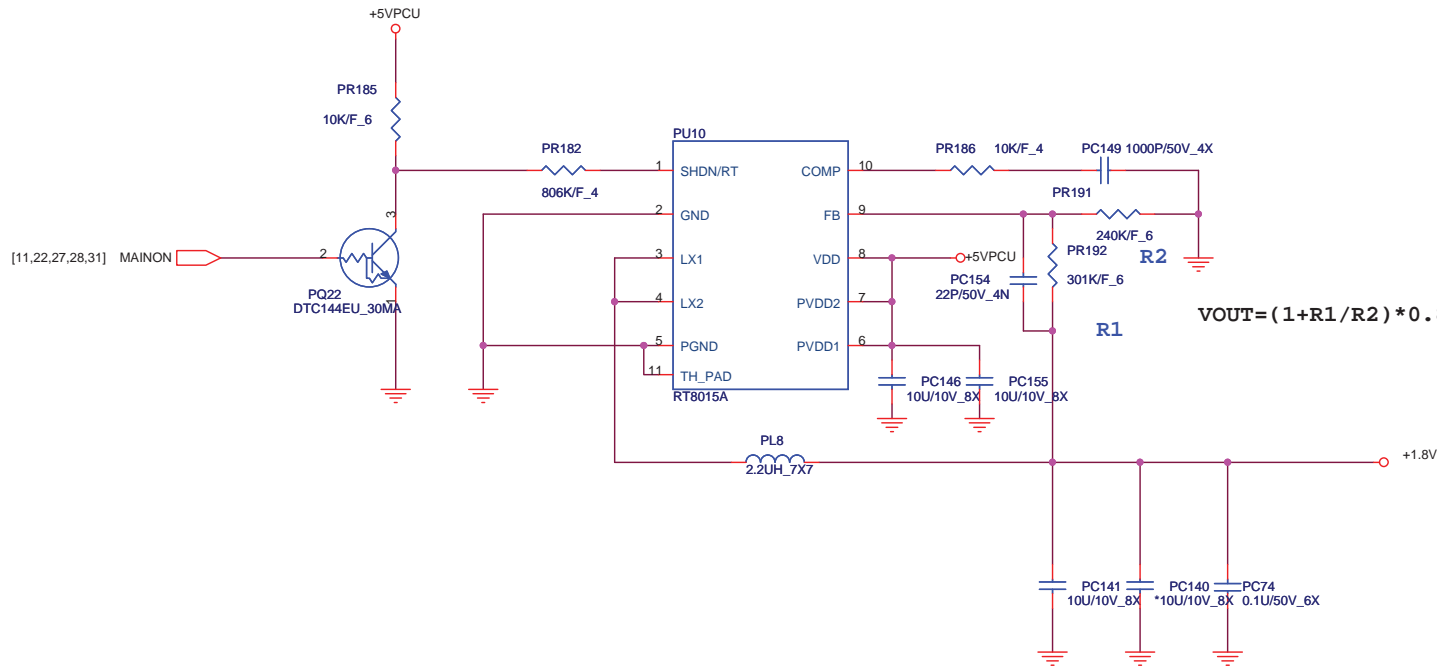
Total capacitor :1007uF
 ESR : 17mΩ
 F: 270k Hz
 (Peak 21.68, AVG 17.073A)
OCP 23A

$$V_{OUT} = (1 + R1/R2) * 0.75$$

OCP: 23.18~23.27A
 FDMS0310 Rdson=5.15mOhm max
 $I_{ocp} = (V_{trip}/R_{dson}) + I_L = ((R_{trip} * I_{trip})/R_{dson}) + (\Delta I)$
 $\Delta I = \{ [1 / (2 * L * f)] * [V_{out} * (V_{in} - V_{out}) / V_{in}] \}$
Rdson * OCP = R_{Ilim} * 20uA
 So, R(Ilim) use 2.7K ==>
 Vin=19V OCP=23.18A ,
 Vin=9V OCP=23.27A

$TON = 3.85p * R_{TON} * V_{out} / (V_{in} - 0.5)$
 Frequency = $V_{out} / (V_{in} * TON)$
 $TON = 3.85p * 1M * 1 / (V_{in} - 0.5)$
 Frequency = $1 / (0.0036767) = 272K$


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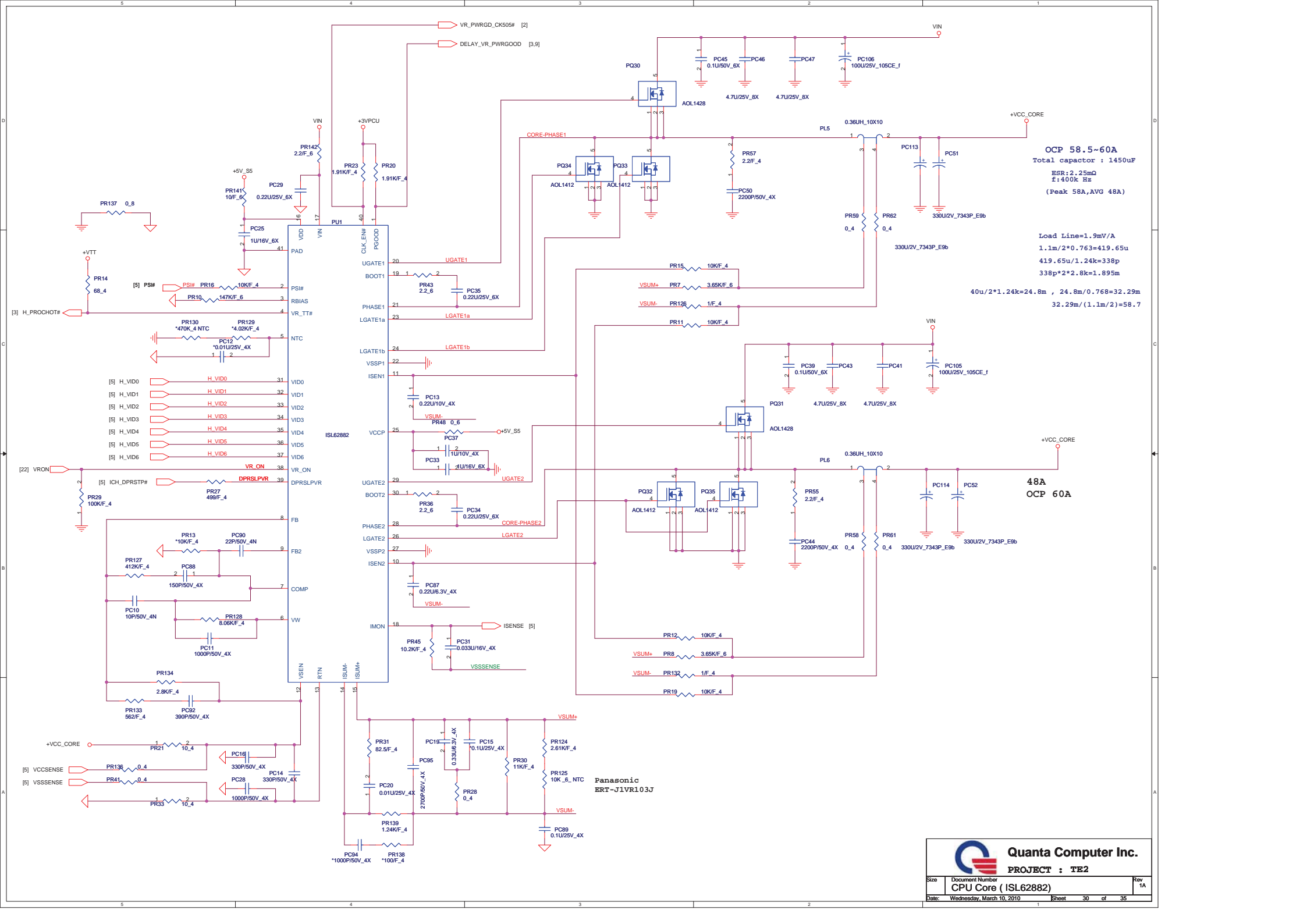


$$V_{OUT} = (1 + R1/R2) * 0.8$$

FOR UMA 0.194A
For VGA 1.345A

OCP Fellow IC spec~3.7A

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			+1.8V (RT8015A)	1A
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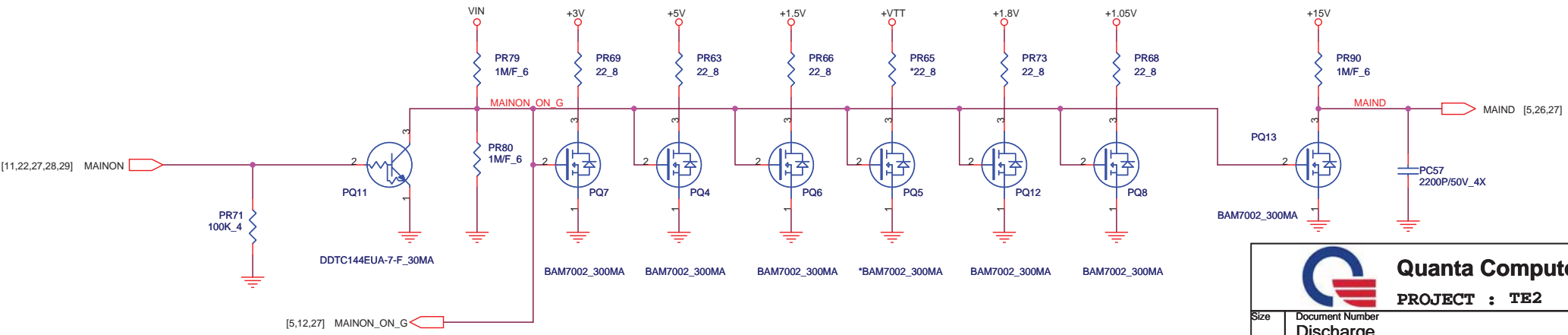
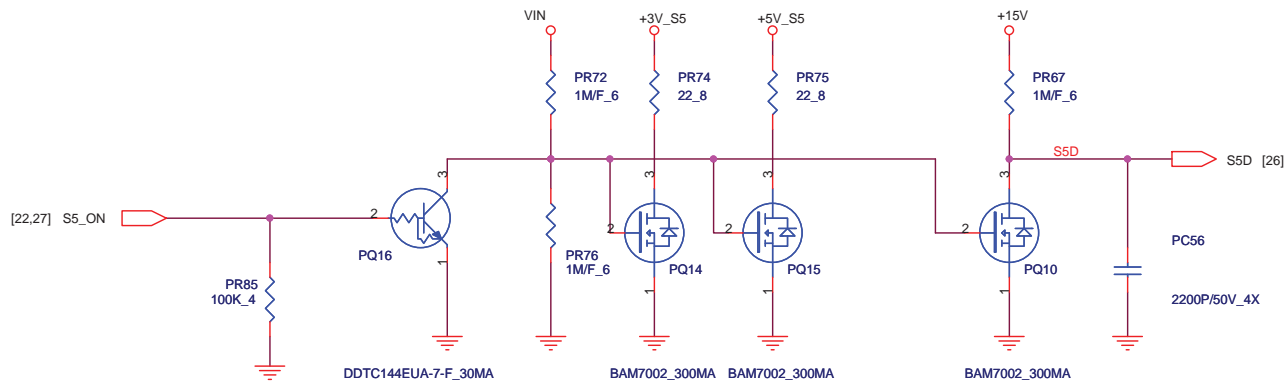
OCP 58.5~60A
 Total capacitor : 1450uF
 ESR: 2.25mΩ
 f: 400k Hz
 (Peak 58A, AVG 48A)


Load Line=1.9mV/A
 $1.1m/2 * 0.763 = 419.65u$
 $419.65u / 1.24k = 338p$
 $338p * 2 * 2.8k = 1.895m$
 $40u / 2 * 1.24k = 24.8m$, $24.8m / 0.768 = 32.29m$
 $32.29m / (1.1m / 2) = 58.7$

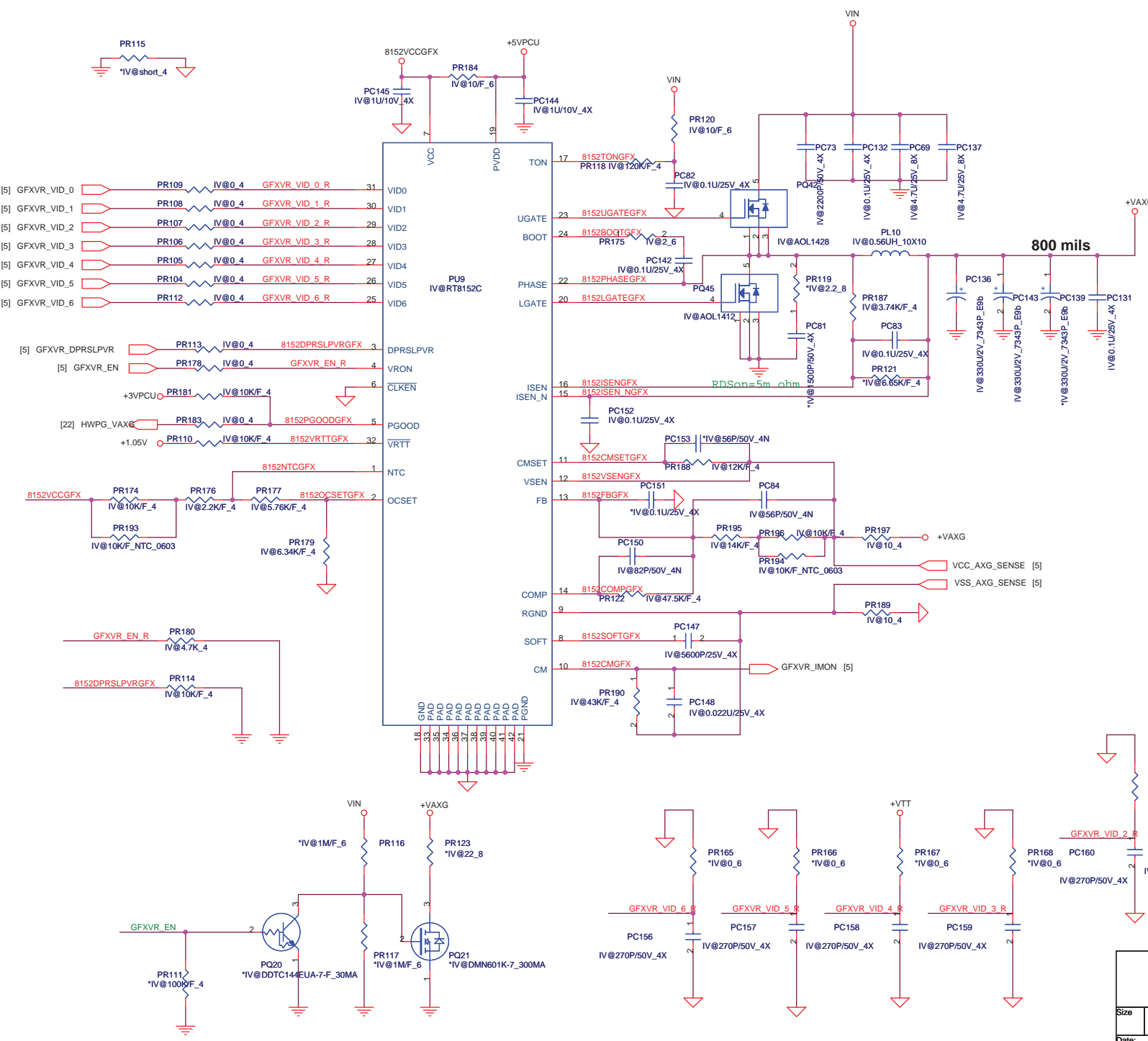
48A
OCP 60A

Panasonic
 ERT-J1VR103J

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Discharge		Sheet	31 of 35



OCP 20A
(Peak 19A, AVG 15.4A)

Total capacitor : 330 uF
ESR : 4.5mΩ
f : 300k Hz






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		Document Number UMA GPU CORE (RT8152C)
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15-16	DDRIII SO-DIMM	DDR
17	VGA Connector	VGA
18	LCD Panel	LDS
	CRT & CRT BUS SWITCH	CRT
	CCD	CCD
	HALL SENSOR&BACK LIGHT SWITCH	HSR
19	Display Port	DPP
20	HDMI comm part	HDM
	HDMI for GM	HMG
21	SATA ODD	ODD
	Main SATA HDD & 2nd SATA HDD	HDD
	G-Sensor	H3D
22	5 IN 1 Card reader	MMC
	IEEE1394	FIW
23	MINI Card (Wi-Fi & WIMAX)	WLN
	MINI Card 2nd	MNC
	MINI Card 3rd	MNC
	TMA Connector	TMA
24	INT KeyBoard & K/B LED Power	KBC
	LED Board	LED
	TP&FP board	TPD,FPD
	Bluetooth Connector	BTM
	Felica Connector	FEC
	MMB Connector	MMB
	Power SW	PSW
	B-CAS Connector	BCS
25	New Card (Express Card)	EXC
	E-SATA comb USB	ESA
	USB Connector	USB
	Audio & USB Board	USB,ADO
	Light Sensor	LSN
	Satellite LED	LED
	RF LED / WIMAX LED / Kill SW	KSW
26	EC WP8763LDG/WPC8769L(O)	KBC
	CIR	CIR
27	Codec (CX20583)	ADO
28	FM Tunner	FMM
	Modem Connector	MDM
	HOLE	
29	Atheros LAN	LAN
30	NVRAM Connecytor	NVR
31	Charger (ISL6251A)	PWM
32	System 5V/3V (ISL6237)	PWM
33	CPU CORE (ISL62882)	PWM

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
+VCCRTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
+5V_TMA	+5V	MAIN_ON	S0
WIMAX_P	+3.3V	WMAX_P for EC	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_S5	+1.5V	S5_ON	S0~S5
+1.5V_SUS	+1.5V	SUSON	S0~S3
+VCC_CORE		VRON	S0
+VTT	+1.05V~+1.1V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		GFXVR_EN	S0

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36	+1.05V (UP6111AQDD)	PWM
37	DDR 1.5V (TPS51116)	PWM
38	Discharge (1.5V_S5/1.8V)	PWM
39	Power Tree Table	
40	PCH Power Plane	
41	Power Management	
42	Change List	




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Model	REV	CHANGE LIST	MODEL		
			PAGE	FROM	To
TE2 MB	B2A	PAGE(16) : Add BT_EN# for combo RF control for BT	1	1A	
		PAGE(27) : Change DDR S3_1.5V ON circuit.	2	1A	
	C3A	PAGE(07) : Add ESATA re-driver IC	3	1A	
			4	1A	
	D3A	PAGE(24) : LED luminance to light,R321 ~ R319 1K-ohm change 2.2K-ohm.	5	1A	
		PAGE(24) : LED luminance too low,R317 560-ohm change 220-ohm.	6	1A	
		PAGE(19) : Add R61,R62,R63,R64 0.1-ohm to avoid speaker burn.	7	1A	
		PAGE(16) : Add Q62 to avoid leakage current.	8	1A	
			9	1A	
			10	1A	
			11	1A	
			12	1A	
			13	1A	
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			17	1A	
			18	1A	
			19	1A	
			20	1A	
			21	1A	
			22	1A	
			23	1A	
			24	1A	
			25	1A	
			26	1A	
			27	1A	
			28	1A	
			29	1A	
			30	1A	

DOC NO. 204	PROJECT MODEL :	TE2	APPROVED BY:	Mosy Li	DATE:	2009/11/13
	PART NUMBER:		DRAWING BY:	Mosy Li	REVISION:	1A



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Change list

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