Model Name : SAGE 3G
Compal Project Name : V1JB1
File Name : LA-A041P

Compal Confidential

V1JB1 UMA M/B Schematics Document

Intel Ivy/Sandy Bridge SFF BGA 1023p Processor
/Panther Point 989p PCH
/ DDR3L Memory Down *8

2013-03-26

REV:2.0

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

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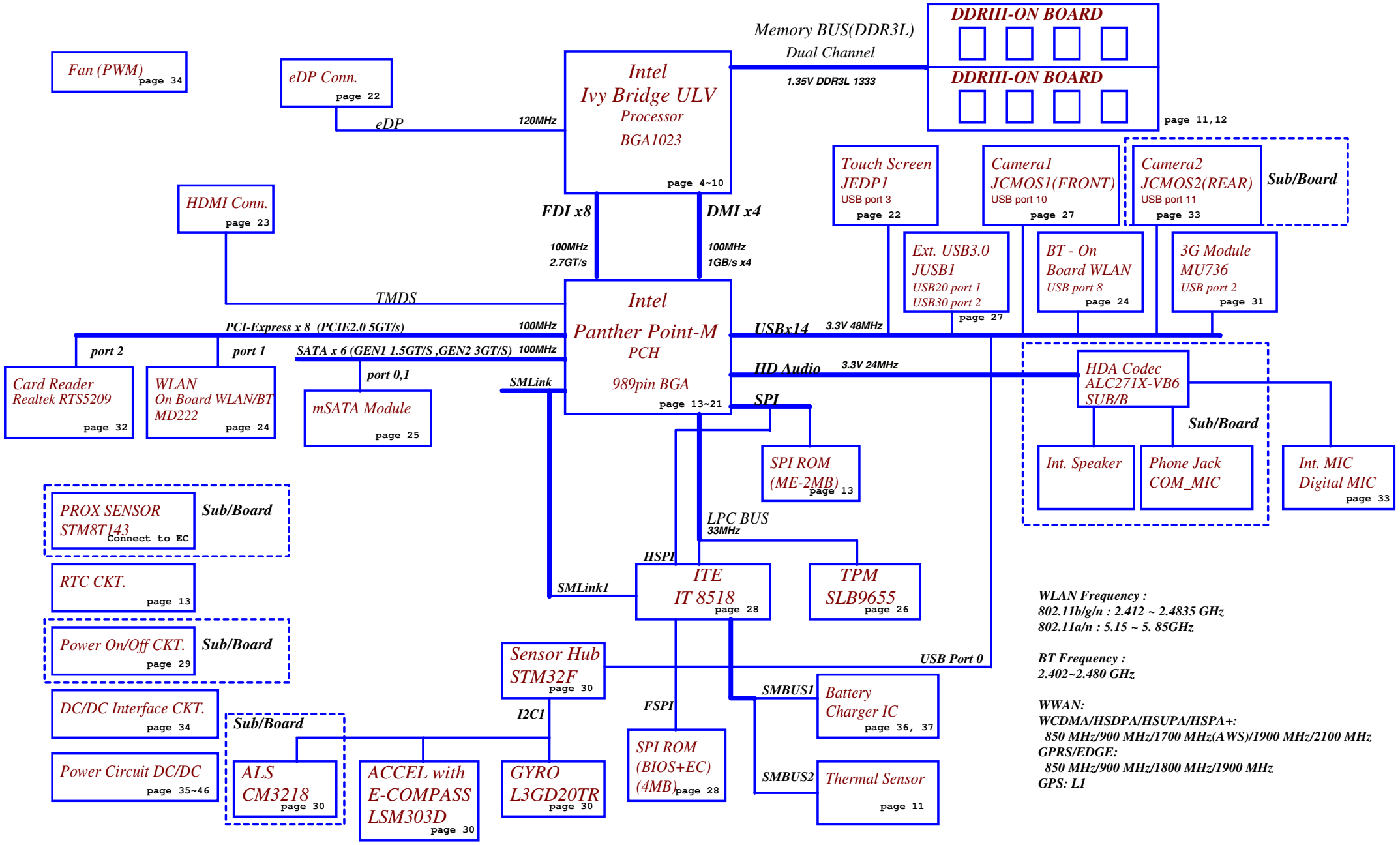
Title: Cover Page

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 2.0

Date: Tuesday, March 26, 2013 | Sheet 1 of 52



WLAN Frequency :
802.11b/g/n : 2.412 ~ 2.4835 GHz
802.11a/n : 5.15 ~ 5. 85GHz

BT Frequency :
2.402~2.480 GHz

WWAN:
WCDMA/HSDPA/HSUPA/HSPA+:
850 MHz/900 MHz/1700 MHz(AWS)/1900 MHz/2100 MHz
GPRS/EDGE:
850 MHz/900 MHz/1800 MHz/1900 MHz
GPS: L1

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	Compal Electronics, Inc.	
Title	Block Diagrams	
Size: Custom	Document Number: V1JB1 M/B LA-A041P Schematic	Rev: 0.1
Date: Tuesday, March 26, 2013	Sheet 2 of 52	

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.35V	+1.35VP to +1.35V power rail for DDR3L	ON	ON	OFF
+1.35VS	+1.35V to +1.35VS switched power rail	ON	OFF	OFF
+0.675VS	+0.675VSP to +0.675VS switched power rail for DDR3L terminator	ON	OFF	OFF
+1.5VS	+1.5VSP to +1.5VS power rail for PCH	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8VS switched power rail for PCH	ON	OFF	OFF
+3VALW	+3VALWP to +3VALW always on power rail	ON	ON	ON*
+VCCSUS3_3	+3VALW to +VCCSUS3_3 power rail for PCH	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW always on power rail	ON	ON	ON*
+V5REF_SUS	+5VALW to +V5REF_SUS power rail for PCH	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

PCH SM Bus address

Device		Address
ChannelA	A0	1010 000X
ChannelB	A4	1010 010X

Sensor HUB SM Bus address

Device		Address
Gyroscope	D1	1101 000X b
	D3	1101 001X b
E-compass + G sensor	33	0011 001X b
ALS sensor	21	0010 000X b

BOM Config

Sensors List

Connect to	Function	Device
Sensor Hub	Gyroscope	ST - L3GD20TR
Sensor Hub	Accel+E-Compass	ST - LSM303DLHCTR
PCH(USB P3)	Sensor Hub	ST - STM32F103RCY6TR
Sensor Hub	ALS	Capella - CM3218
EC	Prox	ST-STM8T143AU62TTRC06

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	2.0*
5	
6	
7	

Note :

BTO Option Table

BTO Item	BOM Structure
Unpop	@
Connector	CONN@
UMA	UMA@
CPU	IVB@
DDR3	DDR3@
DDR3L	DDR3L@
On Board DRAM	X76@
Dual Channel DDR	128@
eDP	eDP@
PCH	HM77@
Normal S3	S3@
Deep S3	DS3@
TPM	TPM@
Non TPM SKU	WOTPM@
Hall Sensor	LID@
Foxconn MD222	FOXMD222@
Lite-On MD222	LIONMD222@
For EMI/RF(Pop)	EMC@
For EMI/RF(Unpop)	XEMC@
Sensor(Intel F/W)	INTEL@
Sensor(ST F/W)	ST@
3G SKU	3G@
3G SKU(EMC part)	3GEMC@

USB Port Table

USB 2.0	USB 1.1	Port	2 External USB Port
EHCI1	UHCI0	0	Sensor Hub
		1	Ext. USB Connector
	UHCI1	2	3G Module - MU736/ME906
		3	Touch Screen
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	BlueTooth(WLAN Module)
		9	Debug Port(Reserve)
	UHCI5	10	Camera(Front)
		11	Camera(Rear)
	UHCI6	12	
		13	

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Title: Notes List

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

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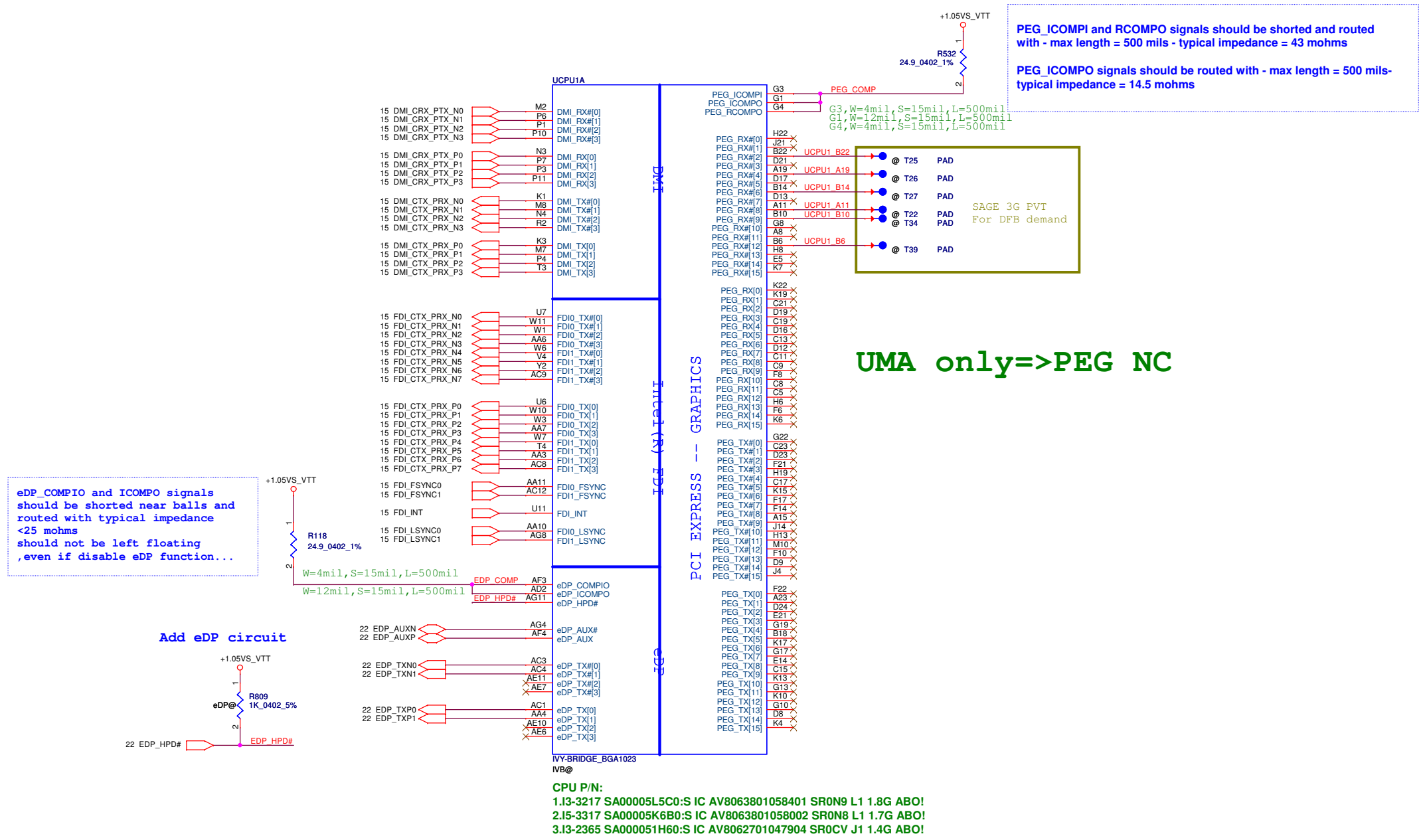

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

Compal Electronics, Inc.			
Title	PROCESSOR(1/7) DMI,FDI,PEG		
Size: Custom	Document Number: V1JB1 M/B LA-A041P Schematic		Rev: 0.1
Date: Wednesday, March 13, 2013	Sheet 4 of 52		

PCH->CPU
UNCOREPWRGOOD:非CORE外的電OK
SM_DRAMPWROK:DRAM power ok
RESET#:都ok後請CPU做reset

Follow DG 1.2 & CRB1.0

C784 2 @ 1 0.1U_0201_10V6K H_CPUPWRGD
R223 2 1 10K_0402_5% H_CPUPWRGD

PROC_SELECT#
Future platforms,PH VCPLL and connect to PCH DF_TVS

偵測CPU有無安裝

XBOX 三紅功能

Processor Pullups follow CRB1.0

+1.05VS_VTT R220 2 1 62_0402_5%
28,36 H_PROCHOT# H_PROCHOT# R216 56_0402_5% H_PROCHOT#_R

Follow DG 1.2 & CRB1.0
Buffered reset to CPU

SAGE 3G

+3VS C396 0.1U_0402_16V4Z
+1.05VS_VTT R226 75_0402_5% R227 43_0402_1%
U15 SN74LVC1G07DCKR_SC70-5
17,26,28,31,32 PLT_RST# BUFO_CPU_RST# BUF_CPU_RST#

RESET#:都ok後請CPU做reset

Use open drain MOS:
+1.05VS_VTT PH pop 75ohm
series resister pop 43ohm

SAGE 3G

UCPU1B

MISC
15 H_SNB_IVB# F49 PROC_SELECT#
C57 PROC_DETECT#

THERMAL
T1 @PAD H_CATERR# C49 CATERR#
28 H_PECI H_PECI A48 PECI
H_PROCHOT# C45 PROCHOT#
18 H_THRMTRIP# D45 THERMTRIP#

PWR MANAGEMENT
15 H_PM_SYNC C48 PM_SYNC
18 H_CPUPWRGD R80 0_0402_5% H_CPUPWRGD_R B46 UNCOREPWRGOOD
UNCOREPWRGOOD:除了CPU_CORE以外的電OK
PM_DRAM_PWRGD_R BE45 SM_DRAMPWROK
SM_DRAMPWROK:DRAM power ok
BUF_CPU_RST# D44 RESET#

IVY-BRIDGE_BGA1023
IVB@

CLOCKS
BCLK J3 CLK_CPU_DMI 14
BCLK# H2 CLK_CPU_DMI# 14
DPLL_REF_CLK AG3 CLK_CPU_DPLL CLK_CPU_DPLL 14
DPLL_REF_CLK# AG1 CLK_CPU_DPLL# CLK_CPU_DPLL# 14

DDR3 MISC
SM_DRAMRST# AT30 SM_DRAMRST# SM_DRAMRST# 6
SM_RCOMP[0] BF44 SM_RCOMP0 R149 2 1 140_0402_1%
SM_RCOMP[1] BE43 SM_RCOMP1 R486 2 1 25.5_0402_1%
SM_RCOMP[2] BG43 SM_RCOMP2 R484 2 1 200_0402_1%

DDR3 Compensation Signals
Trace:10mil ,Spacing:13mil, Max.Length:500mil

JTAG & BPM
PRDY# N53
PREQ# N55
TCK L56 XDP_TCK @PAD T2
TMS L55 XDP_TMS @PAD T3
TRST# J58 XDP_TRST# @PAD T4
TDI M60 XDP_TDI @PAD T5
TDO L59 XDP_TDO @PAD T6
DBR# K58 XDP_DBRESET#
BPM#[0] G58
BPM#[1] E55
BPM#[2] E59
BPM#[3] G55
BPM#[4] G59
BPM#[5] H60
BPM#[6] J59
BPM#[7] J61

XDP_DBRESET# XDP_DBRESET# 15
C102 XEMC@ 100P_0402_50V8J
SAGE 3G
For EMI

+1.05VS_VTT
CLK_CPU_DPLL# R116 2 @ 1 1K_0402_5%
CLK_CPU_DPLL R117 2 @ 1 1K_0402_5%

Checklist1.0 P.64 Processor Graphis Disable Guide
DIS only SKU or UMA eDP disable
DPLL_REF_SSCLK PD 1K_5% to GND
DPLL_REF_SSCLK# PH 1K_5% to +1.05VS_VTT

+3VS
XDP_DBRESET# R569 2 1 1K_0402_5%

CRB1.0 PH 1K +3VS
Check list 1.0 PH 5K +3VS
Check list 1.2 PH 10K +3VS
Debug port DG1.1-1.2 50~5K ohm

Follow DG 1.2 & CRB1.0

+3VALW C101 0.1U_0402_16V4Z
28,42 VR_ON R82 @ 0_0402_5%
15 SYS_PWROK R81 @ 0_0402_5%
15 PM_DRAM_PWRGD
U5 MC74VHC1G09DFT2G_SC70-5
PM_SYS_PWRGD_BUF
+1.35VS R88 200_0402_5%
R97 130_0402_5%
PM_DRAM_PWRGD_R

Use open drain MOS:
+1.35VS PH pop 200ohm
series resister pop 130ohm

SAGE 3G

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

Compal Electronics, Inc.
Title: PROCESSOR(2/7) PM,XDP,CLK
Size: Custom
Document Number: V1JB1 M/B LA-A041P Schematic
Rev: 0.1
Date: Wednesday, March 13, 2013
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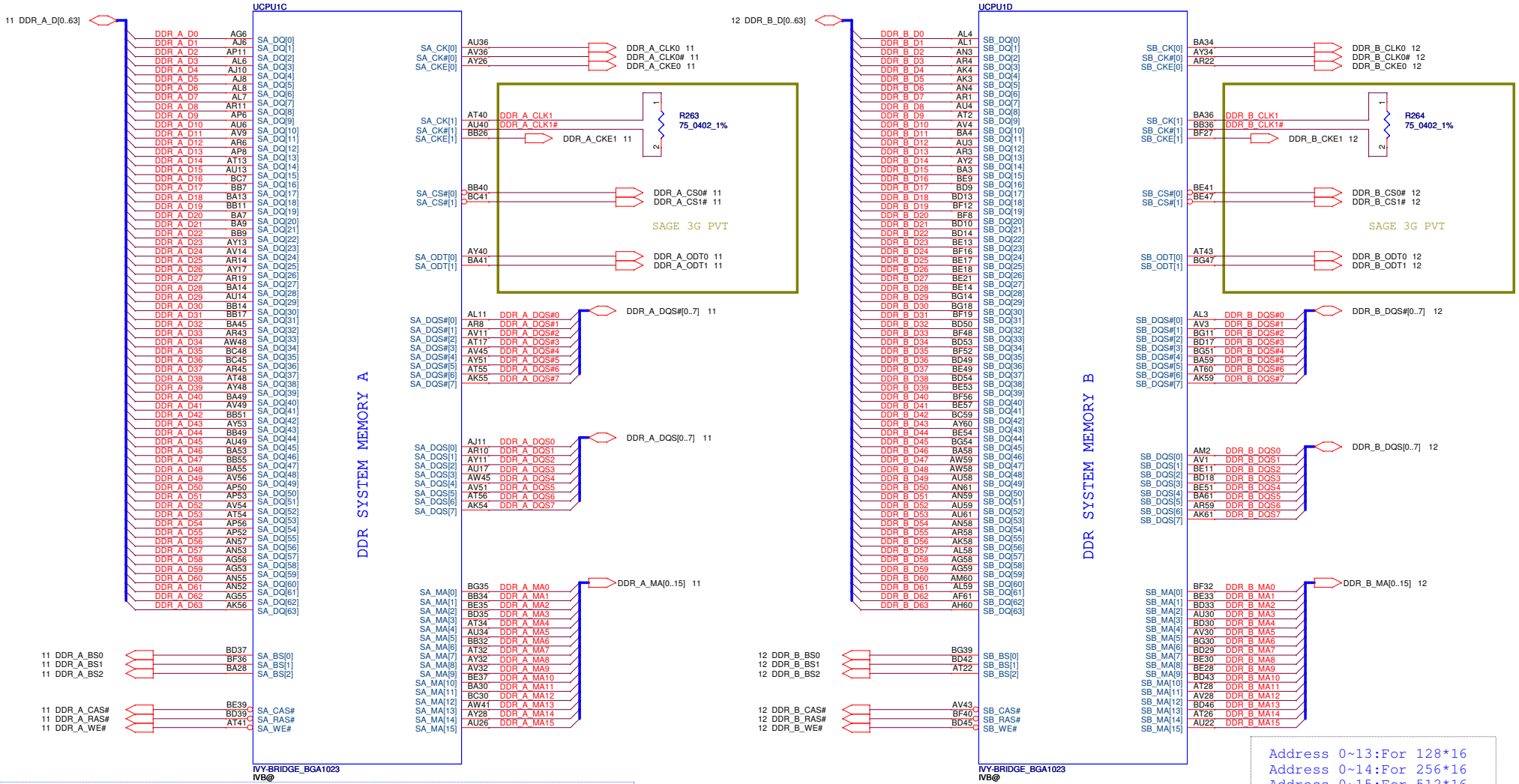
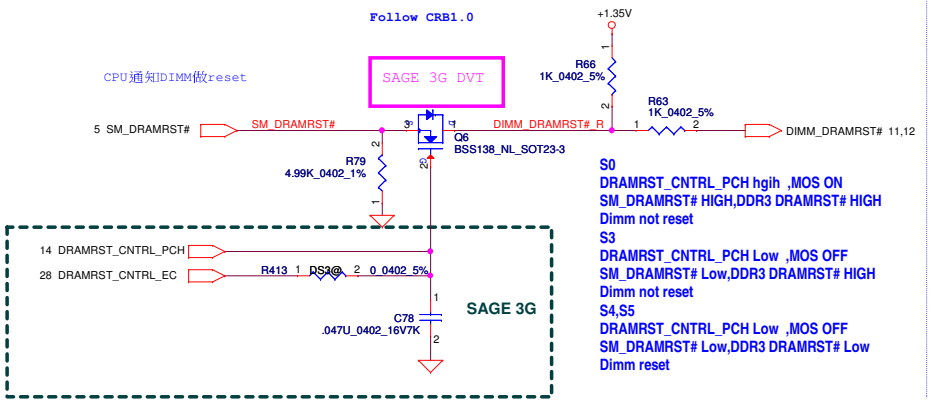




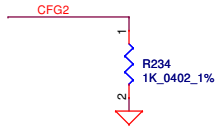
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

Compal Electronics, Inc.			
Title	PROCESSOR(3/7) DDRIII		
Size: Custom	Document Number: V1JB1 M/B LA-A041P Schematic		Rev: 0.1
Date: Wednesday, March 13, 2013	Sheet 6 of 52		

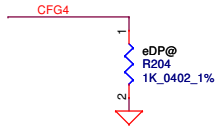
Default "1",EDS R1.0 P.88

CFG Straps for Processor

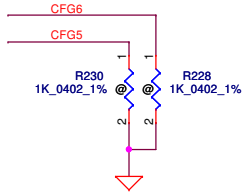
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



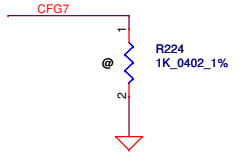
eDP enable	
CFG4	* 1:Disable 0:Enable

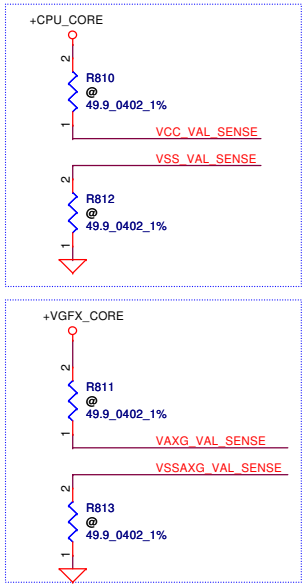


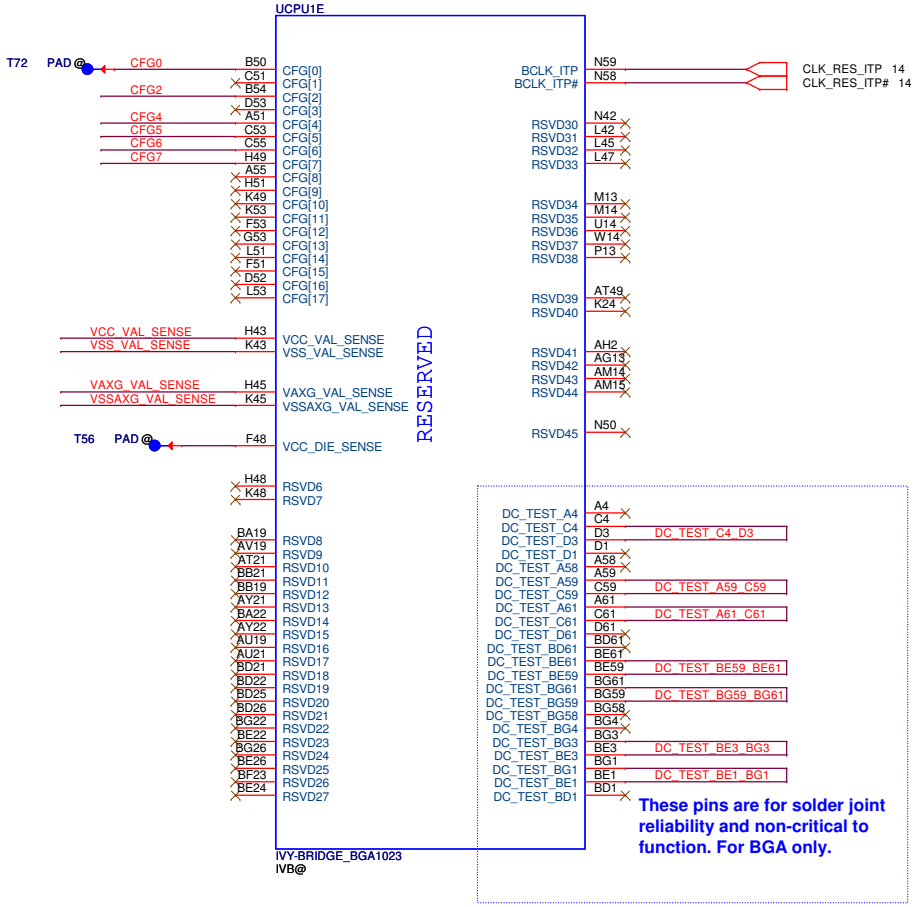
PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) 1x16 PCI Express 10: 2x8 PCI Express 01: Reserved 00: 1x8,2x4 PCI Express



PEG DEFER TRAINING	CRB1.0 P.12
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training







These pins are for solder joint reliability and non-critical to function. For BGA only.

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

Size	Document Number	Rev
Custom	V1JB1 M/B LA-A041P Schematic	0.1

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POWER

INTEL Recommend VCC
3*330uF,12*22uF(0805),16*2.2uF(0402)
PD0.9

UCPU1F

ULV SC/DC 33A

8.5A

+CPU_CORE

VCC[1] A26, VCC[2] A29, VCC[3] A31, VCC[4] A34, VCC[5] A35, VCC[6] A38, VCC[7] A39, VCC[8] A42, VCC[9] C26, VCC[10] C27, VCC[11] C32, VCC[12] C34, VCC[13] C37, VCC[14] C39, VCC[15] C42, VCC[16] D27, VCC[17] D32, VCC[18] D34, VCC[19] D37, VCC[20] D39, VCC[21] D42, VCC[22] E26, VCC[23] E28, VCC[24] E32, VCC[25] E34, VCC[26] E37, VCC[27] E38, VCC[28] F25, VCC[29] F26, VCC[30] F28, VCC[31] F32, VCC[32] F34, VCC[33] F37, VCC[34] F38, VCC[35] F42, VCC[36] G42, VCC[37] H25, VCC[38] H26, VCC[39] H28, VCC[40] H29, VCC[41] H32, VCC[42] H34, VCC[43] H35, VCC[44] H37, VCC[45] H38, VCC[46] H40, VCC[47] J25, VCC[48] J26, VCC[49] J28, VCC[50] J29, VCC[51] J32, VCC[52] J34, VCC[53] J35, VCC[54] J37, VCC[55] J38, VCC[56] J40, VCC[57] J42, VCC[58] K26, VCC[59] K27, VCC[60] K29, VCC[61] K32, VCC[62] K34, VCC[63] K35, VCC[64] K37, VCC[66] K39, VCC[67] K42, VCC[68] L25, VCC[69] L28, VCC[70] L33, VCC[71] L36, VCC[72] L40, VCC[73] N26, VCC[74] N30, VCC[75] N34, VCC[76] N38

CORE SUPPLY

PEG IO AND DDR IO

+1.05VS_VTT

VCCIO[1] AF46, VCCIO[3] AG48, VCCIO[4] AG50, VCCIO[5] AG51, VCCIO[6] AJ17, VCCIO[7] AJ21, VCCIO[8] AJ25, VCCIO[9] AJ43, VCCIO[10] AJ47, VCCIO[11] AK50, VCCIO[12] AK51, VCCIO[13] AL14, VCCIO[14] AL15, VCCIO[15] AL16, VCCIO[16] AL20, VCCIO[17] AL22, VCCIO[18] AL26, VCCIO[19] AL45, VCCIO[20] AL48, VCCIO[21] AM16, VCCIO[22] AM17, VCCIO[23] AM21, VCCIO[24] AM43, VCCIO[25] AM47, VCCIO[26] AN20, VCCIO[27] AN42, VCCIO[28] AN45, VCCIO[29] AN48

INTEL Recommend VCCIO
PD 0.9

330uF 1+1
10uF (0603) *5
1uF (0201) *16

+1.05VS_VTT

VCCIO[30] AA14, VCCIO[31] AA15, VCCIO[32] AB17, VCCIO[33] AB20, VCCIO[34] AC13, VCCIO[35] AD16, VCCIO[36] AD18, VCCIO[37] AD21, VCCIO[38] AE14, VCCIO[39] AE15, VCCIO[40] AF16, VCCIO[41] AF18, VCCIO[42] AF20, VCCIO[43] AG15, VCCIO[44] AG16, VCCIO[45] AG17, VCCIO[46] AG20, VCCIO[47] AG21, VCCIO[48] AJ14, VCCIO[49] AJ15

330uF 1
10uF (0603) *5
1uF (0201) *10

+1.05VS_VTT

VCCIO50 W16, VCCIO51 W17

+3VALW

R521 10K_0402_5%

VCCIO_SEL

R520 10K_0402_5% @

VCCIO_SEL For 2012 CPU support		
A19	*	1 : +1.05VS_VTT 0: +1.05VS_VTT

VCCIO_SEL

BC22 VCCIO_SEL_R R582 @ 0_0402_5%

QUIET RAILS

+1.05VS_VTT

VCCPQE[1] AM25, VCCPQE[2] AN22

SAGE 3G

C951 1U_0402_6.3V6K

+1.05VS_VTT

R574 130_0402_5%

SVID

VIDALERT# A44 H_CPU_SVIDALRT# R576 43_0402_1%
VIDSCLK B43 H_CPU_SVIDCLK R577 @ 0_0402_5%
VIDSOUT C44 H_CPU_SVIDDAT R578 @ 0_0402_5%

VR_SVID_ALRT# 42
VR_SVID_CLK 42
VR_SVID_DAT 42

Check List R1.5
VIDALERT#:75ohm ±5% pull-up to VCCIO close to IMVP7
VIDSCLK: 55ohm ±5% pull-up to VCCIO close to IMVP7
VIDSOUT: 130ohm ±5% pull-up to VCCIO close to CPU
130ohm ±5% pull-up to VCCIO close to IMVP7

SENSE LINES

+CPU_CORE

Place the PU,PD
resistors close to CPU

R588 100_0402_1%

VCC_SENSE F43 VCCSENSE_R R579 @ 0_0402_5%
VSS_SENSE G43 VSSSENSE_R R581 @ 0_0402_5%

VCCSENSE 42
VSSSENSE 42

+1.05VS_VTT

R107 10_0402_5%

VCCIO_SENSE AN16 VCCIO_SENSE
VSS_SENSE_VCCIO AN17 VSSIO_SENSE

VCCIO_SENSE 40

R589 100_0402_1%

R105 10_0402_5%

Check List R1.5
VCCSENSE:100ohm ±1% pull-up to VCC near processor.
VSSSENSE:100ohm ±1% pull-down to GND near processor.

Should change to connect from power cirucit & layout differential with VCCIO_SENSE.

IVY-BRIDGE_BGA1023
IVB@

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: ***PROCESSOR(5/7) PWR,BYPASS***

Size: Custom | Document Number: *V1JB1 M/B LA-A041P Schematic* | Rev: 0.1

Date: Wednesday, March 13, 2013 | Sheet 8 of 52

POWER

ULV SC/DC GT1: 18A
GT2: 33A

INTEL Recommend VAXG
2*330uF,5*22uF(0805),6*10uF(0603),6*1uF(0402)
PD 0.9

UCPU1G

+VGFX_CORE

VAXG[1] AA46
VAXG[2] AB47
VAXG[3] AB50
VAXG[4] AB51
VAXG[5] AB52
VAXG[6] AB53
VAXG[7] AB55
VAXG[8] AB56
VAXG[9] AB58
VAXG[10] AB59
VAXG[11] AC61
VAXG[12] AD47
VAXG[13] AD48
VAXG[14] AD50
VAXG[15] AD51
VAXG[16] AD52
VAXG[17] AD53
VAXG[18] AD55
VAXG[19] AD56
VAXG[20] AD58
VAXG[21] AD59
VAXG[22] AE46
VAXG[23] N45
VAXG[24] P47
VAXG[25] P48
VAXG[26] P50
VAXG[27] P51
VAXG[28] P52
VAXG[29] P53
VAXG[30] P55
VAXG[31] P56
VAXG[32] P61
VAXG[33] T48
VAXG[34] T58
VAXG[35] T59
VAXG[36] T61
VAXG[37] U46
VAXG[38] V47
VAXG[39] V48
VAXG[40] V50
VAXG[41] V51
VAXG[42] V52
VAXG[43] V53
VAXG[44] V55
VAXG[45] V56
VAXG[46] V58
VAXG[47] V59
VAXG[48] W50
VAXG[49] W51
VAXG[50] W52
VAXG[51] W53
VAXG[52] W55
VAXG[53] W56
VAXG[54] W61
VAXG[55] Y48
VAXG[56] Y61

GRAPHICS

Check List R1.5
VCCAXG_SENSE:100ohm ±5% pull-up to VCC near processor.
VSSAXG_SENSE:100ohm ±5% pull-down to GND near processor.

INTEL Recommend VCCPLL
1*330uF,2*1uF(0402)
PD 0.9

+VGFX_CORE
R381 100_0402_5%
42 VCC_AXG_SENSE
42 VSS_AXG_SENSE
VAXG_SENSE F45
VSSAXG_SENSE G45
R396 100_0402_5%

SENSE LINES

+1.8VS
J16 JUMP_43X39
SAGE 3G
+1.35VS
R500 0_0805_5%
C606 220U_B2_2.5VM_R15M SGA00004I00
+1.8VS_VCCPLL
1.2A
C583 1U_0402_6.3V6K
C584 1U_0402_6.3V6K
BB3 VCCPLL[1]
BC1 VCCPLL[2]
BC4 VCCPLL[3]

1.8V RAIL

INTEL Recommend VCCSA
1*330uF,5*10uF(0603) ,5*1uF(0402)
PD0.9

+VCCSA
C607 330U_B2_2VM_R15M SGA00004700
SAGE 3G
C1181 1U_0402_6.3V6K
C1180 1U_0402_6.3V6K
C1179 1U_0402_6.3V6K
6A
L17 VCCSA[1]
L21 VCCSA[2]
N16 VCCSA[3]
N20 VCCSA[4]
N22 VCCSA[5]
P17 VCCSA[6]
P20 VCCSA[7]
R16 VCCSA[8]
R18 VCCSA[9]
R21 VCCSA[10]
U15 VCCSA[11]
V16 VCCSA[12]
V17 VCCSA[13]
V18 VCCSA[14]
V21 VCCSA[15]
W20 VCCSA[16]
C995 10U_0603_6.3V6M
C996 10U_0603_6.3V6M
C997 10U_0603_6.3V6M

SA RAIL

IVY-BRIDGE_BGA1023
IVB@

SA_DIMM_VREFDQ
SB_DIMM_VREFDQ
For Future CPU M3 support,
Sandey bridge not support M3,
Check list1.0 & CRB say can NC

VREF

SM_VREF AY43
+V_SM_VREF
BE7 SA_DIMM_VREFDQ
BG7 SB_DIMM_VREFDQ
R69 1K_0402_1%
R68 1K_0402_1%
SAGE 3G

+V_SM_VREF should have 20 mil trace width

+1.35VS
R534 1K_0402_1%
R540 1K_0402_1%
C647 0.1U_0402_16V4Z

DDR3 - 1.5V RAILS

5A
VDDQ[1] AJ28
VDDQ[2] AJ33
VDDQ[3] AJ36
VDDQ[4] AJ40
VDDQ[5] AL30
VDDQ[6] AL34
VDDQ[7] AL38
VDDQ[8] AL42
VDDQ[9] AM33
VDDQ[10] AM36
VDDQ[11] AM40
VDDQ[12] AN30
VDDQ[13] AN34
VDDQ[14] AN38
VDDQ[15] AR26
VDDQ[16] AR28
VDDQ[17] AR30
VDDQ[18] AR32
VDDQ[19] AR34
VDDQ[20] AR36
VDDQ[21] AR40
VDDQ[22] AV41
VDDQ[23] AW26
VDDQ[24] BA40
VDDQ[25] BB28
VDDQ[26] BG33

INTEL Recommend VDDQ
1*330uF,8*10uF(0603) ,10*1uF(0402)
PD0.9

Short for +1.35VS to +1.35V_CPU_VDDQ

+1.35VS
C977 1U_0402_6.3V6K
C978 1U_0402_6.3V6K
C979 1U_0402_6.3V6K
SAGE 3G
C599 330U_B2_2VM_R15M SGA00004700
C999 10U_0603_6.3V6M
C998 10U_0603_6.3V6M
C990 10U_0603_6.3V6M
C989 10U_0603_6.3V6M
C987 10U_0603_6.3V6M
C970 10U_0603_6.3V6M
Place BOT OUT Conn

QUIET RAILS

VCCDQ[1] AM28
VCCDQ[2] AN26
+1.35VS
C985 1U_0402_6.3V6K
SAGE 3G

SENSE LINES

VDDQ_SENSE BC43
VSS_SENSE_VDDQ BA43

SENSE LINES

VCCSA_SENSE U10
CPU EDS1.3 P.93
VCCSA_VID0 Must PD
SAGE 3G
T55 PAD

VCCSA VID lines

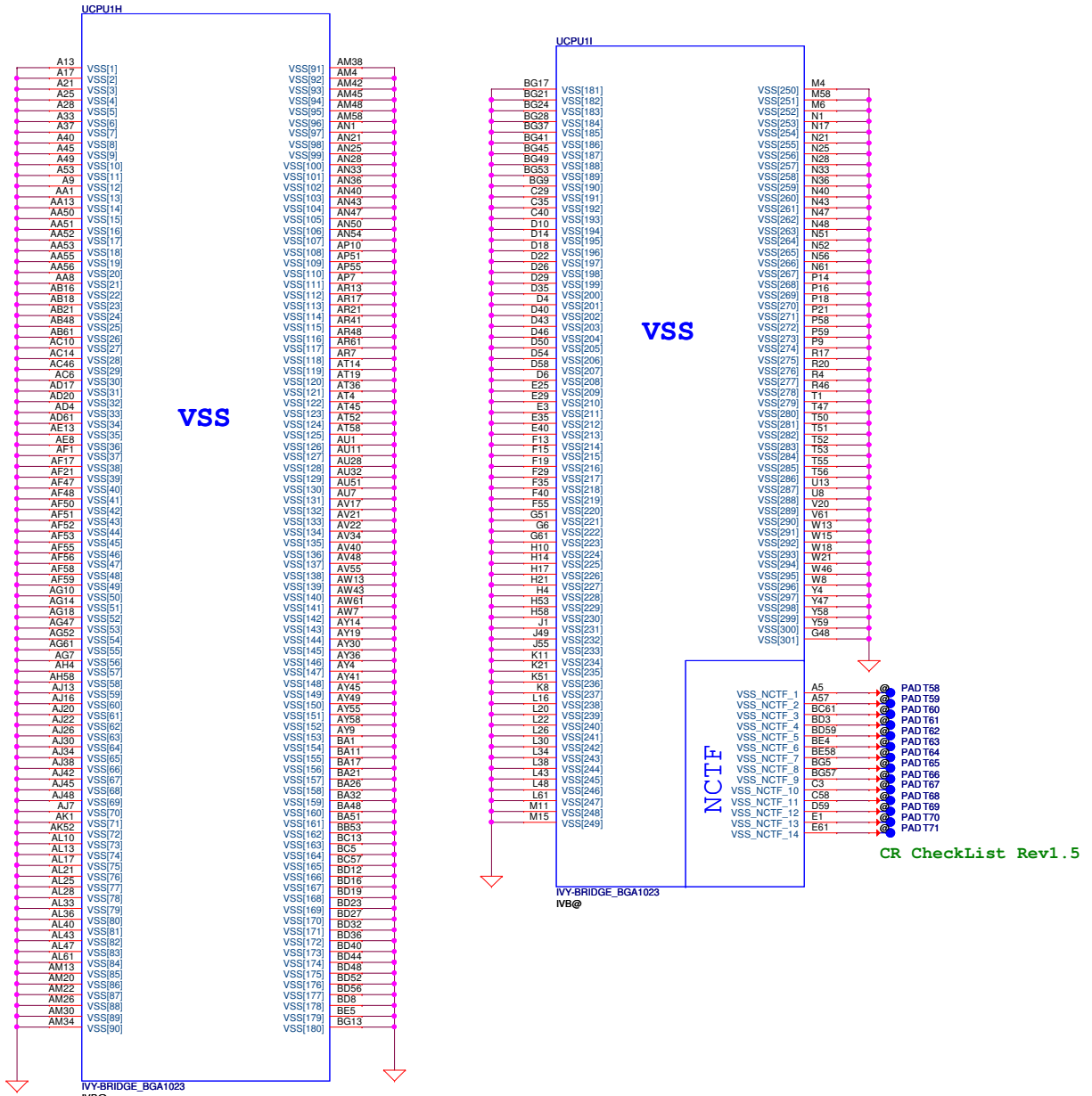
VCCSA_VID[0] D48
VCCSA_VID[1] D49
H_VCCSA_VID0
H_VCCSA_VID1
H_VCCSA_VID0 41
H_VCCSA_VID1 41
R129 0_0402_5%

VCCSA_VID
For 2012 future CPU
VCCSA voltage select

VCCSA					
VID0	VID1	Vout	SNB	IVB	ULV
0	0	0.9V	V	V	V
0	1	0.8V	V	V	
		0.85V			V
1	0	0.725V	X	V	V
1	1	0.675V	X	V	V

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

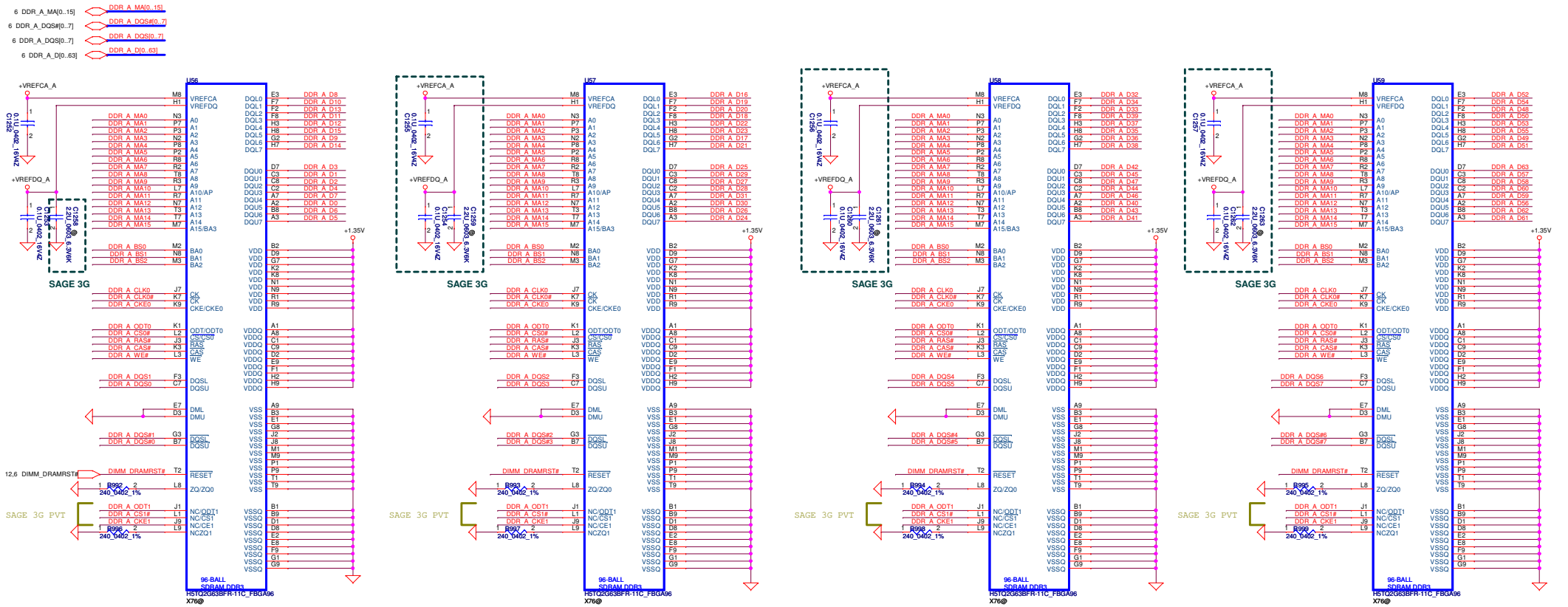
Compal Electronics, Inc.
Title: PROCESSOR(6/7) PWR
Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1
Date: Wednesday, March 13, 2013 | Sheet 9 of 52

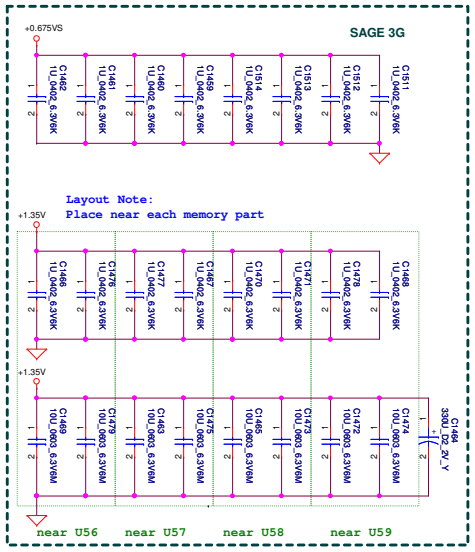


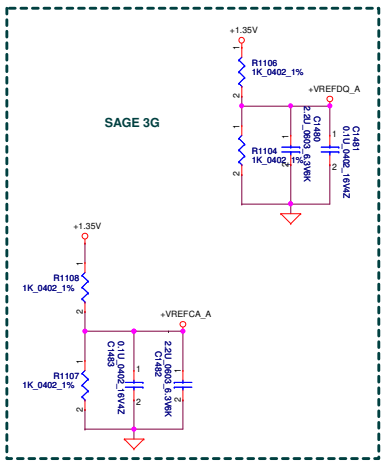
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

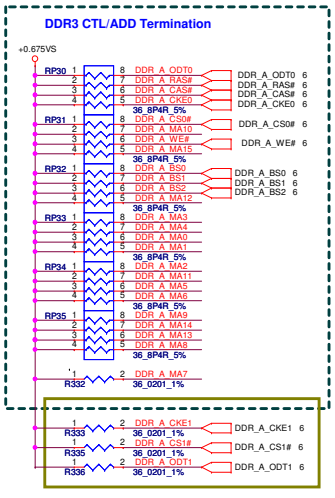
Compal Electronics, Inc.		
Title: PROCESSOR(7/7) VSS		
Size: Custom	Document Number: V1JB1 M/B LA-A041P Schematic	Rev: 0.1
Date: Wednesday, March 13, 2013	Sheet 10 of 52	

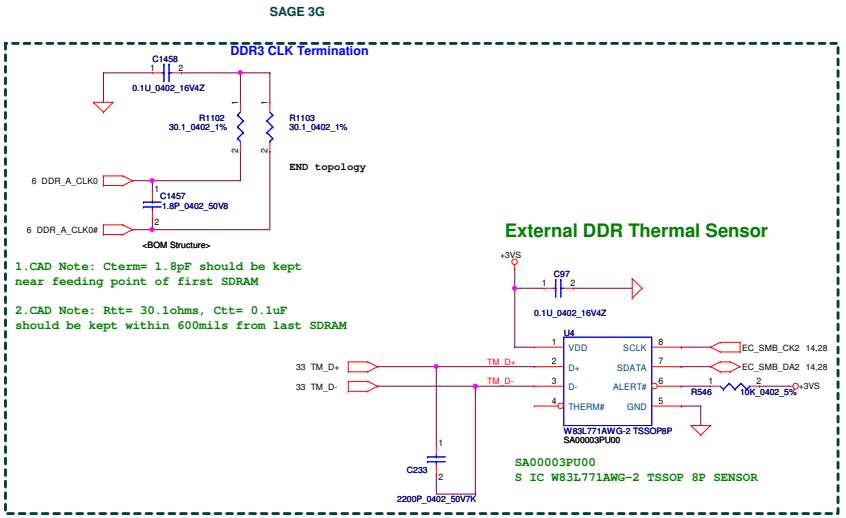
Channel A







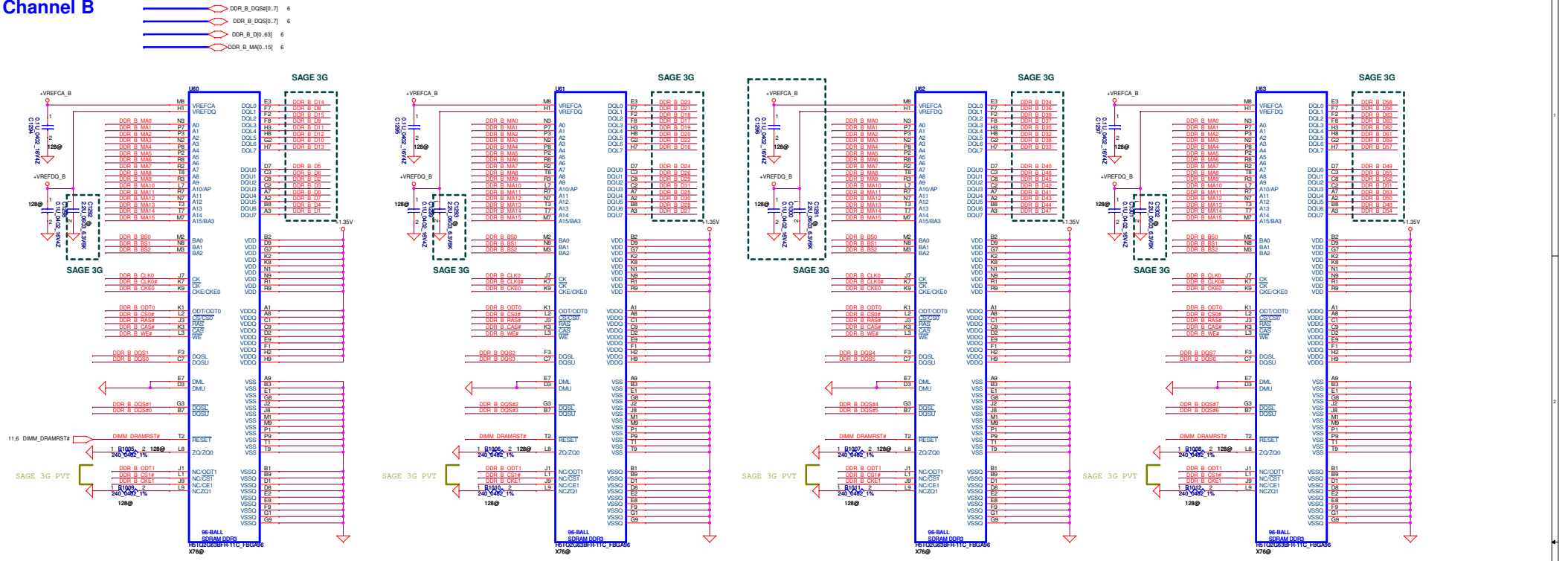


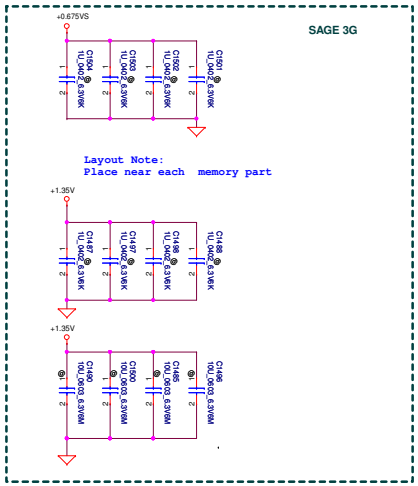


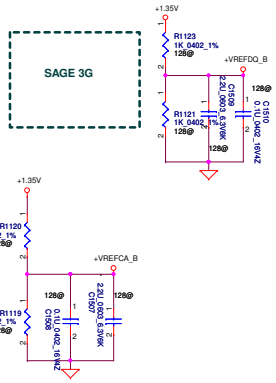
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date 2012/07/12	Title DDRIII DIMMA

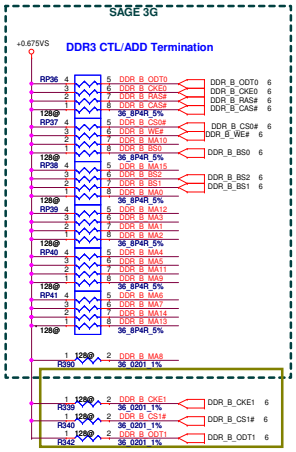
Size Custom	Document Number V1JB1 M/B LA-A041P Schematic		Rev 0.1
Date: Wednesday, March 13, 2013	Sheet 11 of 52		

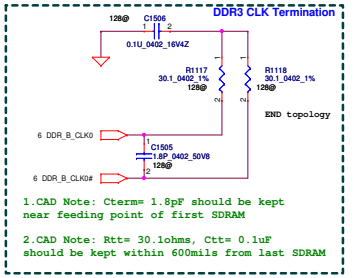
Channel B





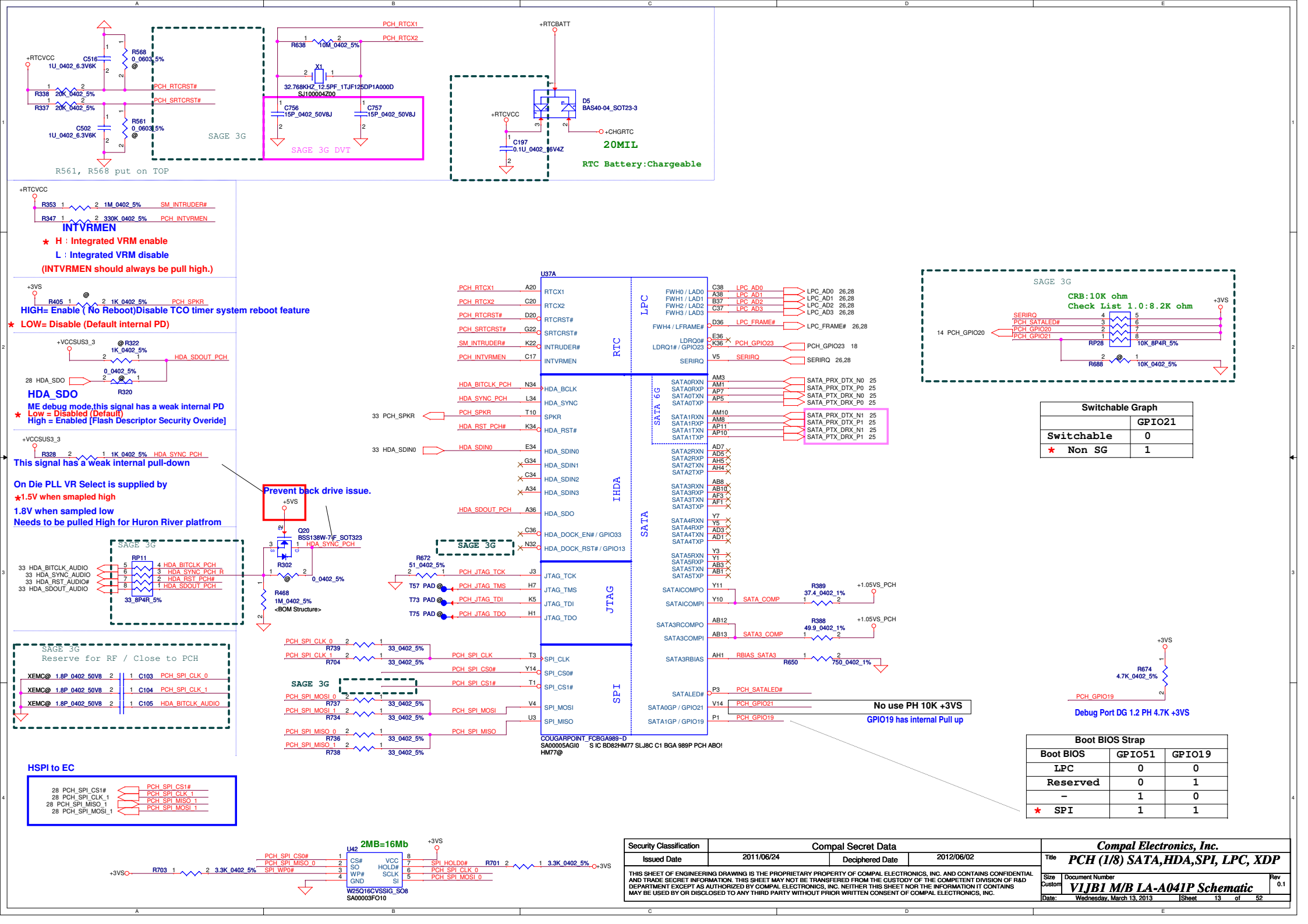






Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date 2012/06/02	Title DDRIII DIMMB

Size Custom	Document Number VIJB1 M/B LA-A041P Schematic		Rev 0.1
Date: Wednesday, March 13, 2013	Sheet 12 of 52		



Switchable Graph	
	GPIO21
Switchable	0
★ Non SG	1

Boot BIOS Strap		
Boot BIOS	GPIO51	GPIO19
LPC	0	0
Reserved	0	1
-	1	0
★ SPI	1	1

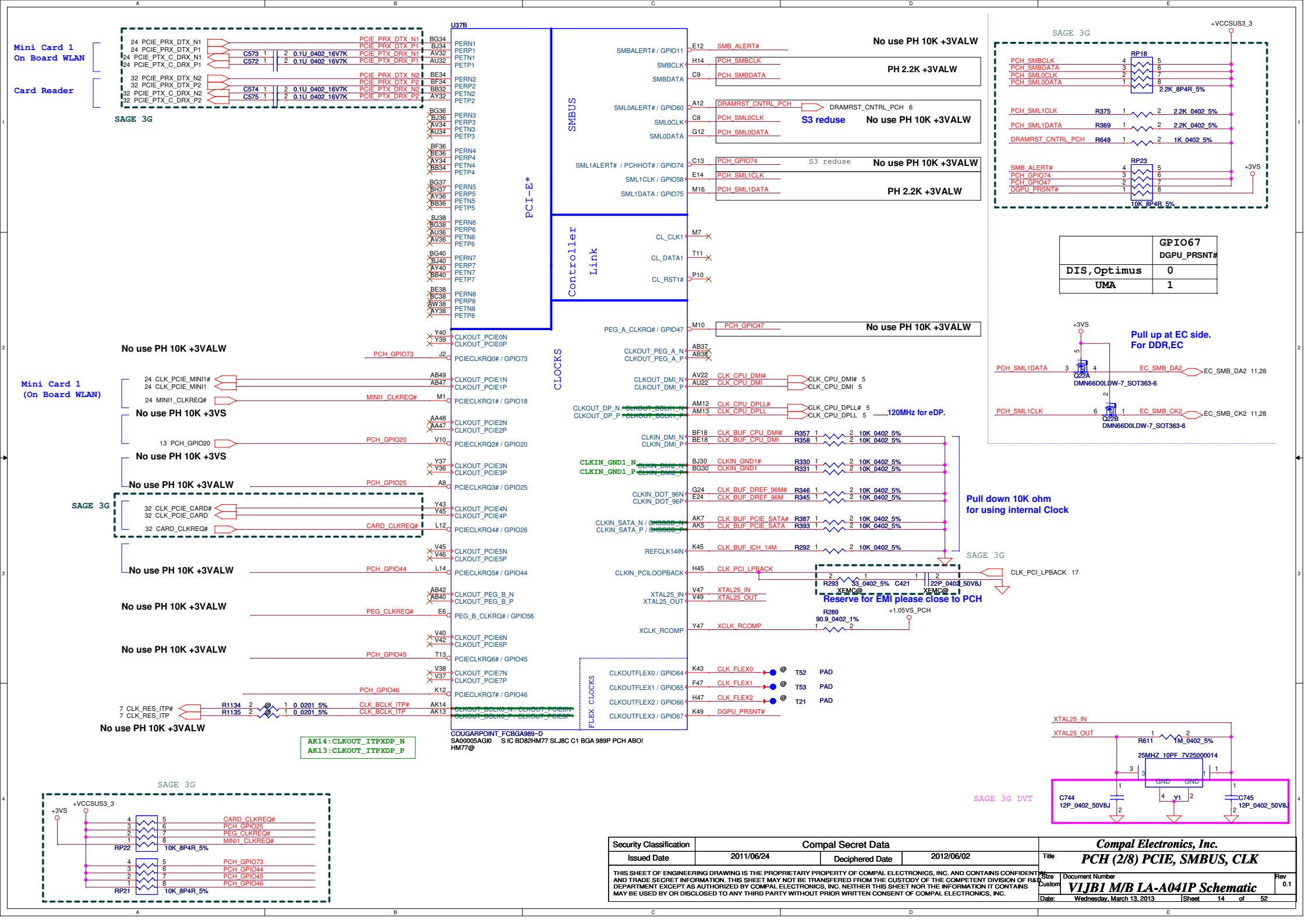
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: PCH (1/8) SATA,HDA,SPI, LPC, XDP

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

Date: Wednesday, March 13, 2013 | Sheet 13 of 52



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

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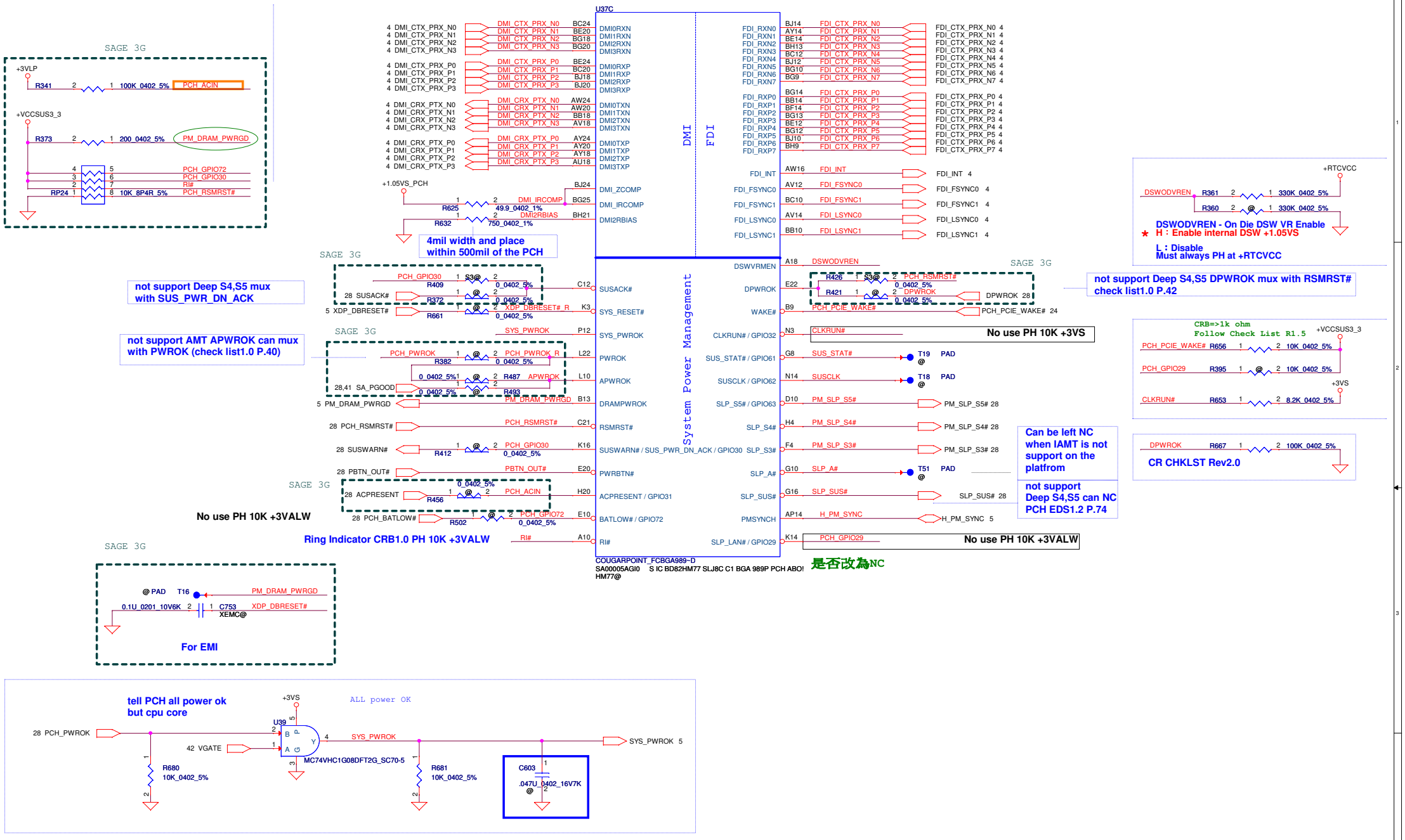
Compal Electronics, Inc.

Title: PCH (2/8) PCIE, SMBUS, CLK

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

Date: Wednesday, March 13, 2013 | Sheet 14 of 52



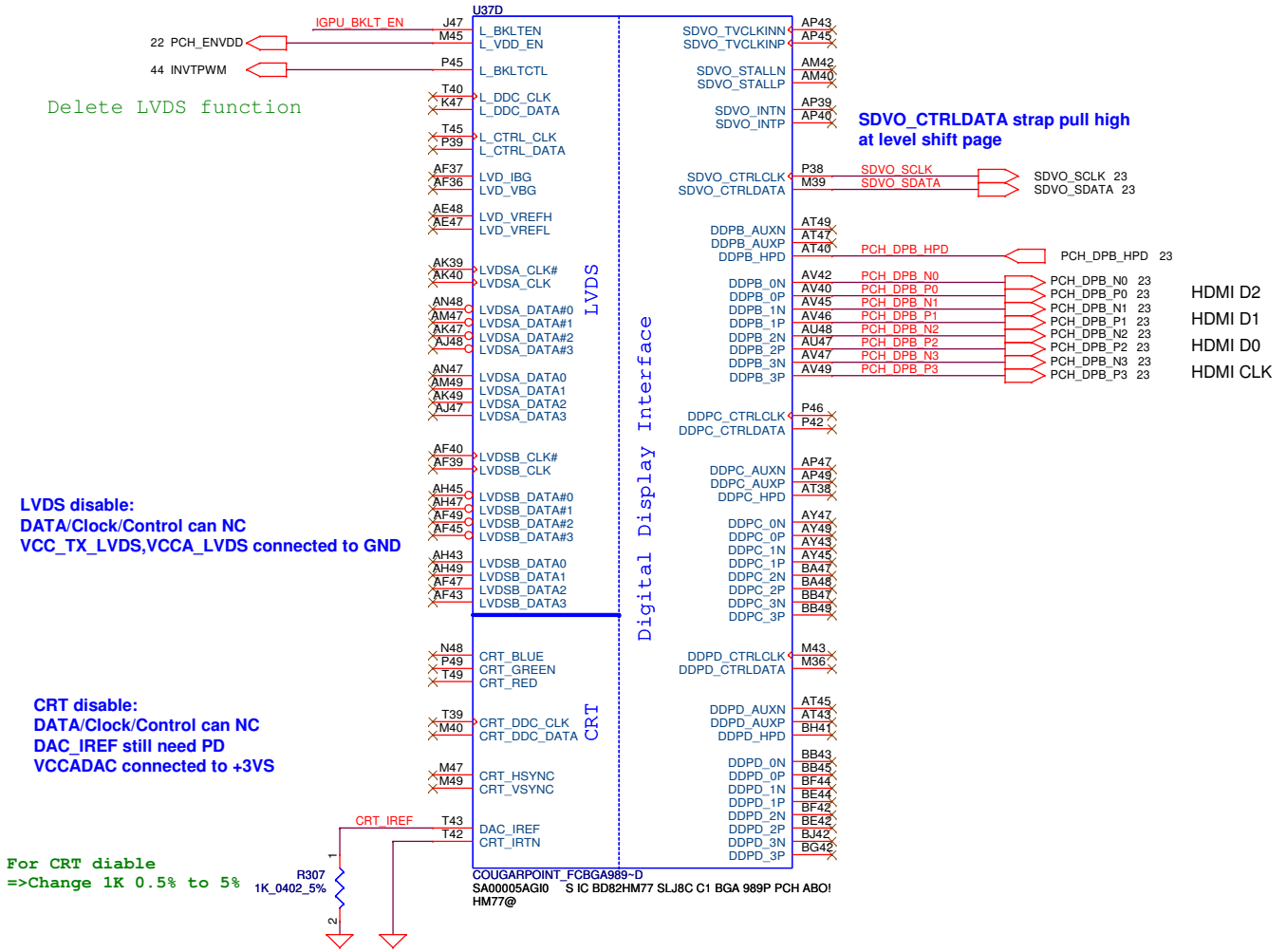
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date 2012/06/02	Title PCH (3/8) DMI,FDI,PM

Size Custom	Document Number V1JB1 M/B LA-A041P Schematic		Rev 0.1
Date: Wednesday, March 13, 2013	Sheet 15 of 52		

UMA Panel Backlight ON/OFF

28 ENBKL — ENBKL — R612 2 @ 1 0_0402_5% — IGPU_BKLT_EN

PD 100K at EC side



Delete LVDS function

SDVO_CTRLDATA strap pull high at level shift page

LVDS disable:
DATA/Clock/Control can NC
VCC_TX_LVDS,VCCA_LVDS connected to GND

CRT disable:
DATA/Clock/Control can NC
DAC_IREF still need PD
VCCADAC connected to +3VS

For CRT diable
=>Change 1K 0.5% to 5%

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: PCH (4/9) LVDS,CRT,DP,HDMI

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

Date: Wednesday, March 13, 2013 | Sheet 16 of 52

SAGE 3G

RP8
PCI_PIRQC#
PCI_PIRQB#
PCI_PIRQA#
PCI_PIRQD#
10K_8P4R_5%

RP9
PCH_GPIO55
PCH_GPIO53
PCH_GPIO52
PCH_GPIO5
10K_8P4R_5%

RP12
PCH_GPIO51
PCH_GPIO2
ODD_DA#
PCH_GPIO4
10K_8P4R_5%

+3VS
R267 10K_0402_5% DGPU_PWR_EN
接至+3VS還是GND
R310 8.2K_0402_5% DGPU_HOLD_RST#

Boot BIOS Strap			
	GPIO19 Bit11	GPIO51 Bit10	Boot BIOS Destination
GNT1#/ GPIO51	0	1	Reserved
	1	0	PCI
Internal PH	1	1	SPI *
	0	0	LPC

只剩GPIO的功能沒有strap function
不做GPIO要PH +3VS,如做GPIO PH +3VS

Only GPIO function

只剩GPIO的功能沒有strap function
無須PH(Internal PH),如做GPIO PH +3VS

SAGE 3G
Reserve for RF / Close to PCH
XEMC@ 1.8P_0402_50V8 C106 CLK_PCI_LPBACK
XEMC@ 1.8P_0402_50V8 C107 CLK_PCI_LPC
XEMC@ 1.8P_0402_50V8 C108 CLK_PCI_TXM
RP43 22_8P4R_5%
14 CLK_PCI_LPBACK
28 CLK_PCI_LPC
26 CLK_PCI_TXM
CLK_PCI_LPBACK
CLK_PCI_LPC
CLK_PCI_TXM
CLK_PCI0 H49
CLK_PCI1 H43
CLK_PCI2 J48
CLK_PCI3 K42
CLK_PCI4 H40
PAD T7 @
PAD T8 @
SAGE 3G R10

SAGE 3G
PLT_RST# 1 2 C1214 1U_0402_6.3V6K

+3VS
U26
PLT_RST#
28 IRST_RST#
SAGE 3G
MC74VHC1G08DFT2G_SC70-5
R376 100K_0402_5%
PLT_RST_BUF# 24

Sideband signal for Touch screen
22 TS_INT# R463 @ 0_0402_5% PCH_GPIO4

U37E

RSVD
BG26 BJ26 BH25 BJ16 BG16 AH38 AH37 AK43 AK45 C18 N30 H3 AH12 AM4 AM5 Y13 K24 L24 AB46 AB45
TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9 TP10 TP11 TP12 TP13 TP14 TP15 TP16 TP17 TP18 TP19 TP20
B21 M20 AY16 BG46
TP21 TP22 TP23 TP24

NVRAM
NV_CE#0 NV_CE#1 NV_CE#2 NV_CE#3
NV_DQS0 NV_DQS1
NV_DQ0 / NV_IO0 ... NV_DQ15 / NV_IO15
NV_ALE NV_CLE
NV_RCOMP
NV_RB#
NV_RE#_WRB0 NV_RE#_WRB1
NV_WE#_CK0 NV_WE#_CK1
AY7 AV7 AU3 BG4 AT10 BC8 AU2 AT4 AT3 AT1 AV3 AT5 AV3 AV1 BB1 BA3 BB5 BB3 BB7 BE8 BD4 BF6 AV5 AY1 AV10 AT8 AY5 BA2 AT12 BF3

Ball AY1 : DF_TVS
DF_TVS
R654 1K_0402_5%
+1.8VS
R651 2.2K_0402_5%
H_SNB_IVB# 5
CLOSE TO THE BRANCHING POINT

DMI,FDI Termination Voltage	
DF_TVS	Set to Vcc when HIGH
	Set to Vss when LOW

DG1.2 CRB1.0 PH 2.2K series 1K
For 2012 support

USB3.0
27 PCH_USB3_RX2_N → PCH_USB3_RX2_N
27 PCH_USB3_RX2_P → PCH_USB3_RX2_P
27 PCH_USB3_TX2_N → PCH_USB3_TX2_N
27 PCH_USB3_TX2_P → PCH_USB3_TX2_P
BE28 BC30 BE32 BJ32 BC28 BE30 BF32 BG32 AV26 BB26 AU28 AY30 AU26 AY26 AV28 AW30
TP25 TP26 TP27 TP28 TP29 TP30 TP31 TP32 TP33 TP34 TP35 TP36 TP37 TP38 TP39 TP40
BE28:USB3Rn1 BC30:USB3Rn2 BE32:USB3Rn3 BJ32:USB3Rn4 BC28:USB3Rp1 BE30:USB3Rp2 BF32:USB3Rp3 BG32:USB3Rp4 AV26:USB3Tn1 BB26:USB3Tn2 AU28:USB3Tn3 AY30:USB3Tn4 AU26:USB3Tp1 AY26:USB3Tp2 AV28:USB3Tp3 AW30:USB3Tp4

PCI Interrupt Requests
PCI_PIRQA# K40 PIRQA#
PCI_PIRQB# K38 PIRQB#
PCI_PIRQC# H38 PIRQC#
PCI_PIRQD# G38 PIRQD#

PCI
DGPU_HOLD_RST# C46 REQ1# / GPIO50
PCH_GPIO52 C44 REQ2# / GPIO52
DGPU_PWR_EN E40 REQ3# / GPIO54
PCH_GPIO51 D47 GNT1# / GPIO51
PCH_GPIO53 E42 GNT2# / GPIO53
PCH_GPIO55 F46 GNT3# / GPIO55
PCH_GPIO2 G42 PIRQE# / GPIO2
ODD_DA# G40 PIRQF# / GPIO3
PCH_GPIO4 C42 PIRQG# / GPIO4
PCH_GPIO5 D44 PIRQH# / GPIO5
PAD T13 @ K10 PME#
26,28,31,32,5 PLT_RST# C6 PLTRST#
CLKOUT_PCI0 H49
CLKOUT_PCI1 H43
CLKOUT_PCI2 J48
CLKOUT_PCI3 K42
CLKOUT_PCI4 H40

USB
USBP0N C24 USB20_N0
USBP0P A24 USB20_P0
USBP1N C25 USB20_N1_R R713 0_0402_5% USB20_N1
USBP1P B25 USB20_P1_R R710 0_0402_5% USB20_P1
USBP2N C26 USB20_N2
USBP2P A26 USB20_P2
USBP3N K28 USB20_N3
USBP3P H28 USB20_P3
USBP4N E28 USB20_N4
USBP4P D28 USB20_P4
@ T15 PAD
@ T17 PAD
USB20_N0 30
USB20_P0 30
USB20_N1 27
USB20_P1 27
USB20_N2 31
USB20_P2 31
USB20_N3 22
USB20_P3 22
3G
Touch Screen
Sensor Hub
USB Connector
EHCI 1

Some PCH config not support USB port 6 & 7.

USBP5N C28
USBP5P A28
USBP6N C29
USBP6P B29
USBP7N N28
USBP7P M28
USBP8N L30 USB20_N8
USBP8P K30 USB20_P8
USBP9N G30 USB20_N9 R714 0_0402_5% USB20_N1
USBP9P E30 USB20_P9 R715 0_0402_5% USB20_P1
USBP10N C30 USB20_N10
USBP10P A30 USB20_P10
USBP11N L32 USB20_N11
USBP11P K32 USB20_P11
USB20_N8 24
USB20_P8 24
USB20_N10 27
USB20_P10 27
USB20_N11 33
USB20_P11 33
Bluetooth
Debug Port
CMOS Camera
CMOS Camera
EHCI 2

USBP12N E32
USBP12P C32
USBP13N A32
USBRBIAS# C33 USBRBIAS
USBRBIAS B33
R620 22.6_0402_1% Within 500 mils

OC0# / GPIO59 A14 USB_OC0#
OC1# / GPIO40 K20 USB_OC1#
OC2# / GPIO41 B17 USB_OC2#
OC3# / GPIO42 C16 USB_OC3#
OC4# / GPIO43 L16 USB_OC4#
OC5# / GPIO9 A16 USB_OC5#
OC6# / GPIO10 D14 USB_OC6#
OC7# / GPIO14 C14 USB_OC7#
USB_OC0# 27

COUGARPOINT_FCBGA989~D
SA00005AGI0 S IC BD82HM77 SLJ8C C1 BGA 989P PCH ABO!
HM77@

SAGE 3G
RP14
USB_OC0# USB_OC2# USB_OC7# USB_OC5#
+VCCSUS3_3
10K_8P4R_5%

SAGE 3G
RP15
USB_OC1# USB_OC4# USB_OC3# USB_OC6#
+VCCSUS3_3
10K_8P4R_5%

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

Compal Electronics, Inc.
Title: PCH (5/9) PCI, USB, NVRAM
Size: Custom
Document Number: V1JB1 M/B LA-A041P Schematic
Rev: 0.1
Date: Wednesday, March 13, 2013
Sheet 17 of 52

HDA_SYNC PH(PLL =+1.5VS)

GPIO28

On-Die PLL Voltage Regulator

This signal has a weak internal pull up

★ H : On-Die PLL voltage regulator enable

L : On-Die PLL Voltage Regulator disable

+VCCSUS3_3

R422 4.7K_0402_5%

PCH_GPIO28

R417 1K_0402_5%

Debug Port DG 1.2 PH 4.7K +3VALW_PCH

Deep S4,S5 wake event signal

RTC alarm,Power BTN,GPIO27

PCH_GPIO27 (Have internal Pull-High)

SAGE 3G

+3VLP R506 DS3@ 100K_0402_5% R362 @ 10K_0402_5% PCH_GPIO27

R364 10K_0402_5% WWAN_OFF#

SATA2GP/GPIO36,SATA3GP/GPIO37

1.Used as for Mechanical Presence detect -

Use a weak external pull-up (150K-200k Ohms) to Vcc3_3 or use 10K external pull-up that is enabled only after PLTRST# de-assertion.

2.Used as GP Input (Pin HW default) -

Ensure GPI is not driven high during strap sampling window

3.Unused as GPIO or SATA*GP -

Use 8.2K-10K pull-down to ground.

+3VS RP16 10K_8P4R_5%

PCH_GPIO0 PCH_GPIO1 DGPU_HPD_INT# MSATA_DET#

RP17 10K_8P4R_5%

DGPU_PWROK PCH_GPIO34 PCH_GPIO48 PCH_GPIO49

SAGE 3G

+VCCSUS3_3 +3VS R391 1K_0402_5% EC_LID_OUT#

RP29 10K_8P4R_5%

PCH_GPIO12 PCH_GPIO57 EC_KBRST# ODD_DETECT#

GPIO24 Unmultiplexed

NOTE: GPIO24 configuration register bits are not cleared by CF9h reset event.

CRB1.0 PH10K to +3VALW

30 HUB_DFU_EN# R256 0_0402_5% PCH_GPIO68

30 HUB_PWRGATE R249 0_0402_5% PCH_GPIO35

25 RAID0_DET R258 0_0402_5% PCH_GPIO1

SAGE 3G

+3VS @R616 10K_0402_5% PCH_GPIO69

+3VS R617 10K_0402_5% TPM@ PCH_GPIO70

R619 10K_0402_5%

R621 10K_0402_5% WOTPM@

SW base on TPM table to detect HW TPM status

TPM Status	GPIO69	GPIO70
HW, SW without support TPM	0	0
Infineon TPM SLB9655	0	1
x	1	0
x	1	1

U37F

No use PH 10K +3VS	PCH_GPIO0	T7	BMBUSY# / GPIO0	TACH4 / GPIO68	C40 PCH_GPIO68
No use PH 10K +3VS	PCH_GPIO1	A42	TACH1 / GPIO1	TACH5 / GPIO69	B41 PCH_GPIO69
No use PH 10K +3VS	DGPU_HPD_INT#	H36	TACH2 / GPIO6	TACH6 / GPIO70	C41 PCH_GPIO70
28 EC_SCI#	EC_SCI#	E38	TACH3 / GPIO7	TACH7 / GPIO71	A40 PCH_GPIO71 @ T45 PAD
28 EC_SMI#	EC_SMI#	C10	GPIO8		
No use PH +3VALW	PCH_GPIO12	C4	LAN_PHY_PWR_CTRL / GPIO12		
EC LID SW OUT					
No use PH +3VALW	EC_LID_OUT#	G2	GPIO15	A20GATE	P4 GATEA20 28
28 EC_LID_OUT#				PECI	AU16 PCH_PECI_R @ T46 PAD SAGE 3G
No use PH +3VS	MSATA_DET#	U2	SATA4GP / GPIO16	RCIN#	P5 EC_KBRST# EC_KBRST# 28
25 MSATA_DET#				PROCPWRGD	AY11 H_CPUPWRGD 5
	DGPU_PWROK	D40	TACH0 / GPIO17	THRMTRIP#	AY10 PCH_THRMTRIP#_R 1 R385 2 390_0402_5% H_THRMTRIP# H_THRMTRIP# 5
No use PH 10K +3VS	PCH_GPIO22	T5	SCLOCK / GPIO22	INIT3_3V#	T14
CRB1.0 PH 10K +3VALW	PCH_GPIO24	E8	GPIO24 / MEM_LED		
No use PD 10K to GND 28 EC_DS3_WAKE#	PCH_GPIO27	E16	GPIO27		
R595 1 @ 2 0_0402_5%					
No use PH 10K +3VALW	PCH_GPIO28	P8	GPIO28		
No use PH 10K +3VS	PCH_GPIO34	K1	STP_PCI# / GPIO34	NC_1	AH8
No use can NC(+3VS power plane)	PCH_GPIO35	K4	GPIO35	NC_2	AK11
Can't PH	ODD_DETECT#	V8	SATA2GP / GPIO36	NC_3	AH10
Can't PH	WWAN_OFF#	M5	SATA3GP / GPIO37	NC_4	AK10
No use PH 10K +3VS Optimus(L)/ non optimus(H)	OPTIMUS_EN#	N2	SLOAD / GPIO38	NC_5	P37
No use PH 10K +3VS	PCH_GPIO39	M3	SDATAOUT0 / GPIO39		
No use PH 10K +3VS	PCH_GPIO48	V13	SDATAOUT1 / GPIO48	VSS_NCTF_15	BG2
SATA5GP&TEMP_ALERT# CRB PH 10K +3VS	PCH_GPIO49	V3	SATA5GP / GPIO49	VSS_NCTF_16	BG48
No use PH +3VALW	PCH_GPIO57	D6	GPIO57	VSS_NCTF_17	BH3
				VSS_NCTF_18	BH47
				VSS_NCTF_19	BJ4
				VSS_NCTF_20	BJ44
				VSS_NCTF_21	BJ45
				VSS_NCTF_22	BJ46
				VSS_NCTF_23	BJ5
				VSS_NCTF_24	BJ6
				VSS_NCTF_25	C2
				VSS_NCTF_26	C48
				VSS_NCTF_27	D1
				VSS_NCTF_28	D49
				VSS_NCTF_29	E1
				VSS_NCTF_30	E49
				VSS_NCTF_31	F1
				VSS_NCTF_32	F49

GPIO CPU/MISC NCTF

VSS_NCTF_1 A4, VSS_NCTF_2 A44, VSS_NCTF_3 A45, VSS_NCTF_4 A46, VSS_NCTF_5 A5, VSS_NCTF_6 A6, VSS_NCTF_7 B3, VSS_NCTF_8 B47, VSS_NCTF_9 BD1, VSS_NCTF_10 BD49, VSS_NCTF_11 BE1, VSS_NCTF_12 BE49, VSS_NCTF_13 BF1, VSS_NCTF_14 BF49

COUGARPOINT_FCBGA989~D

SA00005AGI0 S IC BD82HM77 SLJ8C C1 BGA 989P PCH ABO!

HM77@

INIT3_3V Check list1.0 P.59

This signal has weak internal PU, can't pull low,leave NC

TS_VSS1~4 PD to GND

PECI CPU-EC

CTRL+ALT+DEL

non CPU power ok

130c shut sown

+3VS PCH_GPIO68 R324 10K_0402_5%

+3VS R419 10K_0402_5%

+3VS UMA@ R429 10K_0402_5% OPTIMUS_EN#

@ R430 10K_0402_5%

	GPIO38 OPTIMUS_EN#
Muxless	0
* nonMuxless	1

Define Q5LJ1(DDR3) or V1JV1(DDR3L)

+VCCSUS3_3 R458 DDR3@ 10K_0402_5% PCH_GPIO24

R457 DDR3L@ 10K_0402_5%

	GPIO24 PCH_GPIO24
* DDR3L(V1JV1)	0
DDR3	1

GPIO36/GPIO37 is Strap functionality

that requires internal pull down to be sampled at rising PWROK.

When uses as SATA2GP/SATA3GP for mechanical presence detect

-use a external pull up 150K-200K ohm to Vcc3_3

When used as GP input

-ensure GPI is not driven high during strap sampling window

When Unused as GPIO or SATA*GP

-use 8.2K-10K pull-down

check list page 47

SA000059110 / ELPIDA DDR3L-1333

SA00005FV10 / HYNIX DDR3L-1333

SA00005HT80 / ELPIDA DDR3L-1600

		GPIO39	GPIO23	GPIO22
DDR3L-1333	Elpida Mono 512MB*4(Ch A)	0	0	0
DDR3L-1333	Hynix Mono 512MB*4(Ch A)	0	0	1
DDR3L-1333	Elpida Mono 512MB*8(Ch A,B)	0	1	0
DDR3L-1333	Hynix Mono 512MB*8(Ch A,B)	0	1	1
DDR3L-1600	Elpida Mono 512MB*4(Ch A)	1	0	0
DDR3L-1600		1	0	1
DDR3L-1600	Elpida Mono 512MB*8(Ch A,B)	1	1	0
DDR3L-1600		1	1	1

+3VS R274 X76@ 10K_0402_5% PCH_GPIO22

R275 X76@ 10K_0402_5%

R278 X76@ 10K_0402_5% PCH_GPIO23 PCH_GPIO23 13

R279 X76@ 10K_0402_5%

R281 X76@ 10K_0402_5% PCH_GPIO39

R282 X76@ 10K_0402_5%

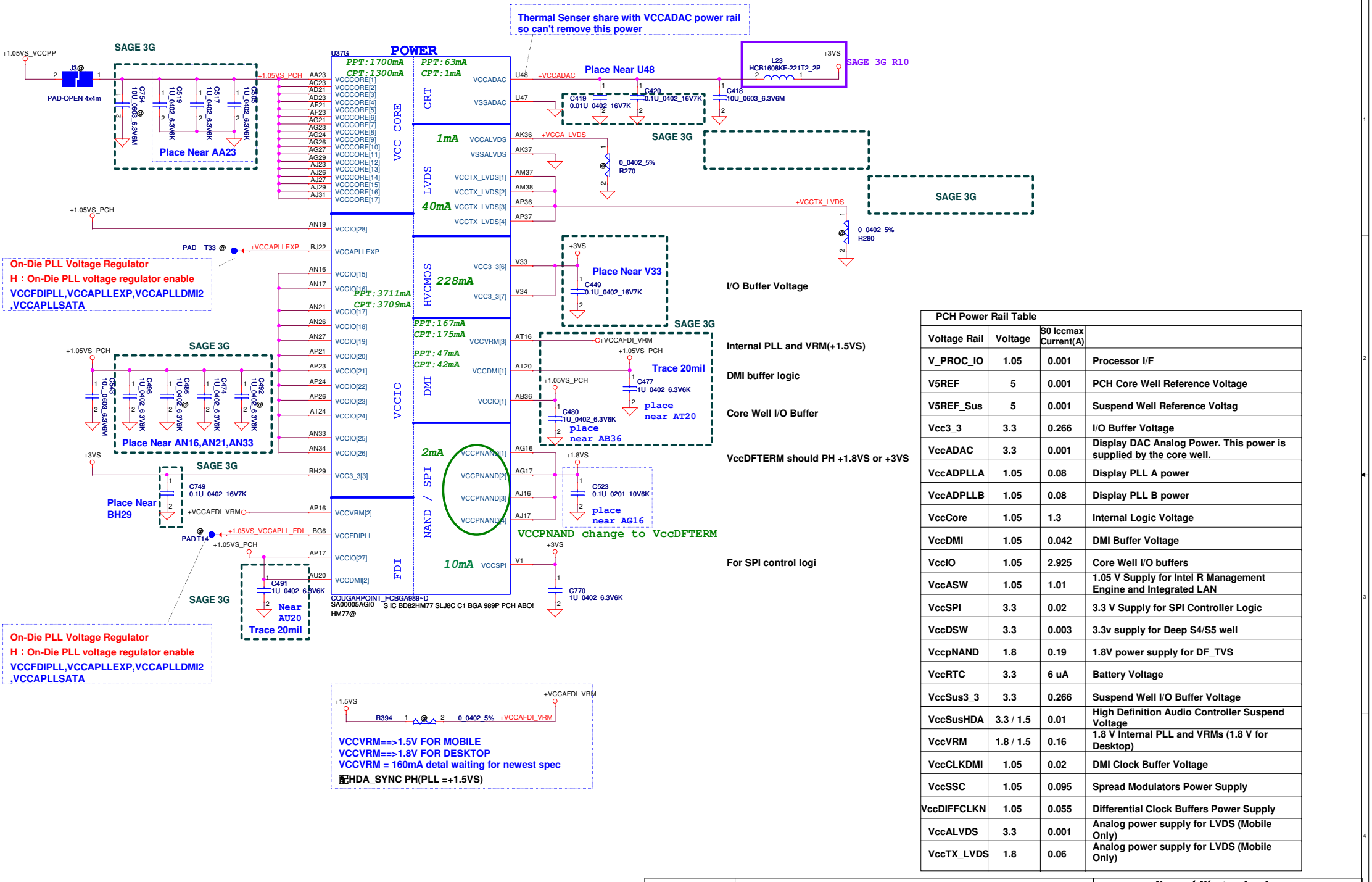
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

Date: Wednesday, March 13, 2013 | Sheet 18 of 52



PCH Power Rail Table			
Voltage Rail	Voltage	S0 Iccmax Current(A)	
V_PROC_IO	1.05	0.001	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltag
Vcc3_3	3.3	0.266	I/O Buffer Voltage
VccADAC	3.3	0.001	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.08	Display PLL A power
VccADPLLB	1.05	0.08	Display PLL B power
VccCore	1.05	1.3	Internal Logic Voltage
VccDMI	1.05	0.042	DMI Buffer Voltage
VccIO	1.05	2.925	Core Well I/O buffers
VccASW	1.05	1.01	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.02	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.19	1.8V power supply for DF_TVS
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.266	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.16	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.02	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.06	Analog power supply for LVDS (Mobile Only)

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date 2012/06/02	Title: PCH (7/9) PWR
Size: Custom	Document Number: V1JB1 M/B LA-A041P Schematic		Rev: 0.1
Date: Tuesday, March 26, 2013	Sheet 19 of 52		

For Deep S3 turn off +V5REF_SUS,+VCCSUS3_3

+1.05V analog internal clock PLL Can NC

Not support Deep S4,S5 connect to +3VALW

suppied by internal 1.05V VR must NC

GPIO28
On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL,VCCAPLLEXP,VCCAPLLDMI2 ,VCCAPLLSATA

suppied by internal 1.05V VR must NC

suppied by internal 1.05V VR Must NC

isolation between SSC (AG33) and DIFFCLKN(AF33,AF34,AG34)
18mil width(DIFFCLKN)
10mil (SSC)

U37J

POWER

VCCACLK
VCCDSW3_3 1mA
DCPSUSBYP
VCC3_3[5]
VCCAPLLDMI2
VCCIO[14]
DCPSUS[3]
VCCASW[1] 903mA
VCCASW[2]
VCCASW[3]
VCCASW[4]
VCCASW[5]
VCCASW[6]
VCCASW[7]
VCCASW[8]
VCCASW[9]
VCCASW[10]
VCCASW[11]
VCCASW[12]
VCCASW[13]
VCCASW[14]
VCCASW[15]
VCCASW[16]
VCCASW[17]
VCCASW[18]
VCCASW[19]
VCCASW[20]
DCPRTC
VCCVRM[4]
VCCADPLLA PPT:80mA CPT:75mA
VCCADPLLB
VCCIO[7]
VCCIO[8]
VCCIO[11] 55mA
VCCIO[10] 95mA
DCPSST
DCPSUS[1]
DCPSUS[2]
V_PROC_IO 1mA
VCCRTC
COUGARPOINT_FCBGA989~D
SA00005AGI0 S IC BD82HM77 SLJ8C C1 BGA 989P PCH ABO!
HM77@

USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
CPU
MISC
RTC
HDA

VCCIO[29]
VCCIO[30]
VCCIO[31]
VCCIO[32]
VCCIO[33]
VCCSUS3_3[7]
VCCSUS3_3[8]
VCCSUS3_3[9]
VCCSUS3_3[10]
VCCSUS3_3[6]
VCCIO[34]
V5REF_SUS 1mA
DCPSUS[4]
VCCSUS3_3[1]
V5REF 1mA
VCCSUS3_3[2]
VCCSUS3_3[3]
VCCSUS3_3[4]
VCCSUS3_3[5]
VCC3_3[1]
VCC3_3[8]
VCC3_3[4]
VCC3_3[2]
VCCIO[5]
VCCIO[12]
VCCIO[13]
VCCIO[6]
VCCAPLLSATA
VCCVRM[1]
VCCIO[2]
VCCIO[3]
VCCIO[4]
VCCASW[22]
VCCASW[23]
VCCASW[21]
VCCSUSHDA 10mA

Deep S3
PPT:126mA
CPT:119mA

SAGE 3G

Near T16
Near T38
Near N26
Near T23
Near P24
Near M26
Near AA19
Near BD47
Near BF47
Near N16
Near N20
Near P34
Near AJ2
Near AA16,W16
Near T34
Near AH13,AH14,AF13
Near AC16
Near V16
Near AF17
Near AF33, AF34,AG34
Near AG33
Near BJ8
Near A22
Near P32

VCCIO[8,9,11] change to VccDIFFCLKN
VCCIO[10] change to VccSSC

(RF requirement)

GPIO28
On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL,VCCAPLLEXP,VCCAPLLDMI2 ,VCCAPLLSATA

Need +3VALW and 0.1U close PCH

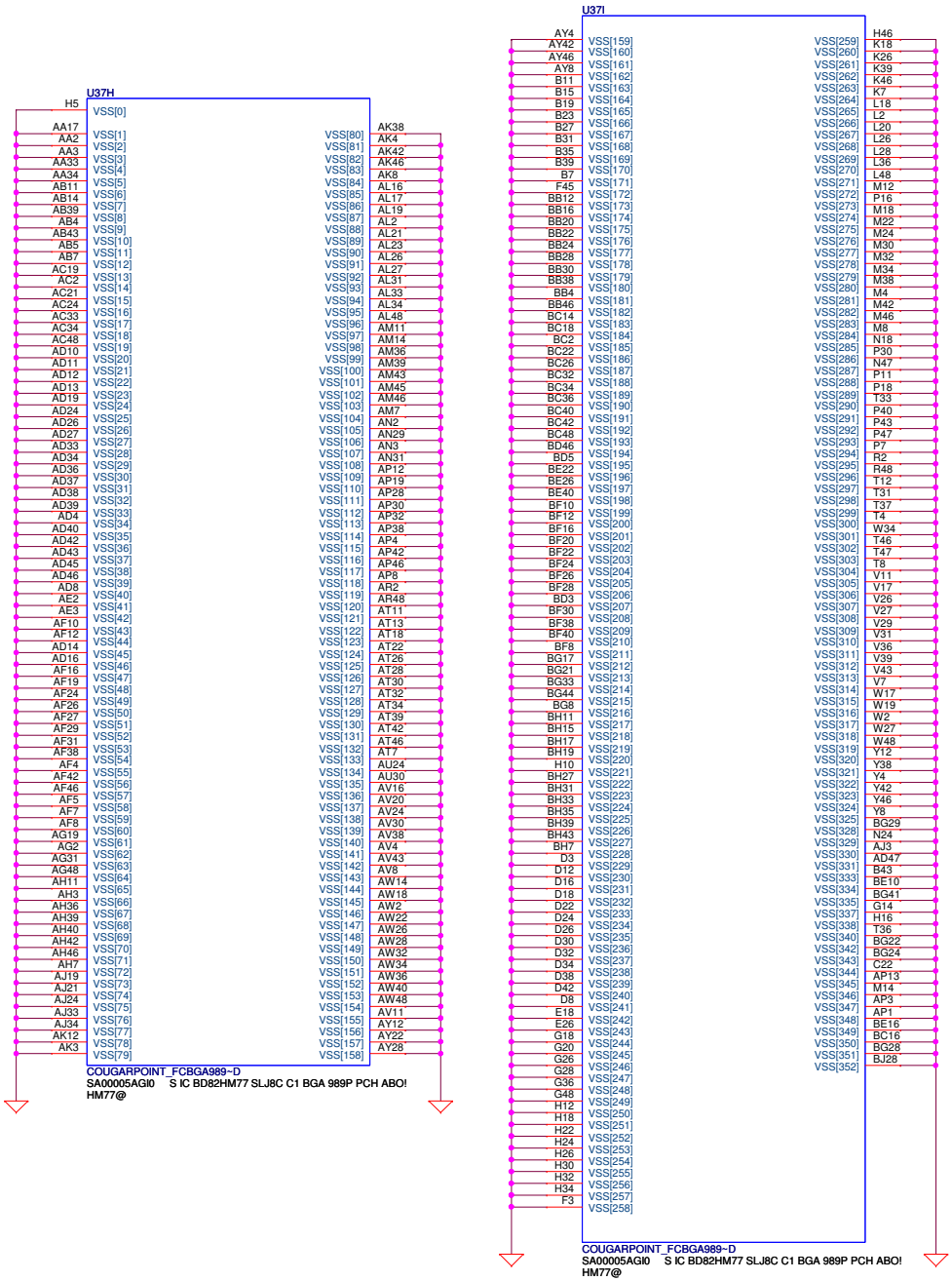
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

Date: Wednesday, March 13, 2013 | Sheet 20 of 52



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: PCH (9/9) VSS

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

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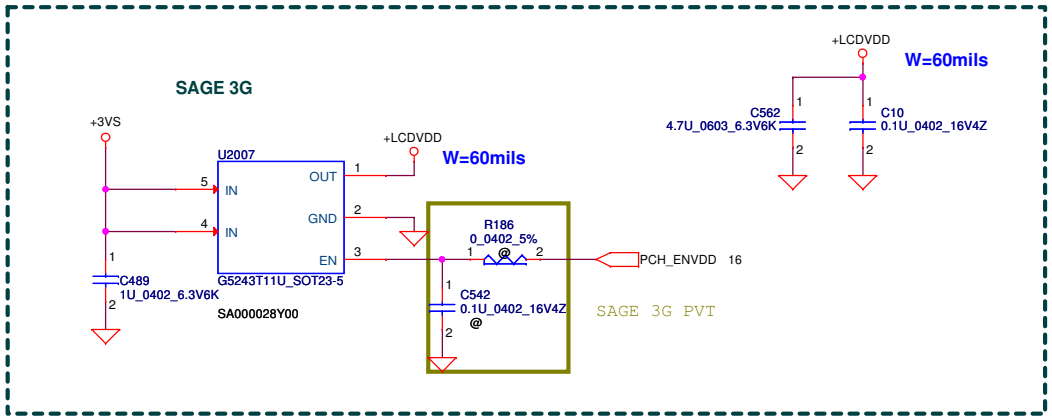
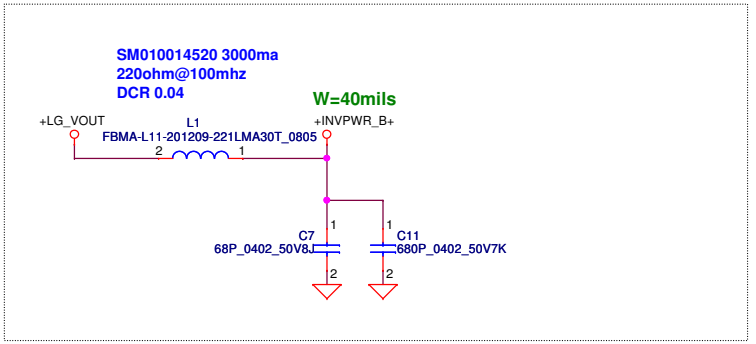
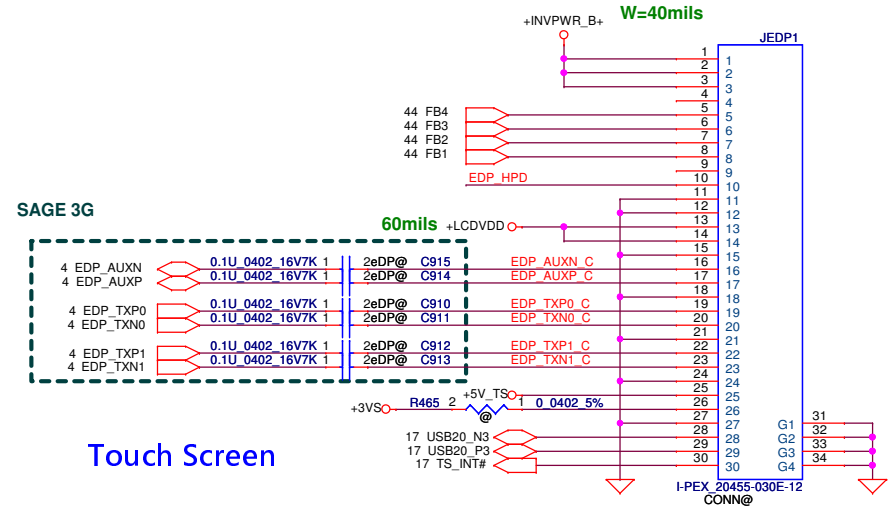
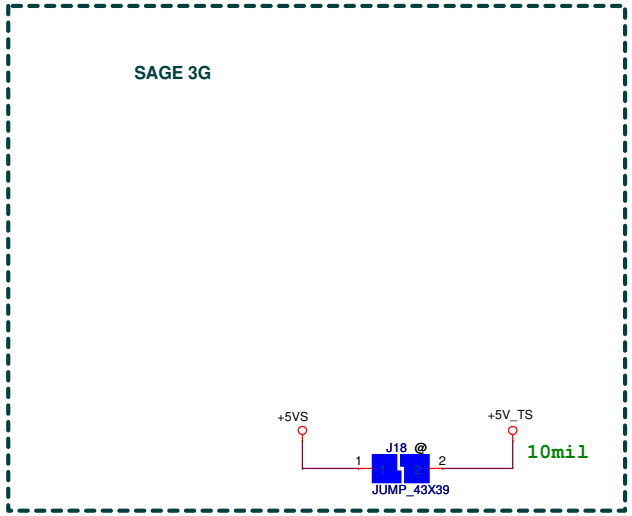
Panel POWER CIRCUIT

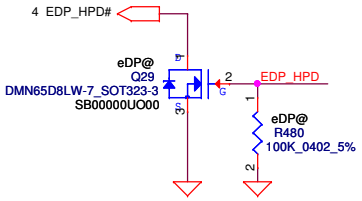


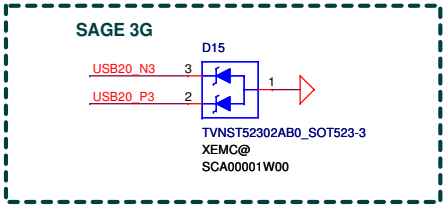


eDP PANEL Conn.









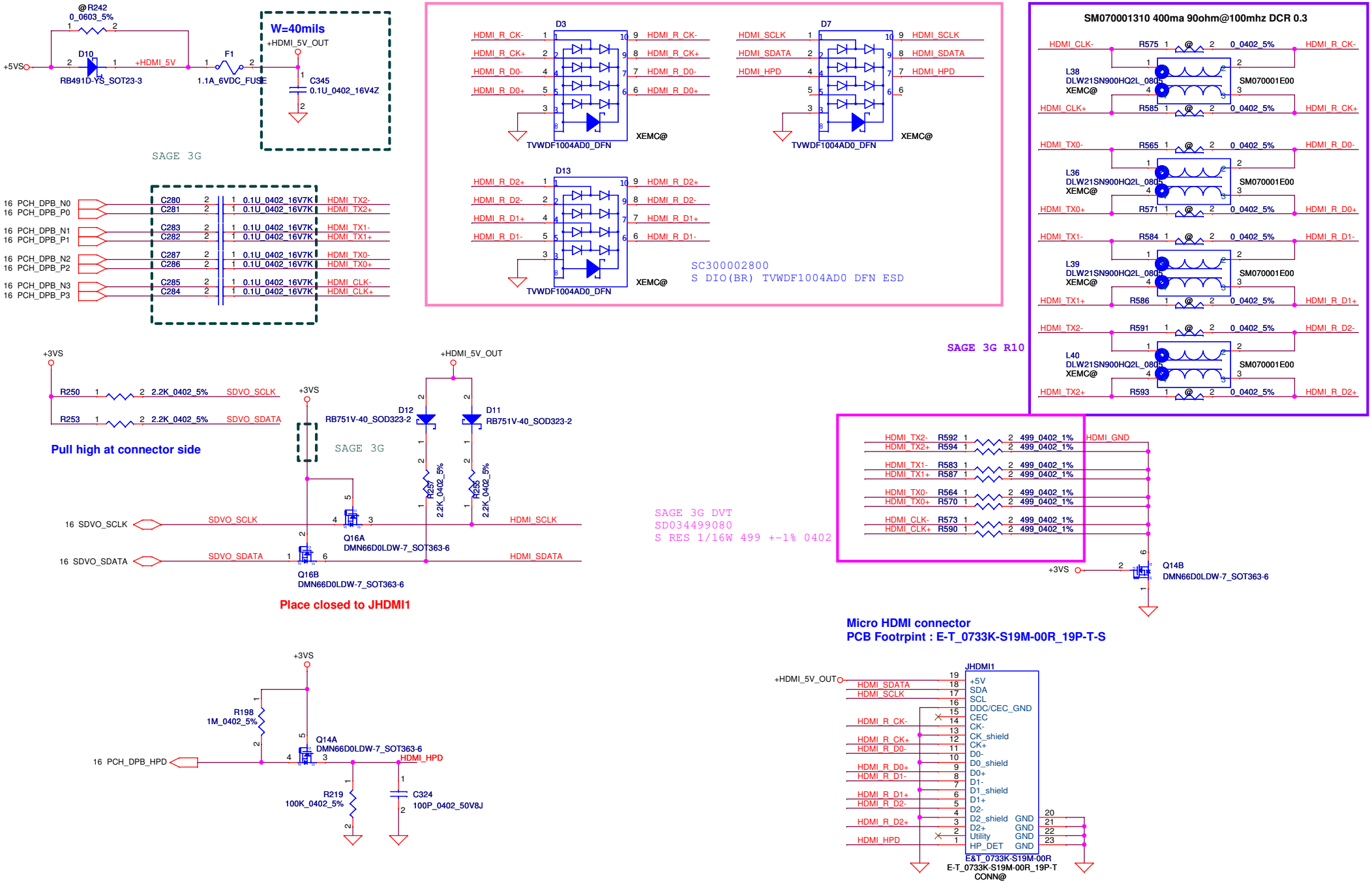
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: LVDS Connector

Size	Document Number	Rev
Custom	V1JB1 M/B LA-A041P Schematic	0.1

Date: Wednesday, March 13, 2013 | Sheet 22 of 52



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

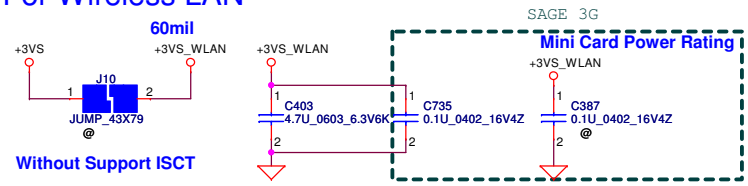
Compal Electronics, Inc.

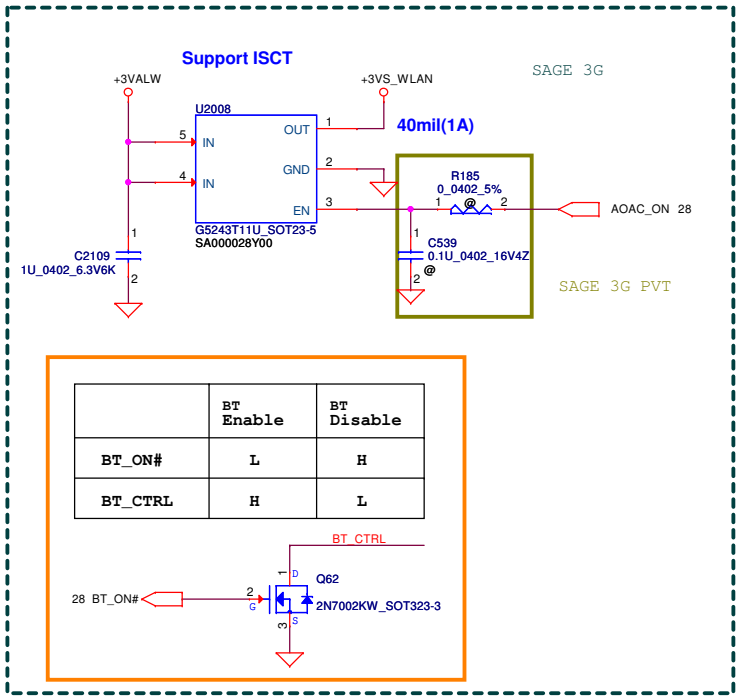
Title: HDMI Connector

Size	Document Number	Rev
Custom	V1JB1 M/B LA-A041P Schematic	0.1

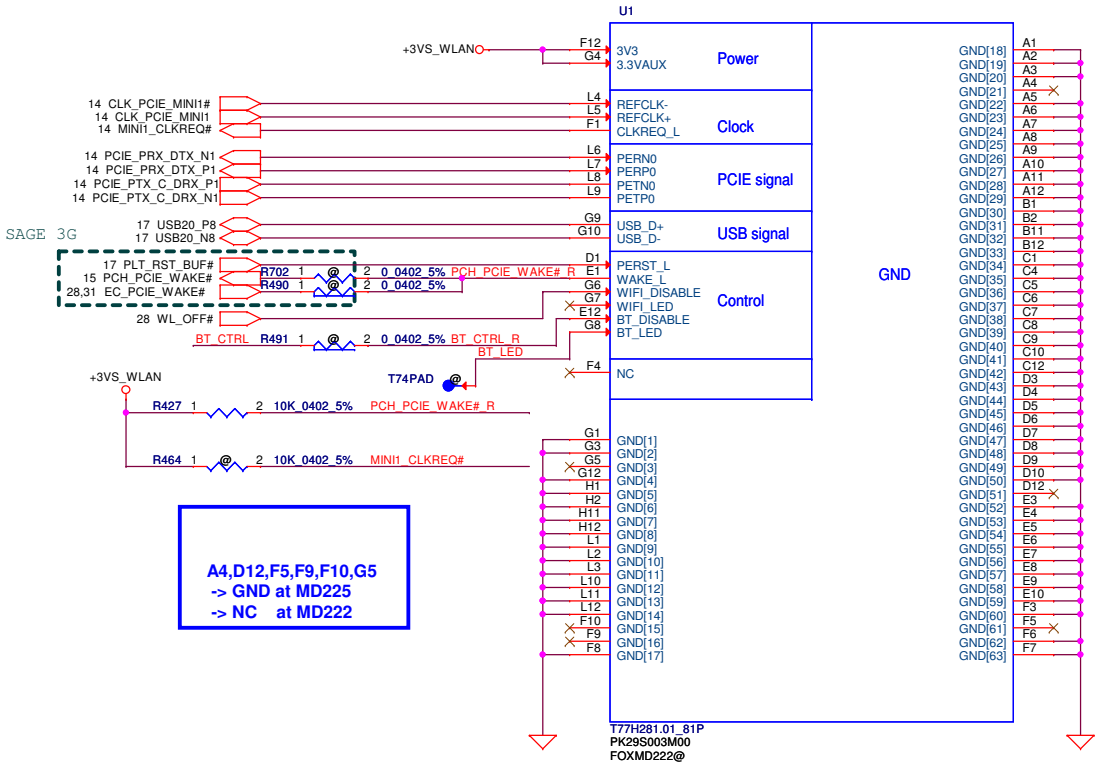
Date: Tuesday, March 26, 2013 | Sheet 23 of 52

For Wireless LAN





	BT Enable	BT Disable
BT_ON#	L	H
BT_CTRL	H	L



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

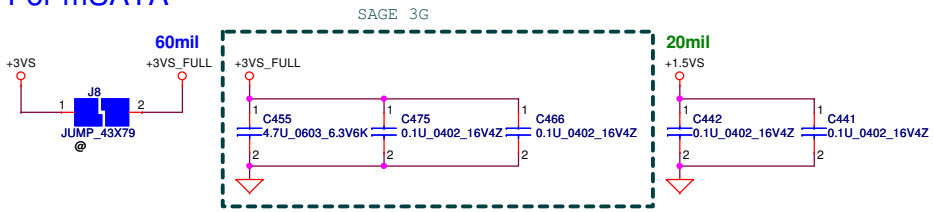
Compal Electronics, Inc.

Title: On Board WLAN

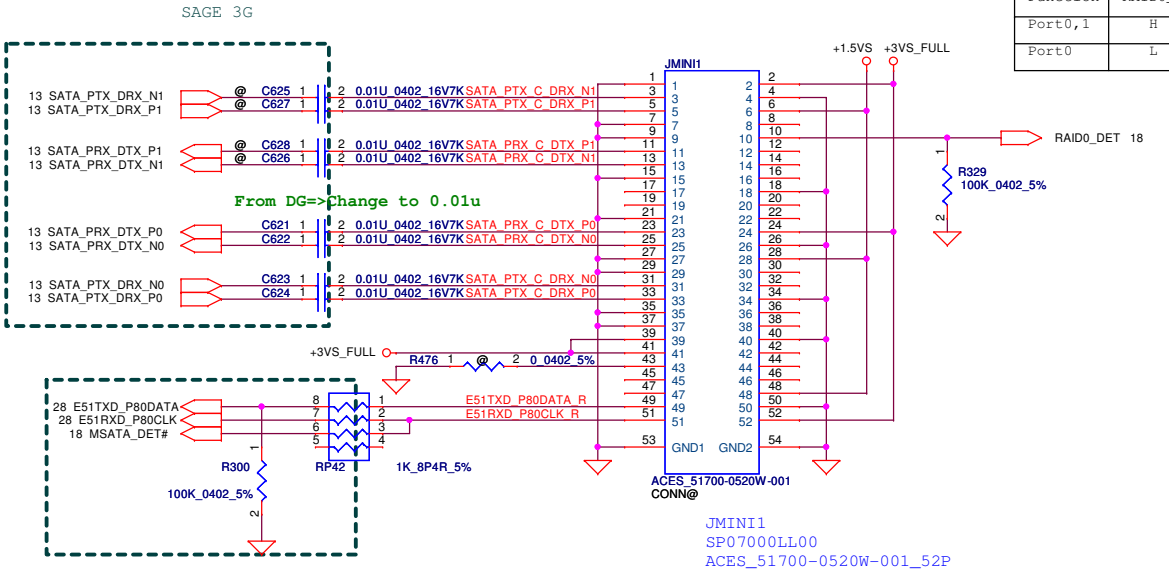
Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

Date: Wednesday, March 13, 2013 | Sheet 24 of 52

For mSATA



Function	RAID0_DET
Port0,1	H
Port0	L



JMINI1
SP07000LL00
ACES_51700-0520W-001_52P

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

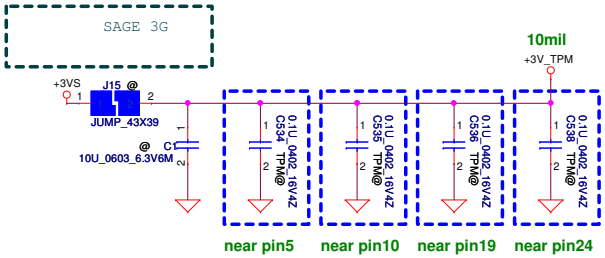
Compal Electronics, Inc.

Title: mSATA HDD Connector

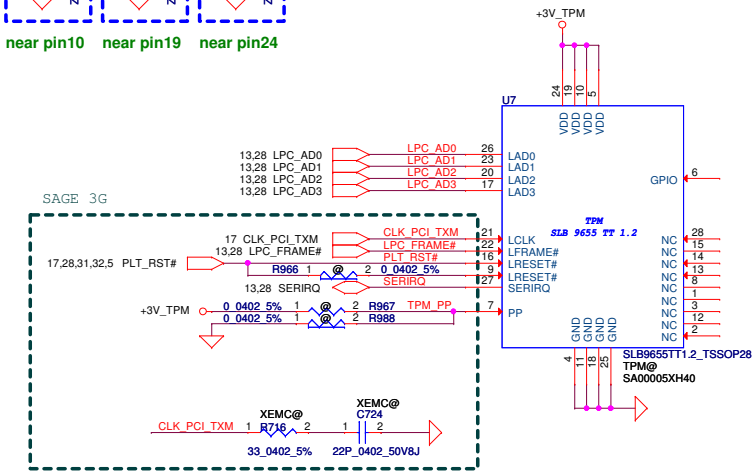
Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

Date: Wednesday, March 13, 2013 | Sheet 25 of 52

TPM



TPM - Infineon
SA00005XH40
S IC SLB9655TT1.2 FW4.31 TSSOP 28P TPM



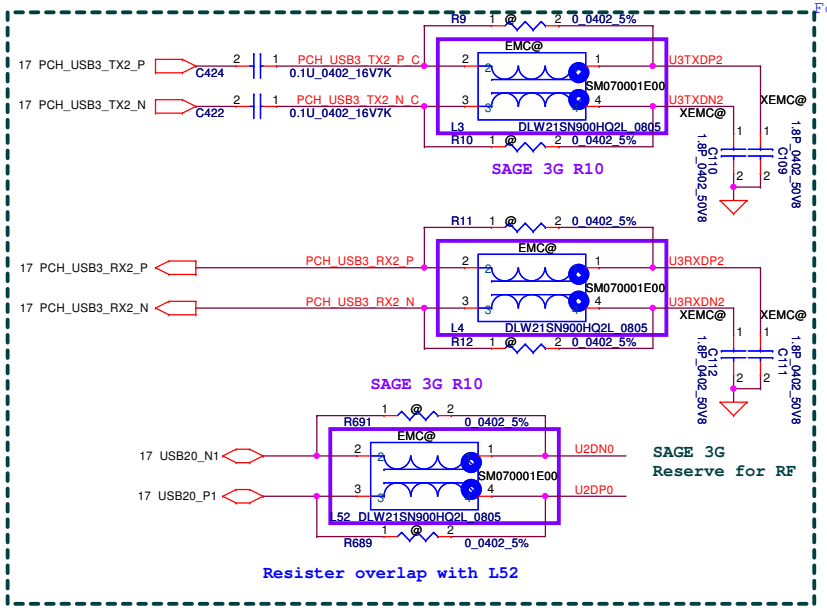
Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

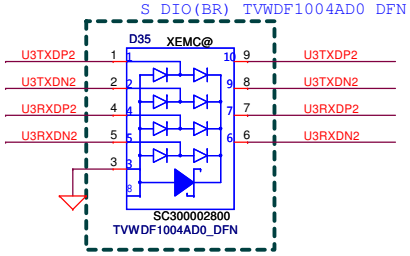
Title: TPM Infineon-SLB9655

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

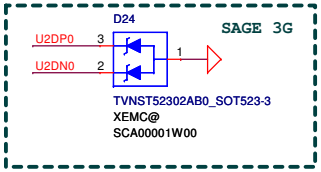
Date: Wednesday, March 13, 2013 | Sheet 26 of 52

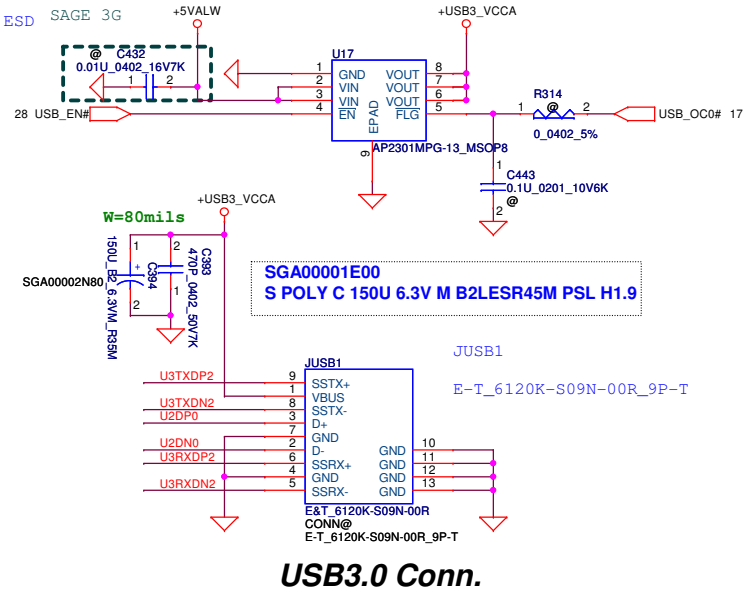


For ESD request SC300002800
S_DIO(BR) TVWDF1004AD0 DFN ESD SAGE 3G

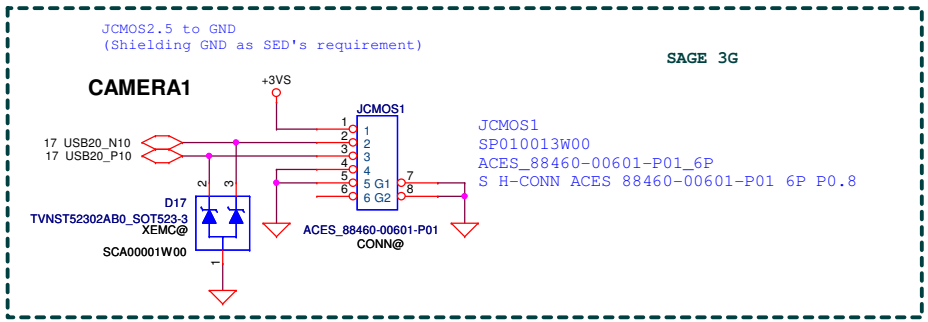


For USB2.0 ESD request





USB3.0 Conn.

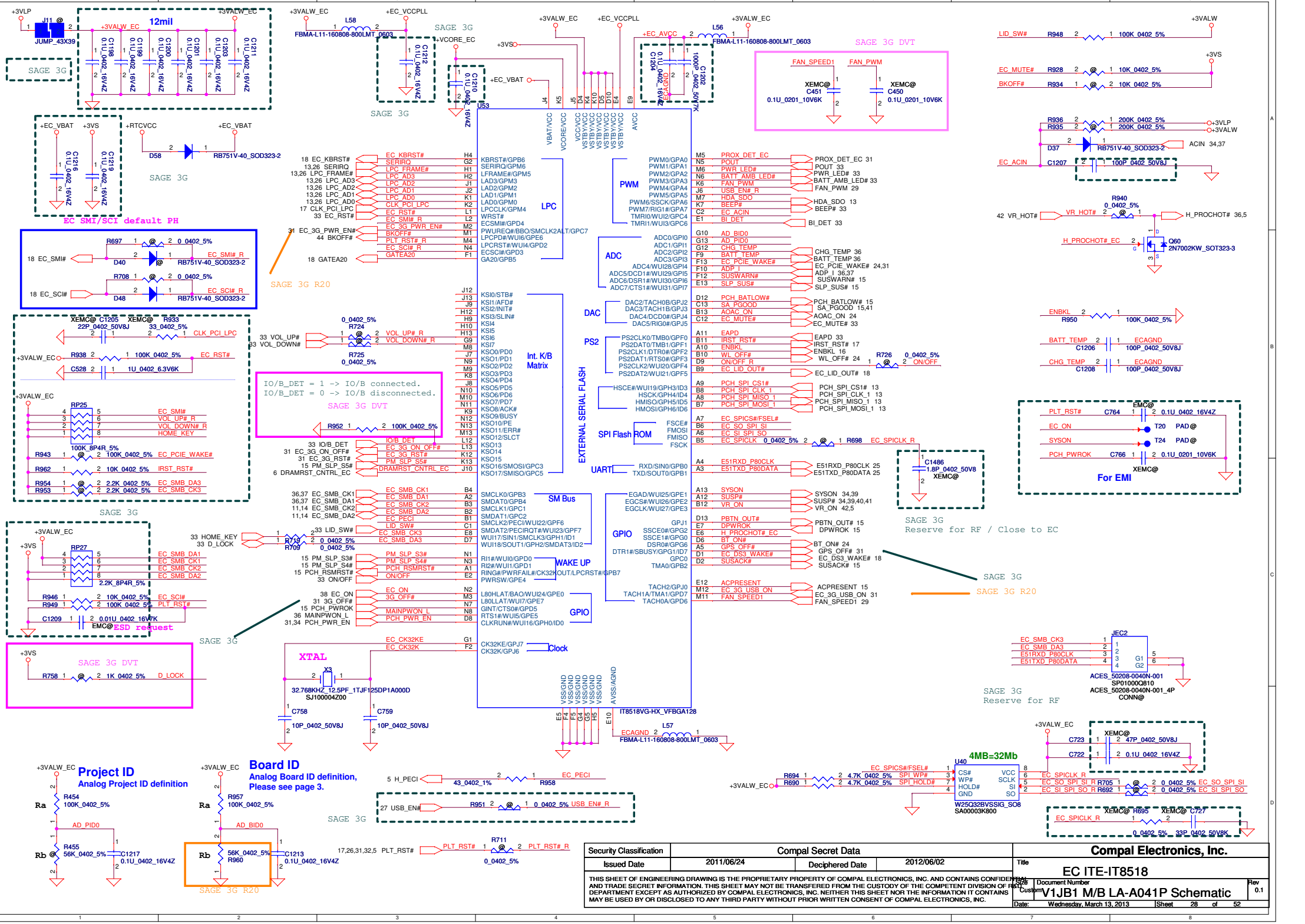


SAGE 3G

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/13

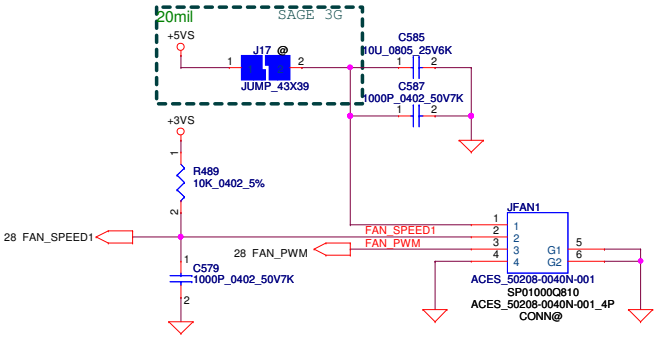
Title: USB3.0

Size	Document Number	Rev
Custom	V1JB1 M/B LA-A041P Schematic	0.1
Date: Tuesday, March 26, 2013	Sheet 27 of 52	



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/06/02
Title	EC ITE-IT8518		
Size: Custom	Document Number: V1JB1 M/B LA-A041P Schematic		Rev: 0.1
Date: Wednesday, March 13, 2013	Sheet 28 of 52		

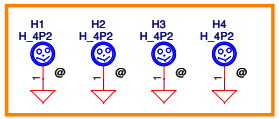
FAN Conn



JFAN1 conn
SP01000Q810
ACES_50208-0040N-001_4P
S H-CONN ACES 50208-0040N-001 4P P.8

定位孔

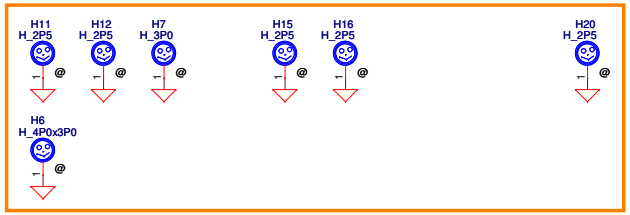
Thermal module

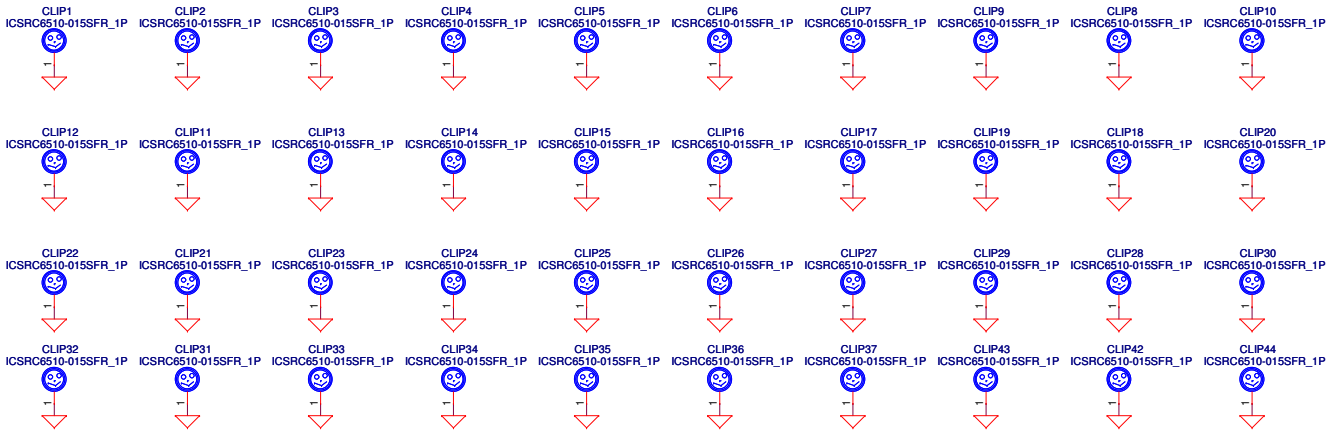


mSATA Stand-Off

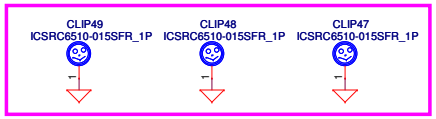
3G Stand-Off

螺孔





SAGE 3G DVT



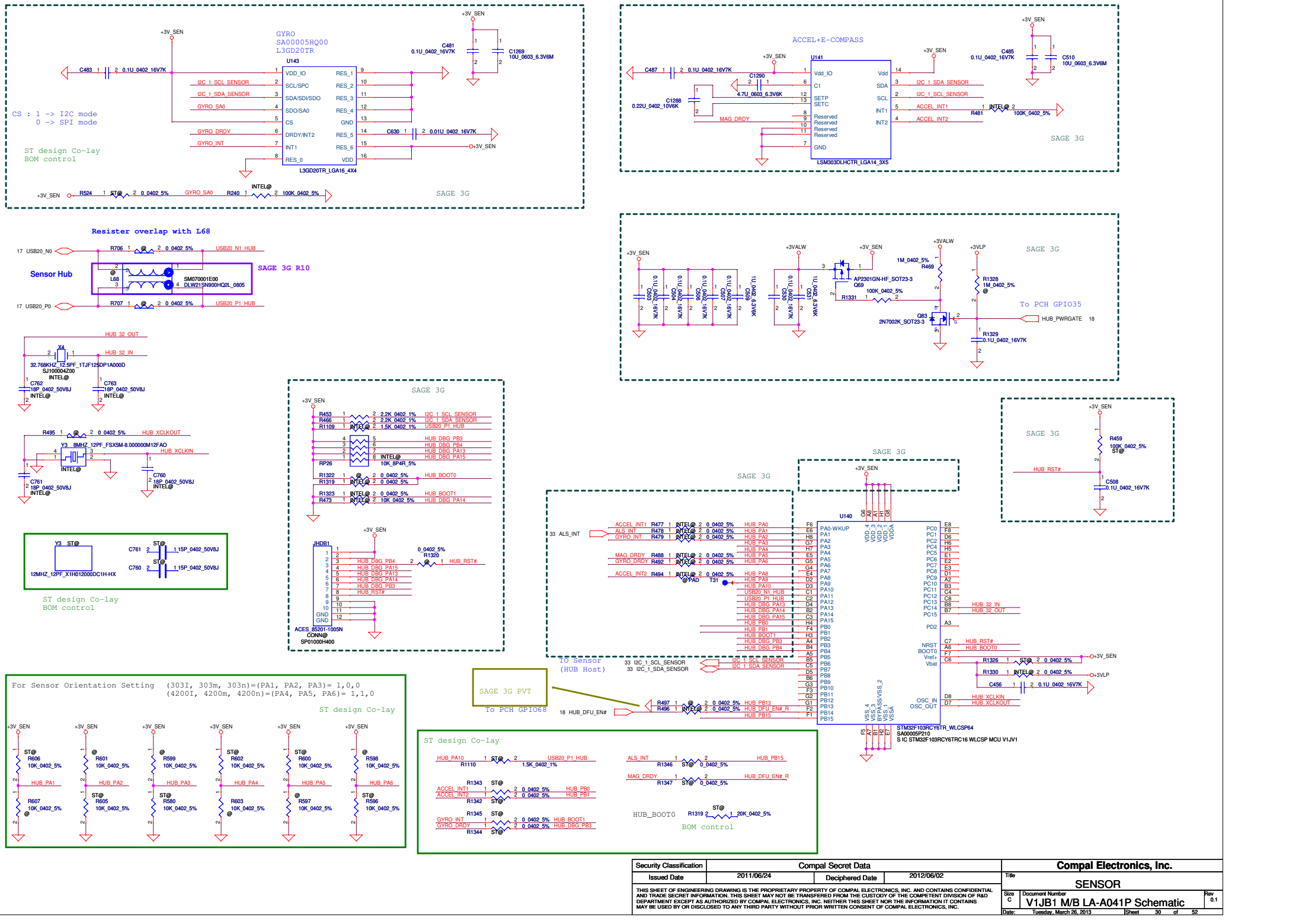
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: FAN,Screw Hole

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

Date: Wednesday, March 13, 2013 | Sheet 29 of 52



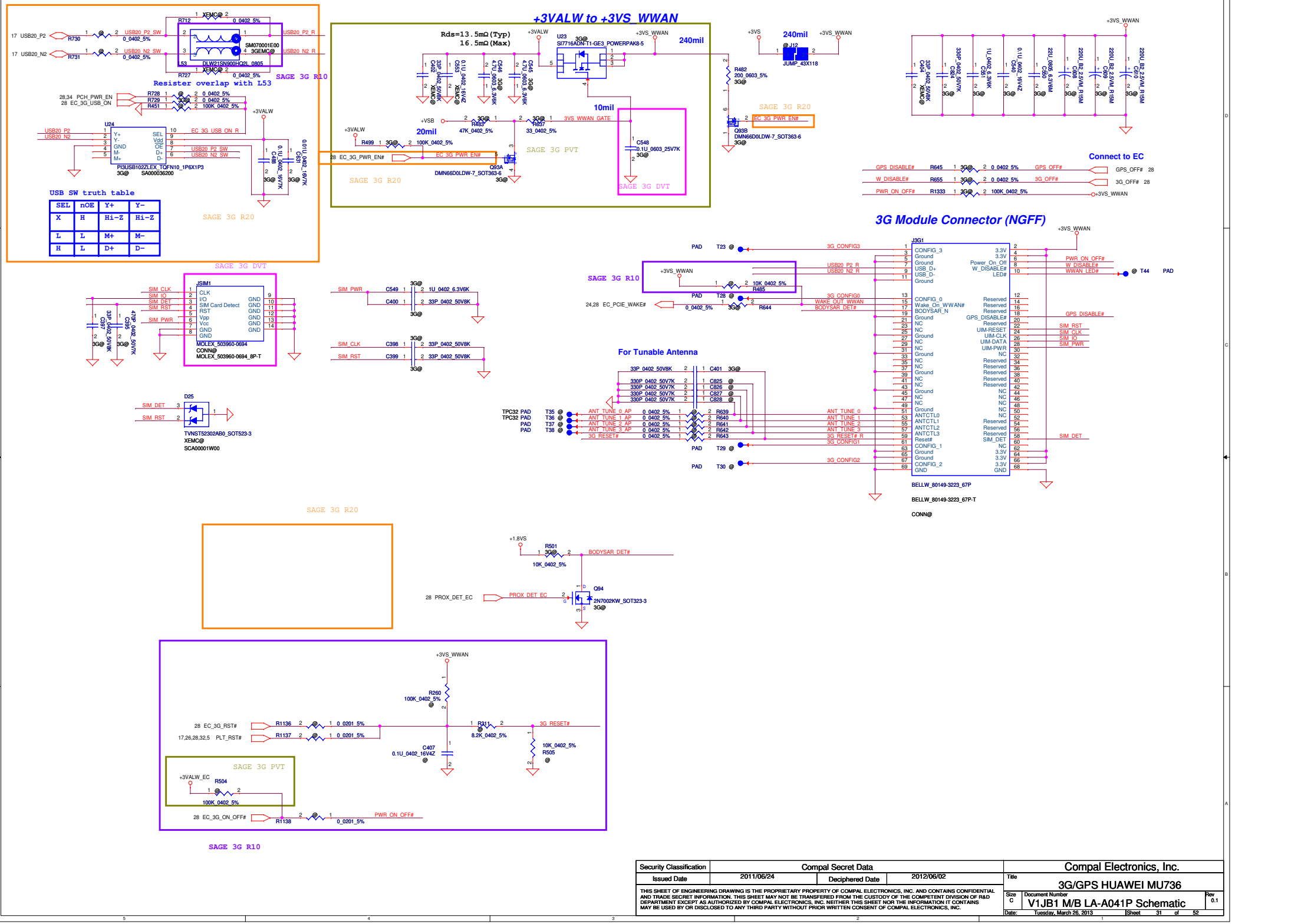
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: SENSOR

Size	Document Number	Rev
C	V1JB1 M/B LA-A041P Schematic	0.1

Date: Tuesday, March 26, 2013 Sheet 30 of 52



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

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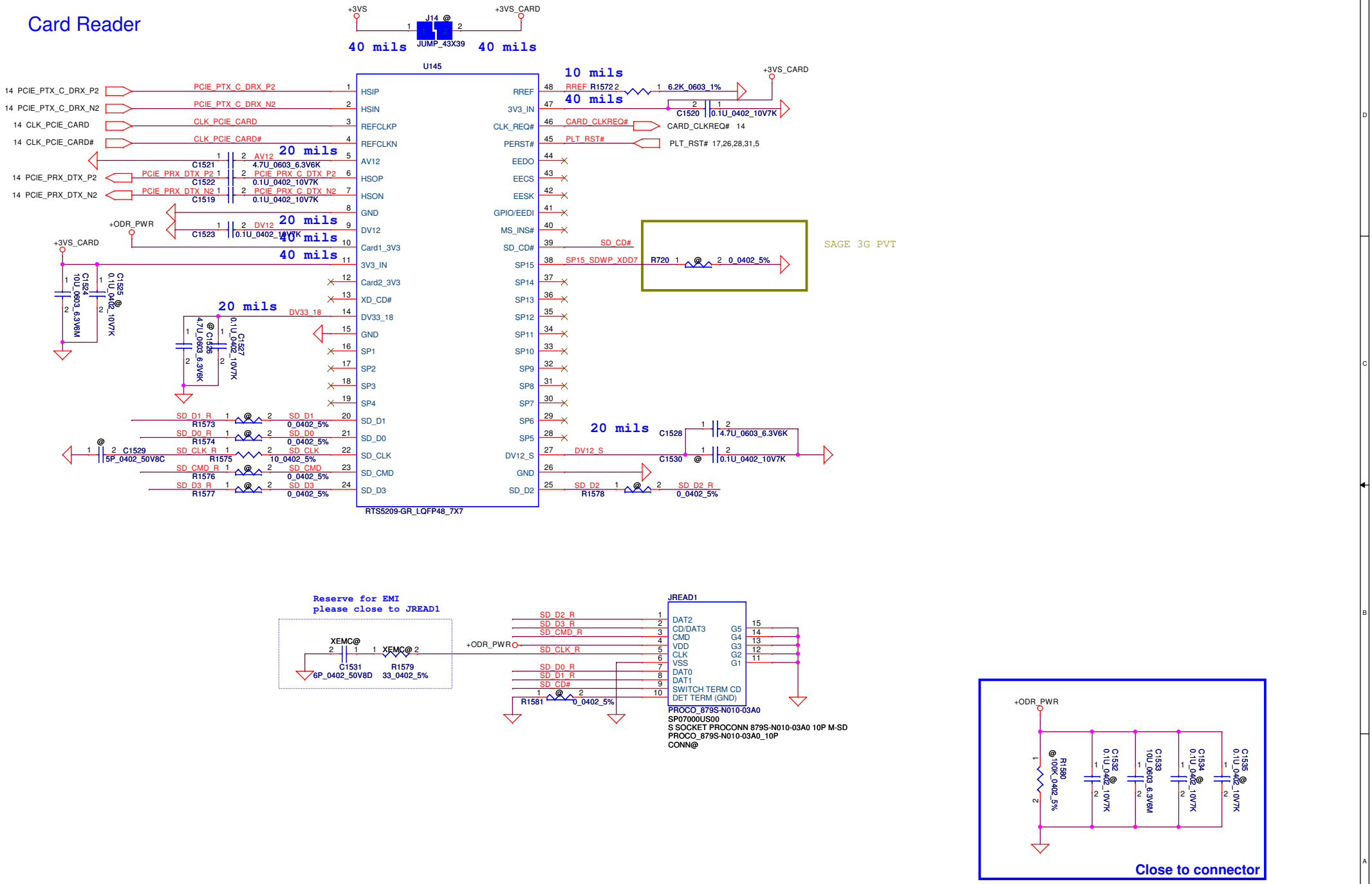
Compal Electronics, Inc.

Title: 3G/GPS HUAWEI MU736

Size: C | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

Date: Tuesday, March 26, 2013 | Sheet 31 of 52

Card Reader



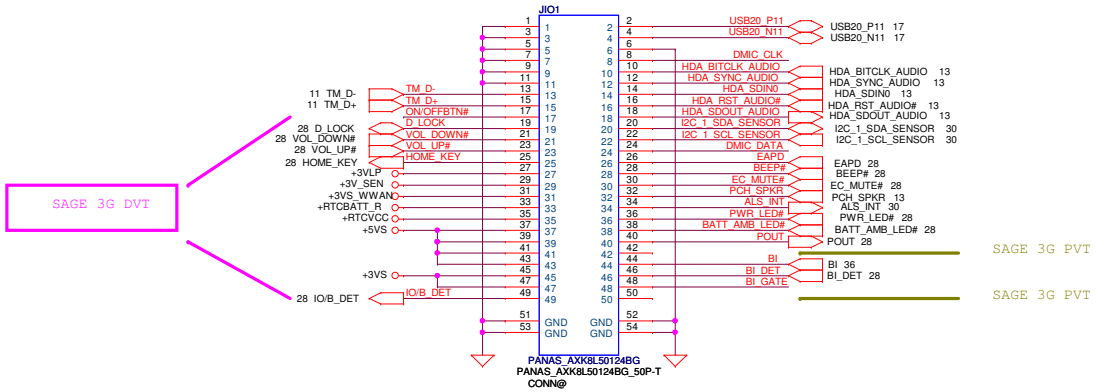
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

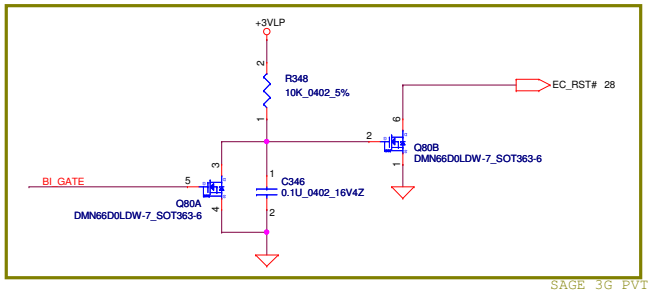
Compal Electronics, Inc.

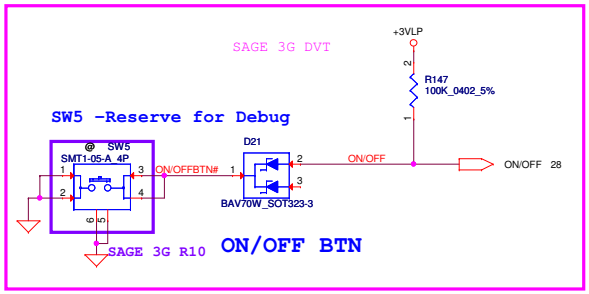
Title: Card Reader RTS5209

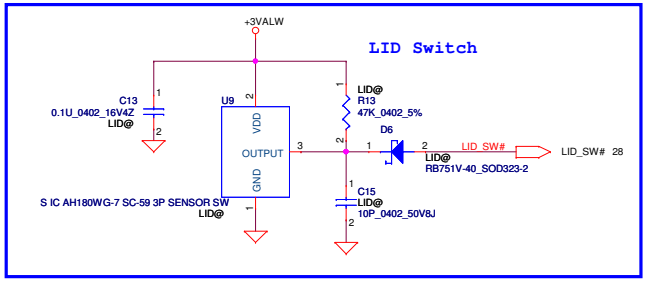
Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

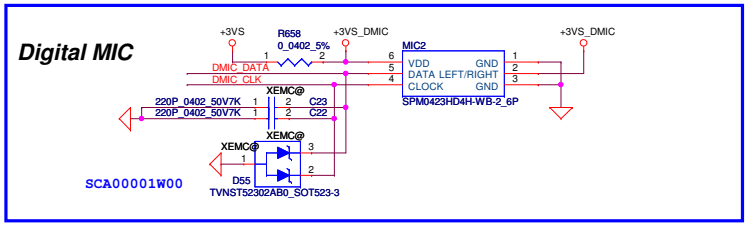
Date: Wednesday, March 13, 2013 | Sheet 32 of 52











Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

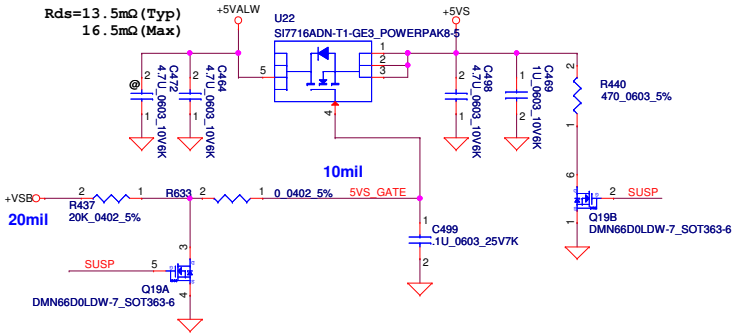
Compal Electronics, Inc.

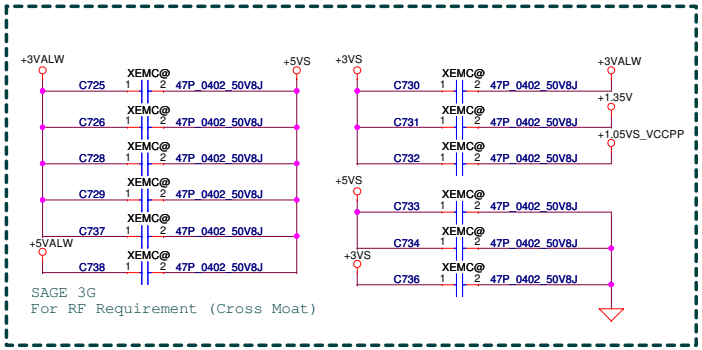
Title: IO Board (Audio / WIN / RST/ LED)

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

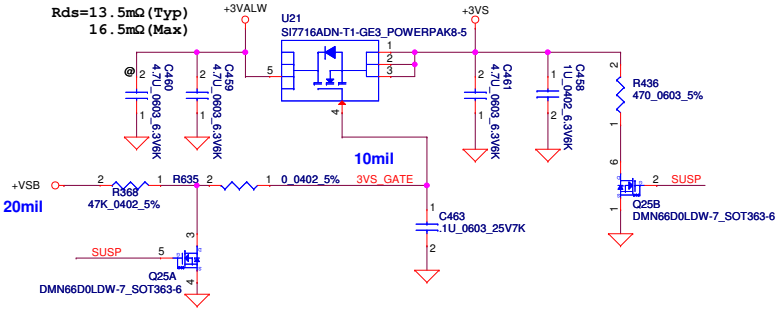
Date: Thursday, March 14, 2013 | Sheet 33 of 52

+5VALW to +5VS

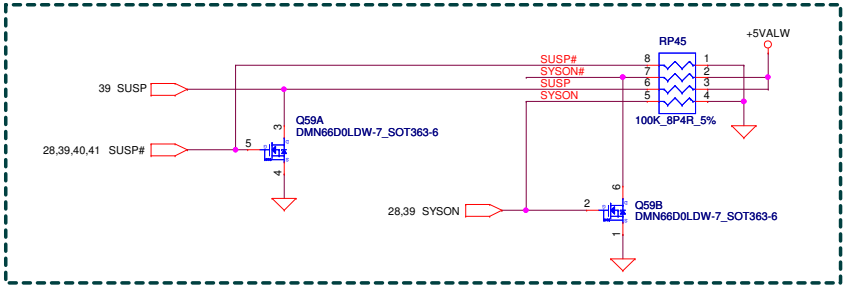




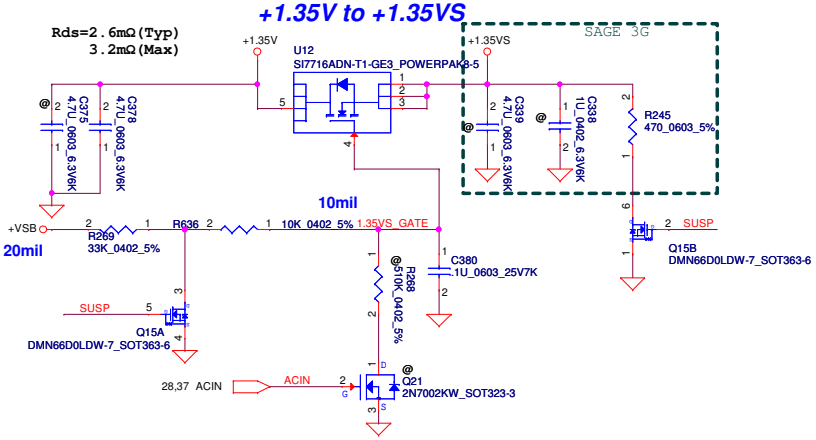
+3VALW to +3VS

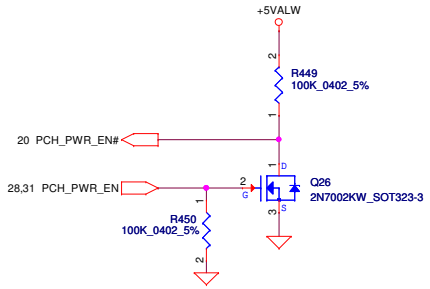


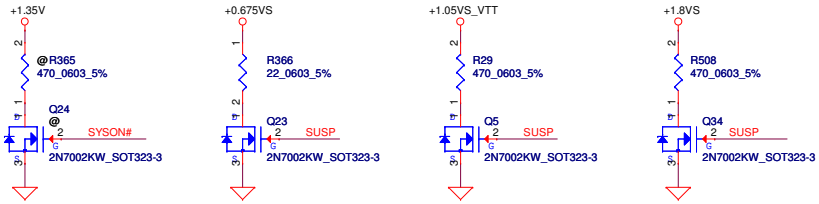
SAGE 3G



+1.35V to +1.35VS







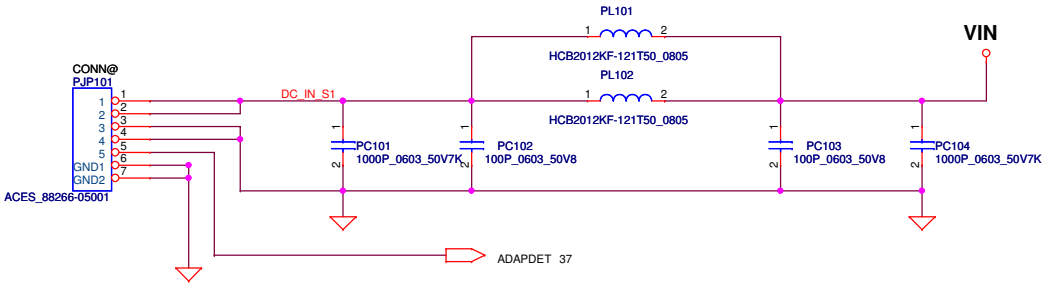
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

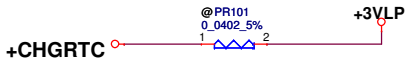
Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

Date: Wednesday, March 13, 2013 | Sheet 34 of 52





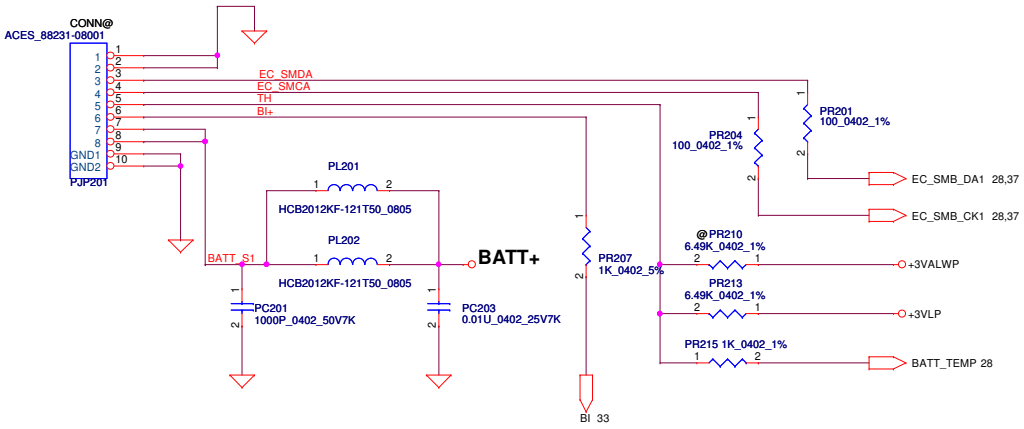
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	Date of EOP

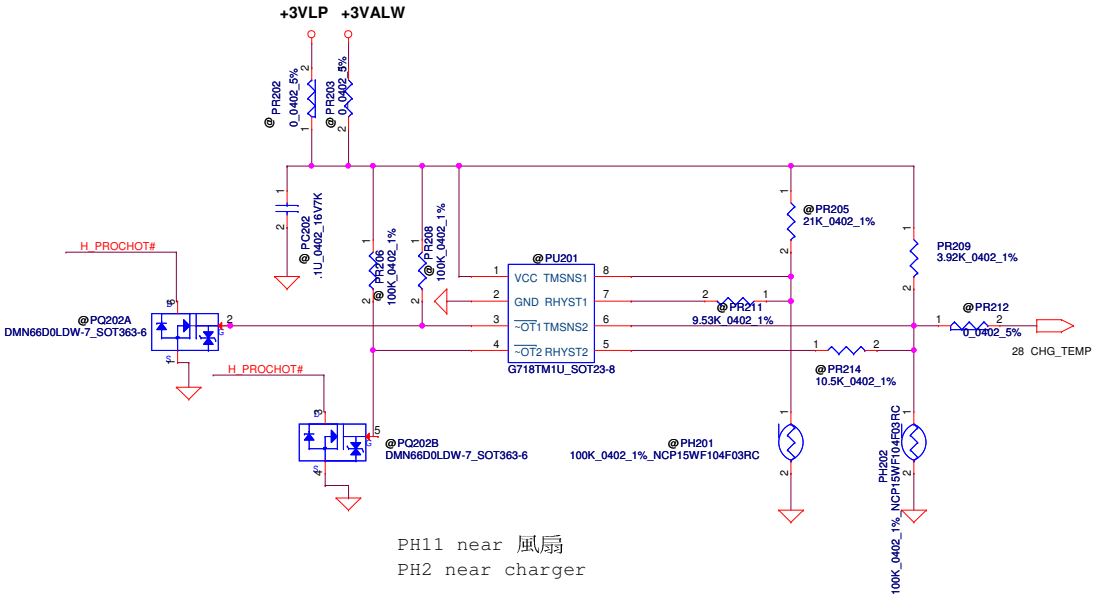
Compal Electronics, Inc.

Title: *DCIN/PRECHARGE*

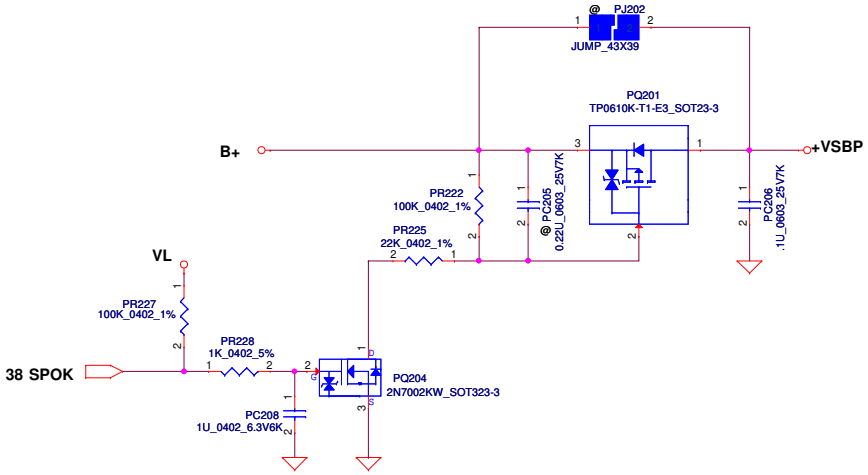
Size: Custom | Document Number: *SAGE 3G* | Rev: 1.0

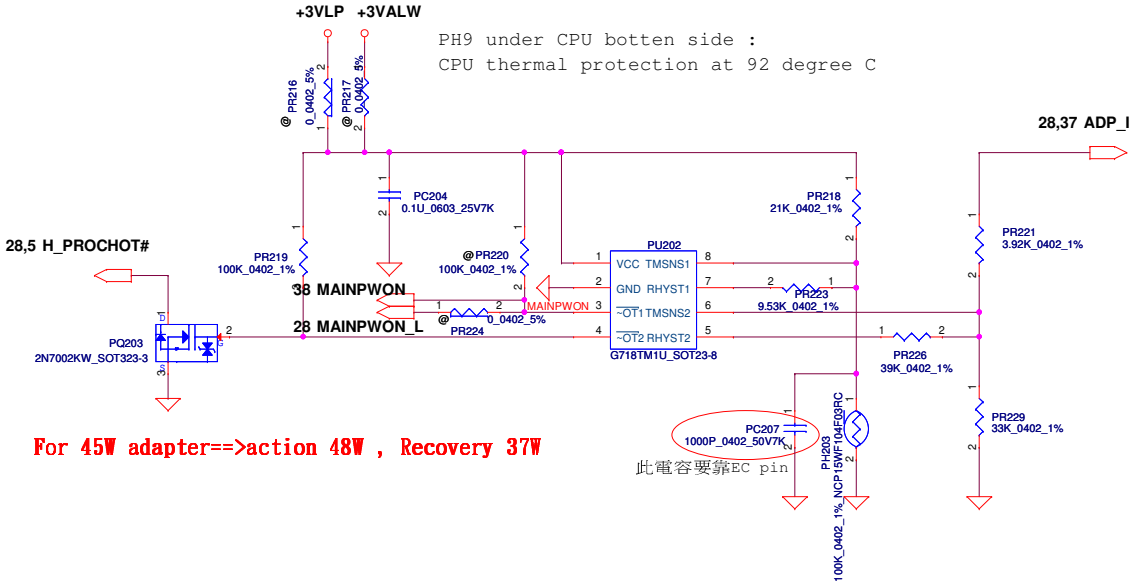
Date: | Sheet 35 of 52





PH11 near 風扇
PH2 near charger





PH9 under CPU botten side :
CPU thermal protection at 92 degree C

For 45W adapter==>action 48W , Recovery 37W

此電容要靠EC pin

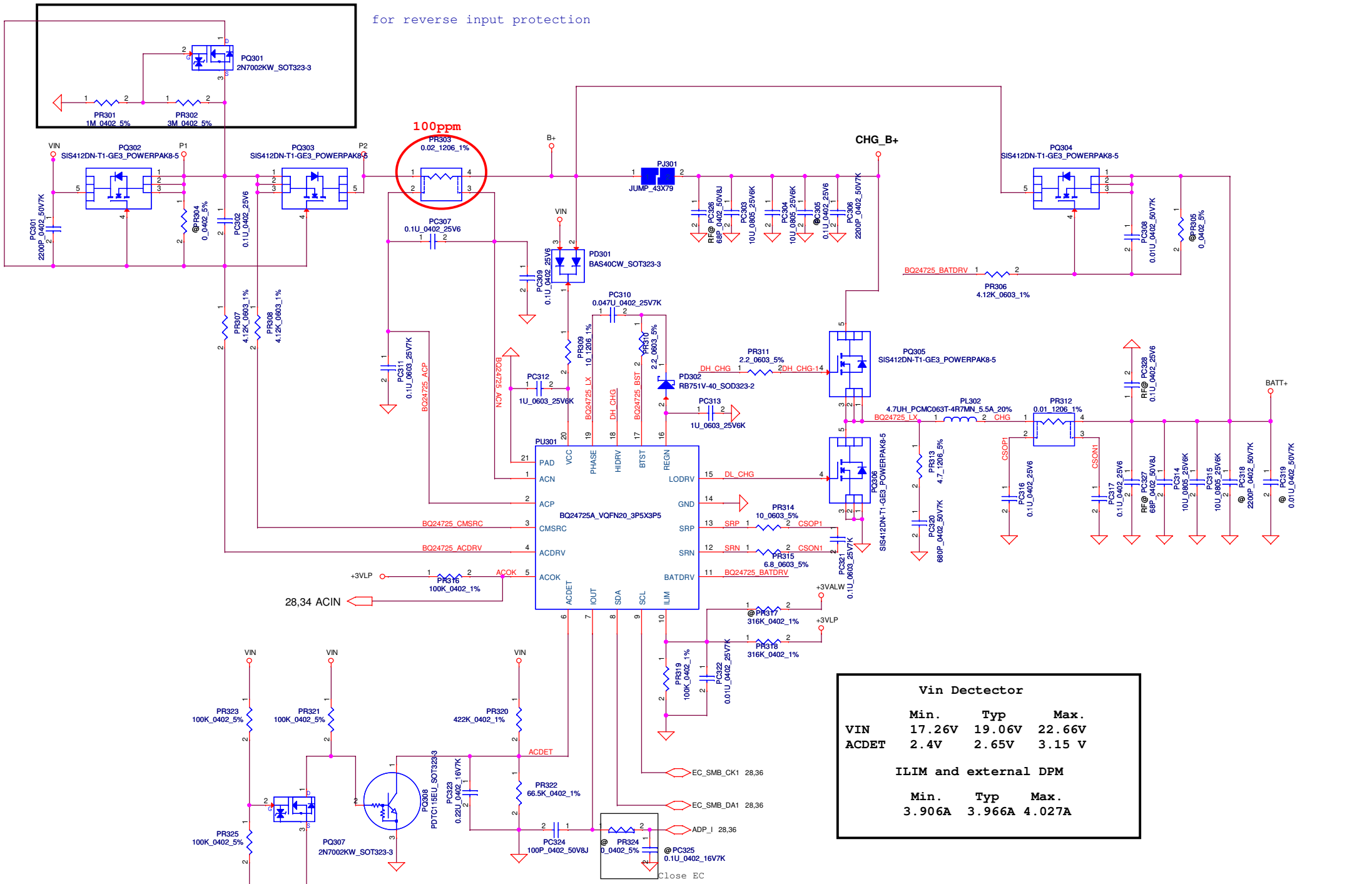
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	Date of EOP

Compal Electronics, Inc.

Title: *BATTERY CONN / OTP*

Size: Custom | Document Number: *SAGE 3G* | Rev: 1.0

Date: | Sheet 36 of 52



Vin Dectector

	Min.	Typ	Max.
VIN	17.26V	19.06V	22.66V
ACDET	2.4V	2.65V	3.15 V

ILIM and external DPM

Min.	Typ	Max.
3.906A	3.966A	4.027A

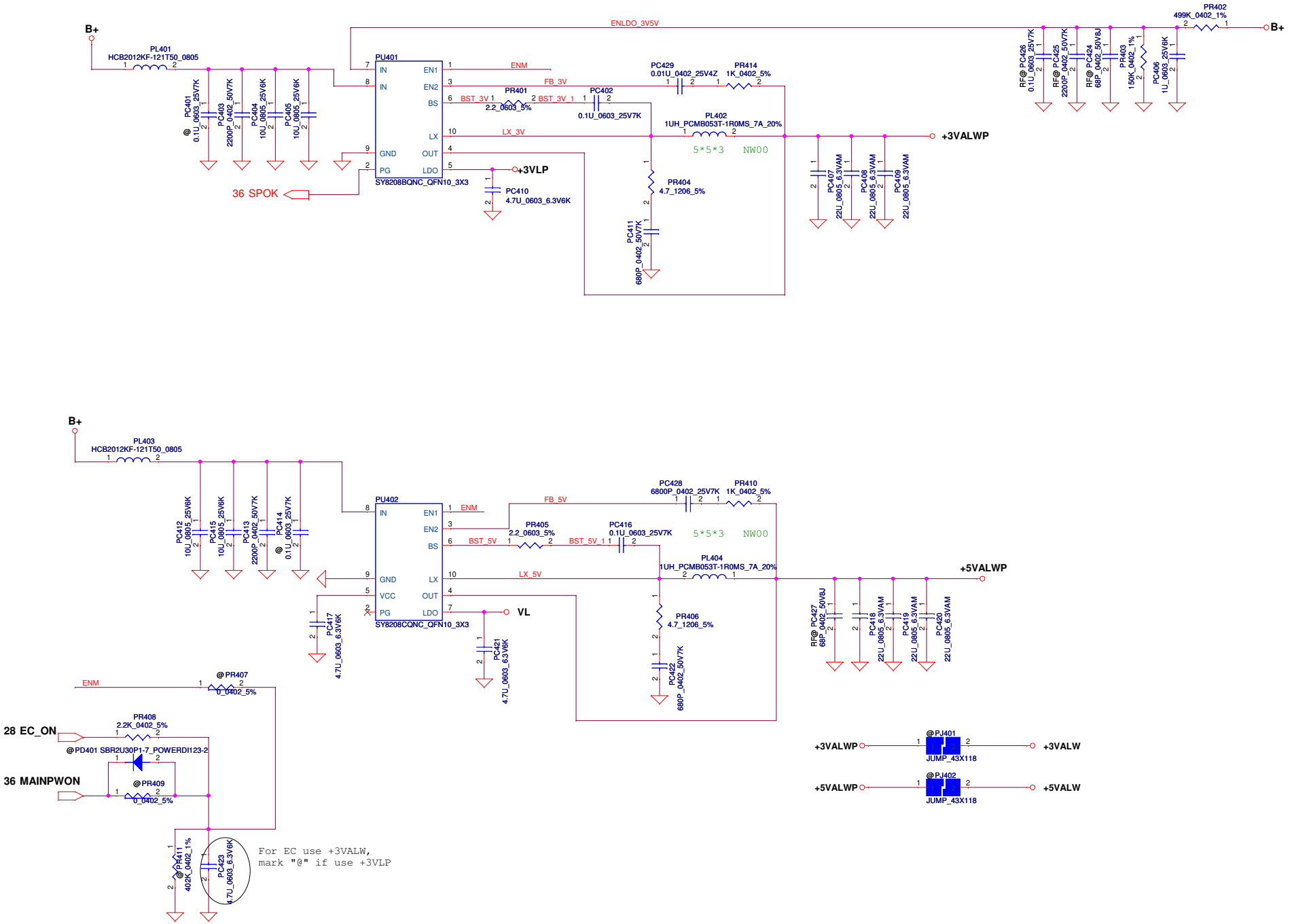
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	Date of EOP

Compal Electronics, Inc.

Title: CHARGER

Size: Custom | Document Number: SAGE 3G | Rev: 1.0

Date: | Sheet 37 of 52



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	Date of EOP

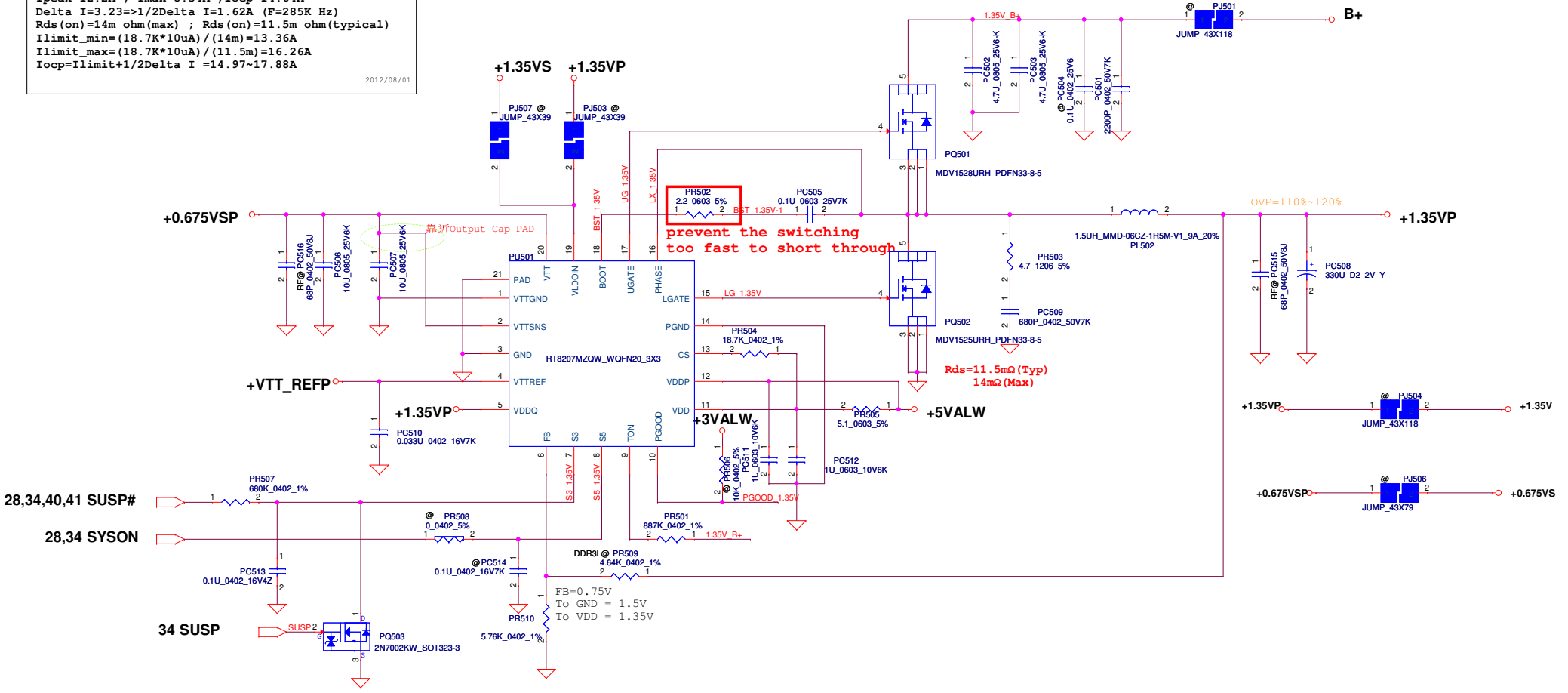
Compal Electronics, Inc.

Title: *3VALW/5VALW*

Size: Custom | Document Number: *SAGE 3G* | Rev: 1.0

Date: | Sheet 38 of 52

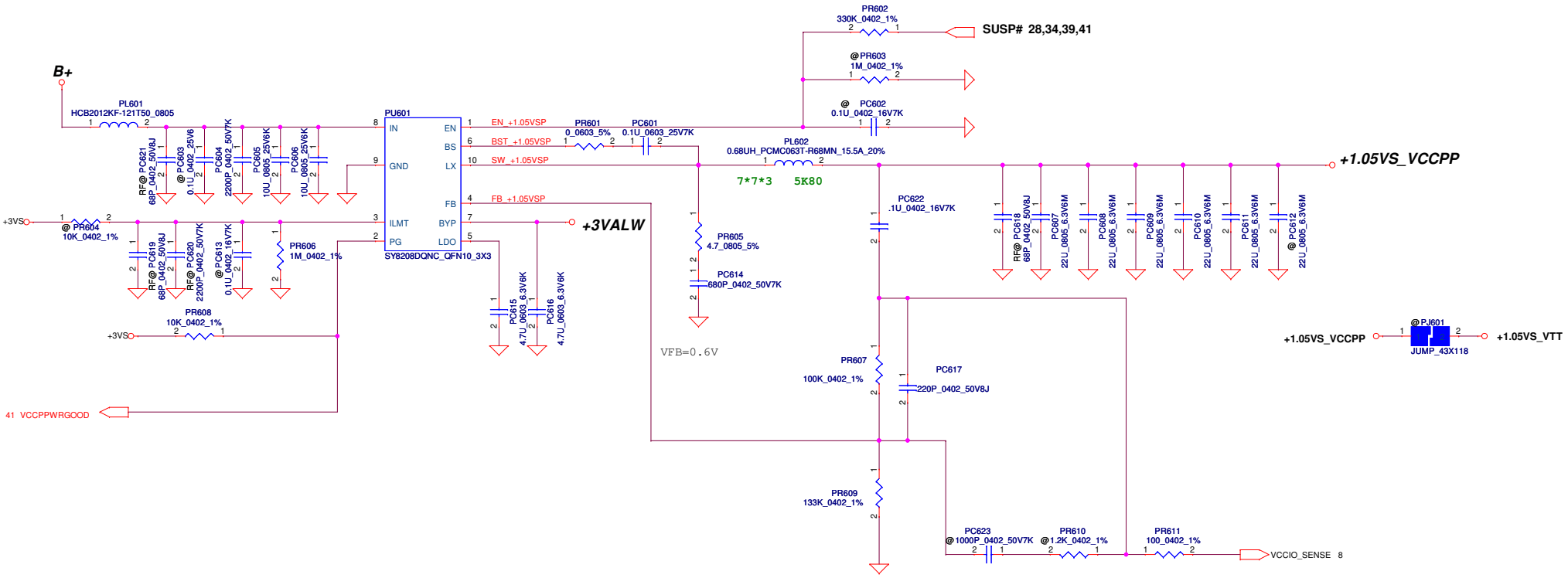
```
Ipeak=12.2A ; Imax=8.54A ;Iocp=14.64A
Delta I=3.23=>1/2Delta I=1.62A (F=285K Hz)
Rds(on)=14m ohm(max) ; Rds(on)=11.5m ohm(typical)
Ilimit_min=(18.7K*10uA)/(14m)=13.36A
Ilimit_max=(18.7K*10uA)/(11.5m)=16.26A
Iocp=Ilimit+1/2Delta I =14.97~17.88A
                                        2012/08/01
```



STATE	S3	S5	1.35VP	VTT_REFP	0.675VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date / Date of EOP	Title: 1.5VP/0.75VSP/1.8VSP
Size: Custom	Document Number: SAGE 3G		Rev: 1.0
Date:	Sheet 39 of 52		



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	Date of EOP

Compal Electronics, Inc.

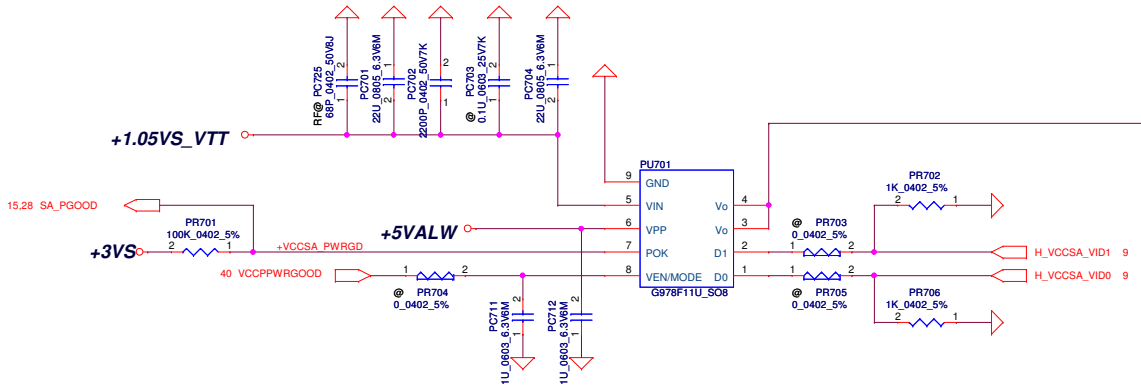
Title: *1.05VS_VTTP*

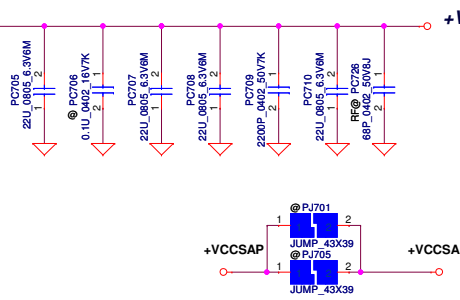
Size: Custom | Document Number: *SAGE 3G* | Rev: 1.0

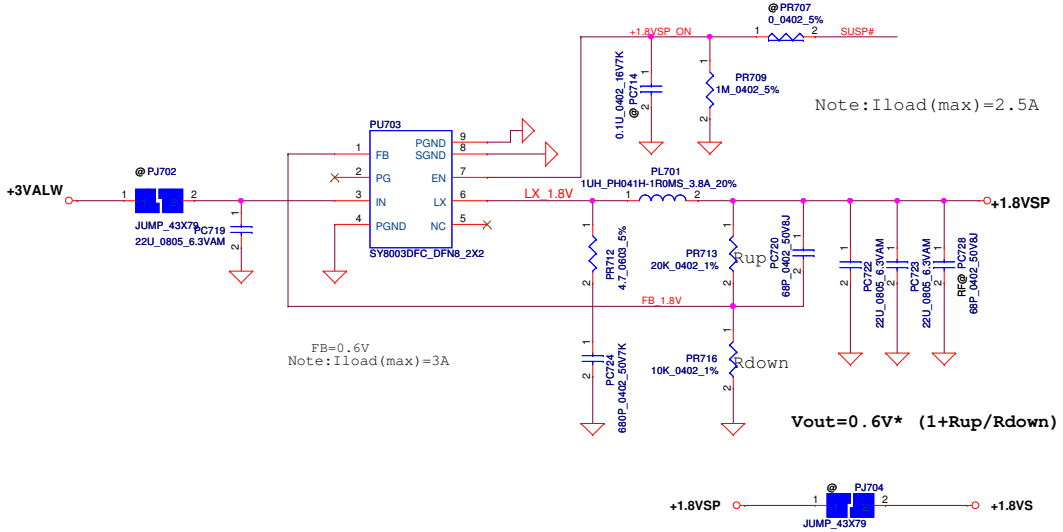
Date: | Sheet 40 of 52

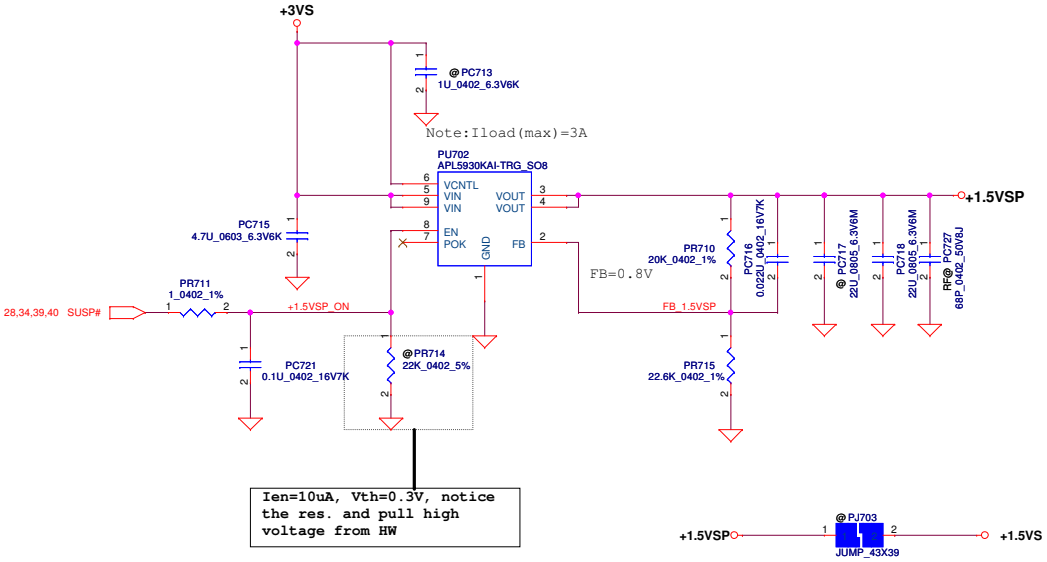
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

output voltage adjustable network









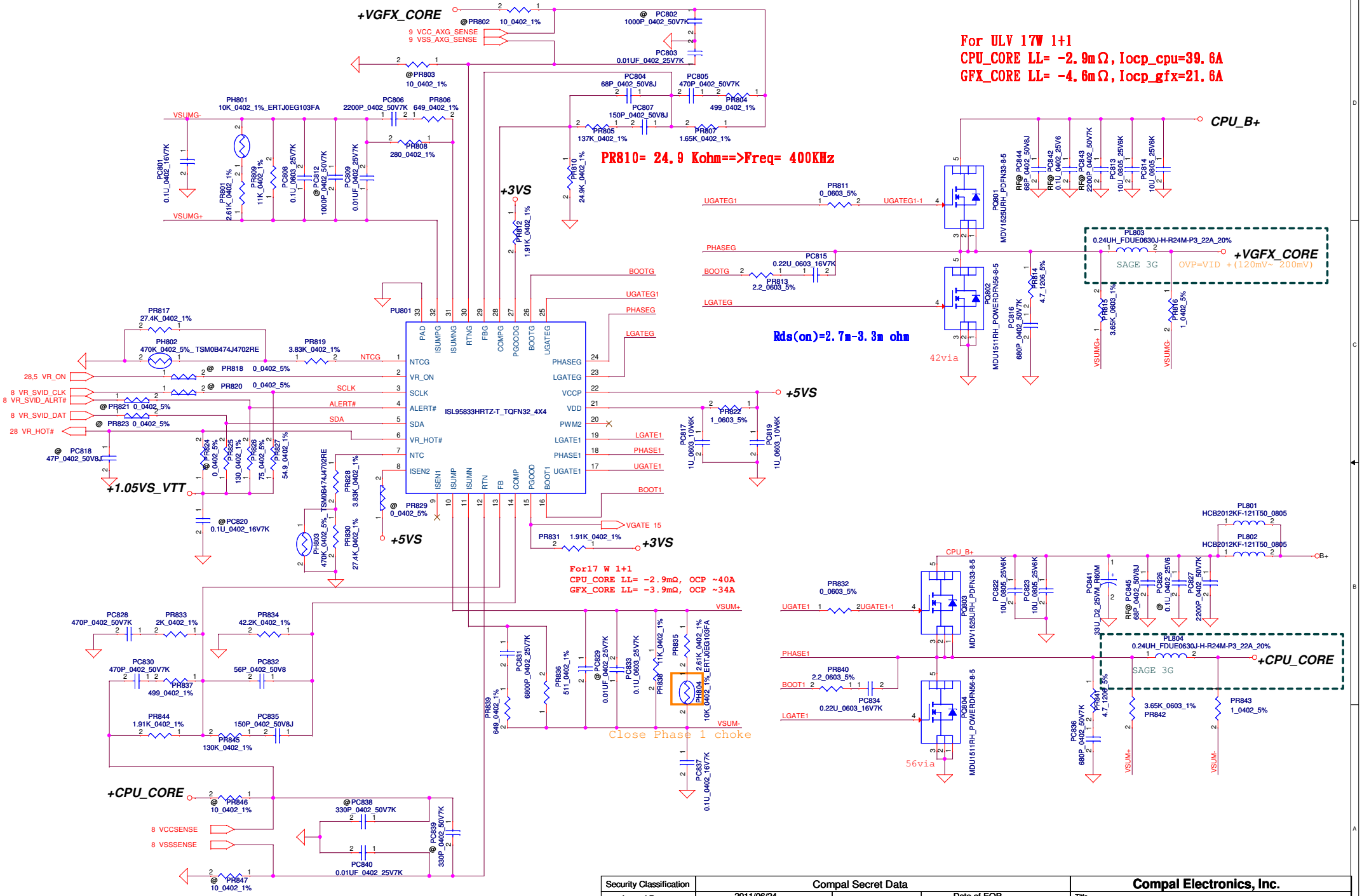
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	Date of EOP

Compal Electronics, Inc.

Title: *VCC_SAP*

Size	Document Number	Rev
Custom	SAGE 3G	1.0

Date: | Sheet 41 of 52



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	Date of EOP

Compal Electronics, Inc.	
Title	CPU_CORE/VGFX_CORE
Size: Custom	Document Number: SAGE 3G
Rev	1.0
Date:	Sheet 42 of 52

PWR Rule 17W@ULV(CR BGA1023_GT2) CPU2.9m GFx3.9m
CPU 330uF/9m *3, 22uF(0805) *12, 2.2uF(0402)*16
GFX 330uF/9m*2, 22uF(0805)*6, 10uF(0603)*6, 1uF(0402)*11
1.05V 330uF*2,10uF(0603)*10,1uF(0402)*26

+VGFX_CORE

PC901 1U_0402_6.3V6K
PC910 1U_0402_6.3V6K
PC911 1U_0402_6.3V6K
PC912 1U_0402_6.3V6K
PC913 1U_0402_6.3V6K
PC914 1U_0402_6.3V6K
PC915 1U_0402_6.3V6K
PC916 1U_0402_6.3V6K
PC917 1U_0402_6.3V6K
PC918 1U_0402_6.3V6K
PC919 1U_0402_6.3V6K

PC928 10U_0603_6.3V6M
PC929 10U_0603_6.3V6M
PC930 10U_0603_6.3V6M
PC931 10U_0603_6.3V6M
PC932 10U_0603_6.3V6M
PC933 10U_0603_6.3V6M

ESR=9m ohm

PC941 330U_D2_2V_Y
PC942 330U_D2_2V_Y
PC943 22U_0805_6.3V6M
PC944 22U_0805_6.3V6M
PC945 22U_0805_6.3V6M
PC946 22U_0805_6.3V6M
PC947 22U_0805_6.3V6M
PC948 22U_0805_6.3V6M

Vaxg

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

+1.05VS_VTT

PC956 1U_0402_6.3V6K
PC957 1U_0402_6.3V6K
PC958 1U_0402_6.3V6K
PC959 1U_0402_6.3V6K
PC960 1U_0402_6.3V6K
PC961 1U_0402_6.3V6K
PC962 1U_0402_6.3V6K
PC963 1U_0402_6.3V6K
PC964 1U_0402_6.3V6K
PC965 1U_0402_6.3V6K
PC966 1U_0402_6.3V6K
PC967 1U_0402_6.3V6K
PC968 1U_0402_6.3V6K
PC972 1U_0402_6.3V6K
PC973 1U_0402_6.3V6K
PC974 1U_0402_6.3V6K
PC975 1U_0402_6.3V6K
PC976 1U_0402_6.3V6K
PC977 1U_0402_6.3V6K
PC978 1U_0402_6.3V6K
PC979 1U_0402_6.3V6K
PC980 1U_0402_6.3V6K
PC981 1U_0402_6.3V6K
PC982 1U_0402_6.3V6K
PC983 1U_0402_6.3V6K
PC984 1U_0402_6.3V6K
PC985 10U_0603_6.3V6M
PC986 10U_0603_6.3V6M
PC987 10U_0603_6.3V6M
PC988 10U_0603_6.3V6M
PC989 10U_0603_6.3V6M
PC990 10U_0603_6.3V6M
PC991 10U_0603_6.3V6M
PC992 10U_0603_6.3V6M
PC993 10U_0603_6.3V6M
PC994 10U_0603_6.3V6M
PC995 330U_D2_2V_Y

ESR=9m ohm

+CPU_CORE

PC902 22U_0402_6.3V6M
PC903 22U_0402_6.3V6M
PC904 22U_0402_6.3V6M
PC905 22U_0402_6.3V6M
PC906 22U_0402_6.3V6M
PC907 22U_0402_6.3V6M
PC908 22U_0402_6.3V6M
PC909 22U_0402_6.3V6M
PC920 22U_0402_6.3V6M
PC921 22U_0402_6.3V6M
PC922 22U_0402_6.3V6M
PC923 22U_0402_6.3V6M
PC924 22U_0402_6.3V6M
PC925 22U_0402_6.3V6M
PC926 22U_0402_6.3V6M
PC927 22U_0402_6.3V6M

For BOT side

+CPU_CORE

PC934 22U_0805_6.3V6M
PC935 22U_0805_6.3V6M
PC936 22U_0805_6.3V6M
PC937 22U_0805_6.3V6M
PC938 22U_0805_6.3V6M
PC939 22U_0805_6.3V6M
@PC940 22U_0805_6.3V6M
PC949 22U_0805_6.3V6M
PC950 22U_0805_6.3V6M
PC951 22U_0805_6.3V6M
PC952 22U_0805_6.3V6M
PC953 22U_0805_6.3V6M
PC954 22U_0805_6.3V6M
@PC955 22U_0805_6.3V6M

For TOP side

+CPU_CORE

PC969 330U_D2_2V_Y
PC970 330U_D2_2V_Y
PC971 330U_D2_2V_Y

ESR=9m ohm

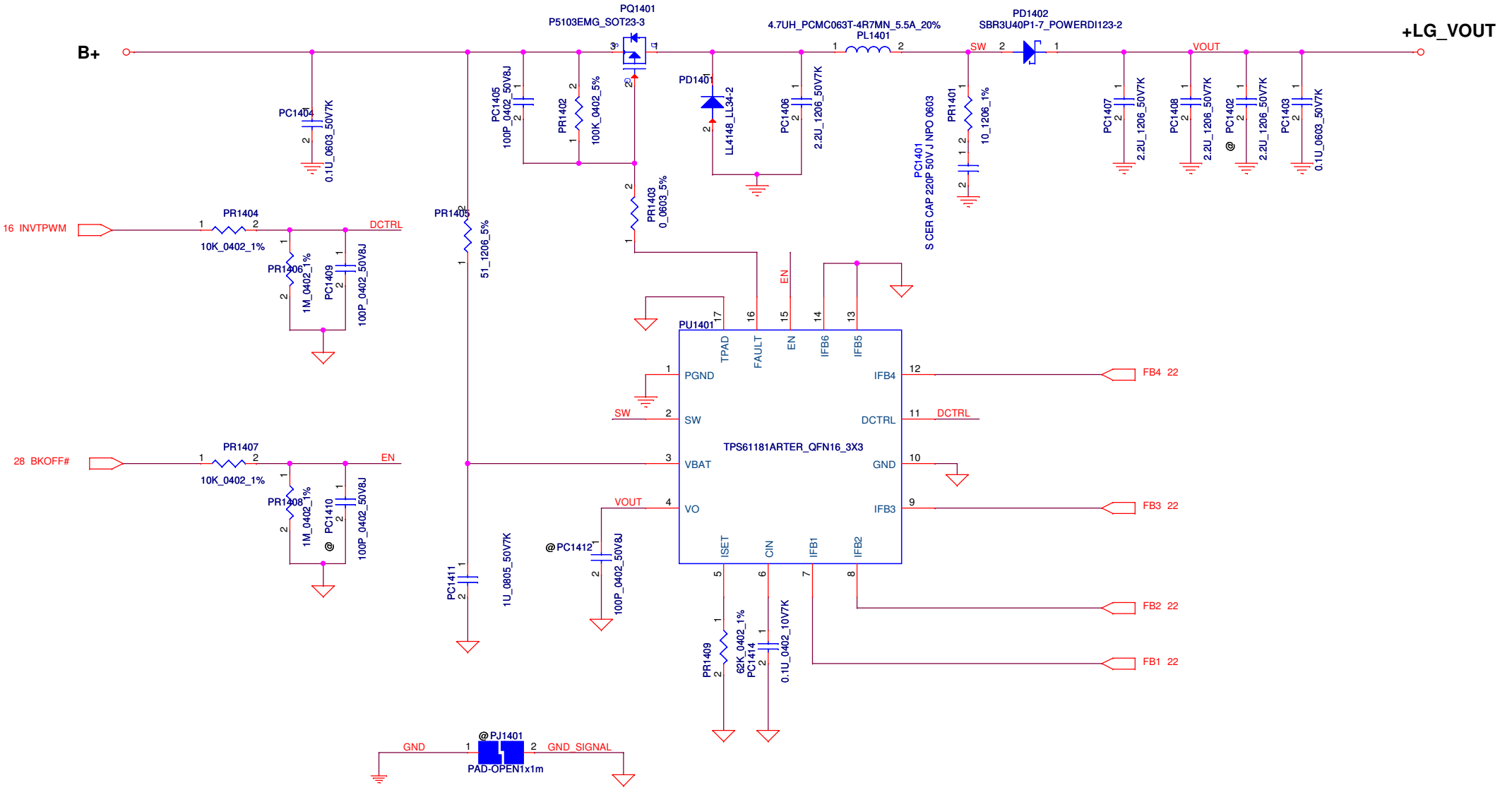
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	Date of EOP

Compal Electronics, Inc.

Title: *CPU_CORE_CAP*

Size: Custom | Document Number: *SAGE 3G* | Rev: 1.0

Date: | Sheet 43 of 52



Compal Electronics, Inc.

Title: LED Converter

Size	Document Number	Rev
Custom	SAGE 3G	0.1

Date: Wednesday, March 13, 2013 Sheet 44 of 52

Version change list (P.I.R. List)

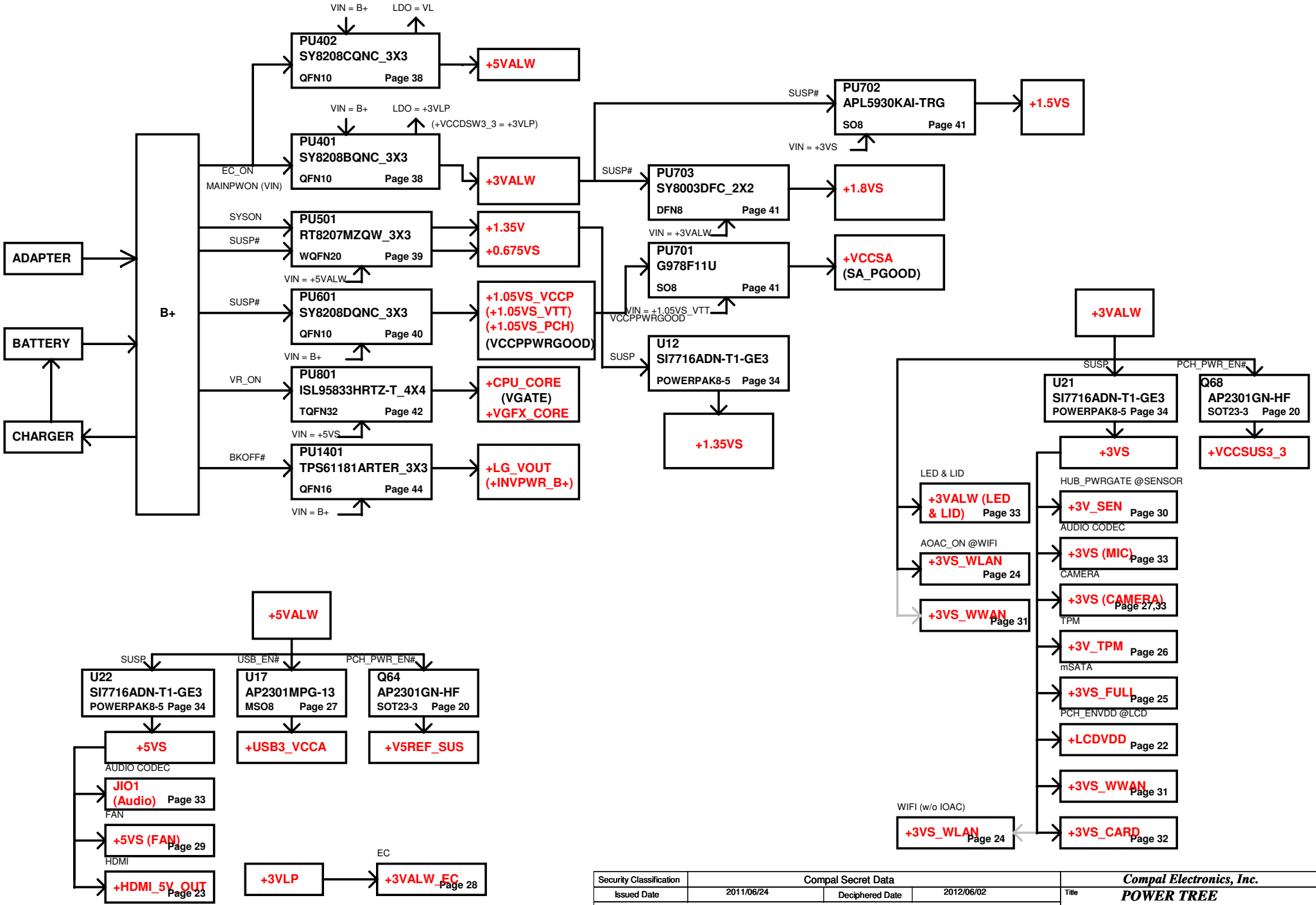
Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Design Change.	Design Change of IC Application.	0.2	38	Add @PR410.@PR414 to SD028100180(S RES 1/16W 1K +-5% 0402) Add @PC429 to SE075472K80(S CER CAP 4700P 25V K X7R 0402) Add @PC428 to SE075472K80(S CER CAP 0.047U 25V K X7R 0402) Add PR412.@PR413.PR415 to SD028000080(S RES 1/16W 0 +-5% 0402)	2012/12/13	DVT
2	Design Change.	Design Change of IC Application.	0.2	44	Delete PC1413.	2012/12/13	DVT
3	Add Adapter Detection Circuit.	Design Change of DC Jack Application.	0.2	35 37	Add PR325 to SD028000080(S RES 1/16W 0 +-5% 0402) Add PR321.PR323 to SD028100380(S RES 1/16W 100K +-5% 0402) Add PQ307 to SB201440000(S TR PDTA144EU PNP SOT323) Add PQ308 to SB301150200(S TR PDTC115EU NPN SOT323)	2012/12/13	DVT
4	Design Change.	Design Change of IC Application.	0.2	42	Change PC831 to SE075682K80(S CER CAP 6800P 25V K X7R 0402) Change PC832 to SE071560J80(S CER CAP 56P 50V J NPO 0402)	2012/12/24	DVT
5	Change Component Part Number.	Factory lack of material.	0.2	44	Change PL1401 to SH000006J80 (S COIL 4.7UH +-20% PCMC063T-4R7MN 5.5A)	2012/12/24	DVT
6	Change Component Part Number.	Factory lack of material.	0.2	42	Change PC841 to SGA00007I00 (S POLY C 33U 25V M D2 ESR60M TQC H1.9)	2012/12/26	DVT
7	Change Component Part Number.	X1 Code.	0.2	44	Change PD1402 to SCS00005Y00 (S SCH DIO SBR3U40P1-7 POWERDI123-2)	2012/12/26	DVT
8	Design Change.	Design Change of IC Application.	0.3	38	Delete PR412.PR413.PR415.	2012/01/29	PVT
9	Design Change.	Design Change of IC Application.	0.3	38	Change @PR410.@PR414.@PC428.@PC429 to PR410.PR414.PC428.PC429.	2012/01/29	PVT
10	Design Change.	Design Change of IC Application.	0.3	38	Change PC428 to SE075682K80(S CER CAP 6800P 25V K X7R 0402) Change PC429 to SE072103Z80(S CER CAP .01U 25V Z Y5V 0402)	2013/02/22	PVT
11	Design Change.	Design Change of Adapter Detection.	0.4	37	Change PQ307 to SB000009Q80(S TR 2N7002KW 1N SOT323-3) Add PR325 to SD028100380(S RES 1/16W 100K +-5% 0402)	2013/02/23	Pre MP

Compal Electronics, Inc.

Title: *PIR (PWR)*

Size: Custom | Document Number: *EG51_HX M/B LA-9491P Schematics* | Rev: 1.0

Date: | Sheet 45 of 52



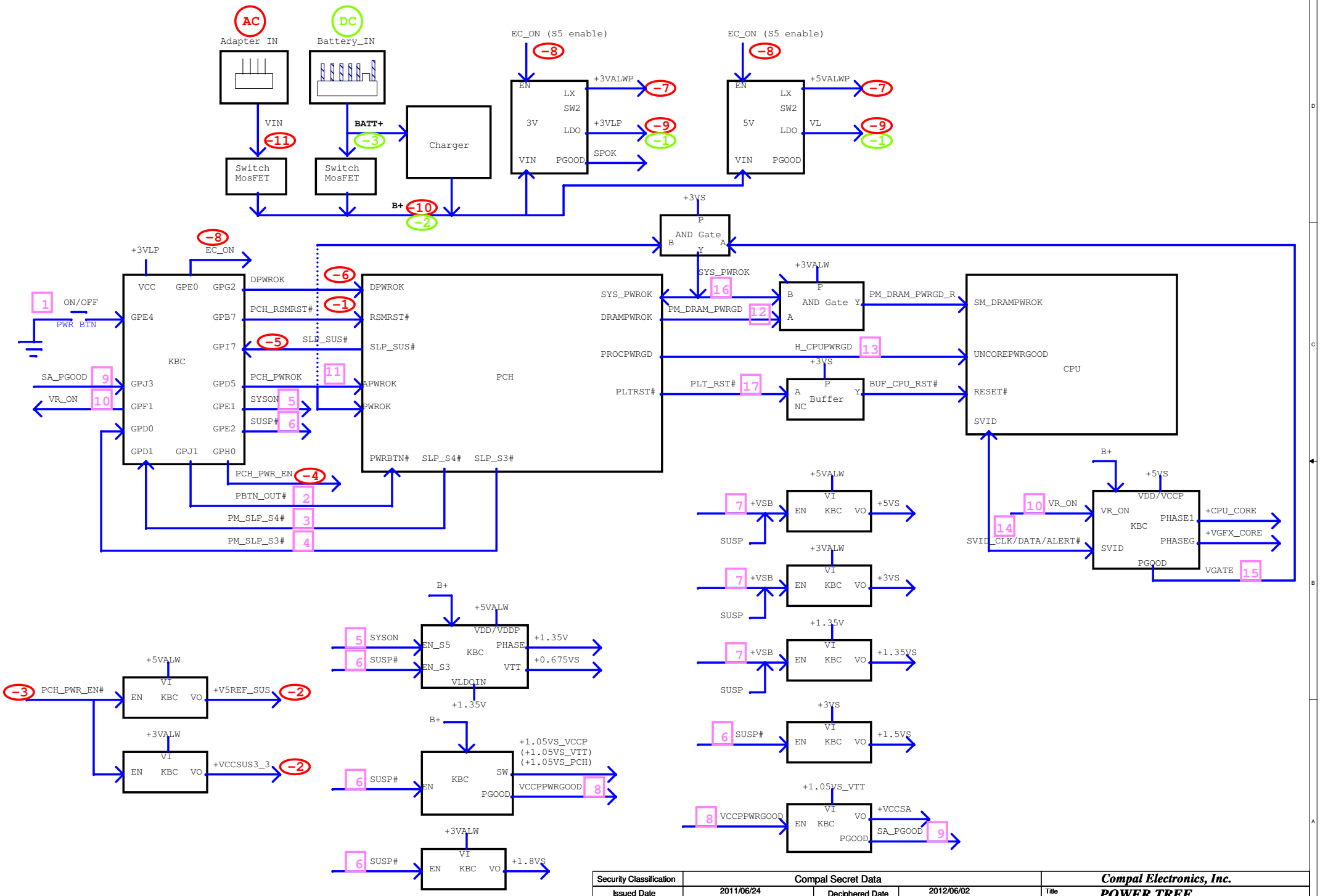
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

Compal Electronics, Inc.

Title: POWER TREE

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

Date: Wednesday, March 13, 2013 | Sheet 46 of 52



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

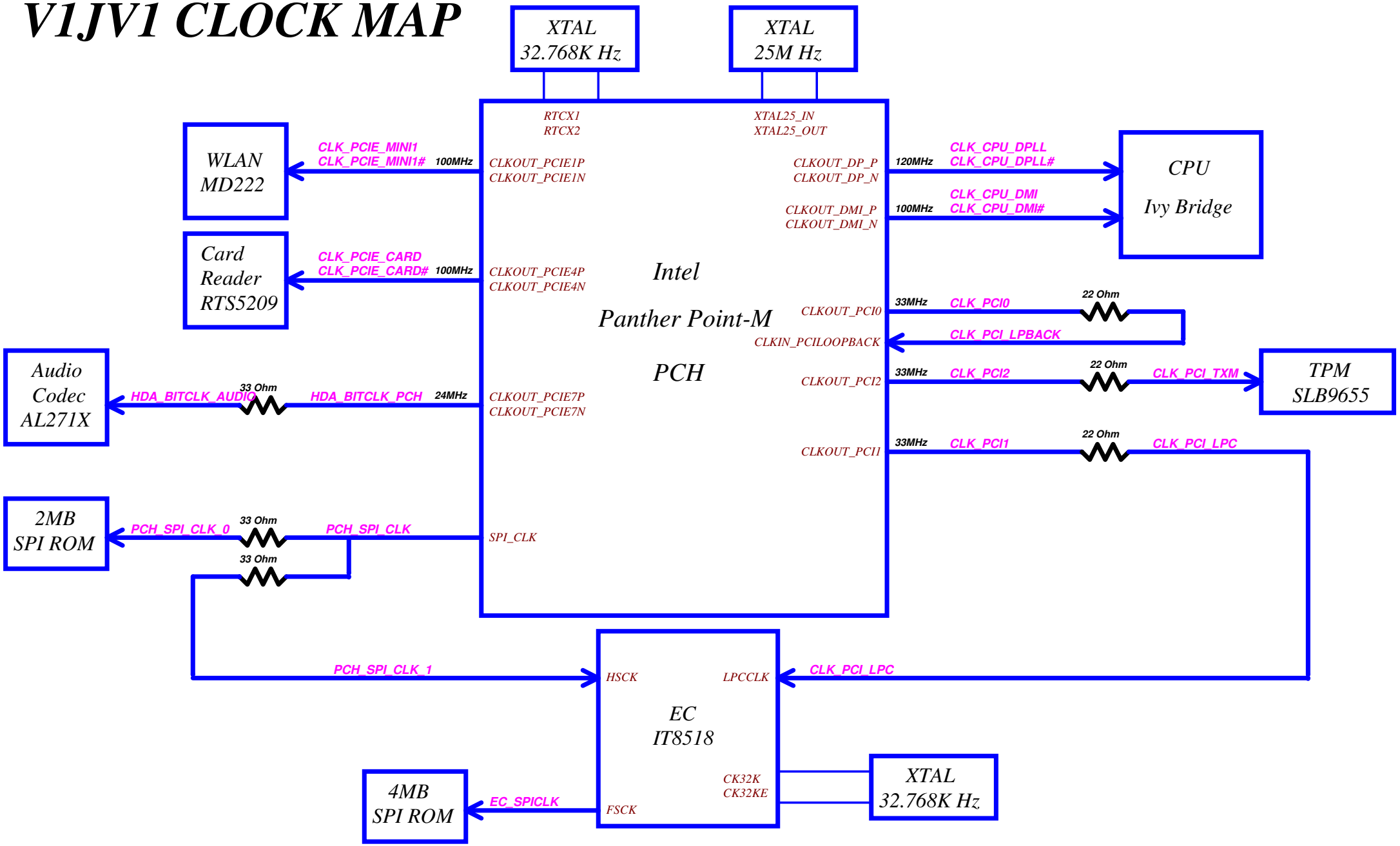
Compal Electronics, Inc.

Title: POWER TREE

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

Date: Wednesday, March 13, 2013 | Sheet 47 of 52

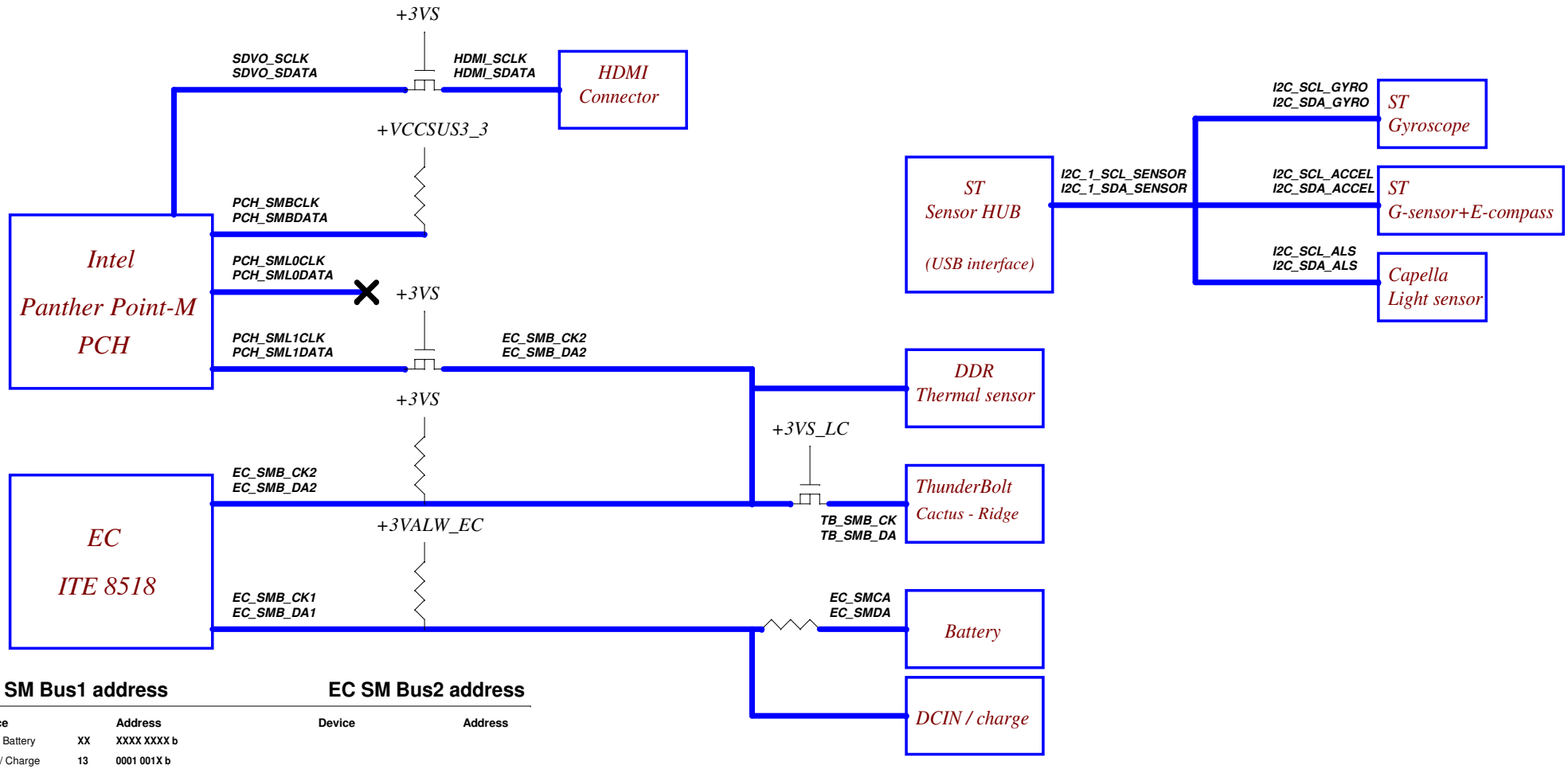
V1JV1 CLOCK MAP



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

Compal Electronics, Inc.			
Title: CLOCK MAP			
Size: Custom	Document Number: V1JB1 M/B LA-A041P Schematic		Rev: 0.1
Date: Wednesday, March 13, 2013	Sheet 48 of 52		

SMBUS Block Diagram



EC SM Bus1 address

Device		Address
Smart Battery	XX	XXXX XXXX b
DCIN / Charge	13	0001 001X b

EC SM Bus2 address

Device	Address

PCH SM Bus address

Device		Address
ST sensor HUB	XX	XXXX XXXX b

PCH SM Bus address(Link 1)

Device		Address
DDR Thermal sensor	99	1001 101X b
Thunderbolt	29	0010 100X b(CIO P1)
	2B	0010 101X b(CIO P2)
	2D	0010 110X b(CIO P3)
	2F	0010 111X b(CIO P4)

Sensor HUB SM Bus address

Device		Address
Gyroscope	D1	1101 000X b
	D3	1101 001X b
E-compass + G sensor	33	0011 001X b
ALS sensor	21	0010 000X b

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

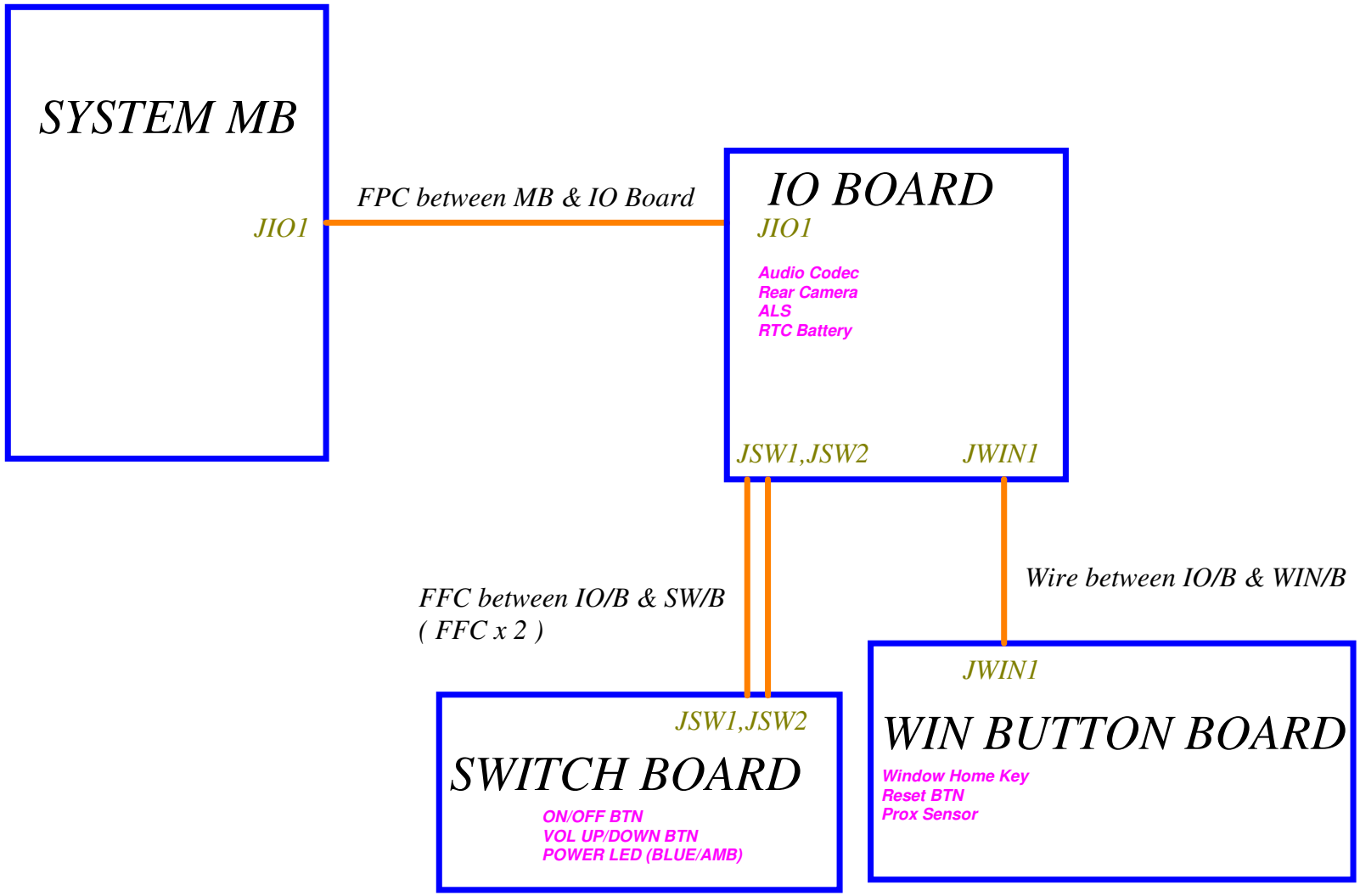
Compal Electronics, Inc.

Title: SMBUS Block Diagrams

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

Date: Wednesday, March 13, 2013 | Sheet 49 of 52

V1JB1 SYSTEM Diagram



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/06/02

Compal Electronics, Inc.		
Title: SYSTEM MAP		
Size: Custom	Document Number: V1JB1 M/B LA-A041P Schematic	Rev: 0.1
Date: Wednesday, March 13, 2013	Sheet 50 of 52	

Version Change List (P. I. R. List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

DVT

01. Add net " IO/B_DET" to detect IO/B
    - Avoid thermal sensor wrong action by remote mode cause system auto shut down
02. Add 3 clips at ext USB area (RF requirement)
03. Move D_LOCK pull up resistor from IO/B to M/B side (Reserve function)
04. Move ON/OFFBTN# circuit from IO/B to M/B side(Sub/B just SW BTN only)
05. Change R960 to 8.2k ohm (Board ID update)
06. Change RP19, RP20 package to R_0402*8 (HDMI signal fine tune requirement)
07. Change C451,C450 BOM structure to XEMC@
08. Delete R78 for Layout components reduce
09. Change SIM Card Connecotor as MOLEX_503960-0694 (ME requirement)
10. Change C548 to 0 ohm resistor (3G power from +3VS, not +3VALW)
11. Base on crystal vender suggest, change C756, C757 to 15pF, C744 & C745 to 12pF

PVT

01. Add test point at CPU pin B22, A19, B14, A11, B10, B6 (DFB requirement)
02. Modify EC_RST# circuit for Reset Button (Dual Mosfet)
03. Add ODT1, CKE1, CS1# net to DDR for 8Gb DRAMs
04. Remove EC_ON, MAINPWON net from JIO1 (un-used net)
05. Change R960 to 18k ohm (Board ID update)
06. Change R185, R186, R720 to short pad
07. Change R637 to 33 ohm (3G PWR SEQ)
08. Reserve 0 ohm resistor to GND for sensor PB13 as ST suggestion
09. Remove Screw "H18" (ME outline modify)
10. Unstuff 3G power switch circuit (un-used -> 3G power source tie to +3VS directly)
11. Add 3G@ BOM option for WiFi only sku
12. Change R499, R503, R504 from 10k to 100k for DS5 power consumption

R10

01. Change RP43 part number from SD302220A00(22 ohm) to SD309220A80 (22 ohm) for Green BOM request
02. Unstuff component of reserve circuit (un-used function) ->
    R503, Q7 (SIM_DET# to EC), R504 (EC_3G_ON_OFF#), R260, R311, R505, C407 (3G Ext. RST#)
03. Change R960 to 33k ohm (Board ID update)
04. Unstuff R485 to avoid leakage to wlan module (3G provide power when S3/DS3)
05. Unstuff SW5 (for test phase only, MP remove)
06. Update PCB PN to R10
07. As source request (cancel vender-Cheng Hann), change below parts~
    1. Change L23 PN from SM01000AX00 to SM01000EP00
    2. Change L3, L4, L36, L38, L39, L40, L53, L68 PN from SM070001600 to SM070001E00
    3. Change L52 PN from SM070001310 to SM070001E00

R20

01. Add USB switch to 3G USB signals for avoid DS3 leakage
02. Delete Q7, R503 (un-used component)
03. Rename EC_SIM_DET# to EC_3G_PWR_EN# (correct net name to meet actual function)
04. Change EC GPD7 (U53.M12) to EC_3G_USB_ON for 3G USB switch
05. Change R960 to 56k ohm (Board ID update)
06. Update PCB PN to R20

Security Classification	Compal Secret Data		
Issued Date	2011/06/13	Deciphered Date	2012/06/13

Compal Electronics, Inc.

Title: EE P.I.R

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

Date: Tuesday, March 26, 2013 | Sheet 51 of 52

PCB

ZZZ1

LA-A041P MB Rev0: DAA0006P000
LA-A041P MB Rev1: DAA0006P010
LA-A041P MB Rev2: DAA0006P020

LA-A041P REV2
DAA0006P020

CPU

UCPU1
I33217@
S IC AV8063801058401 SR0N9 L1 1.8G ABO!
SA00005L5C0
AV8063801058401 SR0N9 L1 1.8G ABO!

UCPU1
I53317@
S IC AV8063801058002 SR0N8 L1 1.7G ABO!
SA00005K6B0
AV8063801058002 SR0N8 L1 1.7G ABO!

UCPU1
I32365M@
S IC AV8062701313000 SR0U3 J1 1.4G ABO!
SA00005UH40
AV8062701313000 SR0U3 J1 1.4G ABO!

WLAN/BT Module

U1
LIONMD222@
PK29S004B00
S_W/L_MOD WCBN3501A W/BT MD222 ABO!
WCBN3501A W/BT MD222

UCPU1
I33227@
S IC AV8063801119500 SR0XF L1 1.9G ABO!
SA00006D990
AV8063801119500 SR0XF L1 1.9G ABO!

UCPU1
I53337@
S IC AV8063801129900 SR0XL L1 1.8G ABO!
SA00006D860
AV8063801129900 SR0XL L1 1.8G ABO!

UCPU1
I32375M@
S IC AV8062701313100 SR0U4 J1 1.5G ABO!
SA00006ED50
AV8062701313100 SR0U4 J1 1.5G ABO!

SAGE 3G

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: Option Component

Size: Custom | Document Number: V1JB1 M/B LA-A041P Schematic | Rev: 0.1

Date: Thursday, March 14, 2013 | Sheet 52 of 52