

Compal Confidential

Huayra UMA (QCL51) Schematics Document

AMD Comal Platform

AMD Trinity APU / Hudson FCH / ATI Thames XT M2

Muxless/UMA / PX 5.0

2012-01-04

LA-8714P REV: 0.3

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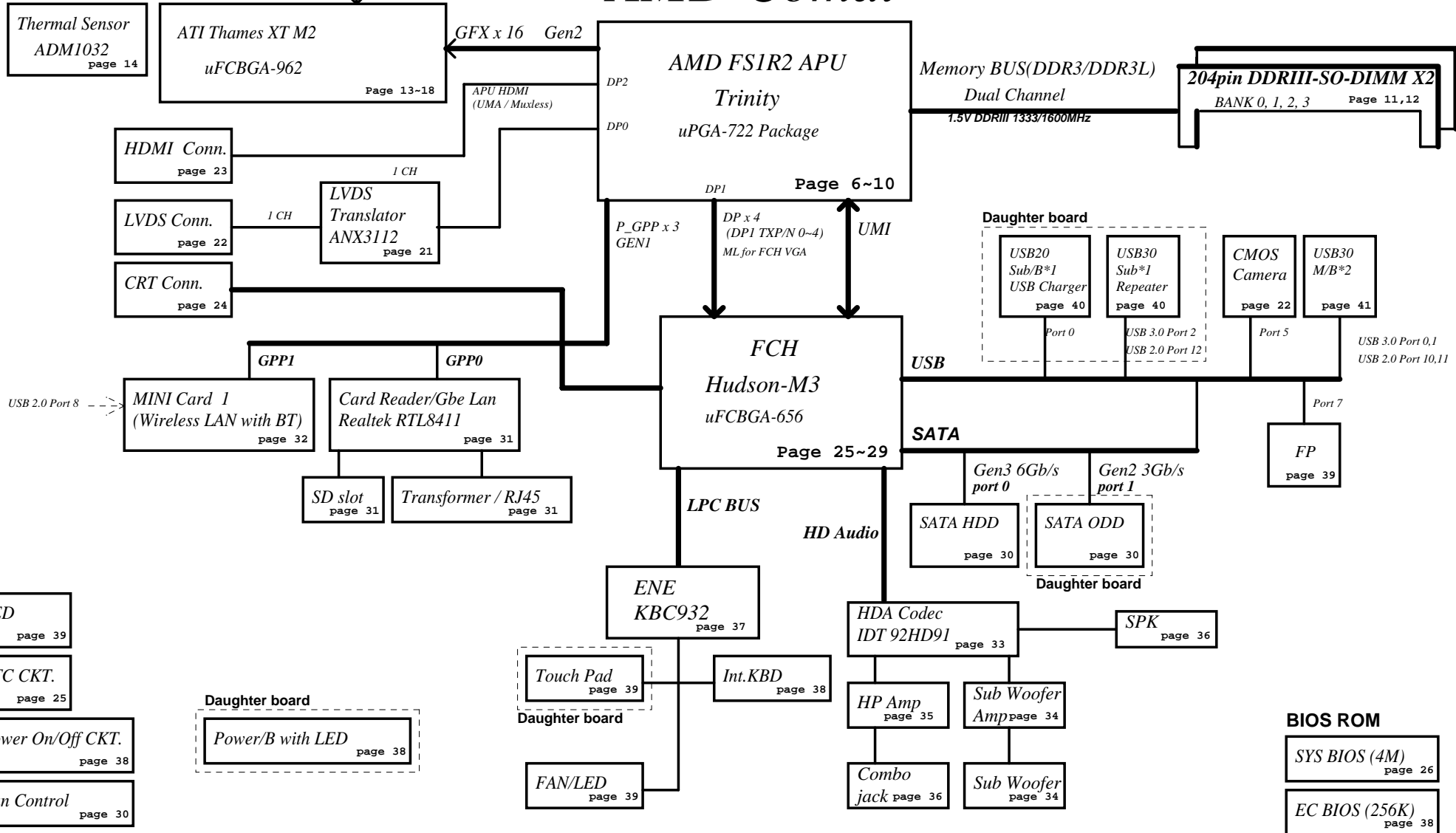
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Model Name : QCL51 AMD
Board Name : LA-8712P

64M x16
128M x 16
VRAM DDR3
page 19, 20

DDR3

AMD Comal



- LED page 39
- RTC CKT. page 25
- Power On/Off CKT. page 38
- Fan Control page 30
- DC/DC Interface CKT. page 42
- Power Circuit page 44-56

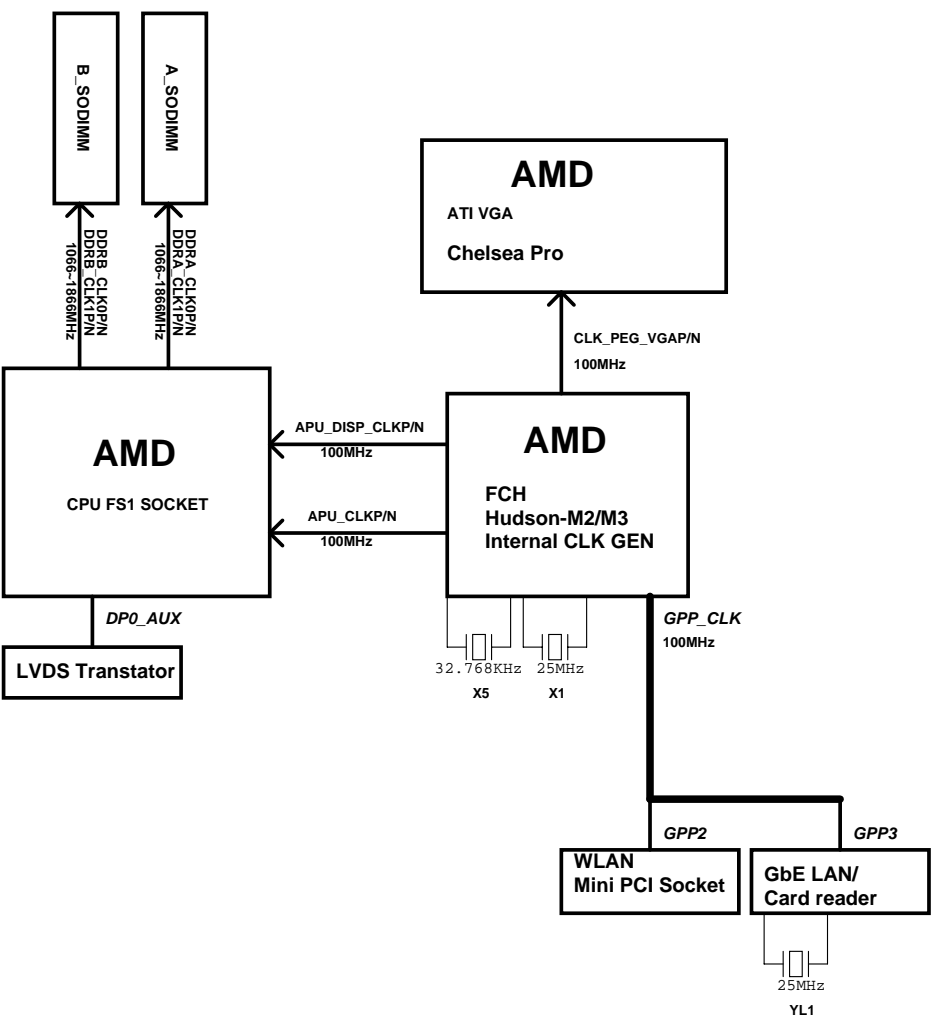
Daughter board
Power/B with LED page 38

Daughter board
Touch Pad page 39

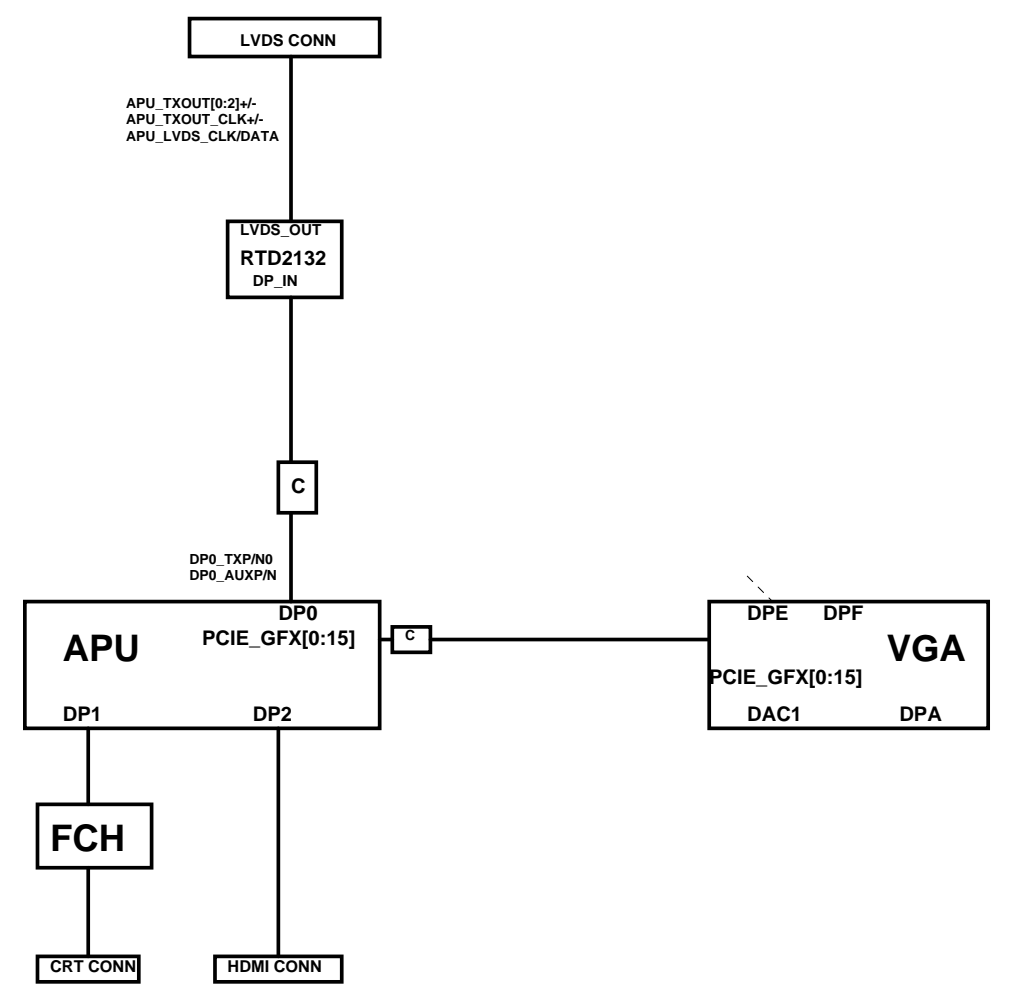
Daughter board
SATA HDD page 30
SATA ODD page 30

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CLOCK DISTRIBUTION



DISPLAY OUTPUT



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+VDDCI	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+0.935VGS	0.935V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5V_PCIE	1.5V switched power rail	ON	OFF	OFF
+1.8VGS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+LAN_VDD_3V3	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

x = 1 is read cmd, x= 0 is writee cmd.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

EC SM Bus2 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	ADI ADM1032 (GPU)	1001 101X b	9AH
			SB-TSI (APU)	1001 100X b	98H
			LVDS TR	1010 100X b	A8H
			VGA Internal Thermal	1000 001X b	82H

FCH (S0)

SM Bus 0 address

FCH (S0~S5)

SM Bus 1 address

Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1010 000X b	A0	Touch pad		
DDR DIMM2	1010 001X b	A2			
Amplifier					

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

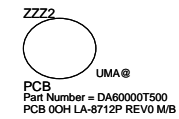
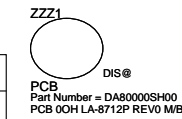
Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rb	100K +/- 5%			
Board ID	Ra / Rb	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	1.8K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOM Option Table

BOM Structure	Description	DIS	PX@ DIS@ Tha@
PX@	PX function	UMA	UMA@
DIS@			
UMA@			
Tha@			

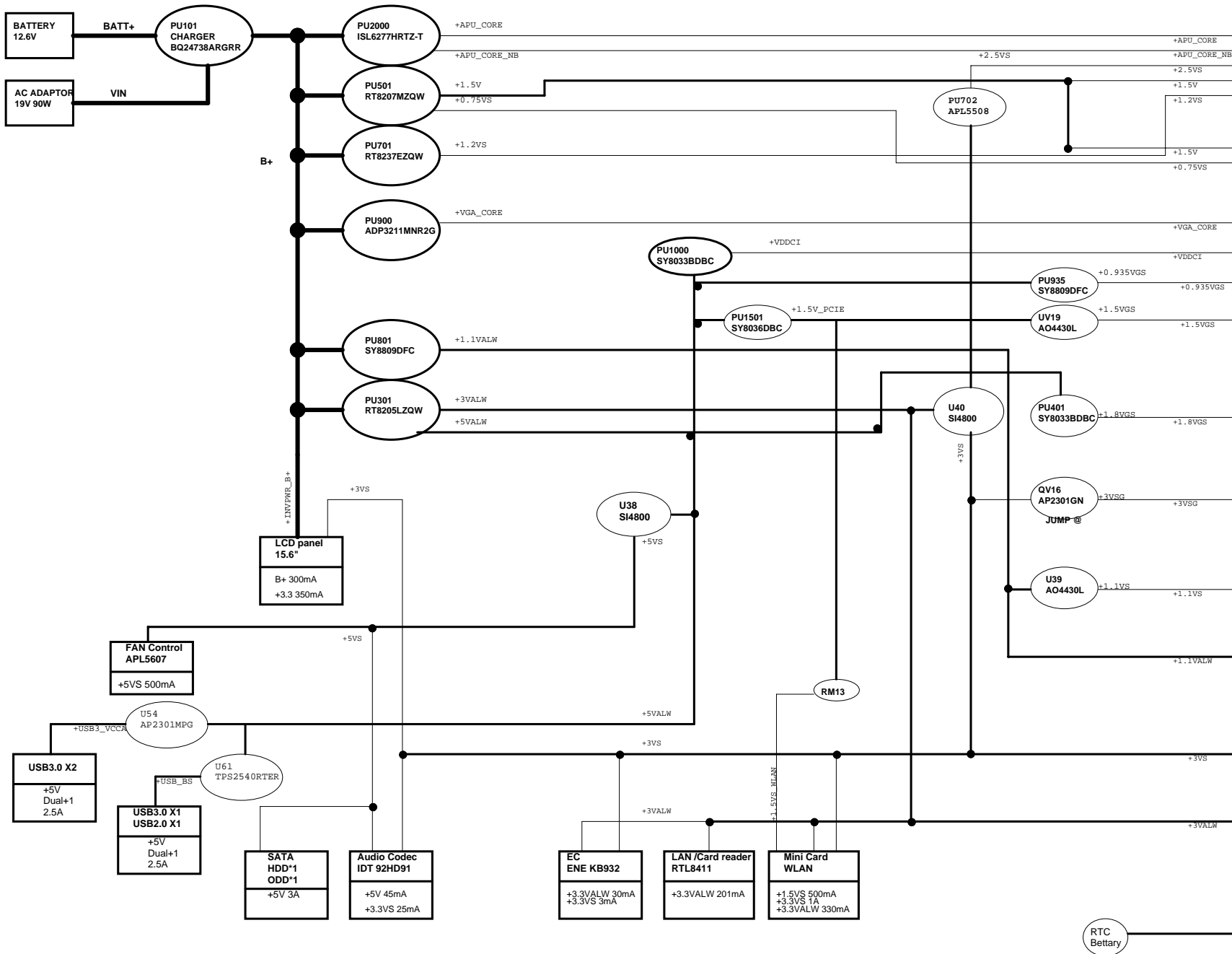
BOM Config



BOARD ID Table

Board ID	PCB Revision
0	DB
1	SI

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AMD APU FS1R2	
0.7-1.475V	VDD CORE 60A
0.7-1.475V	VDDNB 44A
+2.5VS	VDDA 0.5A
+1.5V	VDDIO 3.2A
+1.2VS	VDDR 8.5A

RAM DDRIII SODIMMx2	
+1.5V	VDD_MEM 4A
+0.75VS	VTT_MEM 0.5A

VGA ATI Chelsea Pro	
0.85-1.1V	VDDC 28A
0.9-1.0V	VDDCI 4.6A
+0.935VGS	DPLL_VDDC: 125 mA SPV10: 100 mA PCI_E_VDDC: 1100 mA DP[A,E]_VDD10: 880 mA
+1.5VGS	VDDR3: 1200 mA
+1.8VGS	PLL_PVDD: 75 mA TSVDD: 5 mA AVDD: 70 mA VDD1DI: 45 mA VDD_CT: 17 mA PCI_E_VDDR: 440 mA DP[A,F]_VDD18: 990 mA SPV18: 50 mA MPV18: 150 mA
+3VGS	VDDR3: 60 mA

VRAM 512/1GB/2GB 64M / 128Mx16 * 4 / 8	
+1.5VGS	2.4 A

FCH AMD Hudson M3	
+1.1VS	VDDPL_11_DAC: 7 mA VDDAN_11_ML: 226 mA VDDCR_11: 1007 mA VDDAN_11_CLK: 340 mA VDDAN_11_PCIE: 1088 mA VDDAN_11_SATA: 1337 mA
+1.1VALW	VDDAN_11_USB_S: 140 mA VDDCR_11_USB_S: 42 mA VDDAN_11_SSUSB_S: 282 mA VDDCR_11_SSUSB_S: 424 mA VDDCR_11_S: 187 mA VDDPL_11_SYS: 70 mA VDDCR_11_GBE_S: 63 mA
+3VS	VDDIO_33_PCIEP: 102 mA VDDPL_33_SYS: 47 mA VDDPL_33_DAC: 20 mA VDDPL_33_ML: 12 mA VDDAN_33_DAC: 30 mA VDDPL_33_PCIE: 11 mA VDDPL_33_SATA: 12 mA VDDPL_33_USB_S: 14 mA
+3VALW	VDDPL_33_SSUSB_S: 11 mA VDDIO_AZ_S: 26 mA VDDAN_33_USB_S: 470 mA VDDIO_33_S: 59 mA VDDXL_33_S: 5 mA VDDAN_33_HWM_S: 12 mA VDDIO_GBE_S: 145 mA VDDIO_33_GBE_S: 2 mA
GND	VDDIO_33_GBE_S VDDCR_11_GBE_S VDDIO_GBE_S
RTC BAT	VDDBT_RTC_G

GPU

GPU

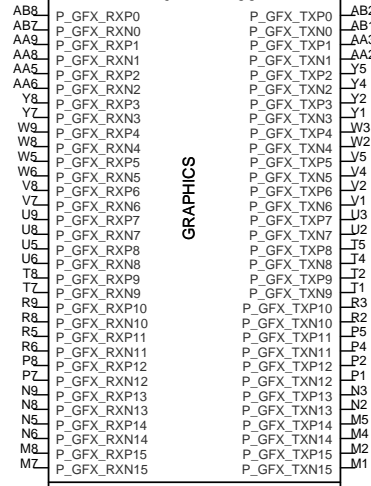
GLAN/Card reader
WLAN

GLAN/Card reader
WLAN

UMI

UMI

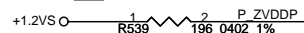
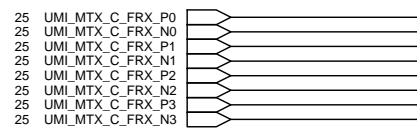
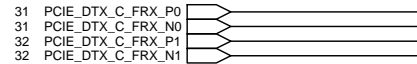
JCPU1A
PCI EXPRESS



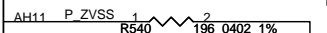
GRAPHICS

GPP

UMI



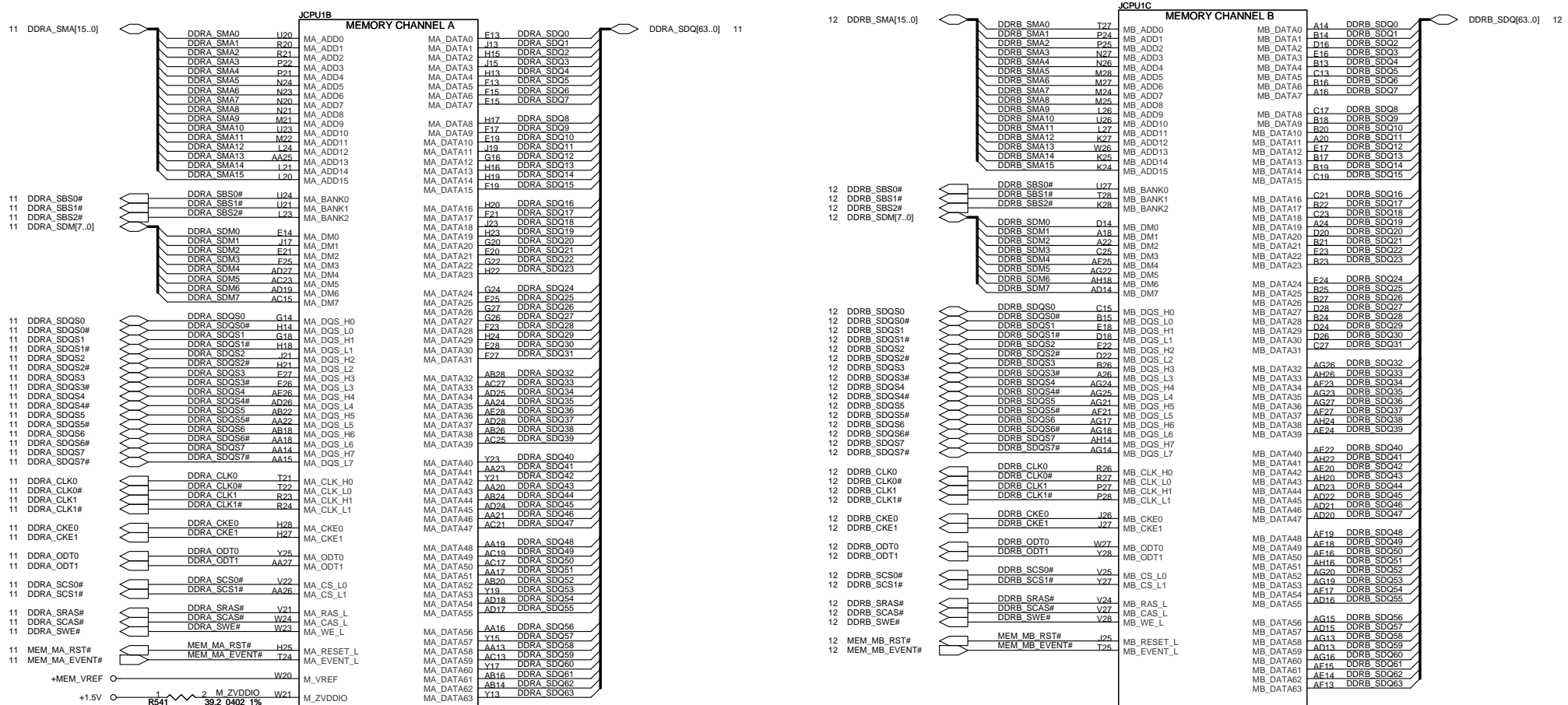
P_ZVDDP W/S=8/12 mil, <3000mil



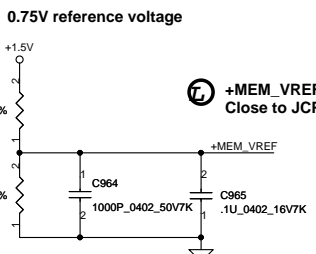
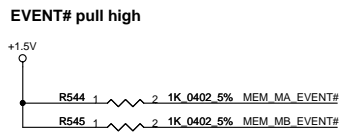
P_ZVSS W/S=8/12 mil, <3000mil

LOTES ACA-ZIF-109-P12-A_FS1R2
CONN@

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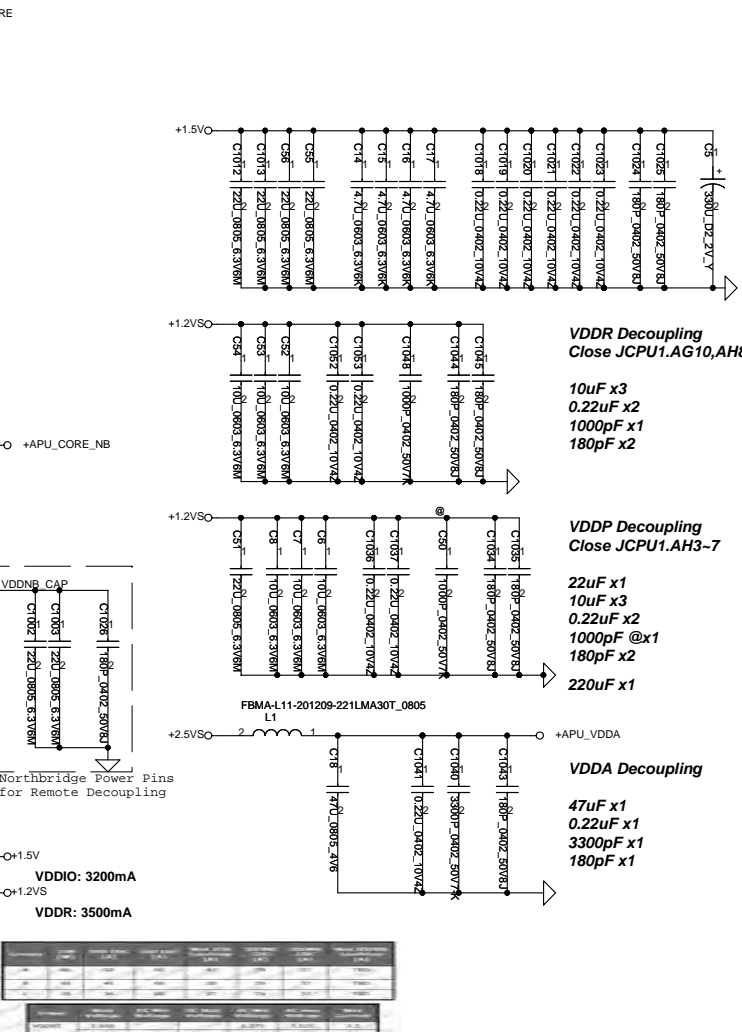
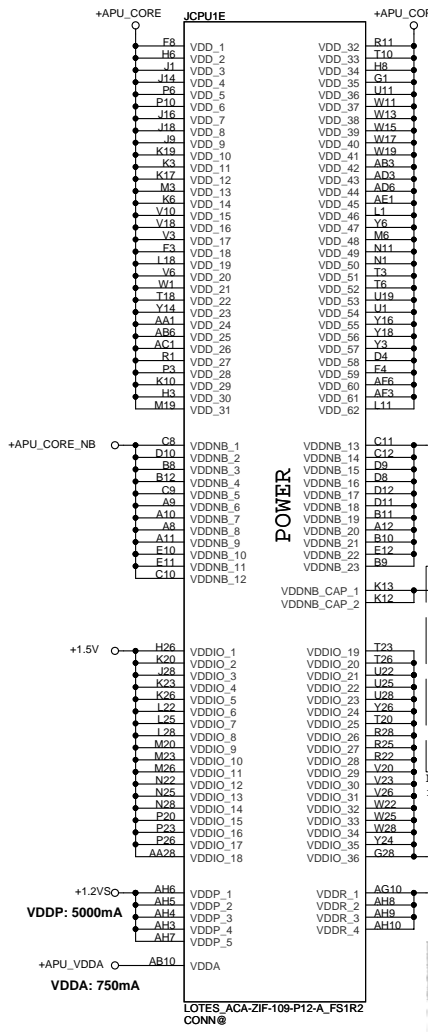


M_ZVDDIO W/S=8/12 mil, <1000mil



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Power Name	Consumption
VDD +CPU_CORE	60A
VDDNB +CPU_CORE_NB	37A
VDDIO +1.5V	3.2A
VDDP / VDDR +1.2VS	5A / 3.5A
VDDA +2.5VS	0.75A

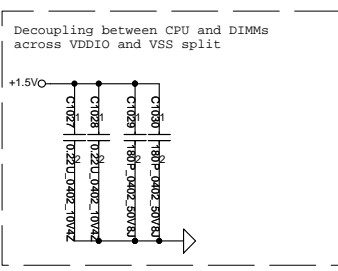


+CPU_CORE_NB Decoupling

- 330uF x2
- 22uF x2 @ x2
- 10uF x1
- 0.22uF x2
- 180pF x3

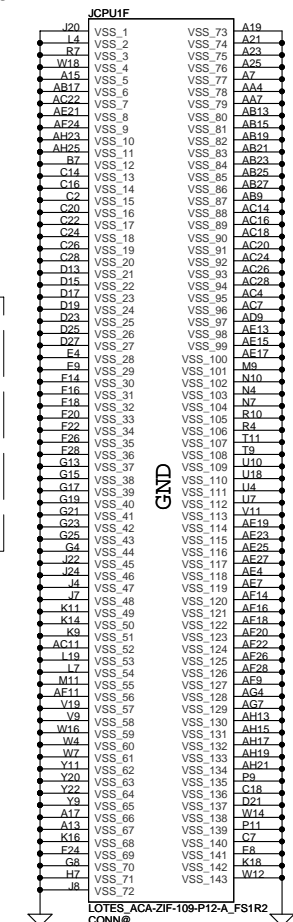
+1.5V / VDDIO Decoupling

- 330uF x1
- 22uF x4
- 4.7uF x4
- 0.22uF x6
- 180pF x1 @x1



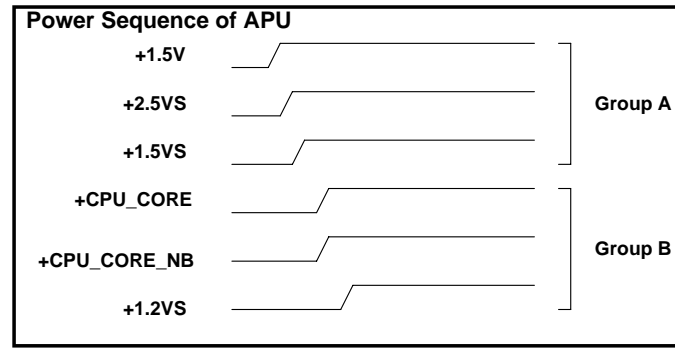
+CPU_CORE Decoupling

- 330uF x 4 @ x1
- 22uF x 10
- 0.22uF x 2
- 0.01uF x 3
- 180pF x 2 @ x1



Decoupling Caps.

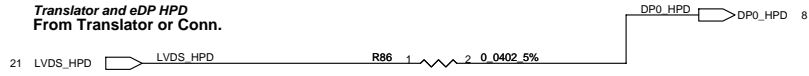
Pop / @	330uF	220uF	47uF	22uF	10uF	4.7uF	0.22uF	0.01uF	3300pF	1nF	180pF
Pumori 2.0	0	19/11	7	5	17	3	1	1 / 1	13/3		
Comal	7 / 2	1	1	19/11	7	4	17	3	1	1 / 1	14/2
P5WS5	7 / 2	1	1	13	3	8	19	3	1	4	16



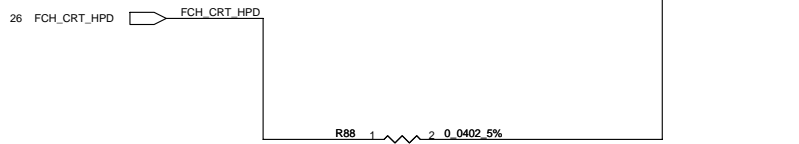
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HPD

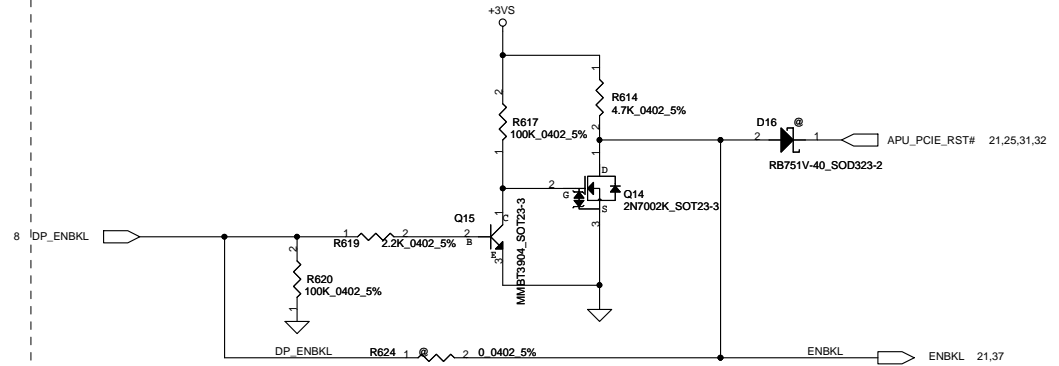
Translator and eDP HPD
From Translator or Conn.



CRT HPD
From FCH

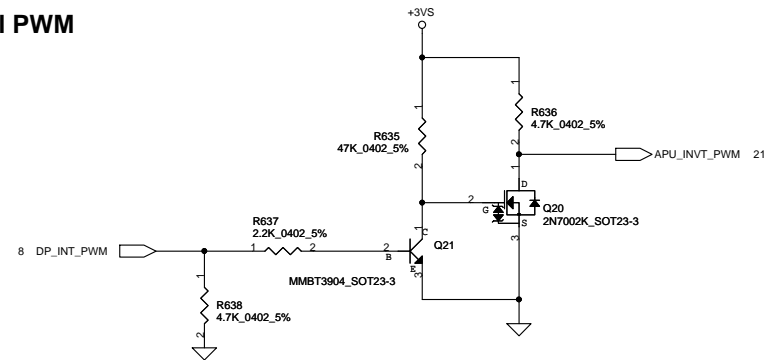


Panel ENBKL



eDP Panel ENVDD

Panel PWM



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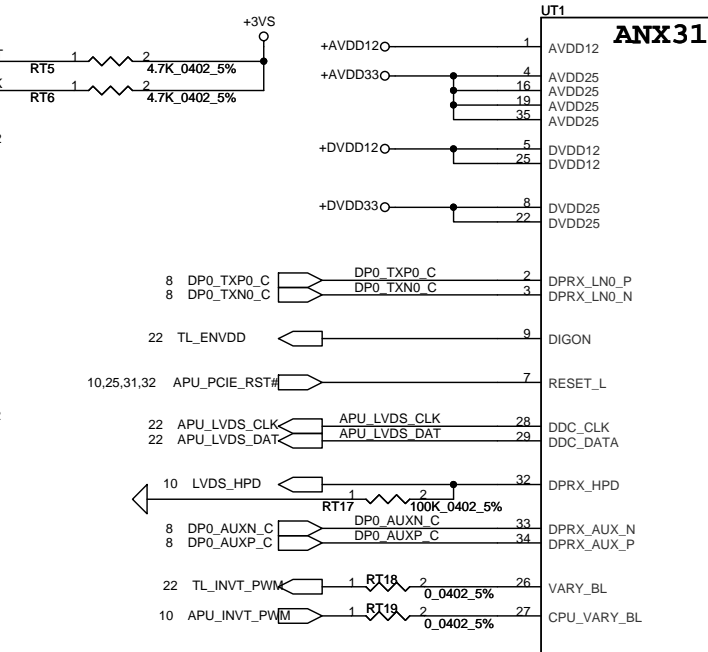
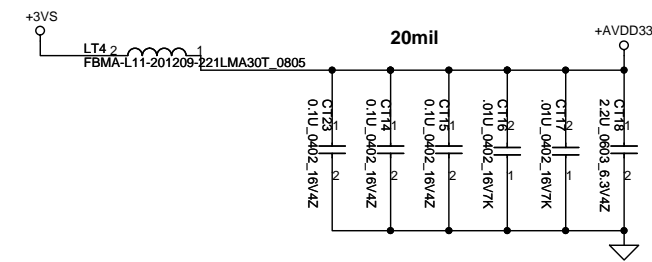
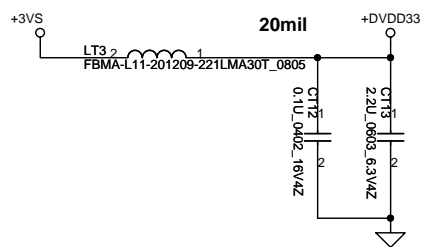
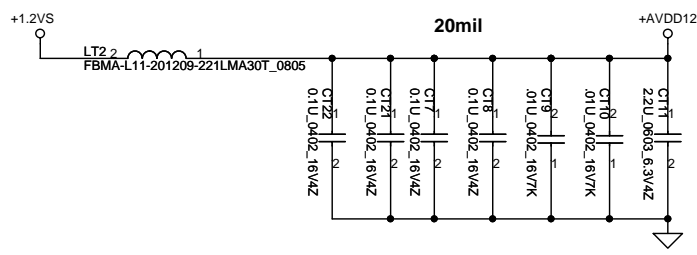
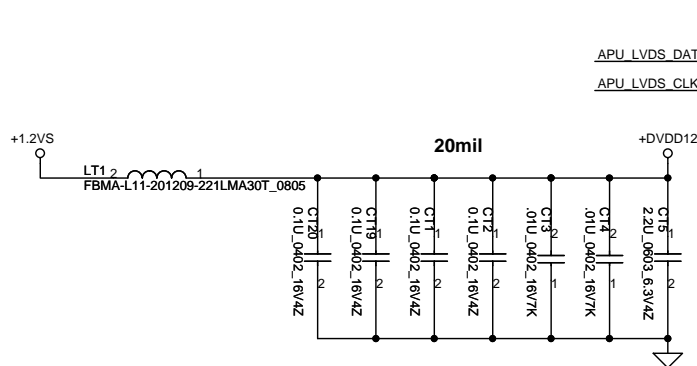
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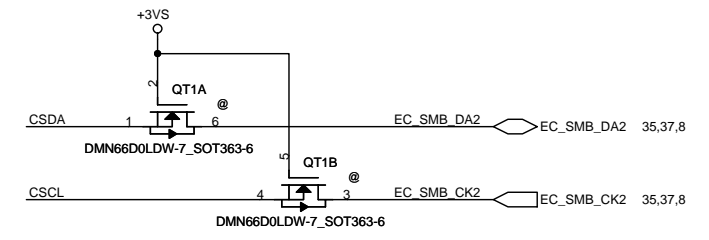
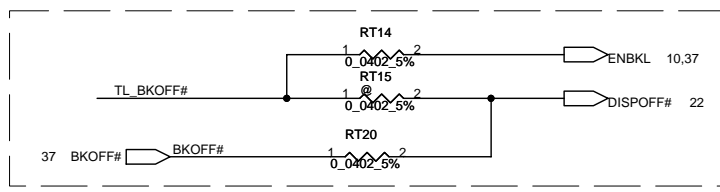
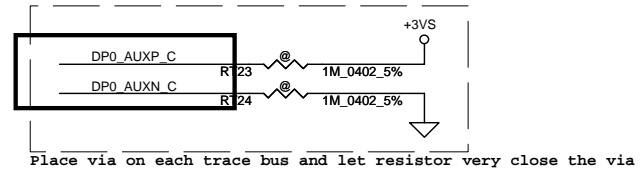
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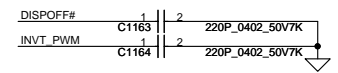
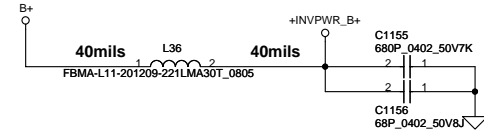
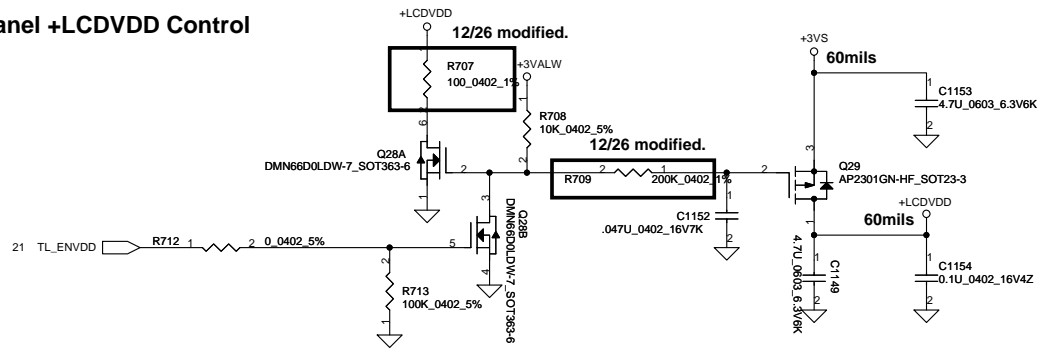
12/01 Swap DPO_AUXP_C/DPO_AUXN_C for vender guideline



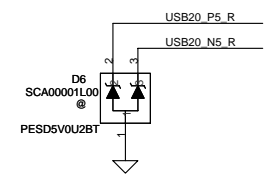
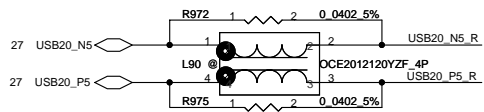
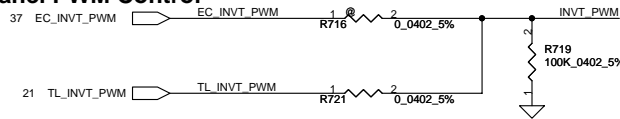
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Panel +LCDVDD Control

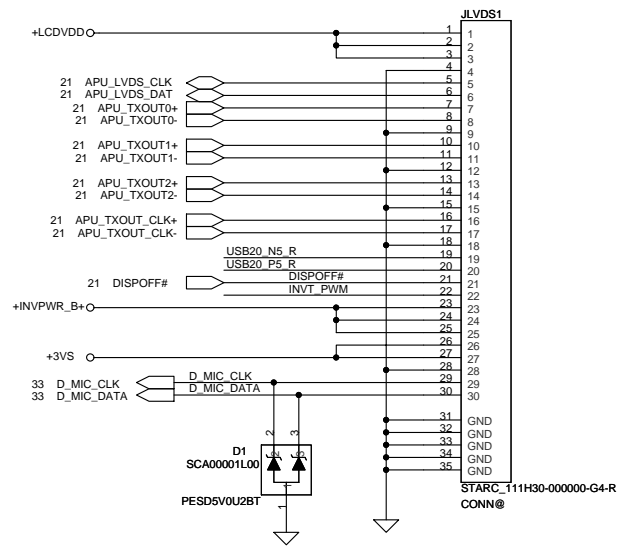


Panel PWM Control



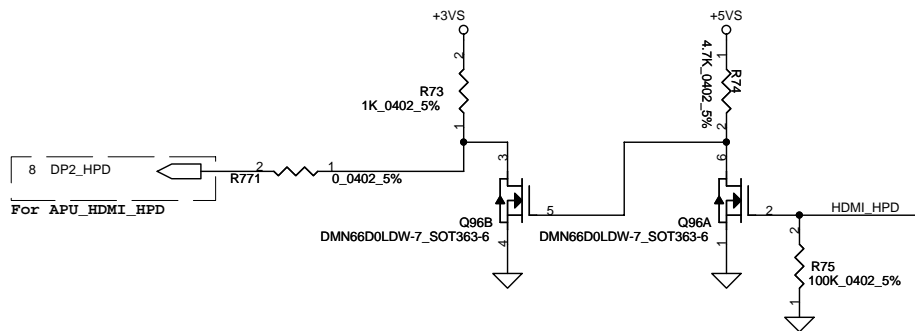
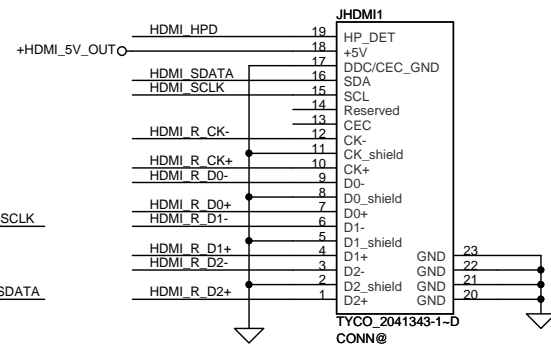
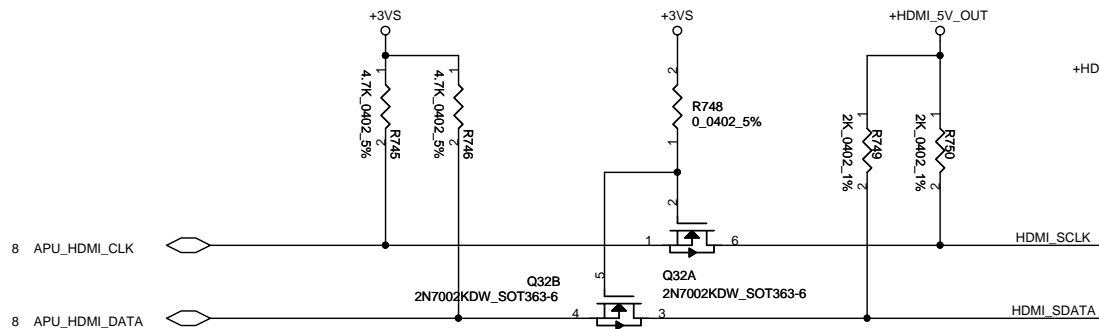
<Translator LVDS Output>

LVDS Connector

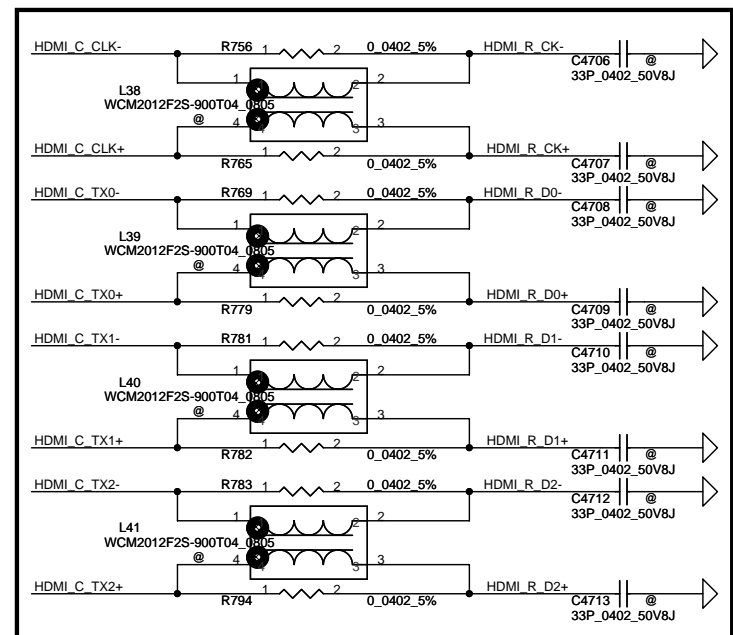


no updated.
11/10 follow QCL50

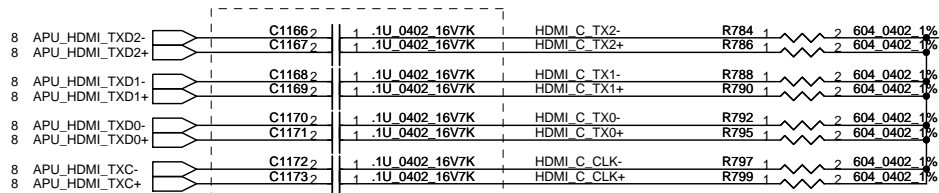
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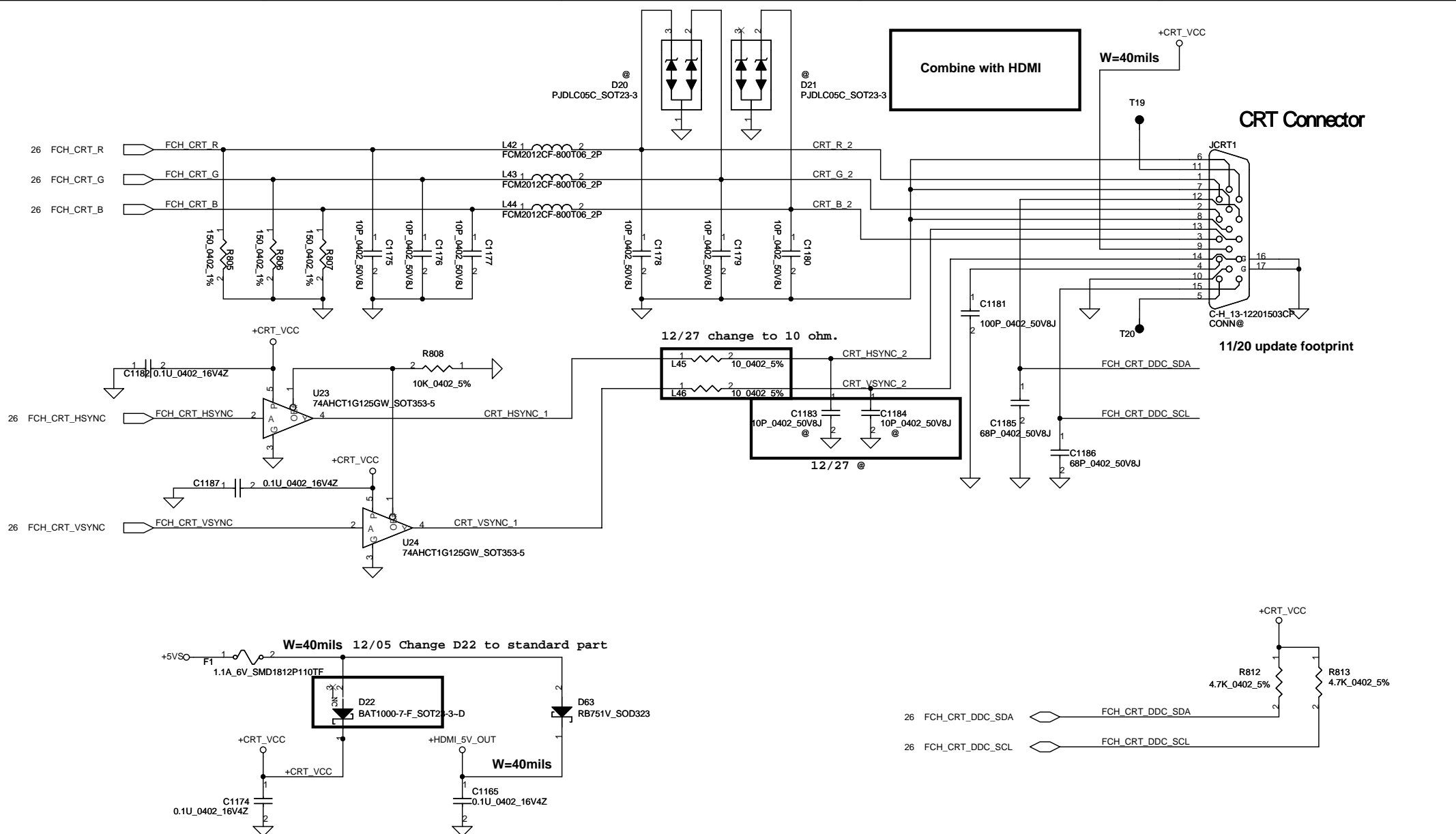
12/7 Swap signals for routing smoothly



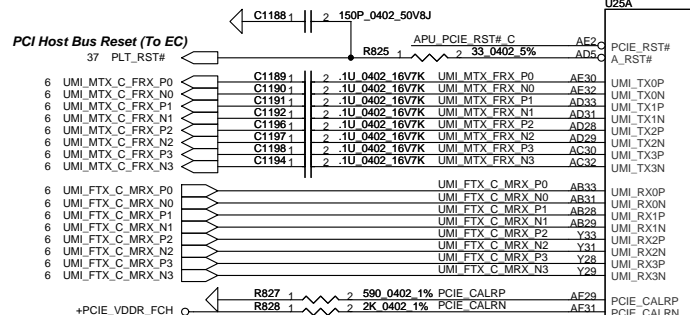
Close to HDMI conn



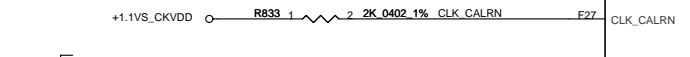
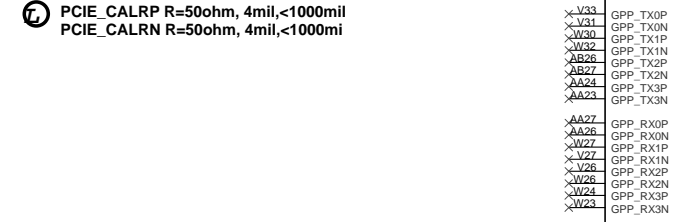
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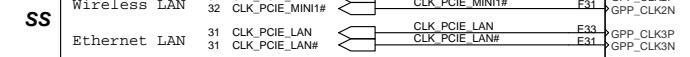
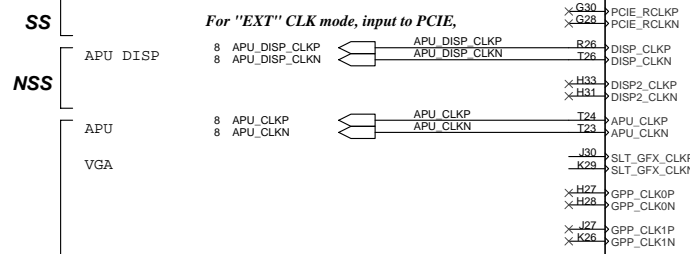
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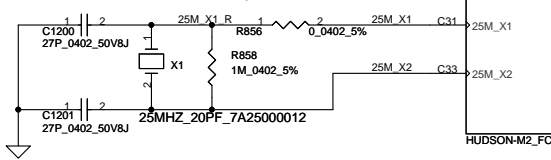
PCIE_CALRP R=50ohm, 4mil, <1000mil
PCIE_CALRN R=50ohm, 4mil, <1000mi



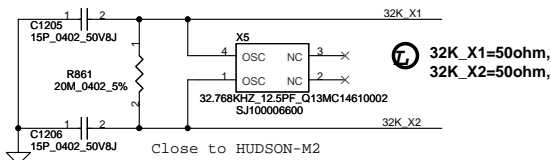
For "EXT" CLK mode, input to PCIE,



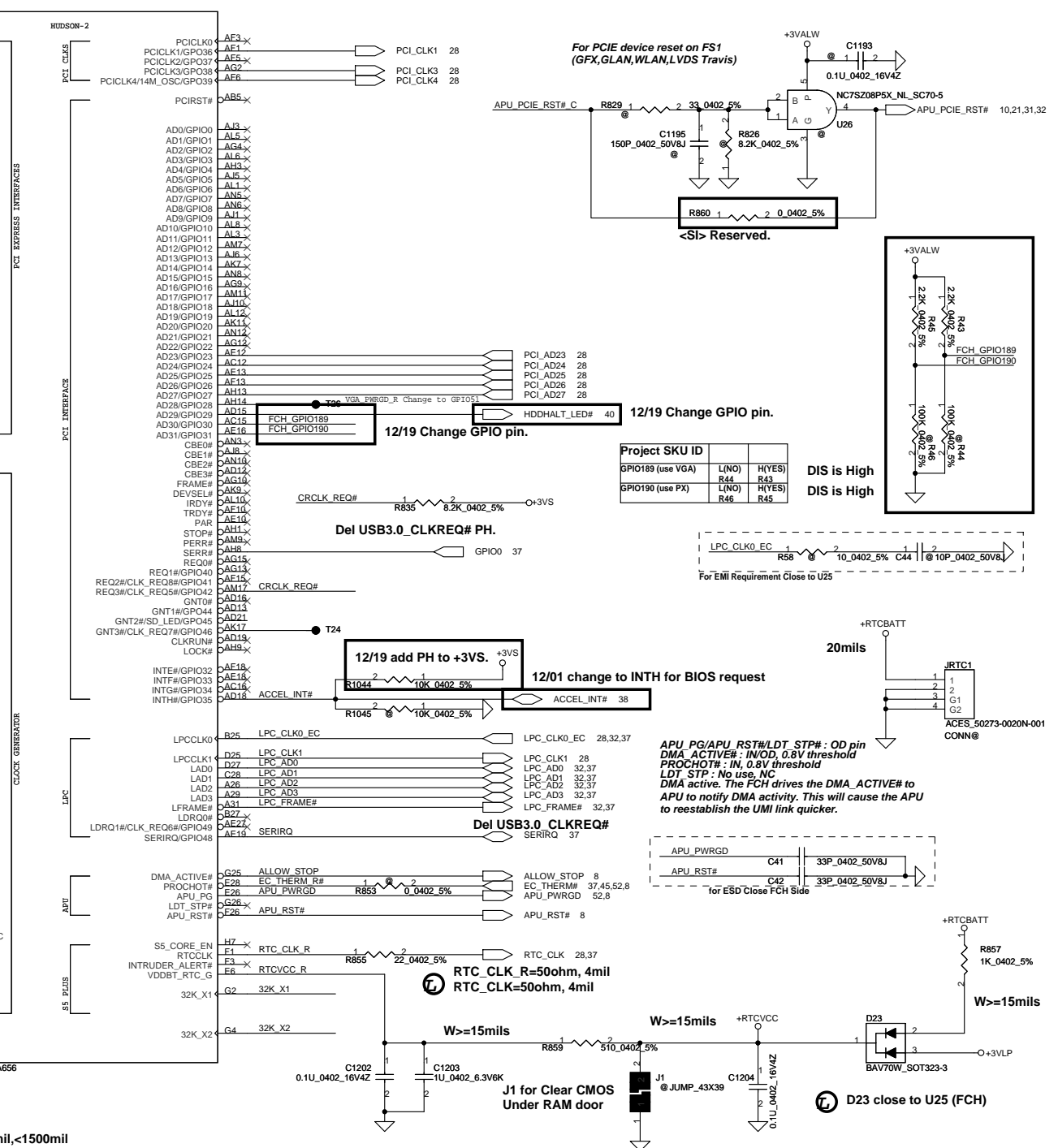
25M_X1 and 25M_X1_R=50ohm, 4mil
25M_X2=50ohm, 4mil



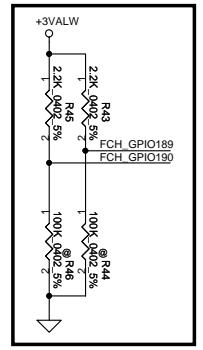
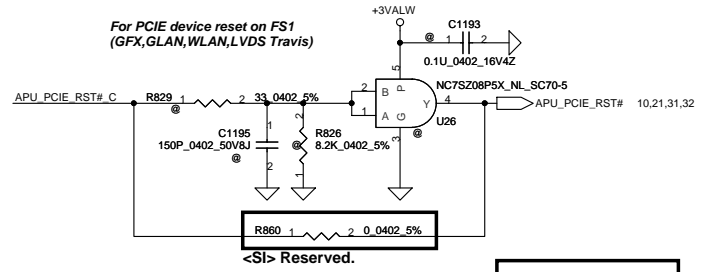
C1205, C1206
Change for G3
RTC timing issue
<improve amplitude>



32K_X1=50ohm, 4mil, <1500mil
32K_X2=50ohm, 4mil, <1500mil



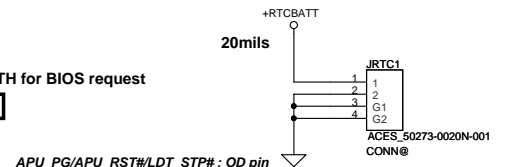
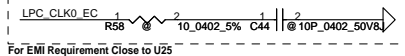
For PCIE device reset on FS1 (GFX, GLAN, WLAN, LVDS, Travis)



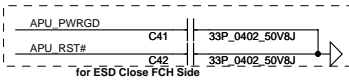
Project SKU ID	L(N)	H(Y)	ESD
GPIO189 (use VGA)	R44	R43	R45
GPIO190 (use PX)	R46	R45	R45

DIS is High

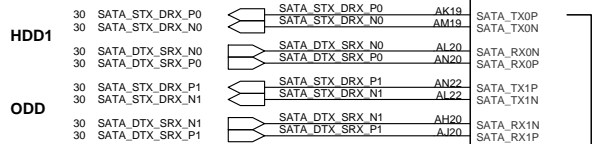
DIS is High



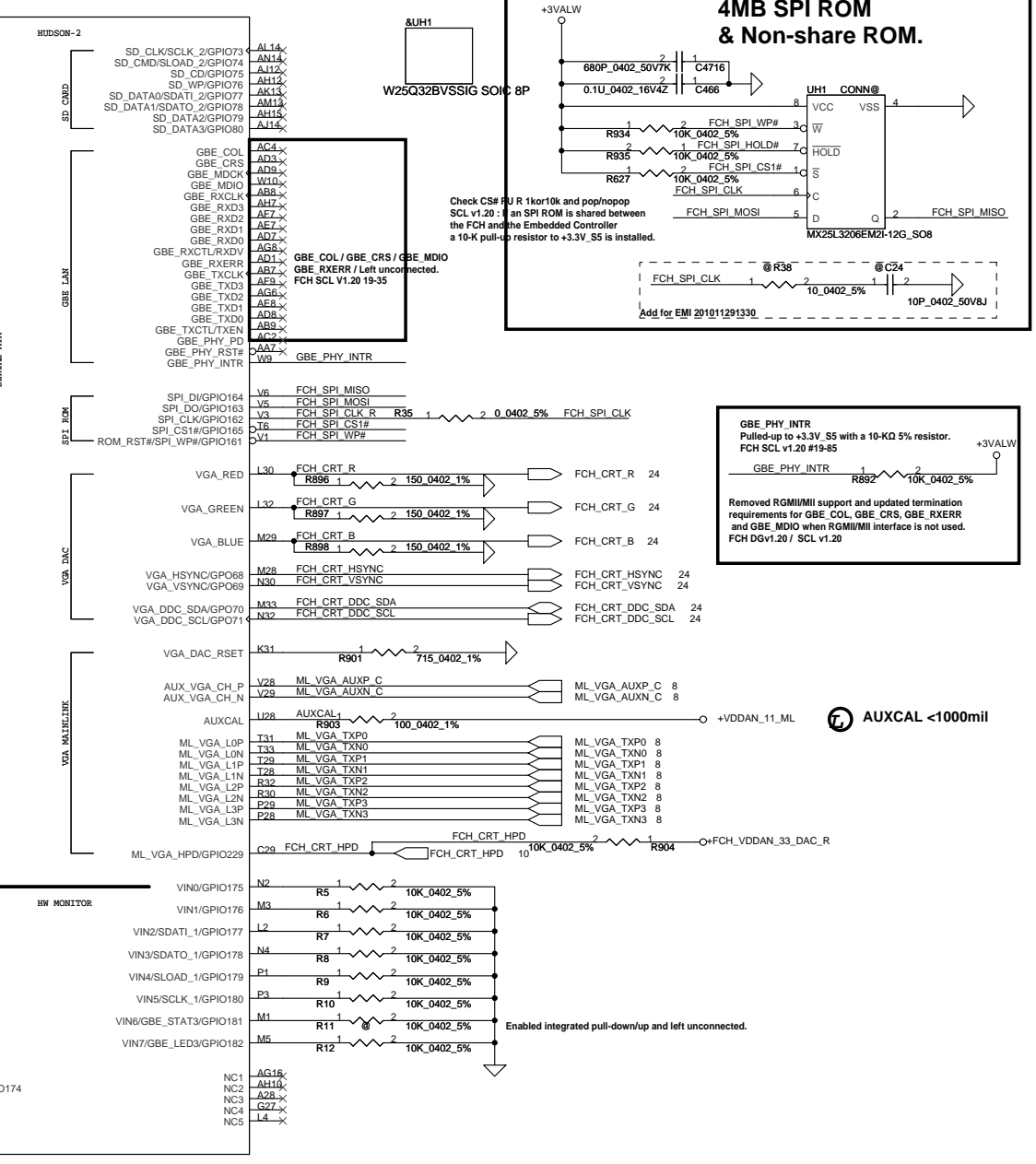
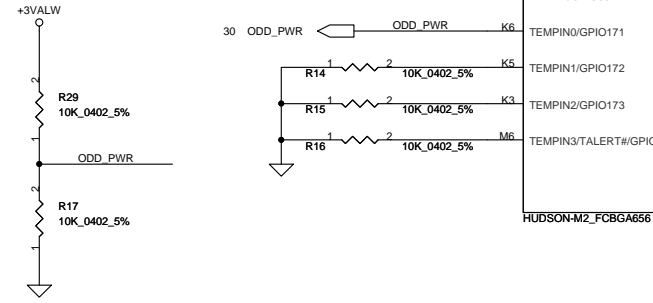
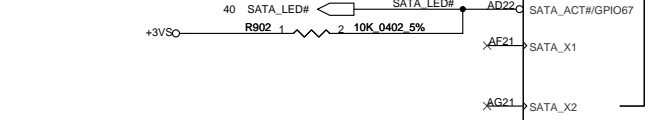
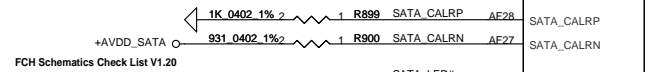
APU_PG/APU_RST#/LDT_STP#: OD pin
DMA_ACTIVE#: INVD, 0.8V threshold
PROCHOT#: IN, 0.8V threshold
LDT_STP: No use, NC
DMA active. The FCH drives the DMA_ACTIVE# to APU to notify DMA activity. This will cause the APU to reestablish the UMI link quicker.



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SATA_CALRP=35ohm,<1000mil
SATA_CALRN=35ohm,<1000mi



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FCH_PCIE_RST# IS FOR PCIE DEVICES ON Hudson-M2/M3

THERMTRIP: Need level shift from +3VALW to +1.5V Note: Ensure FCH internal pull-up resistor to +3.3V S5 is disabled to prevent leakage when APU is powered down.

SM bus 0->S0 PWR domain SM bus 1->S5 PWR domain

FCH GEVENT (S5 domain) with isolation circuit to avoid leakage

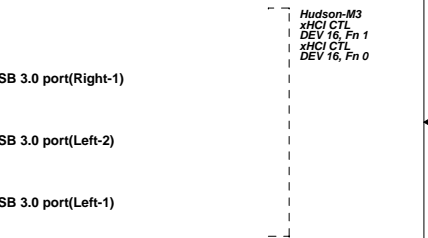
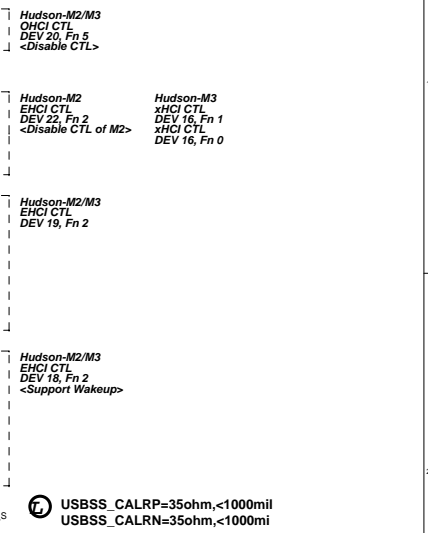
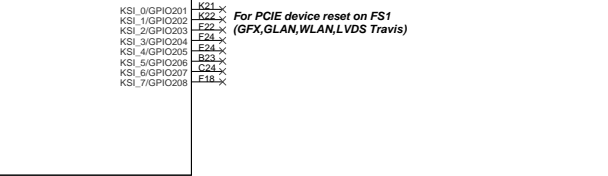
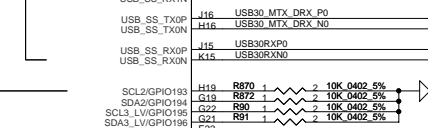
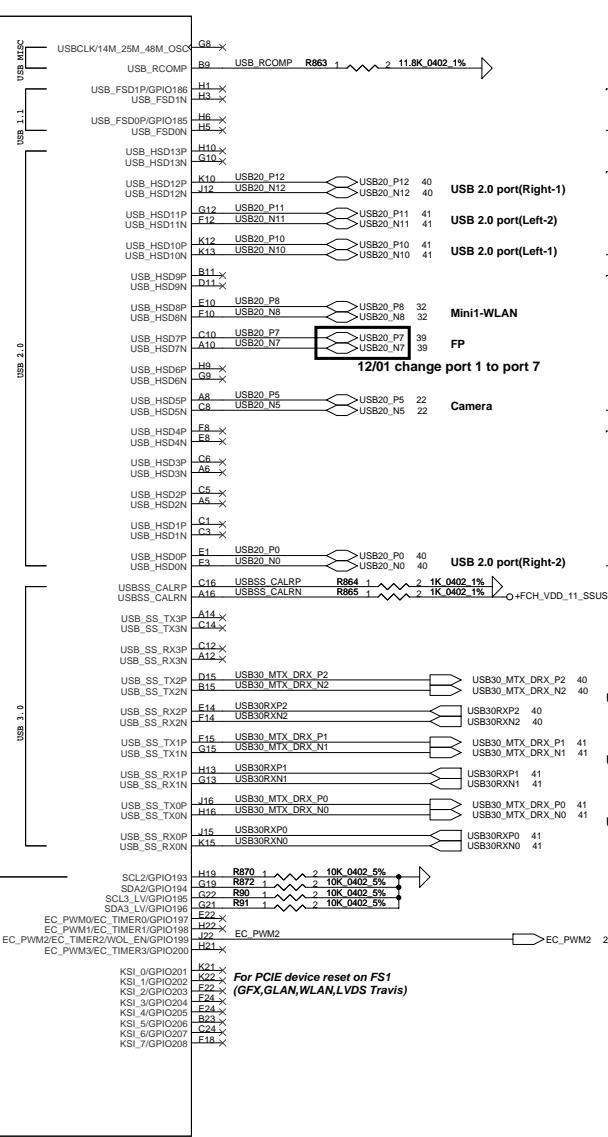
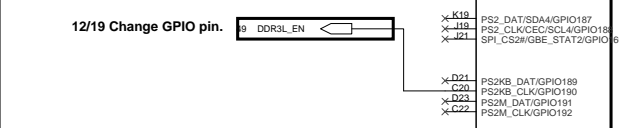
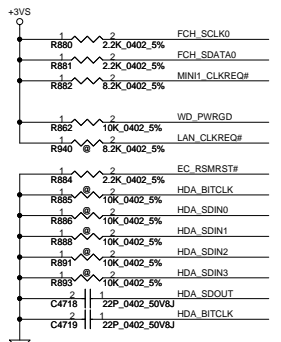
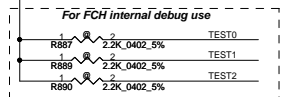
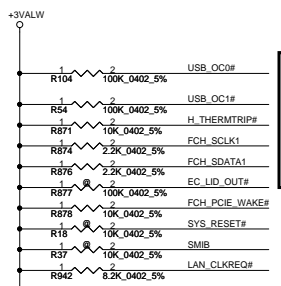
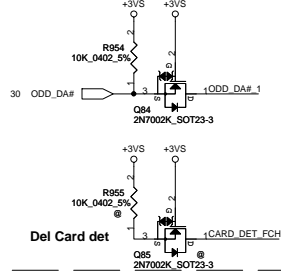
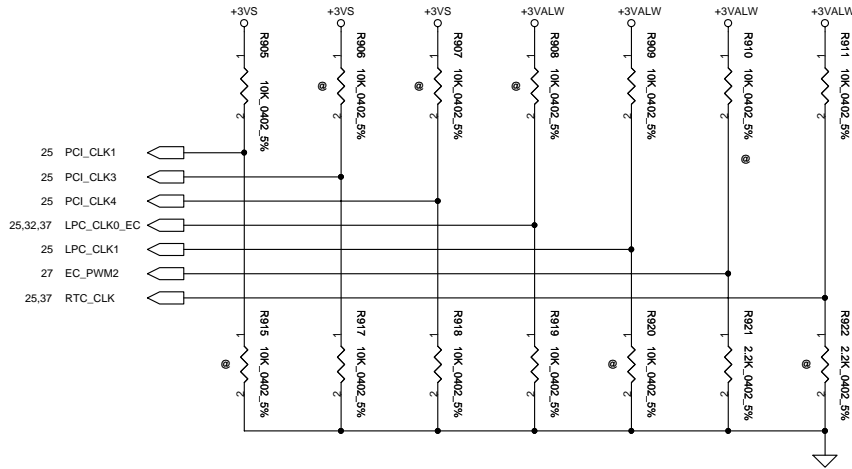


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STRAP PINS

Change to SPI

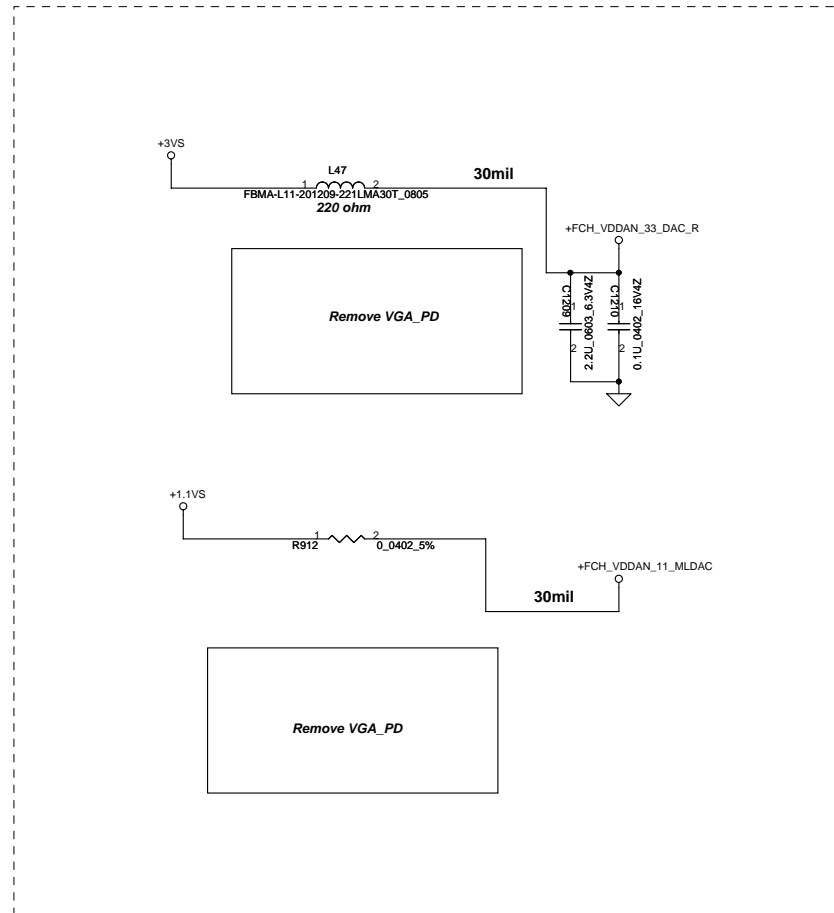
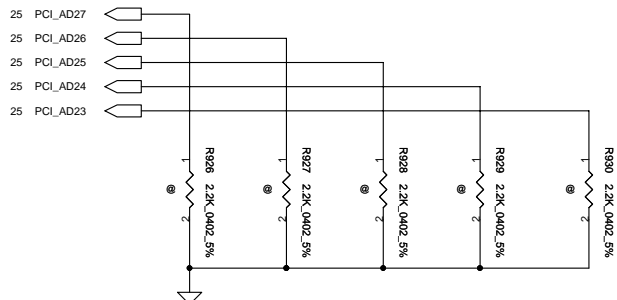
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



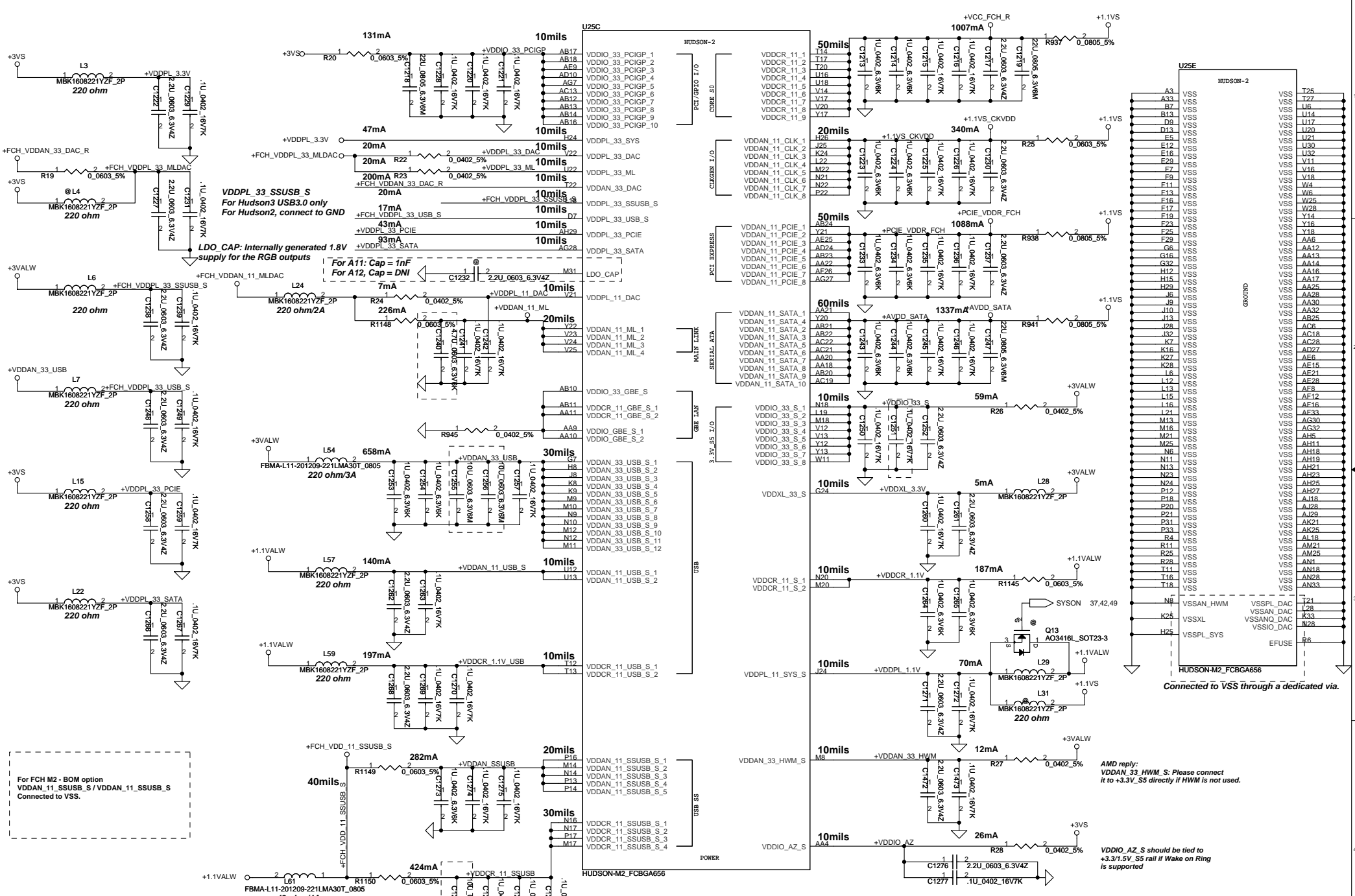
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD25	PCI_AD24	PCI_AD23
No external R	USE PCI PLL DEFAULT	Normal REFCLK termination DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	Inverted REFCLK termination	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

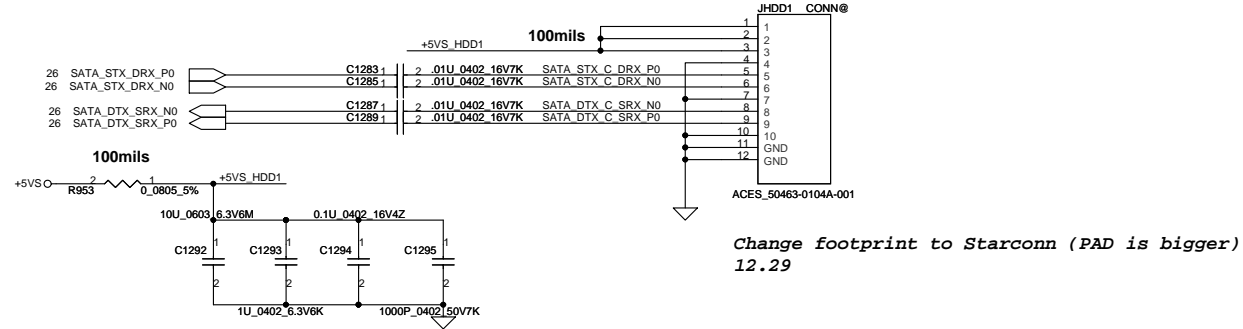


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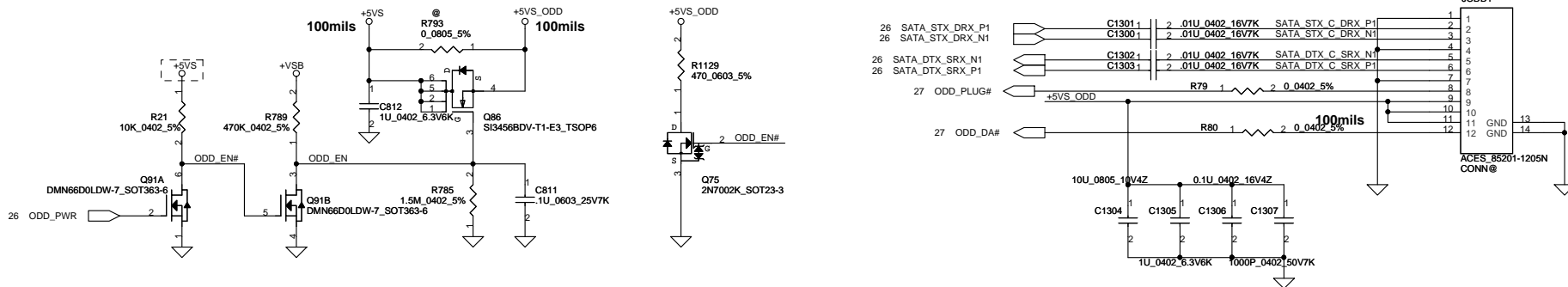


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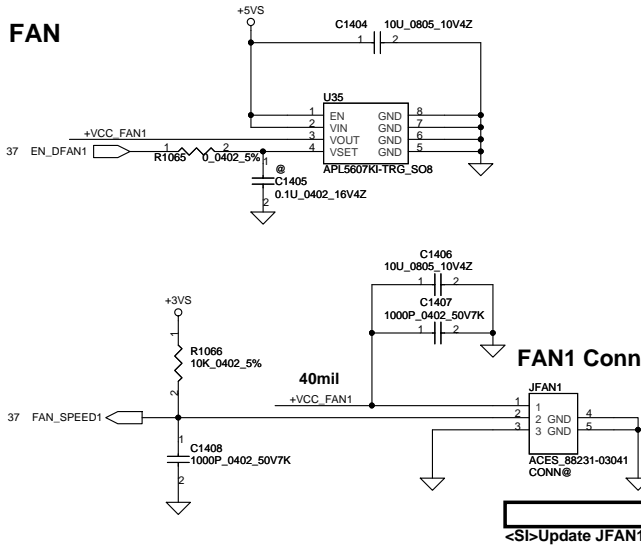
SATA HDD1 Conn.



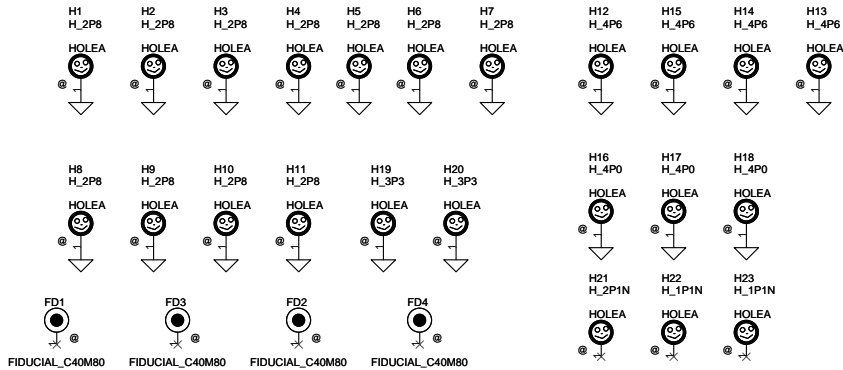
ODD conn



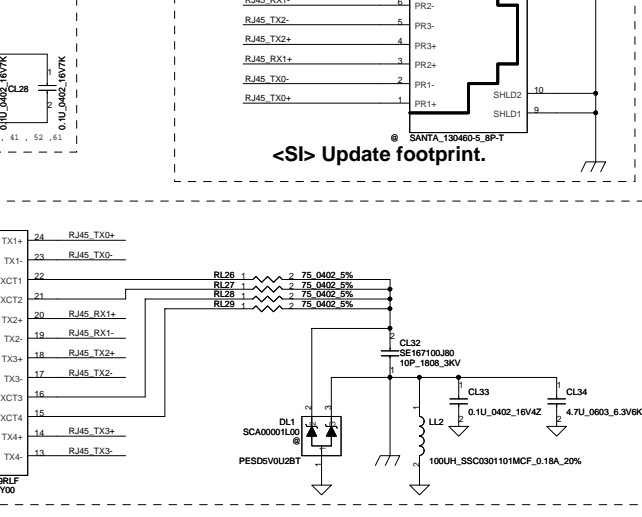
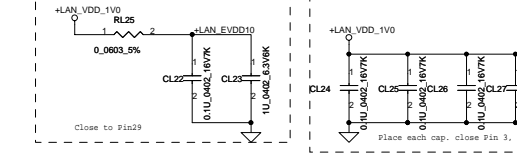
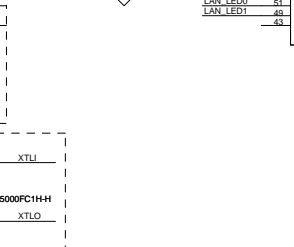
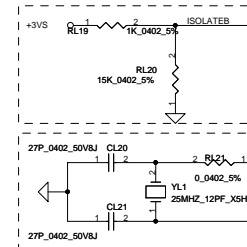
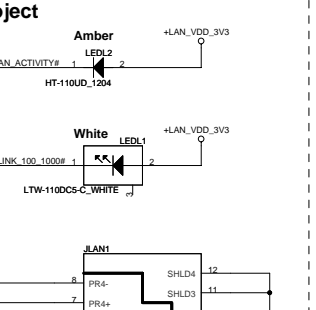
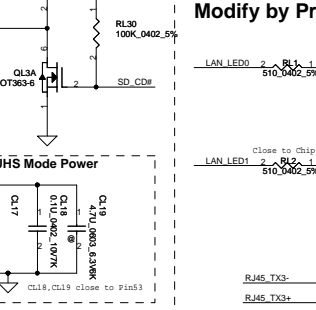
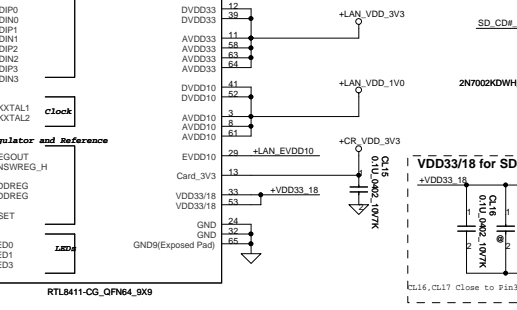
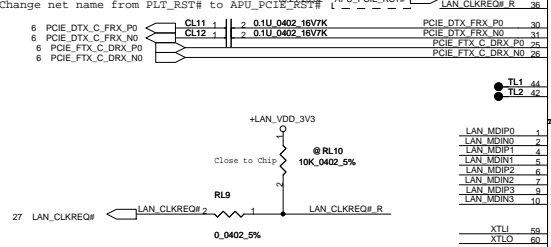
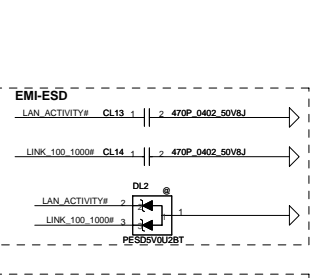
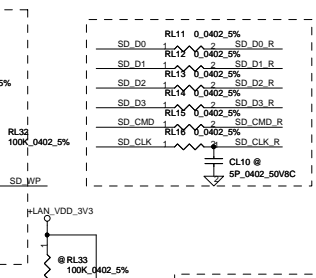
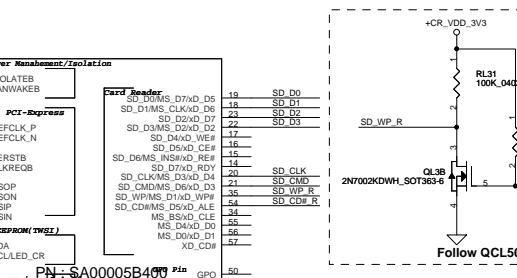
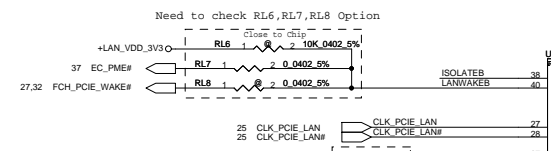
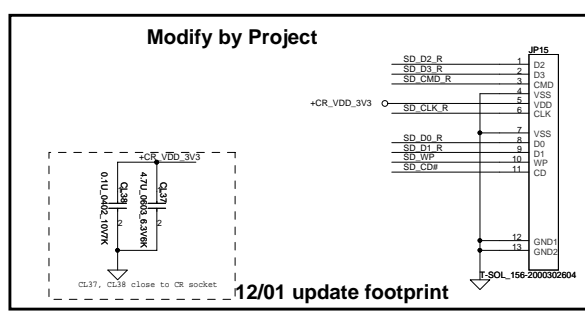
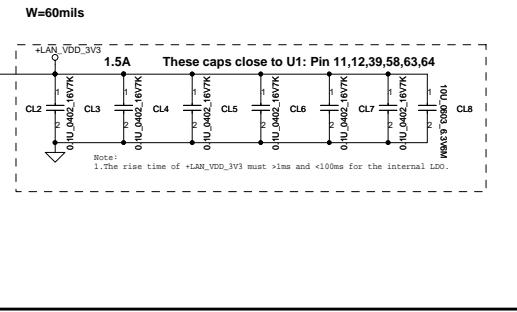
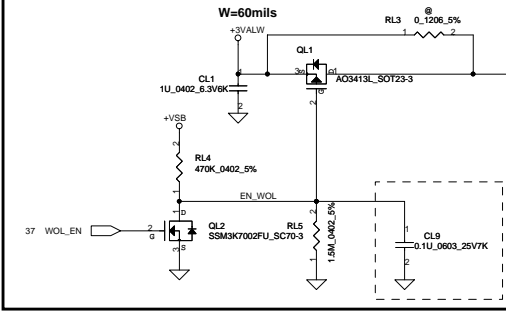
FAN



Screw Hole



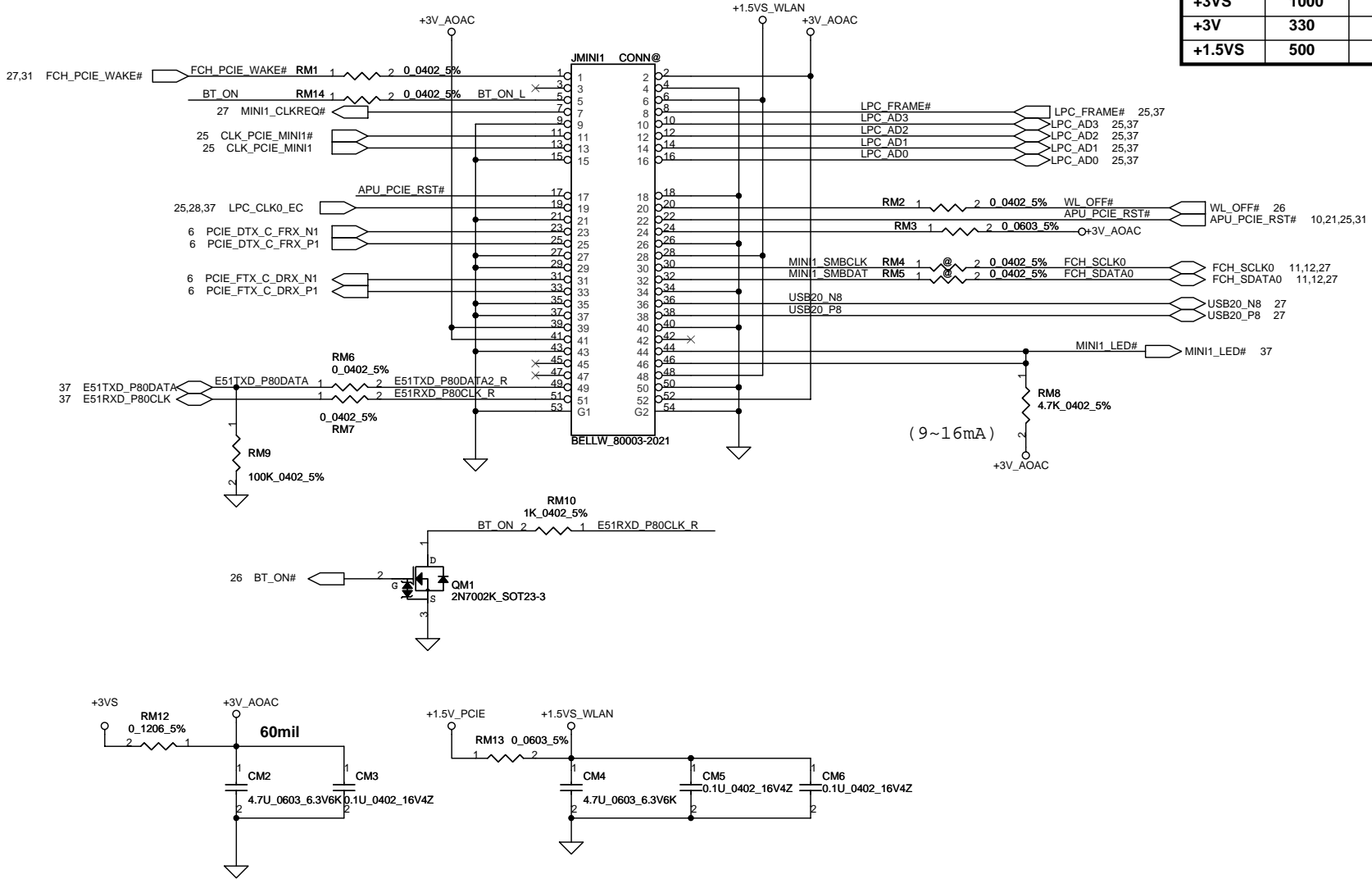
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WLAN

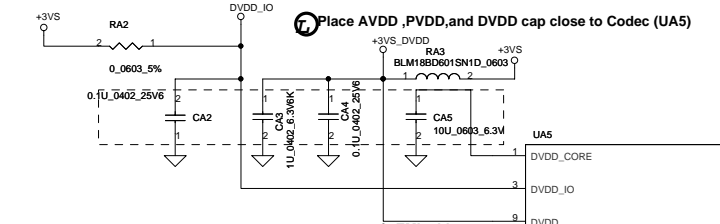


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

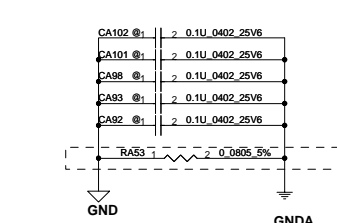
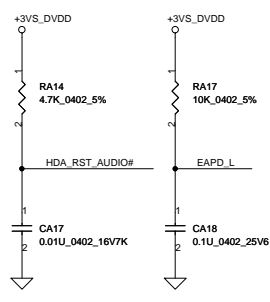
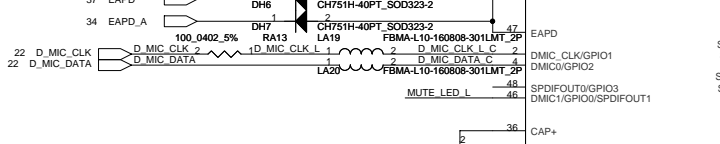
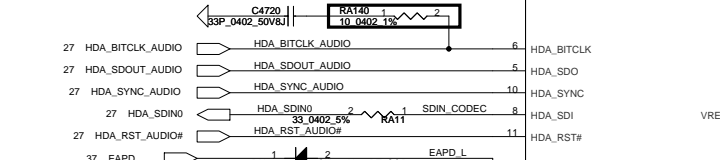
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Notes:
 Keep PVDD supply and speaker traces routed on the DGND plane.
 Keep away from AGND and other analog signals

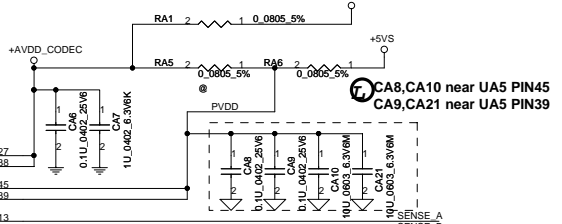
Place AVDD, PVDD, and DVDD cap close to Codec (UA5)



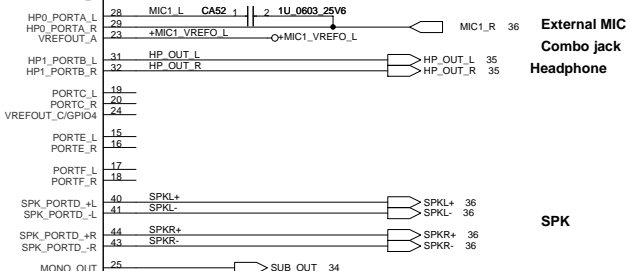
1/3 EMI add



RA53 need under or near UA5



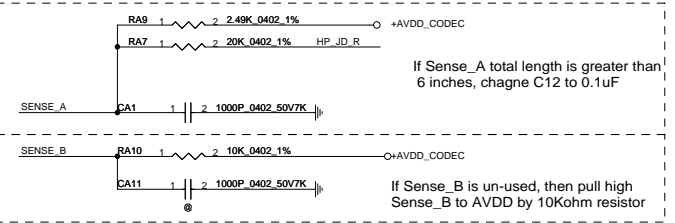
CA8, CA10 near UA5 PIN45
 CA9, CA21 near UA5 PIN39



External MIC
 Combo jack
 Headphone

SPK

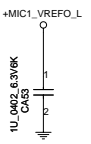
PLACE CLOSE TO UA5 PIN 13



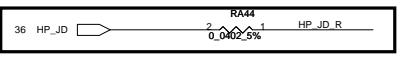
If Sense_A total length is greater than 6 inches, change C12 to 0.1uF

If Sense_B is un-used, then pull high Sense_B to AVDD by 10Kohm resistor

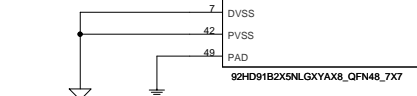
PLACE CLOSE TO UA5 PIN 14



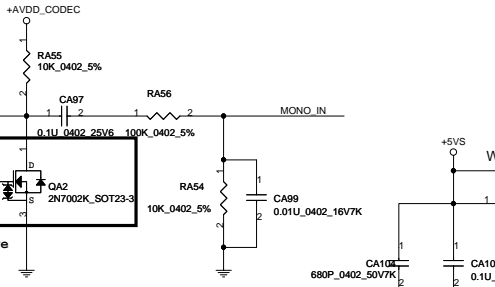
12/5 Audio jack change to normal open, so remove MOS



Place C208 close to Codec

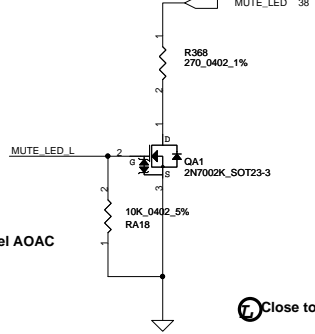


C209, C210, CA87, CA89 close to Codec (UA5)



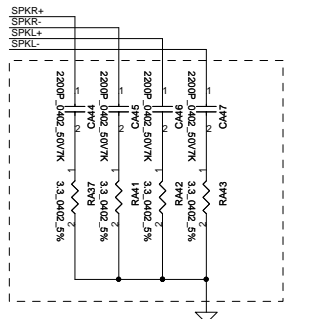
Need confirmed.

12/7 Change to single package

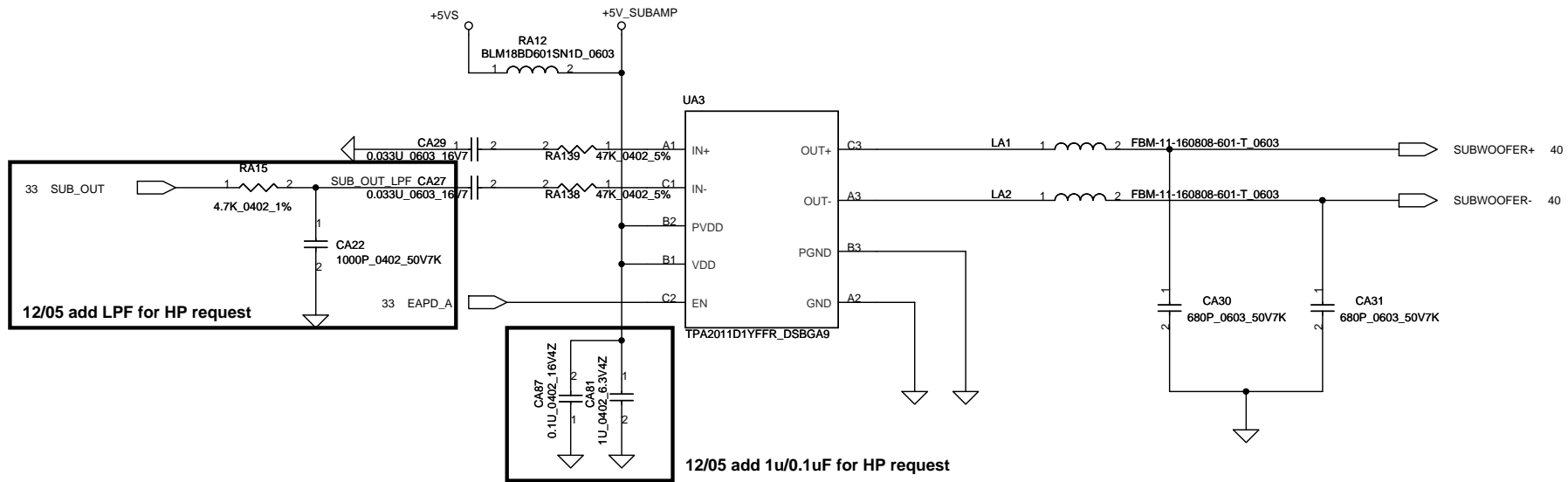


Del AOAC

Close to Audio Codec (UA5)



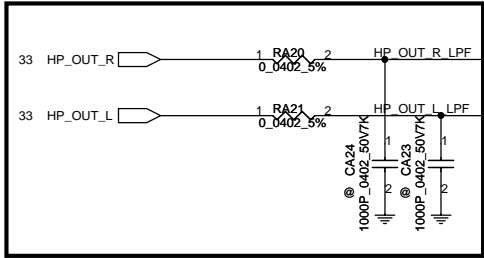
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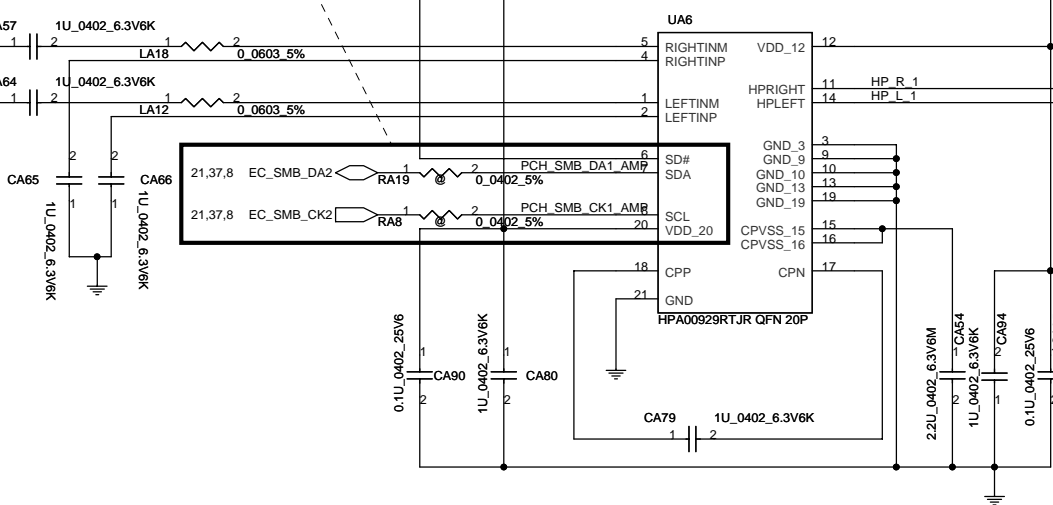
Headphone amplifier

12/05 Add LPF for HP requirement

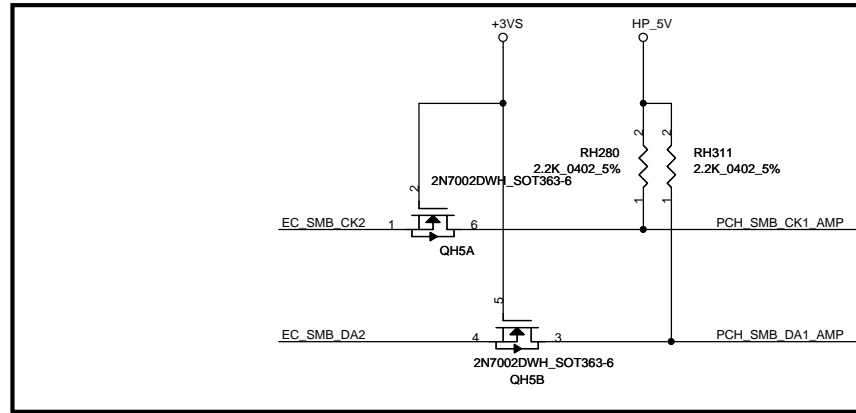


<SI> BOM update :RA20,RA21 4.7K-->0
CA24,CA23 SMT-->@

12/05 Connect HP AMP SMBus to EC

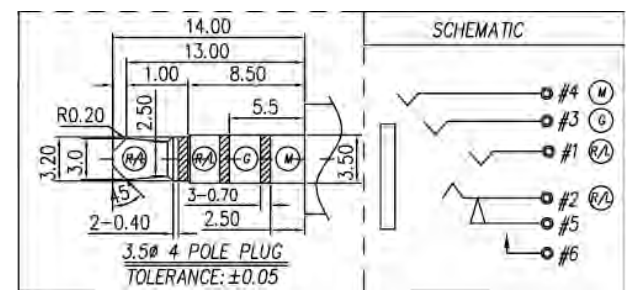
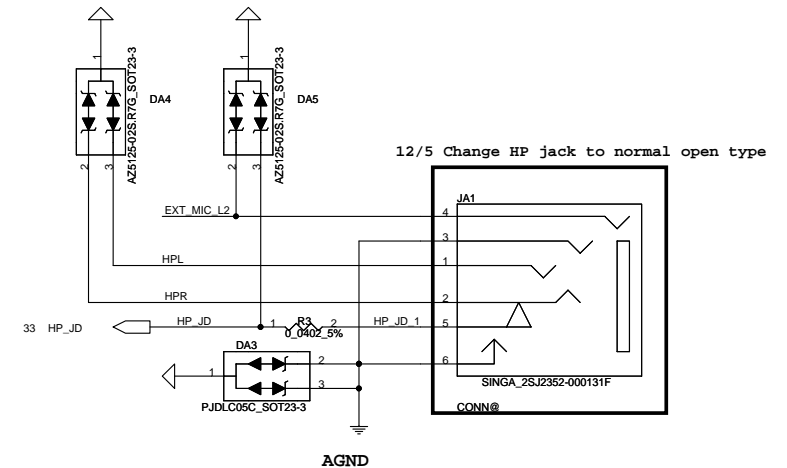
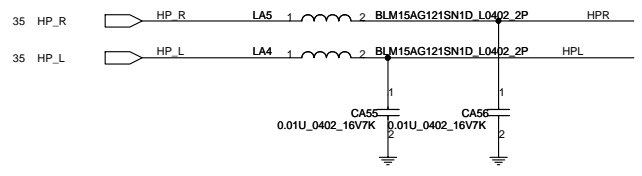
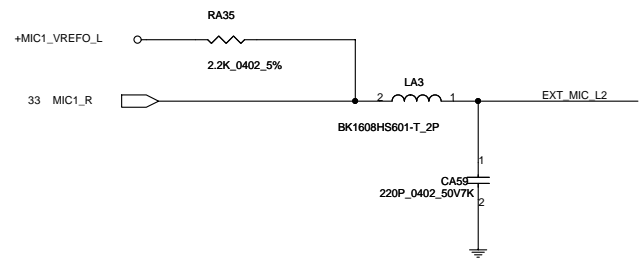
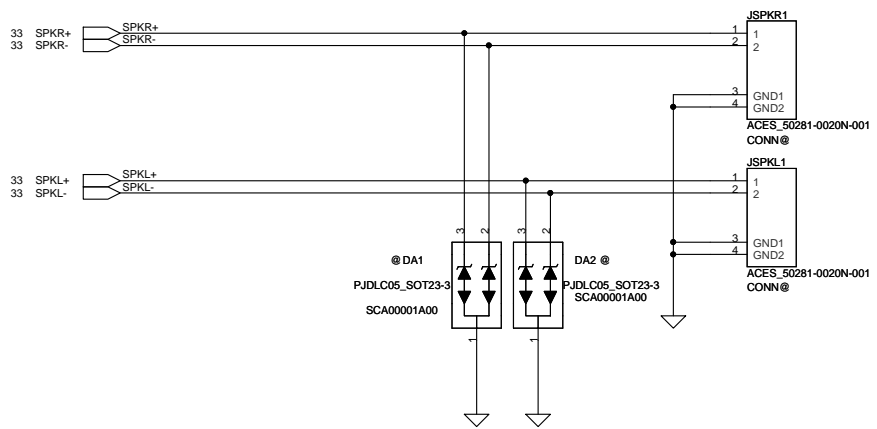


12/05 Reserve level shift Connect to EC

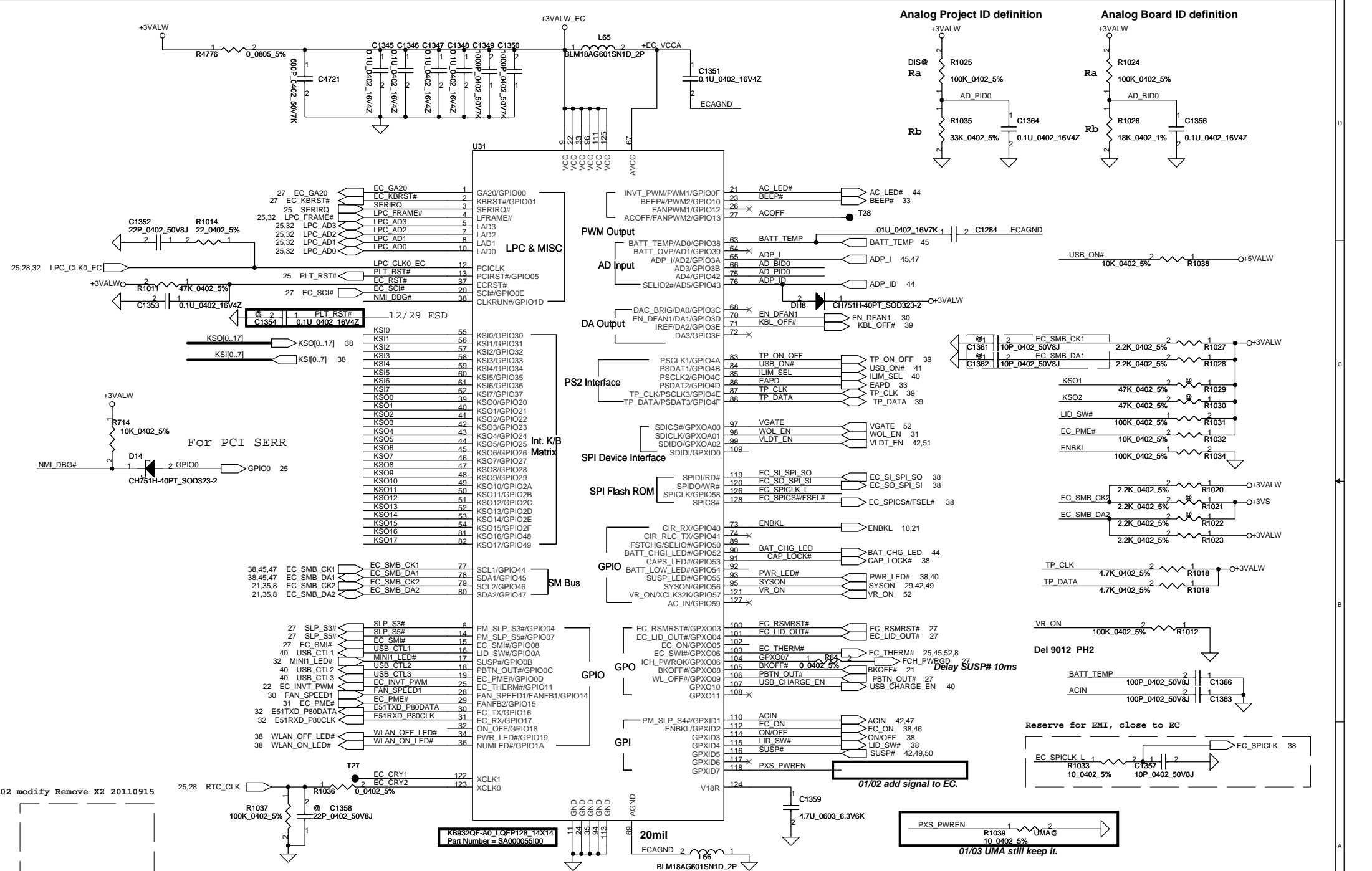


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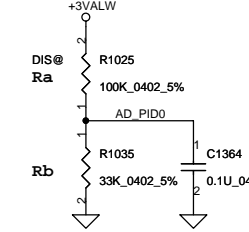
SPK conn



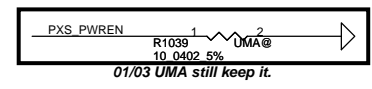
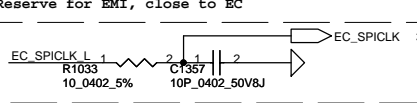
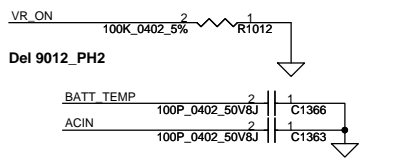
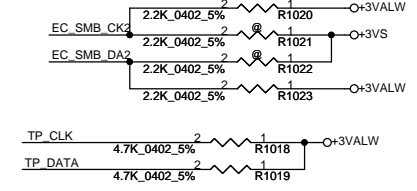
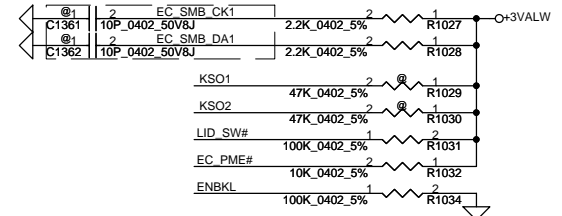
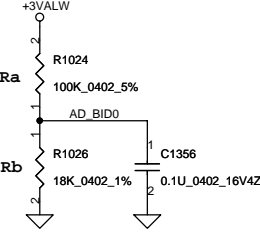
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Analog Project ID definition

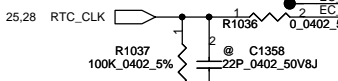


Analog Board ID definition



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				4019IF	
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R02 modify Remove X2 20110915

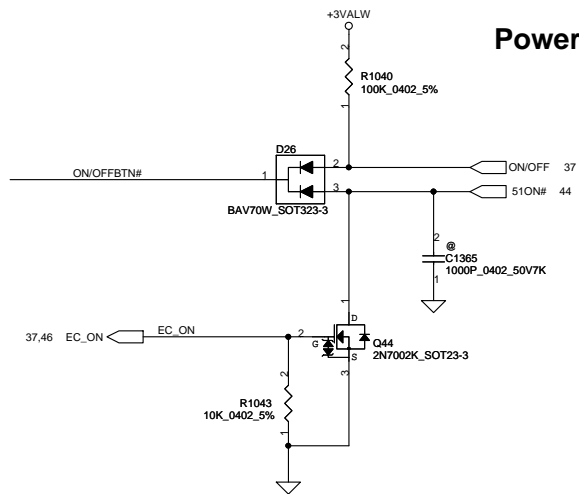


K8932QF-A0 LQFP128_14X14
Part Number = SA000055100

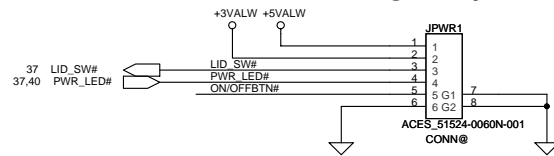
01/02 add signal to EC.

01/03 UMA still keep it.

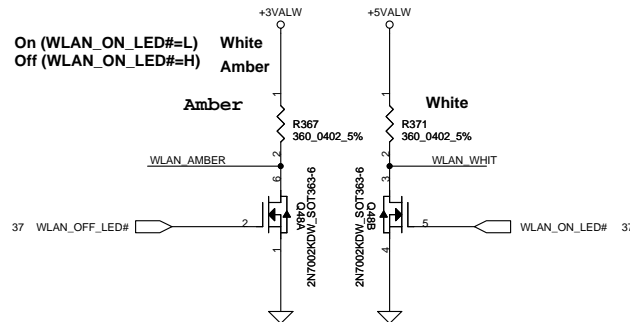
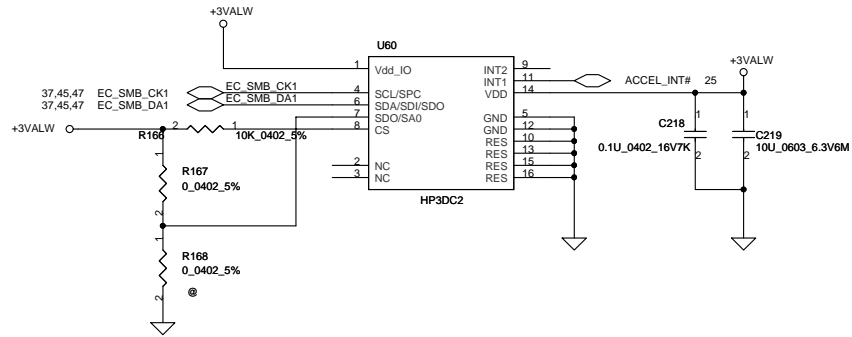
Power Button



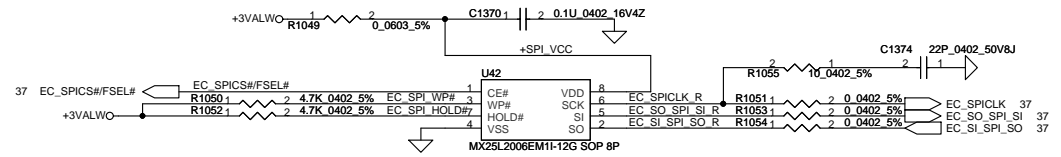
POWER/B



ACCELEROMETER

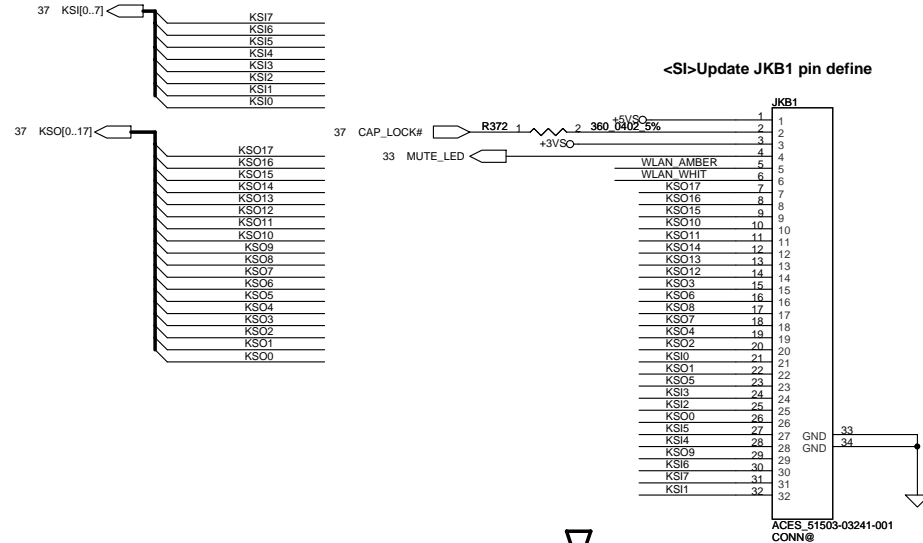


EC BIOS ROM

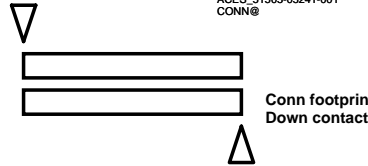


KB conn

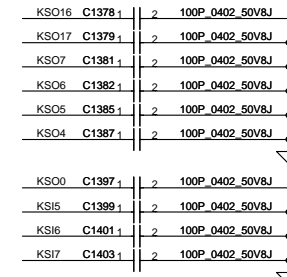
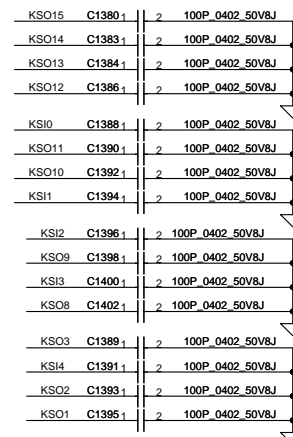
<SI>Update JKB1 pin define



Membrane Down contact

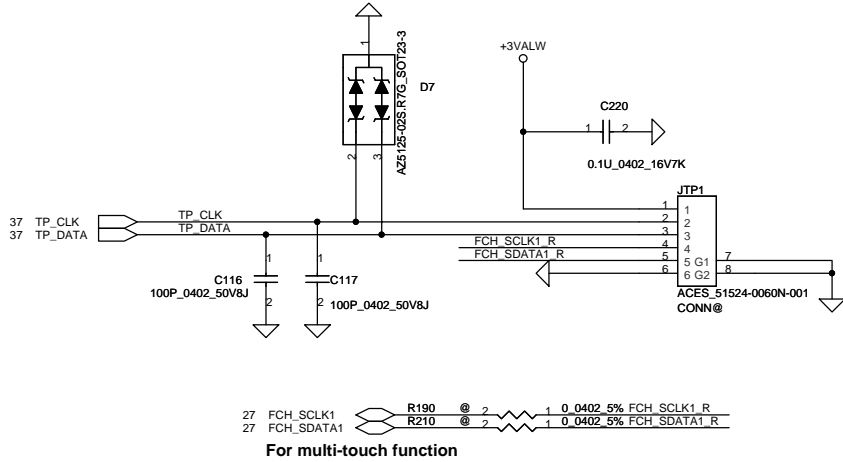


The KB pin define must opposite



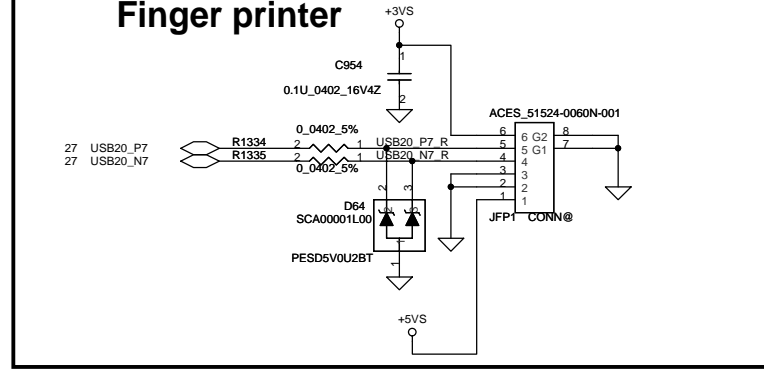
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TP Conn

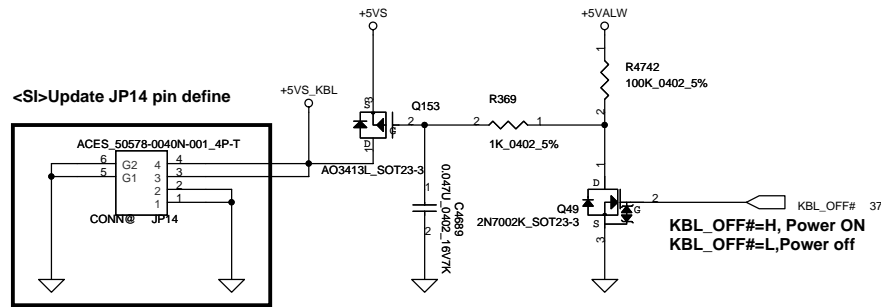


Finger printer

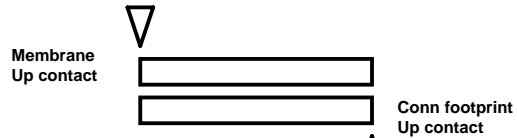
12/06 Change FPR pin define



Keyboard backlight Conn

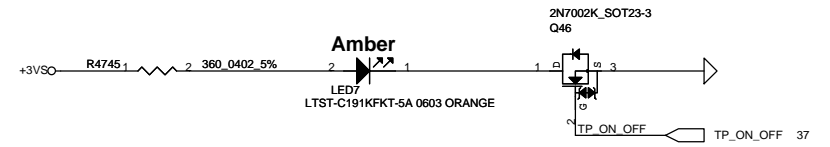


12/06 Change keyboard back light conn



The JP14 pin define must opposite

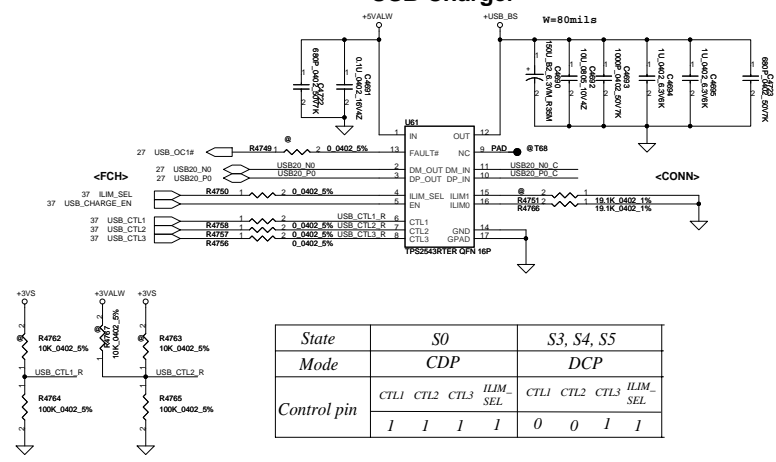
T/P On/Off LED



EC pin

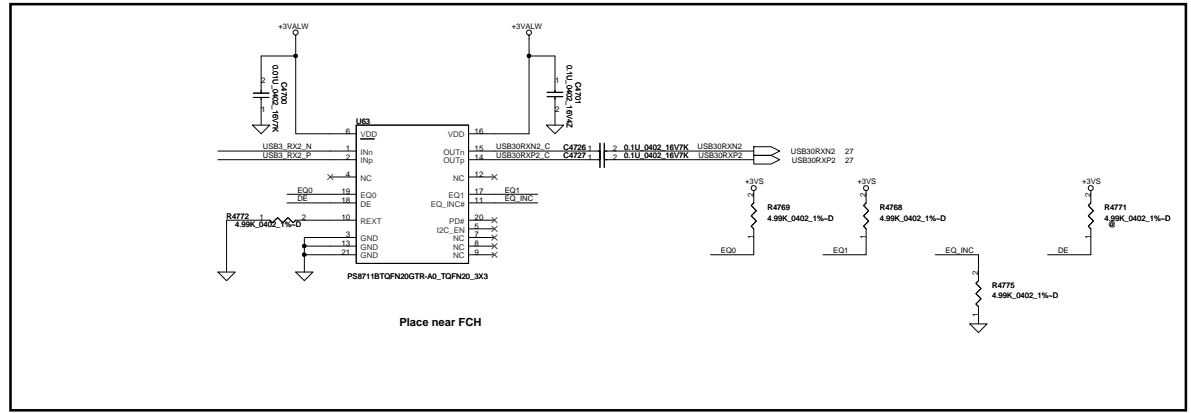
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USB Charger

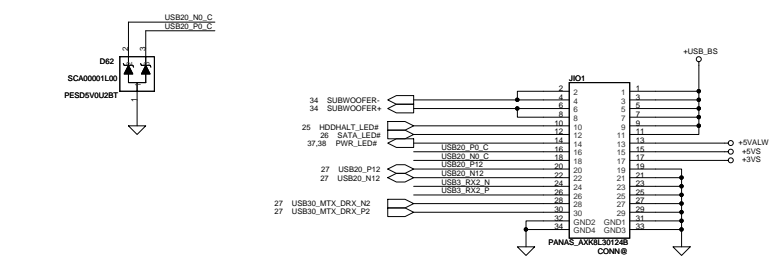


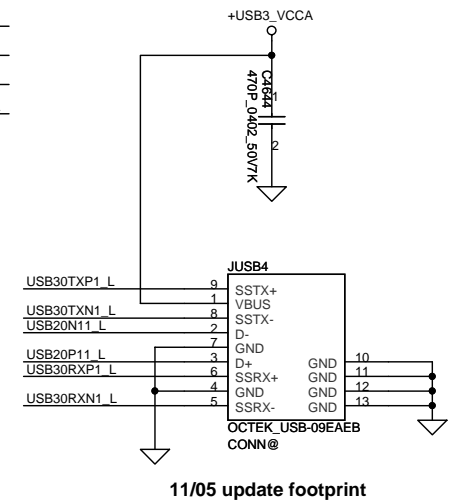
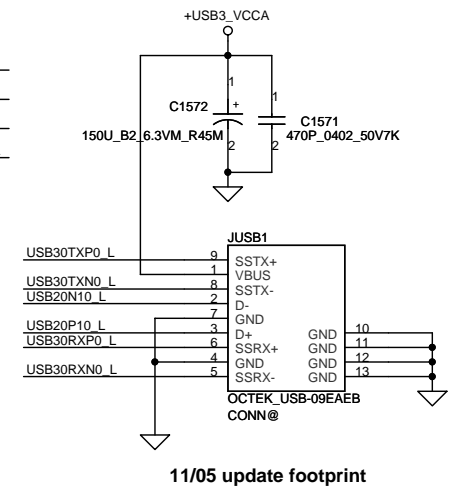
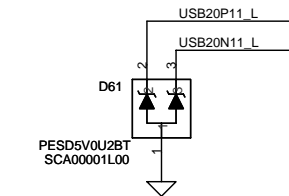
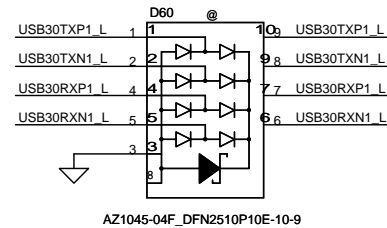
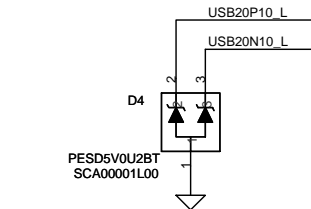
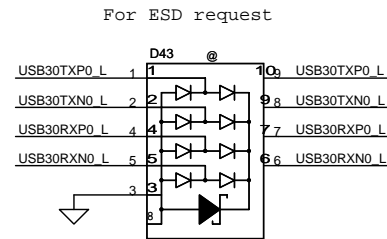
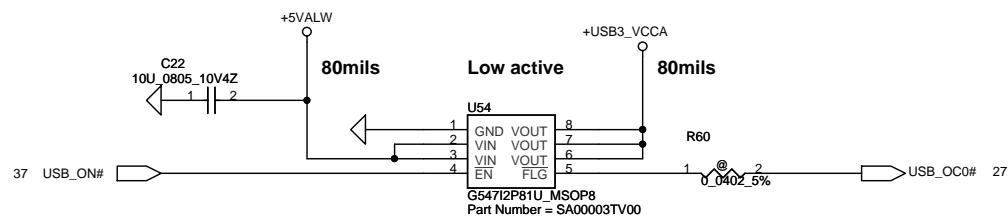
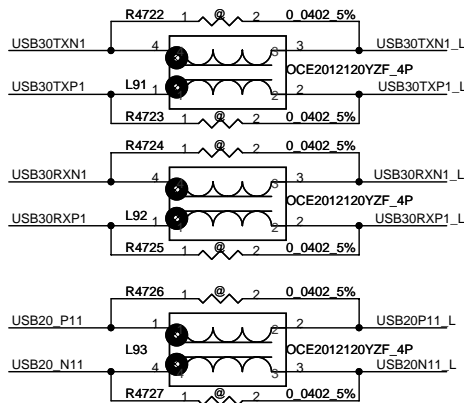
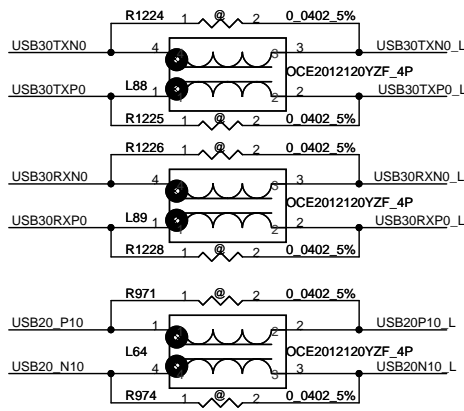
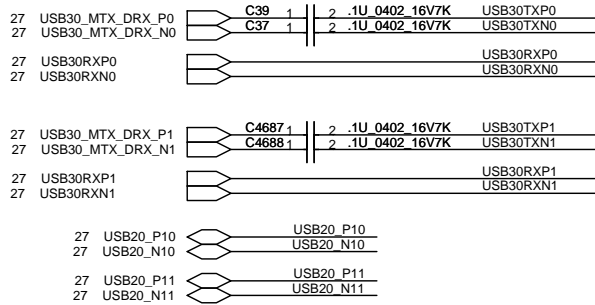
State	S0				S3, S4, S5			
Mode	CDP				DCP			
Control pin	CTL1	CTL2	CTL3	ILIM_SEL	CTL1	CTL2	CTL3	ILIM_SEL
	1	1	1	1	0	0	1	1

USB3.0 Repeater



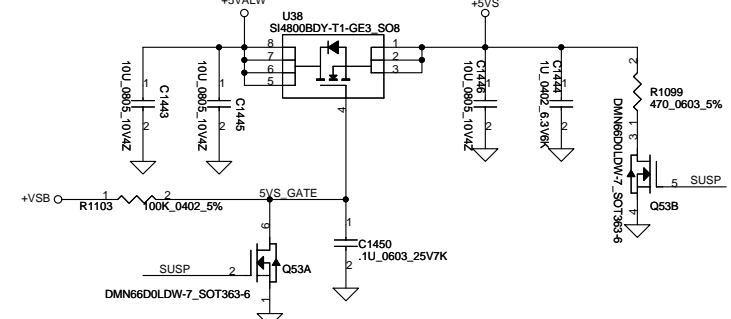
Place near FCH



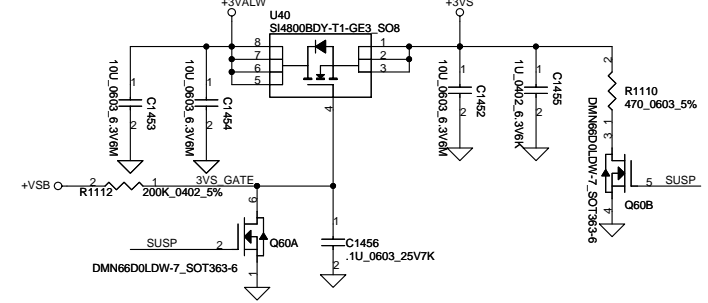


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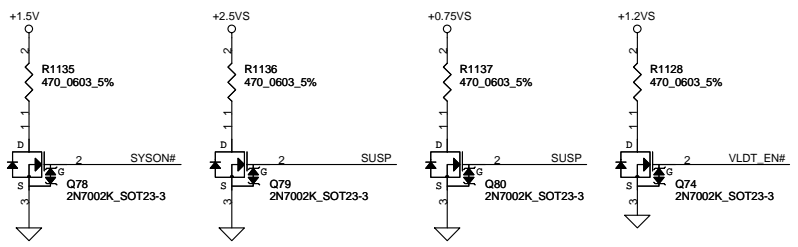
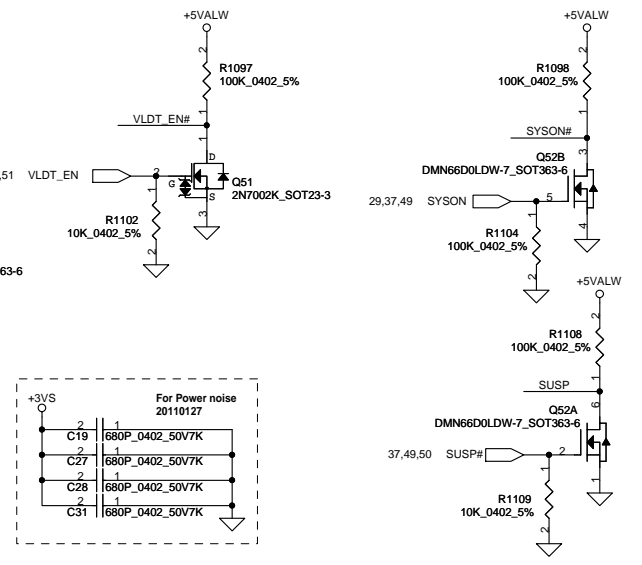
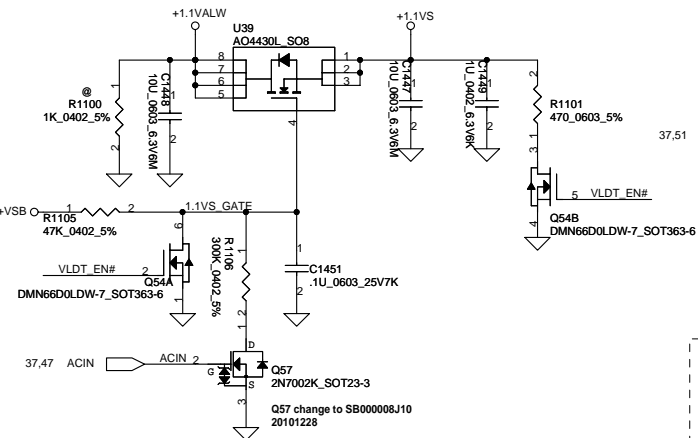
+5VALW TO +5VS (5A)



+3VALW TO +3VS (3.3A)



+1.1VALW TO +1.1VS (1.1A)



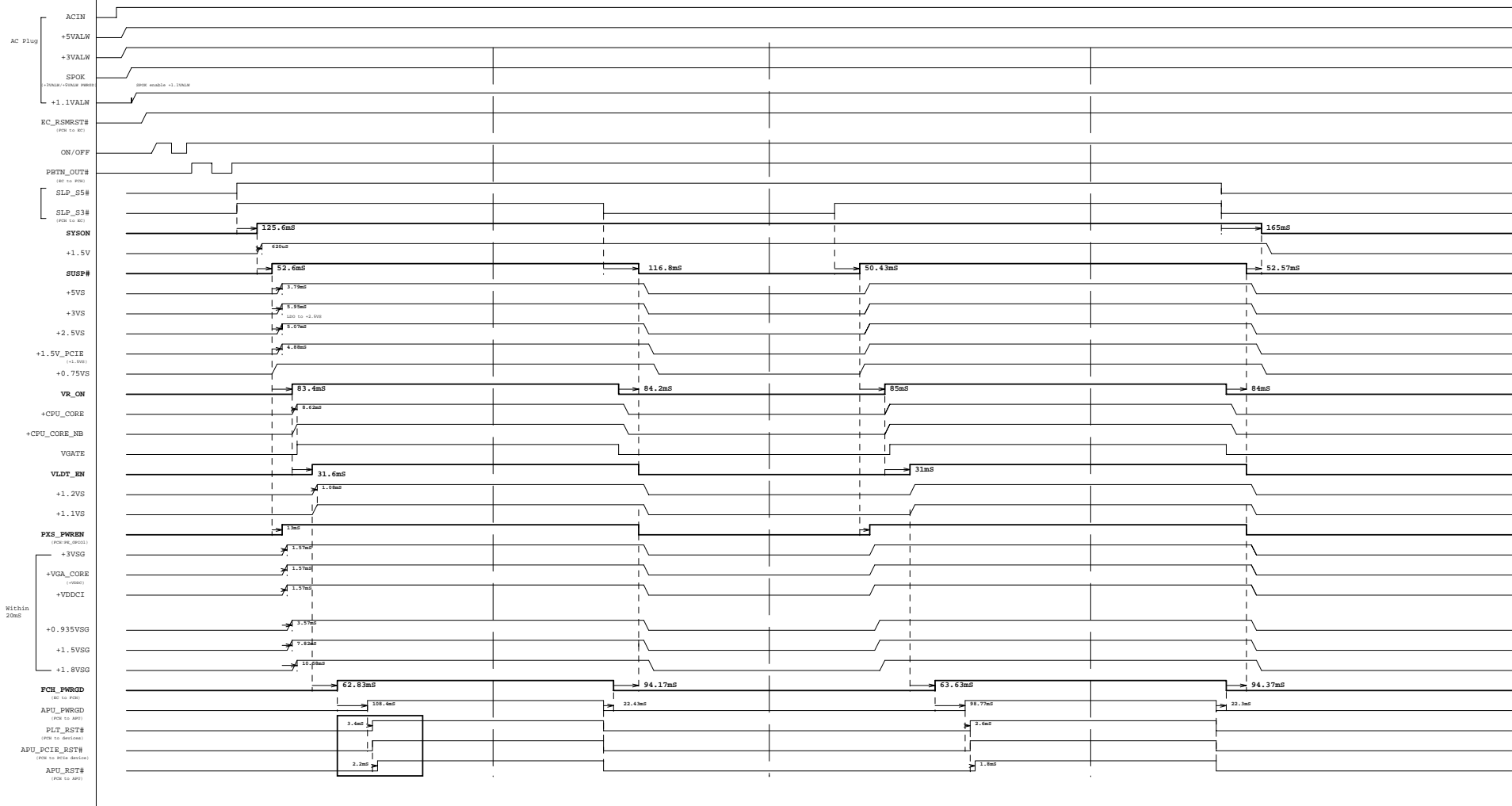
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Boot

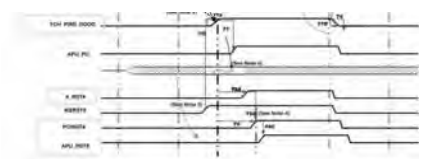
Enter S3

S3 Resume

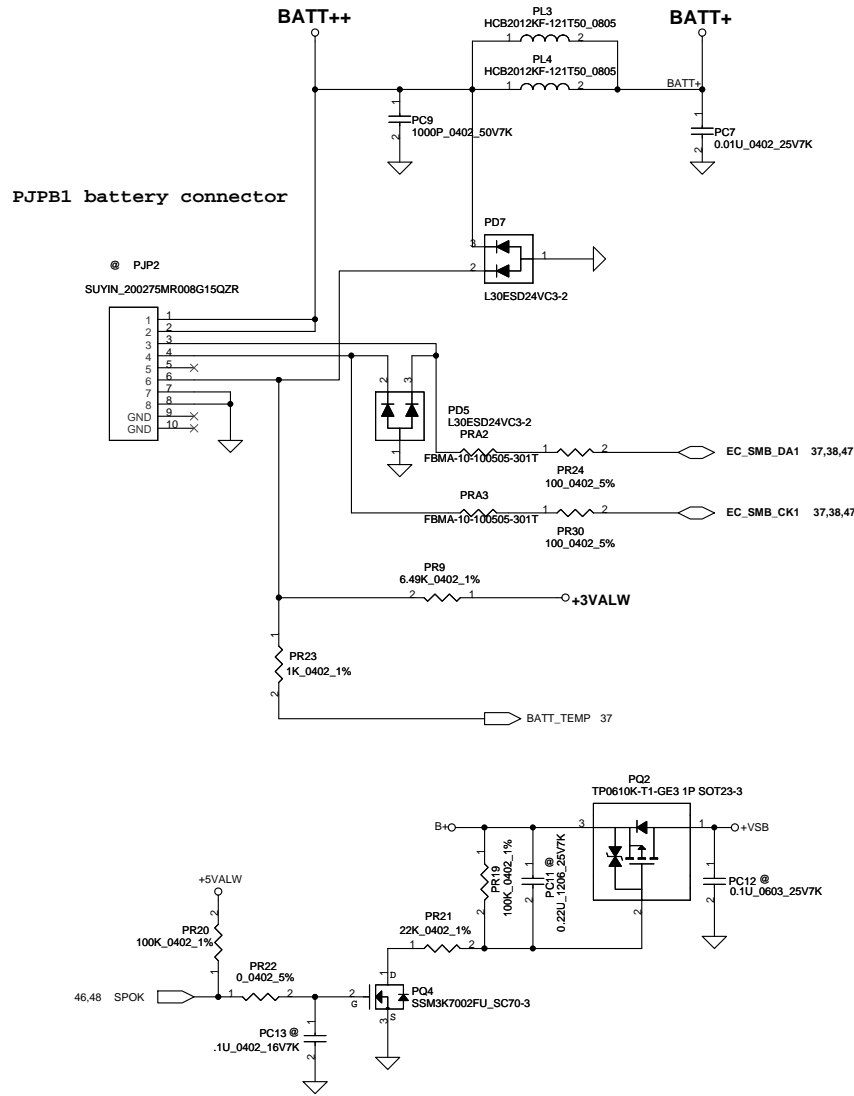
Shut Down



Within 20ms



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Doc#	40191F	Rev#	1	A
Appr	Yongbin Jang	By	Yongbin Jang	2015-07-08



For KB930 --> Keep PU1 circuit
(Vth = 0.825V)

PH1 under CPU bottom side :
CPU thermal protection at 90 +/-3 degree C
Recovery at 56 +/-3 degree C

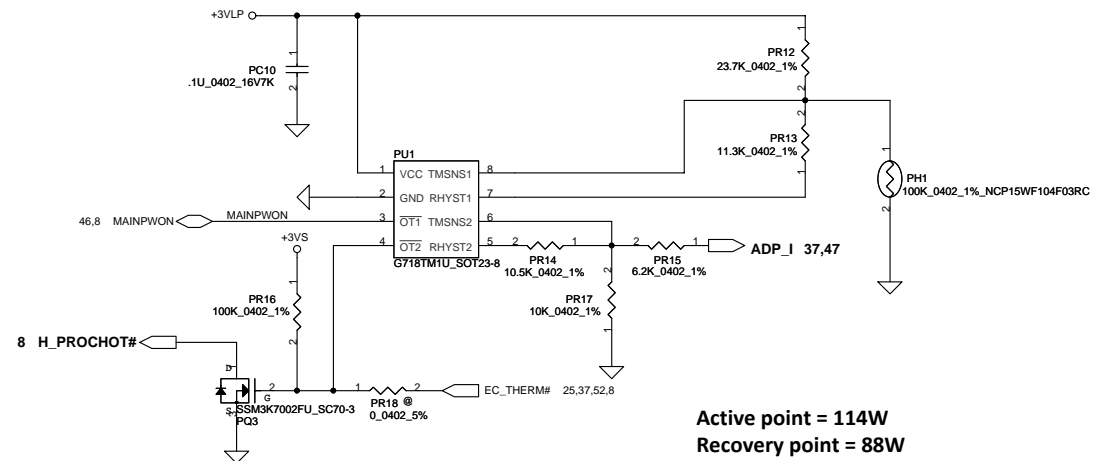
$$R_{set} = 3 * R_{tmh}$$

$$R_{hyst} = (R_{set} * R_{tml}) / (3 * R_{tml} - R_{set})$$

$$R_{tmh} \text{ at } 90C = 7.8K, R_{tml} \text{ at } 56C = 26.1K$$

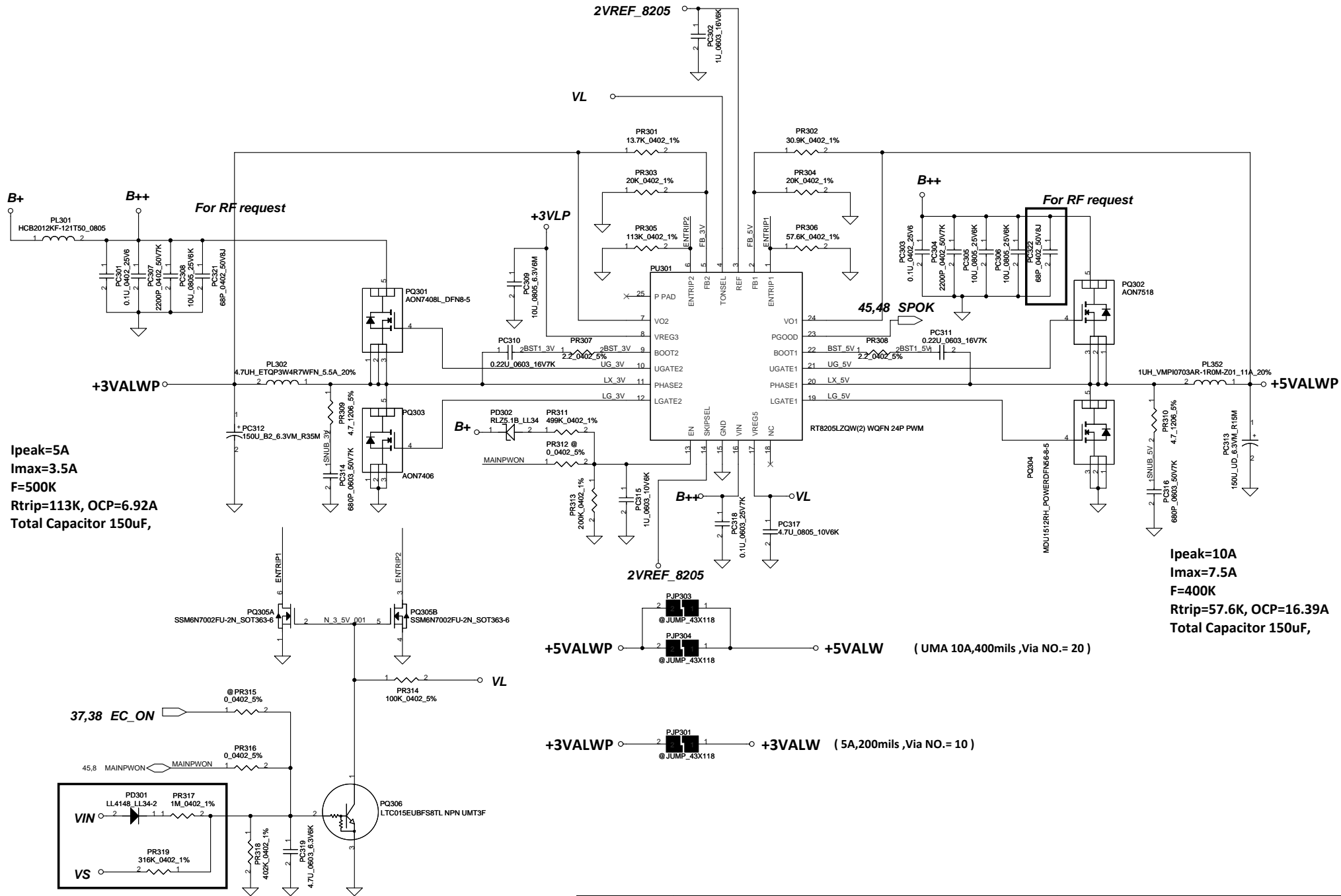
$$R_{set} = 3 * 7.8K = 23.4K \implies 23.7K$$

$$R_{hyst} = (23.4K * 26.1K) / (3 * 26.1K - 23.4K) = 11.12K \implies 11.3K$$



Active point = 114W
Recovery point = 88W

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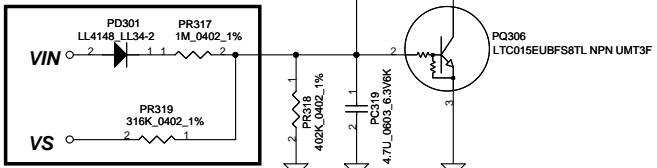


I_{peak}=5A
I_{max}=3.5A
F=500K
R_{trip}=113K, OCP=6.92A
Total Capacitor 150uF,

I_{peak}=10A
I_{max}=7.5A
F=400K
R_{trip}=57.6K, OCP=16.39A
Total Capacitor 150uF,

+5VALWP **+5VALW** (UMA 10A,400mils ,Via NO.= 20)

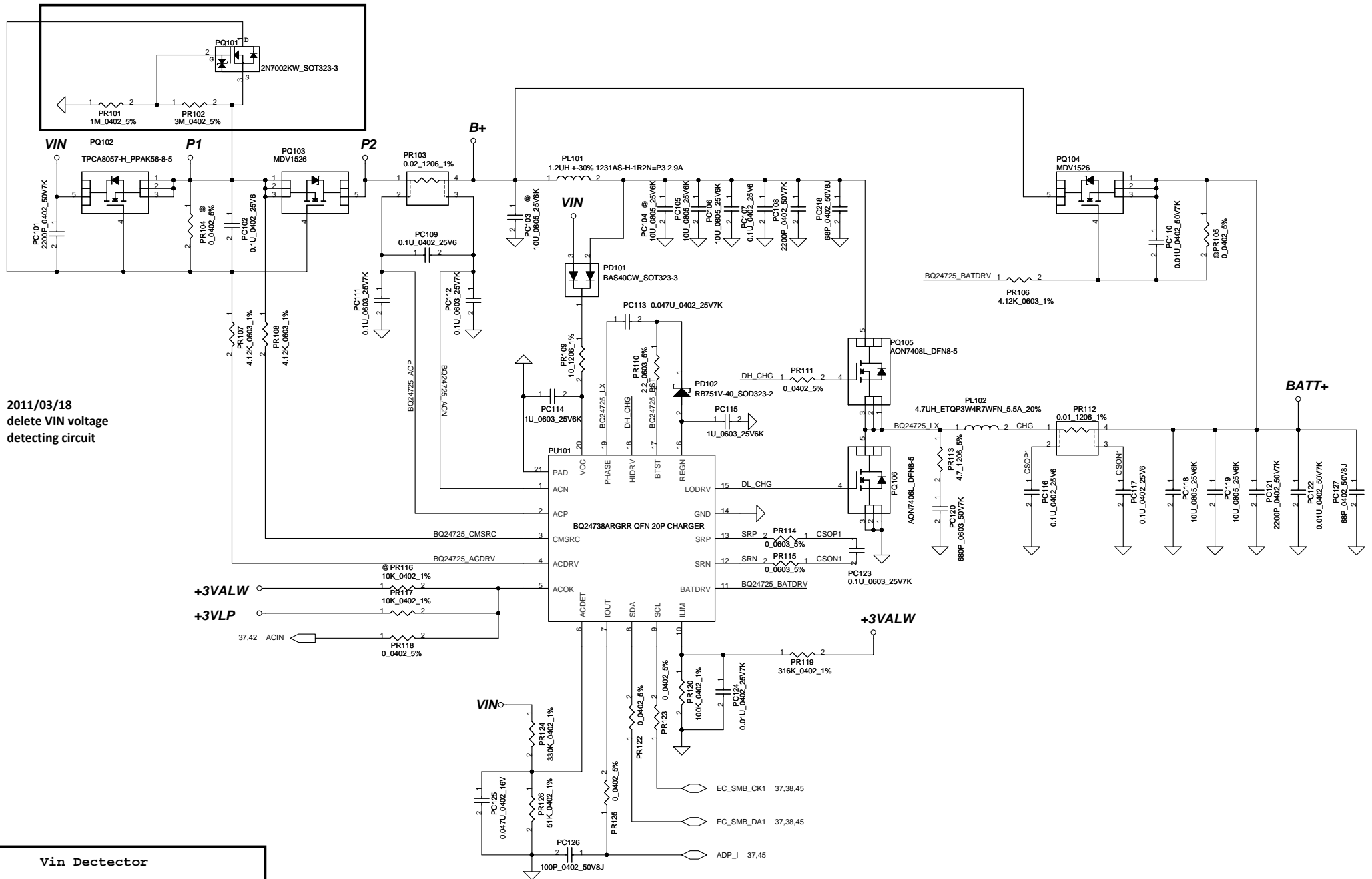
+3VALWP **+3VALW** (5A,200mils ,Via NO.= 10)



For KB930 --> Keep PD301, PR317, PR319

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for reverse input protection



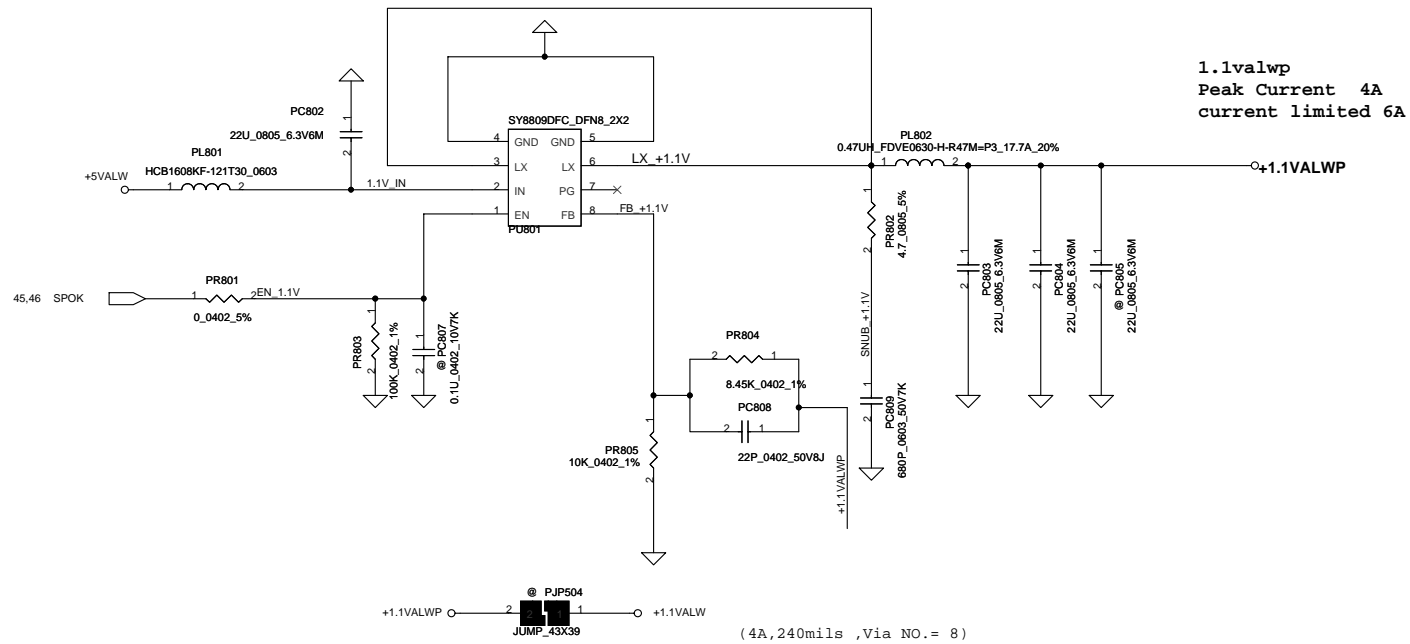
2011/03/18
delete VIN voltage
detecting circuit

Vin Detector

	Min.	Typ	Max.
H-->L		17.33V	
L-->H		16.98V	

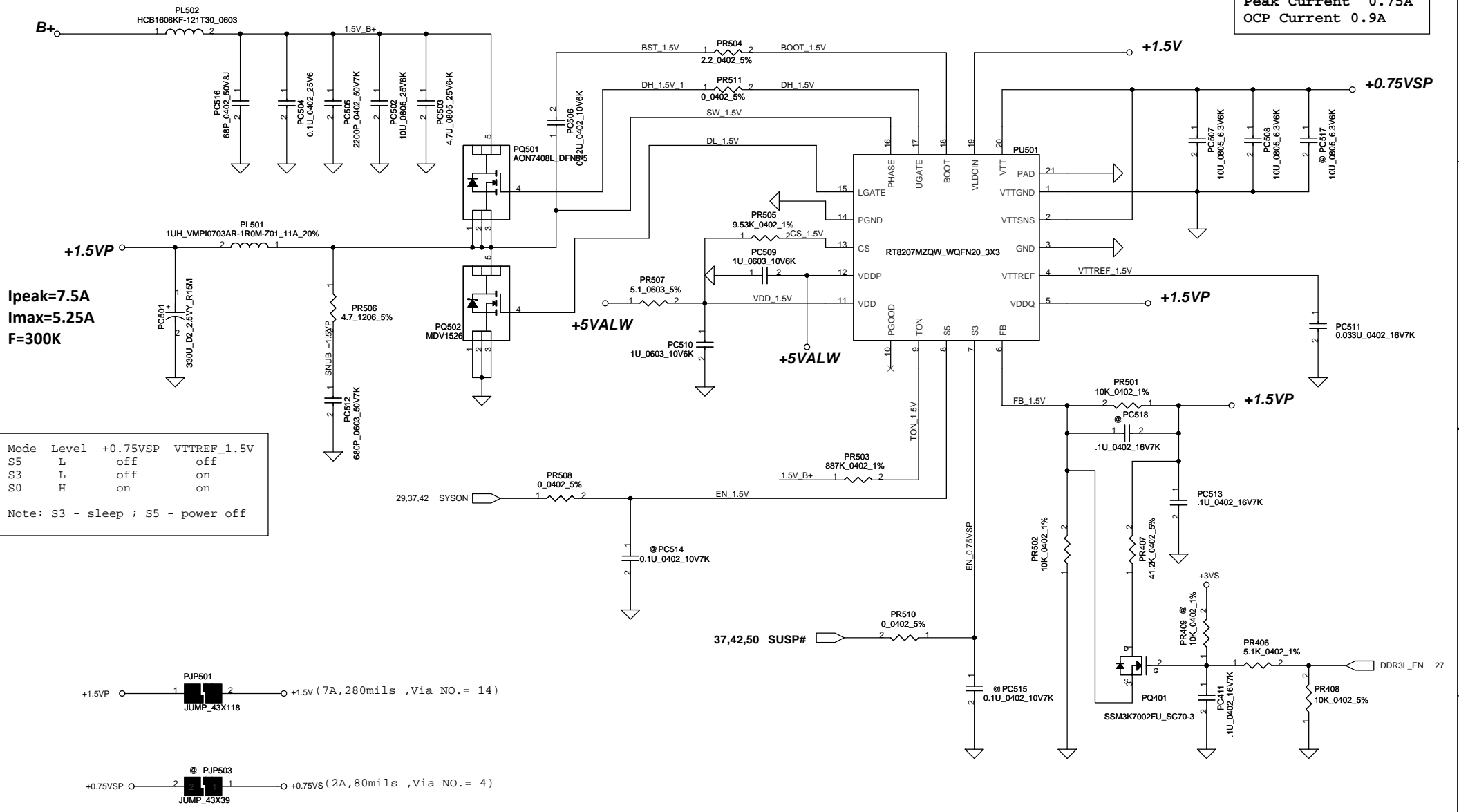
ILIM and external DPM
4.36A

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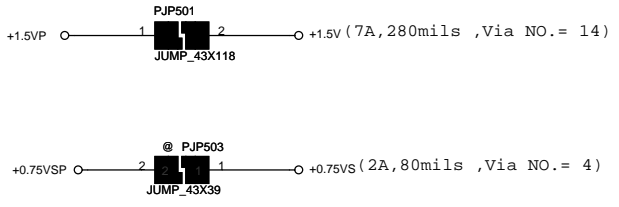
0.75Volt +/- 5%
 TDC 0.525A
 Peak Current 0.75A
 OCP Current 0.9A



I_{peak}=7.5A
 I_{max}=5.25A
 F=300K

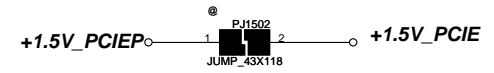
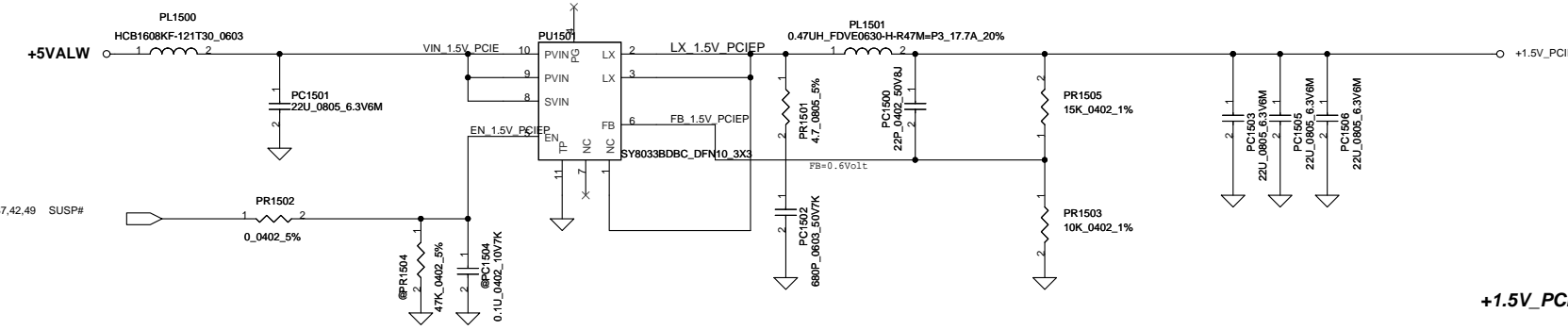
Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	off
S0	H	on	on

Note: S3 - sleep ; S5 - power off



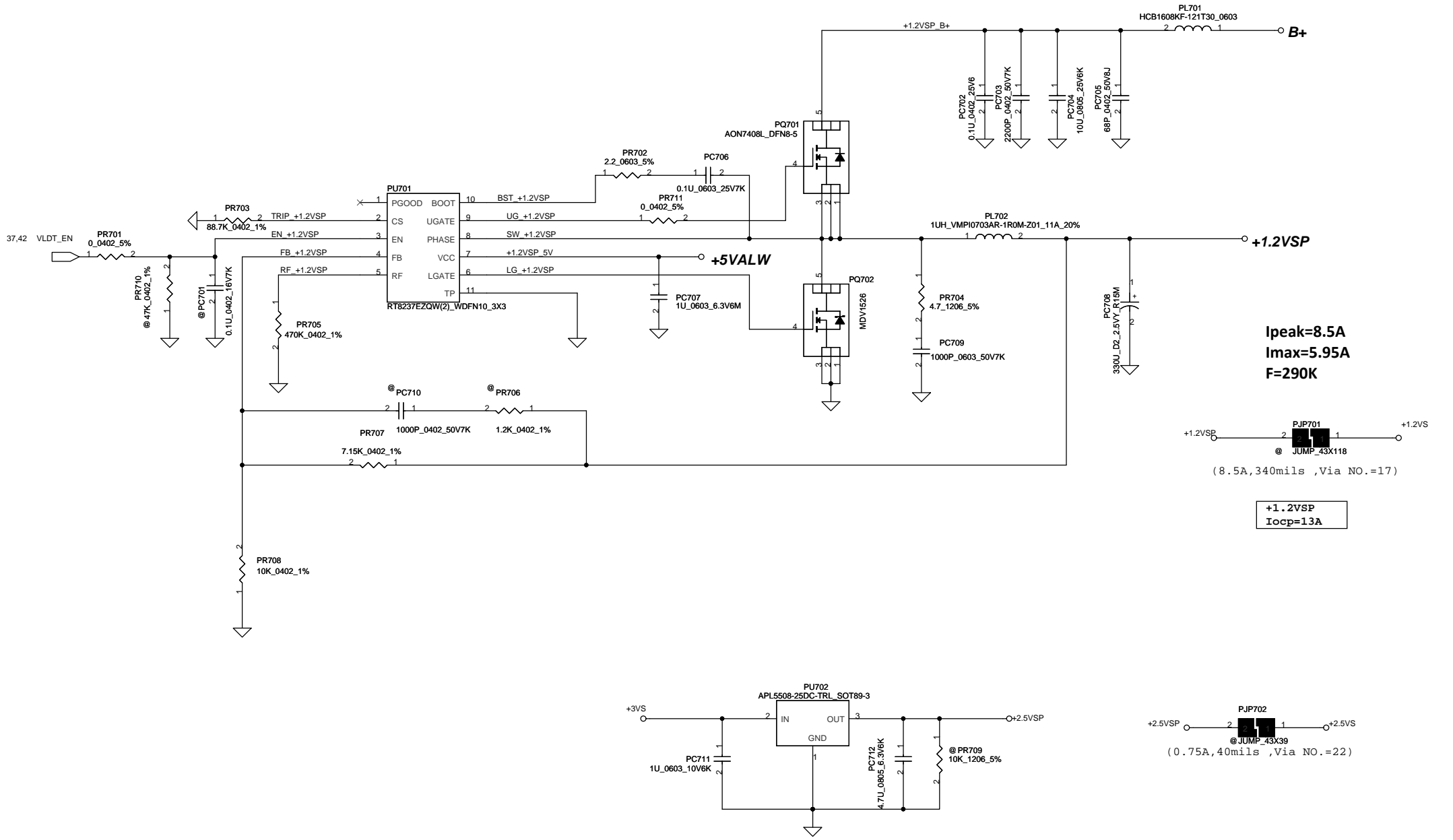
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1.5VPCIEP
 Peak Current 6A
 OCP current 6A



(6A,240mils ,Via NO.= 12)

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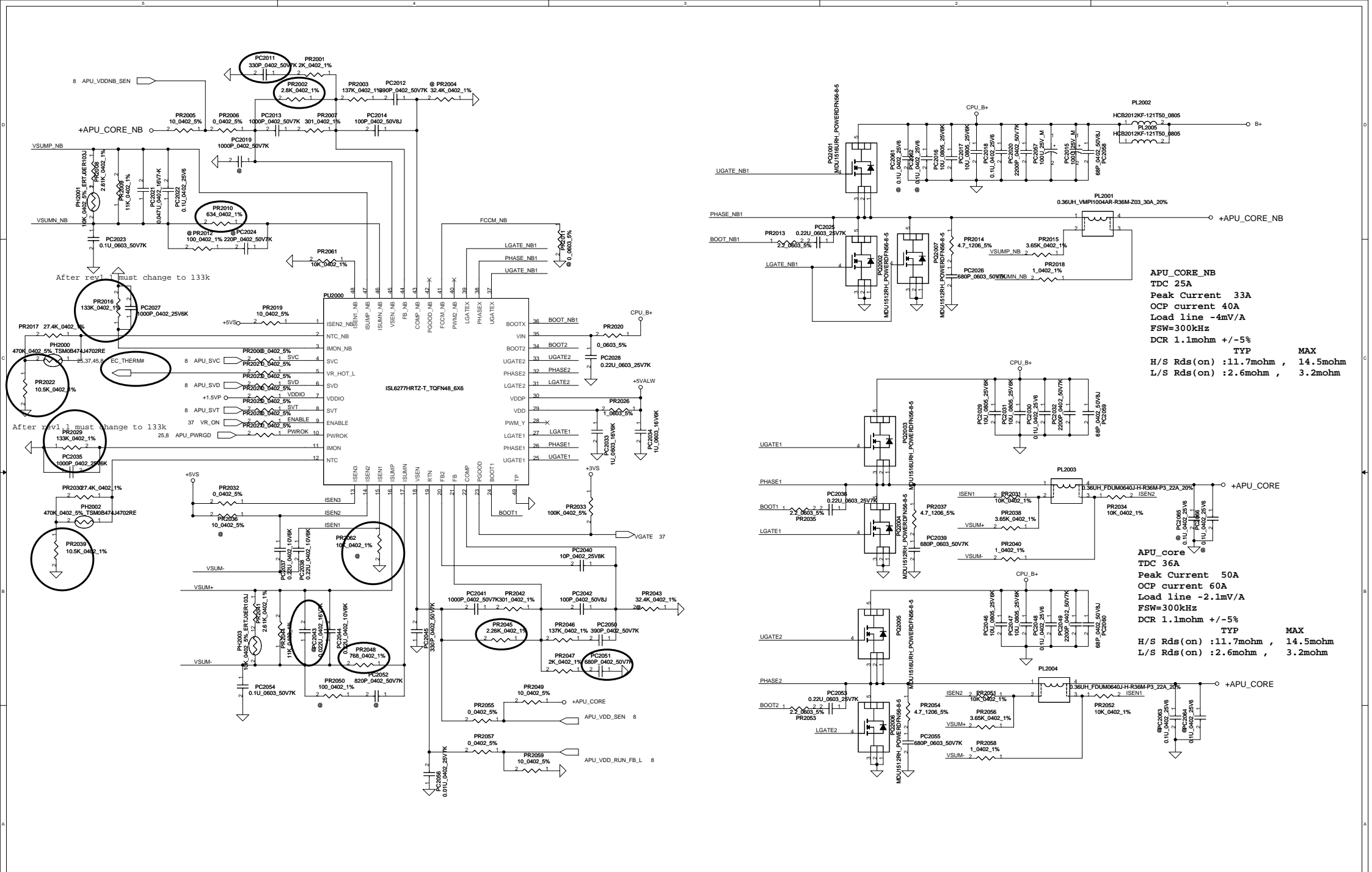


Ipeak=8.5A
I_{max}=5.95A
F=290K

+1.2VSP
I_{ocp}=13A

PJP702
 @ JUMP 43X39
 (0.75A, 40mils, Via NO.=22)

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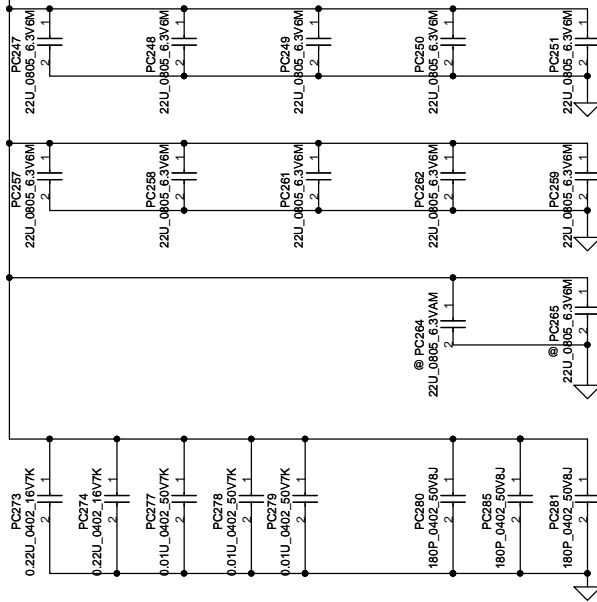
APU_CORE_NB
 TDC 25A
 Peak Current 33A
 OCP current 40A
 Load line -4mV/A
 FSW=300kHz
 DCR 1.1mohm +/-5%
 TYP MAX
 H/S Rds(on) : 11.7mohm , 14.5mohm
 L/S Rds(on) : 2.6mohm , 3.2mohm

APU_core
 TDC 36A
 Peak Current 50A
 OCP current 60A
 Load line -2.1mV/A
 FSW=300kHz
 DCR 1.1mohm +/-5%
 TYP MAX
 H/S Rds(on) : 11.7mohm , 14.5mohm
 L/S Rds(on) : 2.6mohm , 3.2mohm

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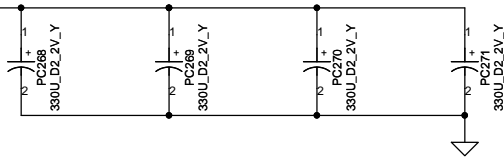
+APU_CORE

+APU_CORE

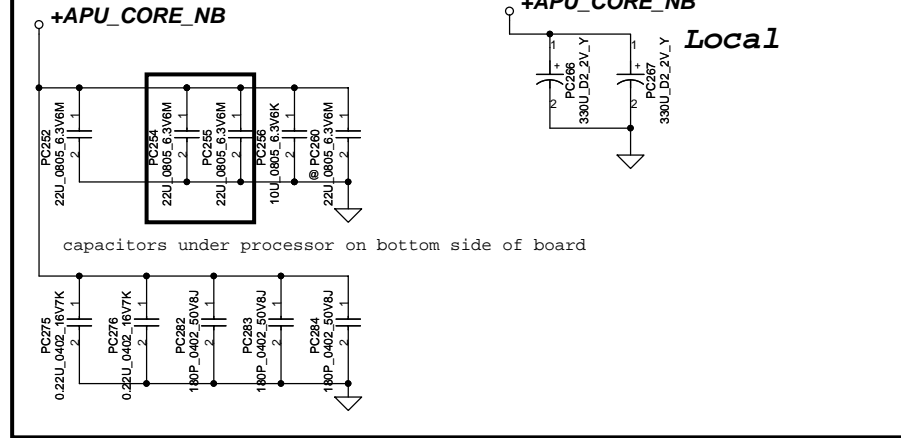


+APU_CORE

Local



+APU_CORE_NB



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NO DATE	PAGE	MODIFICATION LIST	PURPOSE
DB-2(12/2)	P44-PWR-DCIN / Vin Detector	Change to PJP1 pine define	DC-IN jack buy and sale define does not change
DB-2(12/8)	P45-PWR-BATTERY CONN	Pin 7 power source change +3VLP to +3VALW	EC command
DB-2(12/8)	P52-PWR-+1.5VPCIE/0.935V	PC11506 loaction change to PC1156	CIC SMT command
DB-2(12/12)	P52-PWR-+1.5VPCIE/1V	Change PR9352 11.3K to 13.3K (0.935V to 1V)	HW comand
DB-2(12/13)	P50-PWR-1.1VALWP	Add PR803 =10K	SY8809 enbale pin issue

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