

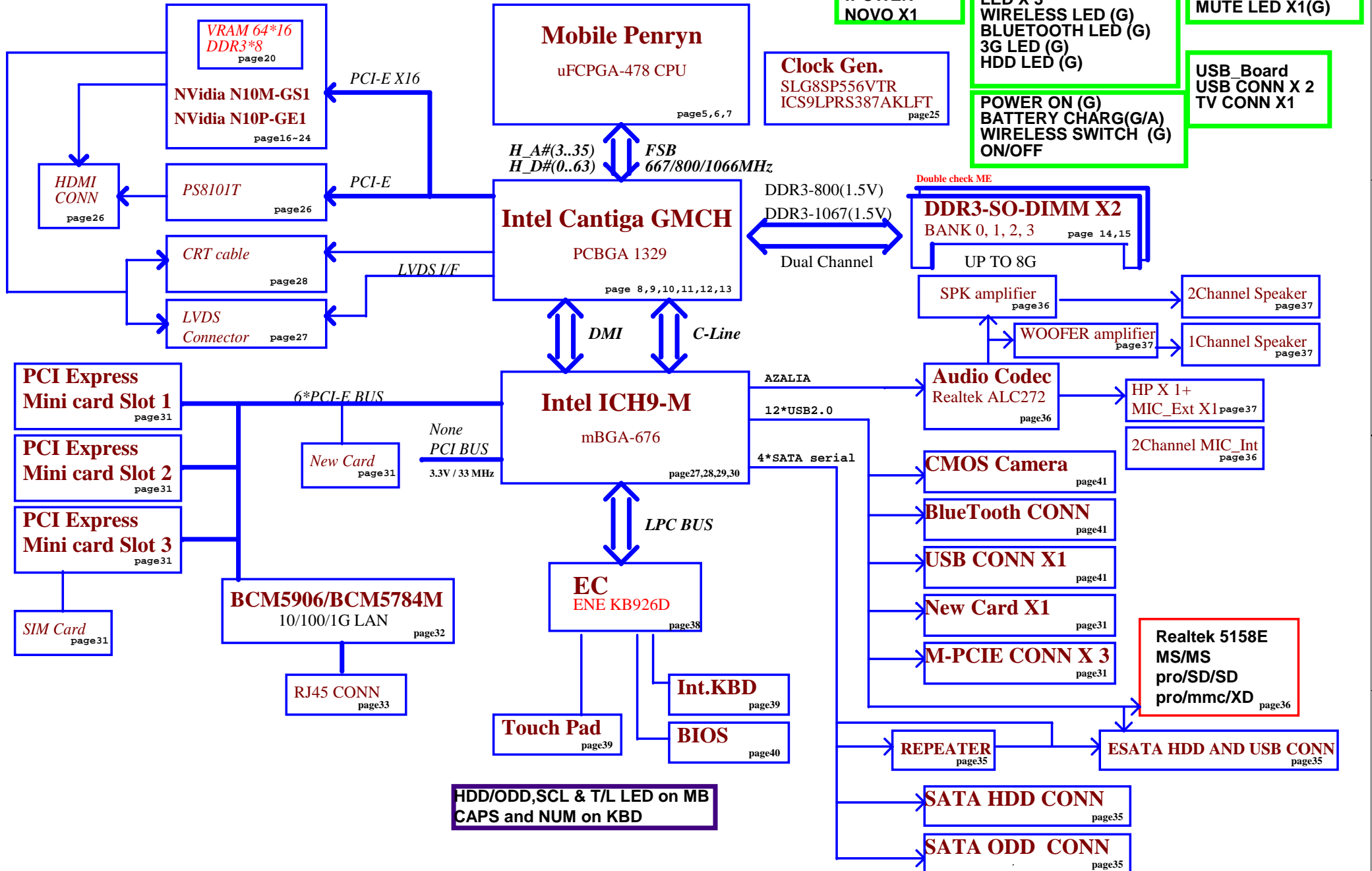
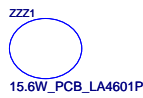
# Blue Moutain KIWB1/B2

## Schematics Document

Mobile Penryn uFCPGA with Intel  
Cantiga\_GM/PM+ICH9-M core logic

REV:2.0

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# DDR3 Voltage Rails

power plane	+B	+5VALW	<b>+1.5V</b>	+5VS +3VS +1.5VS +1.1VS +VCCP +CPU_CORE +VGA_CORE +1.8VS <b>+0.75V</b>
		+3VALW		
State				
S0	○	○	○	○
S3	○	○	○	X
S5 S4/AC	○	○	X	X
S5 S4/ Battery only	○	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

## @ FUNCTION

100@	(100 LAN)		
TVSW@	(TV POWER SW)	10M@	(N10M 40nm CHIPSET)
AO@	(ALWAYS ON SW)	10P@	(N10P 40nm CHIPSET)
MONO@	(MONO MIC)	PM@	(VGA BOM)
X76@	(X76 BOM)	45@	(45 BOM)
		GM@	(UMA BOM)
		GM45@	(GM45 BOM)
		GL40@	(GL40 BOM)
BT@	WITH BLUETOOTH	GIGA@	(GIGA LAN)
3G@	WITH 3G	NO TVSW@	(NON TV POWER SW)
TV@	WITH TV	NO AO@	(NON ALWAYS ON SW)
		ARRAY@	(ARRAY MIC)
		S512@	FOR X76 BOM
		Q512@	FOR X76 BOM
		S256@	FOR X76 BOM
		Q256@	FOR X76 BOM

SMBUS, SPI and I2C Control Table

	SOURCE	HDMI	LVDS	CRT	HDCP	SERIAL EEPROM	NEW CARD	CLK GEN	CAP sensor	Mini CARD1	Mini CARD2	BATT	THERMAL SENSOR (VGA)	THERMAL SENSOR (CPU)
EC_SMB_CK1 EC_SMB_DA1	KB926	X	X	X	X	X	X	X	X	X	X	V	X	X
EC_SMB_CK2 EC_SMB_DA2	KB926	X	X	X	X	X	X	X	V	X	X	X	V	V
ICH_SMBOLK ICH_SMBDAT	ICH9	X	X	X	X	X	V	V	X	V	V	X	X	X
LVDS_SCL LVDS_SDA	Cantiga	X	V	X	X	X	X	X	X	X	X	X	X	X
GMCH_CRT_CLK GMCH_CRT_DAT	Cantiga	X	X	V	X	X	X	X	X	X	X	X	X	X
HDMICLK_NB HDMIDAT_NB	Cantiga	V	X	X	X	X	X	X	X	X	X	X	X	X
VGA_DDCCLK VGA_DDCDATA	VGA	X	X	V	X	X	X	X	X	X	X	X	X	X
VGA_LVDS_SCL VGA_LVDS_DAT	VGA	X	V	X	X	X	X	X	X	X	X	X	X	X
VGA_HDMI_SCL VGA_HDMI_DAT	VGA	V	X	X	X	X	X	X	X	X	X	X	X	X
HDCP_SMB_CK1 HDCP_SMB_DA1	VGA	X	X	X	X	V	X	X	X	X	X	X	X	X
FSEL#SPICS#_SB FRD#SPI_SO_SB SPI_CLK_SB FWR#SPI_SI_SB	ICH9	X	X	X	X	V	X	X	X	X	X	X	X	X
FSEL#SPICS# FRD#SPI_SO SPI_CLK FWR#SPI_SI	KB926	X	X	X	X	V	X	X	X	X	X	X	X	X

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# VGA and DDR3 Voltage Rails (N10x GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	N/A	N/A	
GPIO1	IN	-	Hot plug detect for IFP link C
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID0
GPIO6	OUT	-	GPU VID1
GPIO7	OUT	-	GPU VID2
GPIO8	I/O	L	Thermal Catastrophic Overtemp
GPIO9	OUT	L	Thermal Alert
GPIO10	OUT		Memory VREF switch
GPIO11	I/O	L	SLI raster sync
GPIO12	IN	-	AC power detect pin
GPIO13	OUT	-	MEM_VID or Power supply control
GPIO14	OUT	-	Power supply control
GPIO15	IN	-	Hot plug detect for IFP Link E
GPIO16	OUT	-	Programmable Fan Control
GPIO17	IN	-	
GPIO18	IN	-	
GPIO19	IN	-	Hot plug detect for IFP Link D
GPIO20	IN	-	
GPIO21	IN	-	Hot plug detect for IFP link F
GPIO22	IN	-	SLI swap ready signal
GPIO23	I/O		

GPIO6	GPIO5	N10M-GS	N10P-GS
GPU_VID1	GPU_VID0	VGA_CORE	P-State
0	0	0.8V	12
0	1	0.85V	12
1	1	0.9V	0, 10

# Performance Mode P0 TDP at Tj = 102 C\* (DDR3)

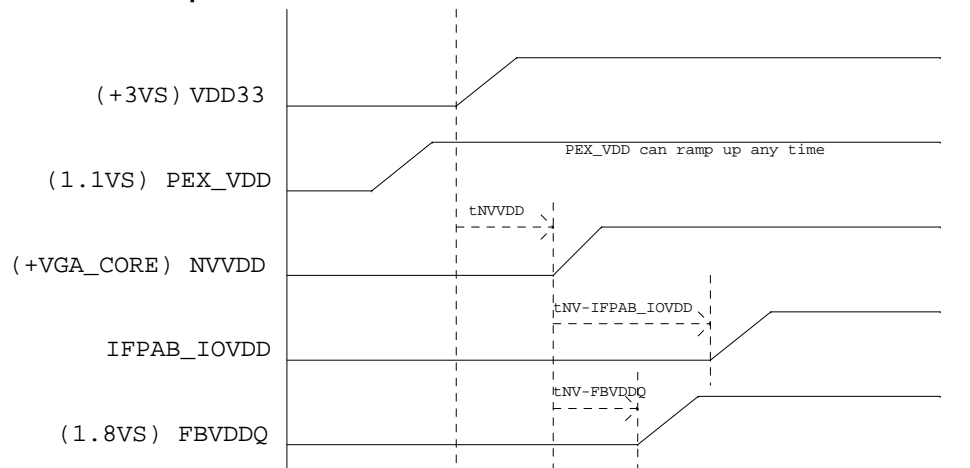
Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)			FBVDD (1.5V) (W)		FBVDDQ (GPU+Mem) (1.5V) (W)		PCI Express (1.05V) (6) (W)		I/O and PLLVDD (1.8V) (W)		I/O and PLLVDD (1.05V) (W)		Other (3.3V) (W)	
				(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N10P-GS 128bit 1024MB DDR3	21.07	6.67	TBD	TBD	18.25	17.34	2.06	3.09	4.09	6.14	850	0.89	75	0.14	63	0.07	55	0.18
N10P-GE 128bit 1024MB DDR3	20.97	6.73	TBD	TBD	19.17	17.25	2.03	3.05	4.09	6.14	840	0.88	75	0.14	63	0.07	55	0.18
N10P-LP 128bit 1024MB DDR3	15.48	6.44	TBD	TBD	13.95	11.86	1.90	2.85	3.99	5.99	810	0.85	75	0.14	63	0.07	55	0.18

# Performance Mode P0 TDP at Tj = 102 C\* (DDR3)

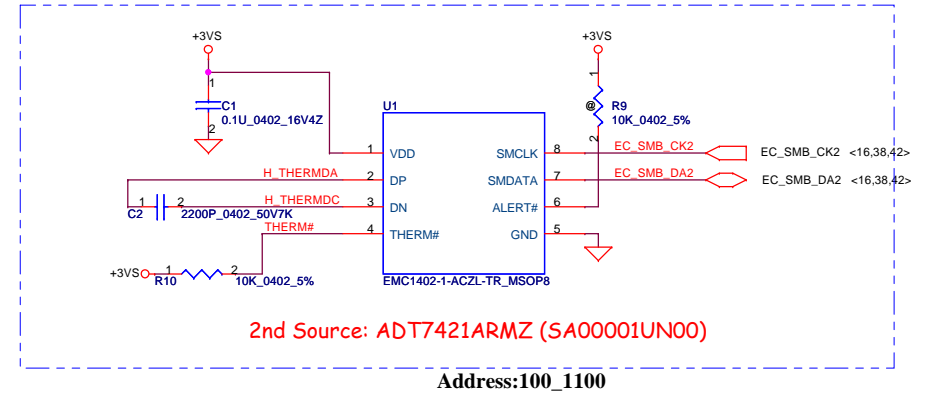
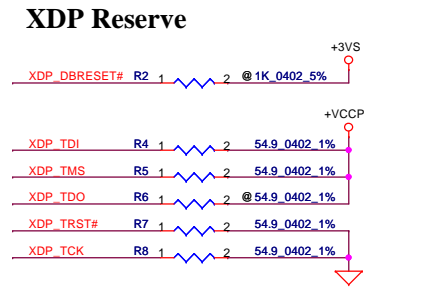
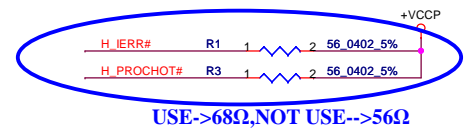
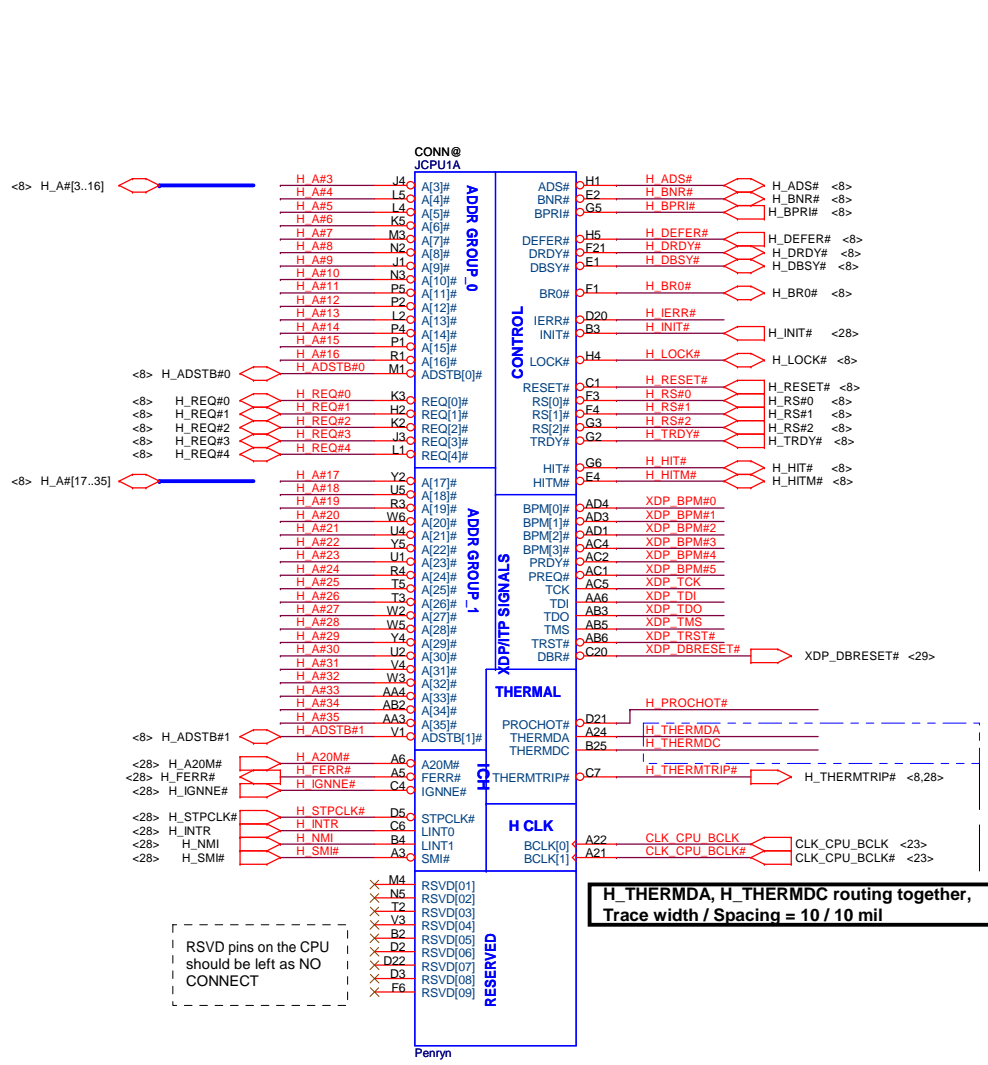
Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)			FBVDD (1.5V) (W)		FBVDDQ (GPU+Mem) (1.5V) (W)		PCI Express (1.05V) (6) (W)		I/O and PLLVDD (1.8V) (W)		I/O and PLLVDD (1.05V) (W)		Other (3.3V) (W)	
				(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N10M-GE 64bit 512MB DDR3	13.36	2.93	TBD	TBD	11.89	10.70	0.66	0.99	2.16	3.24	792	0.83	75	0.14	63	0.07	100	0.33
N10M-GS 64bit 512MB DDR3	14.29	3.10	TBD	TBD	11.53	11.53	0.70	1.05	2.28	3.42	817	0.86	75	0.14	63	0.07	100	0.33
N10M-LP 64bit 512MB DDR3	8.28	2.91	TBD	TBD	6.60	5.61	0.62	0.93	2.20	3.3	782	0.82	75	0.14	63	0.07	100	0.33

# Power Sequence

The ramp time for any rail must be more than 40us

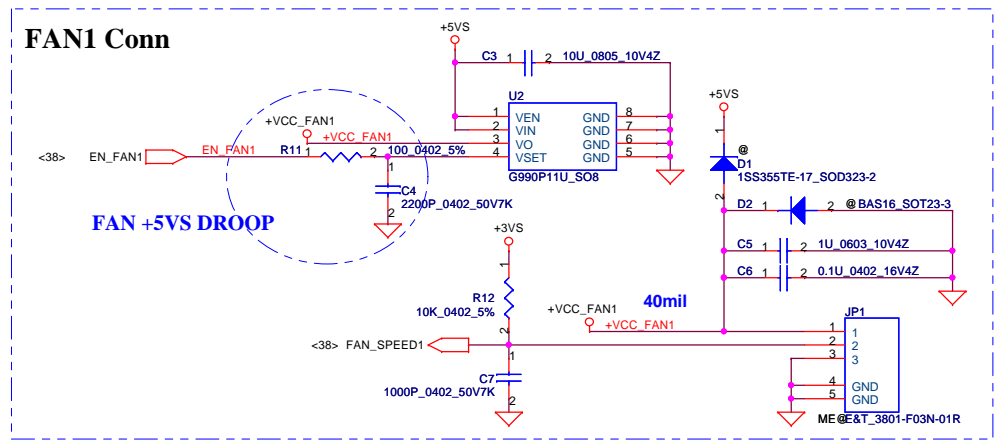


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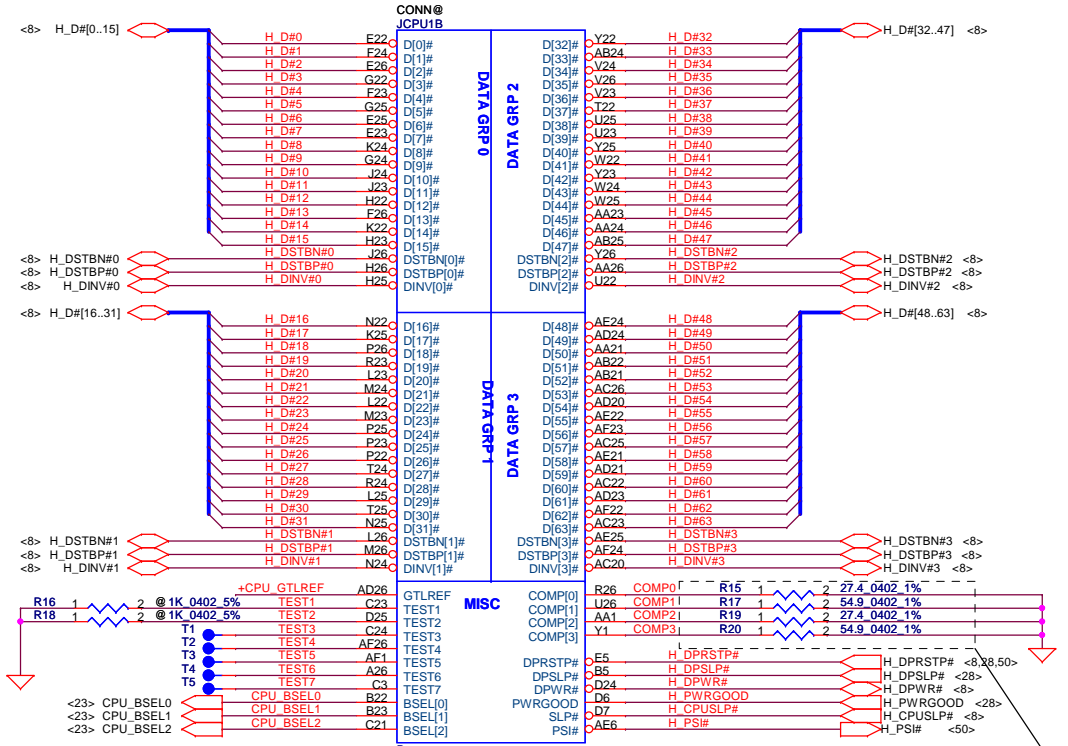


**H\_THERMDA, H\_THERMDC routing together, Trace width / Spacing = 10 / 10 mil**

RSVD pins on the CPU should be left as NO CONNECT



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Trace Close CPU < 0.5"

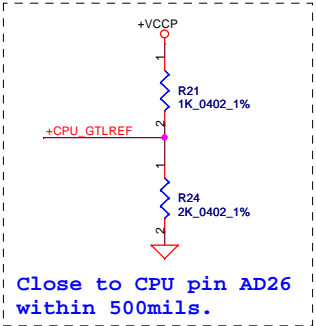
Width=4 mil ,  
Spacing: 15mil  
(55Ohm)

TRACE CLOSELY CPU < 0.5"

COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)  
COMP1, COMP3 layout : Width 5mils and Space 25mils (55Ohms)

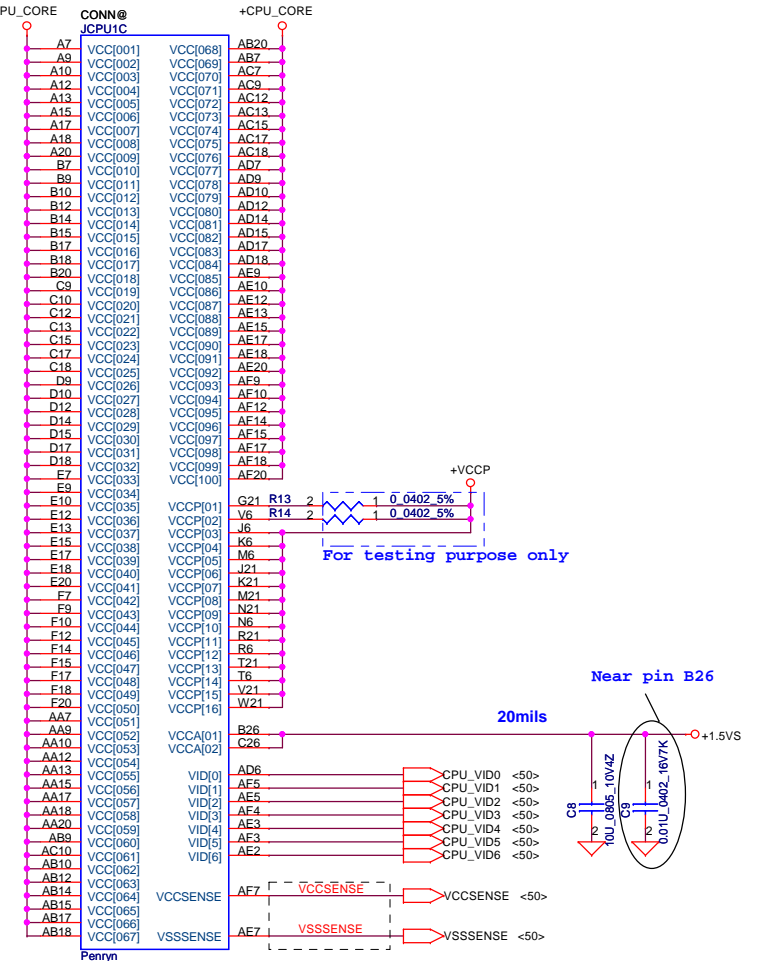
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

Layout note: Z0=55 ohm  
0.5" max for GTLREF.



Close to CPU pin AD26  
within 500mils.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0



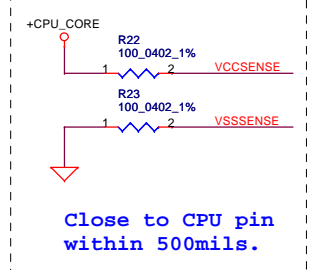
For testing purpose only

Near pin B26

20mils

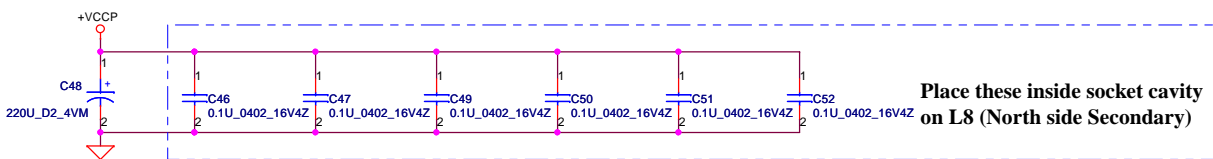
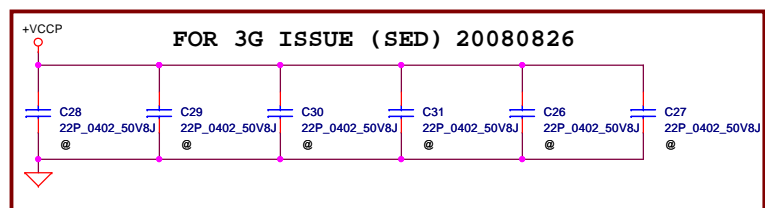
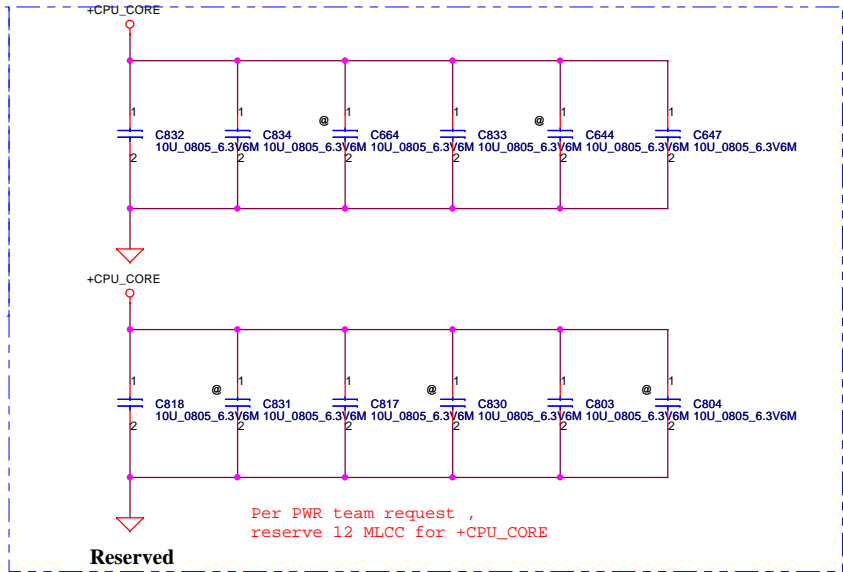
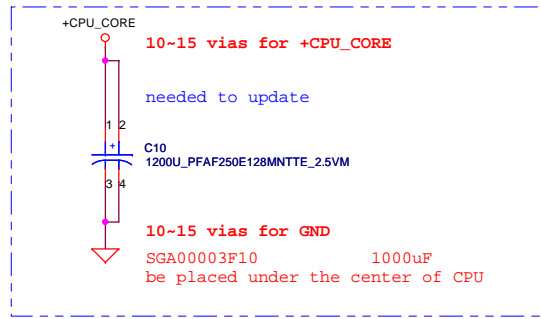
Length match within 25 mils.  
The trace width/space/other is  
18/7/25.

Layout Note:  
Route VCCSENSE and VSSSENSE traces at  
27.4 Ohms with 50 mil spacing.  
Place PU and PD within 1 inch of CPU.  
Length matched to within 25 mils.



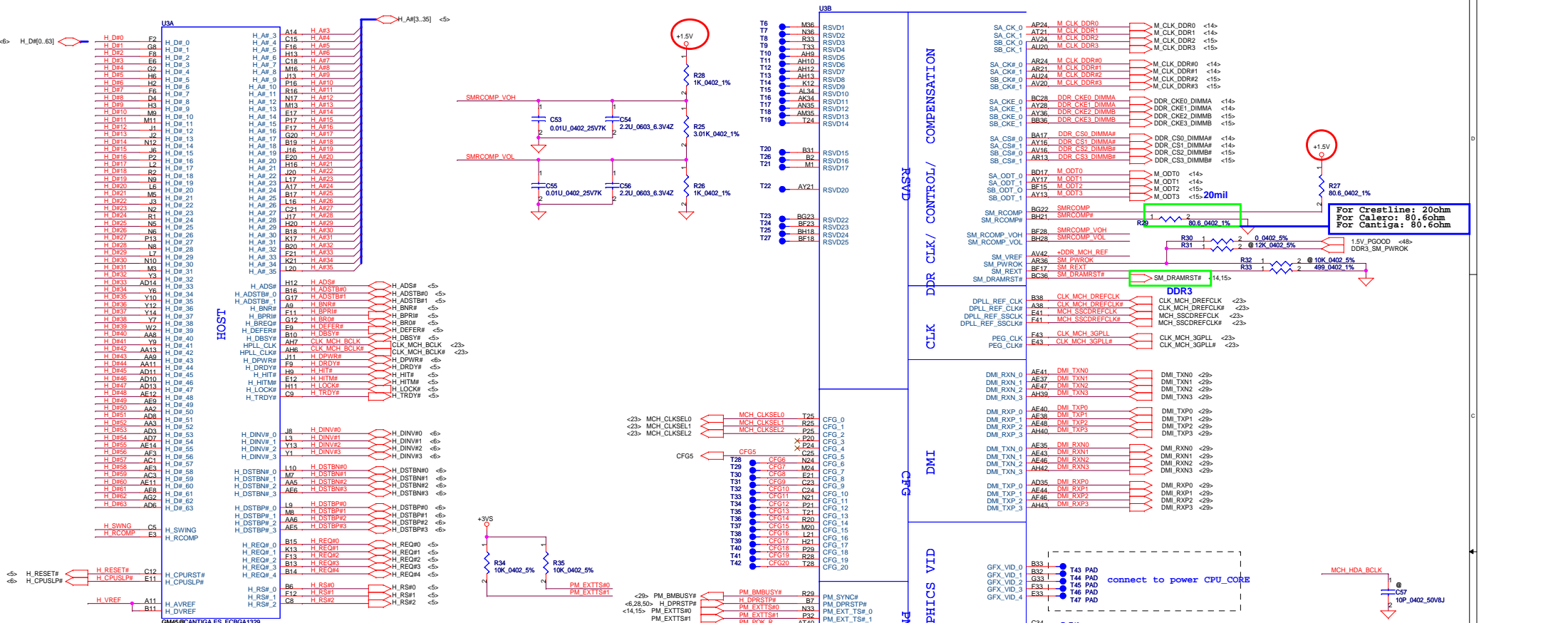
Close to CPU pin  
within 500mils.

CONN@		JCPU1D	
A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[003]	VSS[084]	R2
A16	VSS[004]	VSS[085]	R5
A19	VSS[005]	VSS[086]	R22
A23	VSS[006]	VSS[087]	R25
AF2	VSS[007]	VSS[088]	T1
B6	VSS[008]	VSS[089]	T4
B8	VSS[009]	VSS[090]	T23
B11	VSS[010]	VSS[091]	T26
B13	VSS[011]	VSS[092]	U3
B16	VSS[012]	VSS[093]	U6
B19	VSS[013]	VSS[094]	U21
B21	VSS[014]	VSS[095]	U24
B24	VSS[015]	VSS[096]	V2
C4	VSS[016]	VSS[097]	V5
C8	VSS[017]	VSS[098]	V22
C11	VSS[018]	VSS[099]	V25
C14	VSS[019]	VSS[100]	W1
C16	VSS[020]	VSS[101]	W4
C19	VSS[021]	VSS[102]	W26
C2	VSS[022]	VSS[103]	Y26
C22	VSS[023]	VSS[104]	Y3
C25	VSS[024]	VSS[105]	Y6
D1	VSS[025]	VSS[106]	Y21
D4	VSS[026]	VSS[107]	Y24
D8	VSS[027]	VSS[108]	AA2
D11	VSS[028]	VSS[109]	AA5
D13	VSS[029]	VSS[110]	AA8
D16	VSS[030]	VSS[111]	AA11
D19	VSS[031]	VSS[112]	AA14
D23	VSS[032]	VSS[113]	AA16
D26	VSS[033]	VSS[114]	AA19
E3	VSS[034]	VSS[115]	AA22
E6	VSS[035]	VSS[116]	AA25
E8	VSS[036]	VSS[117]	AB1
E11	VSS[037]	VSS[118]	AB4
E14	VSS[038]	VSS[119]	AB8
E16	VSS[039]	VSS[120]	AB11
E19	VSS[040]	VSS[121]	AB13
E21	VSS[041]	VSS[122]	AB16
E24	VSS[042]	VSS[123]	AB19
F5	VSS[043]	VSS[124]	AB23
F8	VSS[044]	VSS[125]	AB26
F11	VSS[045]	VSS[126]	AC3
F13	VSS[046]	VSS[127]	AC6
F16	VSS[047]	VSS[128]	AC9
F19	VSS[048]	VSS[129]	AC11
F2	VSS[049]	VSS[130]	AC14
F22	VSS[050]	VSS[131]	AC16
F25	VSS[051]	VSS[132]	AC19
G4	VSS[052]	VSS[133]	AC21
G1	VSS[053]	VSS[134]	AC24
G23	VSS[054]	VSS[135]	AD2
G26	VSS[055]	VSS[136]	AD5
H3	VSS[056]	VSS[137]	AD8
H6	VSS[057]	VSS[138]	AD11
H21	VSS[058]	VSS[139]	AD13
H24	VSS[059]	VSS[140]	AD16
J2	VSS[060]	VSS[141]	AD19
J5	VSS[061]	VSS[142]	AD22
J22	VSS[062]	VSS[143]	AD25
J25	VSS[063]	VSS[144]	AE1
K1	VSS[064]	VSS[145]	AE4
K4	VSS[065]	VSS[146]	AE8
K23	VSS[066]	VSS[147]	AE11
K26	VSS[067]	VSS[148]	AE14
L3	VSS[068]	VSS[149]	AE16
L6	VSS[069]	VSS[150]	AE19
L21	VSS[070]	VSS[151]	AE23
L24	VSS[071]	VSS[152]	AE26
M2	VSS[072]	VSS[153]	A2
M5	VSS[073]	VSS[154]	AF6
M22	VSS[074]	VSS[155]	AF8
M25	VSS[075]	VSS[156]	AF11
N1	VSS[076]	VSS[157]	AF13
N4	VSS[077]	VSS[158]	AF16
N23	VSS[078]	VSS[159]	AF19
N26	VSS[079]	VSS[160]	AF21
P3	VSS[080]	VSS[161]	A25
	VSS[081]	VSS[162]	AE25
	VSS[163]		

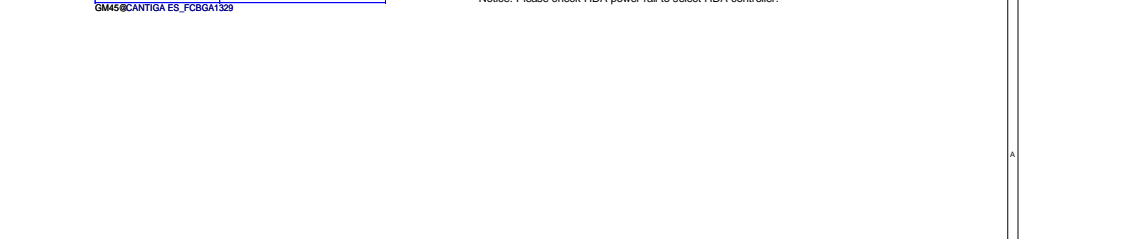
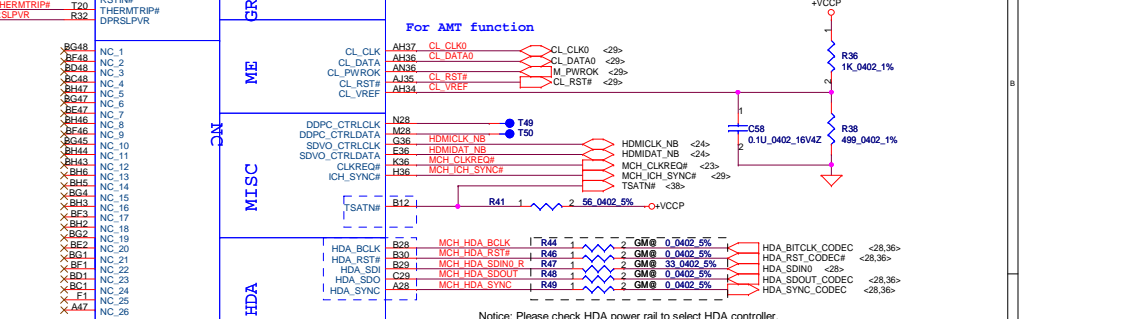
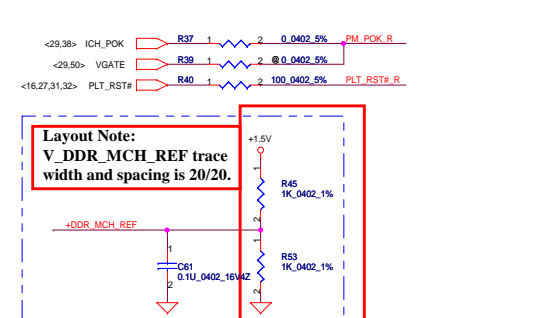
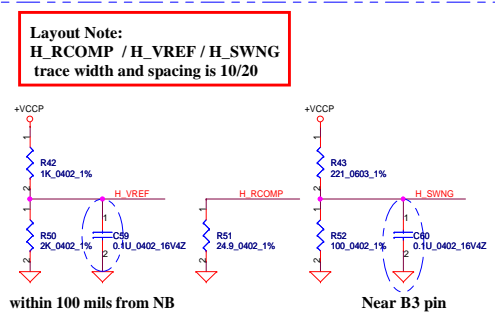


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B	KIW10/11_LA4142P	0.1		Wednesday, March 18, 2009	
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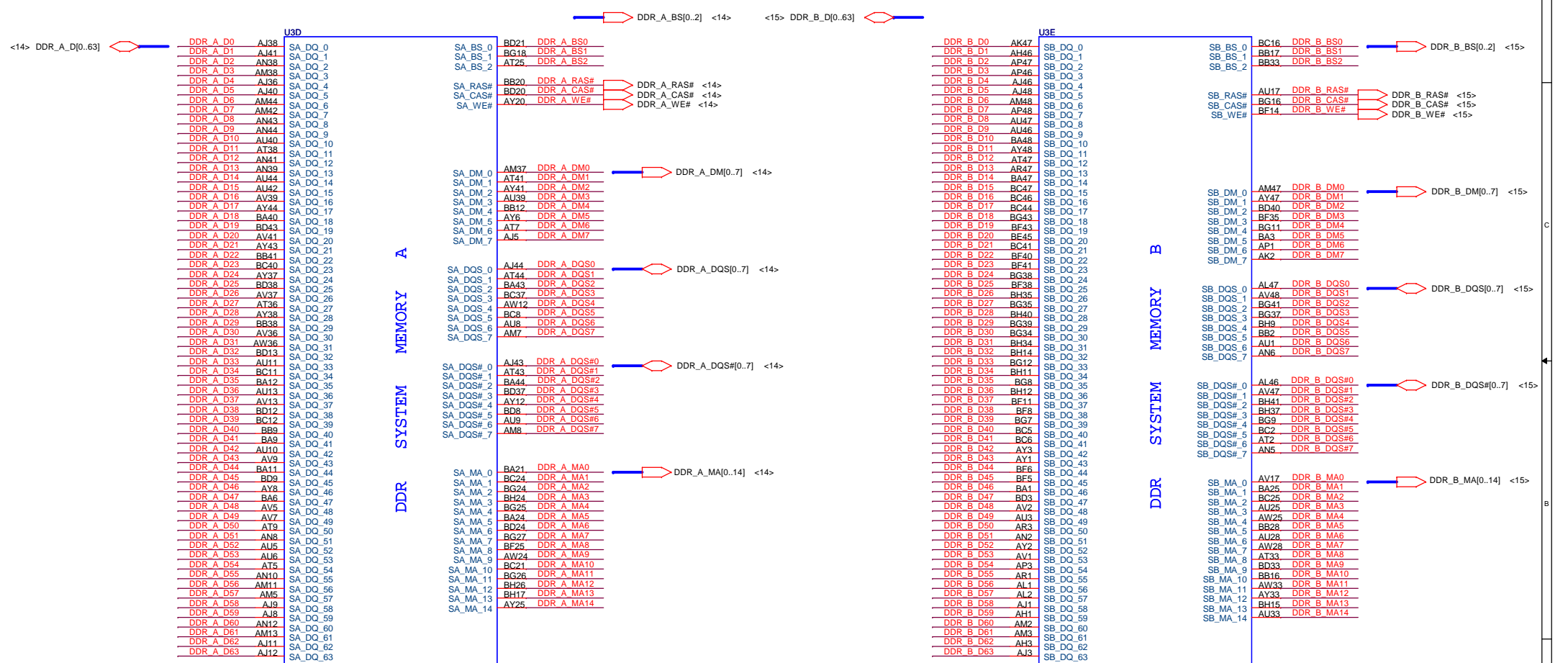




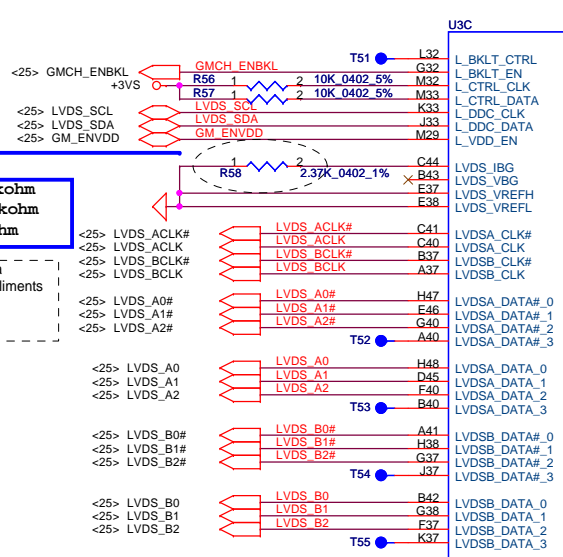
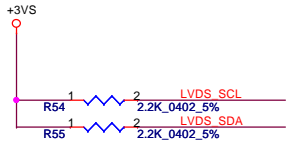
layout note:  
Route H\_SCOMP# and H\_SCOMP# with trace width spacing and impedance (55 ohm) same as FSB data traces







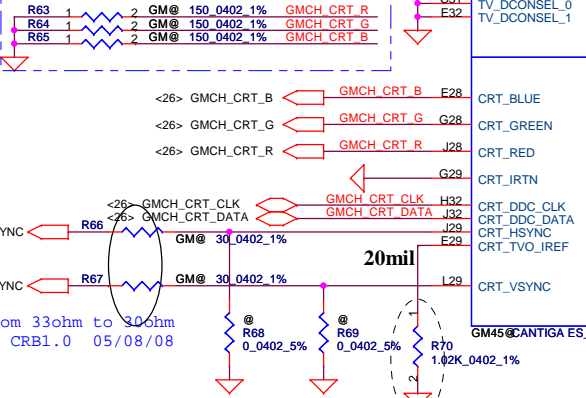
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Size	Document Number			Rev	
B	KIWB3/B4_LA4551P			0.1	
Date:	Wednesday, March 18, 2009			Sheet	9 of 53



For Cantiga: 2.37kohm  
For Crestline: 2.4kohm  
For Calero: 1.5kohm

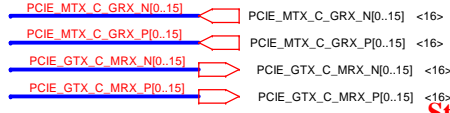
Note: All LVDS data signals and it's compliments should be routed Differentially

Layout Note: Place 150 Ω termination resistors close to GMCH

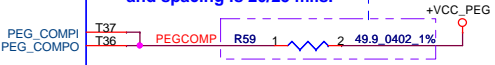


change R64, R65 from 330ohm to 30ohm by checklist 2.0 & CRB1.0 05/08/08

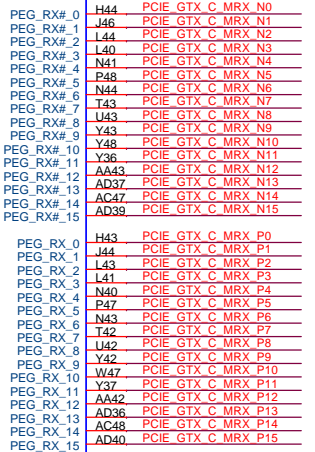
For Cantiga: 1.02kohm  
For Crestline: 1.3kohm  
For Calero: 255ohm



Place the resistor within 500mils (1.27mm) of the (G)MCH PEGCOMP trace width and spacing is 20/25 mils.



Please check Power source if want support IAMT



### Strap Pin Table

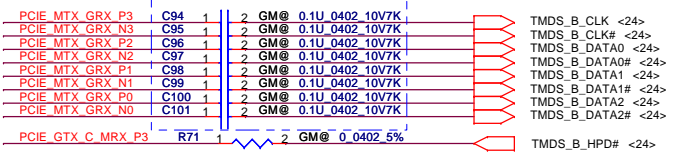
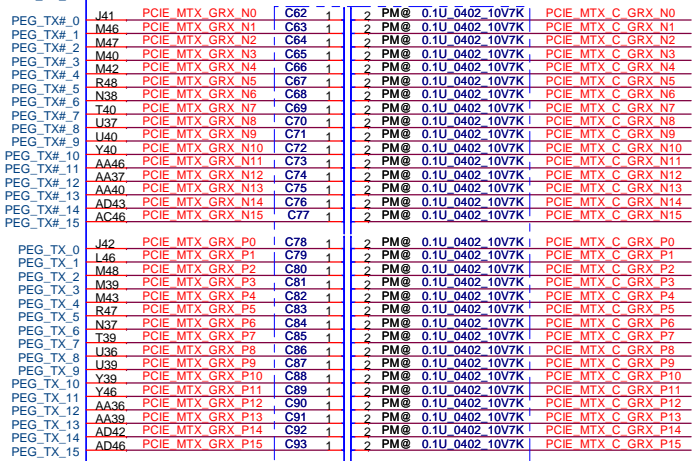
CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The ITPM Host Interface is enable 1 = The ITPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 = (TLS)chipset suite with no confidentiality 1 = (TLS)chipset suite with confidentiality
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane, 15->0, 14->1 1 = Normal Operation, Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) 1 = Reverse Lane *
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu. *

LVDS

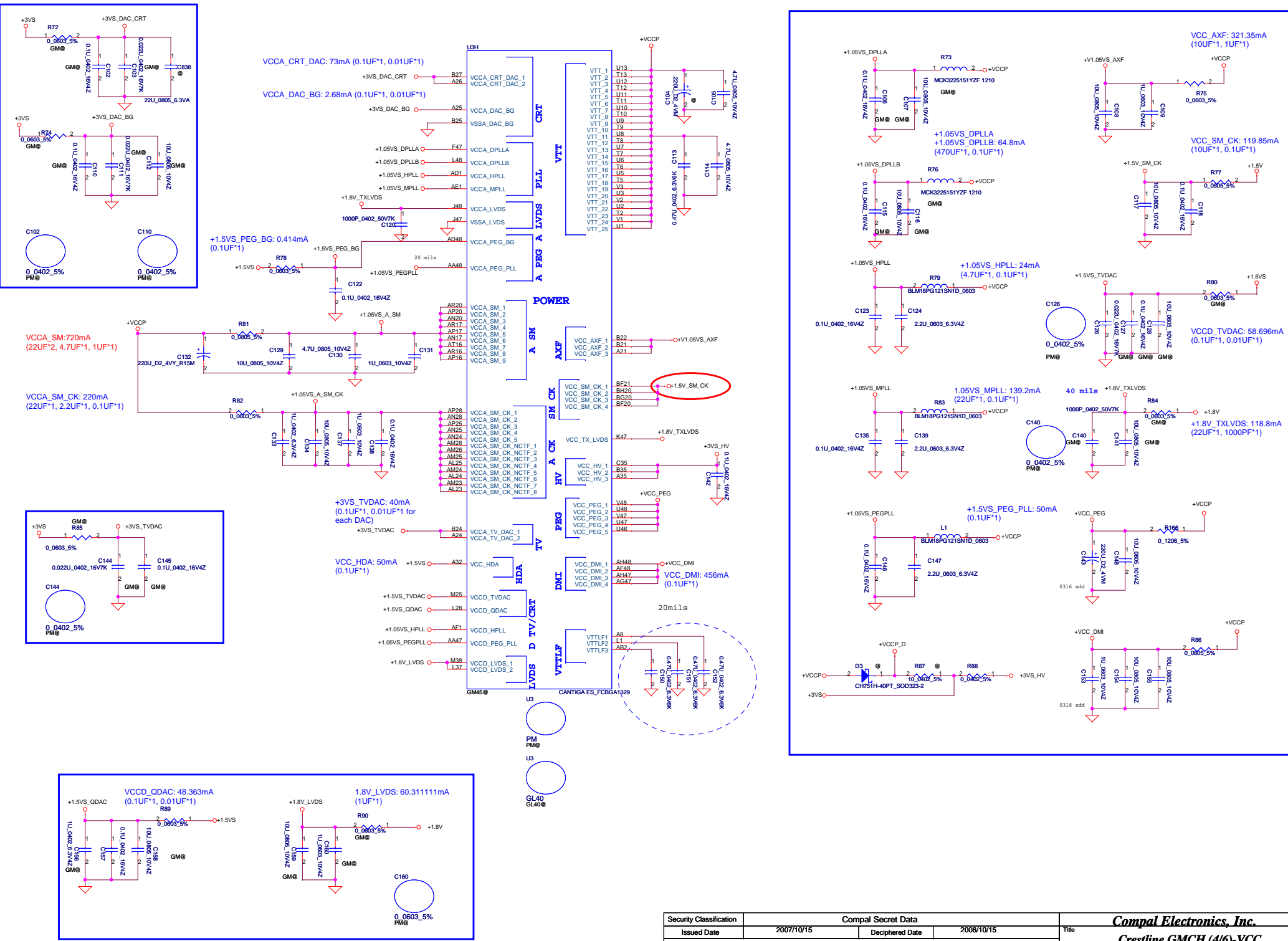
PCI-EXPRESS

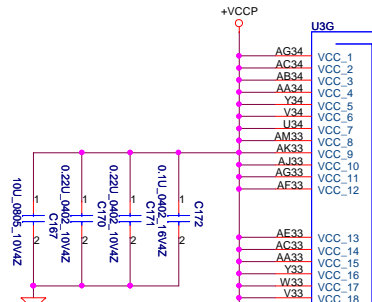
VGA

CLOSE TO MCH



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Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	Cantiga(3/6)-VGA/LVDS/TV
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Custom	KIWB3/B4_LA4551P	0.1			
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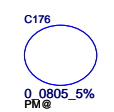
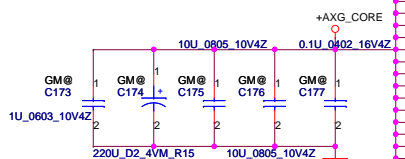
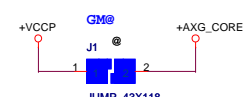
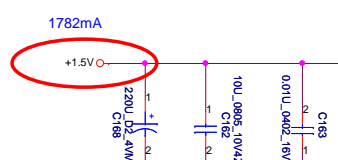


- VCC 1 AG34
- VCC 2 AC34
- VCC 3 AB34
- VCC 4 AA34
- VCC 5 Y34
- VCC 6 U34
- VCC 7 AM33
- VCC 8 AK33
- VCC 9 AJ33
- VCC 10 AG33
- VCC 11 AF33
- VCC 12 T32
- VCC 13 AE33
- VCC 14 AC33
- VCC 15 AB33
- VCC 16 Y33
- VCC 17 U33
- VCC 18 AM28
- VCC 19 AF28
- VCC 20 AJ28
- VCC 21 AG28
- VCC 22 AE28
- VCC 23 AC28
- VCC 24 AB28
- VCC 25 Y28
- VCC 26 U28
- VCC 27 AM25
- VCC 28 AF25
- VCC 29 AJ25
- VCC 30 AG24
- VCC 31 AE24
- VCC 32 AC24
- VCC 33 AB24
- VCC 34 Y24
- VCC 35 T32

VCC CORE  
POWER

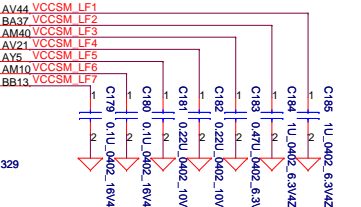
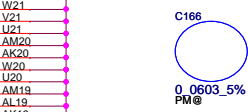
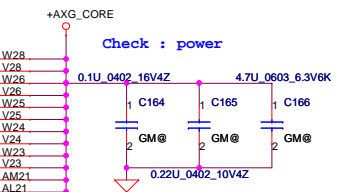
- VCC\_NCTF\_1 AM32
- VCC\_NCTF\_2 AL32
- VCC\_NCTF\_3 AK32
- VCC\_NCTF\_4 AJ32
- VCC\_NCTF\_5 AH32
- VCC\_NCTF\_6 AG32
- VCC\_NCTF\_7 AE32
- VCC\_NCTF\_8 AC32
- VCC\_NCTF\_9 AA32
- VCC\_NCTF\_10 Y32
- VCC\_NCTF\_11 U32
- VCC\_NCTF\_12 AM30
- VCC\_NCTF\_13 AL30
- VCC\_NCTF\_14 AK30
- VCC\_NCTF\_15 AH30
- VCC\_NCTF\_16 AG30
- VCC\_NCTF\_17 AF30
- VCC\_NCTF\_18 AE30
- VCC\_NCTF\_19 AC30
- VCC\_NCTF\_20 AB30
- VCC\_NCTF\_21 Y30
- VCC\_NCTF\_22 U30
- VCC\_NCTF\_23 AM29
- VCC\_NCTF\_24 AL29
- VCC\_NCTF\_25 AK29
- VCC\_NCTF\_26 AH29
- VCC\_NCTF\_27 AG29
- VCC\_NCTF\_28 AF29
- VCC\_NCTF\_29 AE29
- VCC\_NCTF\_30 AC29
- VCC\_NCTF\_31 AB29
- VCC\_NCTF\_32 Y29
- VCC\_NCTF\_33 U29
- VCC\_NCTF\_34 AM28
- VCC\_NCTF\_35 AL28
- VCC\_NCTF\_36 AK28
- VCC\_NCTF\_37 AF28
- VCC\_NCTF\_38 AE28
- VCC\_NCTF\_39 AC28
- VCC\_NCTF\_40 AB28
- VCC\_NCTF\_41 Y28
- VCC\_NCTF\_42 U28
- VCC\_NCTF\_43 AM27
- VCC\_NCTF\_44 AL27

VCC NCTF  
POWER



- VCC\_SM\_1 AP33
- VCC\_SM\_2 AK33
- VCC\_SM\_3 BG32
- VCC\_SM\_4 BF32
- VCC\_SM\_5 BB32
- VCC\_SM\_6 BA32
- VCC\_SM\_7 AW32
- VCC\_SM\_8 AV32
- VCC\_SM\_9 AU32
- VCC\_SM\_10 AR32
- VCC\_SM\_11 BA31
- VCC\_SM\_12 BB31
- VCC\_SM\_13 BF31
- VCC\_SM\_14 BG30
- VCC\_SM\_15 BH29
- VCC\_SM\_16 BF29
- VCC\_SM\_17 BD29
- VCC\_SM\_18 BC29
- VCC\_SM\_19 BA29
- VCC\_SM\_20 AY29
- VCC\_SM\_21 AW29
- VCC\_SM\_22 AU29
- VCC\_SM\_23 AT29
- VCC\_SM\_24 AR29
- VCC\_SM\_25 AP29
- VCC\_SM\_26 BA36
- VCC\_SM\_27 BB24
- VCC\_SM\_28 BD16
- VCC\_SM\_29 BB21
- VCC\_SM\_30 AW18
- VCC\_SM\_31 AW13
- VCC\_SM\_32 AT13
- VCC\_SM\_33 Y26
- VCC\_SM\_34 AE25
- VCC\_SM\_35 AB25
- VCC\_SM\_36 AE25
- VCC\_SM\_37 AC24
- VCC\_SM\_38 AA24
- VCC\_SM\_39 Y24
- VCC\_SM\_40 AE23
- VCC\_SM\_41 AC23
- VCC\_SM\_42 AB23
- VCC\_SM\_43 AA23
- VCC\_SM\_44 AJ21
- VCC\_SM\_45 AE21
- VCC\_SM\_46 AY21
- VCC\_SM\_47 AH20
- VCC\_SM\_48 AF20
- VCC\_SM\_49 AE20
- VCC\_SM\_50 AC20
- VCC\_SM\_51 AB20
- VCC\_SM\_52 AA20
- VCC\_SM\_53 T17
- VCC\_SM\_54 T16
- VCC\_SM\_55 AM15
- VCC\_SM\_56 AL15
- VCC\_SM\_57 AE15
- VCC\_SM\_58 AJ15
- VCC\_SM\_59 AH15
- VCC\_SM\_60 AG15
- VCC\_SM\_61 AF15
- VCC\_SM\_62 AB15
- VCC\_SM\_63 AA15
- VCC\_SM\_64 Y15
- VCC\_SM\_65 U15
- VCC\_SM\_66 U15
- VCC\_SM\_67 U14
- VCC\_SM\_68 T14
- VCC\_SM\_LF1 AV44
- VCC\_SM\_LF2 BA37
- VCC\_SM\_LF3 AM40
- VCC\_SM\_LF4 AV21
- VCC\_SM\_LF5 AY5
- VCC\_SM\_LF6 AM10
- VCC\_SM\_LF7 BB13

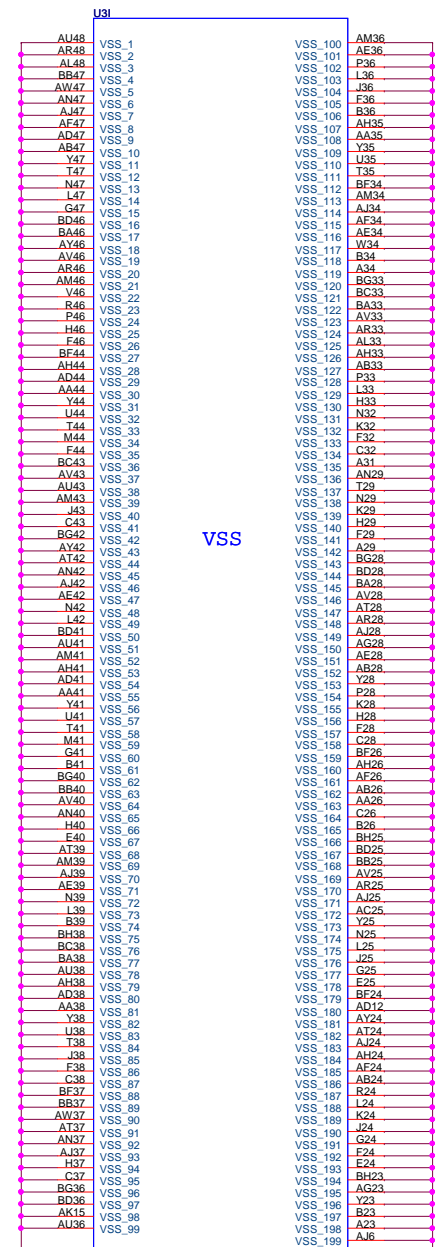
VCC CORE  
POWER  
VCC NCTF  
POWER  
VCC GFX  
POWER  
VCC SM LF  
POWER



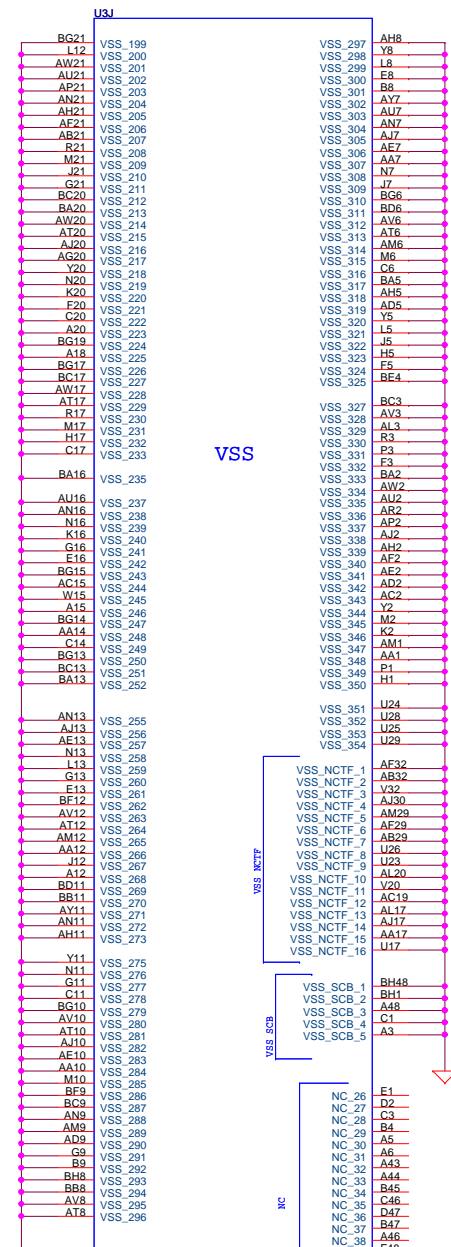
GM45@ CANTIGA ES\_FCBGA1329

GM45@ CANTIGA ES\_FCBGA1329

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Crestline GMCH (5/6)-VCC			1	
Size	Document Number	Rev		
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GM45@ANTIGA ES\_FCBGA1329



GM45@ANTIGA ES\_FCBGA1329

VSS

VSS

VSS\_NCTF

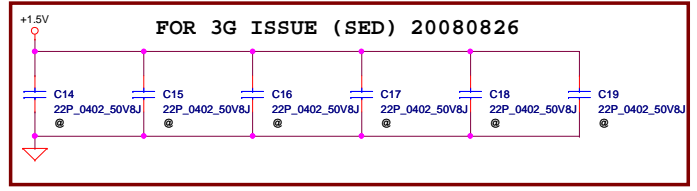
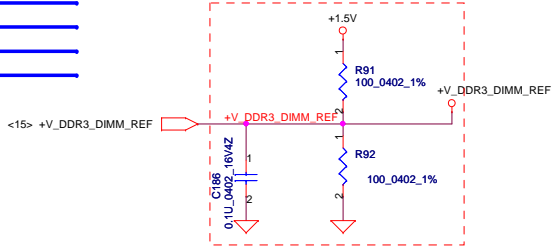
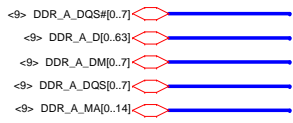
VSS\_SCB

NC

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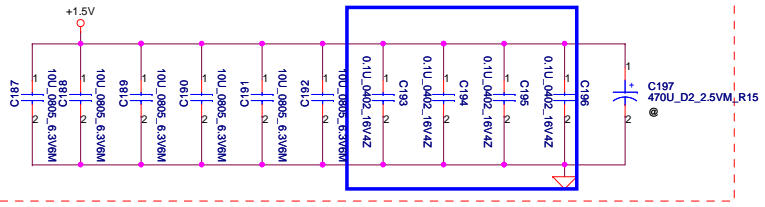
Compal Electronics, Inc.			
Cantiga GMCH (6/6)-GND			
Title			
Size	Document Number	Rev	
Custom	KIWB3/B4_LA451P	0.1	
Date:	Wednesday, March 18, 2009	Sheet	13 of 53



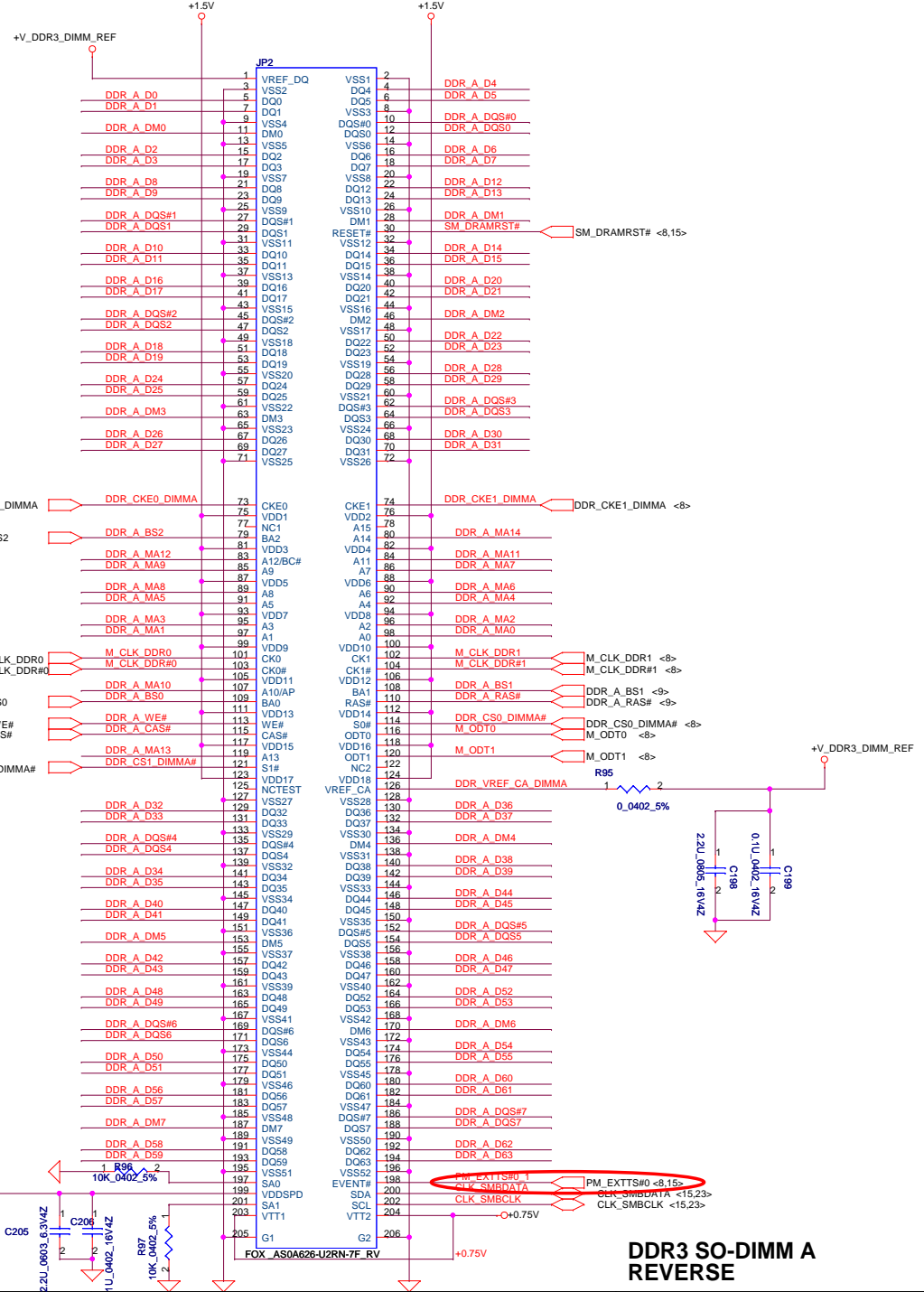
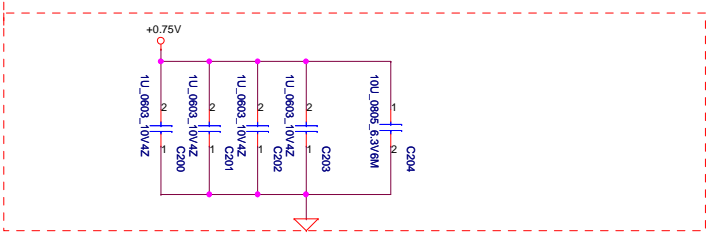


Layout Note:  
Place near JP2

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



Layout Note:  
Place near JP2.203 & JP2.204



### DDR3 SO-DIMM A REVERSE

Security Classification	Compal Secret Data	
Issued Date	2007/09/29	Deciphered Date
		2007/09/29

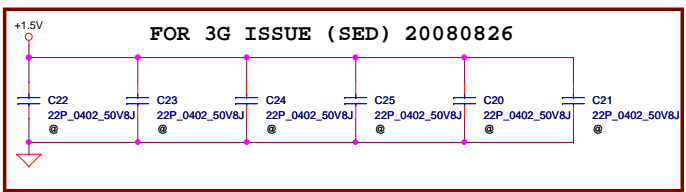
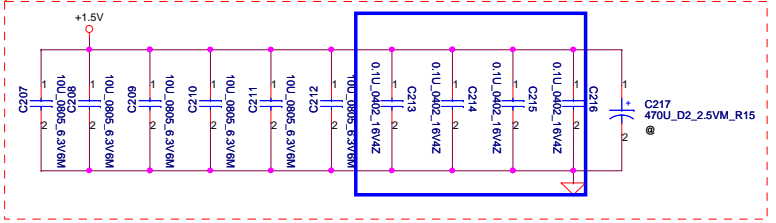
Title		
Compal Electronics, Inc.		
DDRIII-SODIMM SLOT1		
Size	Document Number	Rev
Custor	KIWB1/B2_LA4601P	1.0
Date:	Monday, April 27, 2009	Sheet 14 of 53

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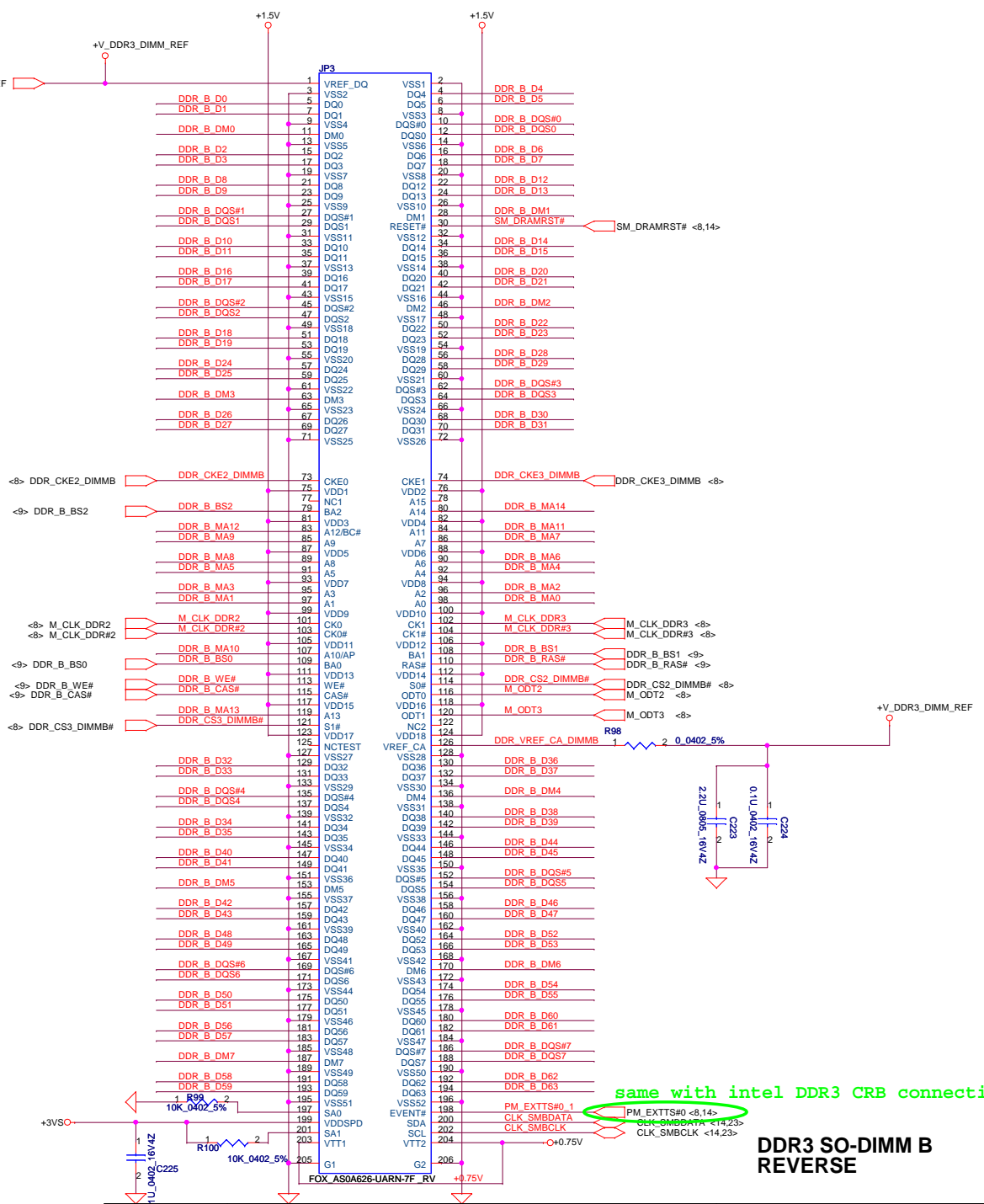
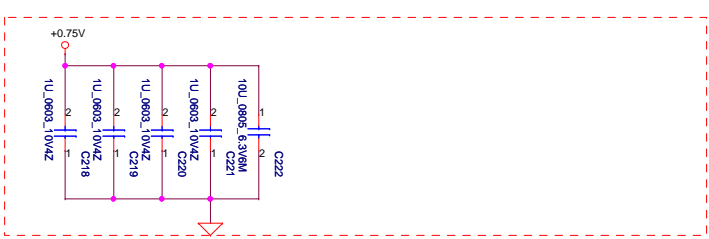
- <9> DDR\_B\_DQS#[0..7]
- <9> DDR\_B\_D[0..63]
- <9> DDR\_B\_DM[0..7]
- <9> DDR\_B\_DQS[0..7]
- <9> DDR\_B\_MA[0..14]

**Layout Note:**  
Place near JP3

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



**Layout Note:**  
Place near JP3.203 & JP3.204



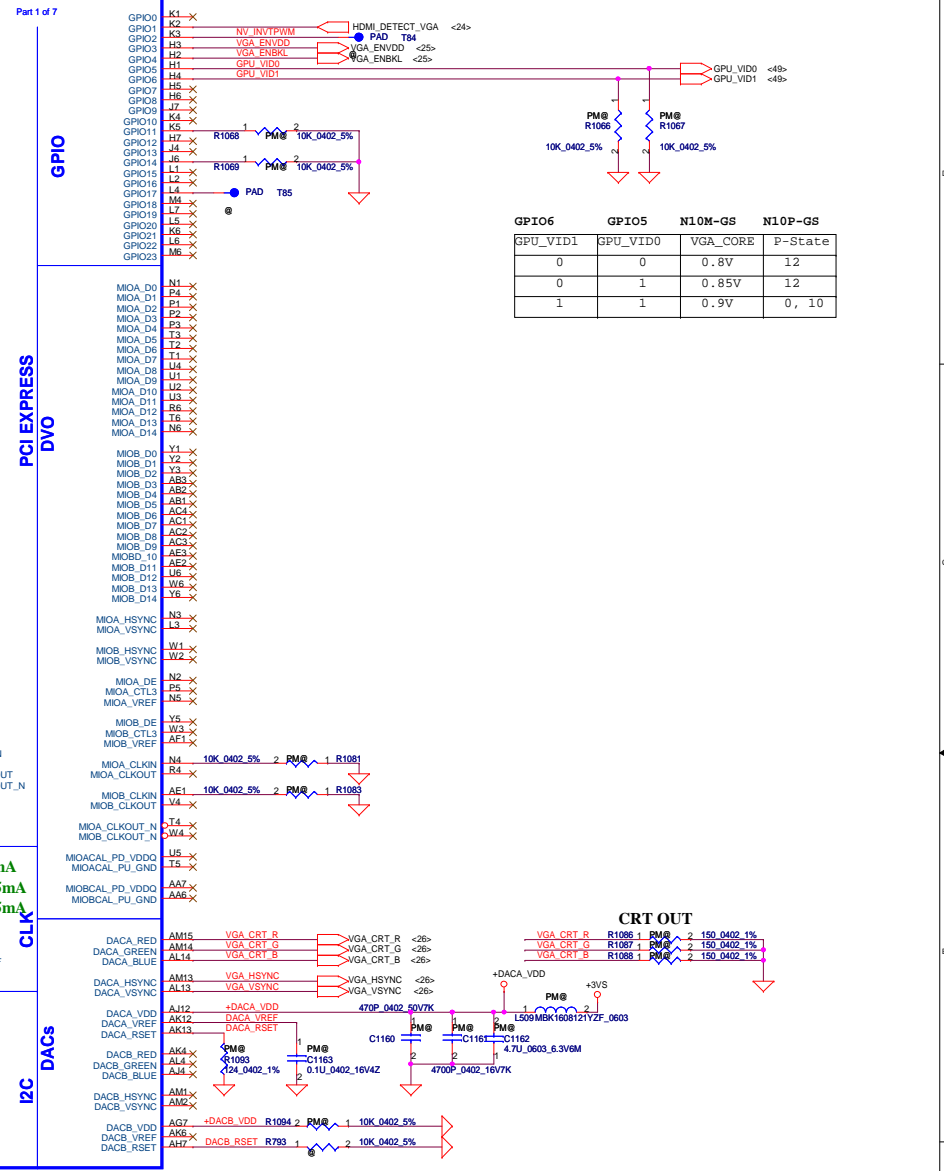
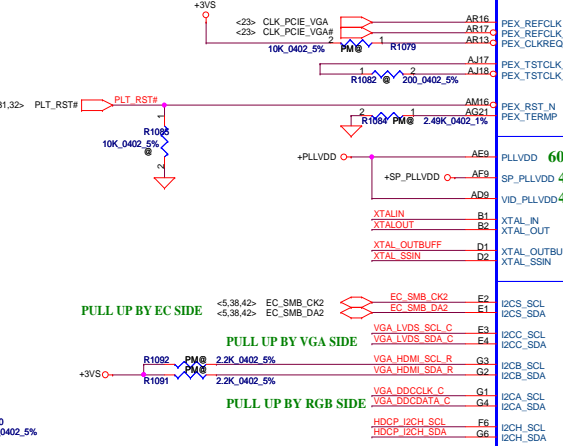
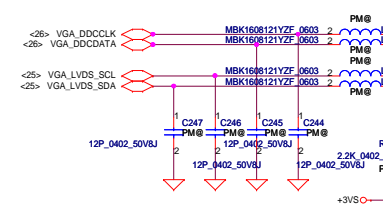
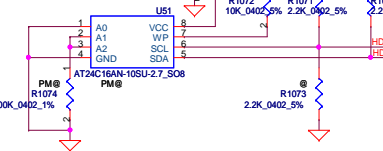
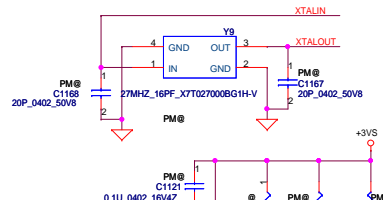
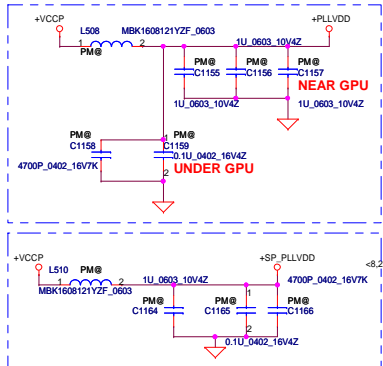
**DDR3 SO-DIMM B  
REVERSE**

Security Classification	Compal Secret Data		Title	
Issued Date	2007/09/29	Deciphered Date	2007/09/29	<b>Compal Electronics, Inc.</b>
				<b>DDRIII-SODIMM SLOT2</b>
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Date: Monday, April 27, 2009				Rev 1.0 1 Sheet 15 of 53

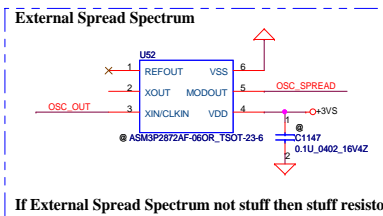


<10> PCIE_MTX_C_GRX_N0_15]	PCIE_MTX_C_GRX_N0_15]	PCIE_MTX_C_GRX_P0	AP17
<10> PCIE_MTX_C_GRX_P0_15]	PCIE_MTX_C_GRX_P0_15]	PCIE_MTX_C_GRX_P1	AN17
<10> PCIE_GTX_C_MRX_N0_15]	PCIE_GTX_C_MRX_N0_15]	PCIE_MTX_C_GRX_N1	AP18
<10> PCIE_GTX_C_MRX_P0_15]	PCIE_GTX_C_MRX_P0_15]	PCIE_MTX_C_GRX_P2	AR18
		PCIE_MTX_C_GRX_N2	AR20
		PCIE_MTX_C_GRX_N3	AN20
		PCIE_MTX_C_GRX_P4	AN22
		PCIE_MTX_C_GRX_N4	AP22
		PCIE_MTX_C_GRX_P5	AR22
		PCIE_MTX_C_GRX_N5	AR23
		PCIE_MTX_C_GRX_P6	AP23
		PCIE_MTX_C_GRX_N6	AN24
		PCIE_MTX_C_GRX_P7	AR24
		PCIE_MTX_C_GRX_N7	AN25
		PCIE_MTX_C_GRX_P8	AR25
		PCIE_MTX_C_GRX_N8	AN26
		PCIE_MTX_C_GRX_P9	AR26
		PCIE_MTX_C_GRX_N9	AN27
		PCIE_MTX_C_GRX_P10	AR27
		PCIE_MTX_C_GRX_N10	AN28
		PCIE_MTX_C_GRX_P11	AR28
		PCIE_MTX_C_GRX_N11	AN29
		PCIE_MTX_C_GRX_P12	AR29
		PCIE_MTX_C_GRX_N12	AN30
		PCIE_MTX_C_GRX_P13	AR30
		PCIE_MTX_C_GRX_N13	AN31
		PCIE_MTX_C_GRX_P14	AR31
		PCIE_MTX_C_GRX_N14	AN32
		PCIE_MTX_C_GRX_P15	AR34
		PCIE_MTX_C_GRX_N15	AP34

PCIE_GTX_C_MRX_P0	C226	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_P0	AL17
PCIE_GTX_C_MRX_N0	C227	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_N0	AM17
PCIE_GTX_C_MRX_P1	C228	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_P1	AM18
PCIE_GTX_C_MRX_N1	C230	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_P2	AM19
PCIE_GTX_C_MRX_P2	C231	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_P2	AL19
PCIE_GTX_C_MRX_N2	C232	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_N2	AK19
PCIE_GTX_C_MRX_P3	C233	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_P3	AL20
PCIE_GTX_C_MRX_N3	C234	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_N3	AM20
PCIE_GTX_C_MRX_P4	C235	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_P4	AM21
PCIE_GTX_C_MRX_N4	C236	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_P4	AM22
PCIE_GTX_C_MRX_P5	C237	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_P5	AL22
PCIE_GTX_C_MRX_N5	C238	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_N5	AK22
PCIE_GTX_C_MRX_P6	C239	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_P6	AL23
PCIE_GTX_C_MRX_N6	C240	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_N6	AK23
PCIE_GTX_C_MRX_P7	C241	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_P7	AM24
PCIE_GTX_C_MRX_N7	C242	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_P7	AM25
PCIE_GTX_C_MRX_P8	C243	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_P8	AL25
PCIE_GTX_C_MRX_N8	C244	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_N8	AK25
PCIE_GTX_C_MRX_P9	C249	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_P9	AL26
PCIE_GTX_C_MRX_N9	C250	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_N9	AM26
PCIE_GTX_C_MRX_P10	C251	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_P10	AM27
PCIE_GTX_C_MRX_N10	C252	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_N10	AM28
PCIE_GTX_C_MRX_P11	C253	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_P11	AL28
PCIE_GTX_C_MRX_N11	C254	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_N11	AK28
PCIE_GTX_C_MRX_P12	C255	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_P12	AK29
PCIE_GTX_C_MRX_N12	C256	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_N12	AL29
PCIE_GTX_C_MRX_P13	C257	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_P13	AM29
PCIE_GTX_C_MRX_N13	C258	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_N13	AM30
PCIE_GTX_C_MRX_P14	C259	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_P14	AM31
PCIE_GTX_C_MRX_N14	C260	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_P14	AM32
PCIE_GTX_C_MRX_P15	C261	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_P15	AN32
PCIE_GTX_C_MRX_N15	C263	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_MRX_N15	AP32

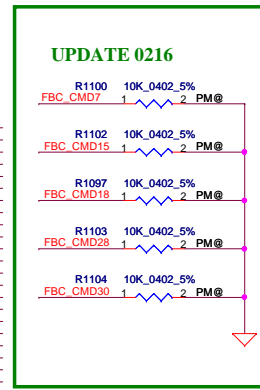
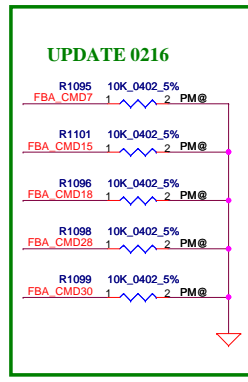
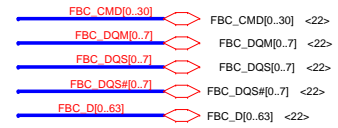
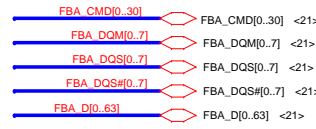


GPIO6	GPIO5	N10M-GS	N10P-GS
GPU_VID1	GPU_VID0	VGA_CORE	P-State
0	0	0.8V	12
0	1	0.85V	12
1	1	0.9V	0, 10



If External Spread Spectrum not stuff then stuff resistor

Security Classification	Compal Secret Data		2008/03/25		Deciphered Date		2008/04/	
Issued Date	2008/03/25		Deciphered Date		2008/04/		Title	
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N10x-GS PCIE, LVDS, GPIO, CLK				N10x-GS PCIE, LVDS, GPIO, CLK		NIWBA LA5371P		Rev 0.1
Date: Wednesday, March 18, 2008				ISheet 16 of 53				



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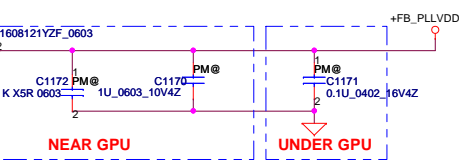
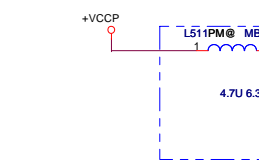
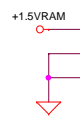
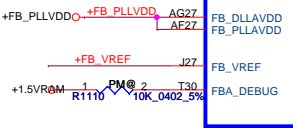
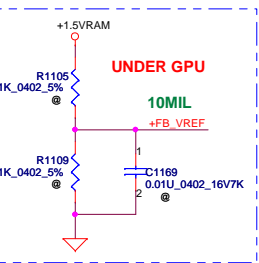
FBA D0	L32	FBA D0	FBA_CMD0	V32	FBA_CMD0
FBA D1	N33	FBA D1	FBA_CMD1	W31	FBA_CMD1
FBA D2	L34	FBA D2	FBA_CMD2	U31	FBA_CMD2
FBA D3	N34	FBA D3	FBA_CMD3	Y32	FBA_CMD3
FBA D4	N35	FBA D4	FBA_CMD4	AB35	FBA_CMD4
FBA D5	P35	FBA D5	FBA_CMD5	AB34	FBA_CMD5
FBA D6	P33	FBA D6	FBA_CMD6	W33	FBA_CMD6
FBA D7	P34	FBA D7	FBA_CMD7	W30	FBA_CMD7
FBA D8	K35	FBA D8	FBA_CMD8	T34	FBA_CMD8
FBA D9	K33	FBA D9	FBA_CMD9	T35	FBA_CMD9
FBA D10	K34	FBA D10	FBA_CMD10	AB31	FBA_CMD10
FBA D11	H33	FBA D11	FBA_CMD11	Y30	FBA_CMD11
FBA D12	G34	FBA D12	FBA_CMD12	Y34	FBA_CMD12
FBA D13	G33	FBA D13	FBA_CMD13	W32	FBA_CMD13
FBA D14	E34	FBA D14	FBA_CMD14	AA30	FBA_CMD14
FBA D15	E33	FBA D15	FBA_CMD15	AA32	FBA_CMD15
FBA D16	G31	FBA D16	FBA_CMD16	U33	FBA_CMD16
FBA D17	F30	FBA D17	FBA_CMD17	U32	FBA_CMD17
FBA D18	G30	FBA D18	FBA_CMD18	U31	FBA_CMD18
FBA D19	G32	FBA D19	FBA_CMD19	W31	FBA_CMD19
FBA D20	K30	FBA D20	FBA_CMD20	Y35	FBA_CMD20
FBA D21	K32	FBA D21	FBA_CMD21	W34	FBA_CMD21
FBA D22	H30	FBA D22	FBA_CMD22	W30	FBA_CMD22
FBA D23	H31	FBA D23	FBA_CMD23	U35	FBA_CMD23
FBA D24	L31	FBA D24	FBA_CMD24	U30	FBA_CMD24
FBA D25	L30	FBA D25	FBA_CMD25	U33	FBA_CMD25
FBA D26	M32	FBA D26	FBA_CMD26	AB30	FBA_CMD26
FBA D27	N30	FBA D27	FBA_CMD27	AB33	FBA_CMD27
FBA D28	M30	FBA D28	FBA_CMD28	T33	FBA_CMD28
FBA D29	P31	FBA D29	FBA_CMD29	W29	FBA_CMD29
FBA D30	R32	FBA D30	FBA_CMD30		
FBA D31	R30	FBA D31			
FBA D32	AG30	FBA D32			
FBA D33	AG32	FBA D33			
FBA D34	AH31	FBA D34			
FBA D35	AE31	FBA D35			
FBA D36	AE32	FBA D36			
FBA D37	AE30	FBA D37			
FBA D38	AC32	FBA D38			
FBA D39	AD30	FBA D39			
FBA D40	AN33	FBA D40			
FBA D41	AL31	FBA D41			
FBA D42	AM33	FBA D42			
FBA D43	AL33	FBA D43			
FBA D44	AK30	FBA D44			
FBA D45	AK32	FBA D45			
FBA D46	AJ30	FBA D46			
FBA D47	AH30	FBA D47			
FBA D48	AH33	FBA D48			
FBA D49	AH35	FBA D49			
FBA D50	AH34	FBA D50			
FBA D51	AH32	FBA D51			
FBA D52	AJ33	FBA D52			
FBA D53	AL35	FBA D53			
FBA D54	AM34	FBA D54			
FBA D55	AM35	FBA D55			
FBA D56	AE33	FBA D56			
FBA D57	AE32	FBA D57			
FBA D58	AF34	FBA D58			
FBA D59	AE35	FBA D59			
FBA D60	AE34	FBA D60			
FBA D61	AE33	FBA D61			
FBA D62	AB32	FBA D62			
FBA D63	AC35	FBA D63			

Part 3 of 7

FBC D0	B13	FBC D0	FBC_CMD0	C17	FBC_CMD0
FBC D1	D13	FBC D1	FBC_CMD1	C19	FBC_CMD1
FBC D2	A13	FBC D2	FBC_CMD2	D18	FBC_CMD2
FBC D3	FBC D3	FBC D3	FBC_CMD3	F21	FBC_CMD3
FBC D4	A14	FBC D4	FBC_CMD4	A23	FBC_CMD4
FBC D5	C16	FBC D5	FBC_CMD5	D21	FBC_CMD5
FBC D6	B15	FBC D6	FBC_CMD6	B23	FBC_CMD6
FBC D7	A17	FBC D7	FBC_CMD7	E20	FBC_CMD7
FBC D8	D16	FBC D8	FBC_CMD8	G21	FBC_CMD8
FBC D9	C13	FBC D9	FBC_CMD9	F19	FBC_CMD9
FBC D10	B11	FBC D10	FBC_CMD10	F18	FBC_CMD10
FBC D11	C11	FBC D11	FBC_CMD11	E23	FBC_CMD11
FBC D12	C10	FBC D12	FBC_CMD12	A22	FBC_CMD12
FBC D13	B8	FBC D13	FBC_CMD13	B17	FBC_CMD13
FBC D14	B8	FBC D14	FBC_CMD14	E24	FBC_CMD14
FBC D15	A8	FBC D15	FBC_CMD15	C25	FBC_CMD15
FBC D16	E8	FBC D16	FBC_CMD16	C20	FBC_CMD16
FBC D17	F8	FBC D17	FBC_CMD17	B22	FBC_CMD17
FBC D18	F10	FBC D18	FBC_CMD18	A19	FBC_CMD18
FBC D19	F9	FBC D19	FBC_CMD19	D22	FBC_CMD19
FBC D20	F12	FBC D20	FBC_CMD20	D20	FBC_CMD20
FBC D21	D8	FBC D21	FBC_CMD21	D22	FBC_CMD21
FBC D22	D16	FBC D22	FBC_CMD22	E19	FBC_CMD22
FBC D23	E11	FBC D23	FBC_CMD23	D19	FBC_CMD23
FBC D24	D12	FBC D24	FBC_CMD24	F18	FBC_CMD24
FBC D25	E13	FBC D25	FBC_CMD25	C19	FBC_CMD25
FBC D26	F14	FBC D26	FBC_CMD26	F22	FBC_CMD26
FBC D27	F14	FBC D27	FBC_CMD27	C23	FBC_CMD27
FBC D28	F15	FBC D28	FBC_CMD28	B20	FBC_CMD28
FBC D29	F16	FBC D29	FBC_CMD29	A20	FBC_CMD29
FBC D30	F16	FBC D30	FBC_CMD30		
FBC D31	F17	FBC D31			
FBC D32	D29	FBC D32			
FBC D33	F27	FBC D33			
FBC D34	E28	FBC D34			
FBC D35	E28	FBC D35			
FBC D36	D28	FBC D36			
FBC D37	F25	FBC D37			
FBC D38	D24	FBC D38			
FBC D39	E26	FBC D39			
FBC D40	E32	FBC D40			
FBC D41	F32	FBC D41			
FBC D42	D33	FBC D42			
FBC D43	E41	FBC D43			
FBC D44	C33	FBC D44			
FBC D45	F29	FBC D45			
FBC D46	D30	FBC D46			
FBC D47	E29	FBC D47			
FBC D48	B29	FBC D48			
FBC D49	C31	FBC D49			
FBC D50	C29	FBC D50			
FBC D51	B31	FBC D51			
FBC D52	C32	FBC D52			
FBC D53	B32	FBC D53			
FBC D54	B35	FBC D54			
FBC D55	B34	FBC D55			
FBC D56	A29	FBC D56			
FBC D57	B28	FBC D57			
FBC D58	A28	FBC D58			
FBC D59	C28	FBC D59			
FBC D60	C26	FBC D60			
FBC D61	D25	FBC D61			
FBC D62	B25	FBC D62			
FBC D63	A25	FBC D63			

MEMORY INTERFACE A

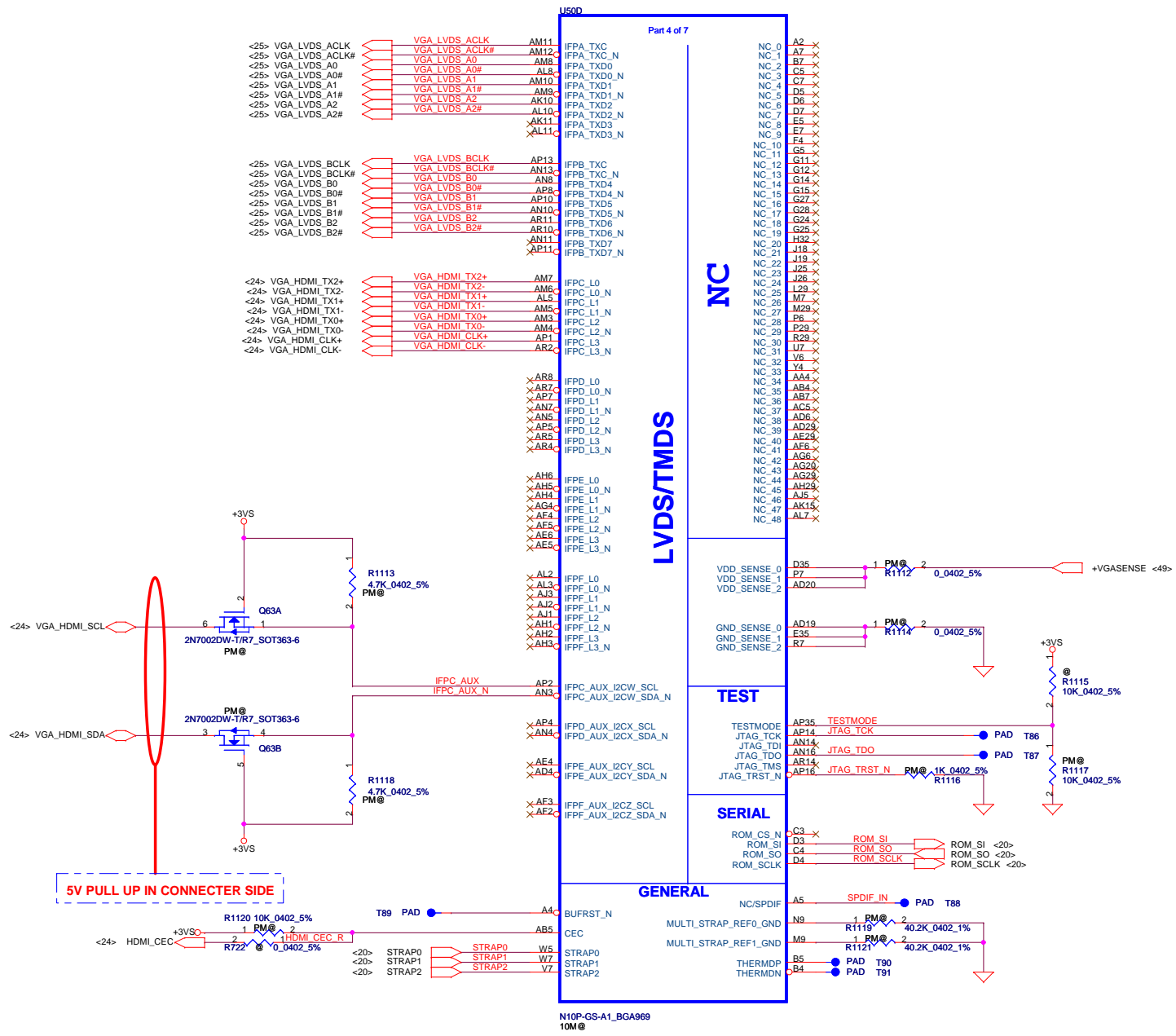
MEMORY INTERFACE C



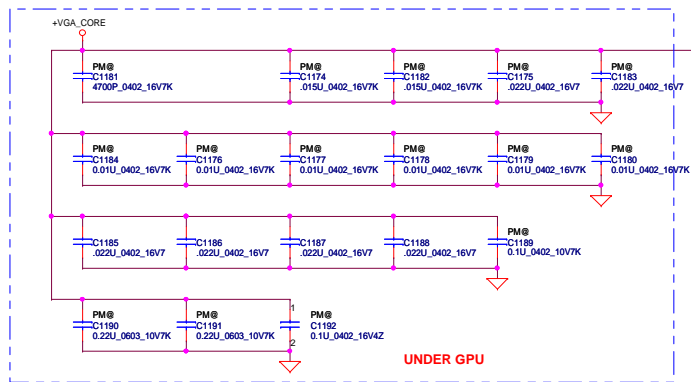
Place Components Close to BGA

Memory/PKG	FBVDDQ	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
DDR3	+1.5VS	40.2 ohm	60.4 ohm	40.2 ohm
GDDR3	+1.8VS	40.2 ohm	60.4 ohm	40.2 ohm

Must be used 1% resistor for driver calibration



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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc.	
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Size	Document Number	Date		Rev	0.1
Custom	N10P/N10M LVDS,HDMI	Wednesday, March 18, 2009		Sheet	18 of 53



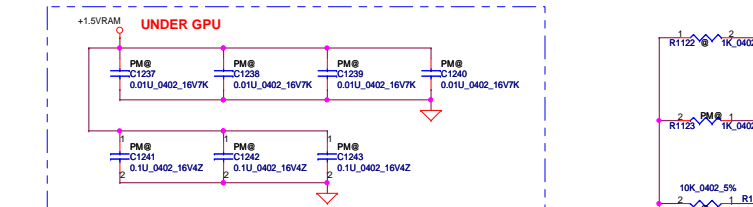
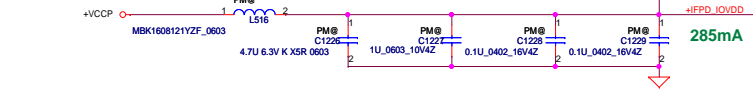
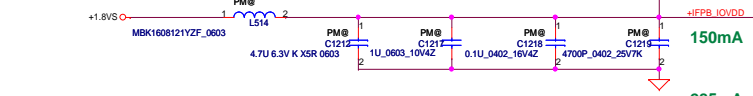
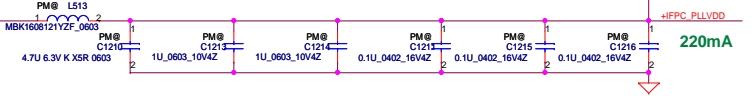
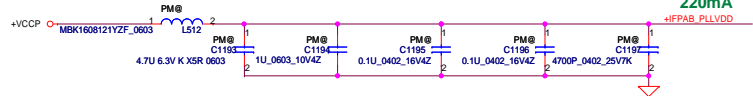
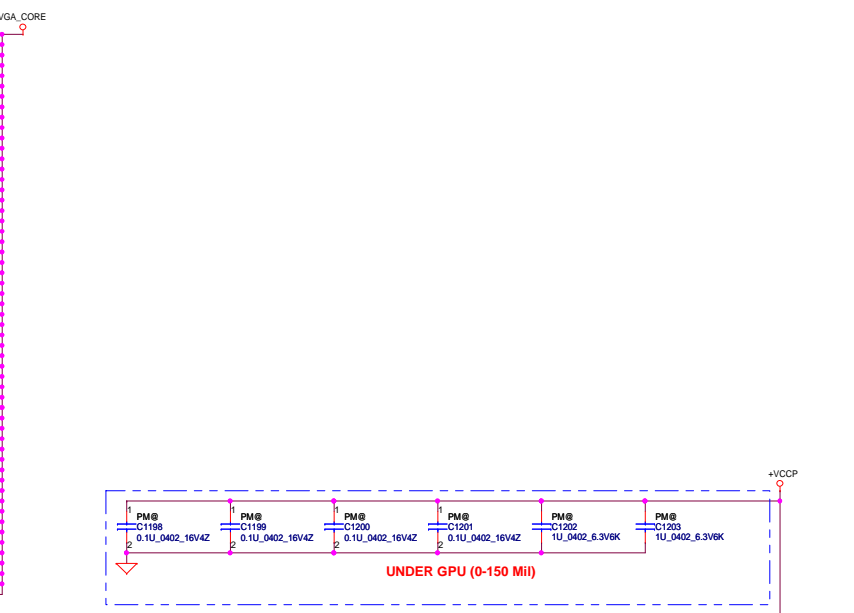
**U50G**

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**22.28A**

**POWER**

AB11	VDD_0	P21	VDD_56
AB13	VDD_1	P23	VDD_57
AB15	VDD_2	P25	VDD_58
AB17	VDD_3	P27	VDD_59
AB19	VDD_4	P29	VDD_60
AB21	VDD_5	P31	VDD_61
AB23	VDD_6	P33	VDD_62
AB25	VDD_7	P35	VDD_63
AC11	VDD_8	P37	VDD_64
AC12	VDD_9	P39	VDD_65
AC14	VDD_10	P41	VDD_66
AC16	VDD_11	P43	VDD_67
AC18	VDD_12	P45	VDD_68
AC20	VDD_13	P47	VDD_69
AC22	VDD_14	P49	VDD_70
AC24	VDD_15	P51	VDD_71
AC26	VDD_16	P53	VDD_72
AC28	VDD_17	P55	VDD_73
AC30	VDD_18	P57	VDD_74
AC32	VDD_19	P59	VDD_75
AC34	VDD_20	P61	VDD_76
AD22	VDD_21	P63	VDD_77
AD24	VDD_22	P65	VDD_78
AD26	VDD_23	P67	VDD_79
AD28	VDD_24	P69	VDD_80
AD30	VDD_25	P71	VDD_81
AD32	VDD_26	P73	VDD_82
AD34	VDD_27	P75	VDD_83
AD36	VDD_28	P77	VDD_84
L11	VDD_29	P79	VDD_85
L13	VDD_30	P81	VDD_86
L15	VDD_31	P83	VDD_87
L17	VDD_32	P85	VDD_88
L19	VDD_33	P87	VDD_89
L21	VDD_34	P89	VDD_90
L23	VDD_35	P91	VDD_91
L25	VDD_36	P93	VDD_92
M14	VDD_37	P95	VDD_93
M16	VDD_38	P97	VDD_94
M18	VDD_39	P99	VDD_95
M20	VDD_40	P101	VDD_96
M22	VDD_41	P103	VDD_97
M24	VDD_42	P105	VDD_98
M26	VDD_43	P107	VDD_99
M28	VDD_44	P109	VDD_100
M30	VDD_45	P111	VDD_101
M32	VDD_46	P113	VDD_102
M34	VDD_47	P115	VDD_103
M36	VDD_48	P117	VDD_104
M38	VDD_49	P119	VDD_105
M40	VDD_50	P121	VDD_106
P11	VDD_51	P123	VDD_107
P13	VDD_52	P125	VDD_108
P15	VDD_53	P127	VDD_109
P17	VDD_54	P129	VDD_110
P19	VDD_55	P131	VDD_111



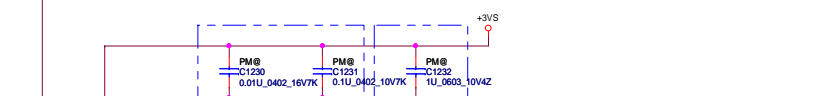
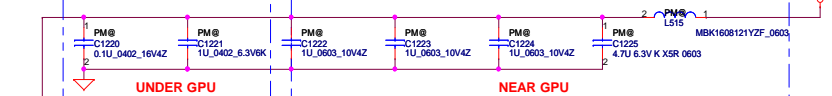
**N10P-GS-A1\_BGA969**

10M@

**POWER**

Part 5 of 7

J23	FBVDDQ_0	AG11	PEX_IOVDDQ_0
J24	FBVDDQ_1	AG12	PEX_IOVDDQ_1
J25	FBVDDQ_2	AG13	PEX_IOVDDQ_2
J26	FBVDDQ_3	AG14	PEX_IOVDDQ_3
AA29	FBVDDQ_4	AG15	PEX_IOVDDQ_4
AA31	FBVDDQ_5	AG16	PEX_IOVDDQ_5
AB27	FBVDDQ_6	AG17	PEX_IOVDDQ_6
AB29	FBVDDQ_7	AG18	PEX_IOVDDQ_7
AC22	FBVDDQ_8	AG19	PEX_IOVDDQ_8
AD27	FBVDDQ_9	AG20	PEX_IOVDDQ_9
AE27	FBVDDQ_10	AG21	PEX_IOVDDQ_10
AG26	FBVDDQ_11	AG22	PEX_IOVDDQ_11
B18	FBVDDQ_12	AG23	PEX_IOVDDQ_12
E21	FBVDDQ_13	AG24	PEX_IOVDDQ_13
G18	FBVDDQ_14	AG25	PEX_IOVDDQ_14
G22	FBVDDQ_15	AG26	PEX_IOVDDQ_15
G8	FBVDDQ_16	AG27	PEX_IOVDDQ_16
G9	FBVDDQ_17	AG28	PEX_IOVDDQ_17
H9	FBVDDQ_18	AG29	PEX_IOVDDQ_18
J14	FBVDDQ_19	AG30	PEX_IOVDDQ_19
J15	FBVDDQ_20	AG31	PEX_IOVDDQ_20
J16	FBVDDQ_21	AG32	PEX_IOVDDQ_21
J17	FBVDDQ_22	AG33	PEX_IOVDDQ_22
J20	FBVDDQ_23	AG34	PEX_IOVDDQ_23
J21	FBVDDQ_24	AG35	PEX_IOVDDQ_24
J22	FBVDDQ_25	AG36	PEX_IOVDDQ_25
J27	FBVDDQ_26	AG37	PEX_IOVDDQ_26
K229	FBVDDQ_27	AG38	PEX_IOVDDQ_27
L27	FBVDDQ_28	AG39	PEX_IOVDDQ_28
L28	FBVDDQ_29	AG40	PEX_IOVDDQ_29
L29	FBVDDQ_30	AG41	PEX_IOVDDQ_30
L30	FBVDDQ_31	AG42	PEX_IOVDDQ_31
L31	FBVDDQ_32	AG43	PEX_IOVDDQ_32
L32	FBVDDQ_33	AG44	PEX_IOVDDQ_33
L33	FBVDDQ_34	AG45	PEX_IOVDDQ_34
L34	FBVDDQ_35	AG46	PEX_IOVDDQ_35
L35	FBVDDQ_36	AG47	PEX_IOVDDQ_36
L36	FBVDDQ_37	AG48	PEX_IOVDDQ_37
L37	FBVDDQ_38	AG49	PEX_IOVDDQ_38



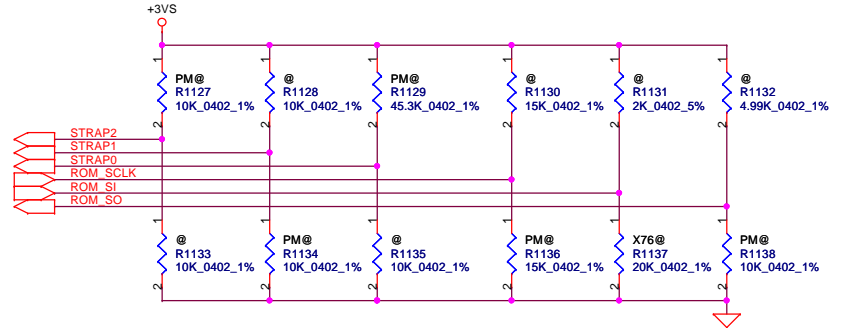
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title
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Size	Document Number	NIWBA_LA5371P		Rev
				0.1
Date:	Wednesday, April 22, 2009	Sheet	19	of
			53	

U50F

Part 6 of 7

B3	GND_0	GND_97	V18
B6	GND_1	GND_98	V20
B9	GND_2	GND_99	V22
B12	GND_3	GND_100	V24
B15	GND_4	GND_101	V31
B21	GND_5	GND_102	V13
B24	GND_6	GND_103	V15
B27	GND_7	GND_104	V17
B30	GND_8	GND_105	V19
B33	GND_9	GND_106	V21
C2	GND_10	GND_107	V23
C34	GND_11	GND_108	V25
E6	GND_12	GND_109	AA2
E9	GND_13	GND_110	AA5
E12	GND_14	GND_111	AA11
E15	GND_15	GND_112	AA12
E18	GND_16	GND_113	AA13
E24	GND_17	GND_114	AA14
E27	GND_18	GND_115	AA15
F30	GND_19	GND_116	AA16
F2	GND_20	GND_117	AA17
F31	GND_21	GND_118	AA18
F34	GND_22	GND_119	AA19
J5	GND_23	GND_120	AA20
J2	GND_24	GND_121	AA21
J31	GND_25	GND_122	AA22
J34	GND_26	GND_123	AA23
K9	GND_27	GND_124	AA24
L9	GND_28	GND_125	AA25
M2	GND_29	GND_126	AA34
M5	GND_30	GND_127	AB12
M11	GND_31	GND_128	AB14
M13	GND_32	GND_129	AB16
M15	GND_33	GND_130	AB18
M17	GND_34	GND_131	AB20
M19	GND_35	GND_132	AB22
M21	GND_36	GND_133	AB24
M23	GND_37	GND_134	AC9
M25	GND_38	GND_135	AD2
M31	GND_39	GND_136	AD5
M34	GND_40	GND_137	AD11
N11	GND_41	GND_138	AD13
N12	GND_42	GND_139	AD15
N13	GND_43	GND_140	AD17
N14	GND_44	GND_141	AD21
N15	GND_45	GND_142	AD23
N16	GND_46	GND_143	AD25
N17	GND_47	GND_144	AD31
N18	GND_48	GND_145	AD34
N19	GND_49	GND_146	AE11
N20	GND_50	GND_147	AE12
N21	GND_51	GND_148	AE13
N22	GND_52	GND_149	AE14
N23	GND_53	GND_150	AE15
N24	GND_54	GND_151	AE16
N25	GND_55	GND_152	AE17
P12	GND_56	GND_153	AE18
P14	GND_57	GND_154	AE19
P16	GND_58	GND_155	AE20
P18	GND_59	GND_156	AE21
P20	GND_60	GND_157	AE22
P22	GND_61	GND_158	AE23
P24	GND_62	GND_159	AE24
R2	GND_63	GND_160	AE25
R5	GND_64	GND_161	AG2
R31	GND_65	GND_162	AG5
R34	GND_66	GND_163	AG31
T11	GND_67	GND_164	AG34
T13	GND_68	GND_165	AK2
T15	GND_69	GND_166	AK5
T17	GND_70	GND_167	AK14
T19	GND_71	GND_168	AK31
T21	GND_72	GND_169	AK34
T23	GND_73	GND_170	AL6
T25	GND_74	GND_171	AL9
U11	GND_75	GND_172	AL12
U12	GND_76	GND_173	AL15
U13	GND_77	GND_174	AL18
U14	GND_78	GND_175	AL21
U15	GND_79	GND_176	AL24
U16	GND_80	GND_177	AL27
U17	GND_81	GND_178	AL30
U18	GND_82	GND_179	AN2
U19	GND_83	GND_180	AN34
U20	GND_84	GND_181	AP3
U21	GND_85	GND_182	AP6
U22	GND_86	GND_183	AP9
U23	GND_87	GND_184	AP12
U24	GND_88	GND_185	AP15
U25	GND_89	GND_186	AP18
V2	GND_90	GND_187	AP21
V5	GND_91	GND_188	AP24
V9	GND_92	GND_189	AP27
V12	GND_93	GND_190	AP30
V14	GND_94	GND_191	AP33
V16	GND_95	GND_192	
	GND_96		

GND



<18> STRAP2  
<18> STRAP1  
<18> STRAP0  
<18> ROM\_SCLK  
<18> ROM\_SI  
<18> ROM\_SO

X2  
S1024@  
X76\_S1024

X3  
H1024@  
X76\_H1024

X4  
S512@  
X76\_S512

X5  
H512@  
X76\_H512

U50  
N10P-GS  
10P@

GB1 Family GPU Strap Options

GPU DEVID    RAM\_CFG    GPU DEVID

GPU	FB Memory	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N10P-GS (0xA34)	Samsung	64Mx16	PD 10K	PD 15K	PD 20K	PU 10K	PD 10K    PU 45K
	Hynix	64Mx16	PD 10K	PD 15K	PD 15K	PU 10K	PD 10K    PU 45K

GPU	FB Memory	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N10M-GS (0xA74)	Samsung	64Mx16	PD 10K	PD 15K	PD 20K	PU 10K	PD 10K    PU 45K
	Hynix	64Mx16	PD 10K	PD 15K	PD 15K	PU 10K	PD 10K    PU 45K

N10P-GS-A1\_BGA969  
10M@

Security Classification		Compal Secret Data		<b>Compal Electronics, Ltd.</b> <b>N10x-GS GND &amp; STRAP</b>	
Issued Date	2008/03/25	Deciphered Date	2008/04/		
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Date: Wednesday, March 18, 2009				Sheet	20 of 53

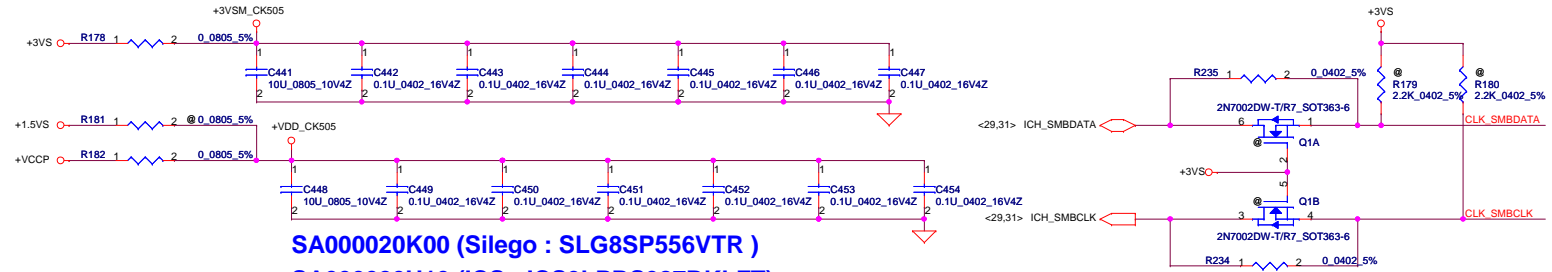




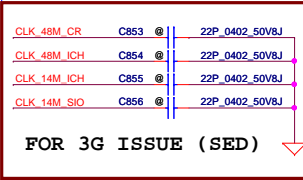
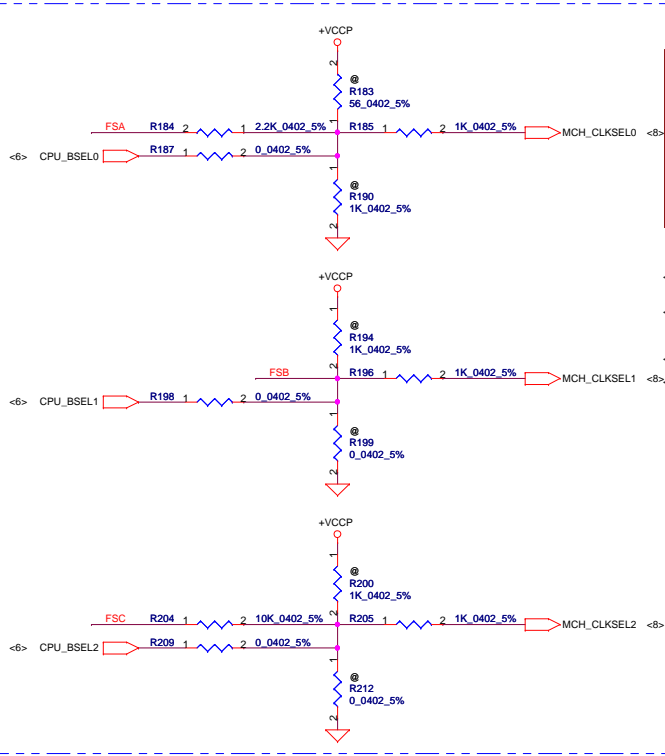


FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHZ	MHZ	MHZ	MHZ	MHZ	MHZ
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						

Reserved

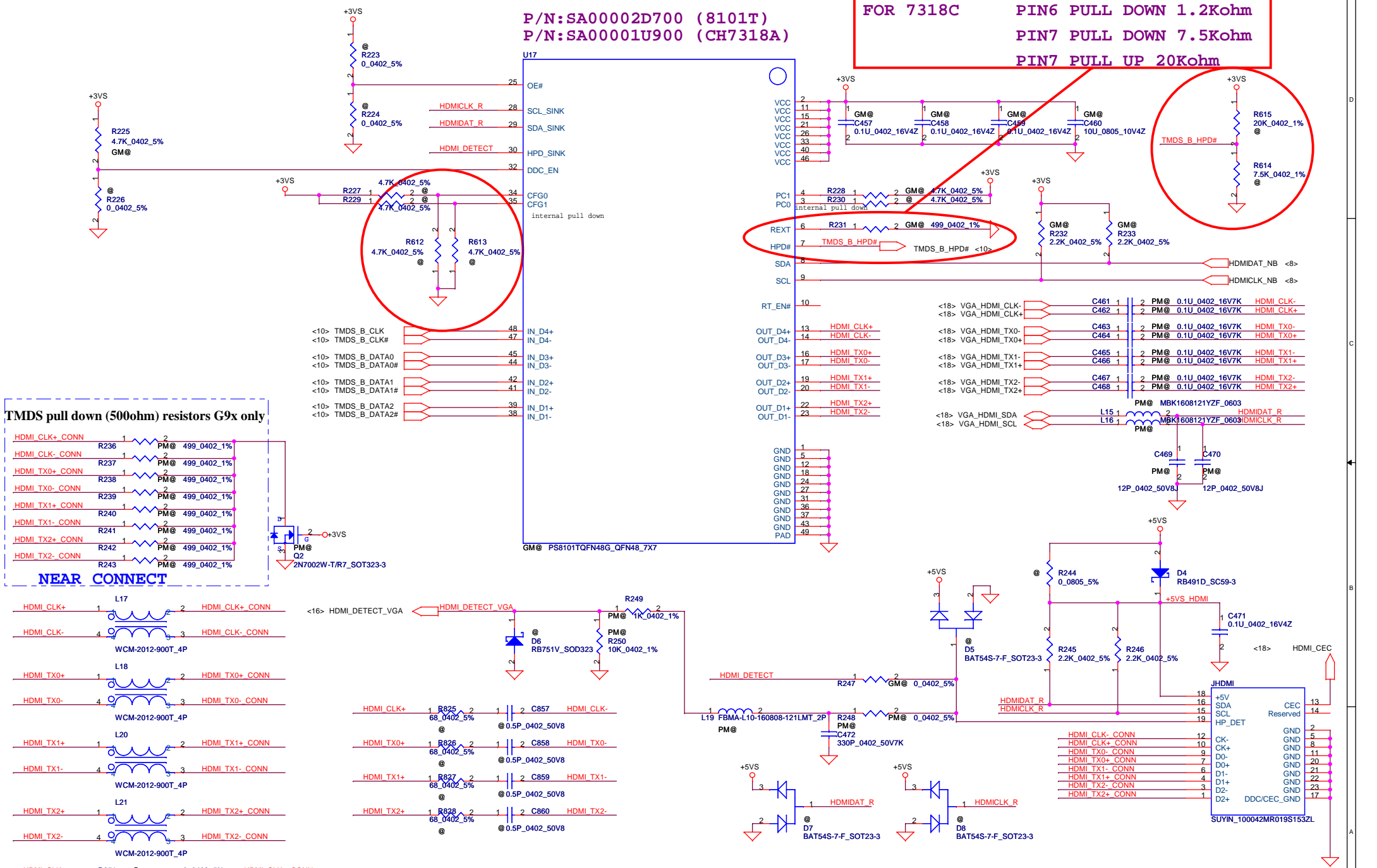


**SA000020K00 (Silego : SLG8SP556VTR )**  
**SA000020H10 (ICS : ICS9LPRS387BKLFT)**



P/N:SA00002D700 (8101T)  
P/N:SA00001U900 (CH7318A)

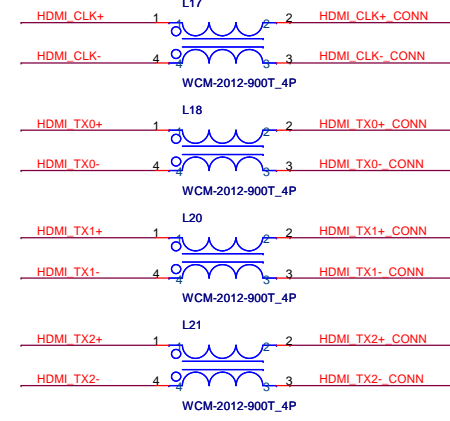
**FOR 7318C**  
PIN6 PULL DOWN 1.2Kohm  
PIN7 PULL DOWN 7.5Kohm  
PIN7 PULL UP 20Kohm



**TMSD pull down (500ohm) resistors G9x only**

HDMI CLK+ CONN	R236	1	2	PM@ 499_0402_1%
HDMI CLK- CONN	R237	1	2	PM@ 499_0402_1%
HDMI TX0+ CONN	R238	1	2	PM@ 499_0402_1%
HDMI TX0- CONN	R239	1	2	PM@ 499_0402_1%
HDMI TX1+ CONN	R240	1	2	PM@ 499_0402_1%
HDMI TX1- CONN	R241	1	2	PM@ 499_0402_1%
HDMI TX2+ CONN	R242	1	2	PM@ 499_0402_1%
HDMI TX2- CONN	R243	1	2	PM@ 499_0402_1%

**NEAR CONNECT**



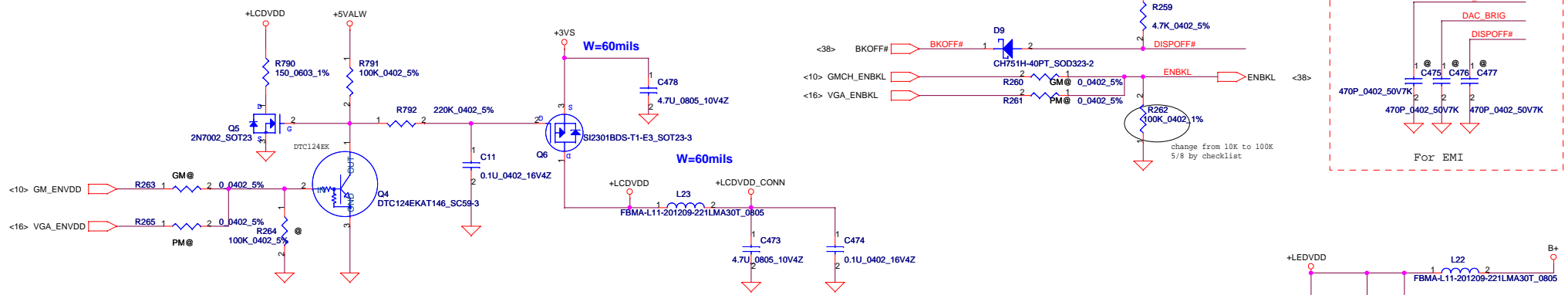
HDMI CLK+	R251	1	2	0.0402 5%	HDMI CLK+ CONN
HDMI CLK-	R252	1	2	0.0402 5%	HDMI CLK- CONN
HDMI TX0+	R253	1	2	0.0402 5%	HDMI TX0+ CONN
HDMI TX0-	R254	1	2	0.0402 5%	HDMI TX0- CONN
HDMI TX1+	R255	1	2	0.0402 5%	HDMI TX1+ CONN
HDMI TX1-	R256	1	2	0.0402 5%	HDMI TX1- CONN
HDMI TX2+	R257	1	2	0.0402 5%	HDMI TX2+ CONN
HDMI TX2-	R258	1	2	0.0402 5%	HDMI TX2- CONN

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Issued Date	2008/03/25	Deciphered Date	2008/04/

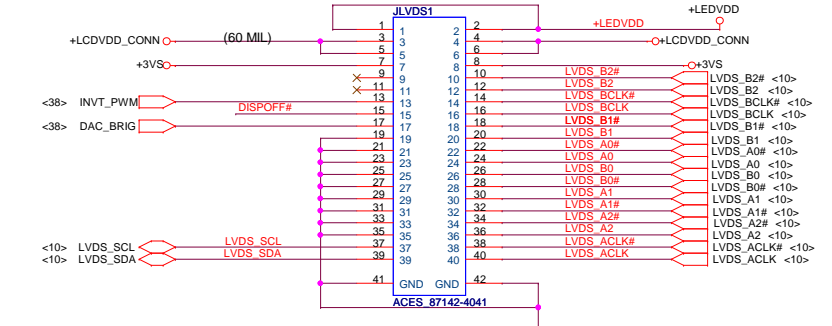
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<b>Compal Electronics, Ltd.</b> <b>Level Shifter PS8101T</b>		Title	Level Shifter PS8101T
		Size	Document Number
Customer	<b>KIWBI/B2_LA4601P</b>	Rev	0.1
Date	Wednesday, March 18, 2009	Sheet	24 of 53

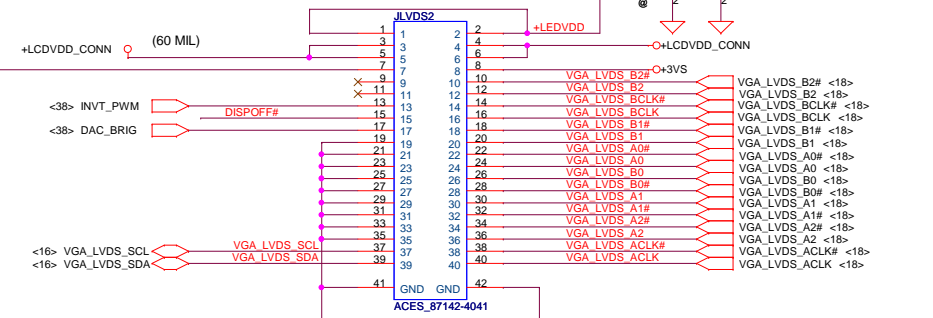
# LCD POWER CIRCUIT



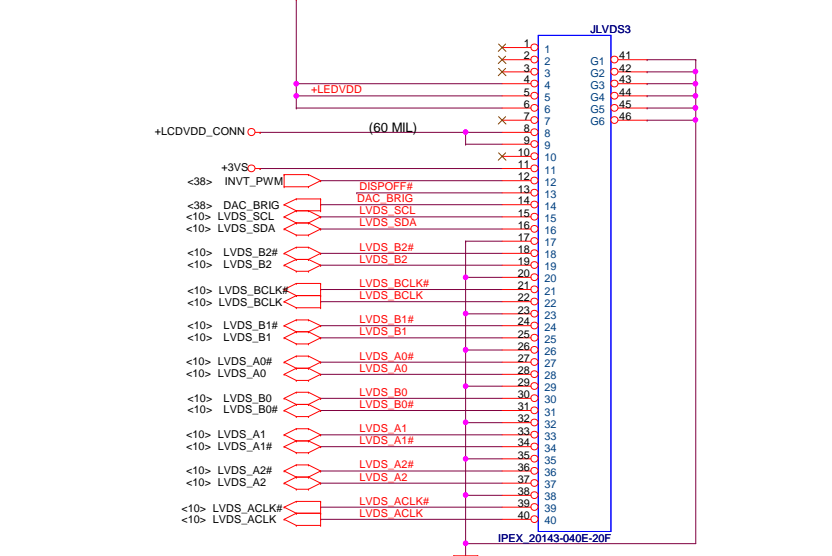
# UMA LCD/PANEL BD. Conn.



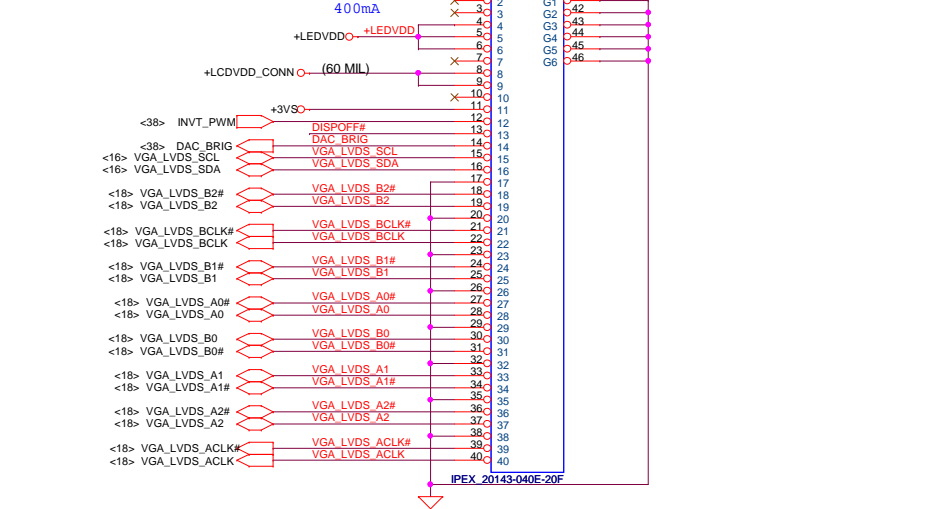
# VGA LCD/PANEL BD. Conn.



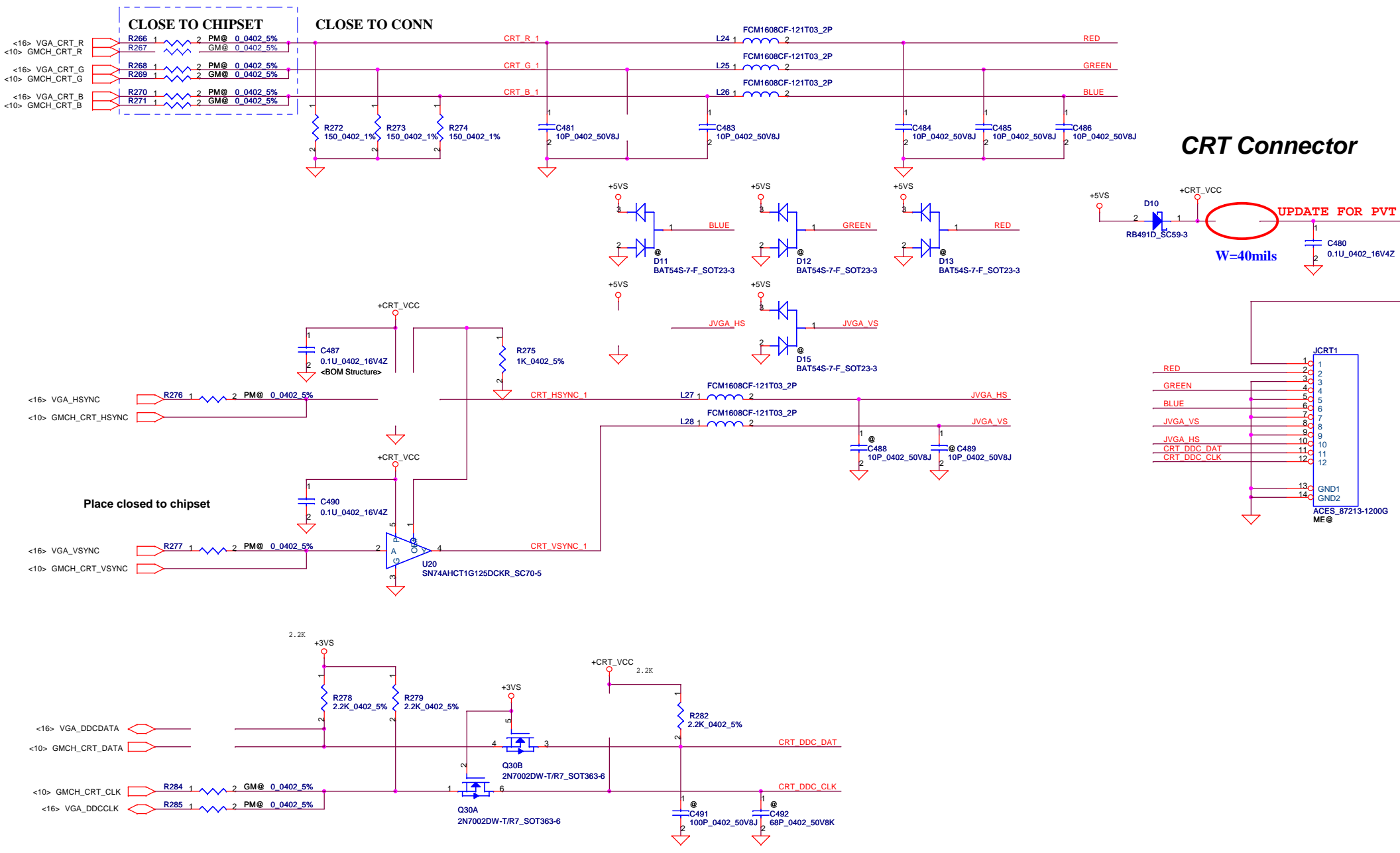
# JLVDS3



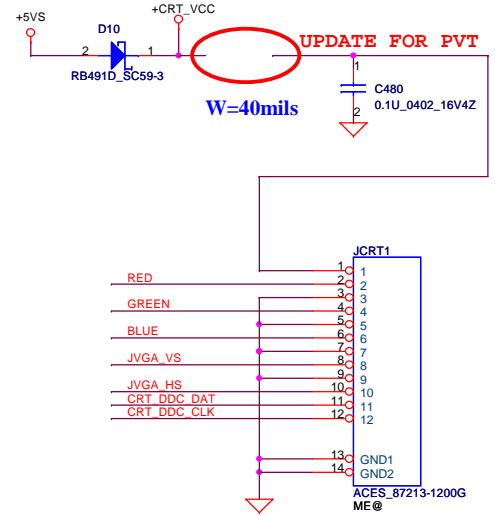
# JLVDS4



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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Size B	
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				KIWB1/B2_LA4601P	
				Rev 0.1	
				Date: Wednesday, March 18, 2009   Sheet 25 of 53	

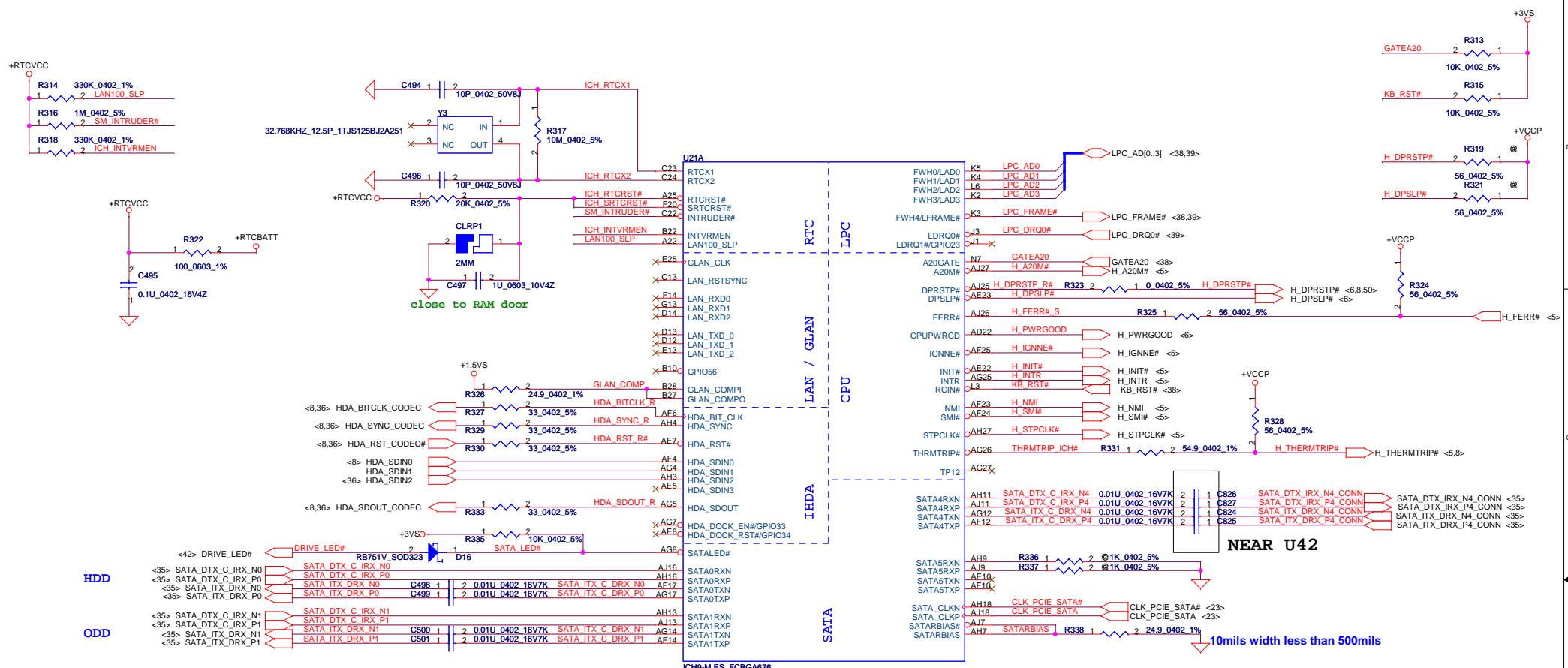


### CRT Connector

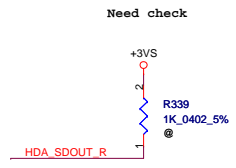


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Issued Date	2007/10/15	Deciphered Date	2008/10/15	<b>Compal Electronics, Inc.</b> <b>R267 CRT Connector</b>	
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				Custom	0.1
				Date:	Wednesday, March 18, 2009
				Sheet	26 of 53



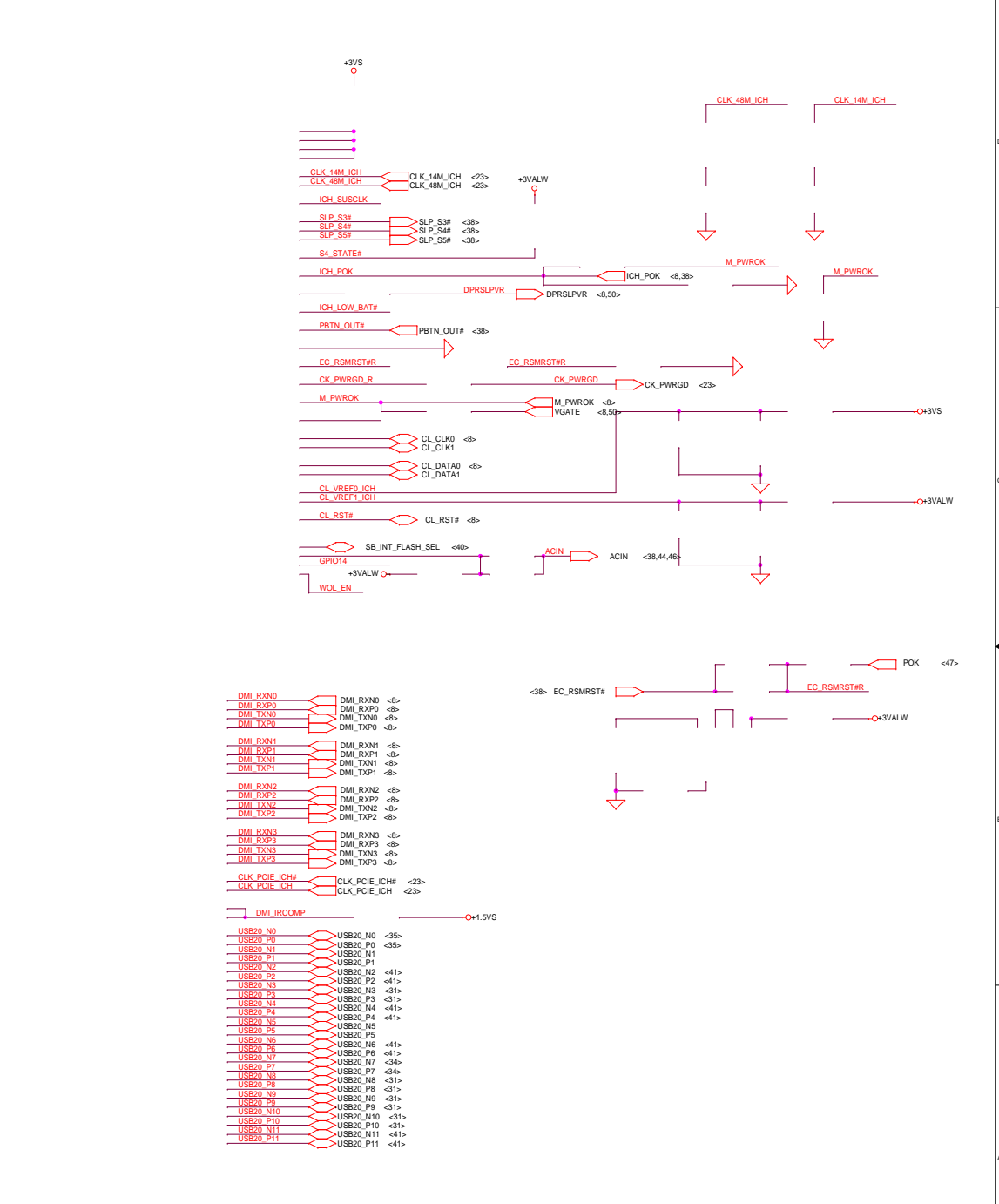
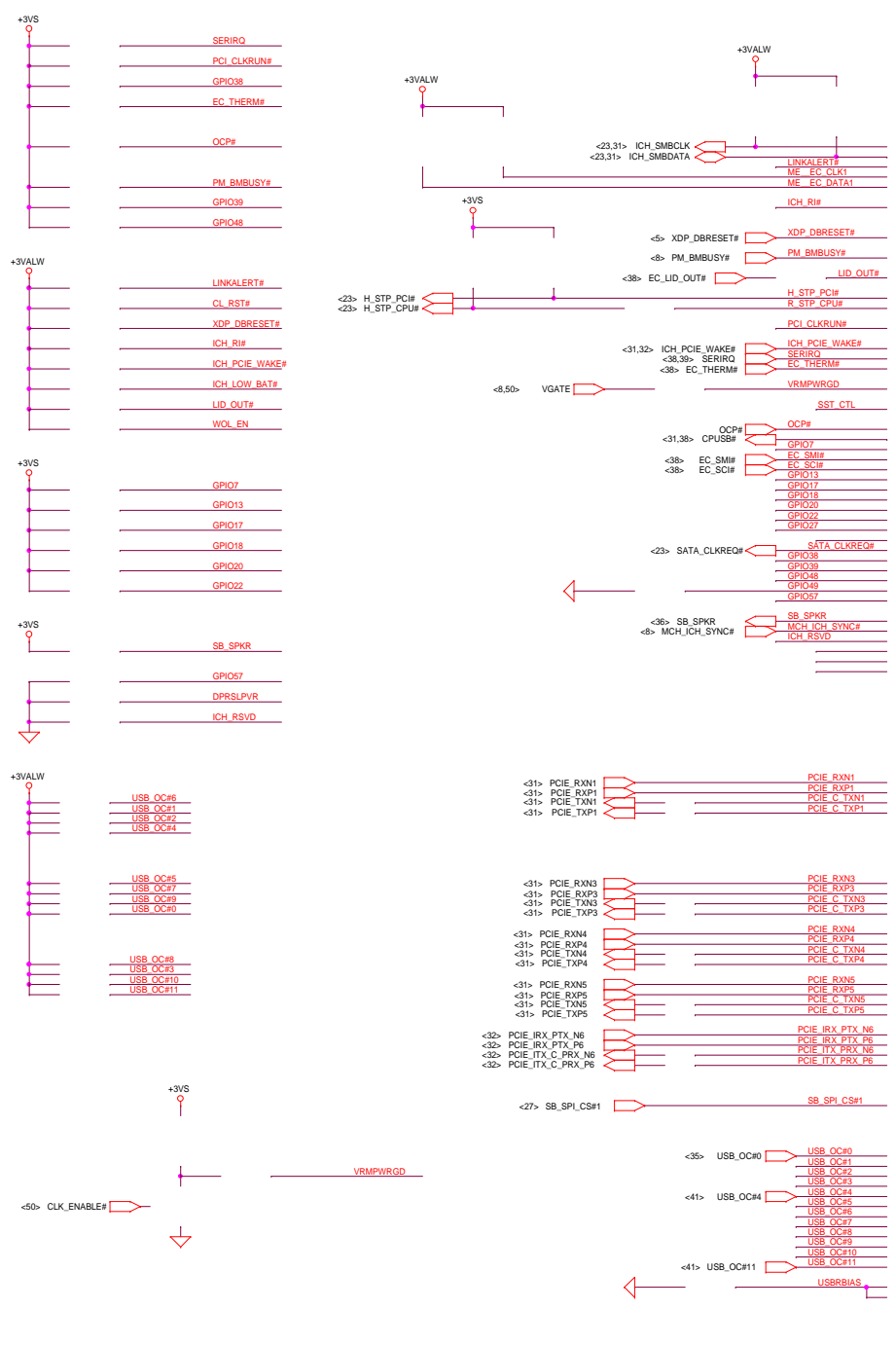


HDD  
ODD



XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

SATA PORT LIST	
PORT	DEVICE
0	HDD
1	ODD
2	X
3	X
4	ESATA
5	X

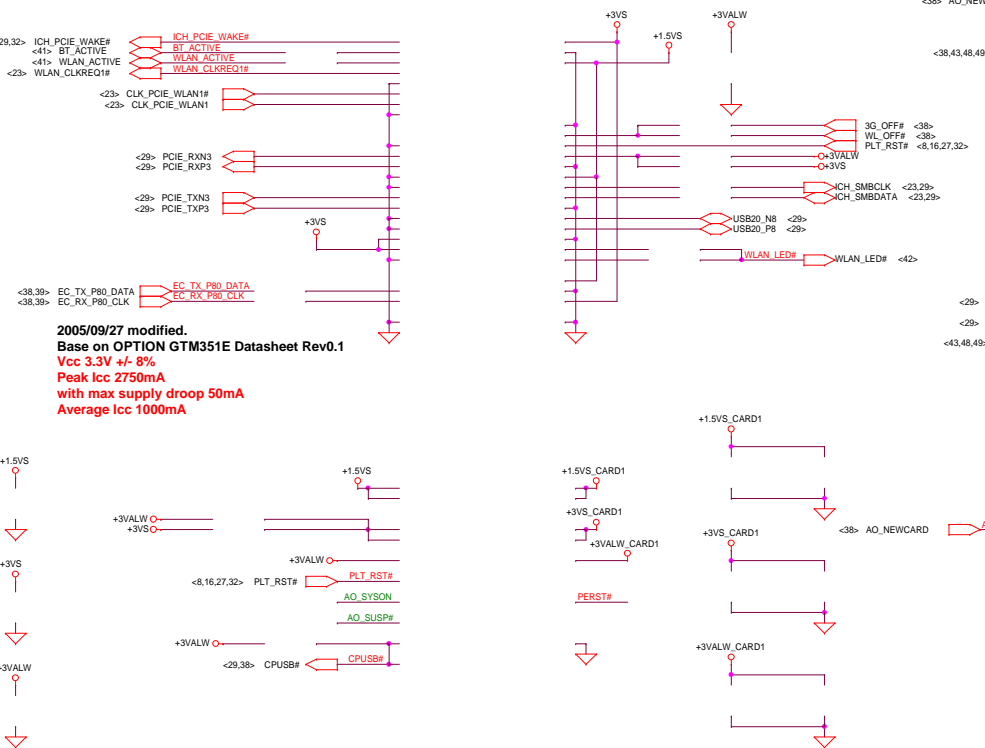
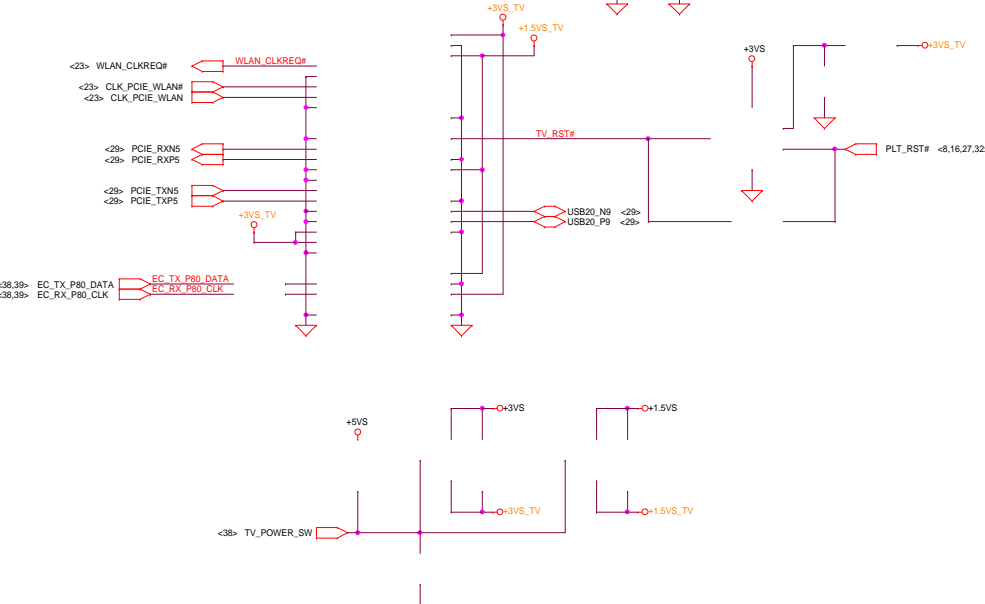






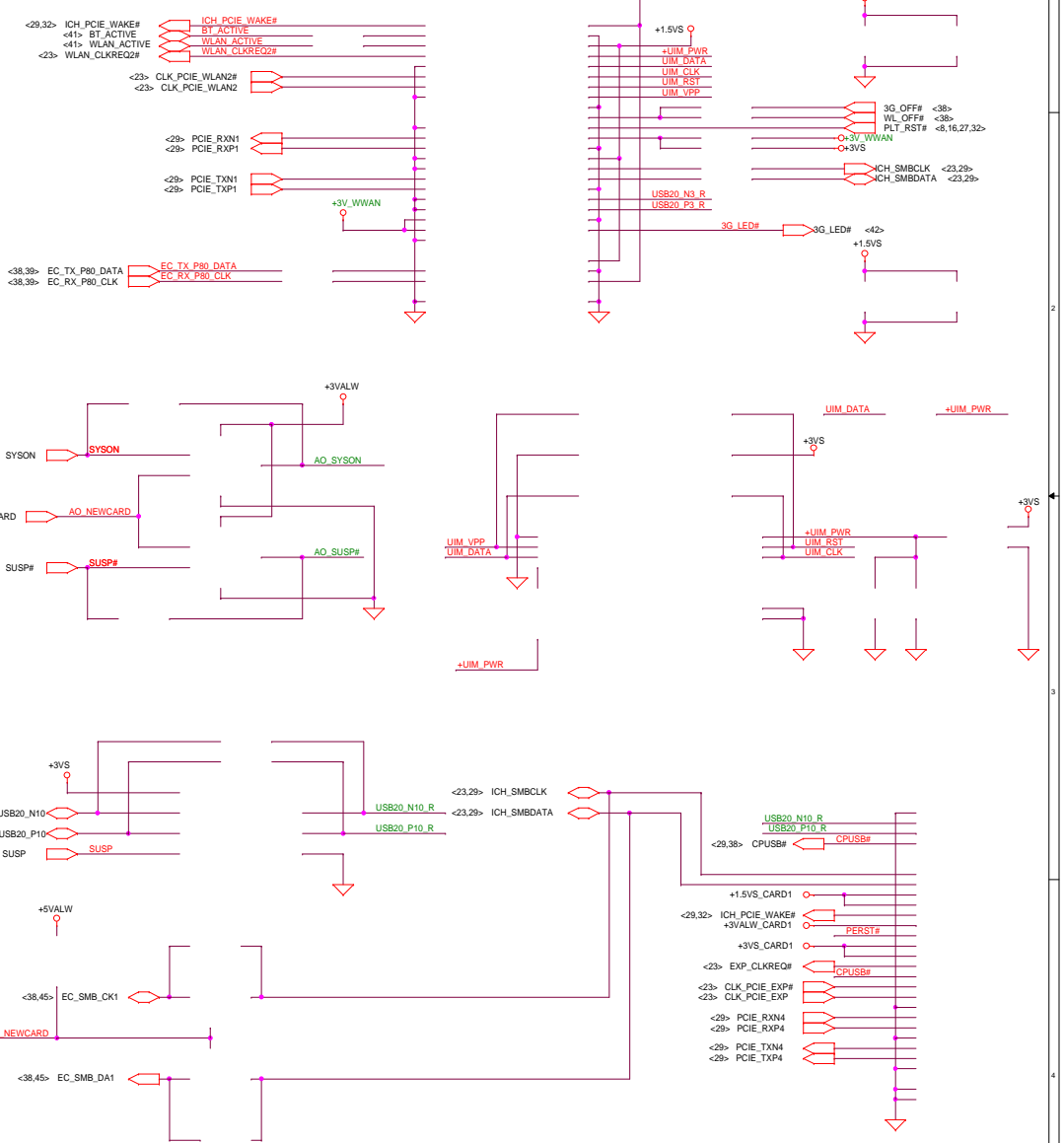
# Mini-Express Card for 3G Or TV Tuner

## Mini-Express Card(Slot 1-TV TUNNER) 4.0mm high

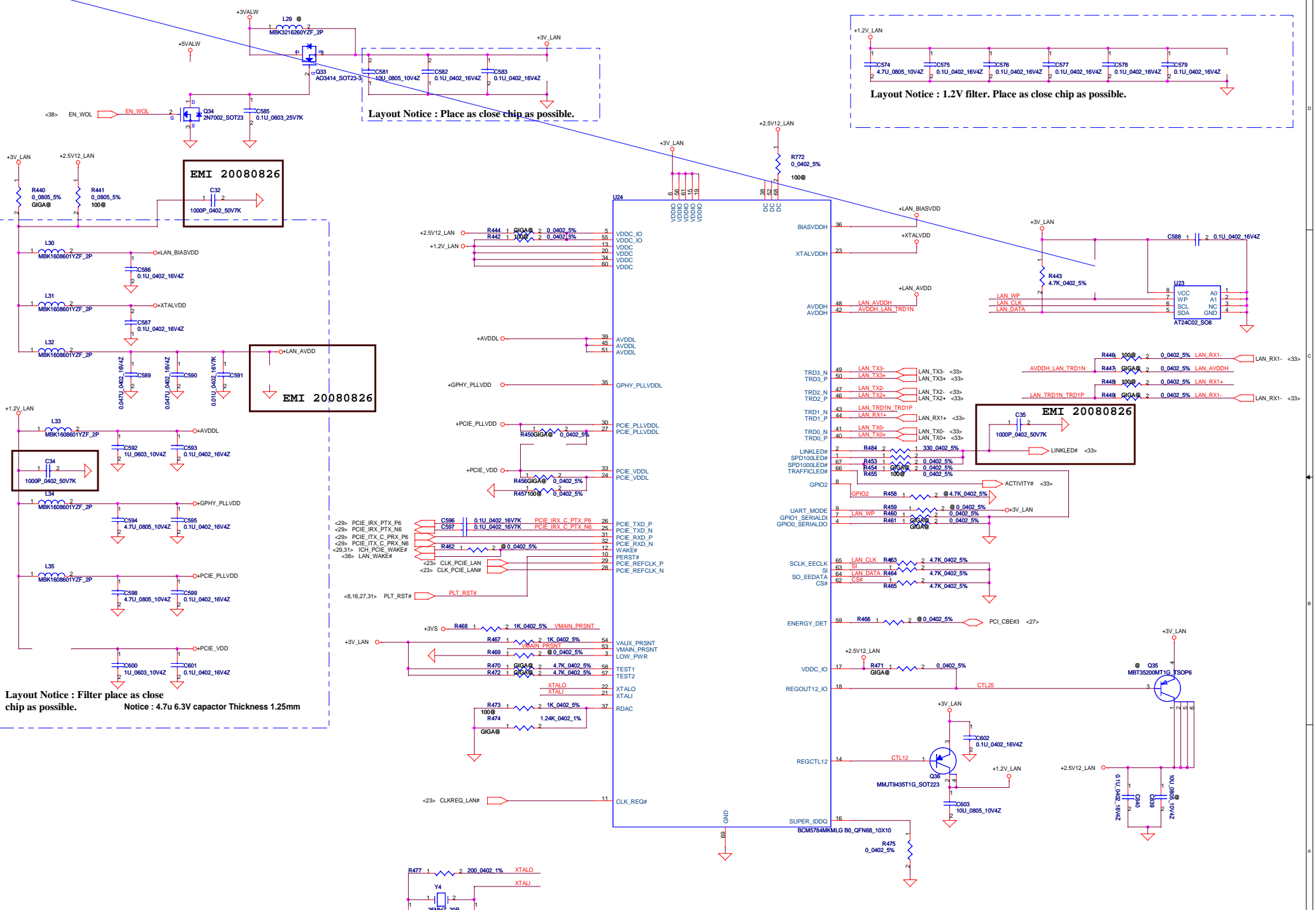


2005/09/27 modified.  
 Base on OPTION GTM351E Datasheet Rev0.1  
 Vcc 3.3V +/- 8%  
 Peak Icc 2750mA  
 with max supply droop 50mA  
 Average Icc 1000mA

## Mini-Exp3(e)8.680405 -62.16S.d[163569]E35363924S050.372AIR(S)6682385(13-889BT/R2.9177)(E)962358A15K59GT(R)N3.2453



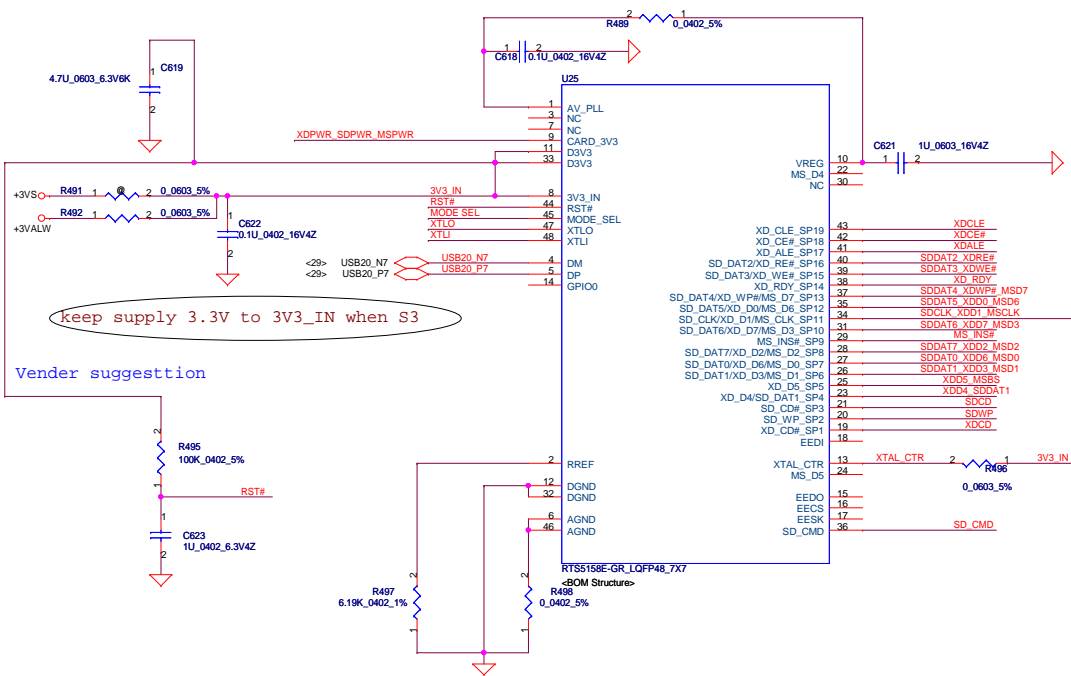
Security Classification	Compal Secret Data		Title	
Id/Rev/Date	2007/10/15	Deciphered Date	2008/10/15	Mini-Card/3G/FeliCa/BT
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	JITR1_LA-4141P	Wednesday, March 18, 2009		0.1
		ISheet	31	of 53



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Issued Date	2008/03/25	Deciphered Date	2008/04/	Broadcom LAN BCM5784M/5906M	
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Size	Document Number	KIWB1/B2_LA4601P		Rev	0.1
Date: Wednesday, March 18, 2009	Sheet	32	of	53	

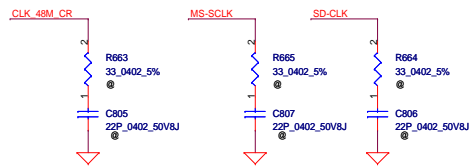
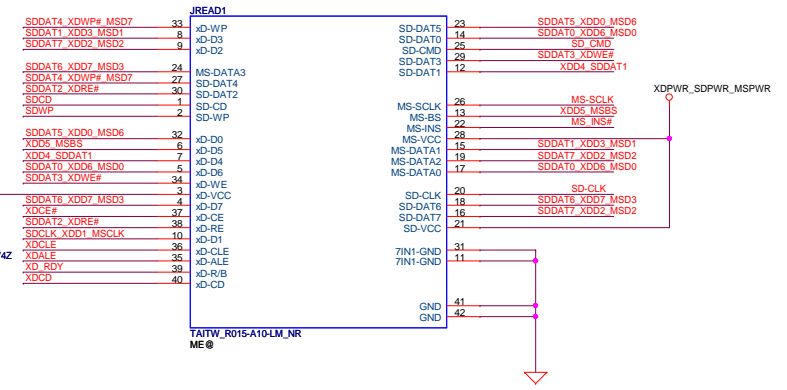


0513 : CARD\_3V3 旁路電阻 100K change to 4.7u CAP=>預留  
 0521 : change C79 form 4.7u to 0.1u, add R47 100K ohm,  
 change C526 form 1u to 4.7u



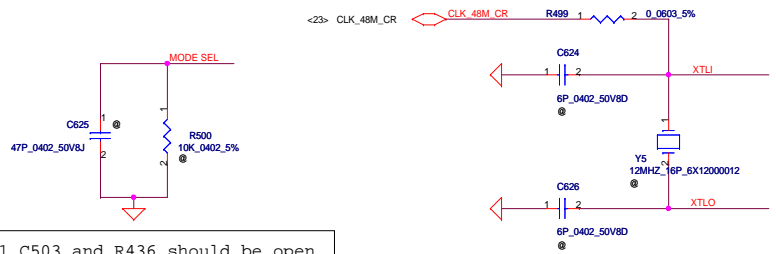
keep supply 3.3V to 3V3\_IN when S3

Vender suggesttion



MSCLK and SDCLK 該二電阻是預留給EMI solution使用, (但請靠近RTS5158E側).

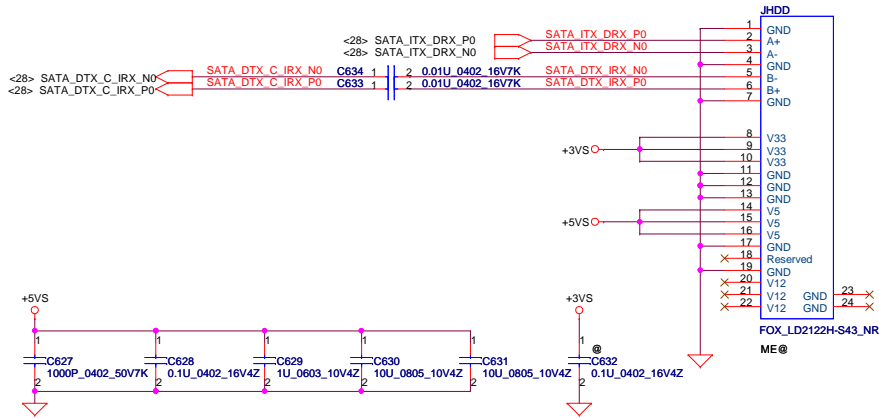
將SD\_DAT1 連接到RTS5158B的pin23



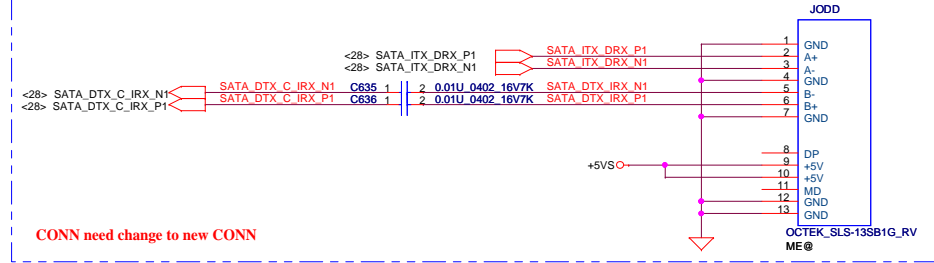
0521\_C503 and R436 should be open

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Issued Date	2006/08/04	Deciphered Date	2006/10/06	1394+3 in 1 Card
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### SATA HDD Conn.

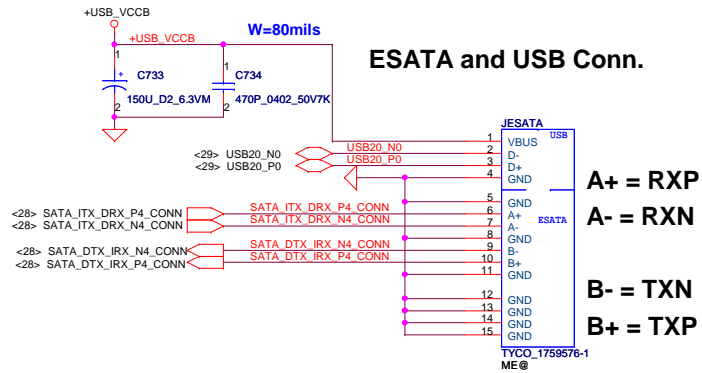


### SATA ODD Conn.

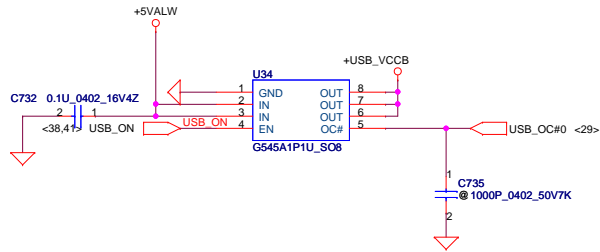


CONN need change to new CONN

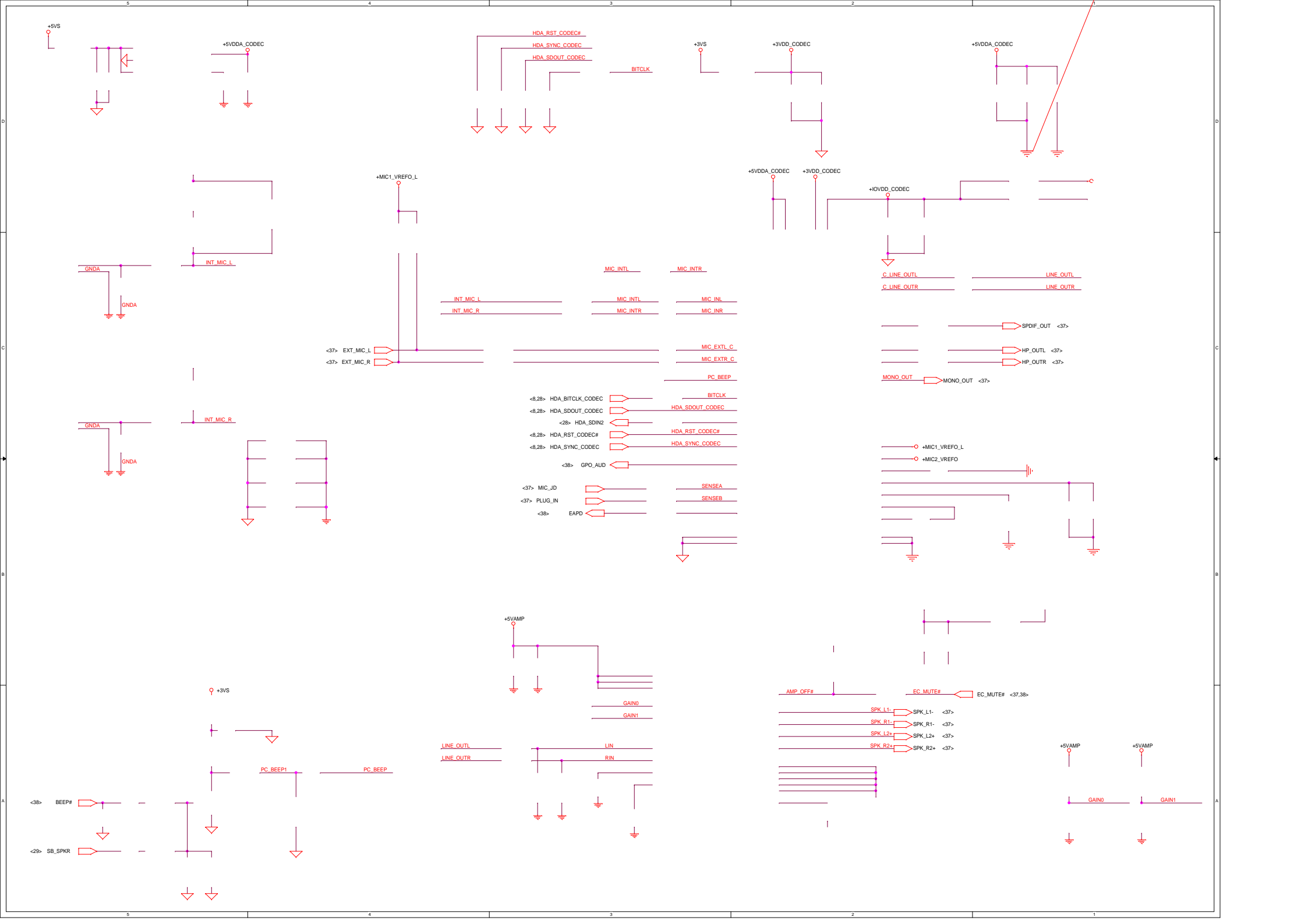
### ESATA and USB Conn.



A+ = RXP  
A- = RXN  
B- = TXN  
B+ = TXP



Security Classification	Compal Secret Data			Title		
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc.		
				HDD & ODD Connector		
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				Date:	Wednesday, March 18, 2009	Sheet 35 of 53



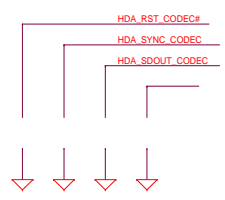
+5VS

+5VDDA\_CODEC

+3VS

+3VDD\_CODEC

+5VDDA\_CODEC

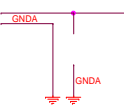


+MIC1\_VREF0\_L

+5VDDA\_CODEC

+3VDD\_CODEC

+IOVDD\_CODEC



INT\_MIC\_L

MIC\_INTL

MIC\_INTR

C\_LINE\_OUTL

C\_LINE\_OUTR

LINE\_OUTL

LINE\_OUTR

<37> EXT\_MIC\_L

<37> EXT\_MIC\_R

INT\_MIC\_L

INT\_MIC\_R

MIC\_INTL

MIC\_INTR

MIC\_INL

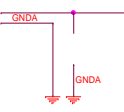
MIC\_INR

SPDFIF\_OUT <37>

HP\_OUTL <37>

HP\_OUTR <37>

MONO\_OUT <37>



INT\_MIC\_R

- <8,28> HDA\_BITCLK\_CODEC
- <8,28> HDA\_SDOUT\_CODEC
- <28> HDA\_SDIN2
- <8,28> HDA\_RST\_CODEC#
- <8,28> HDA\_SYNC\_CODEC
- <38> GPO\_AUD
- <37> MIC\_JD
- <37> PLUG\_IN
- <38> EAPD

BITCLK

HDA\_SDOUT\_CODEC

HDA\_RST\_CODEC#

HDA\_SYNC\_CODEC

SENSEA

SENSEB

+MIC1\_VREF0\_L

+MIC2\_VREF0

+5VAMP

+3VS

GAIN0

GAIN1

LINE\_OUTL

LINE\_OUTR

LIN

RIN

AMP\_OFF#

EC\_MUTE#

EC\_MUTE# <37,38>

SPK\_L1-

SPK\_R1-

SPK\_L2+

SPK\_R2+

SPK\_L1- <37>

SPK\_R1- <37>

SPK\_L2+ <37>

SPK\_R2+ <37>

+5VAMP

+5VAMP

GAIN0

GAIN1

<38> BEEP#

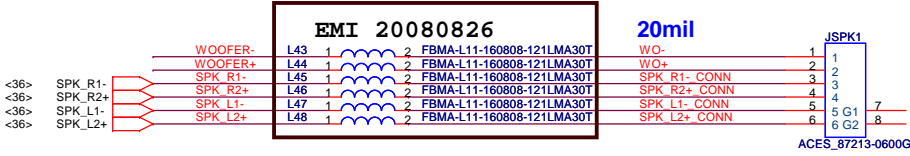
PC\_BEEP1

PC\_BEEP

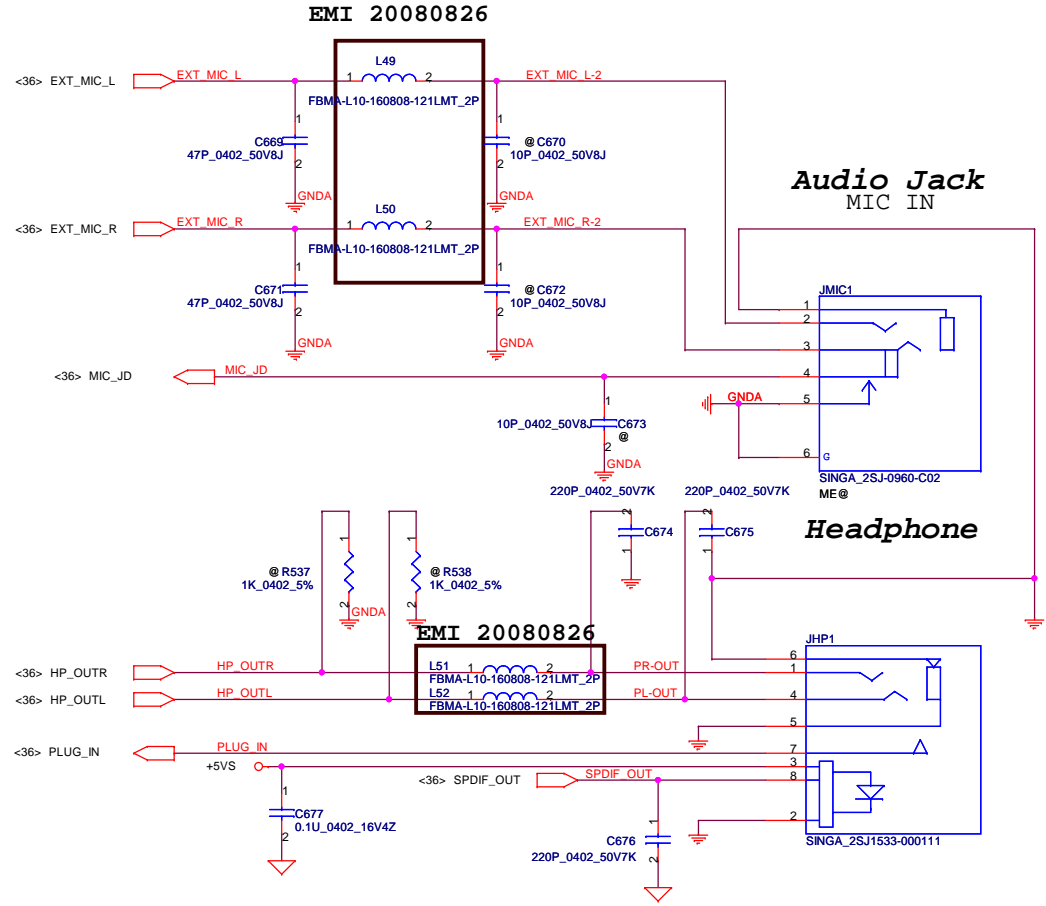
<29> SB\_SPKR



**SubWoofer Conn.  
Speaker Connector**



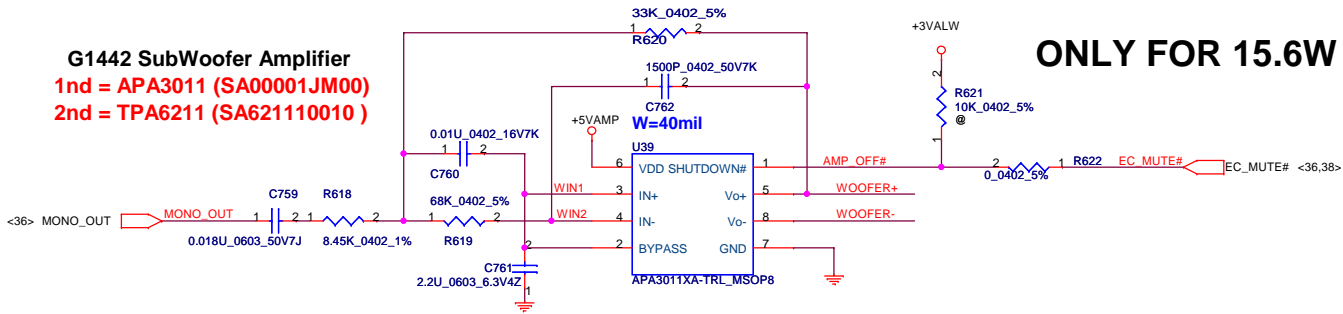
**Audio Jack**



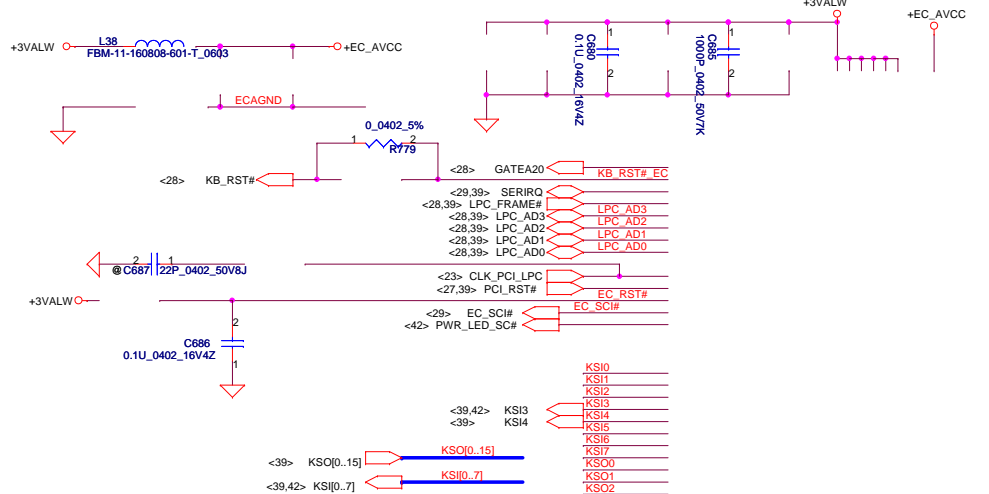
**G1442 SubWoofer Amplifier**

1nd = APA3011 (SA00001JM00)  
2nd = TPA6211 (SA621110010)

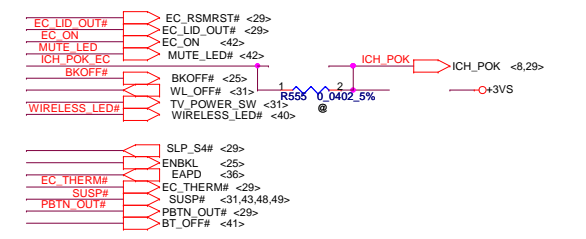
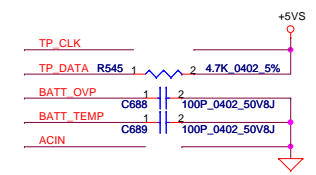
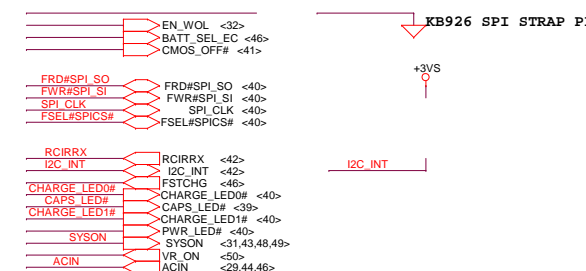
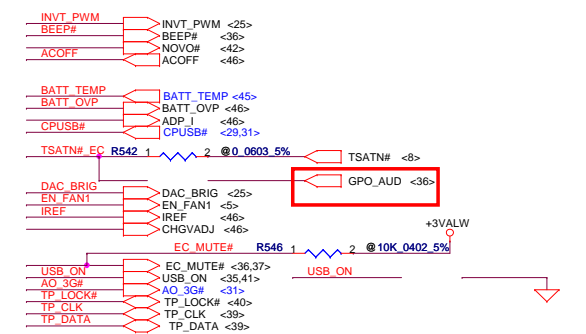
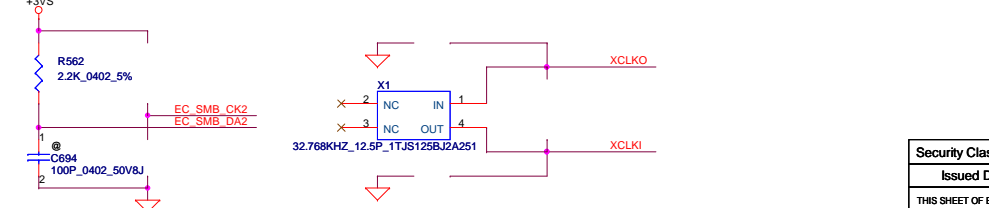
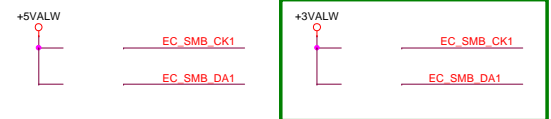
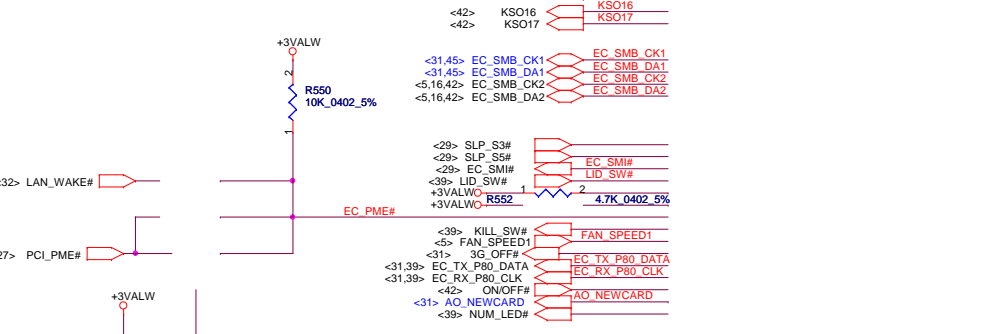
**ONLY FOR 15.6W**



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Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	<b>AMP, Audio speaker CONN</b>
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Custom	KIWB1/B2_LA4601P				
Date:	Wednesday, March 18, 2009	Sheet	37	of	53



**ENE UPDATE 10/21**  
 KSO1  
 KSO2

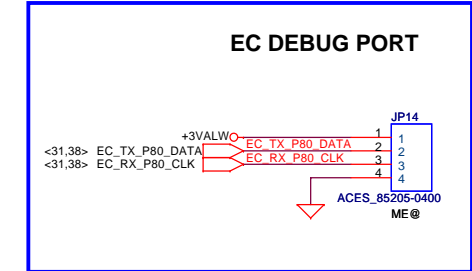
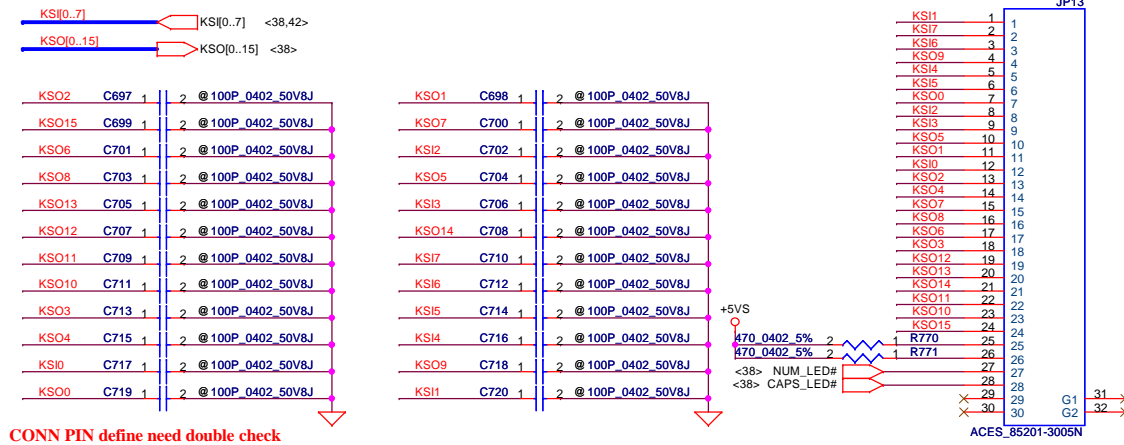


ENE ISSUE CHANGE FROM 4.7uF TO 1uF  
20080606

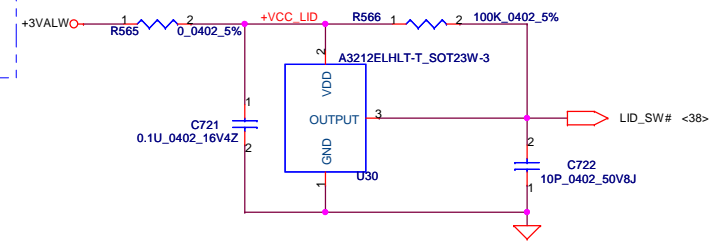
needed to update to D2 version  
SA00001J570

Security Classification	Compal Secret Data		<b>Compal Electronics, Inc.</b>	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title
				<b>BIOS &amp; EC I/O Port</b>
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Size	Document Number	Rev		0.1
Customer	JITRI_LA-414IP			
Date	Wednesday, March 18, 2009	Sheet	38	of 53

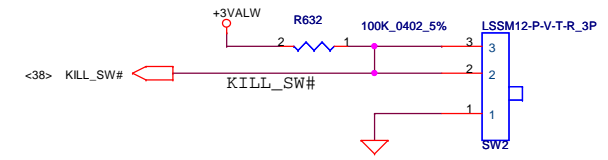
### INT\_KBD Conn.



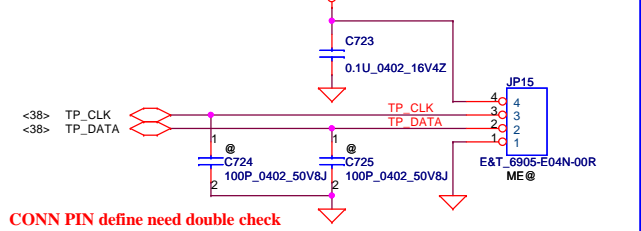
### Lid Switch



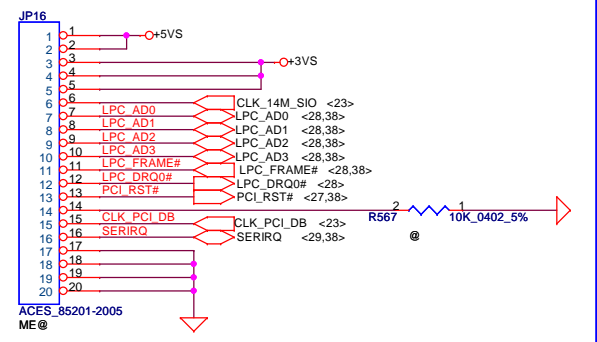
### Kill Switch



### To TP/B Conn.

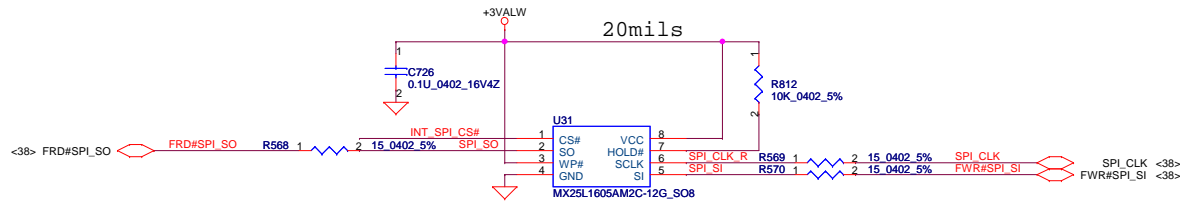


### FOR LPC SIO DEBUG PORT

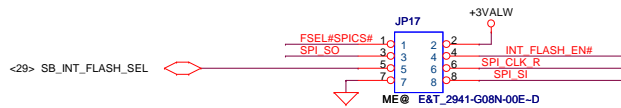
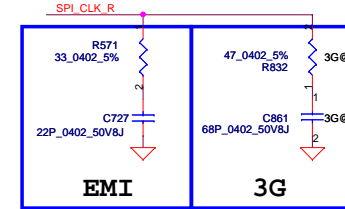
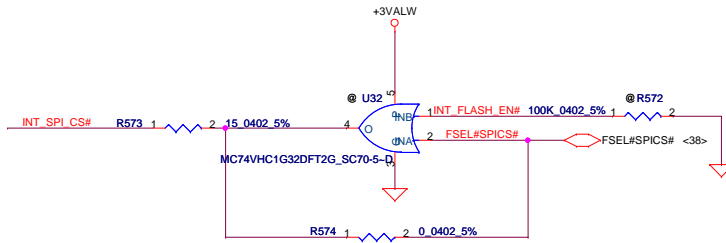


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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc.	
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Size	Document Number	Rev		0.1	
B	KIWB1/B2_LA4601P				
Date:	Wednesday, March 18, 2009	Sheet	39	of	53

# FOR EC 16M SPI ROM

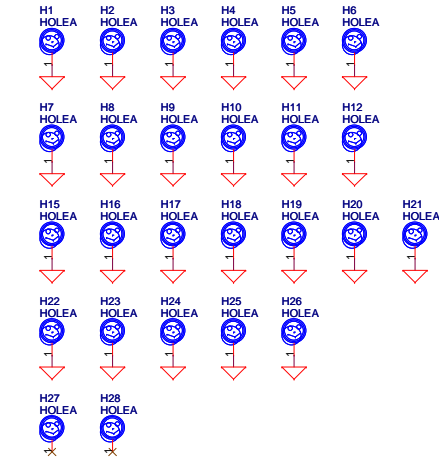
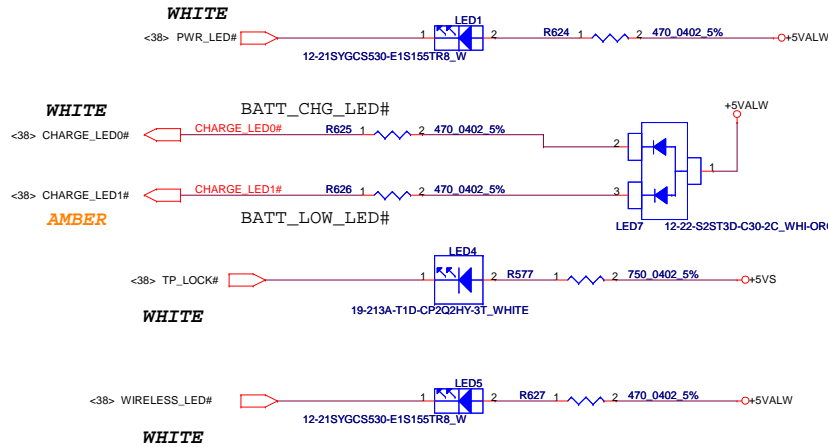


INPUT		OUTPUT
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	H

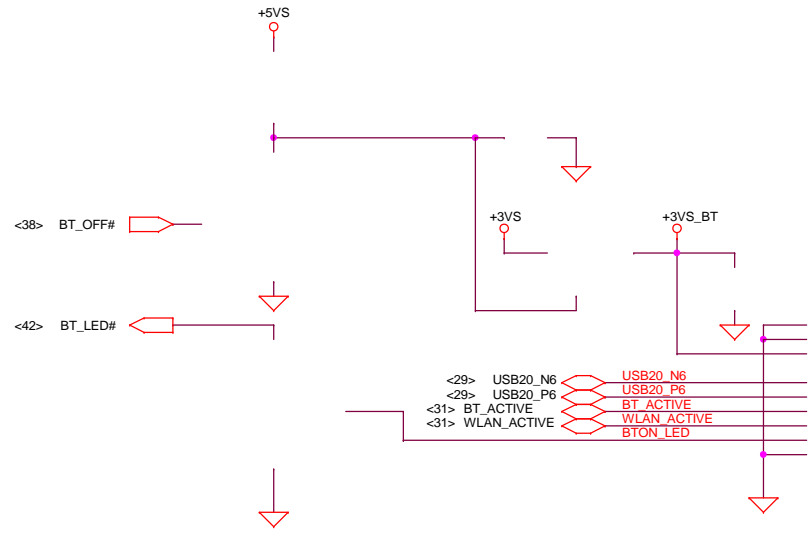
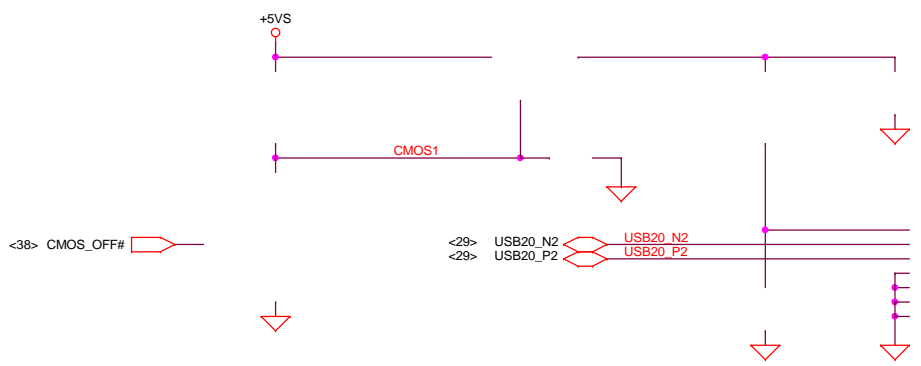
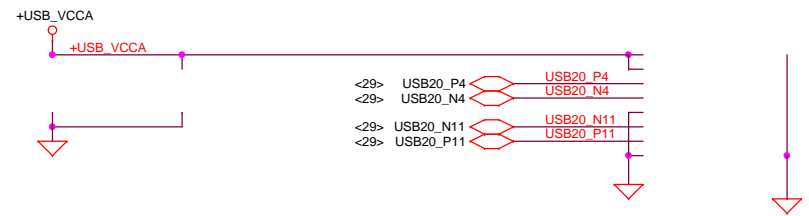
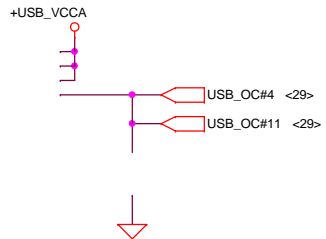
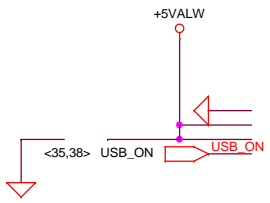


## LED

SC500005B00, If=5mA, Vf=2.7V~3.15V, R=460~390ohm

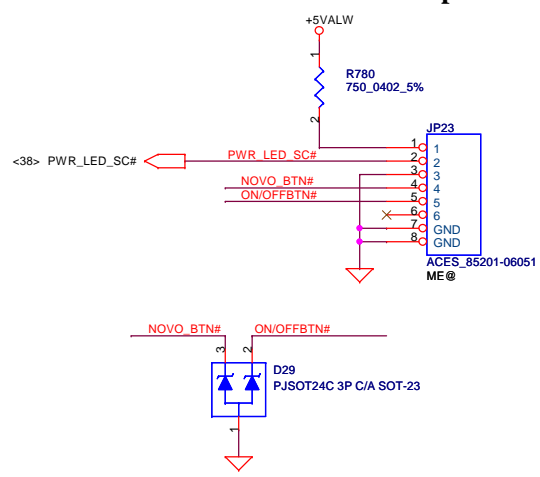


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Size	Document Number	Rev		
B	KIWB1/B2_LA4601P	0.1		
Date:	Wednesday, March 18, 2009	Sheet	40 of 53	

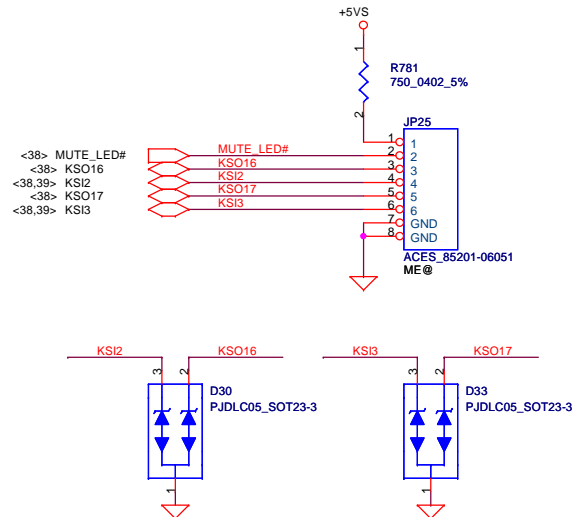


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Date:	Size	Document Number	Rev
		Sheet	of

### Power Bottom Board Conn. 6 pin

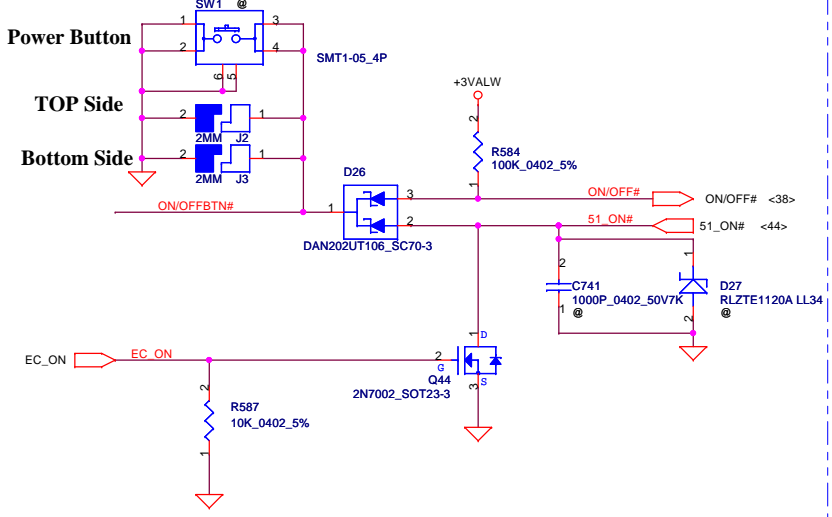


### Bottom Board Conn. 6 pin

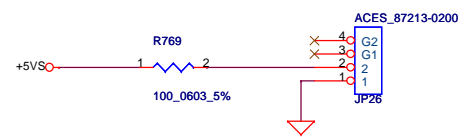


BTN FUNCTION	KEY MATRIX	
	IN	OUT
MUTE BTN	KSO17	KSI3
DOWN	KSO17	KSI2
UP	KSO16	KSI2

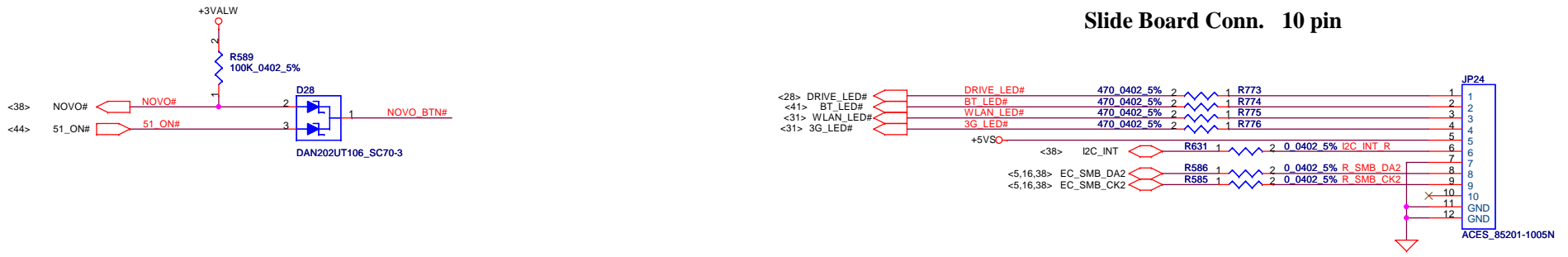
### ON/OFF switch



### IDEAPAD BOARD 2PIN

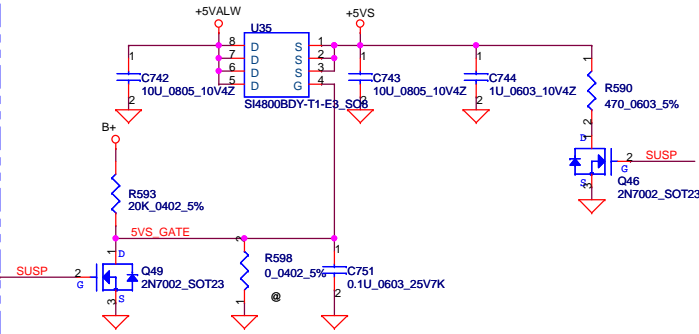


### Slide Board Conn. 10 pin

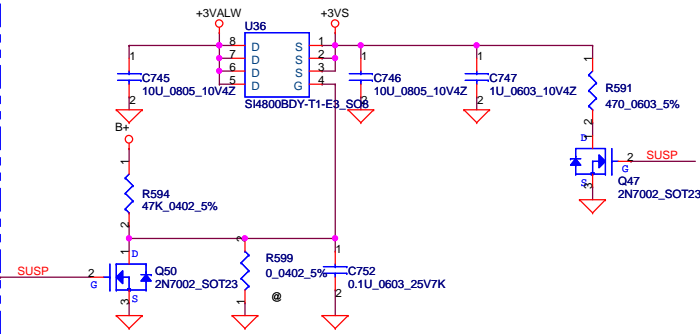


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				Size Custom
				KIWBI/B2_LA4601P
				0.1
Date: Wednesday, March 18, 2009		Sheet 42 of 53		

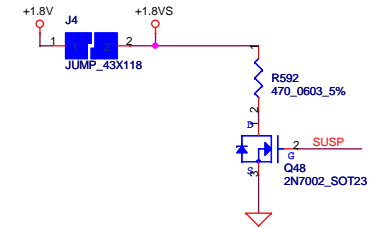
**+5VALW TO +5VS**



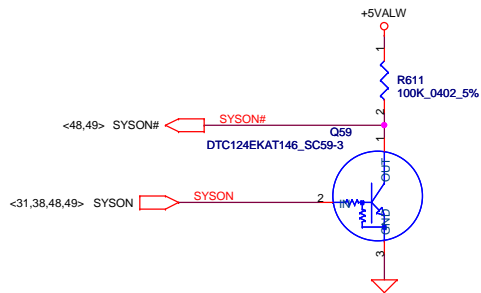
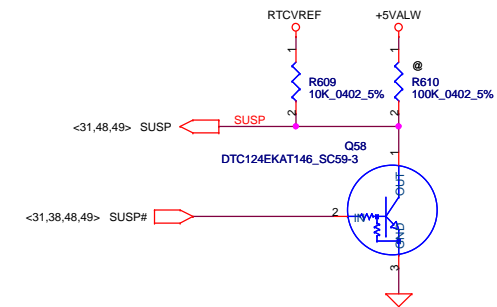
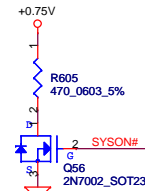
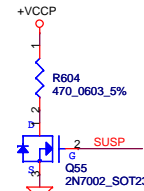
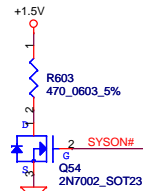
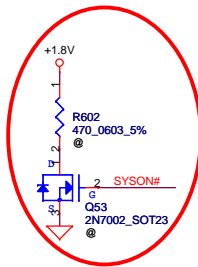
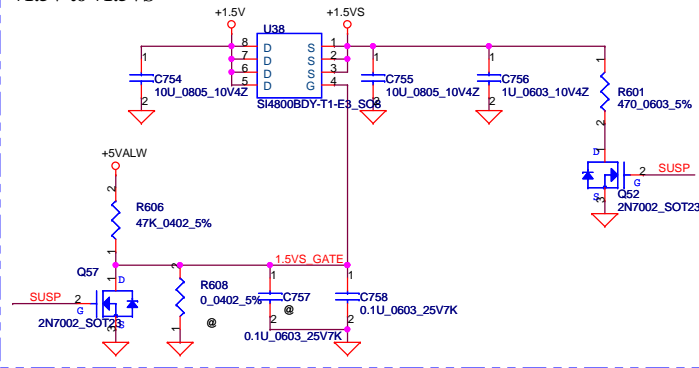
**+3VALW TO +3VS**



**+1.8V to +1.8VS**



**+1.5V to +1.5VS**



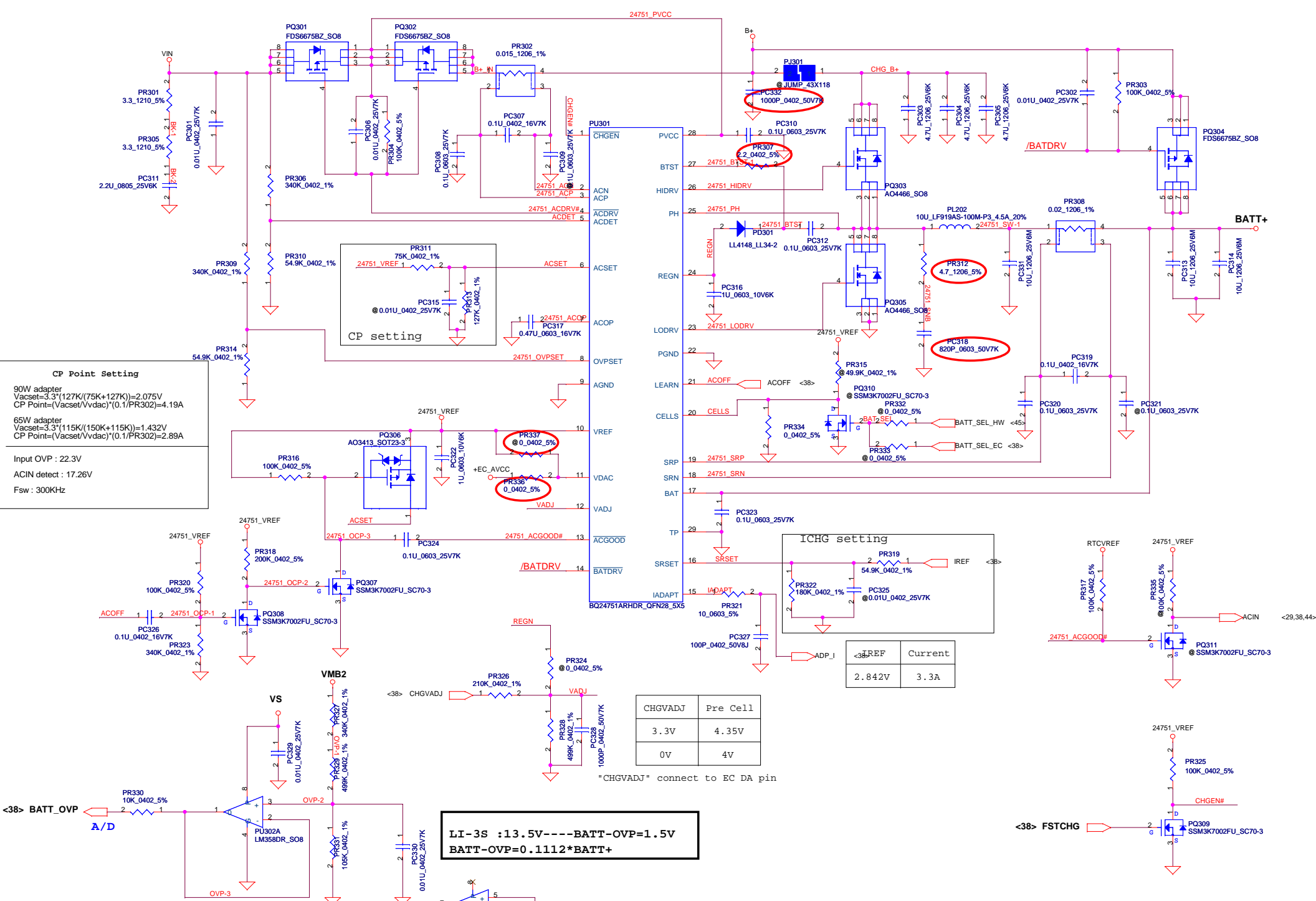
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2006/08/18	Deciphered Date		2007/8/18
Title					
DC Interface					
Size	Document Number				Rev
Custom	KIWB1/B2_LA4601P				0.1
Date:		Monday, April 27, 2009		Sheet	43 of 53

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**CP Point Setting**

90W adapter  
 $V_{acset} = 3.3 \times (127K / (75K + 127K)) = 2.075V$   
 $CP \text{ Point} = (V_{acset} / V_{dacc}) \times (0.1 / PR302) = 4.19A$

65W adapter  
 $V_{acset} = 3.3 \times (115K / (150K + 115K)) = 1.432V$   
 $CP \text{ Point} = (V_{acset} / V_{dacc}) \times (0.1 / PR302) = 2.89A$

Input OVP : 22.3V  
 ACIN detect : 17.26V  
 Fsw : 300KHz

**CP setting**

PR311 75K\_0402\_1%  
 PC315 0.01U\_0402\_25V7K  
 PR313 127K\_0402\_1%  
 PC317 0.47U\_0603\_16V7K  
 24751\_VREF 1  
 24751\_OVPSET 8

**ICHG setting**

PR319 54.9K\_0402\_1%  
 PC322 180K\_0402\_1%  
 PC325 0.01U\_0402\_25V7K  
 IREF <38>  
 ADP\_1

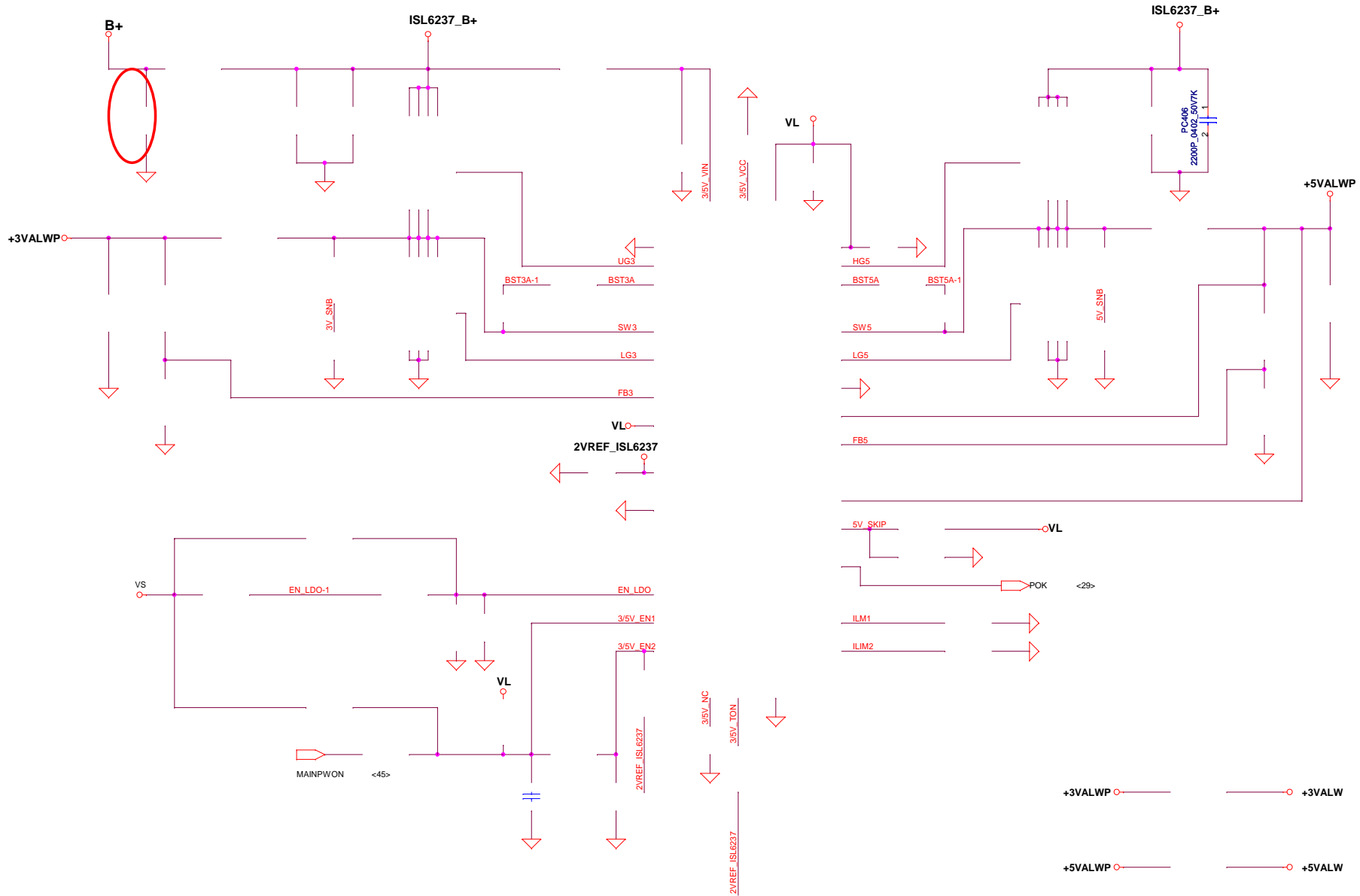
CHGVADJ	Pre Cell
3.3V	4.35V
0V	4V

"CHGVADJ" connect to EC DA pin

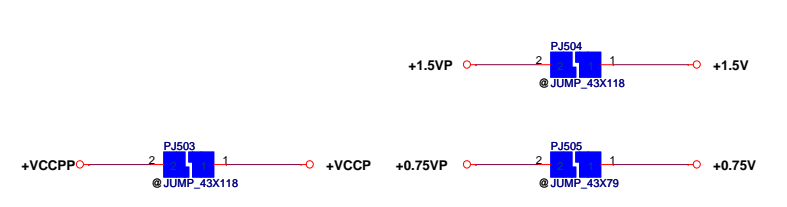
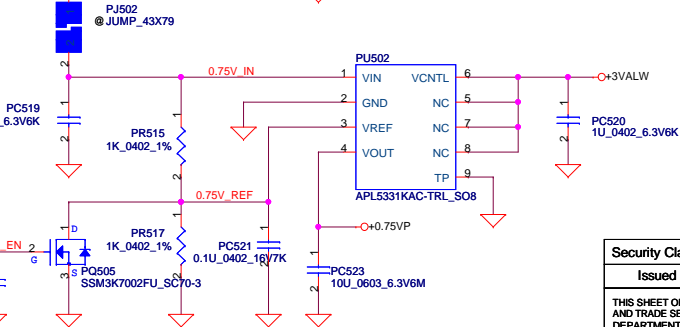
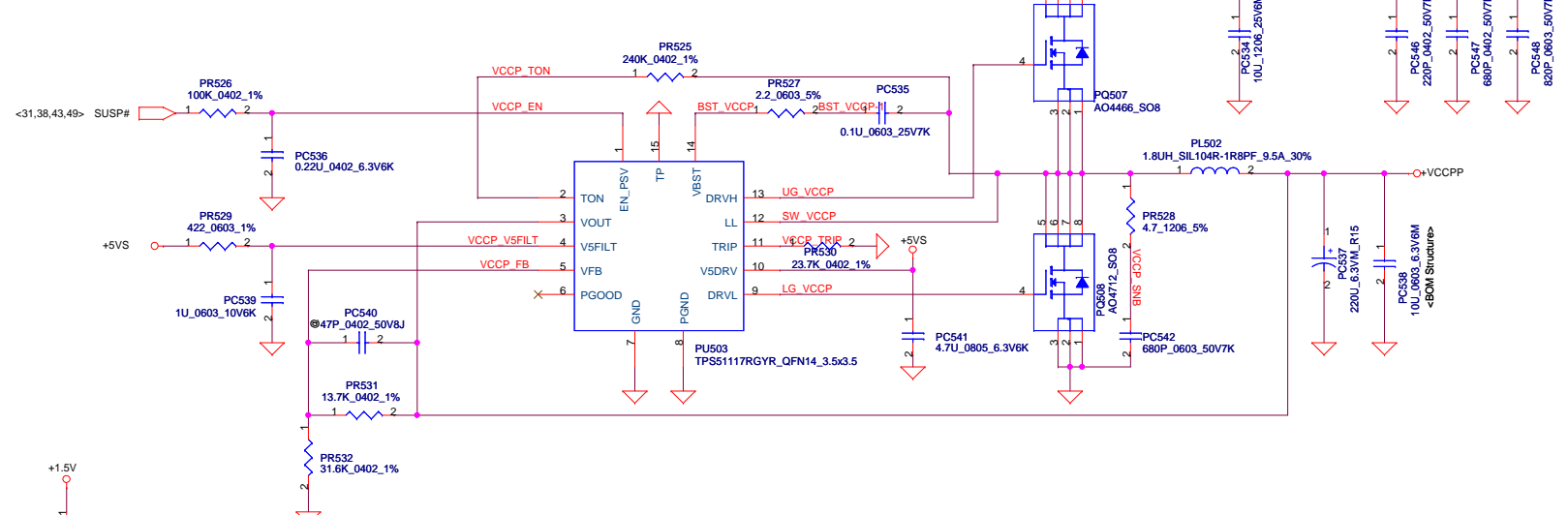
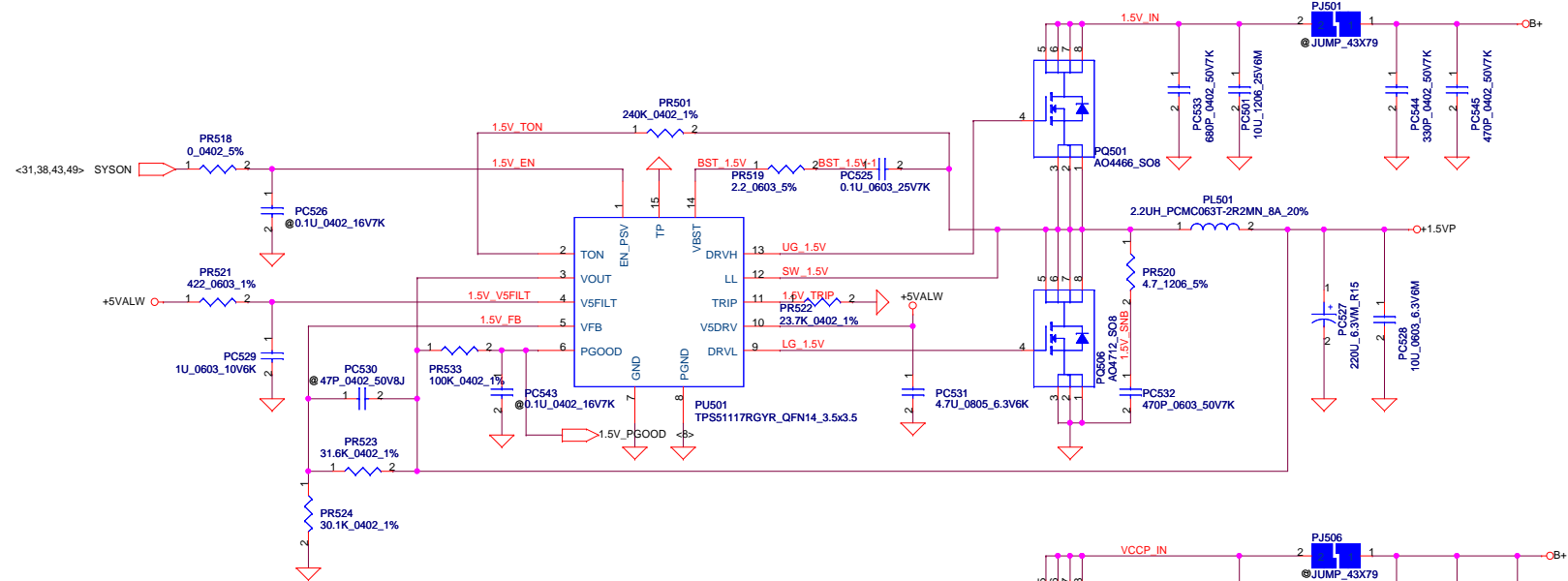
**LI-3S : 13.5V --- BATT-OVP=1.5V**  
 $BATT-OVP = 0.1112 \times BATT+$

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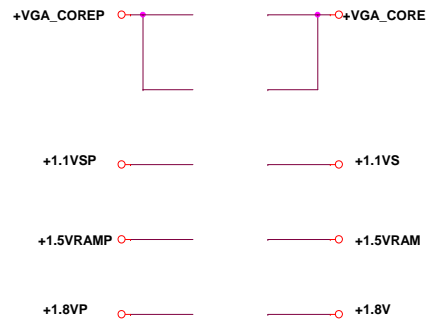
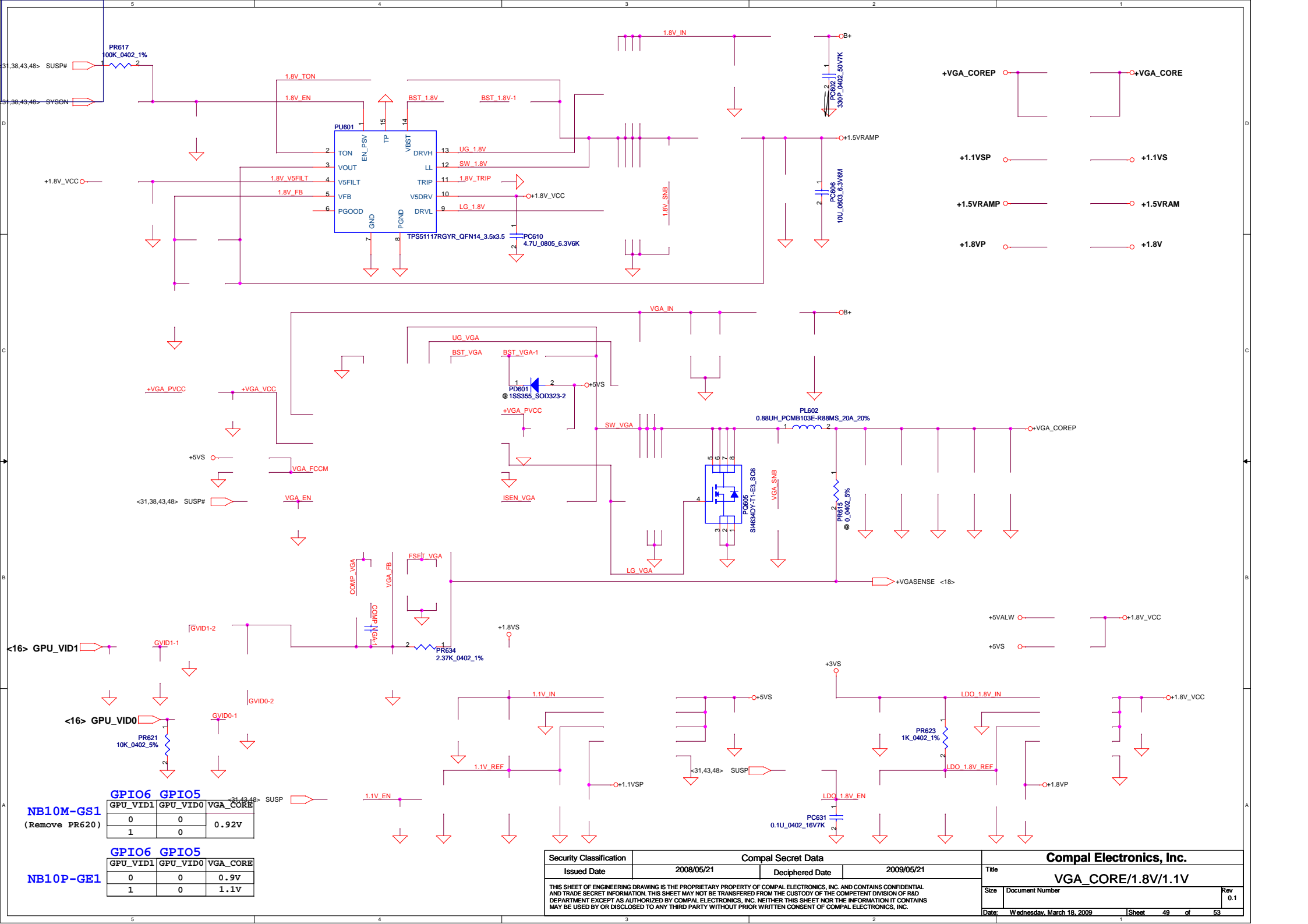
Compal Electronics, Inc.		
<b>CHARGER</b>		
Title	Document Number	Rev
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Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> Title <b>3VALW / 5VALW</b>	
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				Custom	0.1
Date: Wednesday, March 18, 2009				Sheet	47 of 53



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Issued Date	2008/05/21	Deciphered Date	2009/05/21	Title	1.5V/VCCP/0.75V
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**NB10M-GS1**  
(Remove PR620)

GPIO6	GPIO5	VGA_CORE
GPU_VID1	GPU_VID0	0.92V
0	0	
1	0	

**NB10P-GE1**

GPIO6	GPIO5	VGA_CORE
GPU_VID1	GPU_VID0	0.9V
0	0	
1	0	1.1V

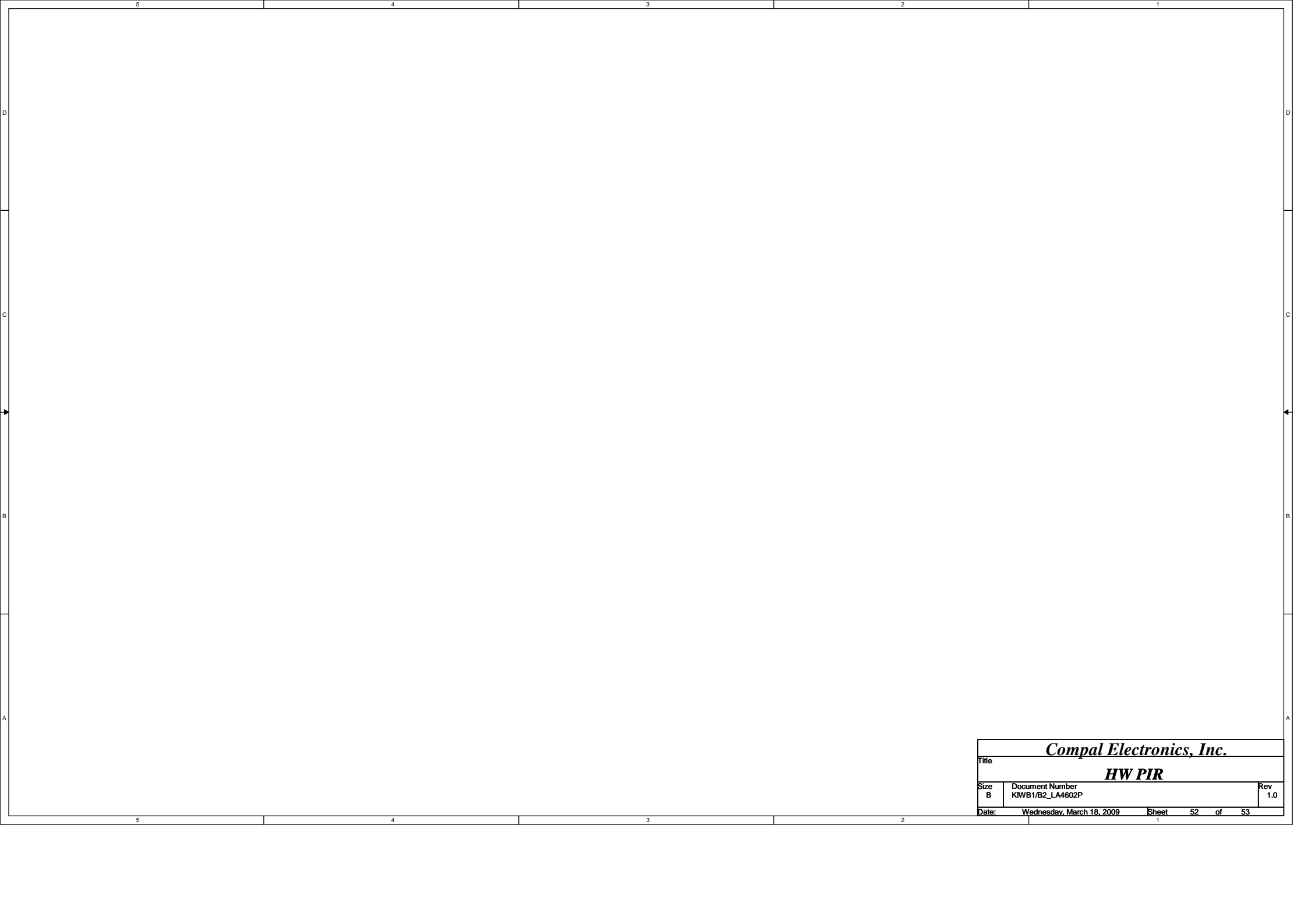
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Issued Date	2008/05/21	Deciphered Date	2009/05/21	Title	
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Version change list (P.I.R. List)

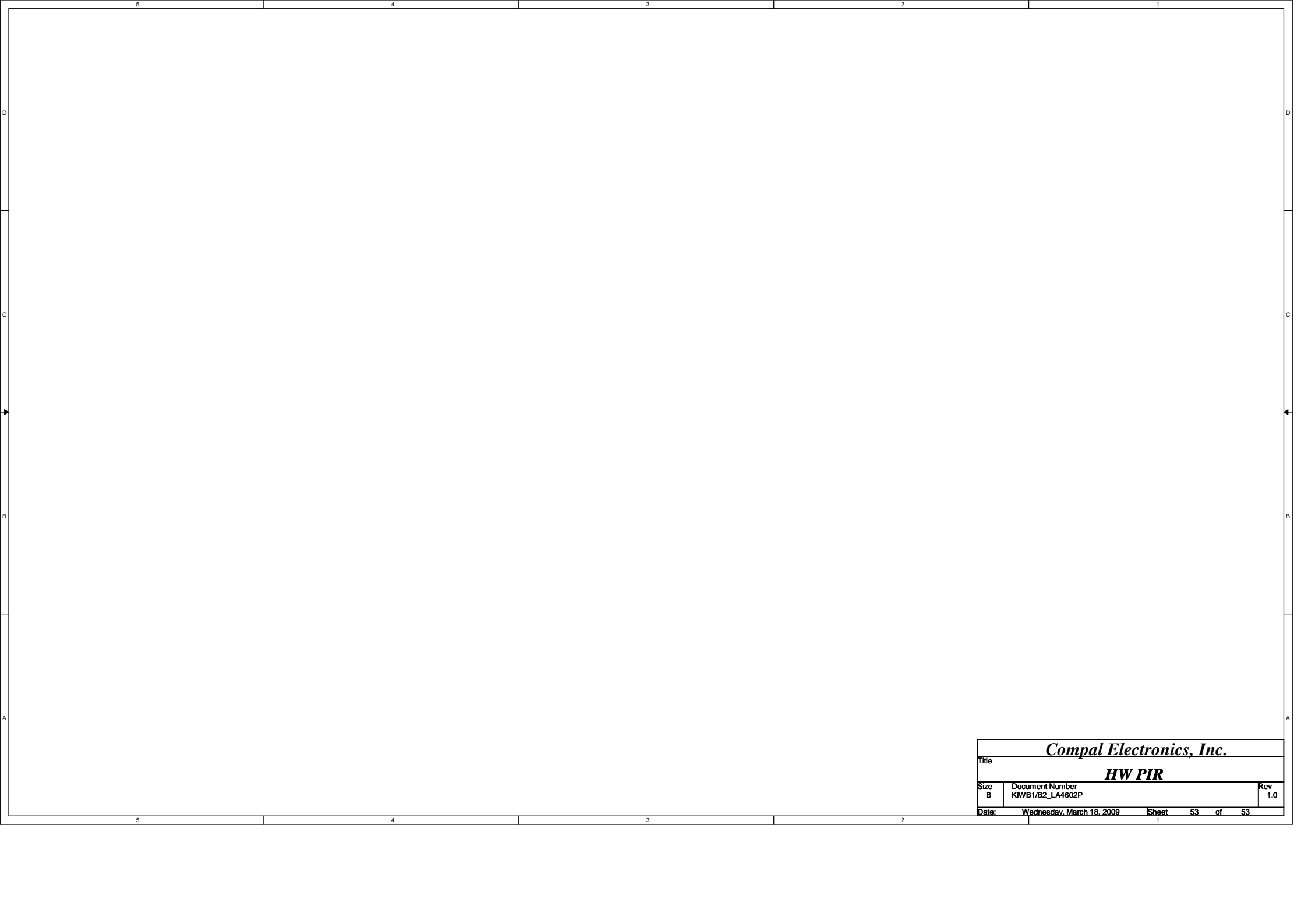
Item	Reason for change	PG#	Modify List	Date	Phase
1	Improve charge output current accuracy.	P46	Change PU301 Pin 11 VDACC source form 24751_VREF to +EC_AVCC.	20080725	DVT
2	Improve CPU_CORE transient response.	P50	Change PR801, PR848 from 15.4k_0402_1% to 17.8k_0402_1% Change PR840, PR850 from 196k_0402_1% to 69.8k_0402_1% Change PC829, PC835 from 0.022u to 0.033u.	20080804	DVT
3	Adjust loadline.	P50	Change PR839 from 5.76k_0402_1% to 4.02k_0402_1%	20080804	DVT
4	Reduce VGA_CORE ripple.	P49	Add PC633, PC634 10u_0603_6.3V_V6M. Add PC619 330u_2.5V_R9M	20080804	DVT
5	Improve VGA_CORE efficiency at heavy load.	P49	Add PD601	20080804	DVT
6	Adjust 0.75V power sequence.	P48	Add PR534.	20080813	DVT
7	Adjust power sequence.	P48 P49	Change PR525 from 0 to 27K. PR526 from 0 to 100k. Add 0.1u_0402 at PC630 0.22u_0402 at PC536.	20080813	DVT
8	For customer upgrade VGA to N10X.	P49	Change PQ603 from SI4686 to SI7686DP. Change PQ604, PQ605 from FDMS670 to SI4634DY. Change PL602 from 1u to .88u. Change PC615 from 220u ESR15 to 330u ESR9.	20080813	DVT
9	Reserve OSR to reduce overshoot.	P50	Add PR865	20080813	DVT
10	Improve VGA CORE driver ability for upgrade VGA chip from N9X to N10X.	P49	Change PU602 VGA CORE solution from TPS51117 to ISL6269A	20080823	DVT
11	Reduce power board band.	P47 P48 P49 P50	Change PR403, PR405, PR519, PR527, PR603, PR611, PR841, PR846 to 2.2ohm at BOM. Change PR402, PR404, PR520, PR528, PR604, PR612, PR819, PR829 to 4.7ohm at BOM. Change PC414, PC415 to 330p_0402_50V at BOM. Change PC542, PC608, PC618, PC815, PC823 680P_0603_50V7K at BOM. Change PC532 to 470P_0603_50V7K. Add PC546 220P_0402_50V7K. Add PC405, PC544, PC602, PC617, PC806 330P_0402_50V7K. Add PC545 470P_0402_50V7K. Add PC533, PC547 680P_0402_50V7K.	20080826	DVT
12	Change 1.8V sequence the same with 1.8VS.	P49	Add PR617, PR631, PR637.	20080902	DVT
13	For solve charger unstable.	P46	Add PC331 10u_1206_25V6M	20080902	DVT
14	Adjust power sequence.	P49	Change PR617, PR632 to 100k_0402_1%. Add PC604, PC631 to 0.1u_0402.	20080905	DVT
15	Reduce power board band.	P46	Add PC332 1000P_0402_50V7K	20081013	PVT
16	Reserve VDACC power connect to 24751_VREF and EC_AVCC	P46	Add PR336, PR337 0_0402_5%	20081015	PVT
17	Reduce power board band.	P44	Add PC112, PC113 0.1u_0603_50V7K	20081022	PVT

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