Blue Moutain KIWB1/B2

Schematics Document

Mobile Penryn uFCPGA with Intel Cantiga_GM/PM+ICH9-M core logic

REV:2.0

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Title: **Cover Sheet**

Size	Document Number	Rev
Custom	KIWB1/B2_LA4602P	2.0

Date: Wednesday, March 18, 2009 Sheet 1 of 53

Compal confidential
File Name :

ZZZ1
15.6W_PCB_LA4601P

POWER BD
Power on X1
LED X1 (G)
:POWER
NOVO X1

Slide Bar LED X 10 (B)
USER-DEFINED (W)
DOLBY (W)
LED X 3
WIRELESS LED (G)
BLUETOOTH LED (G)
3G LED (G)
HDD LED (G)

RIGHT BD
VOLUME UP X1
VOLUME DOWN X1
MUTE X1
MUTE LED X1(G)

USB_Board
USB CONN X 2
TV CONN X1

POWER ON (G)
BATTERY CHARG(G/A)
WIRELESS SWITCH (G)
ON/OFF

VRAM 64*16
DDR3*8
page20

NVidia N10M-GS1
NVidia N10P-GE1
page16~24

PCI-E X16

Mobile Penryn
uFCPGA-478 CPU
page5,6,7

Clock Gen.
SLG8SP556VTR
ICS9LPRS387AKLFT
page25

H_A#(3..35)
H_D#(0..63)
FSB
667/800/1066MHz

HDMI CONN
page26

PS8101T
page26

PCI-E

Intel Cantiga GMCH
PCBGA 1329
page 8,9,10,11,12,13

DDR3-800(1.5V)
DDR3-1067(1.5V)
Dual Channel

Double check ME
DDR3-SO-DIMM X2
BANK 0, 1, 2, 3
page 14,15
UP TO 8G

CRT cable
page28

LVDS I/F

LVDS Connector
page27

DMI
C-Line

SPK amplifier
page36

2Channel Speaker
page37

WOOFER amplifier
page37

1Channel Speaker
page37

PCI Express Mini card Slot 1
page31

PCI Express Mini card Slot 2
page31

PCI Express Mini card Slot 3
page31

6*PCI-E BUS

New Card
page31

None
PCI BUS
3.3V / 33 MHz

Intel ICH9-M
mBGA-676
page27,28,29,30

AZALIA

Audio Codec
Realtek ALC272
page36

HP X 1+
MIC_Ext X1 page37

2Channel MIC_Int
page36

12*USB2.0

4*SATA serial

CMOS Camera
page41

BlueTooth CONN
page41

USB CONN X1
page41

New Card X1
page31

M-PCIE CONN X 3
page31

Realtek 5158E
MS/MS
pro/SD/SD
pro/mmc/XD
page36

LPC BUS

EC
ENE KB926D
page38

SIM Card
page31

BCM5906/BCM5784M
10/100/1G LAN
page32

RJ45 CONN
page33

Int.KBD
page39

Touch Pad
page39

BIOS
page40

REPEATER
page35

ESATA HDD AND USB CONN
page35

SATA HDD CONN
page35

SATA ODD CONN
page35

HDD/ODD,SCL & T/L LED on MB
CAPS and NUM on KBD

Security Classification	Compal Secret Data		
Issued Date	2009/03/16	Deciphered Date	2010/03/

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Title: **MB Block Diagram**

Size	Document Number	Rev
Custom	KIWB1/B2_LA4602P	0.1

Date: Wednesday, March 18, 2009 Sheet 2 of 53

DDR3 Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +1.1VS +VCCP +CPU_CORE +VGA_CORE +1.8VS +0.75V
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

@ FUNCTION

100@	(100 LAN)		
TVSW@	(TV POWER SW)	10M@	(N10M 40nm CHIPSET)
AO@	(ALWAYS ON SW)	10P@	(N10P 40nm CHIPSET)
MONO@	(MONO MIC)	PM@	(VGA BOM)
X76@	(X76 BOM)	45@	(45 BOM)
		GM@	(UMA BOM)
		GM45@	(GM45 BOM)
		GL40@	(GL40 BOM)
BT@	WITH BLUETOOTH	GIGA@	(GIGA LAN)
3G@	WITH 3G	NO_TVSW@	(NON TV POWER SW)
TV@	WITH TV	NO_AO@	(NON ALWAY ON SW)
		ARRAY@	(ARRAY MIC)
		S512@	FOR X76 BOM
		Q512@	FOR X76 BOM
		S256@	FOR X76 BOM
		Q256@	FOR X76 BOM

SMBUS, SPI and I2C Control Table

	SOURCE	HDMI	LVDS	CRT	HDCP	SERIAL EEPROM	NEW CARD	CLK GEN	CAP sensor	Mini CARD1	Mini CARD2	BATT	THERMAL SENSOR (VGA)	THERMAL SENSOR (CPU)
EC_SMB_CK1 EC_SMB_DA1	KB926	X	X	X	X	X	X	X	X	X	X	V	X	X
EC_SMB_CK2 EC_SMB_DA2	KB926	X	X	X	X	X	X	X	V	X	X	X	V	V
ICH_SMBCLK ICH_SMBDAT	ICH9	X	X	X	X	X	V	V	X	V	V	X	X	X
LVDS_SCL LVDS_SDA	Cantiga	X	V	X	X	X	X	X	X	X	X	X	X	X
GMCH_CRT_CLK GMCH_CRT_DAT	Cantiga	X	X	V	X	X	X	X	X	X	X	X	X	X
HDMICLK_NB HDMIDAT_NB	Cantiga	V	X	X	X	X	X	X	X	X	X	X	X	X
VGA_DDCCLK VGA_DDCDATA	VGA	X	X	V	X	X	X	X	X	X	X	X	X	X
VGA_LVDS_SCL VGA_LVDS_DAT	VGA	X	V	X	X	X	X	X	X	X	X	X	X	X
VGA_HDMI_SCL VGA_HDMI_DAT	VGA	V	X	X	X	X	X	X	X	X	X	X	X	X
HDCP_SMB_CK1 HDCP_SMB_DA1	VGA	X	X	X	X	V	X	X	X	X	X	X	X	X
FSEL#SPICS#_SB FRD#SPI_SO_SB SPI_CLK_SB FWR#SPI_SI_SB	ICH9	X	X	X	X	V	X	X	X	X	X	X	X	X
FSEL#SPICS# FRD#SPI_SO SPI_CLK FWR#SPI_SI	KB926	X	X	X	X	V	X	X	X	X	X	X	X	X

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Title: MB Notes List

Size: B | Document Number: KIWB1/B2_LA4601P | Rev: 0.1

Date: Wednesday, March 18, 2009 | Sheet 3 of 53

VGA and DDR3 Voltage Rails (N10x GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	N/A	N/A	
GPIO1	IN	-	Hot plug detect for IFP link C
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID0
GPIO6	OUT	-	GPU VID1
GPIO7	OUT	-	GPU VID2
GPIO8	I/O	L	Thermal Catastrophic Overtemp
GPIO9	OUT	L	Thermal Alert
GPIO10	OUT		Memory VREF switch
GPIO11	I/O	L	SLI raster sync
GPIO12	IN	-	AC power detect pin
GPIO13	OUT	-	MEM_VID orPower supply control
GPIO14	OUT	-	Power supply control
GPIO15	IN	-	Hot plug detect for IFP Link E
GPIO16	OUT	-	Programmable Fan Control
GPIO17	IN	-	
GPIO18	IN	-	
GPIO19	IN	-	Hot plug detect for IFP Link D
GPIO20	IN	-	
GPIO21	IN	-	Hot plug detect for IFP link F
GPIO22	IN	-	SLI swap ready signal
GPIO23	I/O		

GPIO6	GPIO5	N10M-GS	N10P-GS
GPU_VID1	GPU_VID0	VGA_CORE	P-State
0	0	0.8V	12
0	1	0.85V	12
1	1	0.9V	0, 10

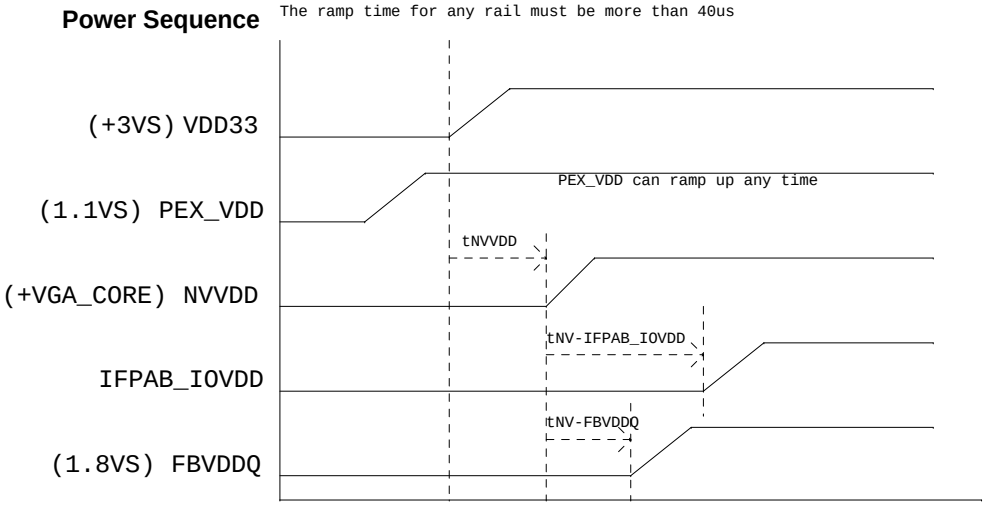
Performance Mode P0 TDP at Tj = 102 C* (DDR3)

Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.5V) (A)	FBVDD (1.5V) (W)	FBVDDQ (GPU+Mem) (1.5V) (A)	FBVDDQ (GPU+Mem) (1.5V) (W)	PCI Express (1.05V) (6) (mA)	PCI Express (1.05V) (6) (W)	I/O and PLLVDD (1.8V) (mA)	I/O and PLLVDD (1.8V) (W)	I/O and PLLVDD (1.05V) (mA)	I/O and PLLVDD (1.05V) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N10P-GS 128bit 1024MB DDR3	21.07	6.67	TBD	TBD	18.25	17.34	2.06	3.09	4.09	6.14	850	0.89	75	0.14	63	0.07	55	0.18
N10P-GE 128bit 1024MB DDR3	20.97	6.73	TBD	TBD	19.17	17.25	2.03	3.05	4.09	6.14	840	0.88	75	0.14	63	0.07	55	0.18
N10P-LP 128bit 1024MB DDR3	15.48	6.44	TBD	TBD	13.95	11.86	1.90	2.85	3.99	5.99	810	0.85	75	0.14	63	0.07	55	0.18

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.5V) (A)	FBVDD (1.5V) (W)	FBVDDQ (GPU+Mem) (1.5V) (A)	FBVDDQ (GPU+Mem) (1.5V) (W)	PCI Express (1.05V) (6) (mA)	PCI Express (1.05V) (6) (W)	I/O and PLLVDD (1.8V) (mA)	I/O and PLLVDD (1.8V) (W)	I/O and PLLVDD (1.05V) (mA)	I/O and PLLVDD (1.05V) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N10M-GE 64bit 512MB DDR3	13.36	2.93	TBD	TBD	11.89	10.70	0.66	0.99	2.16	3.24	792	0.83	75	0.14	63	0.07	100	0.33
N10M-GS 64bit 512MB DDR3	14.29	3.10	TBD	TBD	11.53	11.53	0.70	1.05	2.28	3.42	817	0.86	75	0.14	63	0.07	100	0.33
N10M-LP 64bit 512MB DDR3	8.28	2.91	TBD	TBD	6.60	5.61	0.62	0.93	2.20	3.3	782	0.82	75	0.14	63	0.07	100	0.33

Power Sequence



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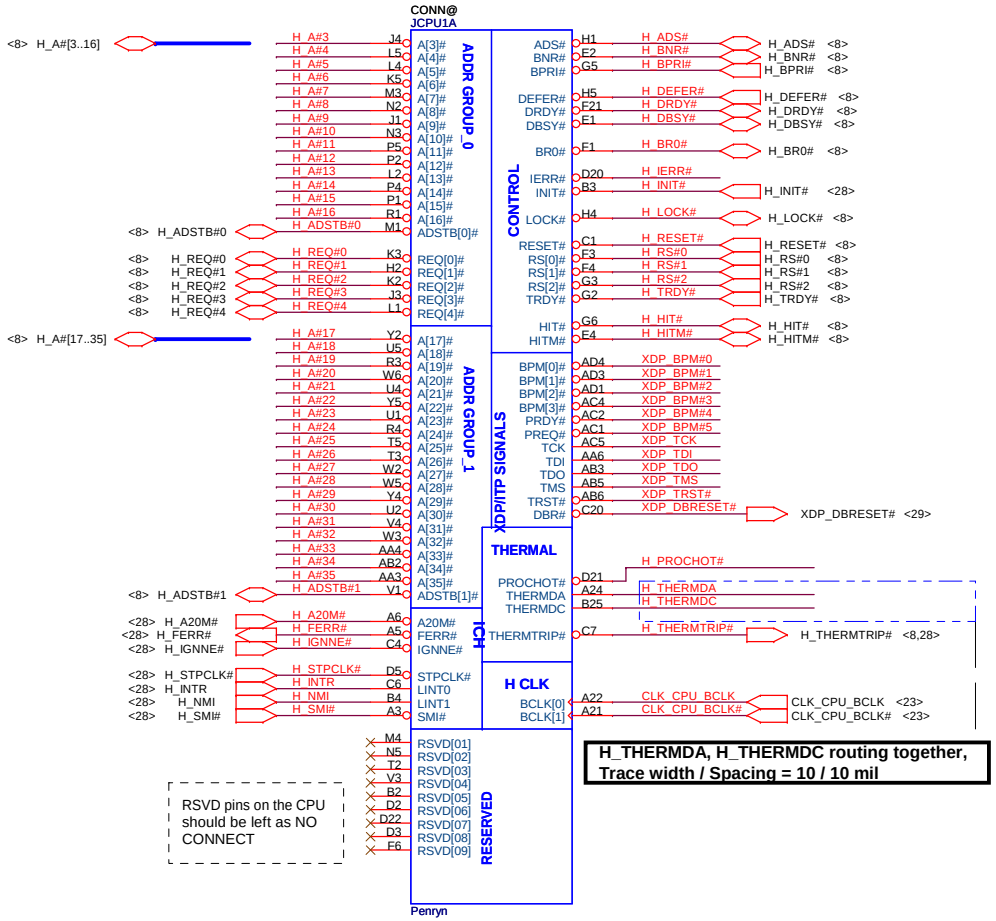
Title: VGA Notes List

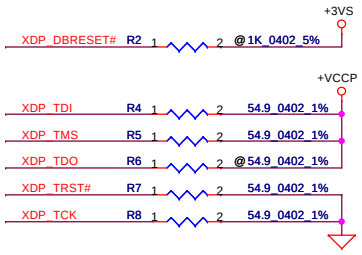
Size: B | Document Number: KIWB1/B2_LA4602P | Rev: 0.1

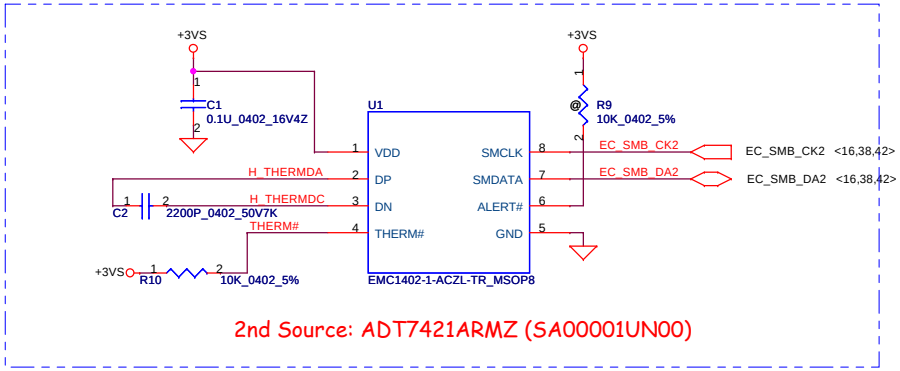
Date: Wednesday, March 18, 2009 | Sheet 4 of 53



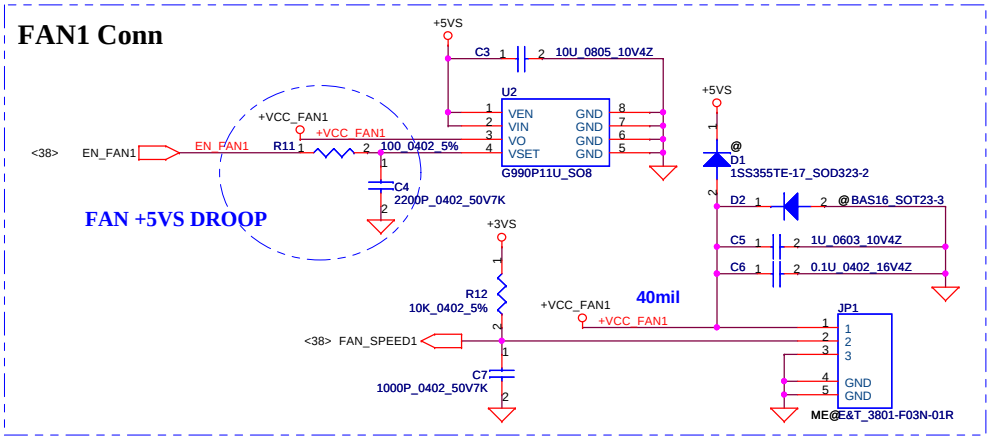
XDP Reserve

USE->68Ω,NOT USE-->56Ω





Address:100_1100



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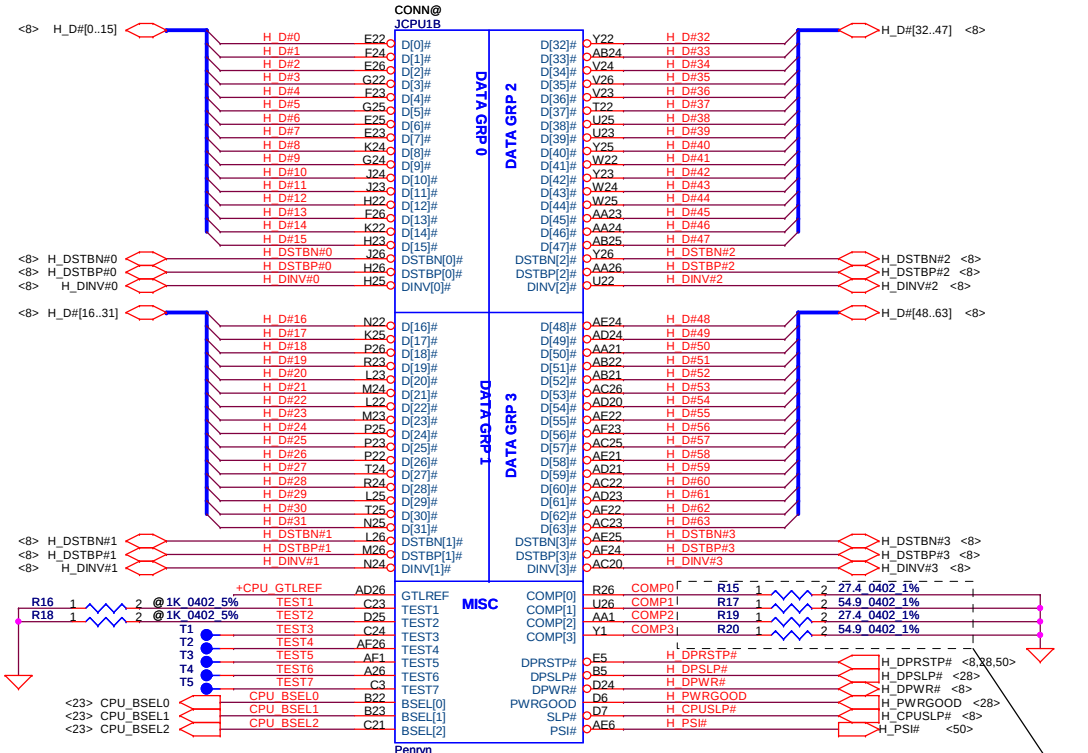
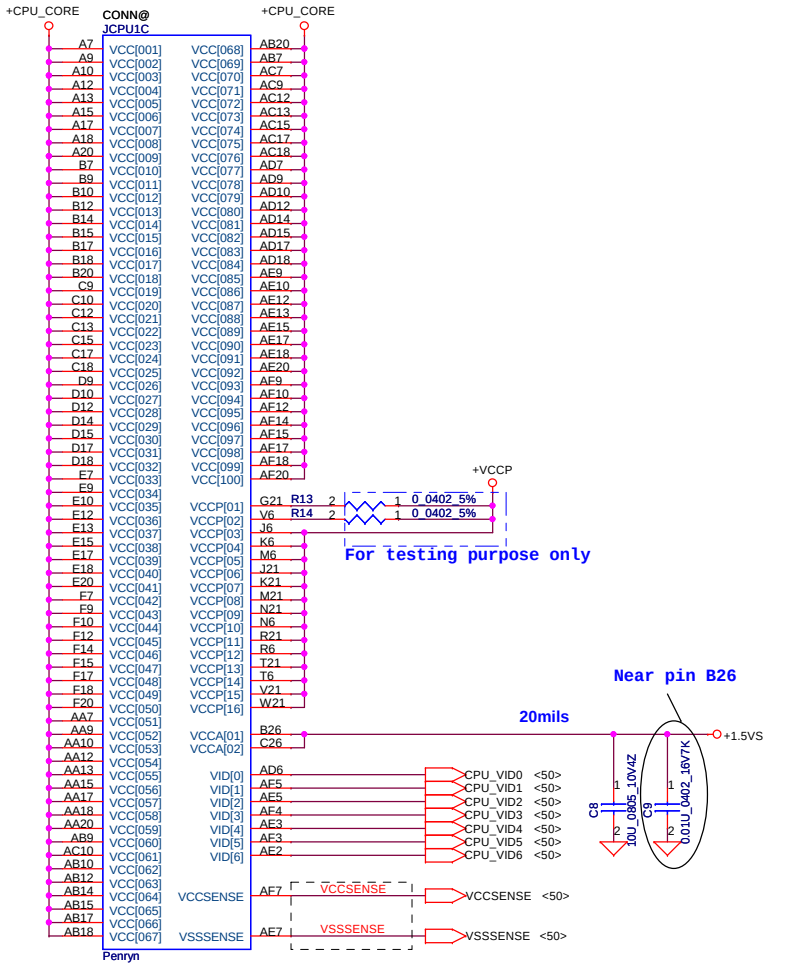
Title: **Penryn(1/3)**

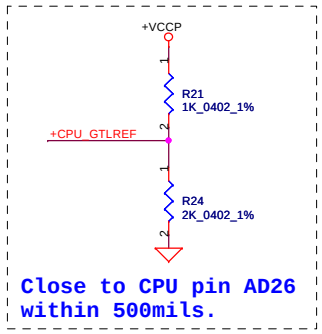
Size	Document Number	Rev
Custom	KIWB1/B2_LA4602P	0.1

Date: Wednesday, March 18, 2009 Sheet 5 of 53





layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

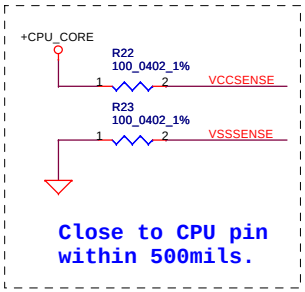


Layout note: Z0=55 ohm
0.5" max for GTLREF.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

Length match within 25 mils.
The trace width/space/other is 18/7/25.

Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.
Length matched to within 25 mils.



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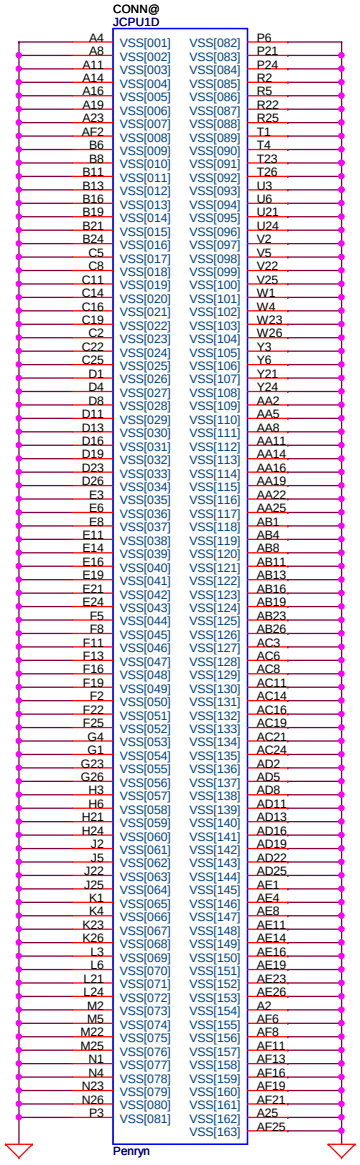
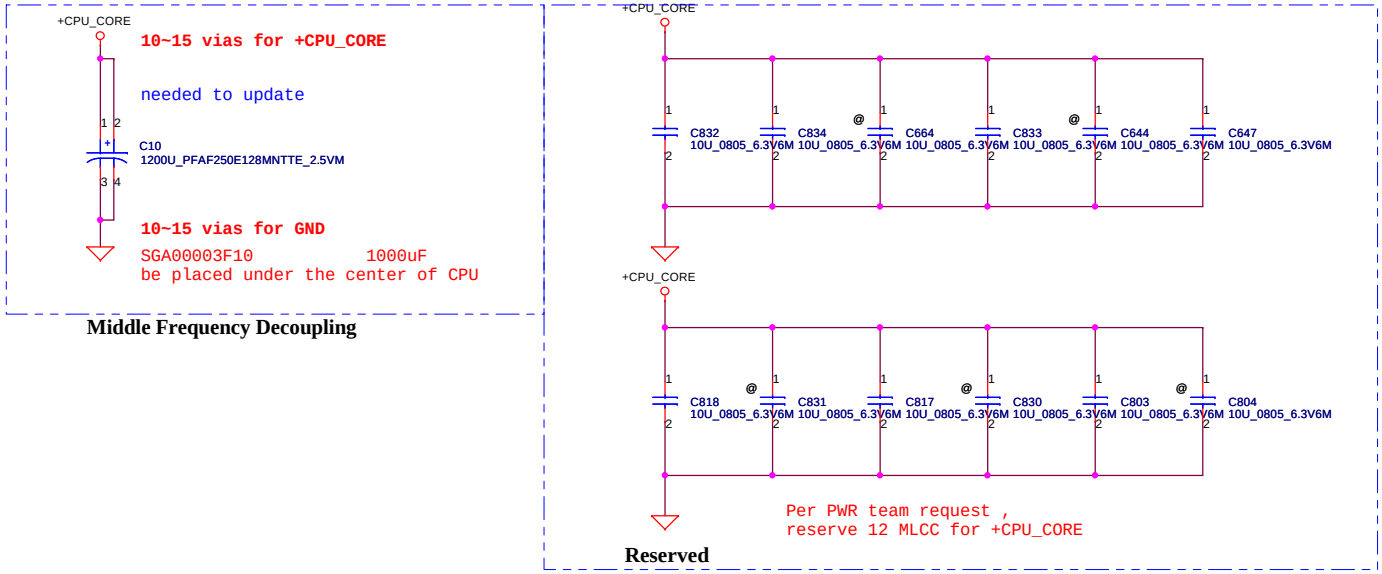
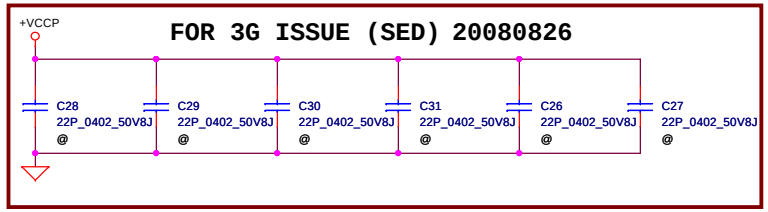
Title: **Penryn (2/3)**

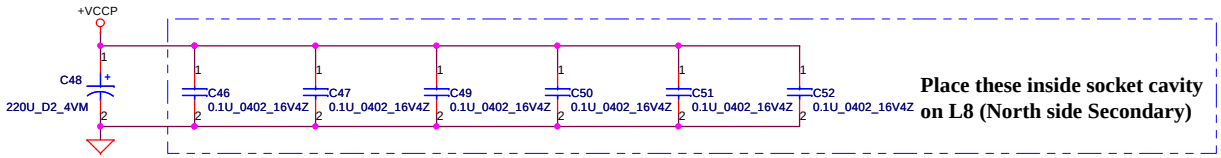
Size	Document Number	Rev
B	KIWB3/B4_LA4551P	0.1

Date: Wednesday, March 18, 2009 Sheet 6 of 53









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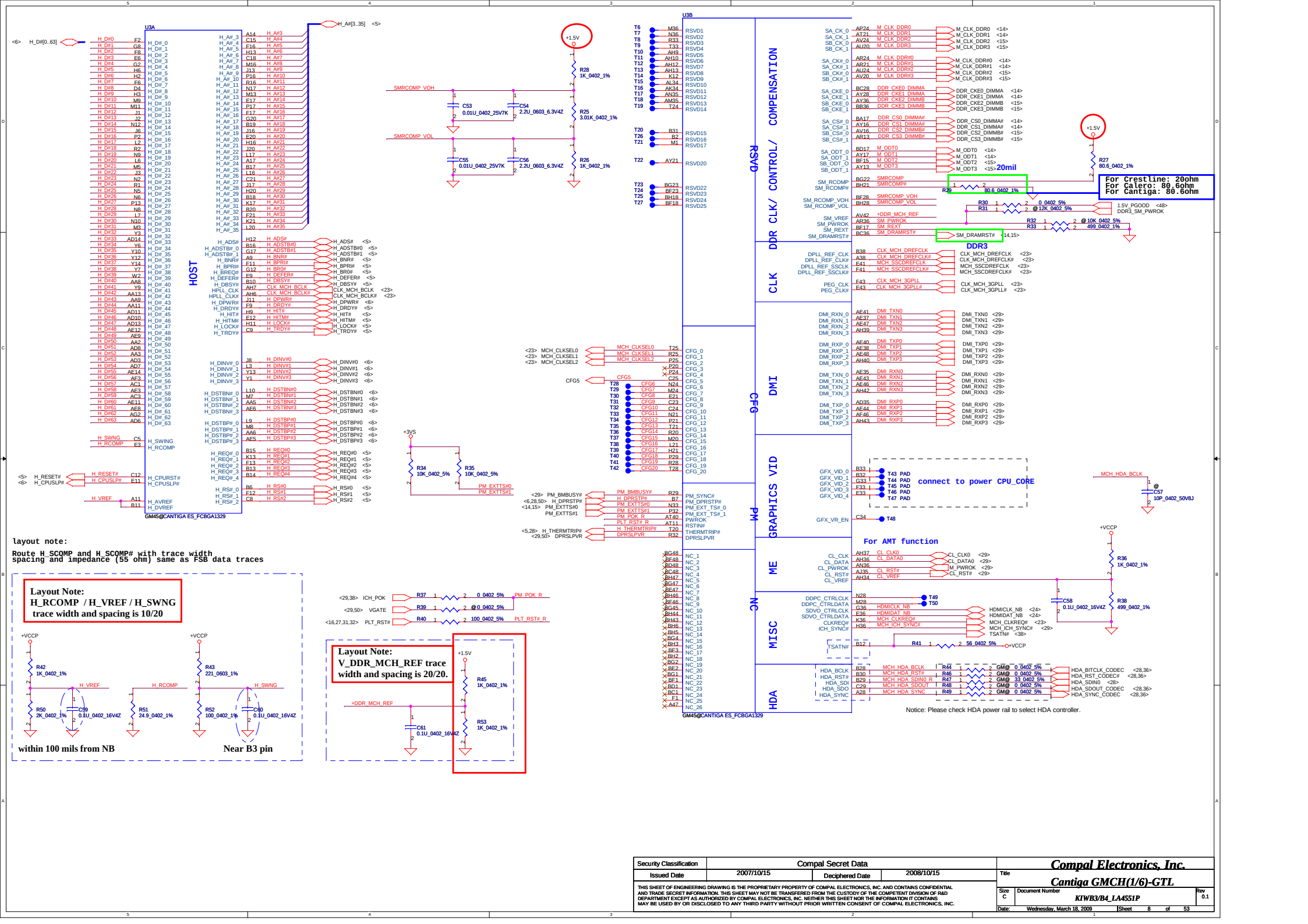
Title: **Penryn (3/3)**

Size	Document Number	Rev
B	KIW10/11_LA4142P	0.1

Date: Wednesday, March 18, 2009 Sheet 7 of 53



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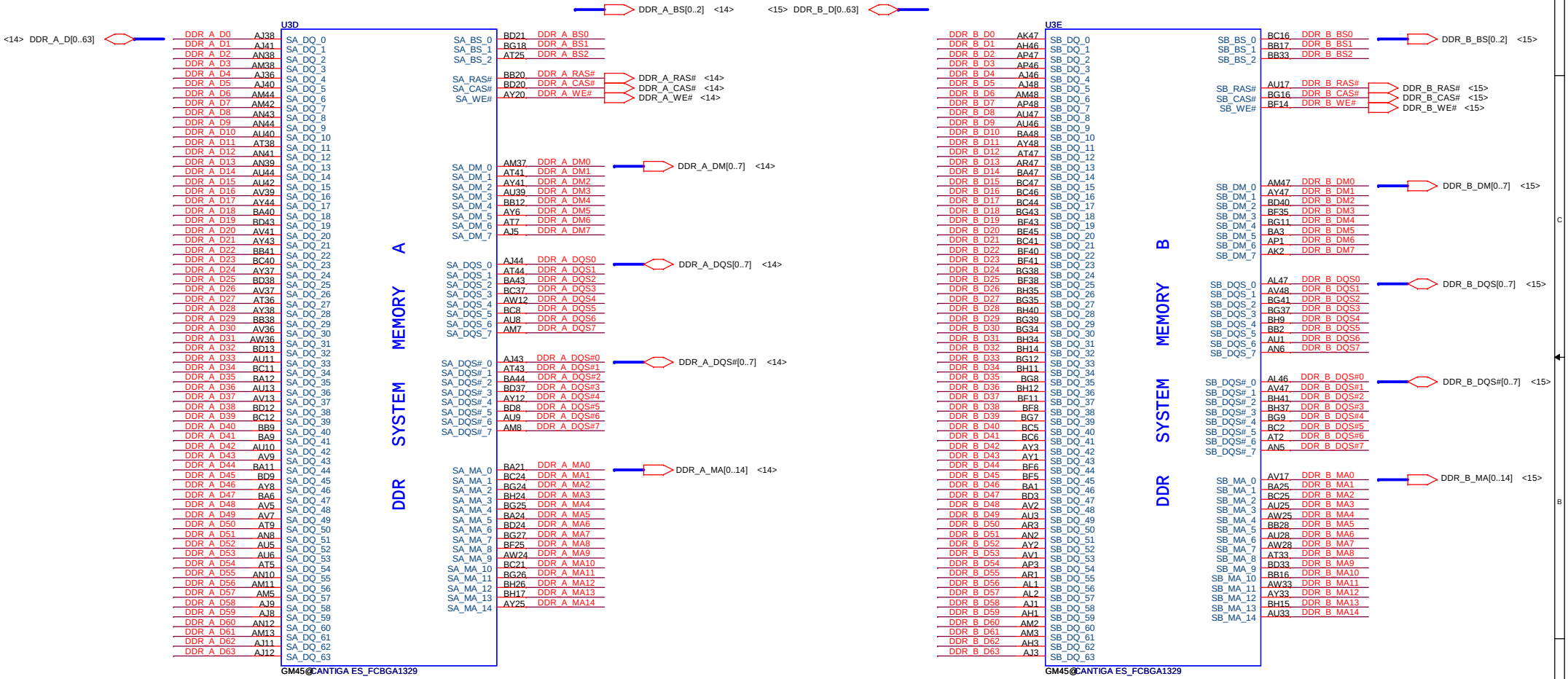
Title: Cantiga GMCH(1/6)-GTL			
Size: C	Document Number: KIWB3/B4_LA4551P		Rev: 0.1
Date: Wednesday, March 18, 2009	Sheet 8 of 53		



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Title: **Cantiga GMCH (2/6)-DDRII**

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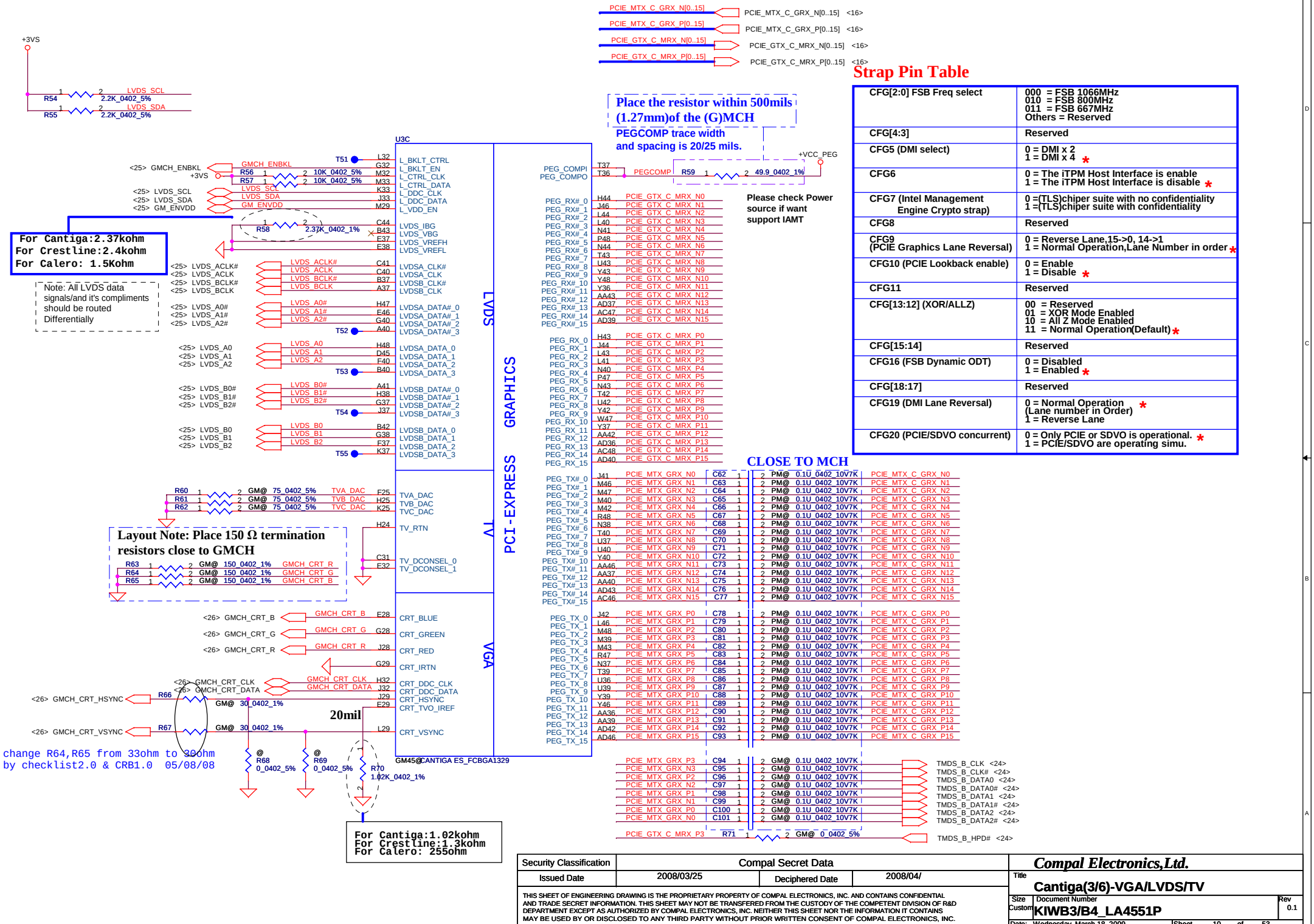
B	KIWB3/B4_LA4551P	0.1

Date: Wednesday, March 18, 2009 | Sheet 9 of 53



Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

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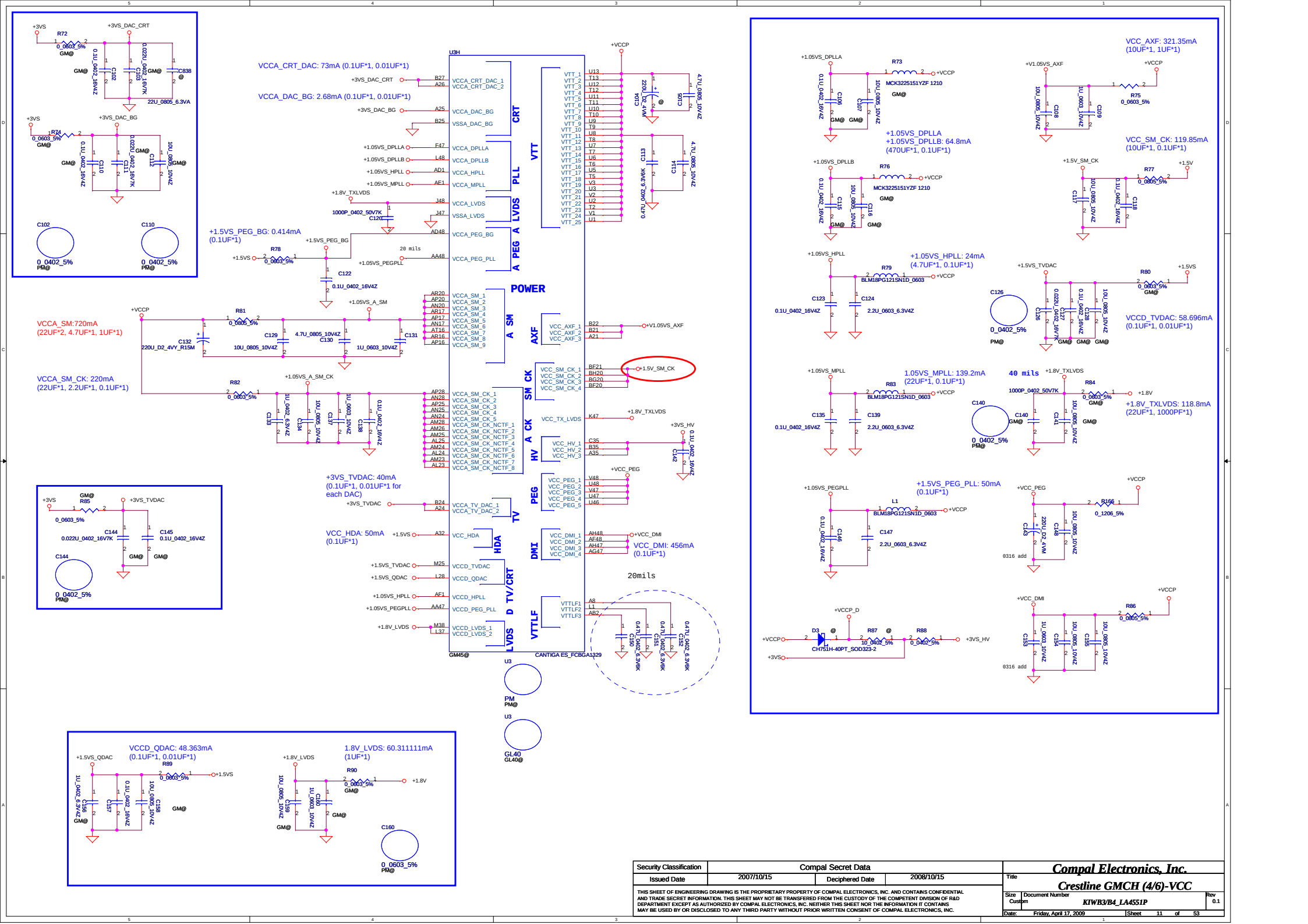
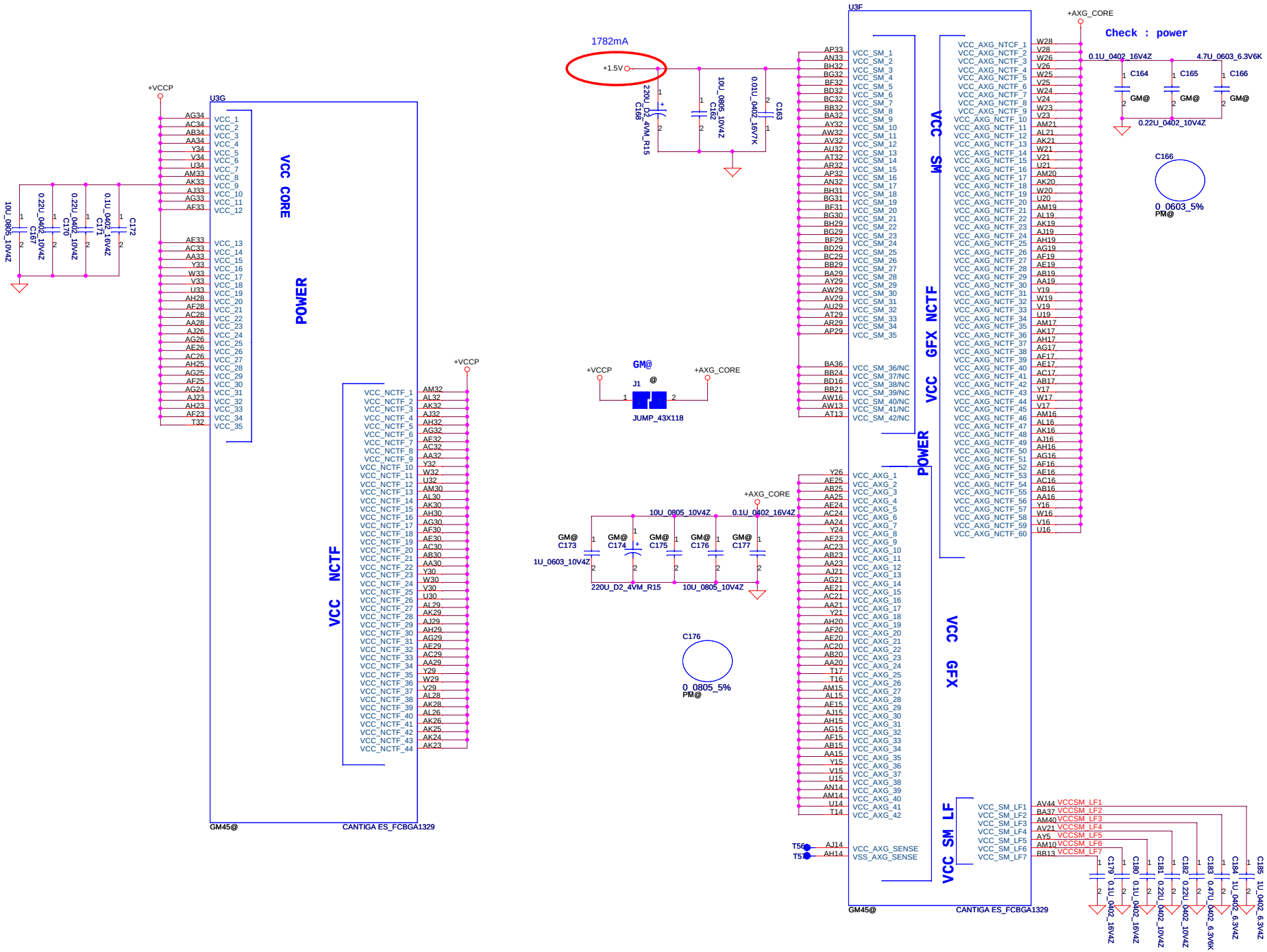
Title: Cantiga(3/6)-VGA/LVDS/TV

Size: Custom | Document Number: KIWB3/B4_LA4551P | Rev: 0.1

Date: Wednesday, March 18, 2009 | Sheet 10 of 53


VCCA_CRT_DAC: 73mA (0.1UF*1, 0.01UF*1)
VCCA_DAC_BG: 2.68mA (0.1UF*1, 0.01UF*1)
+1.5VS_PEG_BG: 0.414mA (0.1UF*1)
VCCA_SM:720mA (22UF*2, 4.7UF*1, 1UF*1)
VCCA_SM_CK: 220mA (22UF*1, 2.2UF*1, 0.1UF*1)
+3VS_TVDAC: 40mA (0.1UF*1, 0.01UF*1 for each DAC)
VCC_HDA: 50mA (0.1UF*1)
VCC_DMI: 456mA (0.1UF*1)
20mils
VCCD_QDAC: 48.363mA (0.1UF*1, 0.01UF*1)
1.8V_LVDS: 60.311111mA (1UF*1)
VCC_AXF: 321.35mA (10UF*1, 1UF*1)
+1.05VS_DPLLA
+1.05VS_DPLLB: 64.8mA (470UF*1, 0.1UF*1)
VCC_SM_CK: 119.85mA (10UF*1, 0.1UF*1)
+1.05VS_HPLL: 24mA (4.7UF*1, 0.1UF*1)
VCCD_TVDAC: 58.696mA (0.1UF*1, 0.01UF*1)
1.05VS_MPLL: 139.2mA (22UF*1, 0.1UF*1)
+1.8V_TXLVDS: 118.8mA (22UF*1, 1000PF*1)
+1.5VS_PEG_PLL: 50mA (0.1UF*1)
U3H
POWER
CRT
DAC
VTT
PLL
LVDS
A PEG
A SM
AXF
SM CK
A CK
HV
PEG
TV
HDA
DMI
D TV/CRT
VTTLF
LVDS
CANTIGA ES_FCBGA1329
GM45@
PM
GL40
Compal Electronics, Inc.
Crestline GMCH (4/6)-VCC
KIWB3/B4_LA4551P
Compal Secret Data
2007/10/15
2008/10/15
Friday, April 17, 2009
Sheet 11 of 53



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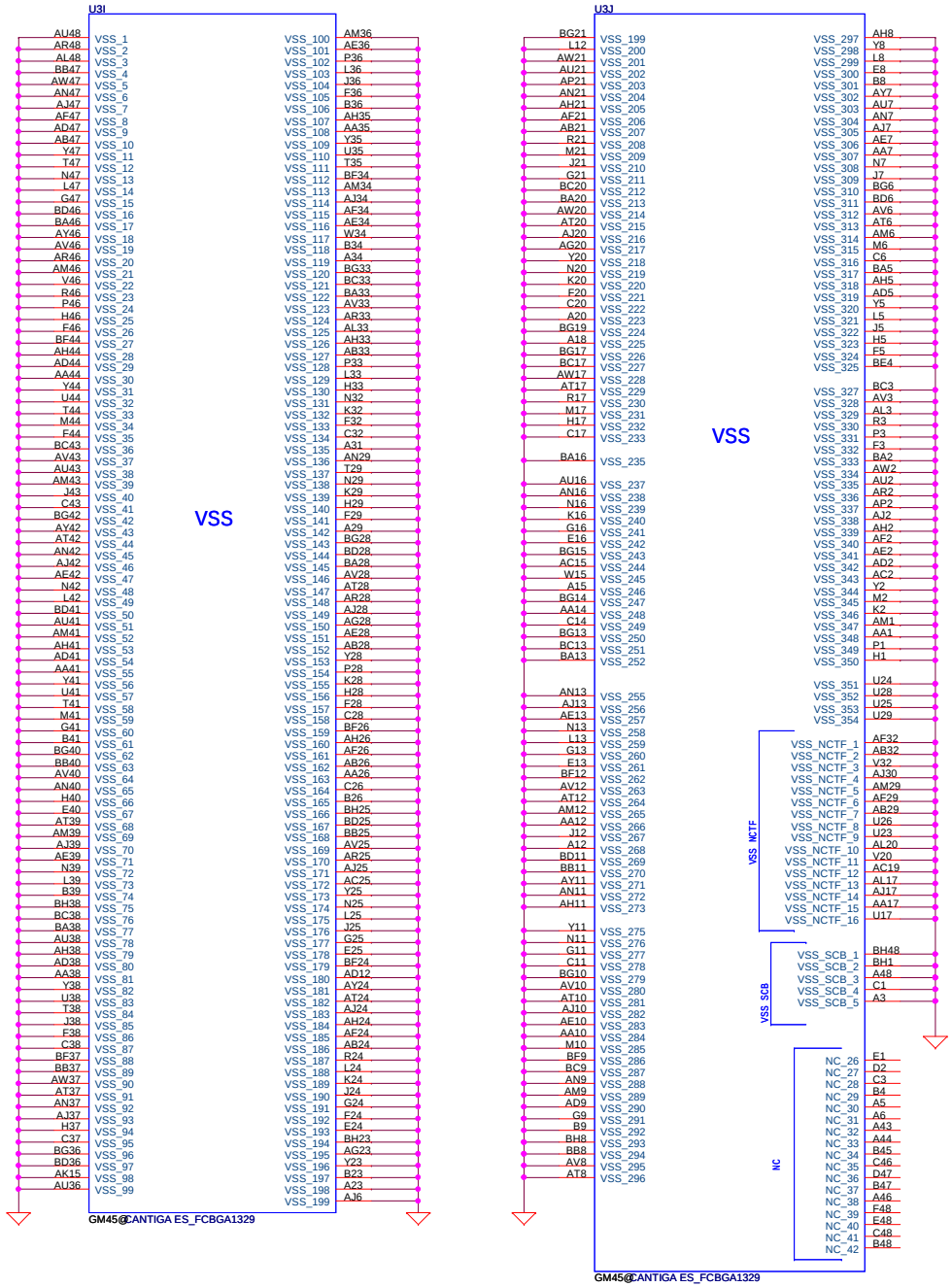
Title: **Crestline GMCH (5/6)-VCC**

Size	Document Number	Rev
Custom	KIWB3/B4_LA4551P	0.1

Date: Wednesday, March 18, 2009 | Sheet 12 of 53



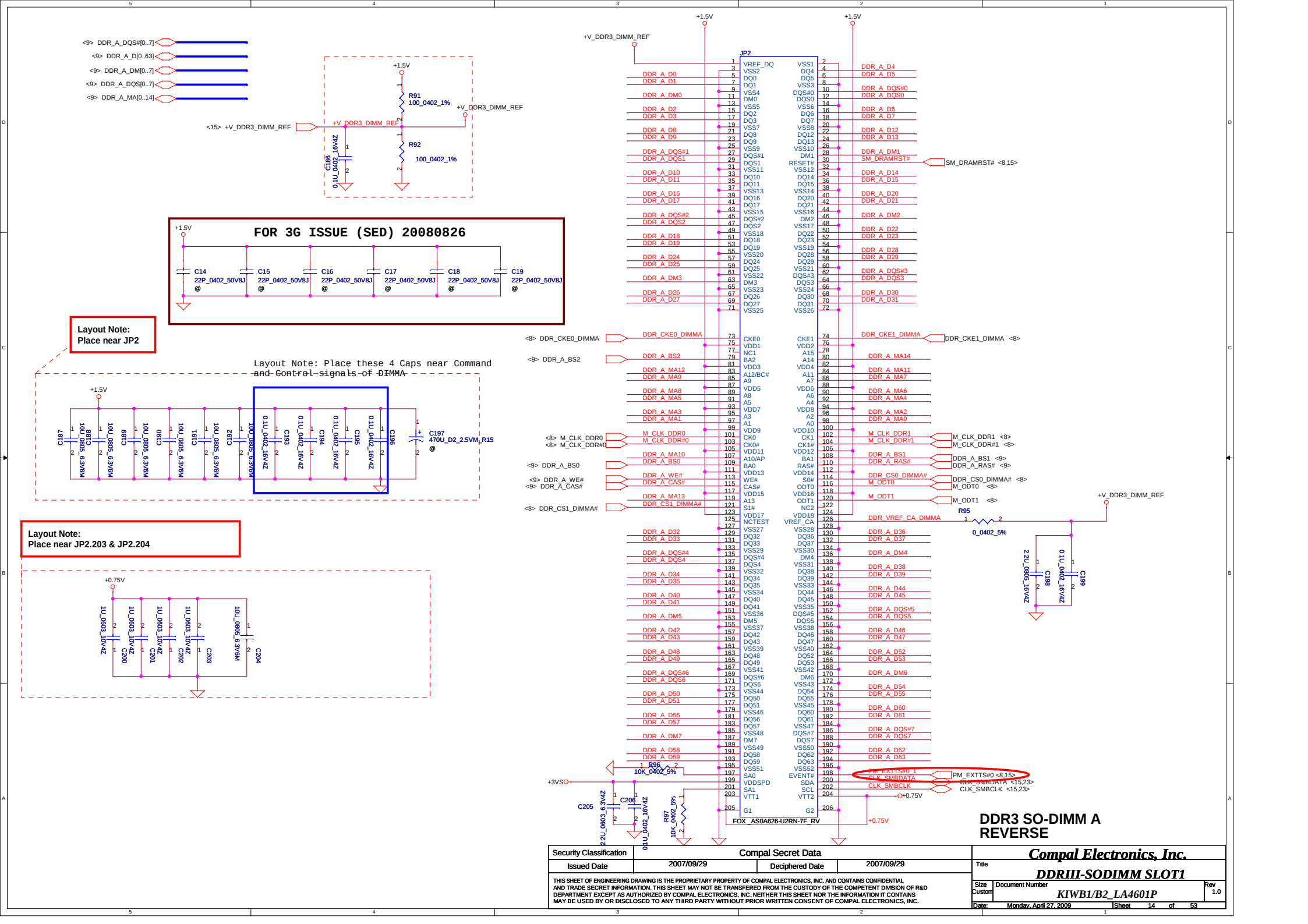
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

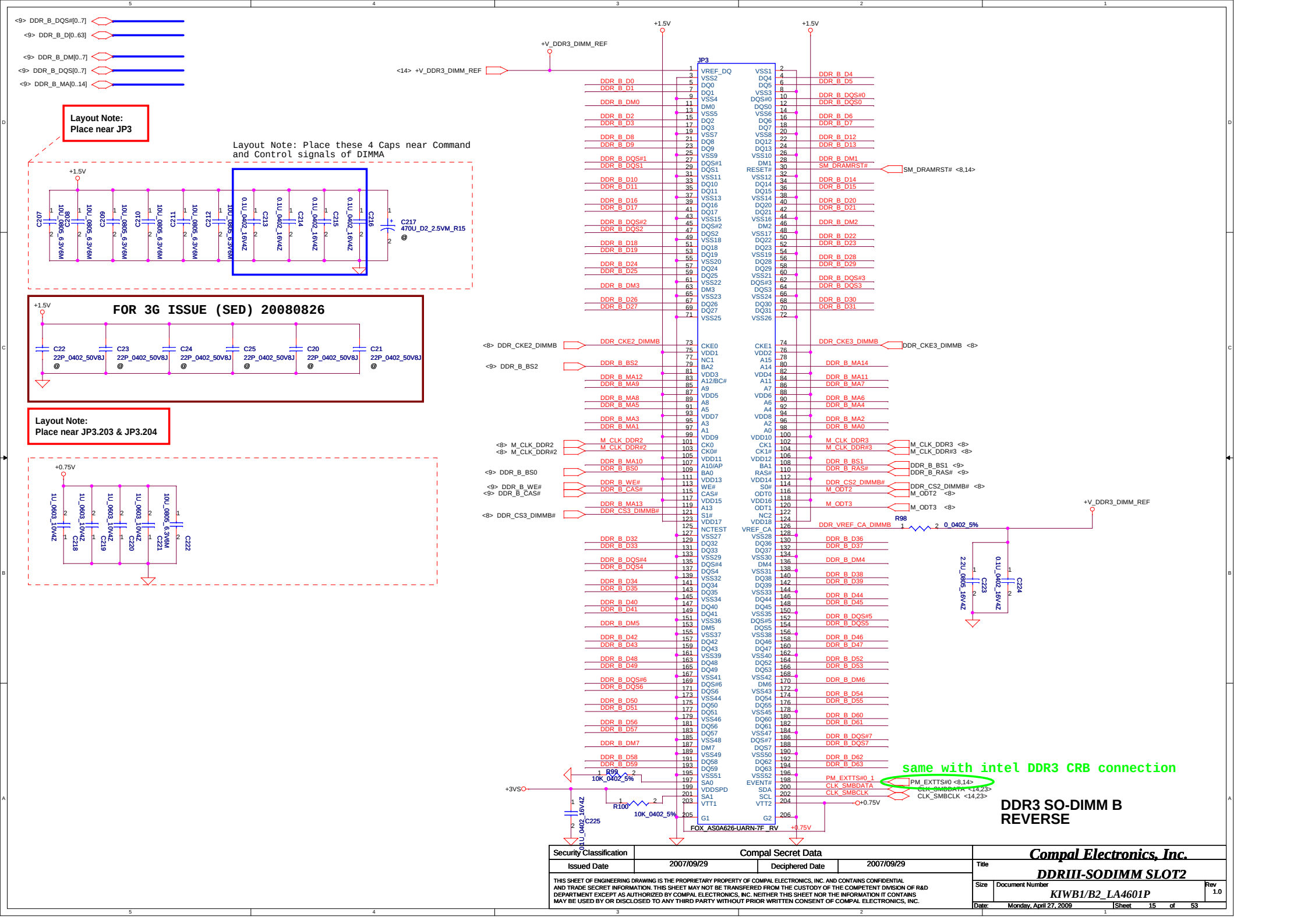
Compal Electronics, Inc.

Title: **Cantiga GMCH (6/6)-GND**

Size	Document Number	Rev
Custom	KIWB3/B4_LA4551P	0.1

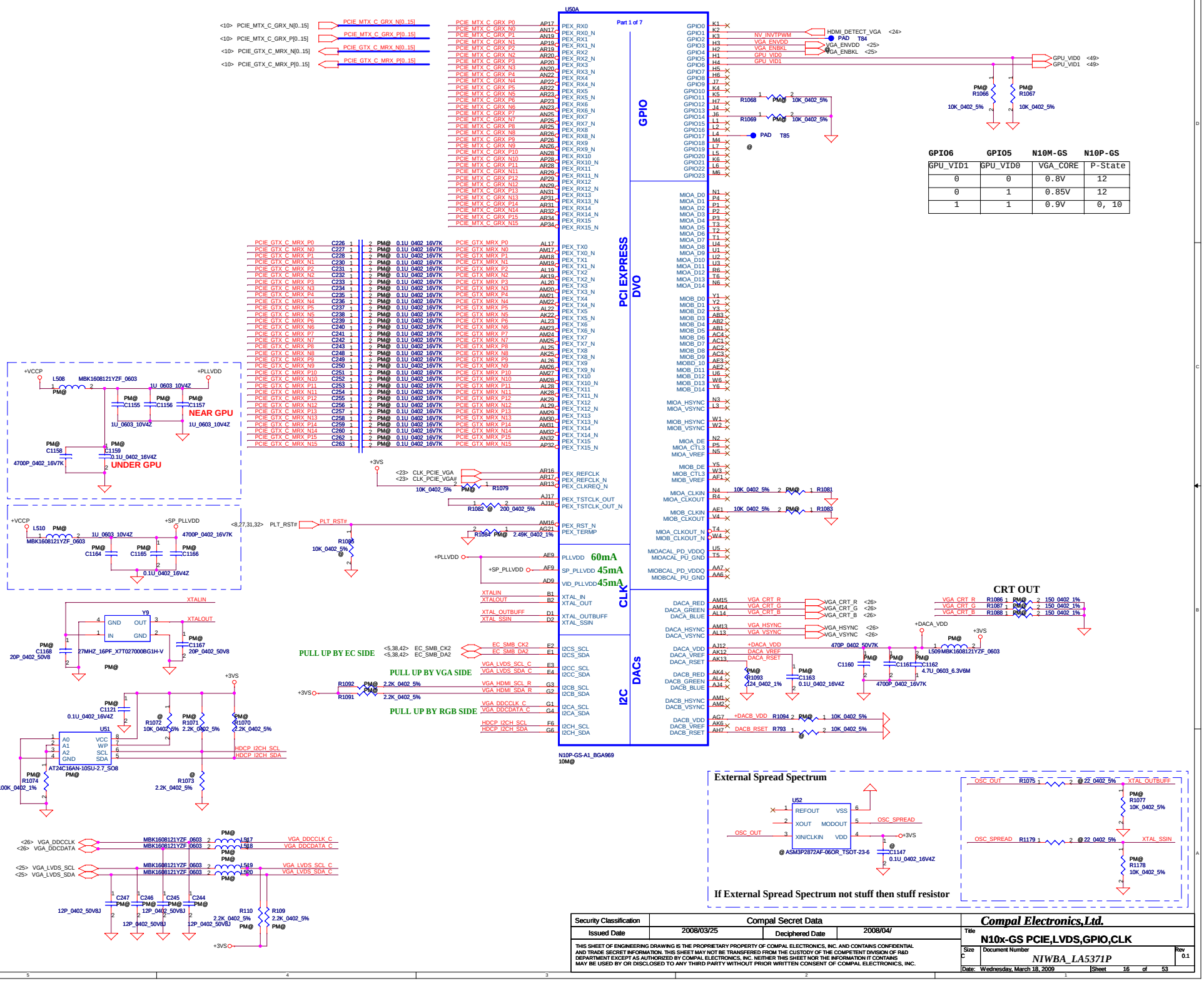
Date: Wednesday, March 18, 2009 | Sheet 13 of 53


FOR 3G ISSUE (SED) 20080826
Layout Note: Place near JP2
Layout Note: Place these 4 Caps near Command and Control signals of DIMMA
Layout Note: Place near JP2.203 & JP2.204
JP2
FOX_AS0A626-U2RN-7F_RV
DDR3 SO-DIMM A REVERSE
Compal Electronics, Inc.
DDRIII-SODIMM SLOT1
KIWB1/B2_LA4601P
Compal Secret Data
2007/09/29
2007/09/29
Monday, April 27, 2009
Sheet 14 of 53



Security Classification	Compal Secret Data		
Issued Date	2007/09/29	Deciphered Date	2007/09/29

Compal Electronics, Inc.			
Title	DDRIII-SODIMM SLOT2		
Size	Document Number	KIWB1/B2_LA4601P	Rev 1.0
Date: Monday, April 27, 2009	Sheet 15 of 53		



Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

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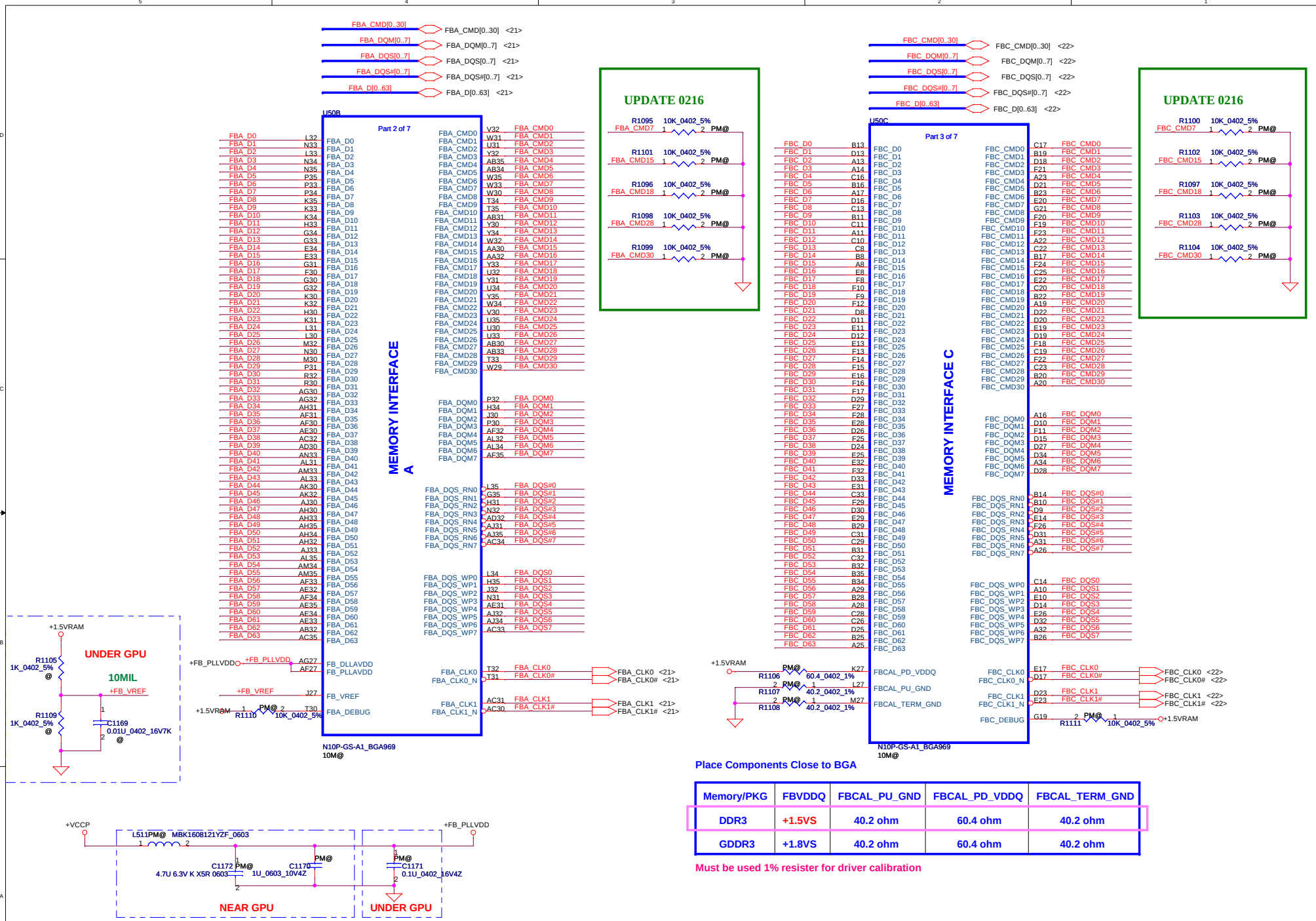
Compal Electronics,Ltd.

Title: N10x-GS PCIE,LVDS,GPIO,CLK

Size	Document Number	Rev
C	NIWBA_LA5371P	0.1

Date: Wednesday, March 18, 2009 Sheet 16 of 53



Place Components Close to BGA

Memory/PKG	FBVDDQ	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
DDR3	+1.5VS	40.2 ohm	60.4 ohm	40.2 ohm
GDDR3	+1.8VS	40.2 ohm	60.4 ohm	40.2 ohm

Must be used 1% resister for driver calibration

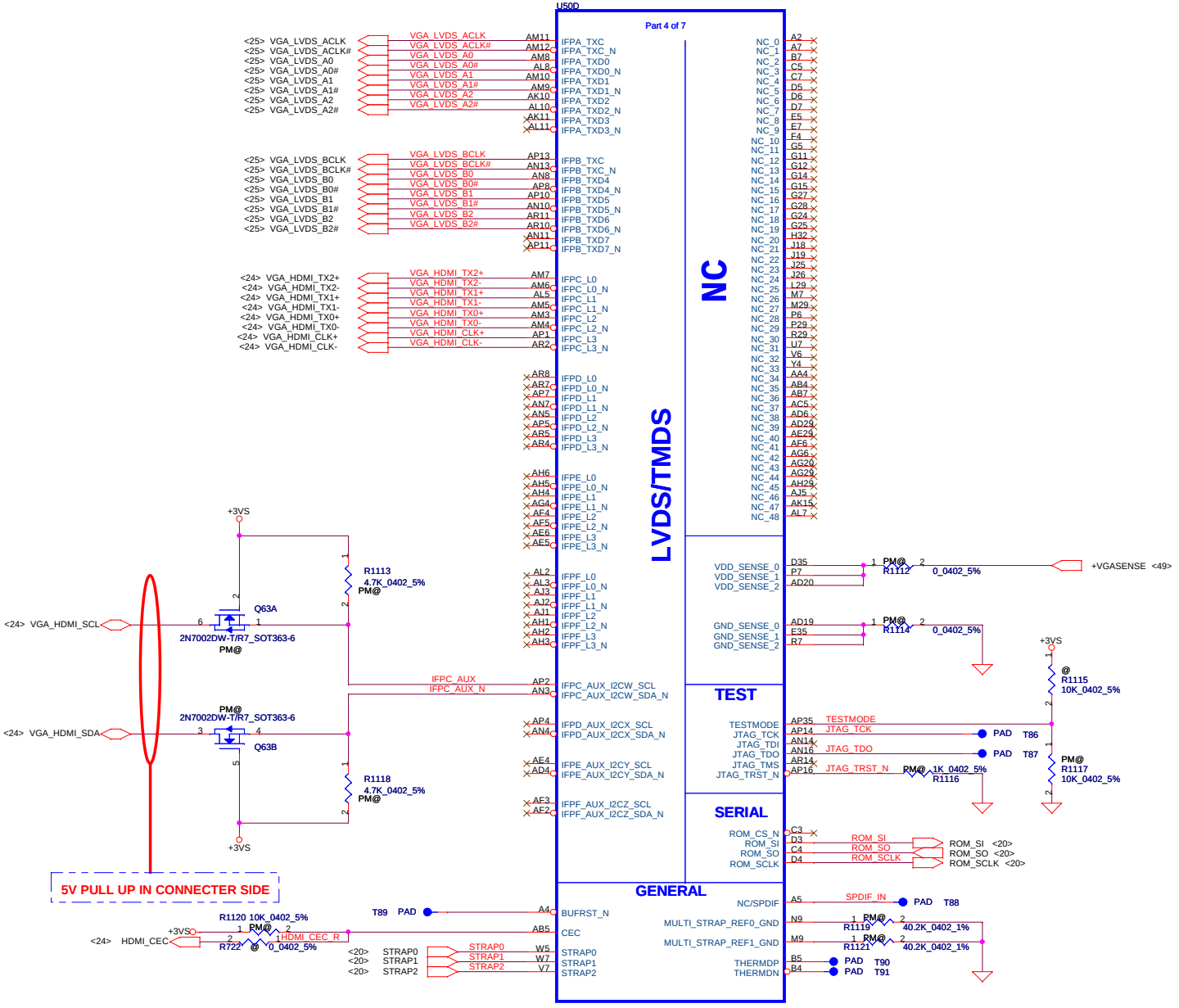
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: N10x-GS Memory

Size: Custom | Document Number: NIWBA_LA5371P | Rev: 0.1

Date: Wednesday, March 18, 2009 | Sheet 17 of 53



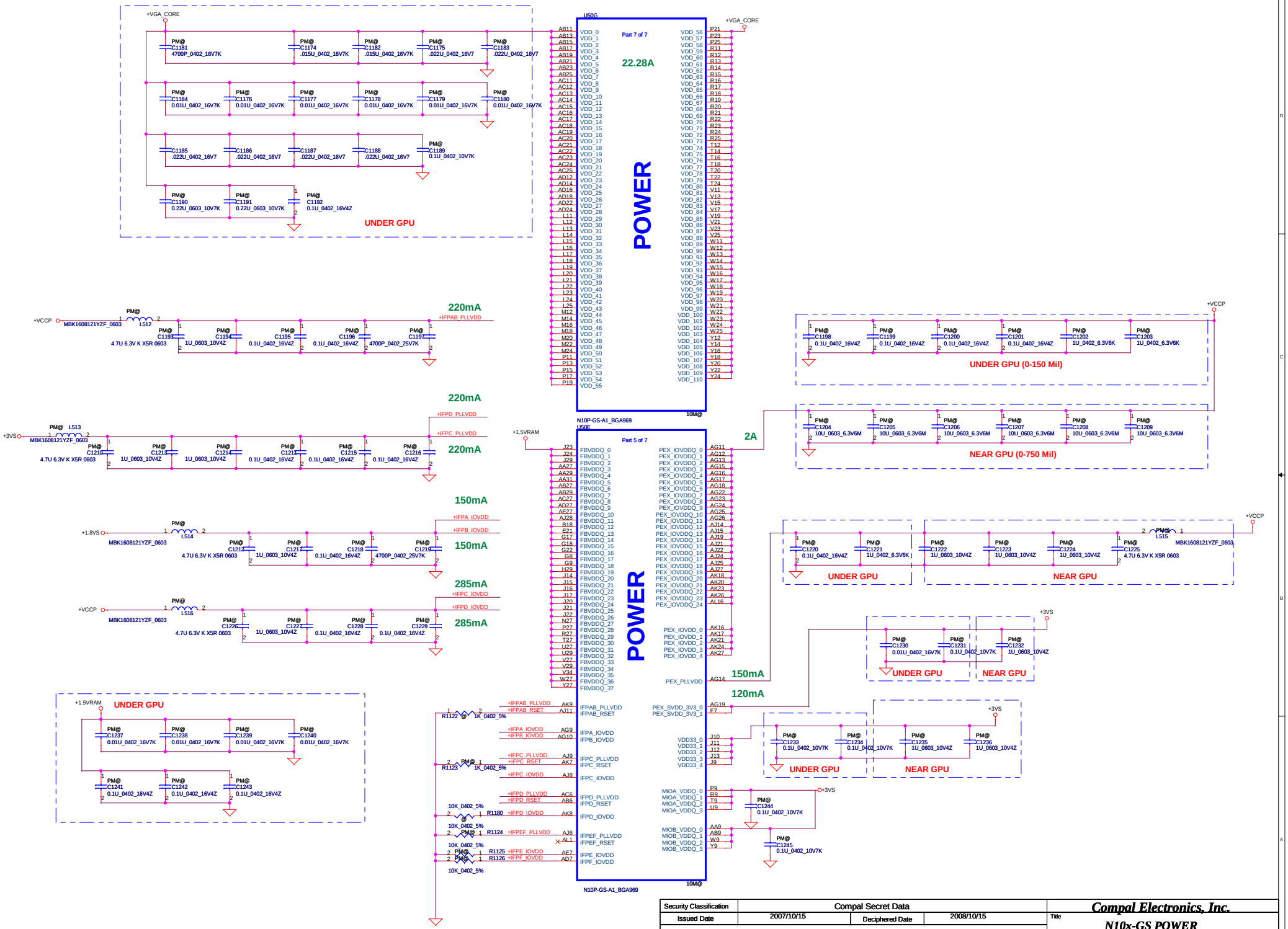
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **N10P/N10M LVDS,HDMI**

Size	Document Number	Rev
Custom	NIWBA_LA5371P	0.1

Date: Wednesday, March 18, 2009 | Sheet 18 of 53



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

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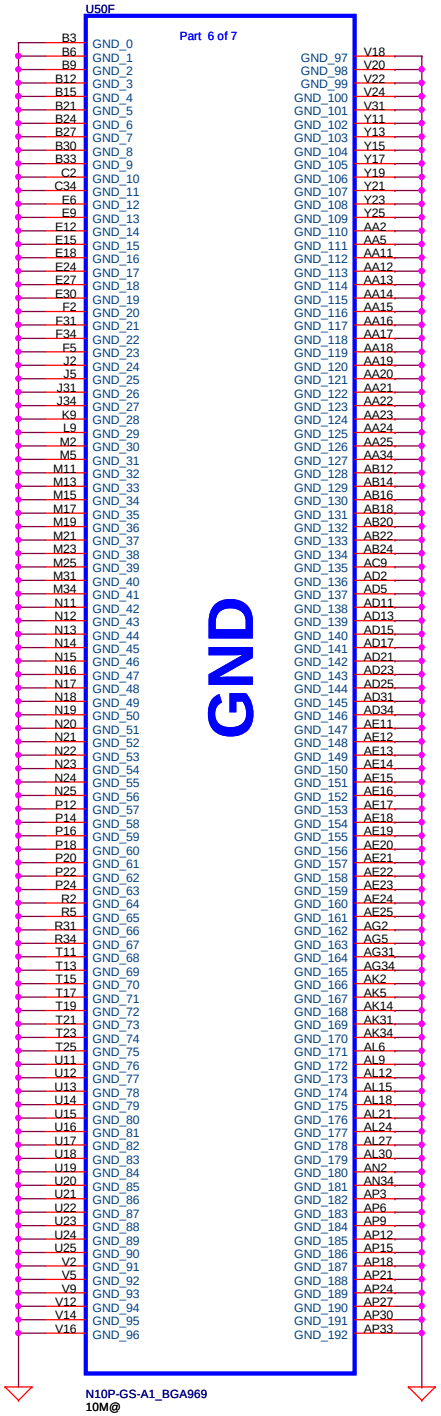
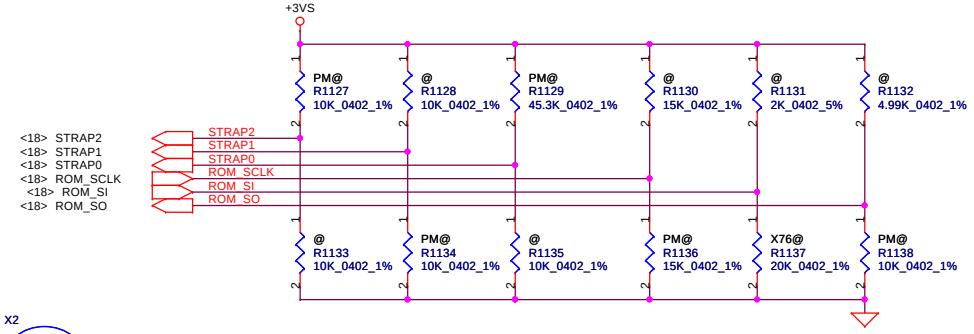
Compal Electronics, Inc.

Title: **N10x-GS POWER**

Size	Document Number	Rev
C	NIWBA_LA5371P	0.1

Date: Wednesday, April 22, 2009 Sheet 19 of 53





X2 S1024@ X76_S1024

X3 H1024@ X76_H1024

X4 S512@ X76_S512

X5 H512@ X76_H512

U50 N10P-GS 10P@

GB1 Family GPU Strap Qptions

GPU	FB Memory		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N10P-GS (0xA34)	Samsung	64Mx16	PD 10K	PD 15K	PD 20K	PU 10K	PD 10K	PU 45K
	Hynix	64Mx16	PD 10K	PD 15K	PD 15K	PU 10K	PD 10K	PU 45K

GPU	FB Memory		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N10M-GS (0xA74)	Samsung	64Mx16	PD 10K	PD 15K	PD 20K	PU 10K	PD 10K	PU 45K
	Hynix	64Mx16	PD 10K	PD 15K	PD 15K	PU 10K	PD 10K	PU 45K

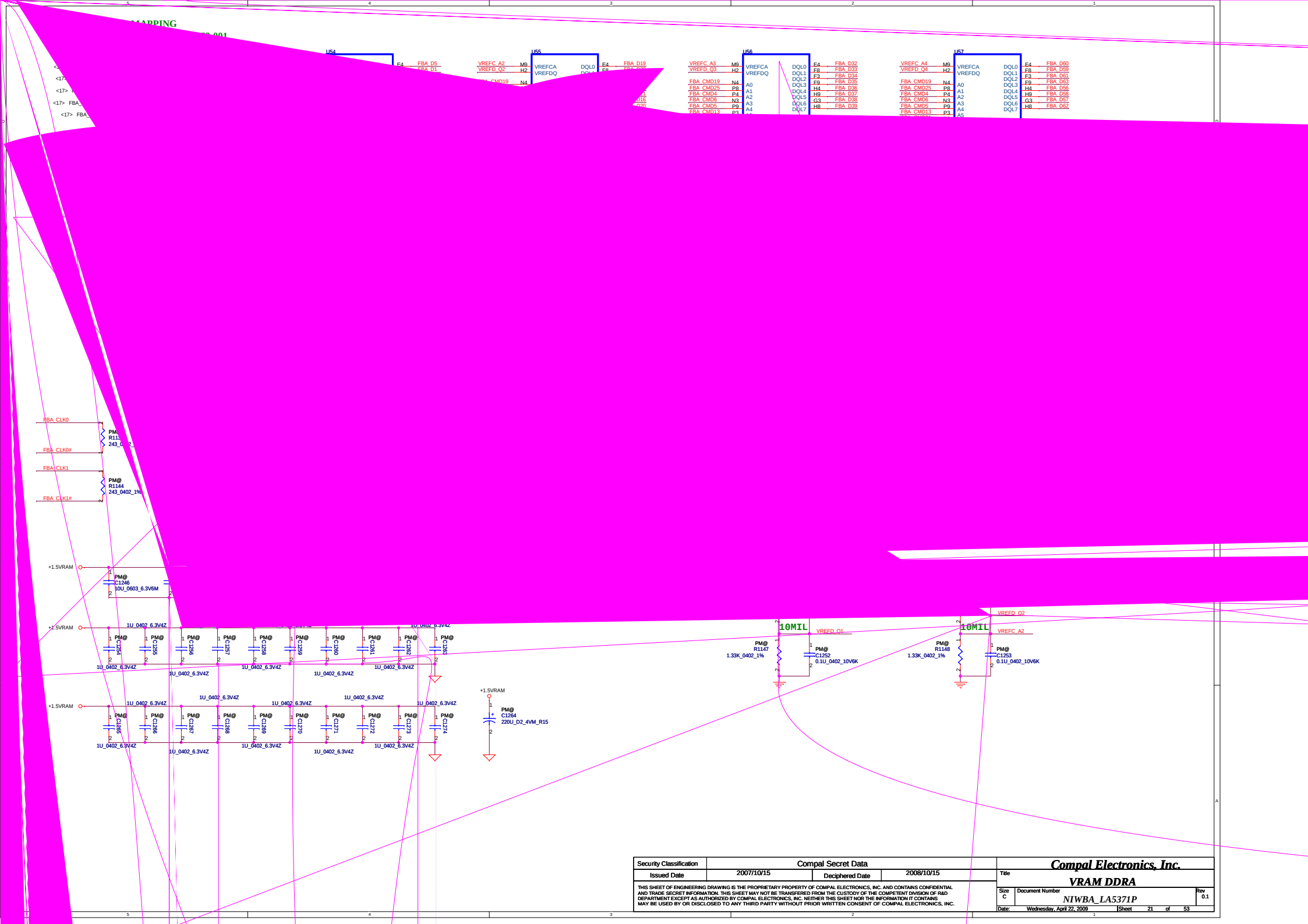
Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

Title: N10x-GS GND & STRAP

Size: Custom | Document Number: NIWBA_LA5371P | Rev: 0.1

Date: Wednesday, March 18, 2009 | Sheet 20 of 53



Compal Electronics, Inc.

Title: VRAM DDRA

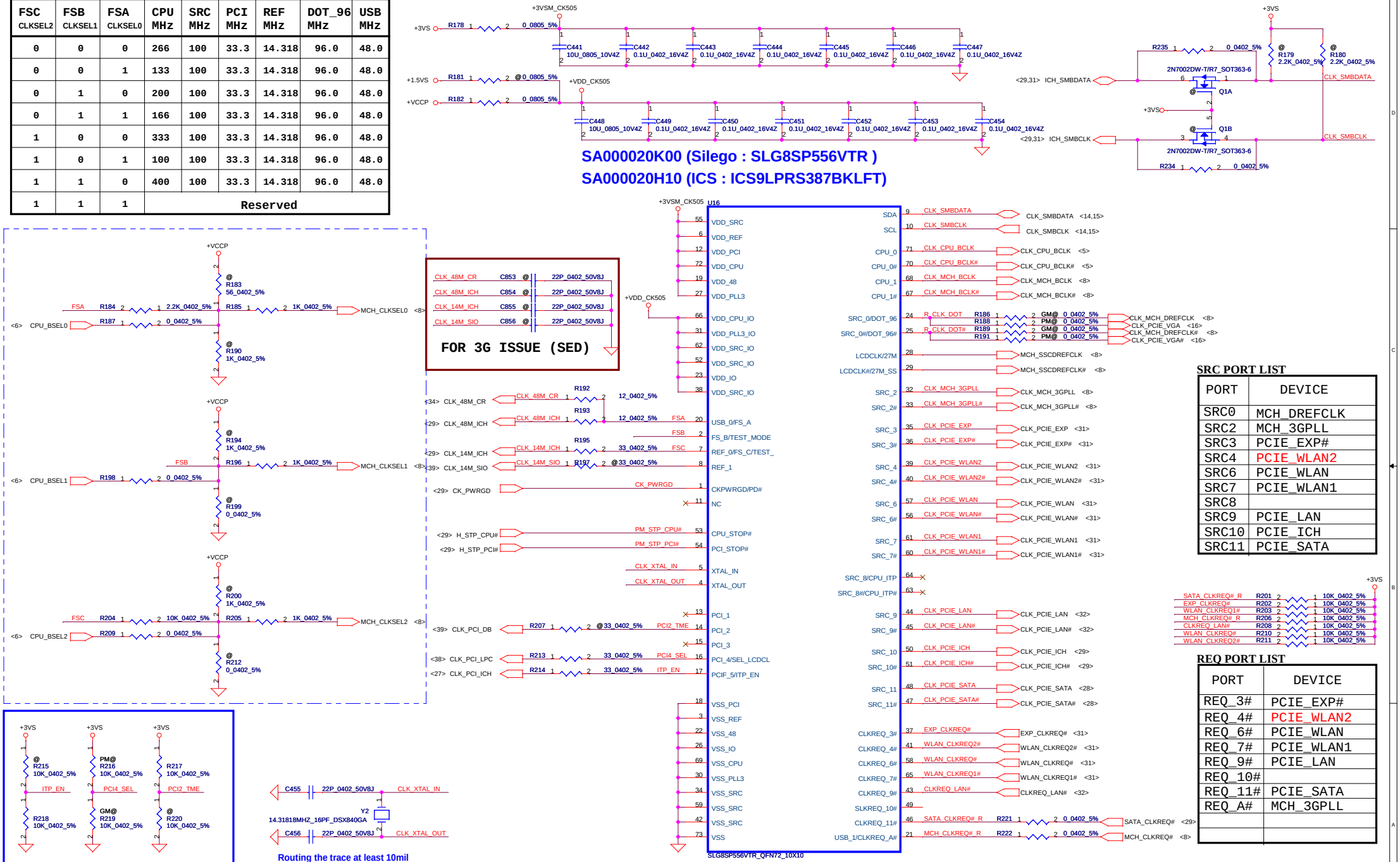
Size	Document Number	Rev
C	NIWBA_LA5371P	0.1

Date: Wednesday, April 22, 2009 | Sheet 21 of 53

FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

SA000020K00 (Silego : SLG8SP556VTR)

SA000020H10 (ICS : ICS9LPRS387BKLFT)



SRC PORT LIST

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	PCIE_EXP#
SRC4	PCIE_WLAN2
SRC6	PCIE_WLAN
SRC7	PCIE_WLAN1
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA

REQ PORT LIST

PORT	DEVICE
REQ_3#	PCIE_EXP#
REQ_4#	PCIE_WLAN2
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL

Routing the trace at least 10mil

For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#

For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS

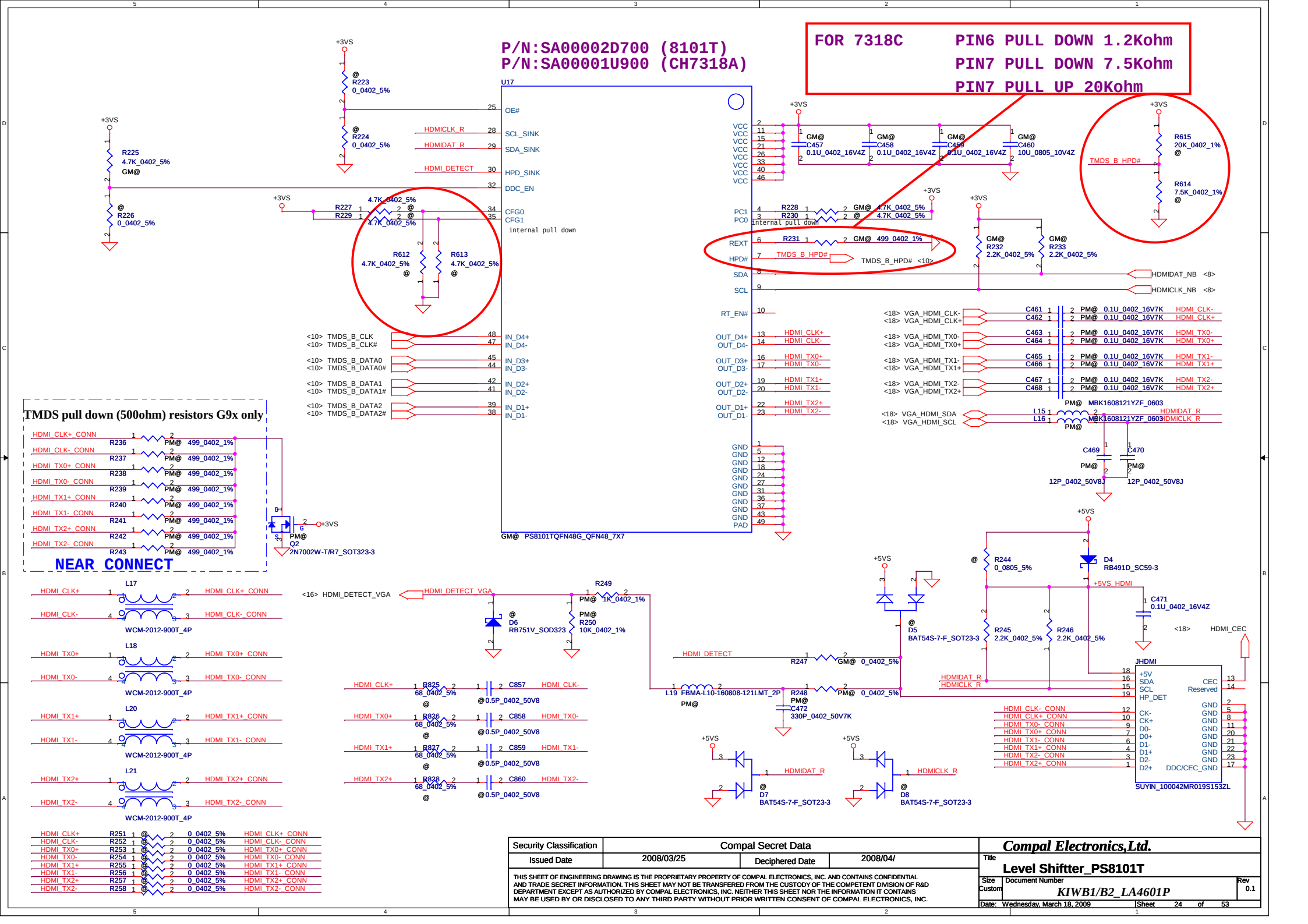
Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

Title: Clock Generator CK505

Size: Custom | Document Number: KIWB3/B4_LA4551P | Rev: 0.1

Date: Wednesday, March 18, 2009 | Sheet 23 of 53


P/N:SA00002D700 (8101T)
P/N:SA00001U900 (CH7318A)
FOR 7318C
PIN6 PULL DOWN 1.2Kohm
PIN7 PULL DOWN 7.5Kohm
PIN7 PULL UP 20Kohm
U17
GM@ PS8101TQFN48G_QFN48_7X7
TMDS pull down (500ohm) resistors G9x only
NEAR CONNECT
2N7002W-T/R7_SOT323-3
WCM-2012-900T_4P
SUYIN_100042MR019S153ZL
JHDMI
BAT54S-7-F_SOT23-3
RB491D_SC59-3
RB751V_SOD323
MBK1608121YZF_0603
FBMA-L10-160808-121LMT_2P
internal pull down
TMDS_B_HPD#
HDMIDAT_NB
HDMICLK_NB
HDMI_DETECT_VGA
HDMI_CEC
Security Classification
Compal Secret Data
Issued Date
2008/03/25
Deciphered Date
2008/04/
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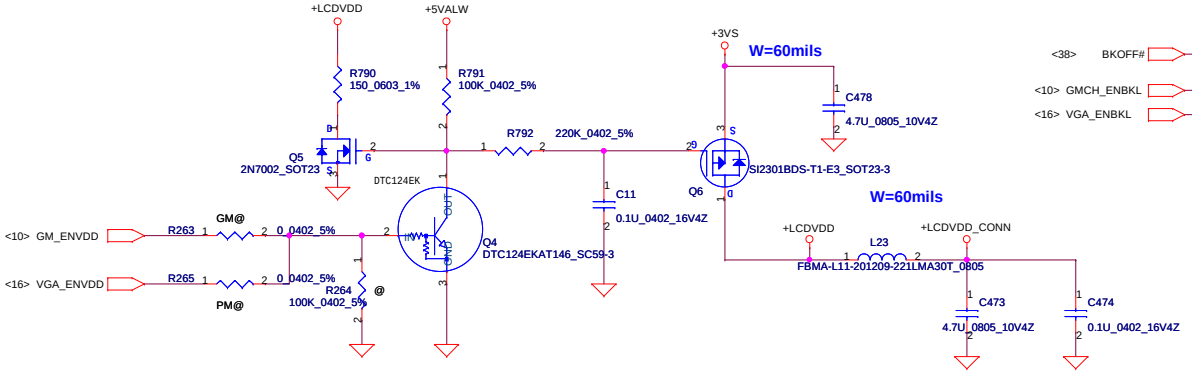
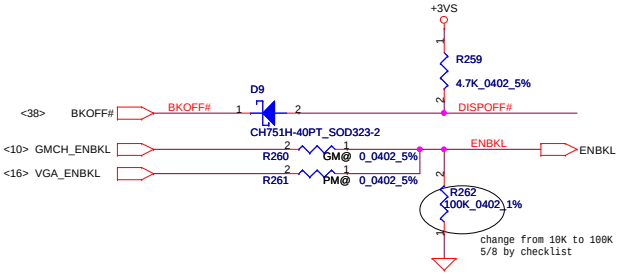
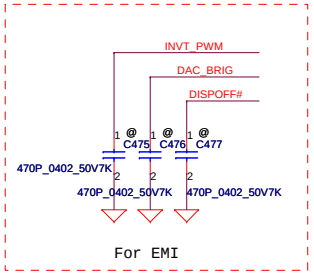
Compal Electronics,Ltd.
Title
Level Shiftter_PS8101T
Size
Custom
Document Number
KIWB1/B2_LA4601P
Rev
0.1
Date: Wednesday, March 18, 2009
Sheet 24 of 53

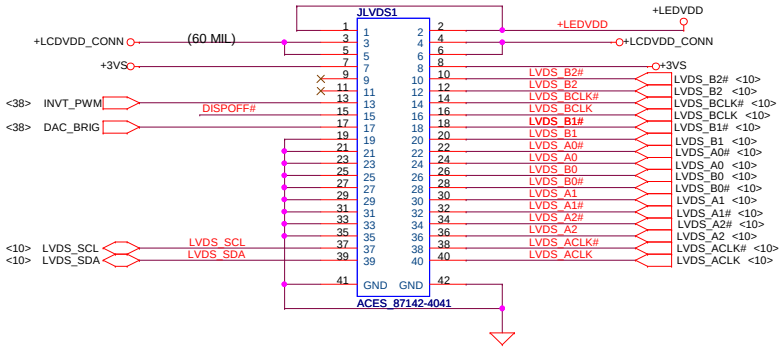
LCD POWER CIRCUIT



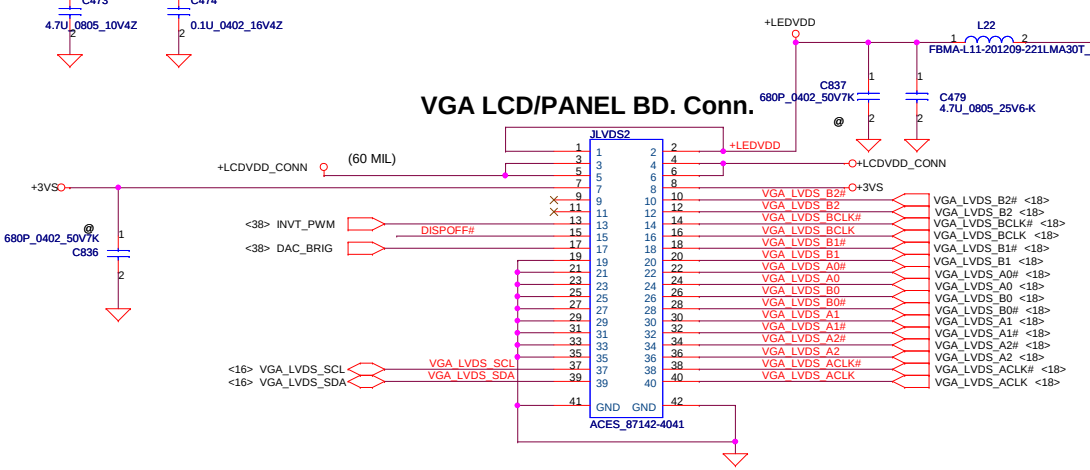


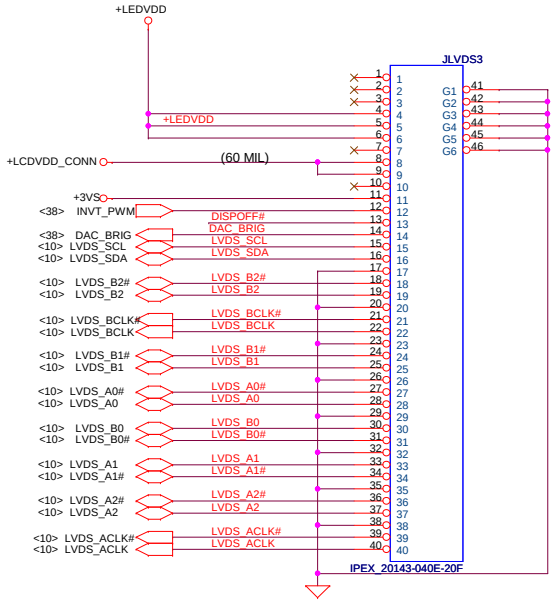


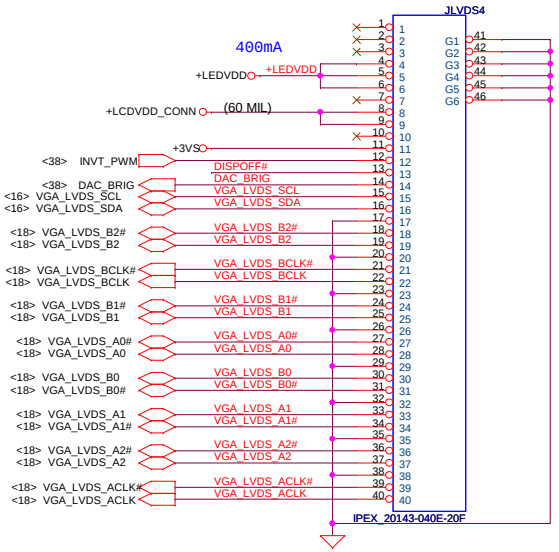
UMA LCD/PANEL BD. Conn.



VGA LCD/PANEL BD. Conn.







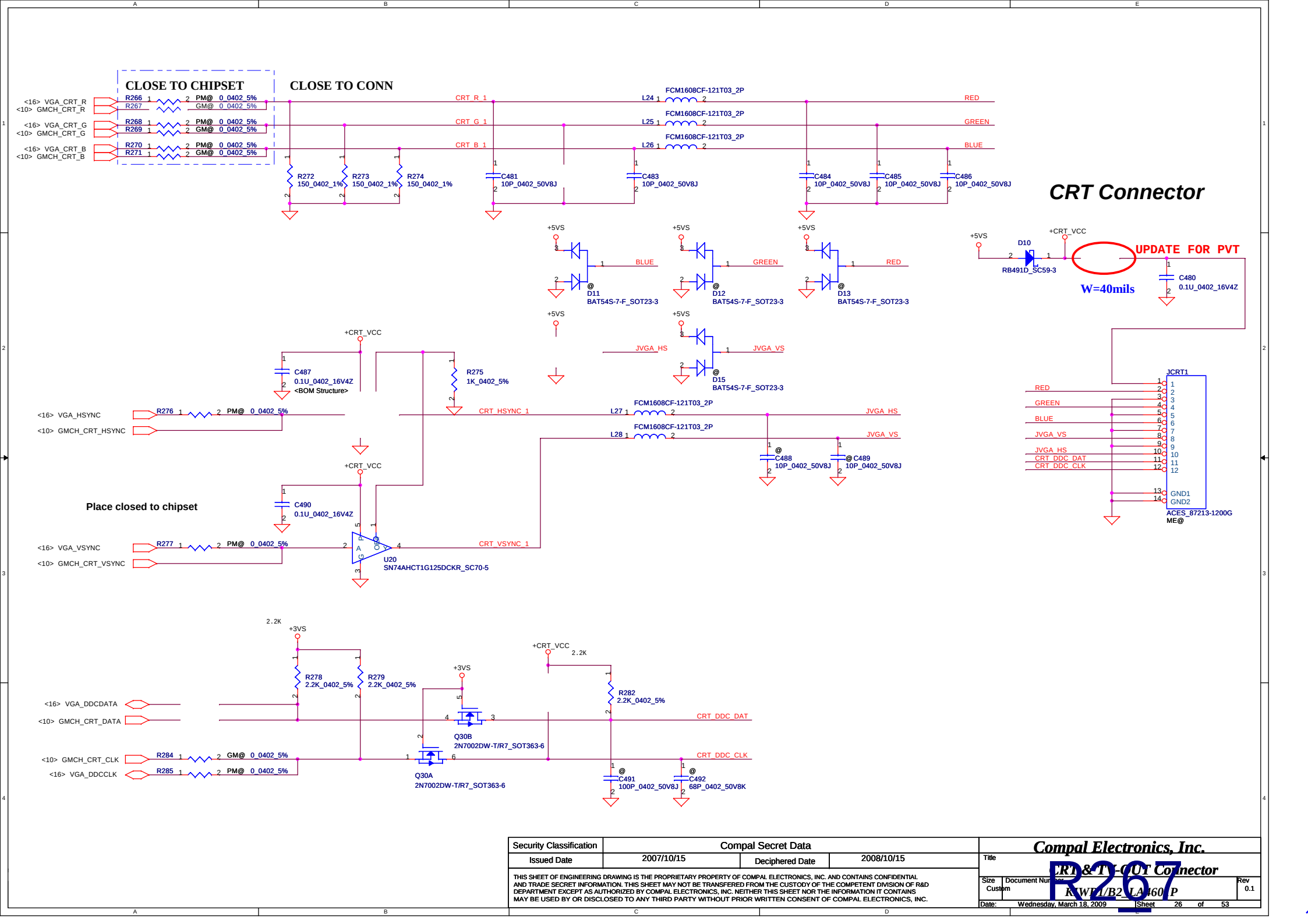
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **LVDS & DVI Connector**

Size	Document Number	Rev
B	KIWB1/B2_LA4601P	0.1

Date: Wednesday, March 18, 2009 | Sheet 25 of 53



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

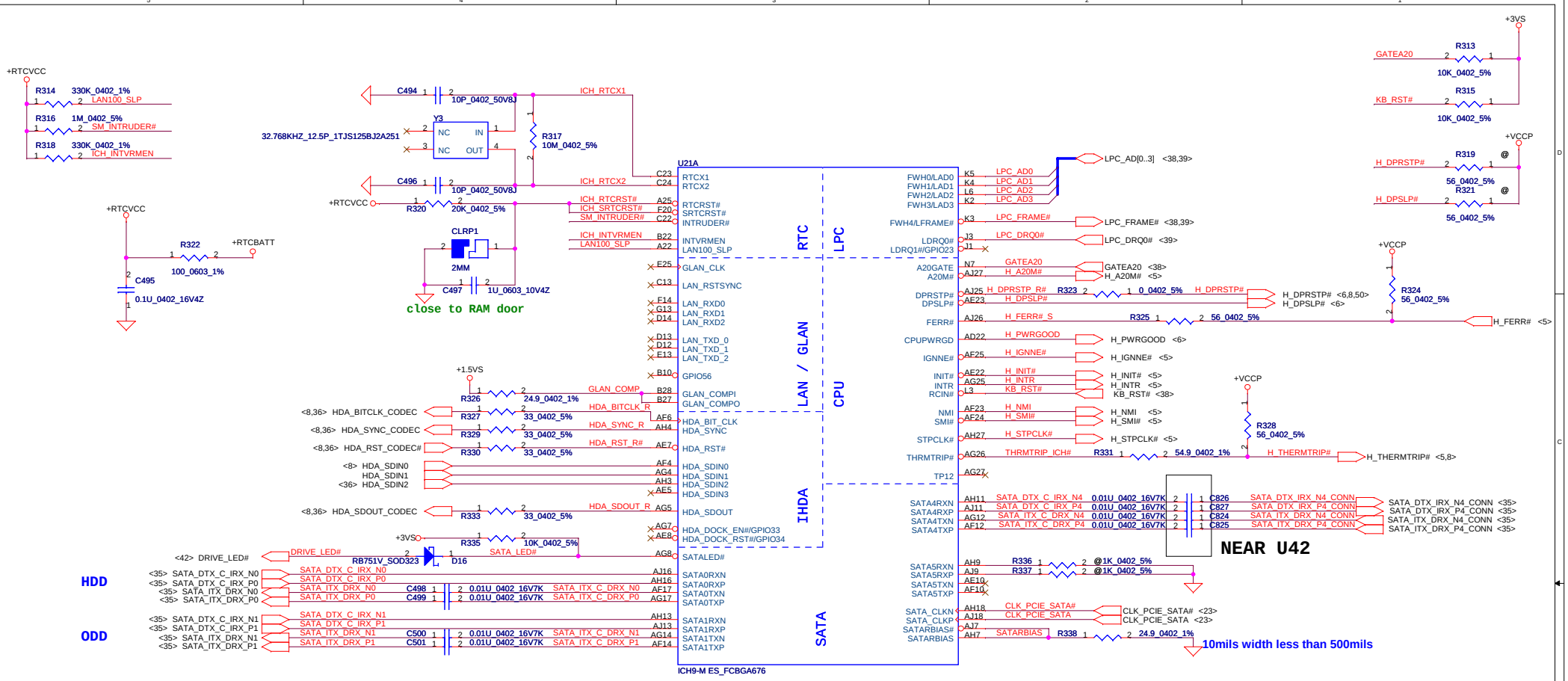
Compal Electronics, Inc.

Title: CRT & TV-OUT Connector

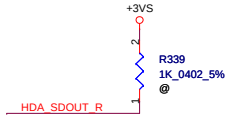
Size	Document Number	Rev
Custom	KWF1/B2_LA-4601P	0.1

Date: Wednesday, March 18, 2009 Sheet 26 of 53

R267



Need check



XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

SATA PORT LIST

PORT	DEVICE
0	HDD
1	ODD
2	X
3	X
4	ESATA
5	X

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

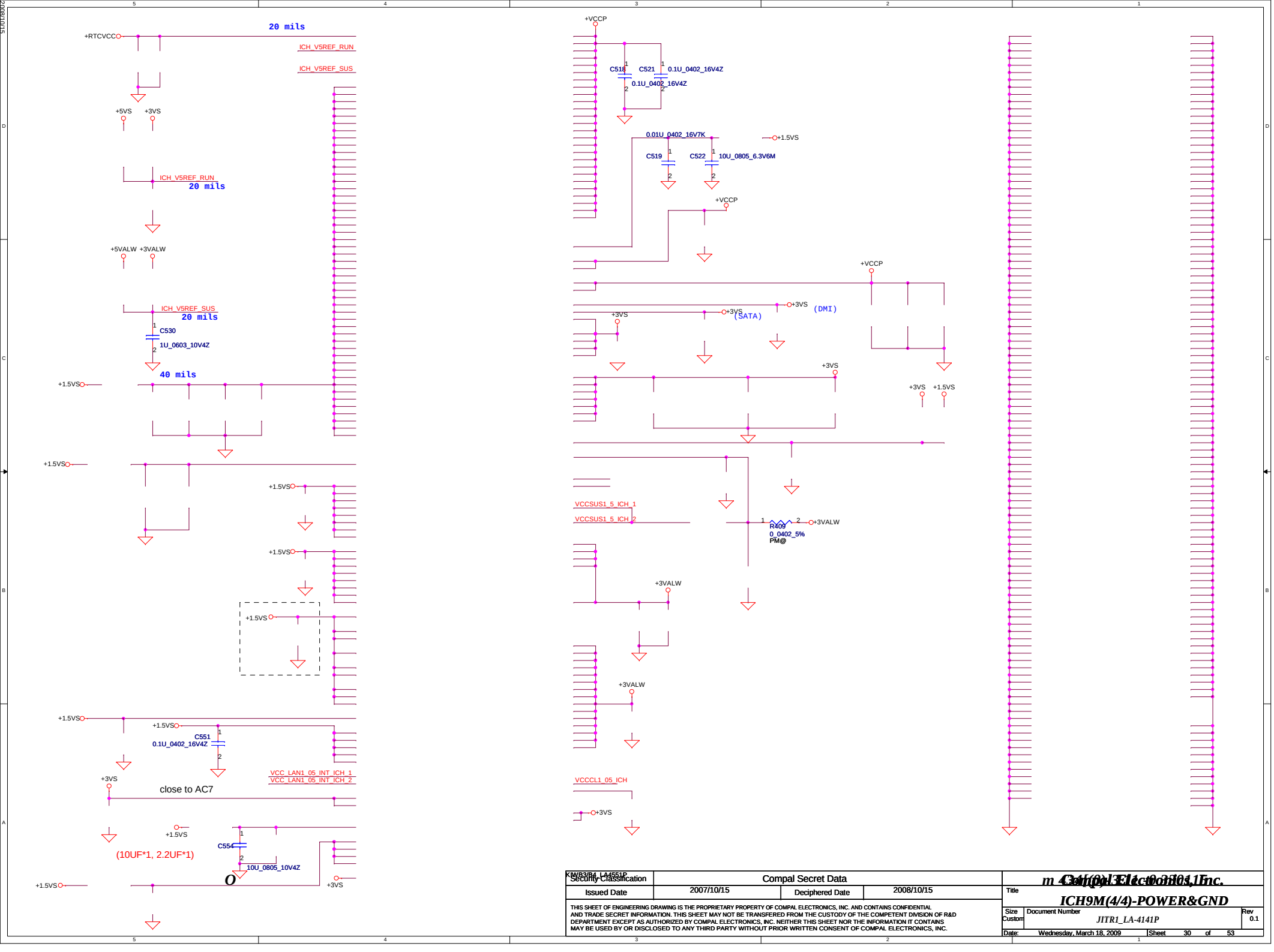
Title: ICH9M(2/4)-LAN,IDELPC,RTC

Size	Document Number	Rev
Custom	JITR1_LA-4141P	0.1

Date: Wednesday, March 18, 2009 Sheet 28 of 53

Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	

Title	ICH9M(3/4)-USB,GPIO,PCIE		
Size	Document Number		Rev
		a	0.1
Date:		Sheet	of



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

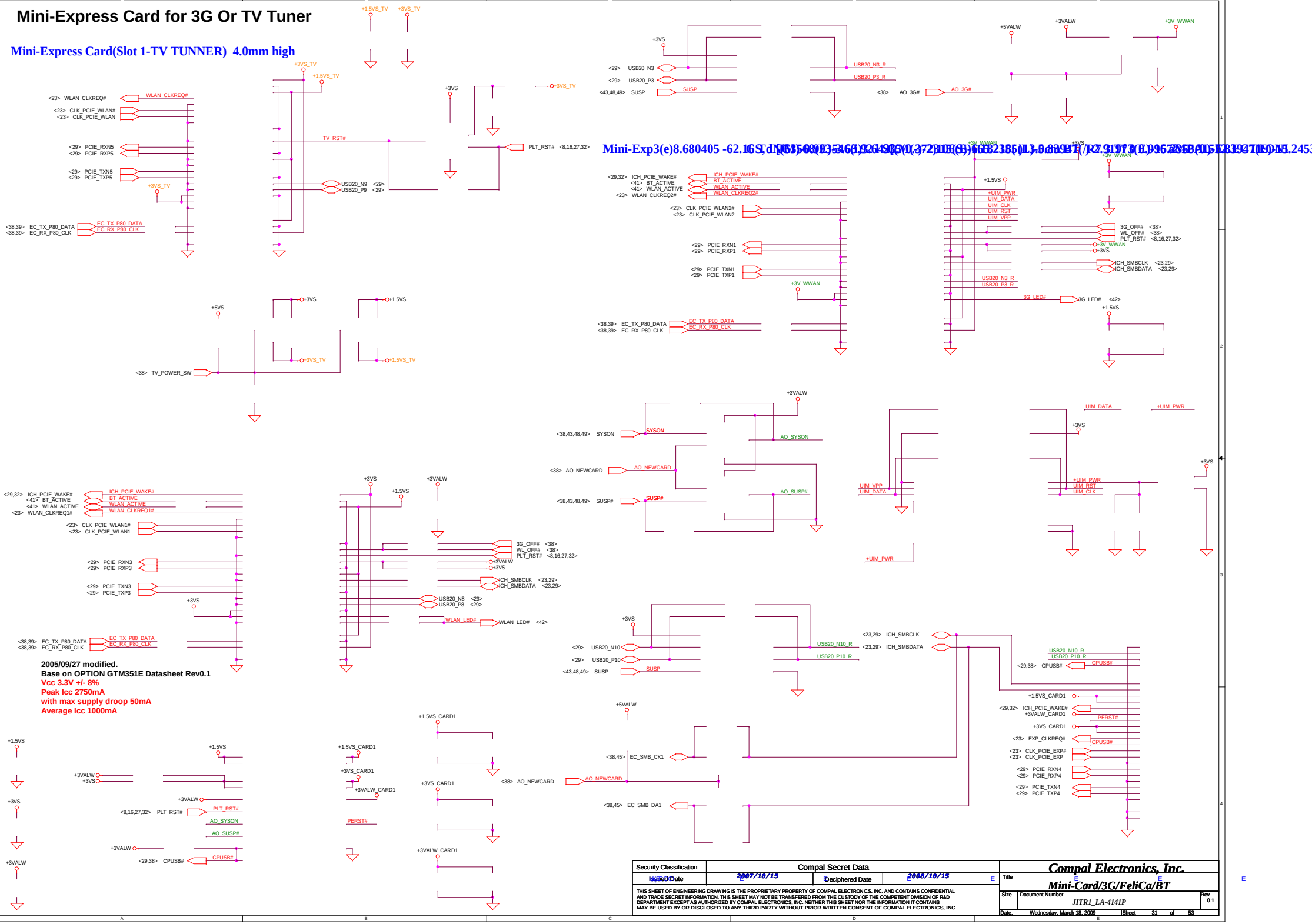
KNWB3/B4_LA4551P

Compal Electronics, Inc.

Title	ICH9M(4/4)-POWER&GND		
Size: Custom	Document Number: JITR1_LA-4141P		Rev: 0.1
Date: Wednesday, March 18, 2009	Sheet 30 of 53		

Mini-Express Card for 3G Or TV Tuner

Mini-Express Card(Slot 1-TV TUNNER) 4.0mm high

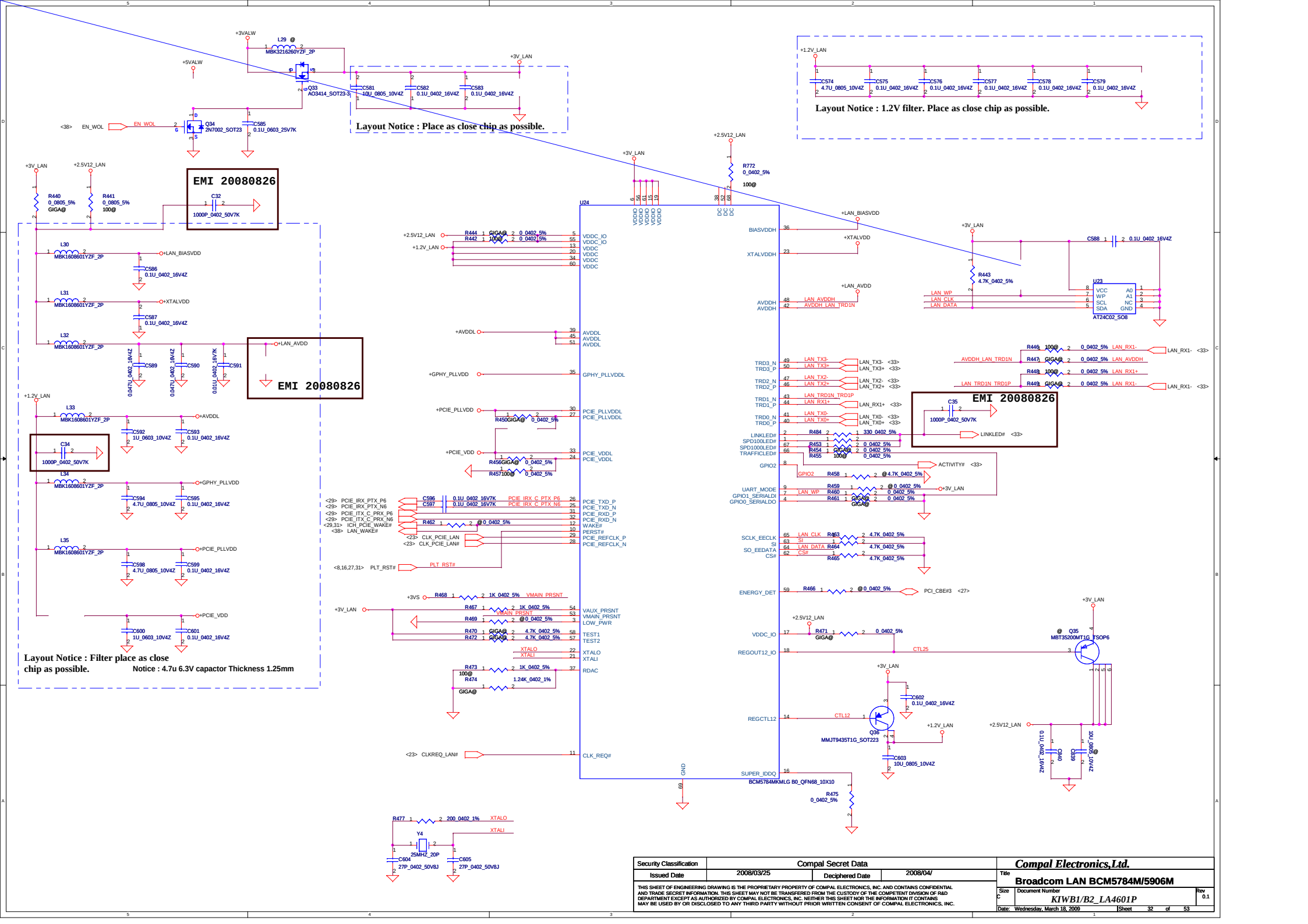


2005/09/27 modified.
Base on OPTION GTM351E Datasheet Rev0.1
Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title	Mini-Card/3G/FeliCa/BT	
Size	Document Number: JITR1_LA-4141P	Rev: 0.1
Date: Wednesday, March 18, 2009	Sheet 31 of 53	



Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

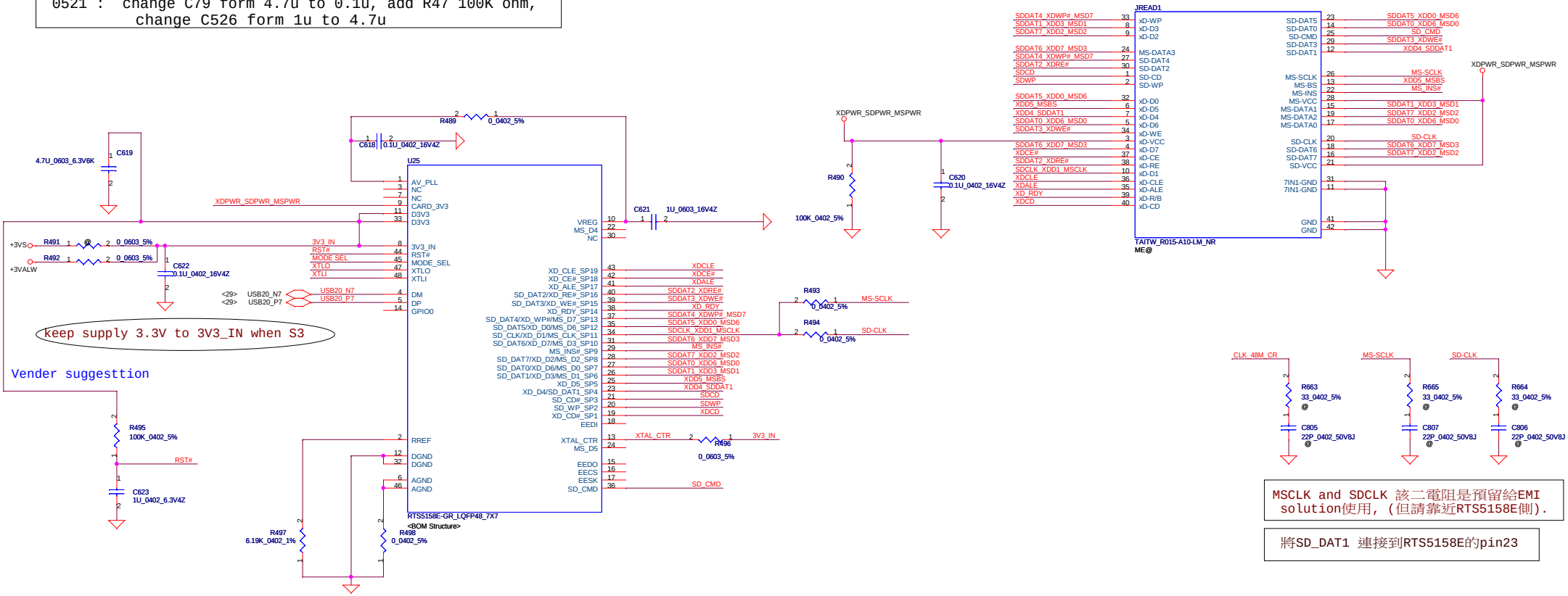
Compal Electronics,Ltd.

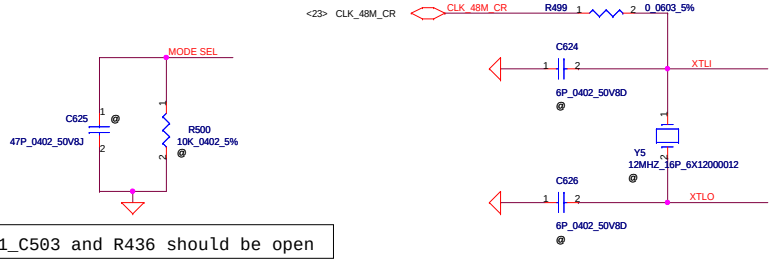
Title: **Broadcom LAN BCM5784M/5906M**

Size	Document Number	Rev
C	KIWB1/B2_LA4601P	0.1

Date: Wednesday, March 18, 2009 Sheet 32 of 53

0513 : CARD_3V3 旁路電阻 100K change to 4.7u CAP==>預留
0521 : change C79 form 4.7u to 0.1u, add R47 100K ohm,
change C526 form 1u to 4.7u





Security Classification	Compal Secret Data		
Issued Date	2006/08/04	Deciphered Date	2006/10/06

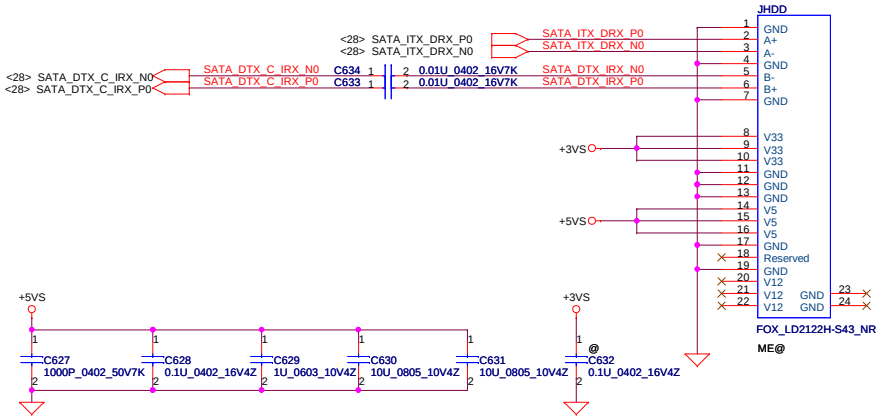
Compal Electronics, Inc.

Title: **1394+3 in 1 Card**

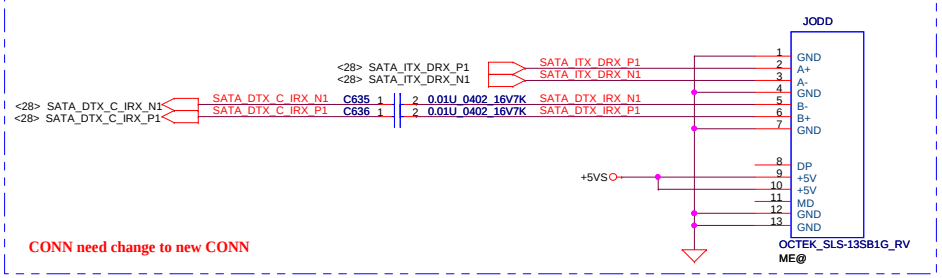
Size	Document Number	Rev
Custom	LA-3691P	1.0

Date: Wednesday, March 18, 2009 Sheet 34 of 53

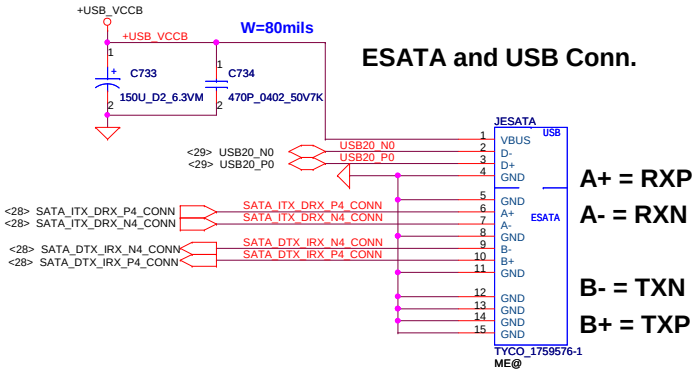
SATA HDD Conn.

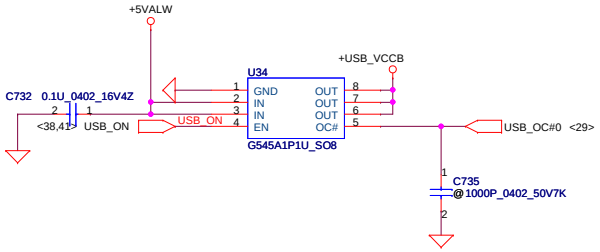


SATA ODD Conn.



ESATA and USB Conn.





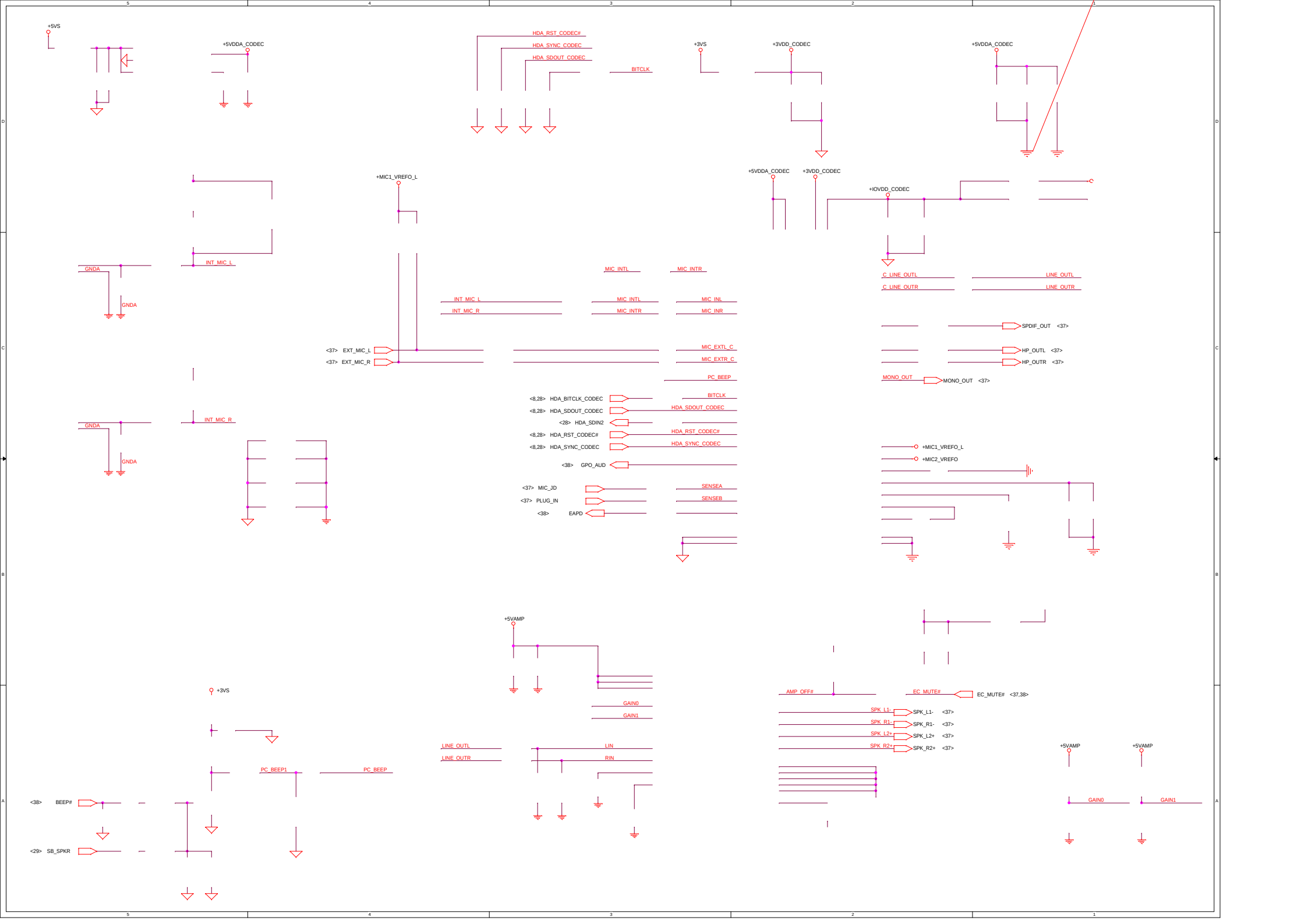
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

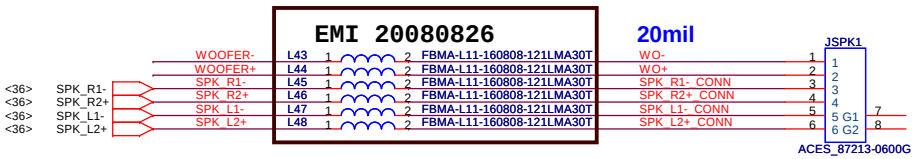
Title: **HDD & ODD Connector**

Size	Document Number	Rev
B	KIWB1/B2_LA4601P	0.1

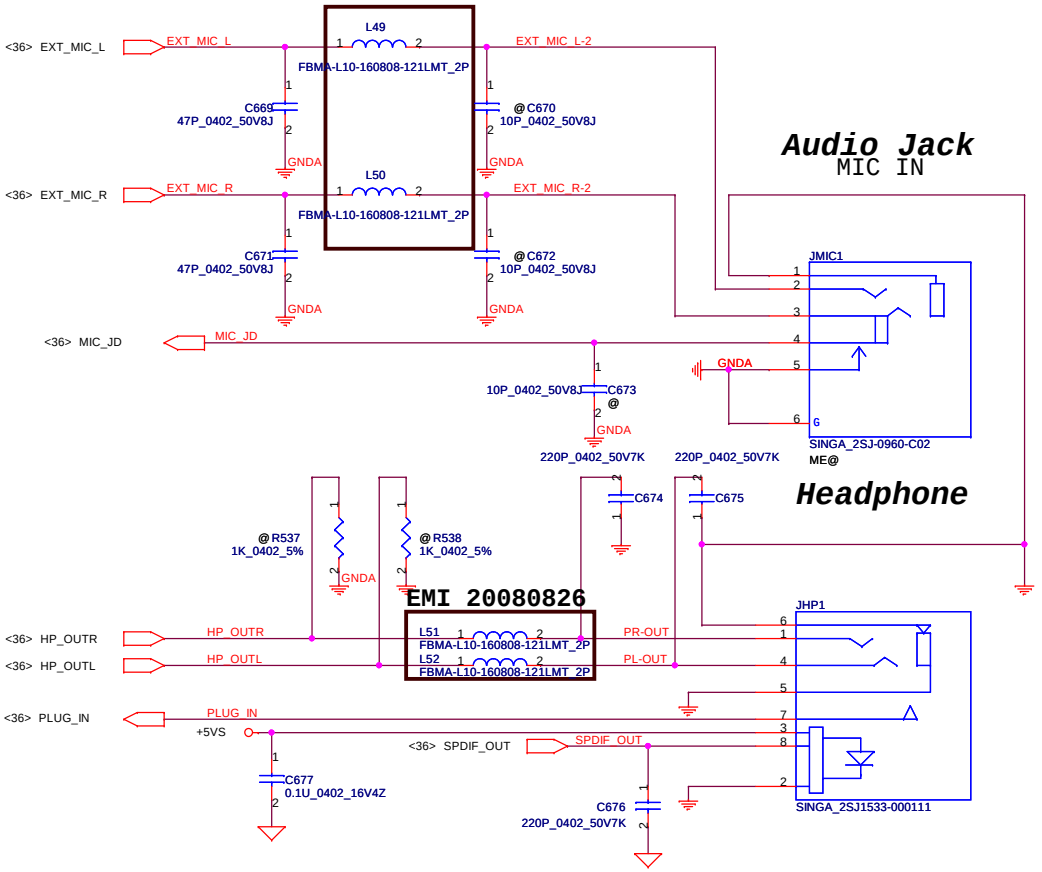
Date: Wednesday, March 18, 2009 | Sheet 35 of 53


+5VS
+5VDDA_CODEC
HDA_RST_CODEC#
HDA_SYNC_CODEC
HDA_SDOUT_CODEC
BITCLK
+3VS
+3VDD_CODEC
+5VDDA_CODEC
+MIC1_VREFO_L
INT_MIC_L
GNDA
INT_MIC_R
MIC_INTL
MIC_INTR
MIC_INL
MIC_INR
<37> EXT_MIC_L
<37> EXT_MIC_R
MIC_EXTL_C
MIC_EXTR_C
PC_BEEP
<8,28> HDA_BITCLK_CODEC
<8,28> HDA_SDOUT_CODEC
<28> HDA_SDIN2
<8,28> HDA_RST_CODEC#
<8,28> HDA_SYNC_CODEC
<38> GPO_AUD
<37> MIC_JD
<37> PLUG_IN
<38> EAPD
SENSEA
SENSEB
+IOVDD_CODEC
C_LINE_OUTL
C_LINE_OUTR
LINE_OUTL
LINE_OUTR
SPDIF_OUT <37>
HP_OUTL <37>
HP_OUTR <37>
MONO_OUT
MONO_OUT <37>
+MIC2_VREFO
+5VAMP
GAIN0
GAIN1
LIN
RIN
PC_BEEP1
<38> BEEP#
<29> SB_SPKR
AMP_OFF#
EC_MUTE#
EC_MUTE# <37,38>
SPK_L1-
SPK_R1-
SPK_L2+
SPK_R2+
SPK_L1- <37>
SPK_R1- <37>
SPK_L2+ <37>
SPK_R2+ <37>

SubWoofer Conn.
Speaker Connector

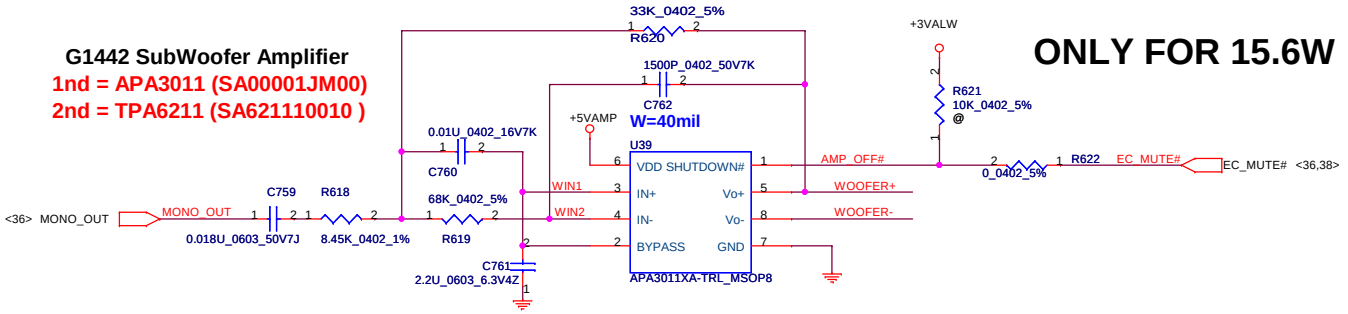


Audio Jack
EMI 20080826



G1442 SubWoofer Amplifier
1nd = APA3011 (SA00001JM00)
2nd = TPA6211 (SA621110010)

ONLY FOR 15.6W



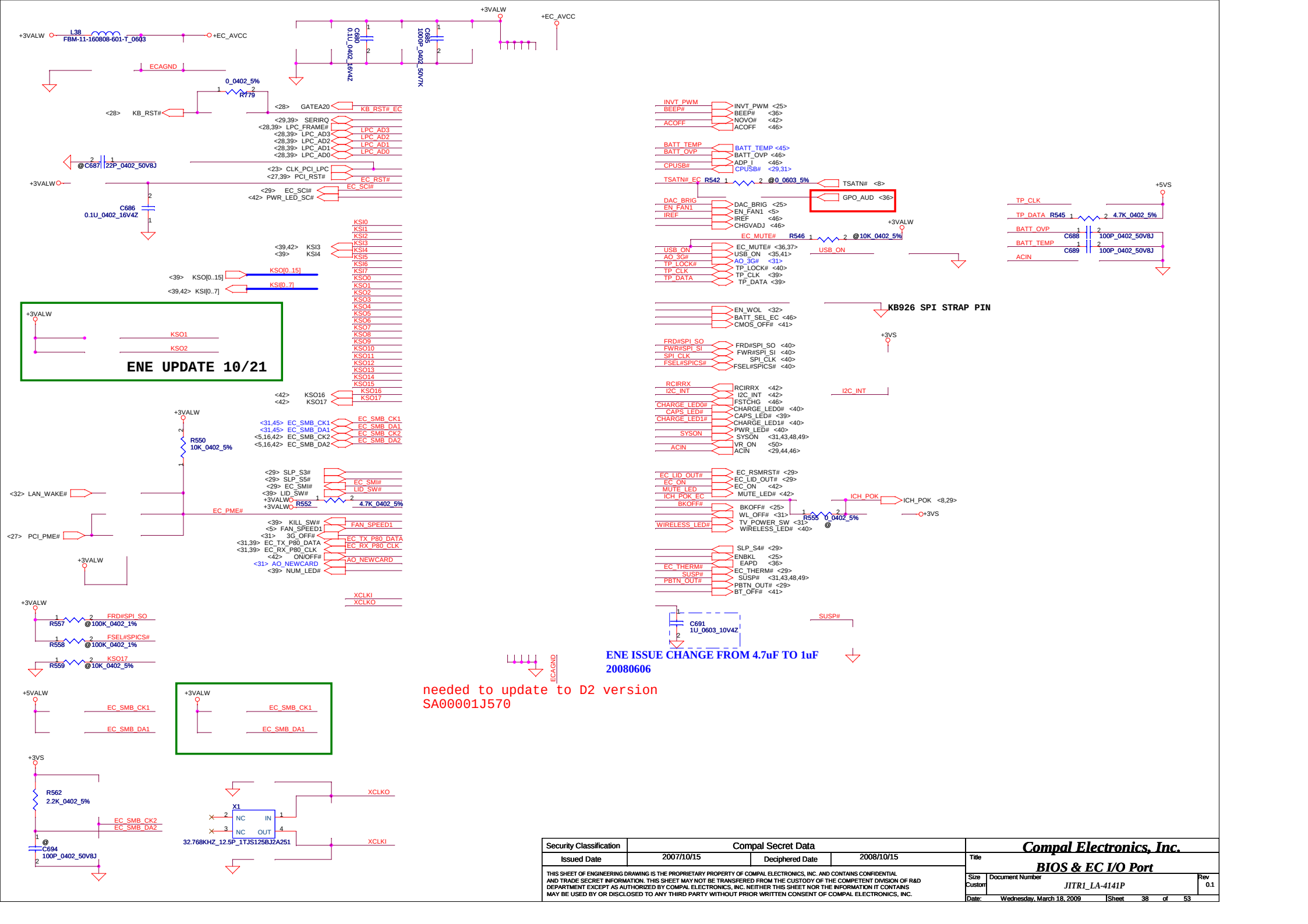
Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

Title: AMP,Audio speaker CONN

Size	Document Number	Rev
Custom	KIWB1/B2_LA4601P	0.1

Date: Wednesday, March 18, 2009 Sheet 37 of 53



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

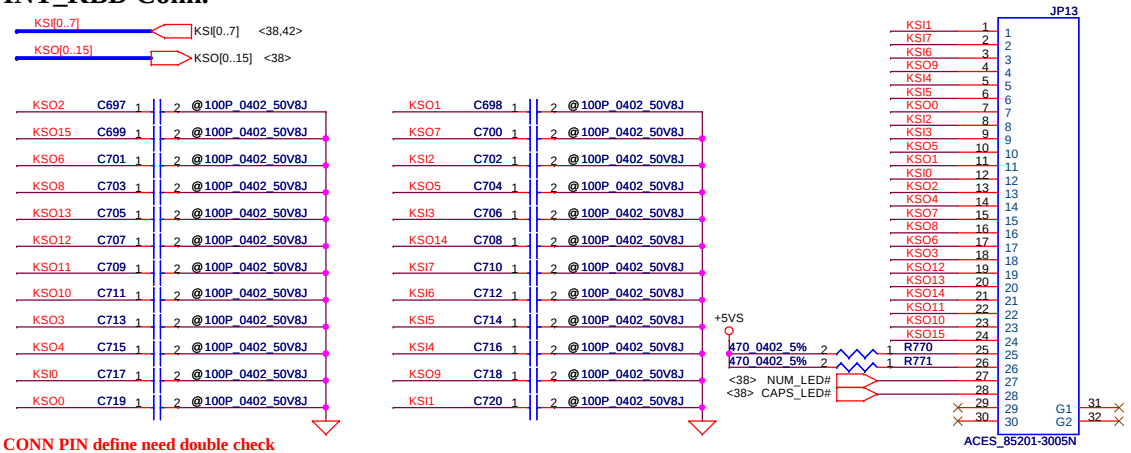
Compal Electronics, Inc.

Title: **BIOS & EC I/O Port**

Size	Document Number	Rev
Custom	JITR1_LA-4141P	0.1

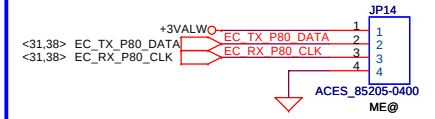
Date: Wednesday, March 18, 2009 | Sheet 38 of 53

INT_KBD Conn.

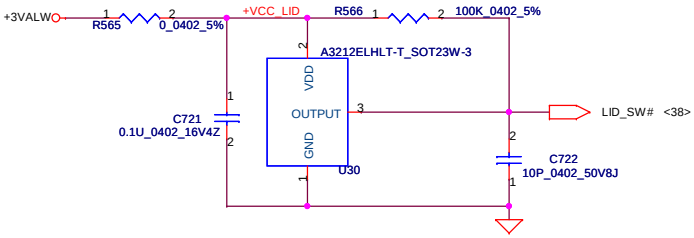


CONN PIN define need double check

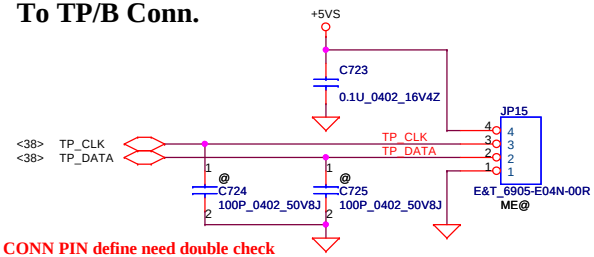
EC DEBUG PORT



Lid Switch

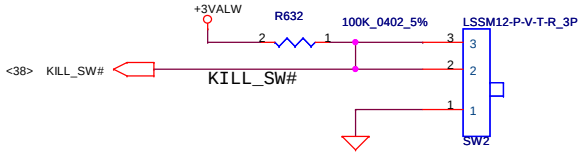


To TP/B Conn.

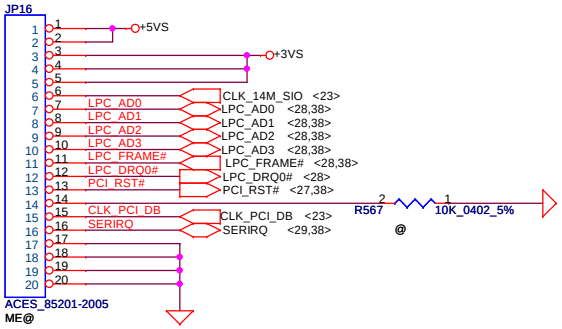


CONN PIN define need double check

Kill Switch



FOR LPC SIO DEBUG PORT



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

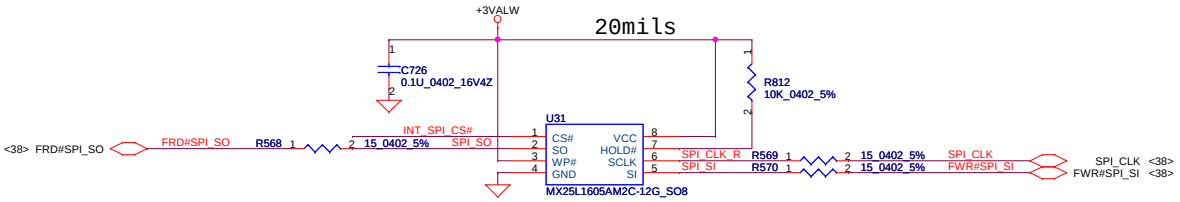
Compal Electronics, Inc.

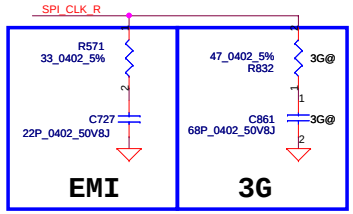
Title: KB /SW /LPC Debug Conn.

Size	Document Number	Rev
B	KIWB1/B2_LA4601P	0.1

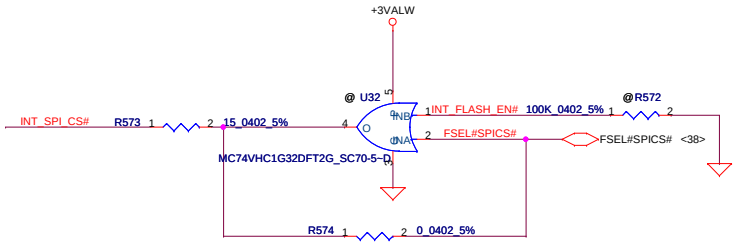
Date: Wednesday, March 18, 2009 Sheet 39 of 53

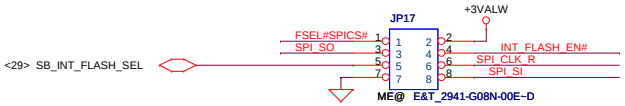
FOR EC 16M SPI ROM

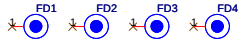




INPUT		OUTPUT
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	H

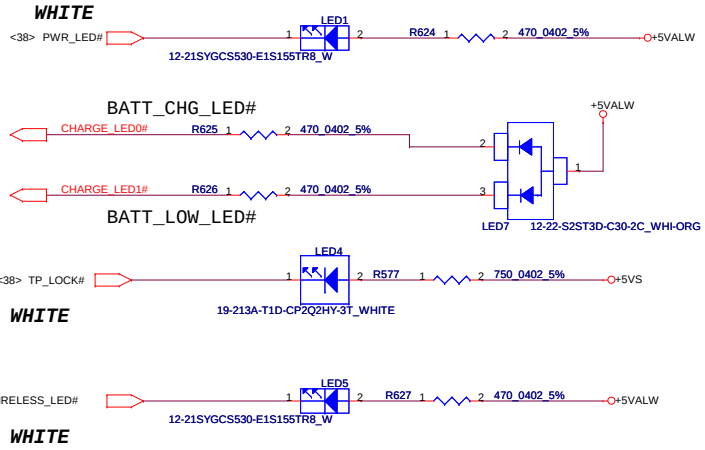


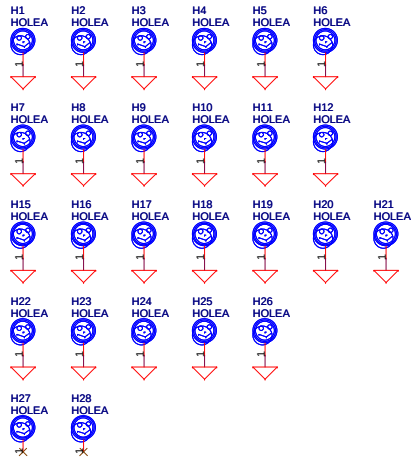




LED

SC500005B00,If=5mA,Vf=2.7V~3.15V,R=460~390ohm





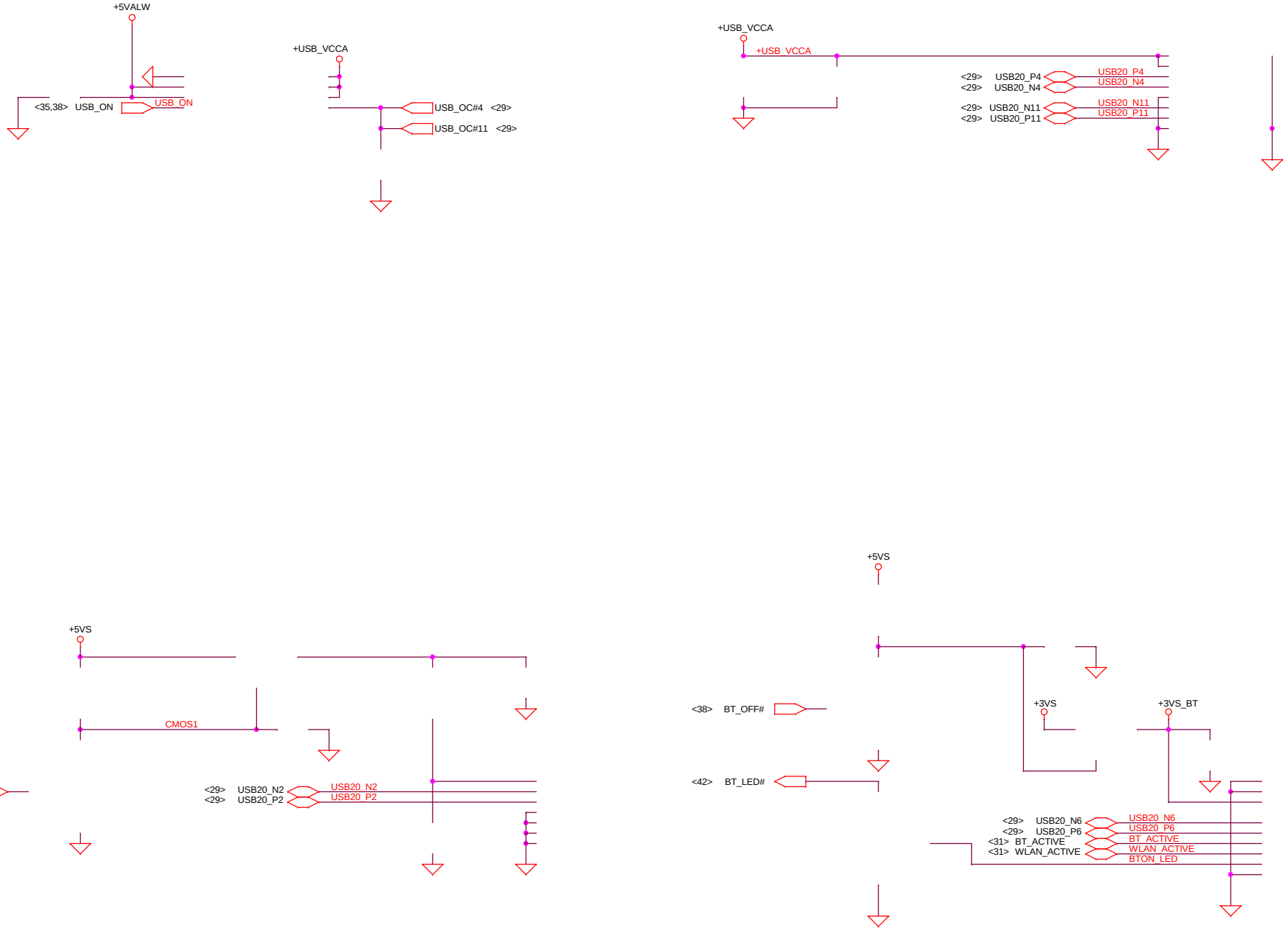
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **LED/EC SPI ROM**

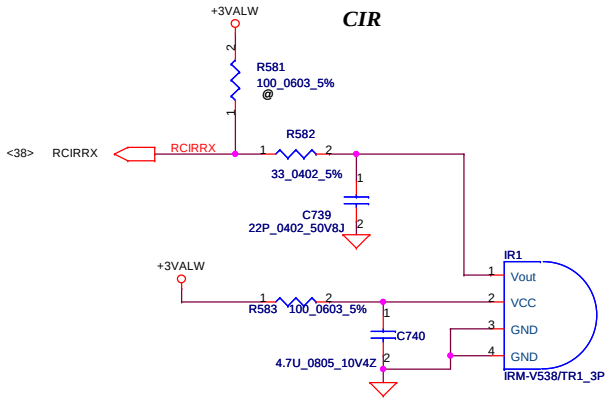
Size	Document Number	Rev
B	KIWB1/B2_LA4601P	0.1

Date: Wednesday, March 18, 2009 Sheet 40 of 53

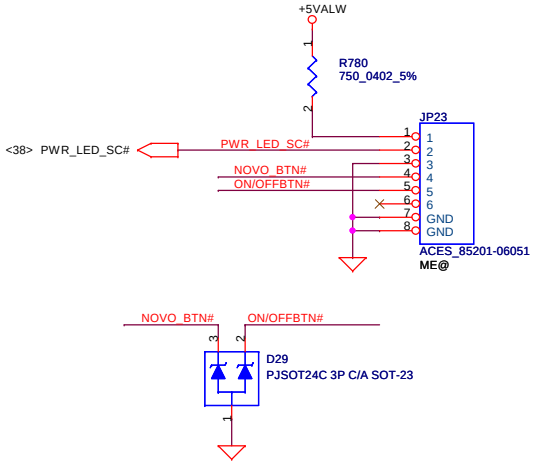


Security Classification	Compal Secret Data	
		Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONI		Size / Document Number / Rev
		Date: / Sheet of

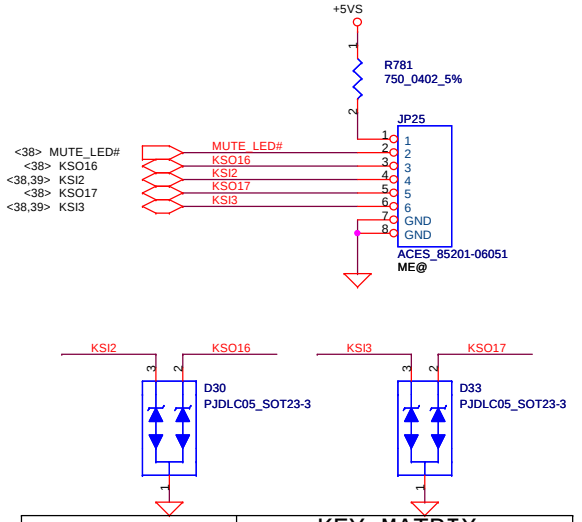
CIR



Power Bottom Board Conn. 6 pin

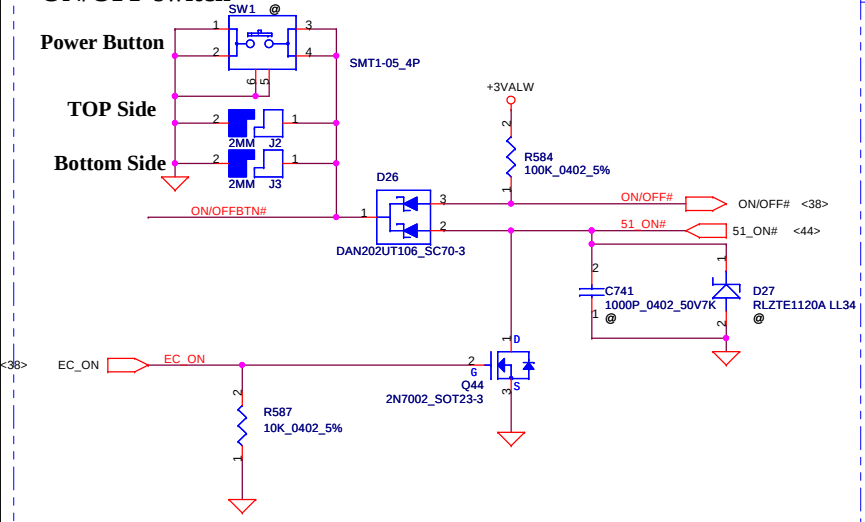


Bottom Board Conn. 6 pin

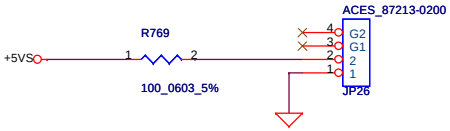


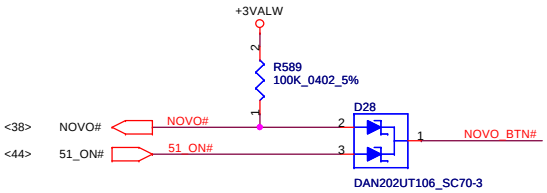
BTN FUNCTION	KEY MATRIX	
	IN	OUT
MUTE BTN	KSO17	KSI3
DOWN	KSO17	KSI2
UP	KSO16	KSI2

ON/OFF switch

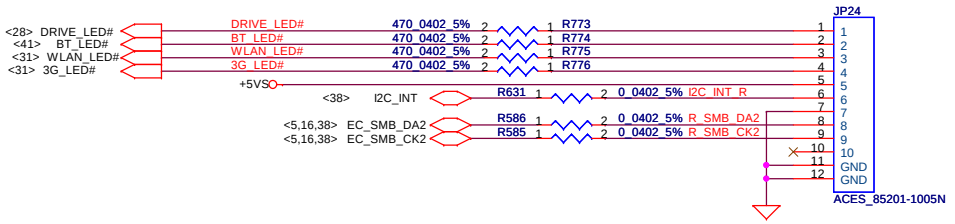


IDEAPAD BOARD 2PIN





Slide Board Conn. 10 pin



Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

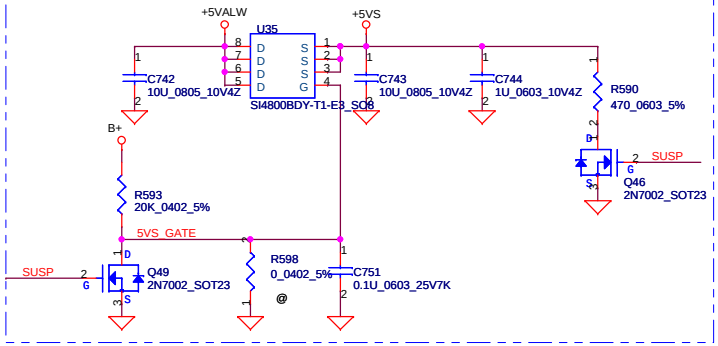
Compal Electronics,Ltd.

Title: Audio Jack & SW connector

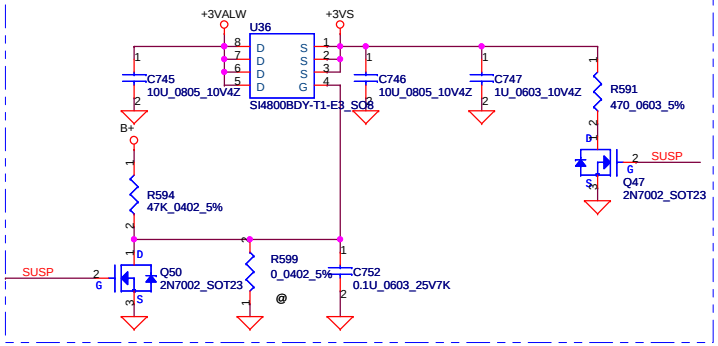
Size	Document Number	Rev
Custom	KIWB1/B2_LA4601P	0.1

Date: Wednesday, March 18, 2009 Sheet 42 of 53

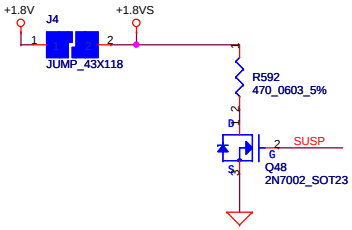
+5VALW TO +5VS



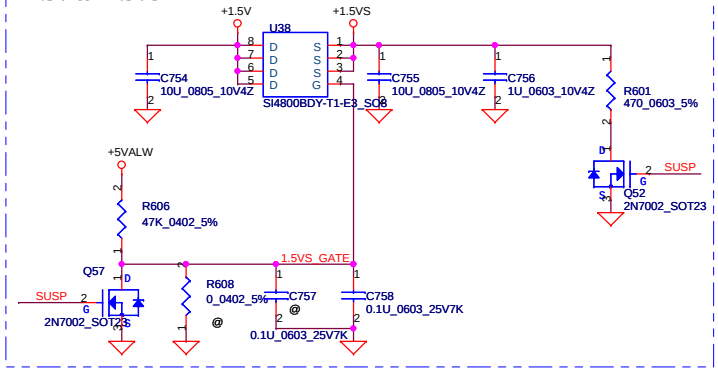
+3VALW TO +3VS

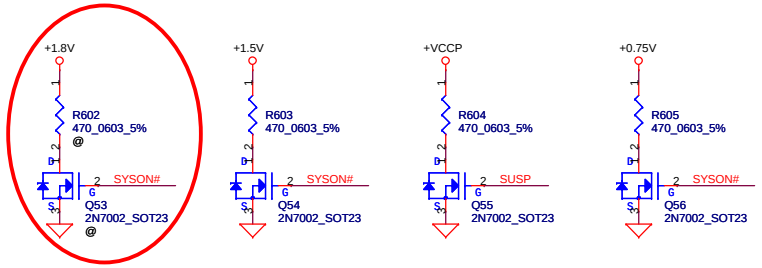


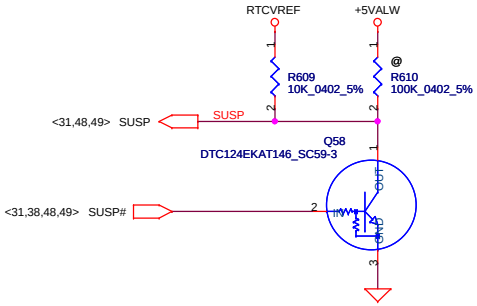
+1.8V to +1.8VS

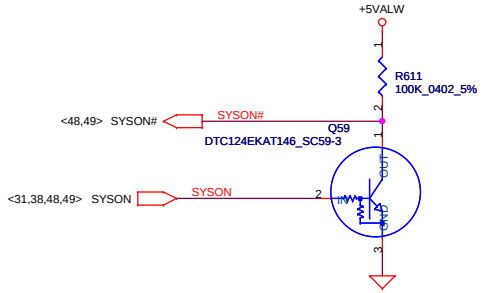


+1.5V to +1.5VS









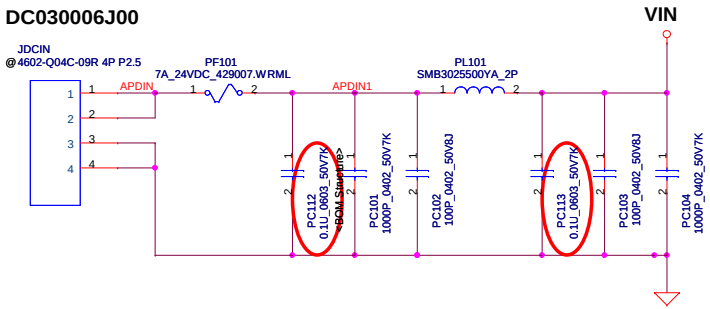
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

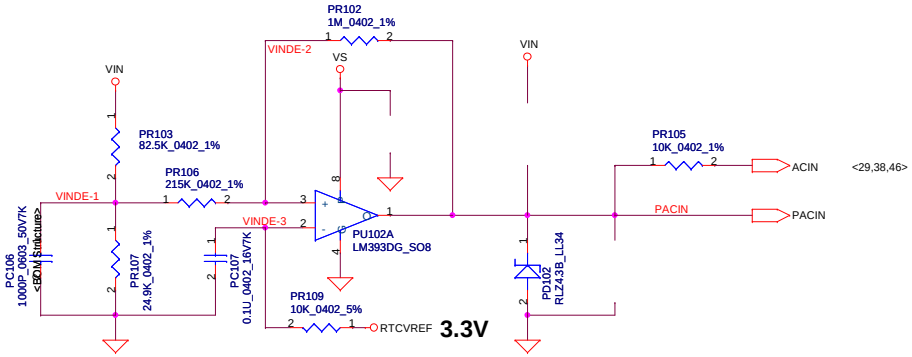
Compal Electronics, Inc.

Title: DC Interface

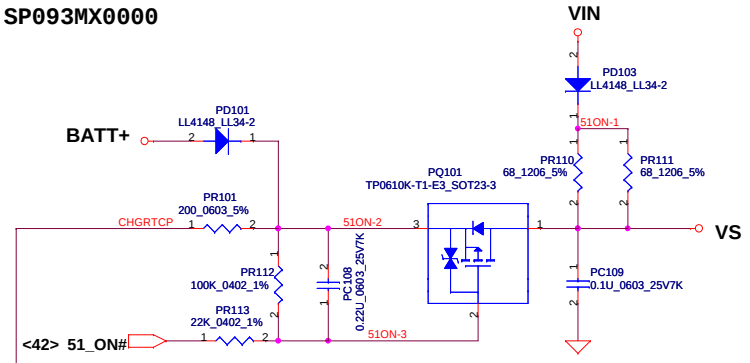
Size	Document Number	Rev
Custom	KIWB1/B2_LA4601P	0.1

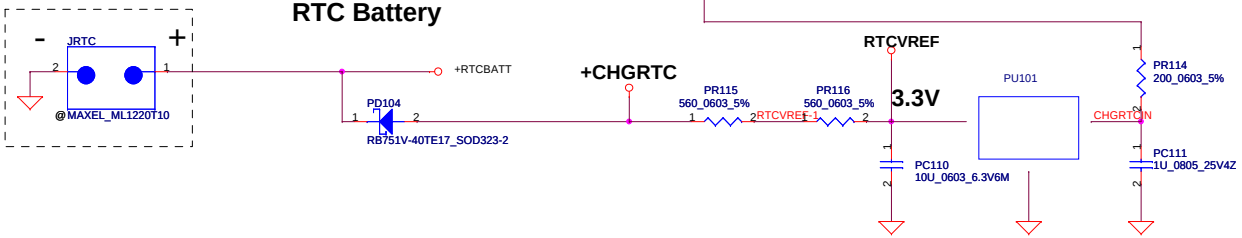
Date: Monday, April 27, 2009 Sheet 43 of 53





Vin Detector			
High	18.135	17.566	17.011
Low	14.866	14.355	14.063





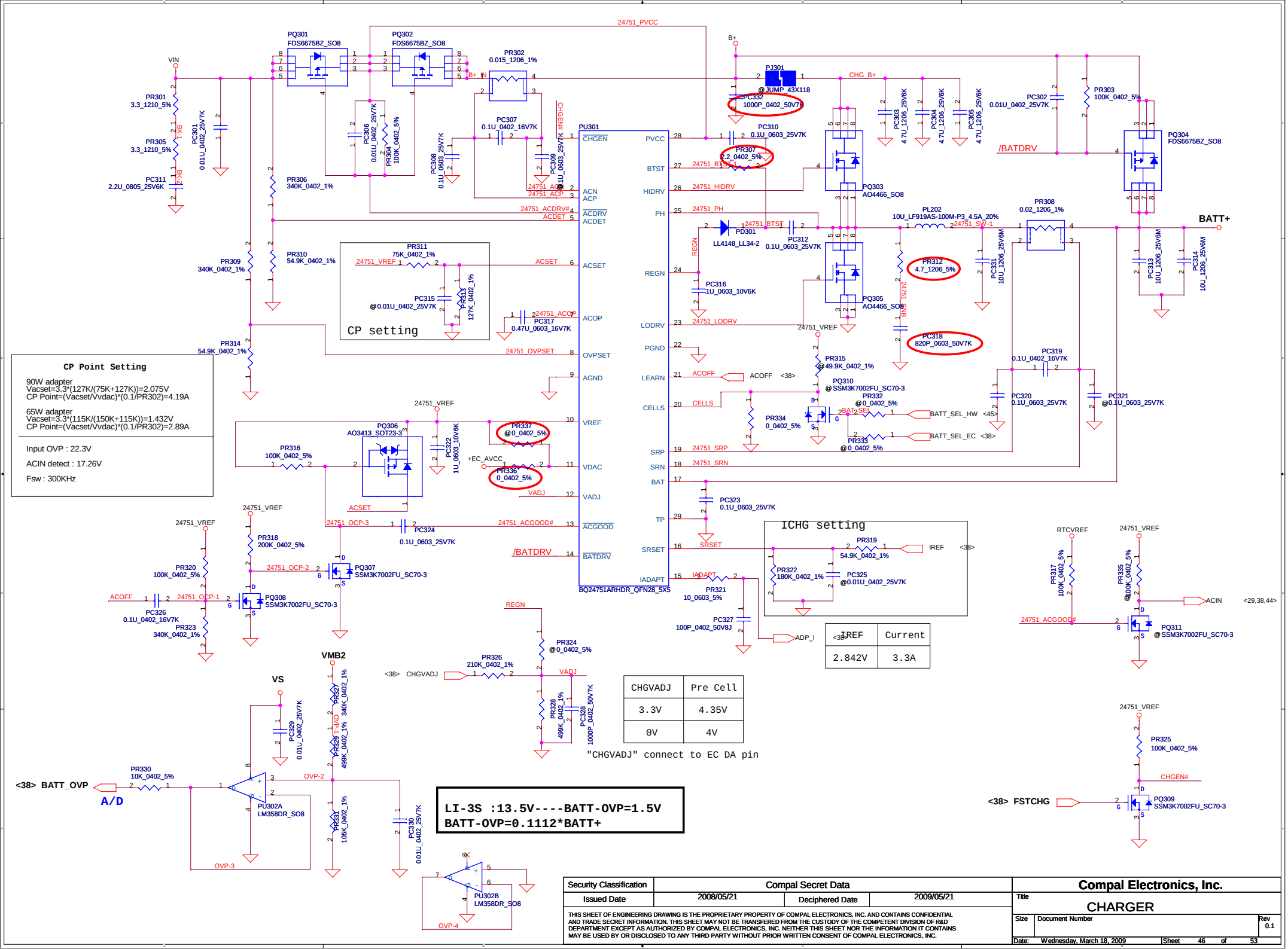
Security Classification	Compal Secret Data		
Issued Date	2008/05/21	Deciphered Date	2009/05/21

Compal Electronics, Inc.

Title: DCIN & DETECTOR

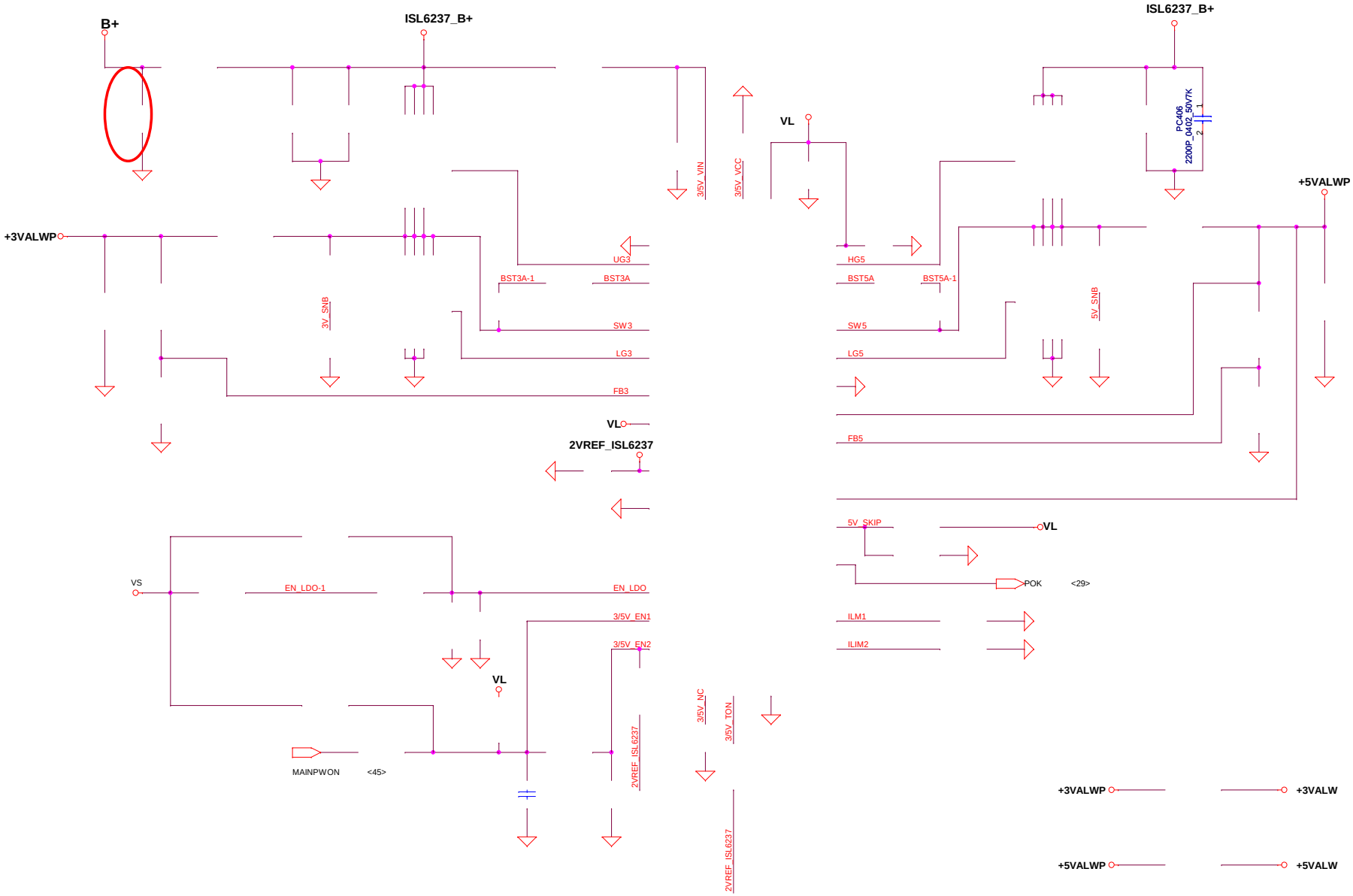
Size	Document Number	Rev
Custom		0.1

Date: Wednesday, March 18, 2009 | Sheet 44 of 53



IREF	Current
2.842V	3.3A

CHGVADJ	Pre Cell
3.3V	4.35V
0V	4V



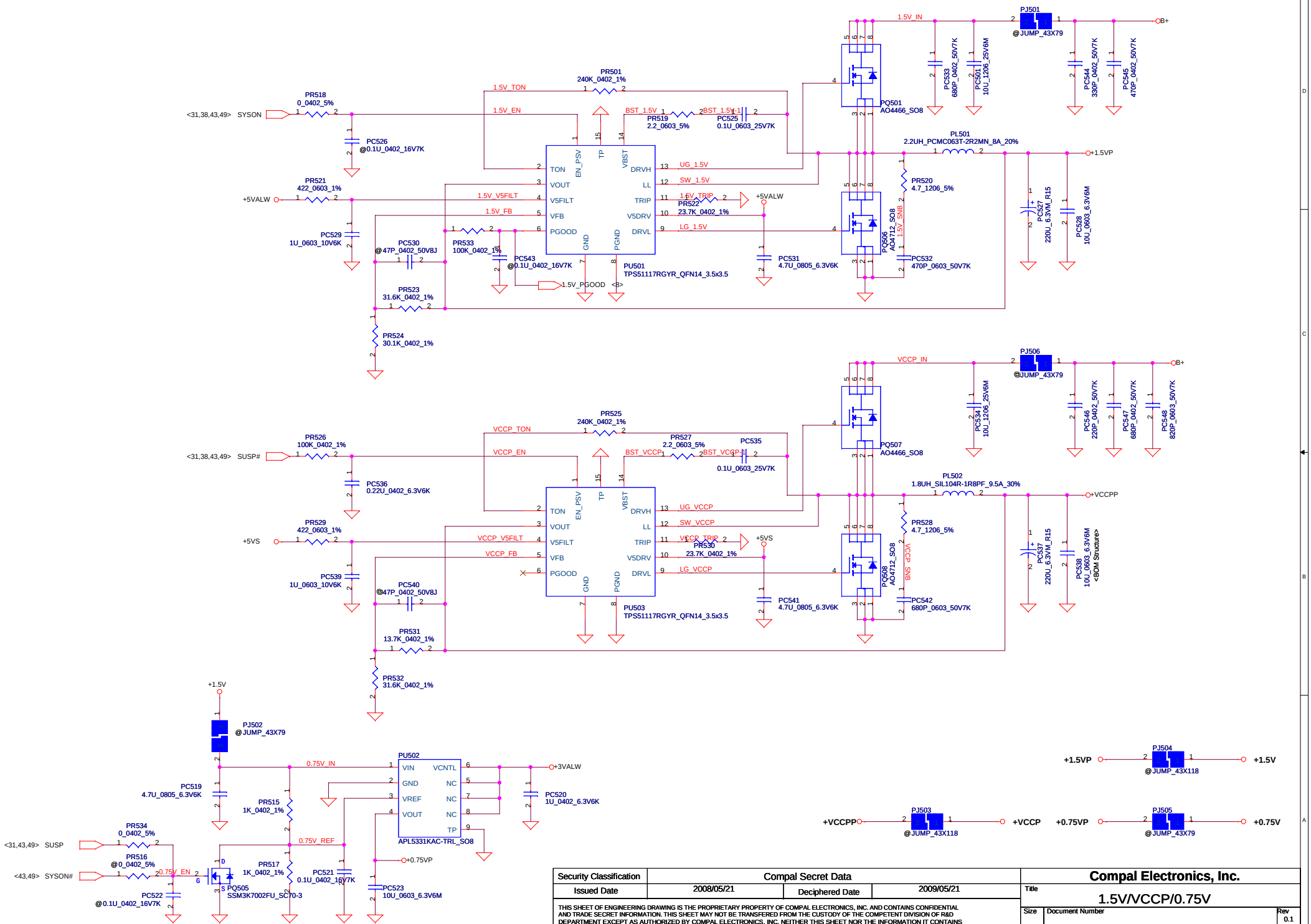
Security Classification	Compal Secret Data		
Issued Date	2008/05/21	Deciphered Date	2009/05/21

Compal Electronics, Inc.

Title: **3VALW/5VALW**

Size	Document Number	Rev
Custom		0.1

Date: Wednesday, March 18, 2009 | Sheet 47 of 53



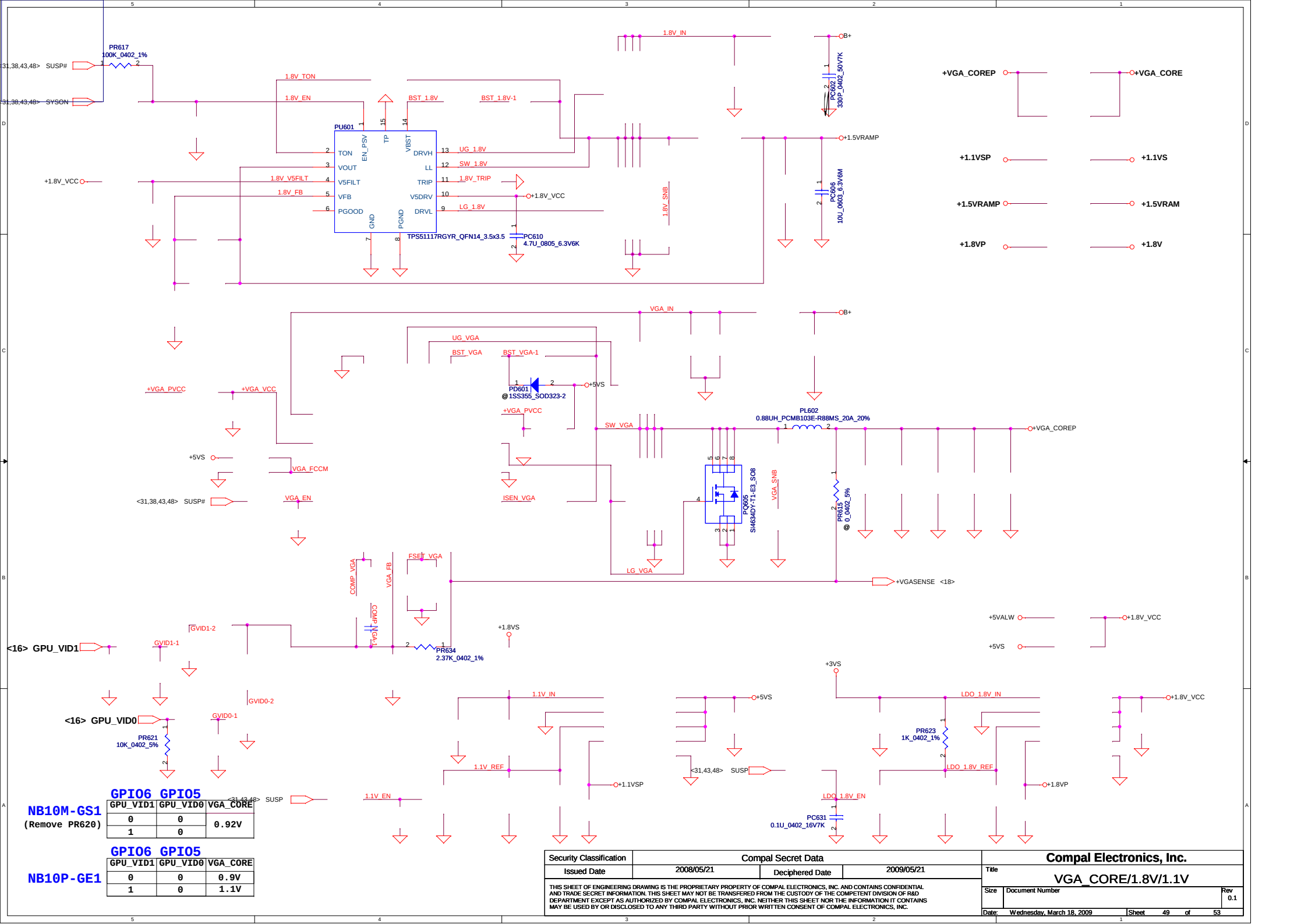
Security Classification	Compal Secret Data		
Issued Date	2008/05/21	Deciphered Date	2009/05/21

Compal Electronics, Inc.

Title: 1.5V/VCCP/0.75V

Size	Document Number	Rev
		0.1

Date: Wednesday, March 18, 2009 | Sheet 48 of 53



NB10M-GS1
(Remove PR620)

GPIO6	GPIO5	
GPU_VID1	GPU_VID0	VGA_CORE
0	0	0.92V
1	0	

NB10P-GE1

GPIO6	GPIO5	
GPU_VID1	GPU_VID0	VGA_CORE
0	0	0.9V
1	0	1.1V

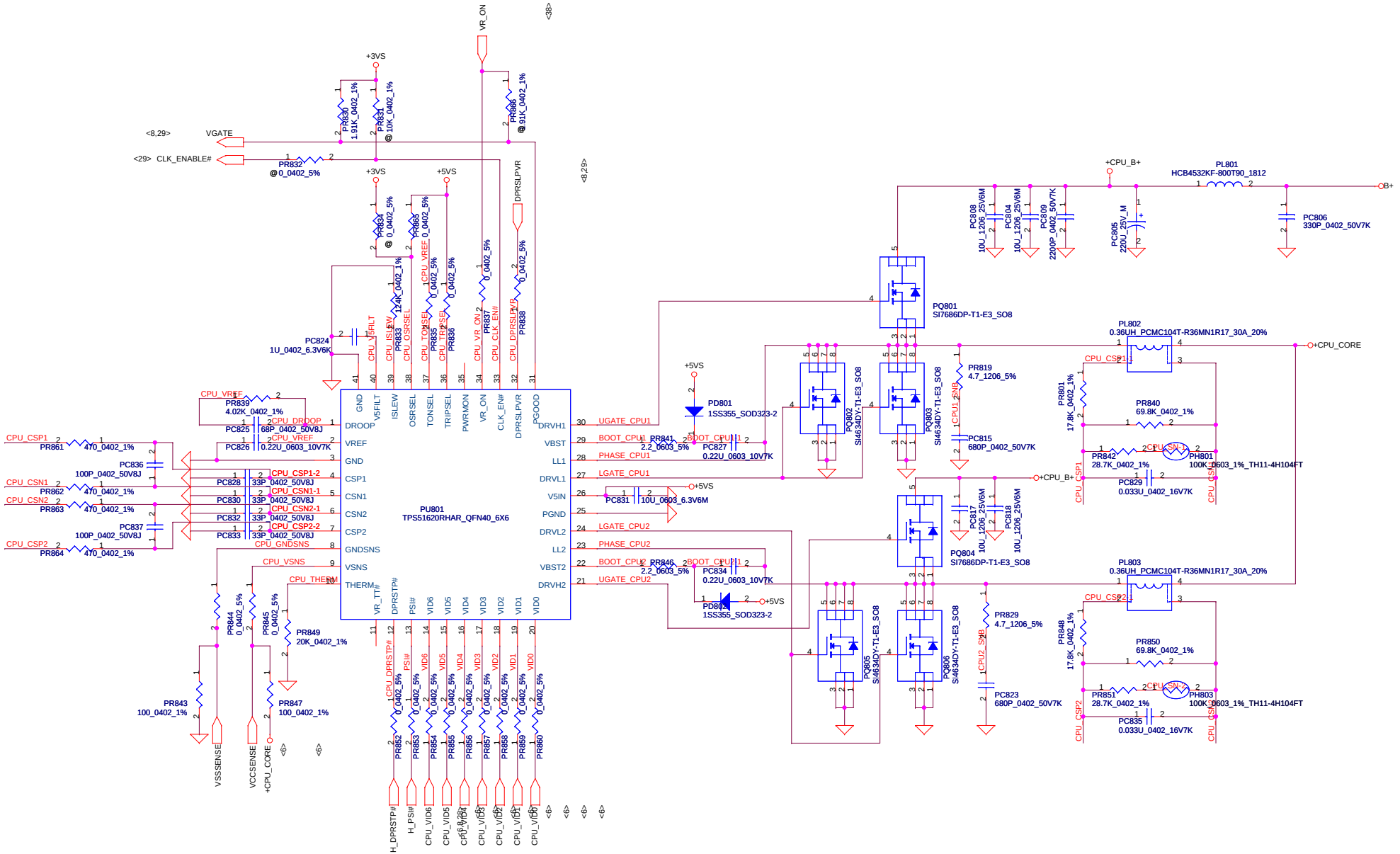
Security Classification	Compal Secret Data		
Issued Date	2008/05/21	Deciphered Date	2009/05/21

Compal Electronics, Inc.

Title: VGA_CORE/1.8V/1.1V

Size	Document Number	Rev
		0.1

Date: Wednesday, March 18, 2009 | Sheet 49 of 53



Security Classification	Compal Secret Data		
Issued Date	2008/05/21	Deciphered Date	2009/05/21

Compal Electronics, Inc.

Title: **+CPU_CORE**

Size	Document Number	Rev
Custom		0.1

Date: Wednesday, March 18, 2009 | Sheet 50 of 53

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Improve charge output current accuracy.	P46	Change PU301 Pin 11 VDAC source form 24751_VRFE to +EC_AVCC.	20080725	DVT
2	Improve CPU_CORE transient response.	P50	Change PR801, PR848 from 15.4k_0402_1% to 17.8k_0402_1% Change PR840, PR850 from 196k_0402_1% to 69.8k_0402_1% Change PC829, PC835 from 0.022u to 0.033u.	20080804	DVT
3	Adjust loadline.	P50	Change PR839 from 5.76k_0402_1% to 4.02k_0402_1%	20080804	DVT
4	Reduce VGA_CORE ripple.	P49	Add PC633, PC634 10u_0603_6.3V_V6M. Add PC619 330u_2.5V_R9M	20080804	DVT
5	Improve VGA_CORE efficiency at heavy load.	P49	Add PD601	20080804	DVT
6	Adjust 0.75V power sequence.	P48	Add PR534.	20080813	DVT
7	Adjust power sequence.	P48 P49	Change PR525 from 0 to 27K. PR526 from 0 to 100k. Add 0.1u_0402 at PC630 0.22u_0402 at PC536.	20080813	DVT
8	For customer upgrade VGA to N10X.	P49	Change PQ603 from SI4686 to SI7686DP. Change PQ604, PQ605 from FDMS670 to SI4634DY. Change PL602 from 1u to .88u. Change PC615 from 220u ESR15 to 330u ESR9.	20080813	DVT
9	Reserve OSR to reduce overshoot.	P50	Add PR865	20080813	DVT
10	Improve VGA CORE driver ability for upgrade VGA chip from N9X to N10X.	P49	Change PU602 VGA CORE solution from TPS51117 to ISL6269A	20080823	DVT
11	Reduce power board band.	P47 P48 P49 P50	Change PR403, PR405, PR519, PR527, PR603, PR611, PR841, PR846 to 2.2ohm at BOM. Change PR402, PR404, PR520, PR528, PR604, PR612, PR819, PR829 to 4.7ohm at BOM. Change PC414, PC415 to 330p_0402_50V at BOM. Change PC542, PC608, PC618, PC815, PC823 680P_0603_50V7K at BOM. Change PC532 to 470P-0603_50V7K. Add PC546 220P_0402_50V7K. Add PC405, PC544, PC602, PC617, PC806 330P_0402_50V7K. Add PC545 470P_0402_50V7K. Add PC533, PC547 680P_0402_50V7K.	20080826	DVT
12	Change 1.8V sequence the same with 1.8VS.	P49	Add PR617, PR631, PR637.	20080902	DVT
13	For solve charger unstable.	P46	Add PC331 10u_1206_25V6M	20080902	DVT
14	Adjust power sequence.	P49	Change PR617, PR632 to 100k_0402_1%. Add PC604, PC631 to 0.1u_0402.	20080905	DVT
15	Reduce power board band.	P46	Add PC332 1000P_0402_50V7K	20081013	PVT
16	Reserve VDAC power connect to 24751_VREF and EC_AVCC	P46	Add PR336, PR337 0_0402_5%	20081015	PVT
17	Reduce power board band.	P44	Add PC112, PC113 0.1U_0603_50V7K	20081022	PVT

Compal Electronics, Inc.	
Title	HW PIR
Size: B	Document Number: KIWB1/B2_LA4602P
Rev: 1.0	
Date: Wednesday, March 18, 2009	Sheet 52 of 53

Compal Electronics, Inc.	
Title	HW PIR
Size: B	Document Number: KIWB1/B2_LA4602P
Rev: 1.0	
Date: Wednesday, March 18, 2009	Sheet 53 of 53