

# Compal Confidential

## Schematics Document

Intel Huron River Platform  
Sandy Bridge (Dual Core BGA 1023) With  
Couger Point Core Logic

LA-7401P

2011-03-24

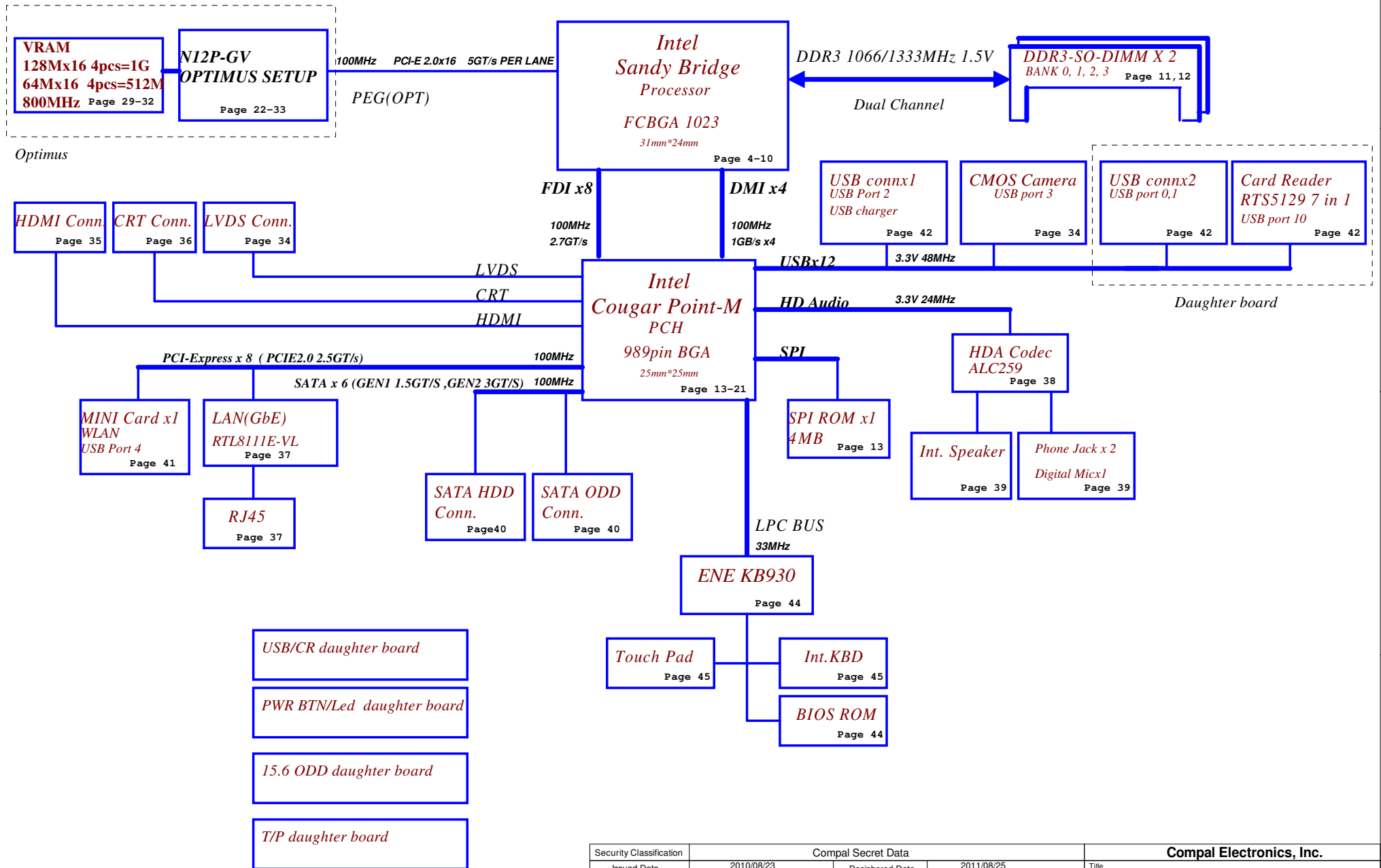
REV:1.0

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				Date: Sunday, April 10, 2011	Sheet 1 of 56	

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Model Name : PAJ80(14" UMA/Dis)/PAJ90(15.6" UMA/Dis)

File Name : LA-7401P



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				Size	Document Number	1.0
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				Date:	Sunday, April 10, 2011	Sheet 2 of 56

### Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
BATT+	Battery power supply (12.6V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGF_X_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_DGPU	+1.05VS to +1.05VS_DGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS	+VCCPP to +1.05VS switched power rail for CPU,PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+VRAM_1.5VS	+1.5V to +VRAM_1.5VS power rail for GPU	ON	OFF	OFF
+1.8VS	+5VALW to 1.8VS switched power rail to CPU,PCH	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+LAN_IO	+3VALW to +LAN_IO power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resistor)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

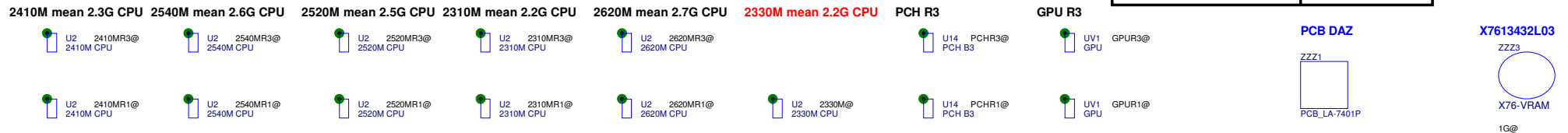
STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

### USB Port Table

USB 2.0	USB 1.1	Port	2 External USB Port
EHC11	UHCI0	0	CONN
		1	CONN
	UHCI1	2	CONN
		3	Camera
		4	Mini Card(WLAN/BT)
	UHCI2	5	NA
		6	
7			
EHC12	UHCI4	8	NA
		9	NA
	UHCI5	10	Card Reader
		11	
		12	
		13	

### BTO Option Table

BTO Item	BOM Structure
Optimus	OPT@
Connector	CONN@
Unpop	@
14" PCB	14@
15.6" PCB	15@
UMA PCB	UMA@
Dis PCB (Optimus)	OPT@
X76 512M	512M@
X76 1G	1G@



### PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b

### EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b

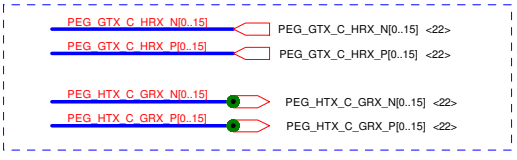
### EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9E H	1001 1110 b

### SMBUS Control Table

	SOURCE	BATT	CPU THERMAL SENSOR	SODIMM 0 SODIMM 1	WLAN WWAN	LCD DDC ROM	HDMI DDC ROM	PCH	GPU
EC_SMB_CK1	KB930	V							
EC_SMB_DA1									
EC_SMB_CK2	KB930							V	V
EC_SMB_DA2									
PCH_LCD_CLK	PCH					V			
PCH_LCD_DATA									
SDVO_SCLK	PCH						V		
SDVO_SDATA									
PCH_SMBCLK	PCH			V	V				
PCH_SMBDATA									

PEG\_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms  
 PEG\_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



PEG_ICOMPI	G3	PEG COMP			
PEG_ICOMPO	G1				
PEG_RCOMPO	G4				
PEG_RX#0	H22	PEG GTX C HRX N15			
PEG_RX#1	J21	PEG GTX C HRX N14			
PEG_RX#2	B22	PEG GTX C HRX N13			
PEG_RX#3	D21	PEG GTX C HRX N12			
PEG_RX#4	A19	PEG GTX C HRX N11			
PEG_RX#5	D17	PEG GTX C HRX N10			
PEG_RX#6	B14	PEG GTX C HRX N9			
PEG_RX#7	D13	PEG GTX C HRX N8			
PEG_RX#8	B10	PEG GTX C HRX N7			
PEG_RX#9	G8	PEG GTX C HRX N6			
PEG_RX#10	A8	PEG GTX C HRX N5			
PEG_RX#11	H8	PEG GTX C HRX N4			
PEG_RX#12	E6	PEG GTX C HRX N3			
PEG_RX#13	K7	PEG GTX C HRX N2			
PEG_RX#14	K22	PEG GTX C HRX N15			
PEG_RX#15	K19	PEG GTX C HRX N14			
PEG_RX#16	C21	PEG GTX C HRX N13			
PEG_RX#17	D19	PEG GTX C HRX N12			
PEG_RX#18	C19	PEG GTX C HRX N11			
PEG_RX#19	D16	PEG GTX C HRX N10			
PEG_RX#20	C13	PEG GTX C HRX N9			
PEG_RX#21	A12	PEG GTX C HRX N8			
PEG_RX#22	C11	PEG GTX C HRX N7			
PEG_RX#23	C9	PEG GTX C HRX N6			
PEG_RX#24	F8	PEG GTX C HRX N5			
PEG_RX#25	C8	PEG GTX C HRX N4			
PEG_RX#26	C5	PEG GTX C HRX N3			
PEG_RX#27	H6	PEG GTX C HRX N2			
PEG_RX#28	F6	PEG GTX C HRX N1			
PEG_RX#29	K6	PEG GTX C HRX N15			
PEG_RX#30	G22	PEG HTX GRX N15	C16	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX N15
PEG_RX#31	C23	PEG HTX GRX N14	C17	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX N14
PEG_RX#32	D23	PEG HTX GRX N13	C18	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX N13
PEG_RX#33	F21	PEG HTX GRX N12	C19	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX N12
PEG_RX#34	H19	PEG HTX GRX N11	C20	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX N11
PEG_RX#35	C17	PEG HTX GRX N10	C21	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX N10
PEG_RX#36	K15	PEG HTX GRX N9	C22	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX N9
PEG_RX#37	F17	PEG HTX GRX N8	C23	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX N8
PEG_RX#38	F14	PEG HTX GRX N7	C24	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX N7
PEG_RX#39	A15	PEG HTX GRX N6	C25	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX N6
PEG_RX#40	J14	PEG HTX GRX N5	C26	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX N5
PEG_RX#41	H13	PEG HTX GRX N4	C27	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX N4
PEG_RX#42	M10	PEG HTX GRX N3	C28	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX N3
PEG_RX#43	F10	PEG HTX GRX N2	C29	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX N2
PEG_RX#44	D9	PEG HTX GRX N1	C30	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX N1
PEG_RX#45	J4	PEG HTX GRX N0	C31	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX N0
PEG_TX#0	F22	PEG HTX GRX P15	C32	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX P15
PEG_TX#1	A23	PEG HTX GRX P14	C33	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX P14
PEG_TX#2	D24	PEG HTX GRX P13	C34	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX P13
PEG_TX#3	E21	PEG HTX GRX P12	C35	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX P12
PEG_TX#4	G19	PEG HTX GRX P11	C36	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX P11
PEG_TX#5	B18	PEG HTX GRX P10	C37	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX P10
PEG_TX#6	K17	PEG HTX GRX P9	C38	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX P9
PEG_TX#7	G17	PEG HTX GRX P8	C39	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX P8
PEG_TX#8	E14	PEG HTX GRX P7	C40	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX P7
PEG_TX#9	C15	PEG HTX GRX P6	C41	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX P6
PEG_TX#10	K13	PEG HTX GRX P5	C42	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX P5
PEG_TX#11	G13	PEG HTX GRX P4	C43	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX P4
PEG_TX#12	M10	PEG HTX GRX P3	C44	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX P3
PEG_TX#13	G10	PEG HTX GRX P2	C45	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX P2
PEG_TX#14	D8	PEG HTX GRX P1	C46	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX P1
PEG_TX#15	K4	PEG HTX GRX P0	C47	1	2 OPT@ 0.1U 0402 16V7K PEG HTX C GRX P0

PCI EXPRESS -- GRAPHICS

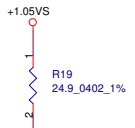
DMI

Intel(R) FDI

DP

SANDY-BRIDGE\_BGA1023-D

- <15> DMI\_CRX\_PTX\_N0 M2 DMI\_RX#0
- <15> DMI\_CRX\_PTX\_N1 P6 DMI\_RX#1
- <15> DMI\_CRX\_PTX\_N2 P1 DMI\_RX#2
- <15> DMI\_CRX\_PTX\_N3 P10 DMI\_RX#3
- <15> DMI\_CRX\_PTX\_P0 N3 DMI\_RX0
- <15> DMI\_CRX\_PTX\_P1 P7 DMI\_RX1
- <15> DMI\_CRX\_PTX\_P2 P9 DMI\_RX2
- <15> DMI\_CRX\_PTX\_P3 P11 DMI\_RX3
- <15> DMI\_CTX\_PRX\_N0 K1 DMI\_TX#0
- <15> DMI\_CTX\_PRX\_N1 M8 DMI\_TX#1
- <15> DMI\_CTX\_PRX\_N2 N4 DMI\_TX#2
- <15> DMI\_CTX\_PRX\_N3 R2 DMI\_TX#3
- <15> DMI\_CTX\_PRX\_P0 K3 DMI\_TX0
- <15> DMI\_CTX\_PRX\_P1 M7 DMI\_TX1
- <15> DMI\_CTX\_PRX\_P2 P4 DMI\_TX2
- <15> DMI\_CTX\_PRX\_P3 T3 DMI\_TX3
- <15> FDI\_CTX\_PRX\_N0 U7 FDI0\_TX#0
- <15> FDI\_CTX\_PRX\_N1 W11 FDI0\_TX#1
- <15> FDI\_CTX\_PRX\_N2 W1 FDI0\_TX#2
- <15> FDI\_CTX\_PRX\_N3 AA6 FDI0\_TX#3
- <15> FDI\_CTX\_PRX\_N4 W6 FDI1\_TX#0
- <15> FDI\_CTX\_PRX\_N5 VA FDI1\_TX#1
- <15> FDI\_CTX\_PRX\_N6 Y2 FDI1\_TX#2
- <15> FDI\_CTX\_PRX\_N7 AC9 FDI1\_TX#3
- <15> FDI\_CTX\_PRX\_P0 U8 FDI0\_TX0
- <15> FDI\_CTX\_PRX\_P1 W10 FDI0\_TX1
- <15> FDI\_CTX\_PRX\_P2 W3 FDI0\_TX2
- <15> FDI\_CTX\_PRX\_P3 AA7 FDI0\_TX3
- <15> FDI\_CTX\_PRX\_P4 T4 FDI1\_TX0
- <15> FDI\_CTX\_PRX\_P5 AA3 FDI1\_TX1
- <15> FDI\_CTX\_PRX\_P6 AA3 FDI1\_TX2
- <15> FDI\_CTX\_PRX\_P7 AC8 FDI1\_TX3
- <15> FDI\_FSYNC0 AA11 FDI0\_FSYNC
- <15> FDI\_FSYNC1 AC12 FDI1\_FSYNC
- <15> FDI\_INT U11 FDI\_INT
- <15> FDI\_LSYNC0 AA10 FDI0\_LSYNC
- <15> FDI\_LSYNC1 AG8 FDI1\_LSYNC



eDP\_COMP and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

<PCH>

<PCH>

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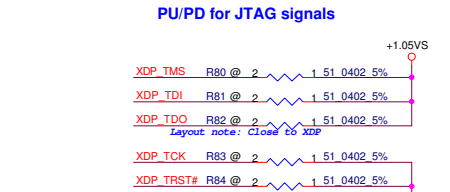
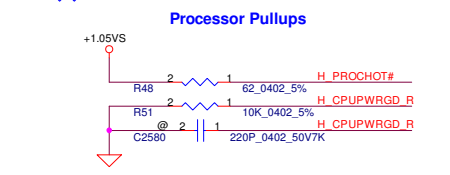
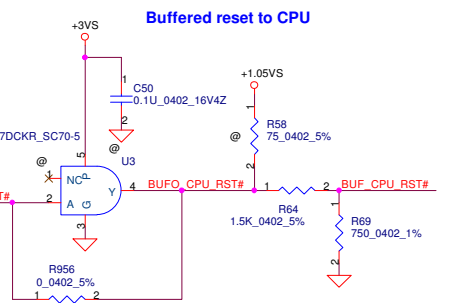
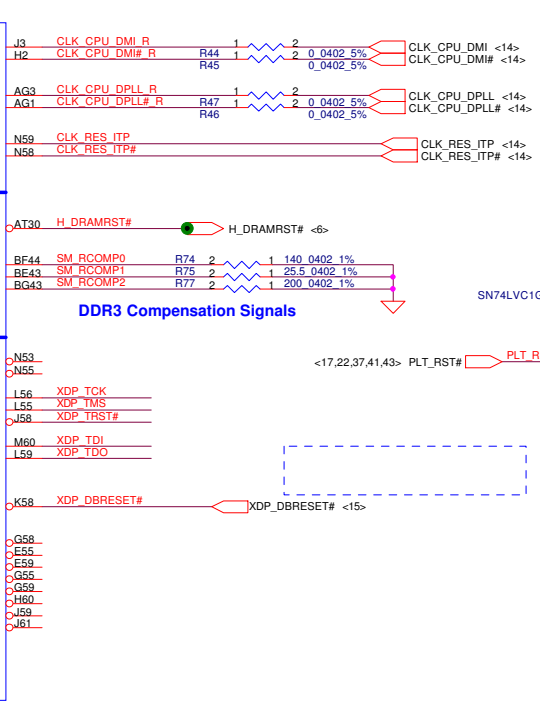
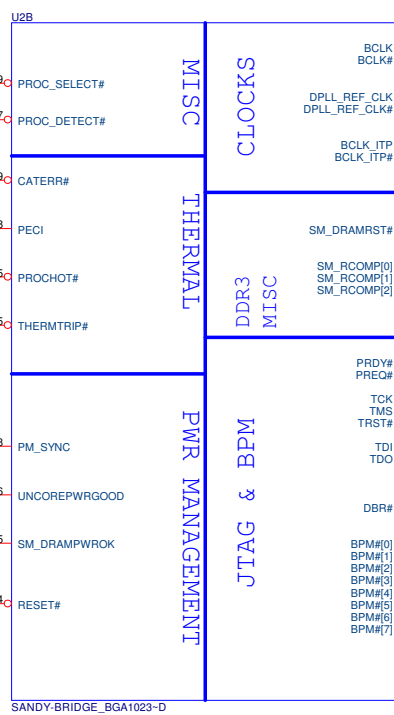
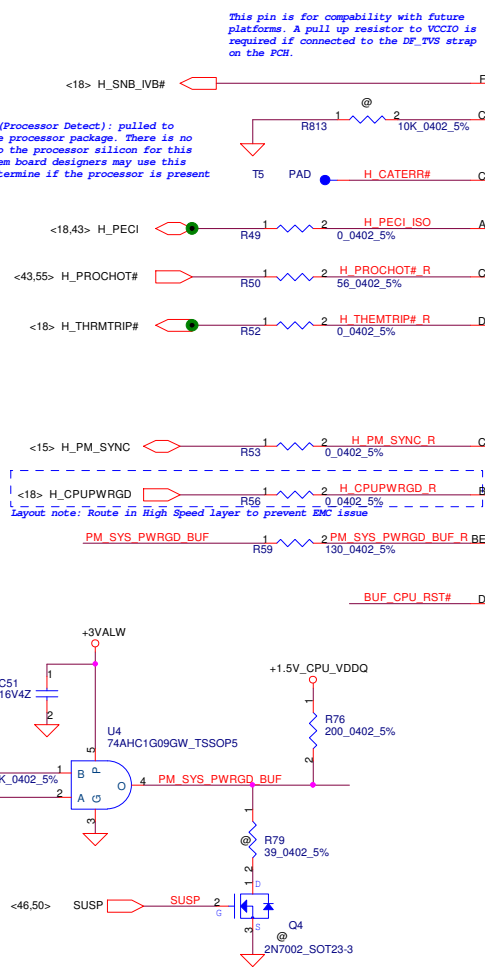
<b>Compal Electronics, Inc.</b>		
<b>PROCESSOR(I7) DMI,FDI,PEG</b>		
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Custom		
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PVT:Remove XDP connector for ESD request

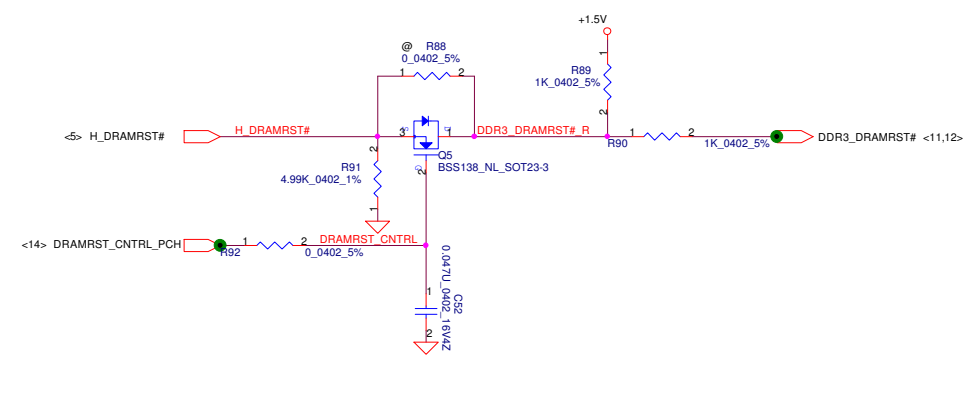
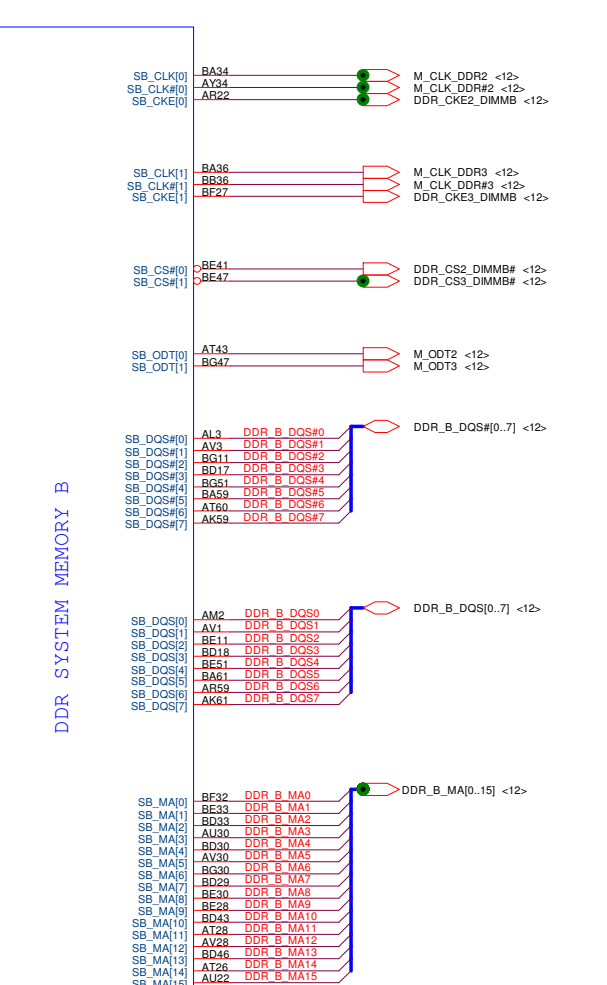
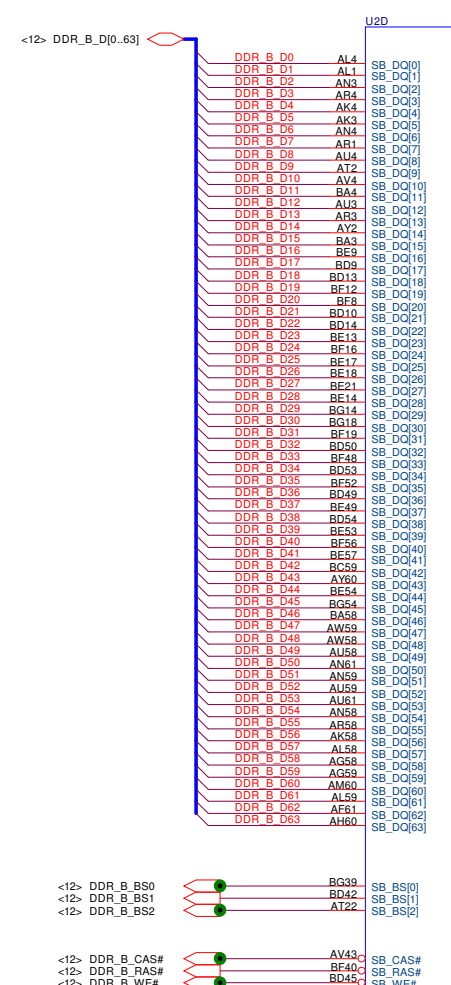
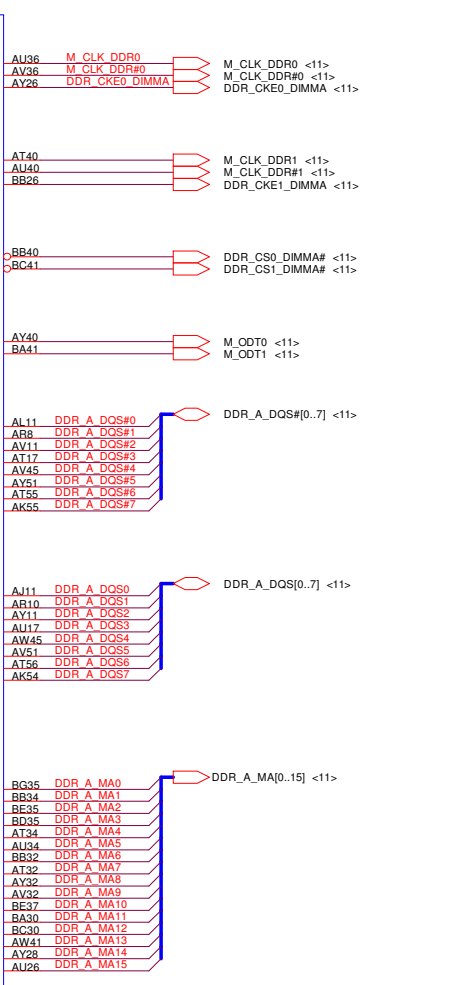
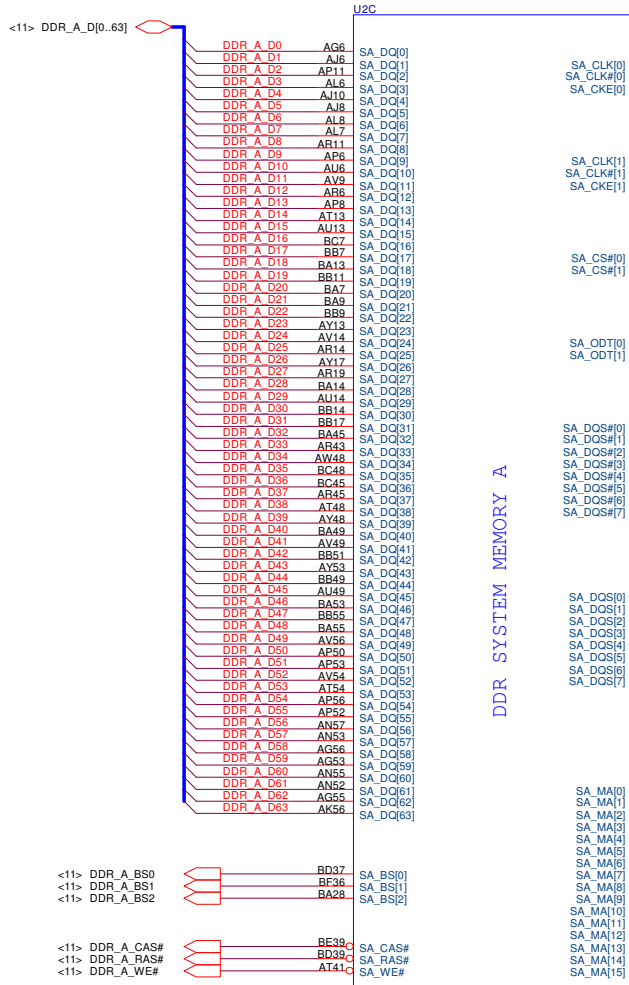
This pin is for compatibility with future platforms. A pull up resistor to VCCIO is required if connected to the DF\_TVS strap on the PCH.

PROC\_DETECT (Processor Detect): pulled to ground on the processor package. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present



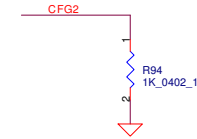
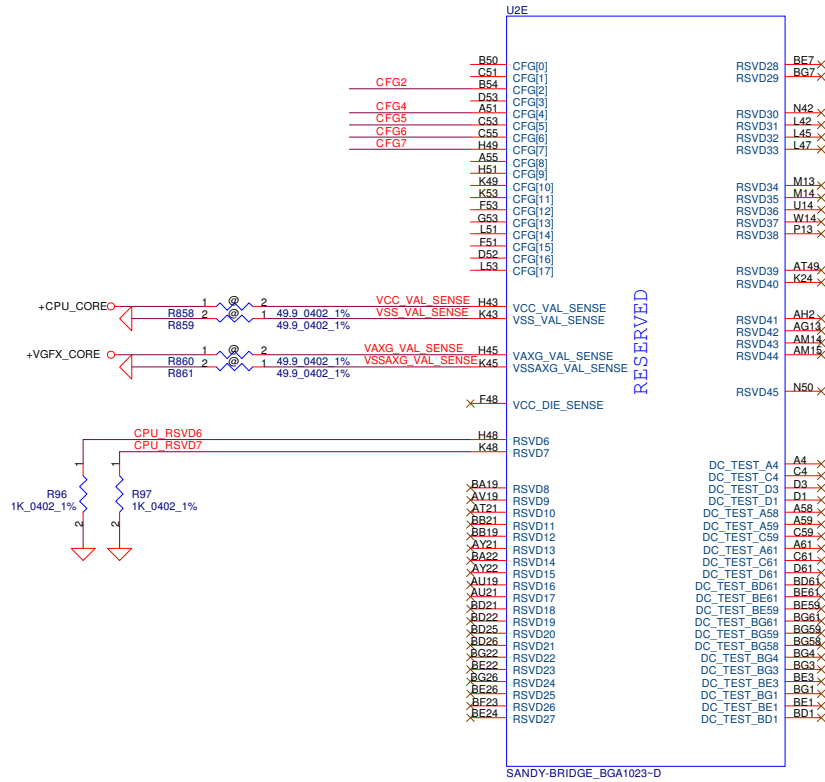
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Compal Electronics, Inc.		
PROCESSOR(2/7) PM,XDP,CLK		
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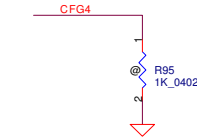


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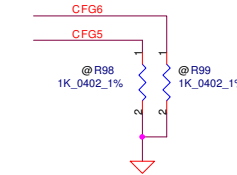
# CFG Straps for Processor



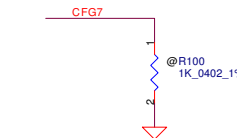
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



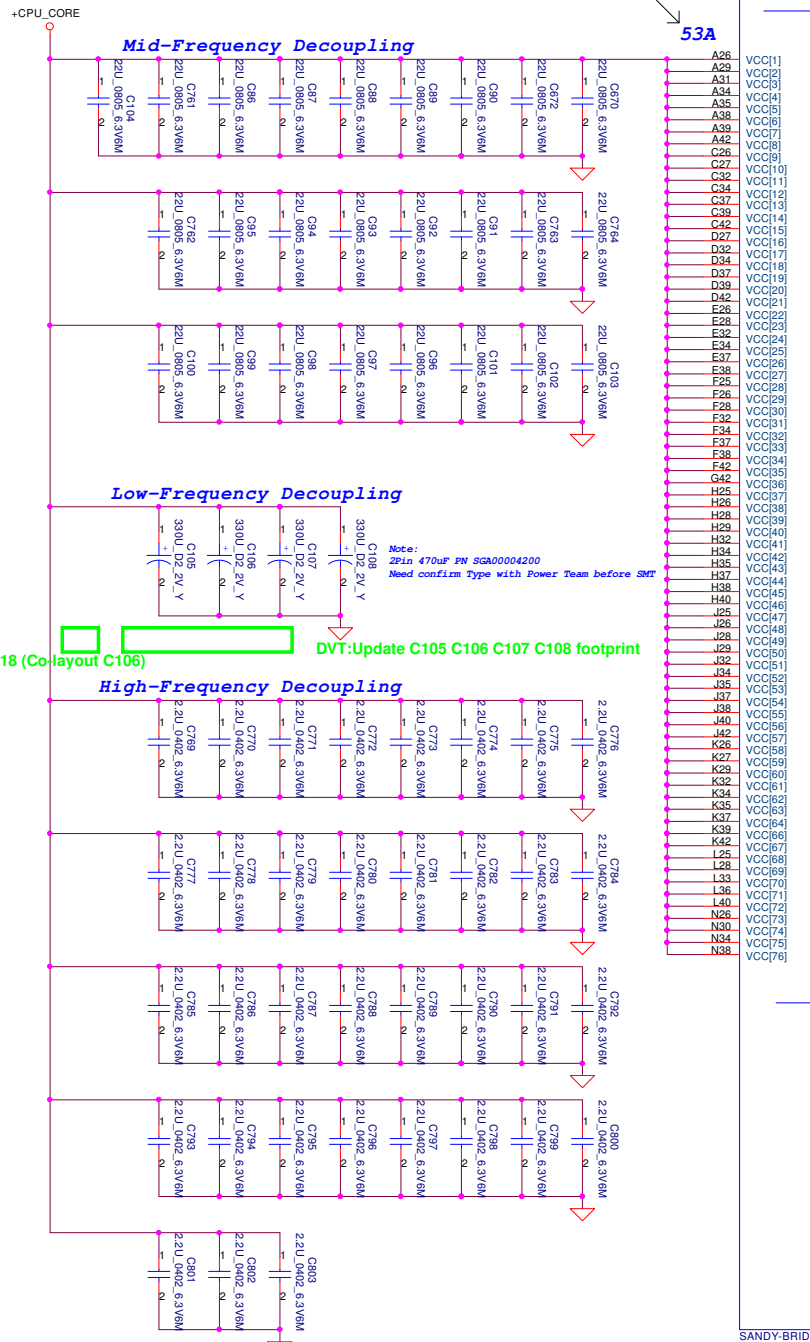
PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

1.9m [ Loadline Design

SV type CPU



DVT:Reserved C918 (Co-layout C106) □ □ □ □ DVT:Update C105 C106 C107 C108 footprint

Note:  
2Pin 470uF PN SGA00004200  
Need confirm Type with Power Team before SMT

CORE SUPPLY

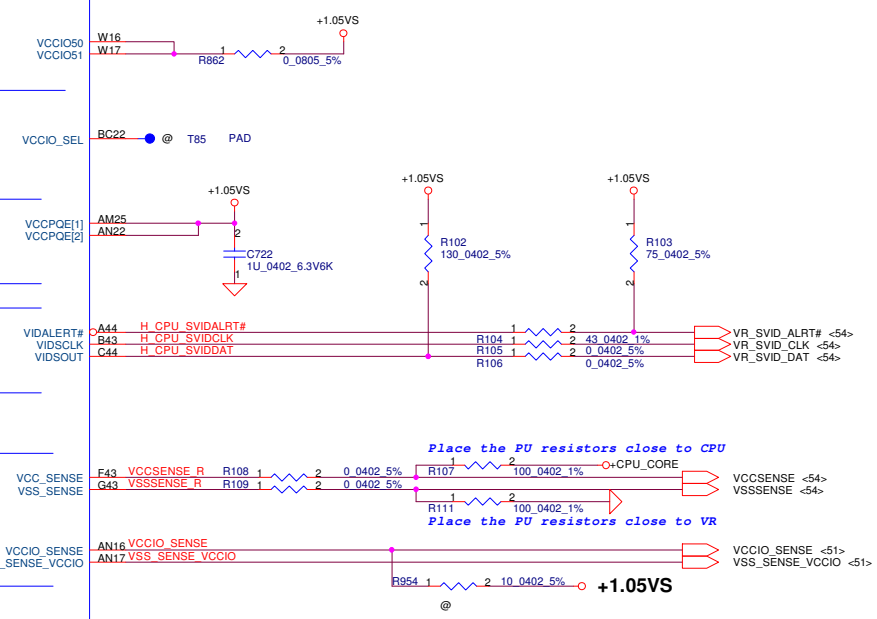
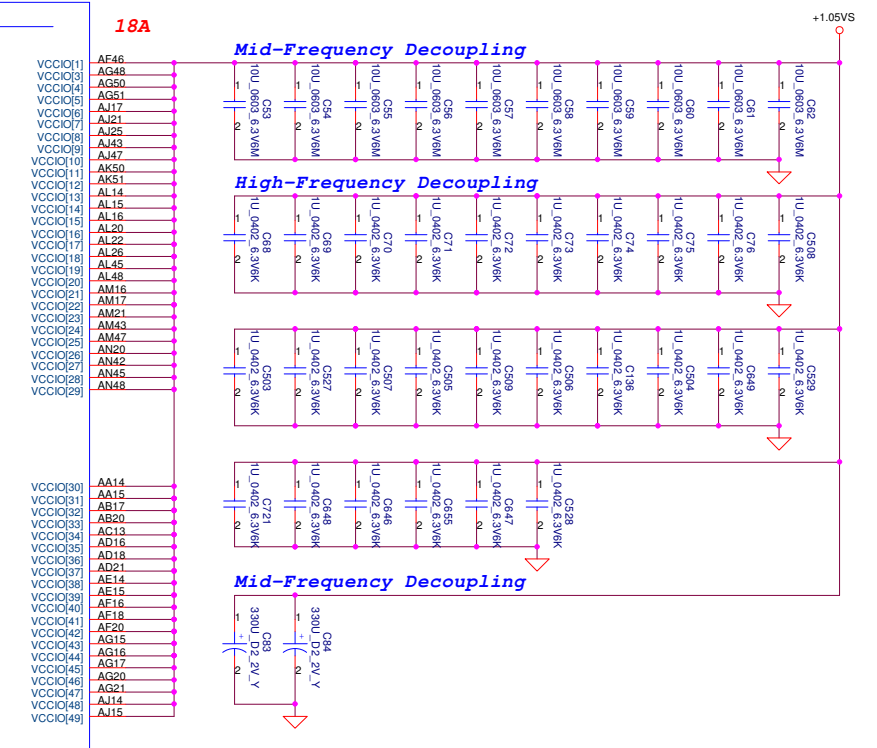
PEG AND DDR

POWER

QUIET RAILS

SVID

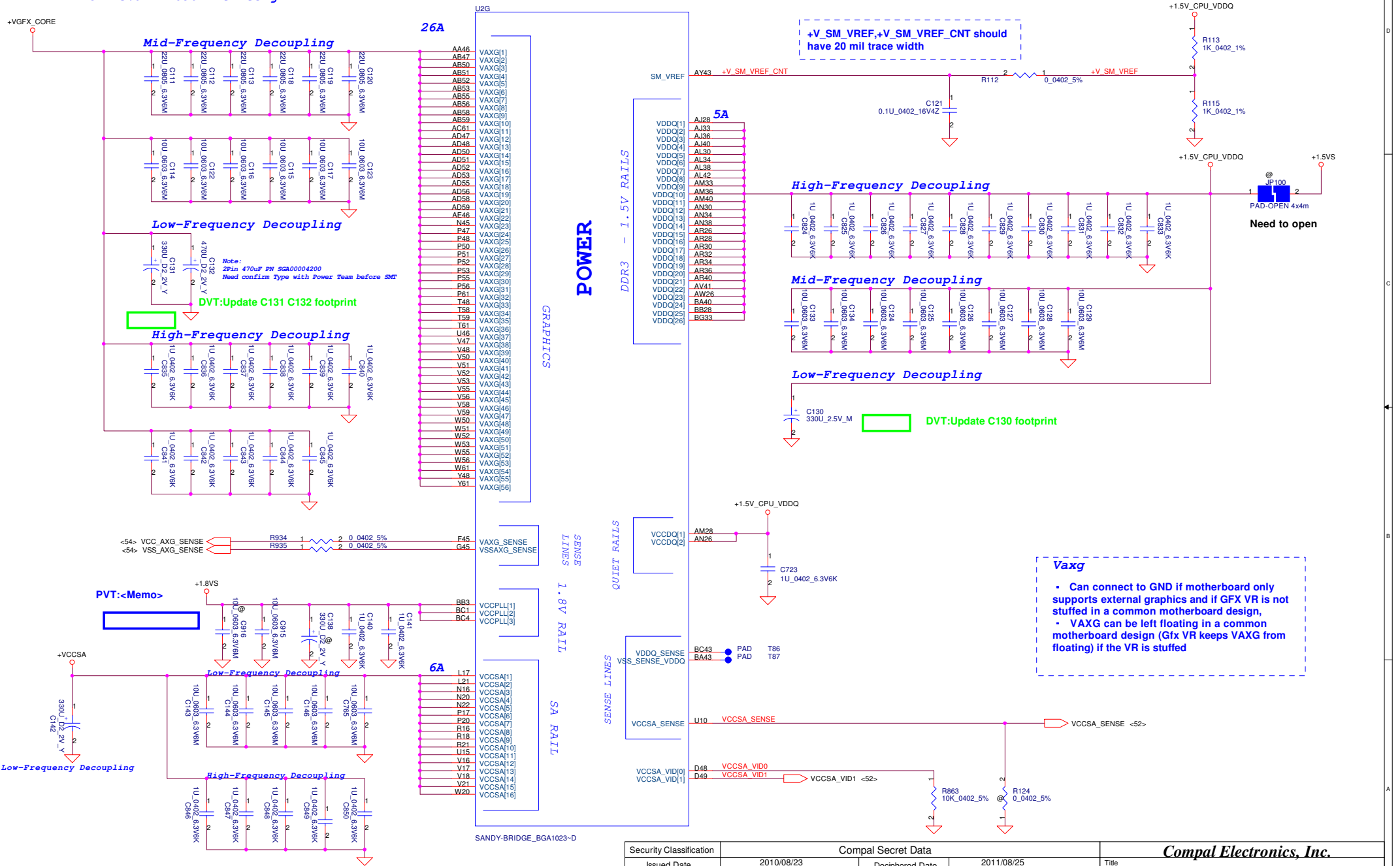
SENSE



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			<b>Compal Electronics, Inc.</b>	
			<b>PROCESSOR(S/7) PWR,BYPASS</b>	
Size	Document Number	Rev	1.0	
Custom		Date:	Sunday, April 10, 2011	Sheet 8 of 56

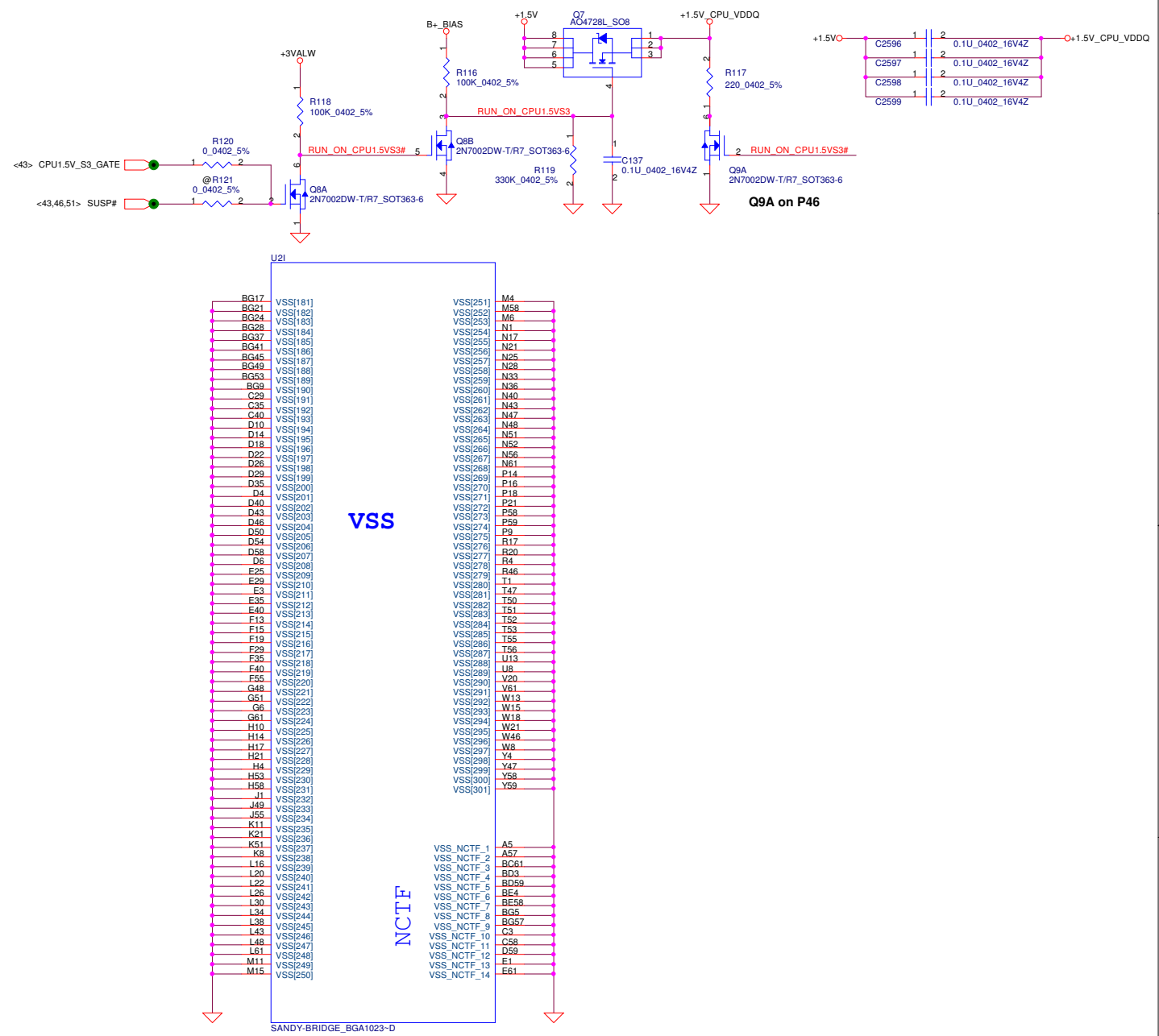
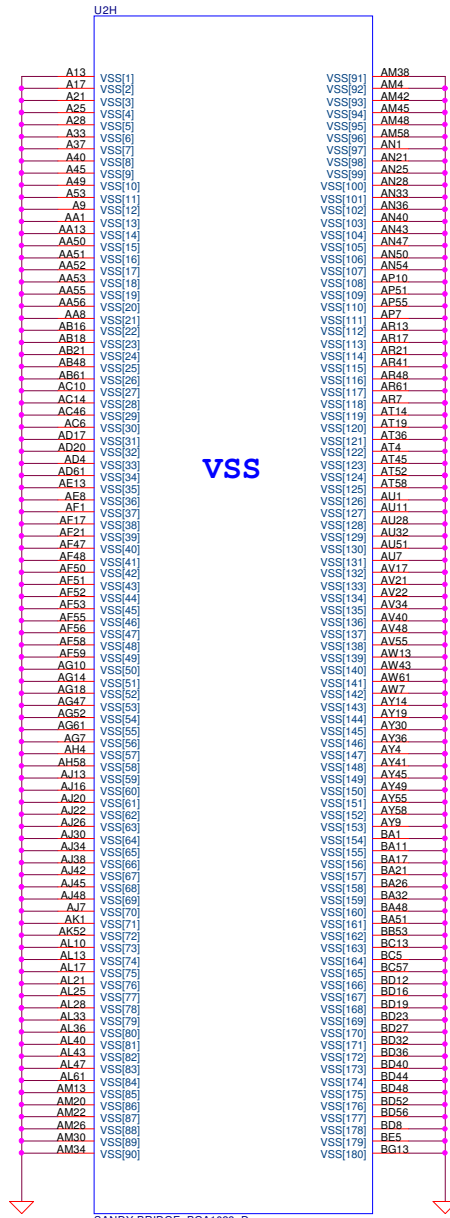


GT2 3.9mΩ Loadline Design



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Size	Document Number	Rev	1.0		
Date:	Sunday, April 10, 2011	Sheet	9	of 56	

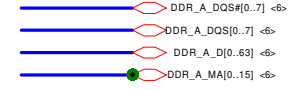
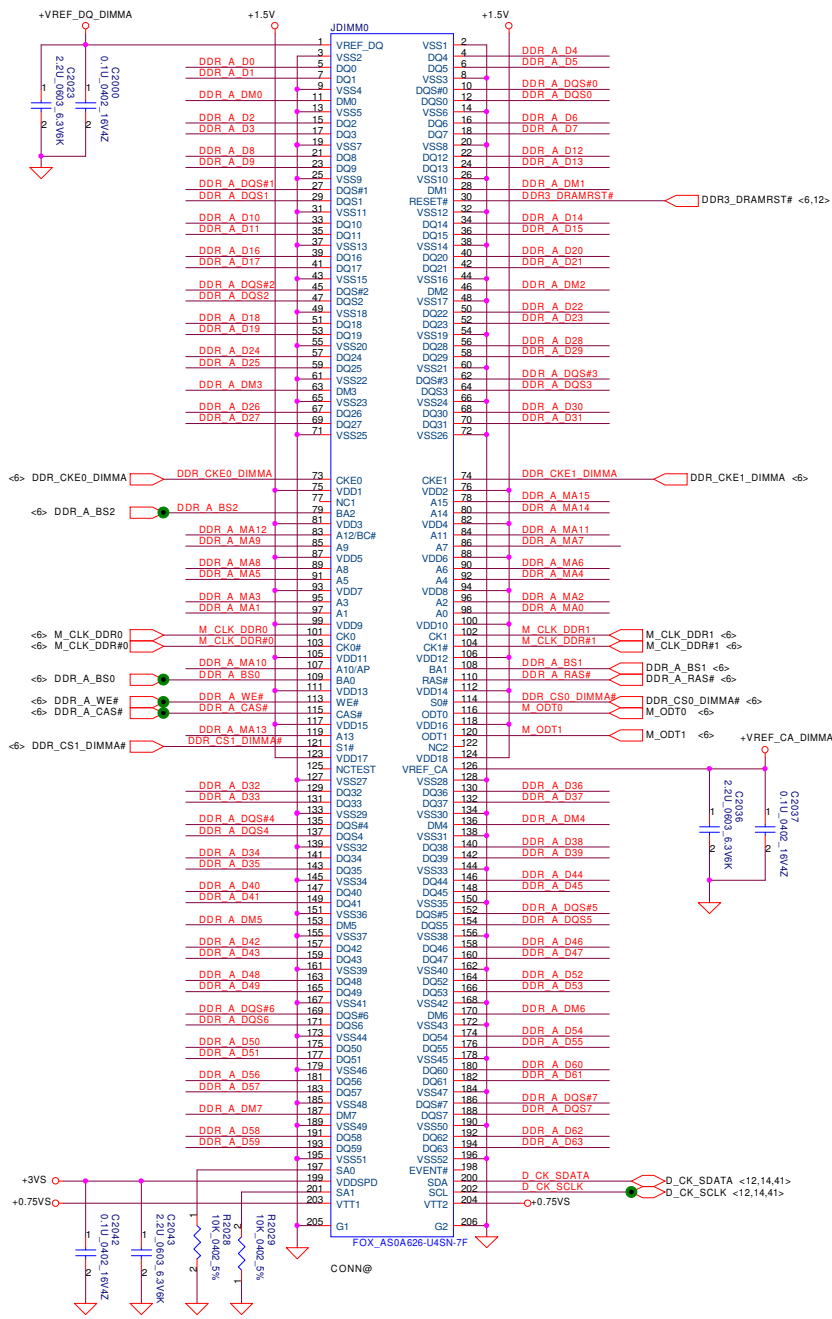
### +1.5V\_CPU\_VDDQ Source



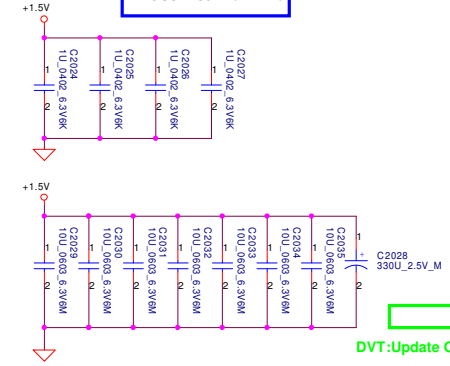
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Issued Date	2010/08/23	Deciphered Date
		2011/08/25
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<b>Compal Electronics, Inc.</b>		
<b>PROCESSOR(7/7) VSS</b>		
Size	Document Number	Rev
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Date:	Monday, April 11, 2011	Sheet 10 of 56

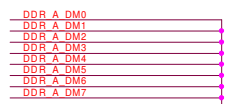
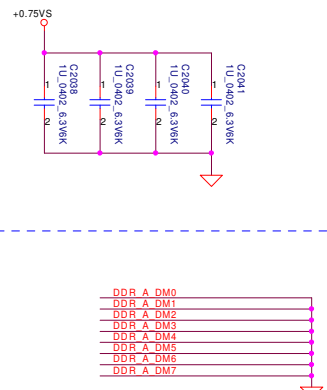
All VREF traces should have 10 mil trace width



**Layout Note:**  
Place near JDIMM0

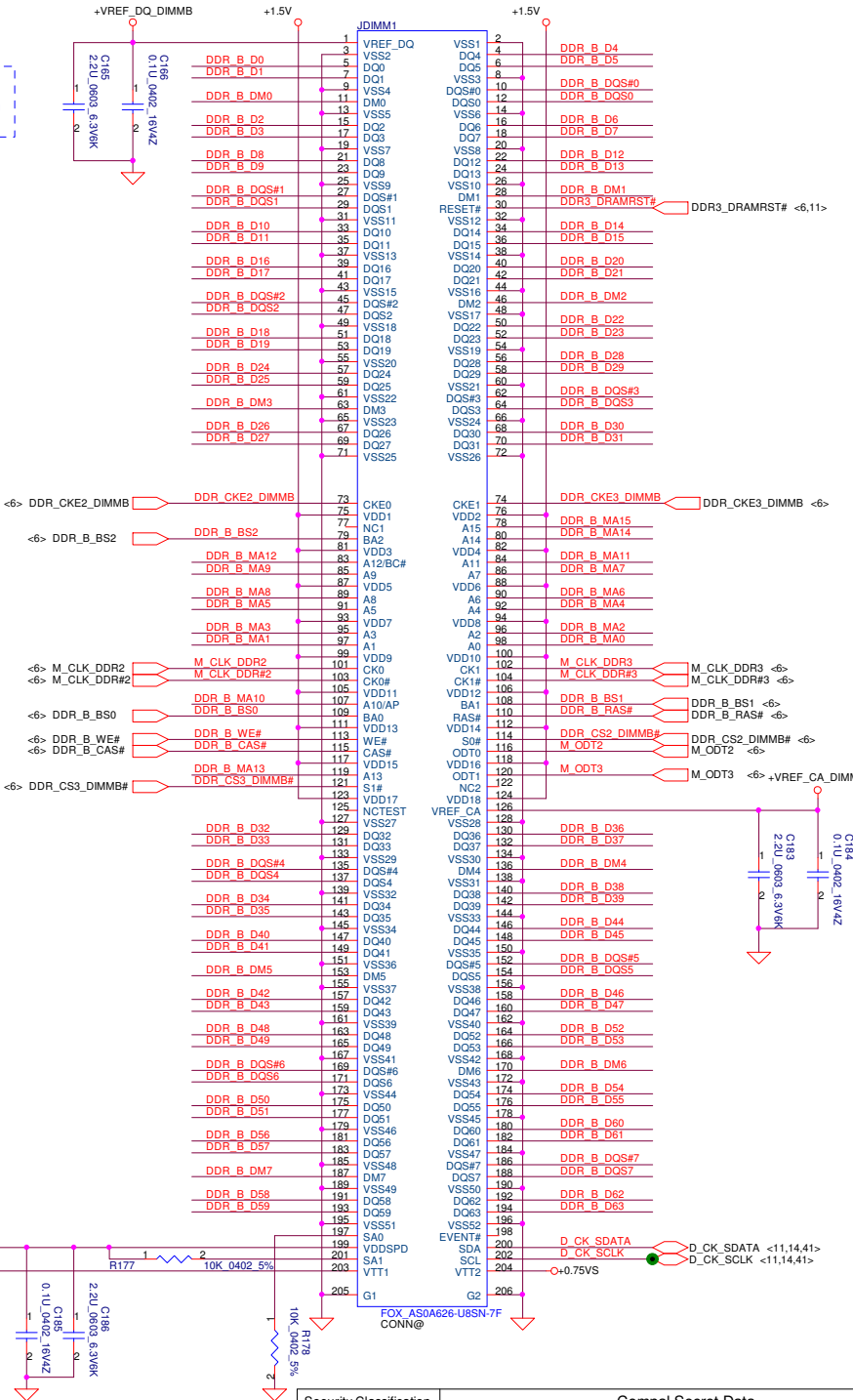


**Layout Note:**  
Place near JDIMM0. 203, 204



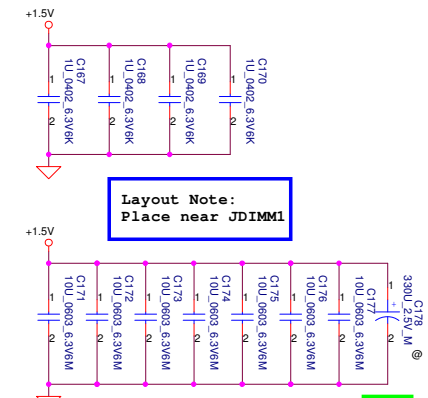
Security Classification		Compal Secret Data		Title	
Issued Date	2010/08/23	Deciphered Date	2011/08/25	DDR III DIMM	
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&amp;D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small>				Size	Rev
Customer	Document Number	LA-7141P		1.0	
Date:	Monday, April 11, 2011	Sheet	11	of	56

All VREF traces should have 10 mil trace width

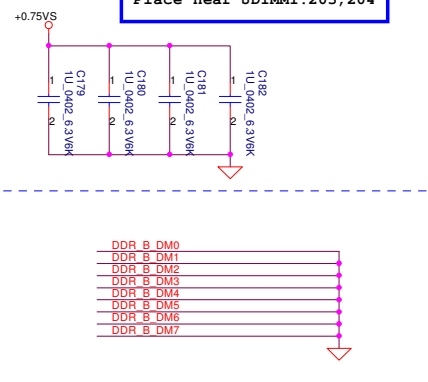


DDR\_B\_DQS#[0..7] <6>  
 DDR\_B\_DOS#[0..7] <6>  
 DDR\_B\_D6 <6>  
 DDR\_B\_D0[63] <6>  
 DDR\_B\_MAJ[0..15] <6>

Layout Note:  
Place near JDIMM1



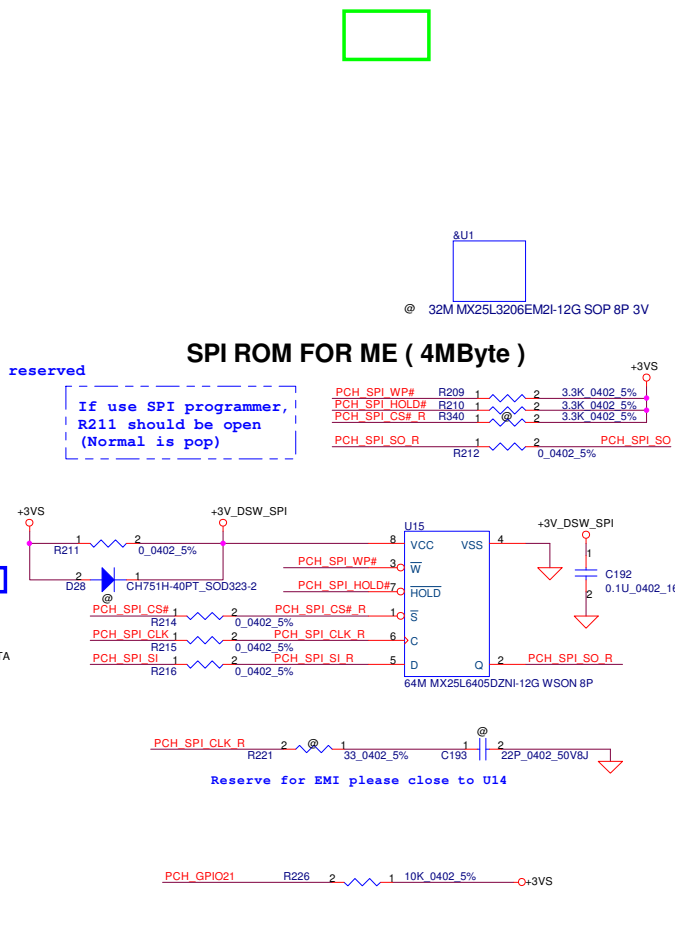
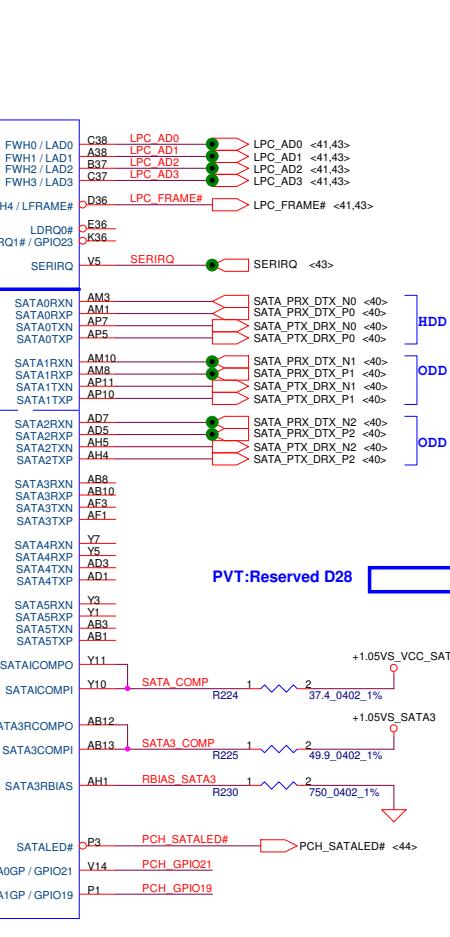
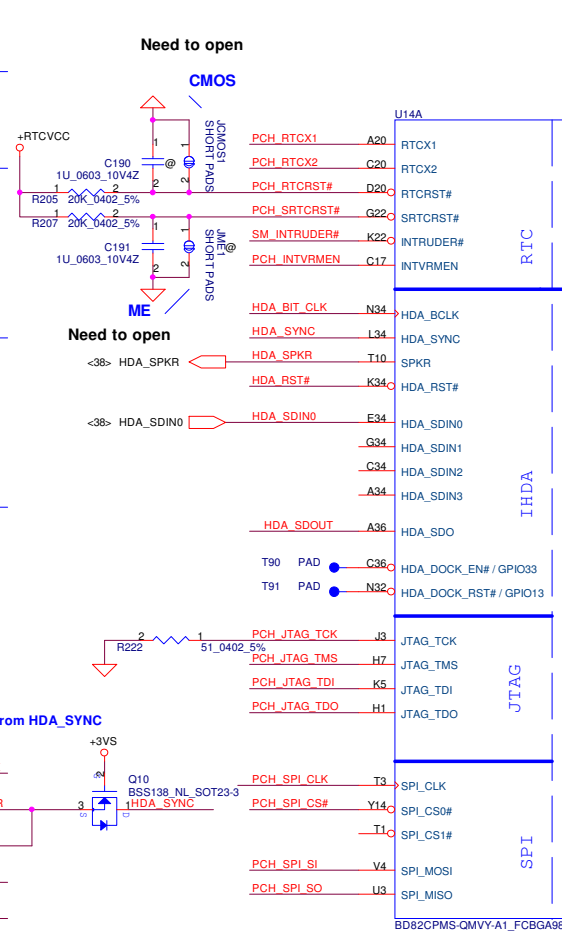
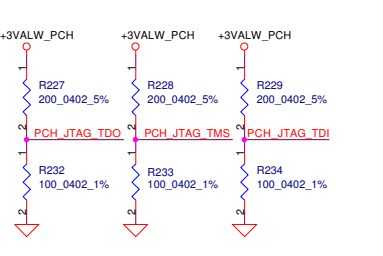
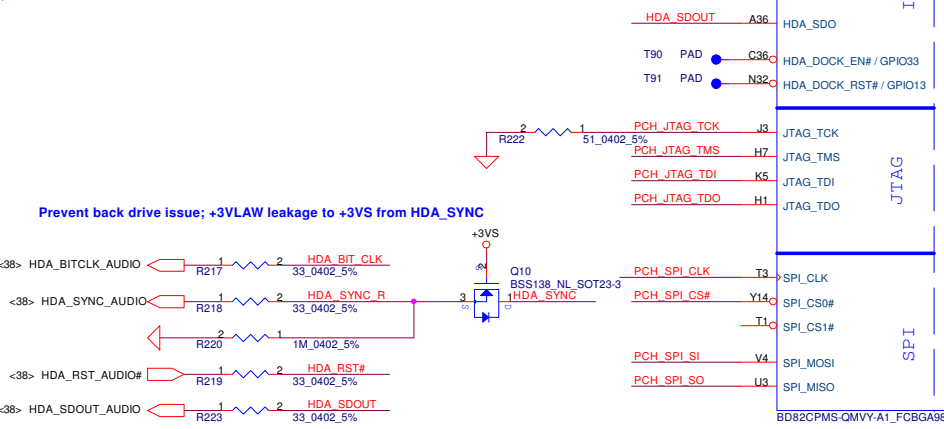
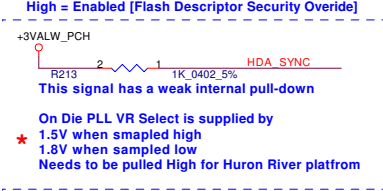
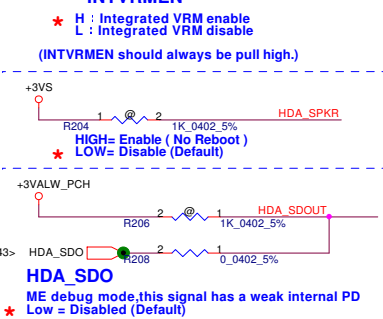
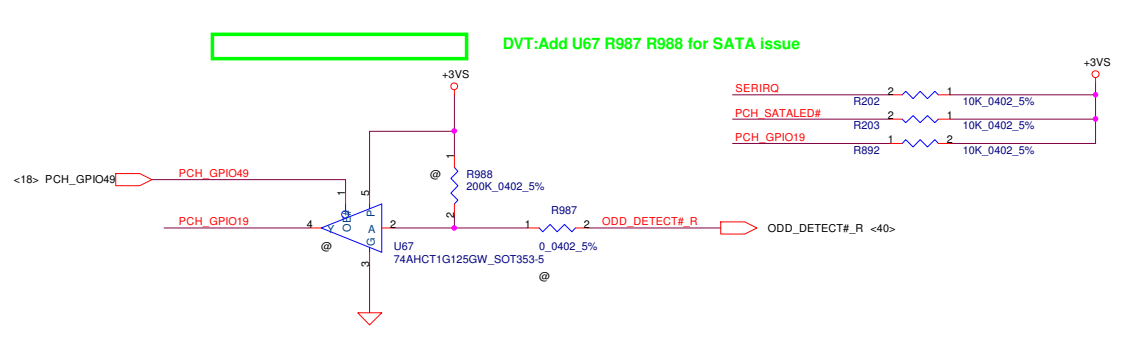
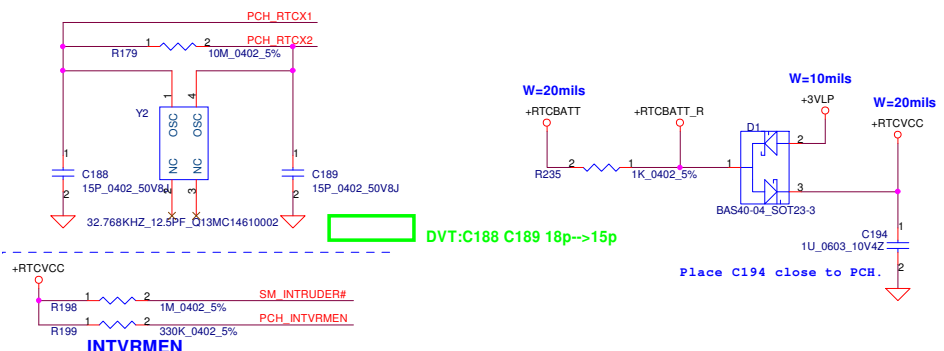
Layout Note:  
Place near JDIMM1.203,204



DDR\_B\_DM0  
 DDR\_B\_DM1  
 DDR\_B\_DM2  
 DDR\_B\_DM3  
 DDR\_B\_DM4  
 DDR\_B\_DM5  
 DDR\_B\_DM6  
 DDR\_B\_DM7

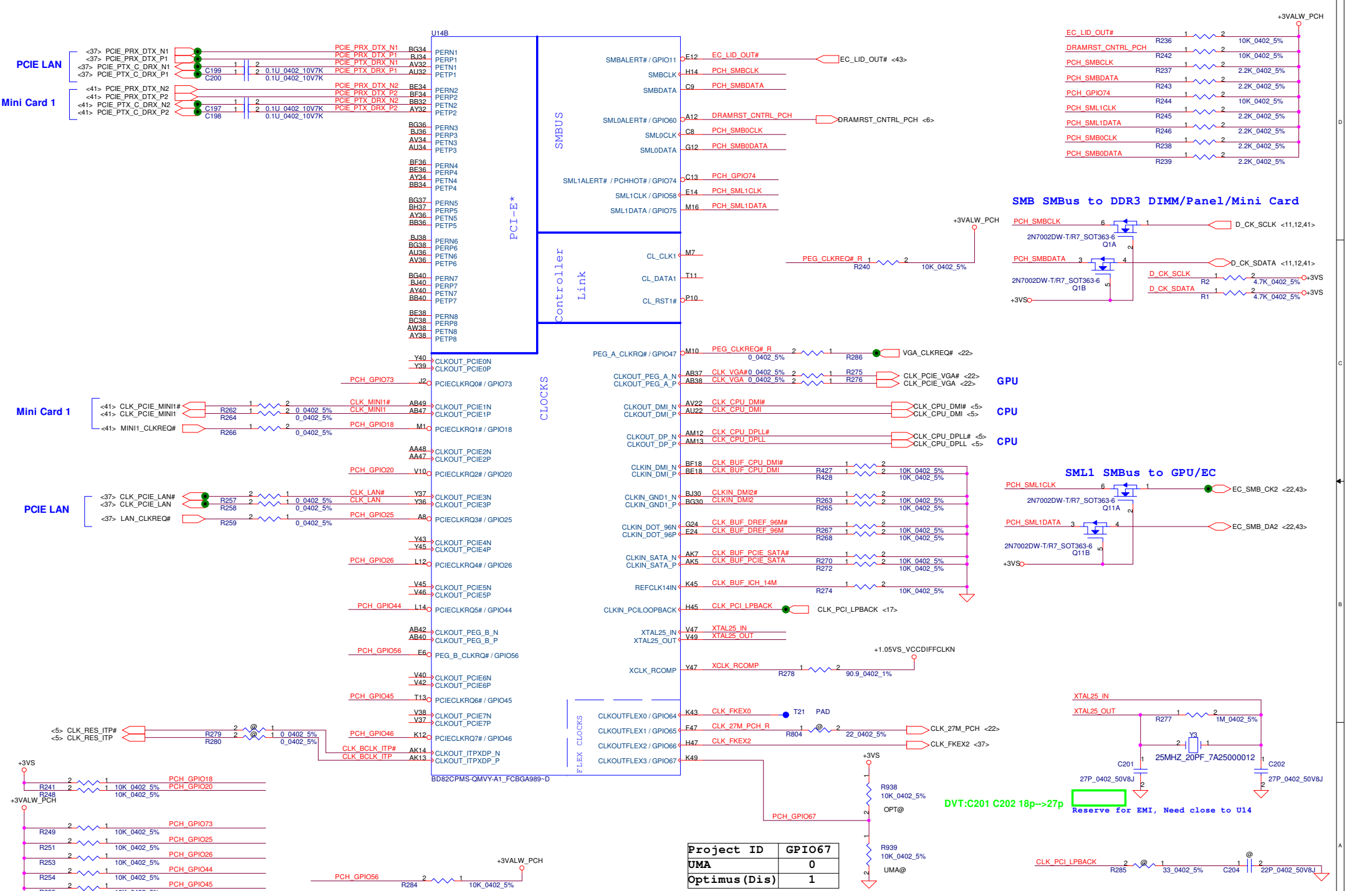
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/08/23	Deciphered Date	2011/08/25	Title	
				DDR3 DIMMB	
				Size	Document Number
				Custom	Rev 1.0
				Date	Monday, April 11, 2011
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**Compal Electronics, Inc.**  
**PCH (U/8) SATA, HDA, SPI, LPC, XDP**  
 Rev 1.0

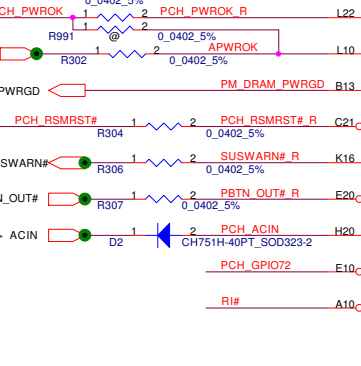
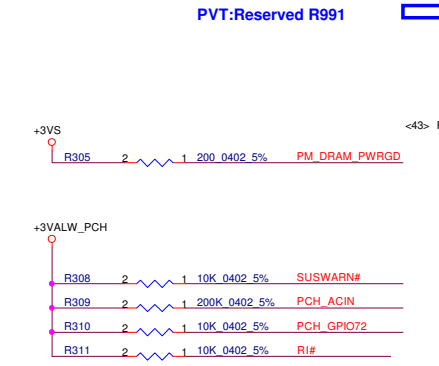
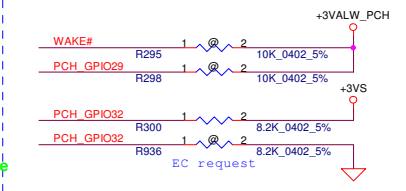
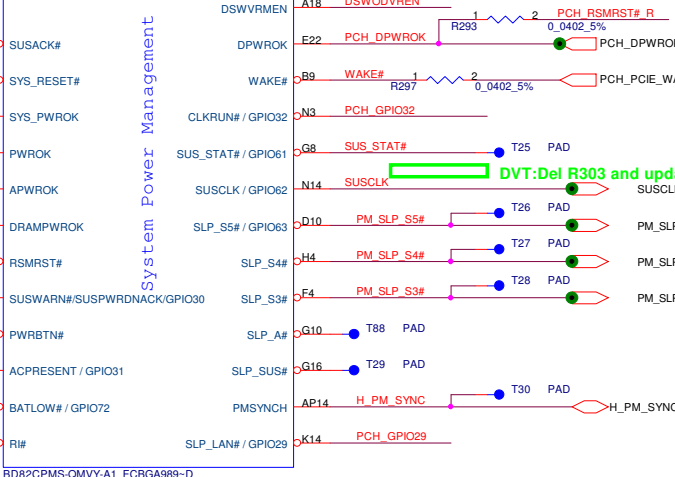
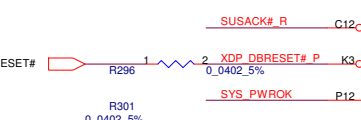
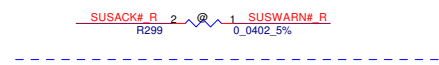
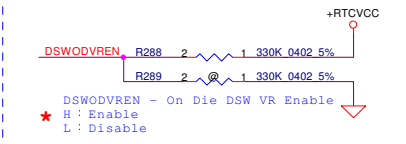
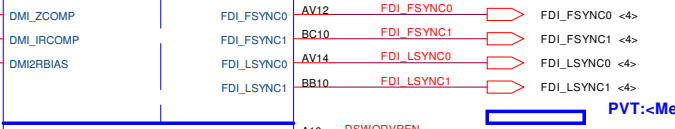
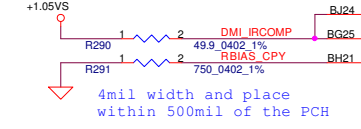
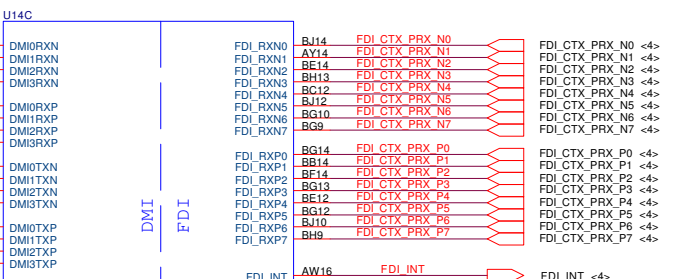
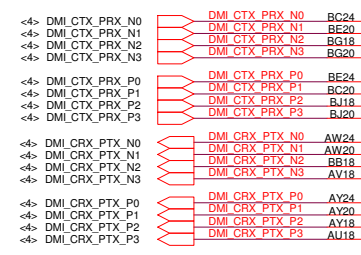
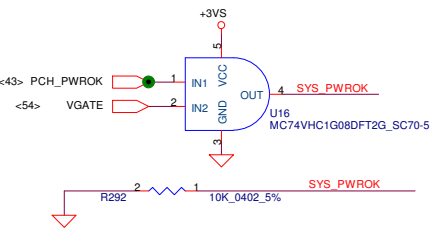


Project ID	GPIO67
UMA	0
Optimus (Dis)	1

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Issued Date	2010/08/23	Deciphered Date
		2011/08/25

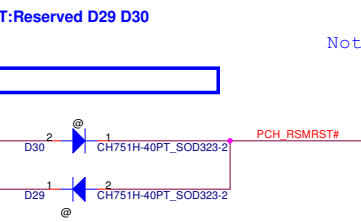
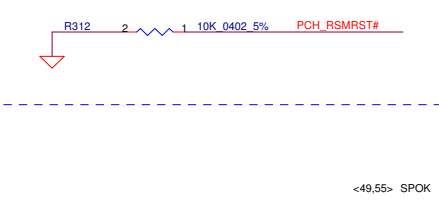
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<b>PCHE (2/8) PCIE, SMBUS, CLK</b>		
Title	Document Number	Rev
		1.0
Date:	Monday, April 11, 2011	Sheet 14 of 56



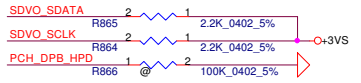
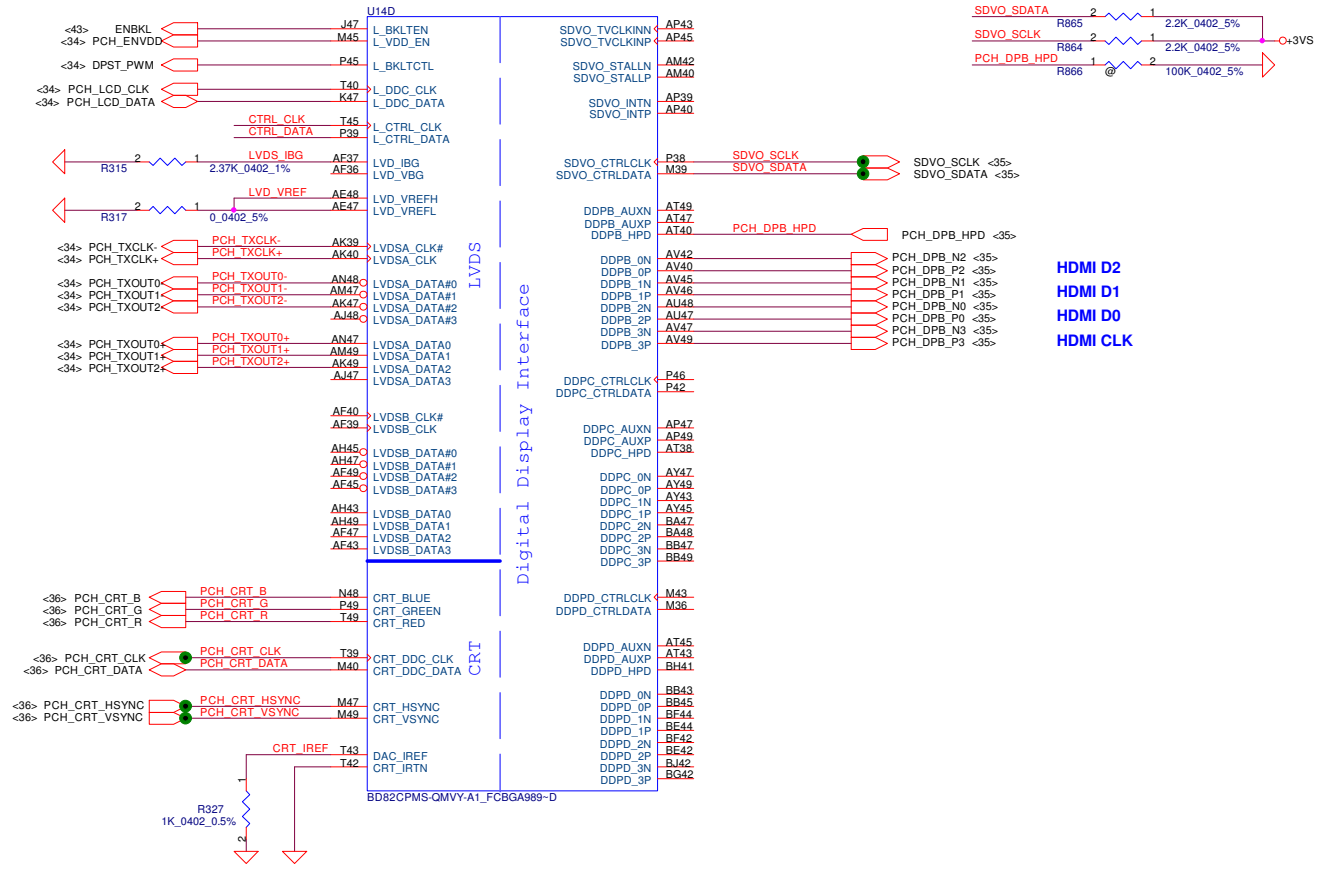
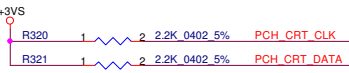
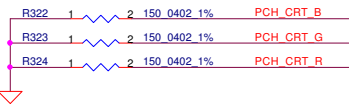
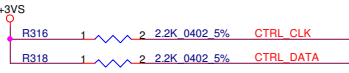
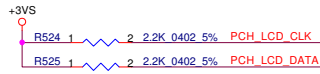
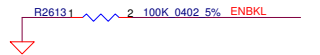
### Default DSW Enable

- Note:
- 1.SLP\_SUS and SUSACK# are NC if DSW is not supported
  - 2.DPWROK should connect to RSMRST# if DSW not supported
  - 3.The DSW rails must be stable for at least 10ms before DPWROK is asserted to PCH
- \*\*4.PCH\_DPWROK pull up to +V3S enables DSW wupport. No install R5261 to disable DSW



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Title <b>PCH (3/8) DMI, FDI, PM,</b>			
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HDMI D2  
HDMI D1  
HDMI D0  
HDMI CLK

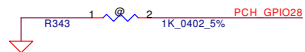
Security Classification	Compal Secret Data		Title	
Issued Date	2010/08/23	Deciphered Date	2011/08/25	Compal Electronics, Inc.
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Size	Document Number	Date	Monday, April 11, 2011	Rev 1.0
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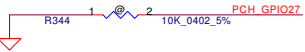
**GPIO28**  
On-Die PLL Voltage Regulator  
This signal has a weak internal pull up

- \* H : On-Die voltage regulator enable
- L : On-Die PLL Voltage Regulator disable

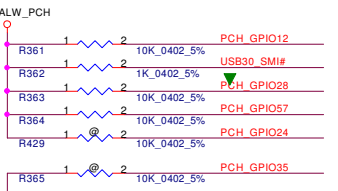
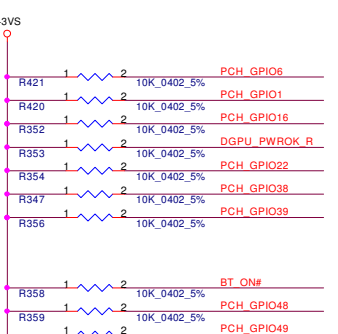


**GPIO27**  
PCH\_GPIO27 (Have internal Pull-High)

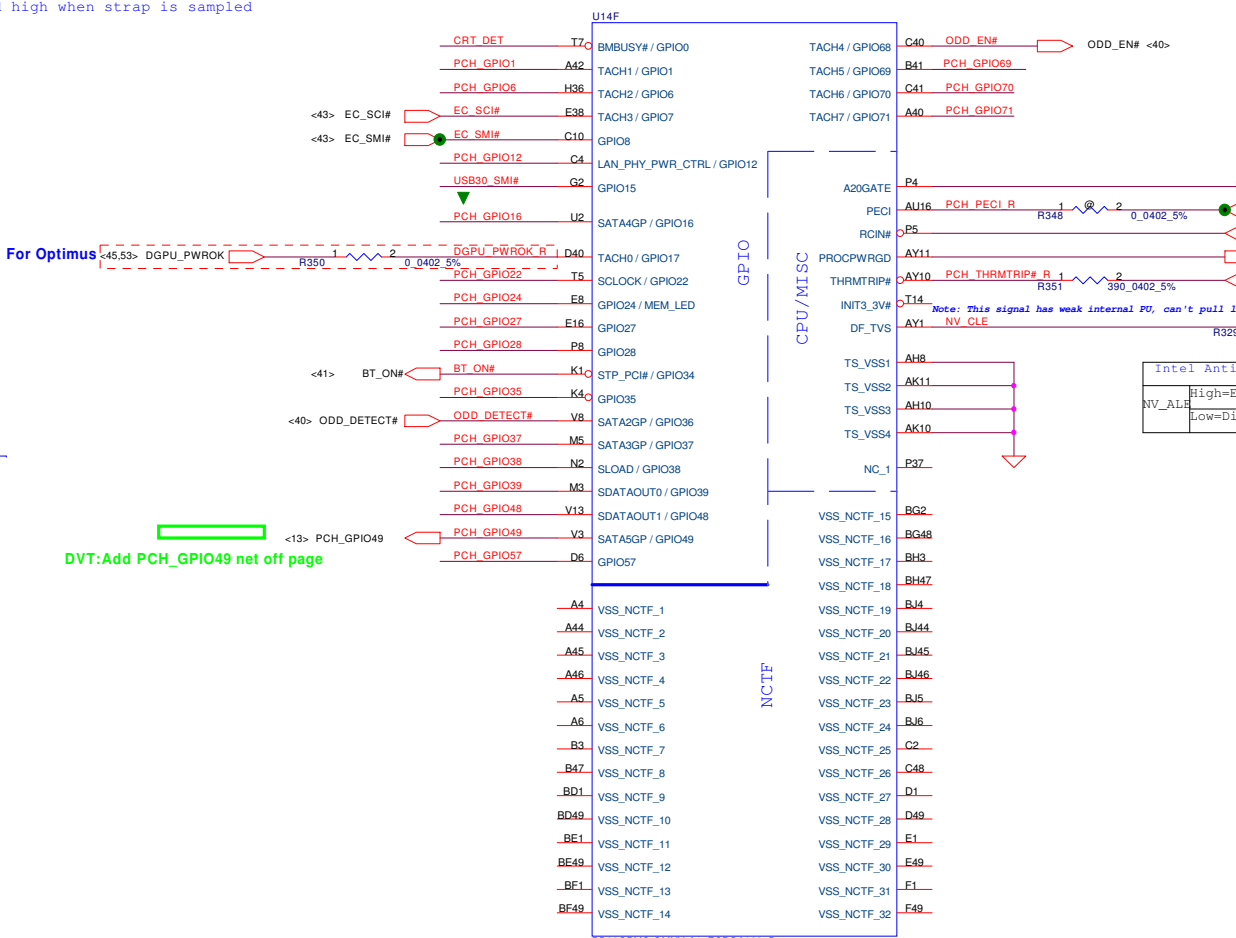
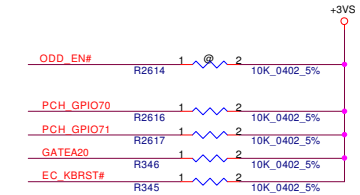
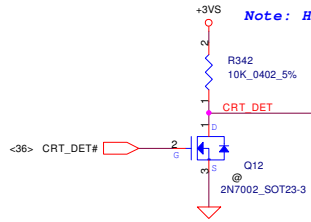
- \* High: VCCVRM VR Enable
- Low: VCCVRM VR Disable



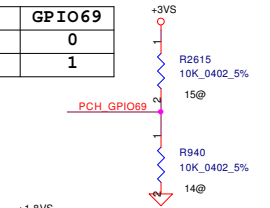
**SATA2GP/GPIO36 & SATA3GP/GPIO37**  
Sampled at Rising edge of PWROK.  
Weak internal pull-down. (weak internal pull-down is disabled after PLTRST# de-asserts)  
NOTE: This signal should NOT be pulled high when strap is sampled



Note: High - CRT Plugged



Project ID	GPIO69
14 "	0
15.6 "	1



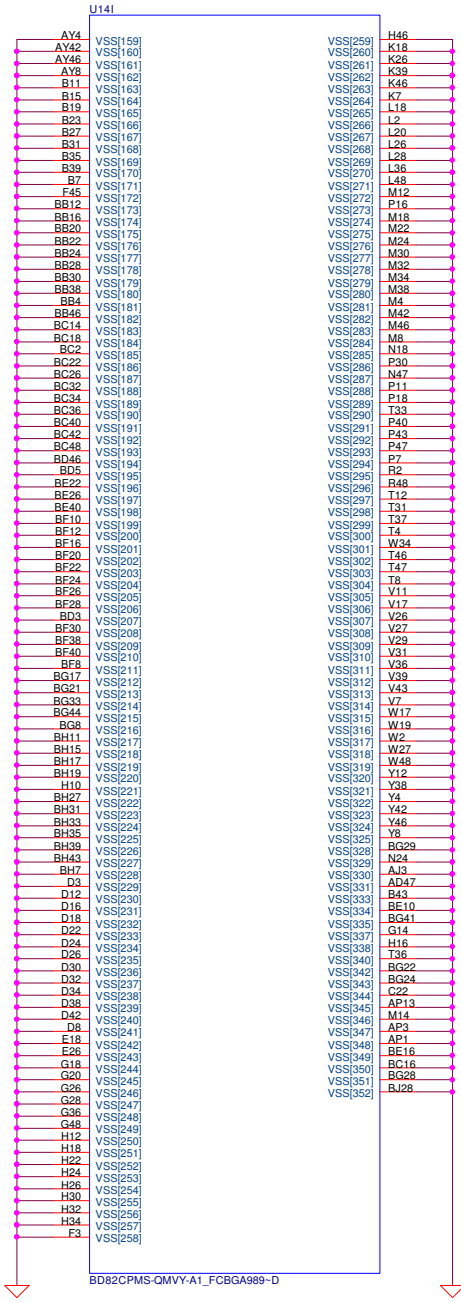
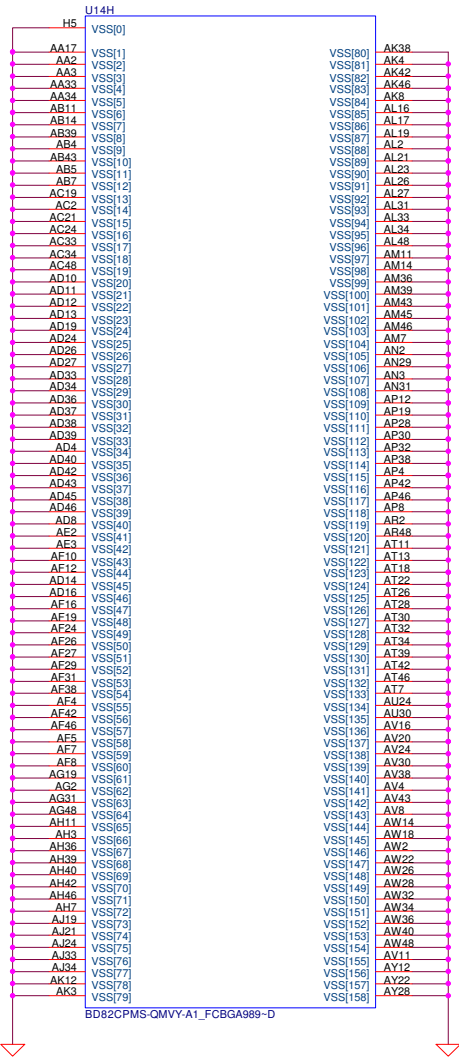
Intel Anti-Theft Technology	
NV_ALE	High=Endabled Low=Disable(floating) *

DVT:Add PCH\_GPIO49 net off page

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Size	Document Number	Rev		1.0	
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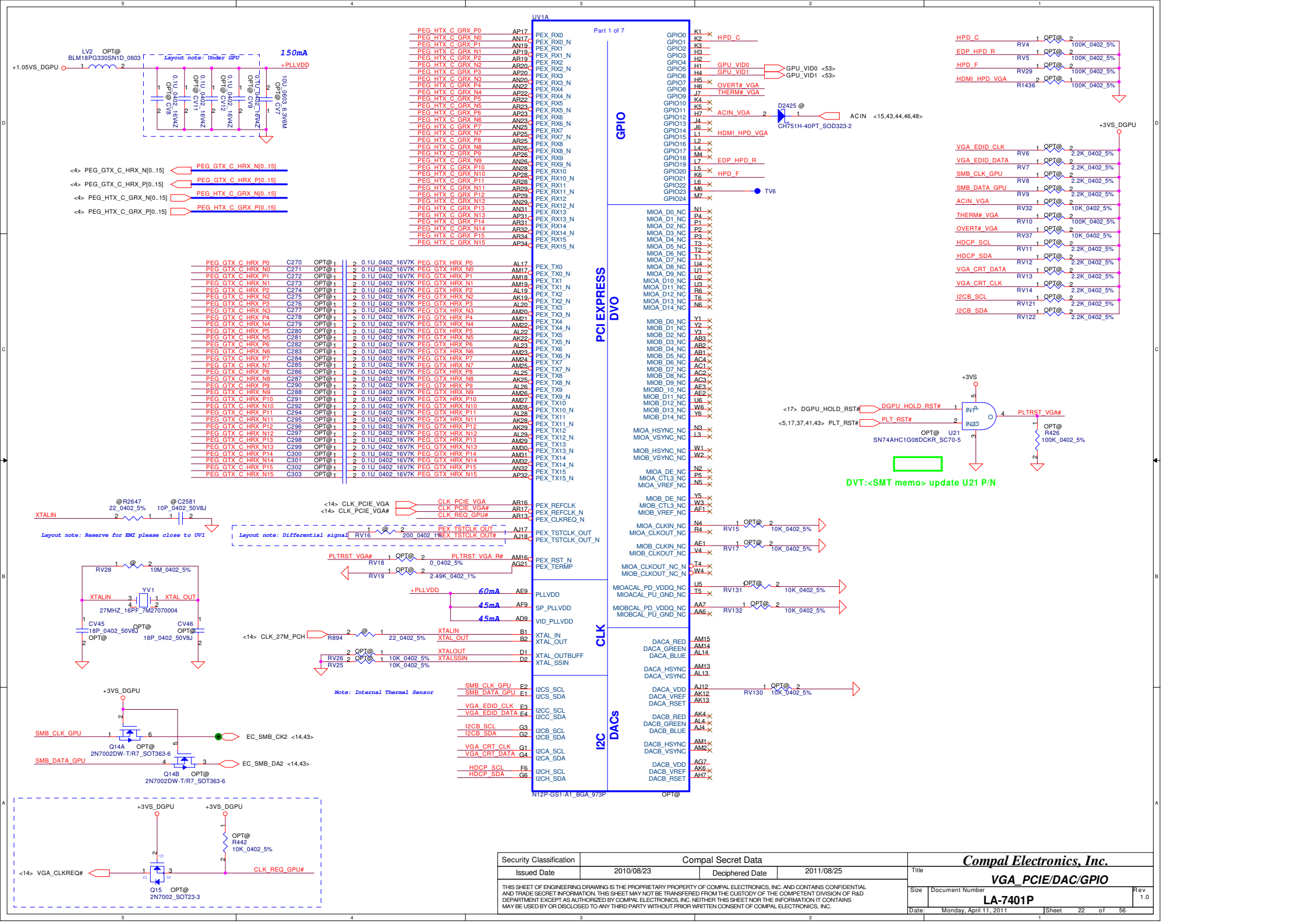






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Issued Date	2010/08/23	Deciphered Date	2011/08/25	
<p><b>Compal Electronics, Inc.</b></p> <p><b>PCMH (9/9) VSS</b></p>				
Title				Rev
Size				1.0
Custom				
Date:	Sunday, April 10, 2011	Sheet	21	of 56

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Part 1 of 7

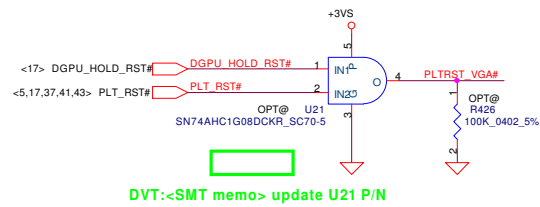
PEG HTX C GRX P0	AP17	PEX_RX0
PEG HTX C GRX P1	AN19	PEX_RX0_N
PEG HTX C GRX N1	AP19	PEX_RX1
PEG HTX C GRX P2	AR19	PEX_RX2
PEG HTX C GRX P3	AR20	PEX_RX2_N
PEG HTX C GRX N3	AN20	PEX_RX3
PEG HTX C GRX P4	AN22	PEX_RX3_N
PEG HTX C GRX M4	AP22	PEX_RX4
PEG HTX C GRX P5	AR22	PEX_RX4_N
PEG HTX C GRX N5	AN23	PEX_RX5
PEG HTX C GRX P6	AP23	PEX_RX5_N
PEG HTX C GRX N6	AN24	PEX_RX6
PEG HTX C GRX P7	AN25	PEX_RX6_N
PEG HTX C GRX N7	AP25	PEX_RX7
PEG HTX C GRX P8	AR25	PEX_RX7_N
PEG HTX C GRX M8	AP26	PEX_RX8
PEG HTX C GRX P9	AP26	PEX_RX8_N
PEG HTX C GRX N9	AN26	PEX_RX9
PEG HTX C GRX P10	AN28	PEX_RX9_N
PEG HTX C GRX M10	AP28	PEX_RX10
PEG HTX C GRX P11	AR28	PEX_RX10_N
PEG HTX C GRX N11	AR29	PEX_RX11
PEG HTX C GRX P12	AP29	PEX_RX11_N
PEG HTX C GRX N12	AN29	PEX_RX12
PEG HTX C GRX P13	AN31	PEX_RX12_N
PEG HTX C GRX N13	AP31	PEX_RX13
PEG HTX C GRX M14	AP31	PEX_RX13_N
PEG HTX C GRX N14	AR32	PEX_RX14
PEG HTX C GRX P15	AR34	PEX_RX14_N
PEG HTX C GRX N15	AP34	PEX_RX15

PEG GTX C HRX P0	C270	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX P0	AL17	PEX_TX0
PEG GTX C HRX N0	C271	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX N0	AM17	PEX_TX0_N
PEG GTX C HRX P1	C272	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX P1	AM18	PEX_TX1
PEG GTX C HRX N1	C273	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX N1	AM19	PEX_TX1_N
PEG GTX C HRX P2	C274	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX P2	AL19	PEX_TX2
PEG GTX C HRX N2	C275	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX N2	AK19	PEX_TX2_N
PEG GTX C HRX P3	C276	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX P3	AL20	PEX_TX3
PEG GTX C HRX N3	C277	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX N3	AM20	PEX_TX3_N
PEG GTX C HRX P4	C278	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX P4	AM21	PEX_TX4
PEG GTX C HRX N4	C279	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX N4	AM22	PEX_TX4_N
PEG GTX C HRX P5	C280	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX P5	AL22	PEX_TX5
PEG GTX C HRX N5	C281	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX N5	AK22	PEX_TX5_N
PEG GTX C HRX P6	C282	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX P6	AL23	PEX_TX6
PEG GTX C HRX N6	C283	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX N6	AM24	PEX_TX7
PEG GTX C HRX P7	C284	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX P7	AM24	PEX_TX7_N
PEG GTX C HRX N7	C285	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX N7	AM25	PEX_TX8
PEG GTX C HRX P8	C286	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX P8	AL25	PEX_TX8_N
PEG GTX C HRX N8	C287	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX N8	AK25	PEX_TX9
PEG GTX C HRX P9	C290	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX P9	AL26	PEX_TX9_N
PEG GTX C HRX N9	C288	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX N9	AM26	PEX_TX10
PEG GTX C HRX P10	C291	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX P10	AM27	PEX_TX10_N
PEG GTX C HRX N10	C292	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX N10	AL28	PEX_TX11
PEG GTX C HRX P11	C294	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX P11	AM28	PEX_TX11_N
PEG GTX C HRX N11	C295	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX N11	AK28	PEX_TX12
PEG GTX C HRX P12	C296	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX P12	AK29	PEX_TX12_N
PEG GTX C HRX N12	C297	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX N12	AL29	PEX_TX13
PEG GTX C HRX P13	C298	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX P13	AM29	PEX_TX13_N
PEG GTX C HRX N13	C299	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX N13	AM30	PEX_TX14
PEG GTX C HRX P14	C300	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX P14	AM31	PEX_TX14_N
PEG GTX C HRX N14	C301	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX N14	AM32	PEX_TX15
PEG GTX C HRX P15	C302	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX P15	AN32	PEX_TX15_N
PEG GTX C HRX N15	C303	OPT@1	2	0.1U	0402	16V7K	PEG GTX HRX N15	AP32	PEX_TX15_N

GPI00	K1	X	HPD C
GPI01	K2	X	HPD R
GPI02	K3	X	HPD F
GPI03	H2	X	GPU_VID0
GPI04	H1	X	GPU_VID1
GPI05	H4	X	GPU_VID0 <53>
GPI06	H2	X	GPU_VID1 <53>
GPI07	H5	X	OVER7# VGA
GPI08	H6	X	THERM# VGA
GPI09	J7	X	
GPI10	K4	X	ACIN VGA
GPI11	K5	X	ACIN <15,43,44,46,48>
GPI12	H7	X	ACIN <15,43,44,46,48>
GPI13	J4	X	CH751H-40PT_SOD323-2
GPI14	J6	X	HDMI_HPD_VGA
GPI15	L1	X	
GPI16	L2	X	
GPI17	L4	X	EDP_HPD_R
GPI18	L7	X	HPD_F
GPI19	L5	X	
GPI20	K6	X	
GPI21	L6	X	
GPI22	M6	X	
GPI23	M7	X	
GPI24	M7	X	

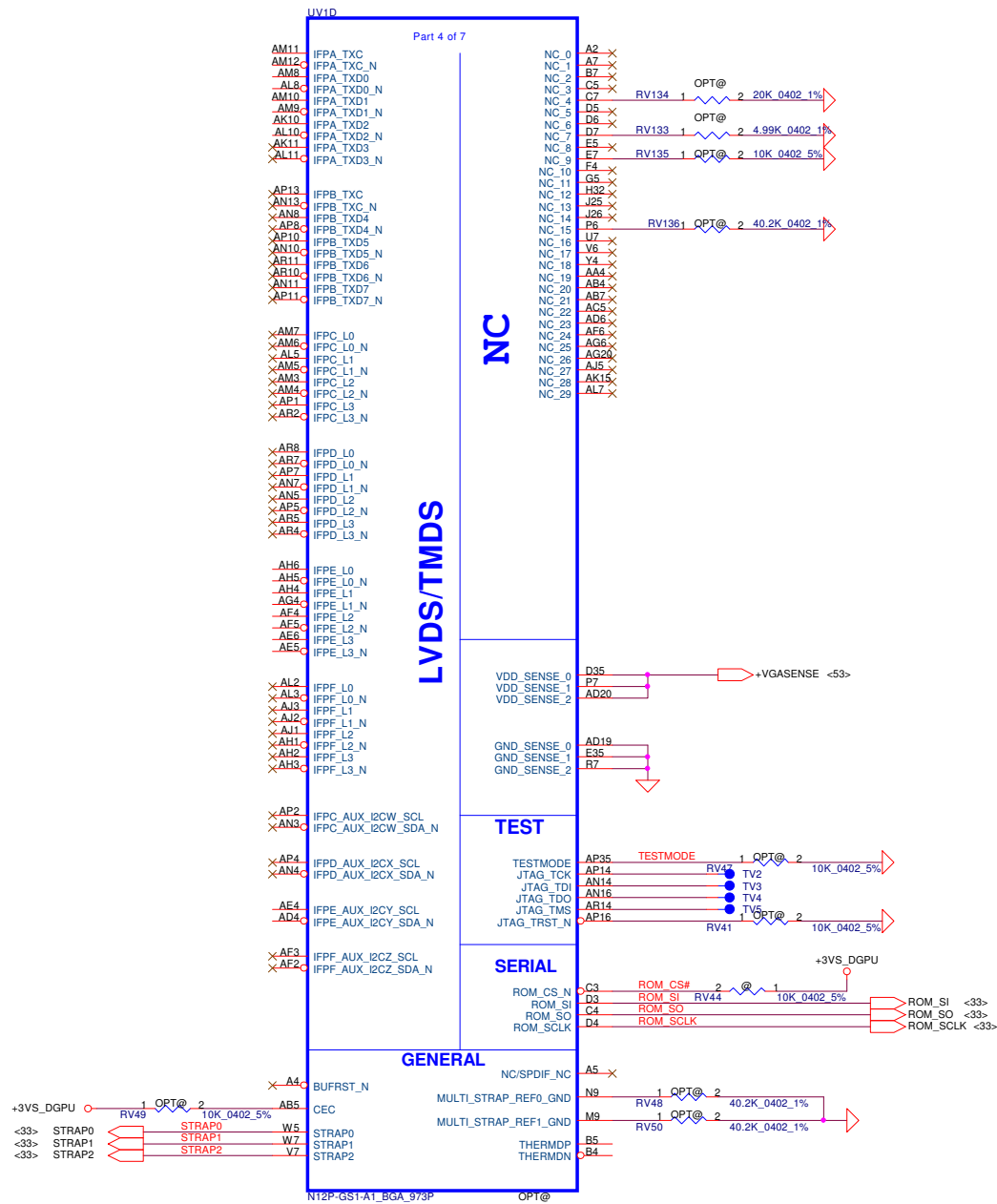
MIOA_D0_NC	N1	X	
MIOA_D1_NC	P4	X	
MIOA_D2_NC	P1	X	
MIOA_D3_NC	P2	X	
MIOA_D4_NC	P3	X	
MIOA_D5_NC	T3	X	
MIOA_D6_NC	T2	X	
MIOA_D7_NC	T1	X	
MIOA_D8_NC	L4	X	
MIOA_D9_NC	L1	X	
MIOA_D10_NC	L3	X	
MIOA_D11_NC	R6	X	
MIOA_D12_NC	L6	X	
MIOA_D13_NC	T8	X	
MIOA_D14_NC	N6	X	
MIOB_D0_NC	Y1	X	
MIOB_D1_NC	Y2	X	
MIOB_D2_NC	AB2	X	
MIOB_D3_NC	AB3	X	
MIOB_D4_NC	AB2	X	
MIOB_D5_NC	AB1	X	
MIOB_D6_NC	AC4	X	
MIOB_D7_NC	AC1	X	
MIOB_D8_NC	AC2	X	
MIOB_D9_NC	AC3	X	
MIOB_D10_NC	AE2	X	
MIOB_D11_NC	AE3	X	
MIOB_D12_NC	UE	X	
MIOB_D13_NC	WE	X	
MIOB_D14_NC	VE	X	
MIOA_HSYNC_NC	N3	X	
MIOA_VSYNC_NC	L3	X	
MIOB_HSYNC_NC	W1	X	
MIOB_VSYNC_NC	W2	X	
MIOA_DE_NC	N2	X	
MIOA_CTL3_NC	P5	X	
MIOA_VREF_NC	N5	X	
MIOB_DE_NC	Y5	X	
MIOB_CTL3_NC	W3	X	
MIOB_VREF_NC	AF1	X	
MIOA_CLKIN_NC	N4	X	
MIOA_CLKOUT_NC	R4	X	
MIOB_CLKIN_NC	AE1	X	
MIOB_CLKOUT_NC	V4	X	
MIOA_CLKOUT_NC	T4	X	
MIOB_CLKOUT_NC	W4	X	
MIOACAL_PD_VDDQ_NC	LU5	X	
MIOACAL_PD_VDDQ_NC	TV	X	
MIOBCAL_PD_VDDQ_NC	AA7	X	
MIOBCAL_PD_VDDQ_NC	AA6	X	
DACA_RED	AM15	X	
DACA_GREEN	AM14	X	
DACA_BLUE	AL14	X	
DACA_HSYNC	AM13	X	
DACA_VSYNC	AL13	X	
DACA_VDD	AJ12	X	
DACA_VREF	AK12	X	
DACA_RSET	AK13	X	
DACB_RED	AK4	X	
DACB_GREEN	AL4	X	
DACB_BLUE	AL4	X	
DACB_HSYNC	AM1	X	
DACB_VSYNC	AM2	X	
DACB_VDD	AG7	X	
DACB_VREF	AK6	X	
DACB_RSET	AK7	X	

HPD_C	RV4	1	OPT@	2	100K_0402_5%
EDP_HPD_R	RV5	1	OPT@	2	100K_0402_5%
HPD_F	RV29	1	OPT@	2	100K_0402_5%
HDMI_HPD_VGA	R1436	2	OPT@	2	100K_0402_5%
VGA_EDID_CLK	RV6	1	OPT@	2	2.2K_0402_5%
VGA_EDID_DATA	RV7	1	OPT@	2	2.2K_0402_5%
SMB_CLK_GPU	RV8	1	OPT@	2	2.2K_0402_5%
SMB_DATA_GPU	RV9	2	OPT@	2	2.2K_0402_5%
ACIN_VGA	RV32	1	OPT@	2	10K_0402_5%
THERM#_VGA	RV10	1	OPT@	2	100K_0402_5%
OVER7#_VGA	RV37	1	OPT@	2	10K_0402_5%
HDPC_SCL	RV11	1	OPT@	2	2.2K_0402_5%
HDPC_SDA	RV12	2	OPT@	2	2.2K_0402_5%
VGA_CRT_DATA	RV13	1	OPT@	2	2.2K_0402_5%
VGA_CRT_CLK	RV14	1	OPT@	2	2.2K_0402_5%
I2CB_SCL	RV121	2	OPT@	2	2.2K_0402_5%
I2CB_SDA	RV122	1	OPT@	2	2.2K_0402_5%



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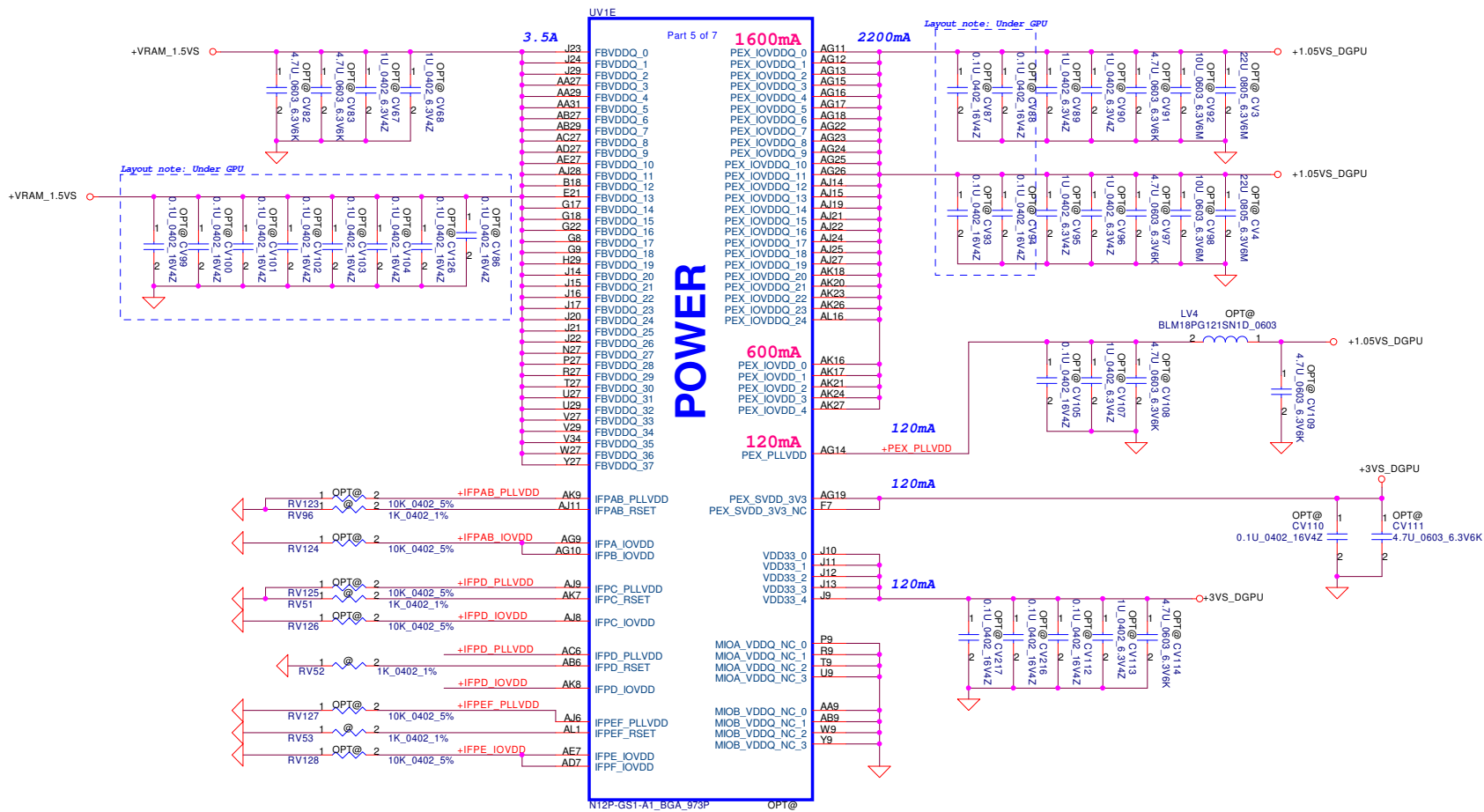
Compal Electronics, Inc.			
VGA_PCIE/DAC/GPIO			
Size	Document Number	Rev	1.0
	LA-7401P		
Date:	Monday, April 11, 2011	Sheet	22 of 56



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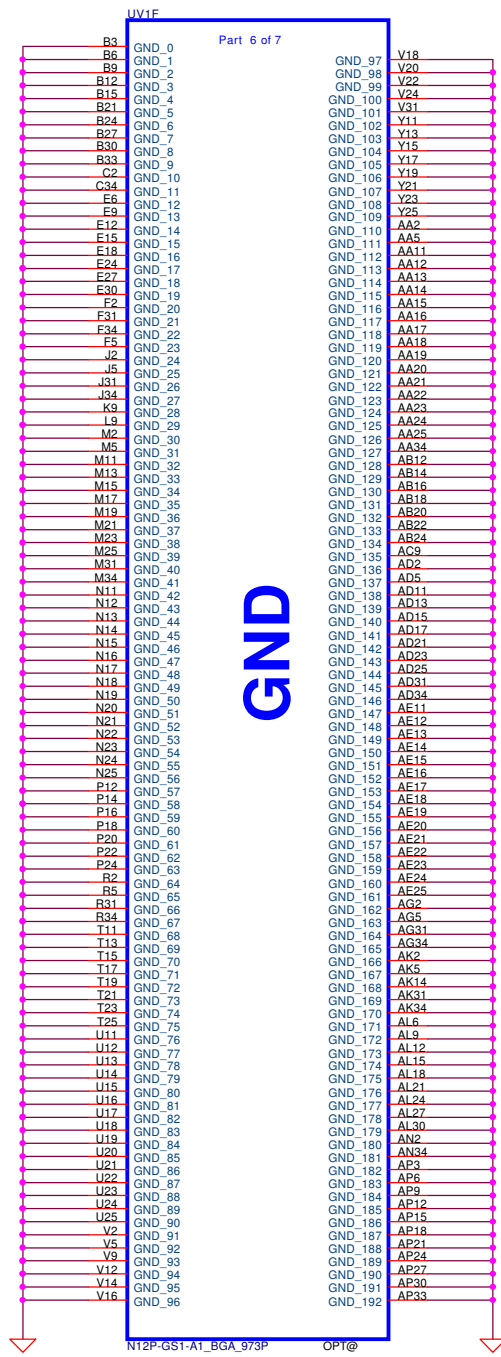


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**VGA\_POWER**

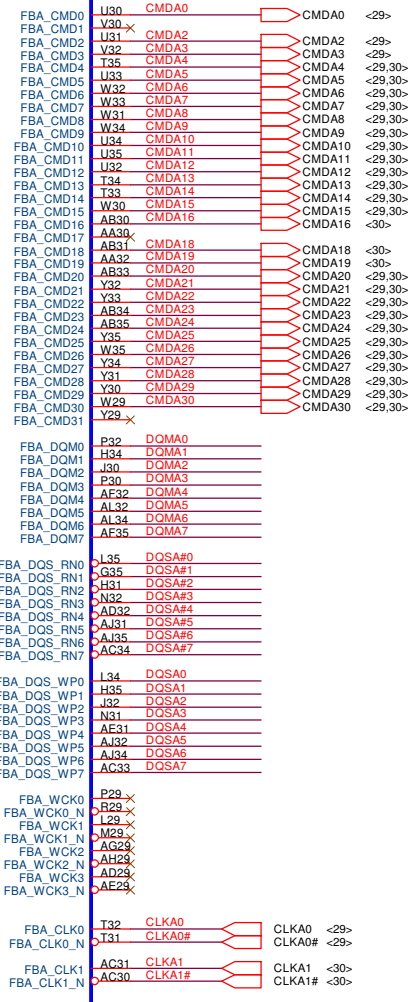
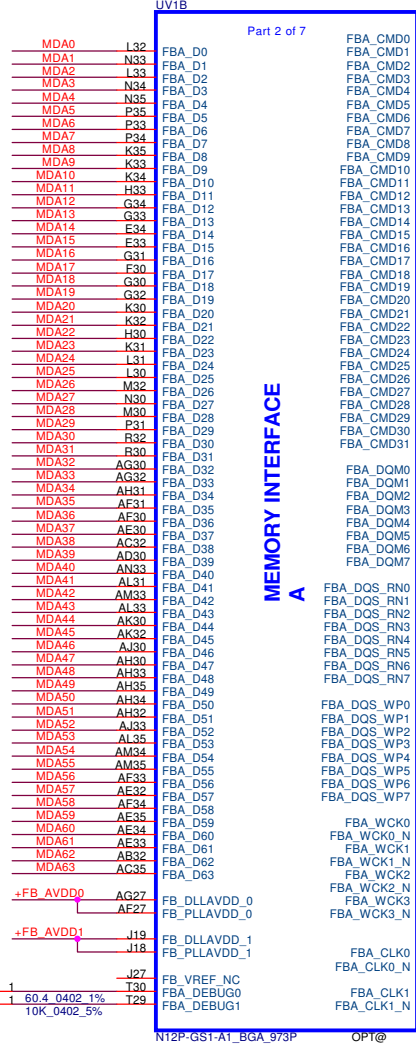
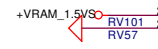
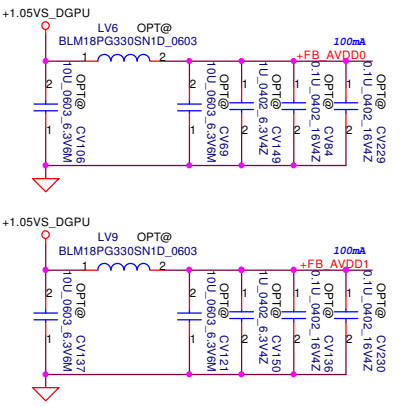
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<b>Compal Electronics, Inc.</b>			
<b>VGA_GND</b>			
Size	Document Number	Rev	
	<b>LA-7401P</b>	1.0	
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<29..30> MDA[0..63] ← MDA[0..63]



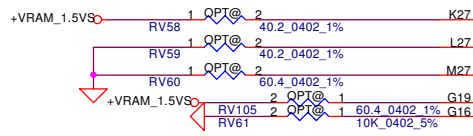
GB2-128  
Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

UV1C  
Part 3 of 7

B13	FBC_D0	FBC_CMD0	F18
D13	FBC_D1	FBC_CMD1	E19 X
A14	FBC_D2	FBC_CMD2	D18
C16	FBC_D3	FBC_CMD3	C17
B16	FBC_D4	FBC_CMD4	F19
A17	FBC_D5	FBC_CMD5	C19
D16	FBC_D6	FBC_CMD6	B17
C13	FBC_D7	FBC_CMD7	E20
B11	FBC_D8	FBC_CMD8	B19
C11	FBC_D9	FBC_CMD9	D20
A11	FBC_D10	FBC_CMD10	A19
C10	FBC_D11	FBC_CMD11	D19
C8	FBC_D12	FBC_CMD12	C20
B8	FBC_D13	FBC_CMD13	E20
A8	FBC_D14	FBC_CMD14	B20
E8	FBC_D15	FBC_CMD15	G21
F8	FBC_D16	FBC_CMD16	F22
F9	FBC_D17	FBC_CMD17	F24 X
F10	FBC_D18	FBC_CMD18	E23
F12	FBC_D19	FBC_CMD19	C25
D8	FBC_D20	FBC_CMD20	F21
D11	FBC_D21	FBC_CMD21	E22
E11	FBC_D22	FBC_CMD22	D21
D12	FBC_D23	FBC_CMD23	A23
E13	FBC_D24	FBC_CMD24	D22
F13	FBC_D25	FBC_CMD25	B23
F14	FBC_D26	FBC_CMD26	C22
F15	FBC_D27	FBC_CMD27	B22
E16	FBC_D28	FBC_CMD28	A22
F16	FBC_D29	FBC_CMD29	A20
F17	FBC_D30	FBC_CMD30	G20 X
D29	FBC_D31	FBC_CMD31	G20 X
F27	FBC_D32	FBC_CMD31	A16
F28	FBC_D33	FBC_CMD31	D10
E28	FBC_D34	FBC_CMD31	F11
D26	FBC_D35	FBC_CMD31	D15
F25	FBC_D36	FBC_CMD31	D27
D24	FBC_D37	FBC_CMD31	D34
E25	FBC_D38	FBC_CMD31	A34
E32	FBC_D39	FBC_CMD31	D28
D33	FBC_D40	FBC_CMD31	D28
E31	FBC_D41	FBC_CMD31	D28
C33	FBC_D42	FBC_CMD31	D28
F29	FBC_D43	FBC_CMD31	D28
D30	FBC_D44	FBC_CMD31	D28
E29	FBC_D45	FBC_CMD31	D28
B29	FBC_D46	FBC_CMD31	D28
C31	FBC_D47	FBC_CMD31	D28
C29	FBC_D48	FBC_CMD31	D28
B31	FBC_D49	FBC_CMD31	D28
C32	FBC_D50	FBC_CMD31	D28
B32	FBC_D51	FBC_CMD31	D28
B35	FBC_D52	FBC_CMD31	D28
B34	FBC_D53	FBC_CMD31	D28
A29	FBC_D54	FBC_CMD31	D28
B28	FBC_D55	FBC_CMD31	D28
A28	FBC_D56	FBC_CMD31	D28
C28	FBC_D57	FBC_CMD31	D28
C26	FBC_D58	FBC_CMD31	D28
D25	FBC_D59	FBC_CMD31	D28
B25	FBC_D60	FBC_CMD31	D28
A25	FBC_D61	FBC_CMD31	D28
	FBC_D62	FBC_CMD31	D28
	FBC_D63	FBC_CMD31	D28

MEMORY INTERFACE C

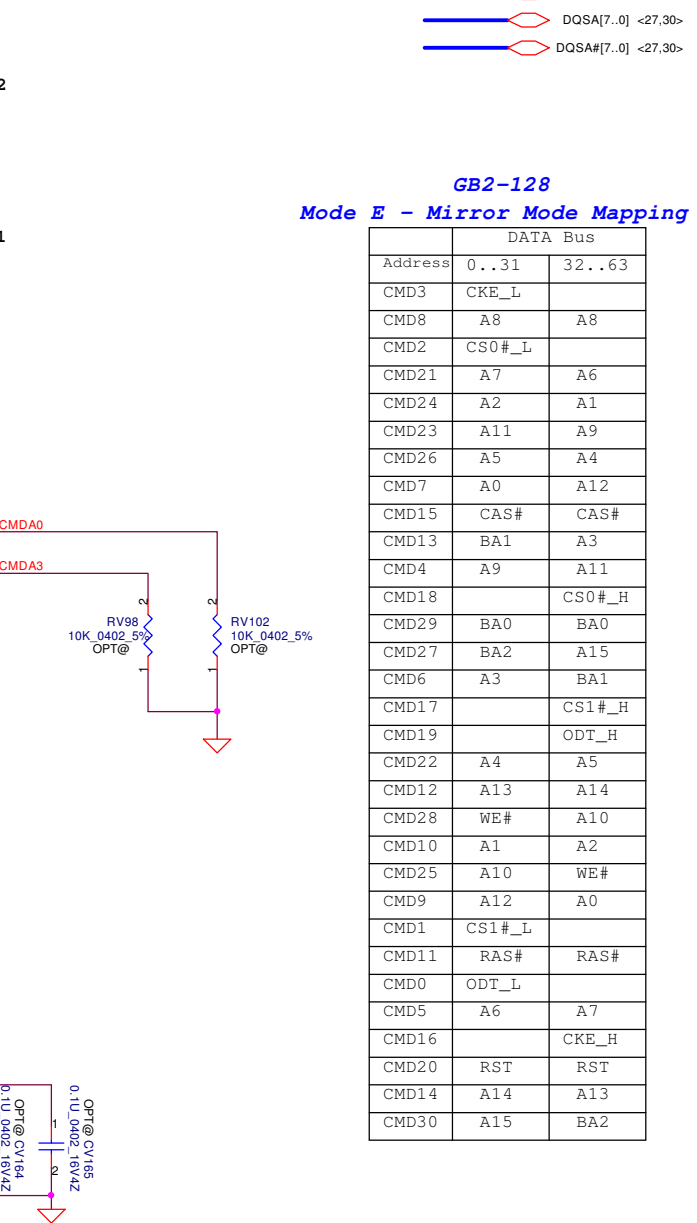
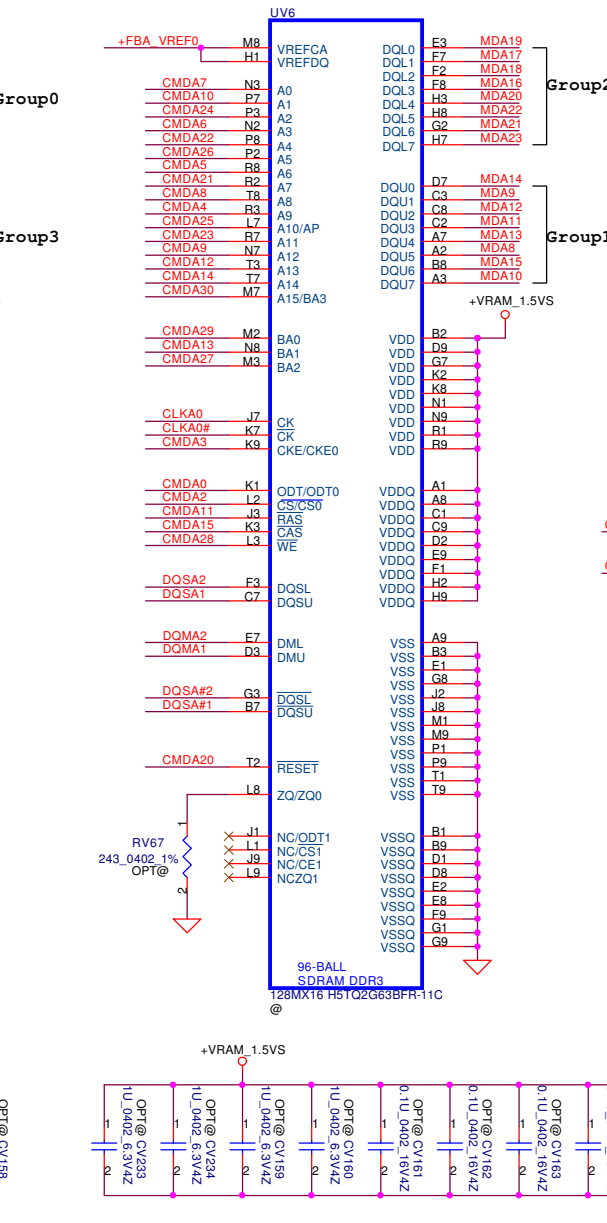
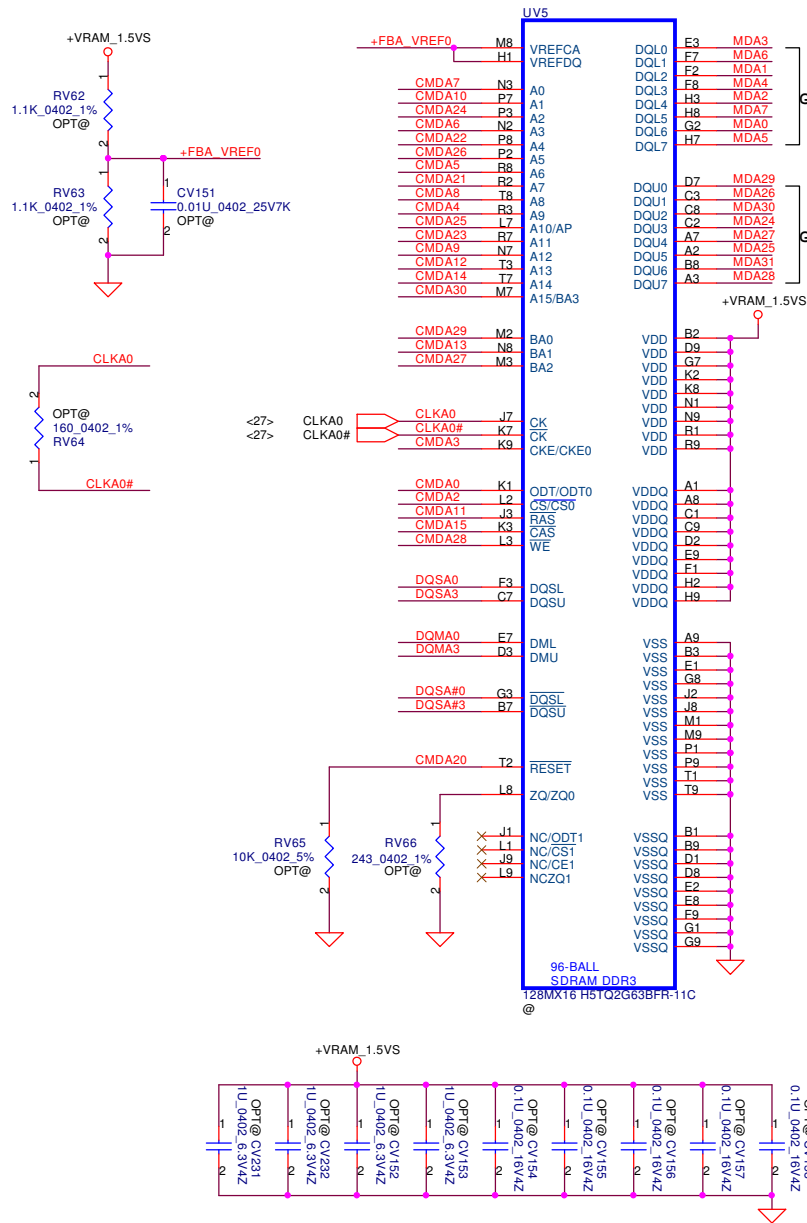


**GB2-128**  
**Mode E - Mirror Mode Mapping**

Address	DATA Bus	
	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

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# Memory Partition A - Lower 32 bits



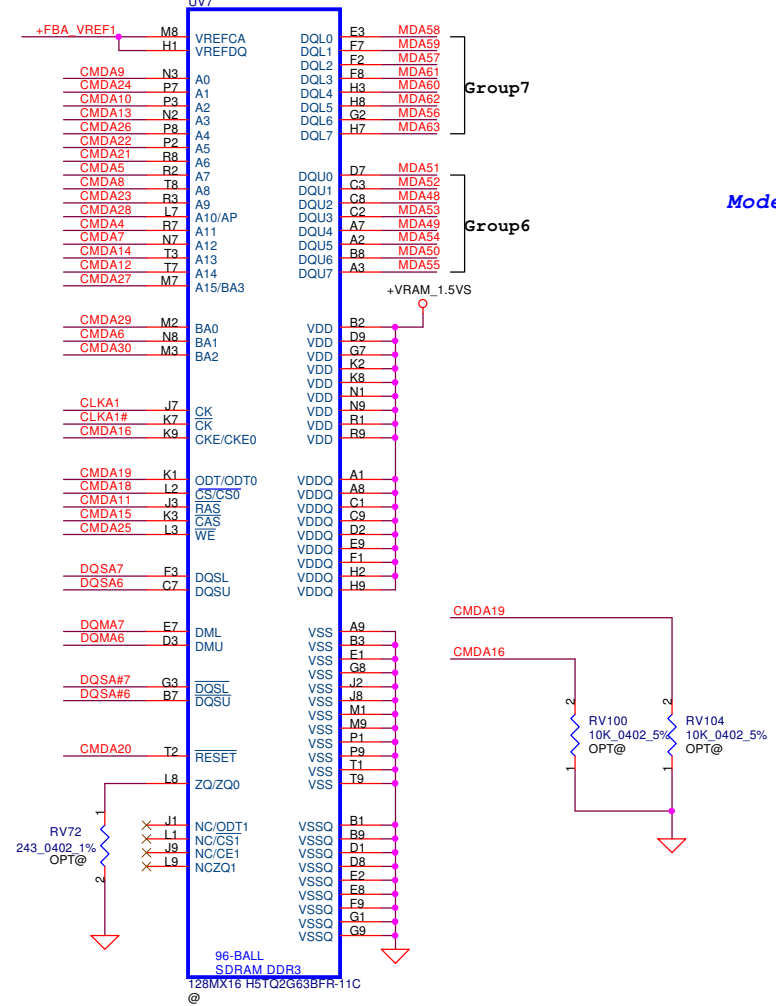
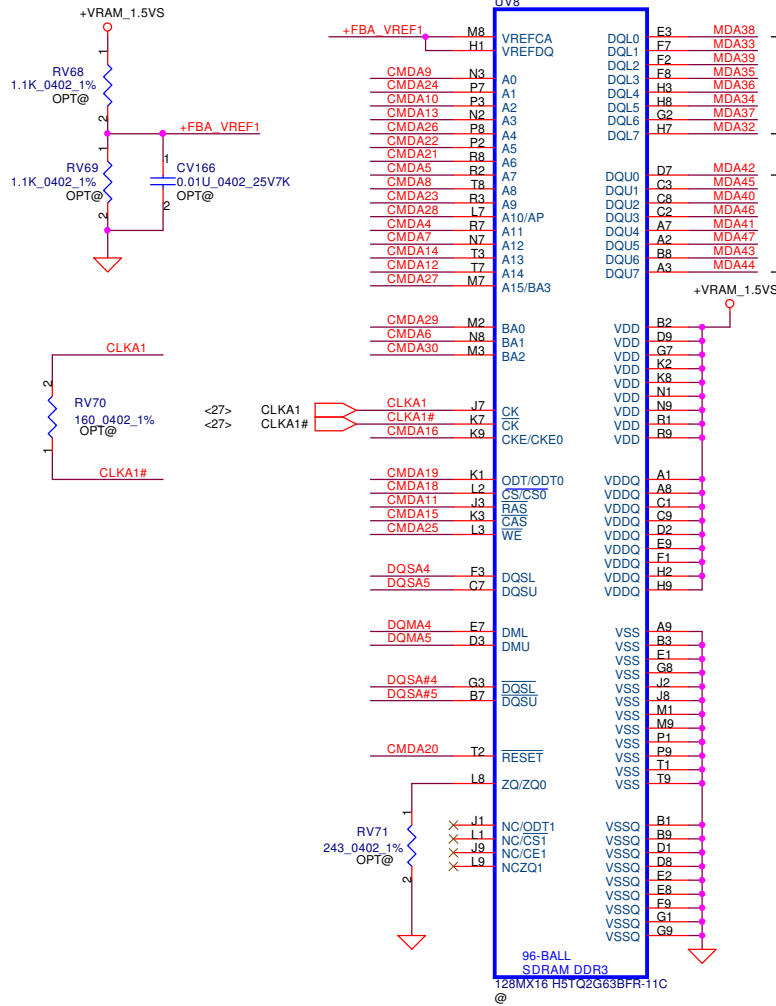
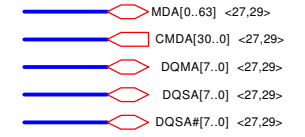
- MDA[0..63] <27,30>
- CMDA[30..0] <27,30>
- DQMA[7..0] <27,30>
- DQSA[7..0] <27,30>
- DQSA#[7..0] <27,30>

## GB2-128 Mode E - Mirror Mode Mapping

Address	DATA Bus	
CMD3	CKE_L	32..63
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

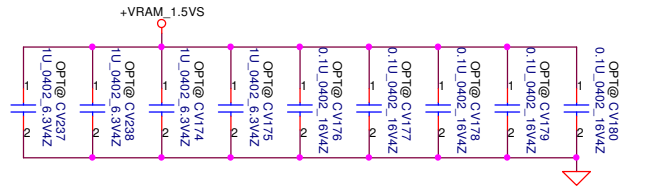
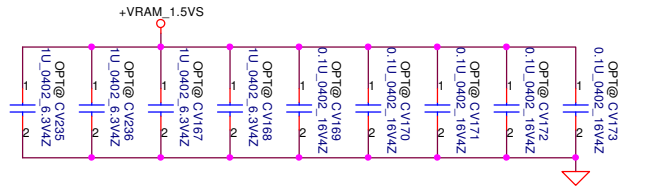
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				VGA_VRAM_A Lower		
Size		Document Number		LA-7401P		
Date:		Sunday, April 10, 2011		Sheet 29 of 56		

# Memory Partition A - Upper 32 bits



## GB2-128 Mode E - Mirror Mode Mapping

Address	DATA Bus	
CMD3	0..31	32..63
CMD8	CKE_L	A8
CMD2	CS0#_L	A6
CMD21	A7	A1
CMD24	A2	A9
CMD23	A11	A4
CMD26	A5	A12
CMD7	A0	CAS#
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2



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Memory Partition C - Lower 32 bits



EVT:Del B ch VRAM

**GB2-128**  
**Mode E - Mirror Mode Mapping**

Address	DATA Bus	
	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>VGA_VRAM_C Lower</b>		
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				Custom	LA-7401P	1.0
Date: Sunday, April 10, 2011				Sheet	31 of 56	

Memory Partition C - Upper 32 bits



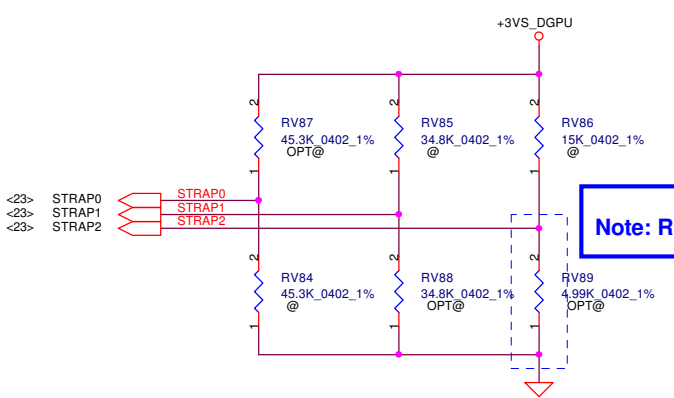
EVT:Del B ch VRAM

GB2-128  
Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

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				Size Custom	Document Number
				LA-7401P	
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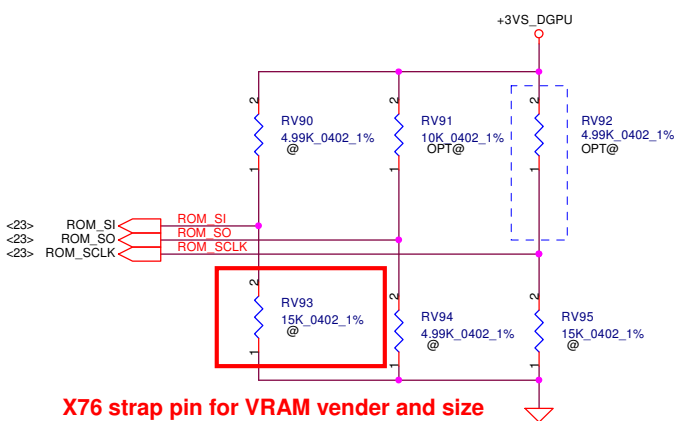


Note: RV89 = 5K for set N12P-GV ,ID=1050

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLEN_TERM
ROM_SI	+3VS_DGPU	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS_DGPU	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]

ROM\_SI net for VRAM strap

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



X76 strap pin for VRAM vender and size

SUB_VENDOR	
0	No VBIOS ROM (Default)
1	BIOS ROM is present

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User [3:0]	
1000-1100	Customer defined

GPU	Project	VRAM size	CH	Description	Compal VRAM P/N	VRAM description	ROM_SI net setup	PD or PU (RV93)	R/PN
N12P-GV (29x29) 64bit (Layout 4pcs only)	PAJ80(14")	512M(X4)	CHA	DDR3 Hynix 64Mx16 1.5V	SA0000324C0	H5TQ1G63DFR-12C 800MHz	0010	PD 15K	SD034150280(15K)
		512M(x4)	CHA	DDR3 Samsung 64Mx16 1.5V	SA00004HS00	K4W1G1646G-BC12 800MHz	0011	PD 20K	SD034200280(20K)
	PAJ90(15.6")	1G(x4)	CHA	DDR3 Hynix 128Mx16 1.5V	SA00003VS00	H5TQ2G63BFR-12C 800MHz	0110	PD 35K	SD034348280(34.8K)
		1G(x4)	CHA	DDR3 Samsung 128Mx16 1.5V	SA00003MQ40	K4W2G1646C-HC12 800MHz	0111	PD 45K	SD034453280(45.3K)

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

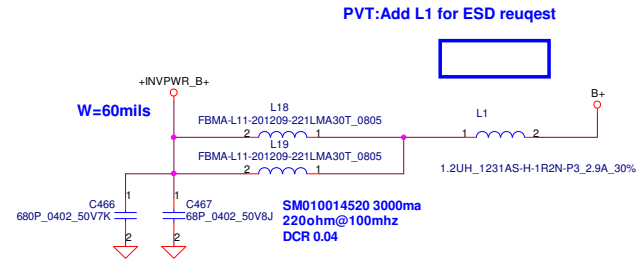
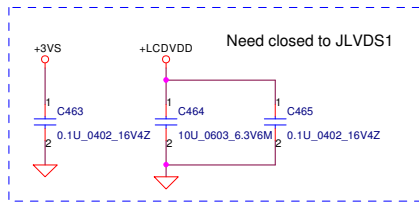
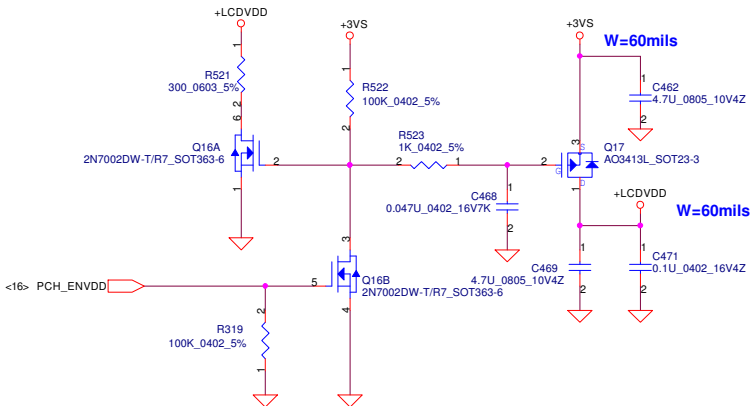
SLOT_CLOCK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

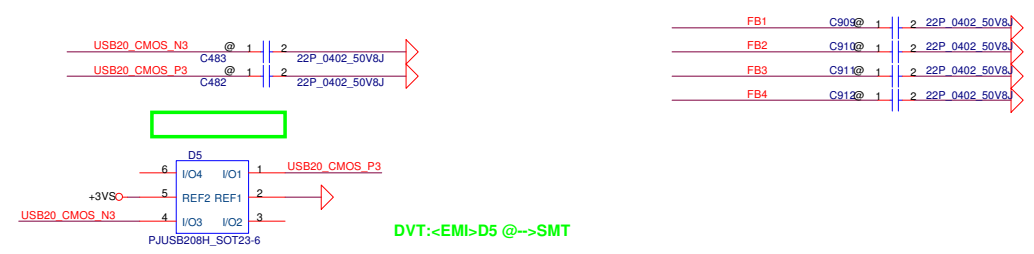
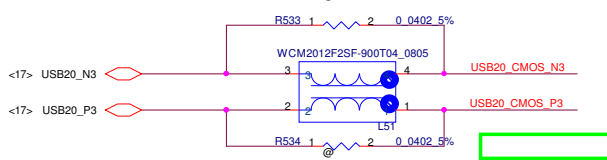
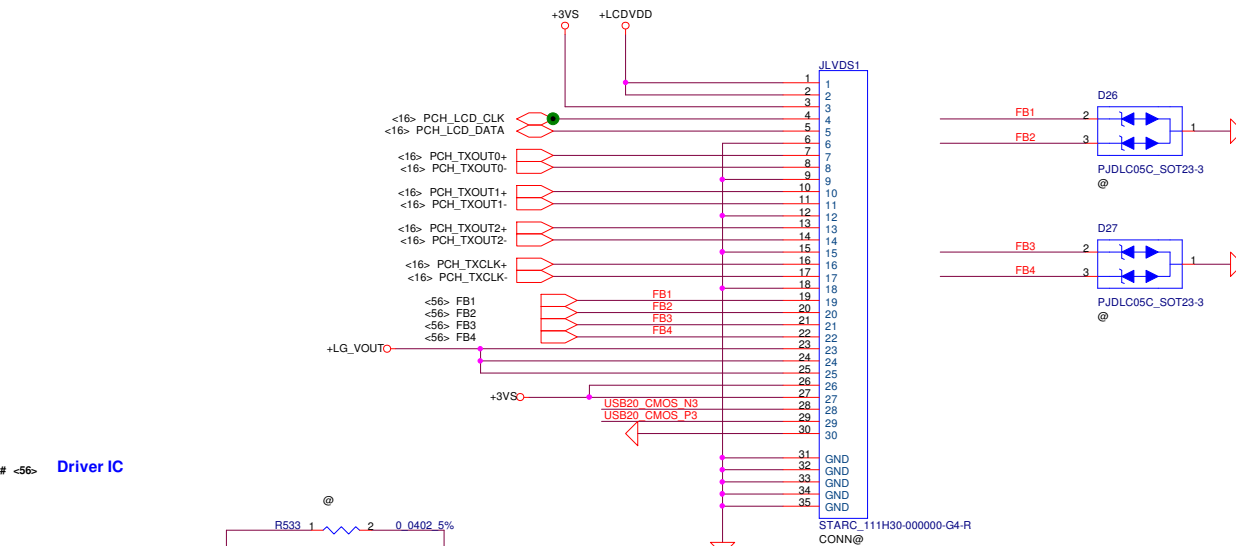
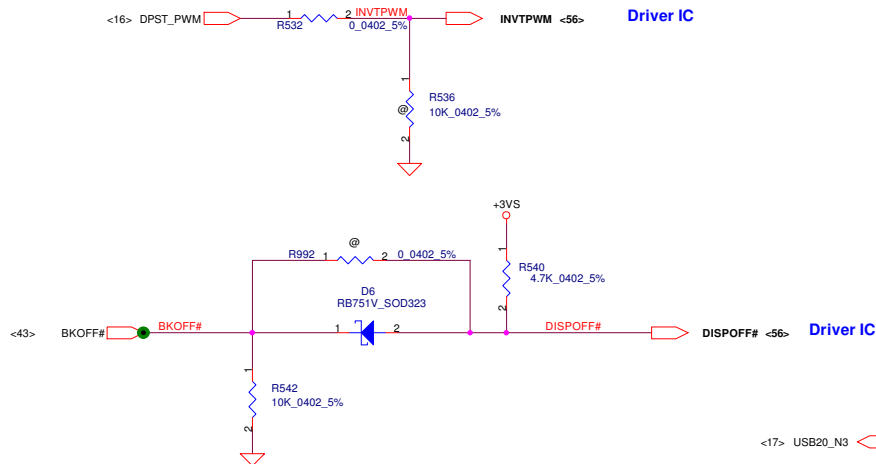
VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

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				Size Custom	Document Number	Rev
			<b>LA-7401P</b>	1.0		
			Date: Sunday, April 10, 2011	Sheet 33 of 56		

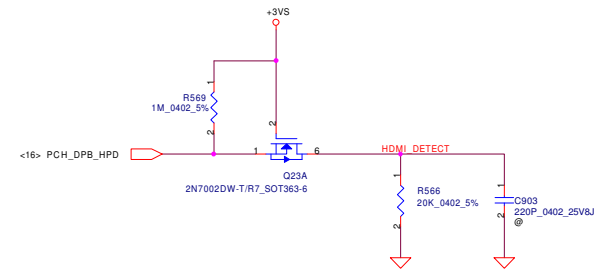
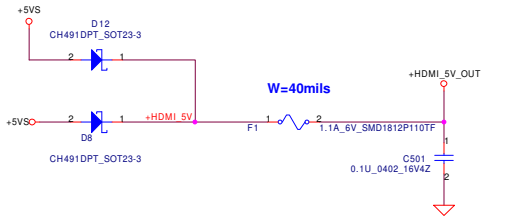
# LCD POWER CIRCUIT



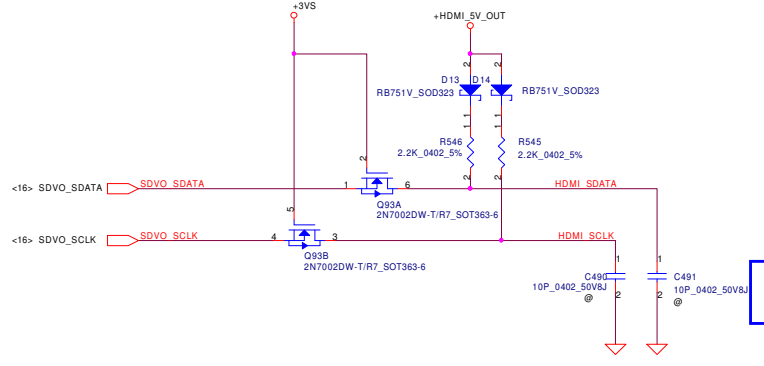
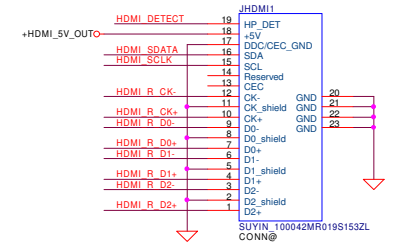
# LCD/LED PANEL Connector



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				Title: LVDS Connector

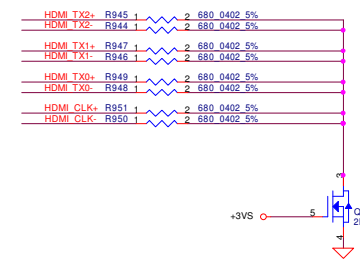


### HDMI Connector



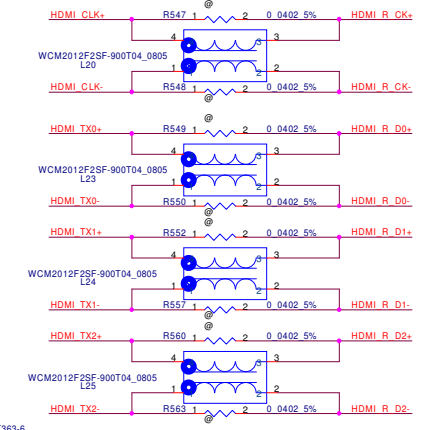
Note: Reresve for RF

<16> PCH_DPB_P2	C497	2	1	0.1U	0.402	16V7K	HDMI TX2+
<16> PCH_DPB_N2	C496	2	1	0.1U	0.402	16V7K	HDMI TX2-
<16> PCH_DPB_P1	C495	2	1	0.1U	0.402	16V7K	HDMI TX1+
<16> PCH_DPB_N1	C494	2	1	0.1U	0.402	16V7K	HDMI TX1-
<16> PCH_DPB_P0	C493	2	1	0.1U	0.402	16V7K	HDMI TX0+
<16> PCH_DPB_N0	C492	2	1	0.1U	0.402	16V7K	HDMI TX0-
<16> PCH_DPB_P3	C499	2	1	0.1U	0.402	16V7K	HDMI CLK+
<16> PCH_DPB_N3	C498	2	1	0.1U	0.402	16V7K	HDMI CLK-



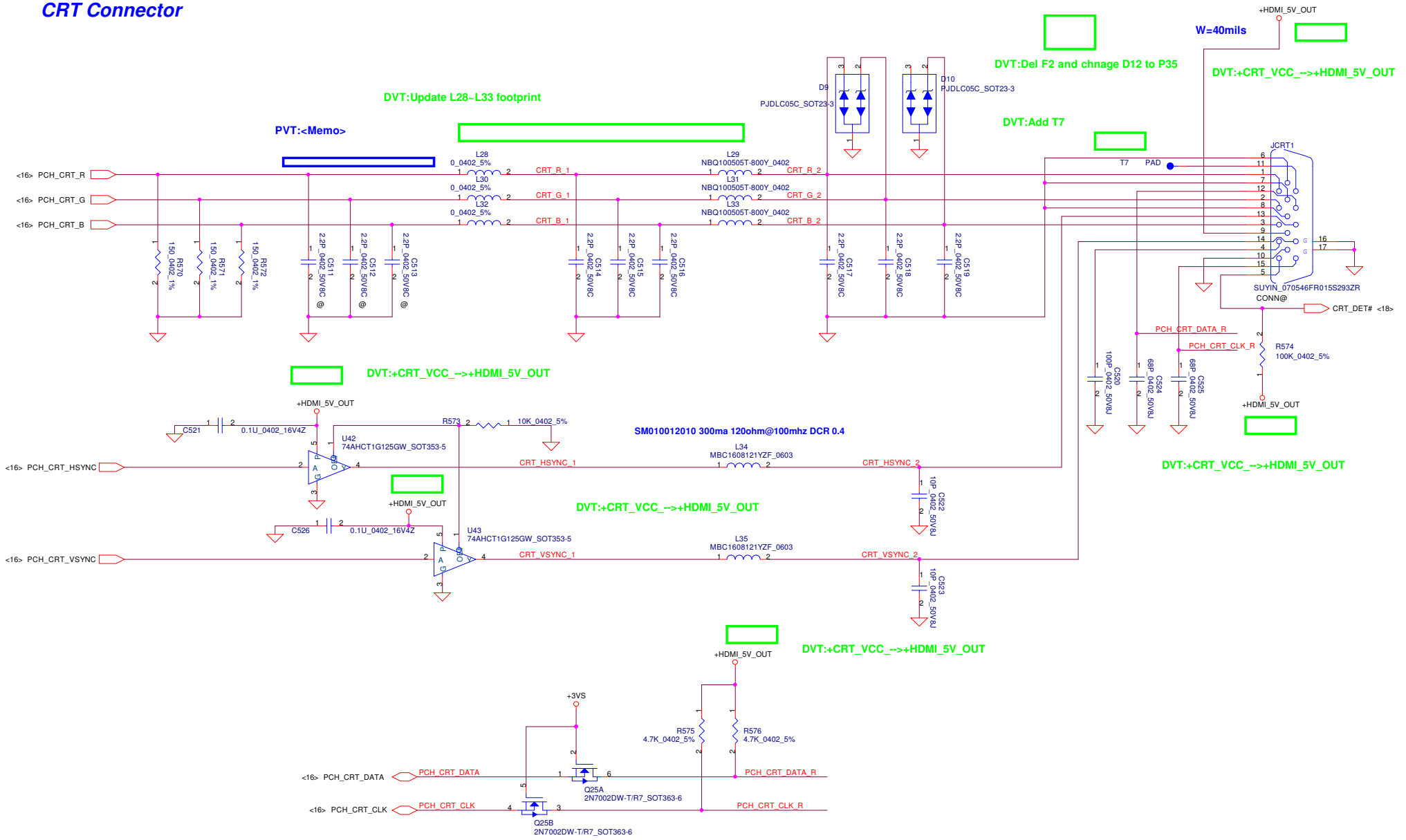
DVT::EMI>L20 L23 L24 L25 @-->SMT

### SM70001310 400ma 90ohm@100mhz DCR 0.3



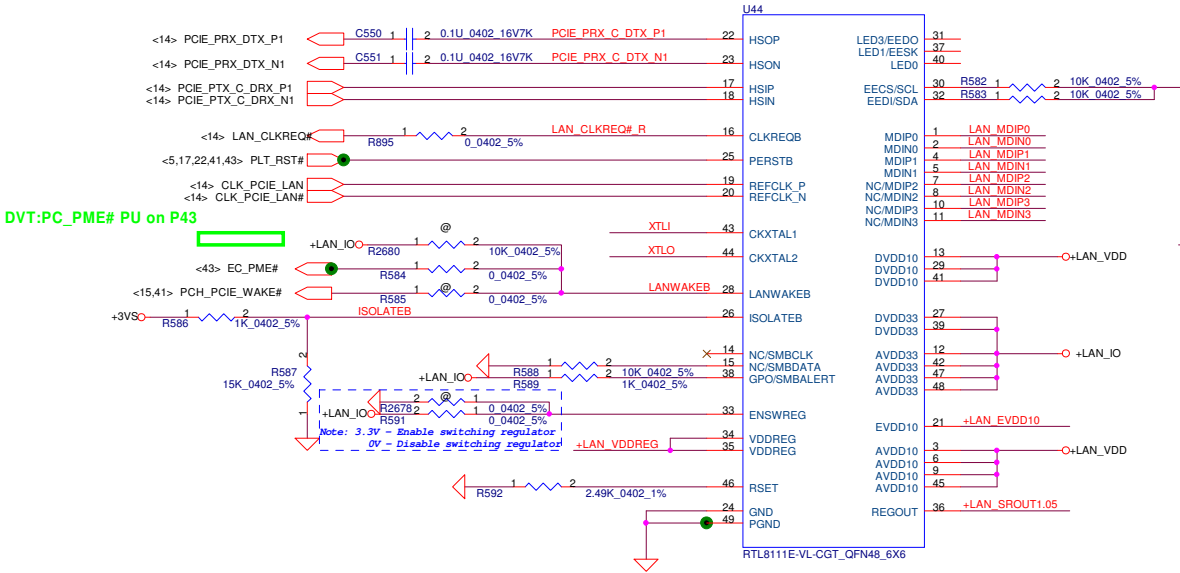
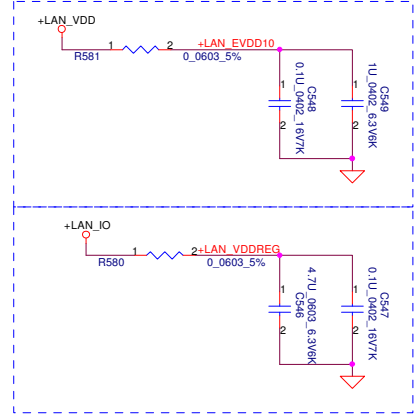
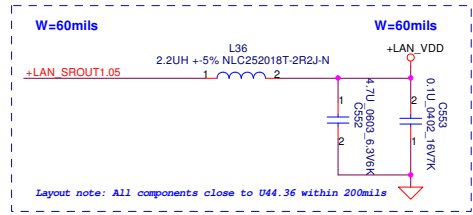
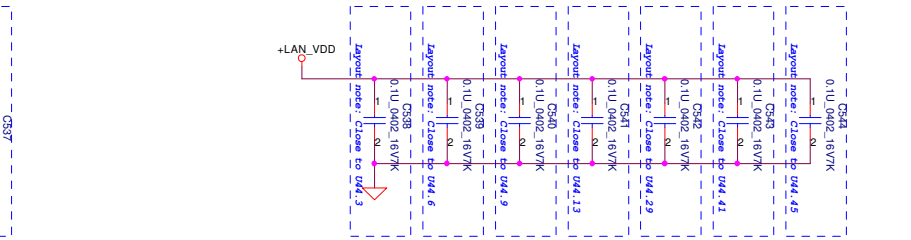
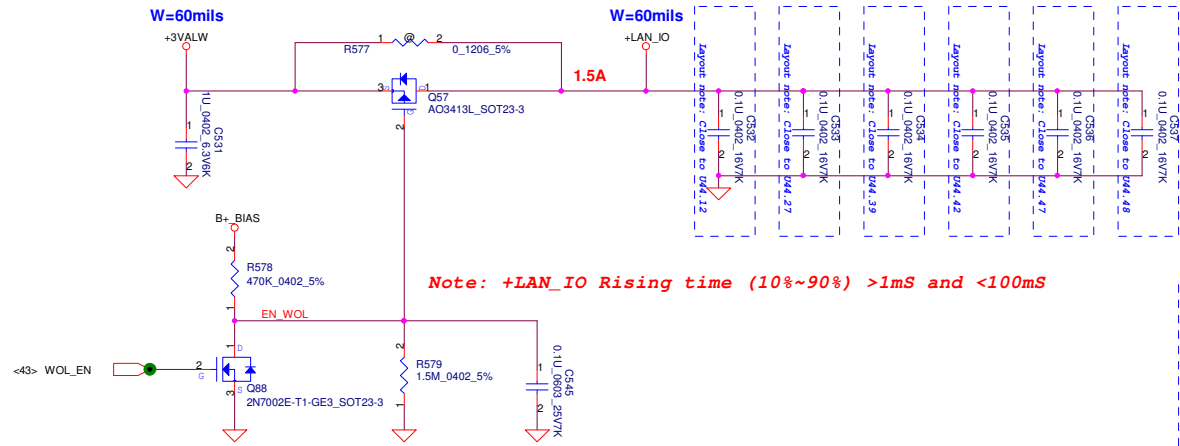
Lane Reversed on Page 16

# CRT Connector



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Title CRT Connector				
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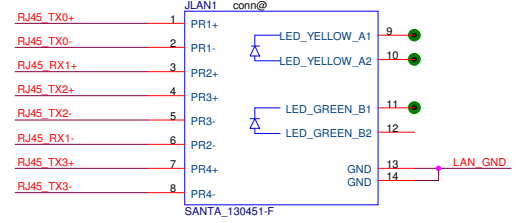
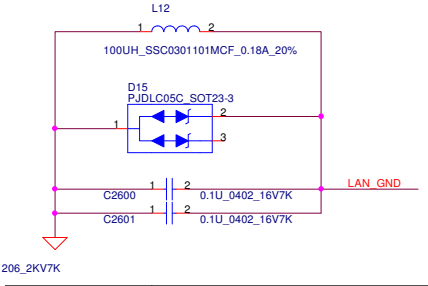
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DVT:PC\_PME# PU on P43

DVT:Add R590 R957

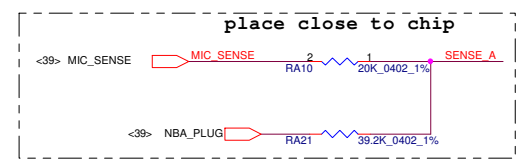
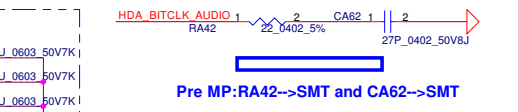
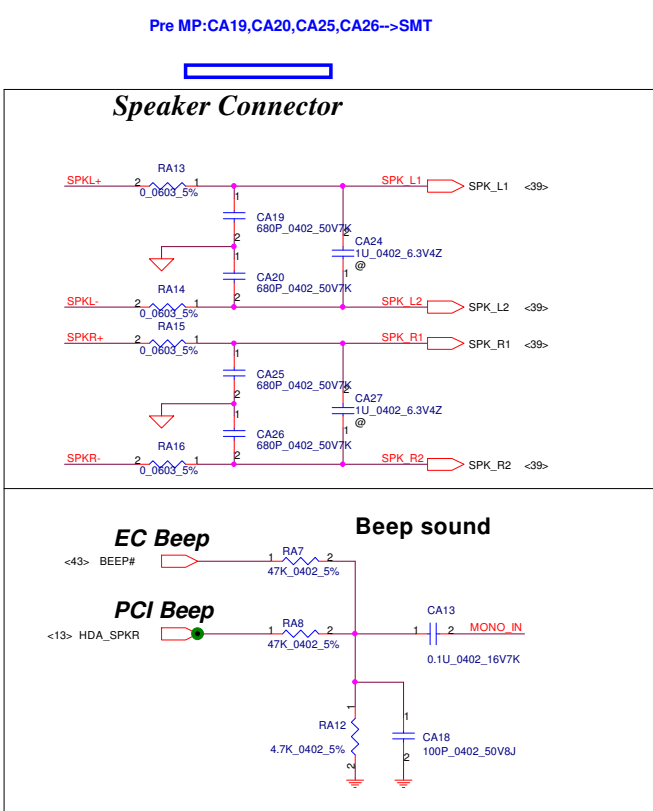
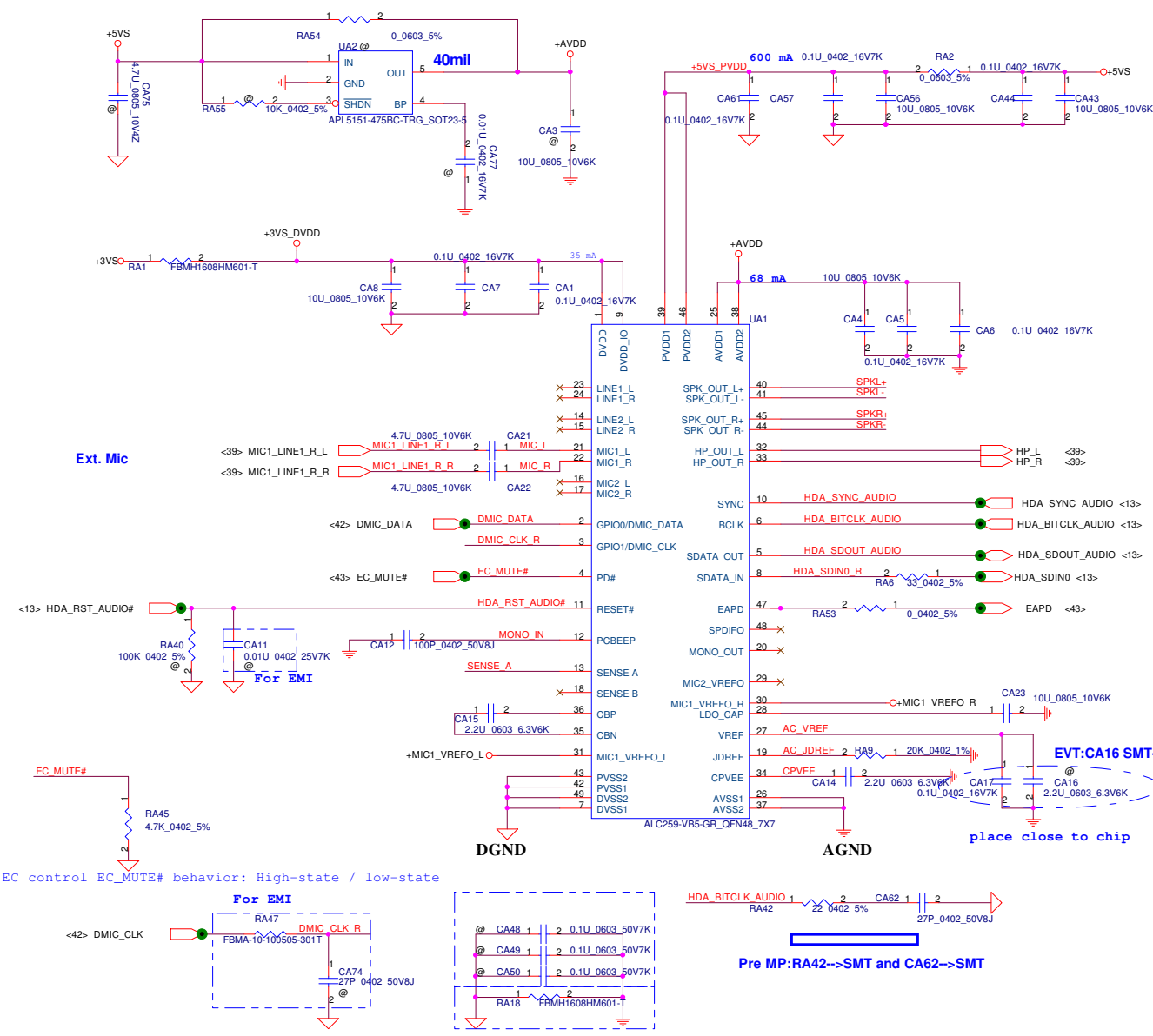
DVT:Update Y5 source



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Issued Date	2010/08/23
Deciphered Date	2011/08/25

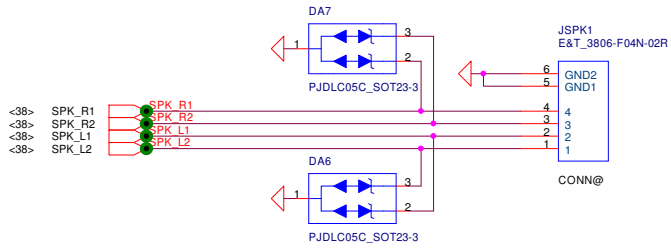
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LAN Realtek RTL8111E	
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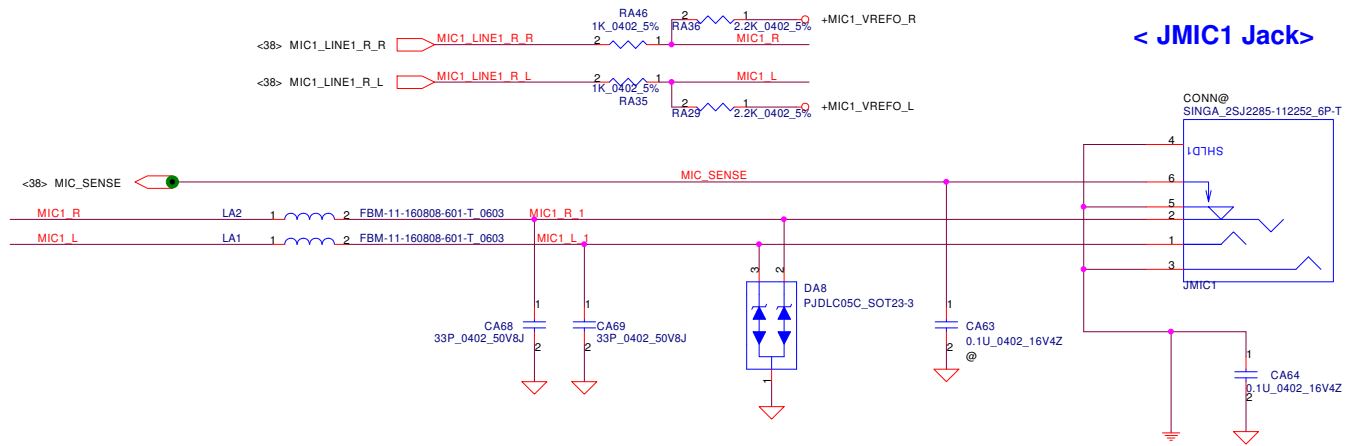


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	

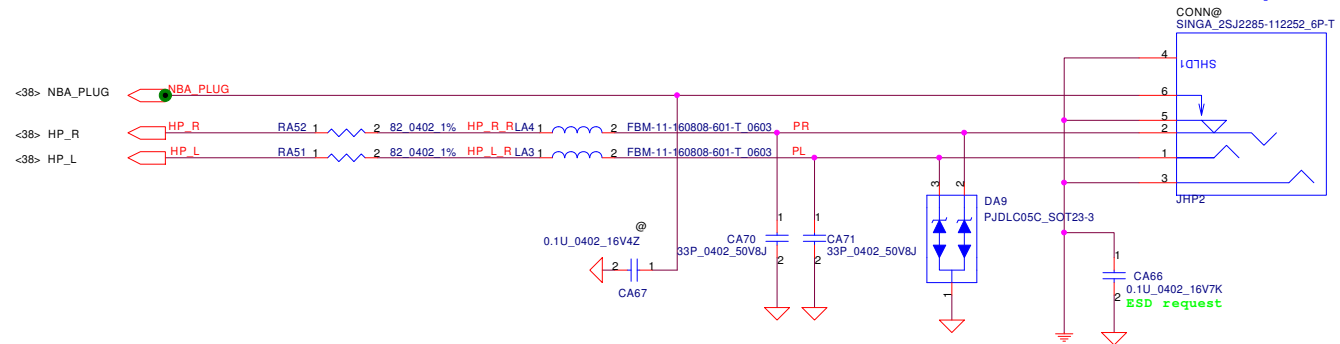
< SPK connector >



< JMIC1 Jack >

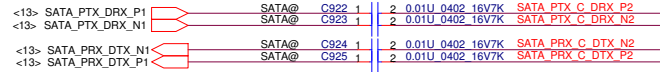
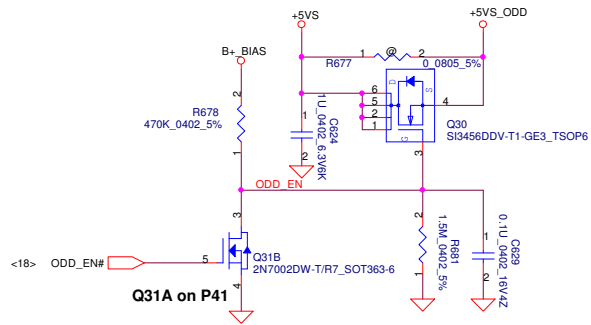
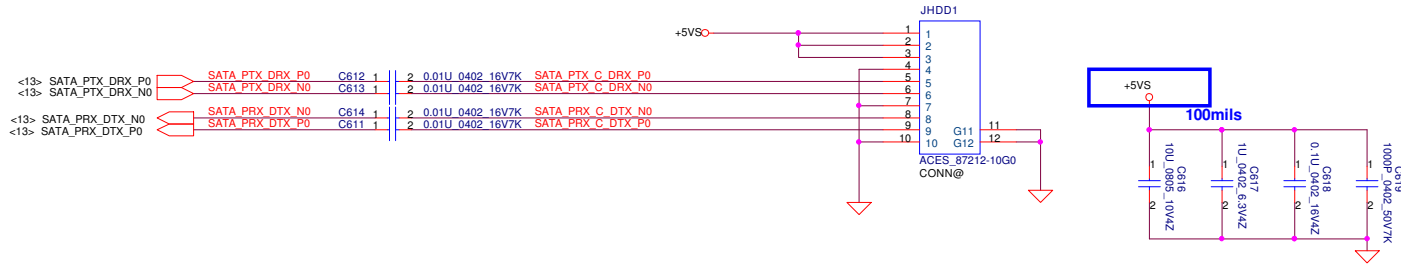


< JHP2 Head phone >

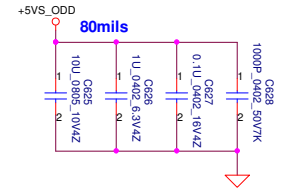
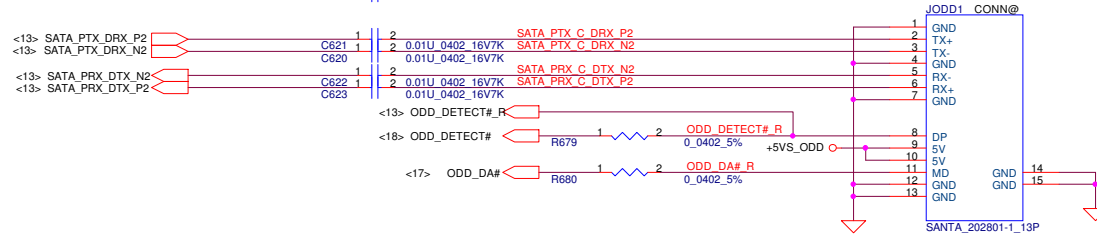


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	LA-7401P			
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## SATA HDD1 Connector



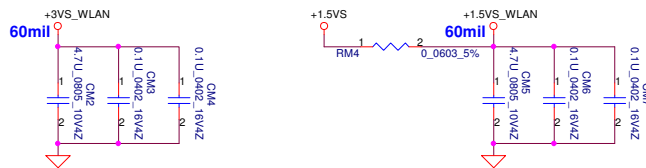
## <14" SATA ODD Connector



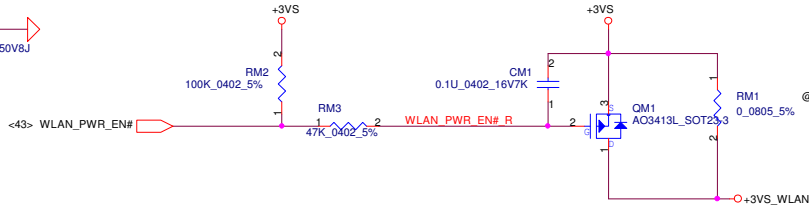
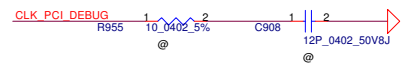
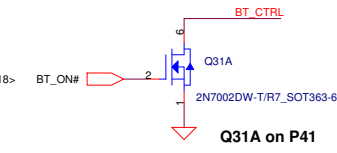
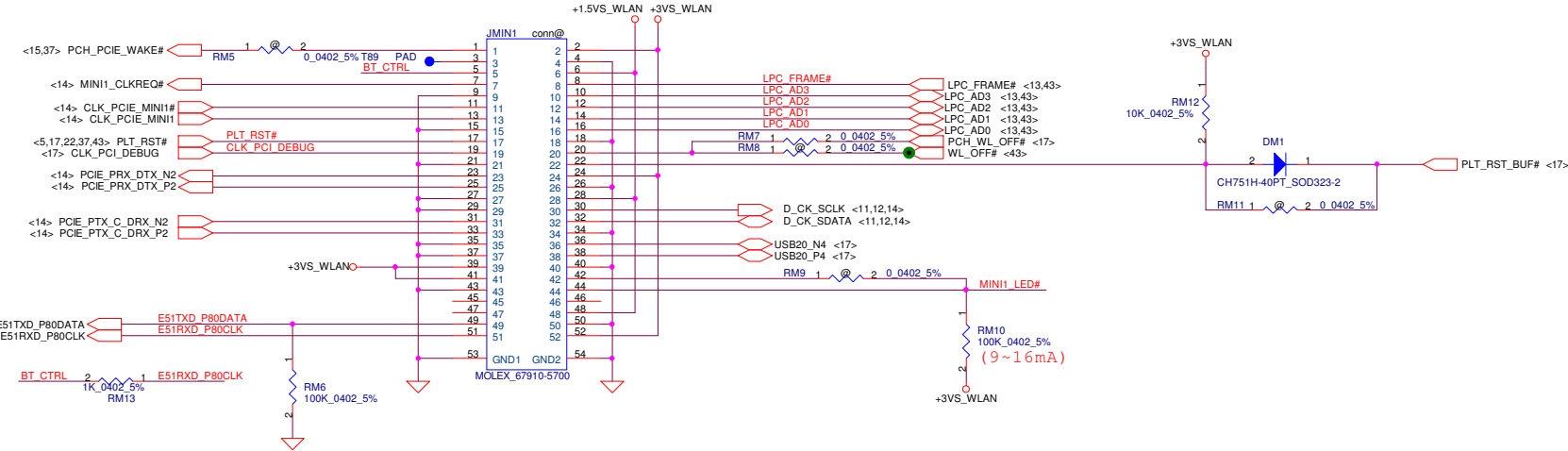
Security Classification		Compal Secret Data		Title <b>HDD/ODD Connector</b>	
Issued Date	2010/08/23	Deciphered Date	2011/08/25		
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# Wireless LAN

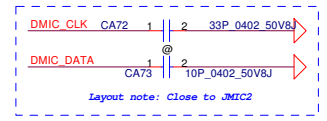
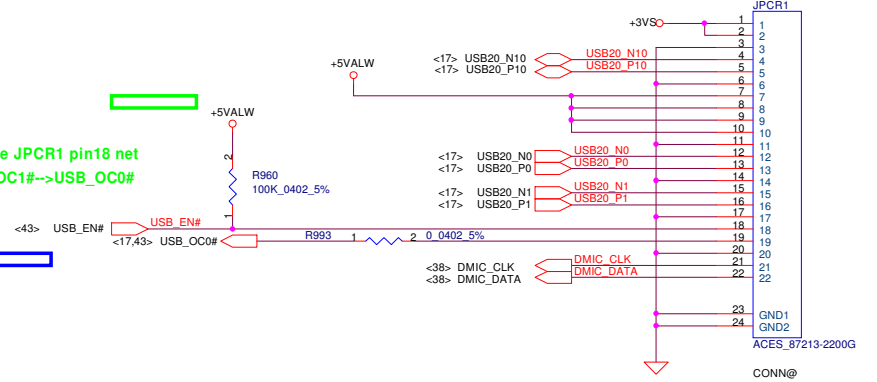


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



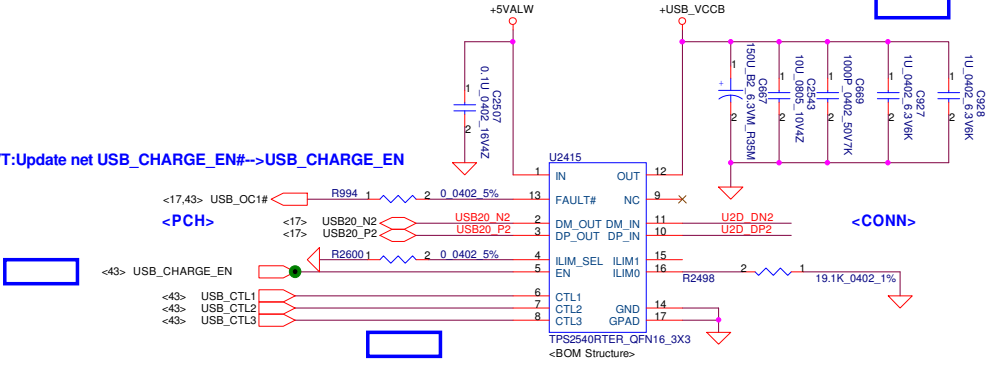
DVT:Add R560 and update JPCR1 pin18 net  
DVT:Update USB\_OC1#-->USB\_OC0#

PVT:Add R993

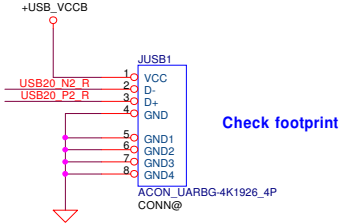
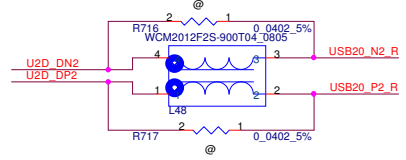


Pre MP:Add C923 C924

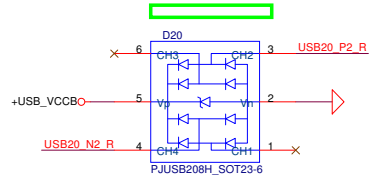
PVT:Update net USB\_CHARGE\_EN#-->USB\_CHARGE\_EN



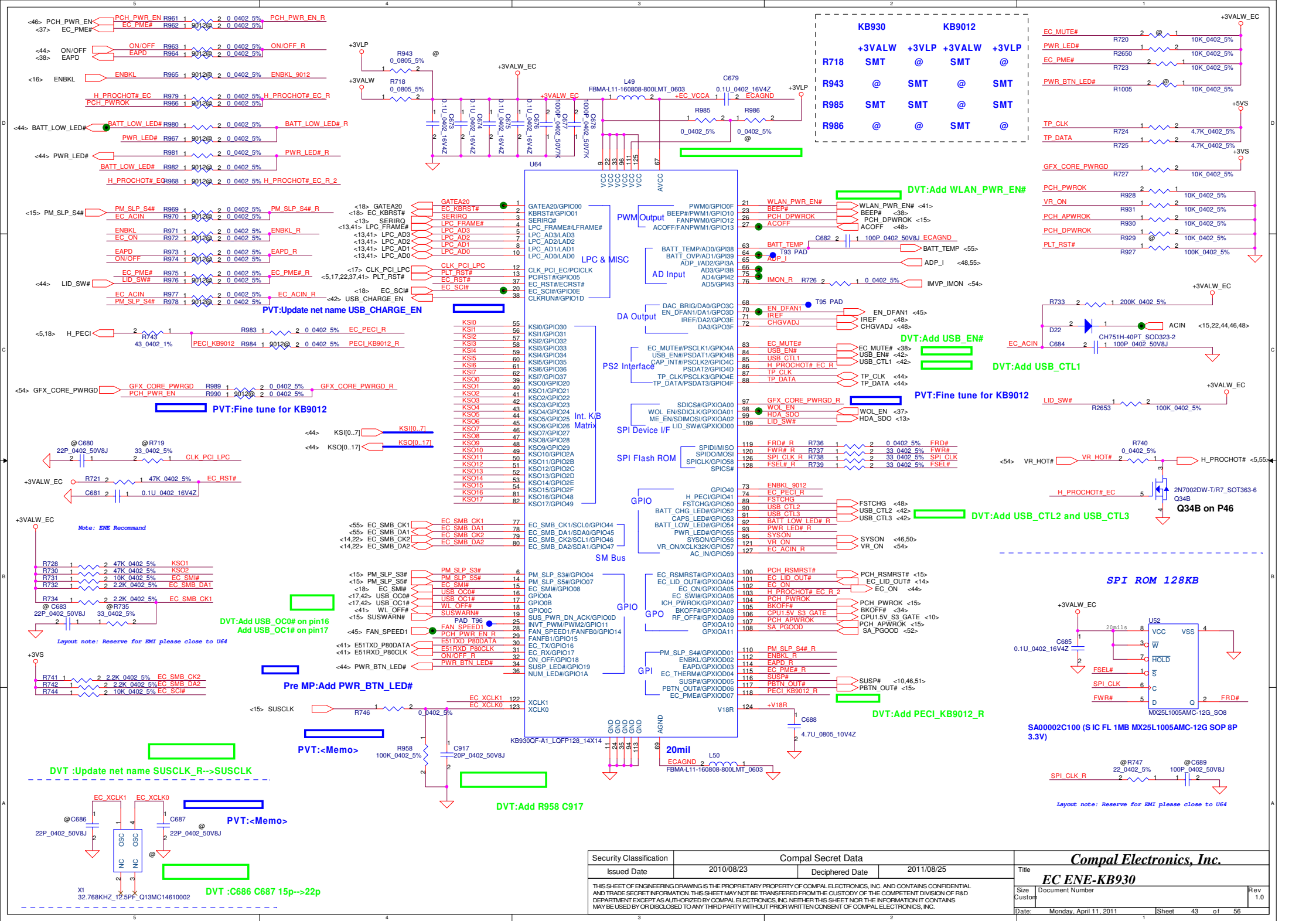
PVT:Remove R2664 R2499 R2500 R2501 for DFX issue



DVT:<EMI>L48 D20 @-->SMT



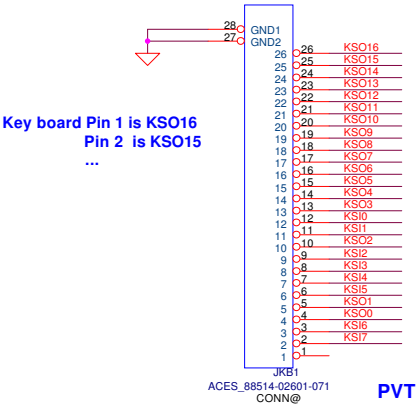
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/08/23	Deciphered Date	2011/08/25	Title	
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Size Custom		Document Number		Rev 1.0	
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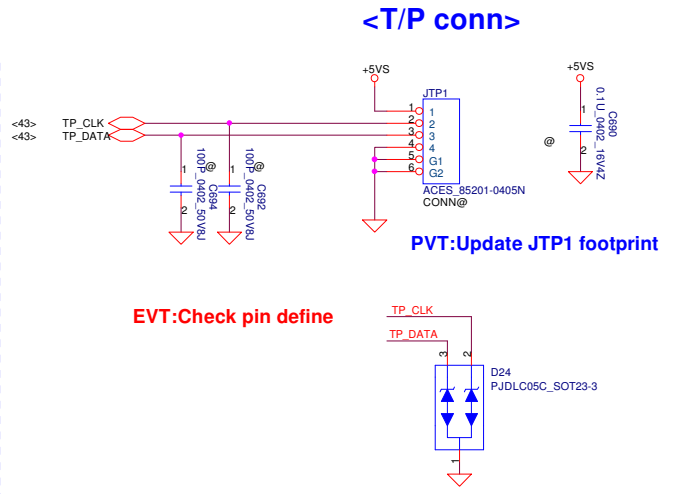
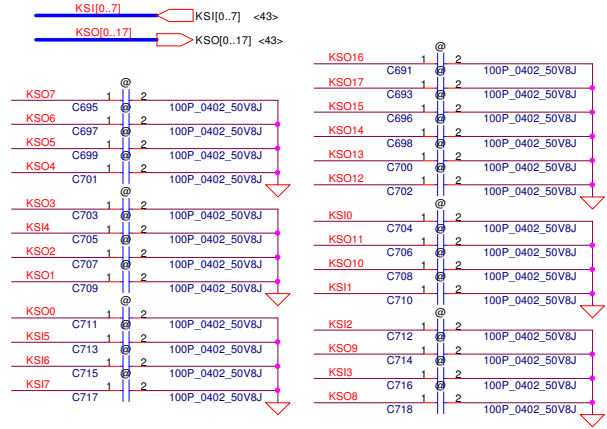
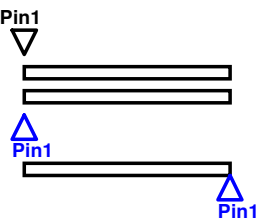
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Issued Date	2010/08/23	Deciphered Date	2011/08/25

**INT\_KBD Connector**  
**New key board**

Key board pin define (Down)  
CIS symbol (DVT)  
CIS symbol (PVT need reverse pin define)

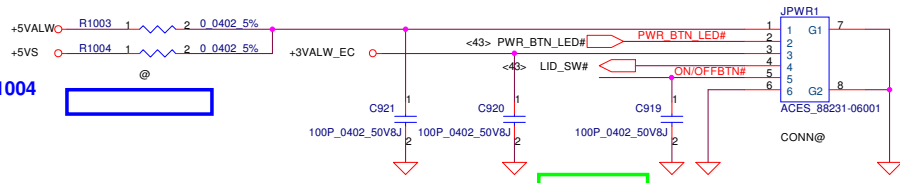


PVT:Update JKB1 footprint



**<Power Button/Lid B conn>**

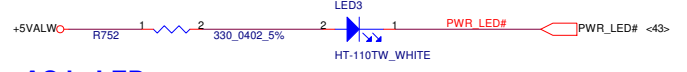
Pre MP:Add R1003 R1004



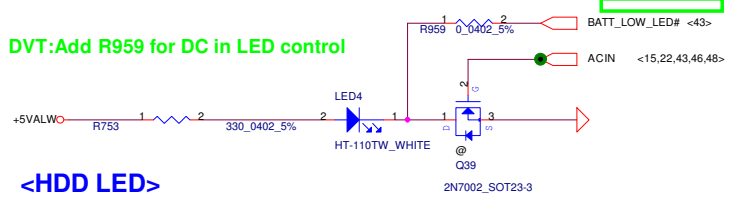
DVT:Update JPWR1 footprint and pin define

Pre MP:Update JPWR1 pin define

**<Power on LED>**



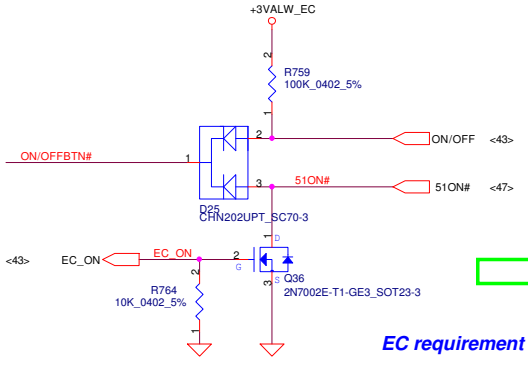
**<AC in LED>**



**<HDD LED>**

**Power Button**

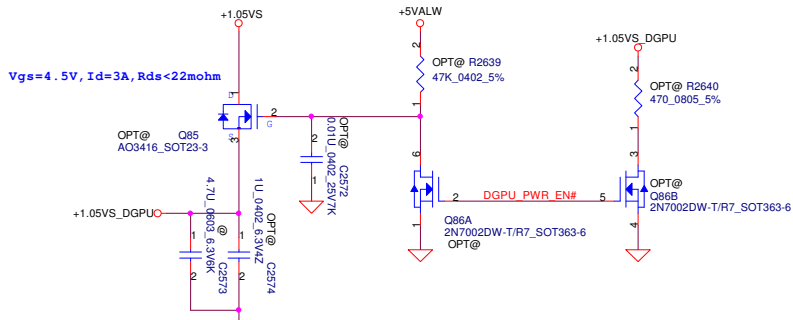
DVT:R759 pin1 +3VALW-->+3VALW\_EC



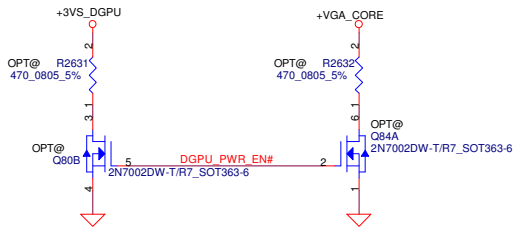
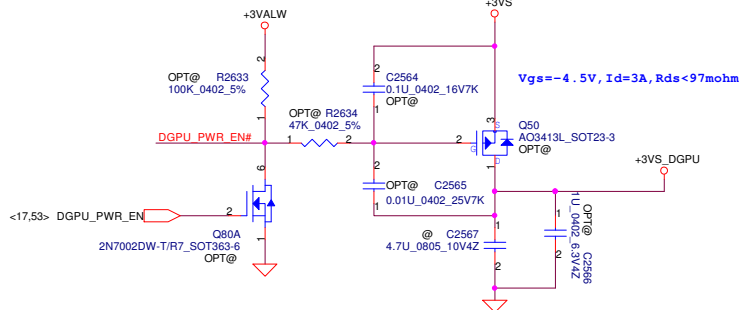
DVT:Del R937

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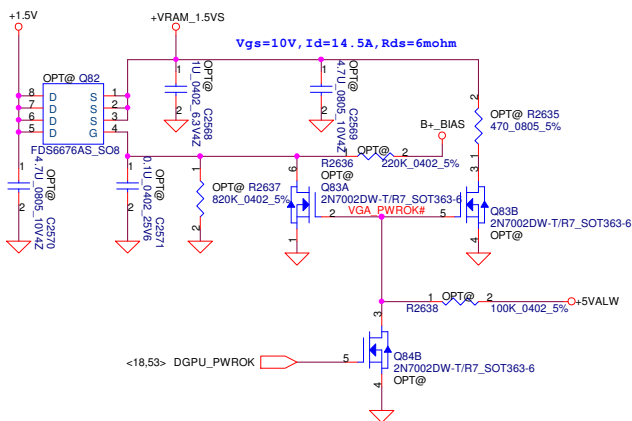
### +1.05VS to +1.05VS\_DGPU



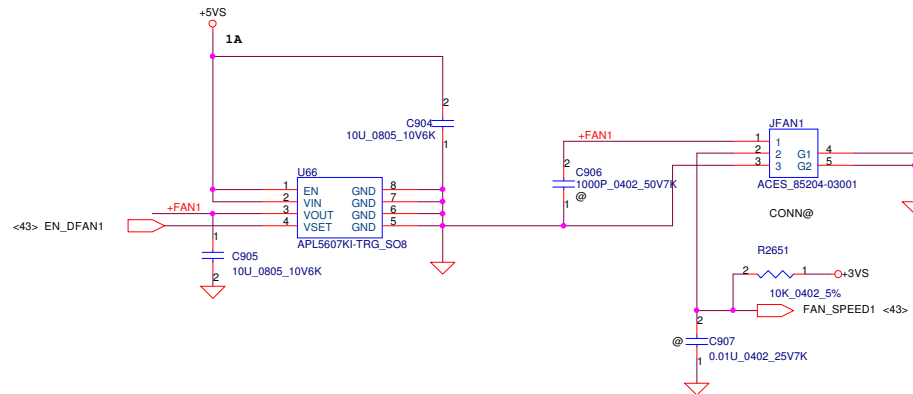
### +3VS TO +3VS\_DGPU



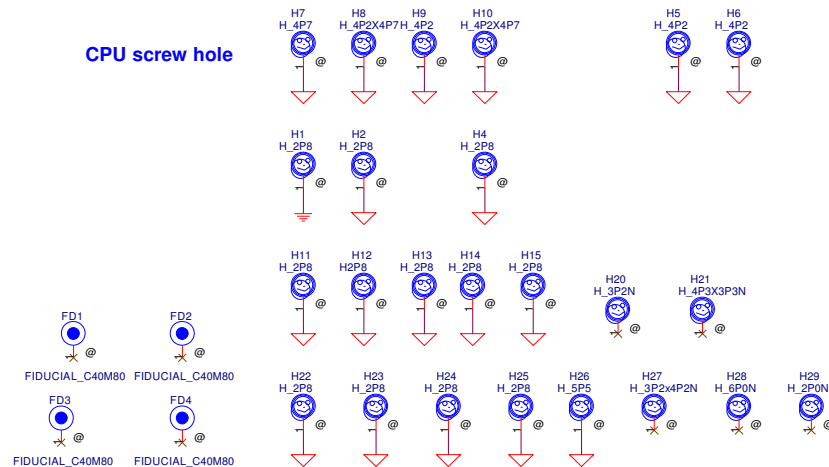
### +1.5V to +VRAM\_1.5VS



### FAN Connector



### CPU screw hole

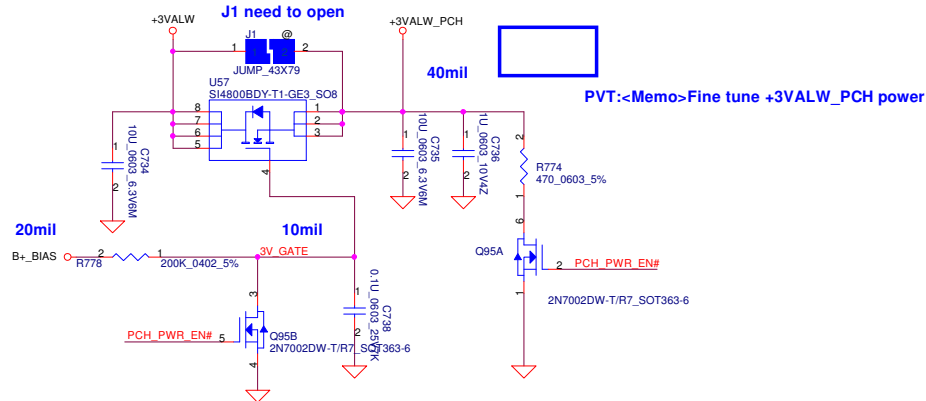


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Size	Document Number	Rev		
Custom		1.0		
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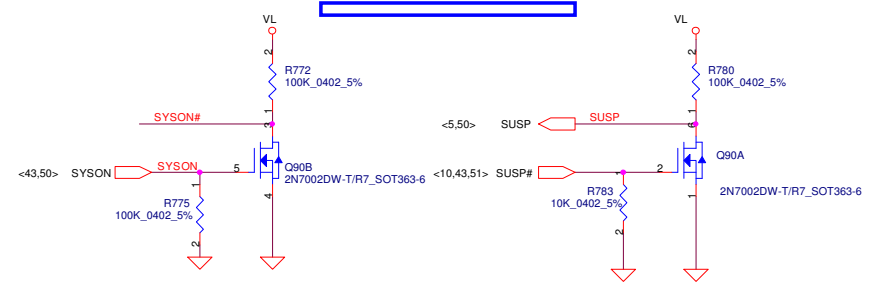
### +3VALW TO +3VALW(PCH AUX Power)

Short J1 for PCH VCCSUS3.3

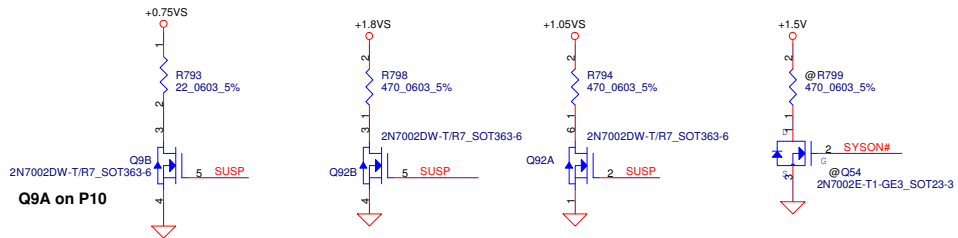
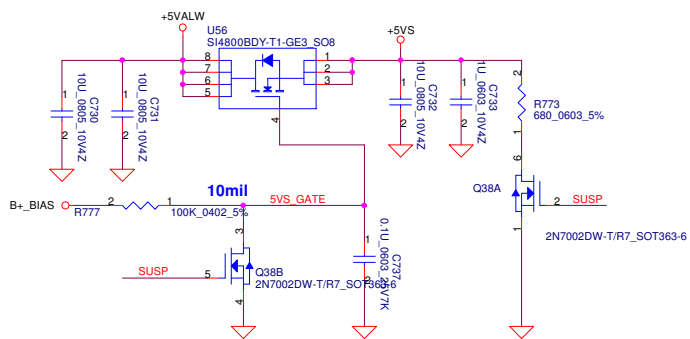
J1 need to open



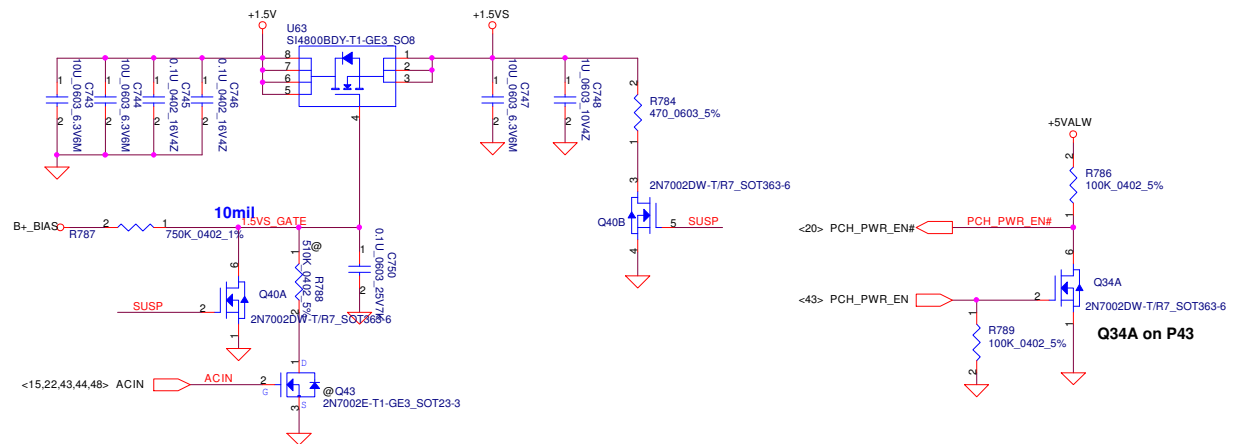
### PVT:R780 R772 +5VALW->VL



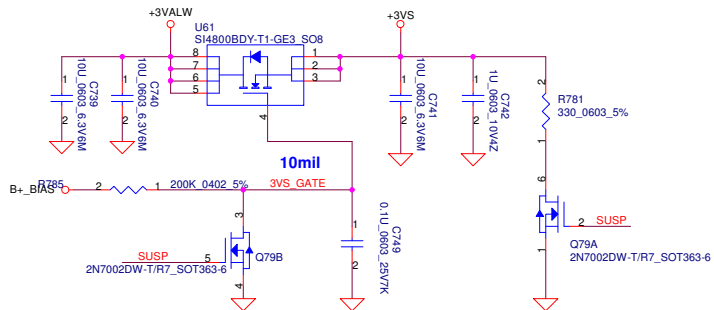
### +5VALW TO +5VS



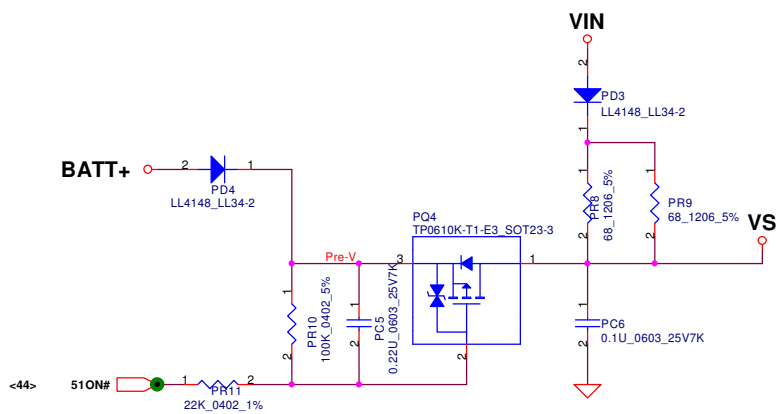
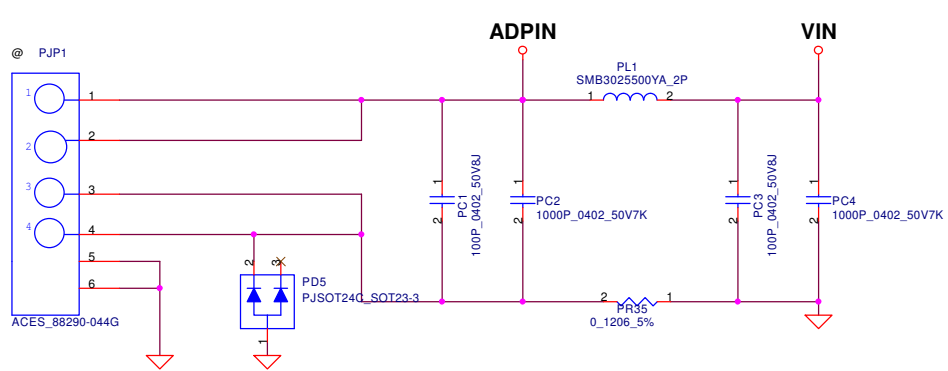
### +1.5V to +1.5VS



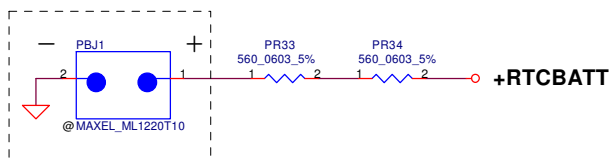
### +3VALW TO +3VS



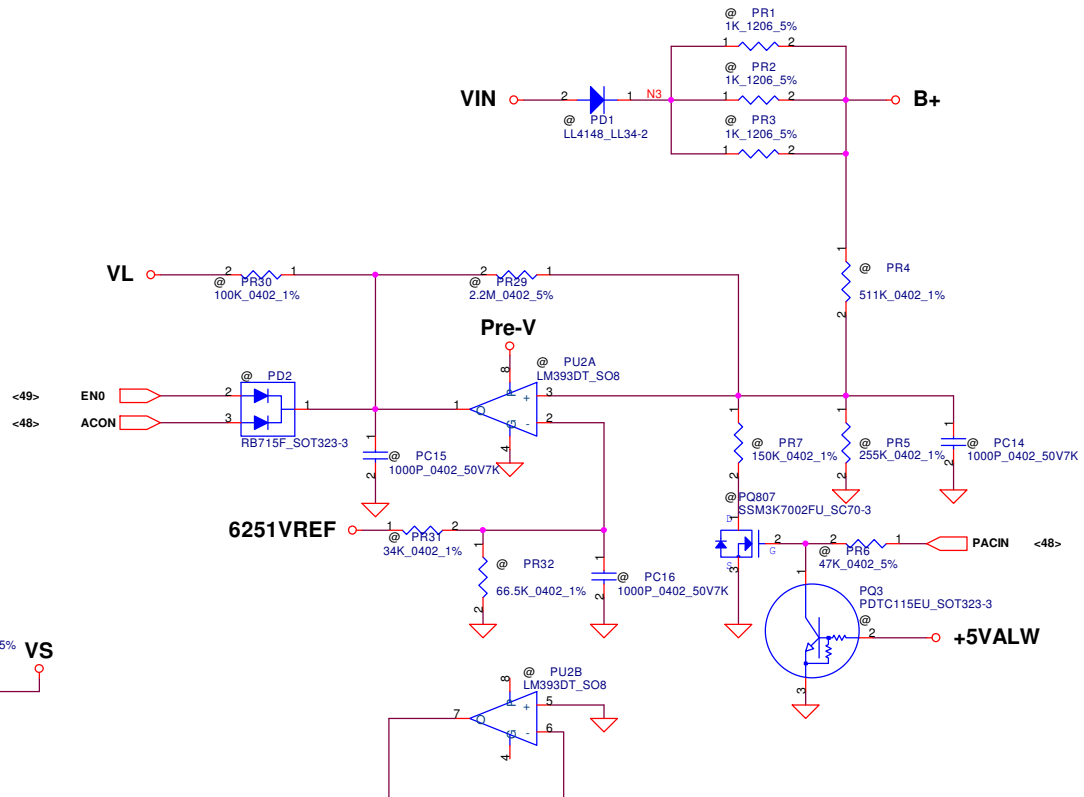
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Size	Document Number	Rev		1.0
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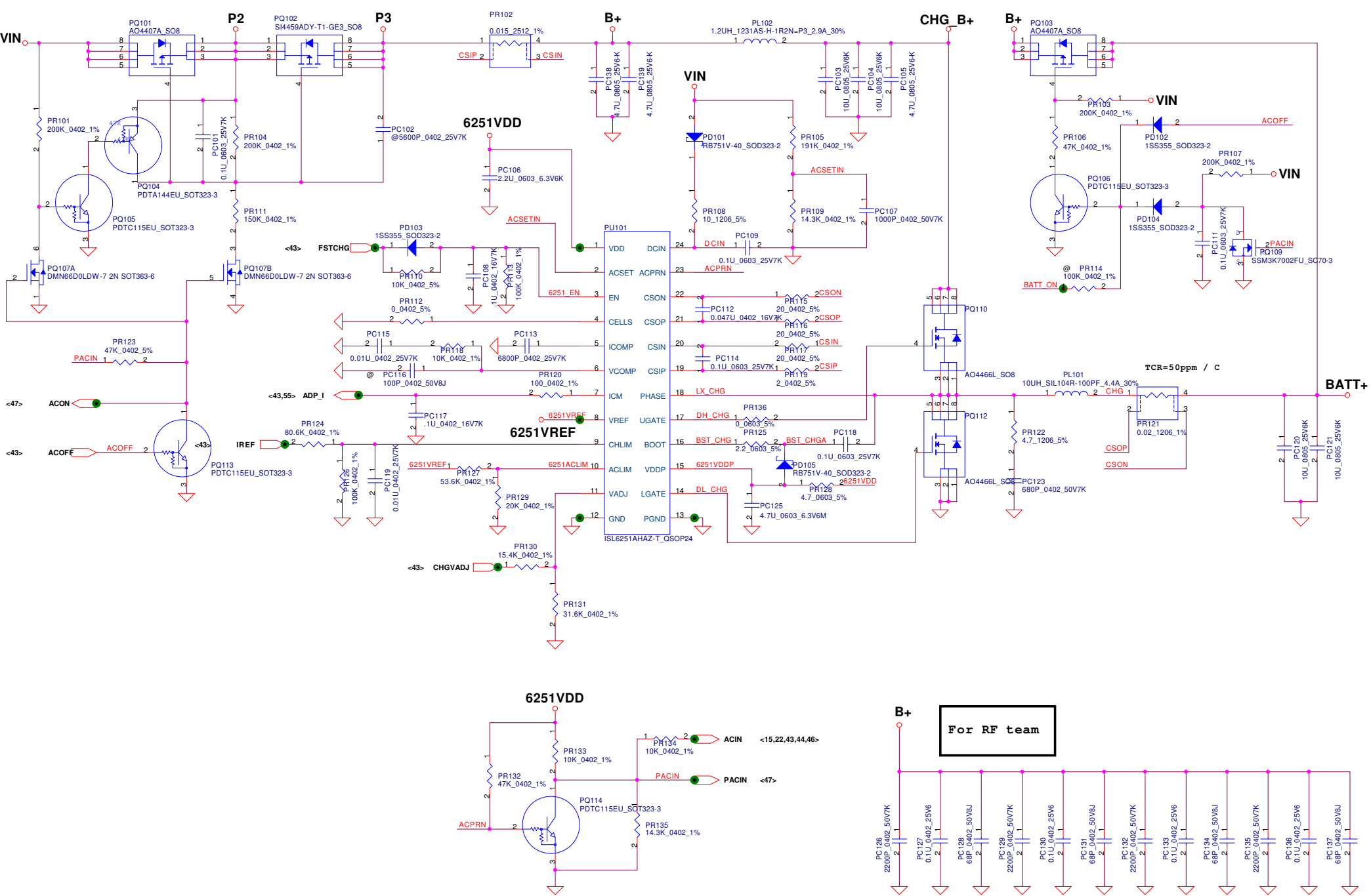
**RTC Battery**



**X7999651L01**



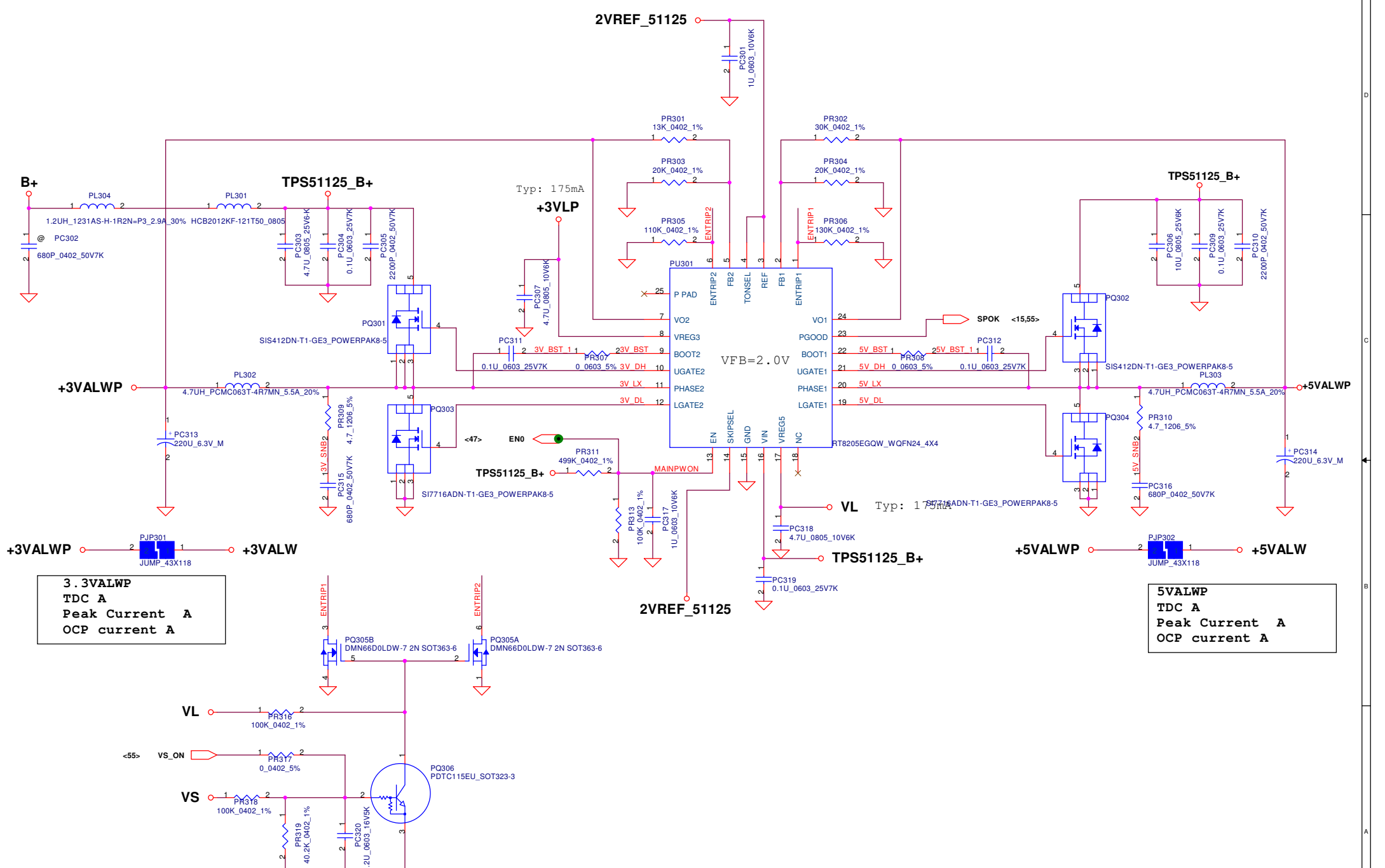
Security Classification		Compal Secret Data		Title	
Issued Date	2009/08/23	Deciphered Date	2011/12/31	<b>PWR-DCIN / Pre-Charge / RTC</b>	
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				Custom	<b>DB-806P</b>
				Date:	Monday, April 11, 2011
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For RF team

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				Size	Document Number
Customer	DB-806P	0.1			
Date:	Monday, April 11, 2011	Sheet	48	of	56

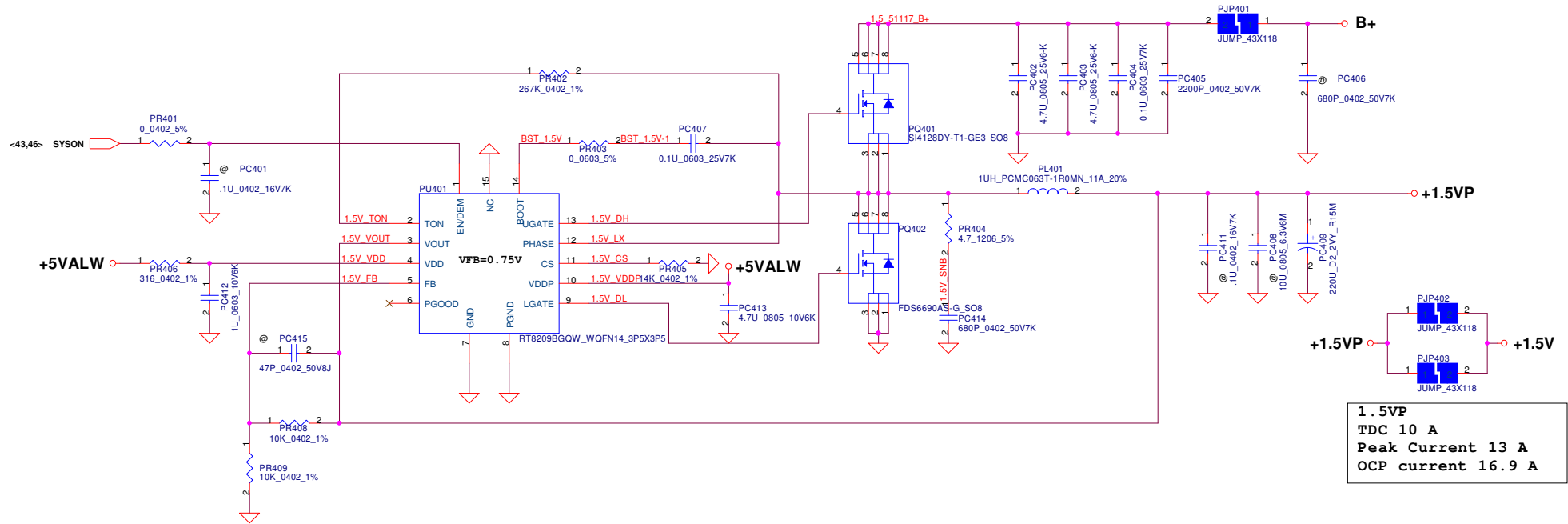




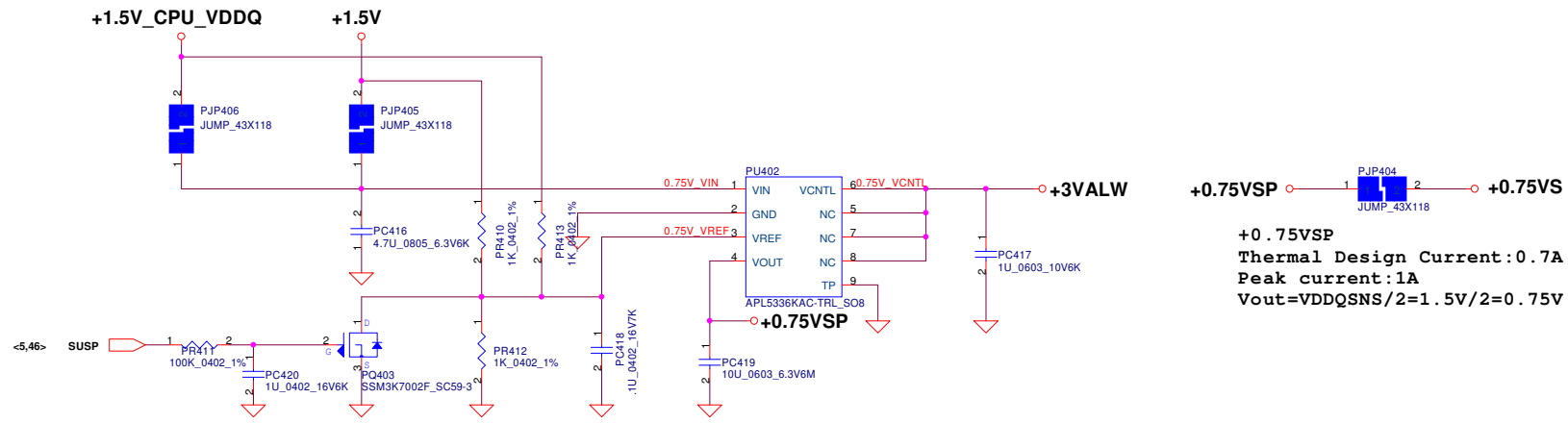
3. 3VALWP  
TDC A  
Peak Current A  
OCP current A

5VALWP  
TDC A  
Peak Current A  
OCP current A

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/08/23	Deciphered Date	2011/12/31	Title	PWR-3VALWP/5VALWP
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				Custom	DB-806P
				Date:	Monday, April 11, 2011
				Sheet	49 of 56
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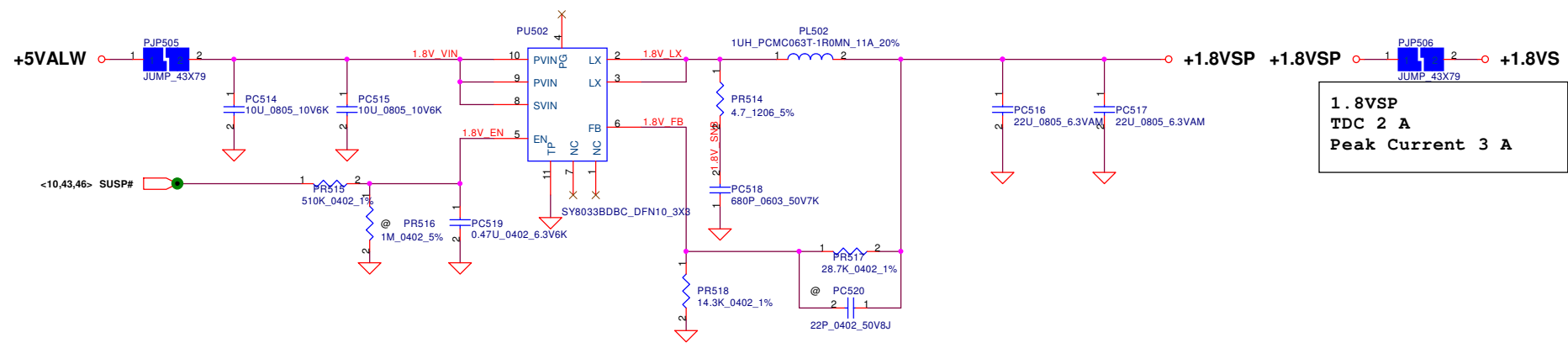
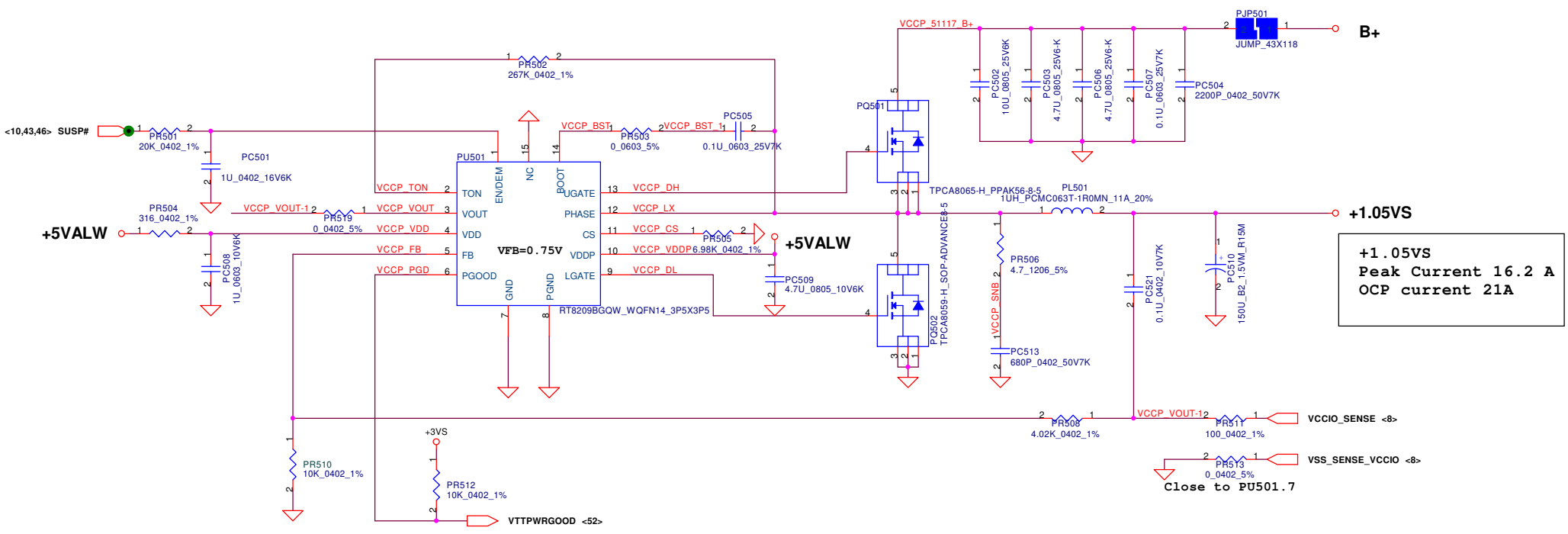


**1.5VP**  
**TDC 10 A**  
**Peak Current 13 A**  
**OCp current 16.9 A**

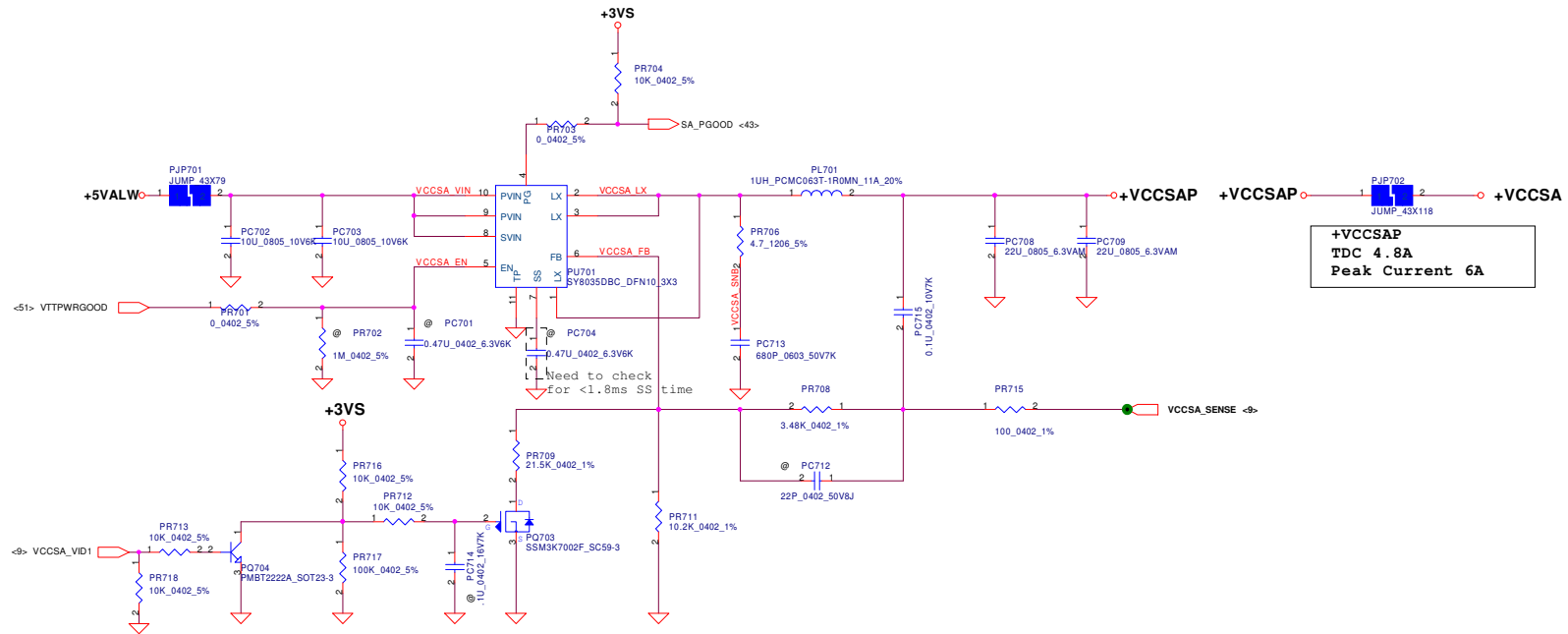


**+0.75VSP**  
**Thermal Design Current: 0.7A**  
**Peak current: 1A**  
**Vout=VDDQ/SNS/2=1.5V/2=0.75V**

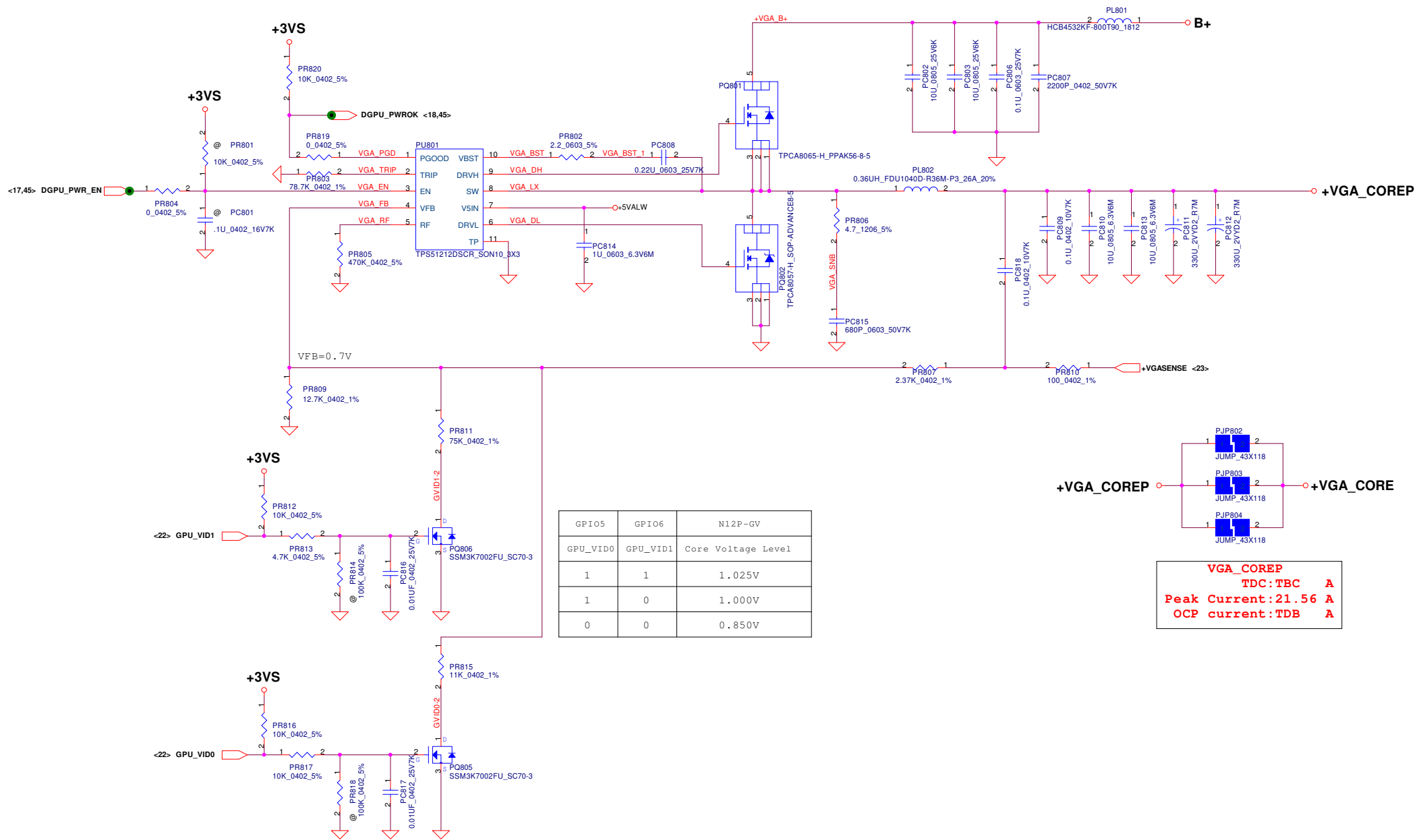
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/08/23	Deciphered Date	2011/12/31	Title	<b>PWR-1.5VP/0.75VSP</b>
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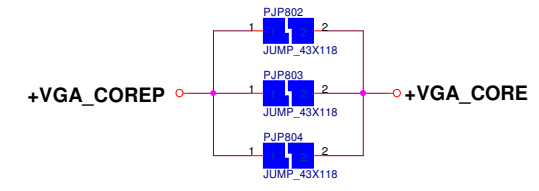
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/08/23	Deciphered Date	2011/12/31	Title	<b>PWR-VCCPP/1.8VSP</b>
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				Date:	Monday, April 11, 2011
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				Rev	0.1



VID[1]	VCCSA Vout	Required	Require on 2012
0	0.9V	Yes	Yes
1	0.8V	Yes	Yes

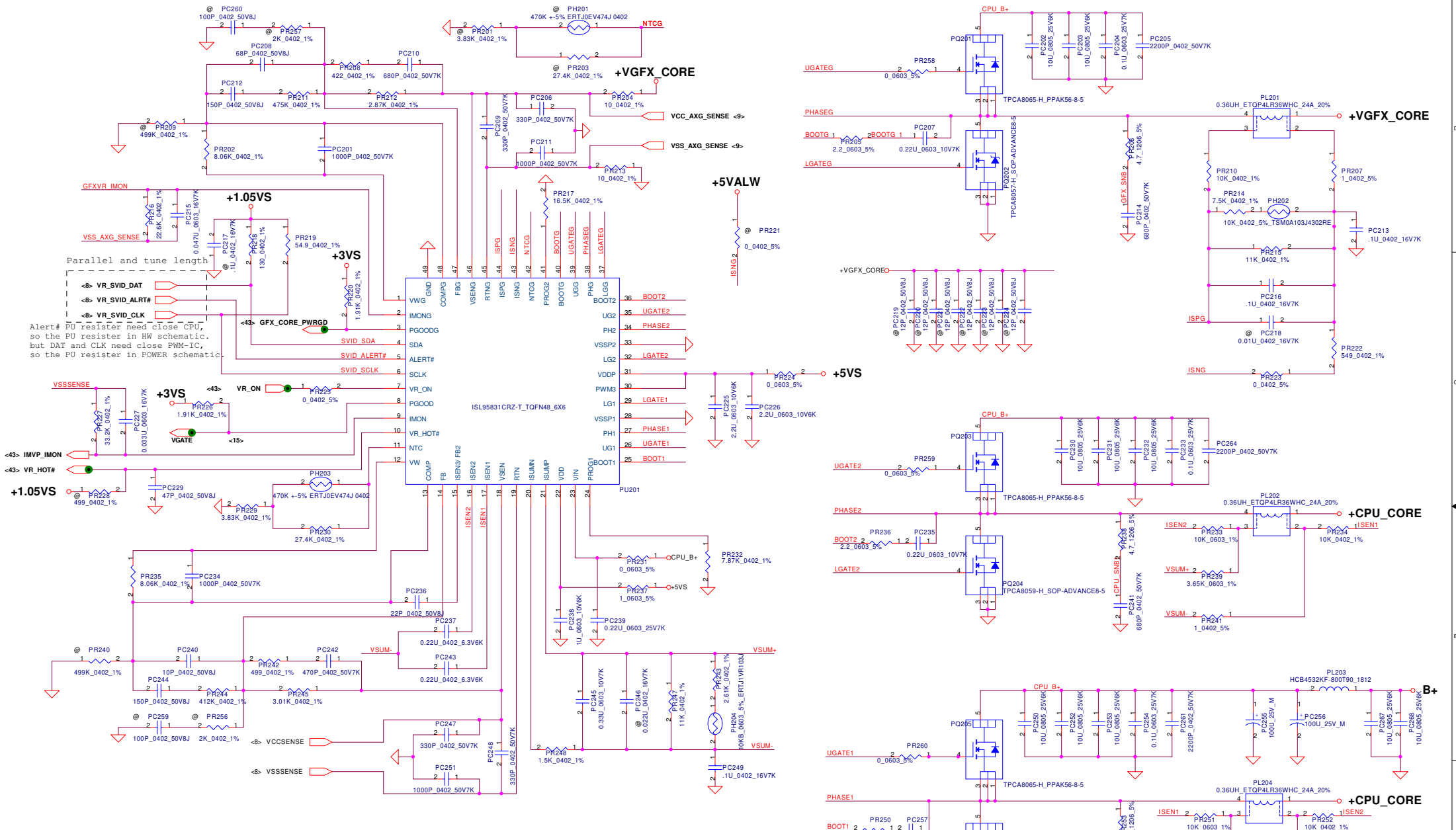


GPIO5	GPIO6	N12P-GV
GPU_VID0	GPU_VID1	Core Voltage Level
1	1	1.025V
1	0	1.000V
0	0	0.850V



**VGA\_COREP**  
 TDC:TBC A  
 Peak Current:21.56 A  
 OCP current:TDB A

Alert# PU resistor need close CPU, so the PU resistor in HW schematic, but DAT and CLK need close PWM-IC, so the PU resistor in POWER schematic.



\*Iccmax in Turbo Mode for SV (35W) is 53A

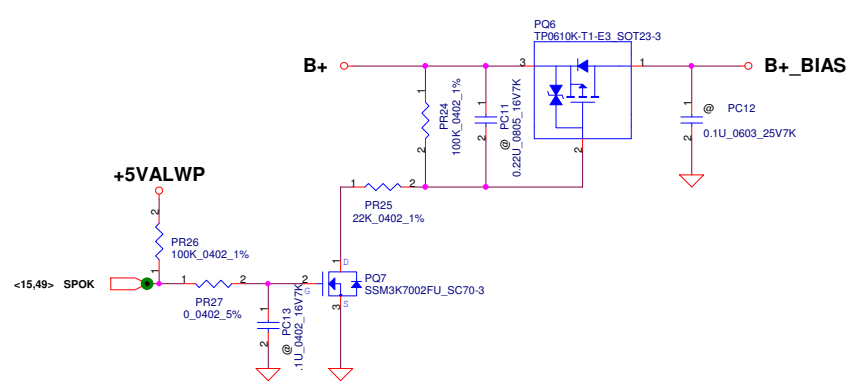
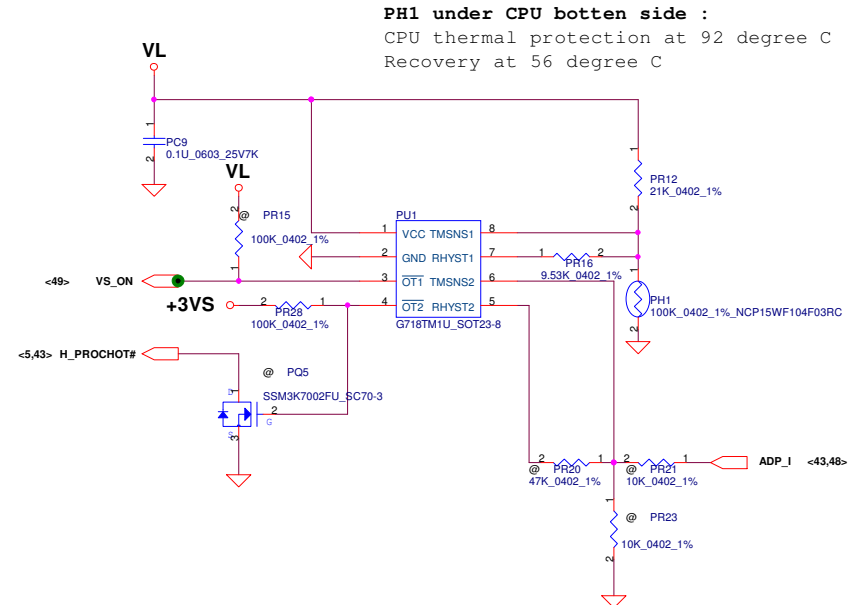
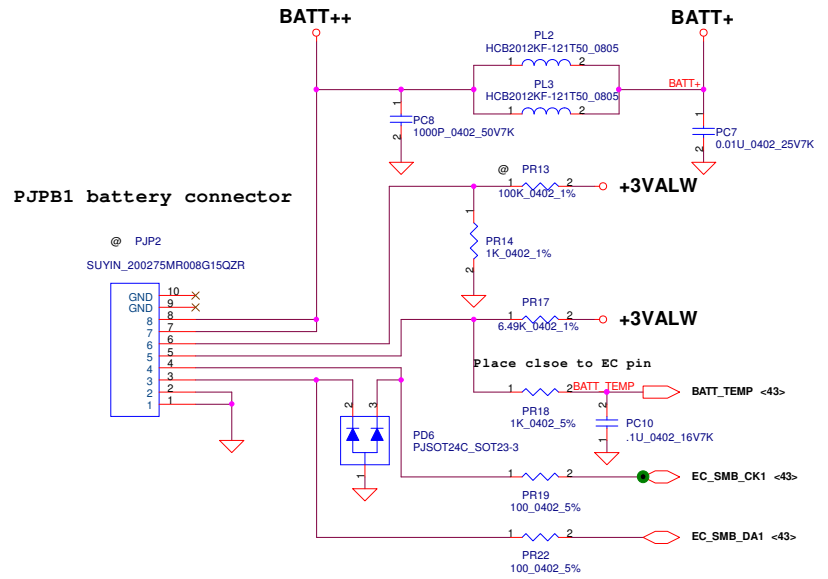
+CPU_CORE	
Icc-max=53A	
Rdson=3.6-4.5m ohm	
DCR=1.1m ohm	
HW output cap:	
(1) 10U_0805_4V *10	
(2) 22U_0805_6.3V *15	
(3) 470U_D2_2V *4 (ESR=4.5m ohm)	

\*OCP setting value=71.5A

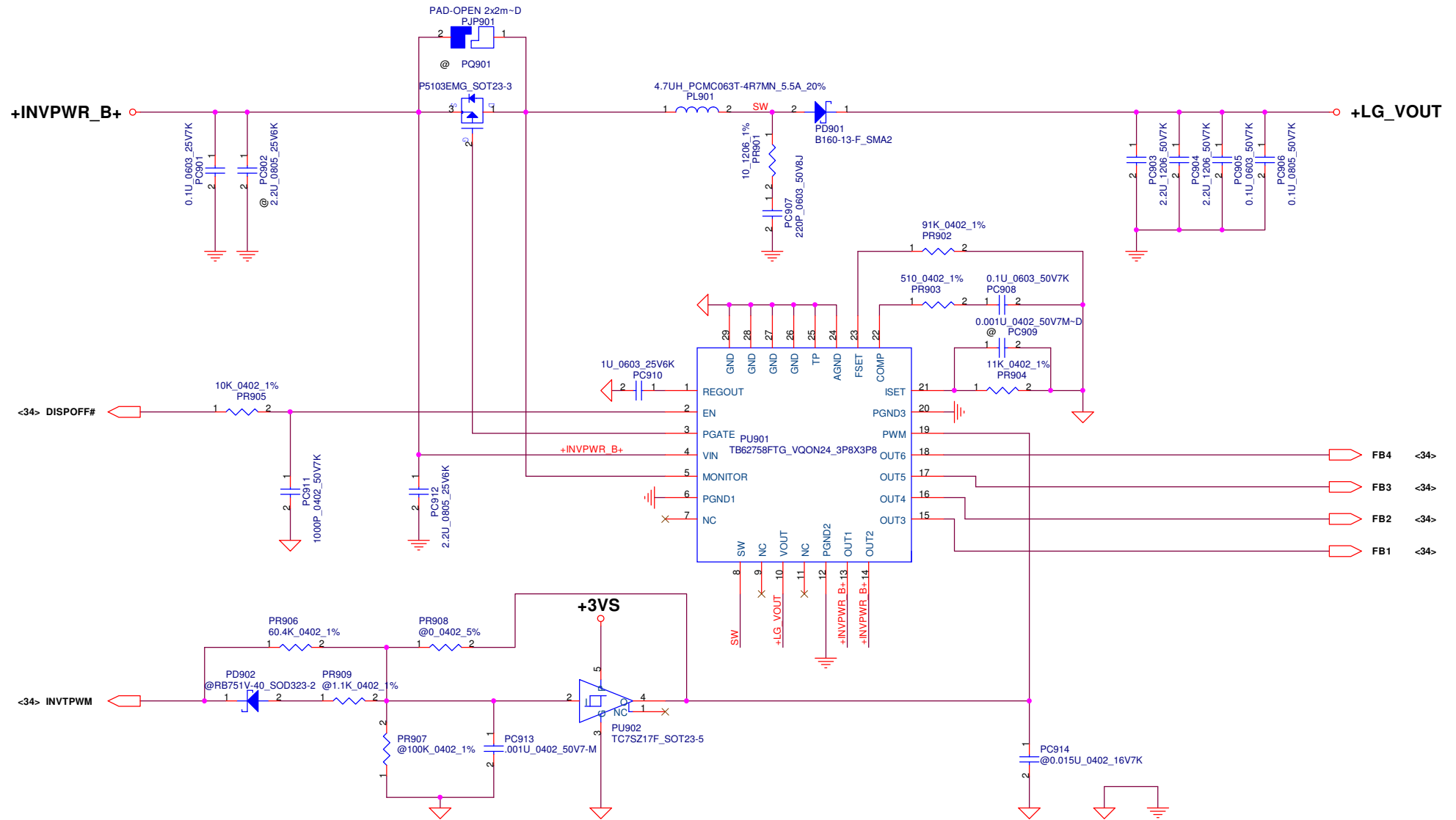
+VGFX_COREP	
Ipeak=26A, Imax=18.2A, 1.2Ipeak=31.2A	
Rdson=3.6-4.5m ohm	
DCR=1.1m ohm	
HW output cap:	
(1) 22U_0805_6.3V *12	
(2) 470U_D2_2V *2 (ESR=4.5m ohm)	

\*OCP setting value=37A

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