WR1D
BIOCK DIAGRAM

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SO-DIMM
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DDR II CHANNEL B
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PCI 2.3 133MB/s (33MHZ)

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WR1D Schematic Ver :3A

02

1. Schematic Page Description :

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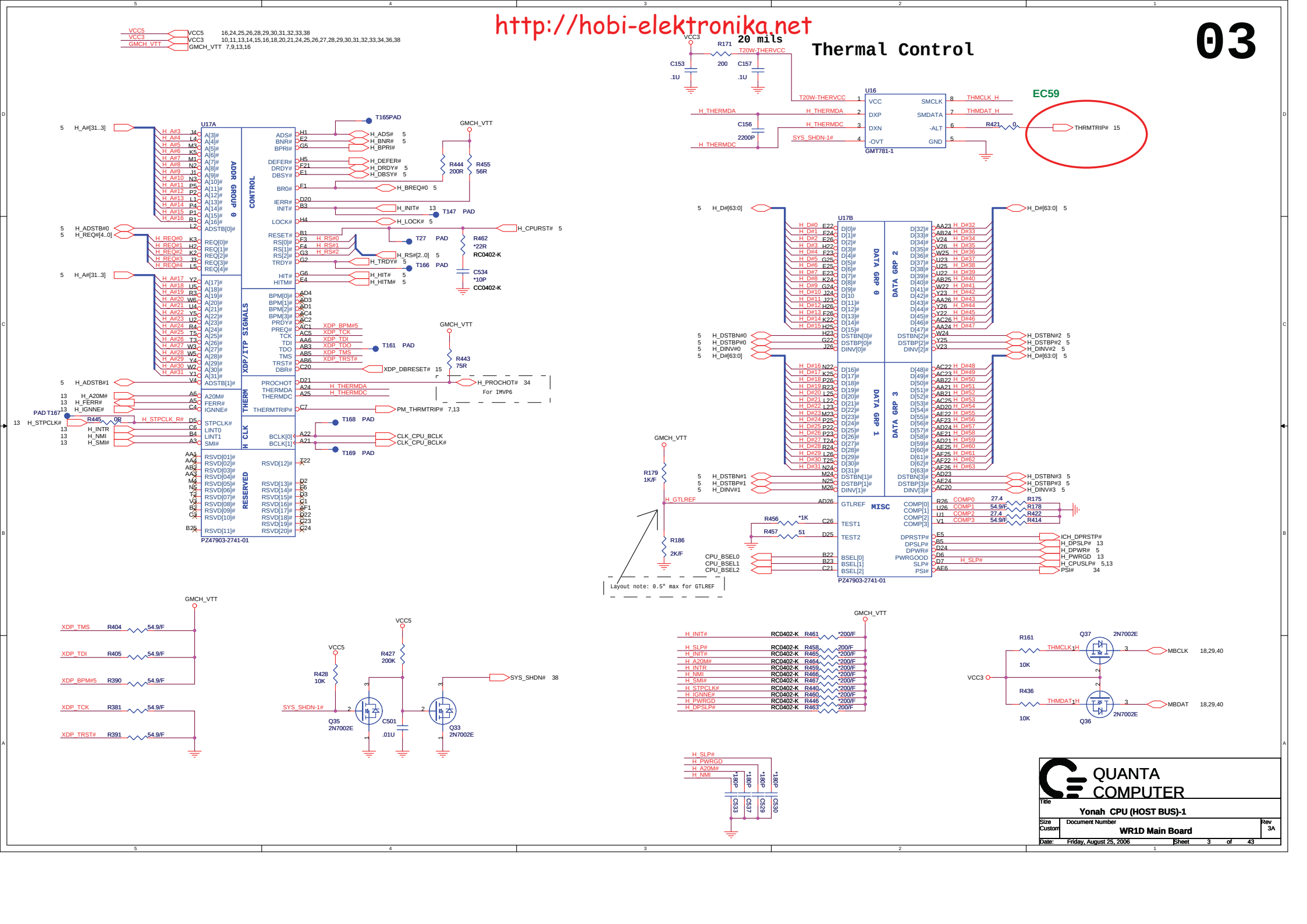
CHIP	
Port 0	BCM5751M LAN

Thermal Control



Title	Yonah CPU (HOST BUS)-1
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QUANTA COMPUTER

GMCH_VTT — GMCH_VTT 7,9,13,16
CPU_CORE — CPU_CORE 34
VCC1.5 — VCC1.5 7,8,14,16,27,38

GMCH_VTT: + C506 330U/2.5V/7343/R=12, C510 0.1U, C504 0.1U, C515 0.1U, C494 0.1U, C493 0.1U

GMCH_VTT: C503 0.1U, C519 0.1U, C485 0.1U, C498 0.1U, C500 0.1U

CPU_CORE: C528 0.1U, C525 0.1U, C478 0.1U, C526 0.1U, C484 0.1U

CPU_CORE: C527 0.1U, C538 0.1U, C476 0.1U, C477 0.1U, C536 0.1U

10U/6.3V/X5R(CC0805)
5 mOhm*35

---> 10U/4V/X5R(CC0603)
Murata

CPU_CORE: C469 10U, C531 10U, C472 10U, C474 10U, C532 10U

CPU_CORE — CPU_CORE

U17C

A7	VCC[001]	VCC[068]	AB20
A9	VCC[002]	VCC[069]	AB7
A10	VCC[003]	VCC[070]	AC7
A12	VCC[004]	VCC[071]	AC9
A13	VCC[005]	VCC[072]	AC12
A15	VCC[006]	VCC[073]	AC13
A17	VCC[007]	VCC[074]	AC15
A18	VCC[008]	VCC[075]	AC17
A20	VCC[009]	VCC[076]	AC18
B7	VCC[010]	VCC[077]	AD7
B9	VCC[011]	VCC[078]	AD9
B10	VCC[012]	VCC[079]	AD10
B12	VCC[013]	VCC[080]	AD12
B14	VCC[014]	VCC[081]	AD14
B15	VCC[015]	VCC[082]	AD15
B17	VCC[016]	VCC[083]	AD17
B18	VCC[017]	VCC[084]	AD18
B20	VCC[018]	VCC[085]	AE9
C9	VCC[019]	VCC[086]	AE10
C10	VCC[020]	VCC[087]	AE12
C12	VCC[021]	VCC[088]	AE13
C13	VCC[022]	VCC[089]	AE15
C15	VCC[023]	VCC[090]	AE17
C17	VCC[024]	VCC[091]	AE18
C18	VCC[025]	VCC[092]	AE20
D9	VCC[026]	VCC[093]	AF9
D10	VCC[027]	VCC[094]	AF10
D12	VCC[028]	VCC[095]	AF12
D14	VCC[029]	VCC[096]	AF14
D15	VCC[030]	VCC[097]	AF15
D17	VCC[031]	VCC[098]	AF17
D18	VCC[032]	VCC[099]	AF18
E7	VCC[033]	VCC[100]	AF20
E9	VCC[034]		
E10	VCC[035]	VCCP[01]	V6
E12	VCC[036]	VCCP[02]	G21
E13	VCC[037]	VCCP[03]	J6
E15	VCC[038]	VCCP[04]	K6
E17	VCC[039]	VCCP[05]	M6
E18	VCC[040]	VCCP[06]	J21
E20	VCC[041]	VCCP[07]	K21
F7	VCC[042]	VCCP[08]	M21
F9	VCC[043]	VCCP[09]	N21
F10	VCC[044]	VCCP[10]	N6
F12	VCC[045]	VCCP[11]	R21
F14	VCC[046]	VCCP[12]	R6
F15	VCC[047]	VCCP[13]	T21
F17	VCC[048]	VCCP[14]	T6
F18	VCC[049]	VCCP[15]	V21
F20	VCC[050]	VCCP[16]	W21
AA7	VCC[051]		
AA9	VCC[052]	VCCA	B26
AA10	VCC[053]		
AA12	VCC[054]		
AA13	VCC[055]	VID[0]	AD6
AA15	VCC[056]	VID[1]	AF5
AA17	VCC[057]	VID[2]	AE5
AA18	VCC[058]	VID[3]	AF4
AA20	VCC[059]	VID[4]	AE3
AB9	VCC[060]	VID[5]	AF2
AC10	VCC[061]	VID[6]	AE2
AB10	VCC[062]		
AB12	VCC[063]		
AB14	VCC[064]		
AB15	VCC[065]	VCCSENSE	AF7
AB17	VCC[066]		
AB18	VCC[067]	VSSSENSE	AE7

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GMCH_VTT — + C505 330U

VCC1.5 — C535 0.01U, C539 10U

VCC1.5

near PIN B26

CPU_VID0 34
CPU_VID1 34
CPU_VID2 34
CPU_VID3 34
CPU_VID4 34
CPU_VID5 34
CPU_VID6 34

CPU_CORE — R380 100/F — VCCSENSE 34

R375 100/F — VSSSENSE 34

GMCH_VTT: C509 0.1U, C520 0.1U, C516 0.1U, C486 0.1U, C487 0.1U, C514 0.1U

U17D

A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R2
A16	VSS[005]	VSS[086]	R5
A19	VSS[006]	VSS[087]	R22
A23	VSS[007]	VSS[088]	R25
A26	VSS[008]	VSS[089]	T1
B6	VSS[009]	VSS[090]	T4
B8	VSS[010]	VSS[091]	T23
B11	VSS[011]	VSS[092]	T26
B13	VSS[012]	VSS[093]	U3
B16	VSS[013]	VSS[094]	U6
B19	VSS[014]	VSS[095]	U21
B21	VSS[015]	VSS[096]	U24
B24	VSS[016]	VSS[097]	V2
C5	VSS[017]	VSS[098]	V5
C8	VSS[018]	VSS[099]	V22
C11	VSS[019]	VSS[100]	V25
C14	VSS[020]	VSS[101]	W1
C16	VSS[021]	VSS[102]	W4
C19	VSS[022]	VSS[103]	W23
C2	VSS[023]	VSS[104]	W26
C22	VSS[024]	VSS[105]	Y3
C25	VSS[025]	VSS[106]	Y6
D1	VSS[026]	VSS[107]	Y21
D4	VSS[027]	VSS[108]	Y24
D8	VSS[028]	VSS[109]	AA2
D11	VSS[029]	VSS[110]	AA5
D13	VSS[030]	VSS[111]	AA8
D16	VSS[031]	VSS[112]	AA11
D19	VSS[032]	VSS[113]	AA14
D23	VSS[033]	VSS[114]	AA16
D26	VSS[034]	VSS[115]	AA19
E3	VSS[035]	VSS[116]	AA22
E6	VSS[036]	VSS[117]	AA25
E8	VSS[037]	VSS[118]	AB1
E11	VSS[038]	VSS[119]	AB4
E14	VSS[039]	VSS[120]	AB8
E16	VSS[040]	VSS[121]	AB11
E19	VSS[041]	VSS[122]	AB13
E21	VSS[042]	VSS[123]	AB16
E24	VSS[043]	VSS[124]	AB19
F5	VSS[044]	VSS[125]	AB23
F8	VSS[045]	VSS[126]	AB26
F11	VSS[046]	VSS[127]	AC3
F13	VSS[047]	VSS[128]	AC6
F16	VSS[048]	VSS[129]	AC8
F19	VSS[049]	VSS[130]	AC11
F2	VSS[050]	VSS[131]	AC14
F22	VSS[051]	VSS[132]	AC16
F25	VSS[052]	VSS[133]	AC19
G4	VSS[053]	VSS[134]	AC21
G1	VSS[054]	VSS[135]	AC24
G23	VSS[055]	VSS[136]	AD2
G26	VSS[056]	VSS[137]	AD5
H3	VSS[057]	VSS[138]	AD8
H6	VSS[058]	VSS[139]	AD11
H21	VSS[059]	VSS[140]	AD13
H24	VSS[060]	VSS[141]	AD16
J2	VSS[061]	VSS[142]	AD19
J5	VSS[062]	VSS[143]	AD22
J22	VSS[063]	VSS[144]	AD25
J25	VSS[064]	VSS[145]	AE1
K1	VSS[065]	VSS[146]	AE4
K4	VSS[066]	VSS[147]	AE8
K23	VSS[067]	VSS[148]	AE11
K26	VSS[068]	VSS[149]	AE14
L3	VSS[069]	VSS[150]	AE16
L6	VSS[070]	VSS[151]	AE19
L21	VSS[071]	VSS[152]	AE23
L24	VSS[072]	VSS[153]	AE26
M2	VSS[073]	VSS[154]	AF3
M5	VSS[074]	VSS[155]	AF6
M22	VSS[075]	VSS[156]	AF8
M25	VSS[076]	VSS[157]	AF11
N1	VSS[077]	VSS[158]	AF13
N4	VSS[078]	VSS[159]	AF16
N23	VSS[079]	VSS[160]	AF19
N26	VSS[080]	VSS[161]	AF21
P3	VSS[081]	VSS[162]	AF24

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Title: Yonah CPU (POWER/NC)-2

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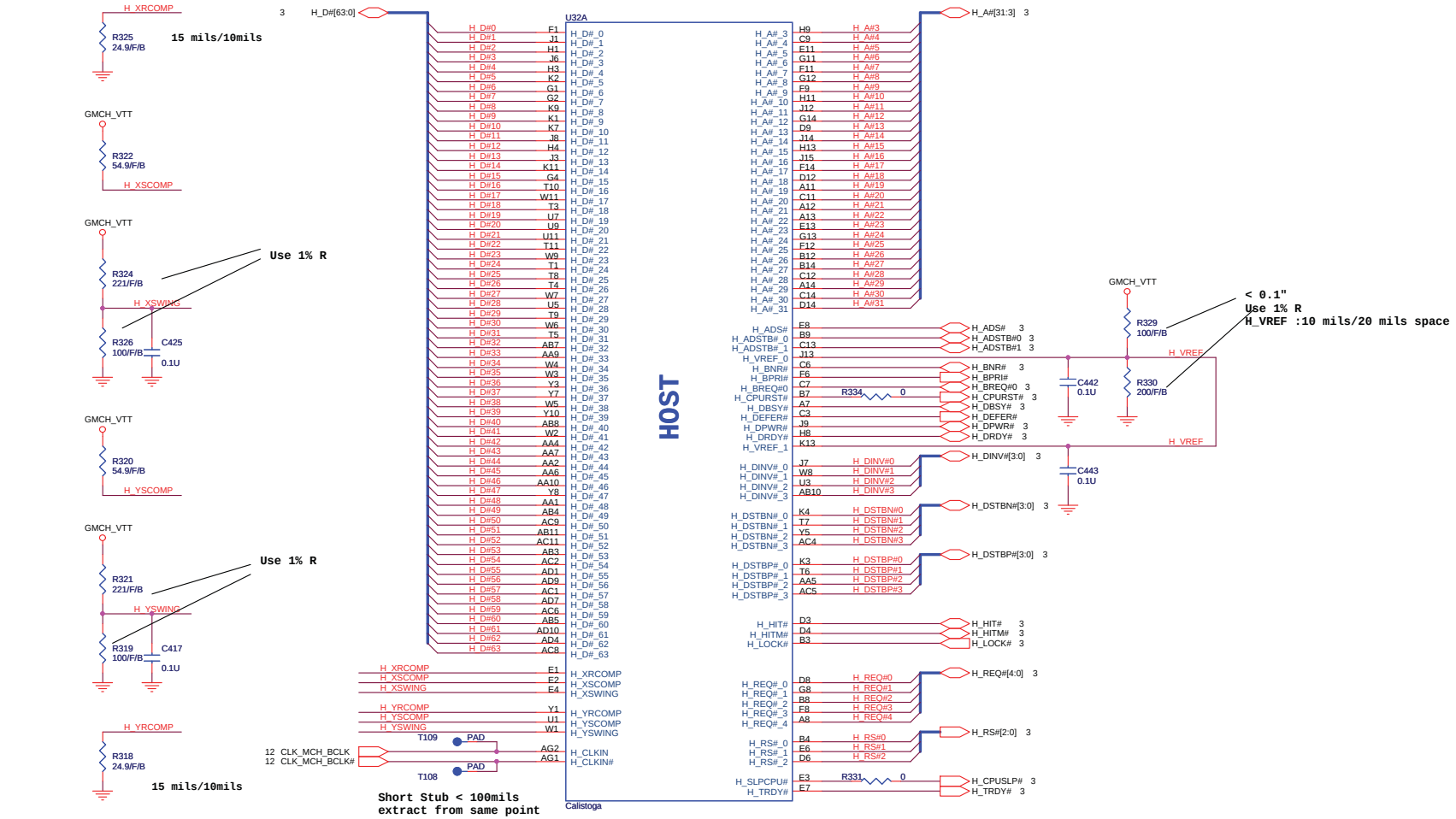

QUANTA COMPUTER			
Title: Calistoga HOST 1/6			
Size: Custom	Document Number: WR1D MAIN BOARD	Rev: 3A	
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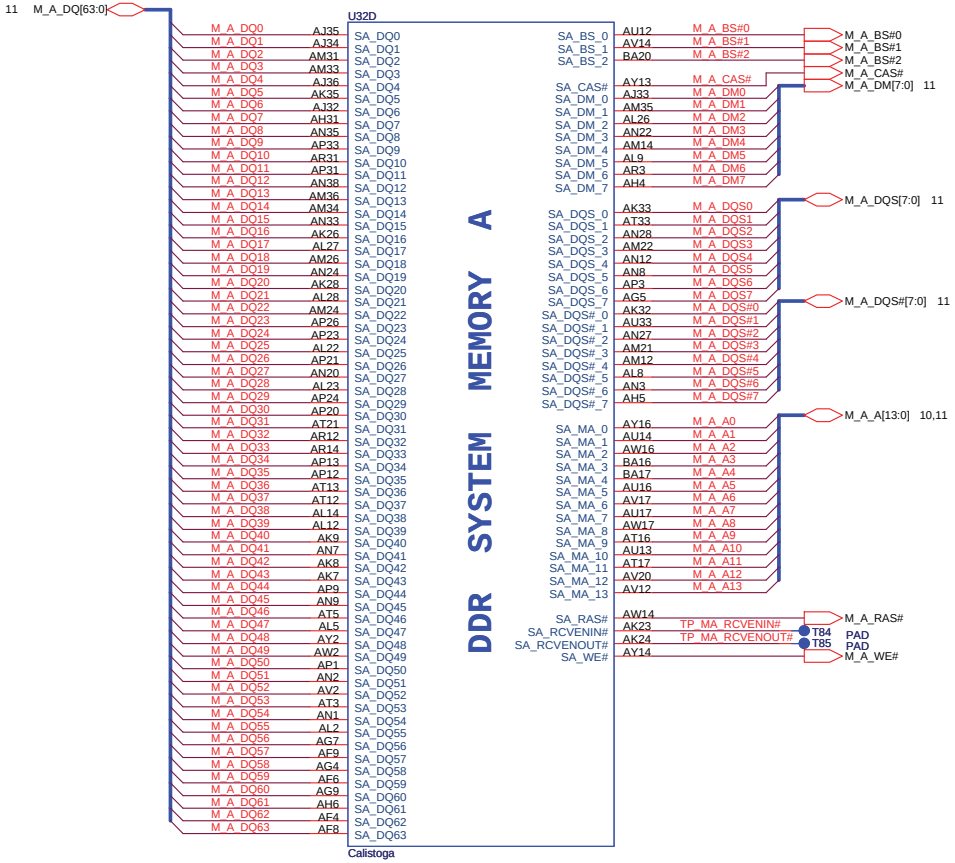

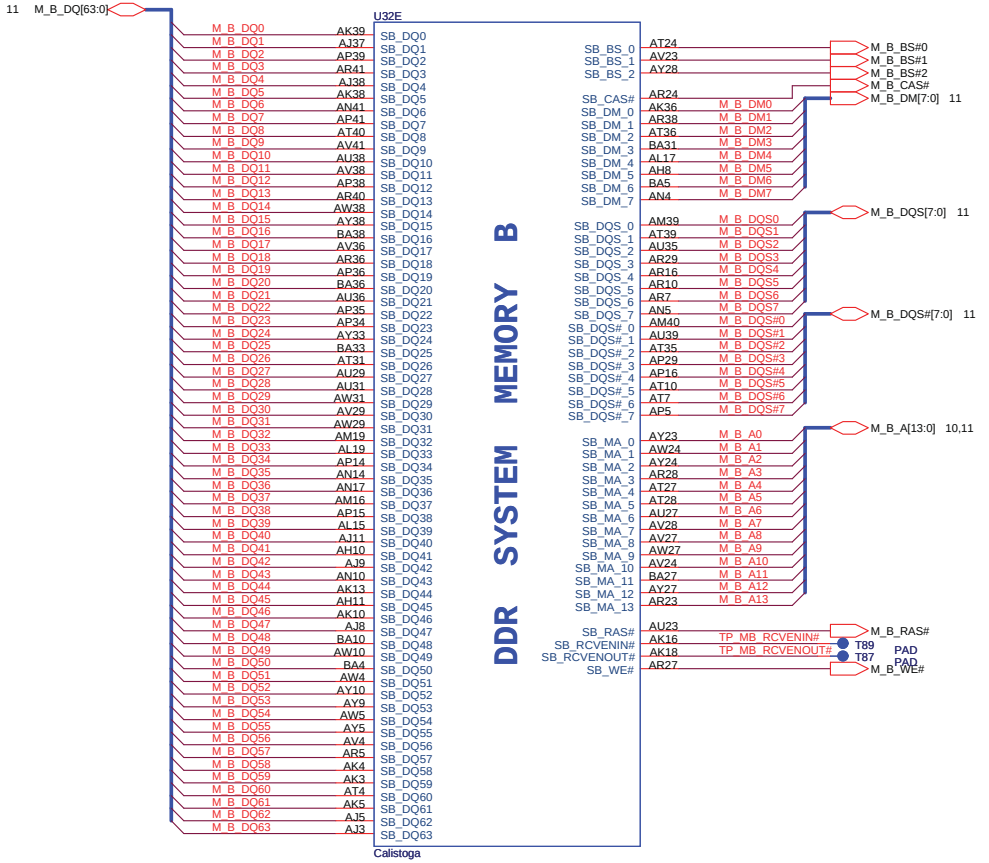

QUANTA COMPUTER

Title	Calistoga DDRII 2/6	
Size: Custom	Document Number: WR1D MAIN BOARD	Rev: 3A
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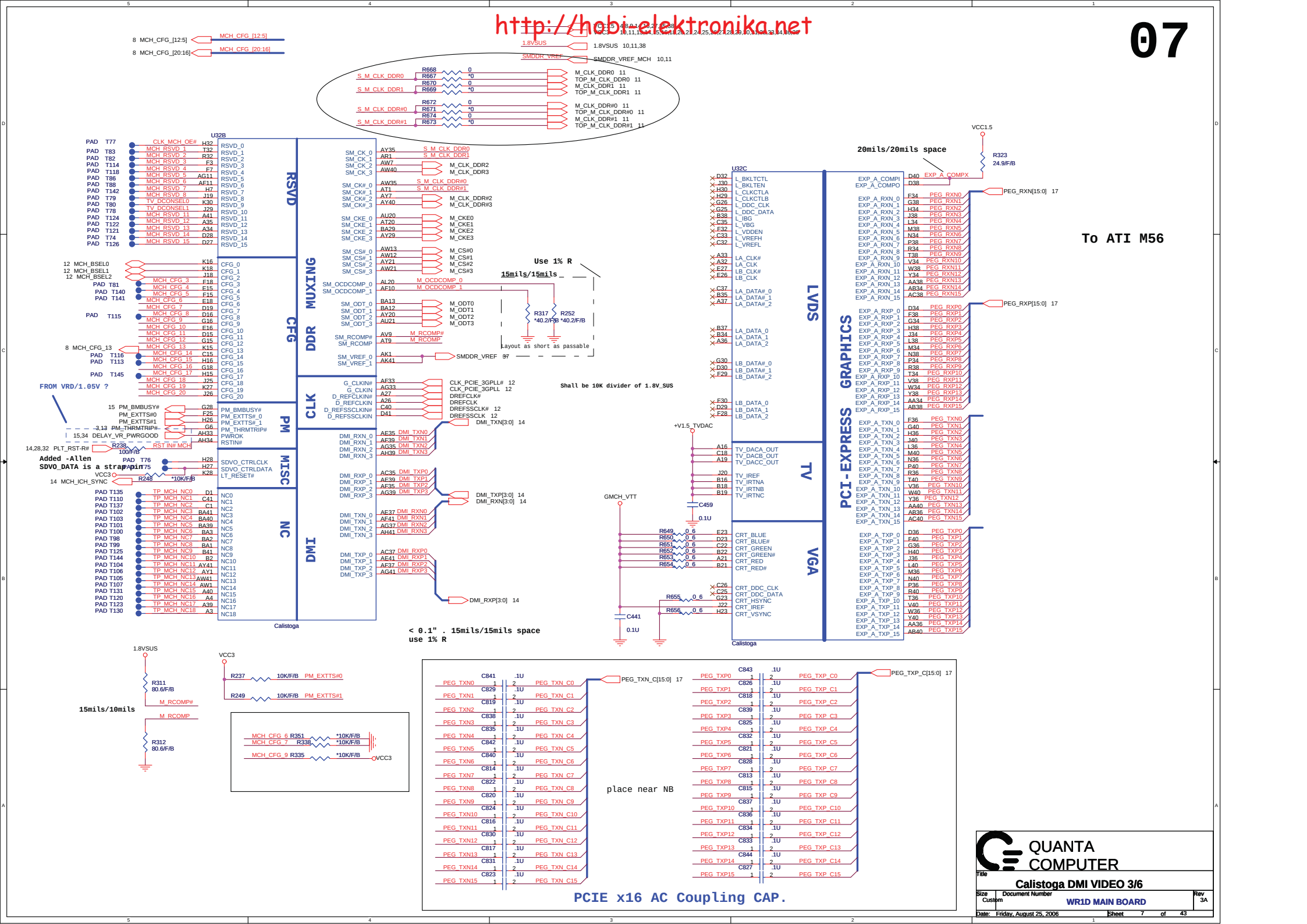

Title	Calistoga DMI VIDEO 3/6
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QUANTA COMPUTER

GMCH_VTT
VCC1.5
VCC3
1.8VSUS

GMCH_VTT 7,9,13,16
VCC1.5 4,7,9,14,16,27,35,38
VCC3 10,11,13,14,15,16,18,20,21,24,25,26,27,28,29,30,31,32,33,34,36,38
1.8VSUS 10,11,38

U32G

GMCH_VTT — C420 330U/2.5V/ESR=9mOS

VCC_0 VCC_1 VCC_2 VCC_3 VCC_4 VCC_5 VCC_6 VCC_7 VCC_8 VCC_9 VCC_10 VCC_11 VCC_12 VCC_13 VCC_14 VCC_15 VCC_16 VCC_17 VCC_18 VCC_19 VCC_20 VCC_21 VCC_22 VCC_23 VCC_24 VCC_25 VCC_26 VCC_27 VCC_28 VCC_29 VCC_30 VCC_31 VCC_32 VCC_33 VCC_34 VCC_35 VCC_36 VCC_37 VCC_38 VCC_39 VCC_40 VCC_41 VCC_42 VCC_43 VCC_44 VCC_45 VCC_46 VCC_47 VCC_48 VCC_49 VCC_50 VCC_51 VCC_52 VCC_53 VCC_54 VCC_55 VCC_56 VCC_57 VCC_58 VCC_59 VCC_60 VCC_61 VCC_62 VCC_63 VCC_64 VCC_65 VCC_66 VCC_67 VCC_68 VCC_69 VCC_70 VCC_71 VCC_72 VCC_73 VCC_74 VCC_75 VCC_76 VCC_77 VCC_78 VCC_79 VCC_80 VCC_81 VCC_82 VCC_83 VCC_84 VCC_85 VCC_86 VCC_87 VCC_88 VCC_89 VCC_90 VCC_91 VCC_92 VCC_93 VCC_94 VCC_95 VCC_96 VCC_97 VCC_98 VCC_99 VCC_100 VCC_101 VCC_102 VCC_103 VCC_104 VCC_105 VCC_106 VCC_107 VCC_108 VCC_109 VCC_110

VCC

VCC_SM_0 VCC_SM_1 VCC_SM_2 VCC_SM_3 VCC_SM_4 VCC_SM_5 VCC_SM_6 VCC_SM_7 VCC_SM_8 VCC_SM_9 VCC_SM_10 VCC_SM_11 VCC_SM_12 VCC_SM_13 VCC_SM_14 VCC_SM_15 VCC_SM_16 VCC_SM_17 VCC_SM_18 VCC_SM_19 VCC_SM_20 VCC_SM_21 VCC_SM_22 VCC_SM_23 VCC_SM_24 VCC_SM_25 VCC_SM_26 VCC_SM_27 VCC_SM_28 VCC_SM_29 VCC_SM_30 VCC_SM_31 VCC_SM_32 VCC_SM_33 VCC_SM_34 VCC_SM_35 VCC_SM_36 VCC_SM_37 VCC_SM_38 VCC_SM_39 VCC_SM_40 VCC_SM_41 VCC_SM_42 VCC_SM_43 VCC_SM_44 VCC_SM_45 VCC_SM_46 VCC_SM_47 VCC_SM_48 VCC_SM_49 VCC_SM_50 VCC_SM_51 VCC_SM_52 VCC_SM_53 VCC_SM_54 VCC_SM_55 VCC_SM_56 VCC_SM_57 VCC_SM_58 VCC_SM_59 VCC_SM_60 VCC_SM_61 VCC_SM_62 VCC_SM_63 VCC_SM_64 VCC_SM_65 VCC_SM_66 VCC_SM_67 VCC_SM_68 VCC_SM_69 VCC_SM_70 VCC_SM_71 VCC_SM_72 VCC_SM_73 VCC_SM_74 VCC_SM_75 VCC_SM_76 VCC_SM_77 VCC_SM_78 VCC_SM_79 VCC_SM_80 VCC_SM_81 VCC_SM_82 VCC_SM_83 VCC_SM_84 VCC_SM_85 VCC_SM_86 VCC_SM_87 VCC_SM_88 VCC_SM_89 VCC_SM_90 VCC_SM_91 VCC_SM_92 VCC_SM_93 VCC_SM_94 VCC_SM_95 VCC_SM_96 VCC_SM_97 VCC_SM_98 VCC_SM_99 VCC_SM_100 VCC_SM_101 VCC_SM_102 VCC_SM_103 VCC_SM_104 VCC_SM_105 VCC_SM_106 VCC_SM_107

Calistoga

25mils

AU41 VCC_SM1 — C406 0.47U
AM41 VCC_SM2 — C411 0.47U

1.8VSUS

120mils

PC76 330U 2.5 — C400 10U/X6S — C401 10U/X6S — C335 0.47U — C382 0.1U — C381 0.1U — C380 0.1U

place C403 on BA23 Ball

C336 0.47U — C403 0.47U

place C336 on AJ23 Ball

place C338 on BA15 Ball

C338 0.47U

25mils

AV1 VCC_SM106 — C409 0.47U
AJ1 VCC_SM107 — C412 0.47U

25mils

intel WW51 recommand

C422 330U/2.5V/ESR=9mOS — C248 10U/X6S — C444 10U/X6S — C249 1U — C242 0.1U — C246 0.1U — C247 0.1U

U32F

VCC_NCTF0 VCC_NCTF1 VCC_NCTF2 VCC_NCTF3 VCC_NCTF4 VCC_NCTF5 VCC_NCTF6 VCC_NCTF7 VCC_NCTF8 VCC_NCTF9 VCC_NCTF10 VCC_NCTF11 VCC_NCTF12 VCC_NCTF13 VCC_NCTF14 VCC_NCTF15 VCC_NCTF16 VCC_NCTF17 VCC_NCTF18 VCC_NCTF19 VCC_NCTF20 VCC_NCTF21 VCC_NCTF22 VCC_NCTF23 VCC_NCTF24 VCC_NCTF25 VCC_NCTF26 VCC_NCTF27 VCC_NCTF28 VCC_NCTF29 VCC_NCTF30 VCC_NCTF31 VCC_NCTF32 VCC_NCTF33 VCC_NCTF34 VCC_NCTF35 VCC_NCTF36 VCC_NCTF37 VCC_NCTF38 VCC_NCTF39 VCC_NCTF40 VCC_NCTF41 VCC_NCTF42 VCC_NCTF43 VCC_NCTF44 VCC_NCTF45 VCC_NCTF46 VCC_NCTF47 VCC_NCTF48 VCC_NCTF49 VCC_NCTF50 VCC_NCTF51 VCC_NCTF52 VCC_NCTF53 VCC_NCTF54 VCC_NCTF55 VCC_NCTF56 VCC_NCTF57 VCC_NCTF58 VCC_NCTF59 VCC_NCTF60 VCC_NCTF61 VCC_NCTF62 VCC_NCTF63 VCC_NCTF64 VCC_NCTF65 VCC_NCTF66 VCC_NCTF67 VCC_NCTF68 VCC_NCTF69 VCC_NCTF70 VCC_NCTF71 VCC_NCTF72

NCTF

VSS_NCTF0 VSS_NCTF1 VSS_NCTF2 VSS_NCTF3 VSS_NCTF4 VSS_NCTF5 VSS_NCTF6 VSS_NCTF7 VSS_NCTF8 VSS_NCTF9 VSS_NCTF10 VSS_NCTF11 VSS_NCTF12

VCCAUX_NCTF0 VCCAUX_NCTF1 VCCAUX_NCTF2 VCCAUX_NCTF3 VCCAUX_NCTF4 VCCAUX_NCTF5 VCCAUX_NCTF6 VCCAUX_NCTF7 VCCAUX_NCTF8 VCCAUX_NCTF9 VCCAUX_NCTF10 VCCAUX_NCTF11 VCCAUX_NCTF12 VCCAUX_NCTF13 VCCAUX_NCTF14 VCCAUX_NCTF15 VCCAUX_NCTF16 VCCAUX_NCTF17 VCCAUX_NCTF18 VCCAUX_NCTF19 VCCAUX_NCTF20 VCCAUX_NCTF21 VCCAUX_NCTF22 VCCAUX_NCTF23 VCCAUX_NCTF24 VCCAUX_NCTF25 VCCAUX_NCTF26 VCCAUX_NCTF27 VCCAUX_NCTF28 VCCAUX_NCTF29 VCCAUX_NCTF30 VCCAUX_NCTF31 VCCAUX_NCTF32 VCCAUX_NCTF33 VCCAUX_NCTF34 VCCAUX_NCTF35 VCCAUX_NCTF36 VCCAUX_NCTF37 VCCAUX_NCTF38 VCCAUX_NCTF39 VCCAUX_NCTF40 VCCAUX_NCTF41 VCCAUX_NCTF42 VCCAUX_NCTF43 VCCAUX_NCTF44 VCCAUX_NCTF45 VCCAUX_NCTF46 VCCAUX_NCTF47 VCCAUX_NCTF48 VCCAUX_NCTF49 VCCAUX_NCTF50 VCCAUX_NCTF51 VCCAUX_NCTF52 VCCAUX_NCTF53 VCCAUX_NCTF54 VCCAUX_NCTF55 VCCAUX_NCTF56 VCCAUX_NCTF57

Calistoga

VCC1.5

100mils

Have to review again
ADD Matrix in silkscreen

GMCH Strap pin

7	MCH_CFG_5	R348	*2.2K/B	
7	MCH_CFG_6	R350	*2.2K/B	
7	MCH_CFG_7	R339	*2.2K/B	
7	MCH_CFG_9	R336	*2.2K/B	
7	MCH_CFG_10	R337	*2.2K/B	
7	MCH_CFG_11	R346	2.2K/B	
7	MCH_CFG_12	R347	2.2K/B	
7	MCH_CFG_13	R345	2.2K/B	
7	MCH_CFG_16	R349	*2.2K/B	
7	MCH_CFG_18	R234	1K/F/B CFG_RSVD_0_R	VCC3 R235 *0/B
7	MCH_CFG_19	R251	*1K/F/B	VCC3
7	MCH_CFG_20	R250	*1K/F/B	VCC3

1.MCH_CFG_5 Low = DMI X2, High=DMIX4

2.MCH_CFG_6 DDR : Low =Moby Dick, High= Calistoga (Default)

3.MCH_CFG_7 CPU Strap Low=RSVD, High=Mobile CPU

4.MCH_CFG_9 PCI Exp Graphics Lane: Low =Reserved,High=Mobility

5.MCH_CFG_10 Host PLL VCC Select: Low=Reserved, High=Mobility

6.MCH_CFG_11: Low=Calistoga, High=Reserved

7.MCH_CFG_16 FSB Dynmic ODT: Low=Dynamic ODT Disabled,
High=Dynamic ODT Enabled.

8.MCH_CFG_18 VCC Select: LOW=1.05V, High=1.5V

9.MCH_CFG_19 DMI LANE Reversal:Low=Normal,High=LANES Reversed.

10.MCH_CFG_20 PCIE Backward interpoerability mode: Low= only SDVO or PCIE x1 is operational (defaults) ,High=SDVO and PCIE x1 are operation simultaneously via the PEG port.

QUANTA COMPUTER

Title: Calistoga Power&Strap 4/6

Size	Document Number	Rev
Custom	WR1D MAIN BOARD	3A

Date: Friday, August 25, 2006 Sheet 8 of 43

VCC1.5 — VCC1.5 — 7,8,14,16,27,38
VCC2.5 — VCC2.5 — 18,20,38
VCC3 — VCC3 — 10,11,13,14,15,16,18,20,21,24,25,26,27,28,29,30,31,32,33,34,36,38

U32H — POWER — Calistoga

Shall Add more bypass caps for 1.05V

VTT_56 , VTT_71 and 72 are attached with 0.1u seperated .Checking

80mils

60mils

40mils

RC0805

Oregianl FCM2012C-181 "CX000181008"

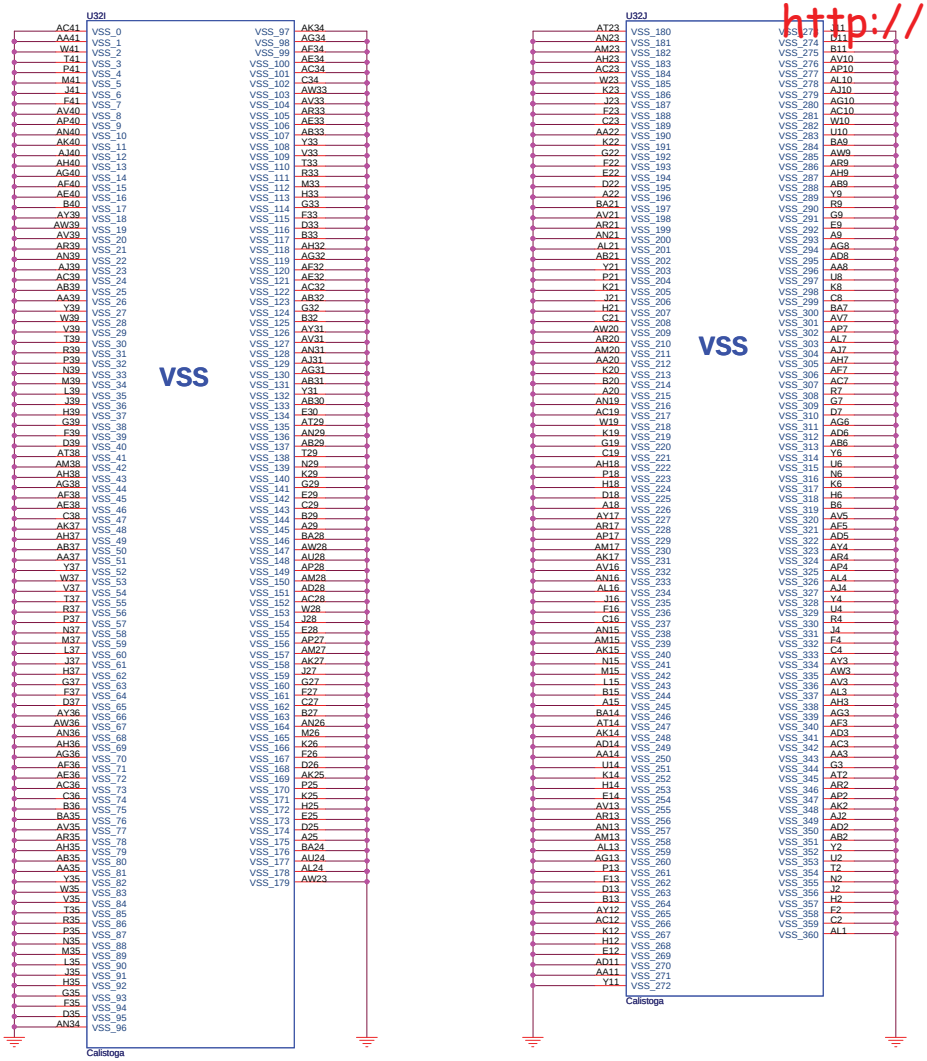
QUANTA COMPUTER

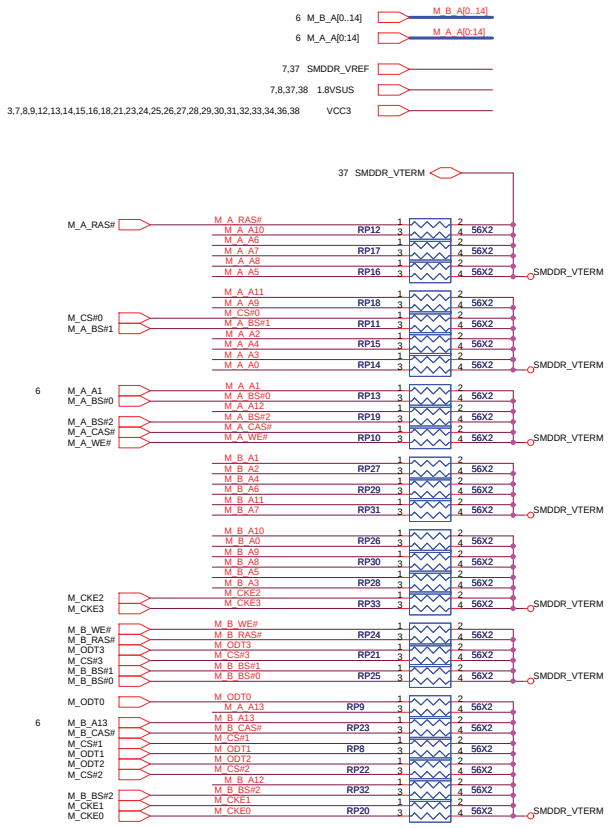
Title: Calistoga Power 2 5/6

Size: Custom | Document Number: WR1D MAIN BOARD | Rev: 3A

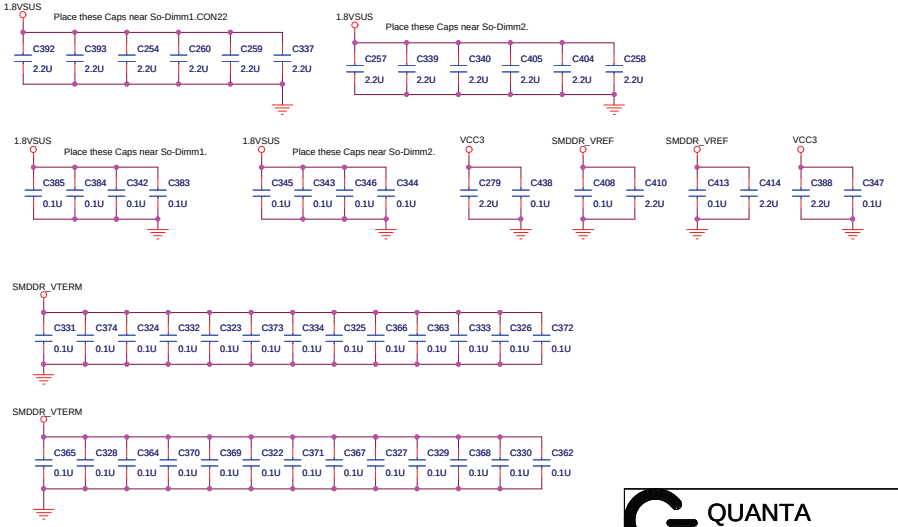
Date: Friday, August 25, 2006 | Sheet 9 of 43

2DPC Terminal Resistor





Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

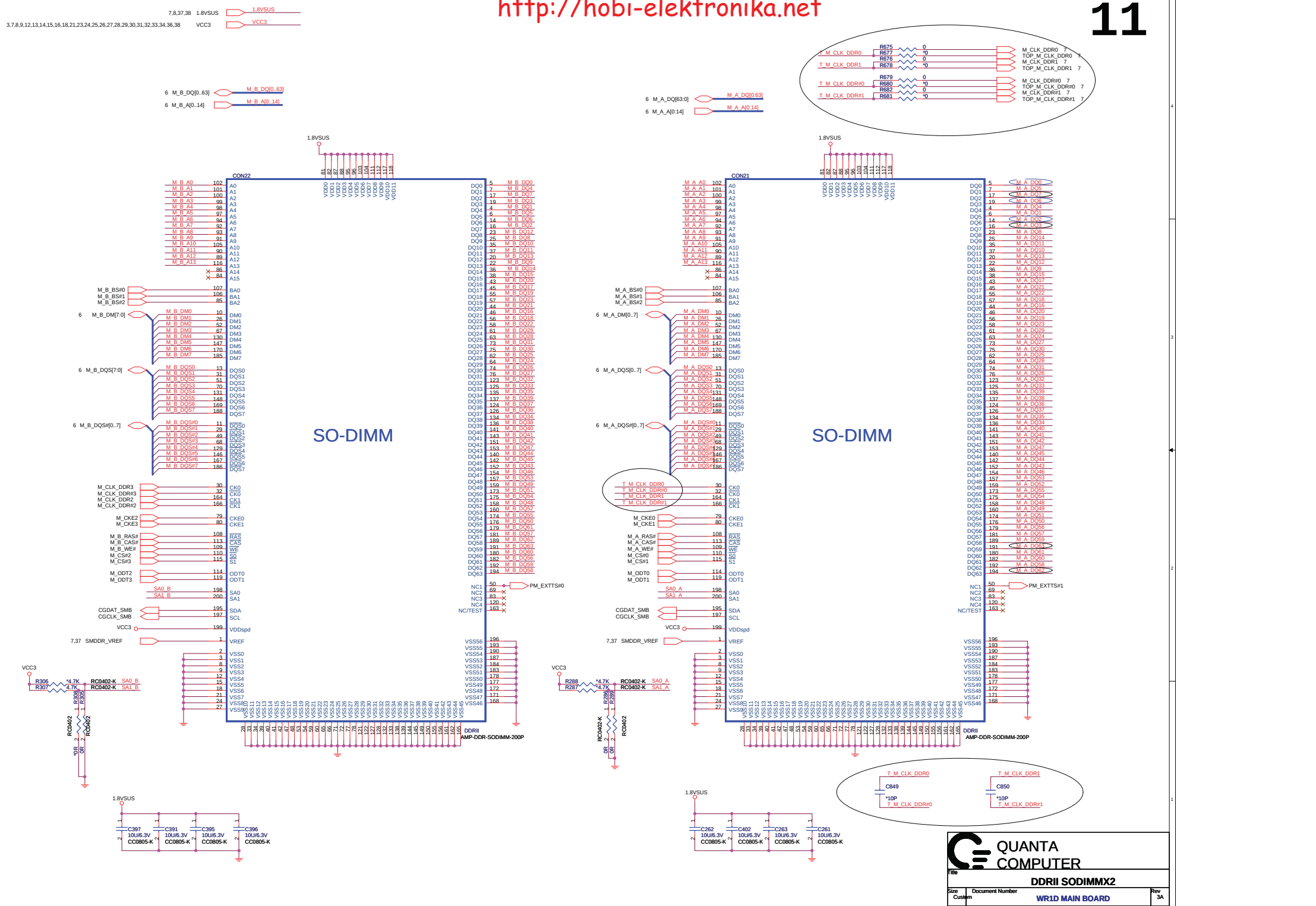


QUANTA COMPUTER

Title: Calistoga GND 6/6&DDR Terminal Resistors

Size	Document Number	Rev
C	WR1D MAIN BOARD	3A

Date: Friday, August 25, 2006 Sheet 10 of 43

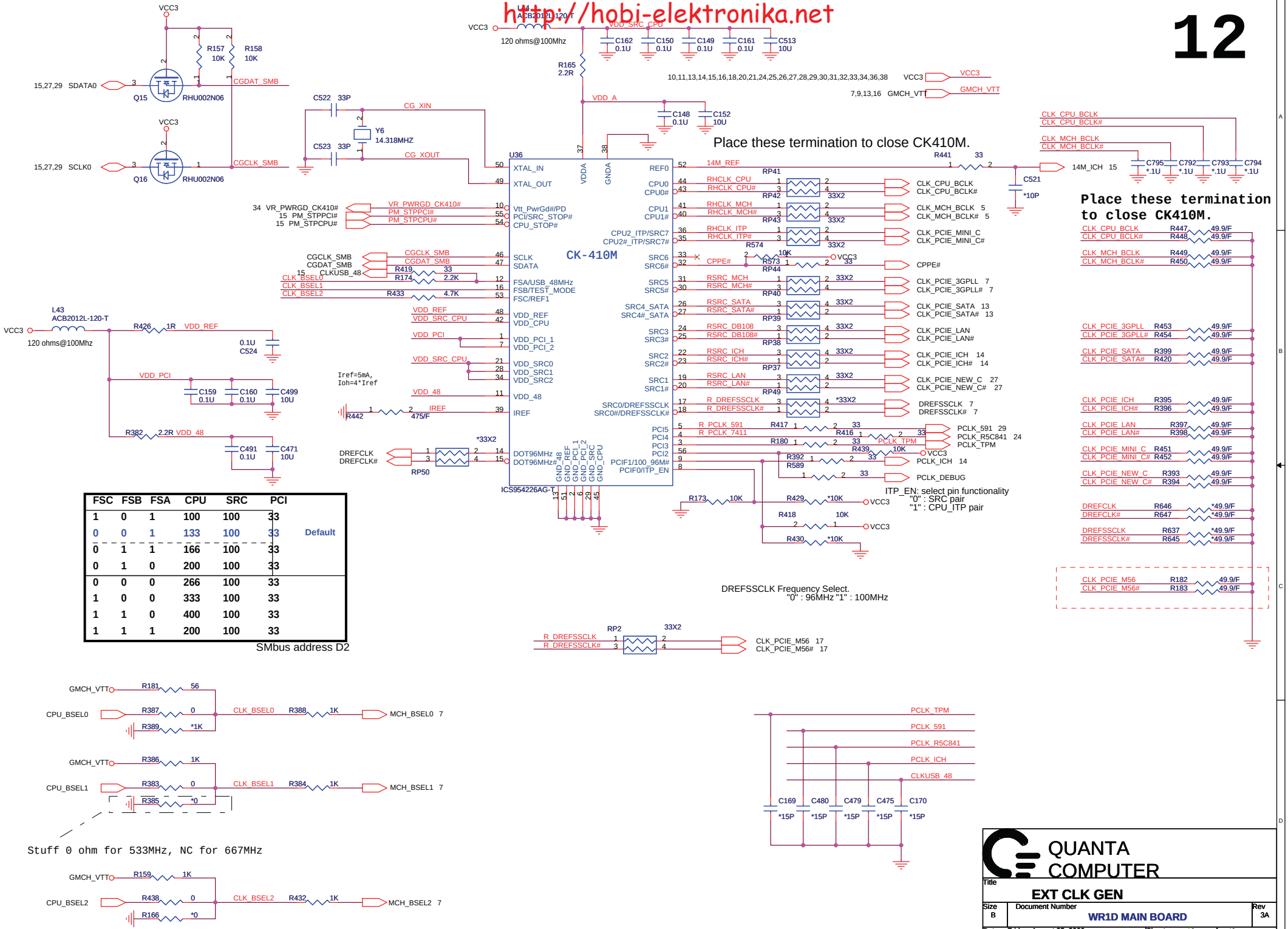


QUANTA COMPUTER

Title: DDRII SODIMMX2

Size: Custom | Document Number: WR1D MAIN BOARD | Rev: 3A

Date: Friday, August 25, 2006 | Sheet 11 of 43



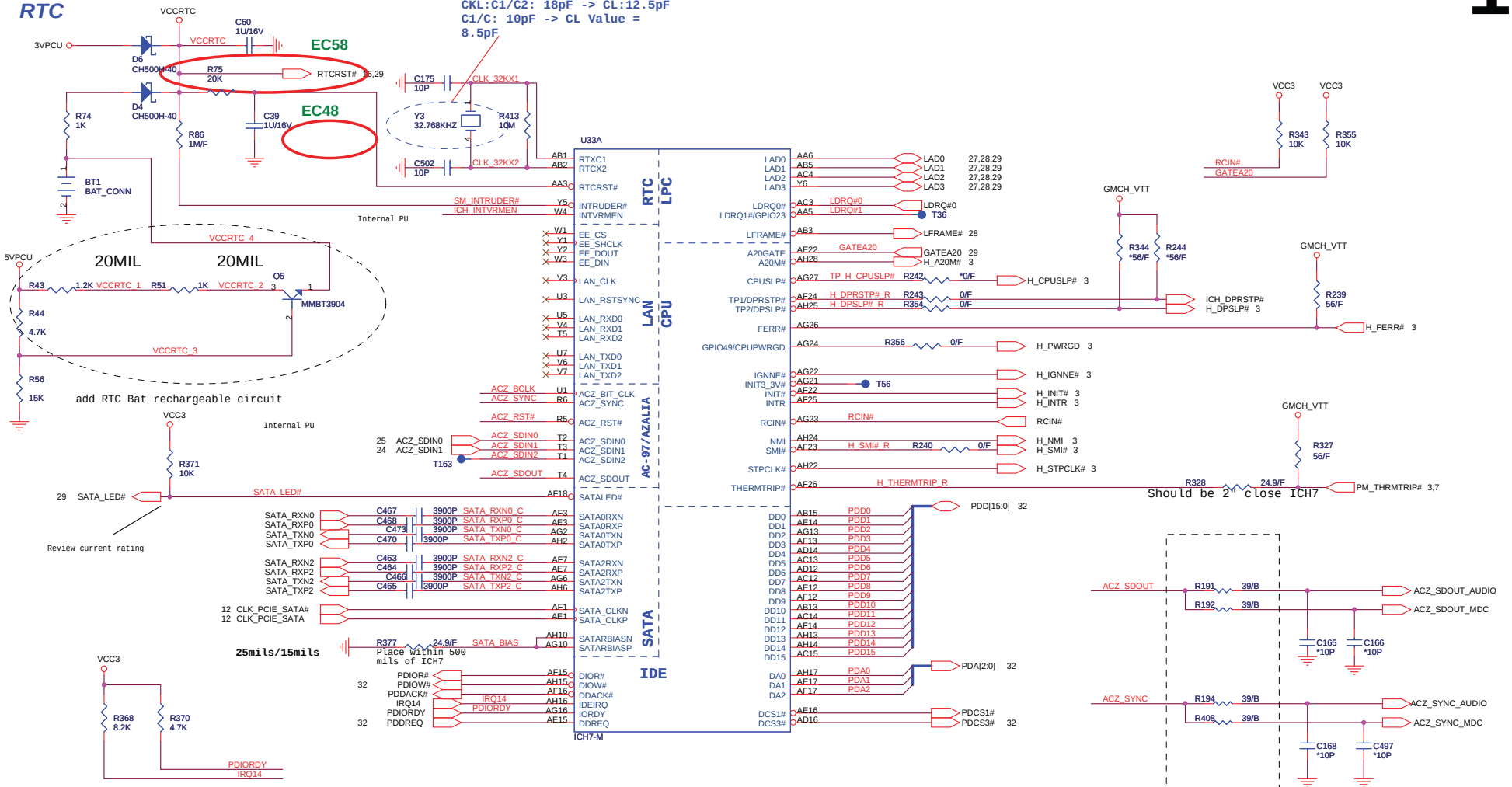
FSC	FSB	FSA	CPU	SRC	PCI	
1	0	1	100	100	33	
0	0	1	133	100	33	Default
0	1	1	166	100	33	
0	1	0	200	100	33	
0	0	0	266	100	33	
1	0	0	333	100	33	
1	1	0	400	100	33	
1	1	1	200	100	33	

Title	EXT CLK GEN
Size B	Document Number WR1D MAIN BOARD
Rev	3A
Date: Friday, August 25, 2006	Sheet 12 of 43

QUANTA COMPUTER

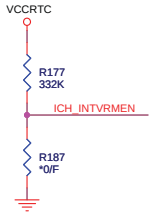
RTC

CKL:C1/C2: 18pF -> CL:12.5pF
C1/C: 10pF -> CL Value = 8.5pF



ICH7 internal VR enable strap

	INTVRMEN
Enable (default)	1
Disable	0



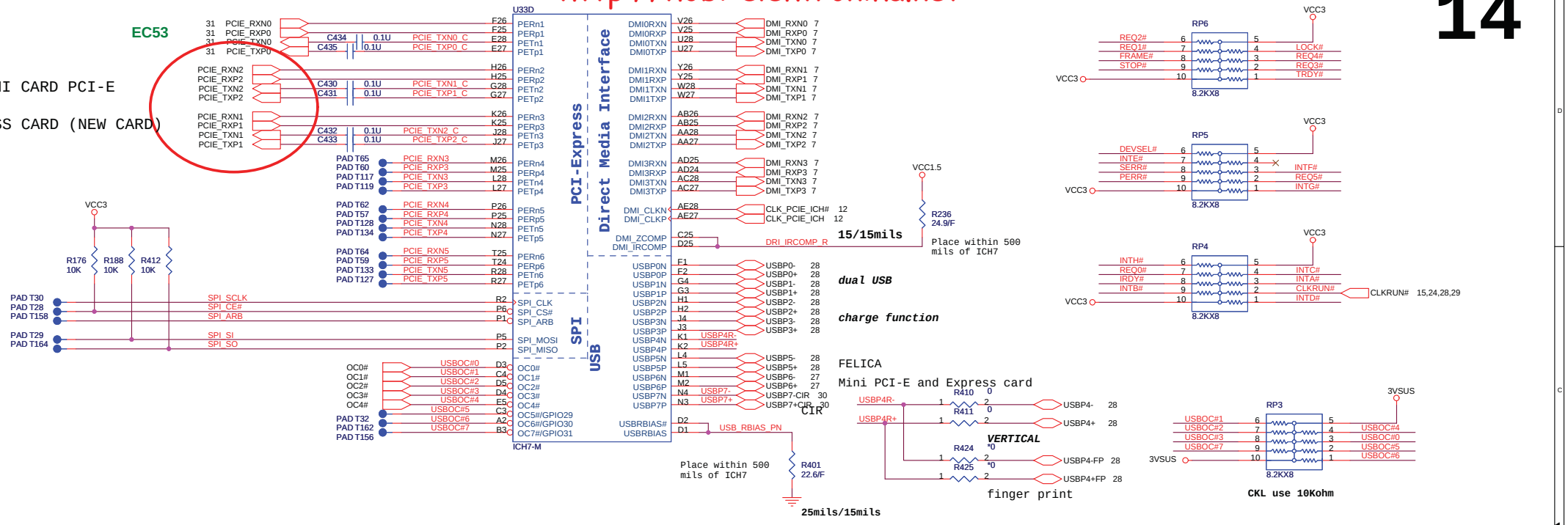
QUANTA COMPUTER

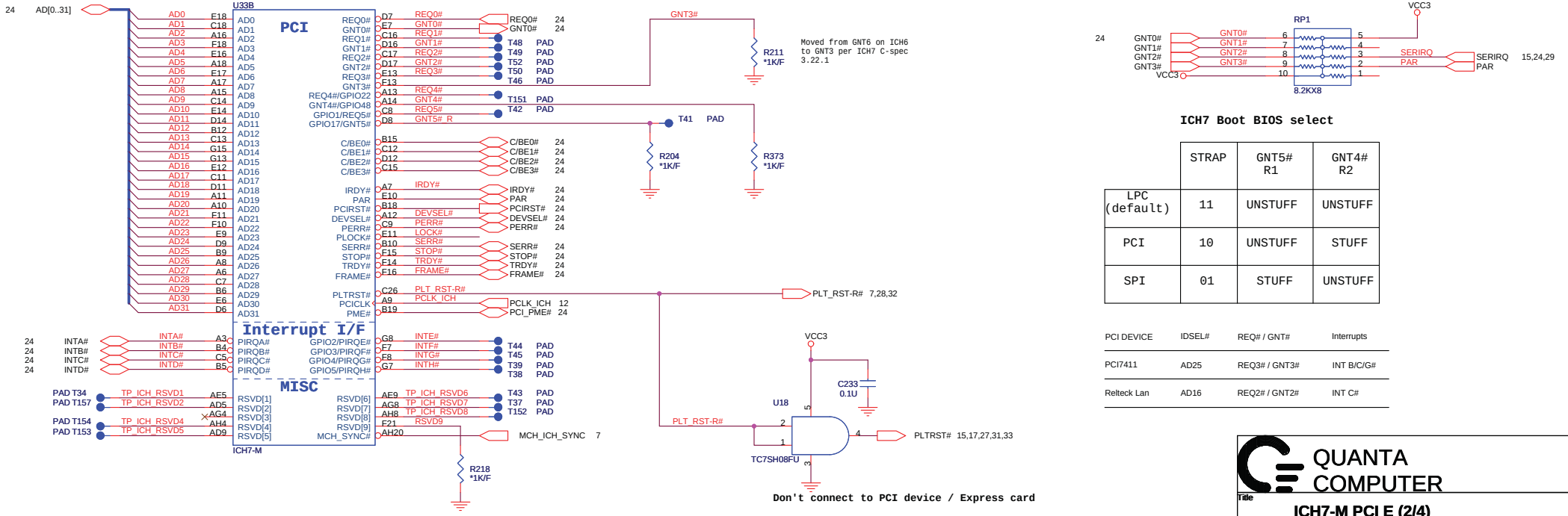
Title	ICH7-M HOST (1/4)	
Size: Custom	Document Number: WR1D MAIN BOARD	Rev: 3A
Date: Friday, August 25, 2006	Sheet 13 of 43	

EC53

MINI CARD PCI-E

EXPRESS CARD (NEW CARD)





	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCI7411	AD25	REQ3# / GNT3#	INT B/C/G#
Relteck Lan	AD16	REQ2# / GNT2#	INT C#

QUANTA COMPUTER

Title: ICH7-M PCI E (2/4)

Size: Custom | Document Number: WR1D MAIN BOARD | Rev: 2A

Date: Friday, August 25, 2006 | Sheet 14 of 43

16,27,31,38 RVCC3

R376
No stuff-->boot
Stuff-->No boot

3VPCU R226 *0/F
RVCC3 R225 0/F

SCLK0 R224 2.2K
SDATA0 R221 2.2K

RI# R332 10K
SMB_LINK_ALERT# R340 10K
SMLINK0 R342 10K
SMLINK1 R341 10K
EXTSMI# R359 10K
WAKE_SCI# R333 10K
SMB_ALERT# R352 10K

DNBSWON# R358 10K
SYS_RST# R229 10K
WAKE# R213 1K
PM_BATLOW# R357 8.2K

CLKRUN# R372 8.2K
SERIRQ R360 8.2K
SATA2GP R369 8.2K
SATA3GP R210 8.2K
RUNTIME_SCI# R R212 10K
BOARD_ID1 R228 8.2K
BOARD_ID0 R232 8.2K

to Clock Gen & DIMM

SYS_RST is suspend rail

U33C

SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
RI#
SPKR
SUS_STAT#
SYS_RST#
GPIO0/BM_BUSY#
GPIO11/SMBALERT#
GPIO18/STPPCI#
GPIO20/STPCPU#
GPIO26
GPIO27
GPIO28
GPIO32/CLKRUN#
GPIO33/AZ_DOCK_EN#
GPIO34/AZ_DOCK_RST#
WAKE#
SERIRQ
THRM#
VRMPWRGD
GPIO6
GPIO7
GPIO8

SMB
SYS GPIO
GPIO

SATA GPIO
GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA2GP
GPIO37/SATA3GP

Clocks
CLK14
CLK48
SUSCLK

Power MGT
SLP_S3#
SLP_S4#
SLP_S5#
PWROK
GPIO16/DPRSLPVR
TP0/BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
GPIO9
GPIO10
GPIO12
GPIO13
GPIO14
GPIO15
GPIO24
GPIO25
GPIO35
GPIO38
GPIO39

GPIO

ICH7-M

12,27,29 SCLK0
12,27,29 SDATA0
SMB_LINK_ALERT#
SMLINK0
SMLINK1
RI#
28 SUS_STAT#
3 XDP_DBRESET#
7 PM_BMBUSY#
SMB_ALERT#
No ASF support
12 PM_STPPCI#
12 PM_STPCPU#
27 BIOS_WP#
BIOS_REC_R
FWH_MFG_MODE_R
14,24,28,29 CLKRUN#
27,31 WAKE#
14,24,28,29 SERIRQ
VR_PWRGD_CK410
29 SCI#
KBSMI#
RUNTIME_SCI# R
EXTSMI# R

AE19 BOARD_ID1
AH18 BOARD_ID0
AH19 SATA2GP
AE19 SATA3GP
AC1 14M_ICH
B2 CLKUSB_48
C20 T54
B24 SUSB# 29
D23 SUSC# 29
E22 T55
AA4 ICH_PWROK
AC22 PM_DPRSLPVR_R
C21 PM_BATLOW#
C23 DNBSWON#
C19 PLTRST# 14,17,27,31,33
Y4 PM_RSMRST#_R
E20 SWI#
A20 DASP_ON
F19 MXM_THERM#
E19 WAKE_SCI# R
R4 T33
E22
R3
D20
AD21
AD20
AE20 FELICA_CD# 28

34 VR_PWRGD_CK410#
RSMRST# R423 10K
Q26 2N7002E
R241 100K
VR_PWRGD_CK410
VCC3

Consider change to logic IC next version

Note: External pull-up 3V

CKL :100Kohm PD

DPRSLPVR 34
RSMRST#
GBE_CLKREQ# 31

GPIO25 /Suspend rail is a HW strap , don't pull down .

Board ID	ID:0	ID0:1
ID1:0		
ID1:1		

MXM_ON#: 1 -> No MXM Module
0 -> MXM Module

EC54

SWI# R216 10K RVCC3
MXM_THERM# R365 *10K RVCC3

CLKUSB_48 R402 10/B C483 10P
14M_ICH R403 33/B C492 10P

3VSUS C789 0.1U CC0402-K
U56 NC7SZ08P5X
7,34 DELAY_VR_PWRGOOD
24 NPWROK
ICH_PWROK R660 10K

R220 10K/F R219 0/F BIOS_REC BIOS_REC_R R361 *0/F
R230 10K/F R233 0/F FWH_MFG_MODE FWH_MFG_MODE_R R227 *0/F

R223 PCLK_SMB 10K Q25 2N7002E SCLK0 12,27,29
R215 PDATA_SMB 10K Q22 2N7002E SDATA0 12,27,29

C100 .1U
U14A U14B 7WZ14
R137 22K C109 1U
RSMRST#

QUANTA COMPUTER

Title: ICH7-M GPIO (3/4)
Size: Custom
Document Number: WR1D MAIN BOARD
Rev: 3A
Date: Friday, August 25, 2006
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13,29 VCCRTC → VCCRTC

3,4,5,7,8,9,12,13,35 GMCH_VTT → GMCH_VTT

U33E

VSS[1] VSS[2] VSS[3] VSS[4] VSS[5] VSS[6] VSS[7] VSS[8] VSS[9] VSS[10] VSS[11] VSS[12] VSS[13] VSS[14] VSS[15] VSS[16] VSS[17] VSS[18] VSS[19] VSS[20] VSS[21] VSS[22] VSS[23] VSS[24] VSS[25] VSS[26] VSS[27] VSS[28] VSS[29] VSS[30] VSS[31] VSS[32] VSS[33] VSS[34] VSS[35] VSS[36] VSS[37] VSS[38] VSS[39] VSS[40] VSS[41] VSS[42] VSS[43] VSS[44] VSS[45] VSS[46] VSS[47] VSS[48] VSS[49] VSS[50] VSS[51] VSS[52] VSS[53] VSS[54] VSS[55] VSS[56] VSS[57] VSS[58] VSS[59] VSS[60] VSS[61] VSS[62] VSS[63] VSS[64] VSS[65] VSS[66] VSS[67] VSS[68] VSS[69] VSS[70] VSS[71] VSS[72] VSS[73] VSS[74] VSS[75] VSS[76] VSS[77] VSS[78] VSS[79] VSS[80] VSS[81] VSS[82] VSS[83] VSS[84] VSS[85] VSS[86] VSS[87] VSS[88] VSS[89] VSS[90] VSS[91] VSS[92] VSS[93] VSS[94] VSS[95] VSS[96] VSS[97] VSS[98] VSS[99] VSS[100] VSS[101] VSS[102] VSS[103] VSS[104] VSS[105] VSS[106] VSS[107] VSS[108] VSS[109] VSS[110] VSS[111] VSS[112] VSS[113] VSS[114] VSS[115] VSS[116] VSS[117] VSS[118] VSS[119] VSS[120] VSS[121] VSS[122] VSS[123] VSS[124] VSS[125] VSS[126] VSS[127] VSS[128] VSS[129] VSS[130] VSS[131] VSS[132] VSS[133] VSS[134] VSS[135] VSS[136] VSS[137] VSS[138] VSS[139] VSS[140] VSS[141] VSS[142] VSS[143] VSS[144] VSS[145] VSS[146] VSS[147] VSS[148] VSS[149] VSS[150] VSS[151] VSS[152] VSS[153] VSS[154] VSS[155] VSS[156] VSS[157] VSS[158] VSS[159] VSS[160] VSS[161] VSS[162] VSS[163] VSS[164] VSS[165] VSS[166] VSS[167] VSS[168] VSS[169] VSS[170] VSS[171] VSS[172] VSS[173] VSS[174] VSS[175] VSS[176] VSS[177] VSS[178] VSS[179] VSS[180] VSS[181] VSS[182] VSS[183] VSS[184] VSS[185] VSS[186] VSS[187] VSS[188] VSS[189] VSS[190] VSS[191] VSS[192] VSS[193] VSS[194]

ICH7-M

VCC5 VCC3 R203 100/F D24 PDZ5.6B 15/15mils V5REF(1) C197 1U C196 0.1U

5VPCU 3VPCU R184 10 D15 PDZ5.6B 15/15mils V5REF_SUS C172 1U C184 0.1U

VCC1.5 L24 BK1608HS800-T Oreginal N1608ZE101T01 "CX8HS800005" +1.5V_PCIE_ICH C426 220U C228 0.1U C226 0.1U C225 0.1U

U33F

V5REF[1] V5REF[2] V5REF_Sus

Vcc1_5_B[1] Vcc1_5_B[2] Vcc1_5_B[3] Vcc1_5_B[4] Vcc1_5_B[5] Vcc1_5_B[6] Vcc1_5_B[7] Vcc1_5_B[8] Vcc1_5_B[9] Vcc1_5_B[10] Vcc1_5_B[11] Vcc1_5_B[12] Vcc1_5_B[13] Vcc1_5_B[14] Vcc1_5_B[15] Vcc1_5_B[16] Vcc1_5_B[17] Vcc1_5_B[18] Vcc1_5_B[19] Vcc1_5_B[20] Vcc1_5_B[21] Vcc1_5_B[22] Vcc1_5_B[23] Vcc1_5_B[24] Vcc1_5_B[25] Vcc1_5_B[26] Vcc1_5_B[27] Vcc1_5_B[28] Vcc1_5_B[29] Vcc1_5_B[30] Vcc1_5_B[31] Vcc1_5_B[32] Vcc1_5_B[33] Vcc1_5_B[34] Vcc1_5_B[35] Vcc1_5_B[36] Vcc1_5_B[37] Vcc1_5_B[38] Vcc1_5_B[39] Vcc1_5_B[40] Vcc1_5_B[41] Vcc1_5_B[42] Vcc1_5_B[43] Vcc1_5_B[44] Vcc1_5_B[45] Vcc1_5_B[46] Vcc1_5_B[47] Vcc1_5_B[48] Vcc1_5_B[49] Vcc1_5_B[50] Vcc1_5_B[51] Vcc1_5_B[52] Vcc1_5_B[53]

Vcc3_3[1] VccDMIPLL VccSATAPLL Vcc3_3[2] VccUSBPLL

Vcc1_5_A[1] Vcc1_5_A[2] Vcc1_5_A[3] Vcc1_5_A[4] Vcc1_5_A[5] Vcc1_5_A[6] Vcc1_5_A[7] Vcc1_5_A[8] Vcc1_5_A[9] Vcc1_5_A[10] Vcc1_5_A[11] Vcc1_5_A[12] Vcc1_5_A[13] Vcc1_5_A[14] Vcc1_5_A[15] Vcc1_5_A[16] Vcc1_5_A[17] Vcc1_5_A[18] Vcc1_5_A[19] Vcc1_5_A[20] Vcc1_5_A[21] Vcc1_5_A[22] Vcc1_5_A[23] Vcc1_5_A[24] Vcc1_5_A[25] Vcc1_5_A[26] Vcc1_5_A[27] Vcc1_5_A[28] Vcc1_5_A[29] Vcc1_5_A[30]

VccSus3_3[19] VccSus1_05/VccLAN1_05[1] VccSus1_05/VccLAN1_05[2]

VCC_PAUX VccSus3_3/VccLAN3_3[1] VccSus3_3/VccLAN3_3[2] VccSus3_3/VccLAN3_3[3] VccSus3_3/VccLAN3_3[4] Vcc3_3/VccHDA VccSus3_3/VccSusHDA

V_CPU_IO[1] V_CPU_IO[2] V_CPU_IO[3]

Vcc3_3[3] Vcc3_3[4] Vcc3_3[5] Vcc3_3[6] Vcc3_3[7] Vcc3_3[8] Vcc3_3[9] Vcc3_3[10] Vcc3_3[11] Vcc3_3[12] Vcc3_3[13] Vcc3_3[14] Vcc3_3[15] Vcc3_3[16] Vcc3_3[17] Vcc3_3[18] Vcc3_3[19] Vcc3_3[20] Vcc3_3[21]

VccRTC

VccSus3_3[1] VccSus3_3[2] VccSus3_3[3] VccSus3_3[4] VccSus3_3[5] VccSus3_3[6] VccSus3_3[7] VccSus3_3[8] VccSus3_3[9] VccSus3_3[10] VccSus3_3[11] VccSus3_3[12] VccSus3_3[13] VccSus3_3[14] VccSus3_3[15] VccSus3_3[16] VccSus3_3[17] VccSus3_3[18]

Vcc1_05[1] Vcc1_05[2] Vcc1_05[3] Vcc1_05[4] Vcc1_05[5] Vcc1_05[6] Vcc1_05[7] Vcc1_05[8] Vcc1_05[9] Vcc1_05[10] Vcc1_05[11] Vcc1_05[12] Vcc1_05[13] Vcc1_05[14] Vcc1_05[15] Vcc1_05[16] Vcc1_05[17] Vcc1_05[18] Vcc1_05[19] Vcc1_05[20]

ICH7-M

GMCH_VTT Oreginal 270U P/N "CH7270LM885"

C203 0.1U C222 0.1U C429 330U

C216 0.1U C202 0.1U C209 0.1U C199 0.1U

C217 0.1U C200 0.1U C214 0.1U C205 0.1U C213 0.1U

VCC3 C231 0.1U RVCC3 C204 0.1U C215 0.1U

GMCH_VTT C219 0.1U C208 0.1U C445 4.7U/10V/1206 VCC3 C223 0.1U

VCC3 C212 0.1U C201 0.1U C207 0.1U C220 0.1U

VCCRTC C187 0.1U C194 0.1U RVCC3 C192 0.1U C221 0.1U

RVCC3 C182 0.1U C227 0.1U

VCC1.5 C186 0.1U C218 0.1U C191 0.1U C188 0.1U C180 0.1U

C211 0.1U

30mils

L37 1uH GPLL_R_L C427 .01U/50V/0603/X7R C428 10U/X6S C185 1U

C195 0.1U C198 0.1U

30mils

C176 1U

200mils

RVCC3 R185 0/F C173 0.1U

3VS5_ICH_SUS3 C189 0.1U

PAD T159 TPVCCSUSLAN1 PAD T40 TPVCCSUSLAN2

TP_ICHVCCSUS1 T35 PAD TP_ICHVCCSUS2 T132 PAD TP_ICHVCCSUS3 T53 PAD

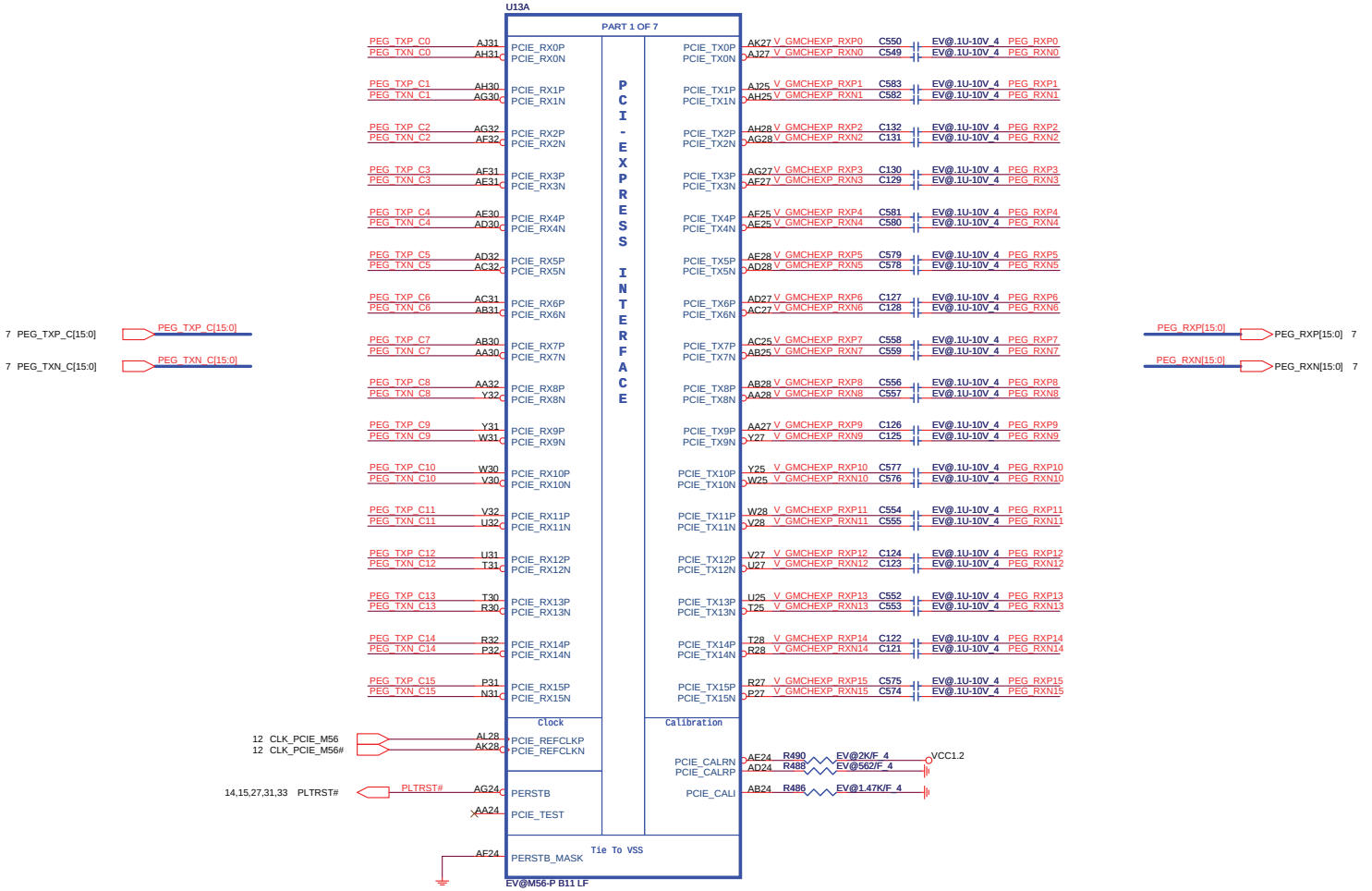
QUANTA COMPUTER

Title: ICH7-M POWER (4/4)

Size: Custom | Document Number: WR1D MAIN BOARD | Rev: 3A

Date: Friday, August 25, 2006 | Sheet 16 of 43

NOTE: some of the PCIE testpoints will be available trought via on traces.

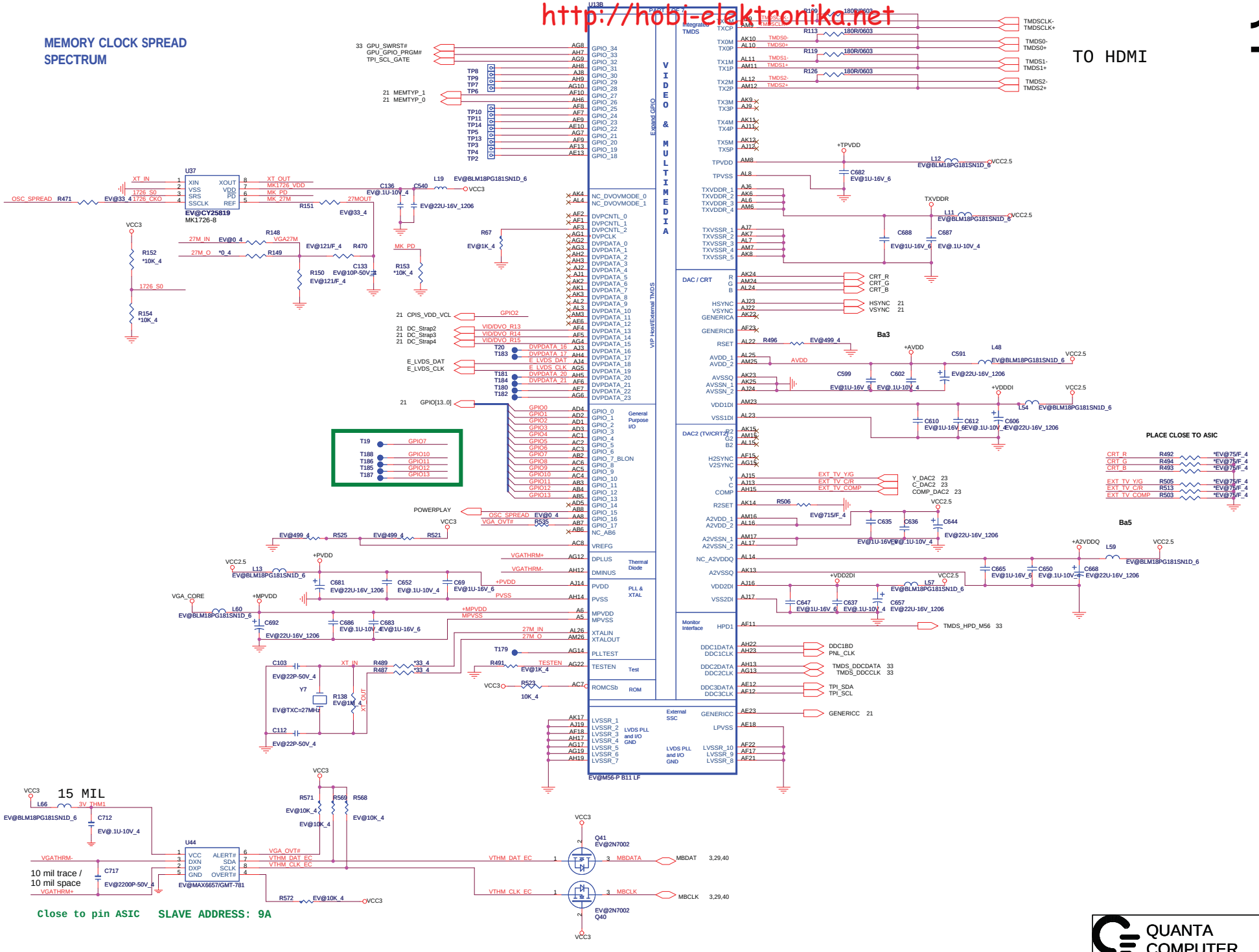


QUANTA COMPUTER

Title	VGA ATi M54P_PCIE_Interface	
Size: Custom	Document Number: WR1D MAIN BOARD	Rev: 3A
Date: Friday, August 25, 2006	Sheet 17 of 43	

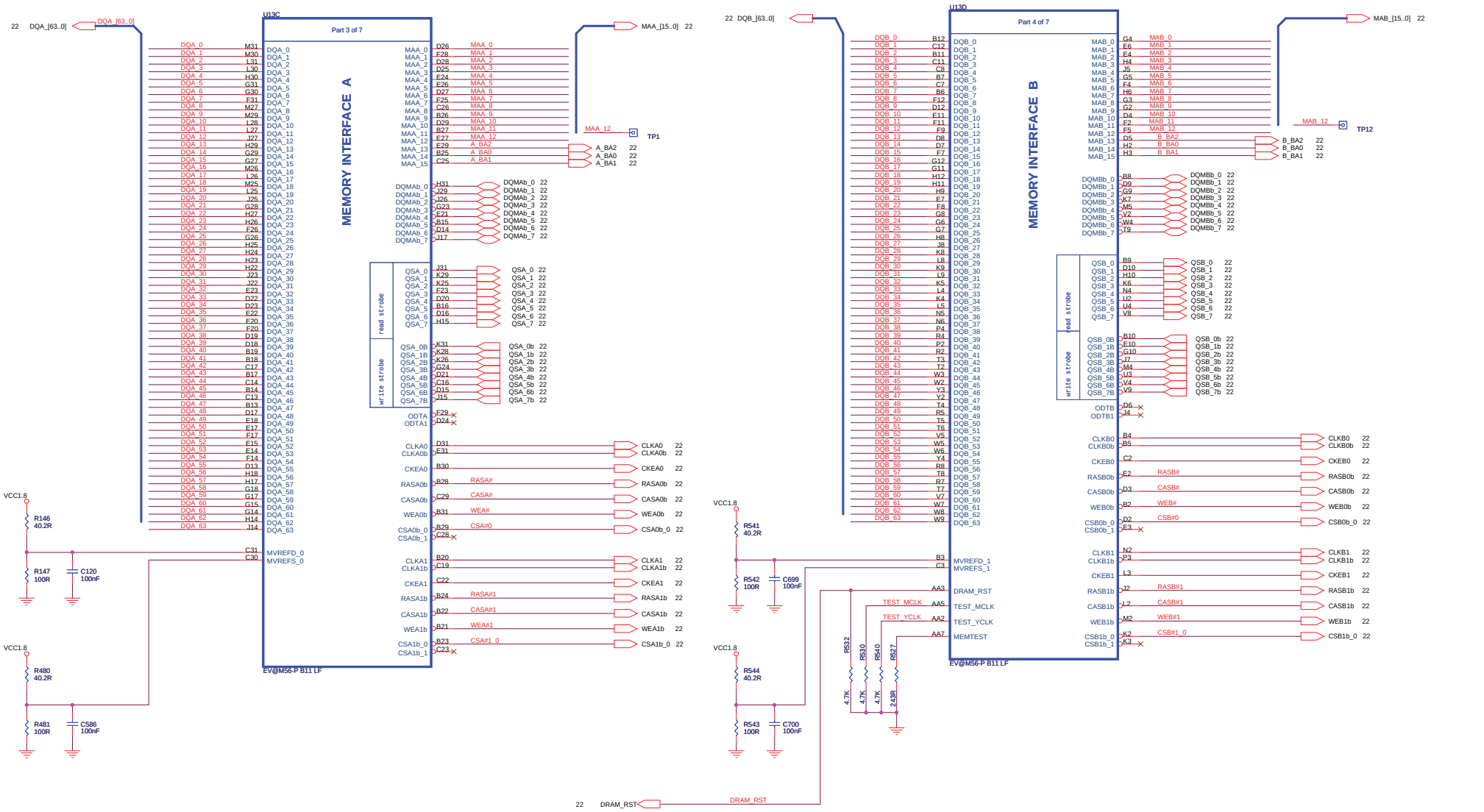
MEMORY CLOCK SPREAD SPECTRUM

TO HDMI

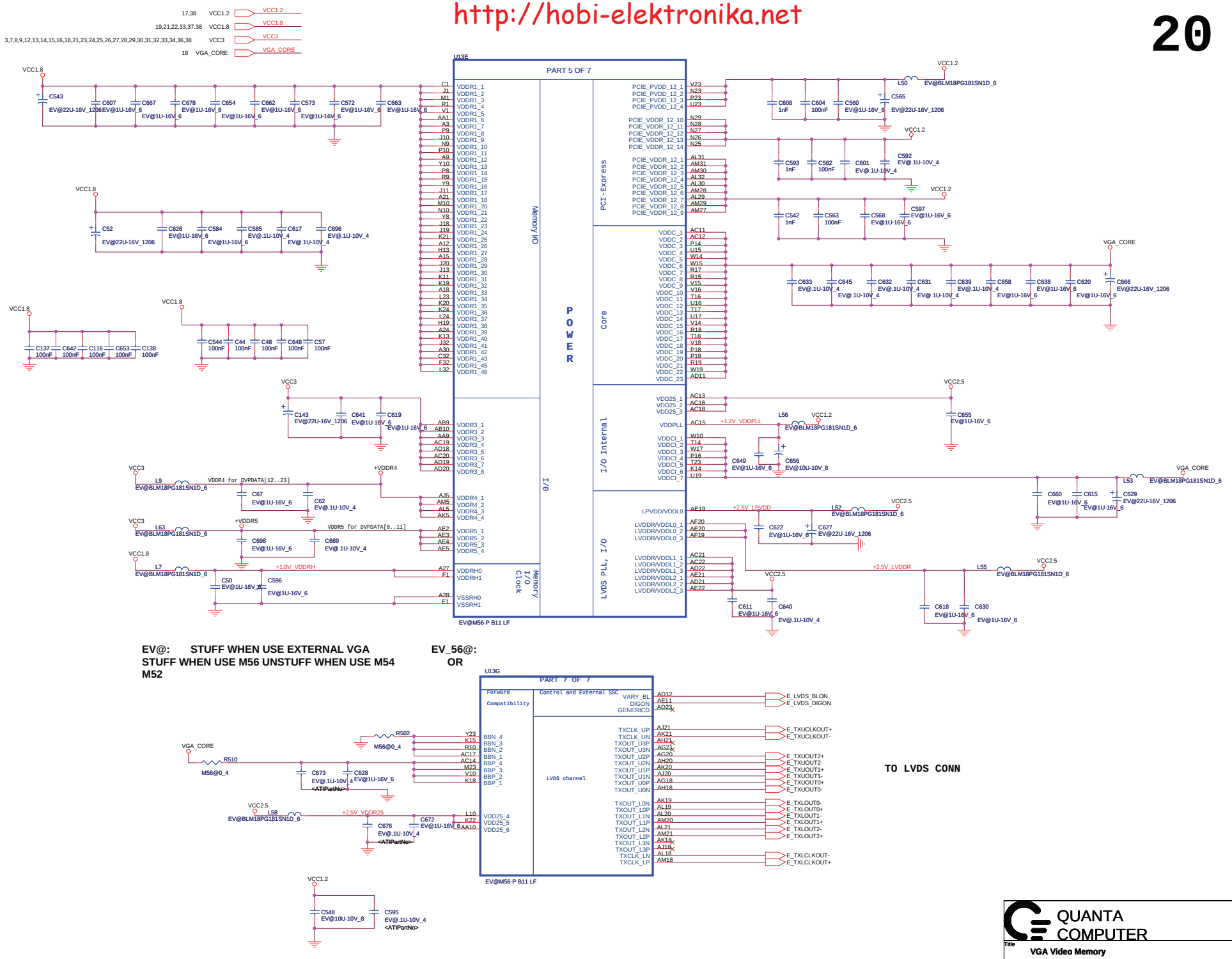


Title	VGA(M56P_Main)
Size	C
Document Number	WR1D MAIN BOARD
Rev	3A
Date:	Friday, August 25, 2006
Sheet	18 of 43

QUANTA COMPUTER

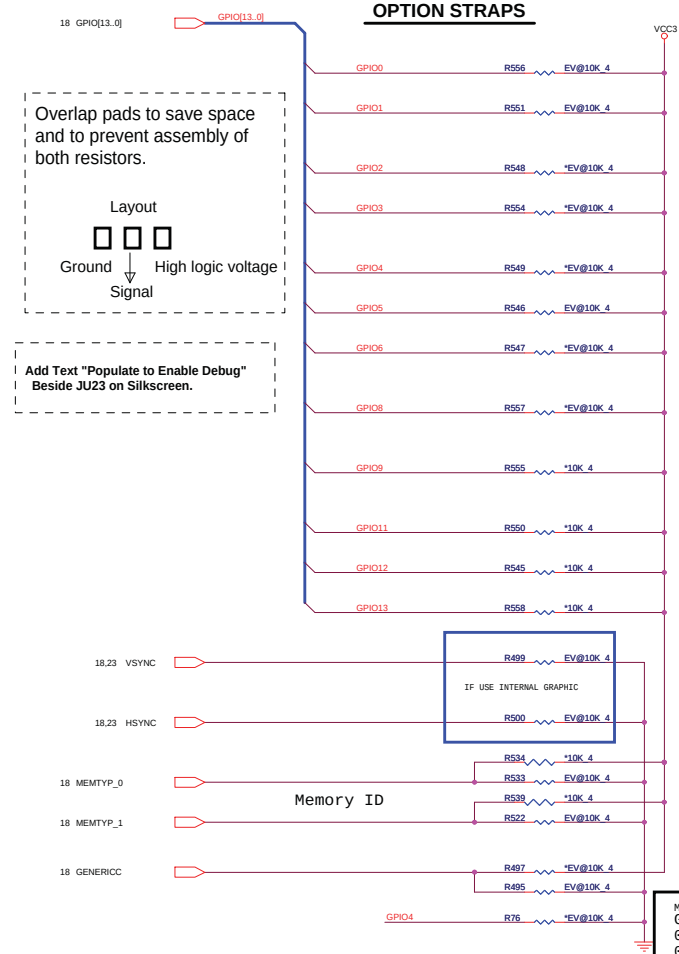


Title	VGA M56P Memory A_B		
Size C	Document Number WR1D MAIN BOARD		Rev 3A
Date: Friday, August 25, 2006		Sheet 19 of 43	



QUANTA COMPUTER		
Title	VGA Video Memory	
Size C	Document Number WR1D MAIN BOARD	Rev 3A
Date: Friday, August 25, 2006	Sheet 20 of 43	

OPTION STRAPS



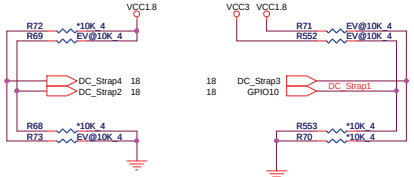
Overlap pads to save space and to prevent assembly of both resistors.

Layout

Ground ↓ High logic voltage

Signal

Add Text "Populate to Enable Debug" Beside JU23 on Silkscreen.



Memory Aperture Size Select
When no ROM is attached, GPIO[9] is set to 0.
GPIO[13:12] is used to select the memory aperture size.
GPIO[13:12] = 00: 128M memory aperture, same as ROM strap 00
GPIO[13:12] = 01: 256M memory aperture, same as ROM strap 01
GPIO[13:12] = 10: 64M memory aperture, same as ROM strap 10
GPIO[13:12] = 11: reserved, same as ROM strap 11

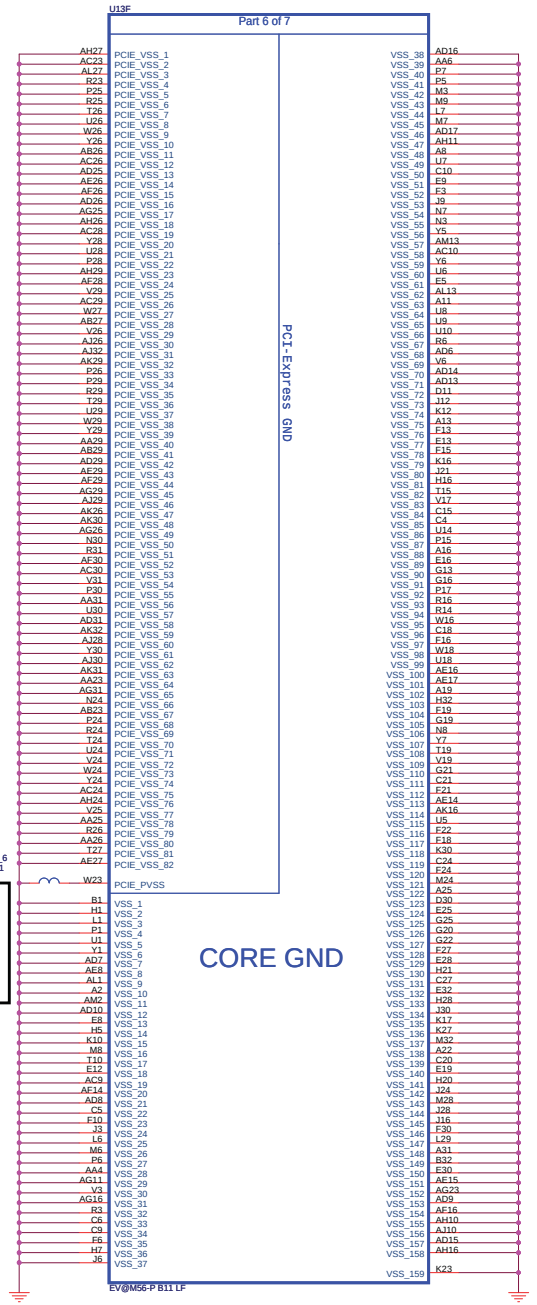
M56-P Strap

STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing 1.full Tx output swing	
TX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1.Tx de-emphasis enabled	
	GPIO(3:2)	RSVD	
DEBUG_ACCESS	GPIO4	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible	0
	GPIO5	RSVD	
	GPIO6	RSVD	
Force_Compliance	GPIO8	Force chip to get to compliance state quickly for Tester purposes	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDis. If rom attached identifies ROM type 000x - No ROM, MEM_AP_SIZE=00 001x - No ROM,MEM_AP_SIZE=01 010x - No Rom, MEM_AP_SIZE=10 011x - No ROM,MEM_AP_SIZE=11 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM **1100 - Serial M25P05 ROM (ST), chip IDis from ROM** 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port devices present. 1-No slave VIP port devices reporting presence during reset	No default
	H2SYNC, V2SYNC, GENERICC	RSVD	
	VSYNC	RSVD	
	HSYNC	RSVD	
	PCIE_TEST	RSVD	

MEMTYP_1	MEMTYP_0	Vendor	Part No	Package organized	Memory Size	
GPIO27	GPIO26					
0	0	Samsung	K4J52324QC-BC14	512M(16Mx32) GDDR3	256MB(dual channel)	R522, R533
0	1	Samsung	K4J55323QG-BC20	256M(8Mx32) GDDR3	128MB(Dual channel)	R522, R534
1	0	Infineon	HYB18H512321AFL20	512M(16Mx32) GDDR3	256MB(dual channel)	R539, R533
1	1	Infineon	HYB18H256321AFL20	256M(8Mx32) GDDR3	128MB(Dual channel)	R539, R534

Board Straps REV. 0.3

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYPE(1:0)	GPIO27,26	Memory Type select 00 Samsung 256MB(dual channel) 01 Samsung 128MB(dual channel) 10 Infineon 256MB(dual channel) 11 Infineon 128MB(dual channel)	00
DC_Strap1	GPIO(10)	Internal TMDS Enabled 0 - Disabled **1 - Enabled**	1
DC_Strap2	LCDDATA(13)	Video Capture Enabled **0 - Disabled** 1 - Not detected	0
DC_Strap3	LCDDATA(14)	HDTV out detect **0 - Detected** 1 - Enabled	1
DC_Strap4, DEMUX_SEL	LCDDATA(15,19)	Video capture enable 00 - DAC2 Off **01 - DAC2 On as CRT** 10 - DAC2 On as TVOUT 11 - DAC2 On as TVOUT and CRT	01
PAL/NTSC	LCDDATA(18)	TVO Standard Default (Resistor pull-up and switch short to GND) **0 - PAL (on board resistor pull-down and switch closed)** **1 -NTSC (on board resistor pull-up)**	1

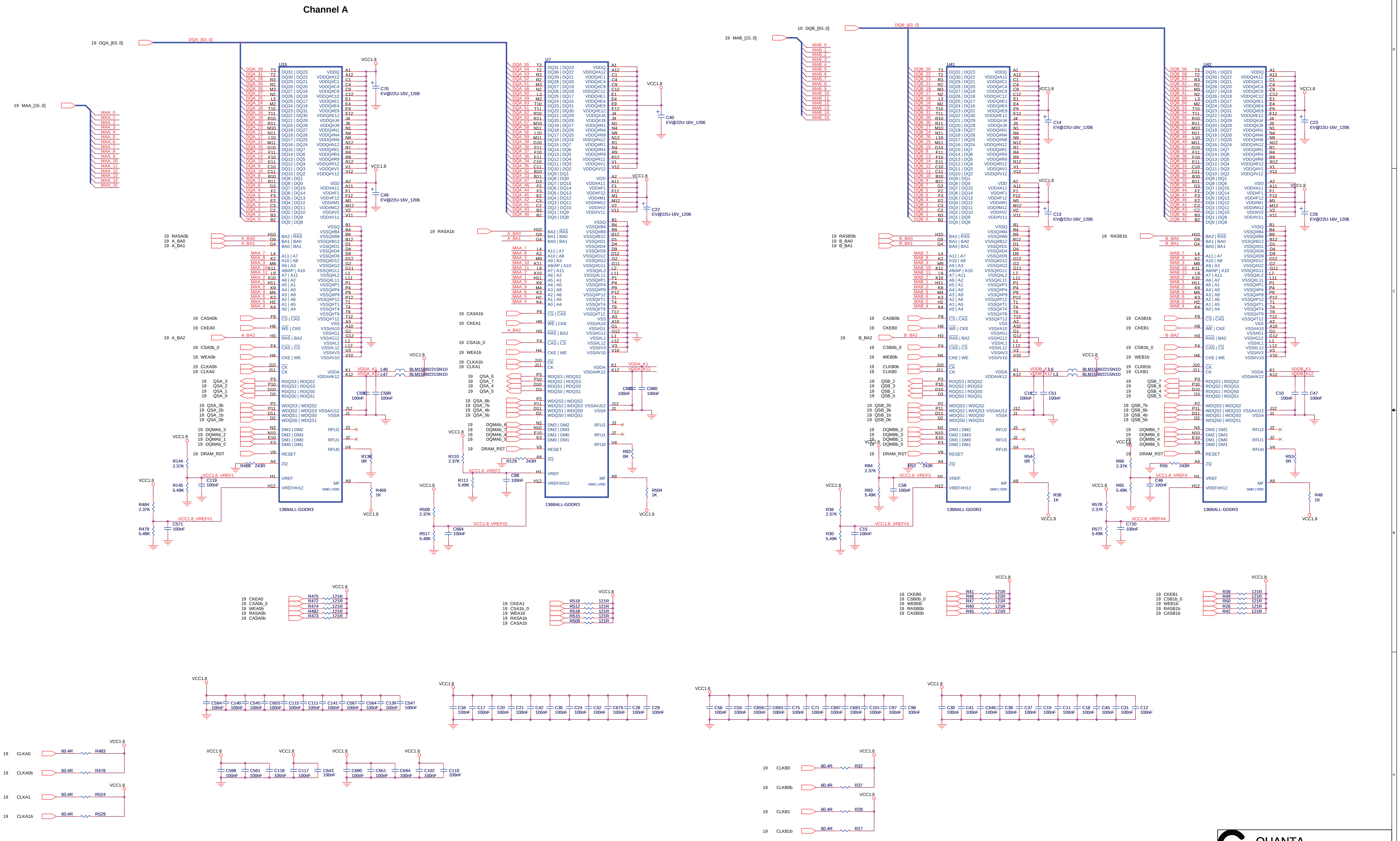


Title: VGA P_Core_GND

Size: Custom | Document Number: WR1D MAIN BOARD | Rev: 3A

Date: Friday, August 25, 2006 | Sheet 21 of 43

256 Mbit GDDRIII Channels A and B Rank 1



QUANTA COMPUTER

Title: VGA Video Memory(GDDRIII_A_B_Rank0)

Size: Custom | Document Number: WR1D MAIN BOARD | Rev: 3A

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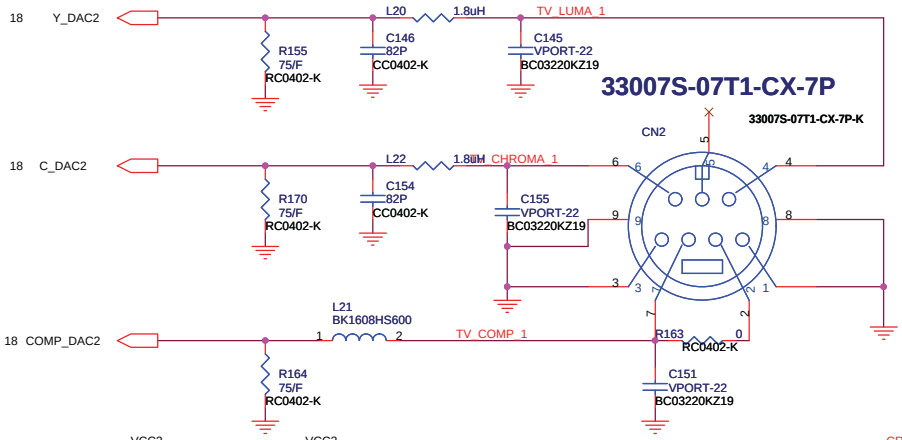
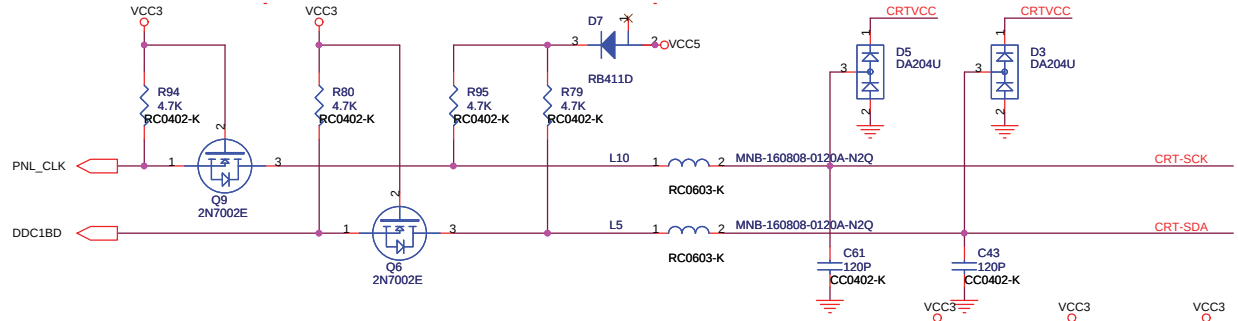
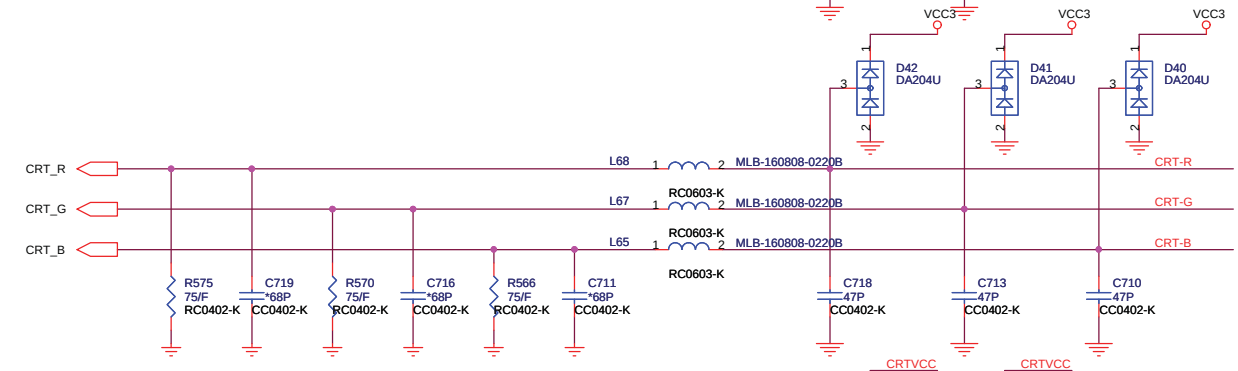
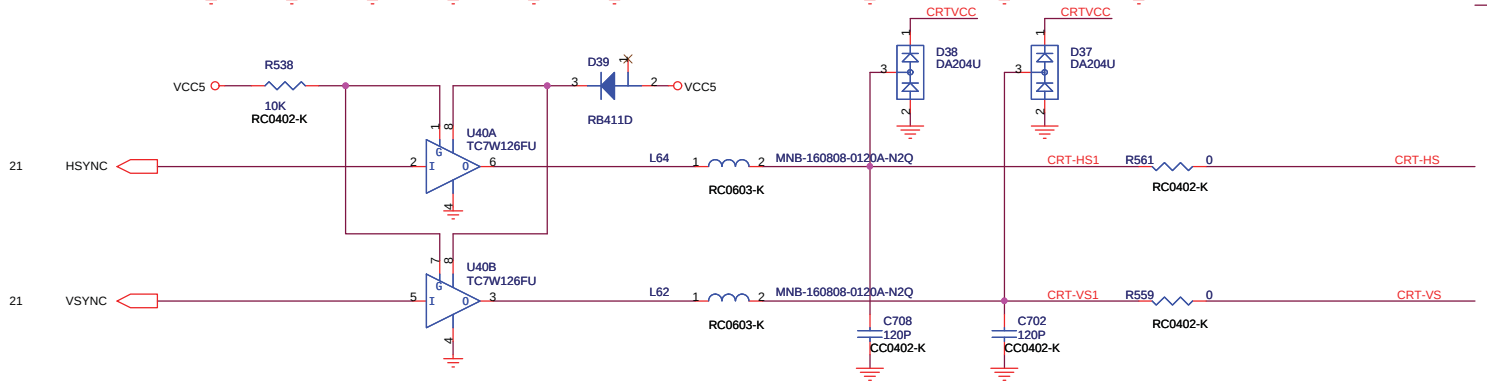
S-VIDEO CONNECTOR

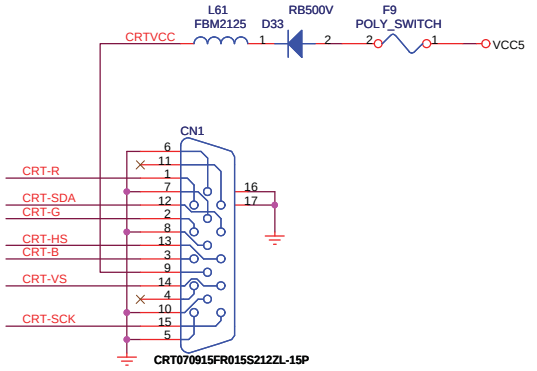








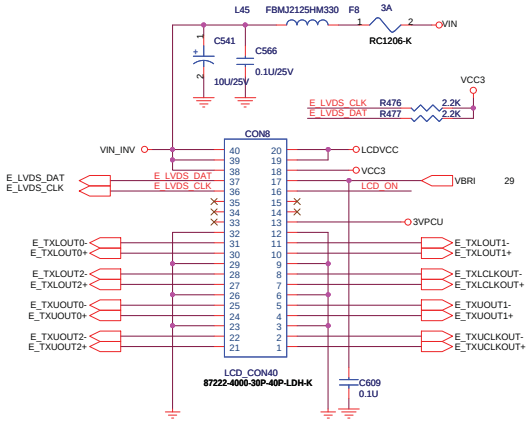
CRT CONNECTOR

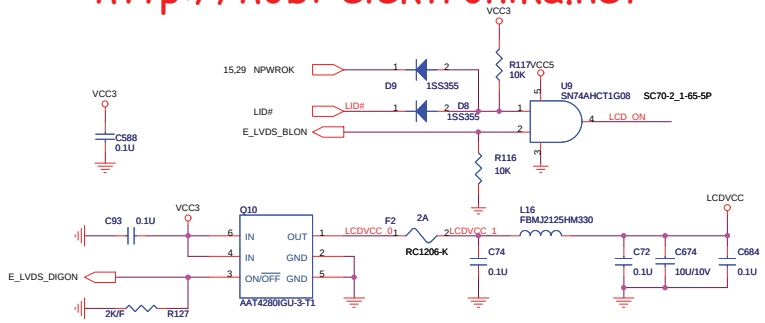


VCC5	VCC5	16,24,25,26,28,29,30,31,32,33,38
VCC3	VCC3	10,11,13,14,15,16,18,20,21,24,25,26,27,28,29,30,31,32,33,34,36,38

QUANTA COMPUTER

Title	CRT/TV OUT PORT	
Size B	Document Number WR1D MAIN BOARD	Rev 3A
Date: Friday, August 25, 2006	Sheet 23 of 43	





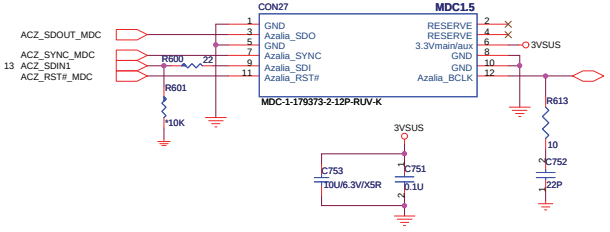
PANEL VCC CONTROL

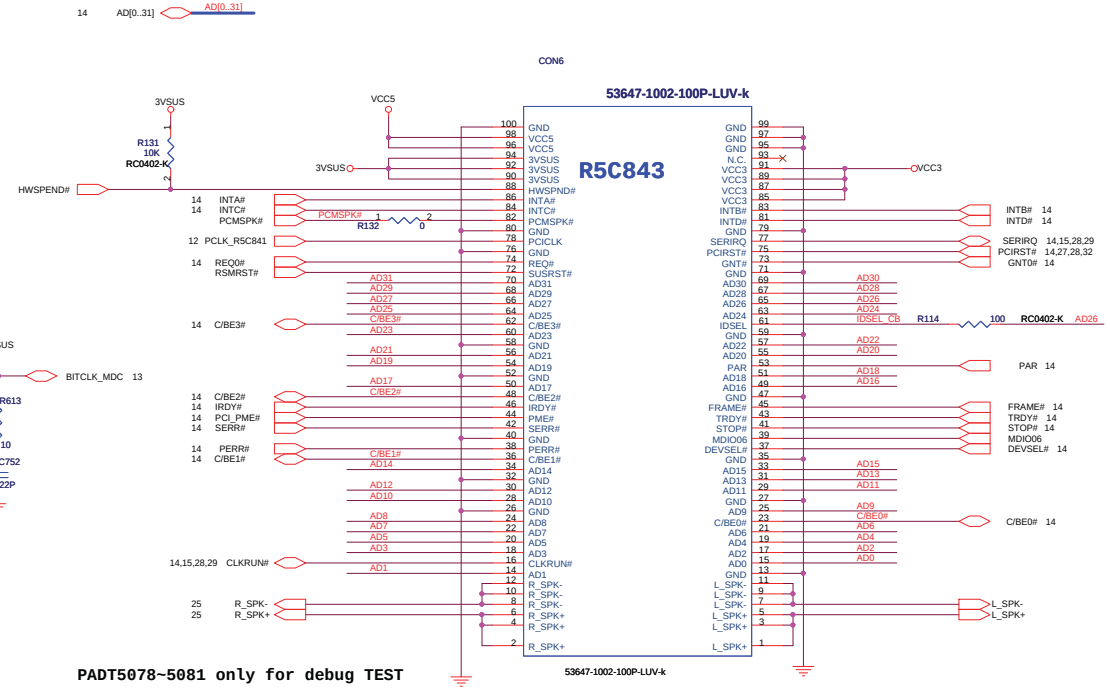
CARD READ
IDSEL:AD26
INTA,B,C
REQ0
PCICLK2

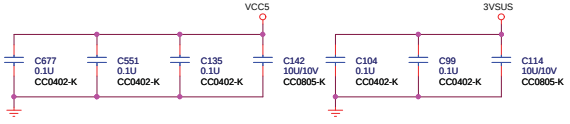
MINIPCI
IDSEL:AD20
INTA,B
REQ2
PCICLK0

TV
IDSEL:AD28
INTC,D
REQ3
PCICLK6

HD_MDC





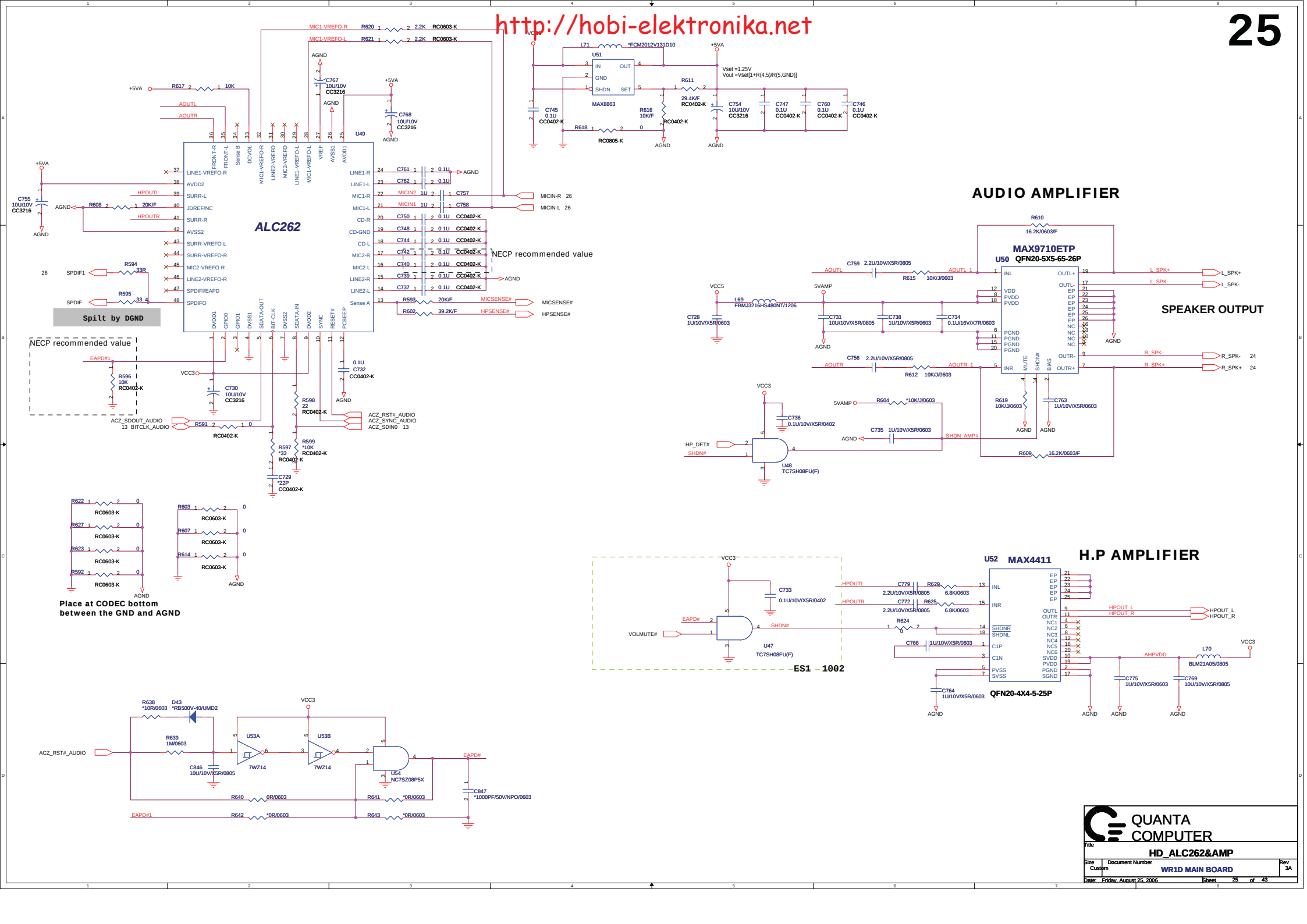


QUANTA COMPUTER

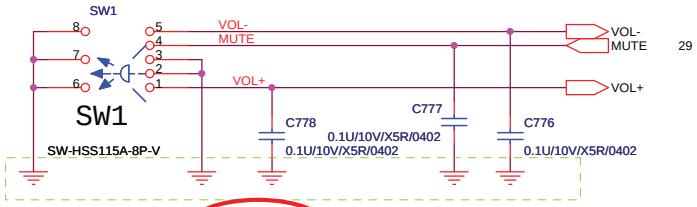
Title: Daughter board CONN

Size: C | Document Number: WR1D MAIN BOARD | Rev: 3A

Date: Friday, August 25, 2006 | Sheet 24 of 43

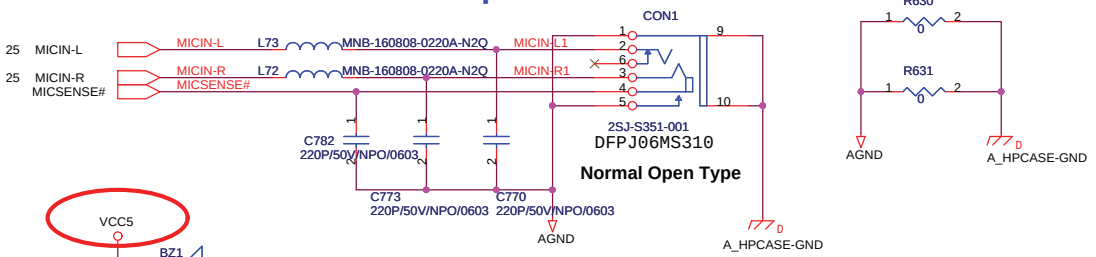


Multi-SW

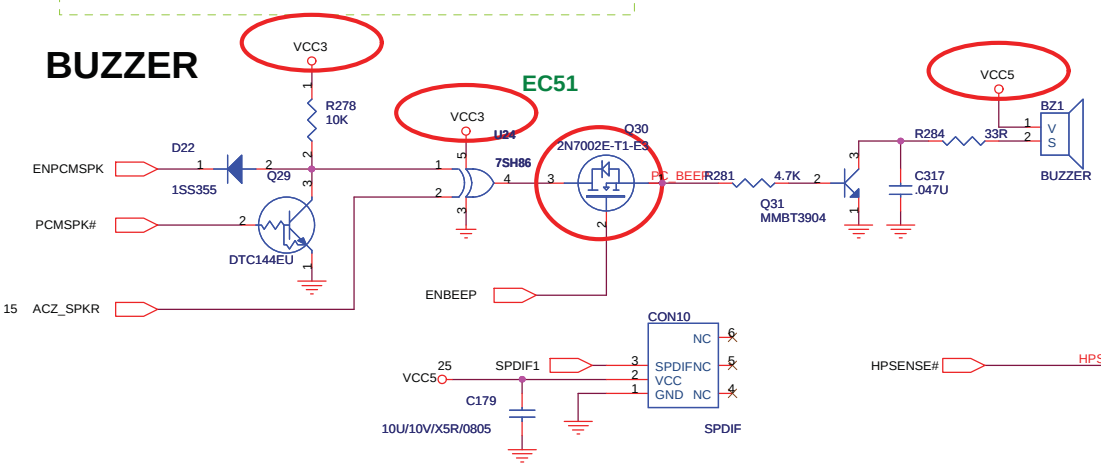


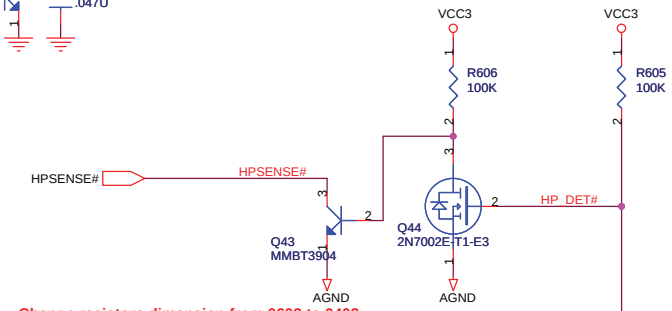
MIC-IN

Max. 100mVrms input for Mic-IN



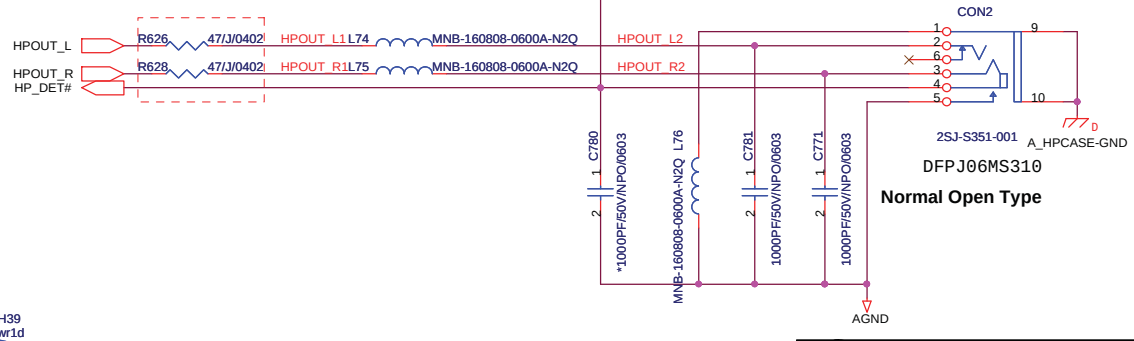
BUZZER

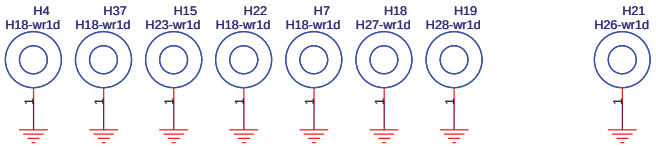




Change resistors dimension from 0603 to 0402
to prevent PCB bending cause solder and components
crack issue!

Headphone-OUT





QUANTA COMPUTER

Title	BUZZER & AUDIO/BOARD	
Size: Custom	Document Number: WR1D MAIN BOARD	Rev: 3A
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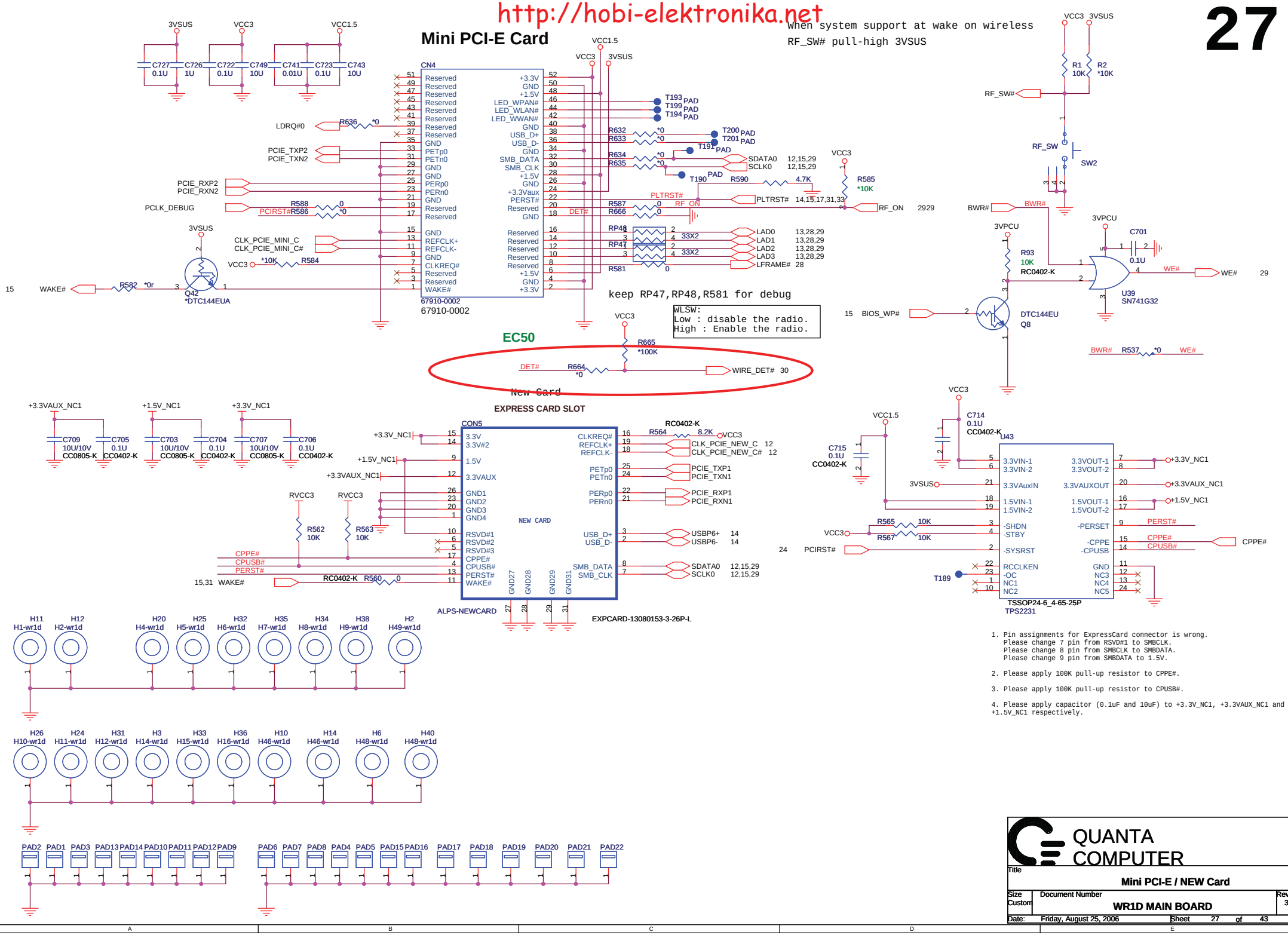
Mini PCI-E Card

when system support at wake on wireless
RF_SW# pull-high 3VSUS



Title	Mini PCI-E / NEW Card		
Size: Custom	Document Number: WR1D MAIN BOARD		Rev: 3A
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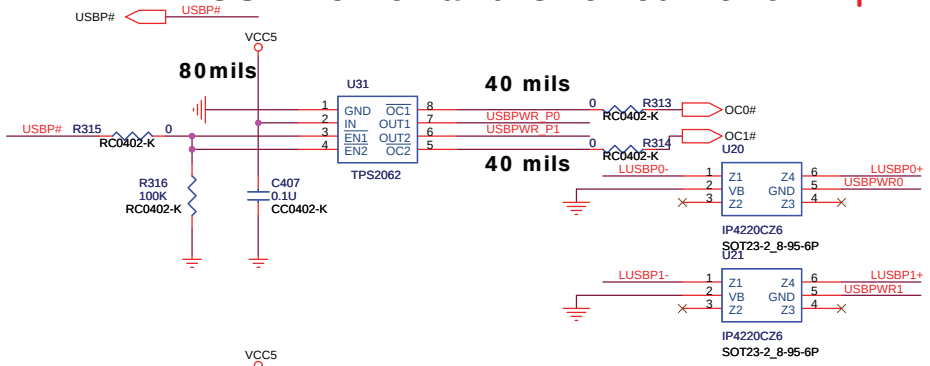
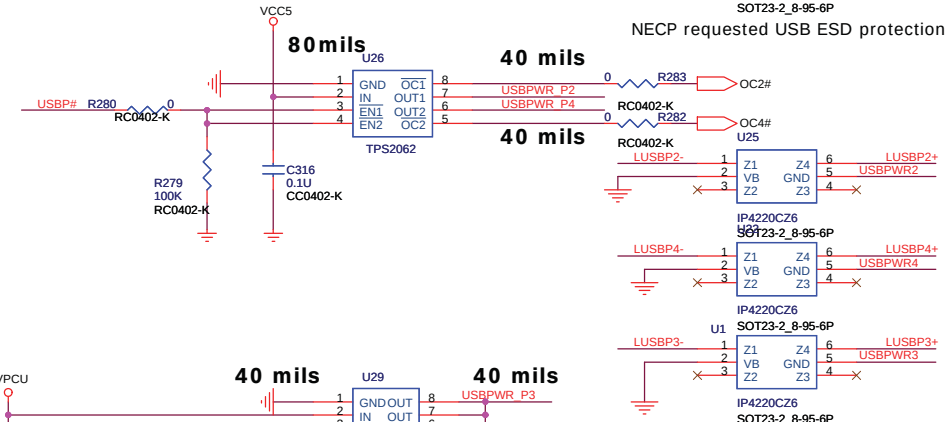
QUANTA COMPUTER

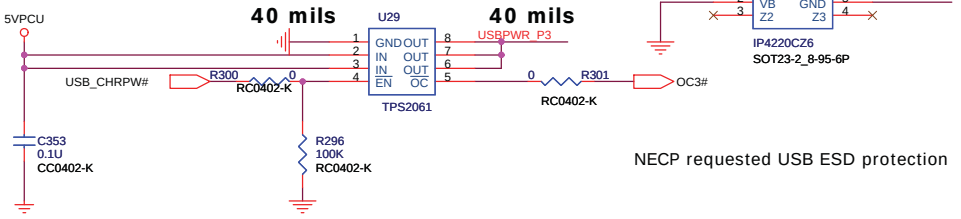
USB Power and Over current

USB Connector

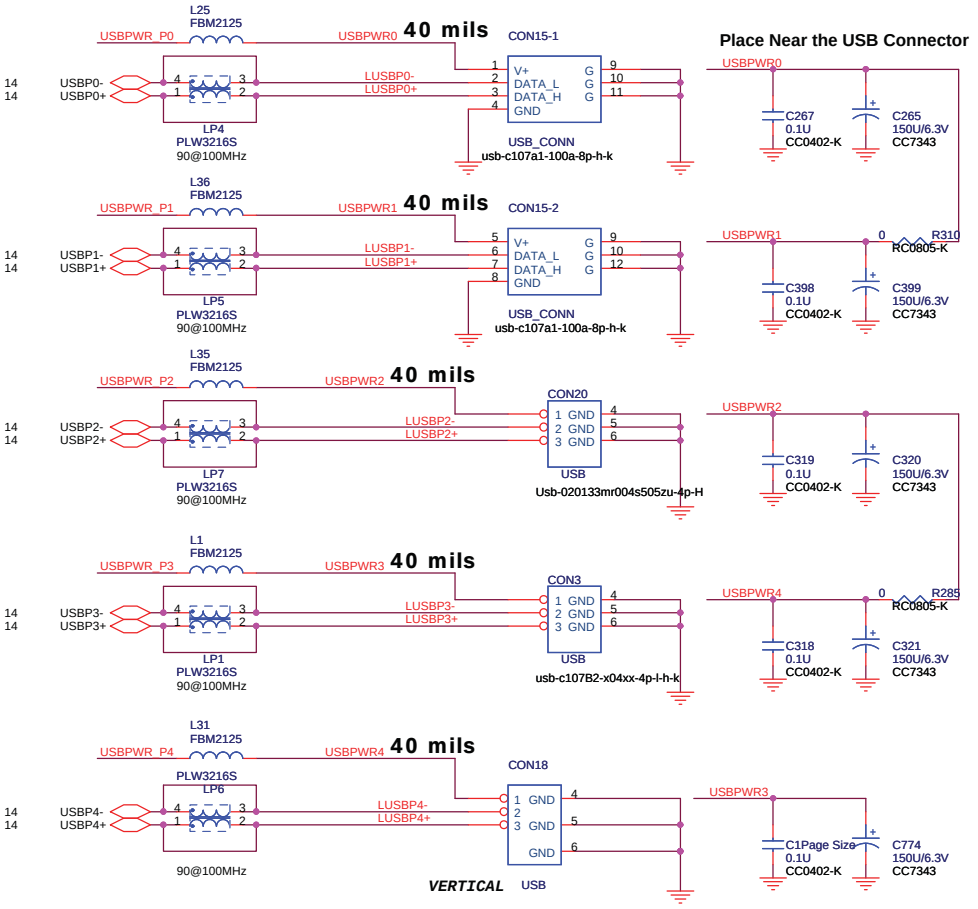


NECP requested USB ESD protection

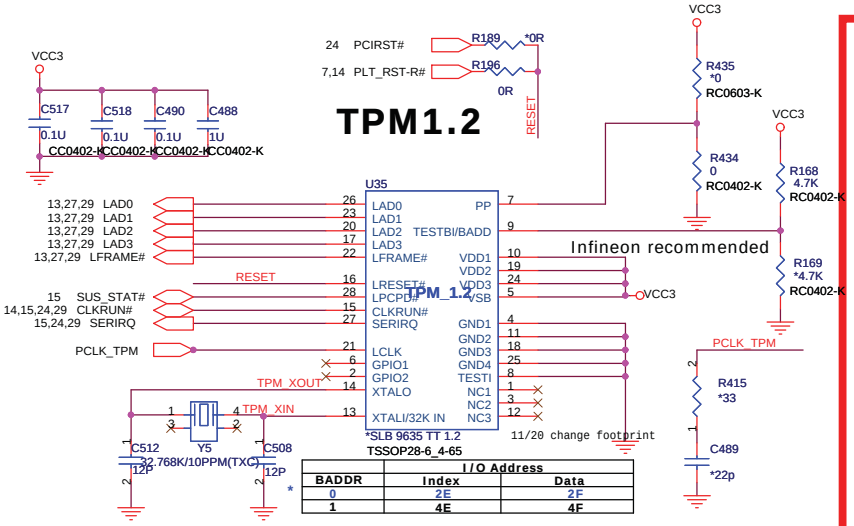




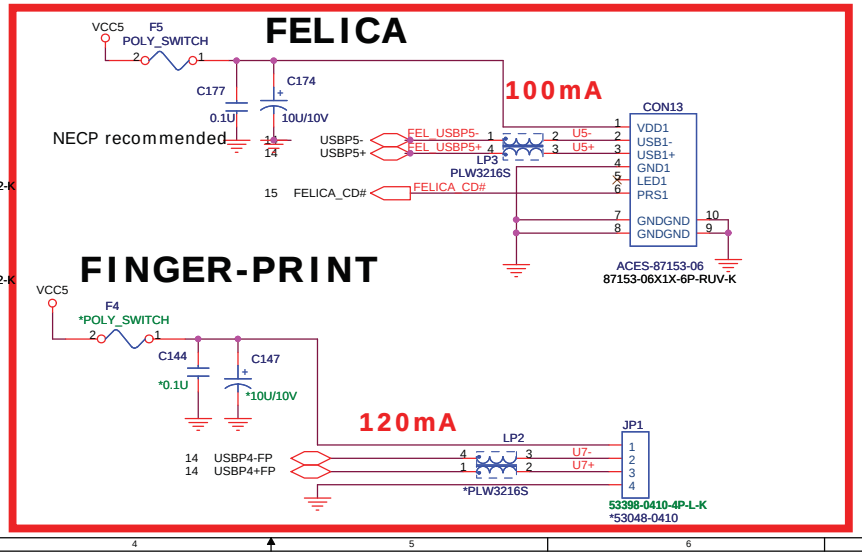
NECP requested USB ESD protection



Place Near the USB Connector



I/O Address		
BADDR	Index	Data
0	2E	2F
1	4E	4F



NECP request to add self power protection

QUANTA COMPUTER

Title	USB&TPM&FELICA&FINGER-PRINT	
Size: Custom	Document Number: WR1D MAIN BOARD	Rev: 3A
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PC87541

TQFP176-S-K

U45

39VF080/AMD-29LV081B

U46

*39VF040

Strapping Pin

BA2	R516	*10K
BA3	R520	10K
BA5	R528	10K
BA1	R514	*10K
LID#	R139	10K
IOPE3	R485	10K
MBDAT	R90	10K
MBCLK	R91	10K

I/O Address		
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
* 1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

BA2 : BADDR0
BA3 : BADDR1

Enviroment	ENV0(BA0)	ENV1(BA1)	TRIS(BA4)
* IRE	0	0	0
OBD	0	1	0
DEV	1	0	0
PROG	1	1	0

BA0 : ENV0
BA1 : ENV1
BA4 : TRIS(If =1 will tristate all I/O pins)
BA5 : SHBM(If =1 Enable share host BIOS memory)

Status indicator LED	Signal name	color
POWER LED	PWRLED0#	BLUE
	PWRLED1#	AMBER
BATTERY LED	BATLED#	BLUE
	BATLED1#	AMBER
ECO LED	ECO_LED#	BLUE
	ECO_LED1#	GREEN

Commercial PIN model only

NECP re-assign DIPSW

Title	PCU-87541 & BIOS
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QUANTA COMPUTER

INT. KEYBOARD

CON12
52610-24
52610-24-48P-RUH-K

CP6 CP2 CP1 CP5 CP4 CP3
220Px4

RP35 RP36 RP34
10KX8

MX[0..7] MX[0..7] 29
MY[0..15] MY[0..15] 29

CPU FAN Circuit

F7 RC1206-K
Q39 2SA1797
D26 1SS355
C511 22U/10V CC1206
D25 1SS355
R162 470R RC0402-K
Q17 2SC4081
R437 470R RC0402-K
R160 100K RC0402-K
R431 10K RC0402-K
Q38 DTC144EU
C507 4700P
CON9 FAN_CONN. 53398-0310-3P-L-K
VFAN FANSIG

ATI FAN Circuit

F1 RC1206-K
Q4 *2SA1797
D2 *1SS355
C9 *22U/10V CC1206
D1 *1SS355
R20 470R RC0402-K
Q1 *2SC4081
R21 *470R RC0402-K
R12 *100K RC0402-K
R5 *10K RC0402-K
Q2 *DTC144EU
C7 *4700P
CON4 *FAN_CONN. 53398-0310-3P-L-K
VFAN_ATI FANSIG_ATI

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ODDON# SOFT# E_MAIL# INTERNET# POWER_ON

EC55

Q18 DTA124EU
RB500V D14 D13 1SS355
R156 100K
NBSWON# ACIN SUSB# PCUHOLD#
Q19 Q11 Q46 Q12 Q13 Q14 DTA124EU
*DTA124EU
RF_SW#

VCC3 VCC3_LED 300mA
Q24 IRLML5103
R222 220K RC0402-K
Q23 DTC144EU
C224 0.1U
LED_ON/OFF
Low= LED Off
Hi=LED ON

EC56

Q21 IRLML5103
R644 220K RC0402-K
C788 0.1U CC0402-K
U55 NC7SZ08P5X
Q45 DTC144EUEUA-7-F
CIR_POWER CIR_SEL
Low= CIR Off
Hi= CIR ON

CIR

CON24
AF2083-A2ZG1Z
C234 4.7U CC0805-K
C232 0.1U CC0402-K
IR_DATA
1SS355 D18
R205 100K
SMK_PTE0
3VPCU PWRLED0# PWRLED1# BATLED# VCC3_LED
RF_LED_ON#
GREEN LED
BATLED1# 29
20 mlis
1SS355 D17
SMK_PTA6
New CIR don't mount from NECP
C190 0.1U CC0402-K
R201 R200 R198 R199 *0
PC/SERVER PowMode BUS/SELF PC/TV
R276 0R RC0402-K
VCC3
RF_LED#
27 WIRE_DET#
U57 *SN741G32
RF_LED_ON#
C178 4.7U CC0805-K
C181 0.1U CC0402-K
SMK_VREG
20 mlis
C183 0.1U CC0402-K

U34
PTD6 PTE2/TCH1(MUTE) PTE1/TCH0 PTE0/TCLK PTA6 PTA5 PTA4 PTA3 PTA2 PTA0 PTA1 PTC0 VREG VDD VSS
IRQ PTA7 PTE4/D- PTE3/D+ PDT5 PTD4 PTD3 PTD2 PTD1 PTD0 RST OSC1 OSC2
MC68HC908JB8 28PIN SOIC

5VPCU_IR
R209 100K RC0402-K
R206 100K RC0402-K
C206 10U/10V CC1206-K
C210 10U/10V CC1206-K
SMK_IRQ SMK_PTA7
USBP7-CIR USBP7+CIR POWER_ON
D16 1SS355
R197 10K RC0402-K
C171 1U/16V/X7R CC1206
SMK_RST
SMK_OSC1 SMK_OSC2
R400 1M
Y4 6MHz_20PPM
CC0402-K C481 33P
CC0402-K C482 33P

QUANTA COMPUTER

Title: INT.KB & FAN & PS2&CIR
Size: Custom
Document Number: WR1D MAIN BOARD
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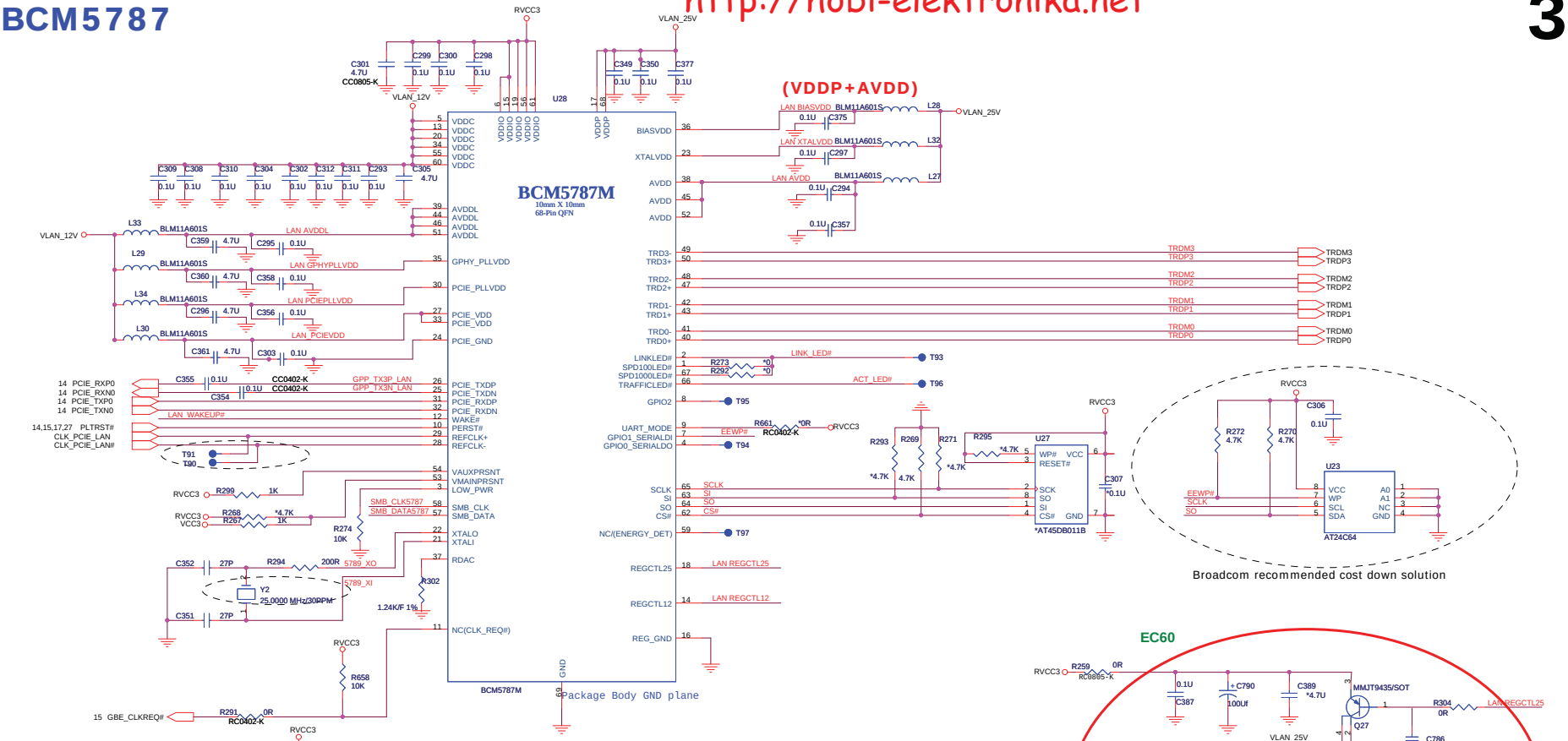

Title	BCM5787M &TouchPAD CONN
Size	Custom
Document Number	WR1D MAIN BOARD
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Sheet	31 of 43

QUANTA COMPUTER

LAN TR & CONNECTOR

http://hobi-elektronika.net

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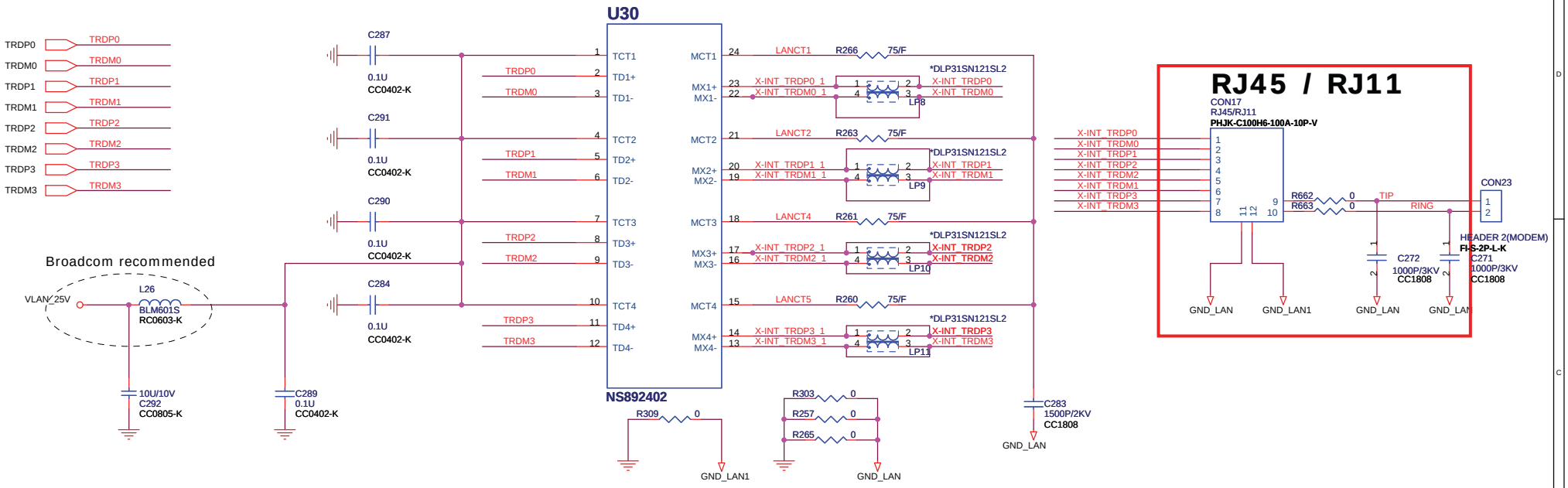
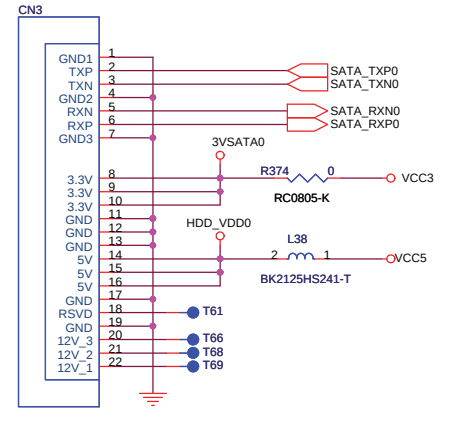
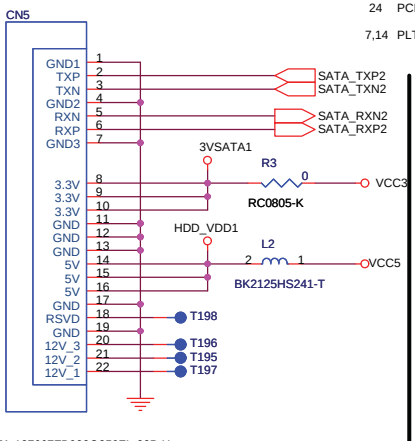
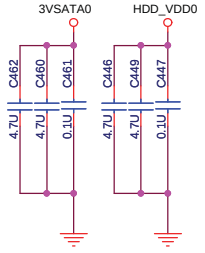


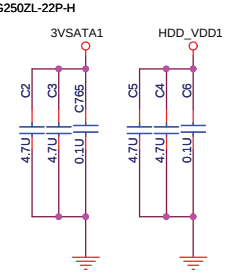
SATA_TOP(MASTER)



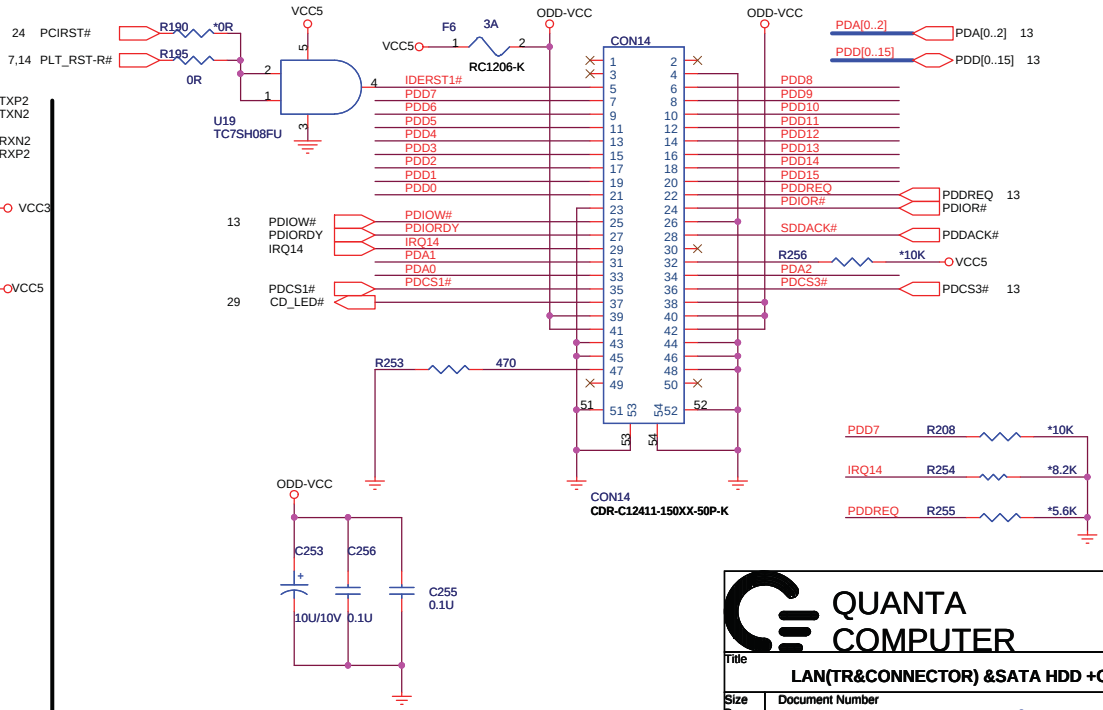
SATA_BOT(SLAVER)







ODD interface



QUANTA COMPUTER		
Title	LAN(TR&CONNECTOR) &SATA HDD +ODD	
Size B	Document Number WR1D MAIN BOARD	Rev 3A
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PVCC1 67mA
PVCC2 13.5mA
SPVCC 30mA
SVCC 323mA
VCC 133mA

HDMI PORT

Place close to the connector

Improve signal swing

Please near U12

Please near U7001

Silicon Image
Sil1930

For Sil1930,should be openned (default)
For Sil1932,should be connected

Sil1930 TQFN package

I2C ADDRESS = 20h

Mount R63, keep R64 NC at the beginning
Remove R63, mount R64 after VBIOS add PRGM# function.

To U7014#4

Open if use Atmel uC

P1.2,P1.3 : Software I2C (SST)
P4.1,P4.3 : Hardware I2C (ATMEL)

R7110 For ES1 debug only

Silicom request need to add this MOSFET to avoid ATMEL latch up

HDMI_SDA & HDMI_SCL capacitance MUST less than 50PF

Title	HDMI INTERFACE
Size / Document Number	Custom / WR1D MAIN BOARD
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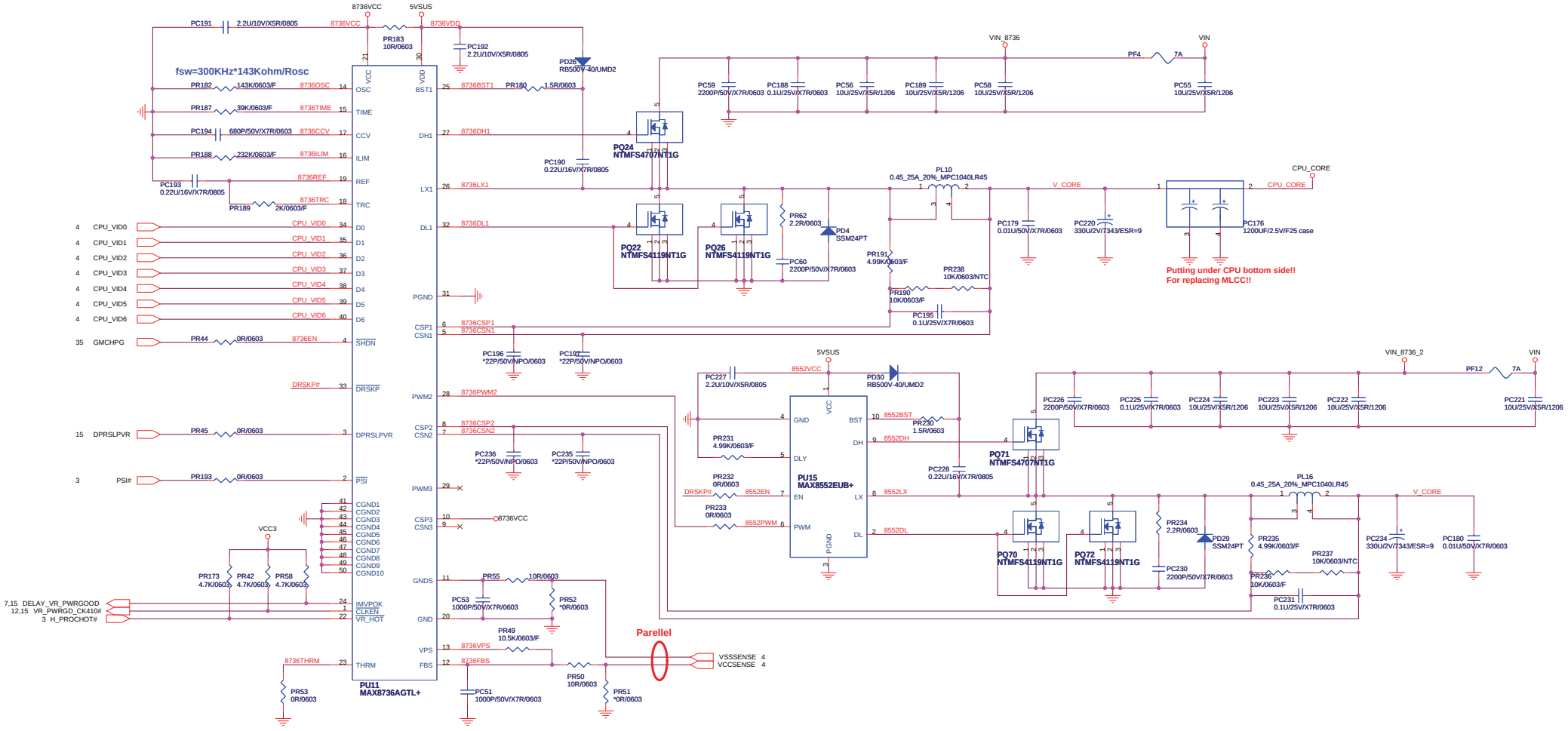
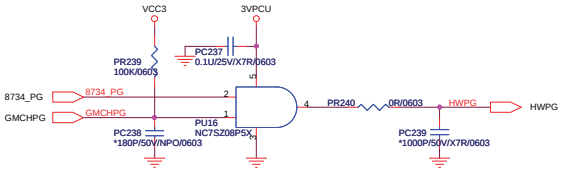
QUANTA COMPUTER

CPU CORE

dV_Target/dt=12.5mV/us*71.5kohm/R_TIME
R_ILIM(PK)=8V*R_TRC/I(PK)LIMIT*Rsense





QUANTA COMPUTER

Title	CPU CORE (MAX8736)	
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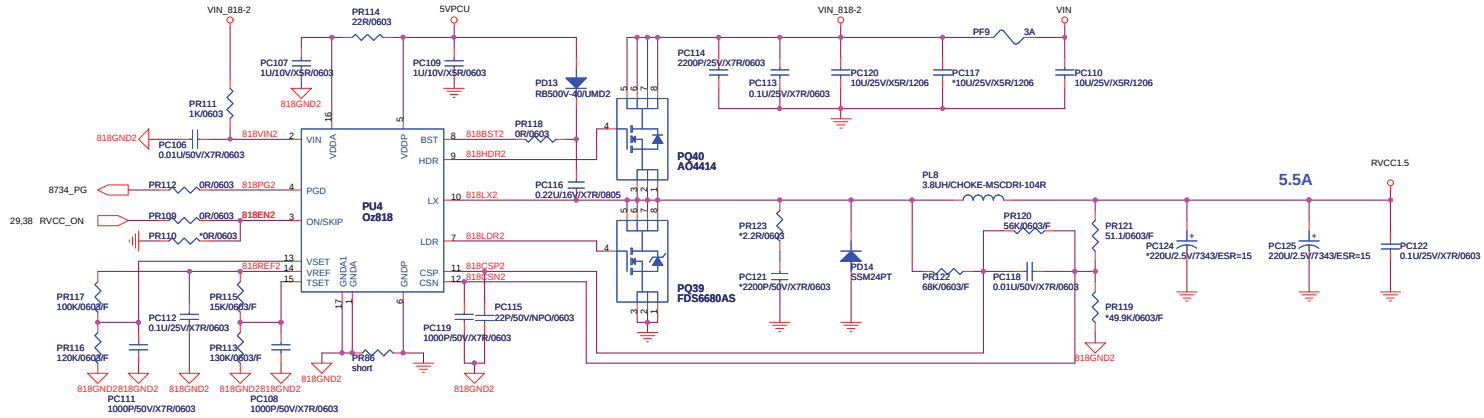
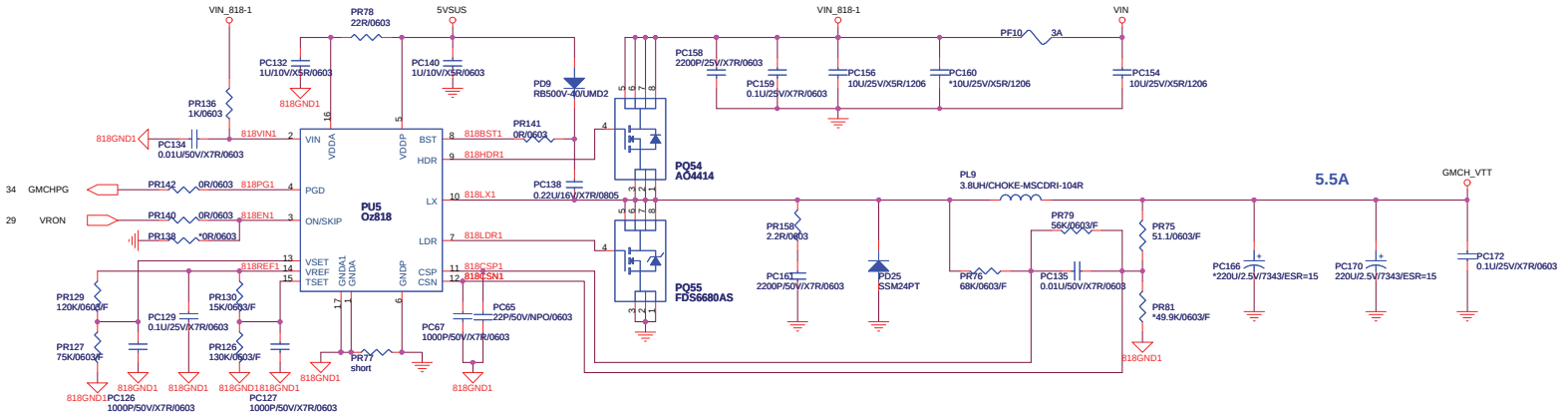
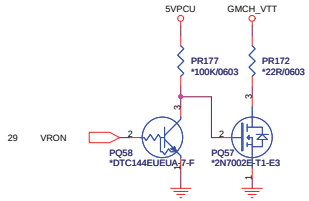
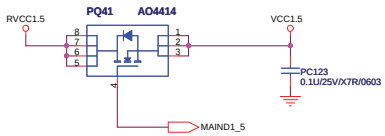
GMCH_VTT(1.05V) / RVCC1.5

38 RVCC1.5 → RVCC1.5
7,8,14,16,27,38 VCC1.5 → VCC1.5
24,34,36,38,39,40 VIN → VIN
7,9,13,16 GMCH_VTT → GMCH_VTT









QUANTA COMPUTER

Title	GMCH_VTT & RVCC1.5	
Size	Document Number: WR1D MAIN BOARD	Rev: 3A
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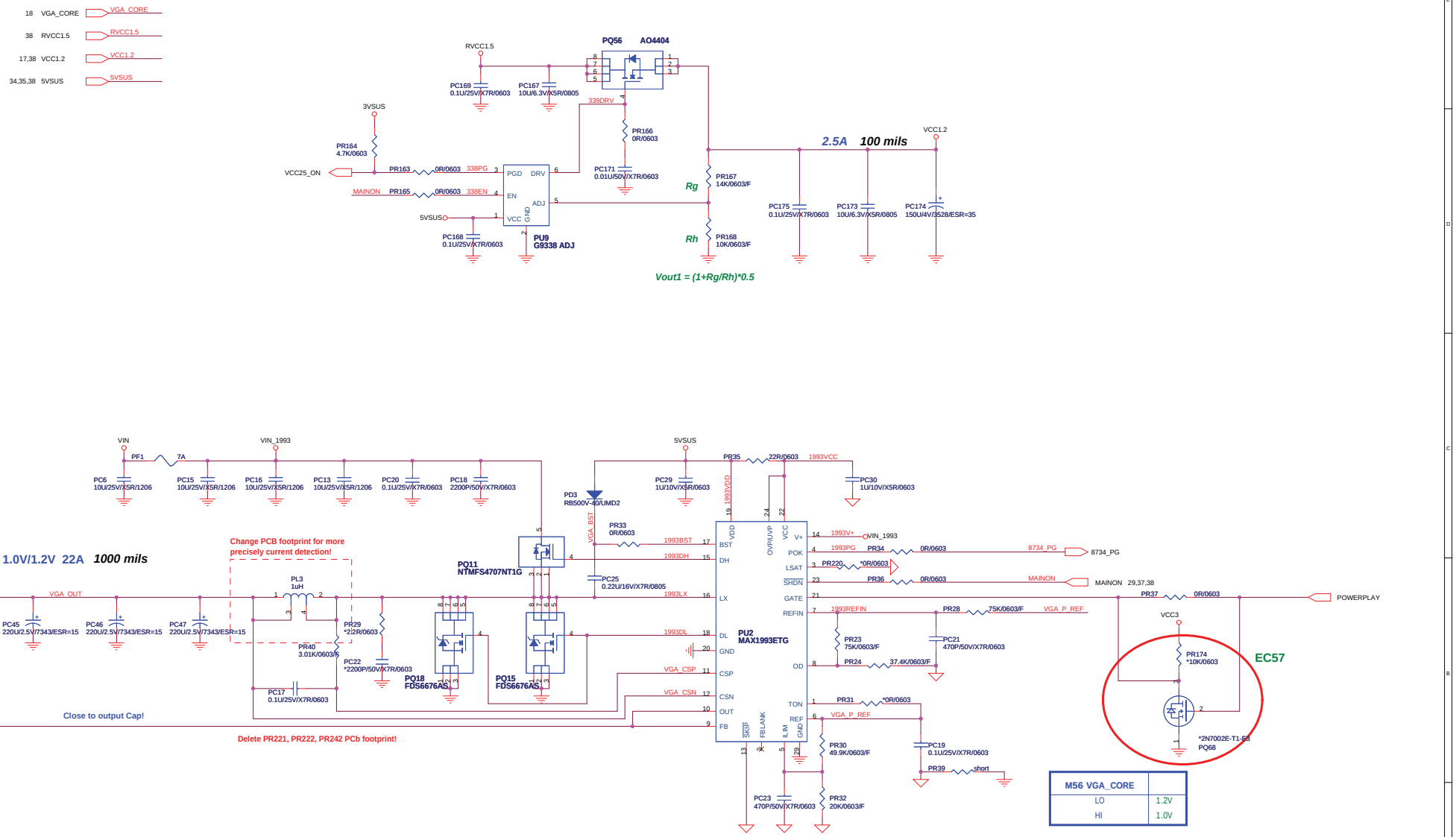

QUANTA COMPUTER

Title: VGA POWER

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SMDDR_VREF — SMDDR_VREF 7,10,11

SMDDR_VTERM — SMDDR_VTERM 10

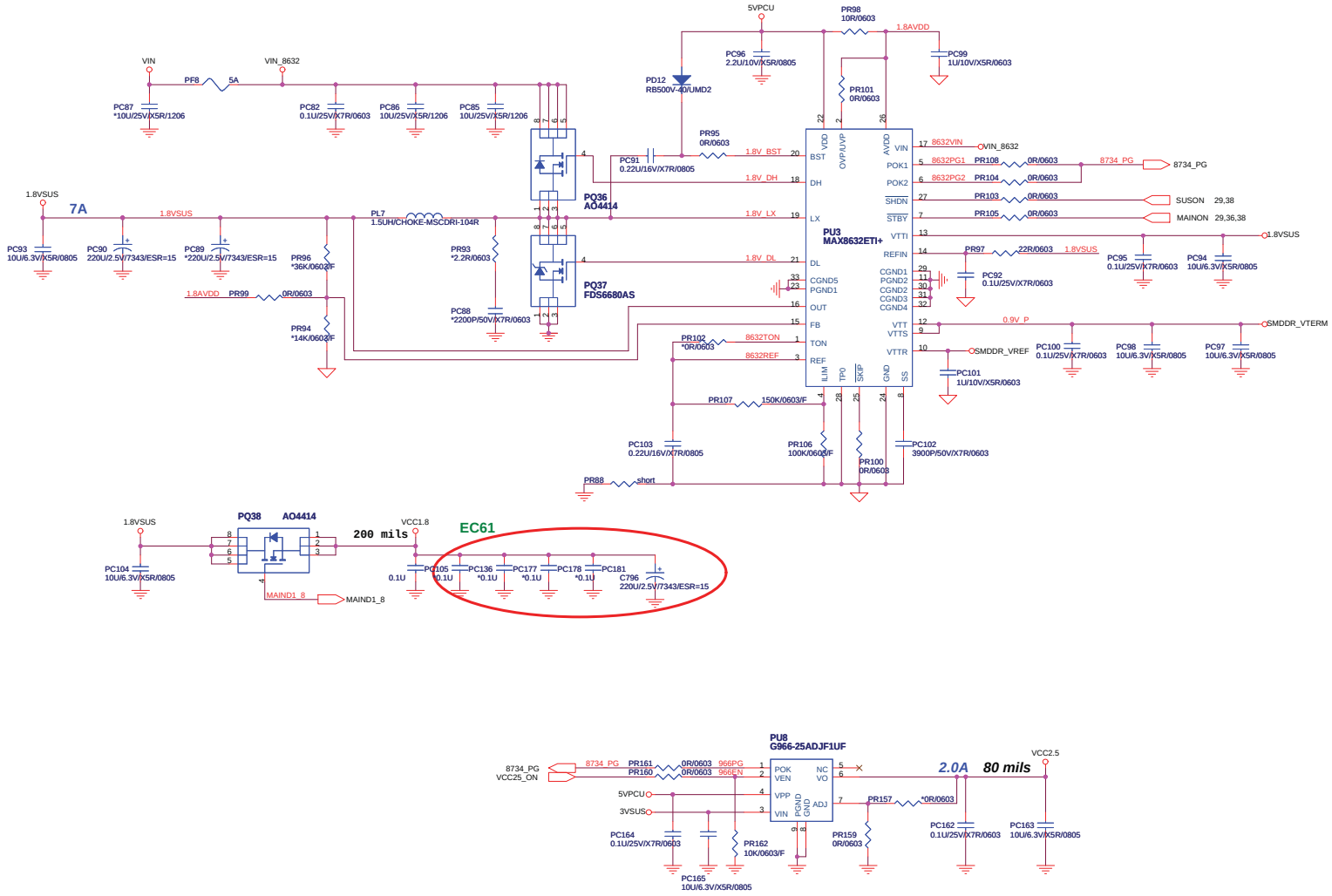
VCC1.8 — VCC1.8 19,20,21,22,33,38

1.8VSUS — 1.8VSUS 10,11,38

VCC2.5 — VCC2.5 18,20,38

VIN — VIN 24,34,36,38,39,40

1.8VSUS & VTT & VCC2.5



QUANTA COMPUTER

Title	1.8VSUS & VTT & VCC2.5	
Size: Custom	Document Number: WR1D Main Board	Rev: 3A
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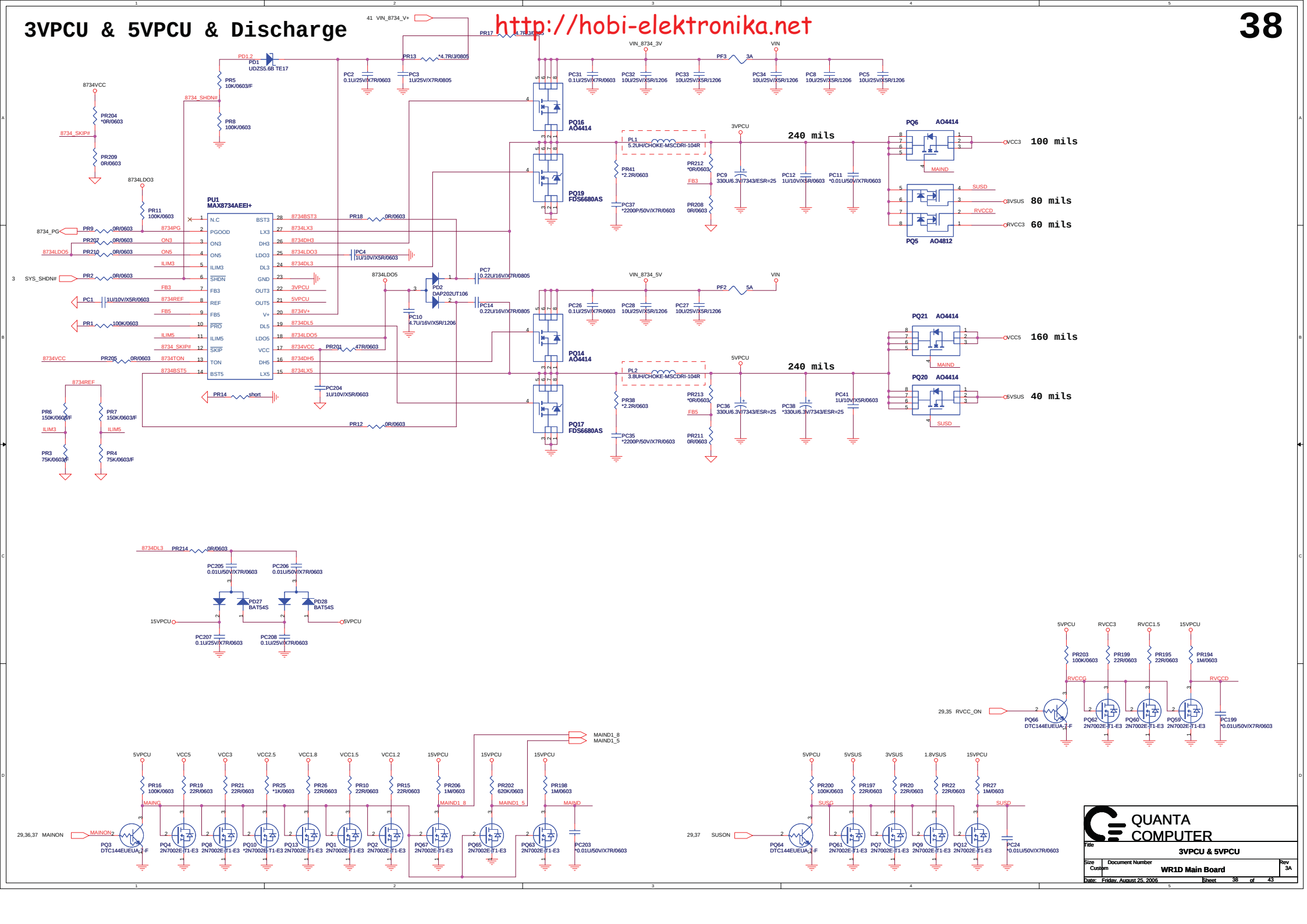
3VPCU & 5VPCU & Discharge



QUANTA COMPUTER

Title	3VPCU & 5VPCU	
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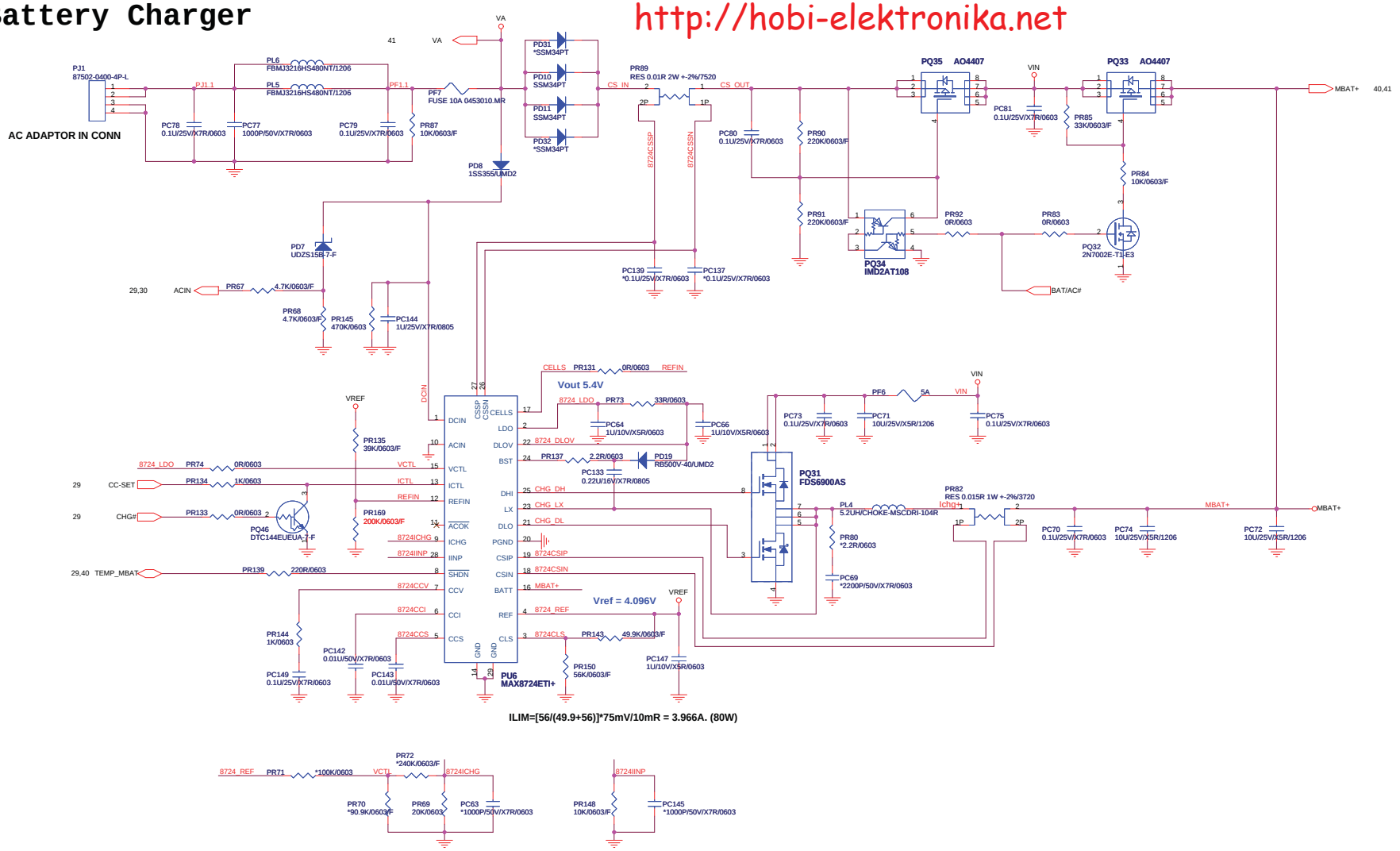
Battery Charger



QUANTA COMPUTER			
Title: BATTERY CHARGER			
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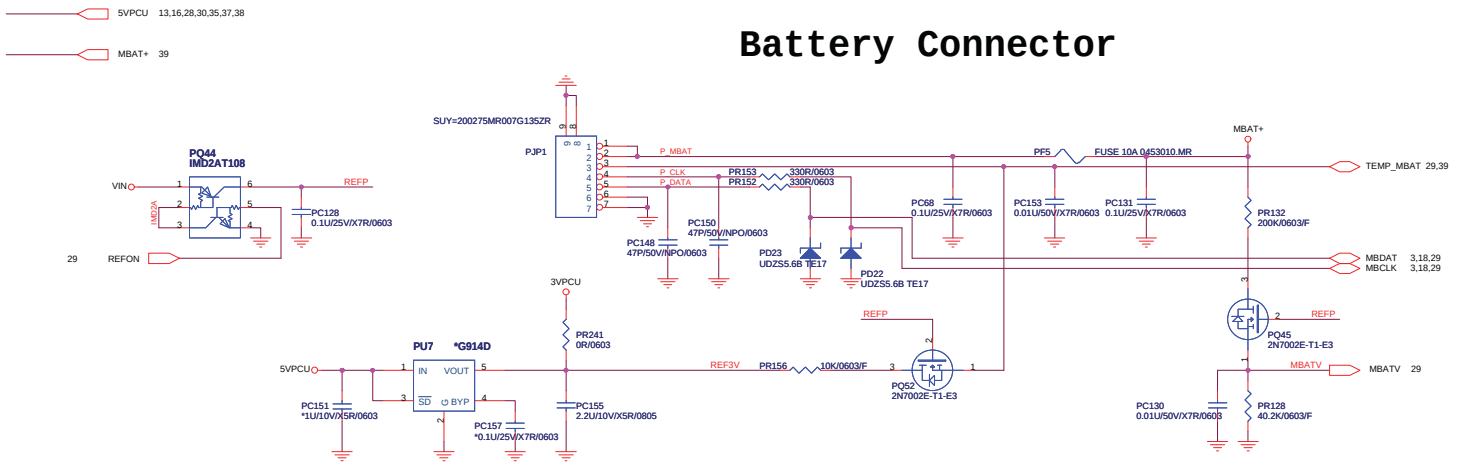
Battery Connector



TEMP_MBAT voltage :		
	System Off	System On
Battery	0V	1.6V
Adapter	3.3V	3.3V
Battery+Adapter	1.6V	1.6V

MBATV voltage :	
Li-ion 4S*P	16.8V*40.2/(200+40.2)= 2.812V 12.0V*40.2/(200+40.2)= 2.008V
Ni-MH 8S1P	8.0V*40.2/(200+40.2)= 1.34V

QUANTA COMPUTER

Title: BATTERY CONNECTOR

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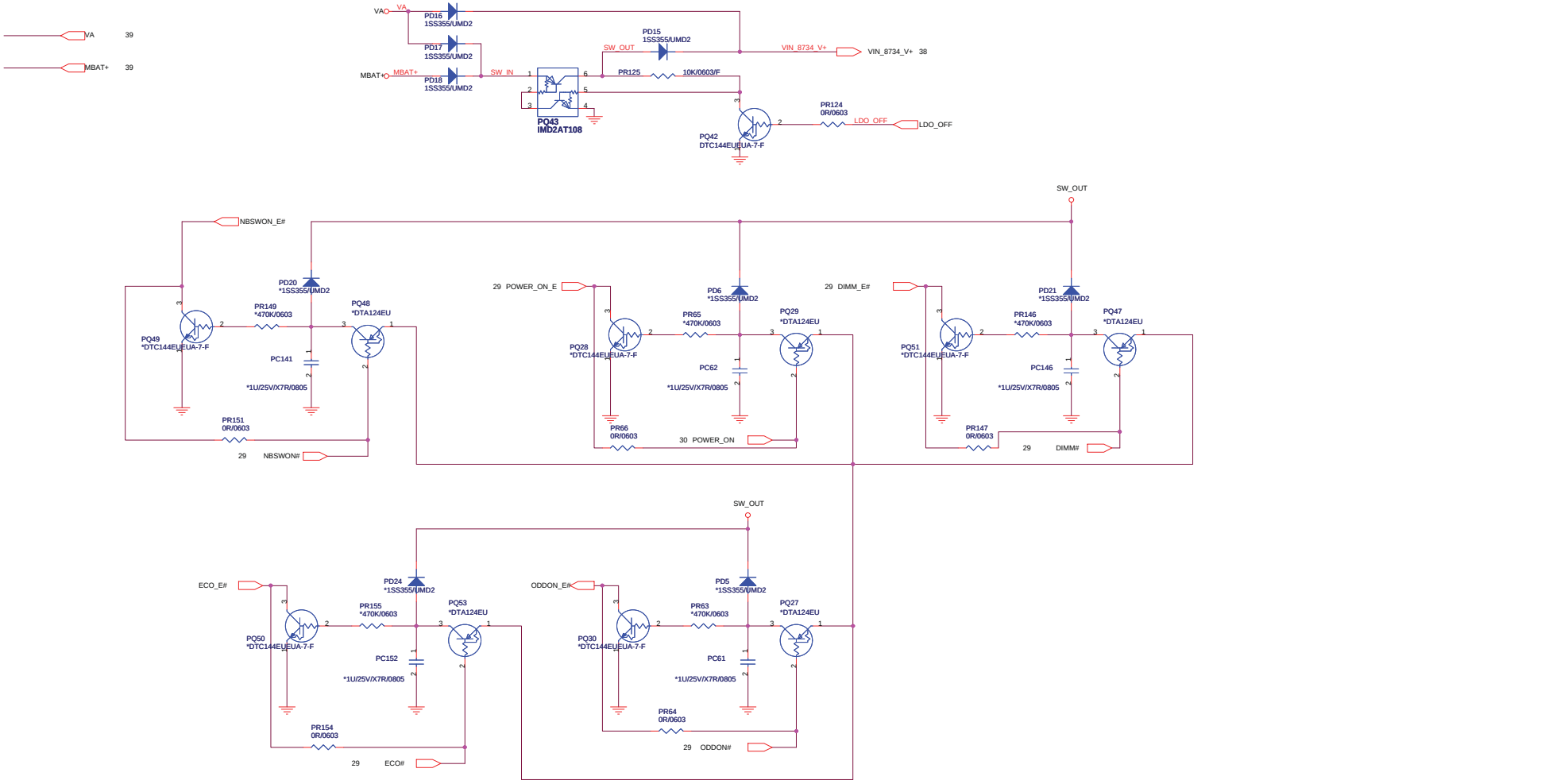

QUANTA COMPUTER

Title: No Power On S5		
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ES1 TO ES2 CHANGE LIST

EC0 PAGE ALL--ALL POSITION RENAME AFTER ES1 for less position code.
EC1 PAGE 27--Add C786,C787 for debug.
EC2 PAGE 30--Change CIR power circuit for reduce leakage issue.
EC3 PAGE 16--Add U56,C789,R660 for correct timing.
EC4 PAGE32---Cahnge C271 , C272 connect from GND to LAN_GND for Broadcom request.
EC5 PAGE31---Add L83,L84,C784,C785 on TPDATA ,TPCLK for EMI request.
EC6 PAGE7,12--Reserve R649~R656 and RP49,RP50 for GMCH GM Version.
EC7 PAGE7---ADD PCIEX16 AC Coupling CAP for can't boot issue.C783~C844 0.1uf.
EC8 PAGE8,9---Modify schematic C273,C277,C338,C403,C848 for Intel platform request.
EC9 PAGE9---Reserve L77~L81 and R143,R258,R657 for GM Version debug.
EC10 PAGE11---SWAP M_CLK_DDR2 and M_CLK_DDR3 AND set SA0_B to low SA1_B to Hi to improve second DIMM can't boot issue.
EC11 PAGE13---Change Y3 pin define from #1,#2 to #1,#4 for correct layout.
EC12 PAGE18---SWAP DDC1BD and PNL_CLK for correct layout.
EC13 PAGE25---Add EAPD function for pop noise.
EC14 PAGE26---Change Q44 to MosFET for HP sense function.
EC15 PAGE27---Reserve R632~R636 for customer request.
EC16 PAGE29---Add ECOLED1# and BATLED1 for customer spec.
EC17 PAGE29---Add ext port for net error to improve net link issue.
EC18 PAGE29---D10 Reverse and mount R585 FOR CORRECT circuit.
EC19 PAGE29---Pull-up E-MAIL# and INTERNET# signal for Auto power on issue.
EC20 PAGE30---Change CIR CONN CON24 from 10pin to 12pin for add BATTERY LED1.
EC21 PAGE32---SWAP LAN Signal P0~3 and M0~3 for correct layout.
EC22 PAGE32---SWAP SATA Signal TXP and TXN for correct layout.
EC23 PAGE33---SWAP TMDS0~2+ and TMDS0~2- for correct layout.
EC24 PAGE33---Change U2,U3 pin define pin3 to GND AND pin5 to VCC for correct layout.
EC25 PAGE33---ADD LP12~LP15 for EMI issue.
EC26 PAGE33---Change net CON7#15 to DDCCLK CON7#16 to DDCDATA for 5V level I2C.
EC27 PAGE27---Change SW2 pin 3 to GND for coreect layout.
EC28 PAGE15---Change The GPIO PIN to GPI pin.
EC29 PAGE28--- U29#2,#3 Change from VCC5 to 5VPCU for USB port Charge function when S3,S4 AC mode.
EC30 PAGE29---Add EC0_LED1# and BAT_LED1 CONTROL PIN.
EC31 PAGE31--Change R267 from 4.7K to 1K for customer request.
EC32 PAGE31---DEL R276 because double pull-high resistor.
EC33 PAGE33---SWAP U4#1,U4#44 for correct layout.
EC34 PAGE34---Change from one phase solution to 2 phase solution for Merom supporting.
EC35 PAGE36; PAGE38---For optimize ATI M56 performance and mechanical required high limit changed.
EC36 PAGE38---Change 9VPCU solution to 15VPCU solution for power saving during S4 & S5.
EC37 PAGE39;40---For power saving suring S4 & S5.
EC38 PAGE29,30---Change CIR circuit for customer request.
EC39 PAGE31---Reserve R661 PAD for debug broadcom request.

ES2 TO PP CHANGE LIST

EC40 PAGE36---Due to ES2 wrong schematic, add PR242 for low side Rdson sense.
EC41 PAGE30---Change RF-LED green Color to match spec.
EC42 PAGE36---Delete PL17, and change PL3 to single large inductor, due to mechanical lift maximum 3mm hight!!
EC43 PAGE30---Delete Q29 DIMM signal for DRD spec.
EC44 PAGE14,27---Change Mini_PCIE circuit to other PCIE bus from SB to avoid same with new card PCIE bus for correct design.
EC45 PAGE13---Add CON28 for CMOS BATTERY leakage and deformed issue ,beacause thermal issue.
EC46 PAGE27,30---Add U57 R664,R665 for LED off ,when wireless lan doesn't install , The LED can't be controlled by EC It is always off.
EC47 PAGE13---Delete the internal link for CMOS BATTERY deform issue.

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PP TO IRT CHANGE LIST

EC48 PAGE13---Delete G1 short PAD Because non-using.Change RTCRST# net for SW can't clear CMOS issue.
EC49 PAGE29---Delete FW PROGRAM SW SET.Original for debug using.
EC50 PAGE27---ADD R664,R665 for when the mini pcie haven't device install on it the led will be disable.
EC51 PAGE26---Change BUZZER power to S0 power to improve leakage issue.
EC52 PAGE29---ADD CIR_SET NET TO EC FOR SOFTWARE DETECT DIP SW ON OR OFF.
EC53 PAGE14---Swap MINI CARD PCI-E and EXPRESS CARD (NEW CARD) signal junction to ICH7 for Software request.
EC54 PAGE15---Change SWI# and MXM_THERM# Power rail to RVCC3 for improve leakage when S5.
EC55 PAGE30---Add Q12,Q46 for E-Mail and Internet EC detect signal ,when S4,S5 can power on.
EC56 PAGE30---modify CIR power circuit support battery mode power on.
EC57 PAGE36---reserve PR174 and PQ68 pad for powerplay control.
EC58 PAGE13---Change RTCRST# net to VCCRTC for CMOS clear function "date and time".
EC59 PAGE3---Change THRMTRIP# net for low temperature can't boot issue.
EC60 PAGE31---Add C790,C791 for 3V singnal drop issue when initial boot.
EC61 PAGE37---Reserve PC136,PC177,PC178,PC181 and C796 for keep VCC 1.8 at right level when run 3D mark.

Title <Title>		
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