

MODEL NAME : *PIM10*

PCB NO : *LA-6501P (DA60000I100)*

BOM P/N : *43190931L01*

Compal Confidential

Kenting Schematics Document

Intel Pine Trail-M (Pineview-M + Tiger point)

2010-03-18

REV: 0.2

@ : Nopop Component

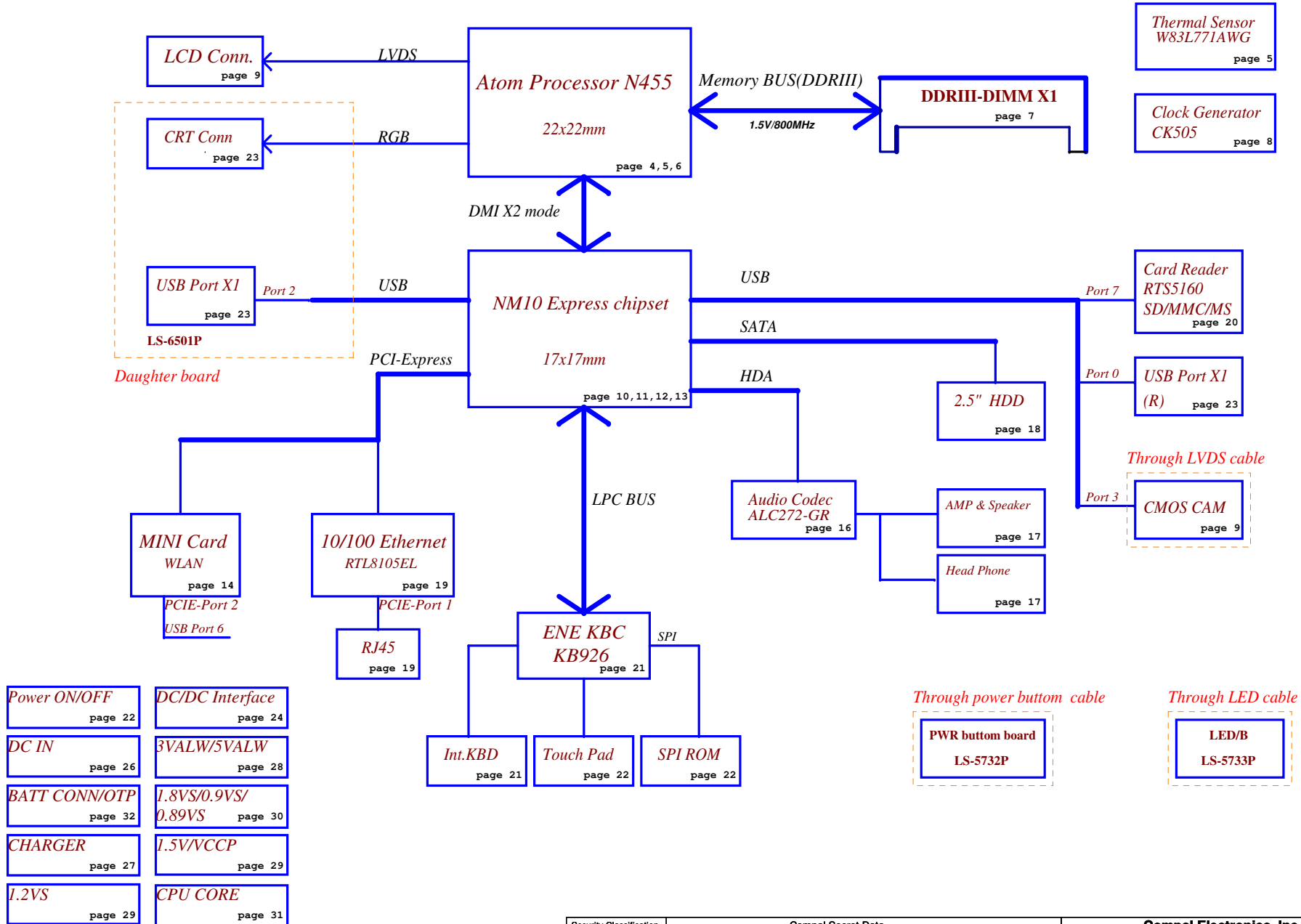
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Issued Date	2010/03/18	Deciphered Date	2011/03/18	Title Cover Page		
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				Custom	LA-6501P	0.2
				Date:	Tuesday, April 27, 2010	Sheet 01 of 35

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Model Name : PIM10

Project Code : ANRPIM1000

Project Name : Kenting



Power ON/OFF page 22	DC/DC Interface page 24
DC IN page 26	3VALW/5VALW page 28
BATT CONN/OTP page 32	1.8VS/0.9VS/ 0.89VS page 30
CHARGER page 27	1.5V/VCCP page 29
I.2VS page 29	CPU CORE page 31

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Title	Block Diagrams			
Size	Document Number	LA-6501P		Rev
Customer				0.2
Date:	Monday, May 10, 2010	Sheet	02	of 35



DA600001100

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.75VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	VCCP switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+0.89VS	CORE VOLTAGE FOR CPU VGA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VS	VS always on power rail	ON	ON	ON*
+RTCBATT	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table(Page 21)

VCC	3.3V +/-5%					
ID	BRD ID	Ra	Rb	Vab (Min)	Vab (Type)	Vab (Max)
0	R01 (SSI)	NC	0	0V	0V	0.155V
1	R02 (PT)	100K +/- 5%	8.2K +/- 5%	0.168V	0.250V	0.362V
2	R03 (ST)	100K +/- 5%	18K +/- 5%	0.375V	0.503V	0.621V
3	R10 (X build)	100K +/- 5%	33K +/- 5%	0.634V	0.819V	0.945V
4	Reserved	100K +/- 5%	56K +/- 5%	0.958V	1.185V	1.359V
5	Reserved	100K +/- 5%	100K +/- 5%	1.372V	1.650V	1.838V
6	Reserved	100K +/- 5%	200K +/- 5%	1.851V	2.200V	2.420V
7	MP	100K +/- 5%	NC	2.433V	3.300V	3.300V

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
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No PCI Device

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b

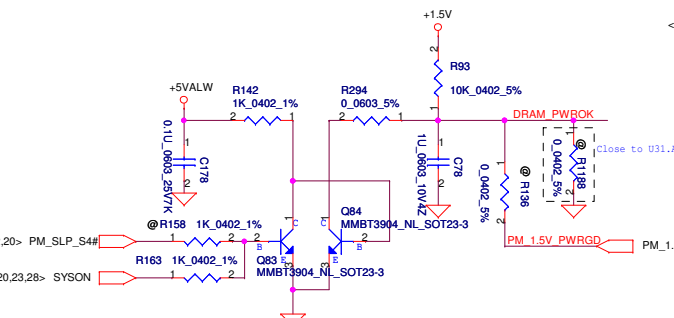
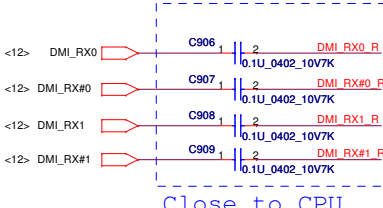
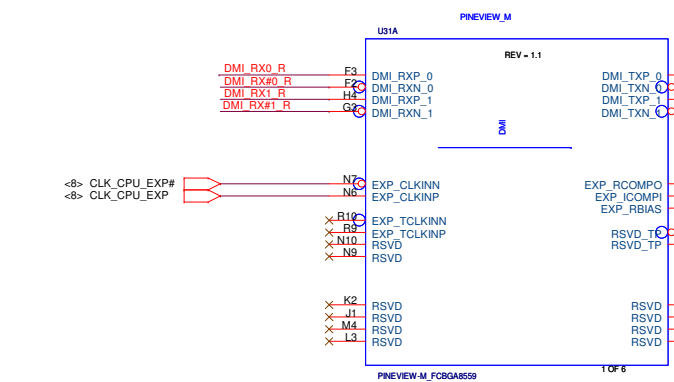
EC SM Bus2 address

Device	Address
W83L771AWG	1001_100X b
EMC1402	100_1100X b

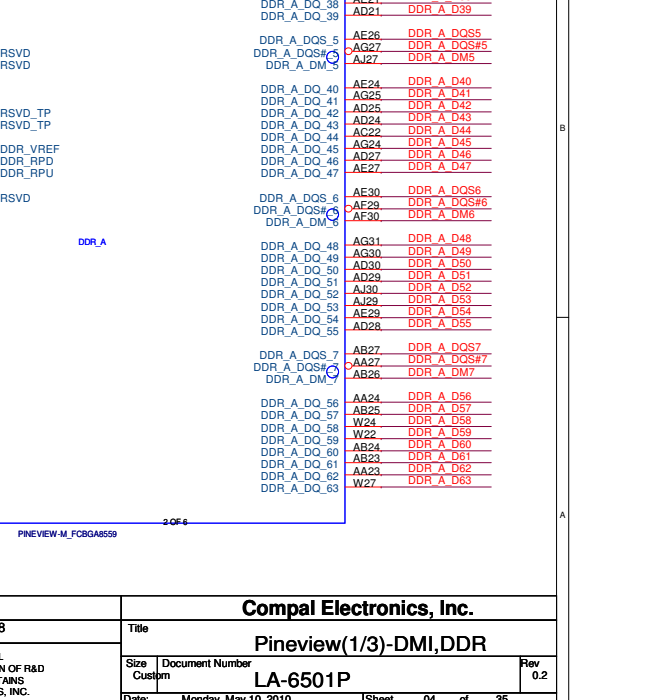
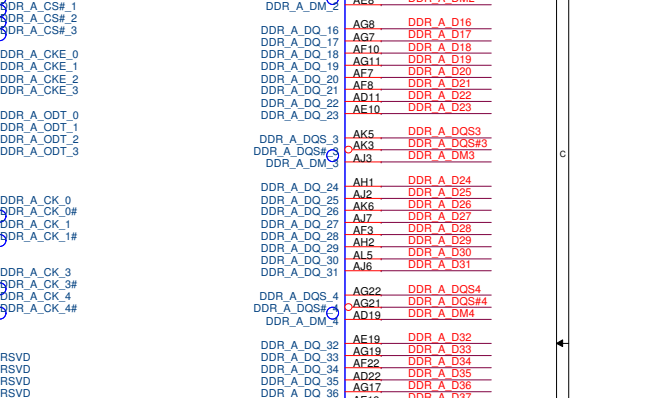
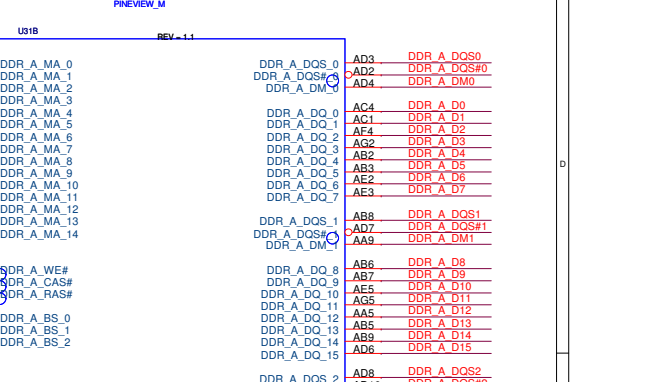
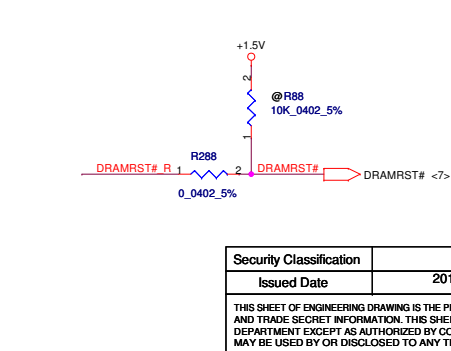
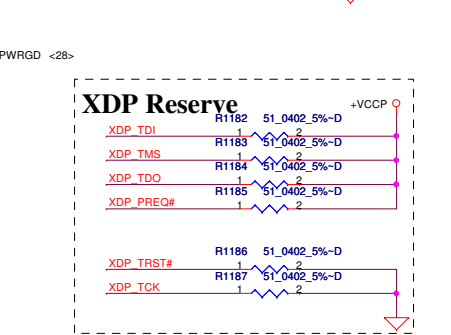
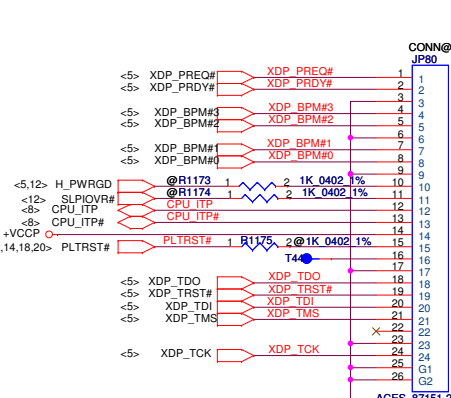
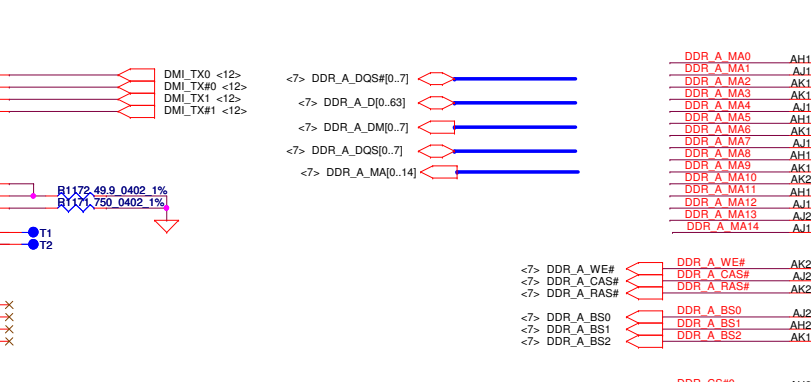
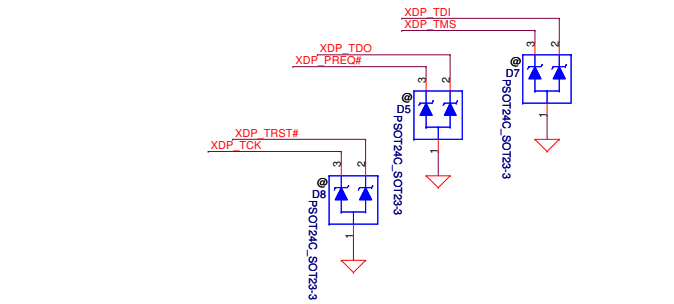
Tiger Point SM Bus address

Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb

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Size	Document Number	Rev		
Custom	LA-6501P	0.2		
Date:	Tuesday, April 27, 2010	Sheet	03	of 35



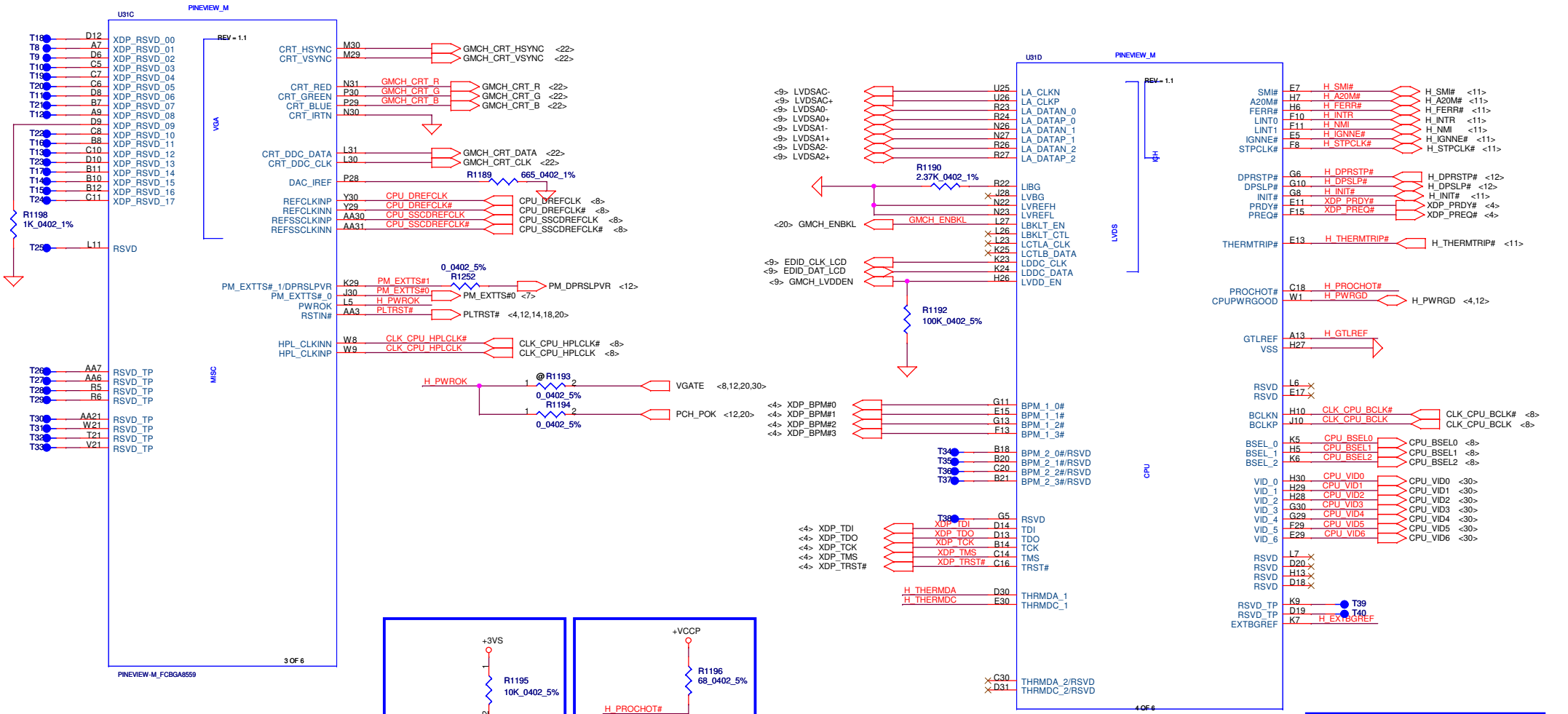
Signal Name	Description	Direction	Type
BCLKP[0]	Differential Core Clock In		Diff Clk CMOS
BCLKN[0]	Differential Core Clock In	I	Diff Clk CMOS
HPL_CLKINP	Differential Host Clock In	I	Diff Clk CMOS
HPL_CLKINN	Differential Host Clock In		Diff Clk CMOS
EXP_CLKINP	Differential DMI Clock In	I	Diff Clk CMOS
EXP_CLKINN	Differential DMI Clock In		Diff Clk CMOS
REFCLKINP	Differential PLL Clock In	I	Diff Clk CMOS
REFCLKINN	Differential PLL Clock In		Diff Clk CMOS
REFSSCLKINP	Differential Spread Spectrum Clock In	I	Diff Clk CMOS
REFSSCLKINN	Differential Spread Spectrum Clock In		Diff Clk CMOS



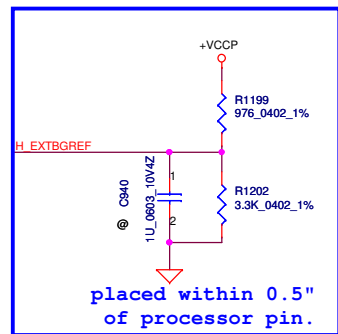
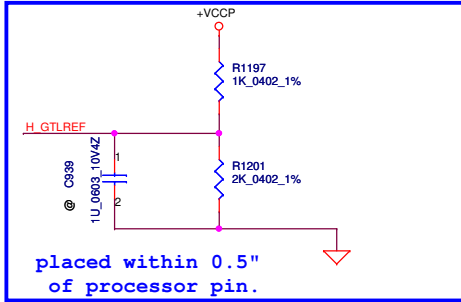
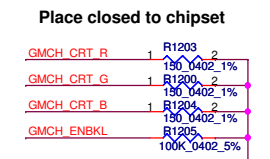
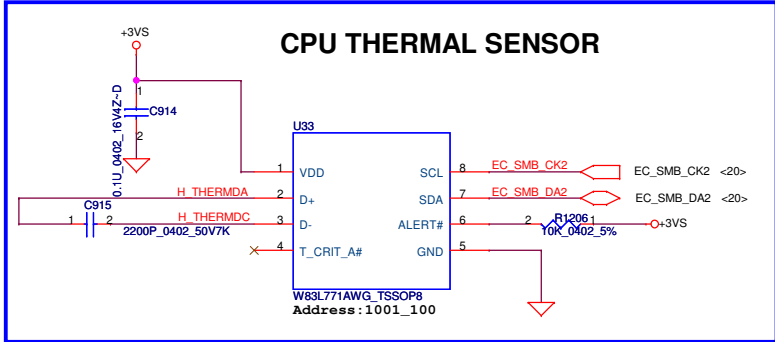
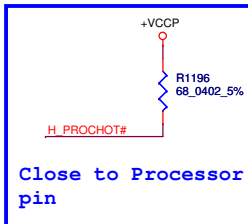
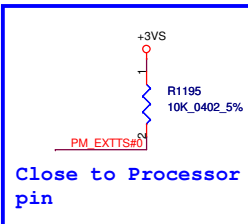
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		2011/03/18

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Pineview (1/3)-DMI,DDR			
Title	Size	Document Number	Rev
	Custom	LA-6501P	0.2
Date:	Monday, May 10, 2010	Sheet	04 of 35

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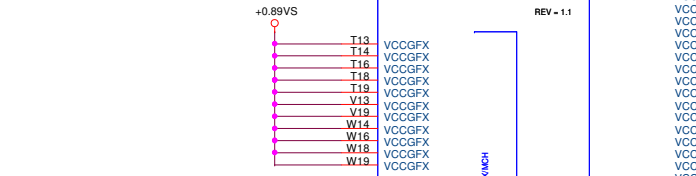


H_THERMDA, H_THERMDC routing together.
Trace width / Spacing = 10 / 10 mil

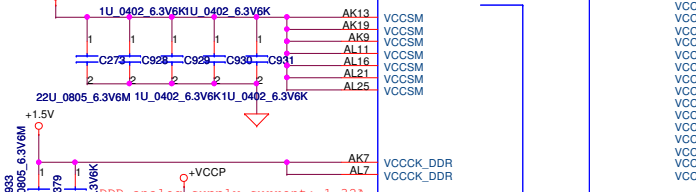


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Size	Document Number	Rev		0.2	
Custom	LA-6501P				
Date:	Monday, May 10, 2010	Sheet	05	of 35	

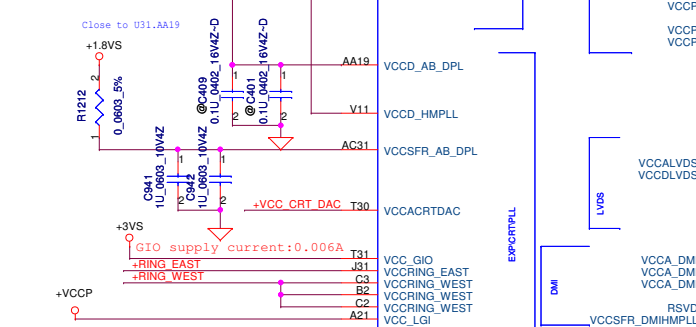
GFX supply current: 1.38A
Sustained GFX supply current: 1.05A



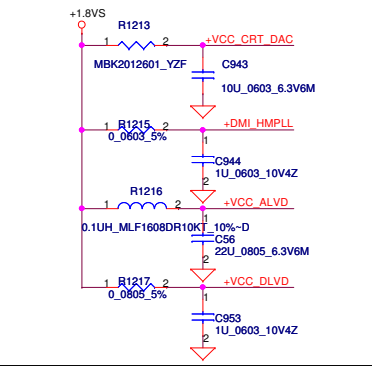
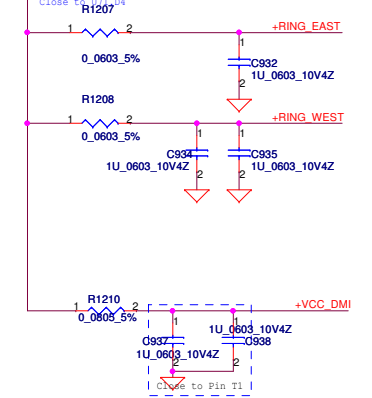
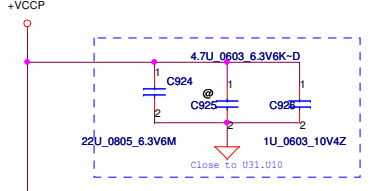
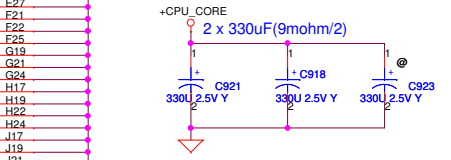
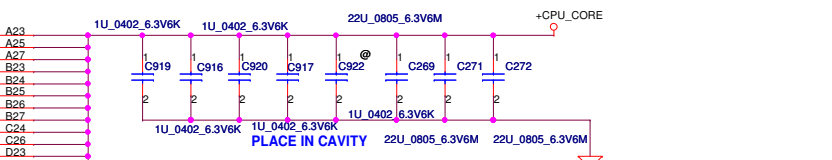
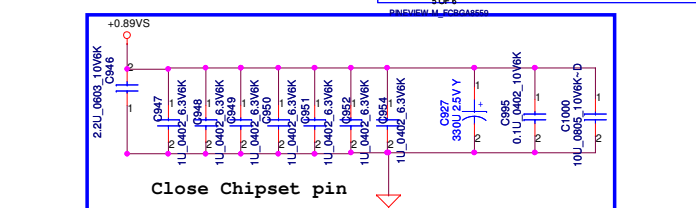
DDR supply current: 2.27A



Display PLL SFR and CRT DAC supply current: 0.154A



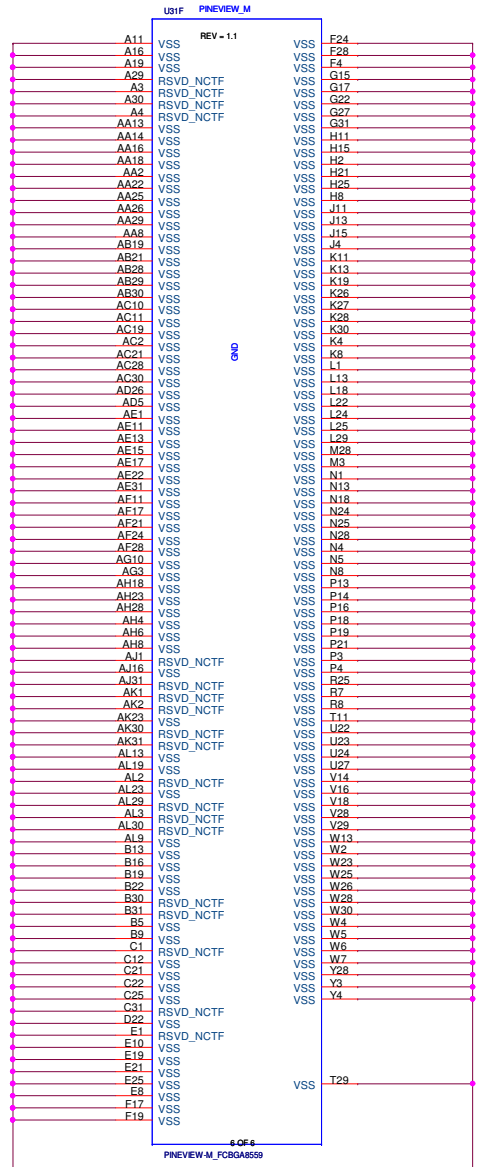
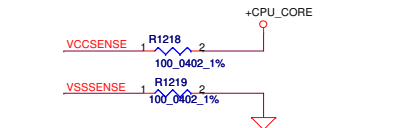
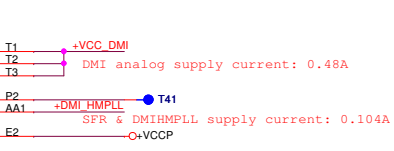
DAC, GIO, LVDS, & LGIO, DPPLL, HMPLL supply current: 0.33A



Processor Core analog supply current: 0.08A



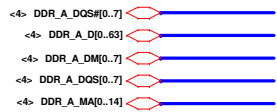
LVDS supply current: 0.06A



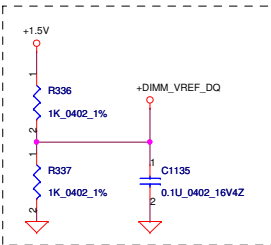
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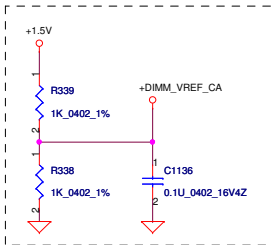
Compal Electronics, Inc.		
Title Pineview(3/3)-POWER,GND		
Size Custom	Document Number LA-6501P	Rev 0.2
Date: Monday, May 10, 2010	Sheet 06	of 35



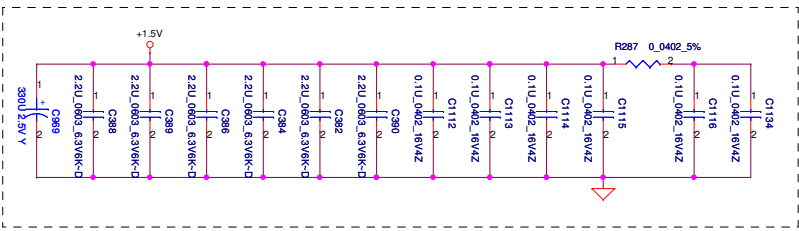
Layout Note:
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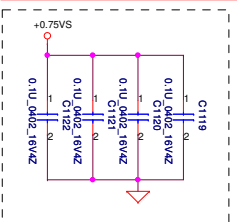
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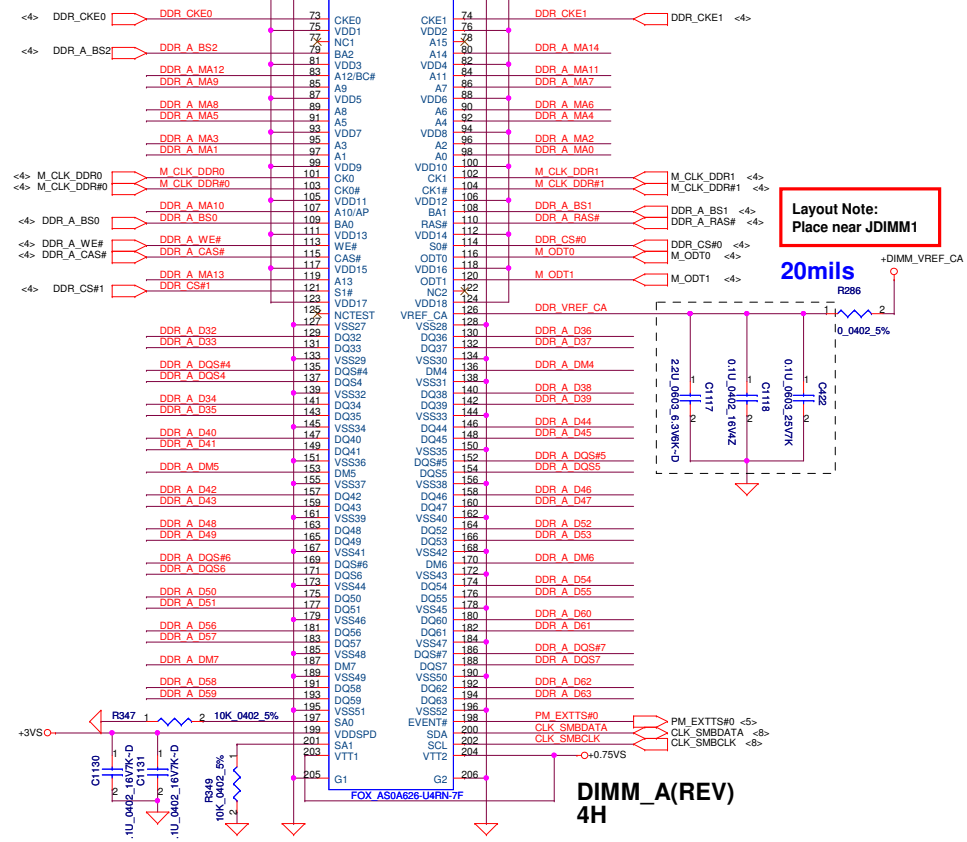
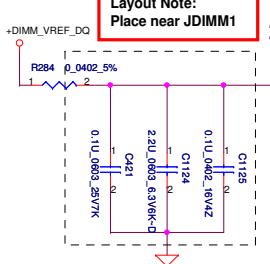
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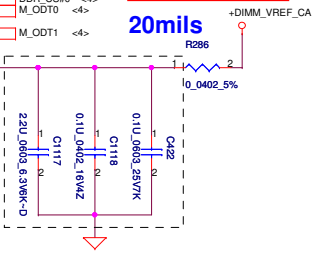
Layout Note:
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Layout Note:
Place near JDIMM1
20mils

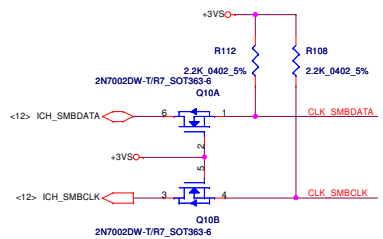
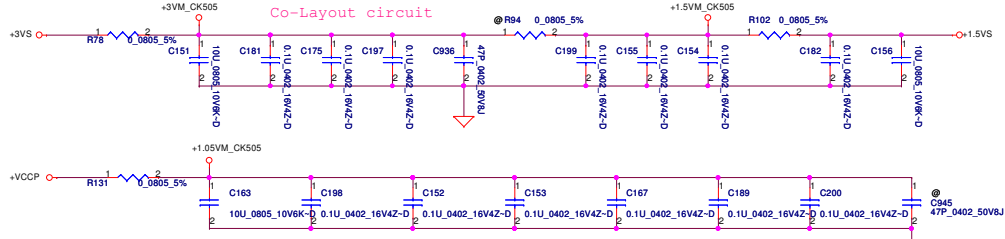


Layout Note:
Place near JDIMM1
20mils



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Size	Document Number	Rev		0.2	
Custom	LA-6501P	Date		Friday, May 07, 2010	
				Sheet 07 of 35	

CLKSEL2	CLKSEL1	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	1	133	100	33.3	14.318	96.0	48.0
0	1	0	0	200	100	33.3	14.318	96.0	48.0
0	1	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	1	100	100	33.3	14.318	96.0	48.0
1	1	0	0	400	100	33.3	14.318	96.0	48.0
1	1	1	1						
Reserved									



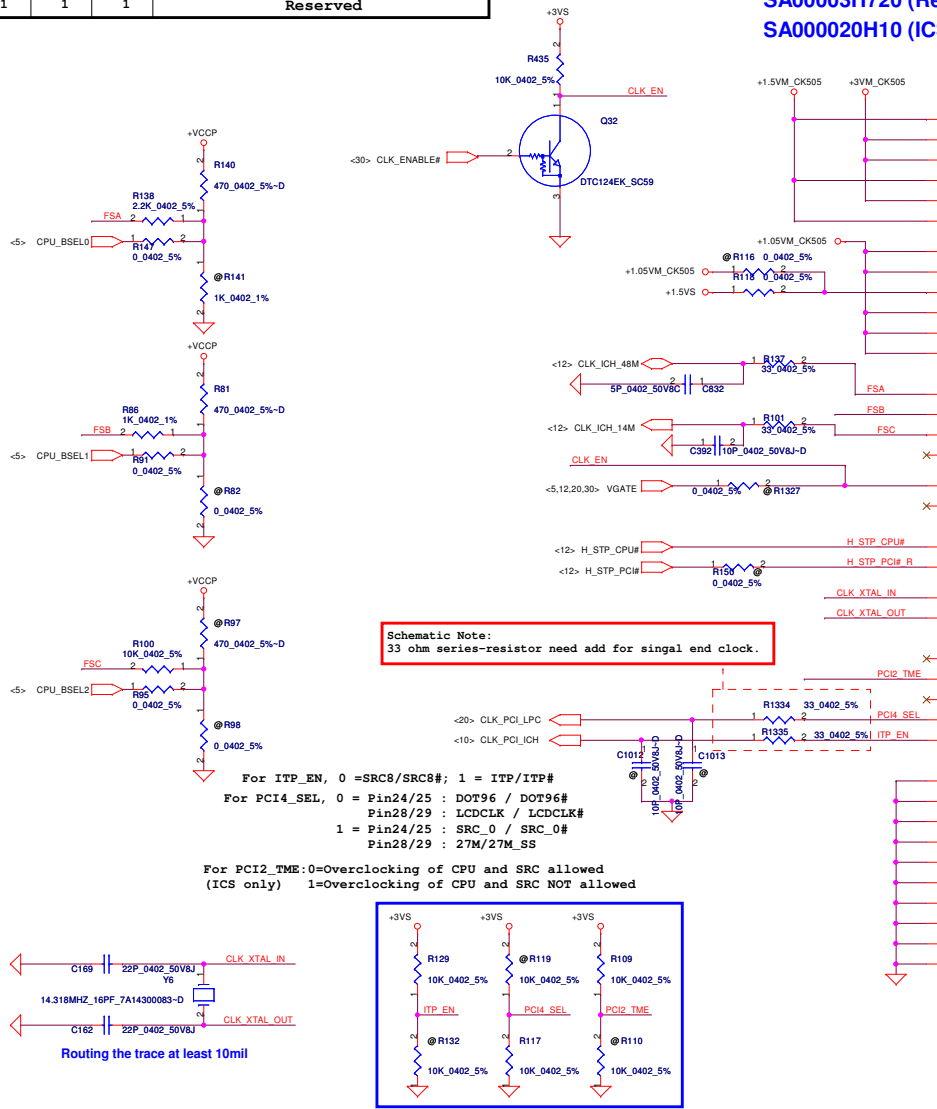
SA0003H720 (Realtek : RTM890N-397-VB-GRT)
SA00020H10 (ICS : ICS9LPRS387AKLFT)

Co-Layout circuit

Realtek (L.P.)	+3VS, +1.5VS	De-pop R94, R118; pop R102, C182, C156, C936, R116
ICS (L.P.)	+3VS, +1.5VS	De-pop R94, R116; pop R102, C182, C156, C936, R118
ICS, Silego	+3VS	De-pop R102, C182, C156, C936, R118; pop R94, R116

SRC PORT LIST

PORT	DEVICE
SRC0	CPU_VGA
SRC2	DMI
SRC3	
SRC4	PCIE_SATA
SRC6	PCIE_WLAN
SRC7	
SRC8	CPU_XDP
SRC9	PCIE_LAN
SRC10	PCIE_TigerPoint
SRC11	

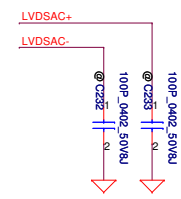
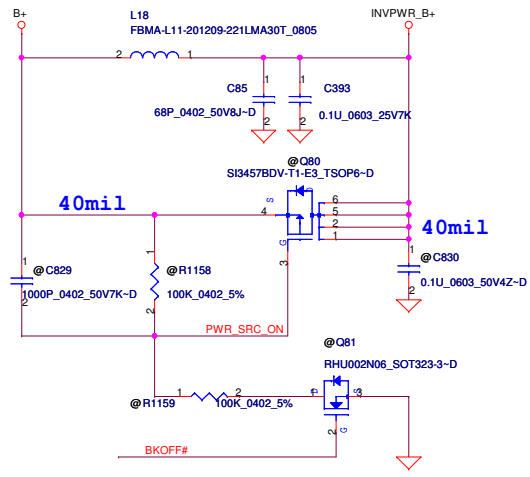
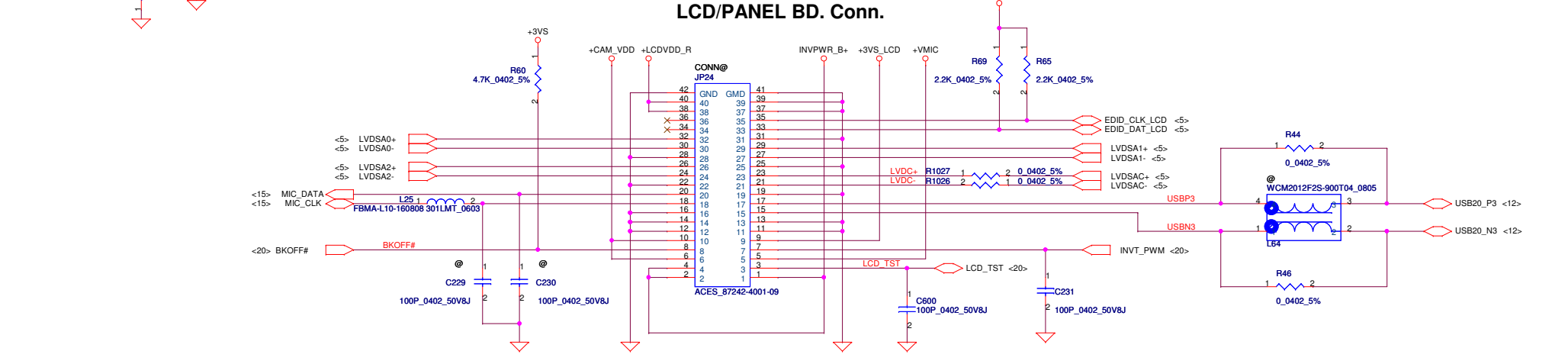
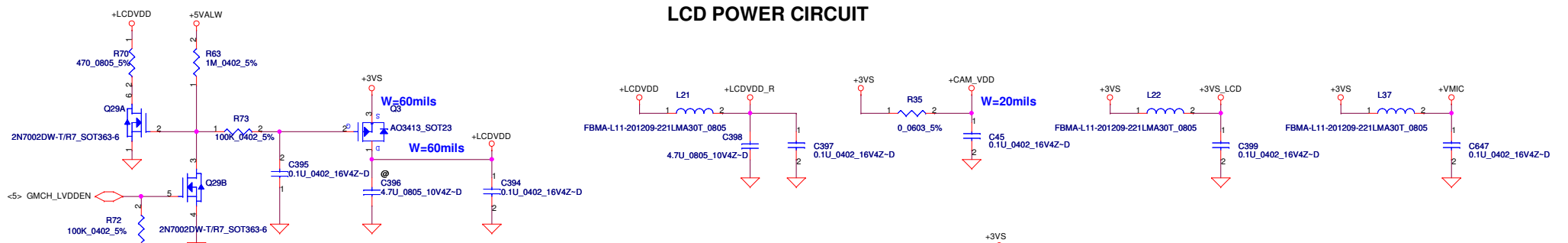


Schematic Note:
33 ohm series-resistor need add for singal end clock.

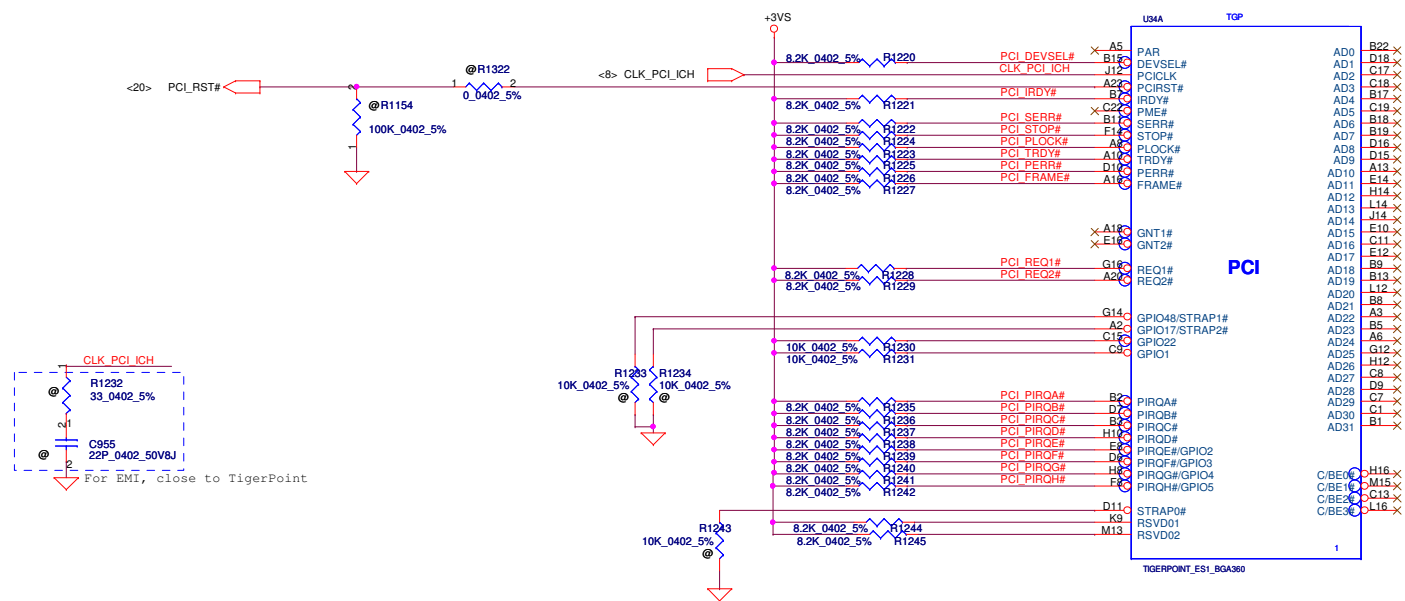
For ITP_EN, 0 = SRC8/SRC8#; 1 = ITP/ITP#
For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LDCCLK / LDCCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS
For PCI2_TME: 0=Overclocking of CPU and SRC allowed
(ICS only) 1=Overclocking of CPU and SRC NOT allowed

Routing the trace at least 10mil

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Title	Compal Electronics, Inc.		
Title	Clock Generator CK505		
Size	Document Number	Rev	0.2
LA-6501P			
Date	Friday, May 07, 2010	Sheet	08 of 35



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Date: Friday, May 07, 2010				Sheet 09 of 35	



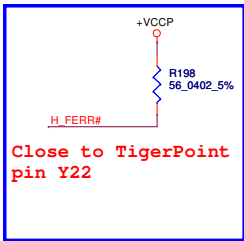
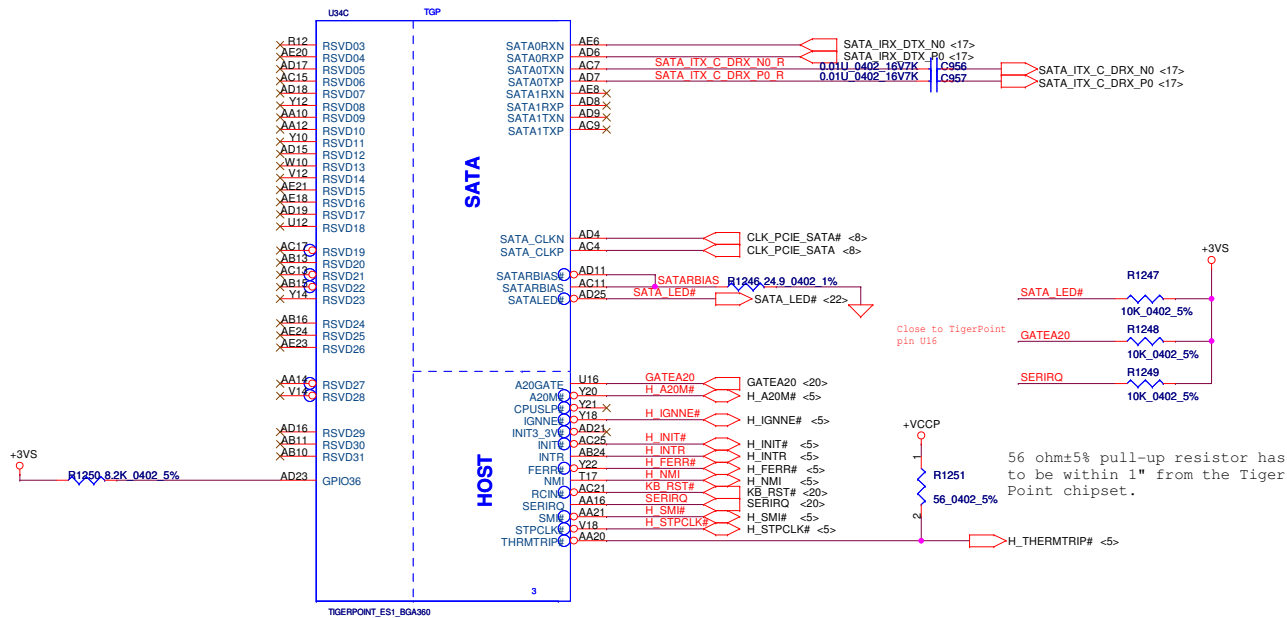
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Issued Date	2010/03/18	Deciphered Date	2011/03/18	Title		
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				LA-6501P		0.2
				Date:	Friday, May 07, 2010	Sheet 10 of 35

Compal Electronics, Inc.

Tigerpoint(1/4)-PCI

LA-6501P

Friday, May 07, 2010 Sheet 10 of 35



ESD request

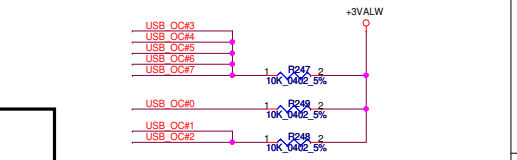
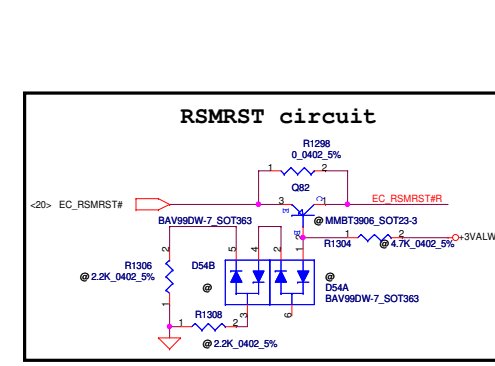
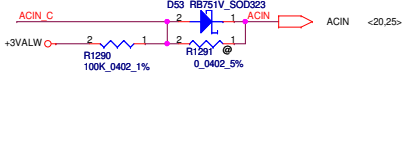
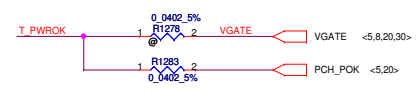
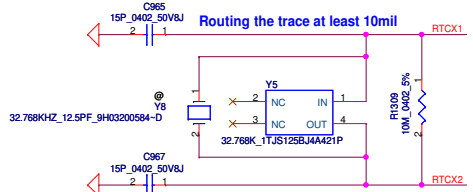
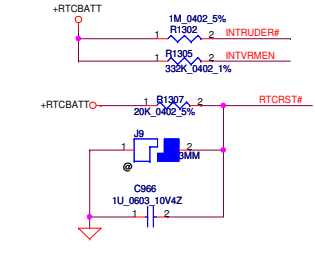
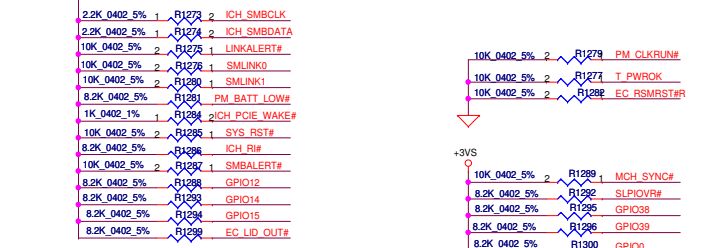
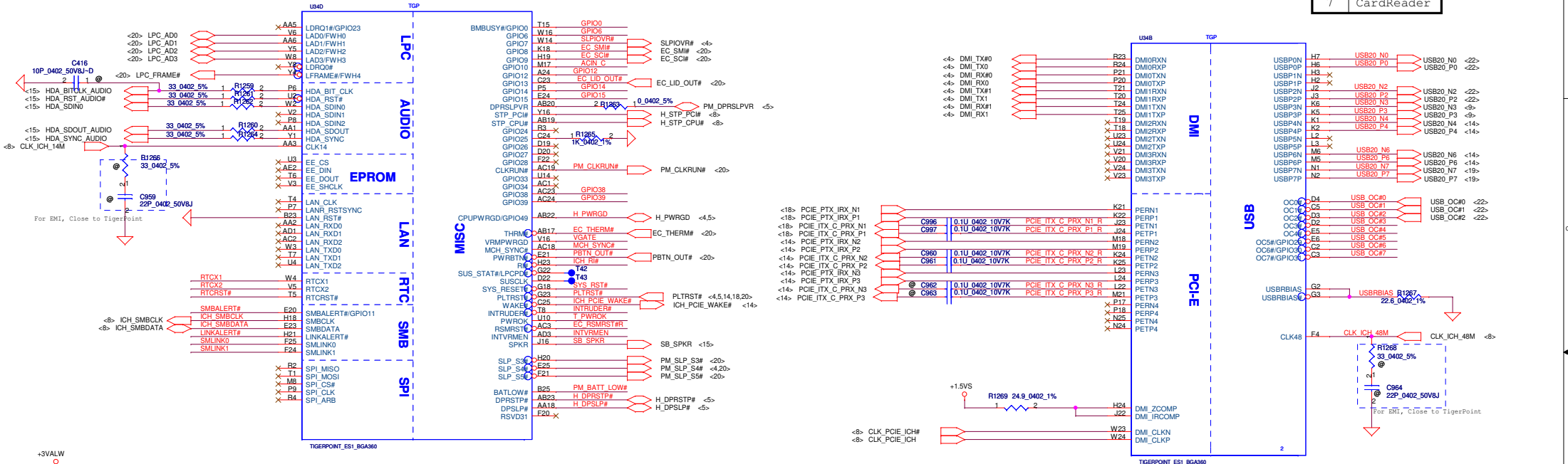
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H_INTR#	C453@	2	100P_0402_50V8J
H_FERR#	C454@	2	100P_0402_50V8J
H_NMI#	C455@	2	100P_0402_50V8J
H_SMI#	C456@	2	100P_0402_50V8J
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Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/03/18	Deciphered Date	2011/03/18	
Title			Tigerpoint(2/4)-HOST,SATA	
Size	Document Number	Rev	LA-6501P 0.2	
Date:	Friday, May 07, 2010	Sheet	11	of 35

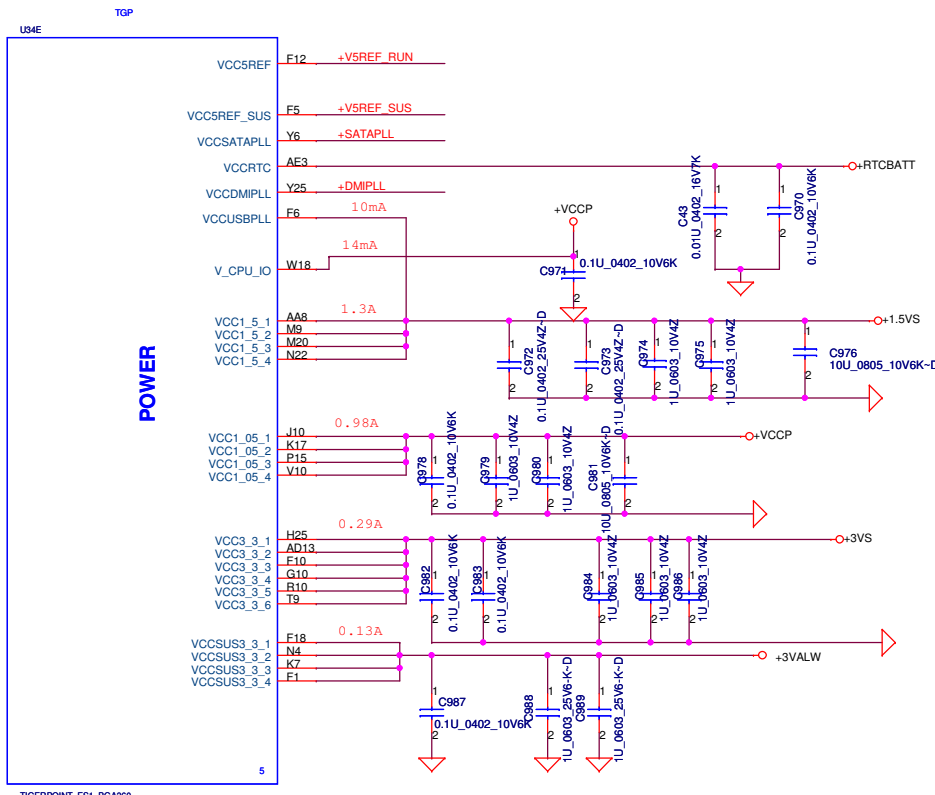
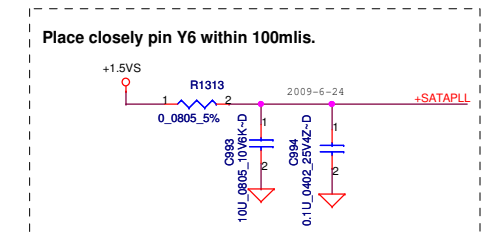
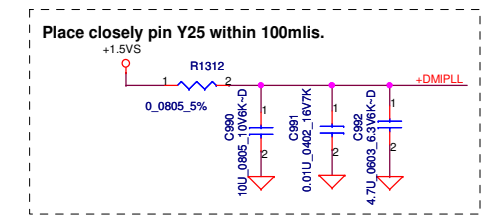
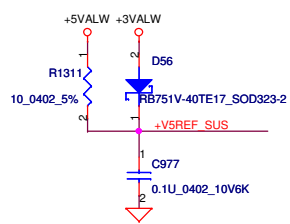
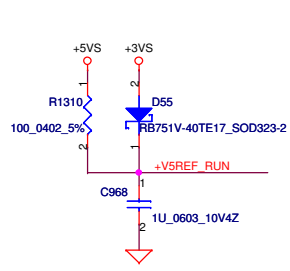
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PCIe Port List	
1	LAN
2	WLAN
3	

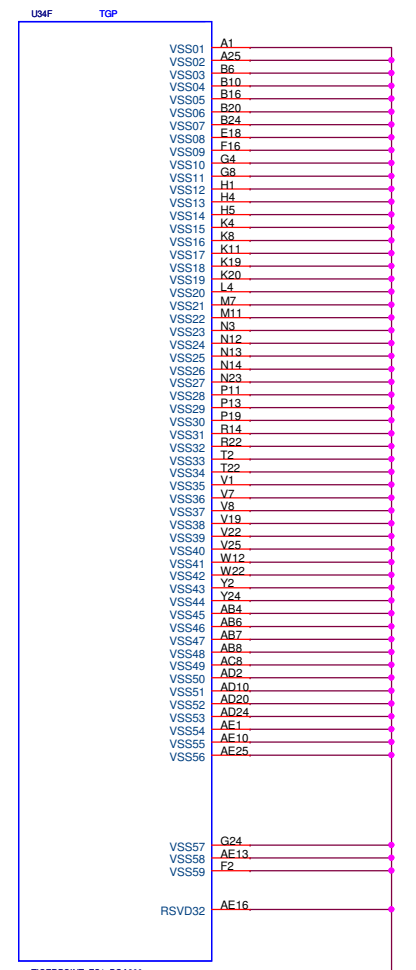
USB Port List	
0	USB1 (Right)
1	
2	USB2 (Left)
3	Camera
4	
5	
6	WLAN + BT
7	CardReader



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Size	Document Number	Rev		0.2	
Custom	LA-6501P	Date:		Friday, May 07, 2010	
Sheet		12		of 35	



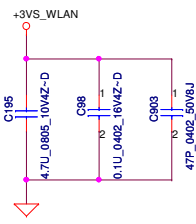
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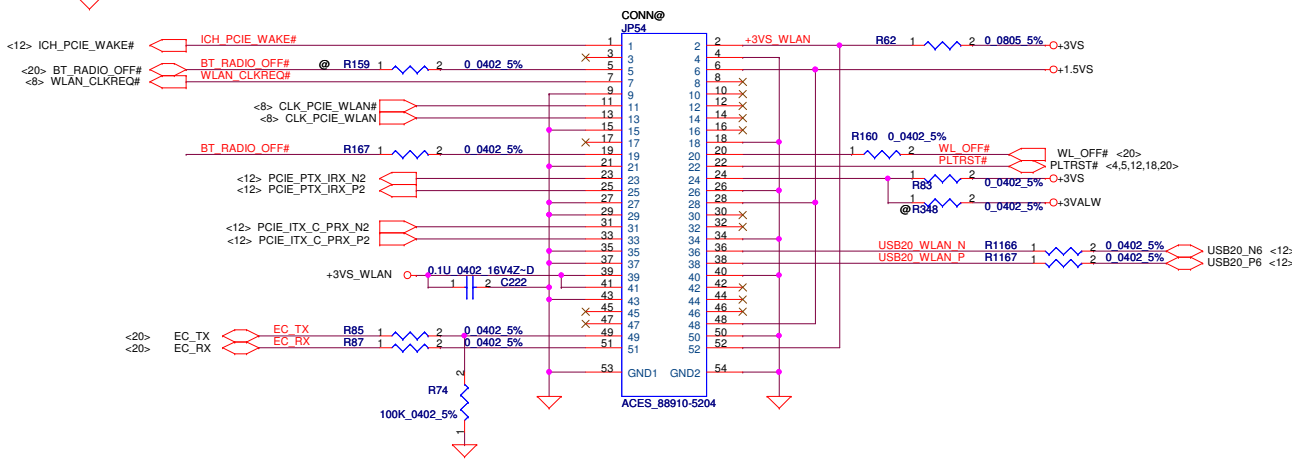
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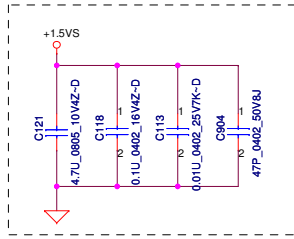
Compal Electronics, Inc.			
Title Tigerpoint(4/4)-Power_GND			
Size Custom	Document Number LA-6501P	Rev 0.2	
Date: Monday, May 10, 2010	Sheet 13	of 35	



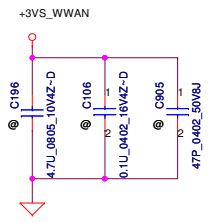
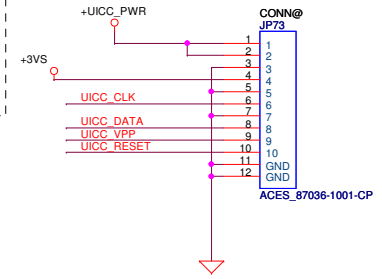
Mini-Express Card for WLAN



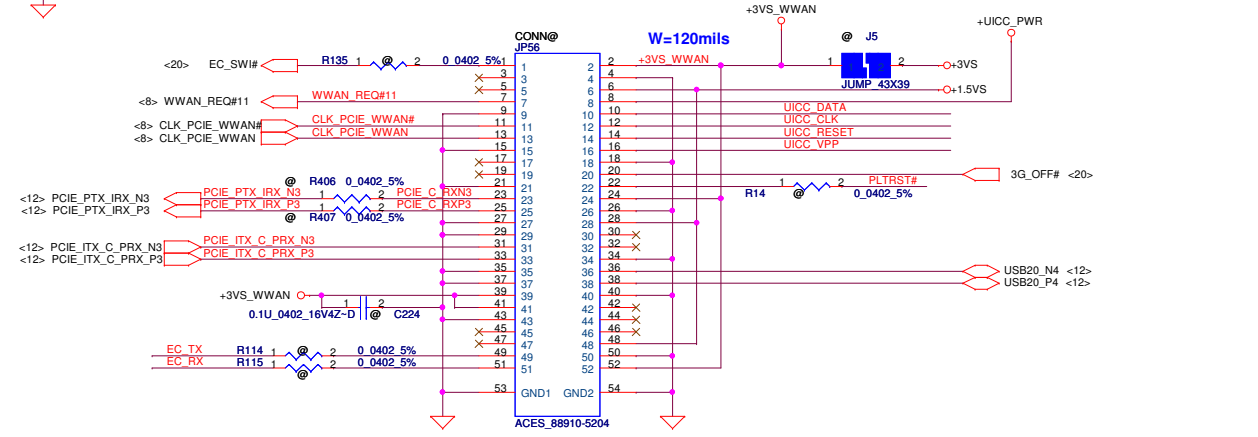
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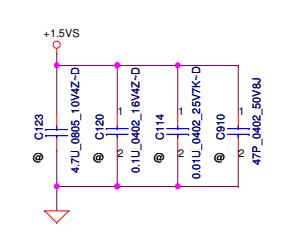
SIM Interface



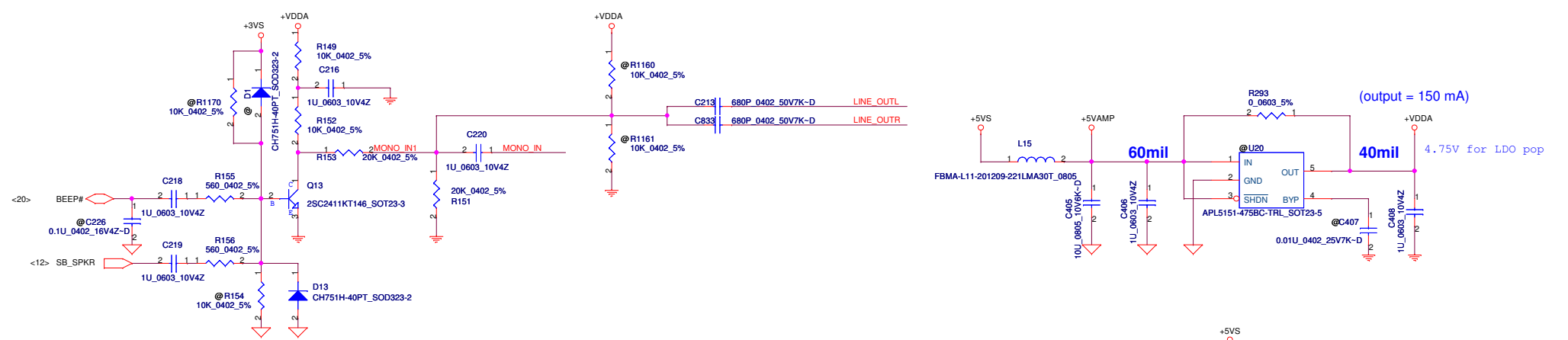
Mini-Express Card for WWAN



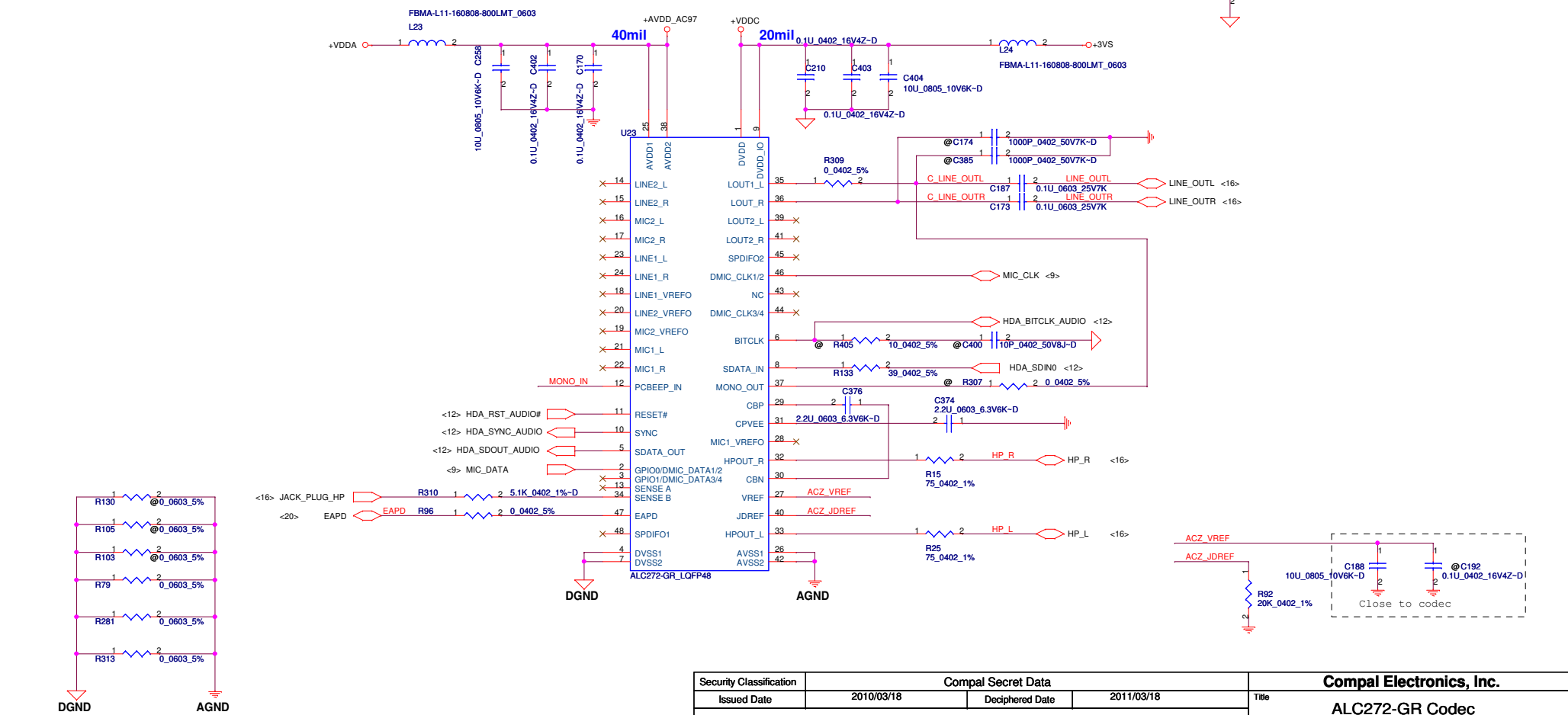
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Size	Document Number	LA-6501P		Rev	0.2
Date:	Friday, May 07, 2010	Sheet	14	of	35



HD Audio Codec



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				Custom	0.2
				Date: Friday, May 07, 2010	
				Sheet 15 of 35	

Compal Electronics, Inc.

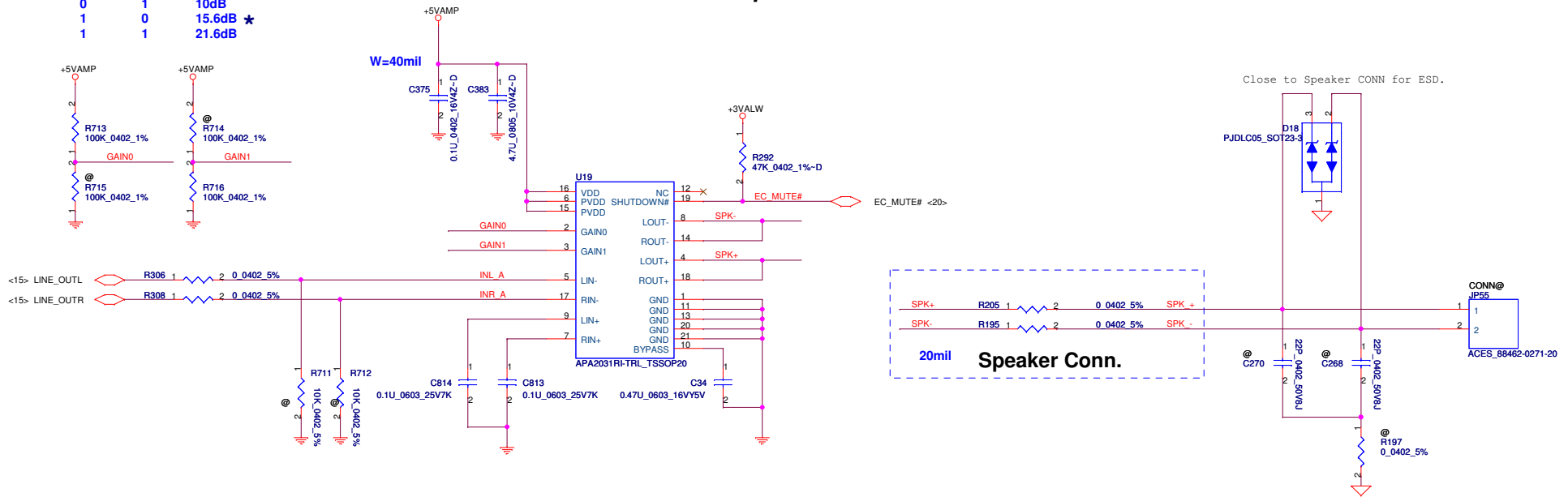
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LA-6501P

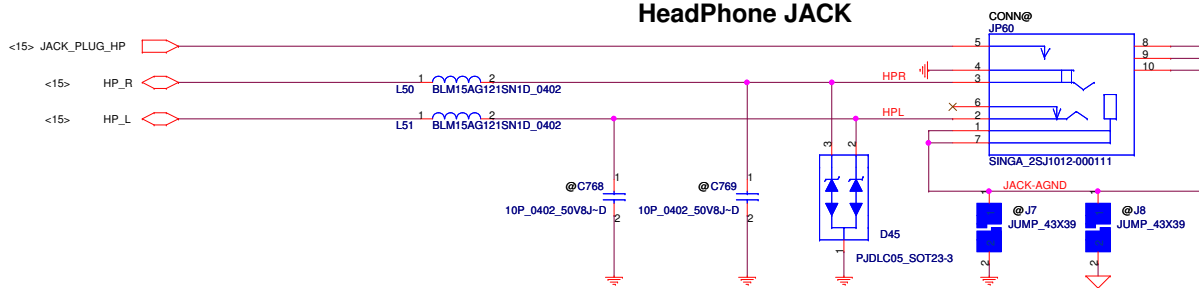
Friday, May 07, 2010

APA2031A SPK Amplifier

GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB *
1	1	21.6dB



HeadPhone JACK



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Size	Document Number	Rev		0.2
Custom	LA-6501P	Date:		Monday, May 10, 2010
Sheet		16 of 35		

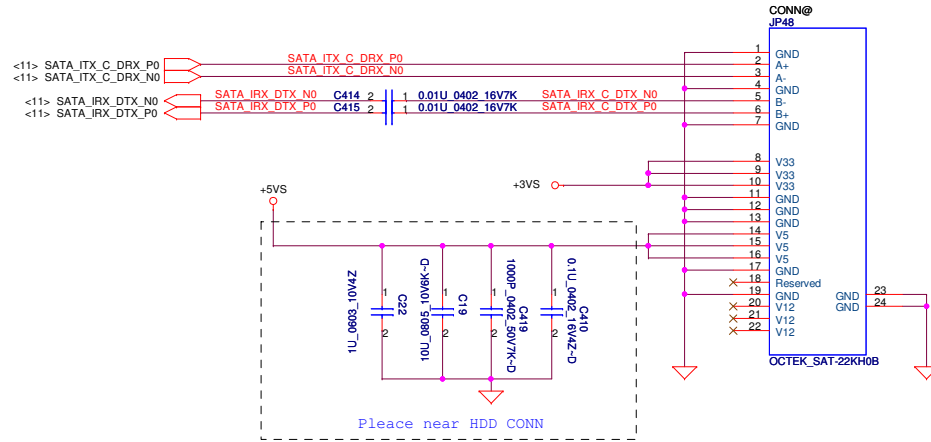
Compal Electronics, Inc.

Speaker/Audio Jack

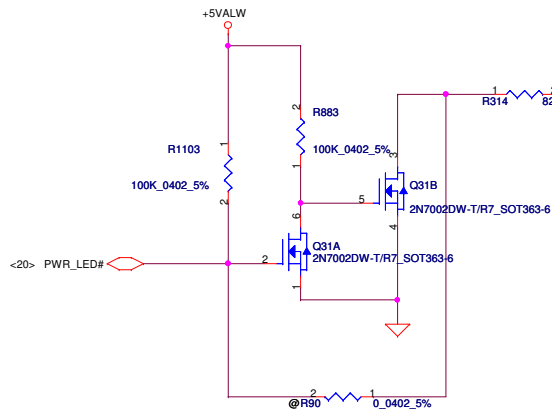
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Monday, May 10, 2010 Sheet 16 of 35

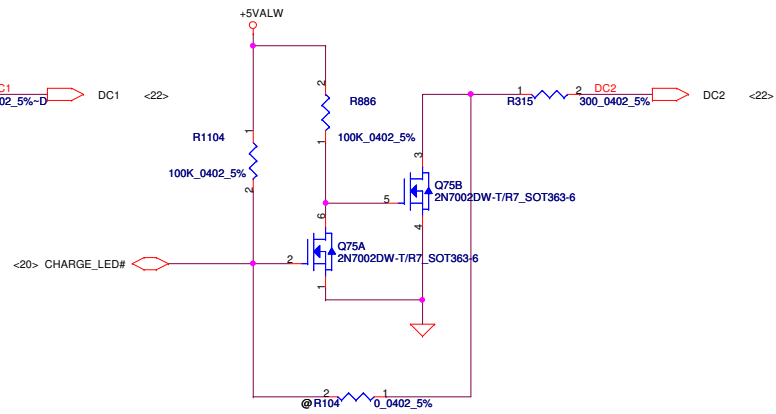
For SATA HDD



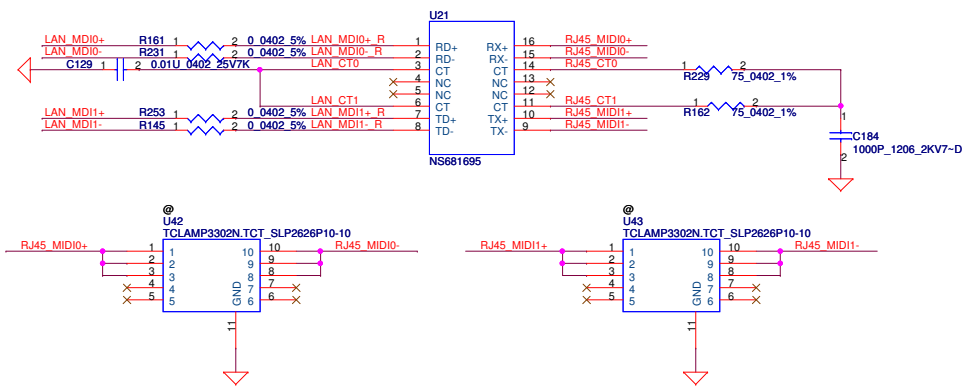
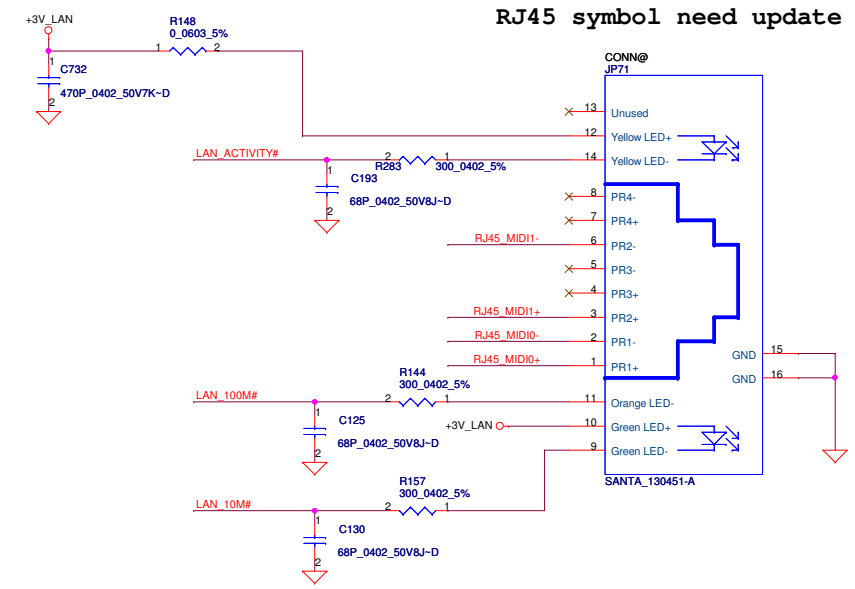
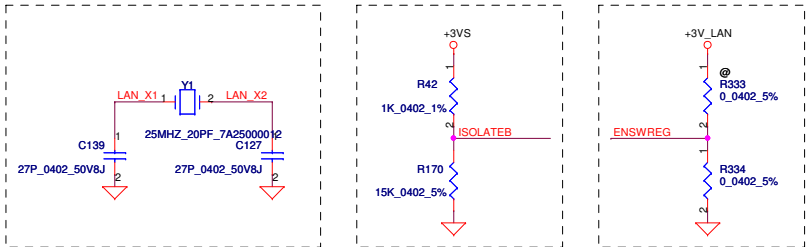
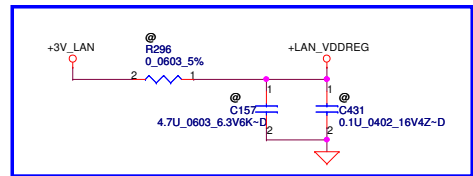
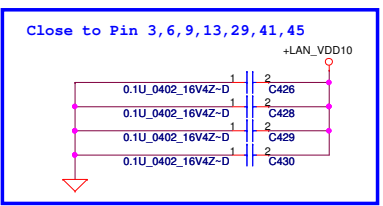
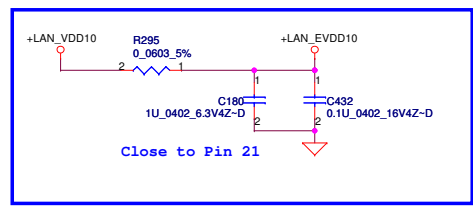
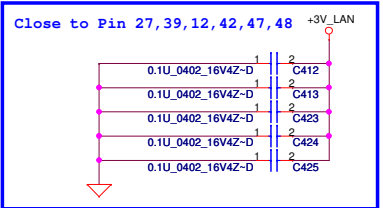
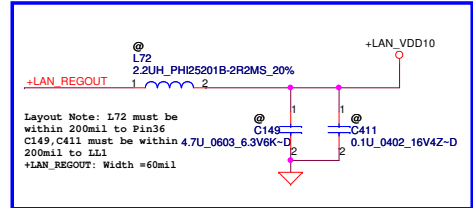
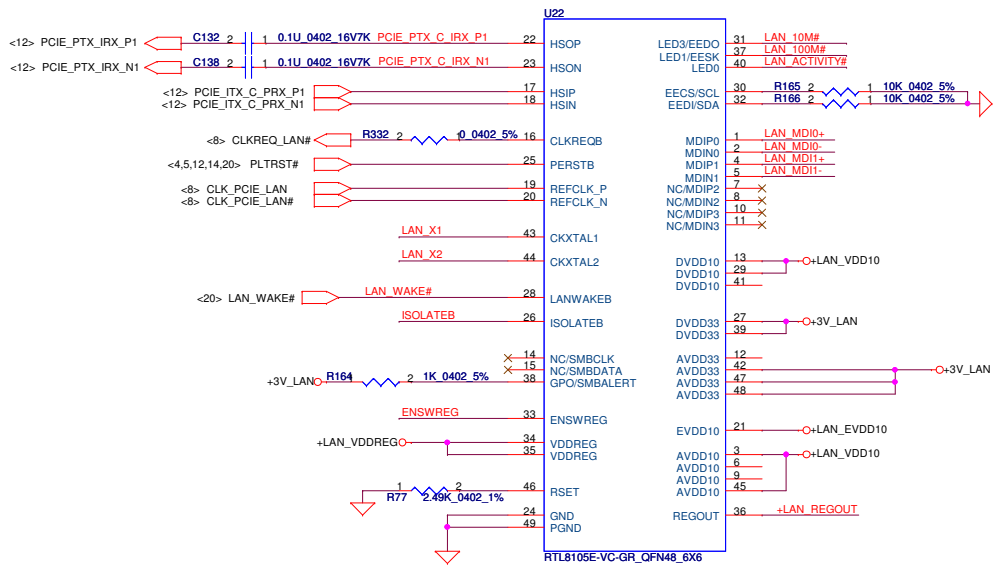
POWER LED



BATT CHARGE LED

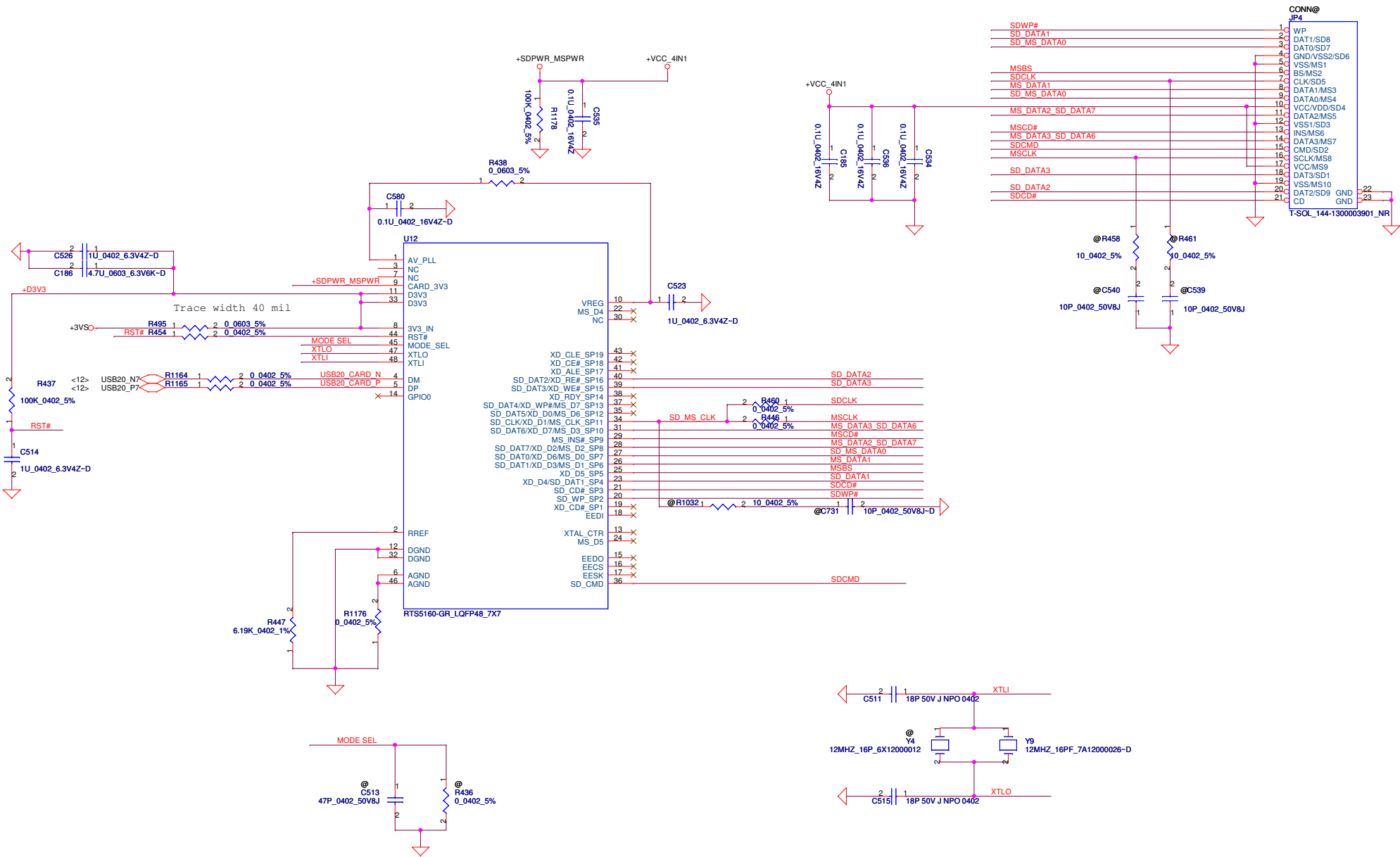


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				SATA/LED		
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				Custom	LA-6501P	0.2
				Date:	Monday, May 10, 2010	Sheet 17 of 35

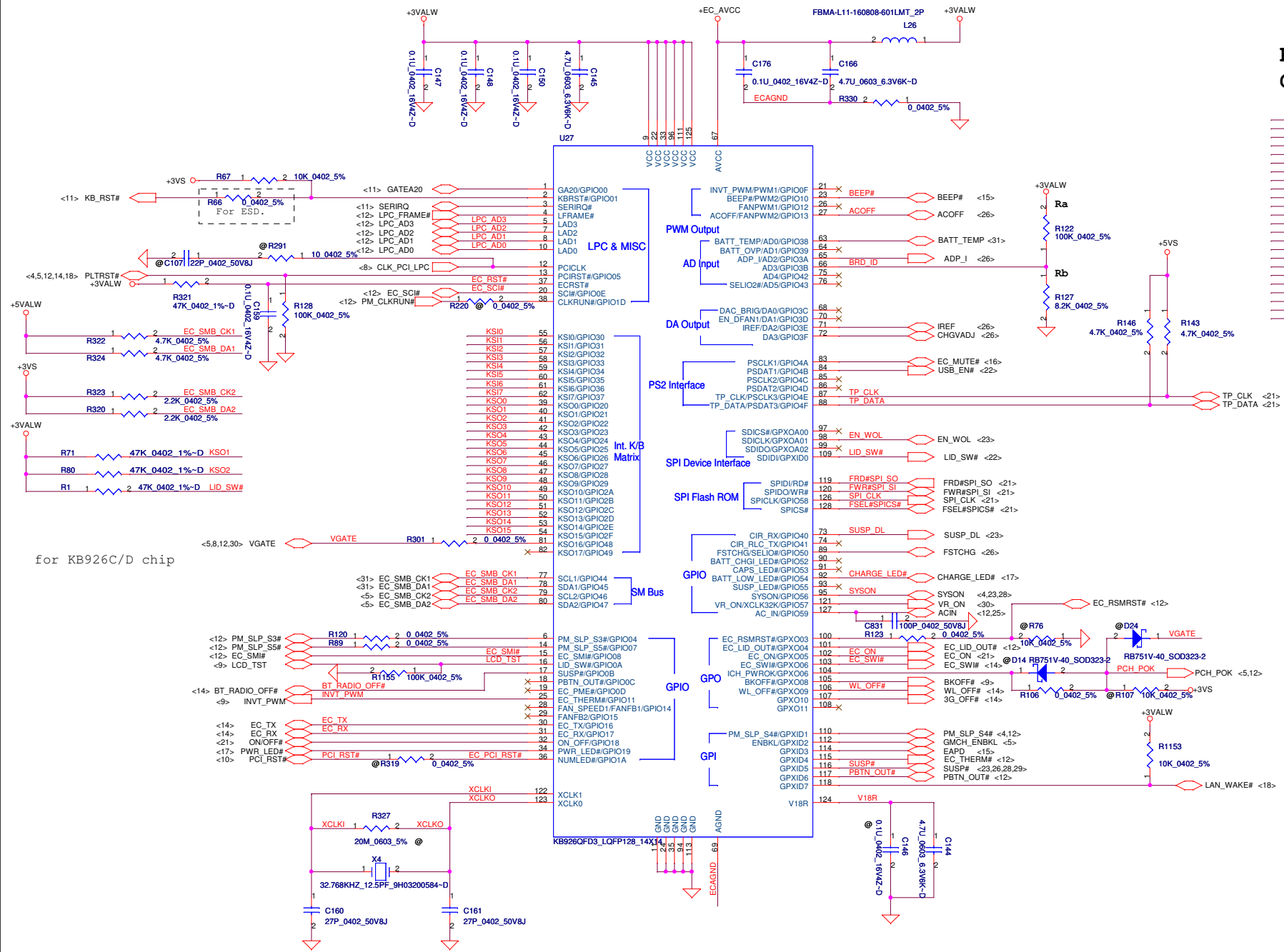


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Issued Date	2010/03/18	Deciphered Date	2011/03/18	Title		
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				Custom	LA-6501P	0.2
				Date:	Monday, May 10, 2010	Sheet 18 of 35

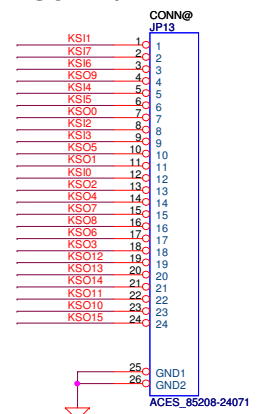
3 in 1 Card Reader



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Size	Document Number	Rev		
Custom	LA-6501P	0.2		
Date:	Monday, May 10, 2010	Sheet	19	of 35

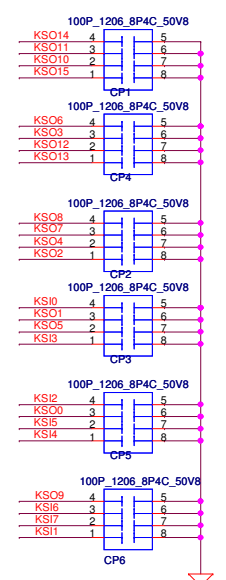


KEYBOARD CONN.



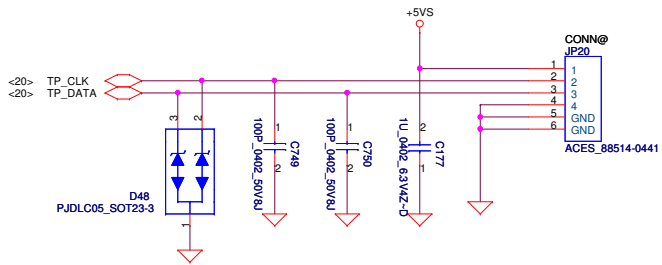
for KB926C/D chip

For EMI

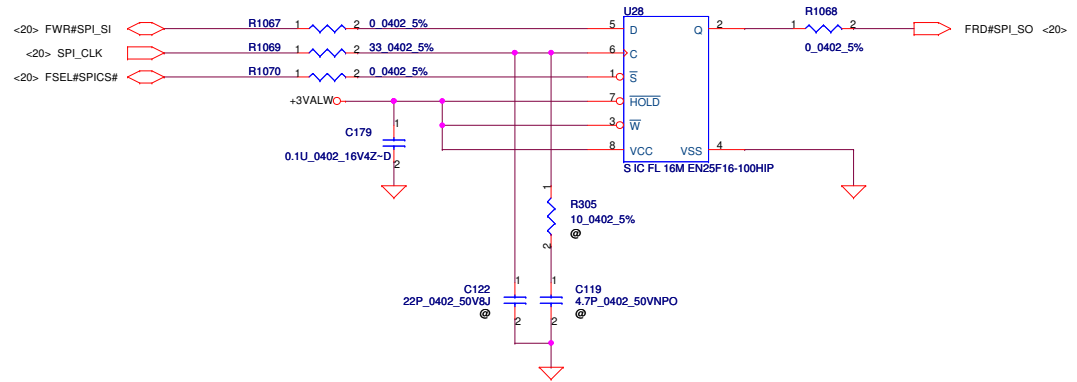


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Size		Document Number		Date		Friday, May 07, 2010		Sheet		20 of 35	
Customer		LA-6501P		Rev		0.2					

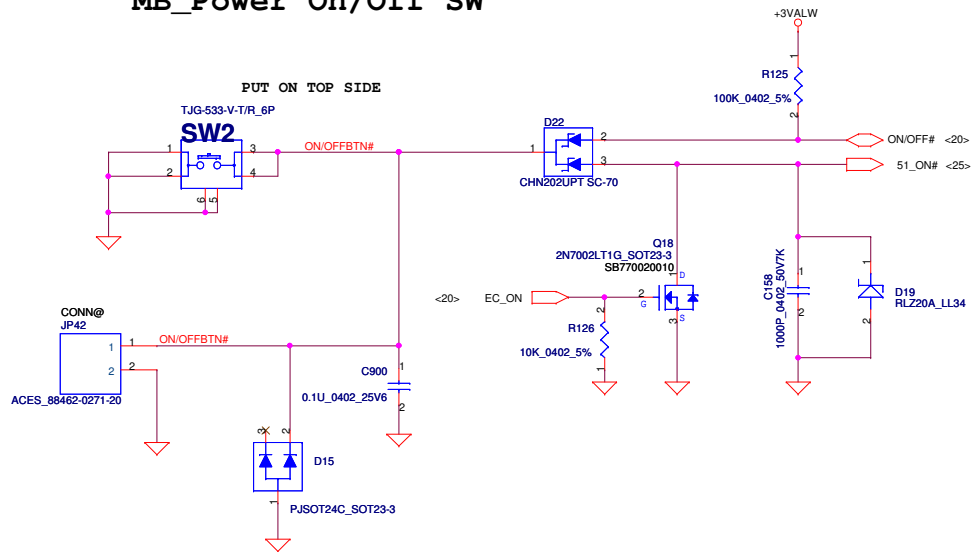
Touch/B Connector



System SPI Flash ROM (16Mb)

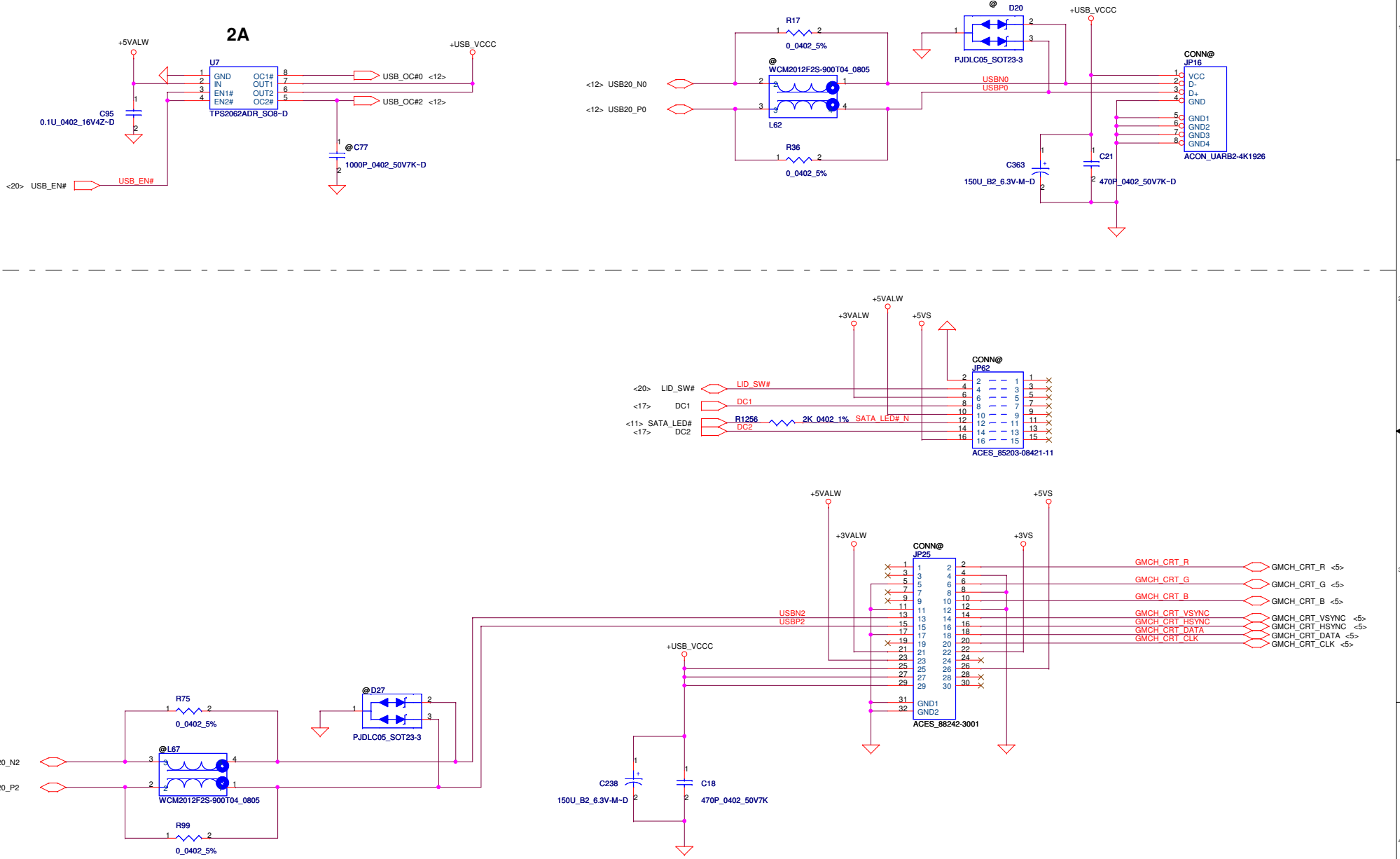


MB_Power On/Off SW



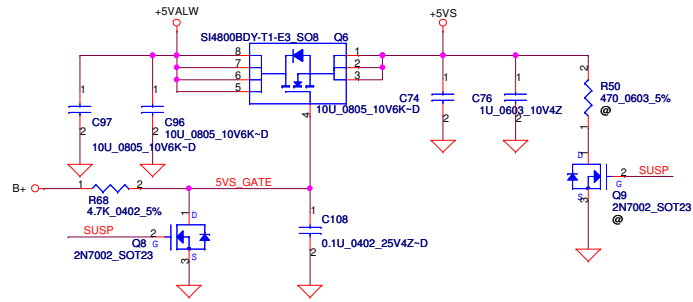
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				Size	Document Number	Rev
				Custom	LA-6501P	0.2
Date:	Monday, May 10, 2010	Sheet	21 of 35			

On Board USB Connector

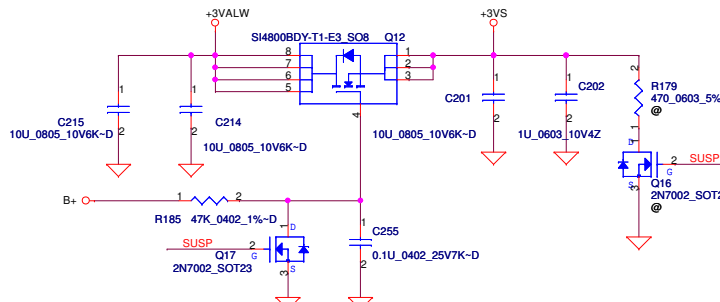


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				Size	Document Number
				LA-6501P	
				Date:	Friday, May 07, 2010
				Sheet	22 of 35

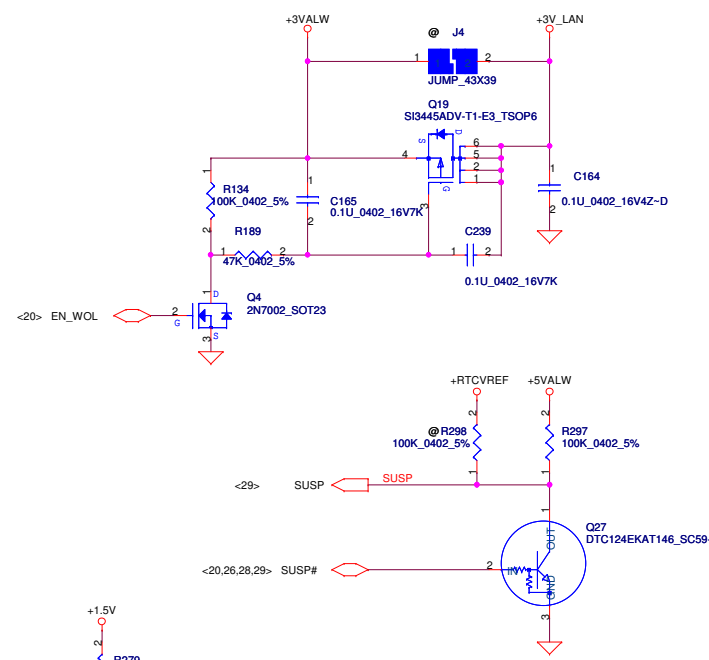
+5VALW TO +5VS



+3VALW TO +3VS

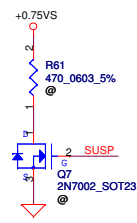
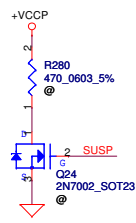
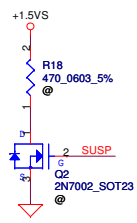
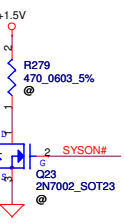
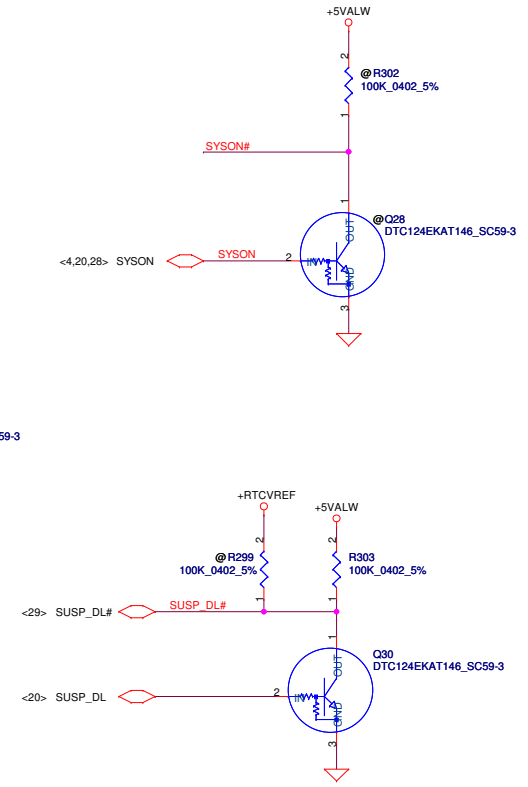
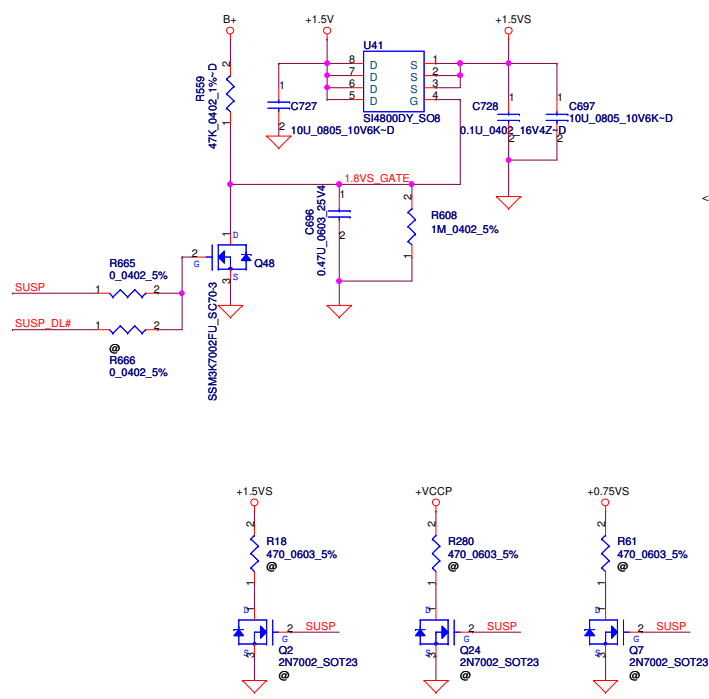


+3VALW to +3V_LAN

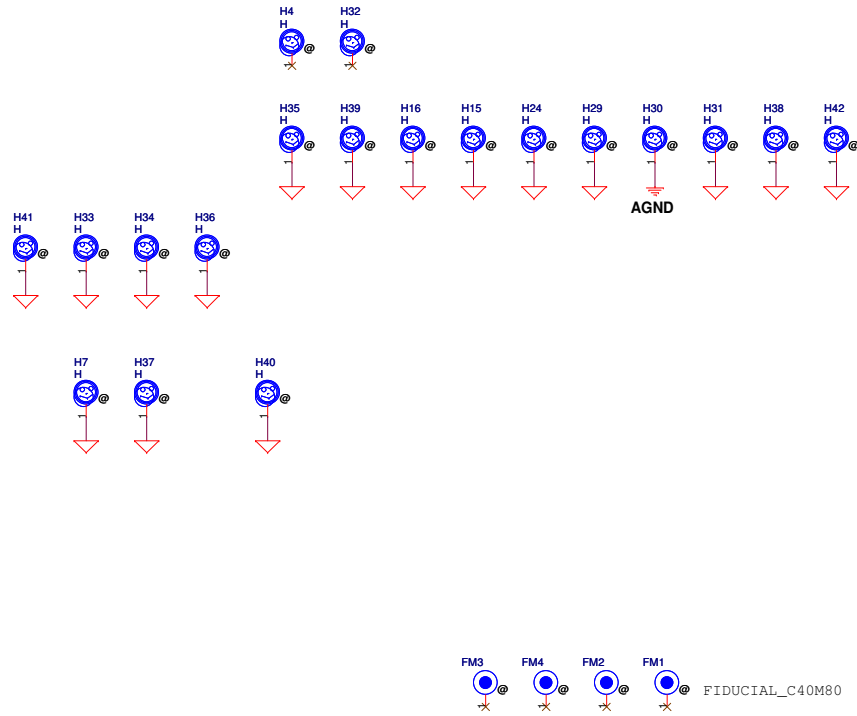


If the +1.5V discharge circuit is pop, R302, Q28 need pop.

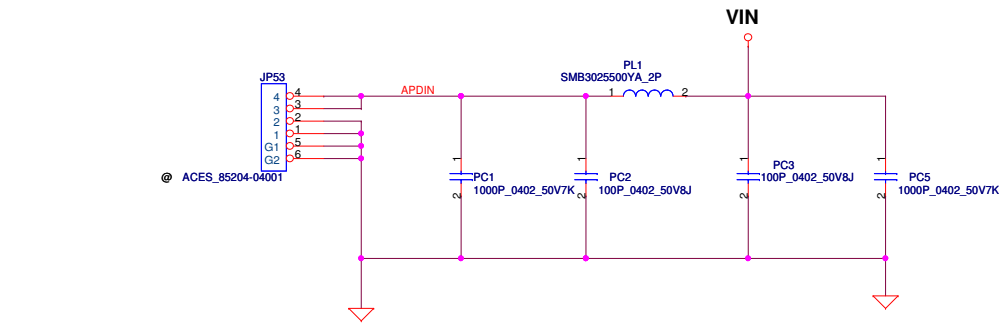
+1.5V to +1.5VS Transfer



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Size	Document Number	Rev		
Custom	LA-6501P	0.2		
Date:	Friday, May 07, 2010	Sheet	23	of 35

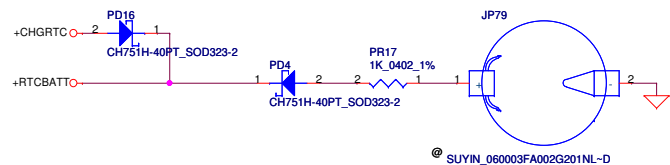
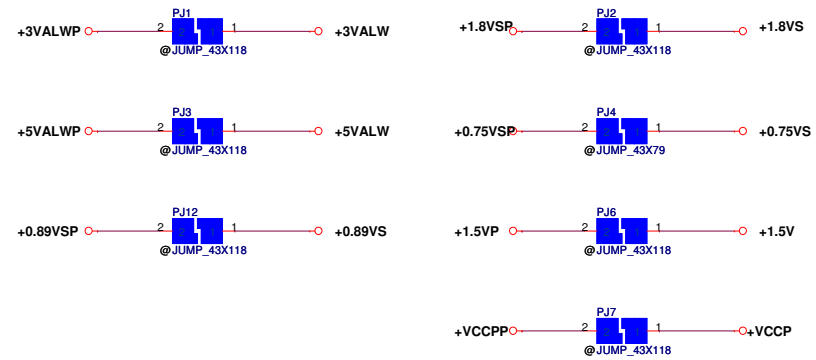
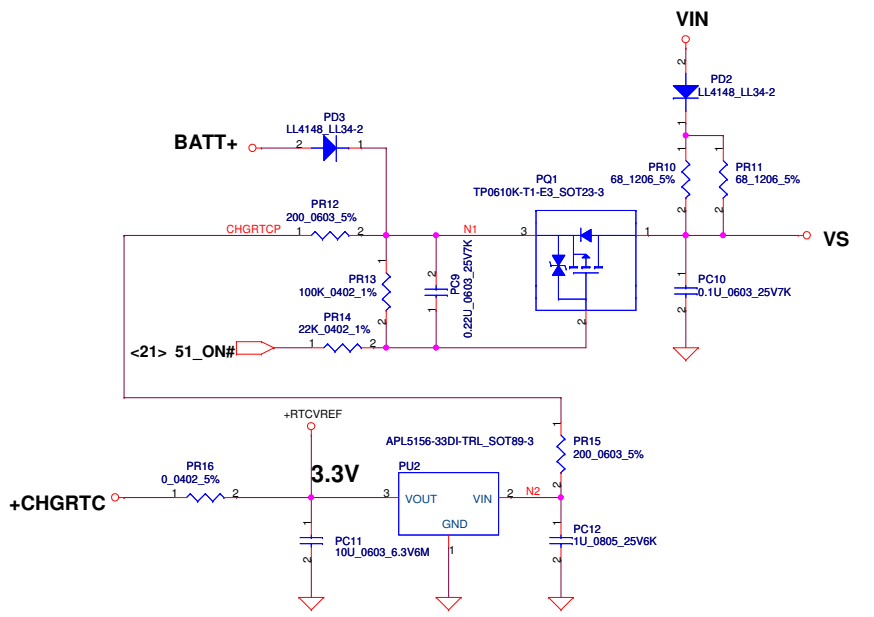
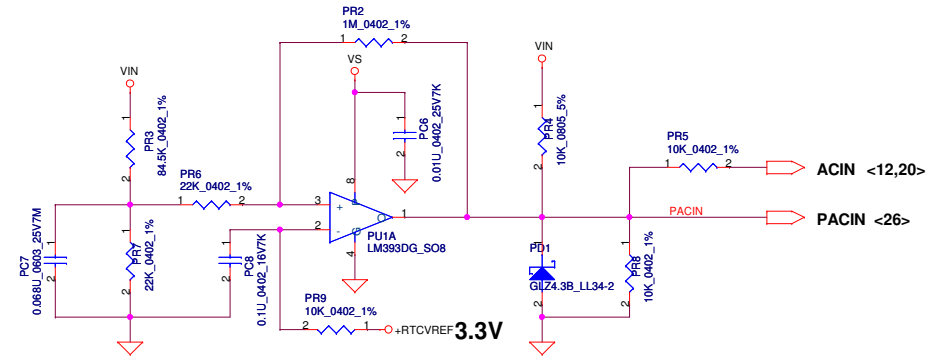


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			Custom	LA-6501P
			Date:	Tuesday, April 27, 2010
			Sheet	24 of 35
			Rev	0.2

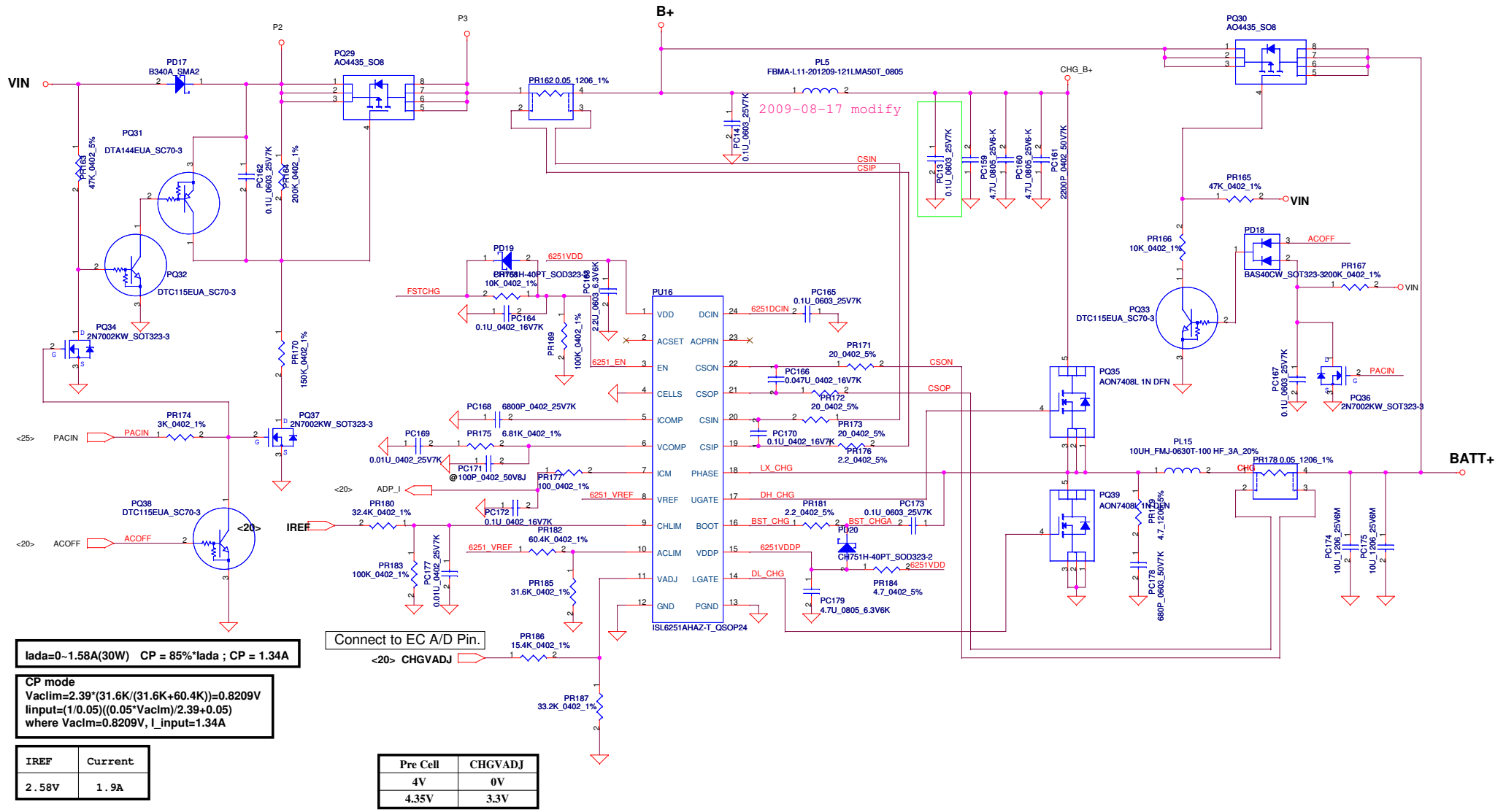


Vin Detector

High	17.944	17.706	17.470
Low	16.242	16.027	15.808



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Size	Custom	Document Number		Rev	0.2
Date:	Friday, May 07, 2010	Sheet	25	of	35



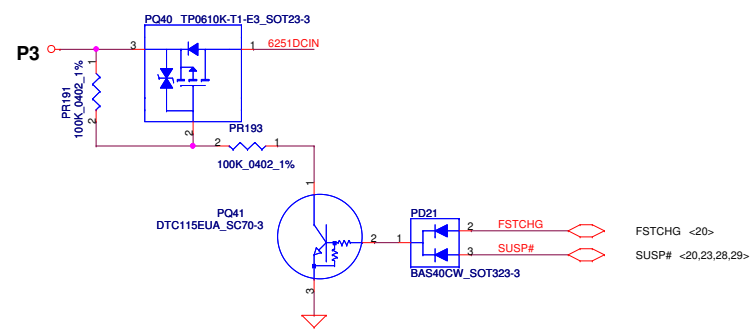
I_{ada} = 0 ~ 1.58A (30W) CP = 85% * I_{ada}; CP = 1.34A

CP mode
 Vac_{lim} = 2.39 * (31.6K / (31.6K + 60.4K)) = 0.8209V
 I_{input} = (1 / 0.05) * ((0.05 * Vac_{lim}) / (2.39 + 0.05))
 where Vac_{lim} = 0.8209V, I_{input} = 1.34A

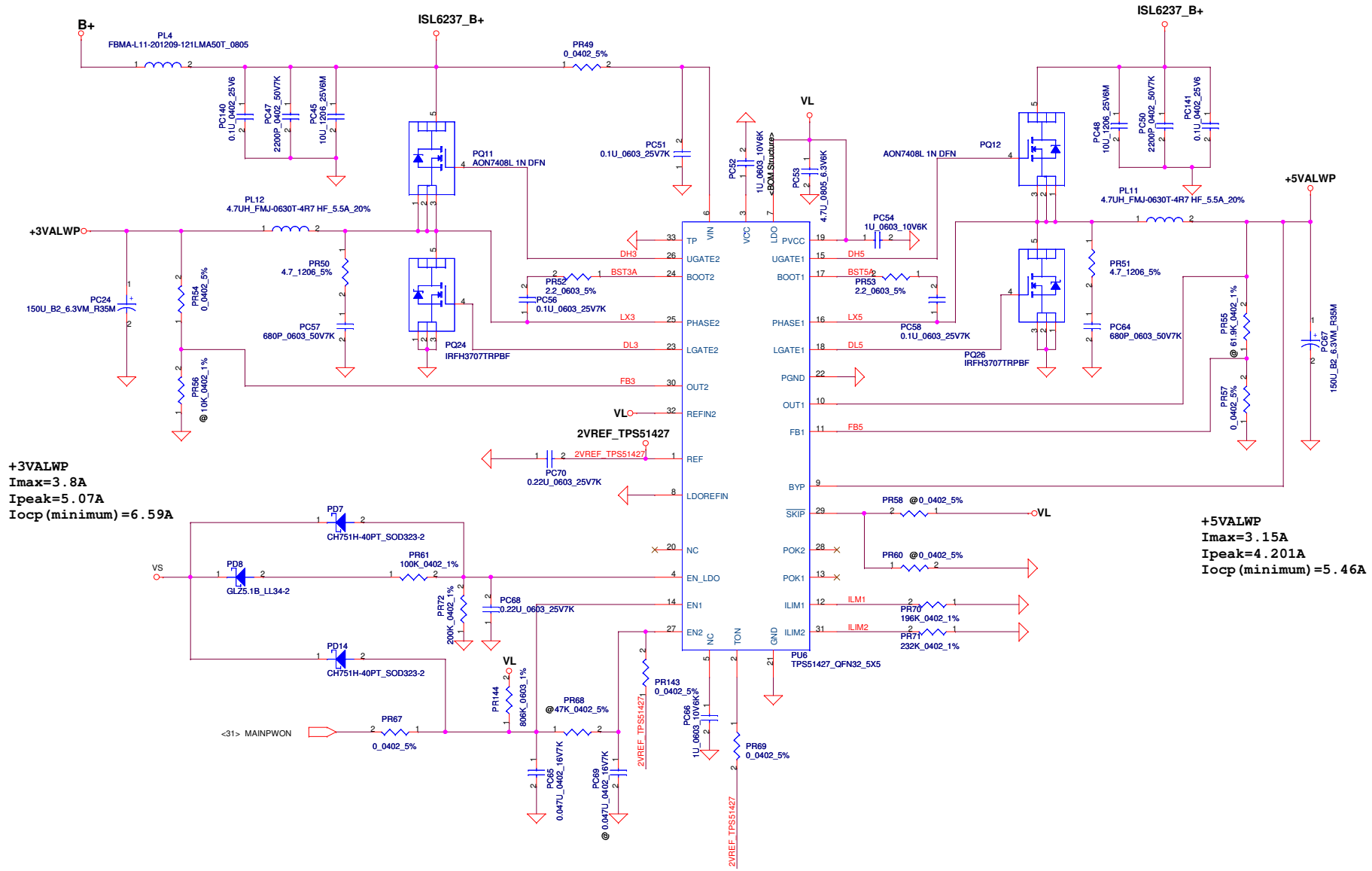
IREF	Current
2.58V	1.9A

Connect to EC A/D Pin.

Pre Cell	CHGVADJ
4V	0V
4.35V	3.3V



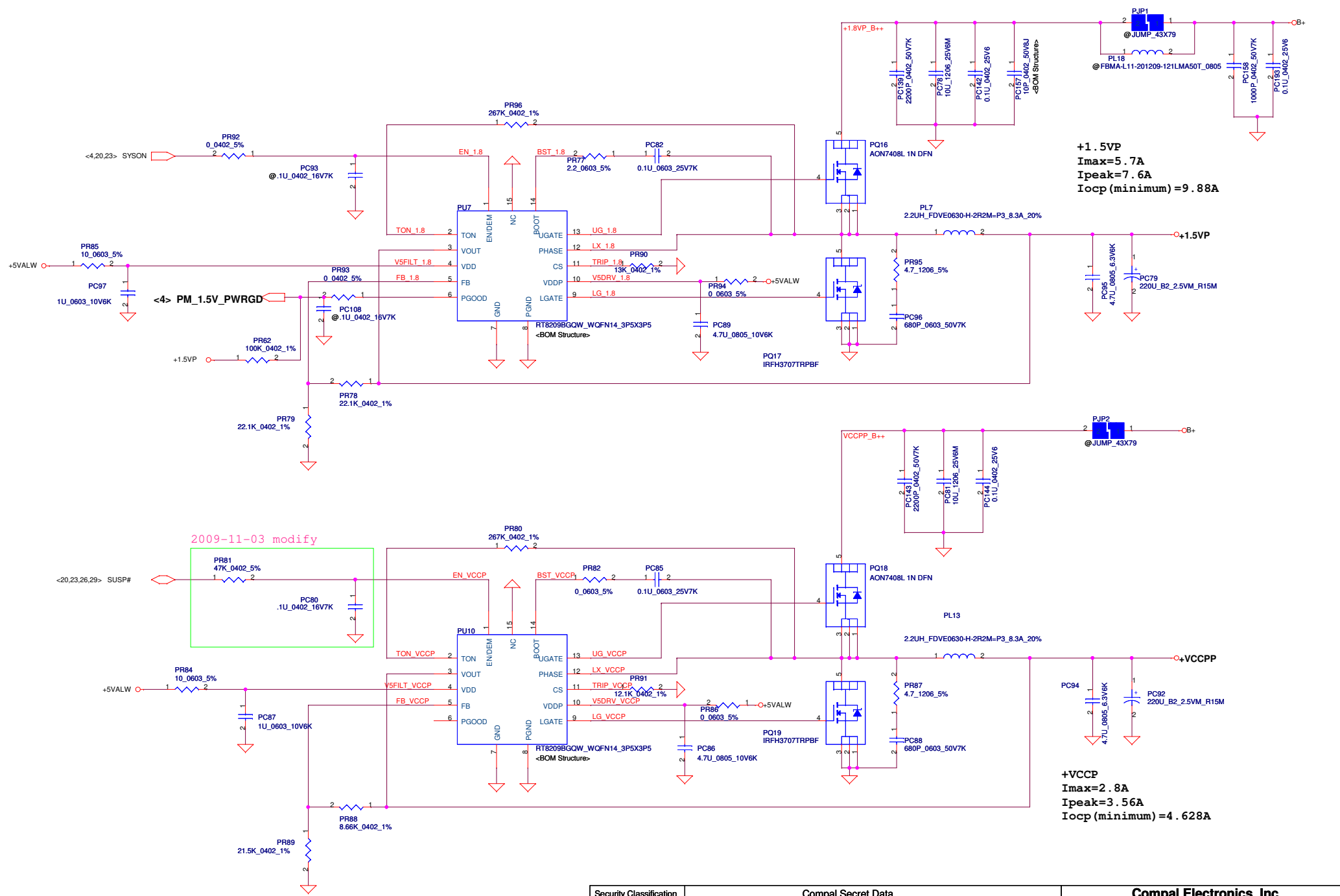
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Issued Date	2010/03/18	Deciphered Date	2011/03/18	Compal Electronics, Inc.
				CHARGER
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Date:	Friday, May 07, 2010	Sheet	26	of 35



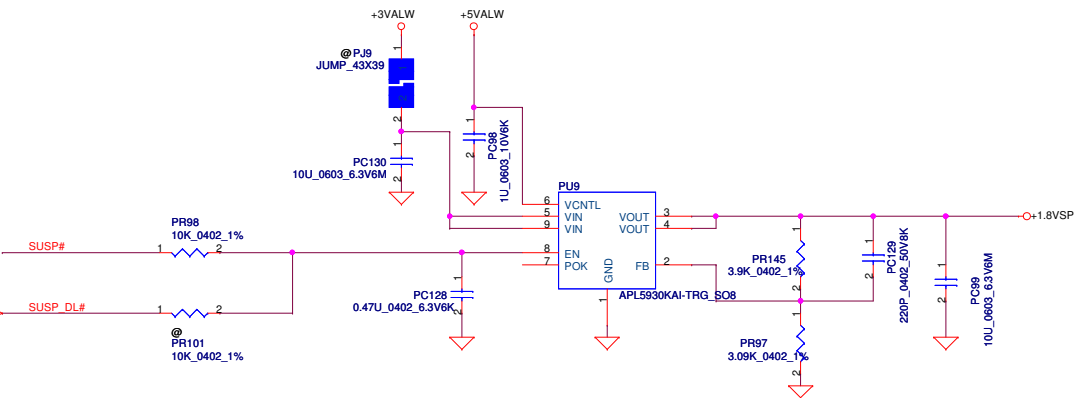
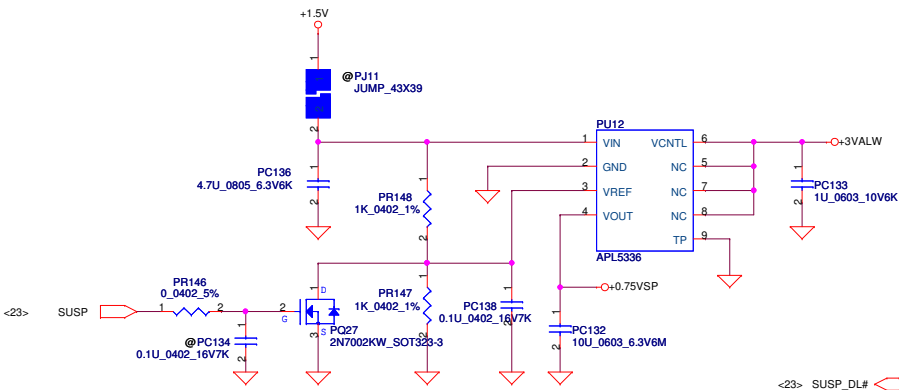
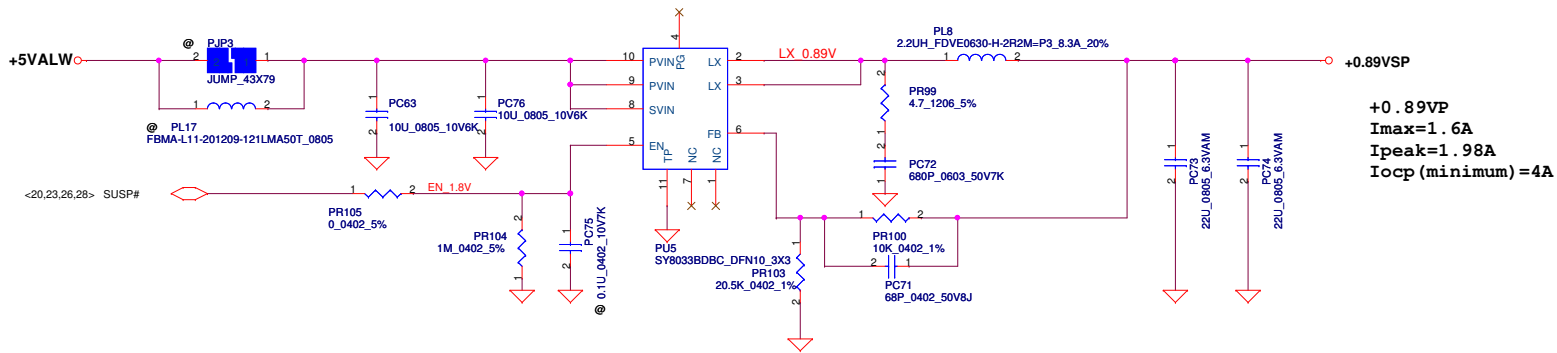
+3VALWP
 $I_{max}=3.8A$
 $I_{peak}=5.07A$
 $I_{ocp}(\text{minimum})=6.59A$

+5VALWP
 $I_{max}=3.15A$
 $I_{peak}=4.201A$
 $I_{ocp}(\text{minimum})=5.46A$

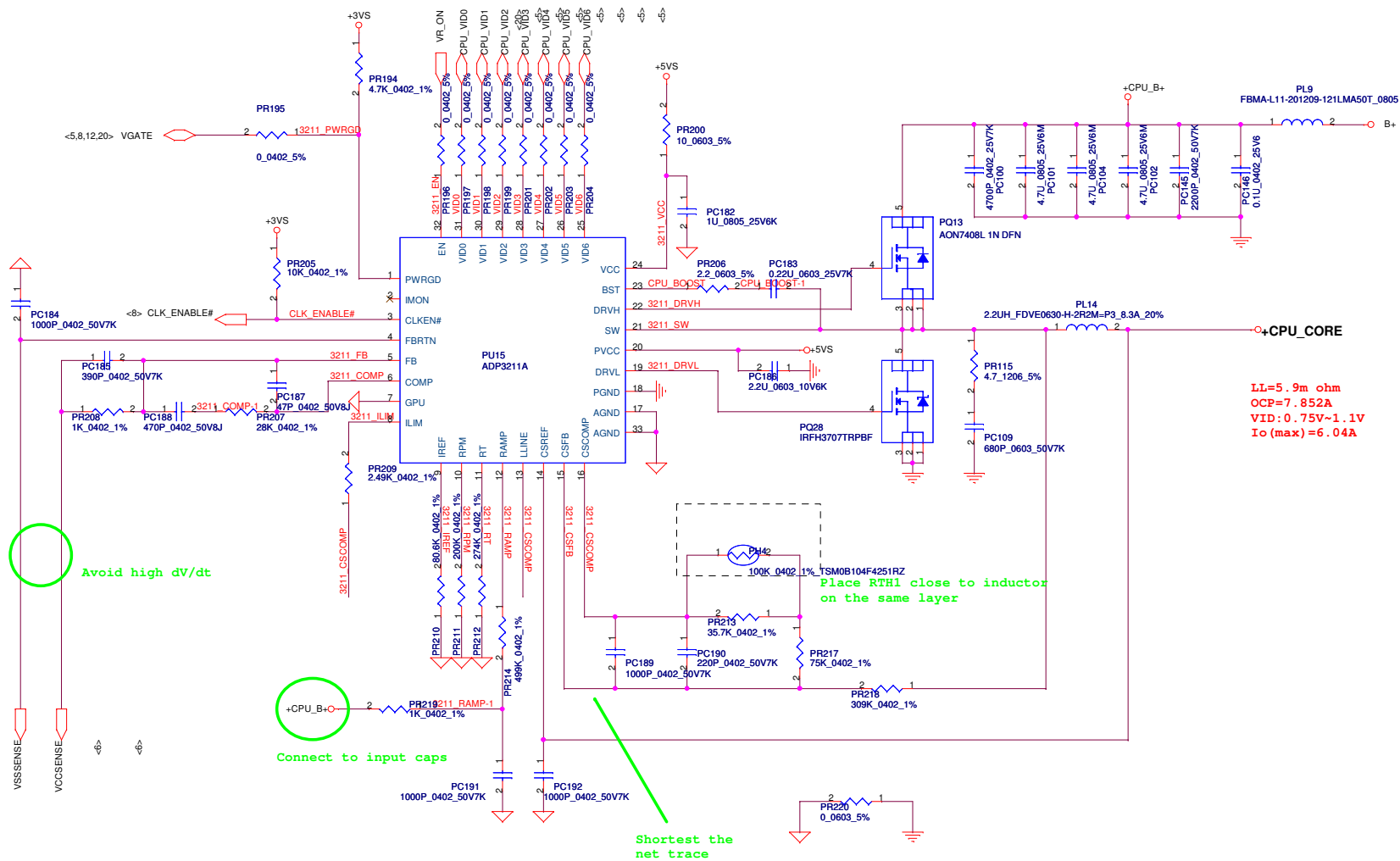
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Issued Date	2010/03/18	Deciphered Date	2011/03/18	
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Title	3VALW/5VALW			
Size	Document Number			Rev
Custom				0.2
Date:	Friday, May 07, 2010	Sheet	27	of 35



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Date:	Friday, May 07, 2010	Sheet	28	of	35

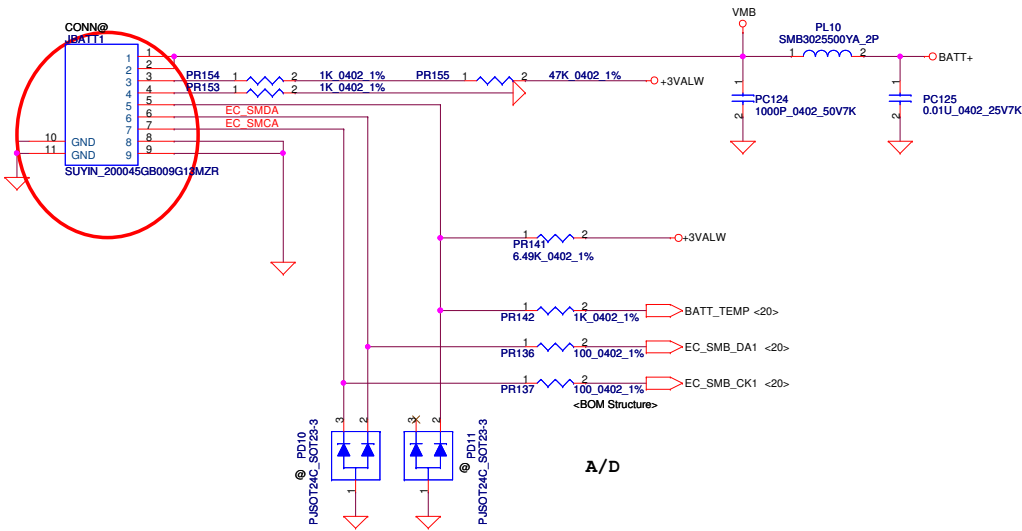


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Size	Document Number			Rev		
Custom				0.2		
Date:	Monday, May 10, 2010	Sheet	29	of 35		

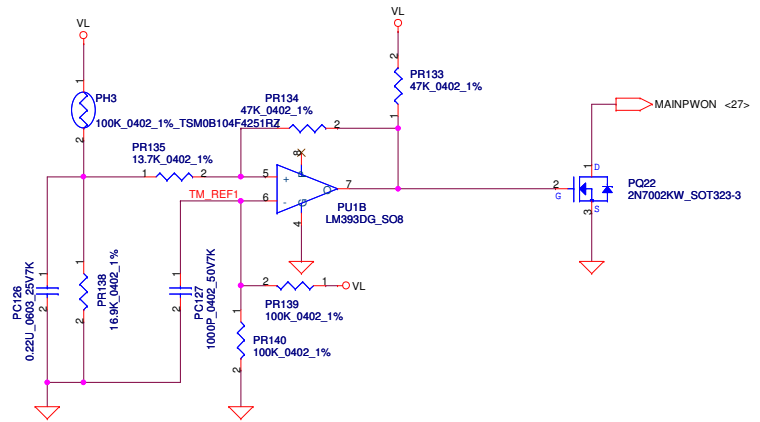


$LL=5.9m\ \text{ohm}$
 $OCP=7.852A$
 $VID: 0.75V\sim 1.1V$
 $I_o(\text{max})=6.04A$

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Size	Document Number			Rev	0.2
Custom				Date:	Friday, May 07, 2010
				Sheet	30 of 35



PH3 under CPU botten side :
 CPU thermal protection at 90 degree C
 Recovery at 50 degree C



A/D

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				Size	Document Number	0.2
				Date:	Friday, May 07, 2010	Sheet 31 of 35

Version change list (P.I.R. List)

Item	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Reserve bead to prevent noise issue happen		P27, P28	Reserve PL16, PL17, PL18	2009.07.24	PT
2	EMI request add snubber to reduce power board band.		P26, P27 P28, P29	Change PR77, PR206 to 2.2_0603_5%. Add PR87, PR95, PR50, PR51, PR115 4.7_1206_5% into BOM. Add PC88, PC96, PC57, PC64, PC109 680P_0603_50V. Add PC157 10P_0402_50V	2009.08.05	PT
3	Reserve 0.89V LDO soultion		P28	Reserve PU11, PC131, PC103, PC155, PC154, PC105 PR99, PR157, PR100	2009.08.05	PT
4	Adjust the +1.5VSP LDO feedback		P28	Change PC129 to 220P 25V K NPO 0402	2009.08.05	PT
5	For reduce trace space.		P30	Change JBATT1 pin3 & pin5 from +3VALWP to +3VALW.	2009.09.17	ST
6	Adjust the VCORE OCP		P30	Change PR209 to 2.49K_0402_1%	2009.09.17	ST
7	Adjust the +0.89VSP OCP		P28	Change PR160 to 5.9K_0402_1%	2009.09.17	ST
8	EMI request add snubber to reduce power board band.		P25, P28 P27	Add PR161, PR179 4.7_1206_5%. Add PC151, PC178 680P_0603_50V7K. Add PC13, PC14, PC193 0.1u_0603_25V Add PC158 1000p_0402_50v	2009.09.21	ST
9						
10						

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Date: Tuesday, April 27, 2010				Sheet 32 of 35		

Item	Date	Fixed Issue	Rev.	PG#	Modify List
01	2009/12/08	Flea chip on board	0.1	P.15	Add U42,U43 and U44
02	2009/12/08	Flea chip on board	0.1	P.14	Remove jp57,C401,C411,C409,C412,C135
03	2009/12/08	for FAN circuit	0.1	P.20 P.21	Add U3,JP14,C10,C427,C420,C418,C417,R47,R307,D6,D9;Connect U27 pin28 to JP14 pin2.
04	2009/12/09	7Beeps hang on ICH7 platform	0.1	P.08	Add R150
05	2009/12/09	BCM BT + WLAN combo	0.1	P.14	Remove jp22, C185, C186,R2,R116
06	2009/12/09	for thermal solution	0.1	P.14	Add U3, C10, C427,R2,JP14,D6,D9,C420,C418,R307,C417
07	2009/12/28	for standard pin define for PCIE MINI Card	0.1	P.14	Connect JP56 pin 6, 28, 48 to +1.5VS, reserve C123,C120,C114,C910.
08	2010/01/06	for DDRIII SODIMM design	0.1	P.4	U31 pin AL28,AJ26 pull high to +1.5V;Add C1102,C256;Connect U31 pin AB4 to PU7 pin 6.
09	2010/01/07	for Intel CRB schematic Rev.0.5	0.1	P.6	Change C928,C929,C930,C931 from 2.2uF to 1uF;Add C273 22uF;Change C379 from 0.1uF to 1uF.
10	2010/01/14	for ICS Low Power CLK Gen. Co-lay circuit	0.1	P.8	U11 pin62 pull high to +1.5VS / +1.05VS.
11	2010/01/14	for touch screen function	0.1	P.9 P.12	Connect JP24 pin 34,36 from USB20_P6/N6 to USB20_P5/N5;Pop R1168 and R1169.
12	2010/01/14	for +1.5VS transfer circuit	0.1	P.23	Connect U41 pin 5,6,7,8 to +1.5V;pin 1,2 to +1.5VS
13	2010/01/14	Change crystal package size	0.1	P.8,12, 19,20	Co-lay Y8 and Y5,change Y1,Y6,Y4 to small size package.
14	2010/01/19	for Intel checklist Rev. 2.0	0.1	P.6	Reserve C401,C409 close to U31.AA19,de-pop C925
15	2010/01/19	for Intel CRB DRAM POWEROK circuit	0.1	P.4	Add U45,R158,R142,R294,R93,R136,R1188,C78,C178
16	2010/01/21	for POWER concern to Delete BATT_OVP circuit	0.1	P.20	Disconnect U27.64
17	2010/01/27	for WLAN+BT module card design	0.1	P.14	Add R159,R160 close to JP54 pin5 and pin20.
18	2010/01/28	for EC team concern	0.1	P.14	Add R74 close to JP54 pin49.
19	2010/01/29	for Broadcom check request	0.1	P.15	Connect U42 pin D11 directly to GND.
20	2010/01/29	for Broadcom check request	0.1	P.15	Add test points on U42 pin M8 and M9.
21	2010/01/29	for Broadcom check request	0.1	P.15	Change L68,L69 to TDK MMZ2012R601AT.
22	2010/01/29	for Broadcom check request	0.1	P.15	Change C1082 and C1083 from 15pF to 18pF;change Y7 from 7M27100019 to 7M27070004.
23	2010/02/04	for power sequence	0.1	P.04	Connect U45 pin5 to SYSON.
24	2010/02/26	for RF concern	0.1	P.08	Pop C832 and C392.
25	2010/02/26	for Power sequence	0.1	P.23 P.29	Change C696 from 0.01uF to 0.47uF;Pop PC128,PC176;Change PR98 to 10K, PR101 to 4.7K.

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				Custom	LA-6501P	0.2
				Date:	Tuesday, April 27, 2010	Sheet 33 of 35

Item	Date	Fixed Issue	Rev.	PG#	Modify List
26	2010/03/12	Change LAN IC	0.1	P.19	Change U22 from RTL8103EL-VB-GR to RTL8105E-VB-GR.
27	2010/03/16	For vender Realtek request	0.1	P.20	Change R1153 from 100K to 10K.
28	2010/03/18	Change +3V_LAN rising time > lms	0.1	P.23	Add C239,C165,C164,Q19,Q4,R134,R189 and de-pop J4
29	2010/03/22	Change KB926 GPIO definition	0.1	P.20	Change BT_RADIO_OFF# from pin108 to pin17
30	2010/03/22	Add card reader IC RTS5160-GR to MB	0.1	P.20	Add U12 card reader IC RTS5160-GR
31	2010/03/23	For vender Realtek request	0.1	P.19	Change U22 Pin 12,6,9,41 to NC;connect Pin 3,6 to together after via one 0.01uF cap. to GND;change C139, C127 to 27P.
32	2010/03/24	For EC team request	0.1	P.21	Pin38 net PM_CLKRUN# BOM @ 0ohm
33	2010/03/24	For EC team request	0.1	P.12	PCH pin AC19 net PM_CLKRUN# pull low 10K ohm
34	2010/03/25	Changer FLEA card DDR3 to DDR2 for cost	0.1	P.15	Change from K4B1G1646E-HCF8 to W9751G6IB-25
35	2010/03/26	Changer USB connector	0.1	P.23	Change JP16 from SUYIN_020133MR004S536ZR to ACON_UARB2-4K1926
36	2010/03/29	Broadcom request pull up GPIO_06 to 3V_BCM	0.1	P.15	Change U43 GPIO_06 pull up to +3V_BCM
36	2010/03/30	For speaker change from 2 to 1	0.1	P.17	Change JP55 from 4 pins to 2 pins
37	2010/04/15	For BOM error	0.2	P.19	Add C535 for BOM error
38	2010/04/15	For BOM error	0.2	P.23	Add R189,Q4 for BOM error
39	2010/04/15	For EC team request add 100K pull low	0.2	P.25	Add R128 pull low for EC
40	2010/04/15	For wake on LAN control net name error	0.2	P.20	Change KB926 pin98 net name from EN_WOL# to EN_WOL
41	2010/04/15	Change LAN RTL8105 to SWR mode	0.2	P.18	BOM @ L72,C149,C411,R296,C157,C431
42	2010/04/15	Change LAN ENSWREQ pin to pull Low	0.2	P.18	Delete R333 and Mount R334
43	2010/04/15	Change BOM from SD02800008L to SD028000080	0.2	P.20	Change R127,R284,R286,R287,R288 CPN
44	2010/04/16	Change BOM from SE070104Z80 to SE070104Z8L	0.2	P.19	Change C185,C534,C536 CPN
45	2010/04/16	Change BOM from SE074102K8L to SE074102K80	0.2	P.17	Change C419 CPN
46	2010/04/16	Change BOM from SE076104K80 to SE076104K8L	0.2	P.17	Change C132,C138,C165,C239 CPN
47	2010/04/16	Add net BT_RADIO_OFF# for JP54 pin19	0.2	P.14	Add R167 0 ohm for net BT_RADIO_OFF#
48	2010/04/21	Change MB ID to R02	0.2	P.20	Change R122 to 100K ohm and R127 to 8.2K ohm
49	2010/04/21	Modify BOM @ parts	0.2	P.09	BOM @ R1168,R1169,R41,R43
50	2010/04/21	Change BOM parts	0.2	P.10	Change U34 from SA000039N2L to SA000039N3L

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				Size	Document Number	0.2
				Custom	LA-6501P	
				Date:	Monday, May 10, 2010	Sheet 34 of 35

Version change list (P.I.R. List)

Item	Date	Fixed Issue	Rev.	PG#	Modify List
51	2010/04/21	Change BOM parts	0.2	P.23	Change Q4,Q8,Q17 from SB570020110 to SB000008J00
52	2010/04/21	Change BOM parts	0.2	P.21	Change D19 from SC45248B010 to SC400001100
53	2010/04/21	Change BOM parts	0.2	P.07	Change C1117,C1124 from SE049225Z8L to SE107225K8L
54	2010/04/21	Change LAN chip from ver.B to ver.C	0.2	P.18	Change U22 from SA00003PO10 to SA00003PO20
55	2010/04/21	Delete external MIC function	0.2	P.16	Delete JP61
56	2010/04/27	Delete touch panel function	0.2	P.12	Delete USB port5 nets
57	2010/04/27	Delete fan function	0.2	P.21	Delete JP14
58	2010/04/27	Delete USB port function	0.2	P.12	Delete USB port1 nets
59	2010/04/27	Change camera voltage from +5VALW to +3VS	0.2	P.09	Change R35 pin1 to +3VS
60	2010/04/29	Change BOM for EOL parts	0.2	P.23	Change Q2,Q7,Q9,Q16,Q23,Q24 from SB570020110 to SB000009080 or SB000008J00
61	2010/04/29	Change BOM for EOL parts	0.2	P.12	Change X4 from SJ100005L0L to SJ10000B500
62	2010/04/29	Change BOM for EOL parts	0.2	P.21	Change U28 from SA00002TO00 to SA00002KI00
63	2010/05/06	Delete U14 for just two USB ports	0.2	P.22	Delete U14 and +USB_RIGHT,+USB_LEFT change to +USB_VCC
64	2010/05/06	Change parts package	0.2	P.35	Change U45(BC847BS) to Q83,Q84(MMBT3904)
65	2010/05/06	Change amplifier gain from 10dB to 15.6dB	0.2	P.16	BOM @ R714,R715 and mount R713,R716
66	2010/05/06	Add ESD solution for EMI	0.2	P.18	Add U42,U43 to RJ45 connector
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				Custom	LA-6501P	0.2
Date: Friday, May 07, 2010				Sheet 35 of 35		

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