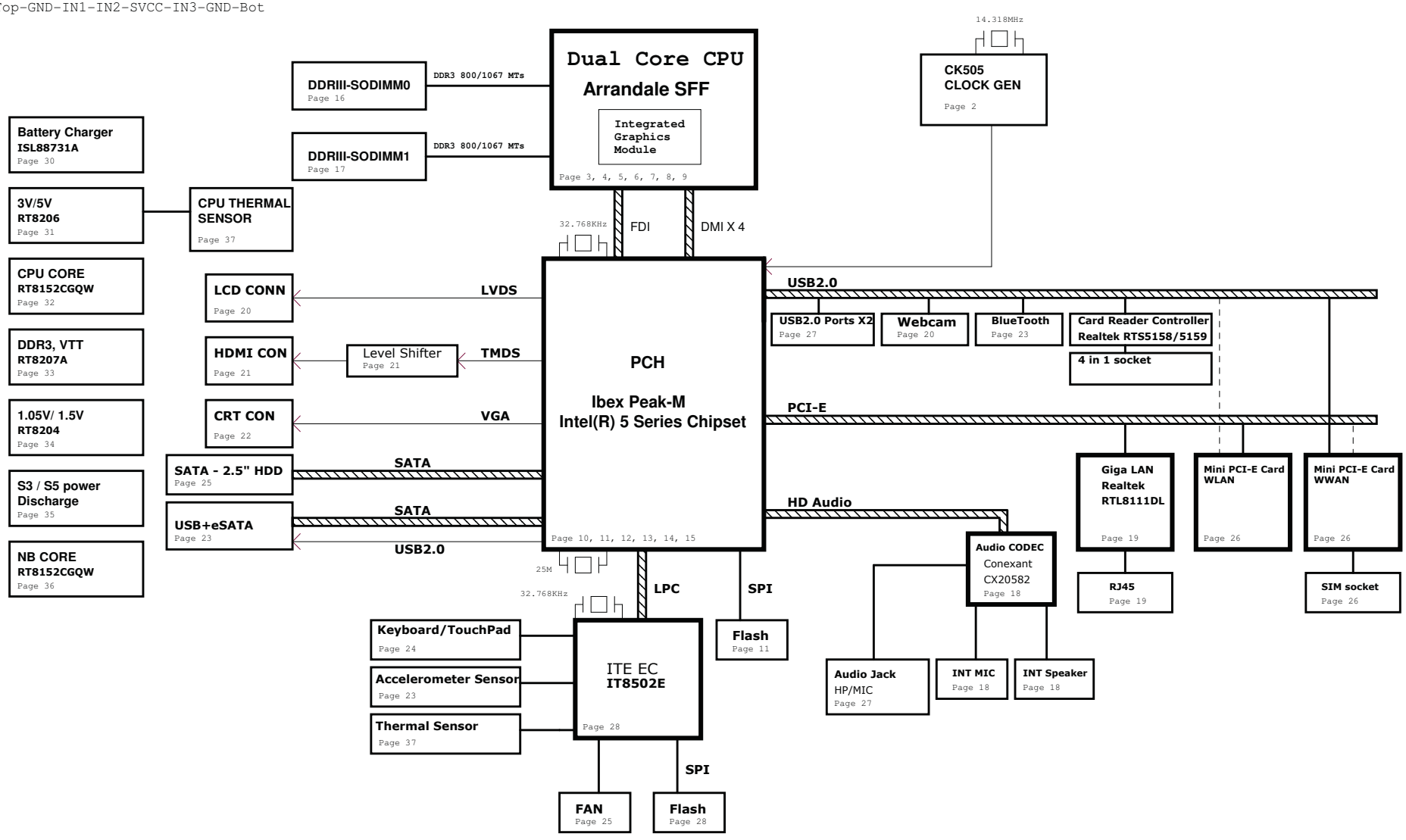
PCB STACK UP

8L

Top-GND-IN1-IN2-SVCC-IN3-GND-Bot

PS-Note, CULV BLOCK DIAGRAM

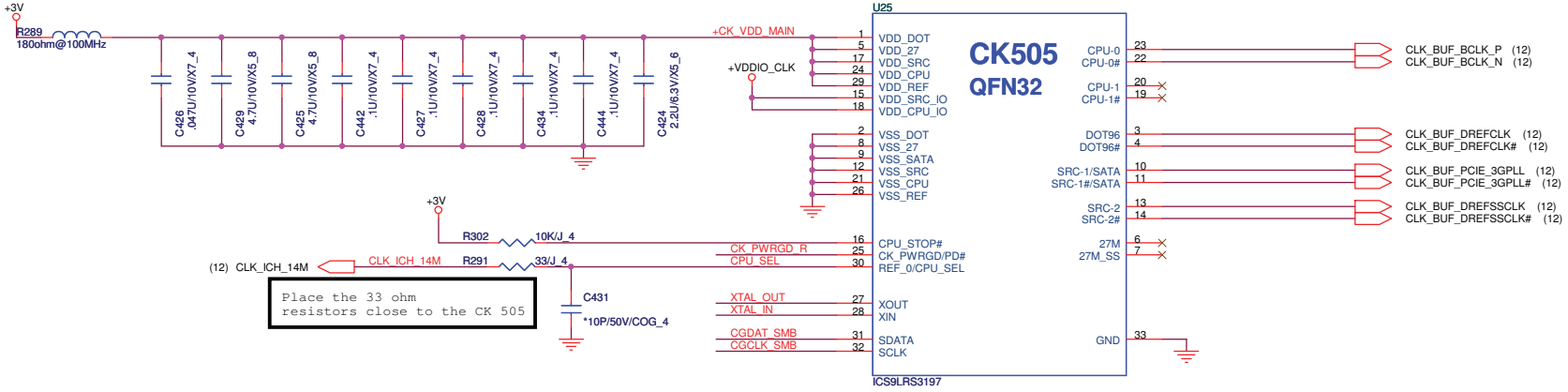


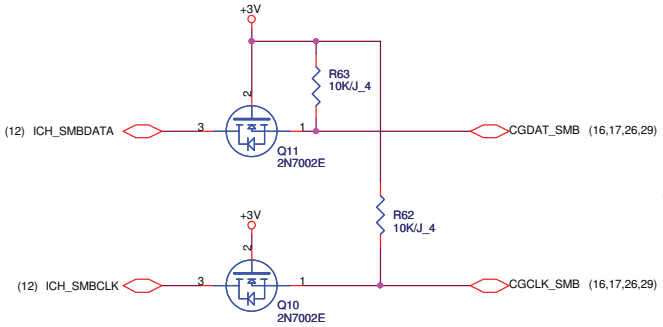
PROJECT : PS2

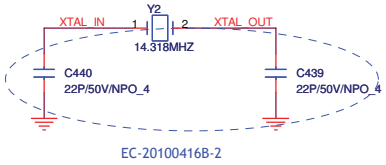
Quanta Computer Inc.

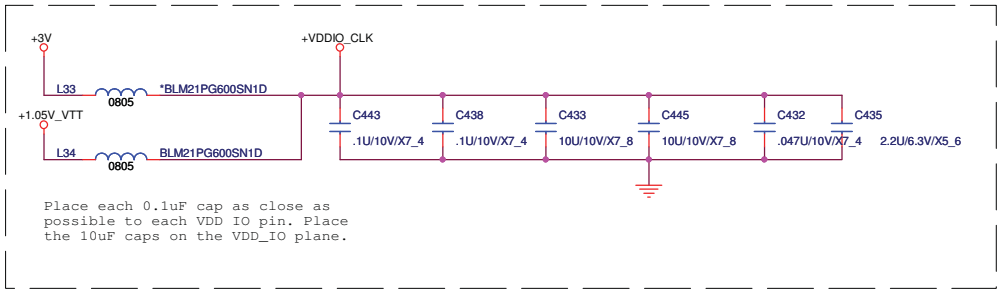
Size	Document Number	Rev
C	<Doc> Block Diagram	1A

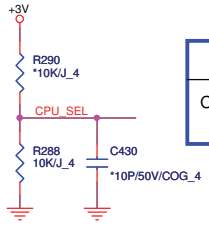
Date: Wednesday, March 03, 2010 Sheet 1 of 44



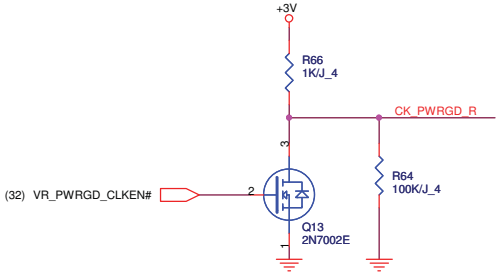








	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz



PROJECT :PS2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> Clock Generator	1A
Date: Tuesday, May 25, 2010	Sheet 2 of 44	

(2,10,11,12,13,14,16,17,18,19,20,21,22,23,25,26,28,29,31,32,34,35,37) +3V
(2,5,6,10,11,12,13,14,34,35,36,38) +1.05V_VTT
(6,16,17,33,35) 1.5VSUS

Processor Compensation Signals

Layout Note: Place these resistors near Processor

U23A

DMI_TXN0 (10) F7 DMI_RX#[0]
DMI_TXN1 (10) J8 DMI_RX#[1]
DMI_TXN2 (10) K8 DMI_RX#[2]
DMI_TXN3 (10) J4 DMI_RX#[3]
DMI_TXP0 (10) F9 DMI_RX[0]
DMI_TXP1 (10) J6 DMI_RX[1]
DMI_TXP2 (10) K9 DMI_RX[2]
DMI_TXP3 (10) J2 DMI_RX[3]
DMI_RXN0 (10) H17 DMI_TX#[0]
DMI_RXN1 (10) K15 DMI_TX#[1]
DMI_RXN2 (10) J13 DMI_TX#[2]
DMI_RXN3 (10) F10 DMI_TX#[3]
DMI_RXP0 (10) G17 DMI_TX[0]
DMI_RXP1 (10) M15 DMI_TX[1]
DMI_RXP2 (10) G13 DMI_TX[2]
DMI_RXP3 (10) J11 DMI_TX[3]

DMI

FDI_TXN[7:0] (10)
FDI_TXN0 L2
FDI_TXN1 N7
FDI_TXN2 M4
FDI_TXN3 P1
FDI_TXN4 N10
FDI_TXN5 R7
FDI_TXN6 U7
FDI_TXN7 W8
FDI_TX#[0..7]

2.7GT/s data rate

FDI_TXP[7:0] (10)
FDI_TXP0 K1
FDI_TXP1 N5
FDI_TXP2 N2
FDI_TXP3 R2
FDI_TXP4 N9
FDI_TXP5 R8
FDI_TXP6 U6
FDI_TXP7 W10
FDI_TX[0..7]

FDI_FSYNC0 (10) AC7
FDI_FSYNC1 (10) AC9
FDI_FSYNC[0..1]
FDI_INT (10) AB5
FDI_LSYNC0 (10) AA1
FDI_LSYNC1 (10) AB2
FDI_LSYNC[0..1]

Intel(R) FDI

PCI EXPRESS -- GRAPHICS

PEG_ICOMPI B12
PEG_ICOMPO A13
PEG_RCOMPO D12
PEG_RBIAS B11
PEG_COMP R226 49.9/F_4
PEG_RBIAS R227 750/F_4

PEG_RX#[0..15] G40 G38 H34 P34 G28 H25 H24 D29 B26 D26 B23 D22 A20 D19 A17 B14
PEG_RX[0..15] F40 J38 G34 M34 J28 G25 K24 B28 A27 B25 A24 B21 B19 B18 B16 D15
PEG_TX#[0..15] N40 L38 M32 D40 A38 G32 B33 B35 L30 A31 B32 L28 N26 M24 G21 J20
PEG_TX[0..15] L40 N38 N32 B39 B37 H32 A34 D36 J30 B30 D33 N28 M25 N24 F21 L20

CPU_Arrandale_1.2G

U23B

H_COMP3 R264 20/F_4 AD71 COMP3
H_COMP2 R262 20/F_4 AC70 COMP2
H_COMP1 R43 49.9/F_4 AD69 COMP1
H_COMP0 R45 49.9/F_4 AE66 COMP0
TP60 M71 PROC_DETECT

Misc

H_CATERR# N61 CATERR#
H_PECI (13) N19 PECI
H_PROCHOT# (32) N67 PROCHOT#
PM_THRMTRIP# (13) N17 THERMTRIP#

Thermal

H_CPURST# N70 RESET_OBS#
PM_SYNC (10) M17 PM_SYNC
AM7 VCCPWRGOOD_1
H_PWRGOOD (13) Y67 VCCPWRGOOD_0
PM_DRAM_PWRGD (10) R272 *0 4S DRAM_PWRGD_CPU AM5 SM_DRAMPWROK
H_VTTPWRGD H15 VTTPWRGOOD
TP7 H_PWRGD_XDP Y70 TAPPWRGOOD
PLTRST# (12,19,26,29) R246 1.5K/J_4 CPU_PLTRST# G3 RSTIN#
R242 750/F_4

Power Management

CPU_Arrandale_1.2G

Clocks

BCLK AK7 CLK_CPU_BCLK (13)
BCLK# AK8 CLK_CPU_BCLK# (13)
BCLK_ITP K71 BCLK_ITP_P TP63
BCLK_ITP# J70 BCLK_ITP_N TP61
PEG_CLK L21 CLK_PCIE_3GPLL (12)
PEG_CLK# J21 CLK_PCIE_3GPLL# (12)
DPLL_REF_SSCLK Y2 DREFSSCLK (12)
DPLL_REF_SSCLK# W4 DREFSSCLK# (12)

DDR3 Compensation Signals

DDR3 Misc

SM_DRAMRST# BJ12 CPU_DRAMRST#
SM_RCOMP[0] BV33 SM_RCOMP_0 R287 100/F_4
SM_RCOMP[1] BP39 SM_RCOMP_1 R286 24.9/F_4
SM_RCOMP[2] BV40 SM_RCOMP_2 R285 130/F_4
R278 10K/F_4 +1.05V_VTT
PM_EXT_TS#[0] AV66 PM_EXT_TS#0 R279 *0 4S SHORT0402 PM_EXTTS#0 (16)
PM_EXT_TS#[1] AV64 PM_EXT_TS#1 R276 *0 4S SHORT0402 PM_EXTTS#1 (17)
R277 10K/F_4 +1.05V_VTT

Layout Note: Place these resistors near Processor

EC-20100526C-1

JTAG & MBP

PRDY# U71 XDP_PRDY# TP65
PREQ# U69 XDP_PREQ# TP66
TCK T67 XDP_TCLK T7
TMS N65 XDP_TMS T40
TRST# P69 XDP_TRST# T5
TDI T69 XDP_TDI_R T4
TDO T71 XDP_TDO_R T8
TDI_M P71 XDP_TDI_M T36
TDO_M T70 XDP_TDO_M T38
DBR# W71 XDP_DBRESET# (10)

11/6 must add test point.

BPM#[0] J69 XDP_OBS0 TP59
BPM#[1] J67 XDP_OBS1 TP4
BPM#[2] J62 XDP_OBS2 TP2
BPM#[3] K65 XDP_OBS3 TP3
BPM#[4] K62 XDP_OBS4 TP5
BPM#[5] J64 XDP_OBS5 TP1
BPM#[6] K69 XDP_OBS6 TP62
BPM#[7] M69 XDP_OBS7 TP64

For S3 leakage issue

1.5VSUS
R55 1K/F_4
DDR_RST# (16,17)
(28) DRAMRST_CNTRL R57 *0/J_4
(12) DRAMRST_PCH R56 0/J_4
Q9 DMN601K-7
C175 .047U/10V/X7_4
CPU_DRAMRST#
R54 100K/F_4

For S3 leakage issue

3V_S5
R284 8.2K/J_4
C412 .1U/10V/X7_4
+1.5V_CPU
R268 *1.1K/F_4
(33) +1.5VCPU_PG
R274 1.5K/J_4
DRAM_PWRGD_CPU
R266 750/F_4
U24 MC74VHC1G08DFT2G
R275 *0/J_4
EC-20100206A-1

+3V
(28,29,31,32,33,34,36) HWPG
R228 2K/F_4
H_VTTPWRGD
U22 MC74VHC1G08DFT2G
R225 1K/F_4

+1.05V_VTT
XDP_TDO R250 51/J_4
H_CATERR# R31 49.9/F_4
H_PROCHOT# R35 68/J_4
H_CPURST# R241 *68/J_4
CPU_PLTRST# R237 *68/J_4
XDP_PRDY# R253 *51/J_4
XDP_TMS R259 *51/J_4
XDP_TDI_R R243 *51/J_4
XDP_PREQ# R257 *51/J_4
XDP_TCLK R254 *51/J_4

NC OTHER

H_PROCHOT#
EC-20100226A-2
EC-20100225A-6
PCH_GPIO54
Q4 *DMN601K-7
Needs to confirm GPIO
For Processor Hot Control

NC OTHER

JTAG MAPPING

RC0402
XDP_TDO_R Ra R251 0/J_4
XDP_TDO_M Rb R248 *0/J_4 XDP_TDO
Rc R244 0/J_4 RC0402
XDP_TDI_M Rd R240 *0/J_4 XDP_TDI
XDP_TDI_R Re R238 0/J_4 RC0402
XDP_TRST# R247 51/J_4

Scan Chain (Default)	STUFF -> Ra, Rc, Re NO STUFF -> Rb, Rd
CPU Only	STUFF -> Ra, Rb NO STUFF -> Rc, Rd, Re
GMCH Only	STUFF -> Rd, Re NO STUFF -> Ra, Rb, Rc

PROJECT : PS2
Quanta Computer Inc.

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C	<Doc> PROCESSER 1/7(HOST&PCI)	1A

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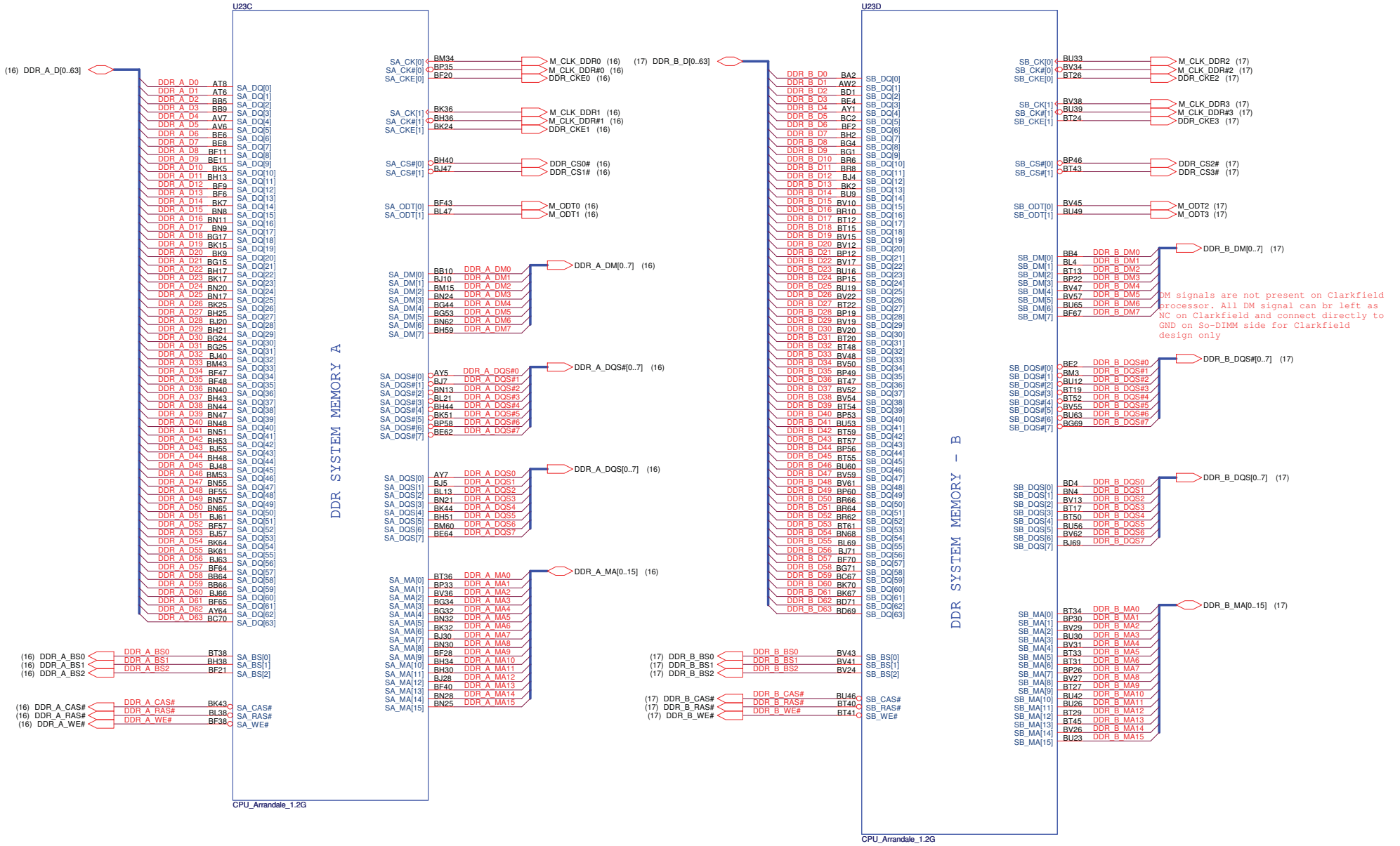
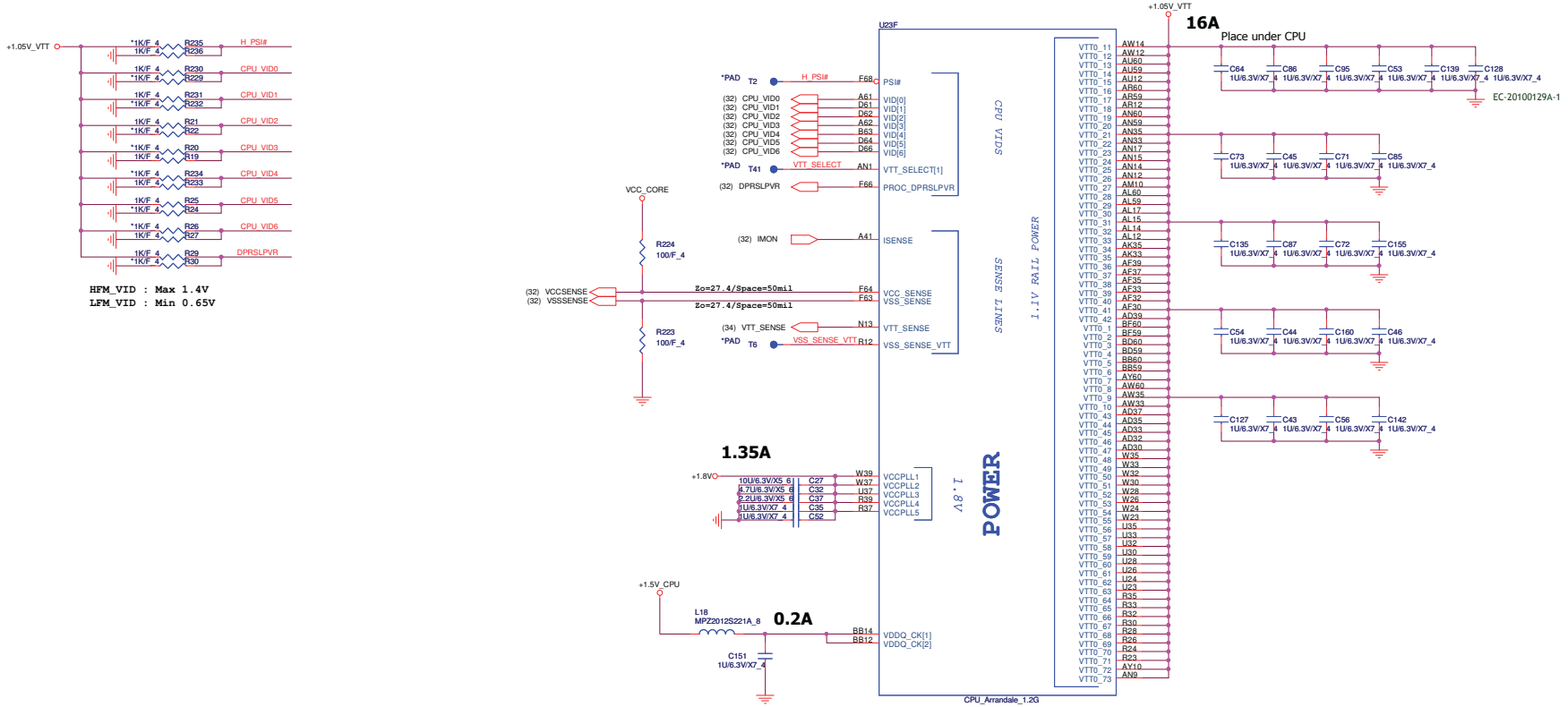
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Quanta Computer Inc.	PROJECT : PS2	
Size: Custom	Document Number: <Doc>	Rev: 1A
Date: Tuesday, May 25, 2010	Sheet 4 of 44	PROCESSER 2/7 (DDR3)



PROJECT :PS2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> PROCESSER 3/7(POWER1)	1A
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(35,36) +VCC_GFX_CORE
(2,3,5,10,11,12,13,14,34,35,36,38) +1.05V_VTT
(3,5,33) +1.5V_CPU

VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V

Max 15A

+VCC_GFX_CORE

Please note that +VCC_GFX_CORE should be 1.05V in Arrandale

U23G

C106 10U/6.3V/X5_6, C105 10U/6.3V/X5_6, C79 10U/6.3V/X5_6
C78 1U/6.3V/X7_4, C89 1U/6.3V/X7_4, C88 1U/6.3V/X7_4, C124 1U/6.3V/X7_4
C76 1U/6.3V/X7_4, C99 1U/6.3V/X7_4, C113 1U/6.3V/X7_4, C123 1U/6.3V/X7_4
C115 1U/6.3V/X7_4, C114 1U/6.3V/X7_4, C97 1U/6.3V/X7_4, C77 1U/6.3V/X7_4
C126 1U/6.3V/X7_4, C125 1U/6.3V/X7_4, C96 1U/6.3V/X7_4, C98 1U/6.3V/X7_4

AN32 AN30 AN28 AN26 AN24 AN23 AN21 AN19 AL32 AL30 AL28 AL26 AL24 AL23 AL21 AL19 AK14 AK12 AJ10 AH14 AH12 AF28 AF26 AF24 AF23 AF21 AF19 AF17 AF15 AF14 AD28 AD26 AD24 AD23 AD21 AD19 AD17

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37

GRAPHICS

+1.05V_VTT

W21 W19 U21 U19 U17 U15 U14 U12 R21 R19 R17 R15

VTT1_1 VTT1_2 VTT1_3 VTT1_4 VTT1_5 VTT1_6 VTT1_7 VTT1_8 VTT1_9 VTT1_10 VTT1_11 VTT1_21

C129 1U/6.3V/X7_4, C70 1U/6.3V/X7_4

PEG & DMI

POWER

AK62 AK60 AK59 AH60 AH59 AF60 AF59 AD60 AD59 AB60 AB59 AA60 AA59 W60 W59 U60 U59 R60 R59

VCAP2_1 VCAP2_2 VCAP2_3 VCAP2_4 VCAP2_5 VCAP2_6 VCAP2_7 VCAP2_8 VCAP2_9 VCAP2_10 VCAP2_11 VCAP2_12 VCAP2_13 VCAP2_14 VCAP2_15 VCAP2_16 VCAP2_17 VCAP2_18 VCAP2_19

+VCCTTG

C80 1U/6.3V/X7_4, C116 1U/6.3V/X7_4, C100 1U/6.3V/X7_4, C63 1U/6.3V/X7_4, C47 1U/6.3V/X7_4

VCAP0
VCAP1
VCAP2

CPU_Arrandale_1.2G

SENSE LINES

VAXG_SENSE AF12 → VCC_AXG_SENSE (36)
VSSAXG_SENSE AF10 → VSS_AXG_SENSE (36)

GRAPHICS VIDs

GFX_VID[0] AF71 → GFXVR_VID_0 (36)
GFX_VID[1] AG67 → GFXVR_VID_1 (36)
GFX_VID[2] AG70 → GFXVR_VID_2 (36)
GFX_VID[3] AH71 → GFXVR_VID_3 (36)
GFX_VID[4] AN71 → GFXVR_VID_4 (36)
GFX_VID[5] AM67 → GFXVR_VID_5 (36)
GFX_VID[6] AM70 → GFXVR_VID_6 (36)

GFXVR_EN R267 4.7K/F_4
GFX_IMON R270 *1K/F_4

GFX_VR_EN AH69 GFXVR_EN → GFXVR_EN (36)
GFX_DPRSLPVR AL71 GFX_DPRSLPVR R271 *0_4S → GFXVR_DPRSLPVR (36)
GFX_IMON AL69 GFX_IMON R269 *0_4S → GFXVR_IMON (36)

DDR3 - 1.5V RAILS

VDDQ1 BU40
VDDQ2 BU35
VDDQ3 BU28
VDDQ4 BN38
VDDQ5 BM25
VDDQ6 BL30
VDDQ7 BJ38
VDDQ8 BH32
VDDQ9 BH28
VDDQ10 BG43
VDDQ11 BF16
VDDQ12 BF15
VDDQ13 BD35
VDDQ14 BD33
VDDQ15 BD32
VDDQ16 BD30
VDDQ17 BD28
VDDQ18 BD26
VDDQ19 BD24
VDDQ20 BD23
VDDQ21 BD21
VDDQ22 BD19
VDDQ23 BD17
VDDQ24 BD15
VDDQ25 BB35
VDDQ26 BB33
VDDQ27 BB32
VDDQ28 BB30
VDDQ29 BB28
VDDQ30 BB26
VDDQ31 BB24
VDDQ32 BB23
VDDQ33 BB21
VDDQ34 BB19
VDDQ35 BB17
VDDQ36 BB15

+1.5V_CPU

3A EC-20100526C-1

C158 1U/6.3V/X7_4, C143 1U/6.3V/X7_4, C159 1U/6.3V/X7_4, C149 1U/6.3V/X7_4, C150 1U/6.3V/X7_4

C169 *10U/6.3V/X5_6, C168 10U/6.3V/X5_6, C170 10U/6.3V/X5_6, C171 *330U/2.5V/ESR9_3528

1.5VSUS
C173 .1U/10V/X7_4
C174 .1U/10V/X7_4
+1.5V_CPU

VTT0_DDR AW32
VTT0_DDR[1] AW30
VTT0_DDR[2] AW28
VTT0_DDR[3] AW26
VTT0_DDR[4] AW24
VTT0_DDR[5] AW23
VTT0_DDR[6] AW21
VTT0_DDR[7] AW19
VTT0_DDR[8] AW17
VTT0_DDR[9] AW15

+1.05V_VTT

2.6A

C138 1U/6.3V/X7_4, C136 1U/6.3V/X7_4, C137 1U/6.3V/X7_4

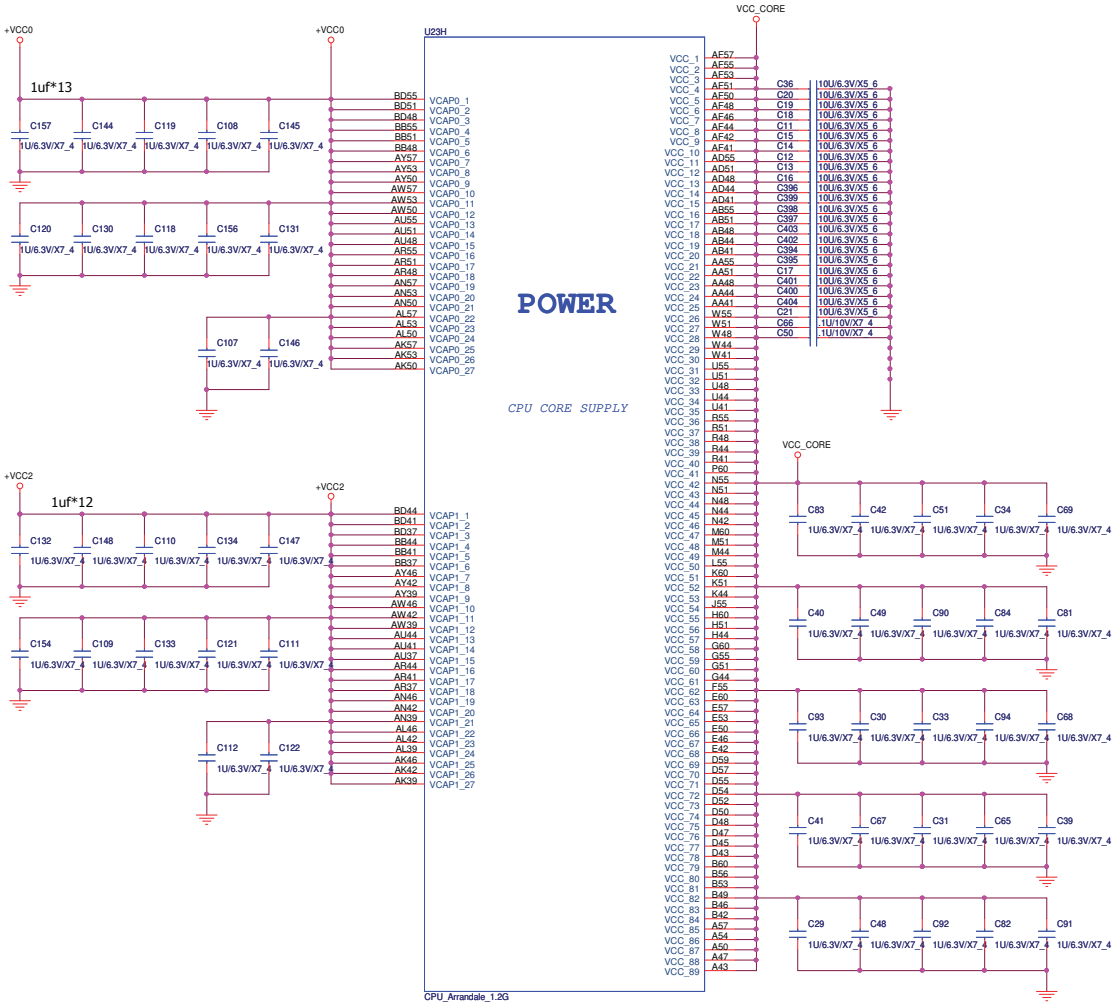
VTT1_12 AD15
VTT1_13 AD14
VTT1_14 AD12
VTT1_15 AB12
VTT1_16 AA12
VTT1_17 W17
VTT1_18 W15
VTT1_19 W14
VTT1_20 W12

+1.05V_VTT

C58 10U/6.3V/X5_6, C55 1U/6.3V/X7_4, C57 1U/6.3V/X7_4

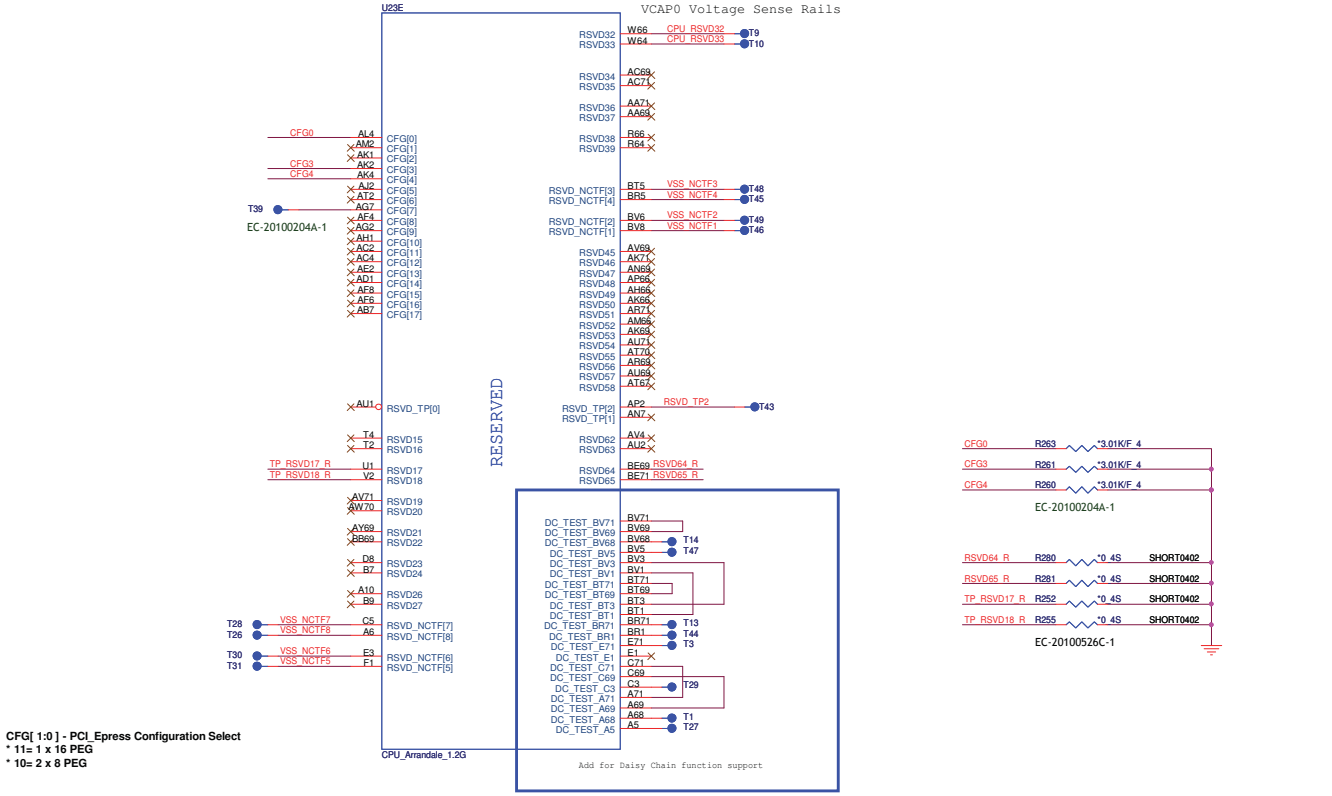
PROJECT : PS2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> PROCESSER 4/7 (POWER2)	1A
Date: Wednesday, May 26, 2010	Sheet 6 of 44	



PROJECT :PS2
Quanta Computer Inc.

Size	Document Number	Rev
C	<Doc> PROCESSER 5/7(POWER3)	1A
Date: Friday, April 30, 2010	Sheet 7 of 44	

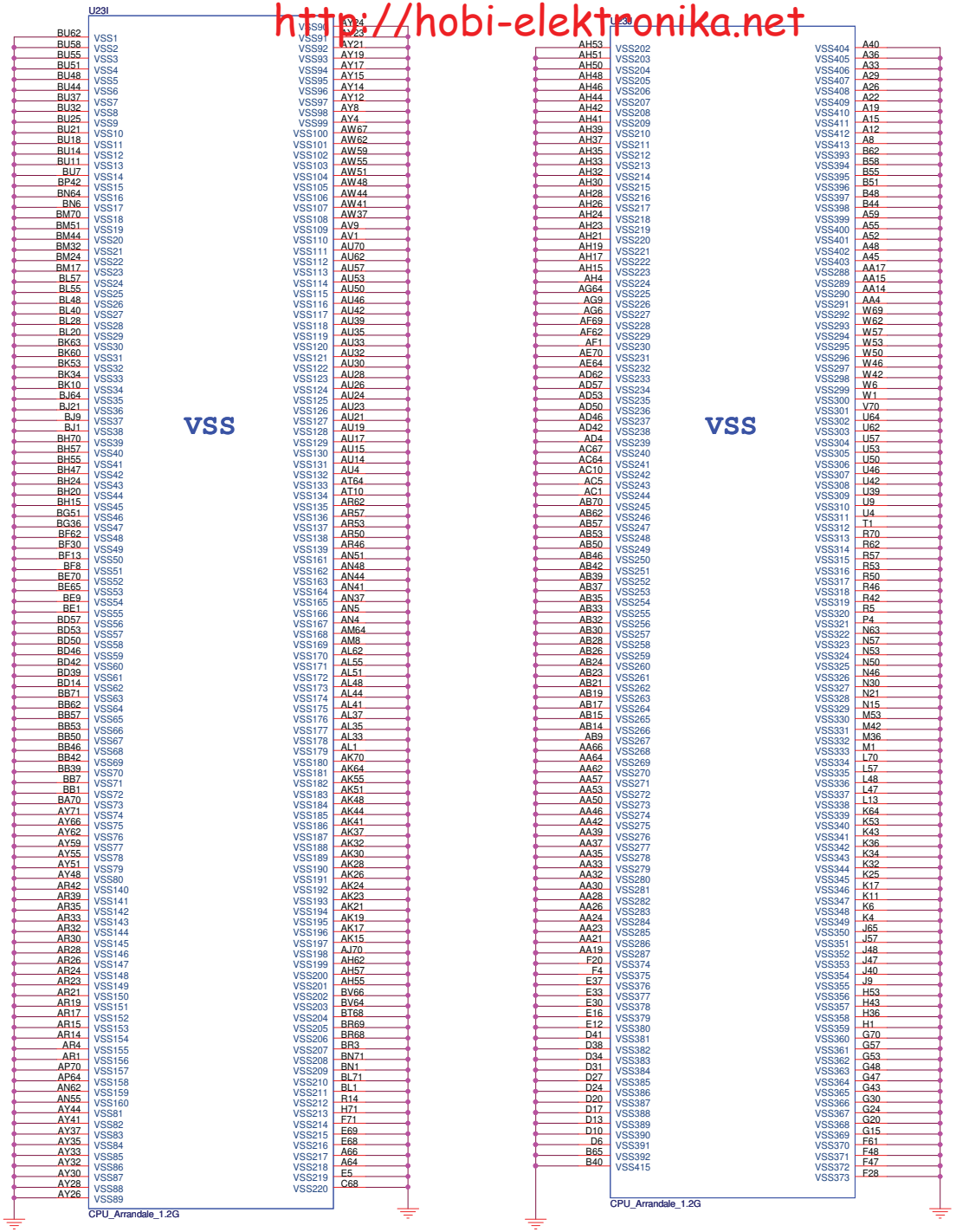


CFG[1:0] - PCI_Epress Configuration Select
*** 11= 1 x 16 PEG**
*** 10= 2 x 8 PEG**

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

ARRANDALE PROCESSOR (GND)



PROJECT : PS2

Quanta Computer Inc.

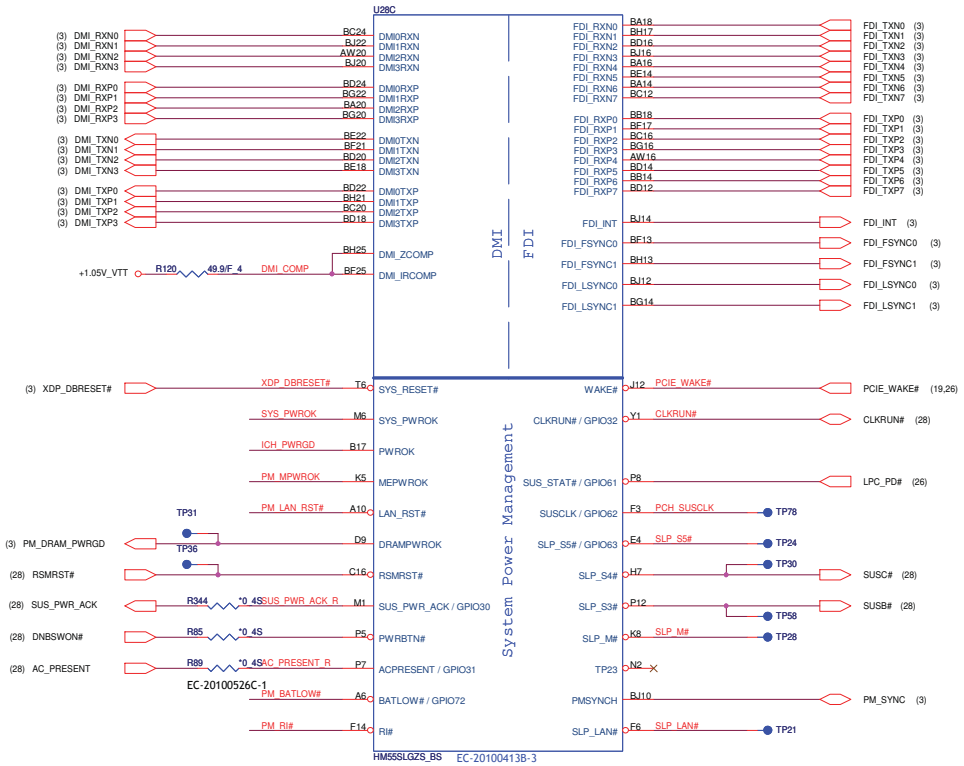
Size	Document Number	Rev
Custom	<Doc>	1A

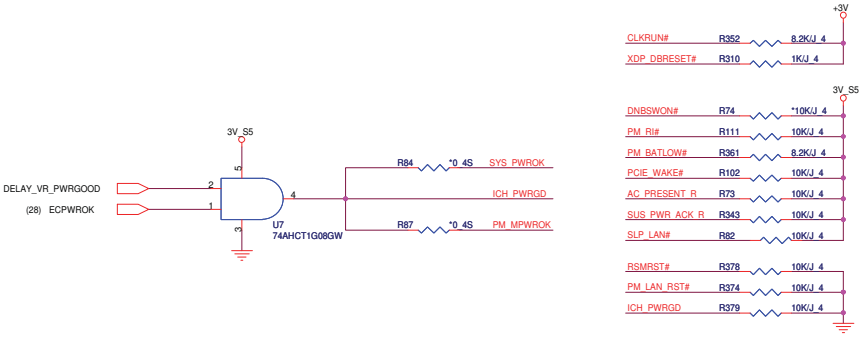
PROCESSER 7/7 (GND)

Date: Friday, April 30, 2010 Sheet 9 of 44

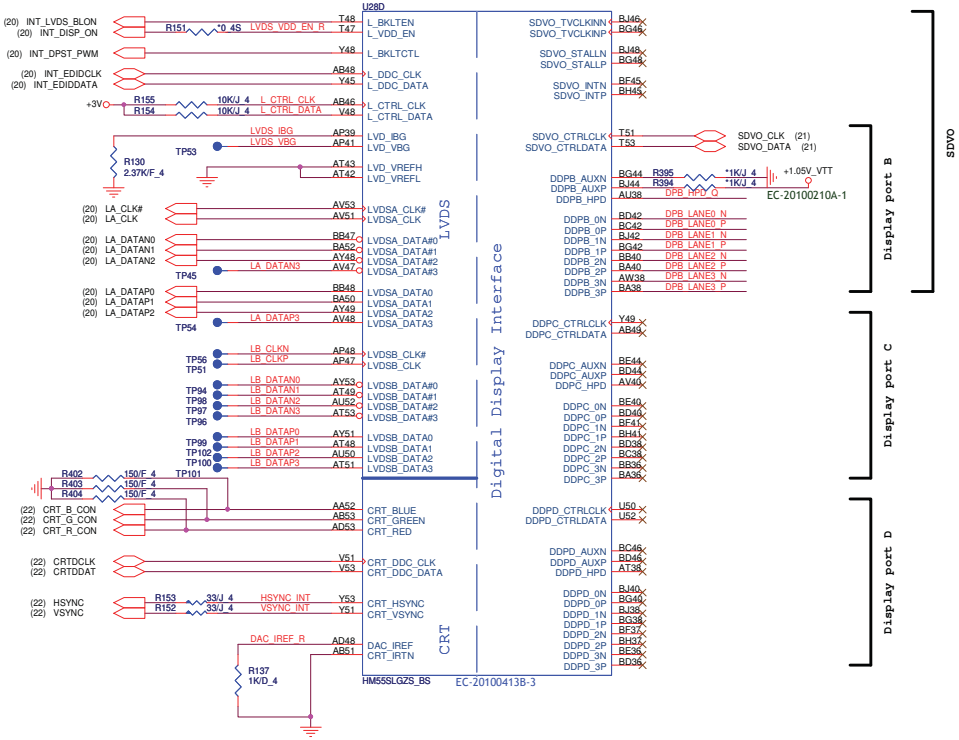
(2,3,5,6,11,12,13,14,34,35,36,38) +1.05V_VTT
(3,11,12,13,14,28,33,35) 3V_S5
(2,3,11,12,13,14,16,17,18,19,20,21,22,23,25,26,28,29,31,32,34,35,37) +3V
(14,18,20,21,22,23,24,25,28,35) +5V

IBEX PEAK-M (DMI,FDI,GPIO)

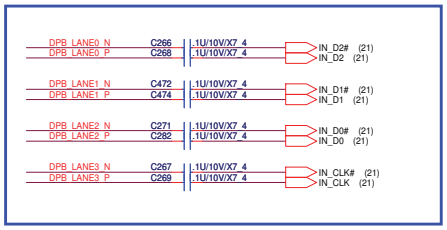


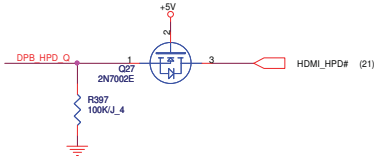


IBEX PEAK-M (LVDS,DDI)



For UMA HDMI Function





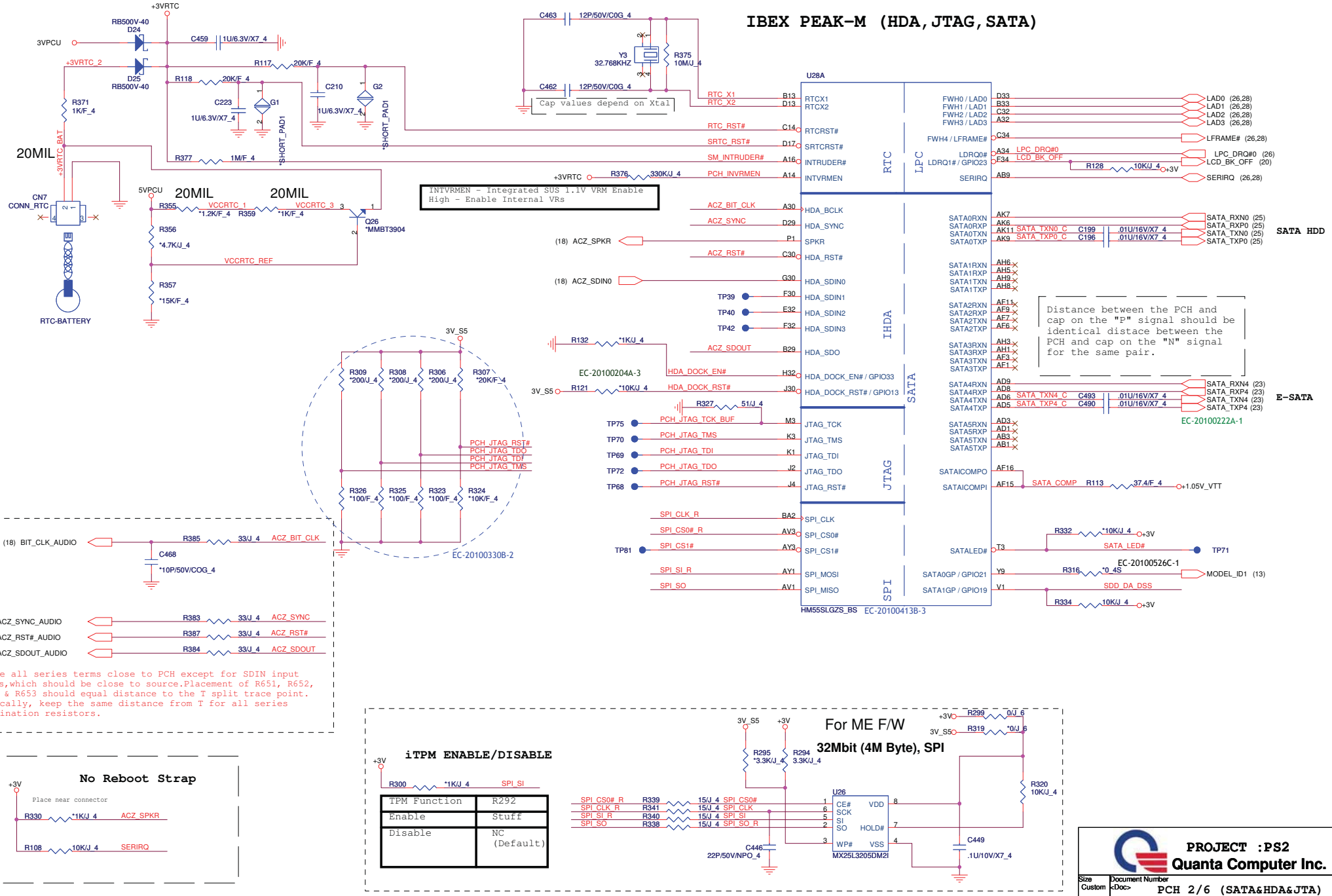
Follow Intel DG Mika

PROJECT : PS2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> PCH 1/6 (DMI&VIDEO)	1A
Date: Wednesday, May 26, 2010	Sheet 10 of 44	

(14,28) +3VRTC
(19,20,24,27,28,30,31,34,35) 3VPCU
(2,3,10,12,13,14,16,17,18,19,20,21,22,23,25,26,28,29,31,32,34,35,37) +3V
(3,10,12,13,14,28,33,35) 3V_S5
(2,3,5,6,10,12,13,14,34,35,36,38) +1.05V_VTT

IBEX PEAK-M (HDA, JTAG, SATA)



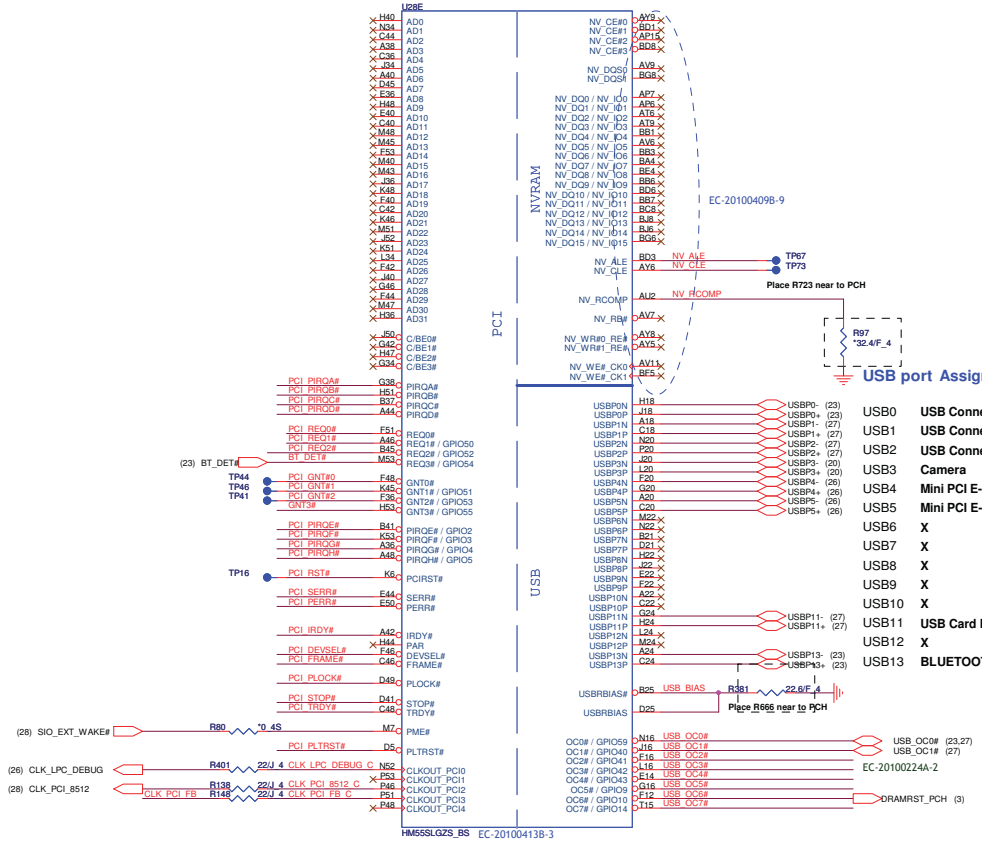
TPM Function	R292
Enable	Stuff
Disable	NC (Default)

PROJECT : PS2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> PCH 2/6 (SATA&HDA&JTA)	1A
Date: Wednesday, May 26, 2010	Sheet 11 of 44	

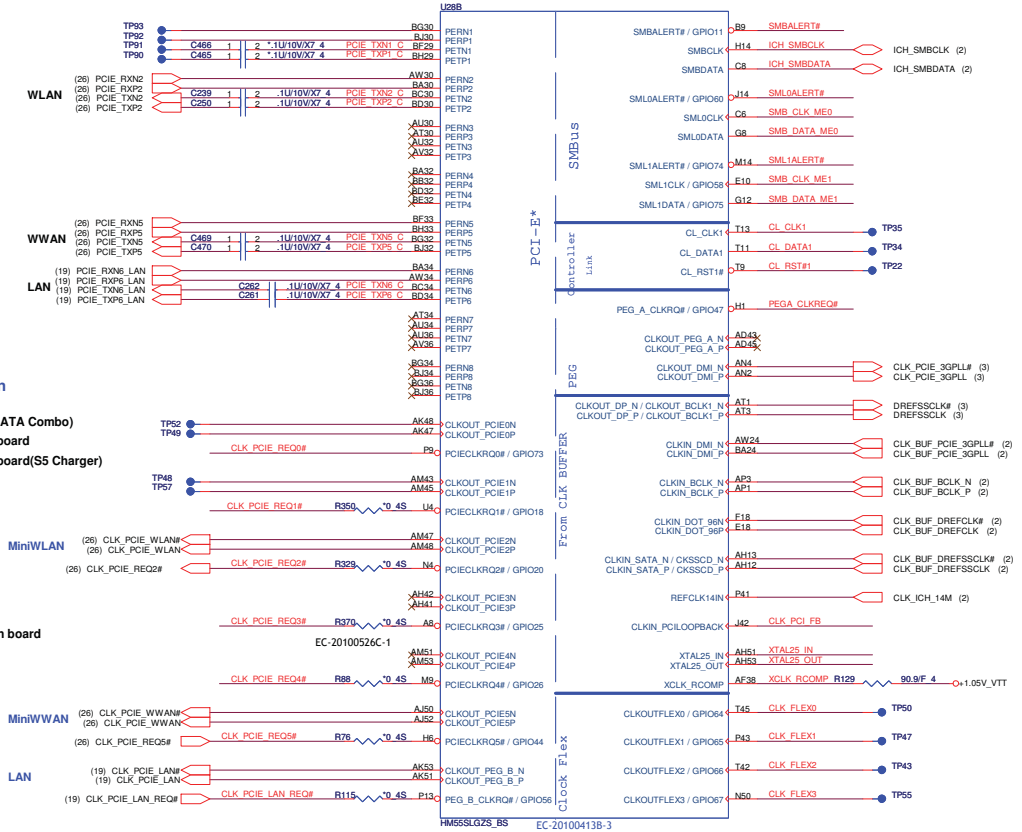
IBEX PEAK-M (PCI,USB,NVRAM)

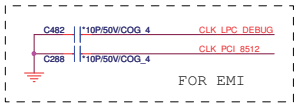
IBEX PEAK-M (PCI-E,SMBUS,CLK)

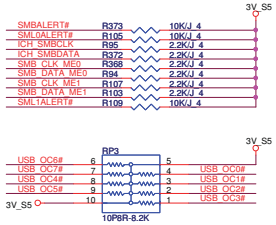


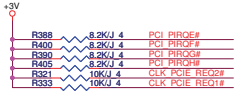
USB port Assignment function

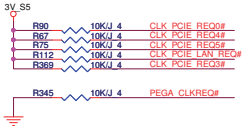
USB0	USB Connector onboard(E-SATA Combo)
USB1	USB Connector on function board
USB2	USB Connector on function board(S5 Charger)
USB3	Camera
USB4	Mini PCI E-WLAN
USB5	Mini PCI E-WWAN
USB6	X
USB7	X
USB8	X
USB9	X
USB10	X
USB11	USB Card Reader on function board
USB12	X
USB13	BLUETOOTH

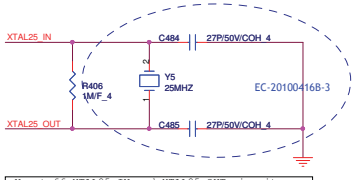


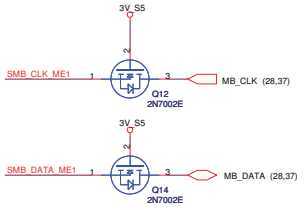


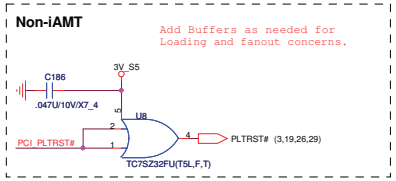


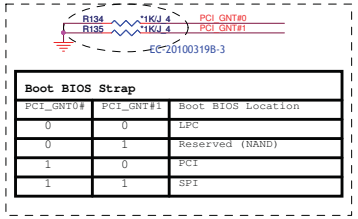












Boot BIOS Strap

PCI_GNT0#	PCI_GNT1#	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

DMI Termination Voltage

NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

Danbury Technology Enabled

NV_ALE	High = Enable Low = Disable

A16 swap override Strap/Top-Block Swap Override jumper

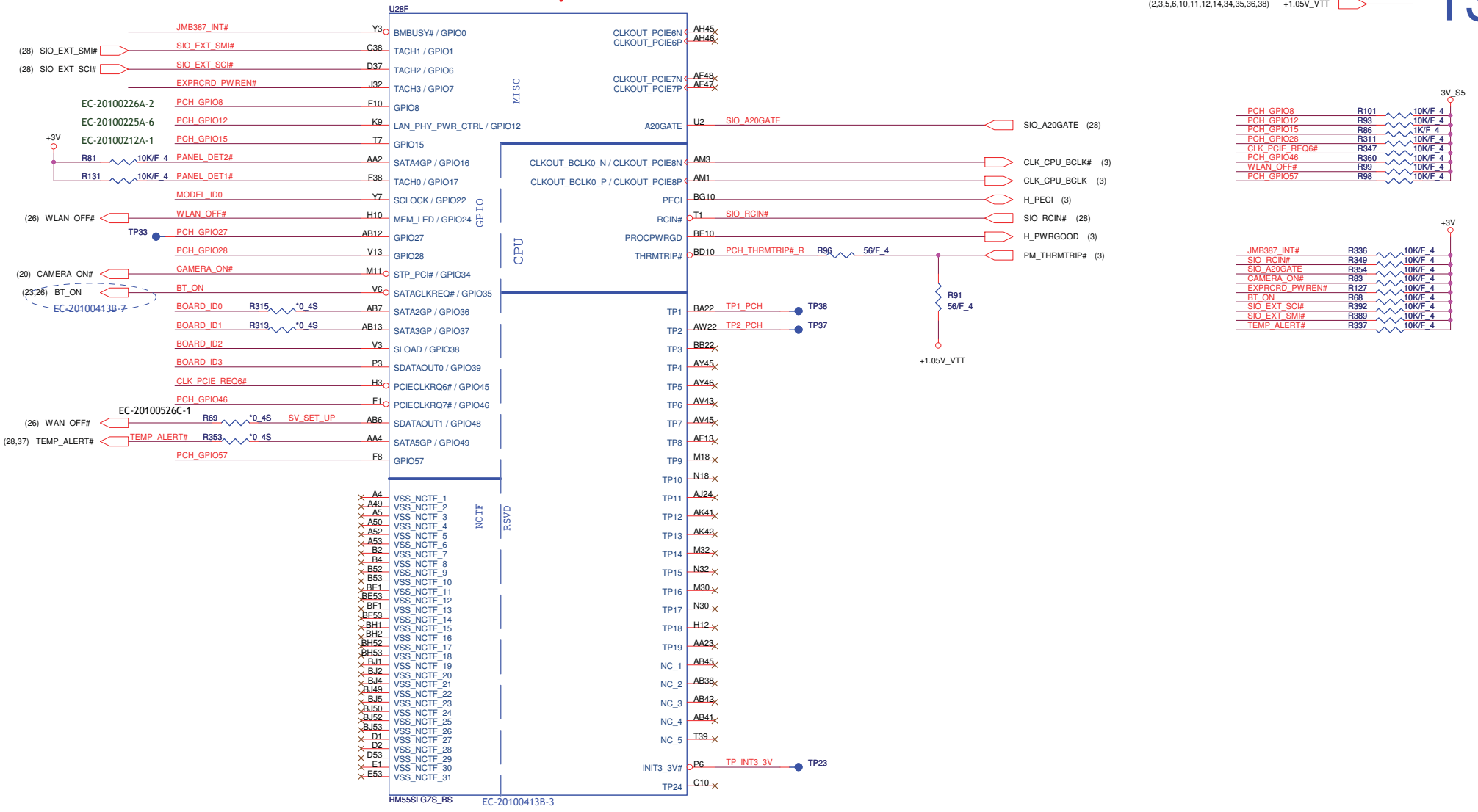
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

PROJECT :PS2
Quanta Computer Inc.

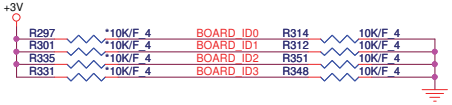
Size	Document Number	Rev
Custom	<Doc> PCH 3/6 (PCI)	1A
Date: Wednesday, May 26, 2010	Sheet 12 of 44	

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

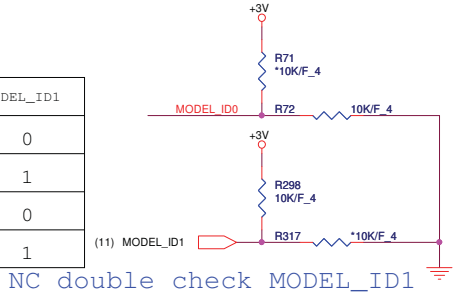
(2,3,10,11,12,14,16,17,18,19,20,21,22,23,25,26,28,29,31,32,34,35,37) +3V
(3,10,11,12,14,28,33,35) 3V_S5
(2,3,5,6,10,11,12,14,34,35,36,38) +1.05V_VTT



Board ID For Function	ID3 GPIO39	ID2 GPIO38	ID1 GPIO37	ID0 GPIO36
SDV	0	0	0	0
SIV	0	0	0	1
SIT	0	0	1	0
SVT	0	1	0	0
SOVP	1	0	0	0



Model ID	MODEL_ID0	MODEL_ID1
13"	0	0
14"	0	1
15"	1	0
Default	1	1



NC double check MODEL_ID1

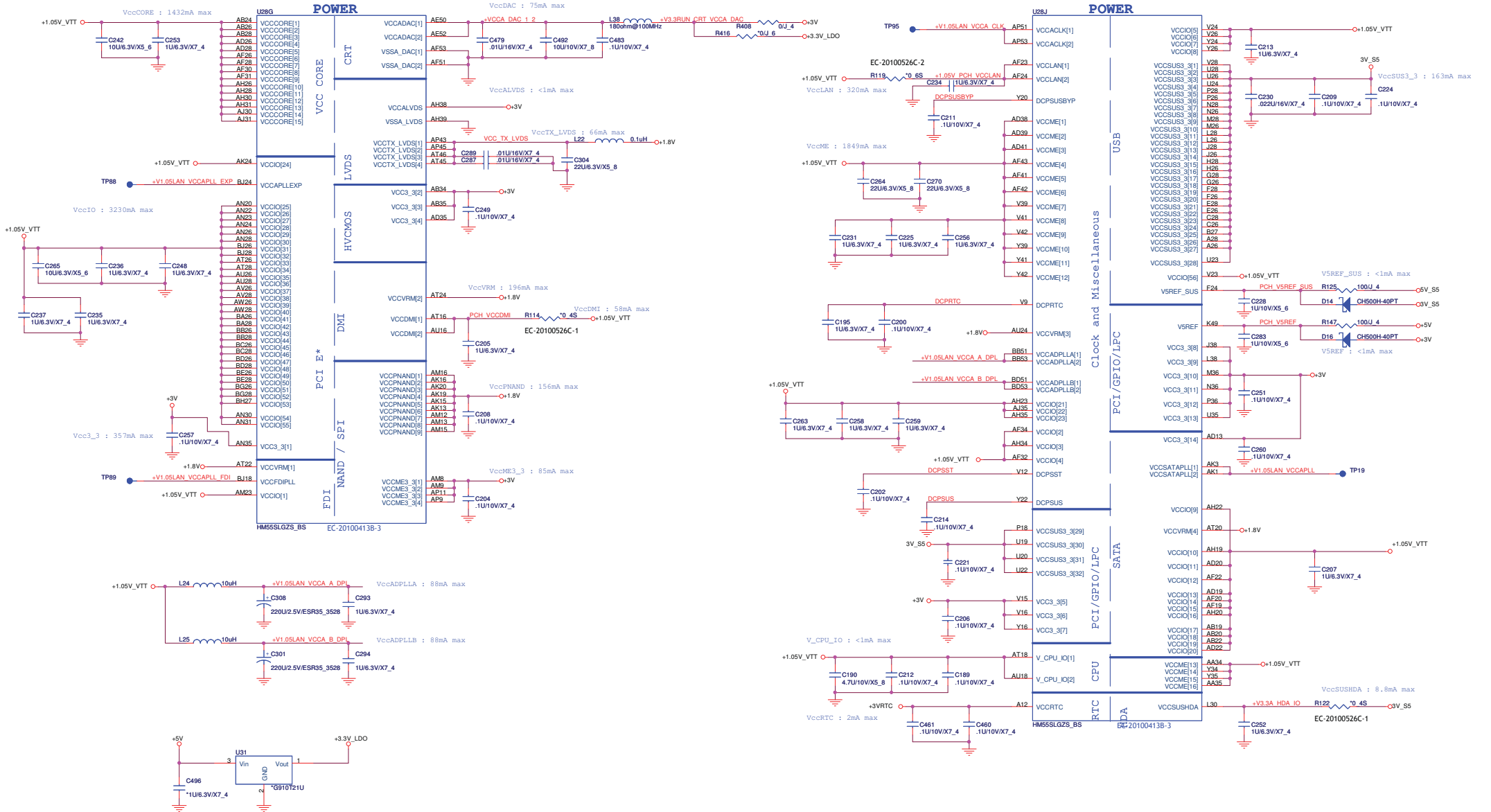
SV_SET_UP	1-X High = Strong (Default)

PROJECT : PS2
Quanta Computer Inc.

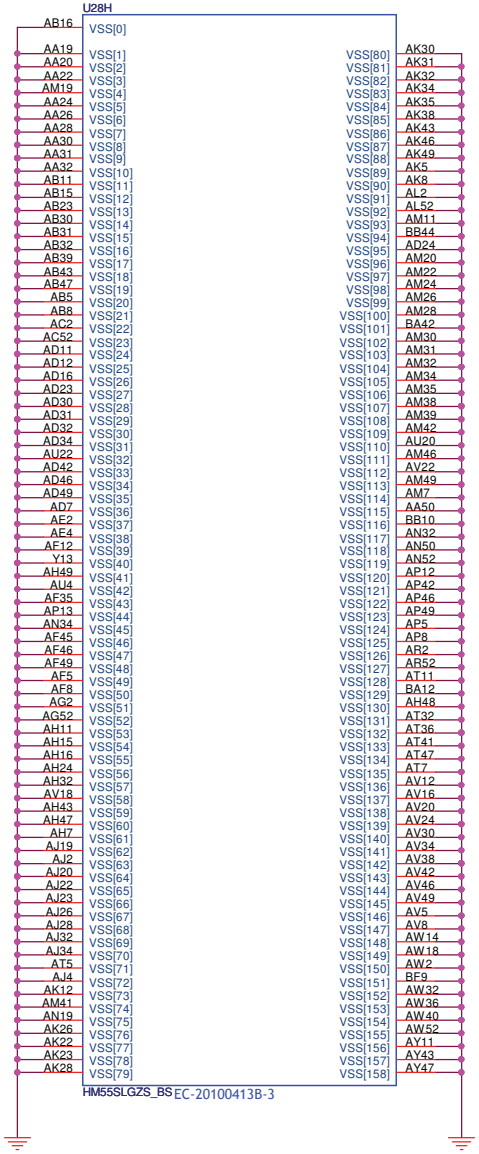
Size	Document Number	Rev
Custom	<Doc>	1A

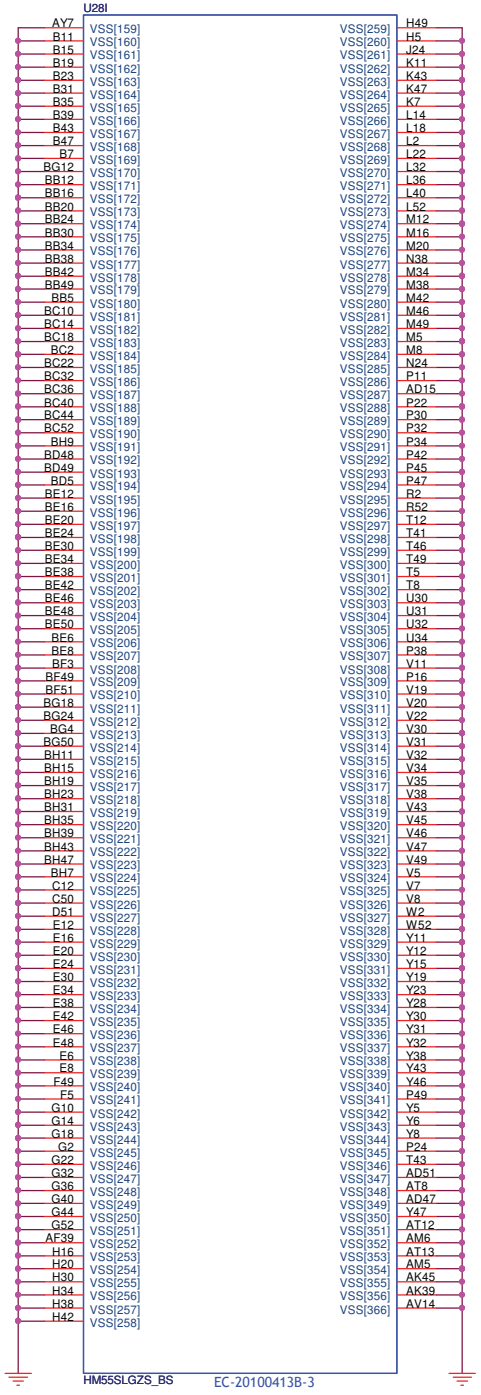
PCH 4/6 (GPIO)

Date: Wednesday, May 26, 2010 Sheet 13 of 44



IBEX PEAK-M (GND)

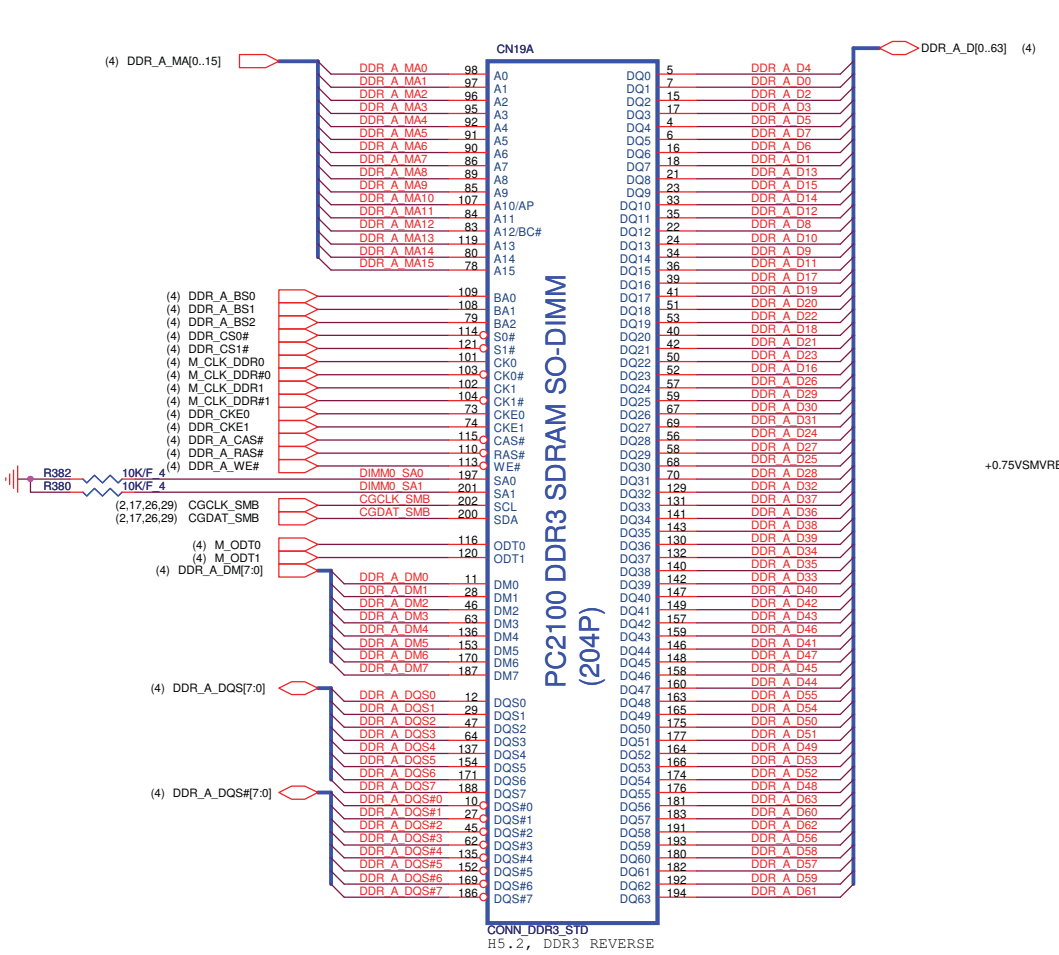


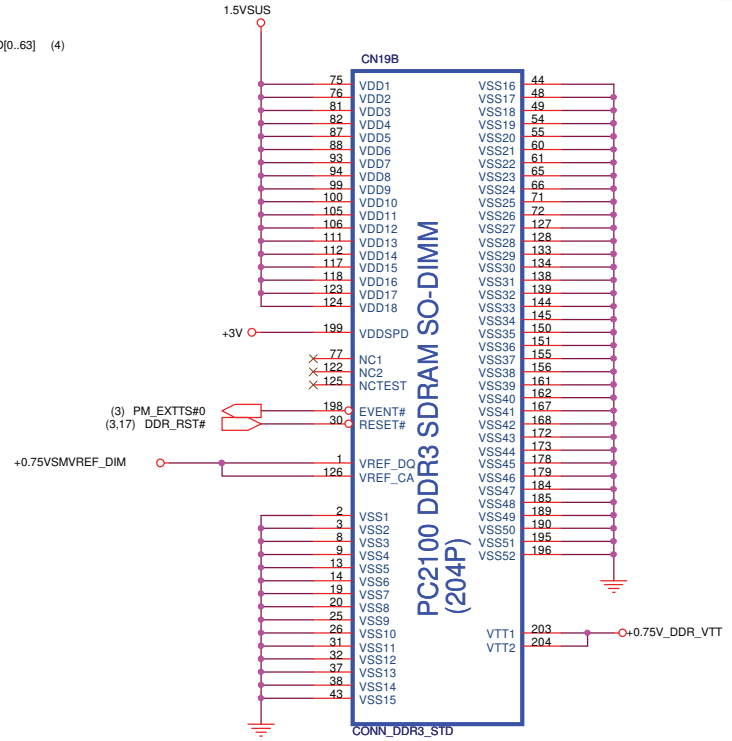


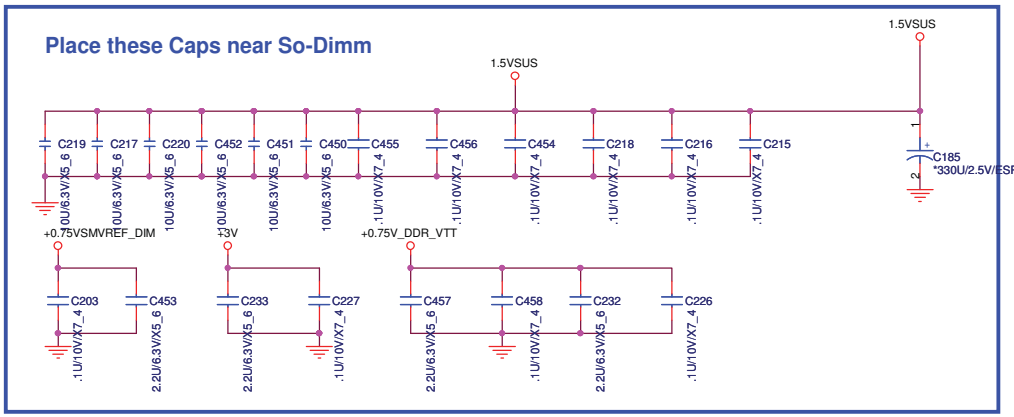
PROJECT : PS2

Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> PCH 6/6 (GND)	1A
Date: Friday, April 30, 2010	Sheet 15 of 44	



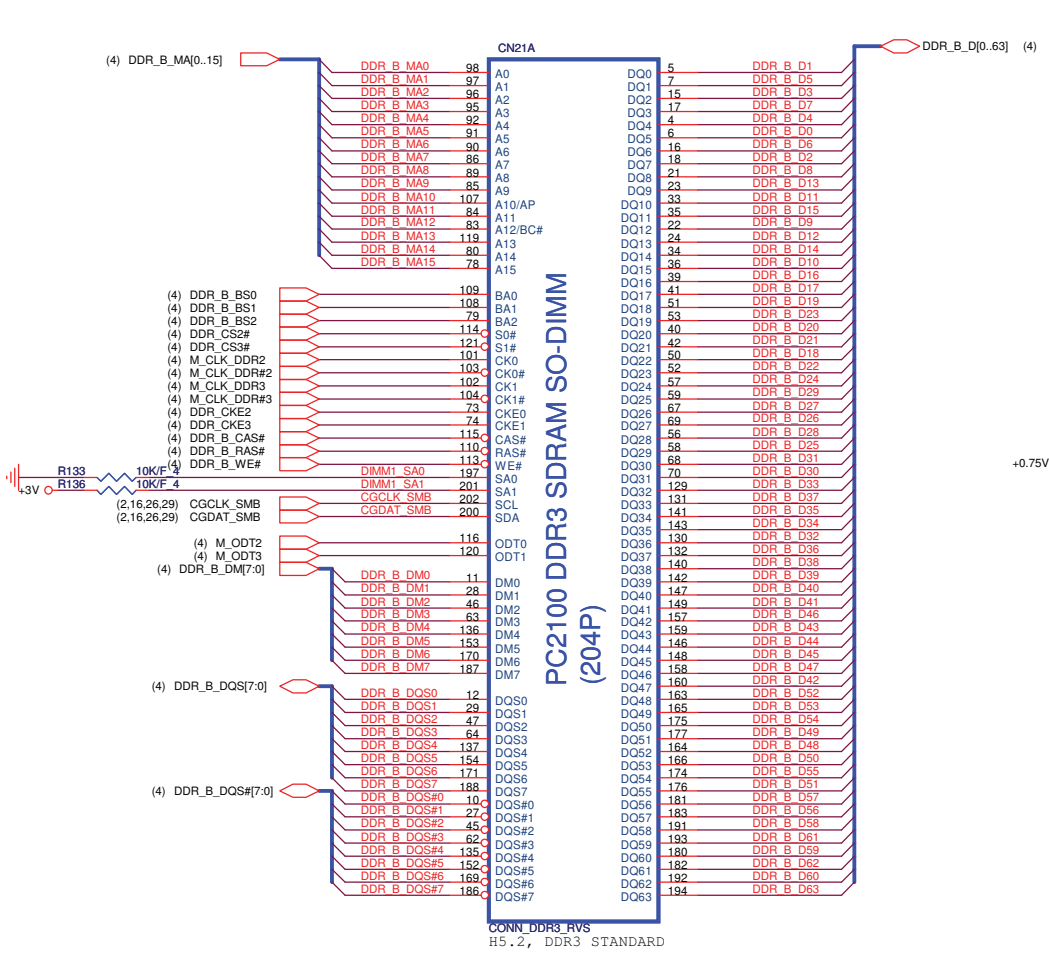


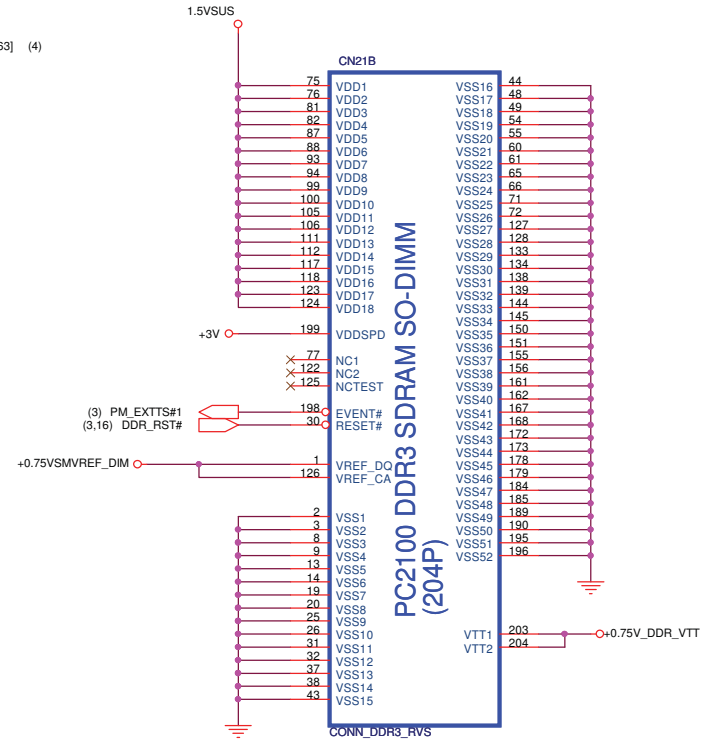


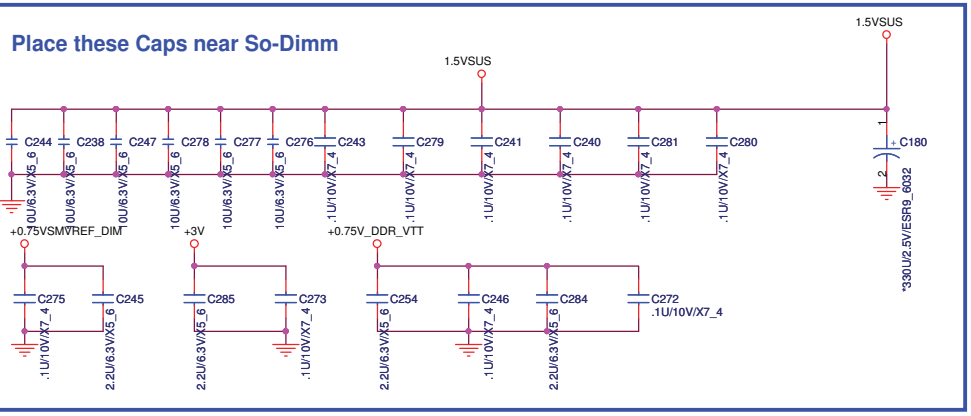
PROJECT :PS2
Quanta Computer Inc.

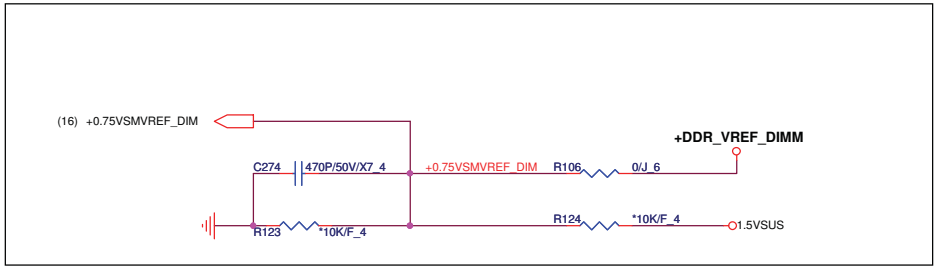
Size	Document Number	Rev
Custom	<Doc> DDR3 (A) SO-DIMM RVS	1A
Date: Tuesday, May 25, 2010	Sheet 16 of 44	

(3,6,16,33,35) 1.5VSUS
(2,3,10,11,12,13,14,16,18,19,20,21,22,23,25,26,28,29,31,32,34,35,37) +3V
(16,33,35) +0.75V_DDR_VTT



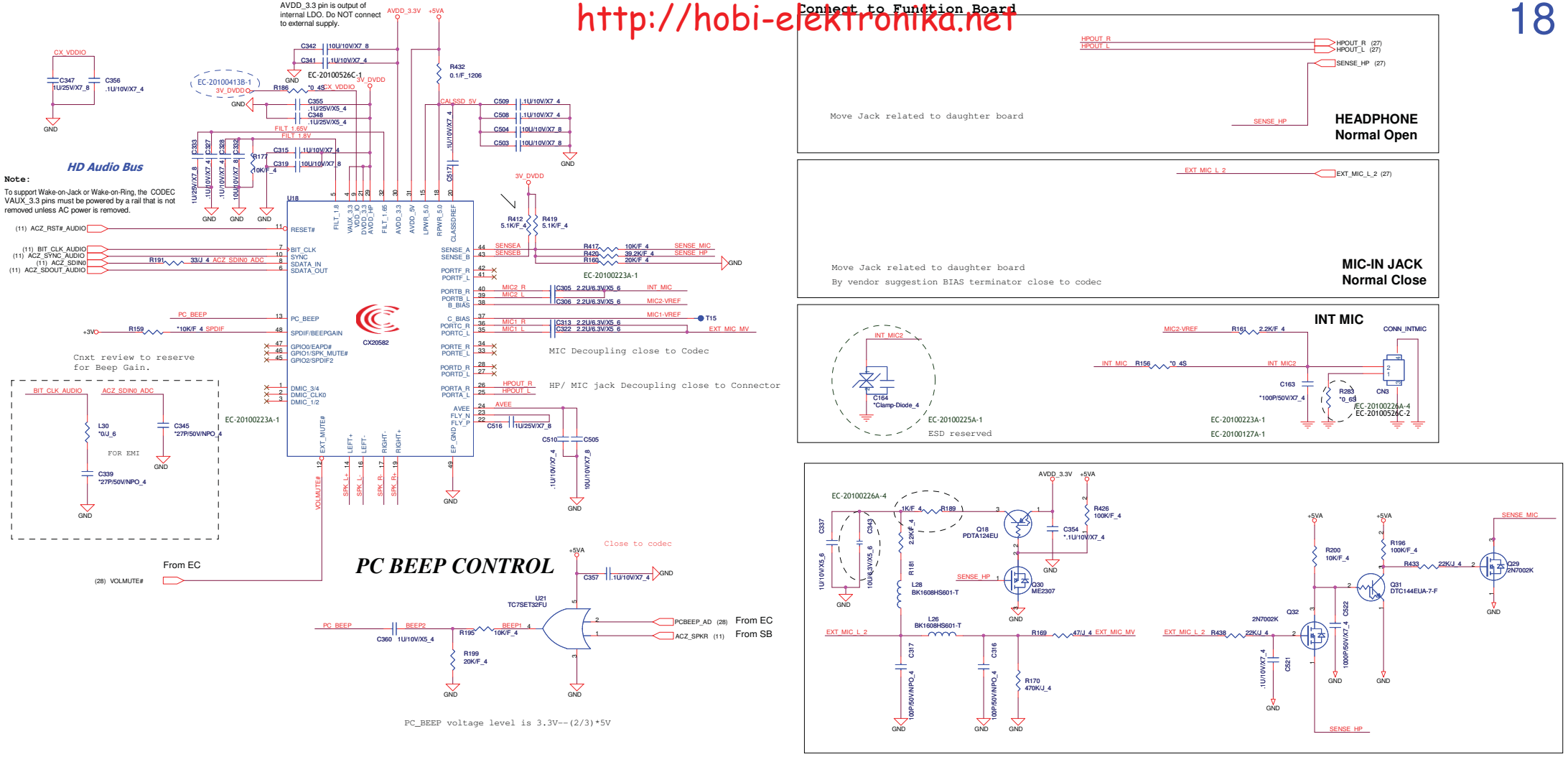




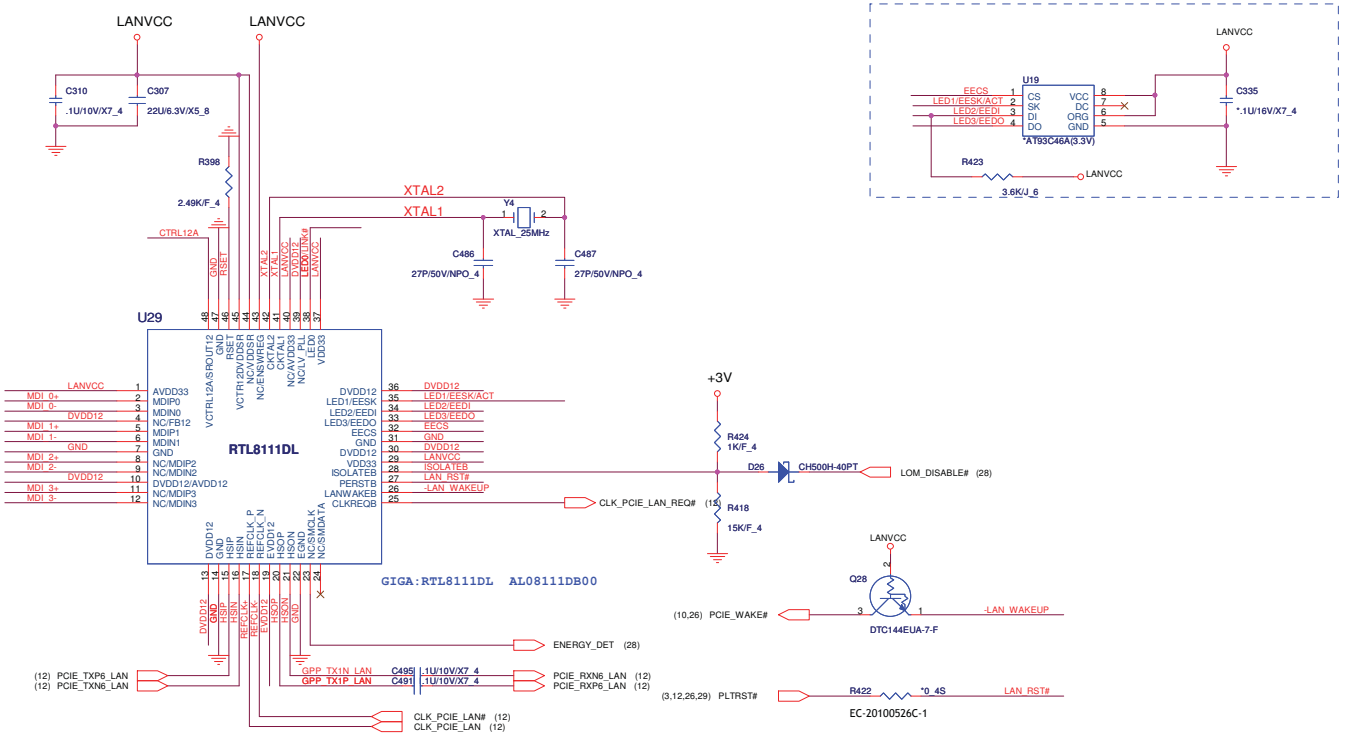


PROJECT :PS2
Quanta Computer Inc.

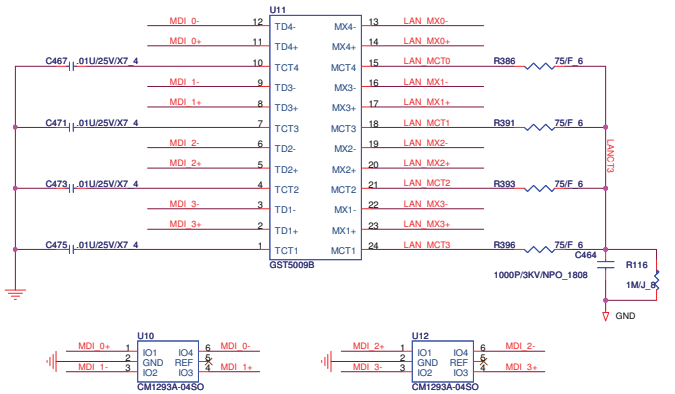
Size	Document Number	Rev
Custom	<Doc> DDR3 (B) SO-DIMM STD	1A
Date: Wednesday, May 26, 2010	Sheet 17 of 44	



PROJECT :PS2			
Quanta Computer Inc.			
Size: Custom	Document Number: <Doc>	AUDIO (CX20582, SPK)	Rev: 1A
Date: Wednesday, May 26, 2010	Sheet 18 of 44		

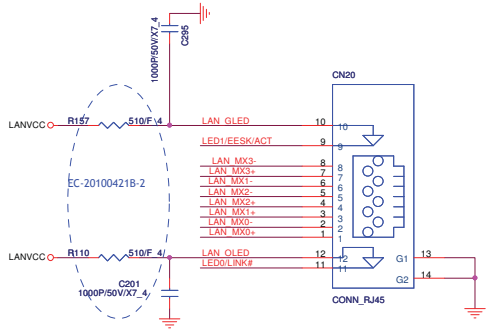


Transformer

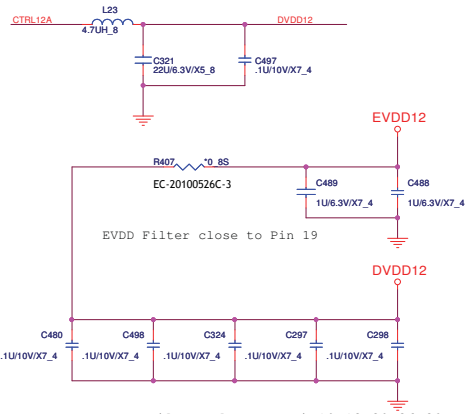


RJ45 Connector

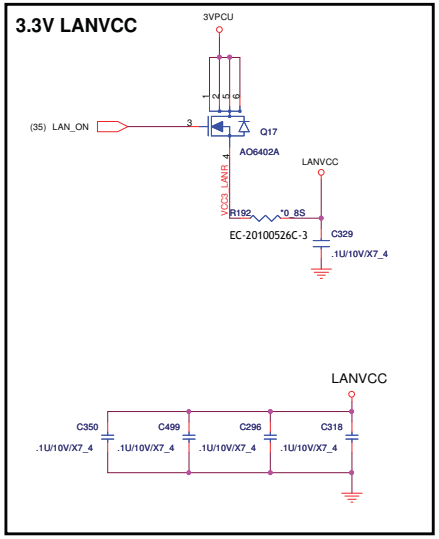
EMI: Close RJ45 Conn.



EMI: Close RJ45 Conn.



3.3V LANVCC

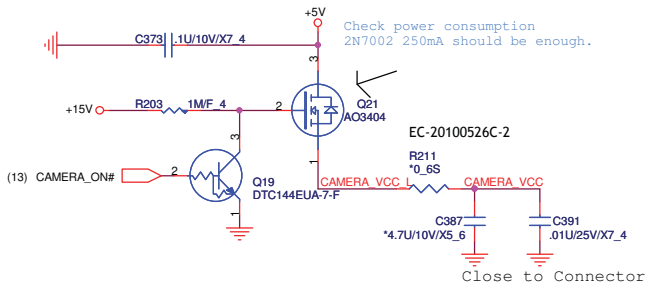


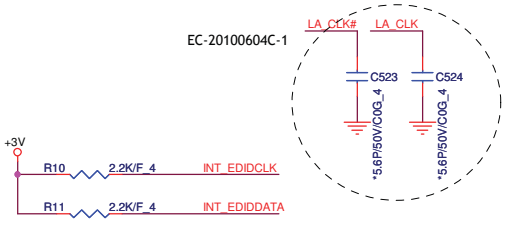
PROJECT : PS2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> LAN (RTL8111DL, RJ45)	1A

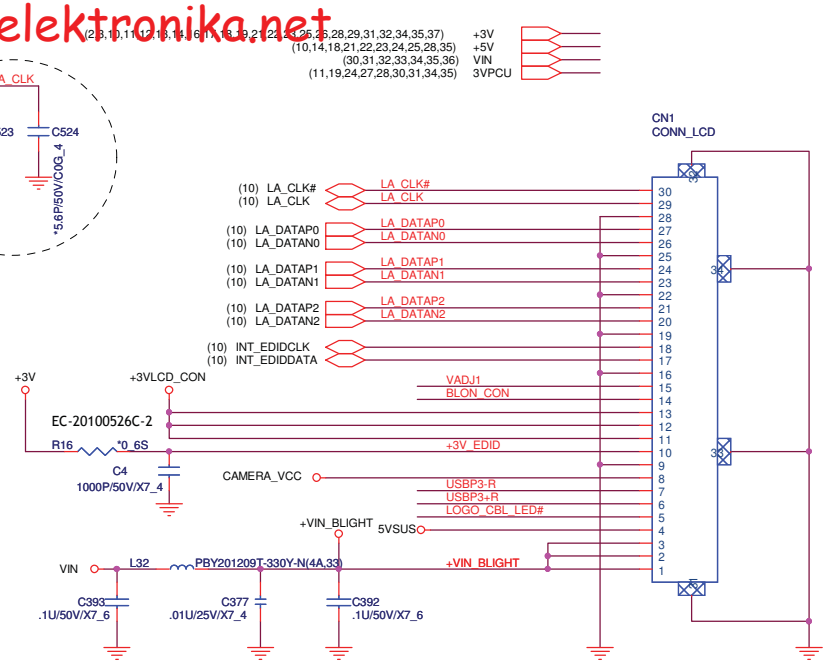
Date: Wednesday, May 26, 2010 Sheet 19 of 44

CCD POWER CONTROL

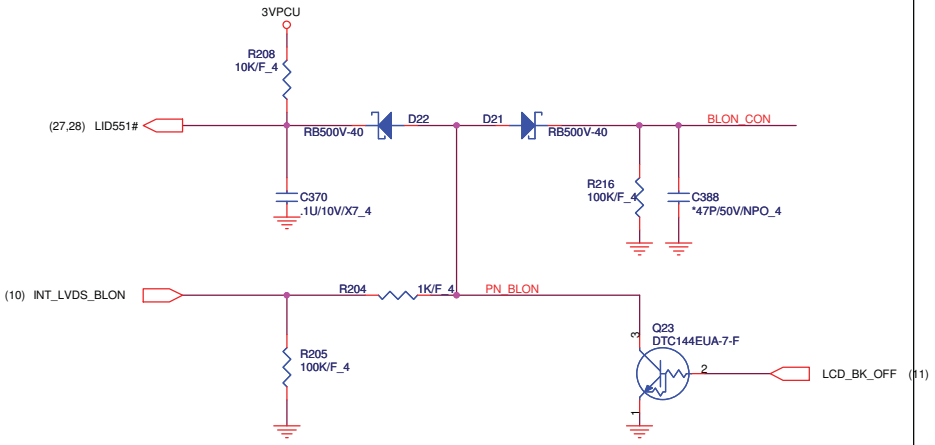


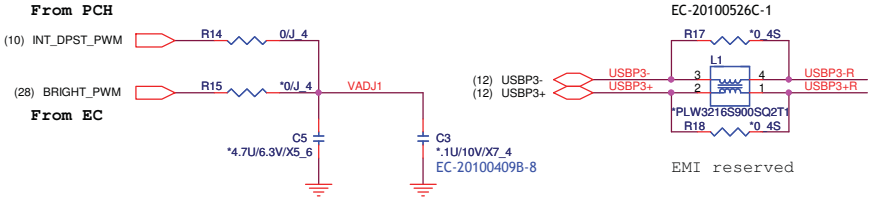


SUPPORT 13.3" LED TYPE LCD

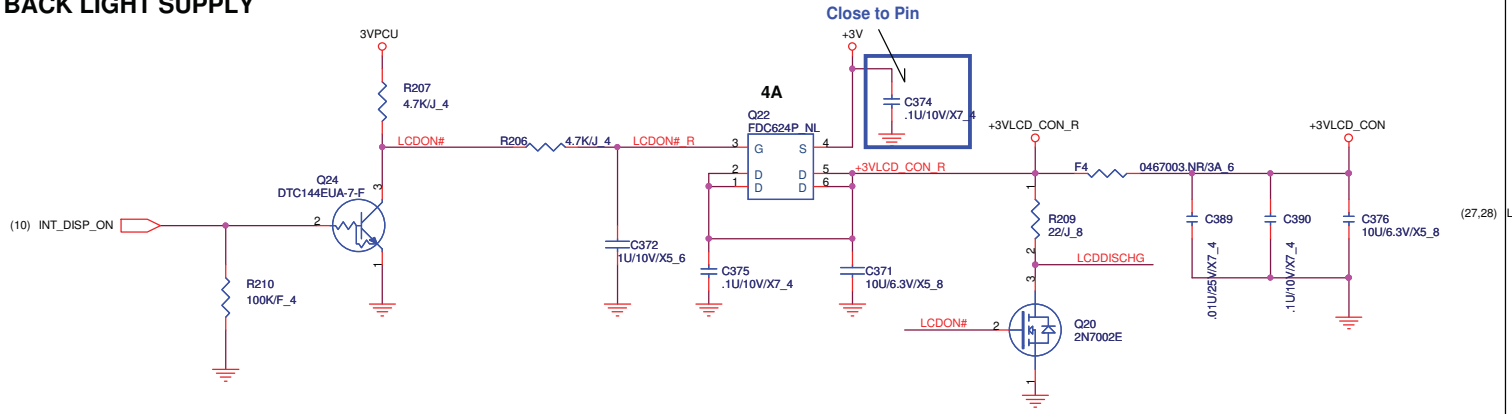


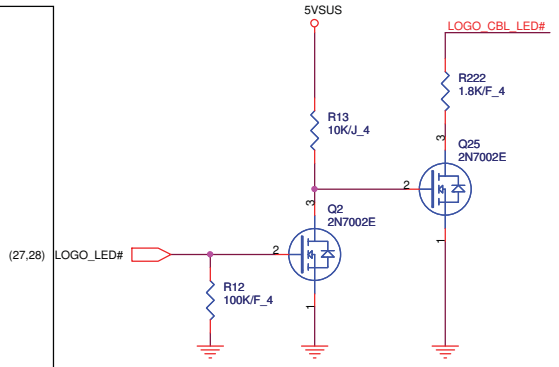
BACK LIGHT CONTROL





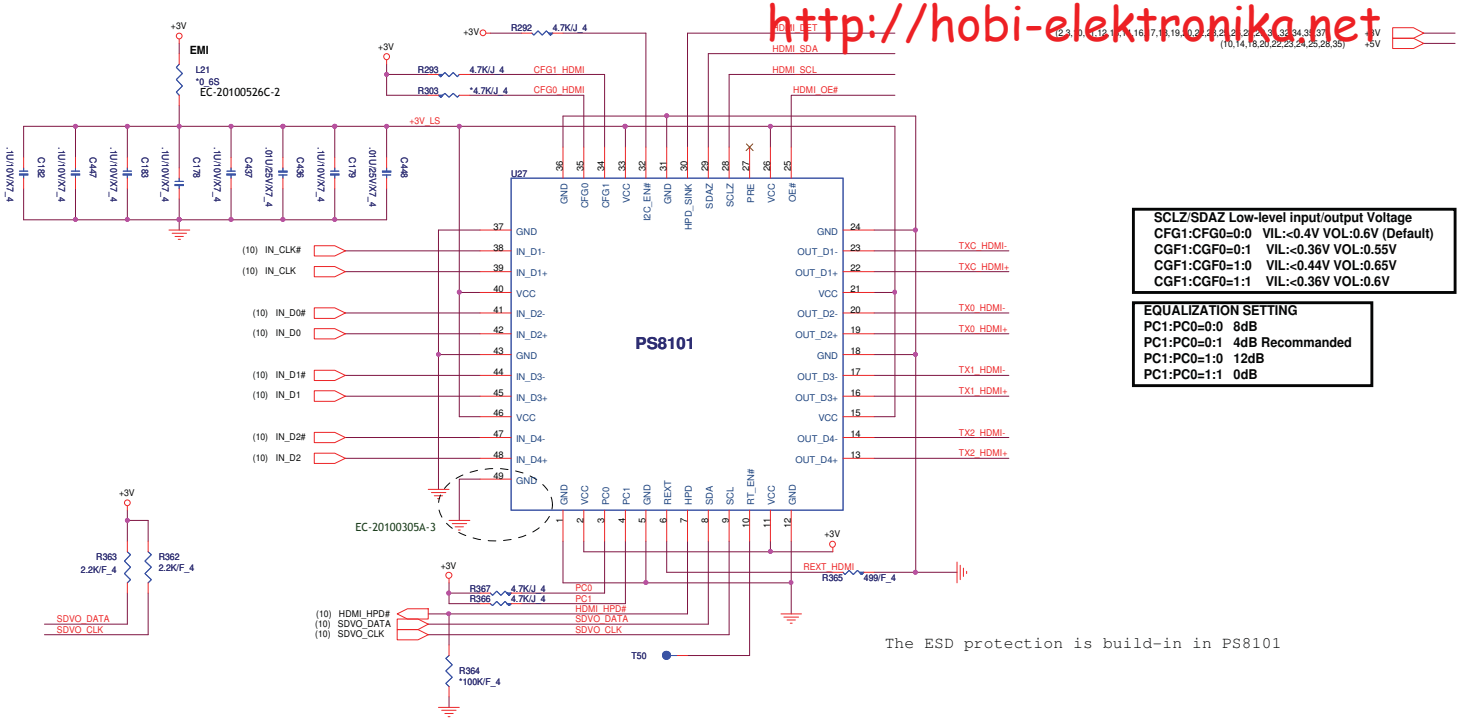
BACK LIGHT SUPPLY





PROJECT : PS2
Quanta Computer Inc.

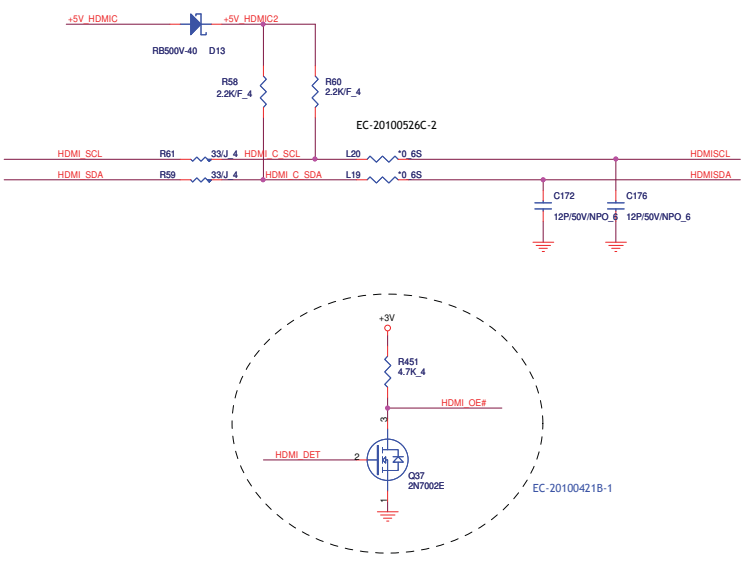
Size	Document Number	Rev
Custom	<Doc> CONN (LVDS, CCD)	1A
Date: Friday, June 04, 2010	Sheet 20 of 44	

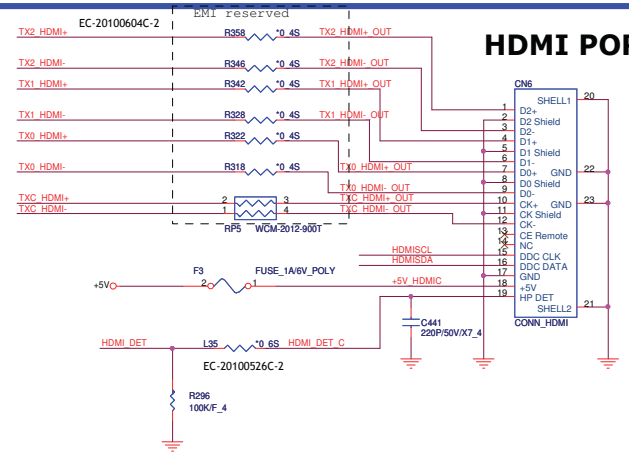


SCLZ/SDAZ Low-level input/output Voltage
CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF1:CGF0=0:1 VIL:<0.36V VOL:0.55V
CGF1:CGF0=1:0 VIL:<0.44V VOL:0.65V
CGF1:CGF0=1:1 VIL:<0.36V VOL:0.6V

EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

The ESD protection is build-in in PS8101





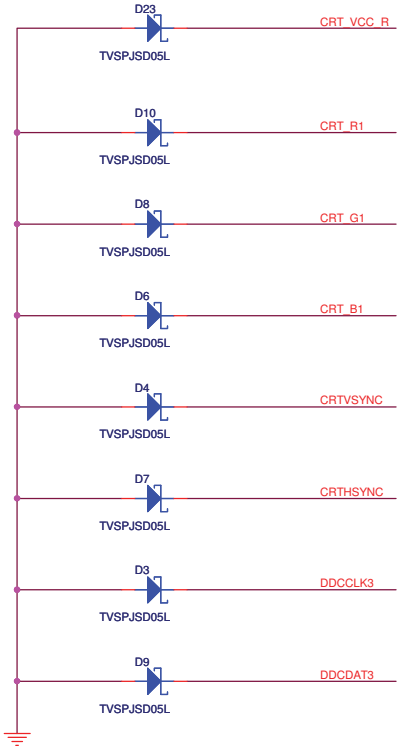
HDMI PORT

PROJECT : PS2		
Quanta Computer Inc.		
Size: C	Document Number: <Doc> CONN (HDMI, level Shift)	Rev: 1A
Date: Friday, June 04, 2010	Sheet 21 of 44	

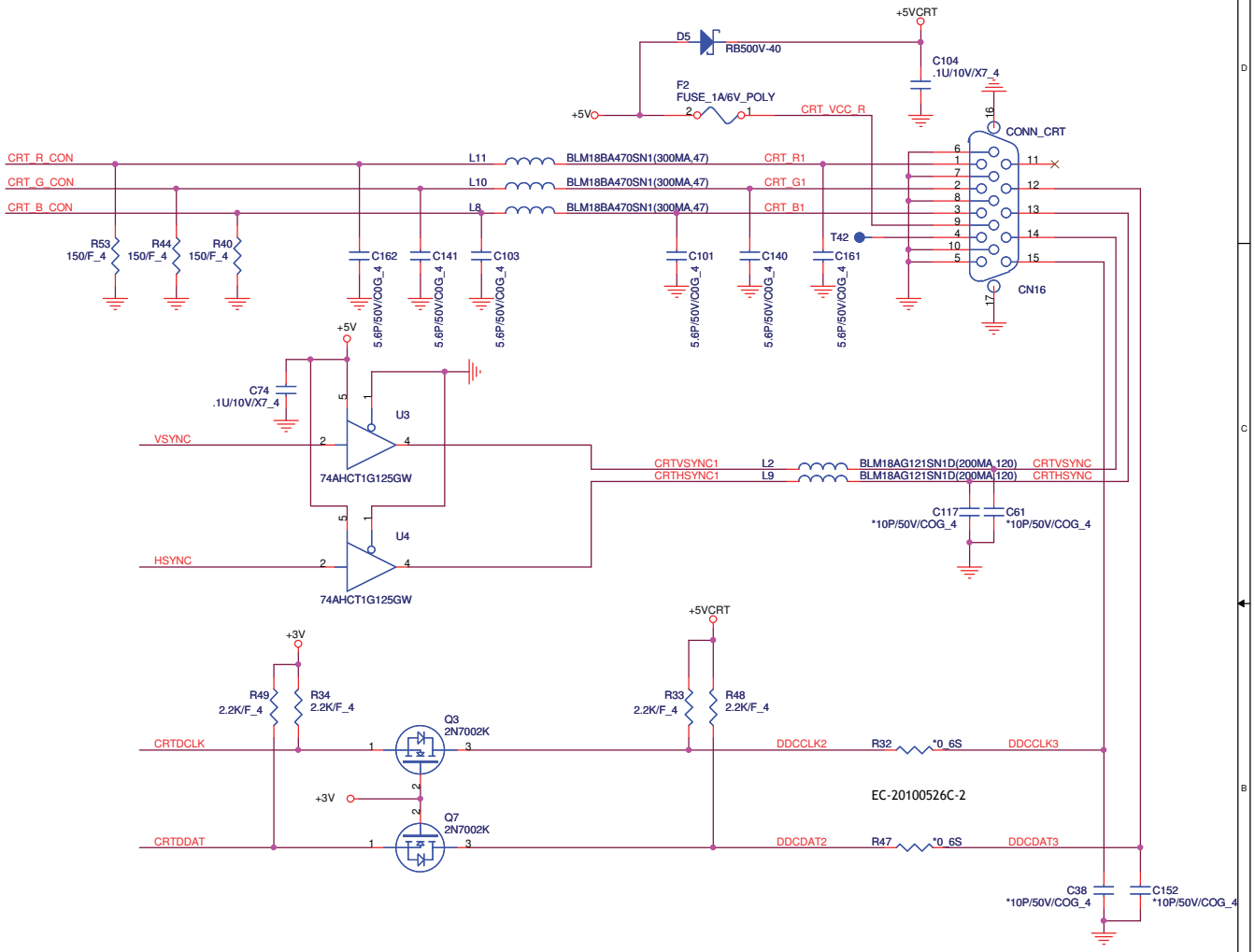
New Tooling footpint was on-Going 0730

CRT PORT

(10) CRT_R_CON → CRT_R_CON
(10) CRT_G_CON → CRT_G_CON
(10) CRT_B_CON → CRT_B_CON
(10) HSYNC → HSYNC
(10) VSYNC → VSYNC
(10) CRTDCLK → CRTDCLK
(10) CRTDDAT → CRTDDAT



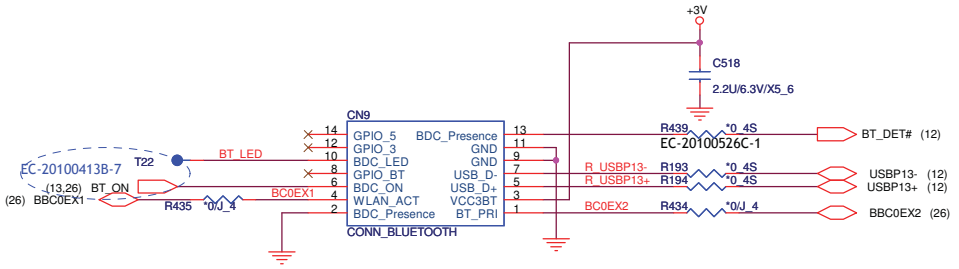
By ESD suggestion



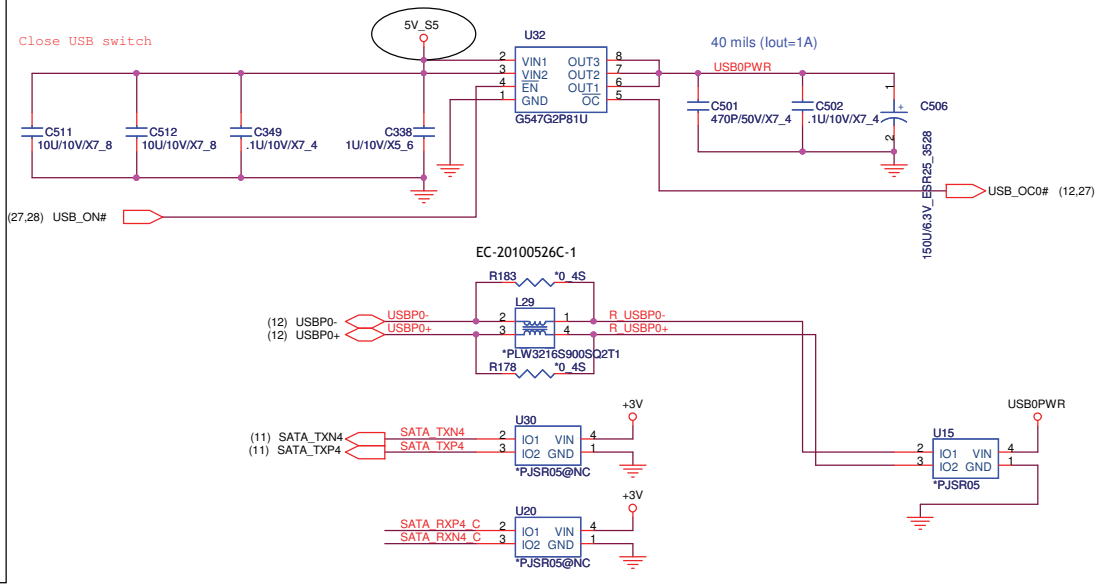
PROJECT : PS2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> CONN (CRT)	1A
Date: Wednesday, May 26, 2010	Sheet 22 of 44	

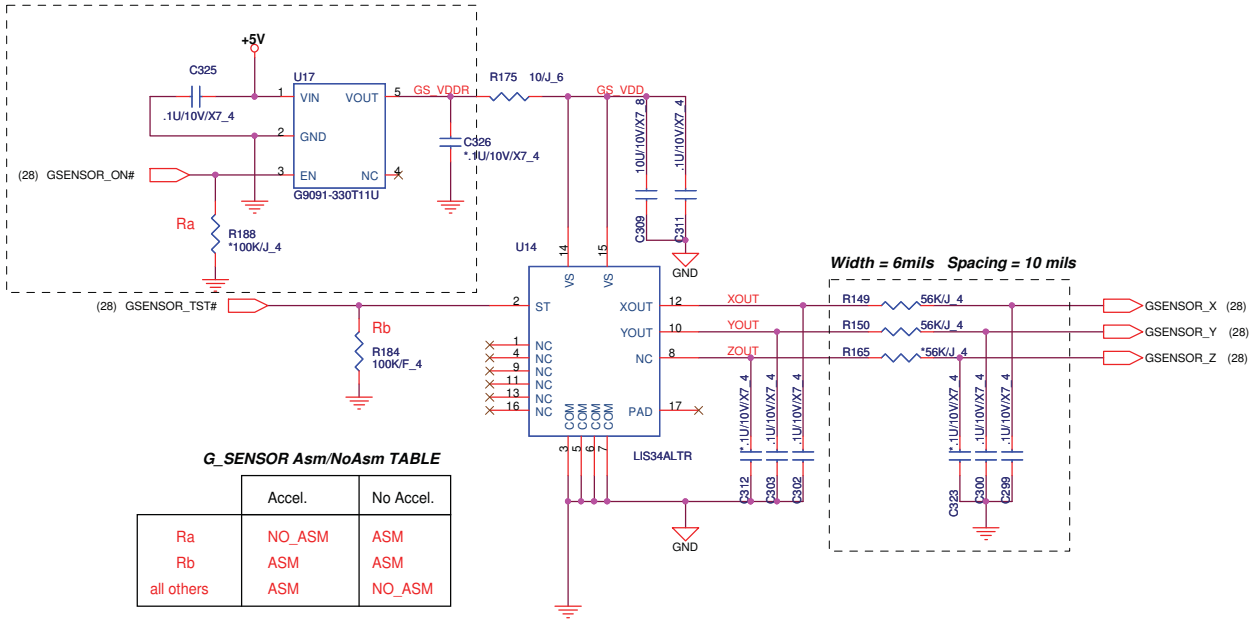
Blue Tooth control



USB+E-SATA



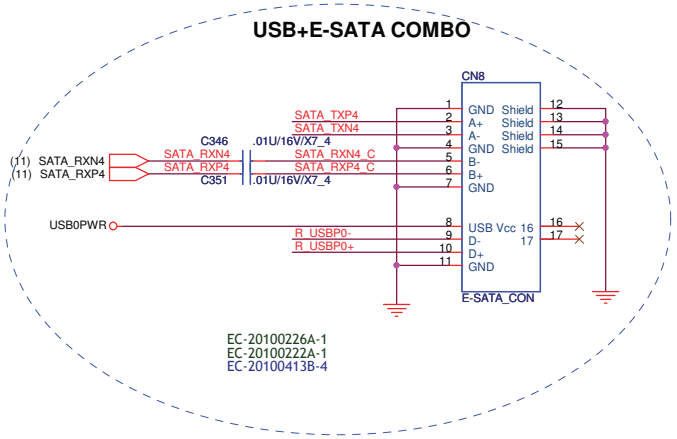
Accelerometer Sensor



G_SENSOR Asm/NoAsm TABLE

	Accel.	No Accel.
Ra	NO_ASM	ASM
Rb	ASM	ASM
all others	ASM	NO_ASM

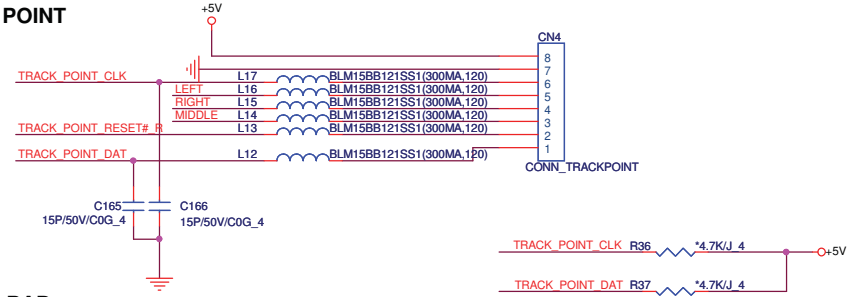
USB+E-SATA COMBO



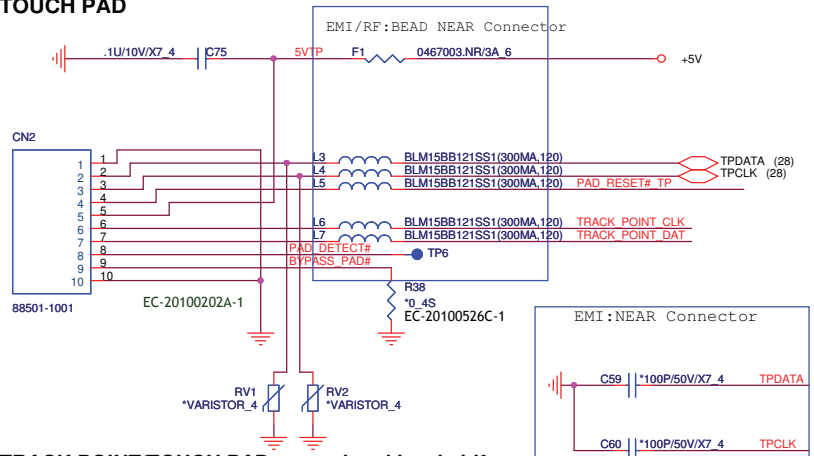
PROJECT :PS2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> CONN (ESATA, BT, G sensor)	1A
Date: Wednesday, May 26, 2010	Sheet 23 of 44	

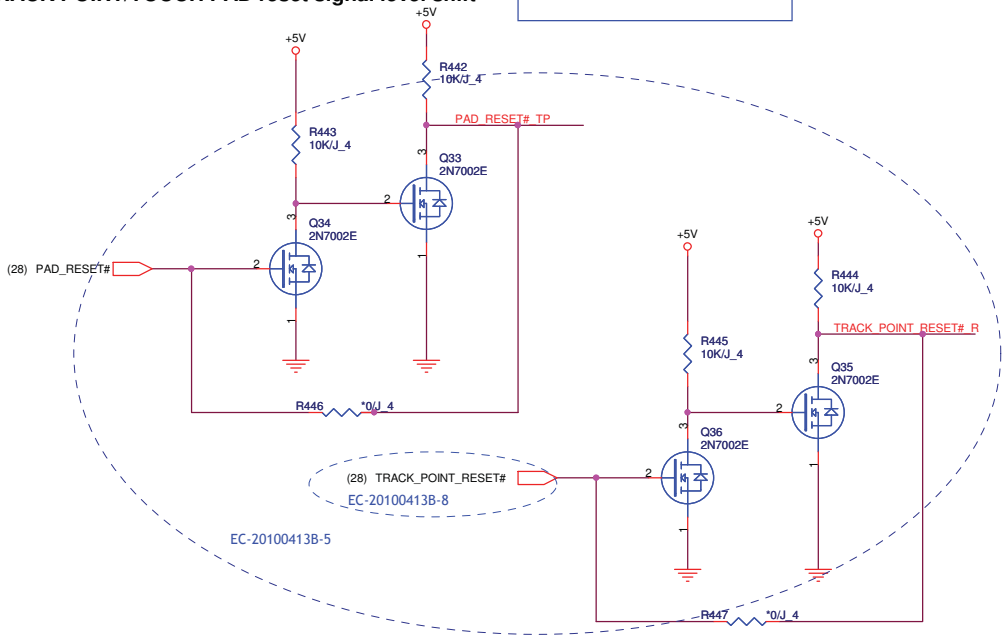
TRACK POINT

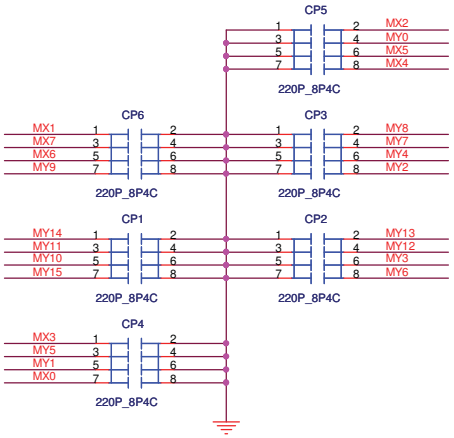


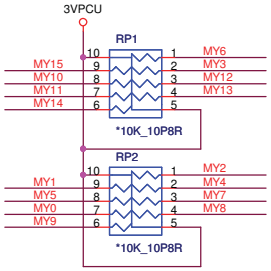
TOUCH PAD



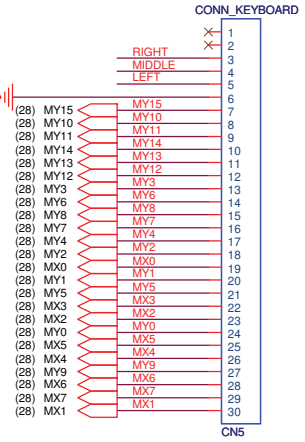
TRACK POINT/TOUCH PAD reset signal level shift







KEYBOARD connector



CONN (KB, TP, TrackPoint)

PROJECT : PS2

Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc>	1A

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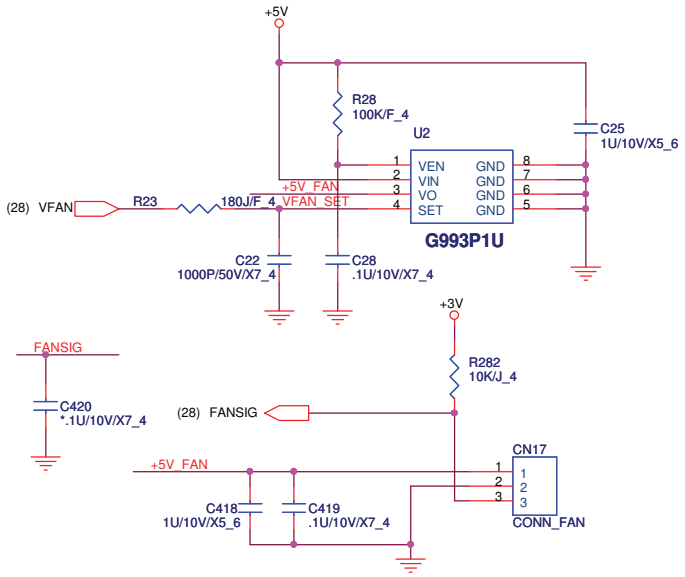
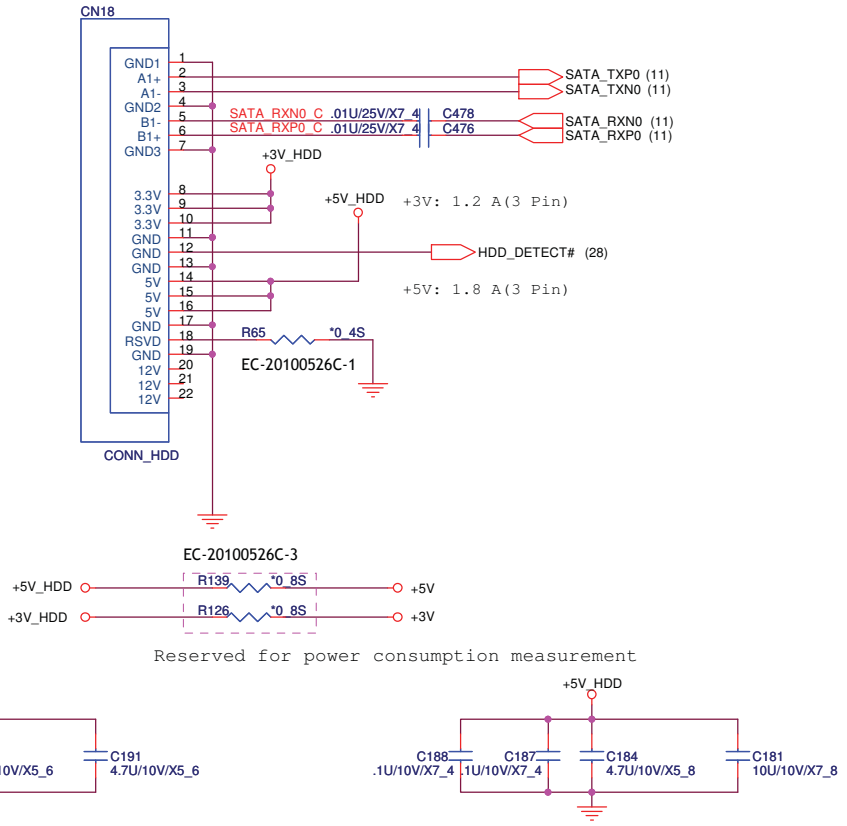
FAN CONTROL



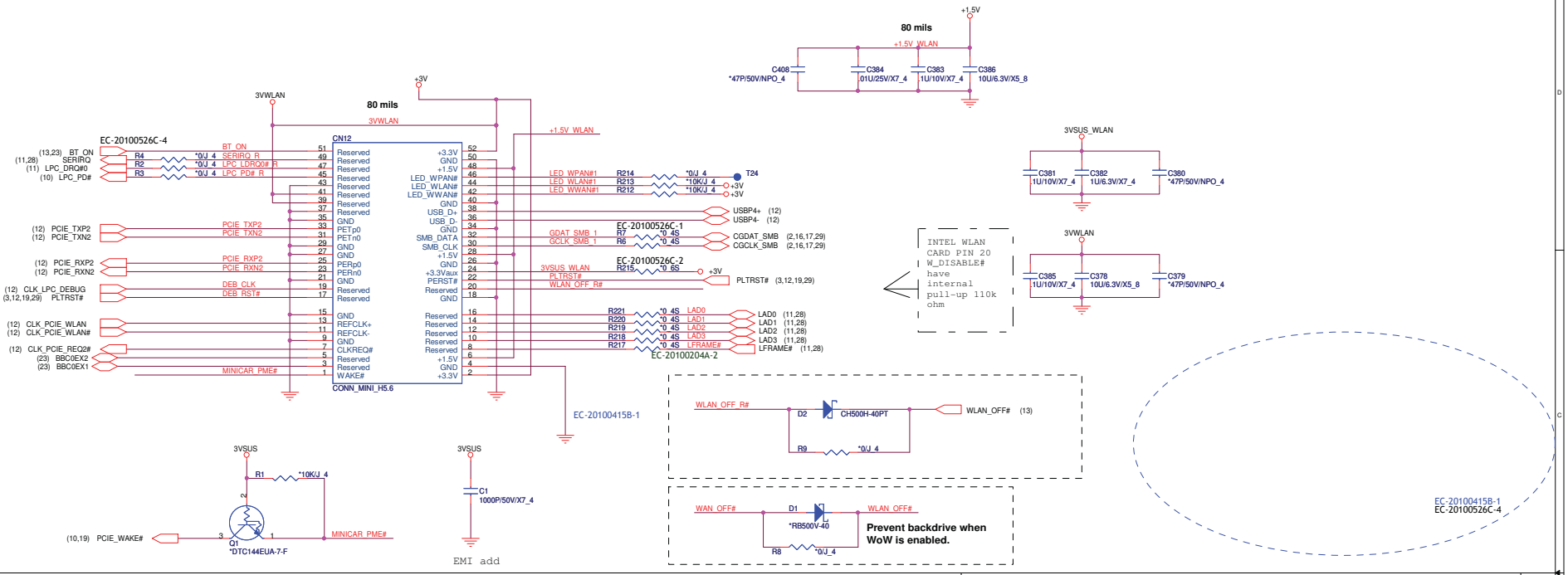
SATA-HDD CONNECTOR



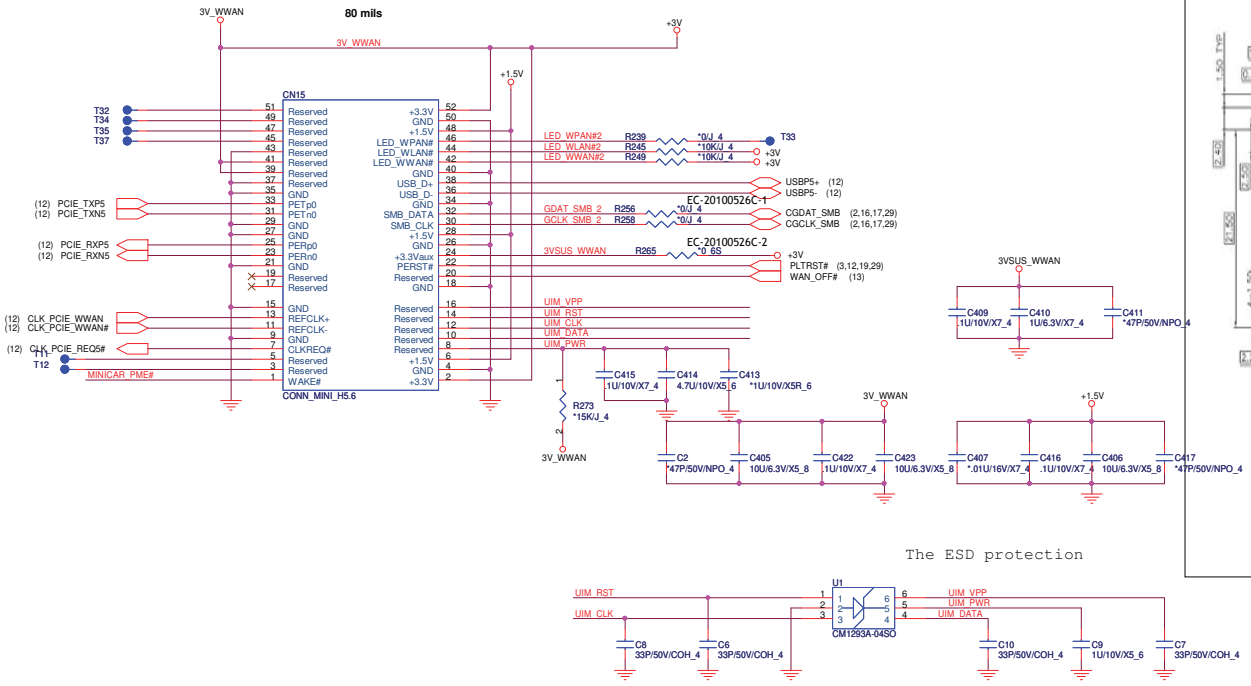
PROJECT : PS2
Quanta Computer Inc.

Size	Document Number	Rev
B	<Doc> CONN (HDD, FAN)	1A
Date: Wednesday, May 26, 2010	Sheet 25 of 44	

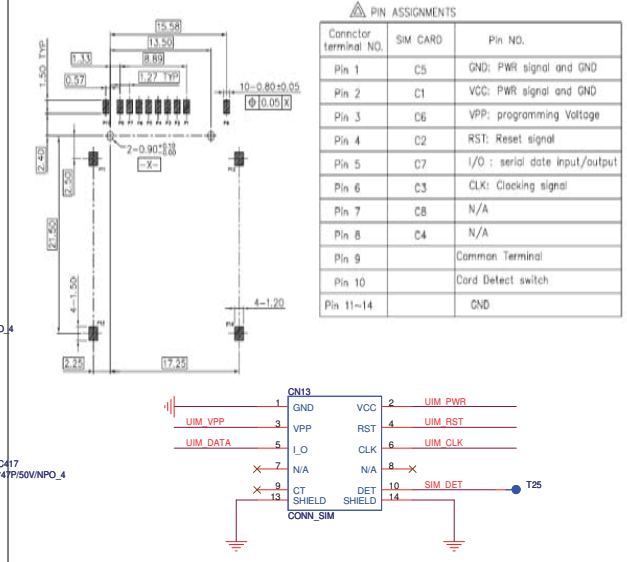
Mini PCI-E Card 1
WLAN



Mini PCI-E Card 2
WWAN(W/SIM)



SIM SOCKET



PIN ASSIGNMENTS

Connector terminal NO.	SIM CARD	Pin NO.
Pin 1	C5	GND: PWR signal and GND
Pin 2	C1	VCC: PWR signal and GND
Pin 3	C6	VPP: programming Voltage
Pin 4	C2	RST: Reset signal
Pin 5	C7	I/O : serial date input/output
Pin 6	C3	CLK: Clocking signal
Pin 7	C8	N/A
Pin 8	C4	N/A
Pin 9		Common Terminal
Pin 10		Card Detect switch
Pin 11~14		GND

PROJECT : PS2
Quanta Computer Inc.

Size	Document Number	Rev
C	<Doc> CONN (MINI PCI-E, SIM)	1A

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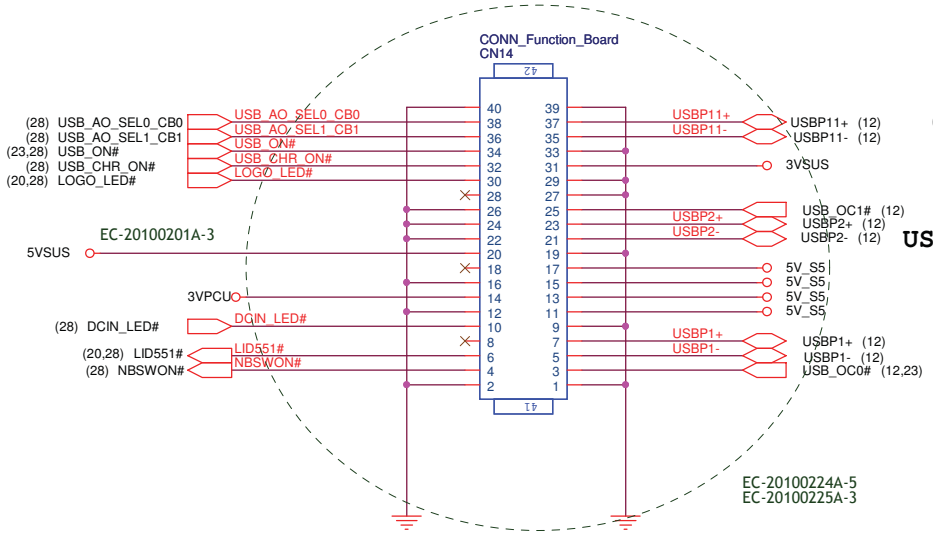
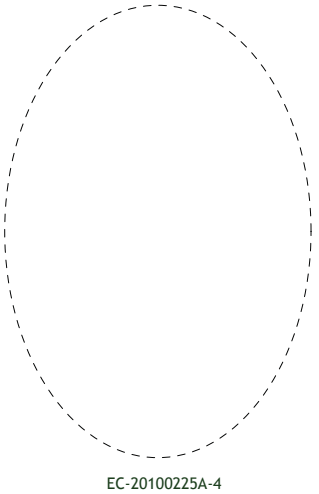
Function Board

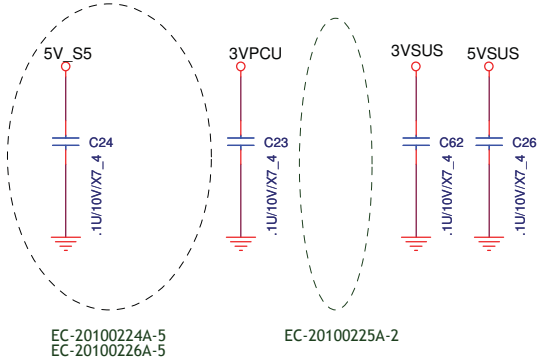


CARD READER

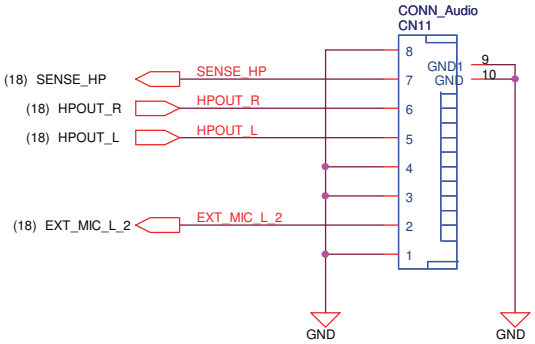
USB PORT(S5 Charger)

USB PORT

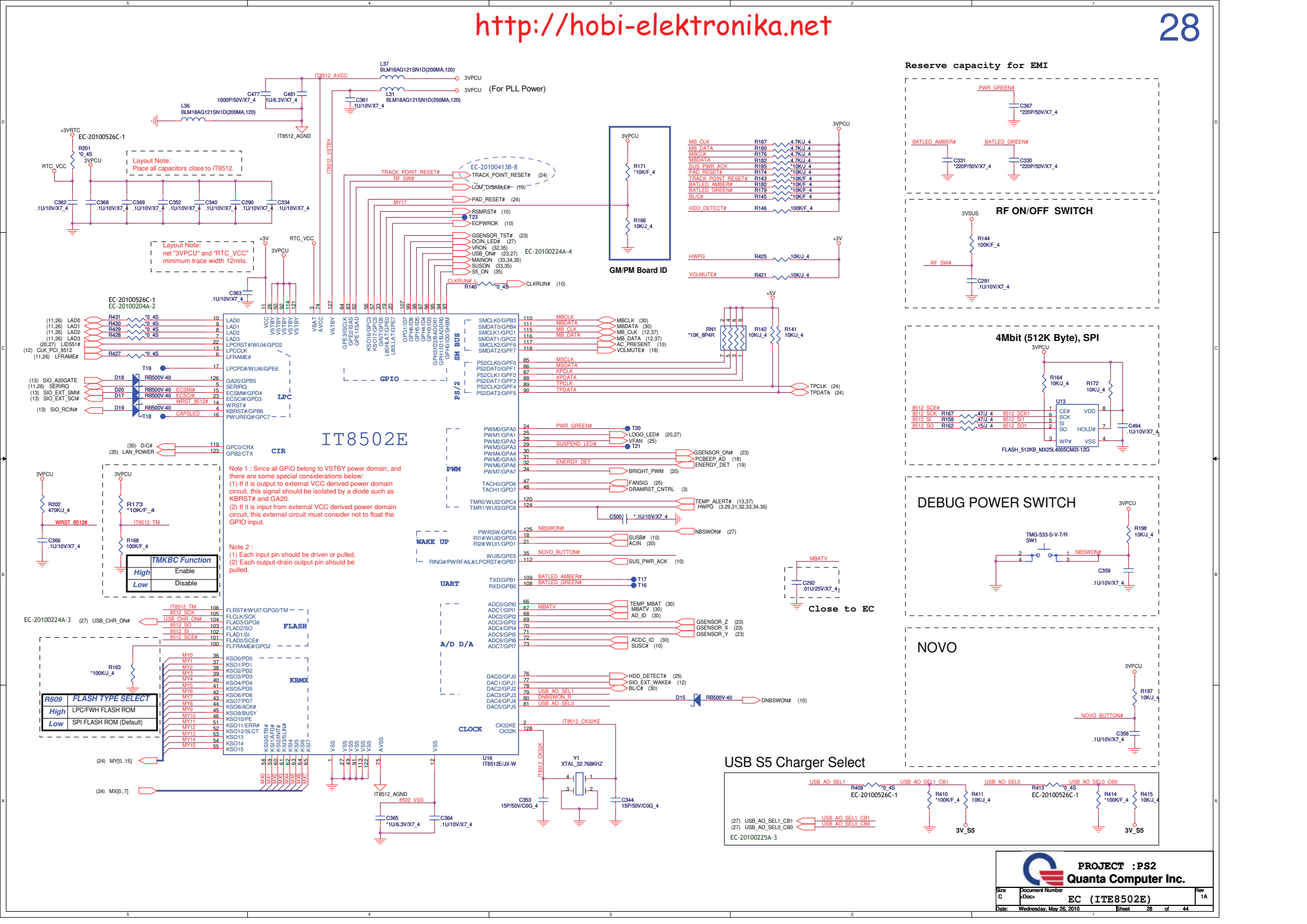




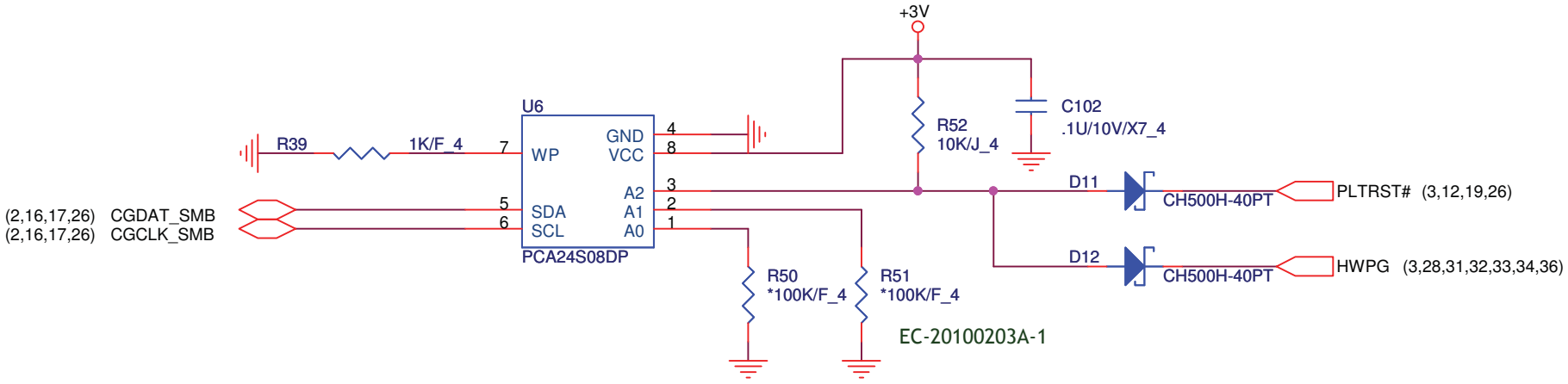
Audio connect



PROJECT : PS2		
Quanta Computer Inc.		
Size: B	Document Number: <Doc> CONN (Wire to Board)	Rev: 1A
Date: Tuesday, May 25, 2010	Sheet 27 of 44	



RFID EEPROM

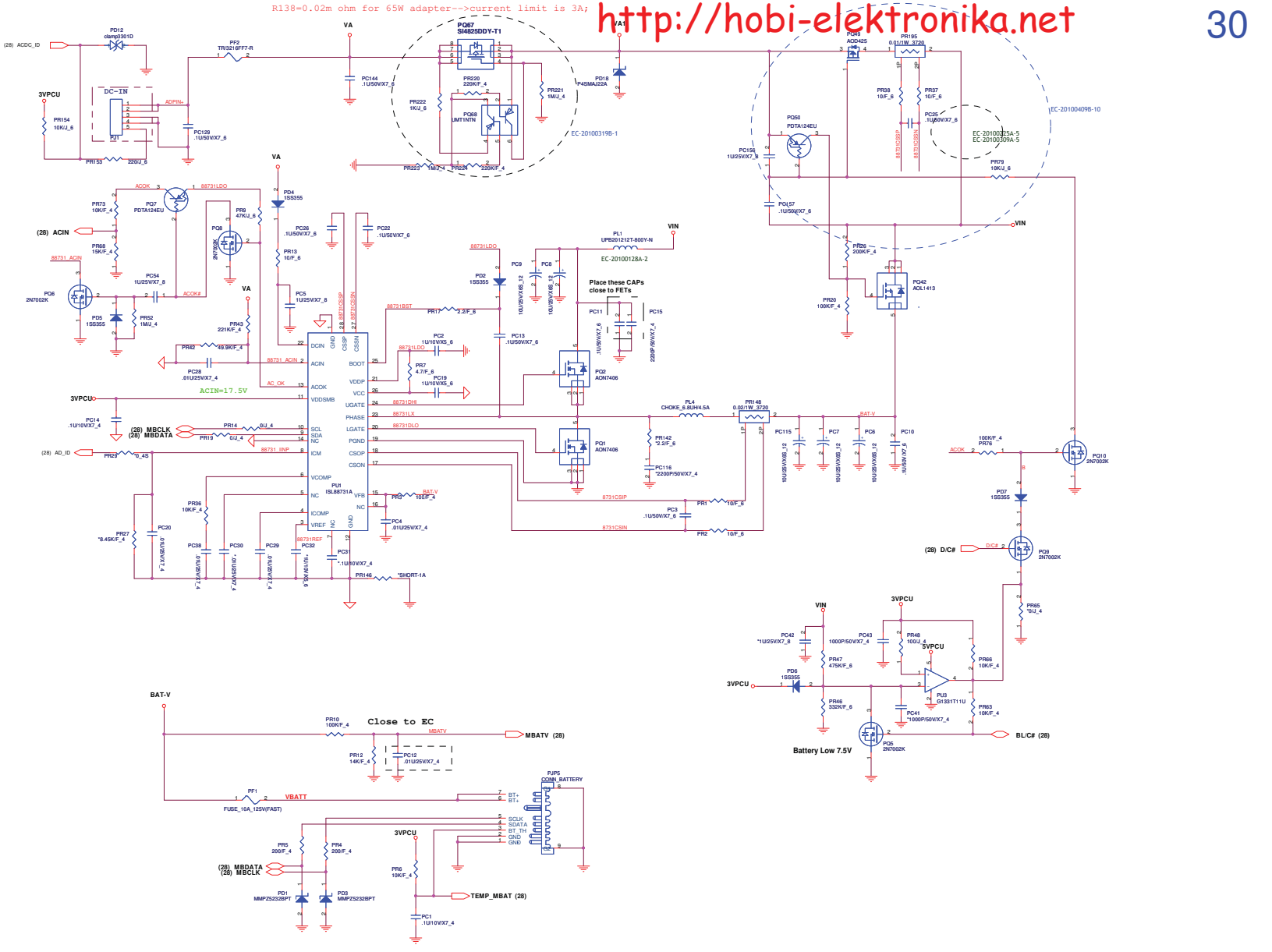


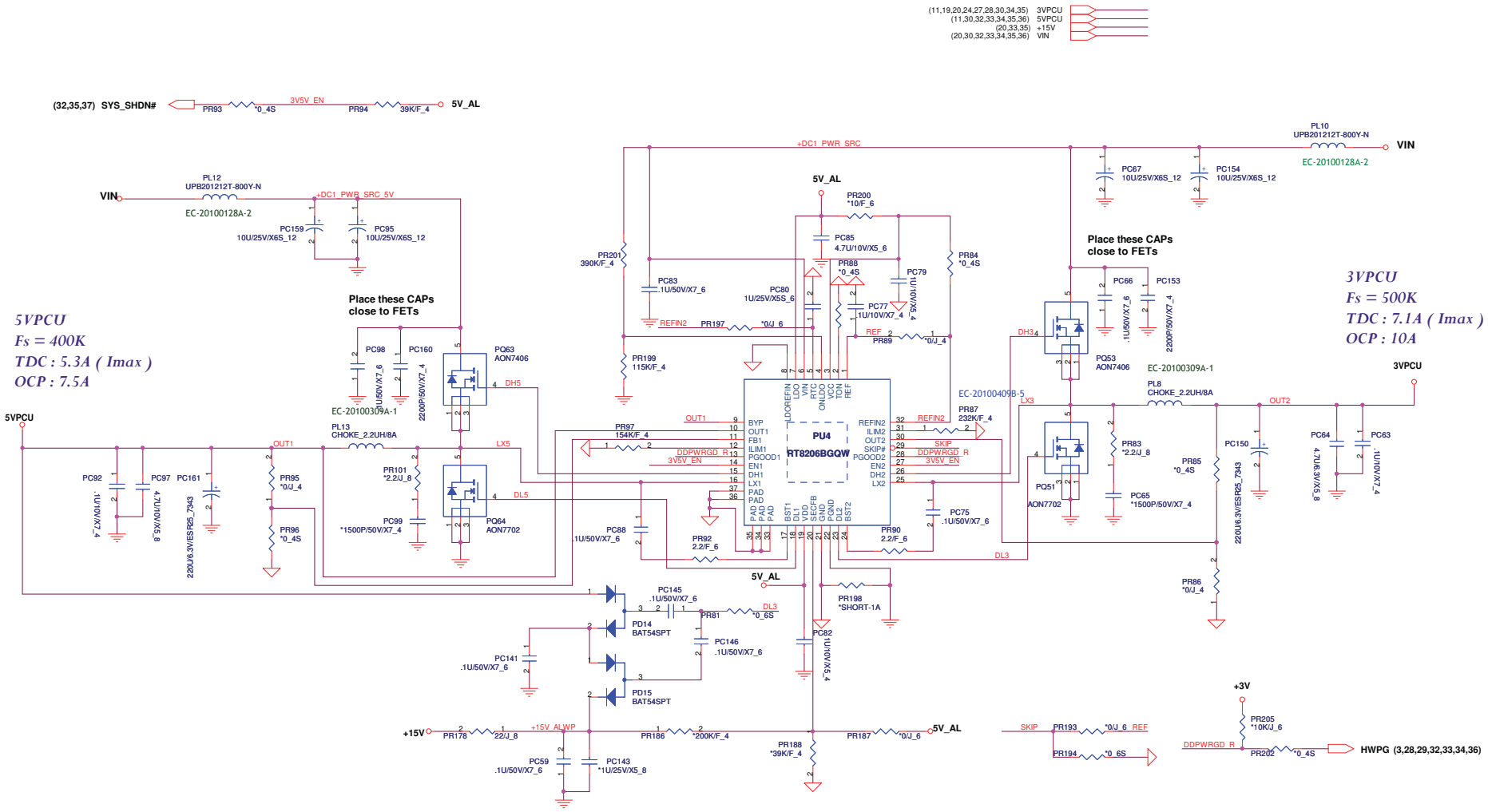
PROJECT :PS2

Quanta Computer Inc.

Size	Document Number	Rev
A	<Doc> RFID EEPROM	1A
Date: Tuesday, May 25, 2010	Sheet 29 of 44	

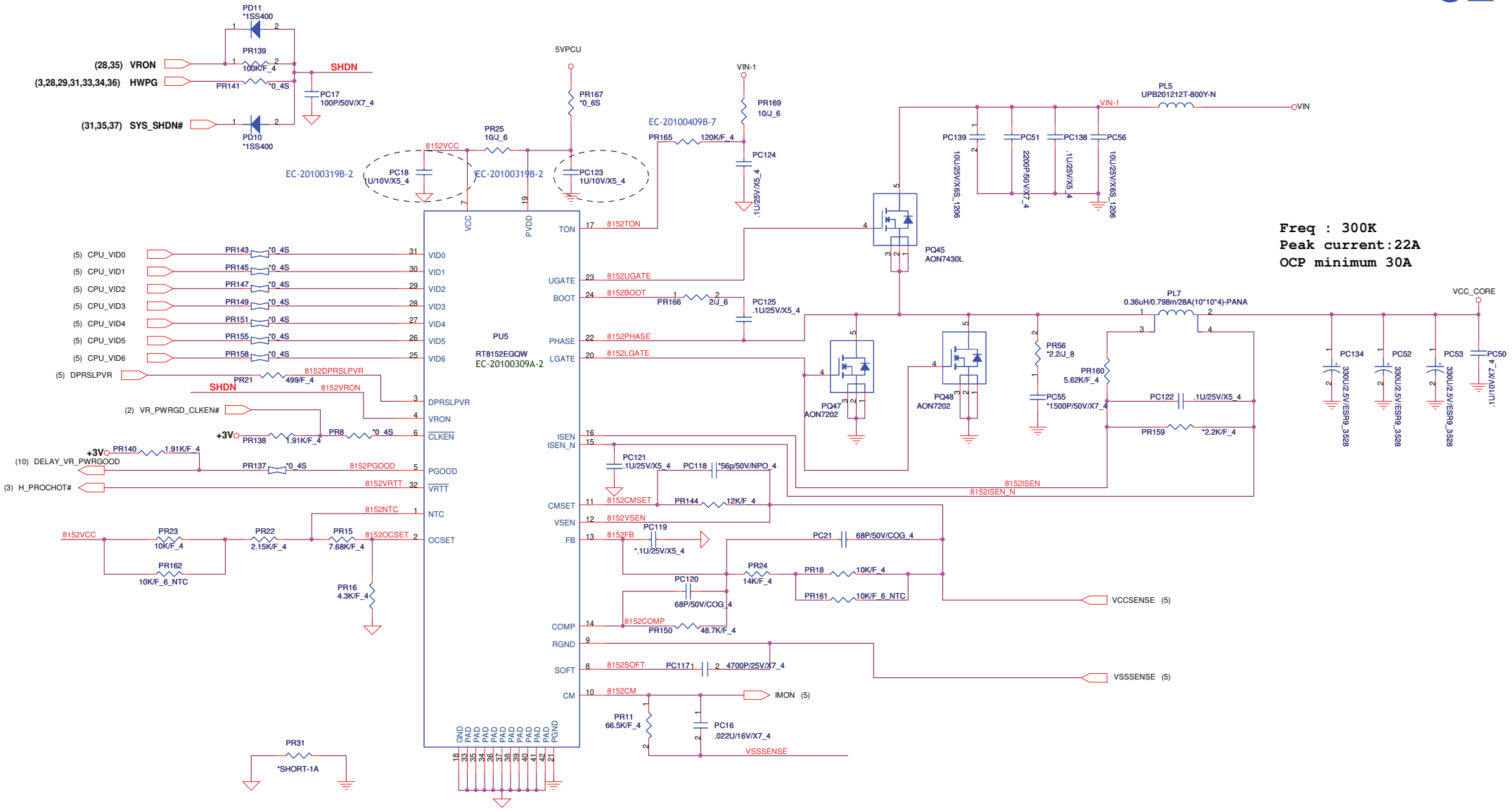
R138=0.02m ohm for 65W adapter-->current limit is 3A;





EC-20100526C-1

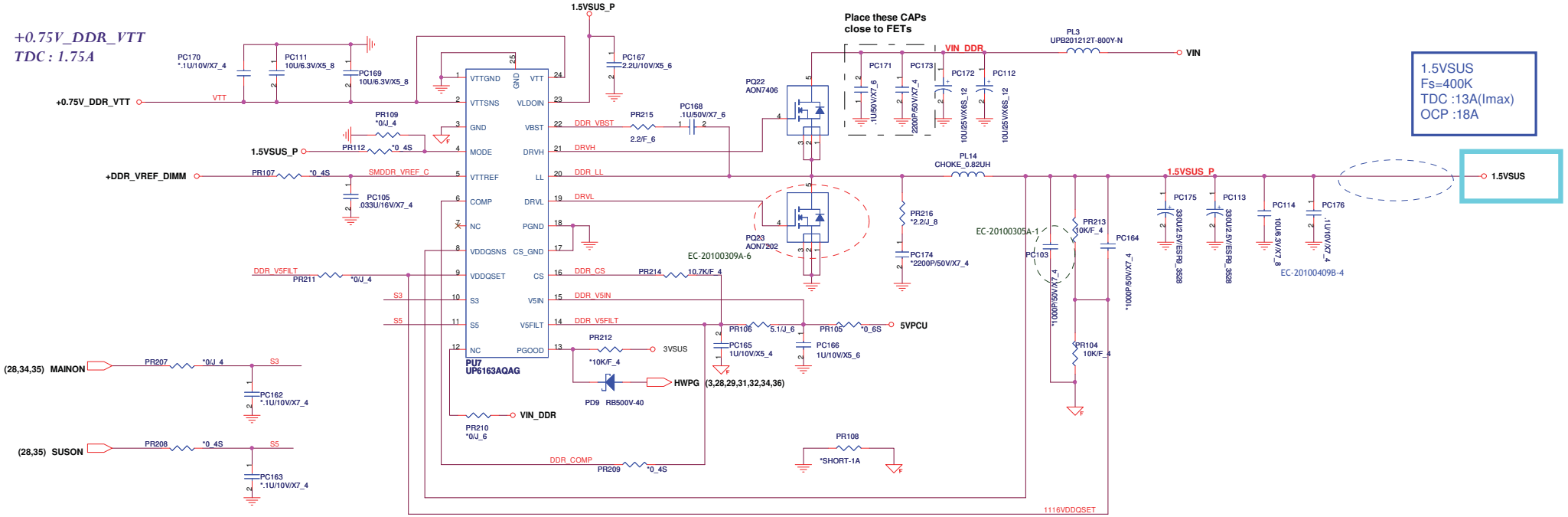
PROJECT : PS2 Quanta Computer Inc.			
Size: Custom	Document Number: <Doc> POWER_3V/5V (ISL6237)		Rev: 1A
Date: Wednesday, May 26, 2010	Sheet 31 of 44		



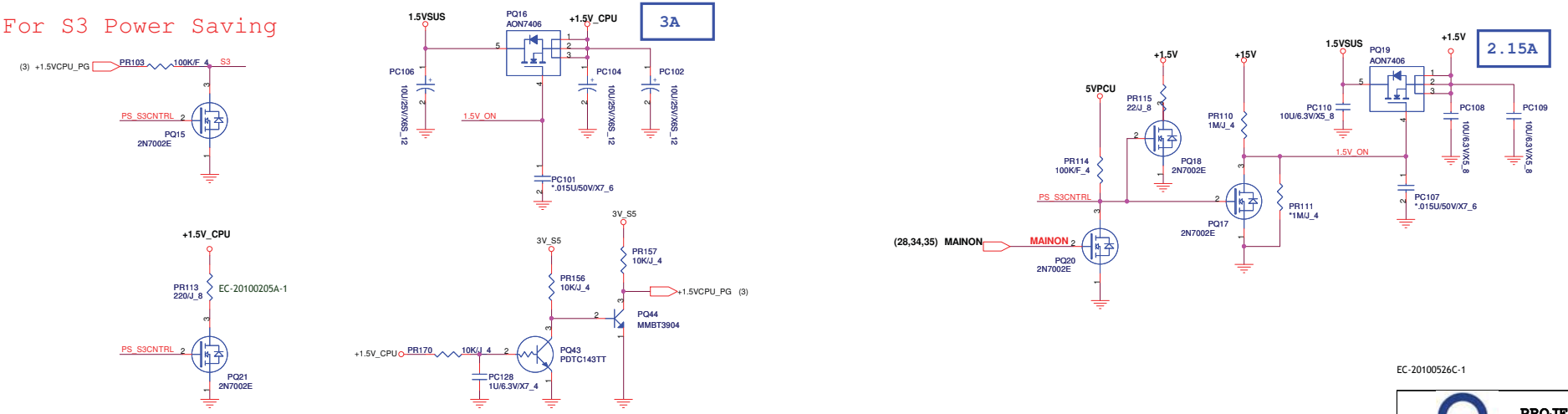
EC-20100526C-1

PROJECT :PS2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> POWER_CPU CORE (RT8152B)	1A
Date: Wednesday, May 26, 2010	Sheet 32 of 44	



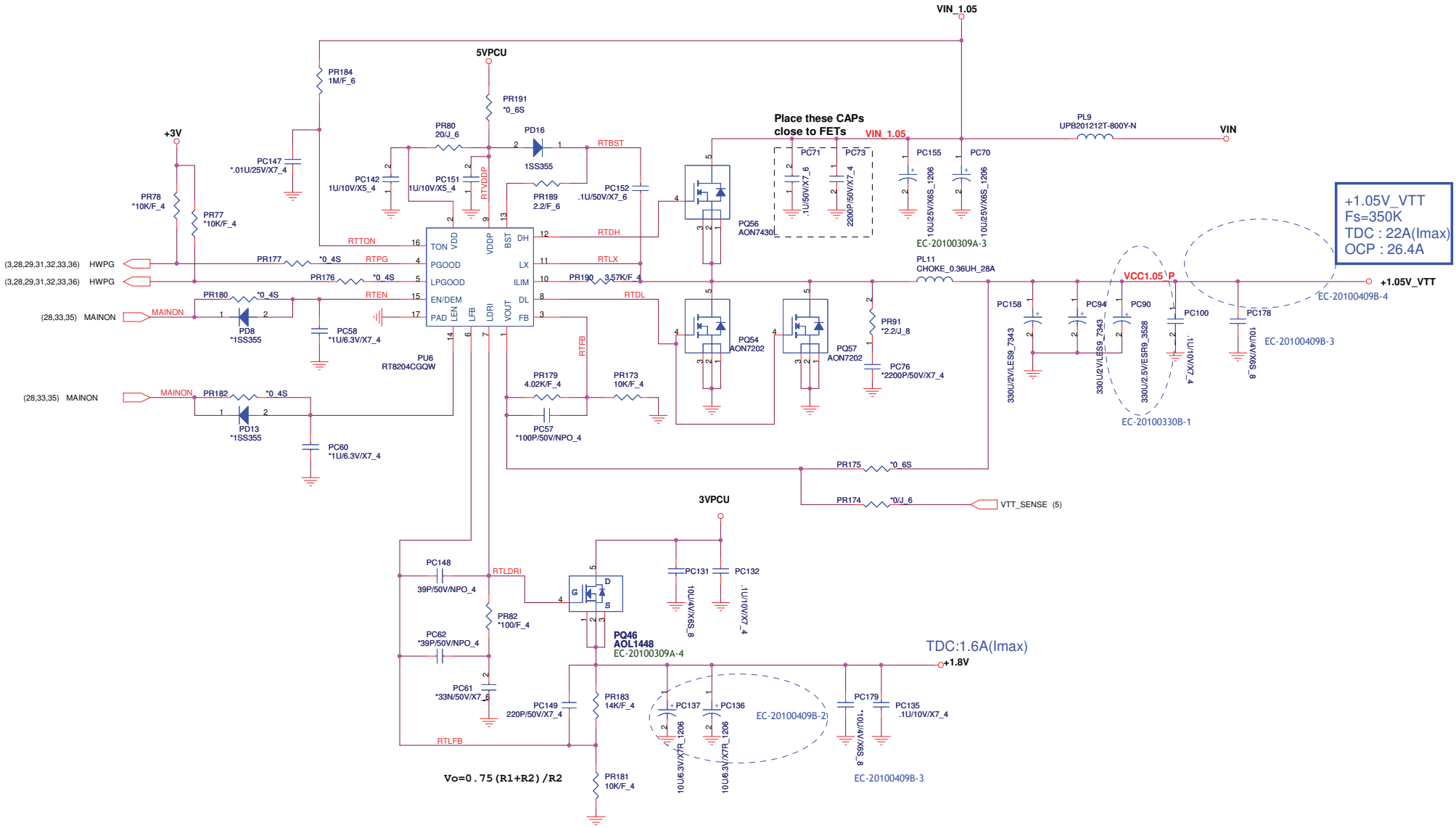
For S3 Power Saving



EC-20100526C-1

PROJECT : PS2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> POWER_DDR3 (TPS51116)	1A
Date: Wednesday, May 26, 2010	Sheet 33 of 44	

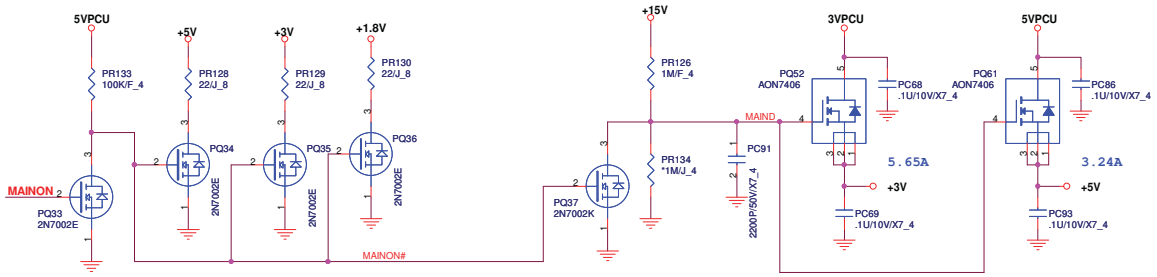


EC-20100526C-1

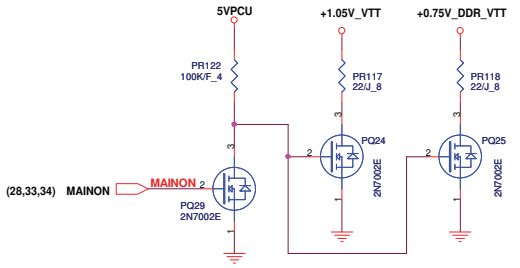
PROJECT : PS2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> POWER_1.05V&1.5V(RT8204C)	1A
Date: Wednesday, May 26, 2010	Sheet 34 of 44	

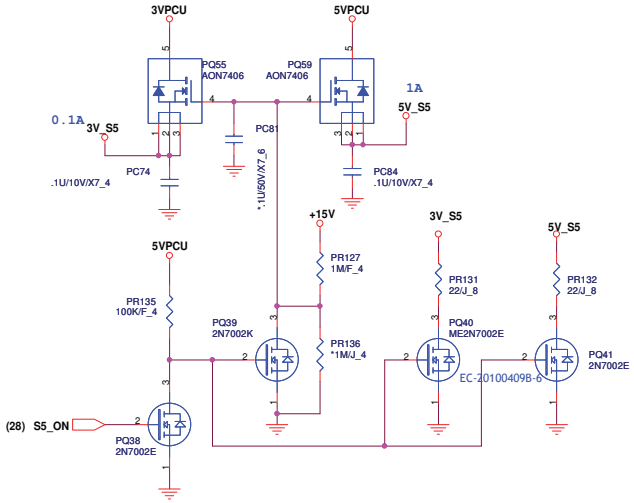
+3V, +5V



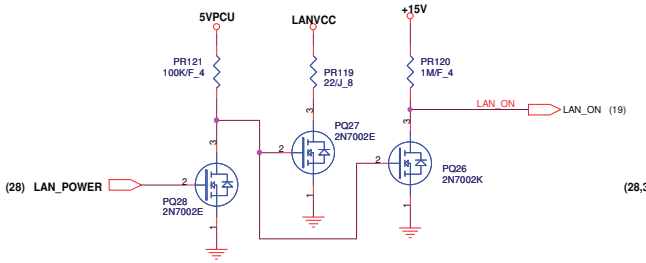
+1.05V, SMDDR_VTERM



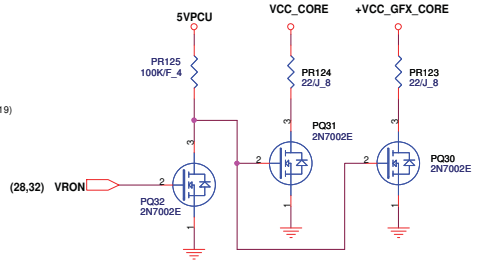
3V_S5, 5V_S5

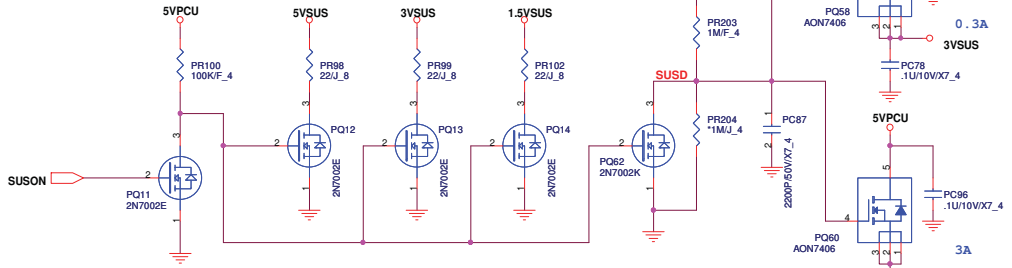


LANVCC

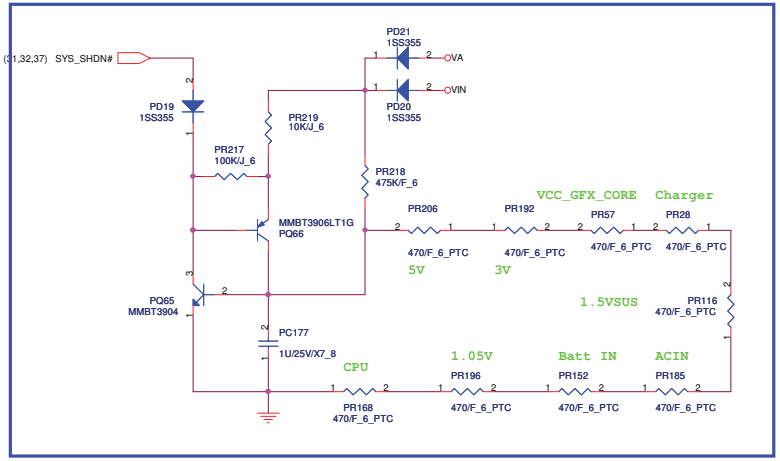


VCC_CORE



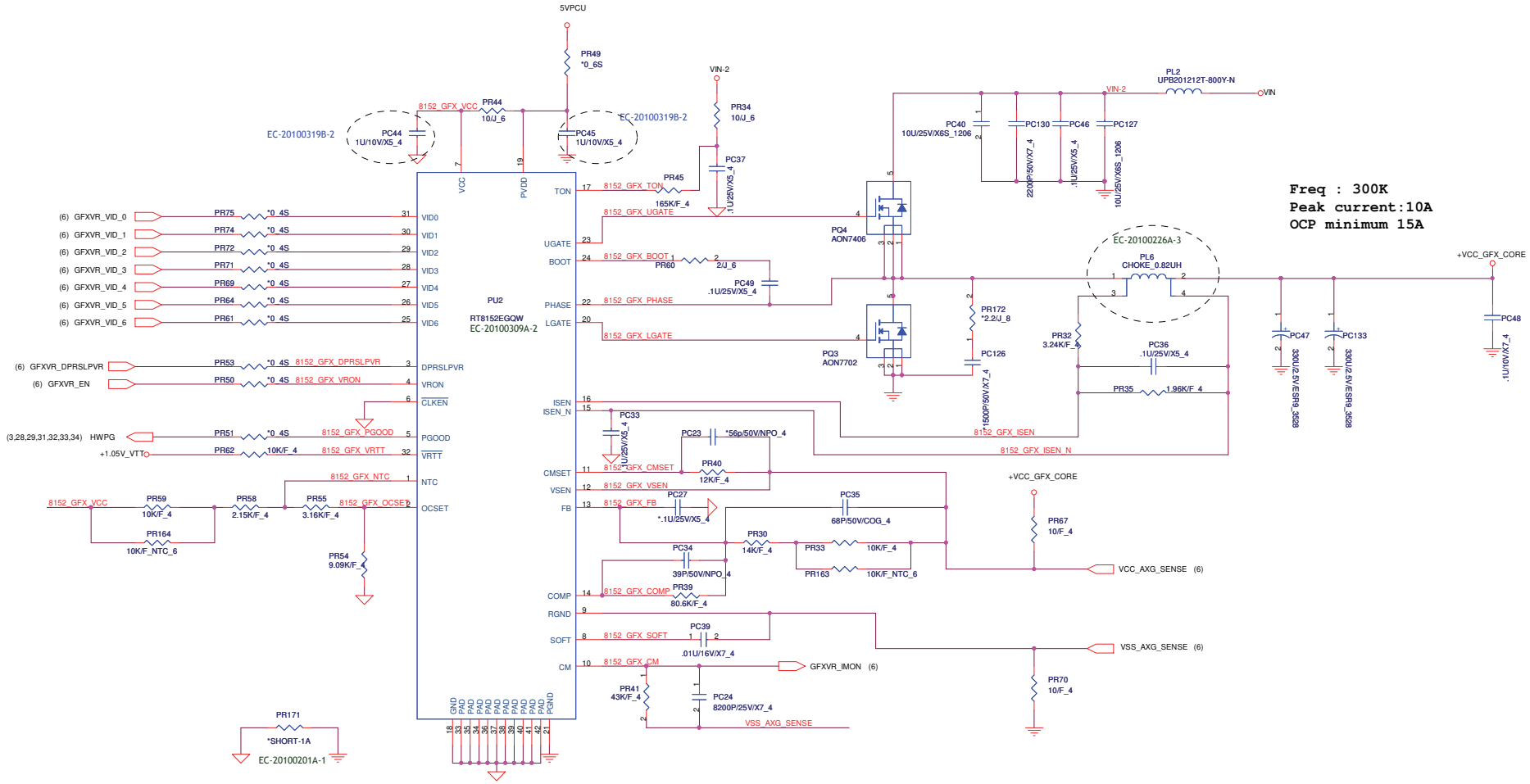


3VSUS, 5VSUS, 1.8VSUS



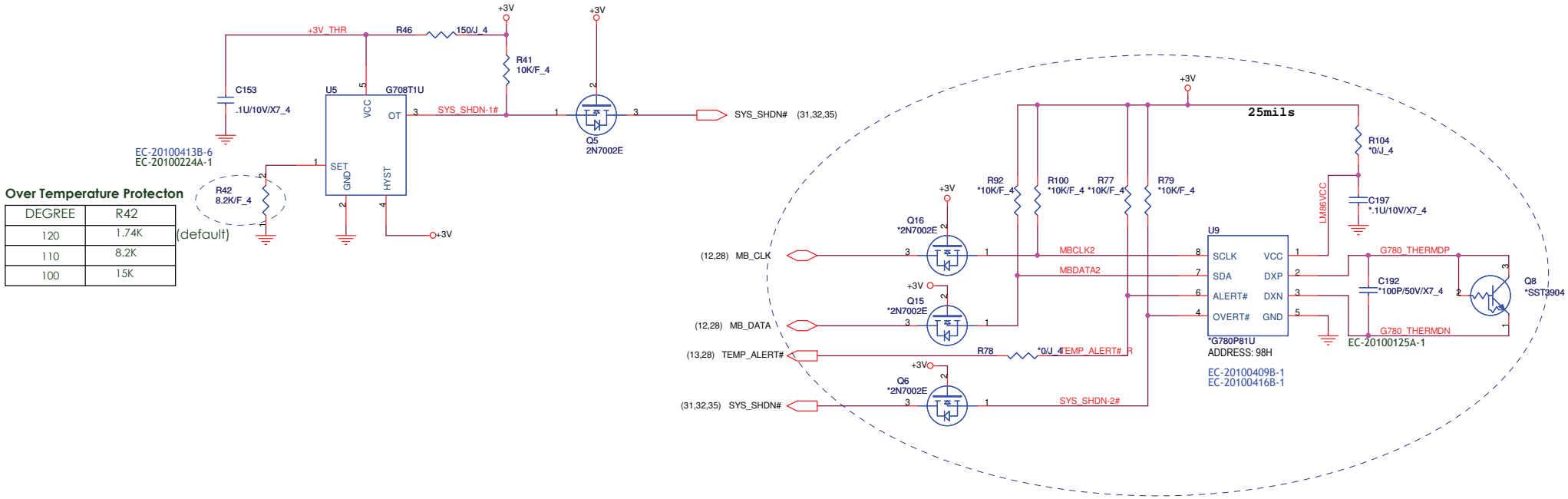
PROJECT :PS2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> POWER_Discharge	1A
Date: Tuesday, May 25, 2010	Sheet 35 of 44	



EC-20100526C-1

PROJECT : PS2 Quanta Computer Inc.			
Size: Custom	Document Number: <Doc> POWER_GFX_CORE		Rev: 1A
Date: Wednesday, May 26, 2010	Sheet 36 of 44		



PROJECT :PS2

Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> Thermal Protect	1A
Date: Tuesday, May 25, 2010	Sheet 37 of 44	

HOLE10 *H-C142D142N
HOLE5 *H-C142D142N
HOLE11 *H-C142D142N
HOLE6 *H-C142D142N
CPU NUT
EC-20100128A-1

HOLE23 H-TC197BC158D122P2
HOLE24 H-TC197BC158D122P2
PCH NUT

SB NUT

HOLE19 H-TC167BC51D51PT
HOLE20 H-TC167BC51D51PT
WWAN NUT

HOLE21 H-TC167BC51D51PT
HOLE22 H-TC167BC51D51PT
WLAN NUT

HOLE14 H-TC236BC154D118P2
Bluetooth NUT

+1.05V_VTT
C229 .1U/10V/X7_4
C222 .1U/10V/X7_4
C194 .1U/10V/X7_4
C286 .1U/10V/X7_4
C177 .1U/10V/X7_4
C167 .1U/10V/X7_4
C421 .1U/10V/X7_4
C255 .1U/10V/X7_4
EC-20100201A-2
EMI reserved

HOLE1 *H-C236D91P2
HOLE3 *H-C236D91P2
HOLE9 *H-C236D91P2
HOLE7 *H-C236D91P2
HOLE18 *H-236CD91P2
HOLE17 *H-C236D98P2
HOLE15 *H-C236D91P22
HOLE13 *H-C236D91P2
MB Screw Hole

HOLE2 *H-C78D78N
HOLE16 *H-C78D78N
MB latch Hole

SPAD13 *SPAD-SHAPE164X613NP
SPAD8 *spad-re270x290NP
SPAD4 *spad-re330x240NP
SPAD3 *spad-re350x390NP
SPAD12 *SPAD-RE151X150NP
SPAD5 *SPAD-RE151X150NP
SPAD1 *spad-shape260x2428NP
SPAD10 *spad-shape266x354NP
SPAD7 *SPAD-SHAPE326X169NP
SPAD2 *spad-shape348x368NP
SPAD9 *SPAD-SHAPE348X386NP
SPAD14 *SPAD-SHAPE326X169NP
SPAD11 *SPAD-RE350X390NP
SPAD15 *SPAD-RE240X470NP
SPAD16 *SPAD-RE330X240NP
EC-20100526C-5
EC-20100304A-1
EC-20100413B-2
PCB SPAD for ESD

HOLE4 *H-TC138BC236D118P2
KB Screw Hole

HOLE8 *O-PS1A-1
Thermal piple
EC-20100208A-1
EC-20100412B-1
EC-20100603C-1

PROJECT :PS2
Quanta Computer Inc.

Size	Document Number	Rev
B	<Doc> HOLES, PAD, NUT	1A
Date: Thursday, June 03, 2010	Sheet 38 of 44	

Revision History

Revision	Date	Phase	Change List	Release Schematic Date	Release Gerber File Date
1A		DV	Initial release		

Schematic Value Explanation Description :

RESISTOR

Value	F	4	6	8	12	1210	*	Description
*1K/F_4	1%	0402 (1005)					DE POP	1K ohm 1% SMD 0402 package and DE POP
1K/J_6	5%		0603 (1608)				POP	1K ohm 5% SMD 0603 package and POP
1K/J_8	5%			0805 (2125)			POP	1K ohm 5% SMD 0805 package and POP
1K/J_12	5%				1206 (3216)		POP	1K ohm 5% SMD 1206 package and POP
1K/J_1210	5%					1210 (3225)	POP	1K ohm 5% SMD 1210 package and POP

CAPACITOR

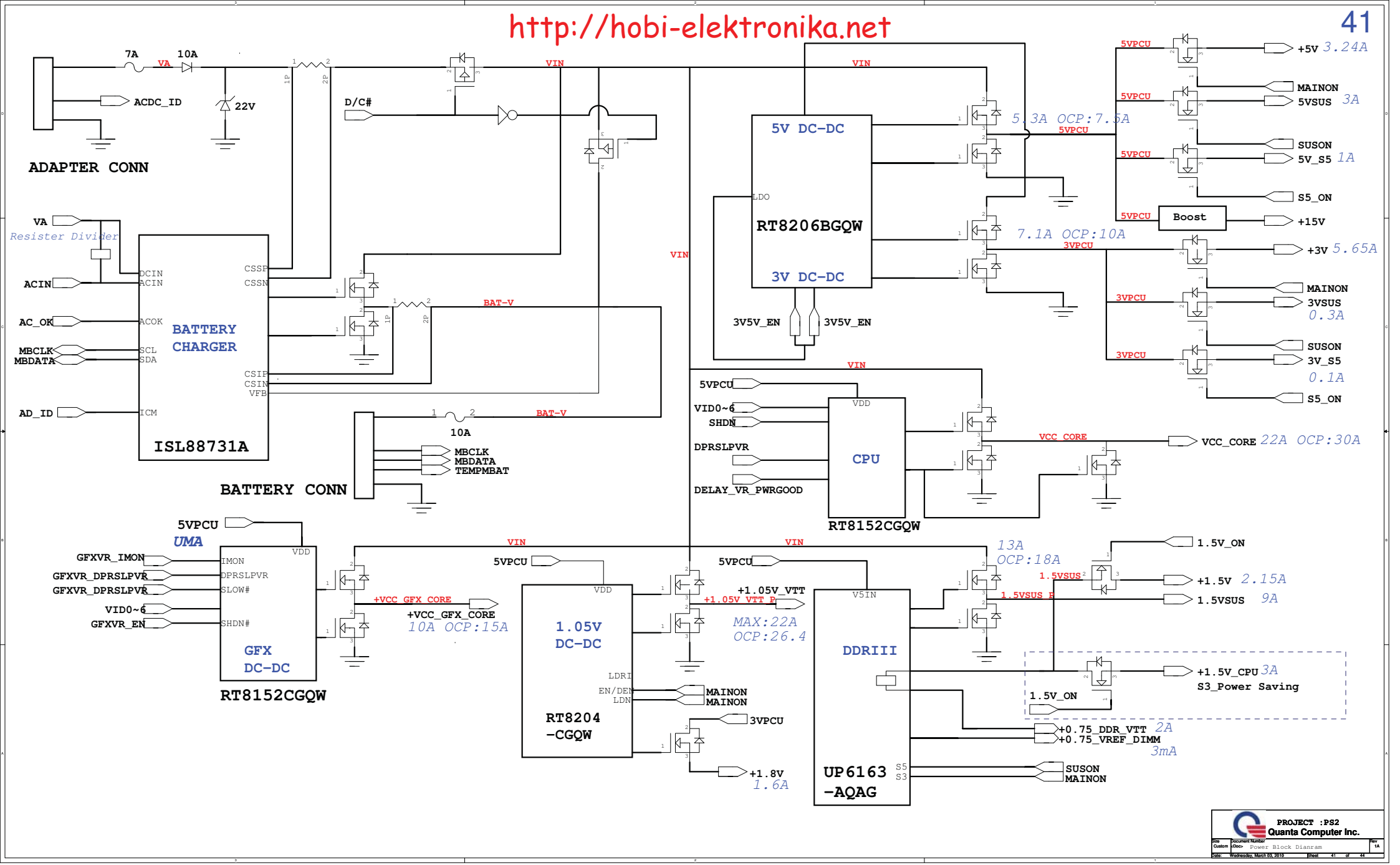
Value	Voltage	Material	6				*	Description
*.1U/10V/X5_4	10V	X5R	0402 (1005)				DE POP	0.1UF 10V X5R SMD 0402 package DE POP
1U/25V/X7_6	25V	X7R	0603 (1608)				POP	0.1UF 25V X7R SMD 0603 package POP

PROJECT : PS2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> Schematic Value Descript	1A
Date:	Wednesday, March 03, 2010	Sheet 39 of 44

Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	20,30,31,32,33,34,35,36	MAIN POWER		S0~S5
+3VRTC	+3.0V~+3.3V	11,14,28	RTC		S0~S5
3VPCU	+3.3V	11,19,20,24,27,28,30,31,34,35	ITE8502 POWER	3V5V_EN	S0~S5
5VPCU	+5V	11,30,31,32,33,34,35,36	DC/DC POWER IC SOURCE	3V5V_EN	S0~S5
+15V	+15V	20,31,33,35	LARGE POWER	3V5V_EN	S0~S5
LANVCC	+3.3V	19,35	LAN POWER	LAN_ON	
5V_S5	+5V	14,23,35	PCH SUS POWER	S5_ON	S0~S3
3V_S5	+3.3V	03,10,11,12,13,14,23,33,35	Sys Management,PCH Resume Well, Intel HD Audio,USB,WLAN,WiMAX POWER	S5_ON	S0~S3
5VSUS	+5V	20,27,35	SLP_S4# CTRLD POWER	SUSON	S0~S3
3VSUS	+3.3V	26,27,28,33,35	SLP_S4# CTRLD POWER	SUSON	S0~S3
1.5VSUS	+1.5V	3,6,16,17,33,35	DDR3 SODIMM POWER	SUSON	S0~S3
+DDR_VREF_DIMM	+0.75V	17,33	DDR3 SODIMM REFERENCE POWER	MAINON	S0
+5V	+5V	10,14,18,20,21,22,23,24,25,28,35	SLP_S3# CTRLD POWER	MAINON	S0
+3V	+3.3V	2,3,10,11,12,13,14,16,17,18,19,20,21,22,23 25,26,27,28,29,31,32,34,35,37	SLP_S3# CTRLD POWER	MAINON	S0
+1.8V	+1.8V	5,12,14,34,35	LVDS,NVM POWER	MAINON	S0
+1.5V	+1.5V	18,26,33	Mini PCIe,Express Card POWER	MAINON	S0
+1.05V_VTT	+1.05V	2,3,5,6,10,11,12,13,14,34,35,36,38	AuBurndale VTT POWER/PCH CORE POWER	MAINON	S0
GFX_CORE		6,36	VGA CORE POWER	GFXVR_EN	S0
VCC_CORE		5,32	CPU CORE POWER	VRON	S0
+3VLCD_CON	+3.3V	20	LCD Power	INT_DISP_ON	S0
+5V_HDD	+5V	25	HDD Power	MAINON	S0
+3V_HDD	+3V	25	HDD Power	MAINON	S0
BAT-V	+10V~+17V	30	MAIN BATTERY		S0~S5



PROJECT :PS2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc> Power Block Dianram	1A
Date: Wednesday, March 03, 2010	Sheet 41 of 44	

EC-20100125A-1	P37	GMT FAE Suggestion	Remodify thermal IC schematic:Q9005 Connection is pin 2 and pin 3 connecting to DXP, pin 1 connect to DXN , R9150 change from NC to 0 ohm
EC-20100127A-1	P18	Conexant FAE Suggestion	Modify Digital MIC schematic:Del component :R24,R23,C61,CN3,R132,C239,C240 Add component :R9151,CN23,R8380
EC-20100128A-1	P38		Update CPU NUT footprint and value from "h-c146d146n" to "h-c142d142n "
EC-20100128A-2	P30	Power RECOMMAND	Del PJP1 and Add PL1015 on PJP1 original location
	P31		Del PJP9 and Add PL1016 on PJP9 original location
			Del PJP8 and Add PL1017 on PJP8 original location
EC-20100129A-1	P5		Reduce Power ripple:Add C8355 and C8354
EC-20100201A-1	P36	Power RECOMMAND	For layout routing:change Net for "8152GND" to "8152GFX_GND"
EC-20100201A-2	P38	EMI RECOMMAND	EMI reserved:add C226,C230,C231,C239,C240,C242,C245,C248
EC-20100201A-3	P27		Del the unused net "+3V" of CN14
EC-20100202A-1	P24		Del the unused 13 pin tp connect "CN2"
EC-20100203A-1	P29	Customer RECOMMAND	R28 and R29 un-mount
EC-20100204A-1	P8	Customer RECOMMAND	Remove CFG7:Del R8339 and del the net of CFG7
EC-20100204A-2	P26		0 ohm resisters for LPC signal:add R15,R19,R23,R24,R31
	P28		0 ohm resisters for LPC signal:add R33,R34,R36,R37,R38
EC-20100204A-3	P11		Remove pull high schematic to GPIO33 of IBEX and del R9014
EC-20100205A-1	P33	Customer RECOMMAND	Change PR366 Vaule and PN form 22 ohm to 220 ohm
EC-20100206A-1	P3	Customer RECOMMAND	Reserve 0 ohm 0402 "R8381" for S3 leakage issue schematic
EC-20100208A-1	P38		Add a pdh screw hole--hole24
EC-20100210A-1	P10		Design guide check:DDPB_AUXP and DDPB_AUXN is not used by HDMI function.R9083 and R9084 un-mount
EC-20100212A-1	P13		Design guide check:GPIO16 and GPIO17 of PCH must be pull high when then function not be used.Add R9068,R9069 and pull high to +3V
EC-20100222A-1	P11	Customer RECOMMAND	Modify E-SATA schematic and connect to SATA port4 of PCH:add C9092 and C9093
	P23		Remove USB S5 Charger schematic and change right side connect from USB to E-Sata combo Del:CN8,R409,R410,U28,C332,R417,R384,R385,R418,R383,R386,R428,R429,R409,R411.Add U9006,U9007,CN24
EC-20100223A-1	P18	Customer RECOMMAND	Remodify Analog MIC schematic:Del R9151,CN23,R8380. Add CN25,R9153,C9098,R9152,R9151 C9096,C9097
EC-20100224A-1	P37	Thermal RECOMMAND	Change temperature protection degree:change R8514 value form 8.2k to 1.74k
EC-20100224A-2	P12		del unused net USB_OC#2
EC-20100224A-3	P28		Change the net from "USB_ON#" to "USB_CHR_ON#"
EC-20100224A-4	P28		Add the net "USB_ON#" to control USB power switch enable and connect to Pin 97 of EC
EC-20100224A-5	P27		To match the signals of function board 40 pin connect: Remodify pin define of CN14 add C9094 and C9095 for EMI
EC-20100225A-1	P18	ESD RECOMMAND	add C9099 for ESD reserved
EC-20100225A-2	P27		Del unused net +3V and C13
EC-20100225A-3	P28	Customer RECOMMAND	Add USB S5 charger select schematic:Add R9154,R9155,R9156,R9157,R9158,R9159
	P27		Add USB S5 charger select schematic:Remodify CN14 pin define.1.change netlsit from "USB_AO_SEL0" to "USB_AO_SEL0_CB0".2.change net from "USB_AO_SEL1" to "USB_AO_SEL1_CB1"3.del the net "3V_S5" of CN13
EC-20100225A-4	P27		Del USB IO EMI reserved schematic:del R256,R255,R250,R249,R236,R235,L47,L46,L45
EC-20100225A-5	P30	Power RECOMMAND	update PQ48 footprint and value
EC-20100225A-6	P3		Add net PCH_GPIO8 to reserve For Processor Hot Control schematic and conect to GPIO8 of PCH
	P13		
EC-20100226A-1	P23	Customer RECOMMAND	Add 0.01uF cap," C9100" ,"C9101" and connect SATA4 RX pair signal
EC-20100226A-2	P3		Remove the net PCH_GPIO8 and disconnect to PCH
	P13		
EC-20100226A-3	P36	Power RECOMMAND	update PL1012 footprint
EC-20100226A-4	P18	Conexant RECOMMAND	1.add Res 0603 0 ohm "R9160" 2.change C500 value from 1uf to 10uf. 3.change R419 value from 100 to 1k
EC-20100226A-5	P27	Customer RECOMMAND	Del C9095
EC-20100304A-1	P38		Add PCB SPAD for ESD
EC-20100305A-1	P33	Power RECOMMAND	Reduce noise:Add PC274
EC-20100305A-2			update footprint:CN22,PU2,PQ1,PQ30,PQ31,PQ36,PQ37,PQ39,PQ4,PQ40,PQ54,PQ55,PQ56,PQ57 ,PQ58,PQ59,PQ60,PQ61,PQ63,PQ69,PQ74,PQ75,PQ86,PQ94,PQ95,PQ97,HOLE15,HOLE16,HOLE17 HOLE18
EC-20100305A-3	P21		Add PS8101 thermal pad
EC-20100309A-1	P31	Power RECOMMAND	update value and part number:PL8 , PL13 CHANGE TO DC-2280M004 CHOKE SMD 2.2UH+-20%8A (PCMC063T-2R2MN)EP
EC-20100309A-2	P32	Power RECOMMAND	update value and part number:PU2, PU5 CHANGE TO AL008152006 IC CTRL (32P) RT8152EGQW (WQFN-32L 5X5)
EC-20100309A-3	P34		update value and part number: PL11 CHANGE TO DC+36T0M000 CHOKE 0.36U +-20%,28A (ETQP4LR36AFC)
EC-20100309A-4	P34		update value and part number:PQ46 CHANGE TO BAM14480000 TRANS MOSFET AOL1448 (30V,36A,30W)
EC-20100309A-5	P30		update value and part number:PQ49 CHANGE TO BAM04250000
EC-20100309A-6	P33		update value and part number:PQ23 CHANGE TO BAM72020000,PR214 CHANGE TO CS31072FB10
EC-20100310A-1		Power RECOMMAND	Power upate BOM:PQ16,PQ19,PQ52,PQ55,PQ58,PQ59,PQ60,PQ61 change from "BAM800030001" to "BAM74060000" and update value

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EC-20100319B-1	P30	Power RECOMMAND	Reduce Vin power lose Del PD17 and add PQ67,PQ68,PR220,PR221,PR222, PR223,PR224
EC-20100319B-2	P32 P36		Add power derating:change PC123,PC18,PC44,PC45 PN to CH5102K9B06
EC-20100319B-3	P12		Bios strap error:R134,R135 un-mount
EC-20100330B-1	P34	Power RECOMMAND	Reduce power ripple:mout Cap 330uF 3528 on PC90
EC-20100330B-2	P11		Reduce S3 leakage :R306,R307,R308,R309,R323,R324,R325,R326 un-mount
EC-20100409B-1	P37		Remove thermal ic U9
EC-20100409B-2	P34	Power RECOMMAND	update power thermal derating from 85 degree to 105 degree :change PC136,PC137 footprint and value, remove PC140
EC-20100409B-3	P34		Reduce Power nois at 1.05_VTT,1.5VSUS:Add PC179 and PC178,PC114 mount
EC-20100409B-4	P33 P34		Power update shcematic:remove power PJP1,PJP2,PJP3,PJP4. Power update schematic (only for debug in A-stage)
EC-20100409B-5	P31		fine tune OCP value:update PR87 value
EC-20100409B-6	P35		Add 3v_S5 discharge path:PQ40 mount and update value
EC-20100409B-7	P32		update correct CPU_CORE frequency:chang PR165 value
EC-20100409B-8	P20		LG panel flick : C3 un-mount
EC-20100409B-9	P12		no layout space, so remove tp of unuse-pin of PCH
EC-20100409B-10	P30		Power update charger schematic
EC-20100412B-1	P38		Hole12 update PCB location and the nut footprint:update Hole 12 footprint from H-BC177D59PB to H-TC166BC276D122P2
EC-20100413B-1	P18		HDA reference voltage error:change from +1.5V to 3V_DVDD
EC-20100413B-2	P38		update ESD SPAD form:Add SPAD15,SPAD16,del SPAD6,update SPAD5,SPAD7,SPAD9,SPAD11, SPAD12,SPAD13,SPAD14 footprint.
EC-20100413B-3	P10 P11 P12 P13 P14 P15	Customer RECOMMAND	It is according to Lenovo request to enhance BGA rework performance, lower the F/R of solder mask or pad peel off from the reworking update IBEX footprint to bga1071-intel-ibexpeak-li
EC-20100413B-4	P23		Esata connect error:remodify USB/ESATA connect schematic and update CN8 footprint
EC-20100413B-5	P24		To correct Vih level for trackpoint and touch pad ,add Track Point/Touch Pad reset level schematic:add Q33,Q34,Q35,Q36,R442,R443,R444,R445,R446,R447
EC-20100413B-6	P37	Thermal RECOMMAND	Update G708 OTP from 120 deegree to 110 degree:changre R42 value from 1.74K to 8.2k
EC-20100413B-7	P13 P23		To fit actual function:change "BT_ON# "to "BT_ON"
EC-20100413B-8	P24 P28		To fit actual function:change "TRACK_POINT_RESET" to "TRACK_POINT_RESET#"
EC-20100415B-1	P26	Customer RECOMMAND	Add debug card/BT_ON select schematic:reserve R448,U33.R449,R450 mount
EC-20100416B-1	P37		Remove G780 function:Q16,Q15,Q6,Q8,R78,R92,R100,R79,R77,R104,C192,C197 un-mount
EC-20100416B-2	P2		Fine tune crysatl frequency:update Y2 Colad value from 30Pf to 22Pf
EC-20100416B-3	P12		Fine tune crysatl frequency:update Y5 Colad value from 18Pf to 27Pf

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EC-20100421B-1	P21		Add U27 idle mode schematic,when hdmi plug in,idle mode will be closed:add Q37 and R451
EC-20100421B-2	P19		Fine tune RJ45 connect LED brightness: change value from 310 ohm to 510 ohm
EC-20100526C-1	P2 P6 P8 P10 P11 P12 P12 P13 P14 P18 P19 P20 P23 P24 P25 P26 P28 P31 P32 P33 P34 P36		Del 0402 0ohm and update footprint from RC0402 to SHORT0402:PR8,PR50,PR51,PR53,PR137,PR141,PR143 PR145,PR147,PR149,PR151,PR155,PR158,PR176,PR177,PR180,PR182,PR202,PR29,PR84,PR85,PR88,PR93 PR145,PR147,PR149,PR151,PR155,PR158,PR176,PR177,PR180,PR182,PR202,PR29,PR84,PR85,PR88,PR93 PR96,PR107,PR112,PR209,PR61,PR64,PR69,PR71,PR72,PR74,PR75,PR208,R6,R7,R217,R218,R219,R220,R221 R427,R428,R429,R430,R431,R17,R18,R140,R156,R178,R183,R186,R193,R194,R201,R409,R413,R38,R69,R76, R88,R114,R115,R151,R252,R255,R269,R271,R276,R279,R280,R281,R313,R315,R316,R329,R350,R353,R370 R80,R84,R85,R87,,R89,R122,R344,R272,R422,R439
EC-20100526C-2	P14 P18 P25 P20 P21 P22 P26 P31 P33 P34 P36		Del 0603 0ohm and update footprint from RC0603 to SHORT0603:R16,L19,L20,L21,R32,R47,PR81,PR175,PR194 ,R211,R215,R265,R283,L35,PR49,PR105,R106,PR167,PR191,R119
EC-20100526C-3	P25 P19		Del 0805 0ohm and update footprint from RC0805 to SHORT0805:R126,R139,R192,R407,
EC-20100526C-4	P26		For new BT/WLAN combo card:Remove R449,R448,R450,U33,R5 and change the netlist BT_ON to Pin 51 of CN12
EC-20100526C-5	P38		update ESD SPAD form:update SPAD5,SPAD12,SPAD13 footprint
EC-20100603C-1		Thermal RECOMMAND	Thermal cancel spring arm:Remove Hole12
EC-20100604C-1	P20	RF RECOMMAND	Add Cap C523,C524 for RF reserve
EC-20100604C-2	P21	EMI RECOMMAND	Remoce EMI reserve and updare 0 ohm footprint:del RP8,RP7,RP6 and update footprint R358,R346,R342,R328,R322 ,R318 from RC0402 to SHORT0402

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