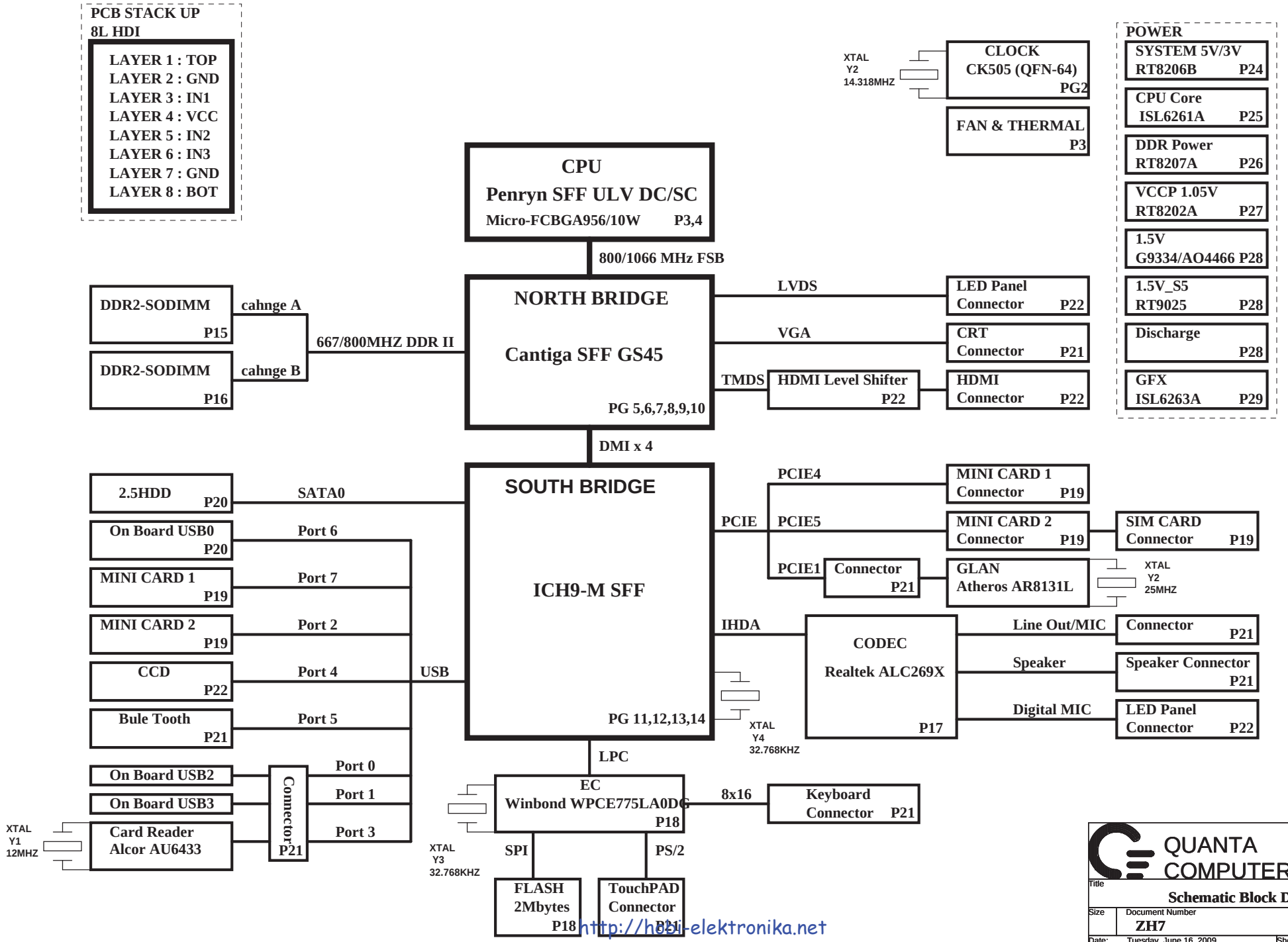
(S)JM11_MS (ZH7) BLOCK DIAGRAM



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QUANTA COMPUTER

Title	Schematic Block Diagram	
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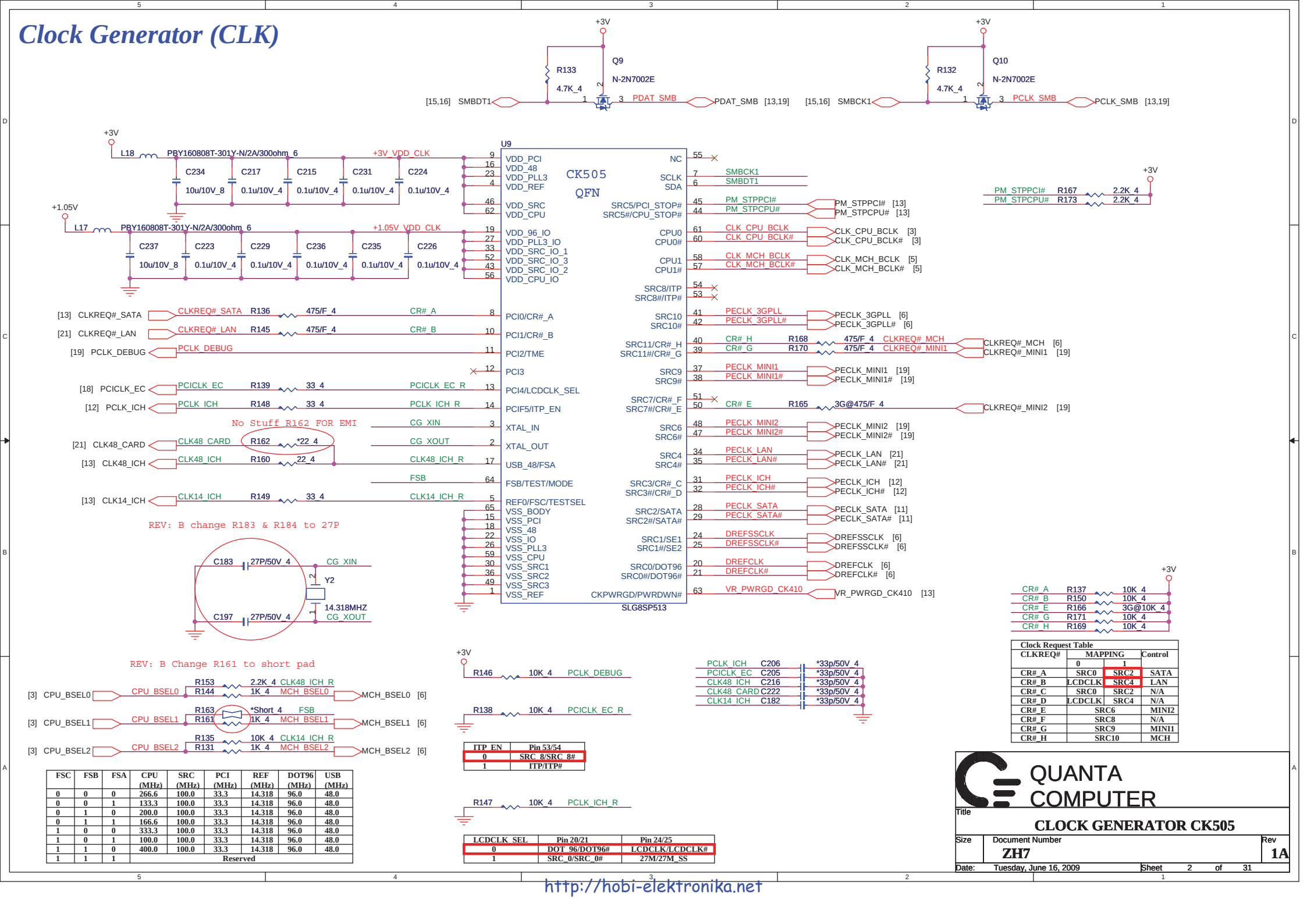
Clock Generator (CLK)



FSC	FSB	FSA	CPU (MHz)	SRC (MHz)	PCI (MHz)	REF (MHz)	DOT96 (MHz)	USB (MHz)
0	0	0	266.6	100.0	33.3	14.318	96.0	48.0
0	0	1	133.3	100.0	33.3	14.318	96.0	48.0
0	1	0	200.0	100.0	33.3	14.318	96.0	48.0
0	1	1	166.6	100.0	33.3	14.318	96.0	48.0
1	0	0	333.3	100.0	33.3	14.318	96.0	48.0
1	0	1	100.0	100.0	33.3	14.318	96.0	48.0
1	1	0	400.0	100.0	33.3	14.318	96.0	48.0
1	1	1	Reserved					

ITP_EN	Pin 53/54
0	SRC_8/SRC_8#
1	ITP/ITP#

LCDCLK_SEL	Pin 20/21	Pin 24/25
0	DOT_96/DOT96#	LCDCLK/LCDCLK#
1	SRC_0/SRC_0#	27M/27M_SS

Clock Request Table			
CLKREQ#	MAPPING		Control
	0	1	
CR#_A	SRC0	SRC2	SATA
CR#_B	LCDCLK	SRC4	LAN
CR#_C	SRC0	SRC2	N/A
CR#_D	LCDCLK	SRC4	N/A
CR#_E	SRC6		MINI2
CR#_F	SRC8		N/A
CR#_G	SRC9		MINI1
CR#_H	SRC10		MCH

QUANTA COMPUTER

Title: CLOCK GENERATOR CK505

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	ZH7	1A

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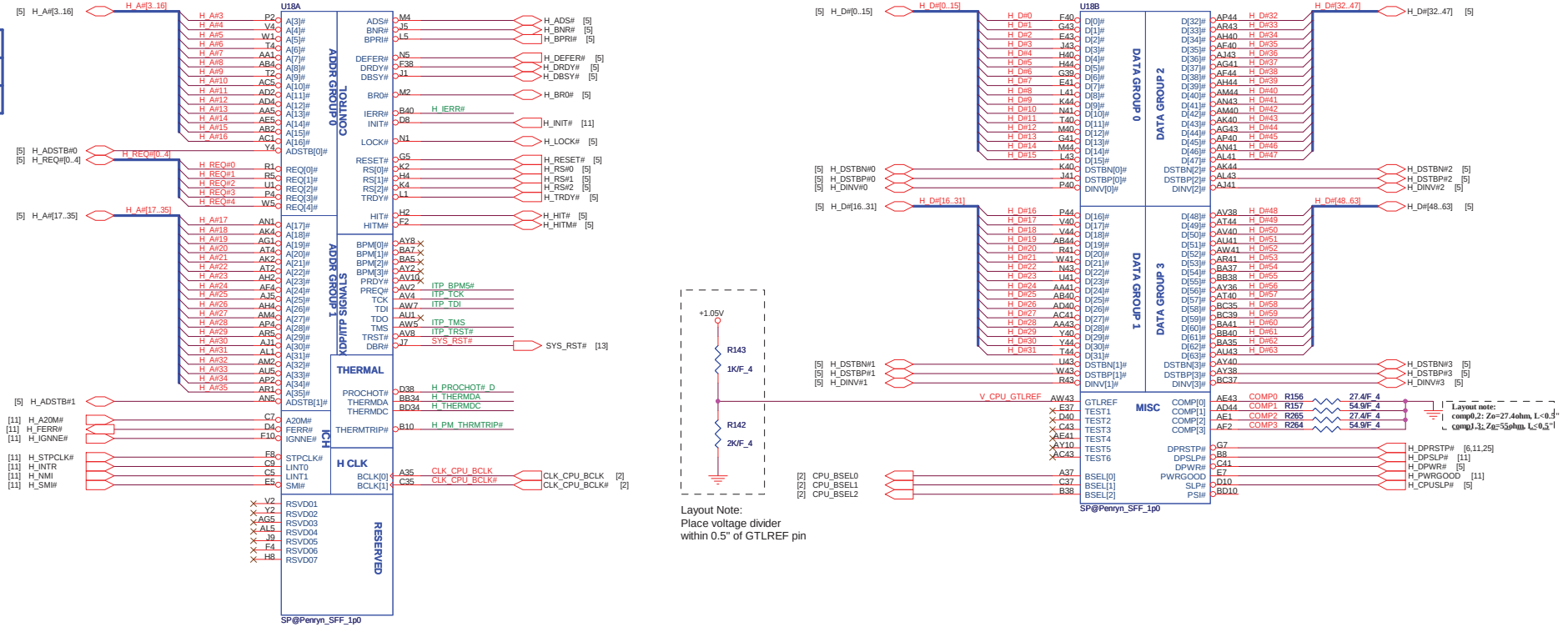
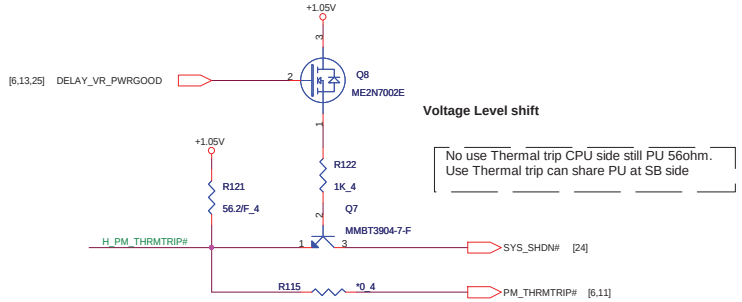
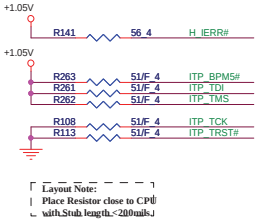
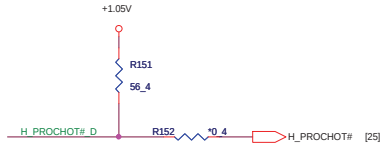
Penryn SFF - Host Bus (CPU)

1.2G	AJSLGAMVT02
1.4G	AJSLGFMTT00

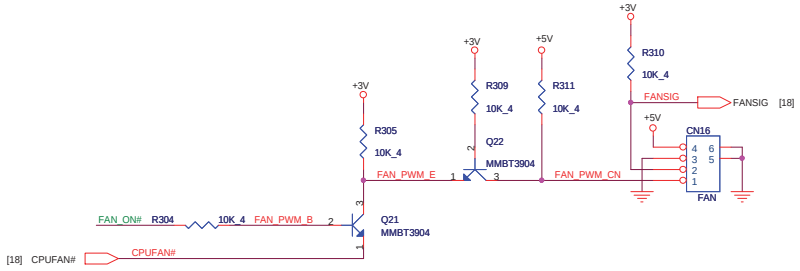




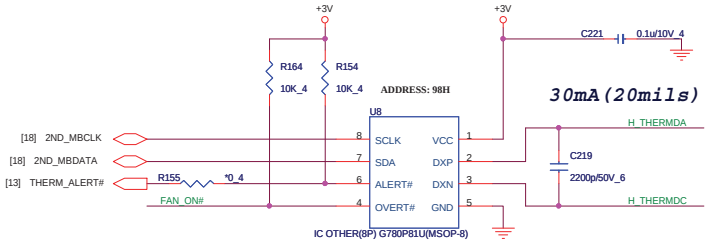




CPU FAN CTRL(THM)



CPU Thermal Monitor(THM)



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QUANTA COMPUTER

Title	Penryn SFF (Host Bus)/FAN/Thermal	
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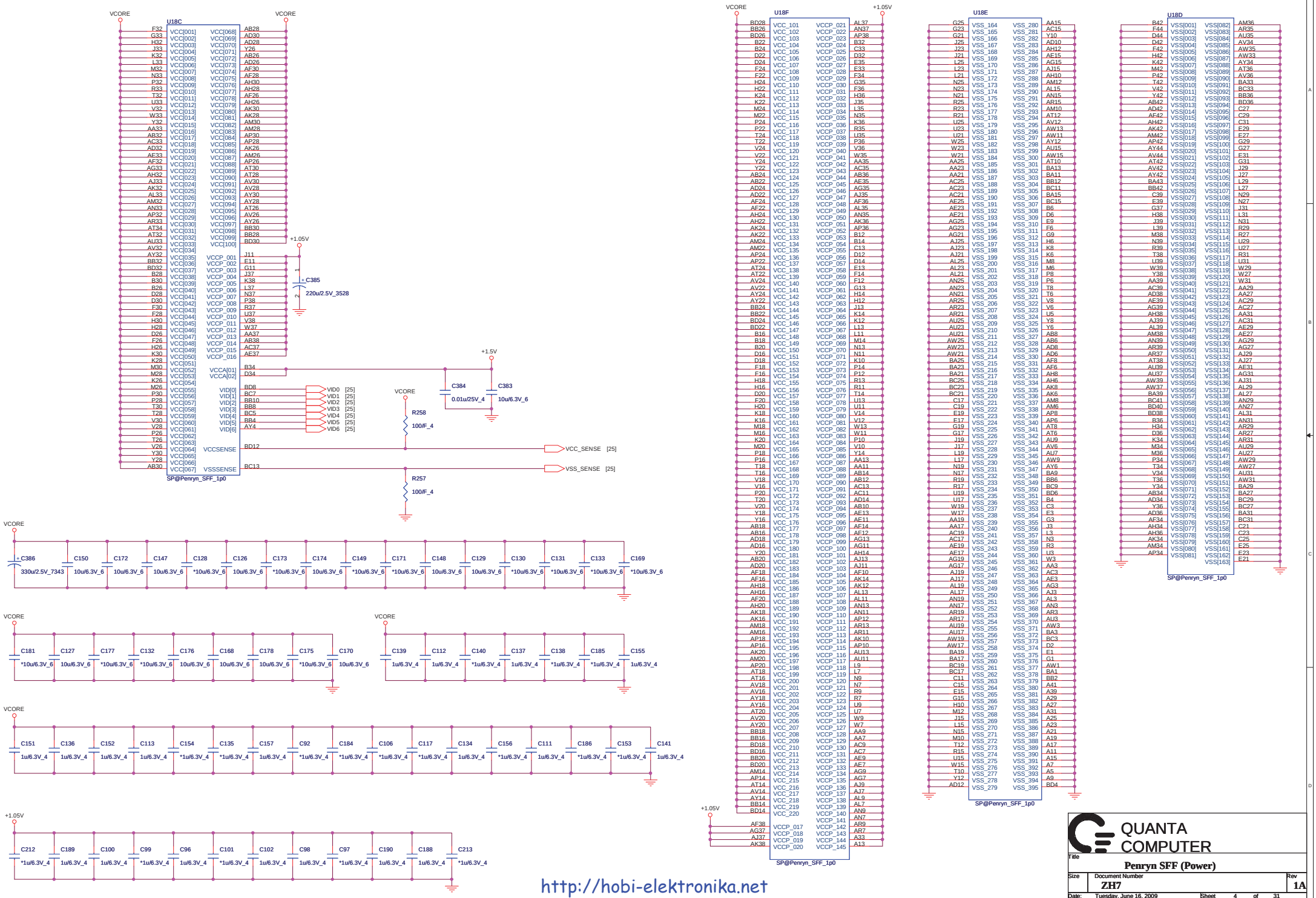
Penryn SFF - Power (CPU)



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QUANTA COMPUTER

Title	Penryn SFF (Power)	
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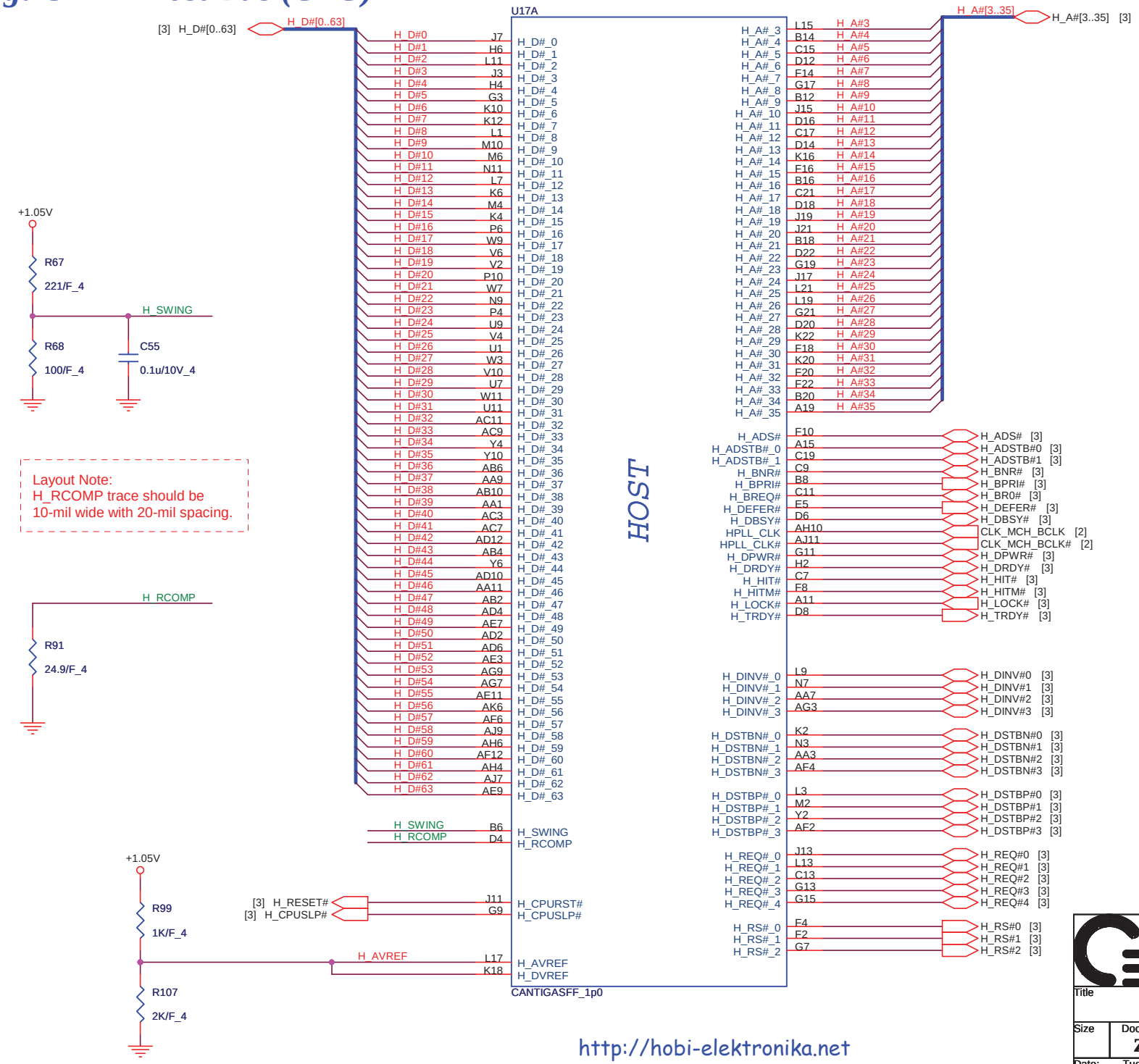
Cantiga SFF - Host Bus (CLG)



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QUANTA COMPUTER

Title	Cantiga SFF (Host Bus)	
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Cantiga SFF - DMI/VGA (CLG)

Intel GS40/GS45 Strapping Signals and Configuration		
Pin Name	**Strap Description**	**Configuration**
CFG2:0	FSB Frequency	000 = FSB1066 010 = FSB800 011 = FSB667 Other = Reserved
CFG4:3	Reserved	
CFG5	DMI x2 Select	1 = DMI x 4 0 = DMI x2
CFG6	ITPM Host Interface	1 = ITPM disabled 0 = ITPM enabled
CFG7	Intel Management Engine Crypto Strap	1 = Intel Management Engine Crypto TLS cipher suite with confidentiality 0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
CFG8	Reserved	
CFG9	PCIE Graphics Lane	1 = Normal operation : Lane Numbered in Order 0 = Reverse Lanes
CFG10	PCIE Loopback enable	1 = Disabled 0 = Enabled
CFG11	Reserved	
CFG12	ALLZ	1 = Disabled 0 = ALLZ mode enabled
CFG13	XOR	1 = Disabled 0 = XOR mode enabled
CFG14	Reserved	
CFG15	Reserved	
CFG16	FSB Dynamic ODT	1 = Dynamic ODT enabled 0 = Dynamic ODT disabled
CFG17	Reserved	
CFG18	Reserved	
CFG19	DMI Lane Reversal	1 = Reverse Lanes 0 = Normal operation : Lane Numbered in Order
CFG20	Digital DisplayPort (SDVO/DP/iHDMI) Concurrent with PCIE	1 = Digital DisplayPort (SDVO/DP/iHDMI) and PCIE are operating simultaneously via the PEG port 0 = Digital DisplayPort (SDVO/DP/iHDMI) or PCIE are operational
SDVO_CTRLDATA	SDVO Present	1 = SDVO/HDMI/DP interface enabled 0 = No SDVO/HDMI/DP interface disabled
L_DDC_DATA	Local Flat Panel (LFP) Present	1 = LFP Card Present; PCIE disabled 0 = LFP Disable
DDPC_CTRLDATA	Digital Display Present	1 = Digital display (iHDMI/DP) devide present 0 = Digital display (iHDMI/DP) interface absent

- The recommended pull-up resistor value is 4.02 kΩ ±1%
- The recommended pull-down resistor value is 2.21 kΩ ±1%.

U17B

RSVD1 RSVD2 RSVD3 RSVD4 RSVD5 RSVD6 RSVD7 RSVD8 RSVD9
RSVD14 RSVD15
RSVD17
RSVD20
RSVD22 RSVD23 RSVD24 RSVD25
ME_JTAG_TCK ME_JTAG_TDI ME_JTAG_TDO ME_JTAG_TMS

HSIO

SA_CK_0 SA_CK_1 SB_CK_0 SB_CK_1 → M_CLK_DDR0 M_CLK_DDR1 M_CLK_DDR2 M_CLK_DDR3 [15][16]
SA_CK#_0 SA_CK#_1 SB_CK#_0 SB_CK#_1 → M_CLK_DDR#0 M_CLK_DDR#1 M_CLK_DDR#2 M_CLK_DDR#3 [15][16]
SA_CKE_0 SA_CKE_1 SB_CKE_0 SB_CKE_1 → M_CKE0 M_CKE1 M_CKE2 M_CKE3 [15][16]
SA_CS#_0 SA_CS#_1 SB_CS#_0 SB_CS#_1 → M_CS#0 M_CS#1 M_CS#2 M_CS#3 [15][16]
SA_ODT_0 SA_ODT_1 SB_ODT_0 SB_ODT_1 → M_ODT0 M_ODT1 M_ODT2 M_ODT3 [15][16]
SM_RCOMP SM_RCOMP# → SMRCOMPP SMRCOMPN
SM_RCOMP_VOH SM_RCOMP_VOL → SM_RCOMP_VOH SM_RCOMP_VOL
SM_VREF SM_PWROK SM_REXT SM_DRAMRST# → +SMDDR_VREF_NB SM_PWROK SM_REXT

DDR CLK/ CONTROL/COMPENSATION

DPLL_REF_CLK DPLL_REF_CLK# DPLL_REF_SSCLK DPLL_REF_SSCLK# → DREFCLK DREFCLK# DREFSSCLK DREFSSCLK# [2]
PEG_CLK PEG_CLK# → PECLK_3GPLL PECLK_3GPLL# [2]

CLK

DMI_RXN_0 DMI_RXN_1 DMI_RXN_2 DMI_RXN_3 → DMI_MRX_ITX_N0 DMI_MRX_ITX_N1 DMI_MRX_ITX_N2 DMI_MRX_ITX_N3 [12]
DMI_RXP_0 DMI_RXP_1 DMI_RXP_2 DMI_RXP_3 → DMI_MRX_ITX_P0 DMI_MRX_ITX_P1 DMI_MRX_ITX_P2 DMI_MRX_ITX_P3 [12]
DMI_TXN_0 DMI_TXN_1 DMI_TXN_2 DMI_TXN_3 → DMI_MTX_IRX_N0 DMI_MTX_IRX_N1 DMI_MTX_IRX_N2 DMI_MTX_IRX_N3 [12]
DMI_TXP_0 DMI_TXP_1 DMI_TXP_2 DMI_TXP_3 → DMI_MTX_IRX_P0 DMI_MTX_IRX_P1 DMI_MTX_IRX_P2 DMI_MTX_IRX_P3 [12]

DMI

[2] MCH_BSEL0 [2] MCH_BSEL1 [2] MCH_BSEL2
T13 MCH_CFG5
T18 MCH_CFG7
T20 MCH_CFG12
T21 MCH_CFG13
T19 MCH_CFG16
T14 MCH_CFG19
T15 MCH_CFG20
CFG_0 CFG_1 CFG_2 CFG_3 CFG_4 CFG_5 CFG_6 CFG_7 CFG_8 CFG_9 CFG_10 CFG_11 CFG_12 CFG_13 CFG_14 CFG_15 CFG_16 CFG_17 CFG_18 CFG_19 CFG_20

CFG

GFX_VID_0 GFX_VID_1 GFX_VID_2 GFX_VID_3 GFX_VID_4 → GPU_VID0 GPU_VID1 GPU_VID2 GPU_VID3 GPU_VID4 [29]
GFX_VR_EN → GFX_VR_EN [29]

GFX VID

[13] PM_SYNC# [3,11,25] H_DPRSTP# [15] PM_EXTTS#0 [16] PM_EXTTS#1 [3,13,25] DELAY_VR_PWRGOOD [12,18,19,21] PLTRST# [3,11] PM_THRMTRIP# [13,25] DPRSLPVR
R134 100_4 RSTIN#_MCH
R267 *0_4
PM_EXTTS#0 PM_EXTTS#1
PM_SYNC# PM_DPRSTP# PM_EXT_TS#_0 PM_EXT_TS#_1 PWROK RSTIN# THERMTRIP# DPRSLPVR

GMCH GRAPHICS VID

CL_CLK CL_DATA CL_PWROK CL_RST# CL_VREF → CL_CLK0 [13] CL_DATA0 [13] MPWROK [13,18] ICH_CL_RST0# [13] MCH_CLVREF

ME

NC_1 NC_2 NC_3 NC_4 NC_5 NC_6 NC_7 NC_8 NC_9 NC_10 NC_11 NC_12 NC_13 NC_14 NC_15 NC_16 NC_17 NC_18 NC_19 NC_20 NC_21 NC_22

NC

DDPC_CTRLCLK DDPC_CTRLDATA SDVO_CTRLCLK SDVO_CTRLDATA CLKREQ# ICH_SYNC# → SDVO_CTRLCLK [22] SDVO_CTRLDATA [22] CLKREQ#_MCH [2] MCH_ICH_SYNC# [13]
TSATN# → TSATN#

MISC

HDA_BCLK HDA_RST# HDA_SDI HDA_SDO HDA_SYNC → HDA_BIT_CLK_HDMI [11] HDA_RST#_HDMI [11] HDA_SDIN_HDMI [11] HDA_SDOUT_HDMI [11] HDA_SYNC_HDMI [11]

HDA

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U17C

[22] INT_LVDS_PWM [22] INT_LVDS_BLON → L_BKLT_CTRL L_BKLT_EN L_CTRL_CLK
L_CTRL_CLK → L_CTRL_CLK
[22] PHL_CLK [22] PHL_DATA → L_CTRL_DATA L_DDC_CLK L_DDC_DATA
PHL_CLK PHL_DATA
[22] INT_LVDS_DIGON → L_VDD_EN
LVDS_IBG → LVDS_IBG LVDS_VBG LVDS_VREFH LVDS_VREFL
[22] TXLCLKOUT- [22] TXLCLKOUT+ → LVDSA_CLK# LVDSA_CLK LVDSB_CLK# LVDSB_CLK
[22] TXLOUT0- [22] TXLOUT1- [22] TXLOUT2- → LVDSA_DATA#_0 LVDSA_DATA#_1 LVDSA_DATA#_2 LVDSA_DATA#_3
[22] TXLOUT0+ [22] TXLOUT1+ [22] TXLOUT2+ → LVDSA_DATA_0 LVDSA_DATA_1 LVDSA_DATA_2 LVDSA_DATA_3
LVDSB_DATA#_0 LVDSB_DATA#_1 LVDSB_DATA#_2 LVDSB_DATA#_3
LVDSB_DATA_0 LVDSB_DATA_1 LVDSB_DATA_2 LVDSB_DATA_3

LVDS

INT_TV_COMP INT_TV_Y/G INT_TV_C/R → TVA_DAC TVB_DAC TVC_DAC
TVA_RTN
TV_DCONSEL_0 TV_DCONSEL_1

SDVO

[21] CRT_B [21] CRT_G [21] CRT_R → CRT_BLUE CRT_GREEN CRT_RED CRT_IRTN
[21] DDCCLK [21] DDCDATA [21] VGAHSYNC [21] VGAVSYNC → CRT_DDC_CLK CRT_DDC_DATA CRT_HSYNC CRT_TVO_IREF CRT_VSYNC
R54 30.1/F_4 HSYNC
R53 30.1/F_4 VSYNC
CRT_IREF

CRT

PEG_COMPI PEG_COMPO → PEG_COMP R114 49.9/F_4 +1.05V
PEG_RX#_0 PEG_RX#_1 PEG_RX#_2 PEG_RX#_3 PEG_RX#_4 PEG_RX#_5 PEG_RX#_6 PEG_RX#_7 PEG_RX#_8 PEG_RX#_9 PEG_RX#_10 PEG_RX#_11 PEG_RX#_12 PEG_RX#_13 PEG_RX#_14 PEG_RX#_15
PEG_RX_0 PEG_RX_1 PEG_RX_2 PEG_RX_3 PEG_RX_4 PEG_RX_5 PEG_RX_6 PEG_RX_7 PEG_RX_8 PEG_RX_9 PEG_RX_10 PEG_RX_11 PEG_RX_12 PEG_RX_13 PEG_RX_14 PEG_RX_15
HDMI_HP_IV# [22]
HDMI Port B
PEG_TX#_0 PEG_TX#_1 PEG_TX#_2 PEG_TX#_3 PEG_TX#_4 PEG_TX#_5 PEG_TX#_6 PEG_TX#_7 PEG_TX#_8 PEG_TX#_9 PEG_TX#_10 PEG_TX#_11 PEG_TX#_12 PEG_TX#_13 PEG_TX#_14 PEG_TX#_15
PEG_TXN0 C71 PEG_TXN1 C65 PEG_TXN2 C73 PEG_TXN3 C57 HD@0.1u/10V_4
HDMITX2N [22] HDMITX1N [22] HDMITX0N [22] HDMICLKN [22]
PEG_TX_0 PEG_TX_1 PEG_TX_2 PEG_TX_3 PEG_TX_4 PEG_TX_5 PEG_TX_6 PEG_TX_7 PEG_TX_8 PEG_TX_9 PEG_TX_10 PEG_TX_11 PEG_TX_12 PEG_TX_13 PEG_TX_14 PEG_TX_15
PEG_TXP0 C69 PEG_TXP1 C68 PEG_TXP2 C86 PEG_TXP3 C62 HD@0.1u/10V_4
HDMITX2P [22] HDMITX1P [22] HDMITX0P [22] HDMICLKP [22]

PCI-EXPRESS GRAPHICS

PCI-E

CANTIGASFF_1p0

CRT setting

R84 1.02K/F CRT_IREF
R58 150/F_4 CRT_B
R59 150/F_4 CRT_G
R60 150/F_4 CRT_R
R56 75/F_4 INT_TV_COMP
R57 75/F_4 INT_TV_Y/G
R96 75/F_4 INT_TV_C/R

LVDS setting

+3V
R70 10K_4 L_CTRL_CLK
R71 10K_4 L_CTRL_DATA
R104 2.2K_4 PHL_DATA
R105 2.2K_4 PHL_CLK
R100 2.4K/F_4 LVDS_IBG

Check list note : CL_REF=0.35V

+1.05V
R126 1K/F_4
(15mils)
MCH_CLVREF
C167 0.1u/10V_4
R125 511/F_6

REV: B Change R254 to short pad

(20mils)
+SMDDR_VREF
+SMDDR_VREF_NB R254 *Short_6
SM_PWROK R129 10K/F_6

<Checklist ver0.8>
If TSATN# is not used, then it must be terminated with a 56-Ω pull-up resistor to VCCP.

TSATN# R80 56_4 +1.05V
PM_EXTTS#0 R86 10K_4
PM_EXTTS#1 R106 10K_4 +3V
SM_REXT R251 *49.9/F

+1.8VSUS
SMRCOMPP R255 80.6/F_4
SMRCOMPN R256 80.6/F_4

+1.8VSUS R250 1K/F_4
SM_RCOMP_VOH
R253 3.01K/F_4 C378 0.01u/25V_4 C228 2.2u/6.3V_6
SM_RCOMP_VOL
R249 1K/F_4 C377 0.01u/25V_4 C227 2.2u/6.3V_6

+3V
DDPC_CTRLCLK R272 2.2K_4
DDPC_CTRLDATA R278 2.2K_4
SDVO_CTRLCLK R77 4.7K_4
SDVO_CTRLDATA R83 4.7K_4

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QUANTA COMPUTER

Title	Cantiga SFF (DMI/VGA)	
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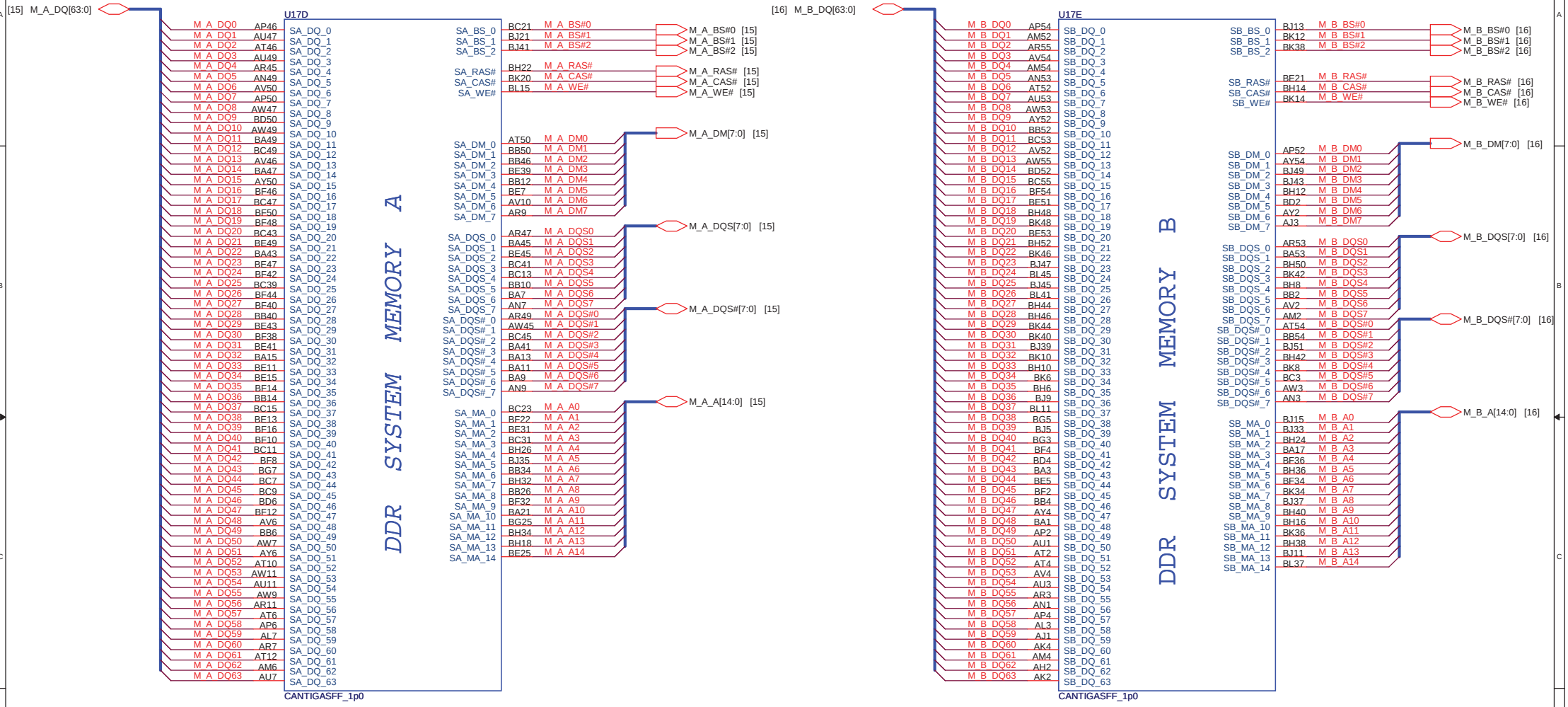
Cantiga SFF - DDRII (CLG)



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QUANTA COMPUTER

Title	Cantiga SFF (DDRII)	
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Cantiga SFF - VCC/NCTF (CLG)

Ivcc internal VGA 2.4A
(Shape or 140mils)

DDR2-667 2.6A
DDR2-800 3A
(Shape or 140mils)

UMA 9.6A(GM45)
(Plane or shape)

U17F

VCC 2200mA

+1.05V

VCC_1 VCC_2 VCC_3 VCC_4 VCC_5 VCC_6 VCC_7 VCC_8 VCC_9 VCC_10 VCC_11 VCC_12
VCC_13 VCC_14 VCC_15 VCC_16 VCC_17 VCC_18 VCC_19 VCC_20 VCC_21 VCC_22 VCC_23 VCC_24 VCC_25 VCC_26 VCC_27 VCC_28 VCC_29 VCC_30 VCC_31 VCC_32 VCC_33 VCC_34
VCC_35 VCC_36
VCC_37 VCC_38 VCC_39 VCC_40 VCC_41 VCC_42 VCC_43 VCC_44 VCC_45 VCC_46 VCC_47 VCC_48 VCC_49 VCC_50 VCC_51 VCC_52 VCC_53 VCC_54 VCC_55 VCC_56 VCC_57 VCC_58 VCC_59 VCC_60 VCC_61

VCC CORE

POWER

VCC NCTF

+1.05V

VCC_NCTF_1 VCC_NCTF_2 VCC_NCTF_3 VCC_NCTF_4 VCC_NCTF_5 VCC_NCTF_6 VCC_NCTF_7 VCC_NCTF_8 VCC_NCTF_9 VCC_NCTF_10 VCC_NCTF_11 VCC_NCTF_12 VCC_NCTF_13 VCC_NCTF_14 VCC_NCTF_15 VCC_NCTF_16 VCC_NCTF_17 VCC_NCTF_18 VCC_NCTF_19 VCC_NCTF_20 VCC_NCTF_21 VCC_NCTF_22 VCC_NCTF_23 VCC_NCTF_24 VCC_NCTF_25 VCC_NCTF_26 VCC_NCTF_27 VCC_NCTF_28 VCC_NCTF_29 VCC_NCTF_30 VCC_NCTF_31 VCC_NCTF_32 VCC_NCTF_33 VCC_NCTF_34 VCC_NCTF_35 VCC_NCTF_36 VCC_NCTF_37 VCC_NCTF_38

CANTIGASFF_1p0

U17G

+1.8VSUS

+VCC_SM_BB36
+VCC_SM_BE35
C198 0.1u/10V_4
C204 0.1u/10V_4

VCC_SM :3000mA

+VCC_SM_BC29
C200 0.1u/10V_4

+VCC_SM_BF24
+VCC_SM_BL19
+VCC_SM_BB16
C203 0.1u/10V_4
C379 0.1u/10V_4
C201 0.1u/10V_4

VCC_SM_1 VCC_SM_2 VCC_SM_3 VCC_SM_4 VCC_SM_5 VCC_SM_6 VCC_SM_7 VCC_SM_8 VCC_SM_9 VCC_SM_10 VCC_SM_11 VCC_SM_12 VCC_SM_13 VCC_SM_14 VCC_SM_15 VCC_SM_16 VCC_SM_17 VCC_SM_18 VCC_SM_19 VCC_SM_20 VCC_SM_21 VCC_SM_22 VCC_SM_23 VCC_SM_24 VCC_SM_25 VCC_SM_26 VCC_SM_27 VCC_SM_28 VCC_SM_29 VCC_SM_30 VCC_SM_31 VCC_SM_32 VCC_SM_33

VCC SM

POWER

+VGFX

VCC_AXG_1 VCC_AXG_2 VCC_AXG_3 VCC_AXG_4 VCC_AXG_5 VCC_AXG_6 VCC_AXG_7 VCC_AXG_8 VCC_AXG_9 VCC_AXG_10 VCC_AXG_11 VCC_AXG_12 VCC_AXG_13 VCC_AXG_14 VCC_AXG_15 VCC_AXG_16 VCC_AXG_17 VCC_AXG_18 VCC_AXG_19 VCC_AXG_20 VCC_AXG_21 VCC_AXG_22 VCC_AXG_23 VCC_AXG_24 VCC_AXG_25 VCC_AXG_26 VCC_AXG_27 VCC_AXG_28 VCC_AXG_29 VCC_AXG_30 VCC_AXG_31 VCC_AXG_32 VCC_AXG_33 VCC_AXG_34 VCC_AXG_35 VCC_AXG_36 VCC_AXG_37 VCC_AXG_38 VCC_AXG_39 VCC_AXG_40 VCC_AXG_41 VCC_AXG_42 VCC_AXG_43 VCC_AXG_44 VCC_AXG_45 VCC_AXG_46 VCC_AXG_47 VCC_AXG_48 VCC_AXG_49 VCC_AXG_50 VCC_AXG_51 VCC_AXG_52 VCC_AXG_53 VCC_AXG_54 VCC_AXG_55 VCC_AXG_56 VCC_AXG_57 VCC_AXG_58 VCC_AXG_59 VCC_AXG_60 VCC_AXG_61

VCC_AXG 7700mA

VCC GFX

VCC_AXG_SENSE
VSS_AXG_SENSE

VCC GFX

CANTIGASFF_1p0

VCC_AXG_NCTF_1 VCC_AXG_NCTF_2 VCC_AXG_NCTF_3 VCC_AXG_NCTF_4 VCC_AXG_NCTF_5 VCC_AXG_NCTF_6 VCC_AXG_NCTF_7 VCC_AXG_NCTF_8 VCC_AXG_NCTF_9 VCC_AXG_NCTF_10 VCC_AXG_NCTF_11 VCC_AXG_NCTF_12 VCC_AXG_NCTF_13 VCC_AXG_NCTF_14 VCC_AXG_NCTF_15 VCC_AXG_NCTF_16 VCC_AXG_NCTF_17 VCC_AXG_NCTF_18 VCC_AXG_NCTF_19 VCC_AXG_NCTF_20 VCC_AXG_NCTF_21 VCC_AXG_NCTF_22 VCC_AXG_NCTF_23 VCC_AXG_NCTF_24 VCC_AXG_NCTF_25 VCC_AXG_NCTF_26 VCC_AXG_NCTF_27 VCC_AXG_NCTF_28 VCC_AXG_NCTF_29 VCC_AXG_NCTF_30 VCC_AXG_NCTF_31 VCC_AXG_NCTF_32 VCC_AXG_NCTF_33 VCC_AXG_NCTF_34 VCC_AXG_NCTF_35 VCC_AXG_NCTF_36 VCC_AXG_NCTF_37 VCC_AXG_NCTF_38 VCC_AXG_NCTF_39 VCC_AXG_NCTF_40 VCC_AXG_NCTF_41 VCC_AXG_NCTF_42 VCC_AXG_NCTF_43 VCC_AXG_NCTF_44

VCC GFX NCTF

VCC_AXG_62 VCC_AXG_63 VCC_AXG_64 VCC_AXG_65 VCC_AXG_66 VCC_AXG_67 VCC_AXG_68 VCC_AXG_69 VCC_AXG_70 VCC_AXG_71 VCC_AXG_72 VCC_AXG_73 VCC_AXG_74 VCC_AXG_75 VCC_AXG_76 VCC_AXG_77 VCC_AXG_78 VCC_AXG_79 VCC_AXG_80

VCC GFX

VCC_SM_LF1 VCC_SM_LF2 VCC_SM_LF3 VCC_SM_LF4 VCC_SM_LF5 VCC_SM_LF6 VCC_SM_LF7

VCC SM LF

VCCSM_LF1 VCCSM_LF2 VCCSM_LF3 VCCSM_LF4 VCCSM_LF5 VCCSM_LF6 VCCSM_LF7

10mil

C165 0.1u/10V_4
C191 0.1u/10V_4
C210 0.22u/10V_4
C202 0.22u/10V_4
C220 0.47u/6.3V_4
C381 1u/10V_6
C382 1u/10V_6

+VGFX
R123 12@10/F_4
R117 12@10/F_4

Differential routing
[29] GFX_VCCSENSE
[29] GFX_VSSSENSE

+VGFX
R119 12@0_8
R120 12@0_8

+1.05V
C179 0.1u/10V_4
C115 0.22u/10V_4
C145 0.22u/10V_4
C196 *10u/6.3V_8
C207 *220u/2.5V_3528

Layout Note:
Inside GMCH cavity.

+1.8VSUS
C209 0.1u/10V_4
C211 10u/6.3V_8
C214 10u/6.3V_8

+VGFX
C108 0.47u/6.3V_4
C163 *1u/16V_6
C162 10u/6.3V_6
C123 10u/6.3V_8
C114 0.1u/10V_4
C109 0.1u/10V_4

+VGFX
C83 *220u/2.5V_3528
C125 220u/2.5V_3528

Close to GMCH

Layout Note:
370 mils from edge.

1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +VGFX_CORE_INT with 100ohm
and VSS_AXG_SENSE PD with 10ohm for Intel suggest

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QUANTA COMPUTER

Title	Cantiga SFF (VCC/NCTF)	
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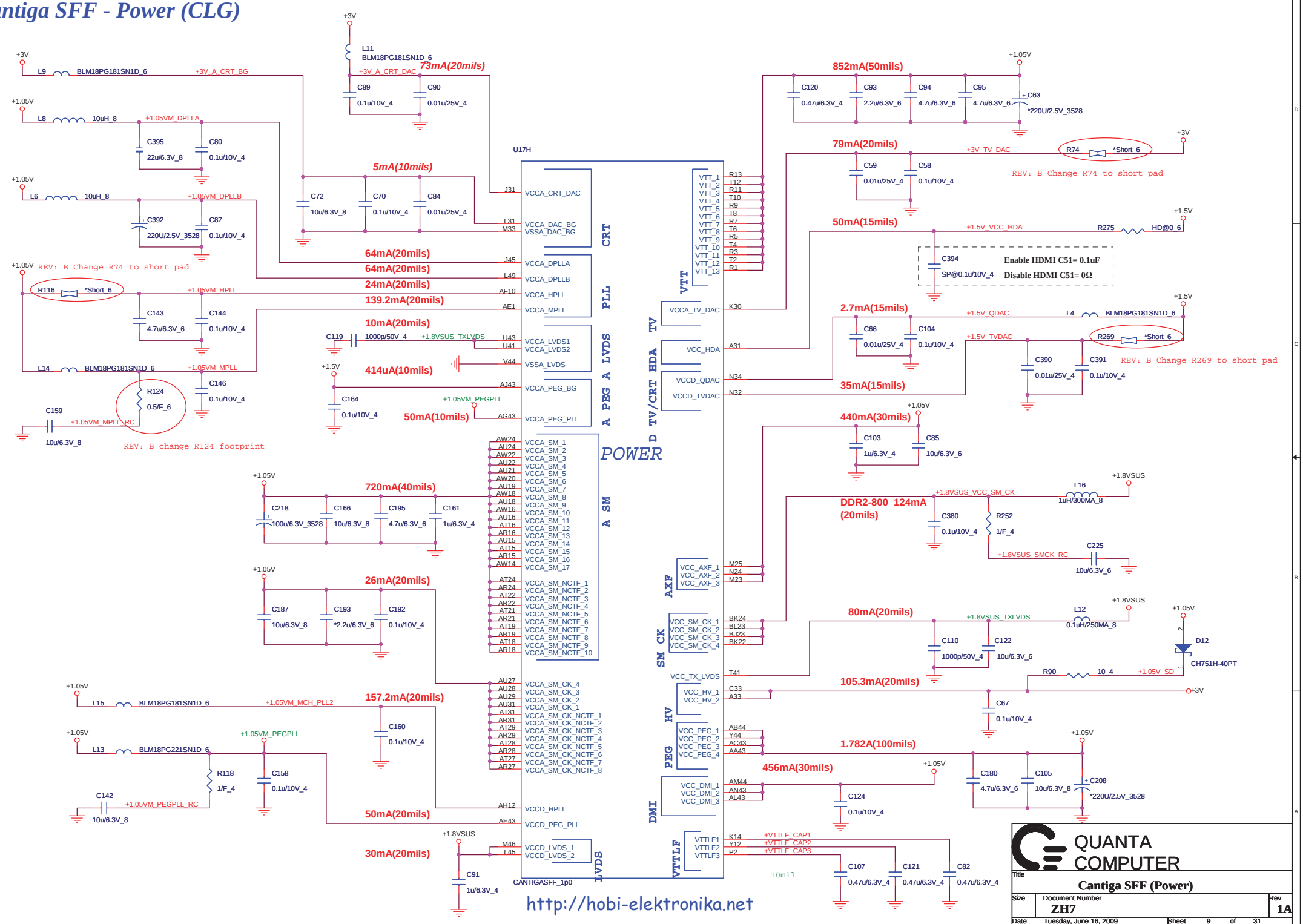
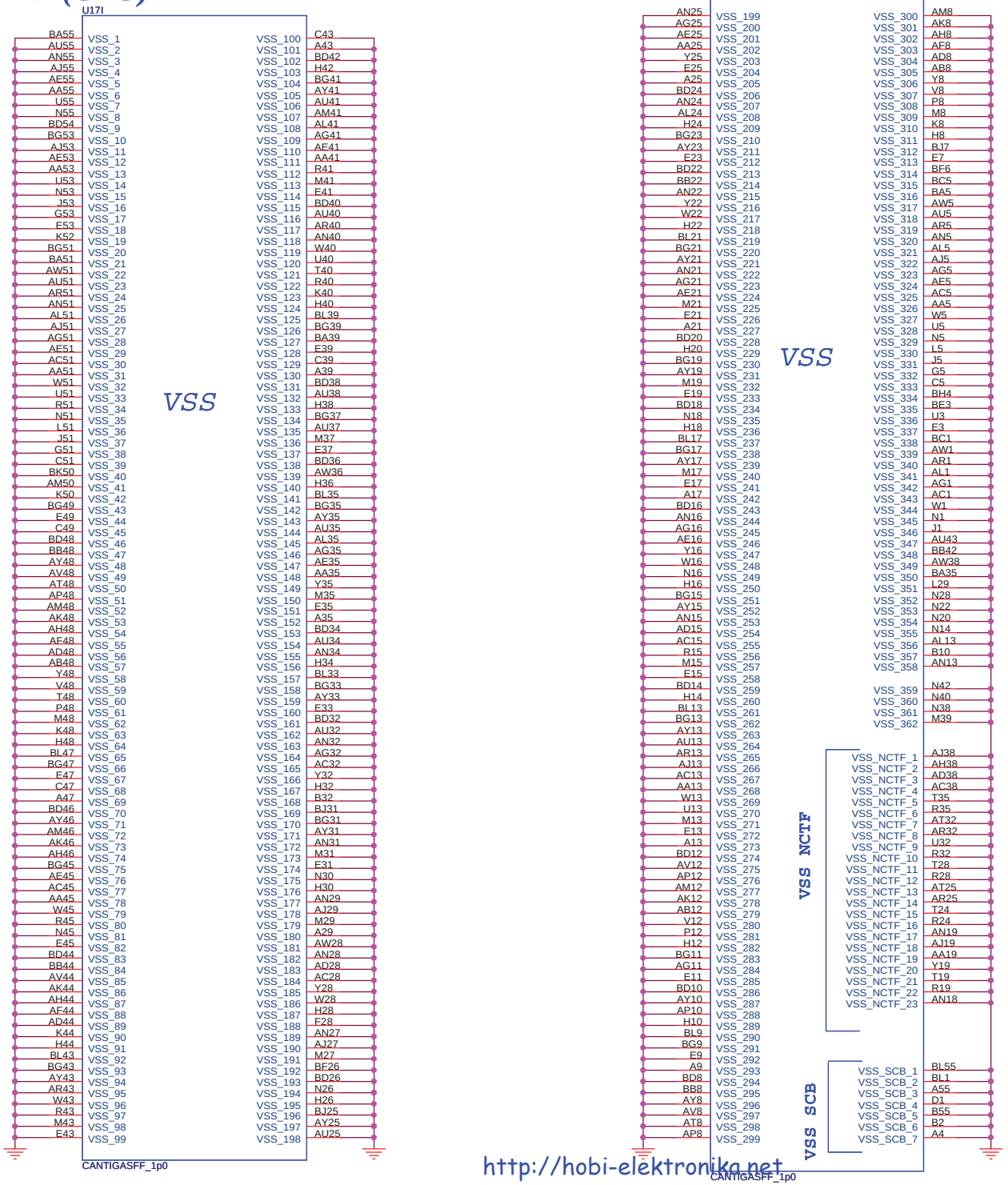
Cantiga SFF - Power (CLG)



Cantiga SFF - GND (CLG)



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QUANTA COMPUTER

Title	Cantiga SFF (GND)	
Size	Document Number: ZH7	Rev: 1A
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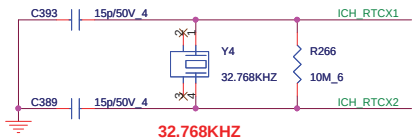
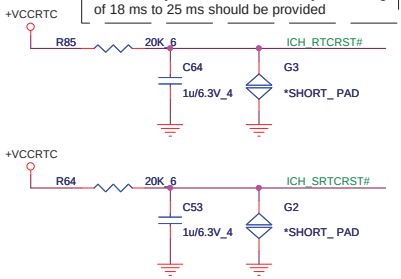
RTC CRYSTAL

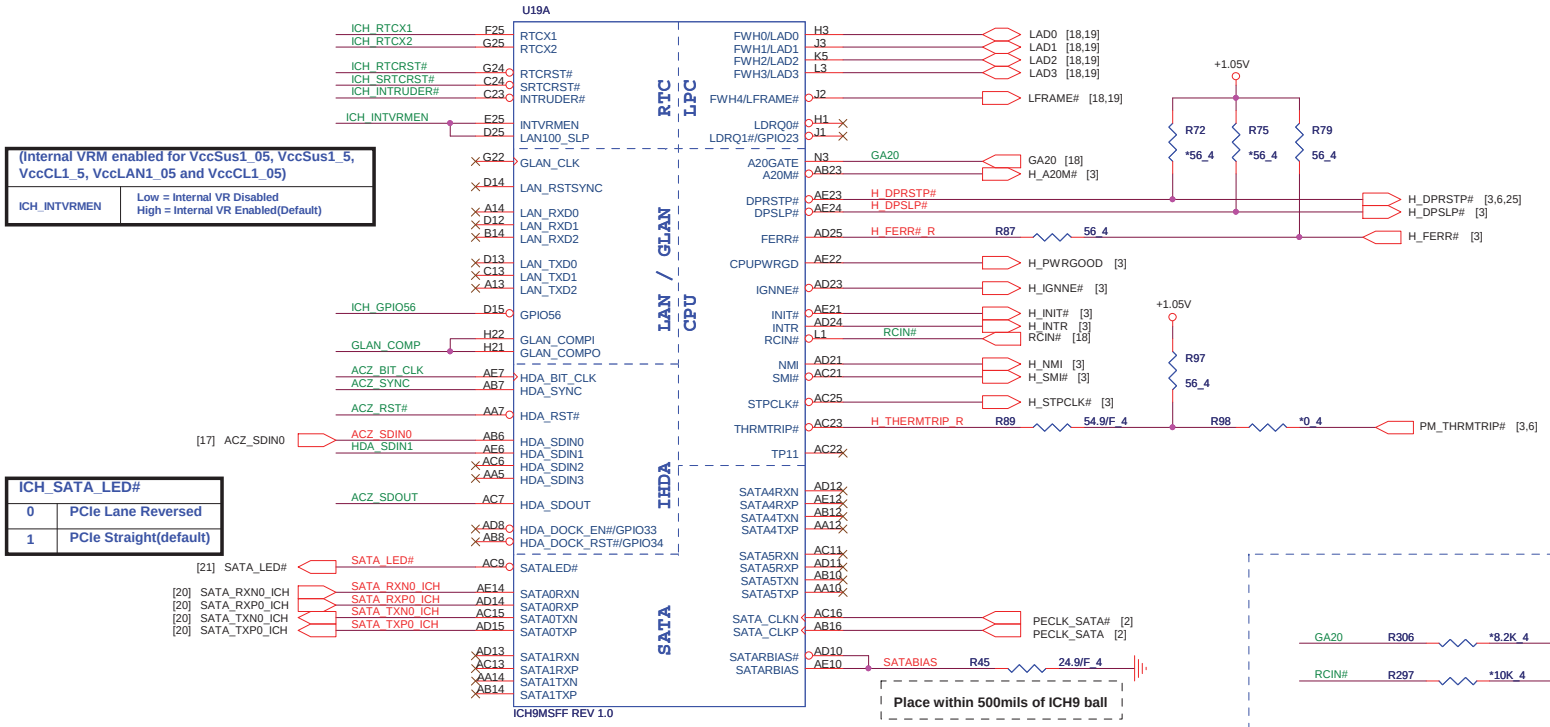


RESET JUMP

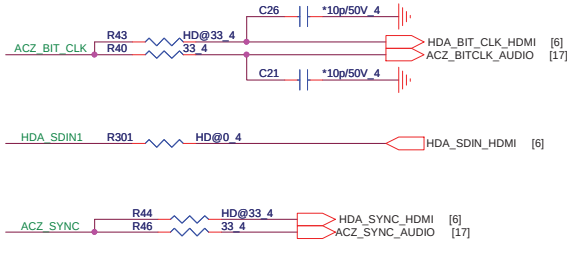
An RC delay circuit with a time delay in the range of 18 ms to 25 ms should be provided

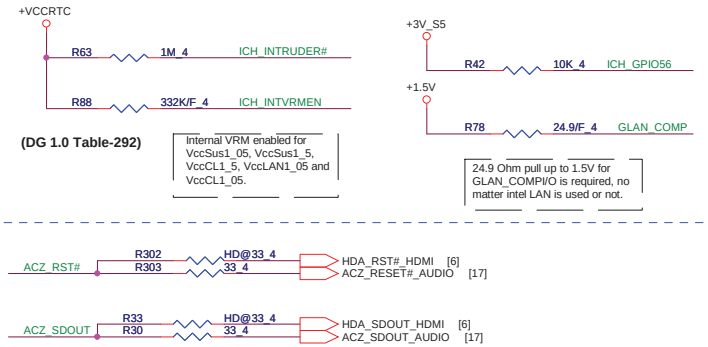


ICH9M SFF - Host,SATA,HDA (CLG)

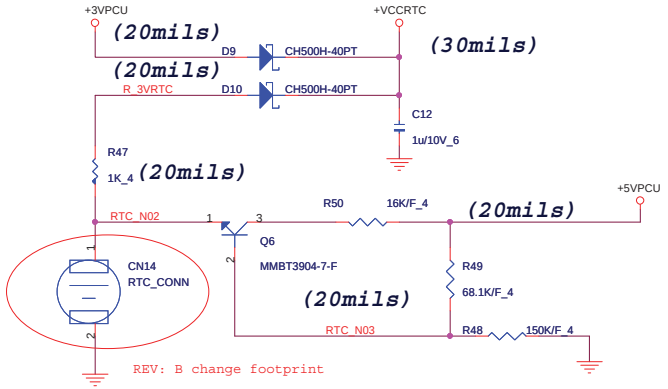


HD Audio Interface





RTC BATTERY (RTC)



South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
	XOR Chain Entrance	PWROK		
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK		

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

REV: B del. R282 , add T23

ACZ_SDOUT T24
ACZ_SYNC T25

REV: B del R36 & R39 , add T24 & T25

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QUANTA COMPUTER

Title	ICH9M SFF (Host/SATA/HDA)	
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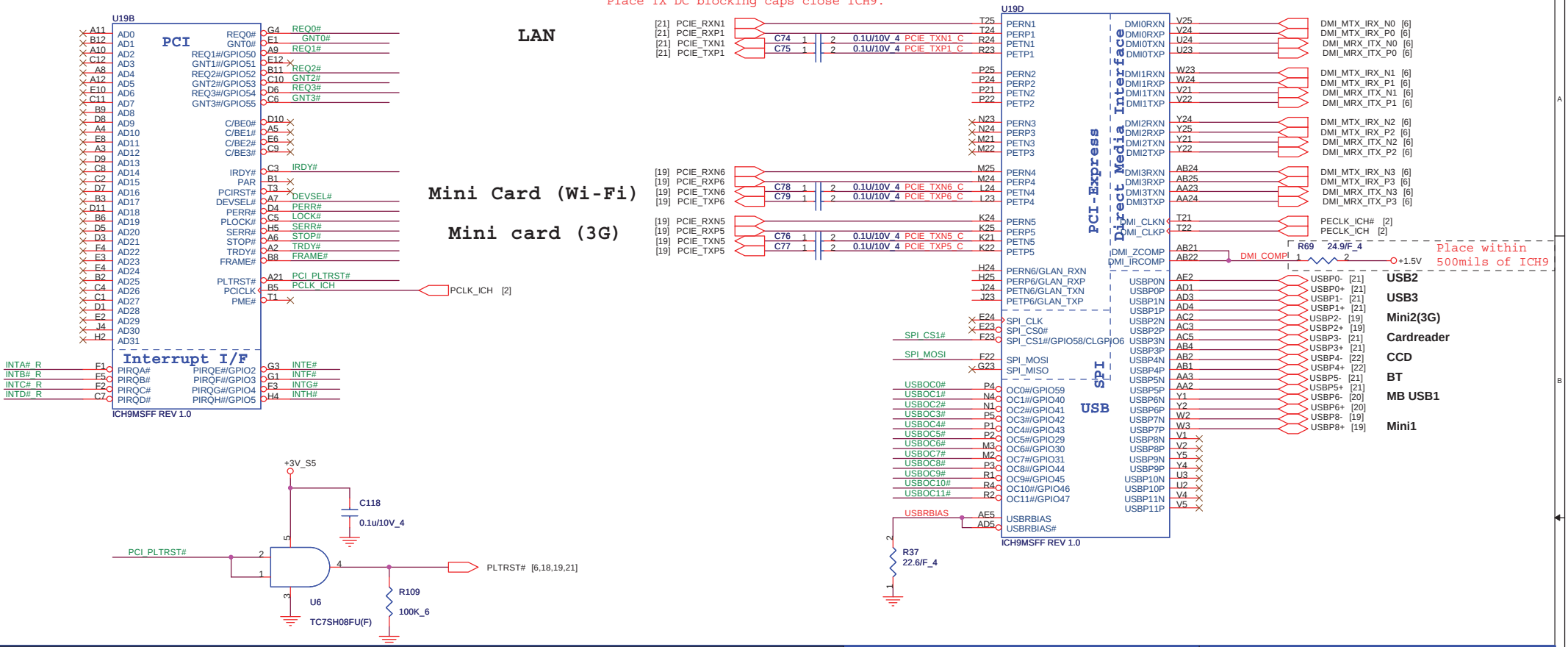
ICH9M SFF - USB/PCIE/DMI (CLG)

Place TX DC blocking caps close ICH9.

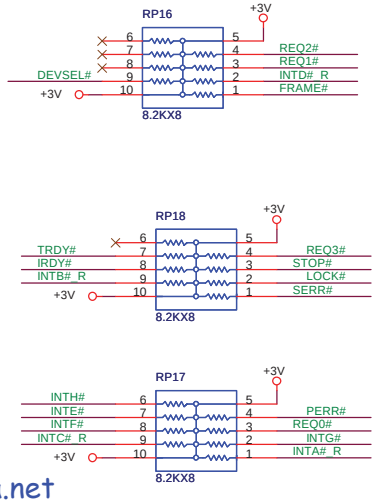


South Bridge Strap Pin (2/3)

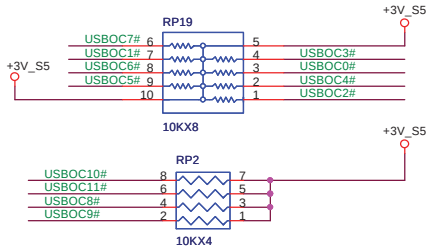
Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	GNT2# — T6
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# — T4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI — T11
GNT0#	Boot BIOS Selection 0	PWROK		GNT0# — T2
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK		SPI_CS1# — T10

PCI_GNT#0	SPI_CS#1	Boot Location
0	1	SPI(Default)
1	0	PCI

PCI PULL-UP



USBOC# PULL-UP



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QUANTA COMPUTER

Title: ICH9M SFF (USB/PCIE/DMI)

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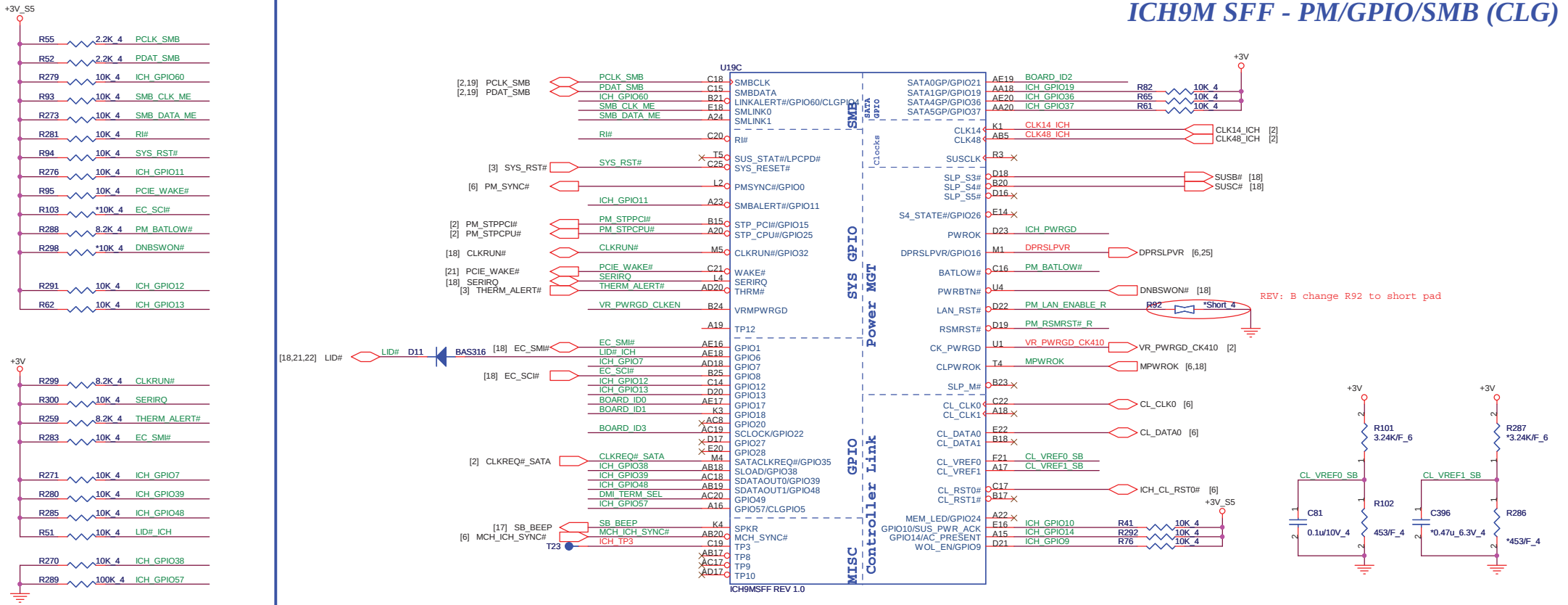
ICH9M SFF - PM/GPIO/SMB (CLG)



South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
PCBEEP	No Reboot	PWROK	0 = Default 1 = No Reboot mode	
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL — T12

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QUANTA COMPUTER

Title: ICH9M SFF (PM/GPIO/SMB)

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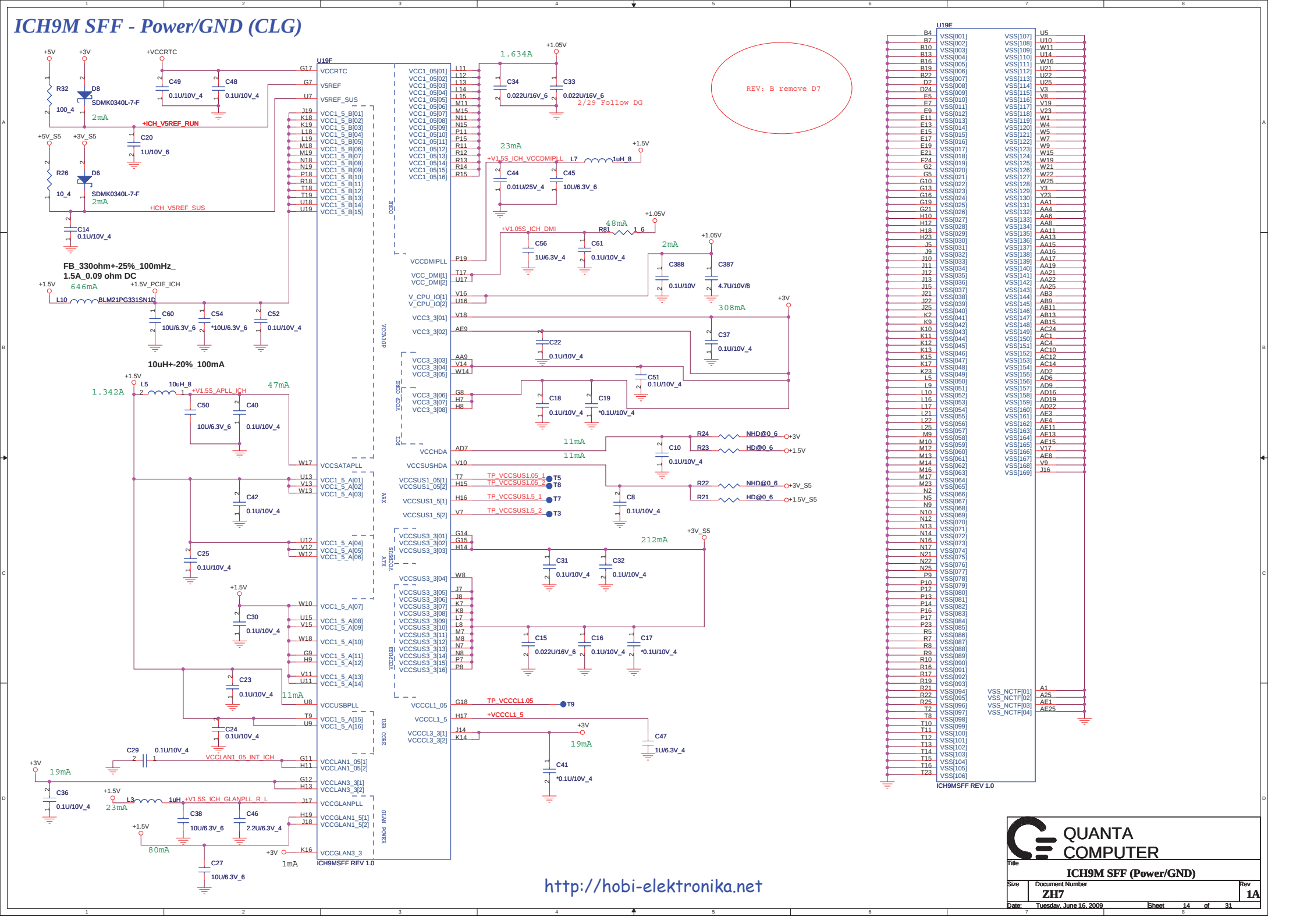
ICH9M SFF - Power/GND (CLG)



Title	ICH9M SFF (Power/GND)
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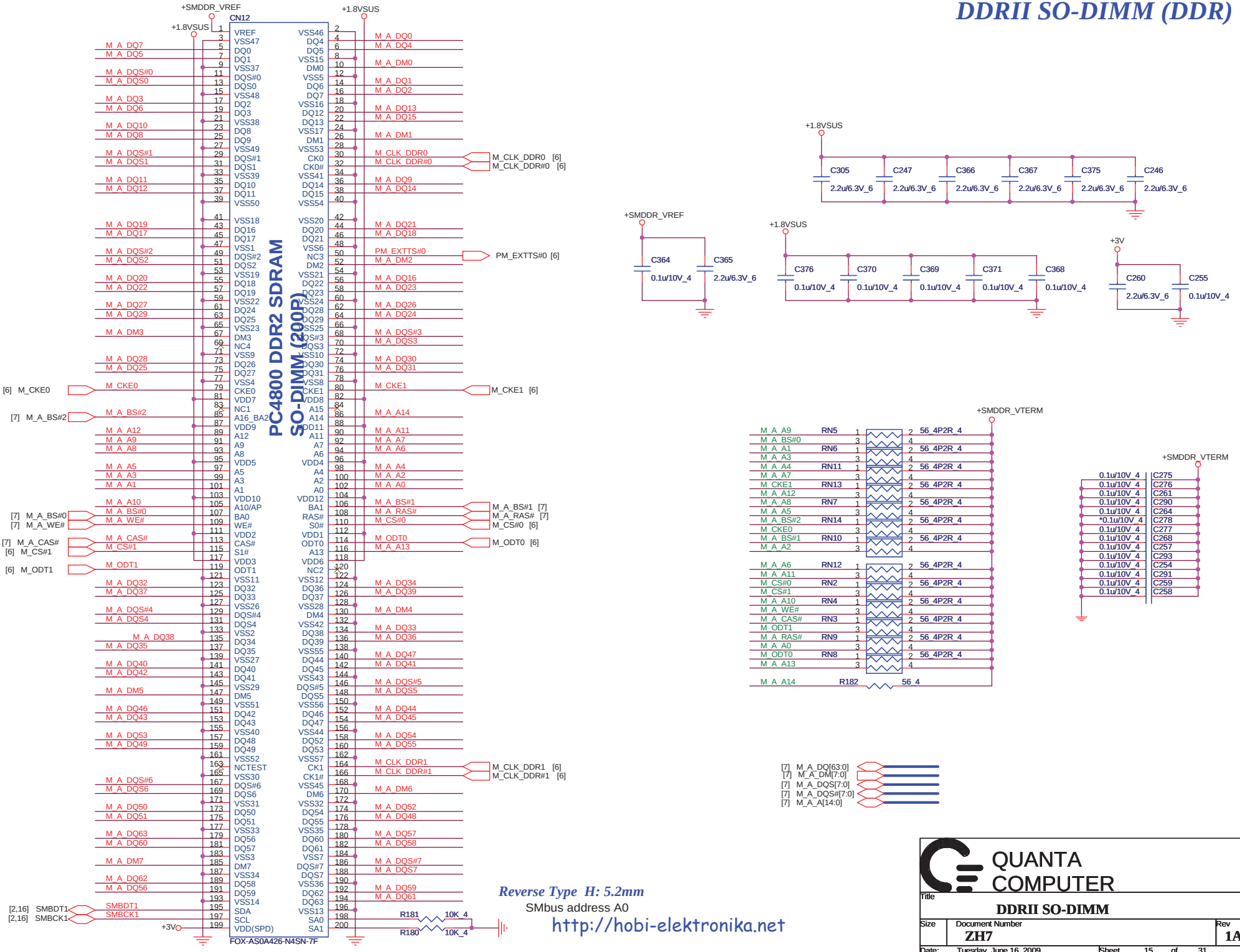
QUANTA COMPUTER

DDRII SO-DIMM (DDR)



[7] M_A_DQ[63:0]
[7] M_A_DM[7:0]
[7] M_A_DQS[7:0]
[7] M_A_DQS#[7:0]
[7] M_A_A[14:0]

Reverse Type H: 5.2mm

SMbus address A0

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QUANTA COMPUTER

Title: DDRII SO-DIMM		
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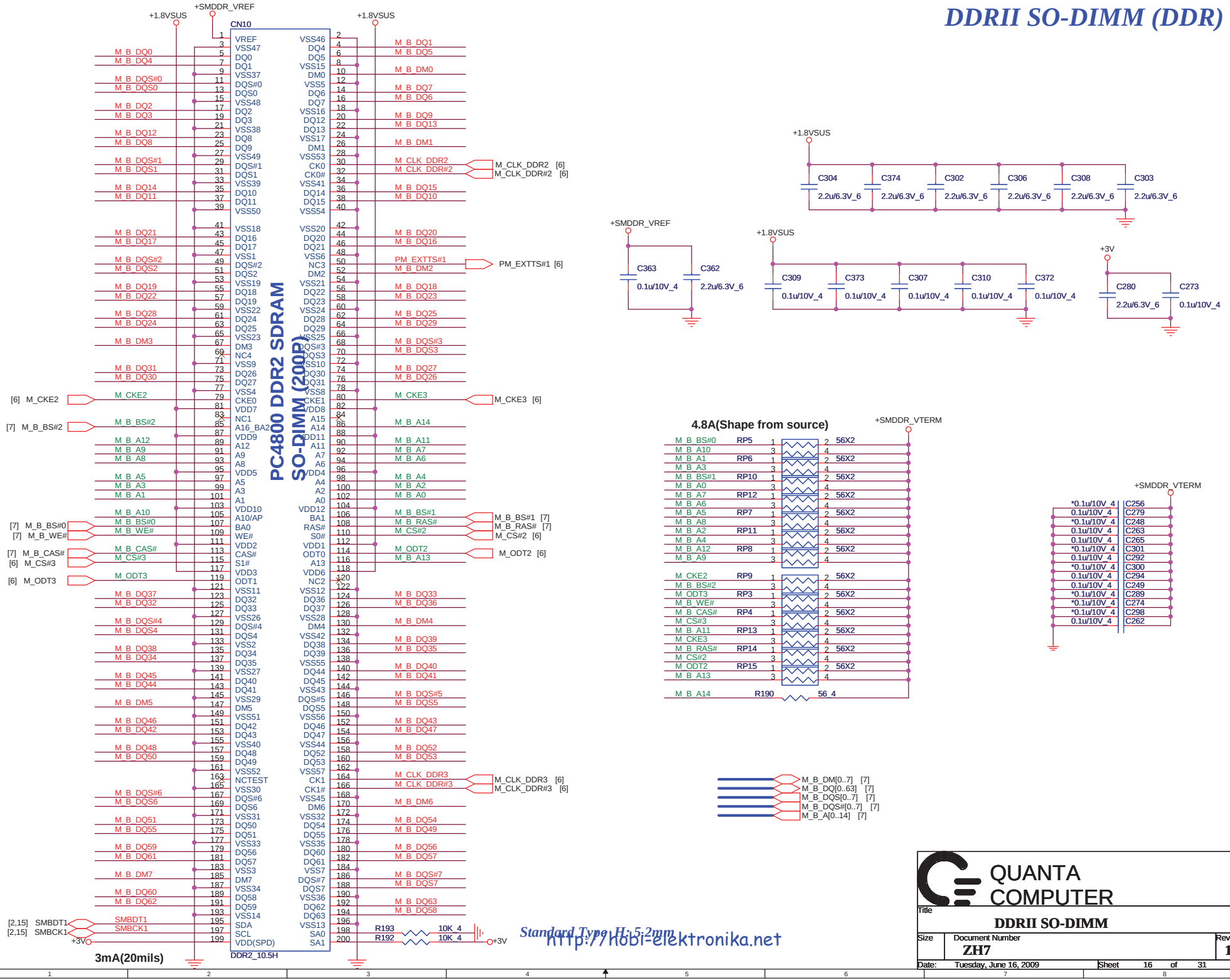
DDRII SO-DIMM (DDR)



Standard Type, H:5.2mm

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QUANTA COMPUTER

Title: DDRII SO-DIMM		
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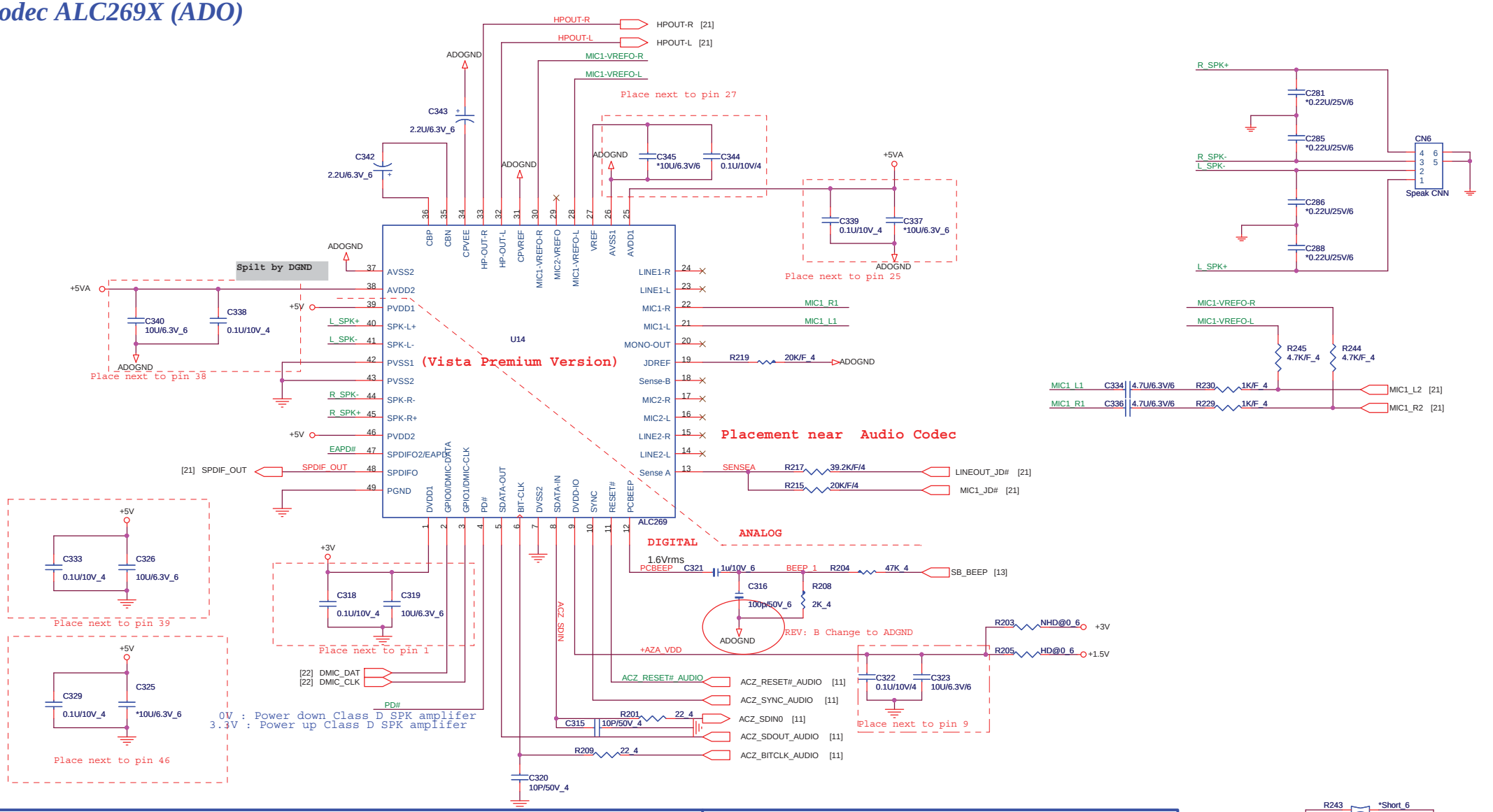
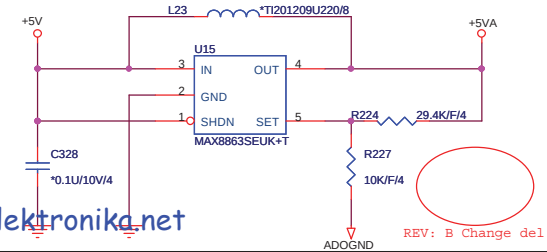
Codec ALC269X (ADO)

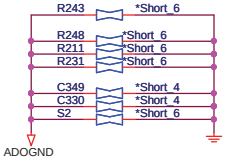


Power (ADO)

Demodulation Filter

Place close to Codec





Title	Codec ALC269X	
Size	Document Number ZH7	Rev 1A
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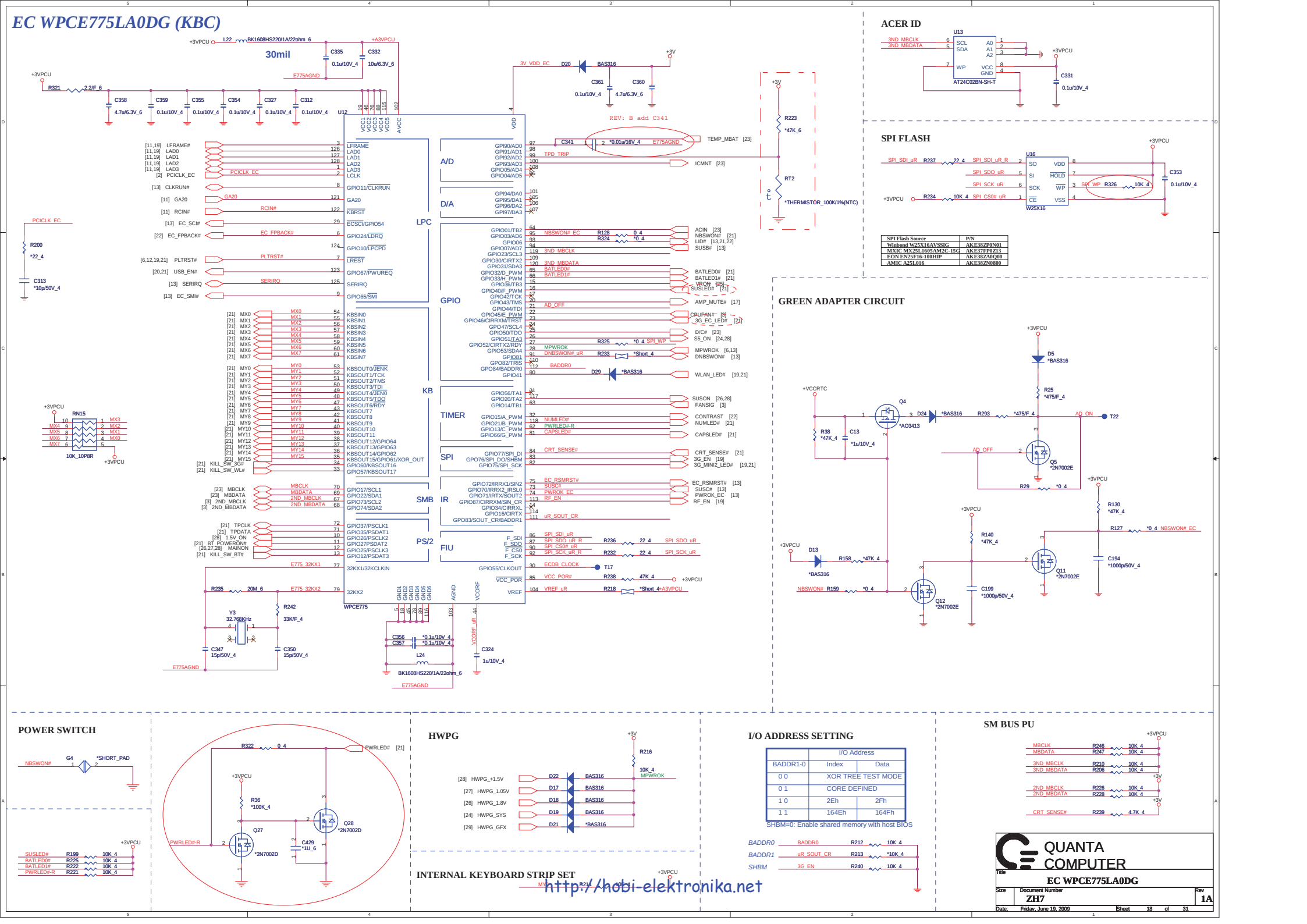
QUANTA COMPUTER

EC WPCE775LA0DG (KBC)



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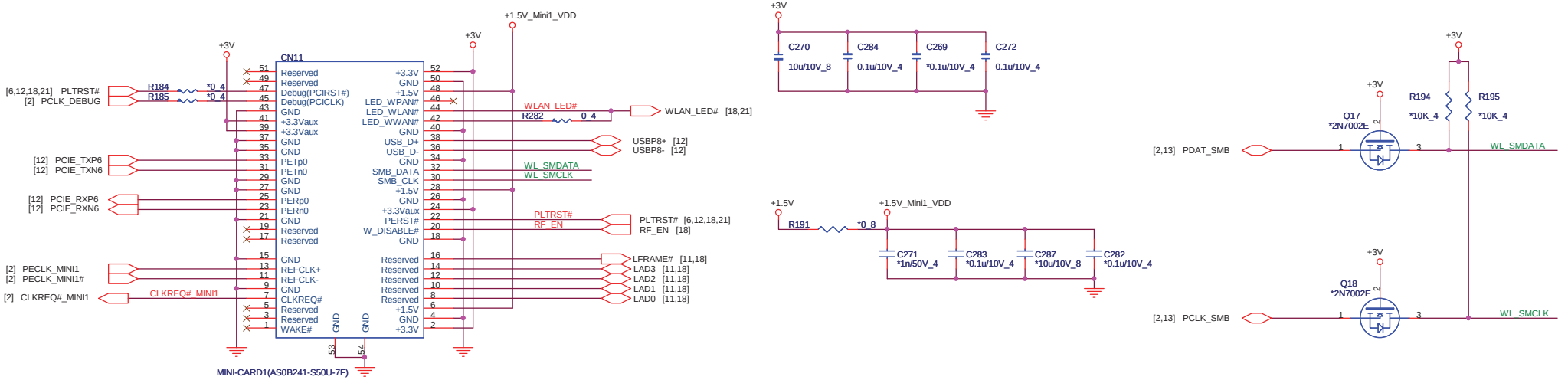
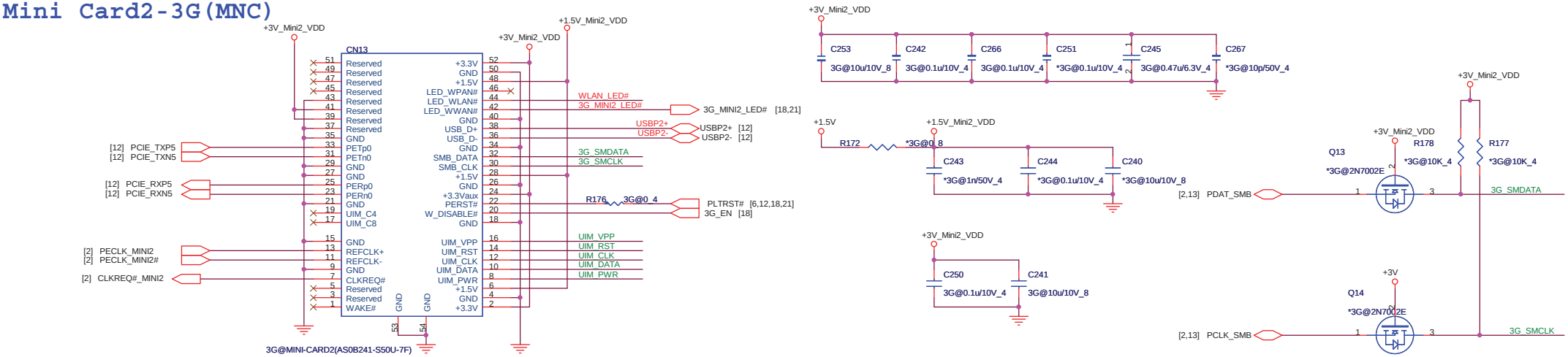
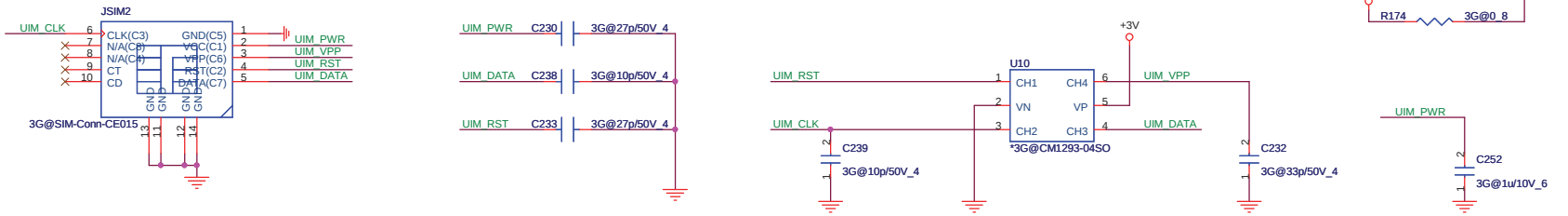
Mini Card1-WLAN/WMAX(MPC)



Mini Card2-3G(MNC)





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QUANTA COMPUTER

Title	MINI PCIE (WLAN/WMAX/3G)	
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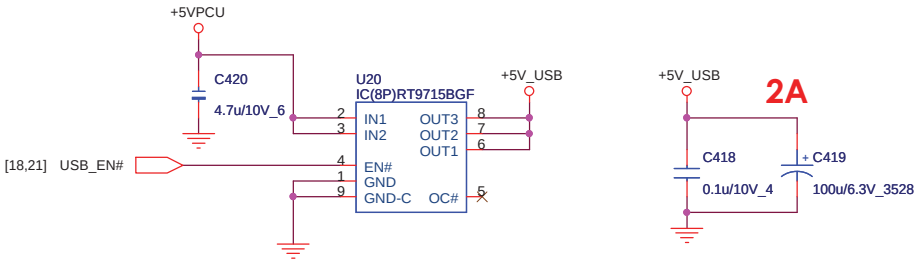
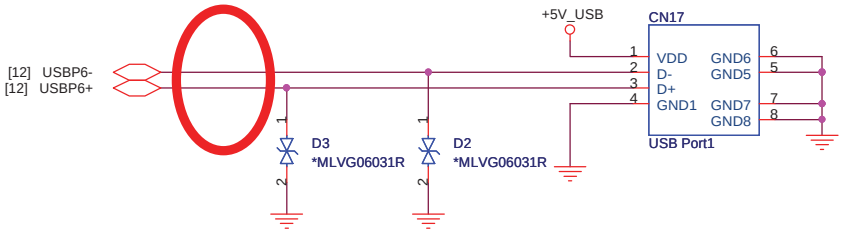
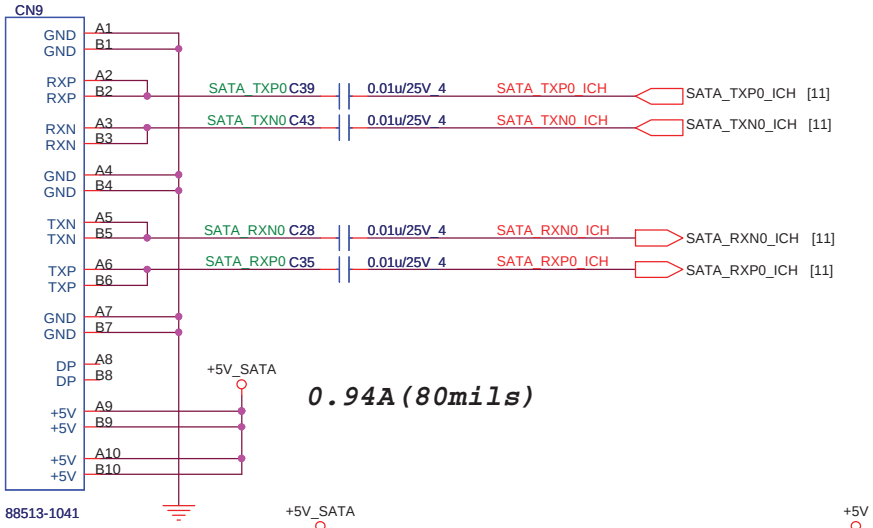
MB USB (USB)

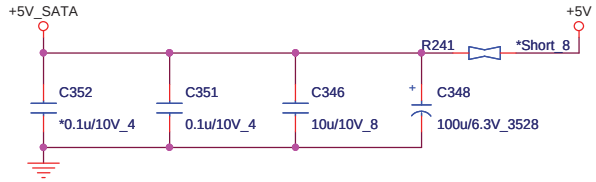


Remove R6、R7、L2

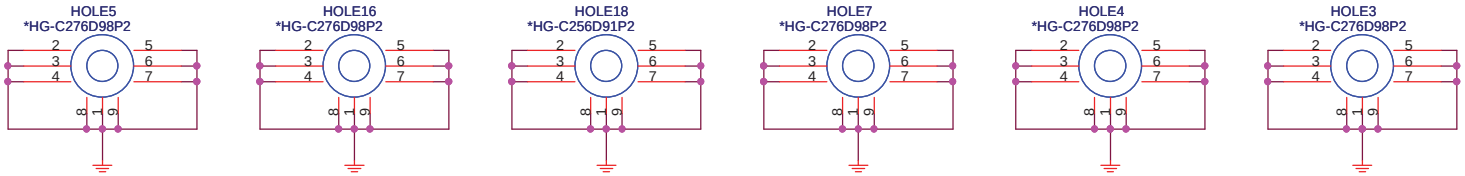


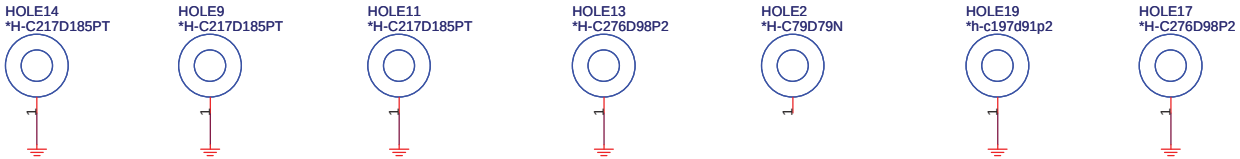
2.5" SATA HDD(HDD)

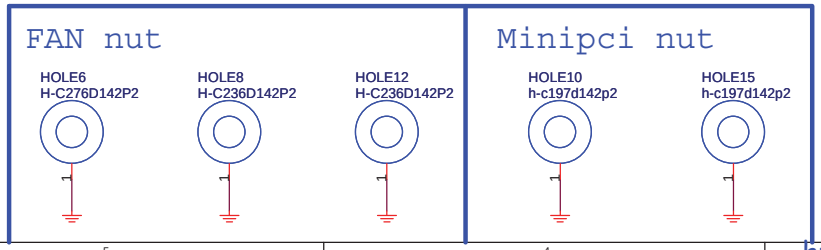


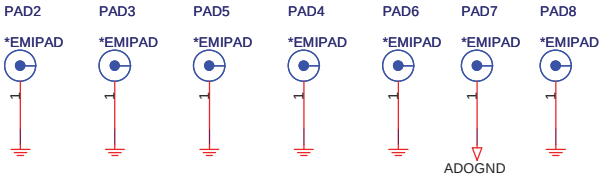


HOLE (EXC)









QUANTA COMPUTER

Title	USB/HDD/HOLE	
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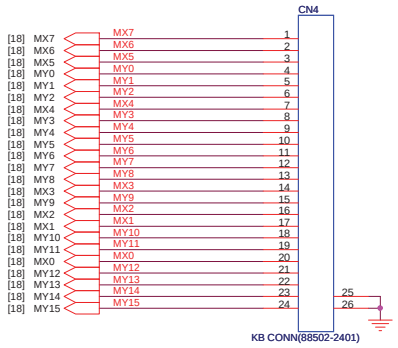
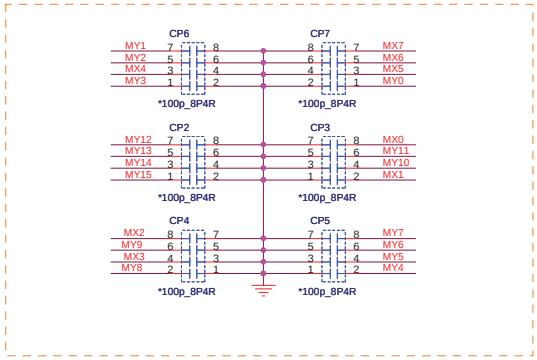
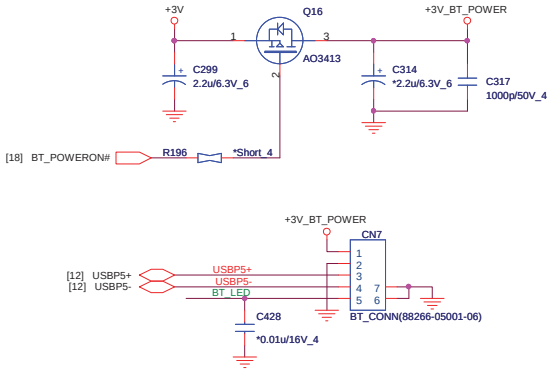
Keyboard(KBC)



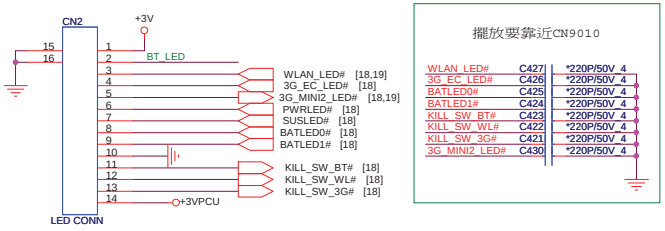
For EMI Reserve Caps for debug



BuleTooth (BTM)

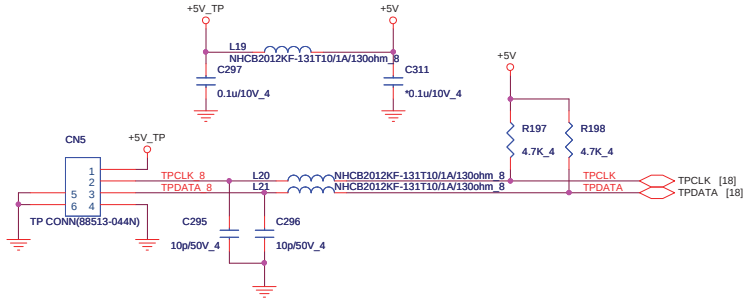


LED D/B (UIF)

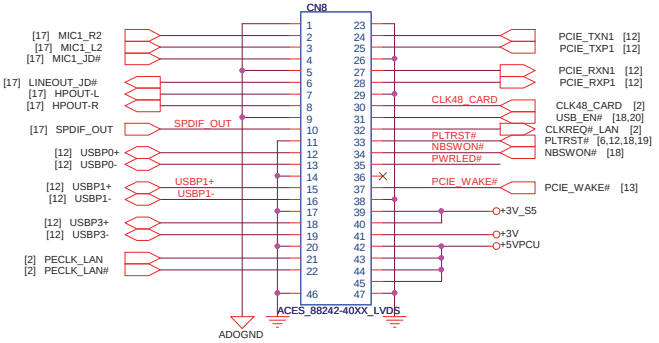


Check P/N footprint

Touch Pad D/B (TPD)

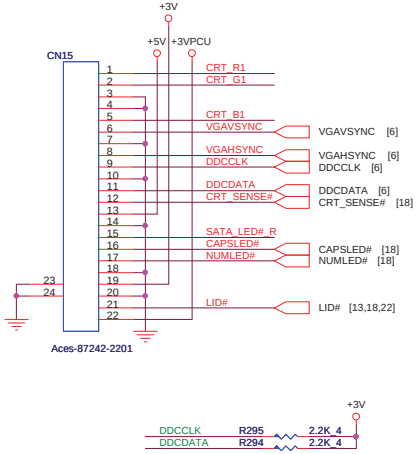


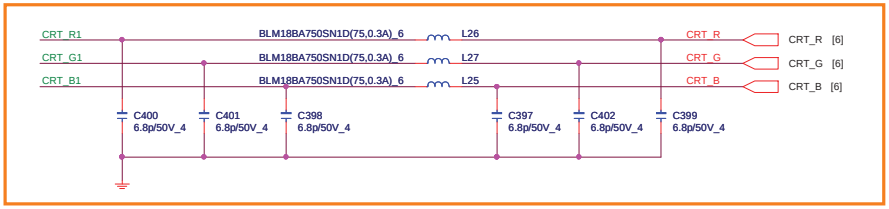
Card Reader/USB DB CONNECTER(MMC)/Power Connector



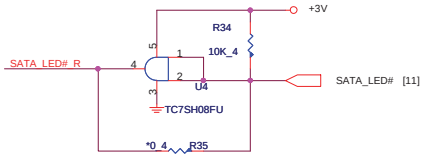
REV: B DEL CN8.36 SUSLED#

CRT D/B (UIF)





For EMI



Title	KB/BT/PR/TP/LAN/LED/CR Connects		
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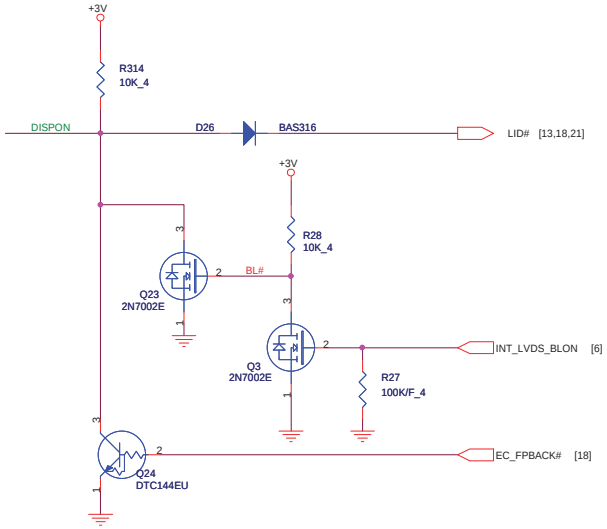
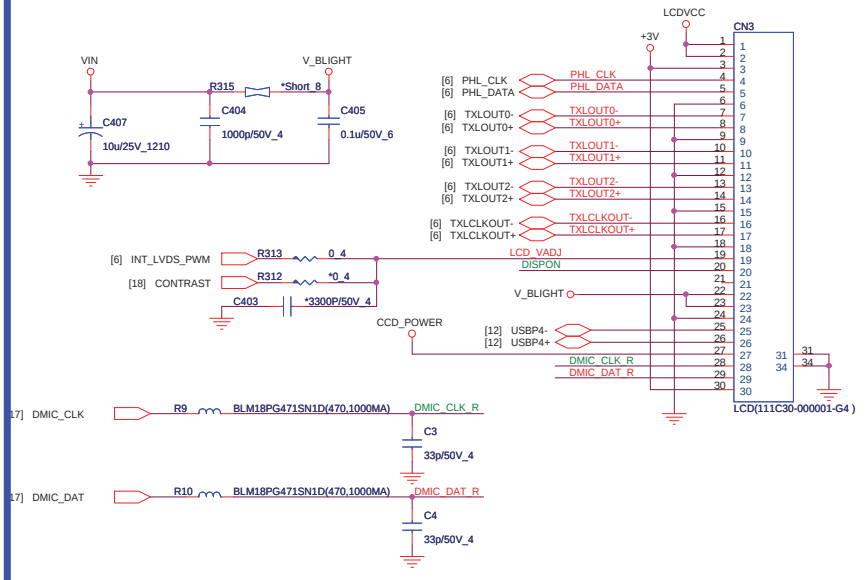
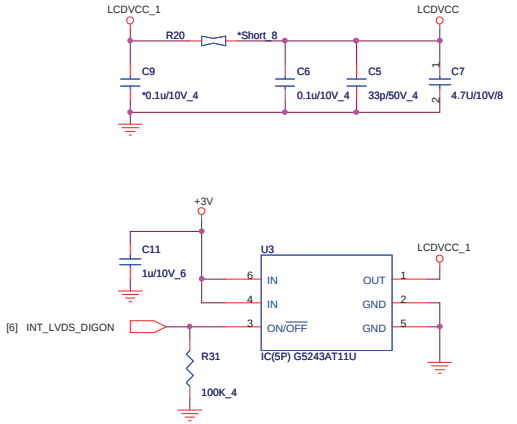
Backlight Control(LDS)



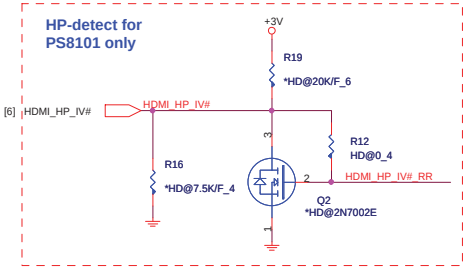
LED Panel(LDS)

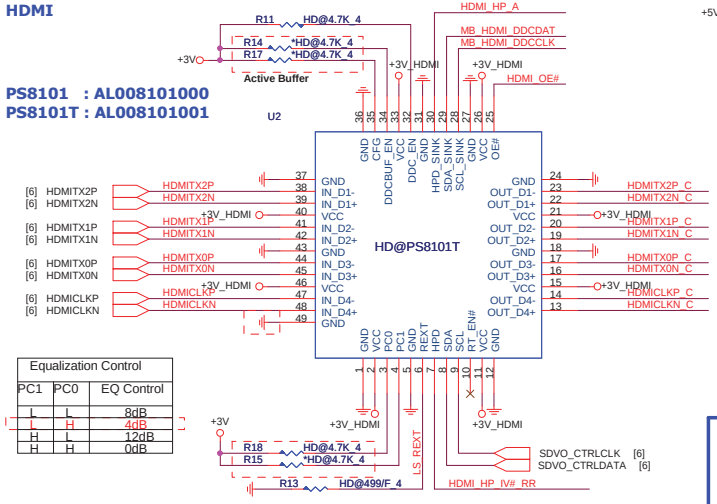


LED Panel POWER SWITCH(LDS)

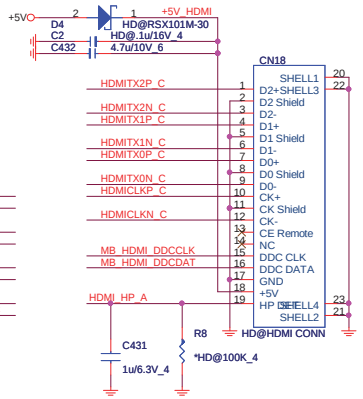


HDMI(HDM)

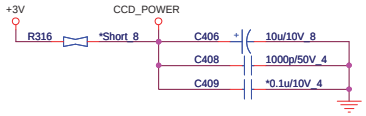




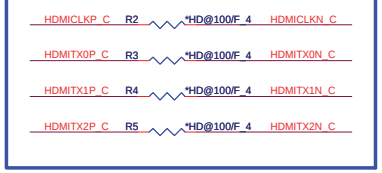
Equalization Control		
PC1	PC0	EQ Control
L	L	8dB
L	H	4dB
H	L	12dB
H	H	0dB



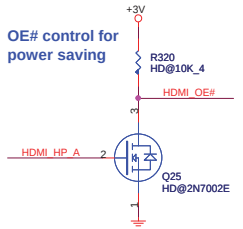
Camera(CCD)



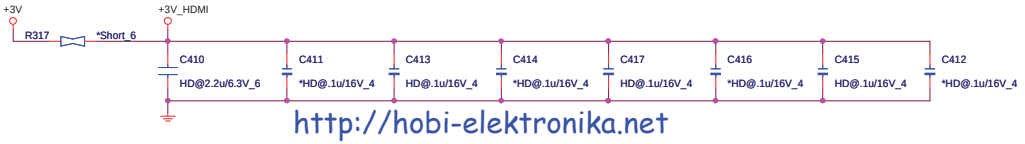
FOR EMI



OE# control for power saving



SDVO I2C Control



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QUANTA COMPUTER

Title	LED Panel/CCD/HDMI	
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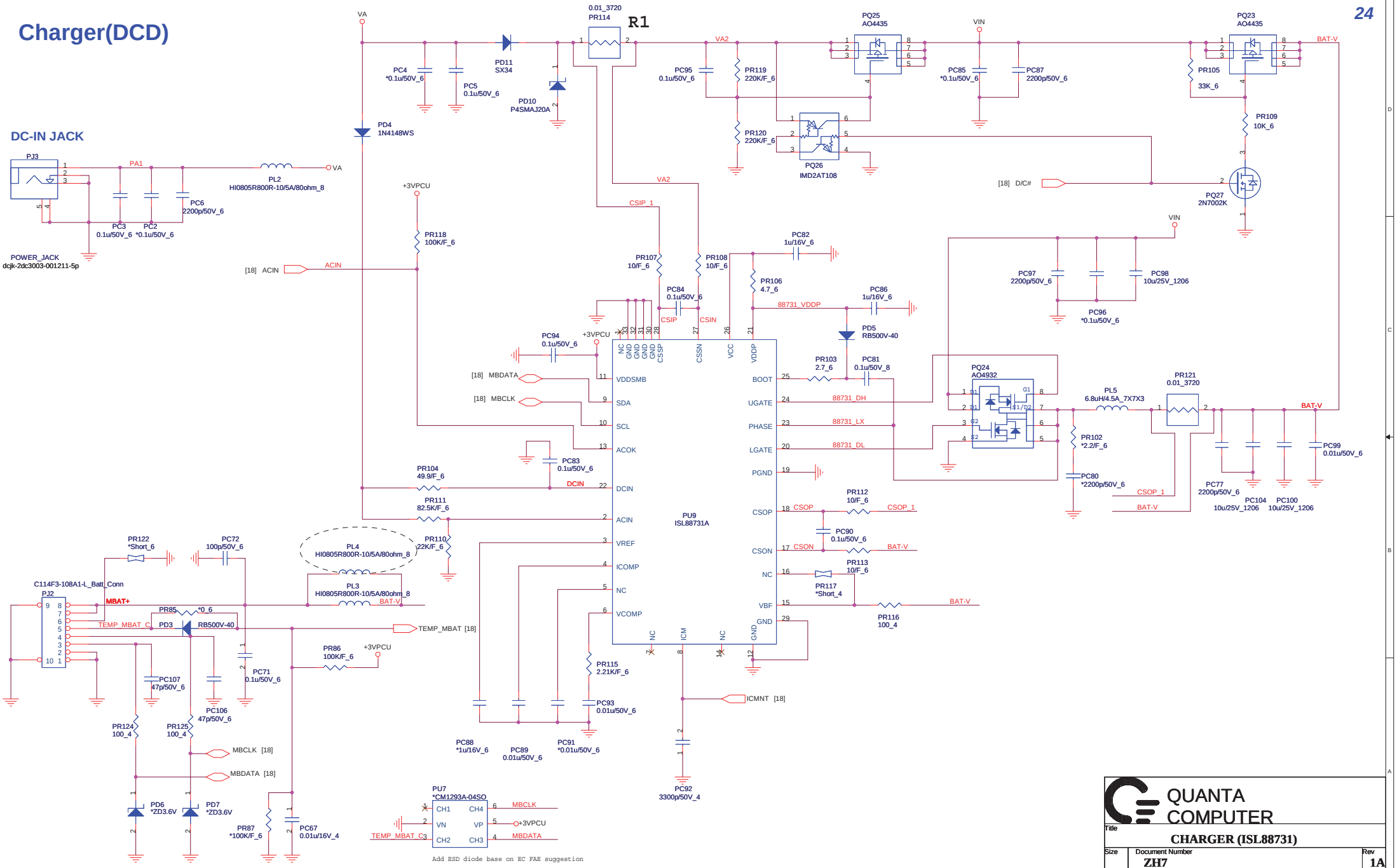
Charger(DCD)



QUANTA COMPUTER		
Title: CHARGER (ISL88731)		
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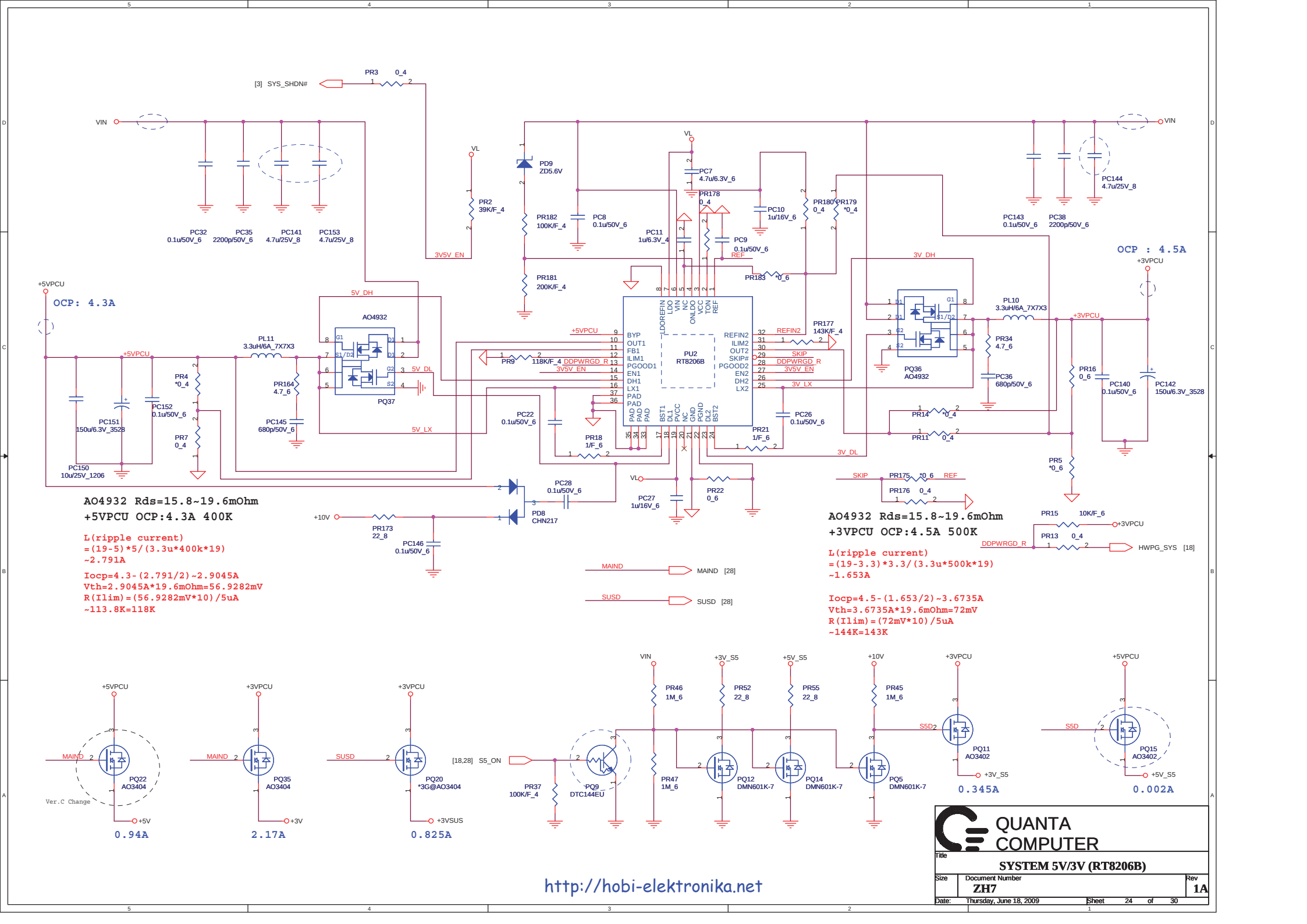
OCP: 4.3A
OCP : 4.5A
AO4932 Rds=15.8~19.6mOhm
+5VPCU OCP:4.3A 400K
L(ripple current)
=(19-5)*5/(3.3u*400k*19)
~2.791A
Iocp=4.3-(2.791/2)~2.9045A
Vth=2.9045A*19.6mOhm=56.9282mV
R(Ilim)=(56.9282mV*10)/5uA
~113.8K=118K
AO4932 Rds=15.8~19.6mOhm
+3VPCU OCP:4.5A 500K
L(ripple current)
=(19-3.3)*3.3/(3.3u*500k*19)
~1.653A
Iocp=4.5-(1.653/2)~3.6735A
Vth=3.6735A*19.6mOhm=72mV
R(Ilim)=(72mV*10)/5uA
~144K=143K
0.94A
2.17A
0.825A
0.345A
0.002A
QUANTA COMPUTER
SYSTEM 5V/3V (RT8206B)
ZH7
1A
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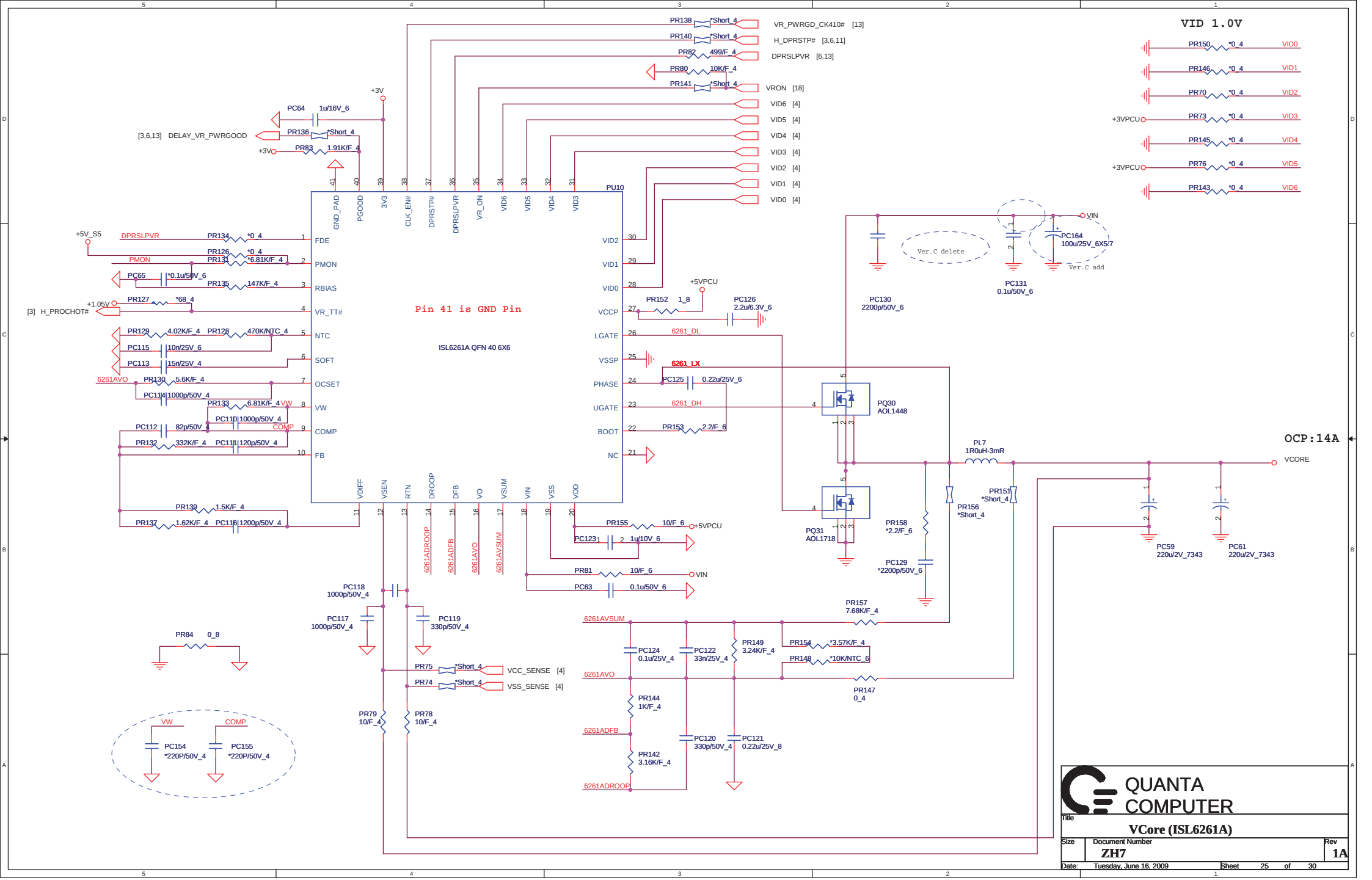

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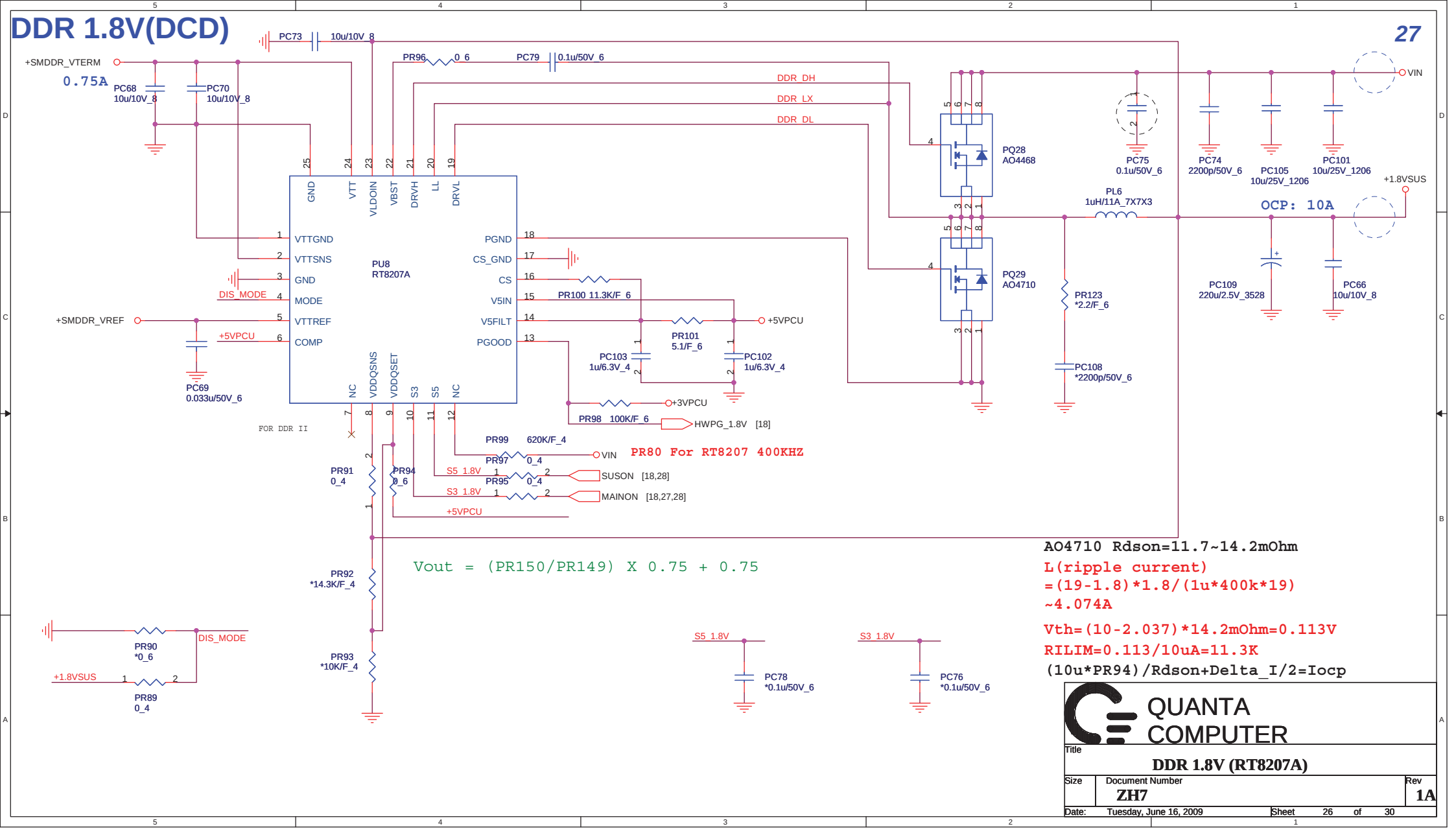
DDR 1.8V(DCD)



Vout = (PR150/PR149) X 0.75 + 0.75

AO4710 Rdson=11.7~14.2mOhm

L(ripple current)
=(19-1.8)*1.8/(1u*400k*19)
~4.074A

Vth=(10-2.037)*14.2mOhm=0.113V

RILIM=0.113/10uA=11.3K

(10u*PR94)/Rdson+Delta_I/2=Iocp

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Title: DDR 1.8V (RT8207A)		
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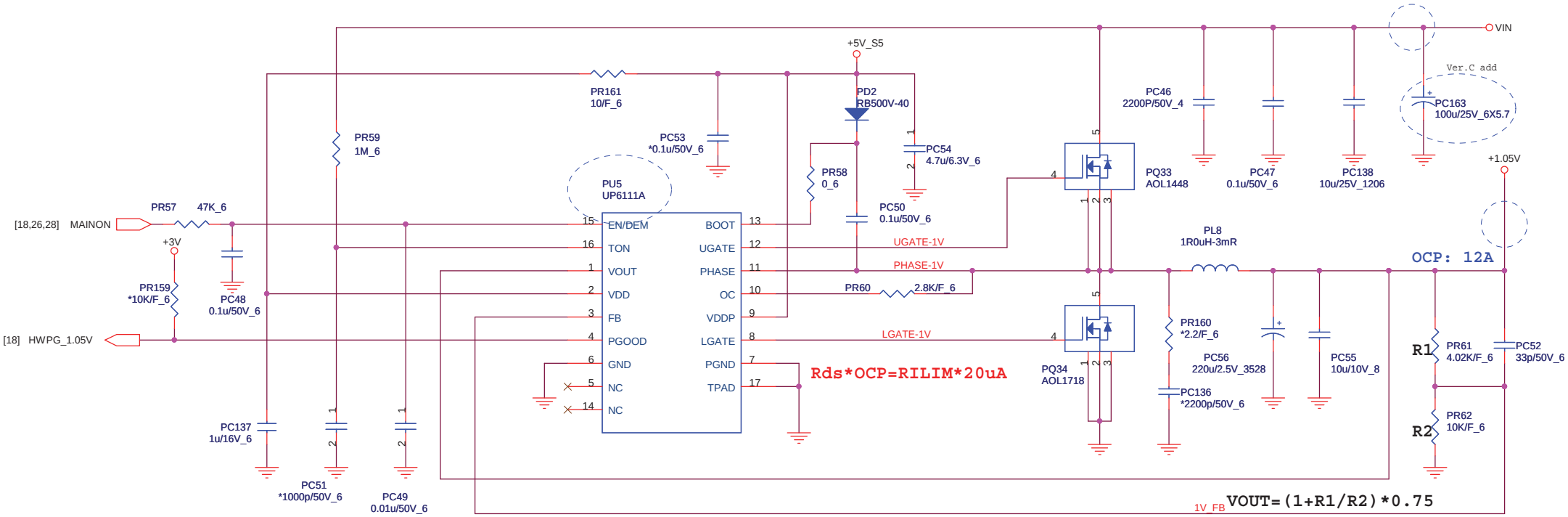


TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

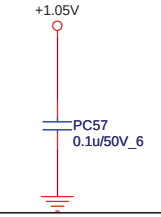
AOL1412 Rdson=4.6mOhm

OCP=16-0.8A

L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.646A

4.6m*12=RILIM*20uA

RILIM=2.76K--- 2.8K



QUANTA COMPUTER

Title: VCCP 1.05V (RT8202A)		
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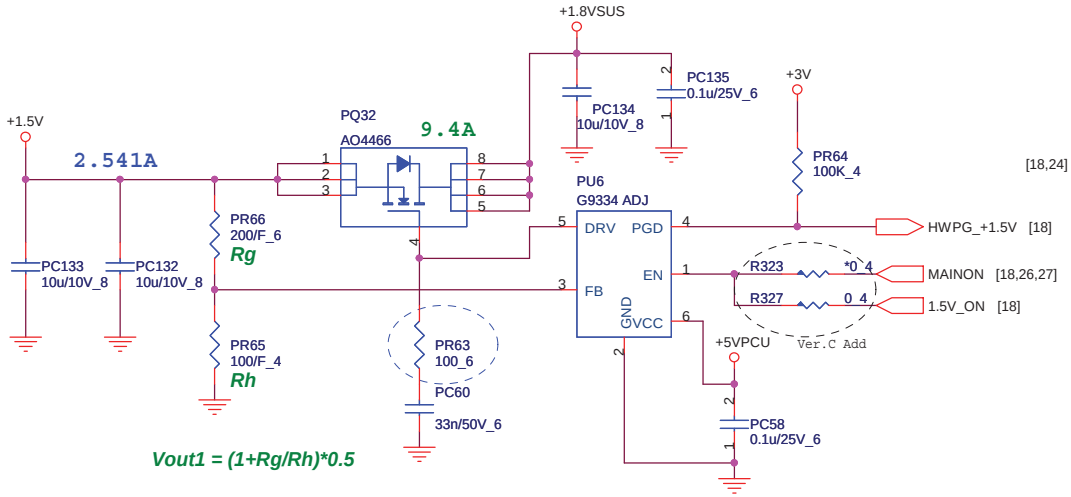
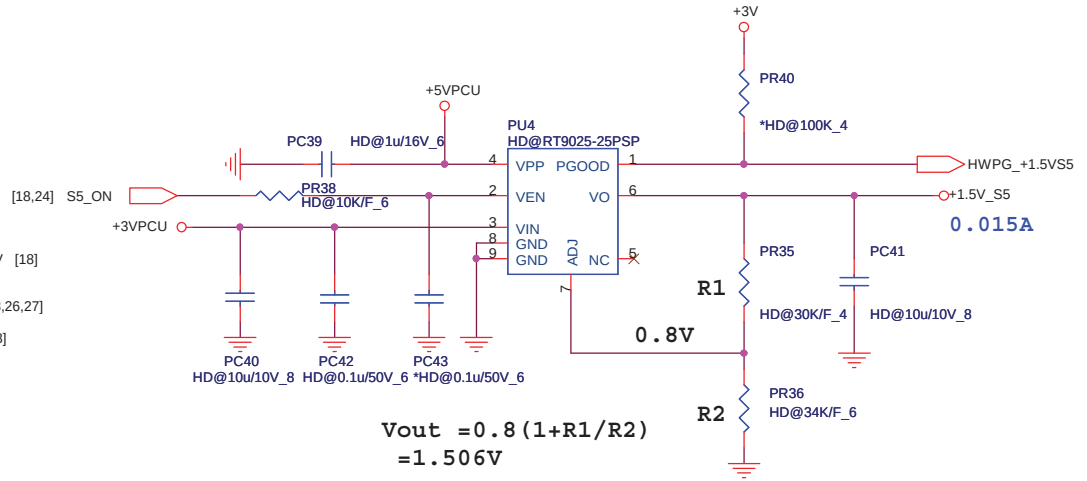
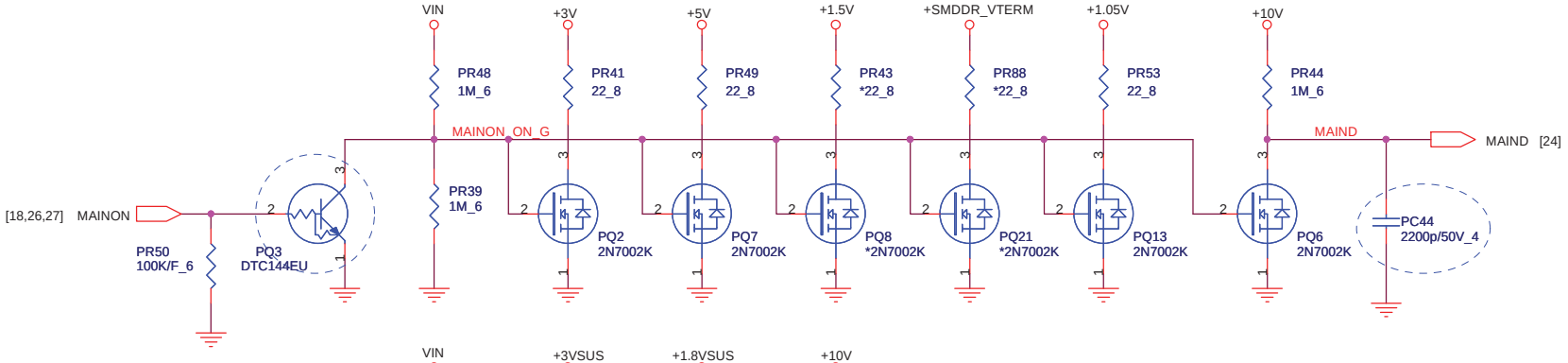
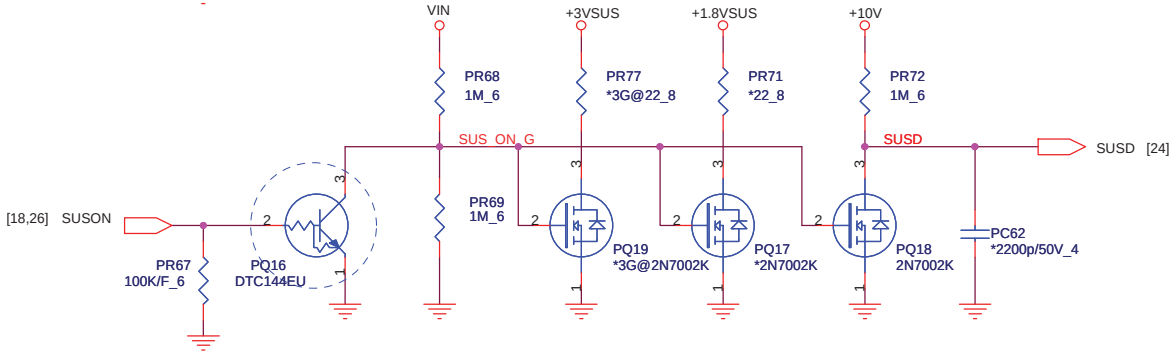
Discharger/1.5V(DCD)









QUANTA COMPUTER

Title: Discharge/1.5V		
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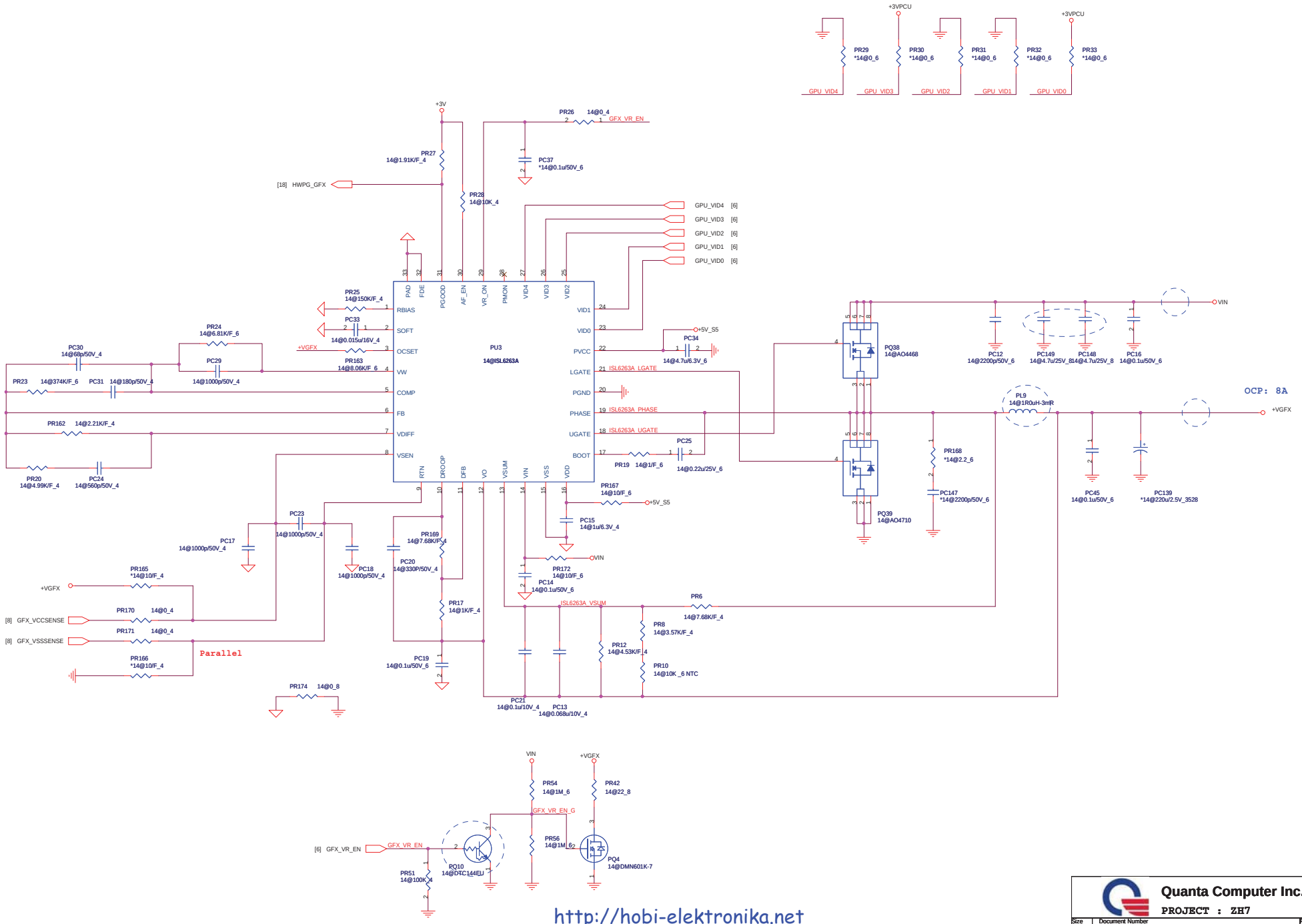
+3VPCU
PR29 *14@0_6
PR30 *14@0_6
PR31 *14@0_6
PR32 *14@0_6
PR33 *14@0_6
GPU_VID4
GPU_VID3
GPU_VID2
GPU_VID1
GPU_VID0
+3V
PR26 14@0_4
GFX_VR_EN
PR27 14@1.91K/F_4
PC37 *14@0.1u/50V_6
[18] HWPG_GFX
PR28 14@10K_4
GPU_VID4 [6]
GPU_VID3 [6]
GPU_VID2 [6]
GPU_VID1 [6]
GPU_VID0 [6]
PU3
14@ISL6263A
PAD
FDE
PGOOD
AF_EN
VR_ON
PMON
VID4
VID3
VID2
VID1
VID0
PVCC
LGATE
PGND
PHASE
UGATE
BOOT
RBIAS
SOFT
OCSET
VW
COMP
FB
VDIFF
VSEN
RTN
DROOP
DFB
VO
VSUM
VIN
VSS
VDD
PR25 14@150K/F_4
PC33 14@0.015u/16V_4
PR24 14@6.81K/F_6
PC30 14@68p/50V_4
PC29 14@1000p/50V_4
PR23 14@374K/F_6
PC31 14@180p/50V_4
PR162 14@2.21K/F_4
PR20 14@4.99K/F_4
PC24 14@560p/50V_4
+VGFX
PR163 14@8.06K/F_6
+5V_S5
PC34 14@4.7u/6.3V_6
ISL6263A_LGATE
ISL6263A_PHASE
ISL6263A_UGATE
PC25 14@0.22u/25V_6
PR19 14@1/F_6
PR167 14@10/F_6
PC15 14@1u/6.3V_4
PC23 14@1000p/50V_4
PC17 14@1000p/50V_4
PC18 14@1000p/50V_4
PR169 14@7.68K/F_4
PC20 14@330P/50V_4
PR17 14@1K/F_4
PR165 *14@10/F_4
PR170 14@0_4
PR171 14@0_4
PR166 *14@10/F_4
[8] GFX_VCCSENSE
[8] GFX_VSSSENSE
Parallel
PR172 14@10/F_6
VIN
PC14 14@0.1u/50V_6
ISL6263A_VSUM
PR6 14@7.68K/F_4
PR8 14@3.57K/F_4
PR12 14@4.53K/F_4
PR10 14@10K_6 NTC
PC19 14@0.1u/50V_6
PR174 14@0_8
PC21 14@0.1u/10V_4
PC13 14@0.068u/10V_4
PQ38 14@AO4468
PQ39 14@AO4710
PC12 14@2200p/50V_6
PC149 14@4.7u/25V_8
PC148 14@4.7u/25V_8
PC16 14@0.1u/50V_6
PL9 14@1R0uH-3mR
PR168 *14@2.2_6
PC147 *14@2200p/50V_6
PC45 14@0.1u/50V_6
PC139 *14@220u/2.5V_3528
OCP: 8A
PR54 14@1M_6
PR42 14@22_8
GFX_VR_EN_G
[6] GFX_VR_EN
PR56 14@1M_6
PQ10 14@DTC144EU
PQ4 14@DMN601K-7
PR51 14@100K
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Model	REV	CHANGE LIST
ZH7 MB	1A	FIRST RELEASED: (PCB:A)
	2B	Page 2 : No Stuff R162 FOR EMI Page11 : Remove R282 ,R36 & R39 Page11 : Change CN14 footprint. Page14 : Remove D7 Page17 : Change Q15 frome 2N7002 to DTC144EU for speaker funcation. Page17 :Stuff U15, R244 & R227 , No stuff L23 for audio noisy. Page18 : Add R324 Page18 : Add R323 Page19 : Add R325 and short to CN11.44 for 3G LED function Page19 : Remove 3G wake up funcation ,Remove R179 , R183 & U11 Page20 : CN9 Change pin define.(CONN. reverse) Page 9 ,13 ,17 ,22 ,23 &25 : R116 ,R269 ,R74 ,R92 ,C330 ,C349 ,R211 ,R220 ,R231 ,R243 ,R248 &R317 Change to short pad Page 18 : D5 ,D20 & D13 Change footprint. Page 29 : PL9 Change footprint. Page 3 : R142 Change footprint. Page 25 : PU10 Change footprint. Page 11 : CN14 Change footprint. Page 21 : CN4 Change footprint.
	3C	Page 17 ,20 ,21 & 22 : R186 ,R187 ,R188 ,R189 ,R241 ,R196 ,R315 ,R20 & R316 Change to short pad Page 18 : Add R321 for ESD(Vedor suggest) Page 18 : D21 connect to HWPG_GFX Page 18 : D29 replace by R323. Page 20 : DEL R6 ,R7 & L2 Page 21 : CN2 connect to 3G_MINI2_LED meet customer request. and add C430 for EMI Page 22 : CN3.21 Change to floating Page 25 : page25 Delete PC127;PC128 10uf/25V_1206 and add PC164 100uF/25V 6x5.7 Page 27 : Add PC163 100uF/25V 6x5.7 Page 28 : Add R323 and R327
	1D	

MODEL	ZH7 FROM	ZH7 To
	X	1A
	X	1A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2B	3A
	2B	3A
	2B	3A
	2B	3A
	2B	3A
	2B	3A
	2B	3A

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	PART NUMBER:		DRAWING BY:		REVISON:	1A

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EC GPIO Setting

Pin Name	Net Name	Setting	Description
GPIO1	ACIN	GPI	EC Detect AC Adapter State
GPIO3	NBSWON#	GPI	Pwer switch in
GPIO4/AD5		GPI	No used
GPIO5/AD4		GPI	No used
GPIO6	LID#	GPI	Reserved for Lid function
GPIO7	SUSB#	GPI	S.B sleep S3 pin
GPIO10/LPCPD#		GPI	No used
GPIO11/CLKRUN#	CLKRUN#	O	Clock Run
GPIO12/PSDAT3	KILL_SW_BT#	GPI	Detect bule tooth enable/disable
GPIO13/C_PWM	PWRLED#	O	Power on LED drive
GPIO14/TB1	FANSIG	GPI	To detect FAN speed
GPIO15/A_PWM	CONTRAST	O	EC PWM for Panel Brightness
GPIO16/CIRTX		GPI	No used
GPIO17/SCL1	MBCLK	O	SMBus Clock for M/B
GPIO20/TA2		GPI	No used
GPIO21/B_PWM	NUMLED#	O	Number Lock LED drive
GPIO22/SDA1	MBDATA	I/O	SMBus Data for M/B
GPIO23/SCL3	3ND_MBCLK	O	SMBus Clock for acer ID flash
GPIO24/LDRQ#	EC_FPBACK#	GPO	Panel back light control
GPIO25/PSCLK3	MAINON	GPO	Turn On/Off main power
GPIO26/PSCLK2		GPI	No used
GPIO27/PSDAT2	BT_POWERON#	GPO	Turn On/Off bule tooth power
GPIO30/CIRTX2		GPI	No used
GPIO31/SDA3	3ND_MBDATA	I/O	SMBus Data for acer ID flash
GPIO32/D_PWM	BATLED0#	GPO	Battery status LED drive
GPIO33/H_PWM	BATLED1#	GPO	Battery status LED drive
GPIO34/CIRRXL		GPI	No used
GPIO35/PSDAT1	TPDATA	O	PS/2 data for touch pad
GPIO36/TB3	VRON	GPO	Turn On/Off CPU Power
GPIO37/PSCLK1	TPCLK	O	PS/2 clock for touch pad
GPIO40/F_PWM	SUSLED	GPO	S3 state LED drive
GPIO41	3G_WAKE_2	GPI	3G wake up
GPIO42/TCK		GPI	No used
GPIO43/TMS	AMP_MUTE#	GPO	Turn On/Off Audio Amplier
GPIO44/TDI		GPI	No used
GPIO45/E_PWM	CPUFAN#	O	EC PWM for Fan Module
GPIO46/cirrxm/trst#	3G_WAKE_1	GPI	3G wake up
GPIO47/SCL4		GPI	No used
GPIO50/TDO	D/C#	GPO	Battery charge / discharge control
GPIO51/TA3	S5_ON	GPO	Turn On/Off S5 Power plane
GPIO52/cirtx2/trdy#	PCIE_WAKE#_EC	GPI	No used
GPIO53/SDA4	EC_SCI#	O	EC SCI
GPIO54/ECSCI#	ECDB_CLOCK	GPI	No used
GPIO55/CLKOUT	ECDB_CLOCK	GPI	No used
GPIO56/TA1		GPI	No used
GPIO57/KBSOUT17	KILL_SW_WL#	GPI	Detect mini card 1 (WLAN) enable/diable
GPIO60/KBSOUT16	KILL_SW_3G#	GPI	Detect mini card 2 (3G) enable/diable
GPIO61/KBSOUT15	MY15	O	Keyboard scan output
GPIO62/KBSOUT14	MY14	O	Keyboard scan output
GPIO63/KBSOUT13	MY13	O	Keyboard scan output
GPIO64/KBSOUT12	MY12	O	Keyboard scan output
GPIO65/SMI#	EC_SMI#	O	EC SMI
GPIO66/G_PWM	CAPSLED#	O	Caps Lock LED drive
GPIO67/PWUREQ	USB_EN#	GPO	USB power enable/disable
GPIO70/IRRX2_IRSL0	SUSC#	GPI	S.B sleep S4 pin
GPIO71/IRTX/SOUT2	PWROK_EC	GPO	System Power Good for PCI Reset
GPIO72/IRRX1/SIN2	EC_RSMRST#	GPO	S.B Resume Power Reset
GPIO73/SCL2	2ND_MBCLK	O	SMBus Clock for CPU thermal
GPIO74/SDA2	2ND_MBDATA	I/O	SMBus Data for CPU thermal
GPIO75/SPI_SCK	PCI_RESET	GPO	PLTRST# enable/diable for mini card 2
GPIO76/SPI_DO/SHBM	3G_EN	GPO	Mini card 2 (3G) enable/disable
GPIO77/SPI_DI	CRT_SENSE#	GPI	To detect CRT
GPIO81	DNBSWON#	GPO	S.B Power button Event
GPIO82/TRIS#		GPI	No used
GPIO83/SOUT_CR/BADDR1	uR_SOUT_CR	GPI	No used (Address Setting)
GPIO84/BADDR0	BADDR0	GPI	No used (Address Setting)
GPIO87/CIRRRXM/SIN_CR	RF_EN	GPO	Mini card 1 (WLAN) enable/disable
GPIO90/AD0	TEMP_MBAT	I	EC detect battery state
GPIO91/AD1		GPI	No used
GPIO92/AD2	TPD_TRIP	GPI	No used
GPIO93/AD3	ICMNT	I	EC detect system current in AC mode
GPIO94/DA0		GPI	No used
GPIO95/DA1		GPI	No used
GPIO96/DA2		GPI	No used
GPIO97/DA3		GPI	No used

ICH9M GPIO Setting

Pin Name	Power	ICH9M Default	Net Name	Description	Setting	Internal PU/PD	External PU/PD
GPIO0/PMSYNC#	Core	GPI	PM_SYNC#	Power Management Sync	O		
GPIO1	Core	GPI	EC_SMI#	EC SMI	GPI		PU 10KΩ to +3V
GPIO2/PIRQE#	Core	GPI	INTE#	No used	GPI		PU 10KΩ to +3V
GPIO3/PIRQF#	Core	GPI	INTF#	No used	GPI		PU 10KΩ to +3V
GPIO4/PIRQG#	Core	GPI	INTG#	No used	GPI		PU 10KΩ to +3V
GPIO5/PIRQH#	Core	GPI	INTH#	No used	GPI		PU 10KΩ to +3V
GPIO6	Core	GPI	LID#_ICH	Lid function	GPI		PU 10KΩ to +3V
GPIO7	Core	GPI		No used	GPI		PU 10KΩ to +3V
GPIO8	S5	GPI	EC_SCI#	EC SCI interrupt	GPI		PU 10KΩ to +3V_S5
GPIO9/WOL_EN	S5	Native	ICH_GPIO9	No used	GPI		PU 10KΩ to +3V_S5
GPIO10/SUS_PWR_ACK	S5	GPI	ICH_GPIO10	No used	GPI		PU 10KΩ to +3V_S5
GPIO11/SMBALERT#	S5	Native	ICH_GPIO11	No used	GPI		PU 10KΩ to +3V_S5
GPIO12/LAN_PHY_PWR_CTRL	S5	GPO	ICH_GPIO12	No used	GPI		PU 10KΩ to +3V_S5
GPIO13	S5	GPI	ICH_GPIO13	No used	GPI		PU 10KΩ to +3V_S5
GPIO14/AC_PRESENT	S5	GPI	ICH_GPIO14	No used	GPI		PU 10KΩ to +3V_S5
GPIO15/STP_PCI#	S5	Native	PM_STPPCI#	Stop PCI Clock	O		
GPIO16/DPRSLPVR	Core	Native	DPRSLPVR	Deeper Sleep-Voltage Regulator	O	PD 20KΩ	
GPIO17	Core	GPI	BORAD_ID0	M/B ID Setting	GPI		PU or PD 10KΩ
GPIO18	Core	GPO	BORAD_ID1	M/B ID Setting	GPI		PU or PD 10KΩ
GPIO19/SATA1GP	Core	GPI	ICH_GPIO19	No used	GPI		PU 10KΩ to +3V
GPIO20	Core	GPO		No used	GPO	PD 20KΩ	
GPIO21/SATA0GP	Core	GPI	BORAD_ID2	M/B ID Setting	GPI		PU or PD 10KΩ
GPIO22/SCLOCK	Core	GPI	BORAD_ID3	M/B ID Setting	GPI		PU or PD 10KΩ
GPIO23/LDRQ1#	Core	Native		No used	GPI	PU 20KΩ	
GPIO24/MEM/LED	S5	GPO		No used	GPO		
GPIO25/STP_CPU#	S5	Native	PM_STPCPU#	Stop CPU Clock	O		
GPIO26/S4_STATE#	S5	Native		No used	GPO		
GPIO27	S5	GPO		No used	GPO		
GPIO28	S5	GPO		No used	GPO		
GPIO29/OC5#	S5	Native	USBOC5#	No used	GPI		PU 10KΩ to +3V_S5
GPIO30/OC6#	S5	Native	USBOC6#	No used	GPI		PU 10KΩ to +3V_S5
GPIO31/OC7#	S5	Native	USBOC7#	No used	GPI		PU 10KΩ to +3V_S5
GPIO32/CLKRUN#	Core	GPO	CLKRUN#	PCI Clock Run	I		PU 8.2KΩ to +3V
GPIO33/HDA_DOCK_EN#	Core	GPO		No used	GPO	PU 20KΩ	
GPIO34/HDA_DOCK_RST#	Core	GPO		No used	GPO		
GPIO35/SATACLKREQ#	Core	GPO	CLKREQ#_SATA	SATA Clock Request	O		PU 10KΩ to +3V
GPIO36/SATA4GP	Core	GPI	ICH_GPIO36	No used	GPI		PU 10KΩ to +3V
GPIO37/SATA5GP	Core	GPI	ICH_GPIO37	No used	GPI		PU 10KΩ to +3V
GPIO38/SLOAD	Core	GPI	ICH_GPIO38	No used	GPI		PD 10KΩ to GND
GPIO39/SDATAOUT0	Core	GPI		No used	GPI		PU 10KΩ to +3V
GPIO40/OC1#	S5	Native	USBOC1#	No used	GPI		PU 10KΩ to +3V_S5
GPIO41/OC2#	S5	Native	USBOC2#	No used	GPI		PU 10KΩ to +3V_S5
GPIO42/OC3#	S5	Native	USBOC3#	No used	GPI		PU 10KΩ to +3V_S5
GPIO43/OC4#	S5	Native	USBOC4#	No used	GPI		PU 10KΩ to +3V_S5
GPIO44/OC8#	S5	Native	USBOC8#	No used	GPI		PU 10KΩ to +3V_S5
GPIO45/OC9#	S5	Native	USBOC9#	No used	GPI		PU 10KΩ to +3V_S5
GPIO46/OC10#	S5	Native	USBOC10#	No used	GPI		PU 10KΩ to +3V_S5
GPIO47/OC11#	S5	Native	USBOC11#	No used	GPI		PU 10KΩ to +3V_S5
GPIO48/SDATAOUT1	Core	GPI		No used	GPI		PU 10KΩ to +3V
GPIO49	Core	GPO	DMI_TERM_SEL	No used	GPO	PU 20KΩ	
GPIO50/REQ1#	Core	Native	REQ1#	No used	GPI		PU 10KΩ to +3V
GPIO51/GNT1#	Core	Native		No used	GPI	PU 20KΩ	
GPIO52/REQ2#	Core	Native	REQ2#	No used	GPI		PU 10KΩ to +3V
GPIO53/GNT2#	Core	Native		No used	GPI	PU 20KΩ	
GPIO54/REQ3#	Core	Native	REQ3#	No used	GPI		PU 10KΩ to +3V
GPIO55/GNT3#	Core	Native		No used	GPI	PU 20KΩ	
GPIO56	S5	GPI	ICH_GPIO56	No used	GPI		PU 10KΩ to +3V_S5
GPIO57	S5	GPI	ICH_GPIO57	No used	GPI		PD 100KΩ to GND
GPIO58/SPI_CS1#	S5	GPI	SPI_CS1#	No used	GPI	PU 20KΩ	
GPIO59/OC0#	S5	Native	USBOC0#	No used	GPI		PU 10KΩ to +3V_S5
GPIO60/LINKALERT#	S5	Native	ICH_GPIO60	No used	GPI		PU 10KΩ to +3V_S5

CK505 Clock Setting Table

Differential CPU Clock

Pin Name	Pin	Net Name	Description
CPU_0	61	CLK_CPU_BCLK	
CPU_0#	60	CLK_CPU_BCLK#	Differential CPU clock
CPU_1	58	CLK_MCH_BCLK	
CPU_1#	57	CLK_MCH_BCLK#	Differential NB GS45 clock

PCI Express Clock

Pin Name	Pin	Net Name	Description
SRC0/DOT96	20	DREFCLK	
SRC0#/DOT96#	21	DREFCLK#	96MHz DOT clock for NB GS45
LCDCLK/27M	24	DREFSSCLK	
LCDCLK#/27M_SS	25	DREFSSCLK#	Clock output for NB GS45 graphic contoller
SRC2	28	PECLK_SATA	
SRC2#	29	PECLK_SATA#	Differential Serial Reference Clock for SB ICH9M SATA
SRC3/CR#_C	31	PECLK_ICH	
SRC3#/CR#_D	32	PECLK_ICH#	Differential Serial Reference Clock for SB ICH9M
SRC4	34	PECLK_LAN	
SRC4#	35	PECLK_LAN#	Differential Serial Reference Clock for on board LAN
SRC6	48	PECLK_MINI2	
SRC6#	47	PECLK_MINI2#	Differential Serial Reference Clock for Mini Card 2
SRC7/CR#_F	51		No use
SRC7#/CR#_E	50	CLKREQ#_MINI2	Clock Request for Mini Card 2 (SRC6)
SRC8/CPU_ITP	54		
SRC8#/CPU_ITP#	53		No use
SRC9	37	PECLK_MINI1	
SRC9#	38	PECLK_MINI1#	Differential Serial Reference Clock for MINI CARD 1
SRC10	41	PECLK_3GPLL	
SRC10#	42	PECLK_3GPLL#	Differential Serial Reference Clock for NB GS45
SRC11/CR#_H	40	CLKREQ#_MCH	Clock Request for NB GS45 (SRC10)
SRC11#/CR#_G	39	CLKREQ#_MINI1	Clock Request for Mini Card 1 (SRC9)

PCI Clock

Pin Name	Pin	Net Name	Description
PCI0/CR#_A	8	CLKREQ#_SATA	Clock Request for SATA (SRC2)
PCI1/CR#_B	10	CLKREQ#_LAN	Clock Request for on board LAN (SRC4)
PCI2	11	PCLK_DEBUG	PCI clock for debug card
PCI3	12		No use
PCI4	13	PCLK_EC	PCI clock for EC
PCI5	14	PCLK_ICH	PCI clock for SB ICH9M

Other Clock

Pin Name	Pin	Net Name	Description
USB_48	17	CLK48_ICH	48MHz for SB ICH9M
		CLK48_CARD	48MHz for USB Card Reader
REF	5	CLK14_ICH	14.318MHz for SB ICH9M

Clock Request Table

CLKREQ#	MAPPING		Control
	0	1	
CR#_A	SRC0	SRC2	SATA
CR#_B	LCDCLK	SRC4	LAN
CR#_C	SRC0	SRC2	N/A
CR#_D	LCDCLK	SRC4	N/A
CR#_E	SRC6		MINI2
CR#_F	SRC8		N/A
CR#_G	SRC9		MINI1
CR#_H	SRC10		MCH

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QUANTA COMPUTER

Title: Schematic Setting

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