

PWWAA

Delhi

LA-6847P REV 1.0 Schematic

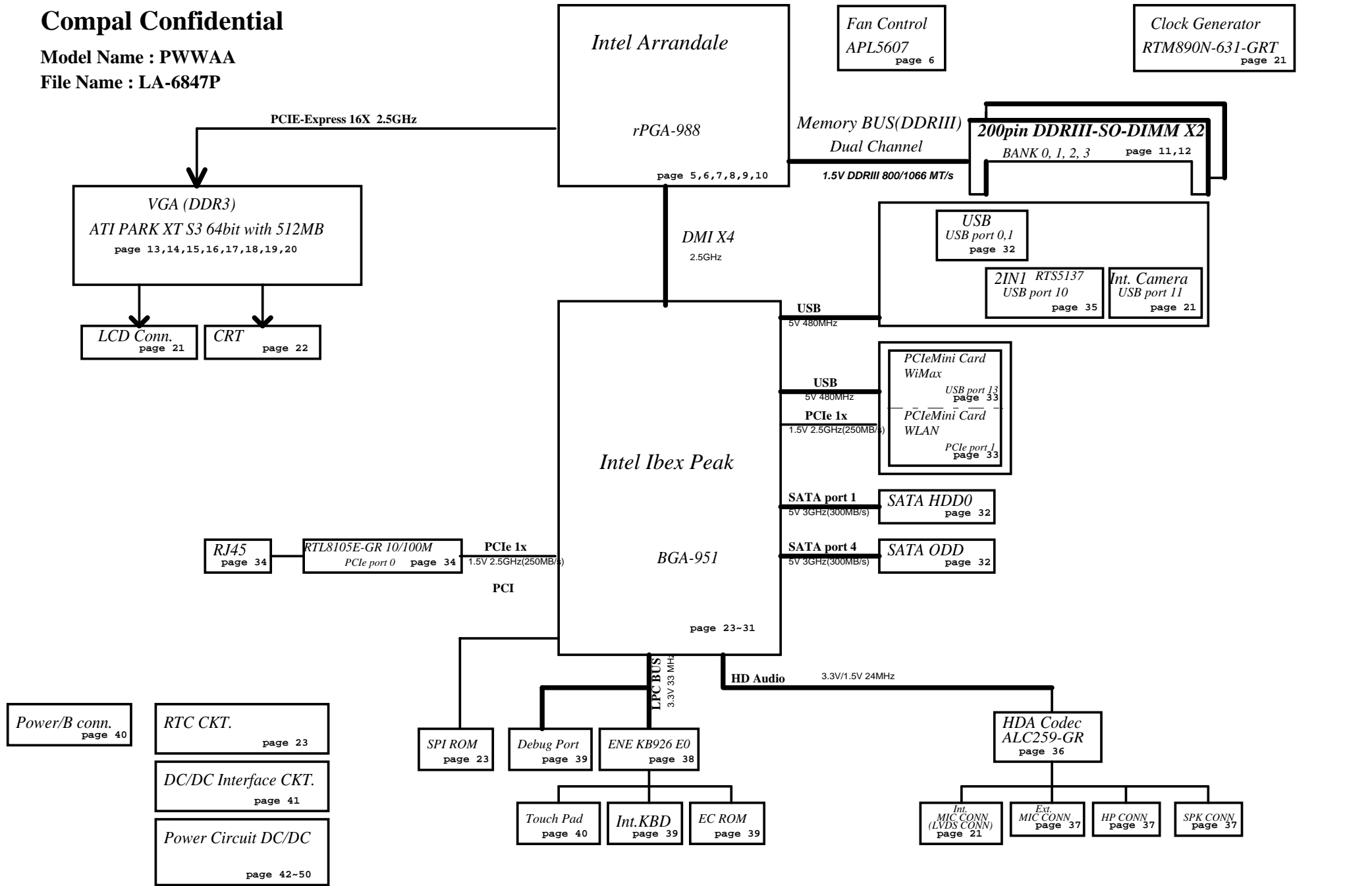
Intel Processor(ARD) /PCH(HM55)
2010-10-07 Rev 1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2010/09/05	Deciphered Date	2011/09/05	Title	SCHEMATICS,MB A6847	
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				B	4019AP	B
Date:	Tuesday, December 28, 2010			Sheet	1	of 52

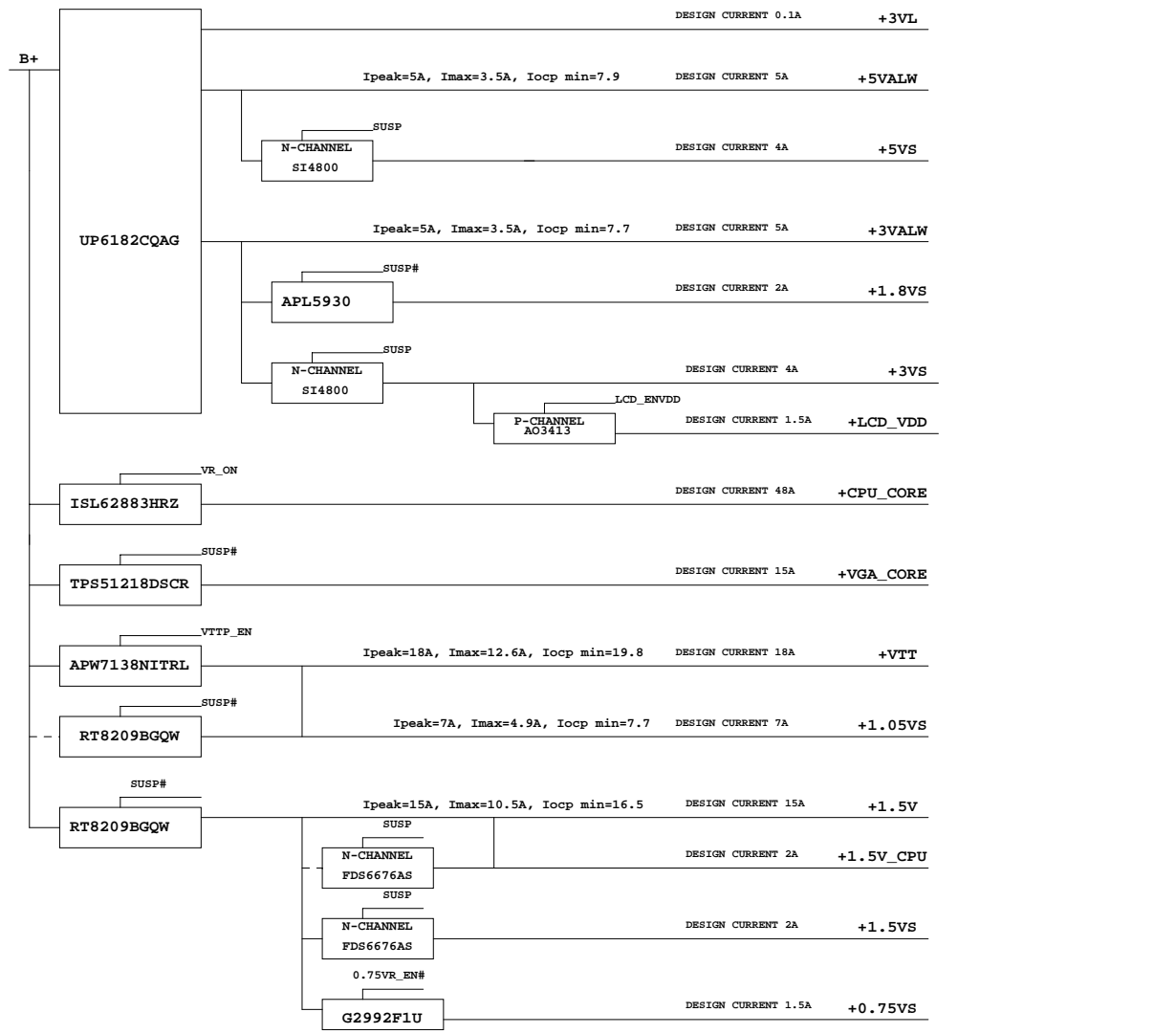
Compal Confidential

Model Name : PWVAA

File Name : LA-6847P



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Document Number			4019AP	Rev B
Date: Tuesday, December 28, 2010				Sheet 2 of 52



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				Date	Tuesday, December 28, 2010
				Sheet	3 of 52

Voltage Rails (O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	+B	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.5VS +VGA_CORE +CPU_CORE +VTT +1.05VS +1.8VS +1.1VS +0.75VS
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

BTO Option Table

Function	MINI PCI-E SLOT	LAN				
description		SLOT1	LAN			
explain		WLAN/BT	10/100M			
BTO						

Function			Camera & Mic			
description			Camera & Mic			
explain			Camera & Mic			
BTO			CAM@			

Function	S3 Power Saving	
description	S3 Power Saving	
explain	Power Saving	
BTO		

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		

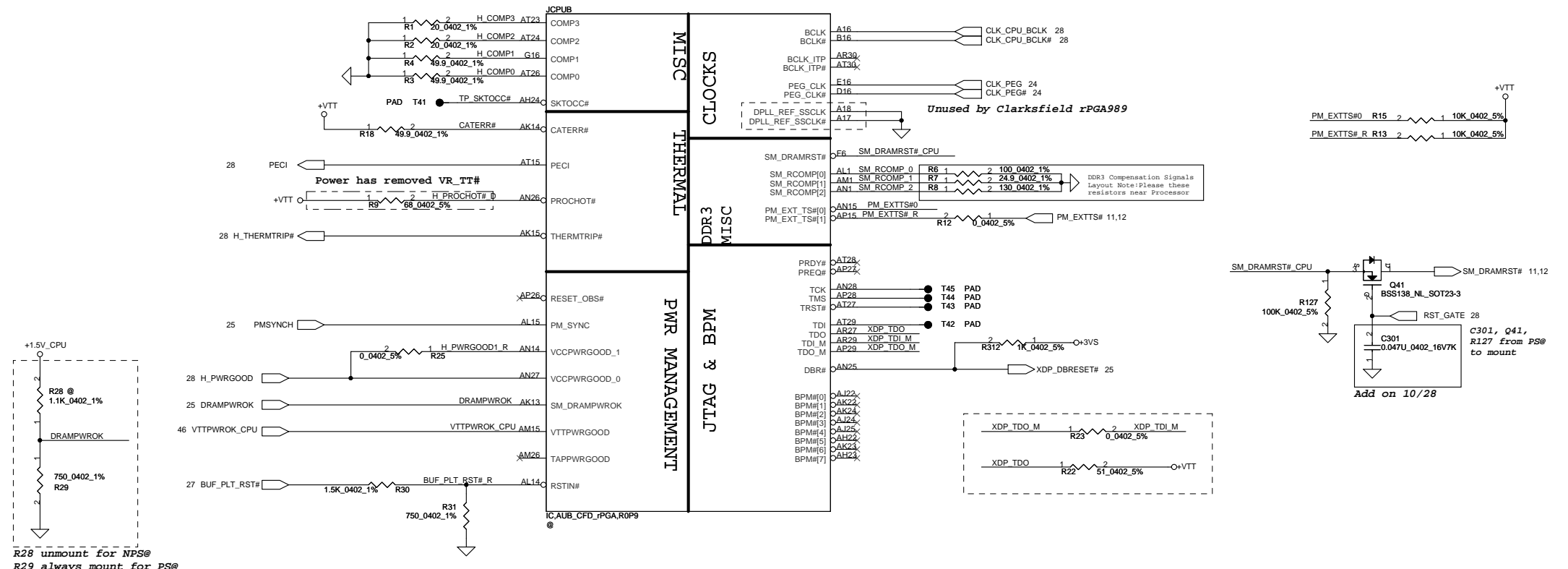
EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b

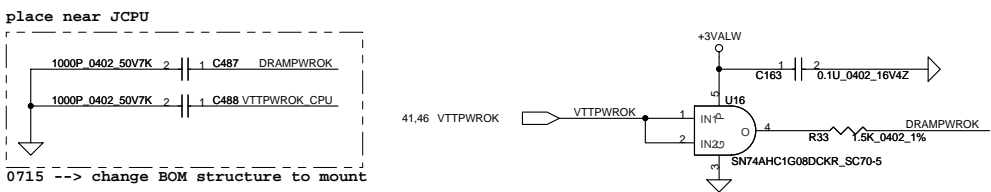
EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b

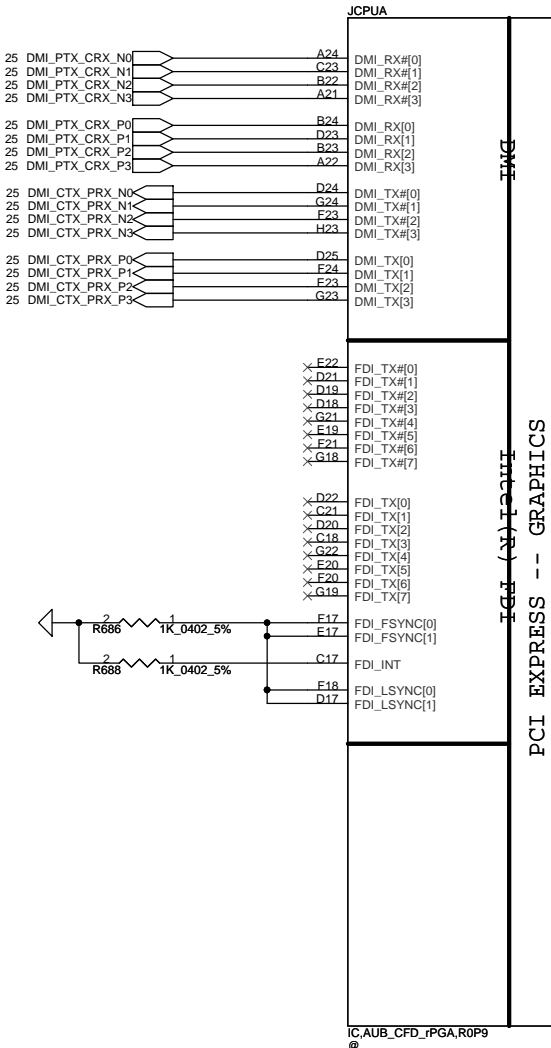
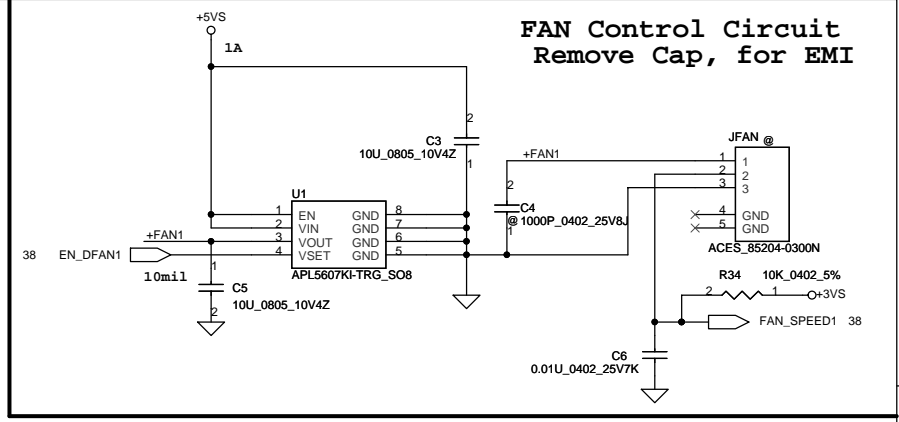
STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW



For S3 CPU Power Saving

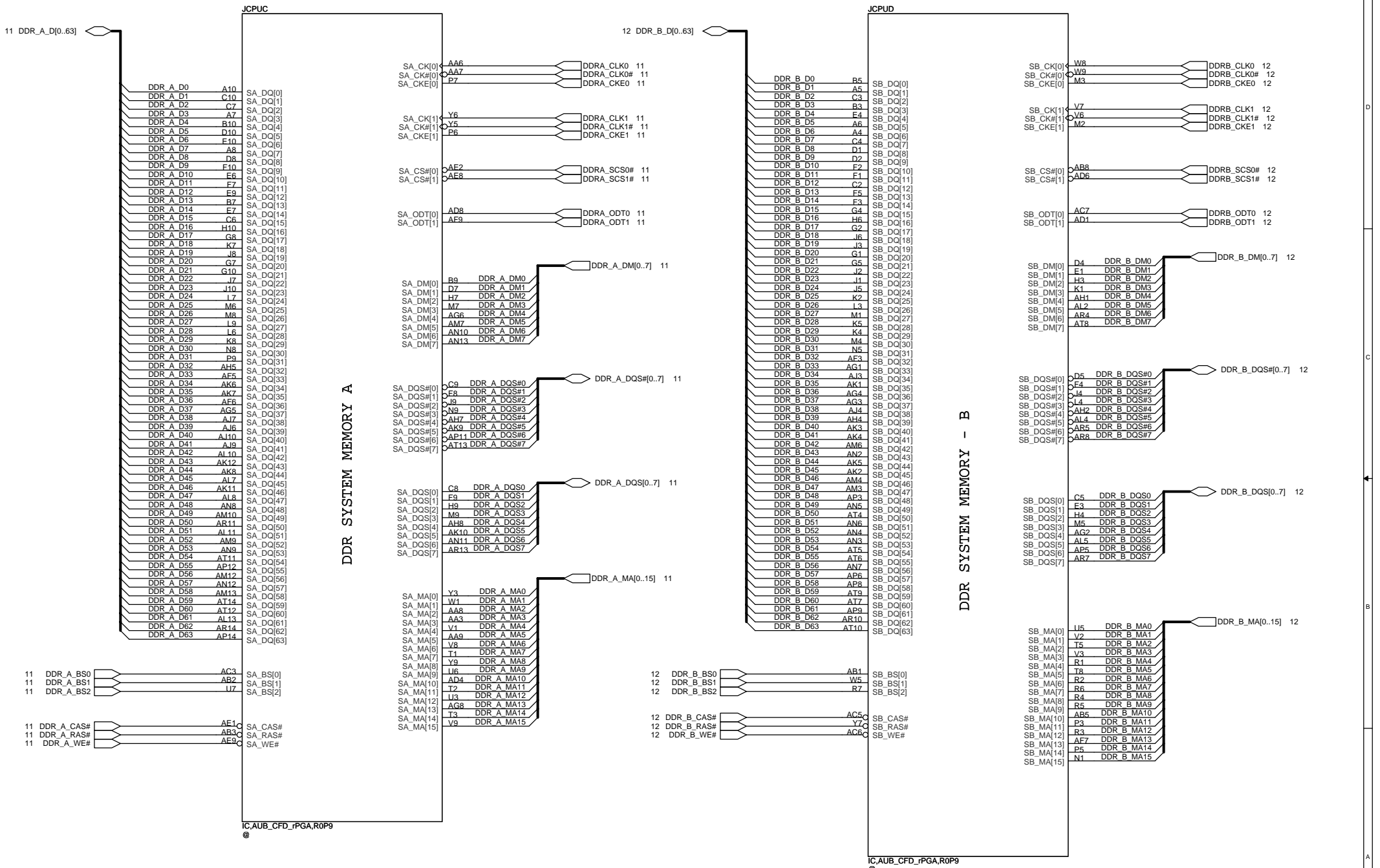


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Size	Custom	Document Number	4019AP	Rev	B
Date:	Tuesday, December 28, 2010	Sheet	5	of	52

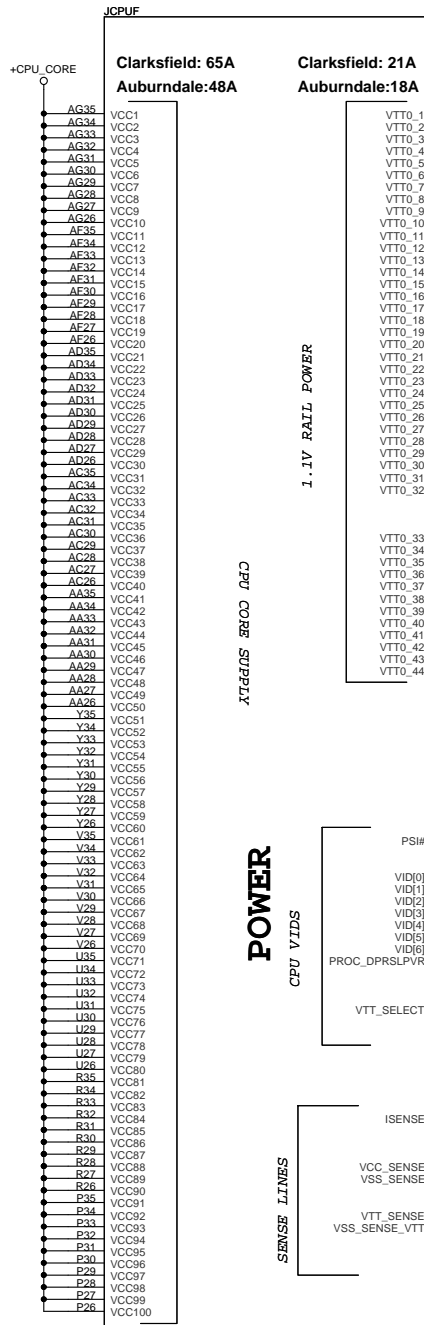


PEG_ICOMPI	B26	PEG_COMP	R38	1	2	49.9_0402_1%			
PEG_ICOMPO	A26								
PEG_RCOMPO	B27								
PEG_RBIBAS	A25	PEG_RBIBAS	R39	1	2	750_0402_1%			
PEG_RX#[0]	K35	PCIE GTX C CRX N0							
PEG_RX#[1]	J34	PCIE GTX C CRX N1							
PEG_RX#[2]	G34	PCIE GTX C CRX N2							
PEG_RX#[3]	G32	PCIE GTX C CRX N3							
PEG_RX#[4]	F34	PCIE GTX C CRX N4							
PEG_RX#[5]	F31	PCIE GTX C CRX N5							
PEG_RX#[6]	D35	PCIE GTX C CRX N6							
PEG_RX#[7]	E33	PCIE GTX C CRX N7							
PEG_RX#[8]	C33	PCIE GTX C CRX N8							
PEG_RX#[9]	D32	PCIE GTX C CRX N9							
PEG_RX#[10]	B32	PCIE GTX C CRX N10							
PEG_RX#[11]	C31	PCIE GTX C CRX N11							
PEG_RX#[12]	B28	PCIE GTX C CRX N12							
PEG_RX#[13]	B30	PCIE GTX C CRX N13							
PEG_RX#[14]	A31	PCIE GTX C CRX N14							
PEG_RX#[15]	A31	PCIE GTX C CRX N15							
PEG_RX[0]	H35	PCIE GTX C CRX P0							
PEG_RX[1]	H34	PCIE GTX C CRX P1							
PEG_RX[2]	H33	PCIE GTX C CRX P2							
PEG_RX[3]	F35	PCIE GTX C CRX P3							
PEG_RX[4]	G34	PCIE GTX C CRX P4							
PEG_RX[5]	E32	PCIE GTX C CRX P5							
PEG_RX[6]	D34	PCIE GTX C CRX P6							
PEG_RX[7]	F33	PCIE GTX C CRX P7							
PEG_RX[8]	B33	PCIE GTX C CRX P8							
PEG_RX[9]	B33	PCIE GTX C CRX P9							
PEG_RX[10]	D31	PCIE GTX C CRX P10							
PEG_RX[11]	A32	PCIE GTX C CRX P11							
PEG_RX[12]	C30	PCIE GTX C CRX P12							
PEG_RX[13]	A28	PCIE GTX C CRX P13							
PEG_RX[14]	B29	PCIE GTX C CRX P14							
PEG_RX[15]	A30	PCIE GTX C CRX P15							
PEG_TX#[0]	L33	PCIE CTX GRX N0	C39	1	2	0.1U 0402 16V7K	PCIE CTX C GRX N0		
PEG_TX#[1]	M35	PCIE CTX GRX N1	C40	1	2	0.1U 0402 16V7K	PCIE CTX C GRX N1		
PEG_TX#[2]	M33	PCIE CTX GRX N2	C41	1	2	0.1U 0402 16V7K	PCIE CTX C GRX N2		
PEG_TX#[3]	M30	PCIE CTX GRX N3	C42	1	2	0.1U 0402 16V7K	PCIE CTX C GRX N3		
PEG_TX#[4]	L31	PCIE CTX GRX N4	C43	1	2	0.1U 0402 16V7K	PCIE CTX C GRX N4		
PEG_TX#[5]	K32	PCIE CTX GRX N5	C44	1	2	0.1U 0402 16V7K	PCIE CTX C GRX N5		
PEG_TX#[6]	M29	PCIE CTX GRX N6	C45	1	2	0.1U 0402 16V7K	PCIE CTX C GRX N6		
PEG_TX#[7]	J31	PCIE CTX GRX N7	C46	1	2	0.1U 0402 16V7K	PCIE CTX C GRX N7		
PEG_TX#[8]	K29	PCIE CTX GRX N8	C47	1	2	0.1U 0402 16V7K	PCIE CTX C GRX N8		
PEG_TX#[9]	H30	PCIE CTX GRX N9	C48	1	2	0.1U 0402 16V7K	PCIE CTX C GRX N9		
PEG_TX#[10]	H29	PCIE CTX GRX N10	C49	1	2	0.1U 0402 16V7K	PCIE CTX C GRX N10		
PEG_TX#[11]	F29	PCIE CTX GRX N11	C50	1	2	0.1U 0402 16V7K	PCIE CTX C GRX N11		
PEG_TX#[12]	E28	PCIE CTX GRX N12	C51	1	2	0.1U 0402 16V7K	PCIE CTX C GRX N12		
PEG_TX#[13]	D29	PCIE CTX GRX N13	C52	1	2	0.1U 0402 16V7K	PCIE CTX C GRX N13		
PEG_TX#[14]	D27	PCIE CTX GRX N14	C53	1	2	0.1U 0402 16V7K	PCIE CTX C GRX N14		
PEG_TX#[15]	C26	PCIE CTX GRX N15	C54	1	2	0.1U 0402 16V7K	PCIE CTX C GRX N15		
PEG_TX[0]	L34	PCIE CTX GRX P0	C55	1	2	0.1U 0402 16V7K	PCIE CTX C GRX P0		
PEG_TX[1]	M34	PCIE CTX GRX P1	C56	1	2	0.1U 0402 16V7K	PCIE CTX C GRX P1		
PEG_TX[2]	M32	PCIE CTX GRX P2	C57	1	2	0.1U 0402 16V7K	PCIE CTX C GRX P2		
PEG_TX[3]	L30	PCIE CTX GRX P3	C58	1	2	0.1U 0402 16V7K	PCIE CTX C GRX P3		
PEG_TX[4]	M31	PCIE CTX GRX P4	C59	1	2	0.1U 0402 16V7K	PCIE CTX C GRX P4		
PEG_TX[5]	K31	PCIE CTX GRX P5	C60	1	2	0.1U 0402 16V7K	PCIE CTX C GRX P5		
PEG_TX[6]	M28	PCIE CTX GRX P6	C61	1	2	0.1U 0402 16V7K	PCIE CTX C GRX P6		
PEG_TX[7]	H31	PCIE CTX GRX P7	C62	1	2	0.1U 0402 16V7K	PCIE CTX C GRX P7		
PEG_TX[8]	K28	PCIE CTX GRX P8	C63	1	2	0.1U 0402 16V7K	PCIE CTX C GRX P8		
PEG_TX[9]	G29	PCIE CTX GRX P9	C64	1	2	0.1U 0402 16V7K	PCIE CTX C GRX P9		
PEG_TX[10]	G29	PCIE CTX GRX P10	C65	1	2	0.1U 0402 16V7K	PCIE CTX C GRX P10		
PEG_TX[11]	F28	PCIE CTX GRX P11	C66	1	2	0.1U 0402 16V7K	PCIE CTX C GRX P11		
PEG_TX[12]	E27	PCIE CTX GRX P12	C67	1	2	0.1U 0402 16V7K	PCIE CTX C GRX P12		
PEG_TX[13]	D28	PCIE CTX GRX P13	C68	1	2	0.1U 0402 16V7K	PCIE CTX C GRX P13		
PEG_TX[14]	C27	PCIE CTX GRX P14	C69	1	2	0.1U 0402 16V7K	PCIE CTX C GRX P14		
PEG_TX[15]	C25	PCIE CTX GRX P15	C70	1	2	0.1U 0402 16V7K	PCIE CTX C GRX P15		

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				4019AP	
Date:	Tuesday, December 28, 2010	Sheet	6	of	52

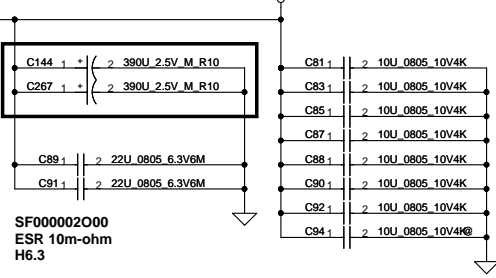


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				B	4019AP
				Date:	Tuesday, December 28, 2010
				Sheet	7 of 52



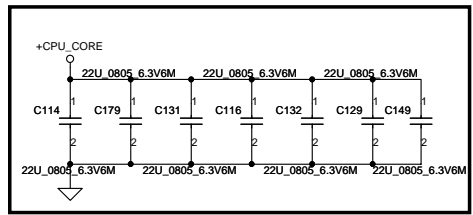
Material Note (+VTT):
390uF/ 10mohm, number are 3,
power x1, HW x2

(Place these capacitors under CPU socket Edge, top layer)



SF000002O00
ESR 10m-ohm
H6.3

Power team request for F-Din



CRB default setting:
VID[6:0]=[0100111]

VTT Rail
Auburndale +1.1VS_VTT=1.05V
Clarksfield +1.1VS_VTT=1.1V

1.1V RAIL POWER

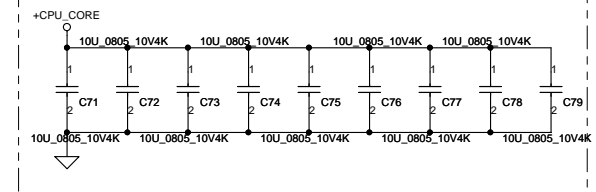
CPU CORE SUPPLY

POWER

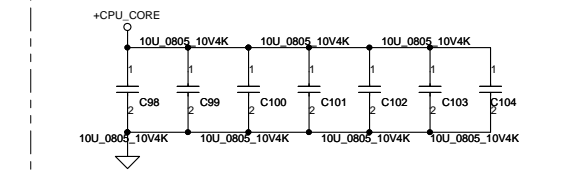
CPU VIDS

SENSE LINES

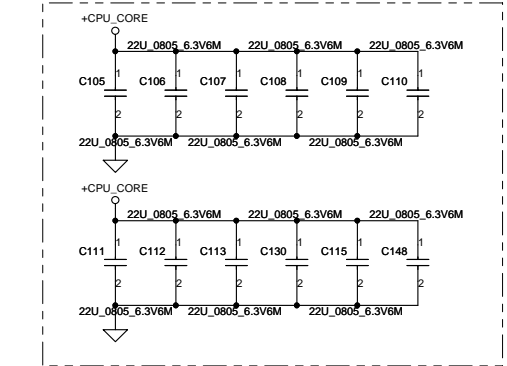
(Place these capacitors between inductor and socket on Bottom)



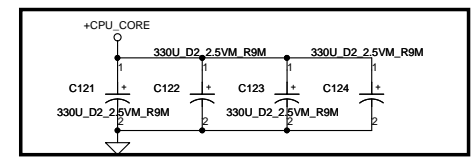
(Place these capacitors under CPU socket, top layer)



(Place these capacitors on CPU cavity, Bottom Layer)



TOP side (under inductor)

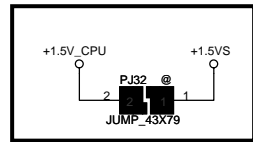


Check list:

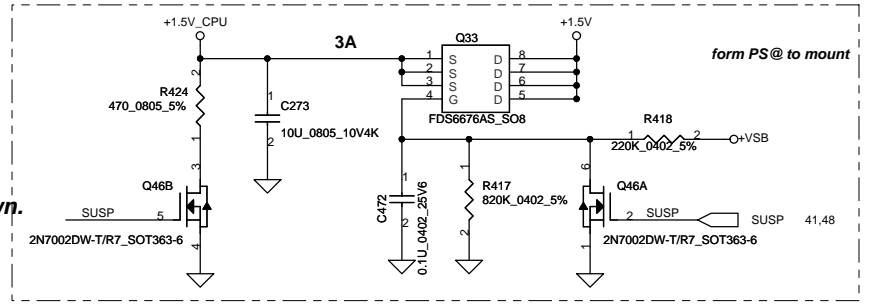
- +CPU_CORE: 6x 470uF, 12x 22uF, 17x 10uF
- +VTT: 4x 330uF, 7x 22uF, 8x 10uF

IC_AUB_CFD_rPGA_R0P9

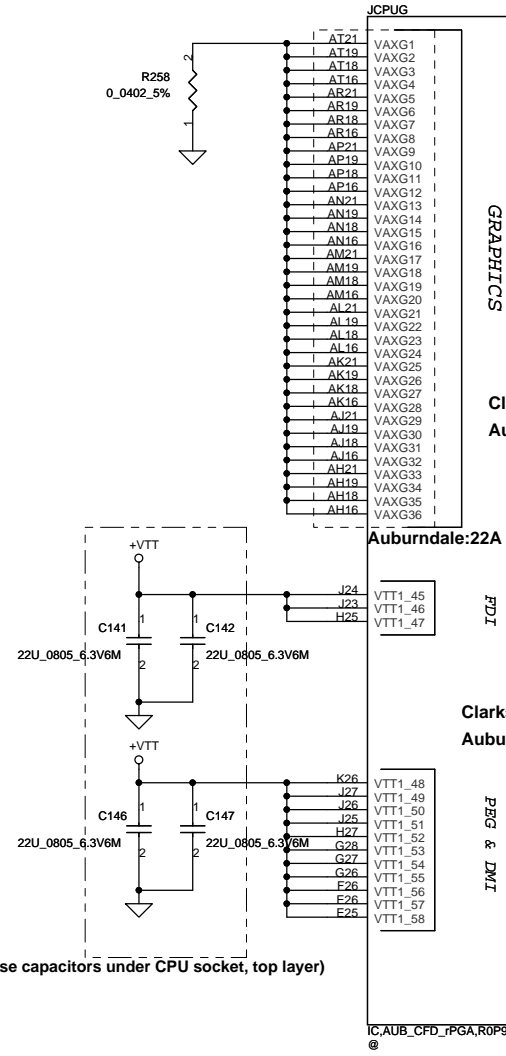
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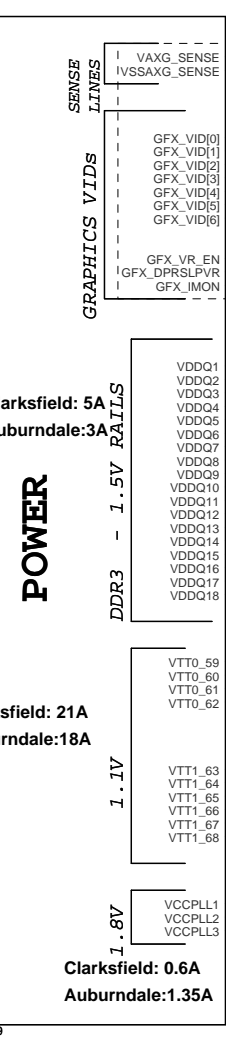
7/22 modified for cost down.



form PS@ to mount

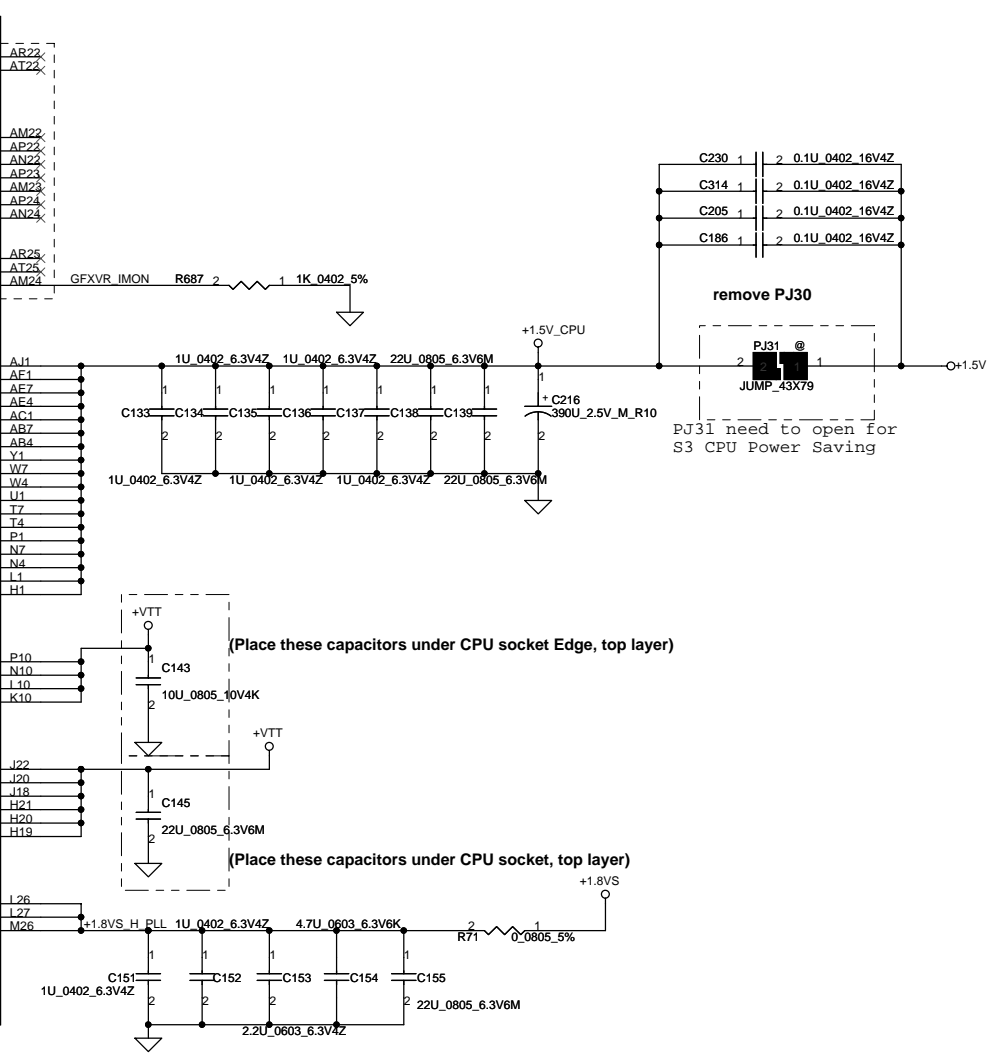


(Place these capacitors under CPU socket, top layer)



POWER

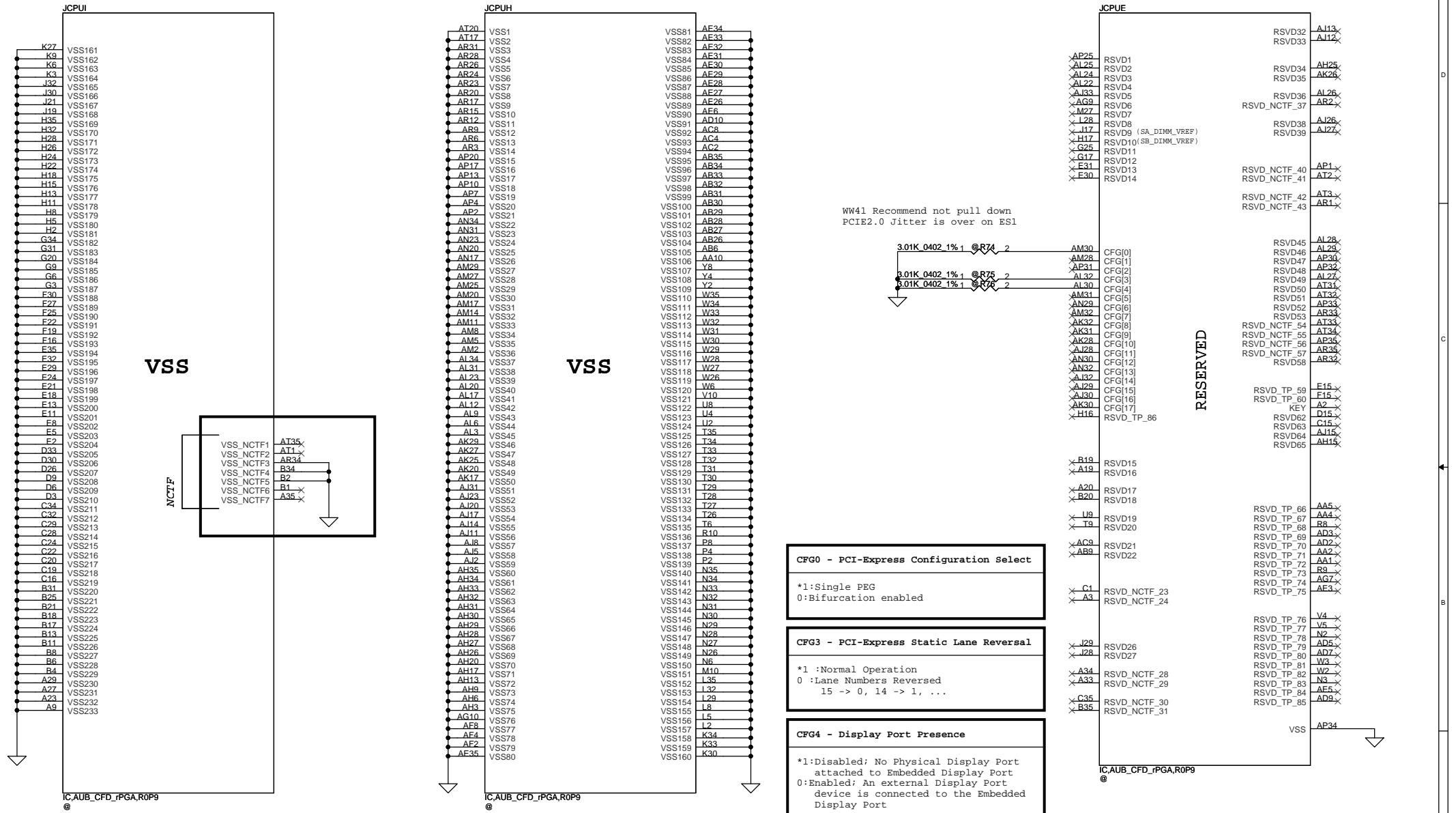
Clarksfield: 0.6A
Auburndale: 1.35A



(Place these capacitors under CPU socket Edge, top layer)

(Place these capacitors under CPU socket, top layer)

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				4019AP	
Date: Tuesday, December 28, 2010				Sheet	9 of 52



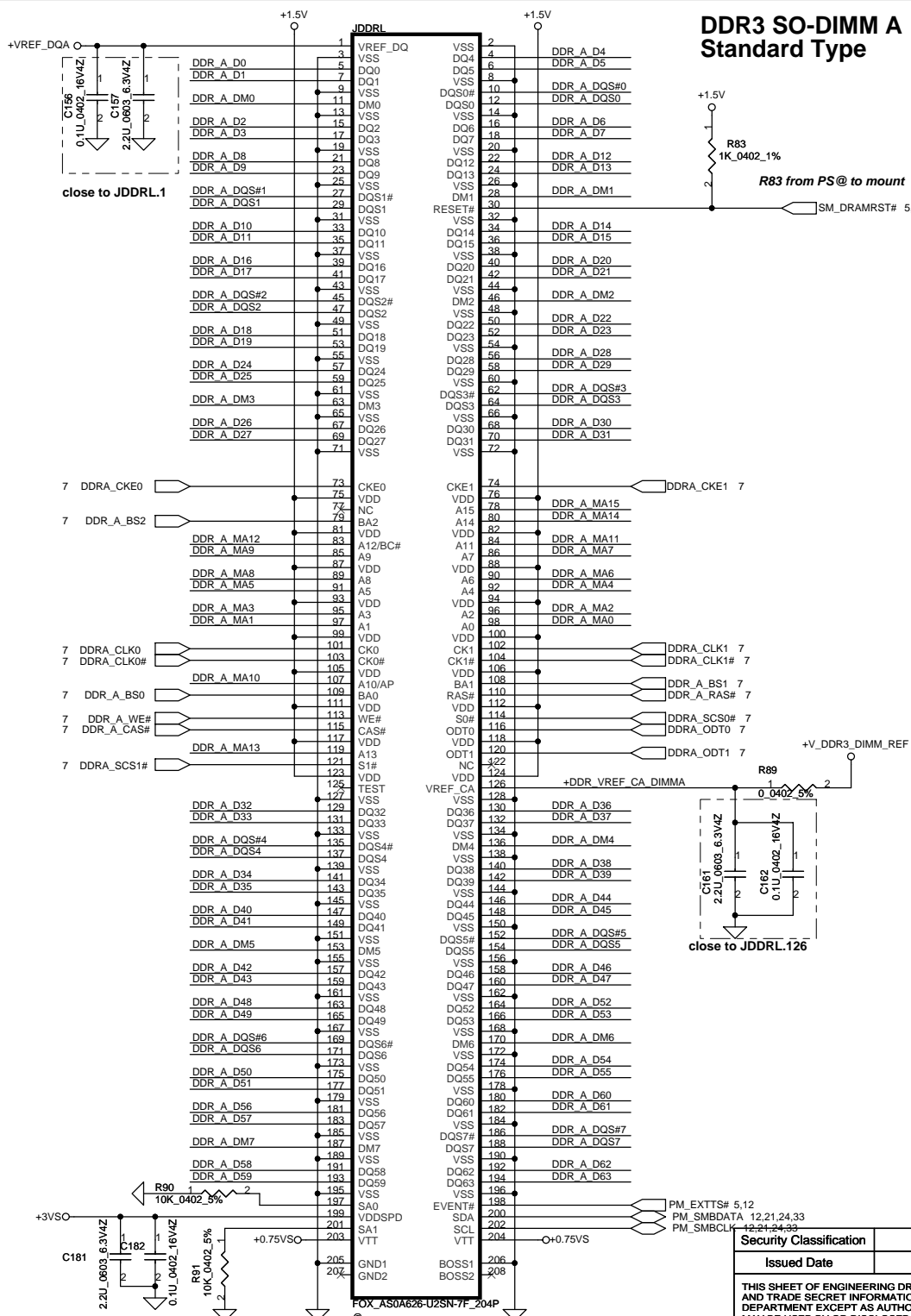
CFG0 - PCI-Express Configuration Select
 *1:Single PEG
 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal
 *1 :Normal Operation
 0 :Lane Numbers Reversed
 15 -> 0, 14 -> 1, ...

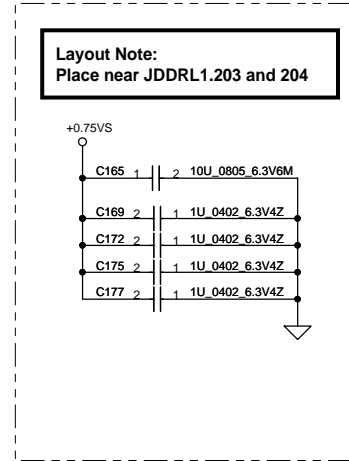
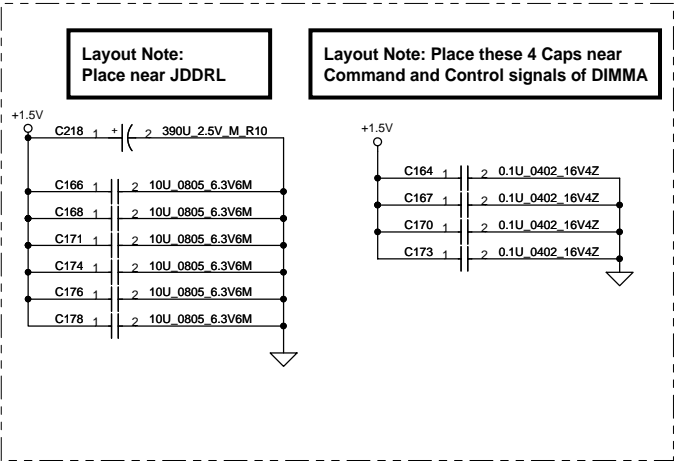
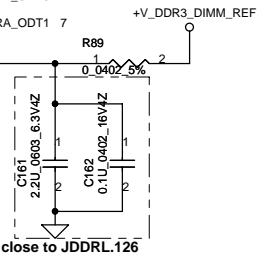
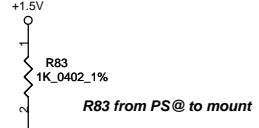
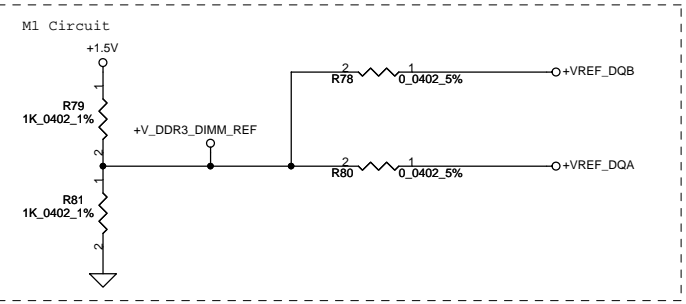
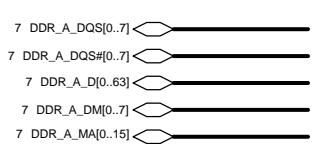
CFG4 - Display Port Presence
 *1:Disabled; No Physical Display Port attached to Embedded Display Port
 0:Enabled; An external Display Port device is connected to the Embedded Display Port

**Default

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Date: Tuesday, December 28, 2010				Sheet	10 of 52



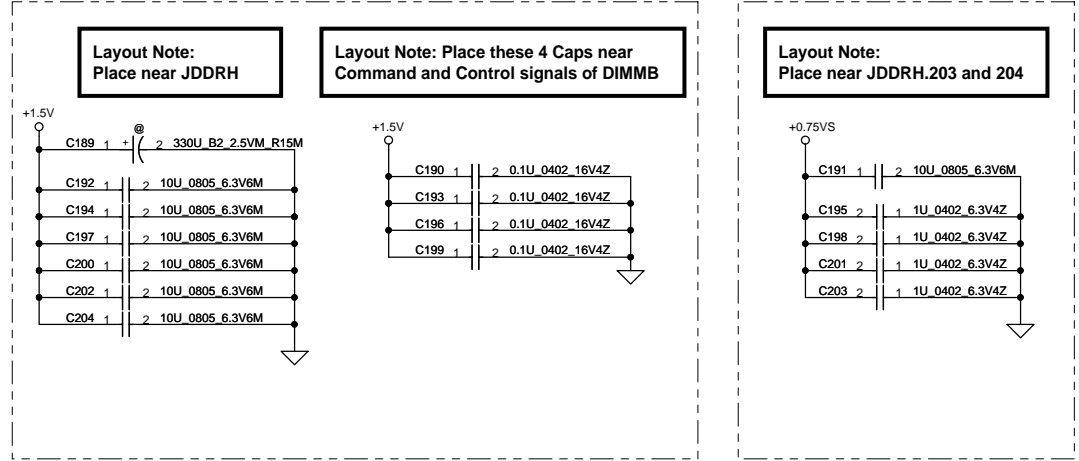
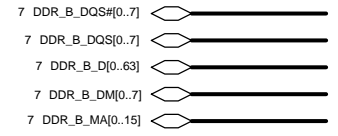
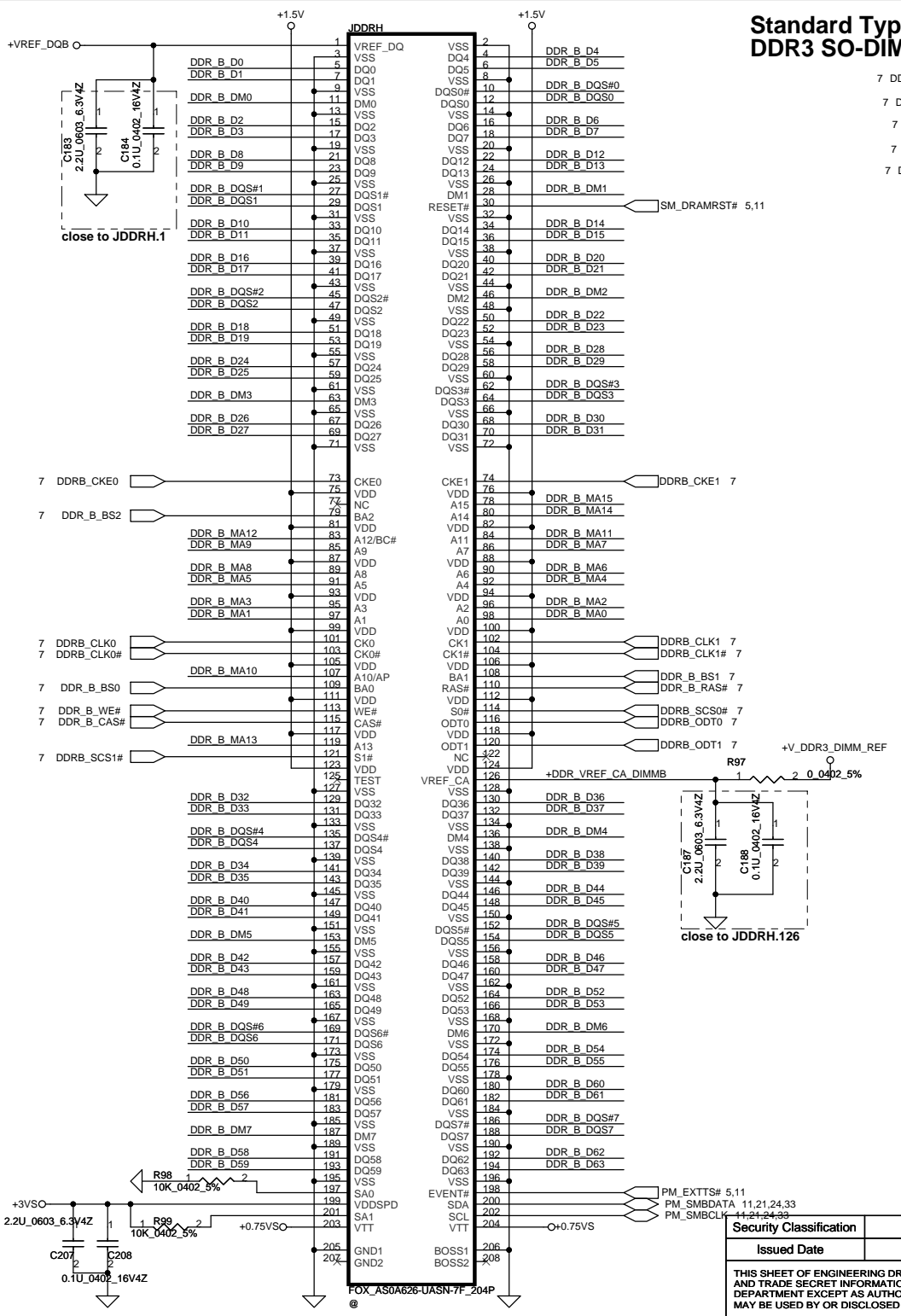
DDR3 SO-DIMM A Standard Type



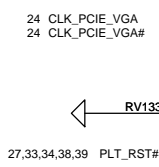
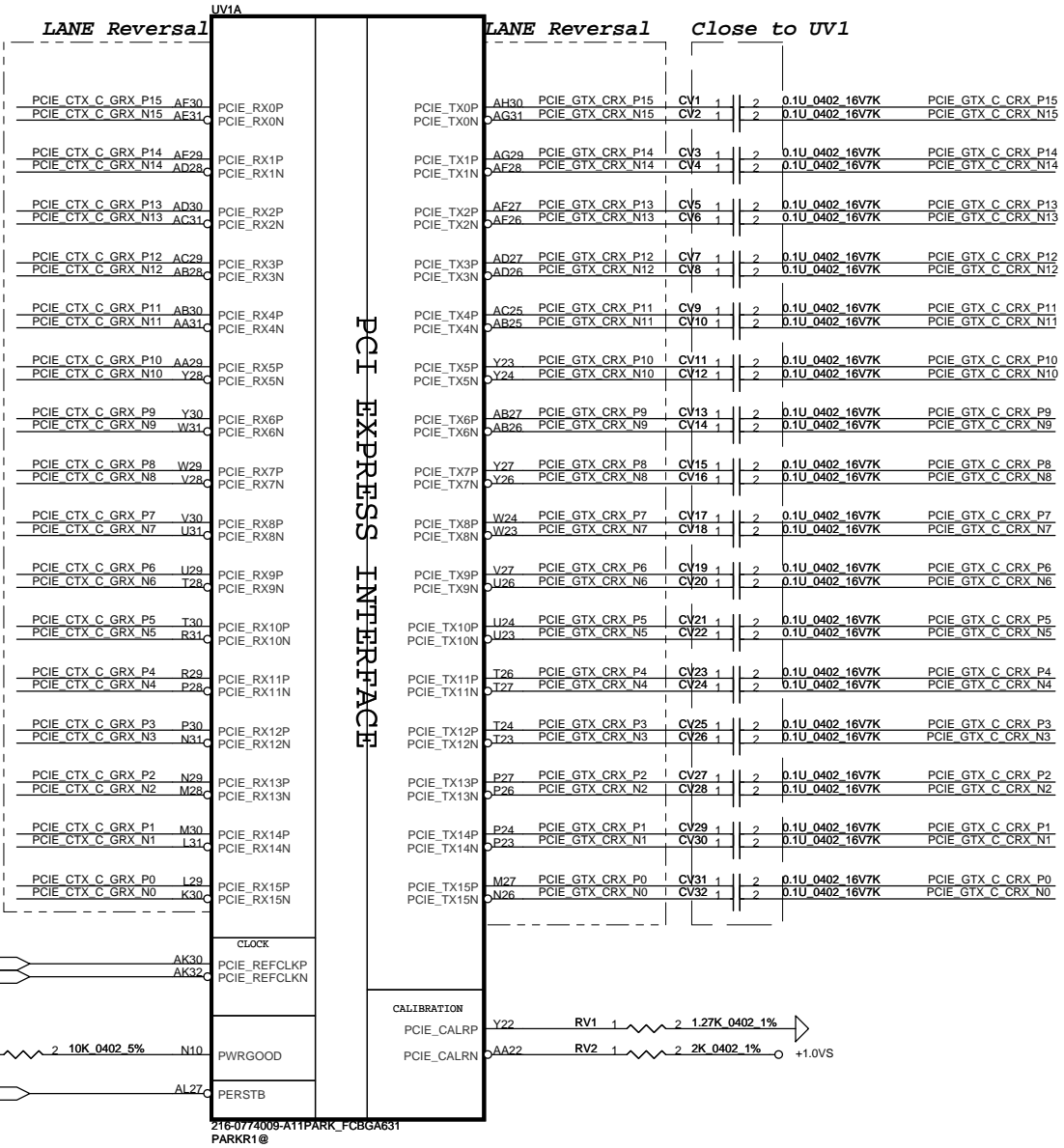
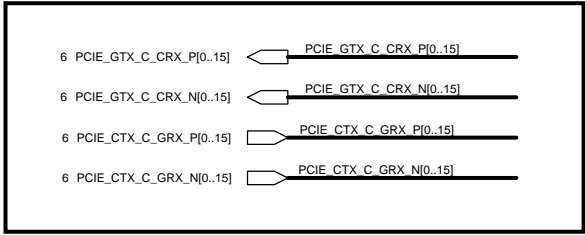
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Title: SCHEMATICS, MB A6847		
Document Number: 4019AP	Rev: B	Date: Tuesday, December 28, 2010
Sheet: 11	of: 52	

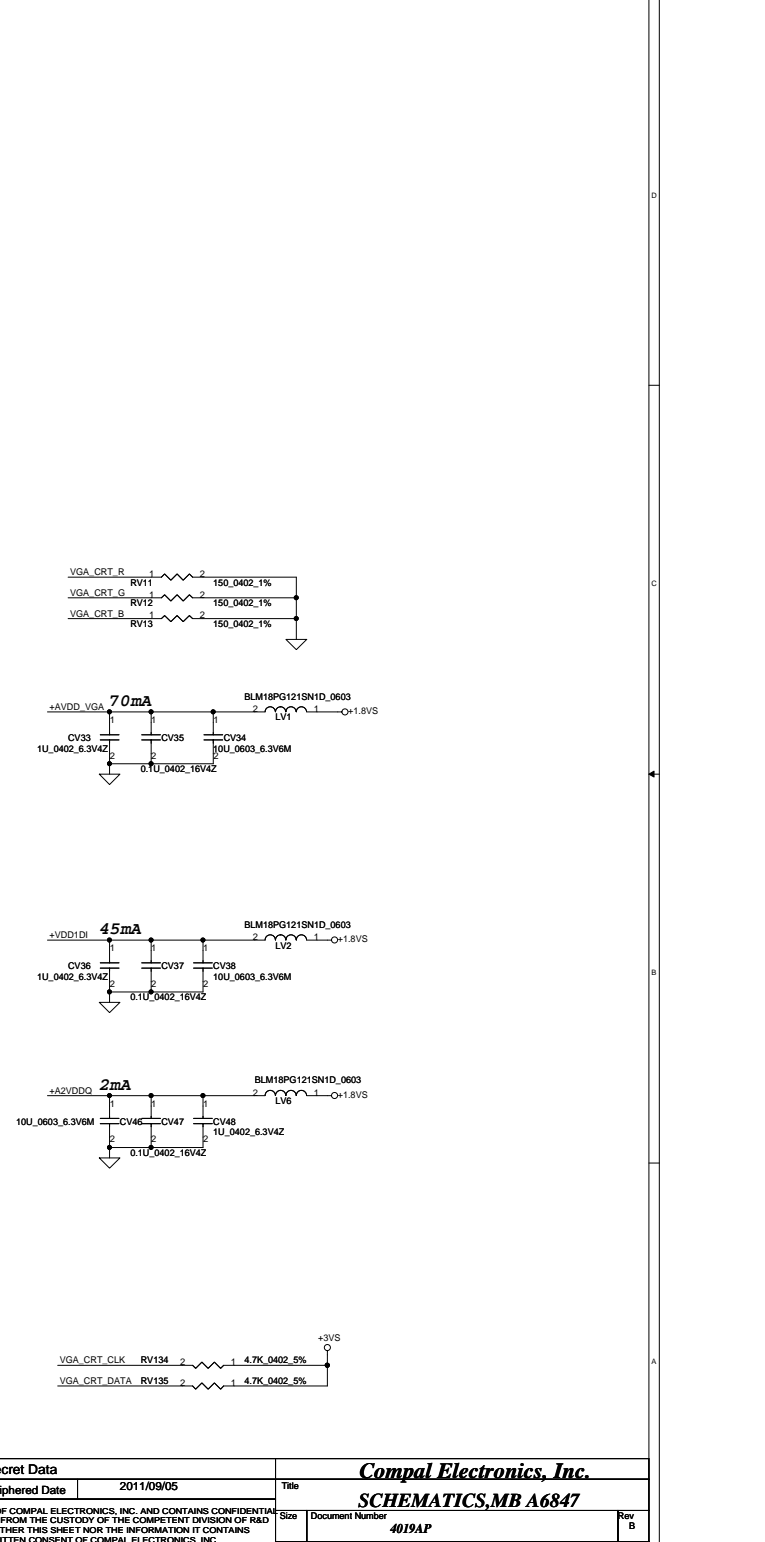
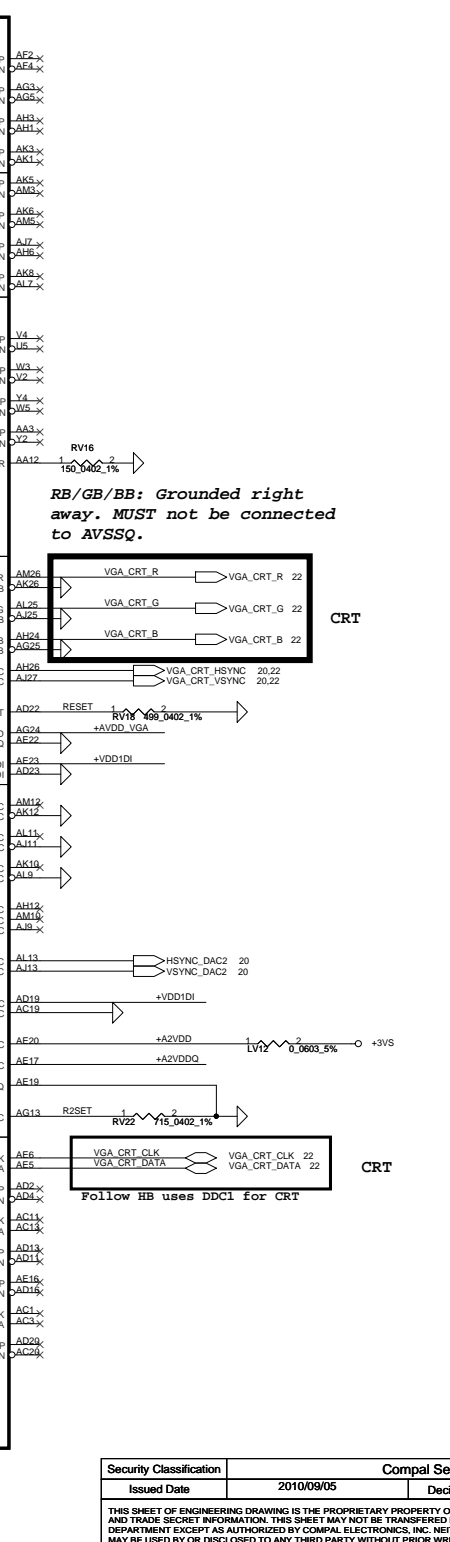
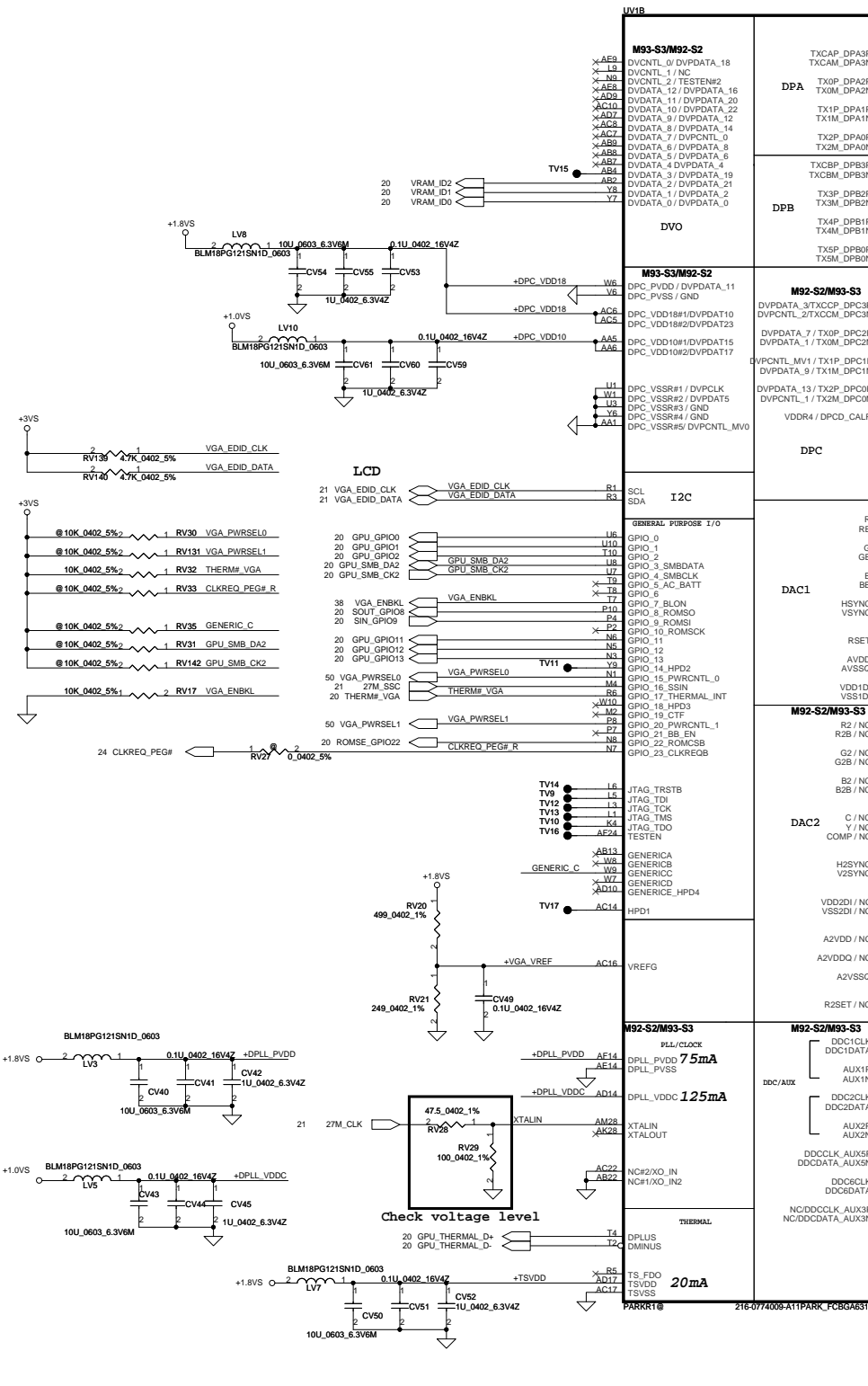
Standard Type DDR3 SO-DIMM B



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				4019AP	B
Date: Tuesday, December 28, 2010				Sheet	12 of 52



Security Classification		Compal Secret Data		Title	
Issued Date	2010/09/05	Deciphered Date	2011/09/05	Compal Electronics, Inc.	
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				4019AP	B
Date:				Tuesday, December 28, 2010	Sheet 13 of 52

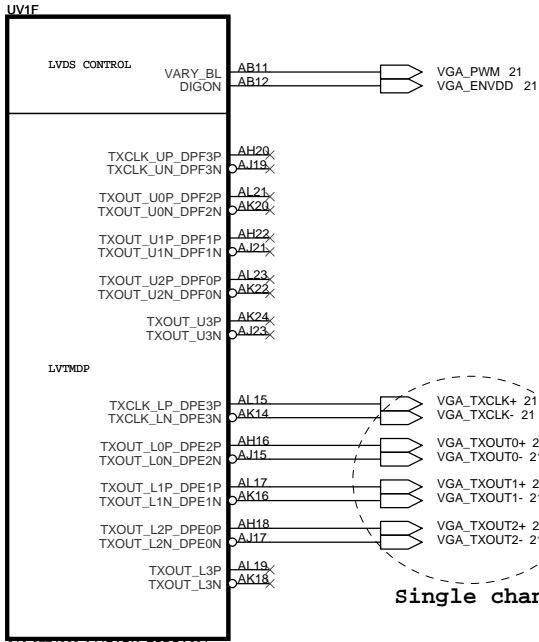


RB/GB/BB: Grounded right away. MUST not be connected to AVSSQ.

Follow HB uses DDC1 for CRT

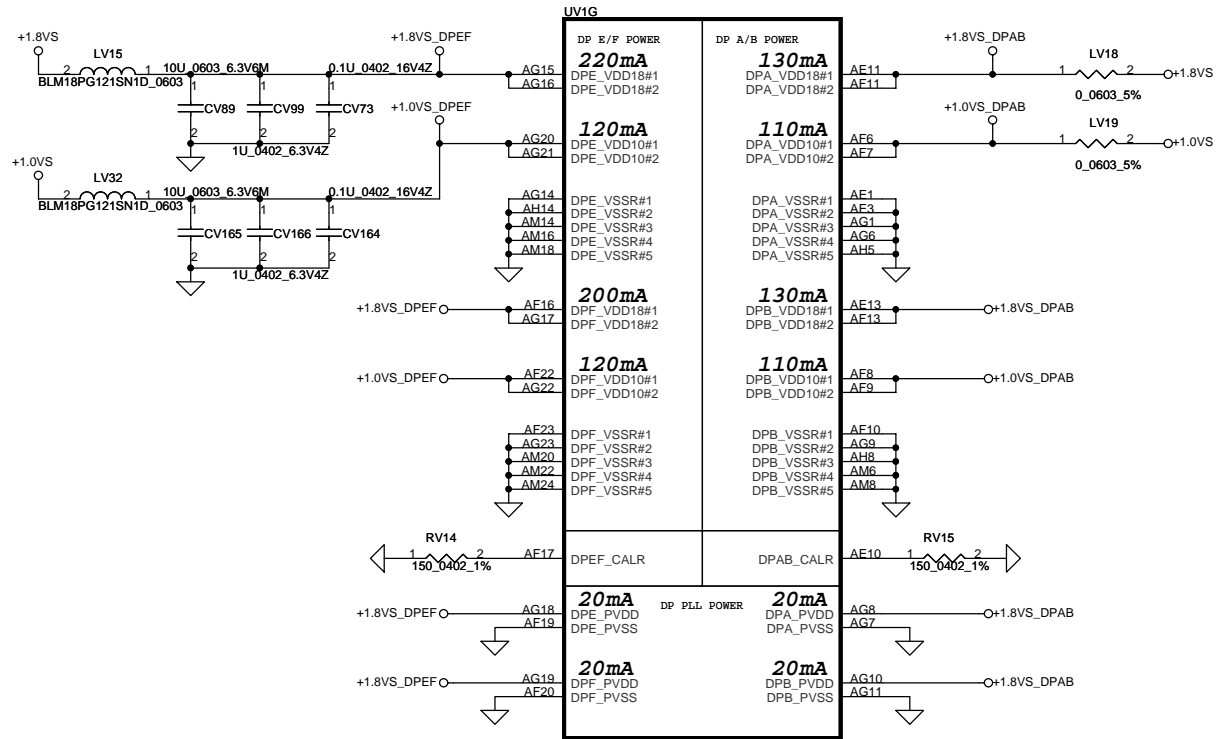
Check voltage level

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Size	Document Number	Rev	B	
	4019AP			
Date:	Tuesday, December 28, 2010	Sheet	14	of 52



Single channel

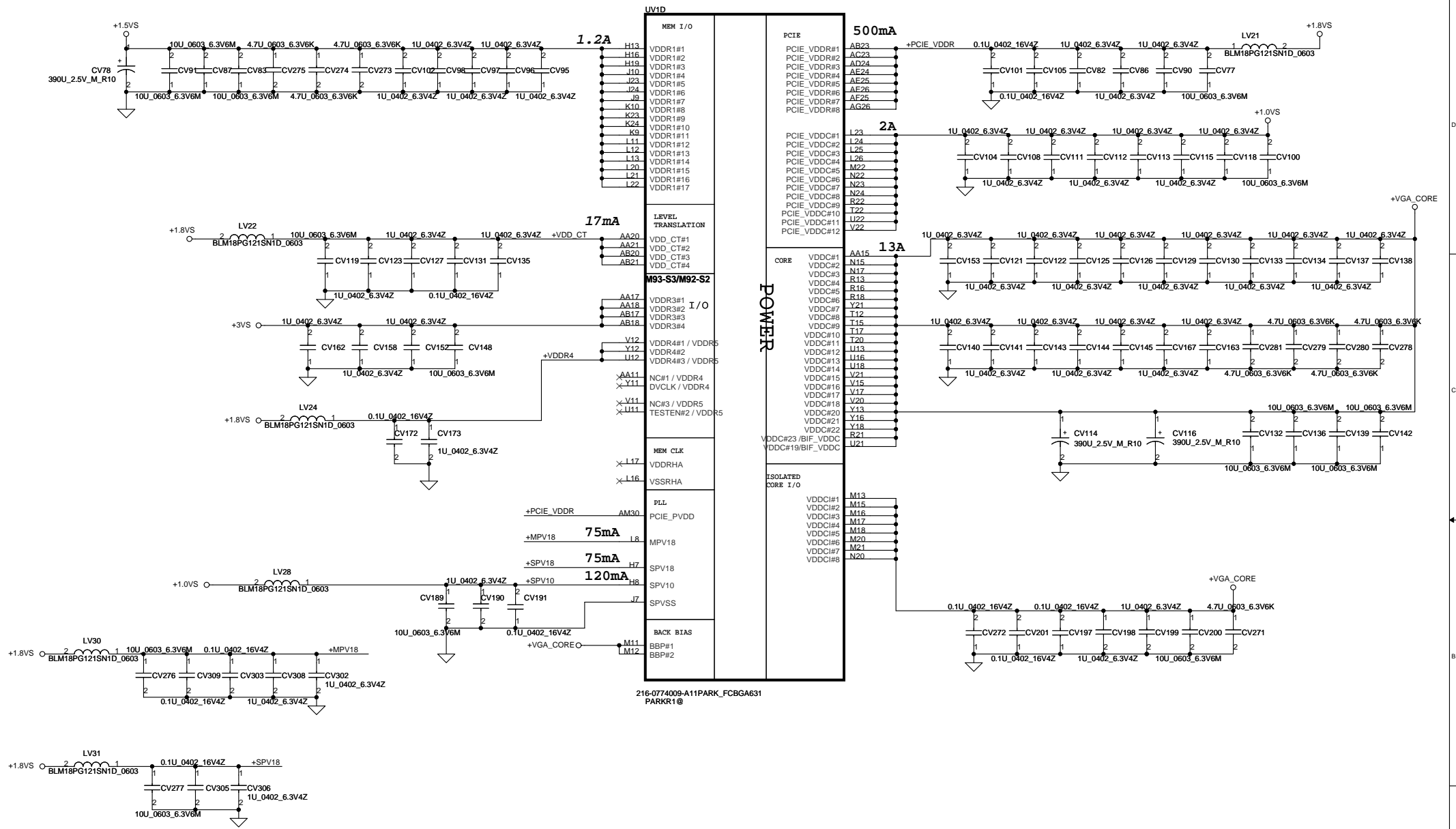
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PARKR1@



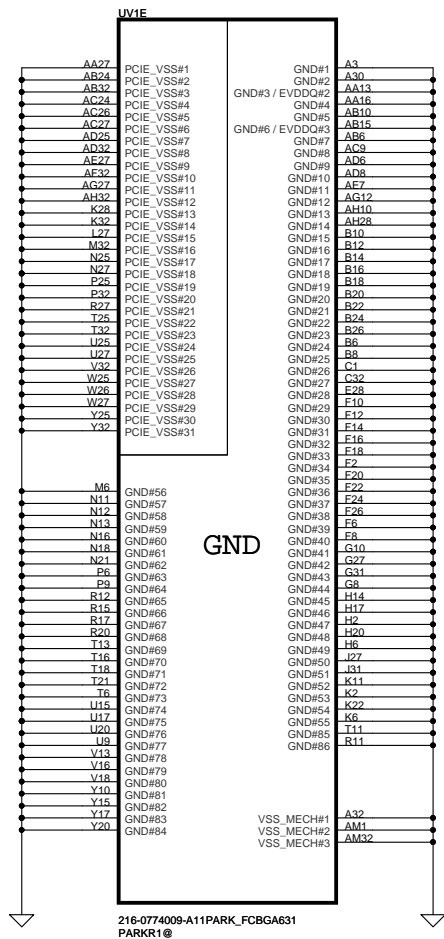
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PARKR1@

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				4019AP	B
Date: Tuesday, December 28, 2010				Sheet	15 of 52

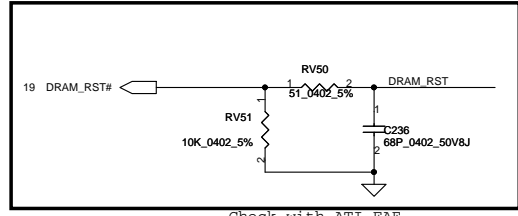
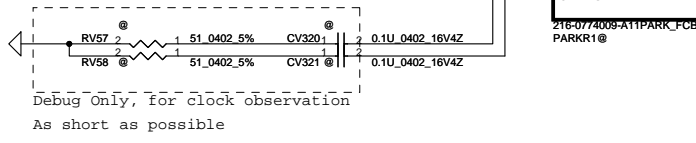
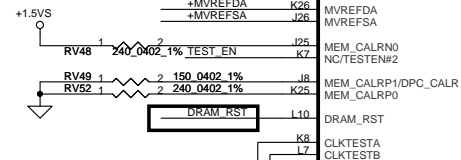
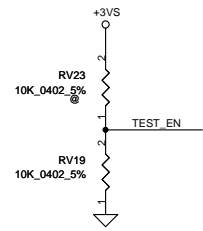
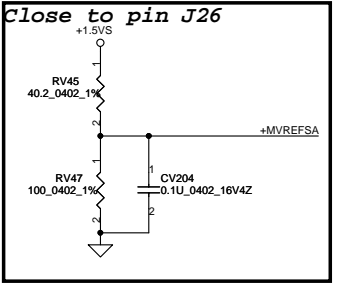
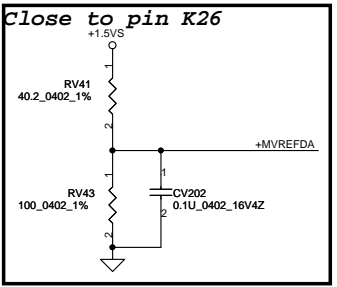
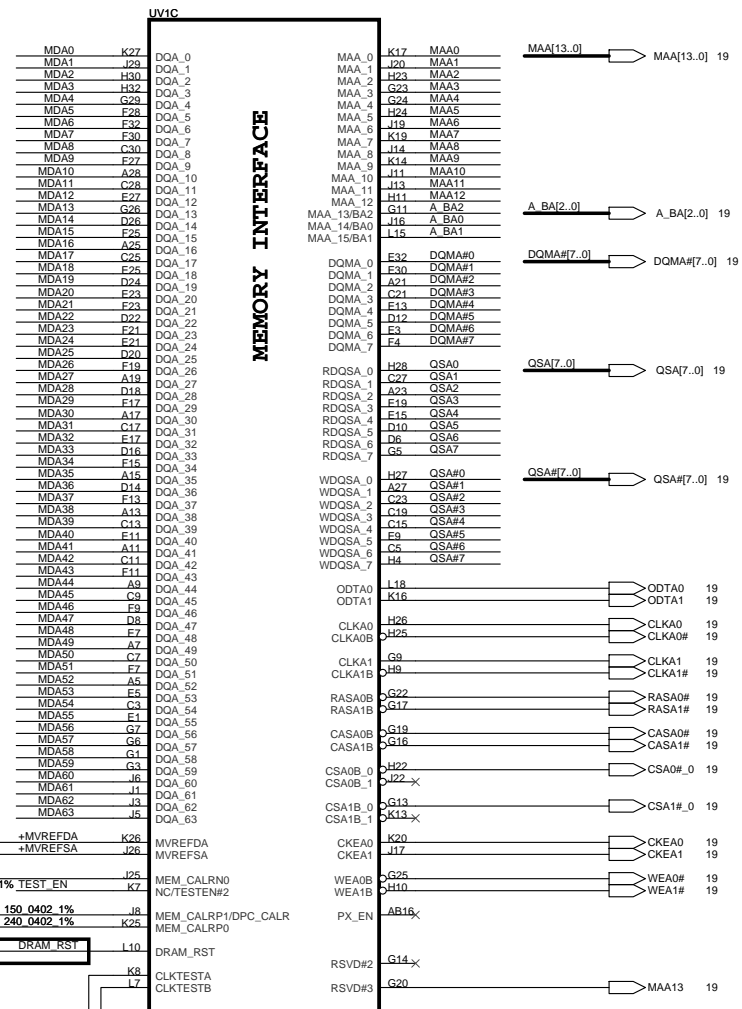
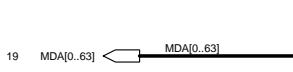
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Date: Tuesday, December 28, 2010			Sheet 16 of 52	Rev B



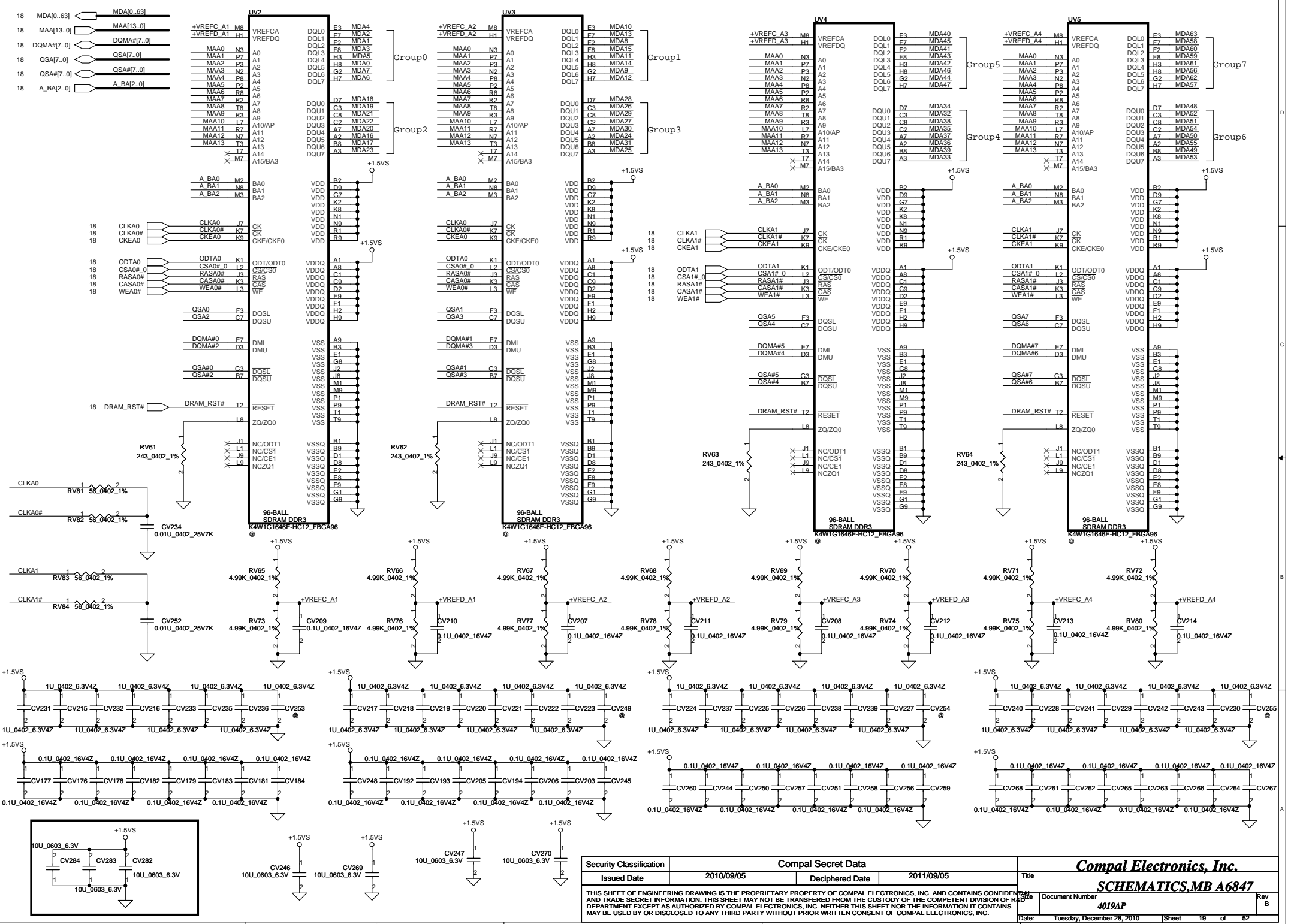
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				4019AP	B
				Date: Tuesday, December 28, 2010	Sheet 17 of 52



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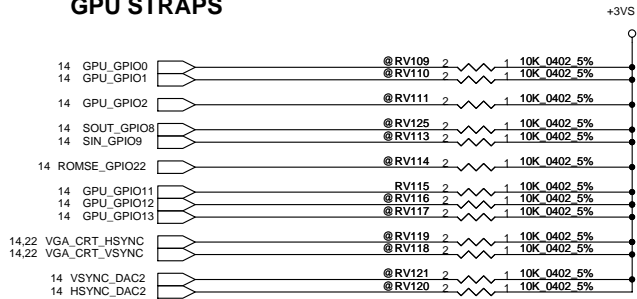
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SCHMATICS, MB A6847	
Document Number	4019AP
Date:	Tuesday, December 28, 2010
Sheet	18 of 52



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				4019AP	B
Date: Tuesday, December 28, 2010				Sheet	19 of 52

SCHMATIC, MB A6847

GPU STRAPS



GPU by the system BIOS		GPU by VBIOS
GPIO22 = 0 (BIOS_ROM_EN = 0)		GPIO22 = 1 (BIOS_ROM_EN = 1)
GPIO[13:11]	MEMORY SIZE	GPIO[13:11]
0 0 0	128MB	1 0 0
0 0 1	256MB	(M25P05A)
0 1 0	64MB	

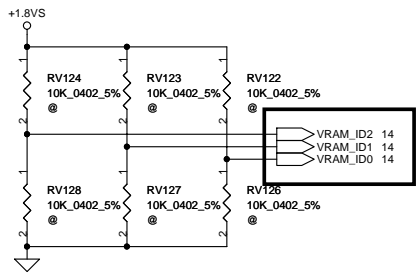
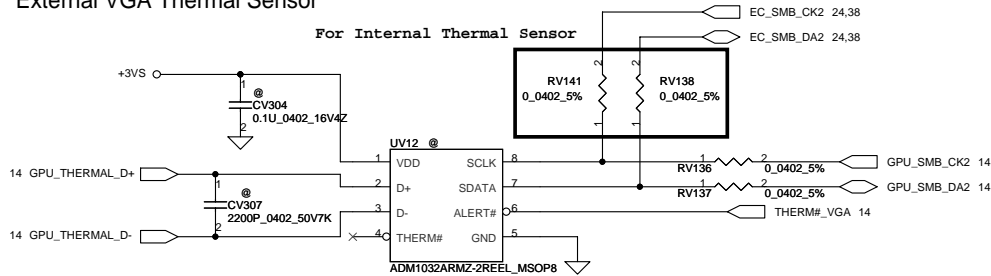
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

Straps Name	Pin Name	Net Name	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	GPU_GPI00	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	0
TX_DEEMPH_EN	GPIO1	GPU_GPI01	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	0
BIF_GEN2_EN_A	GPIO2	GPU_GPI02	PCIE GNE2 ENABLED 0 = Advertises the PCIe device as 2.5 GT/s capable at power-on 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	0 5.0 GT/s capability will be controlled by software
RESERVED	GPIO_8_ROMSO	SOUT_GPI08	RESERVED	0
RESERVED	GPIO_21_BB_EN	N.C	RESERVED	0 (Internal pulldown)
VGA_DIS	GPIO_9_ROMSI	SIN_GPI09	VGA Controller 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0 (Enable)
BIOS_ROM_EN	GPIO_22_ROMCSB	ROMSE_GPI022	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0
CONFIG(2:0)	GPIO[13:11]	GPU_GPI011 GPU_GPI012 GPU_GPI013	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size.	0 0 1 (256M)
VIP_DEVICE_STRAP_DIS	V2SYNC	VSYNC_DAC2	VIP Device Strap Enable indicates to the software driver 0 - Driver would ignore the value sampled on VHAD_0 during reset 1 - Driver would use the value sampled at reset from VHAD_0 to determine whether or not a VIP slave device is connected	0
RESERVED	H2SYNC	HSYNC_DAC2	RESERVED	0
AUD[1] AUD[0]	HSYNC VSYNC	VGA_CRT_HSYNC VGA_CRT_VSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	0 0

External VGA Thermal Sensor

For Internal Thermal Sensor

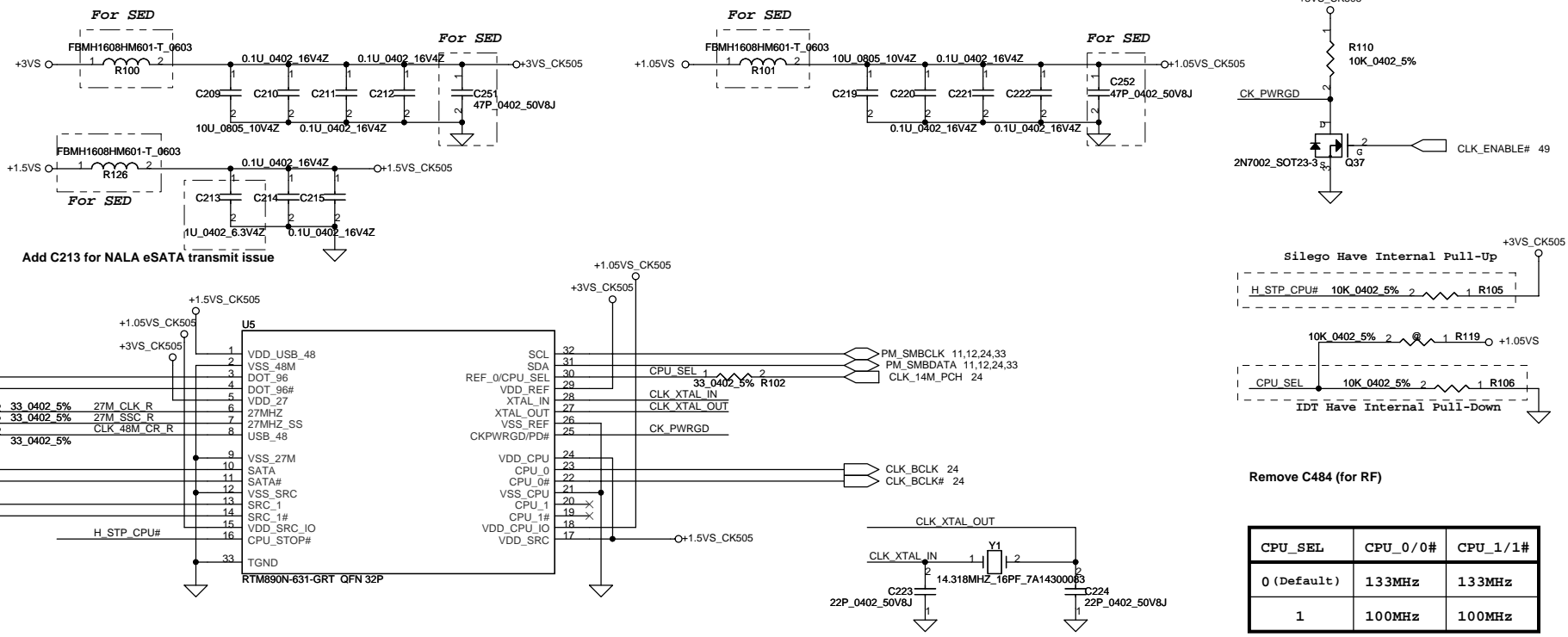


Need to check the VBIOS setting

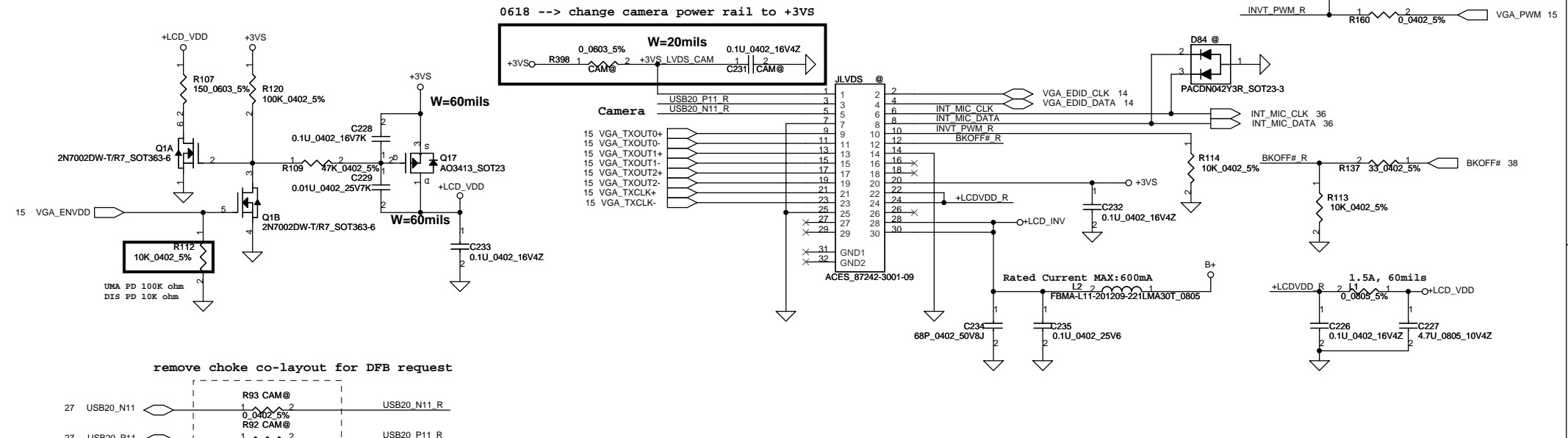
STRAPS	PIN	GPU	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 2,1,0	
VRAM_ID[2:0]	DVDATA (2,1,0)	Park XT S3	512M 64Mx16 (x4)	HYN H5TQ1G63BFR-12C-C	SA000032460	0 0 0	
			512M 64Mx16 (x4)	SAM K4W1G1646E-HC12	SA000035700	0 0 1	
			1G 128Mx16 (x4)	HYN H5TQ2G63BFR-12C	SA00003VS00	0 1 0	
			1G 128Mx16 (x4)	SAM K4W2G1646C-HC12	SA00003M040	0 1 1	
		Design Ready					
		Robson LP S3	512M 64Mx16 (x4)	HYN H5TQ1G63BFR-12C-C	SA000032460	1 0 0	
512M 64Mx16 (x4)	SAM K4W1G1646E-HC12		SA000035700	1 0 1			
1G 128Mx16 (x4)	HYN H5TQ2G63BFR-12C		SA00003VS00	1 1 0			
1G 128Mx16 (x4)	SAM K4W2G1646C-HC12		SA00003M040	1 1 1			
Design Ready							

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				4019AP	
				Date: Tuesday, December 28, 2010	Sheet 20 of 52

Clock Generator

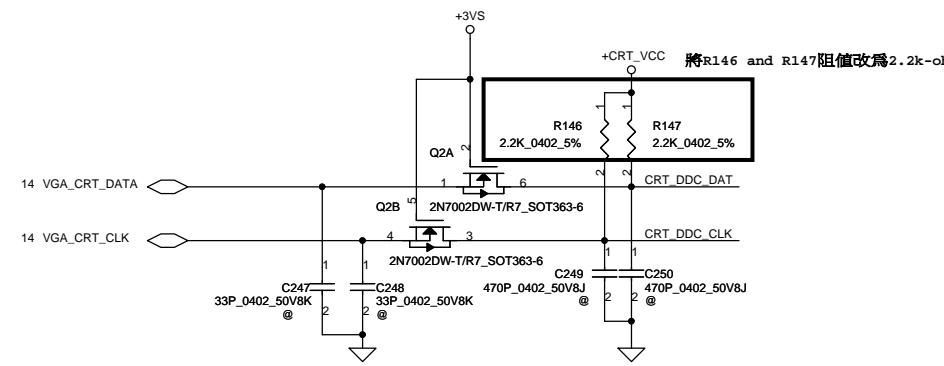
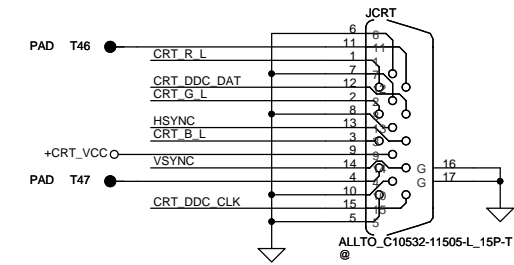
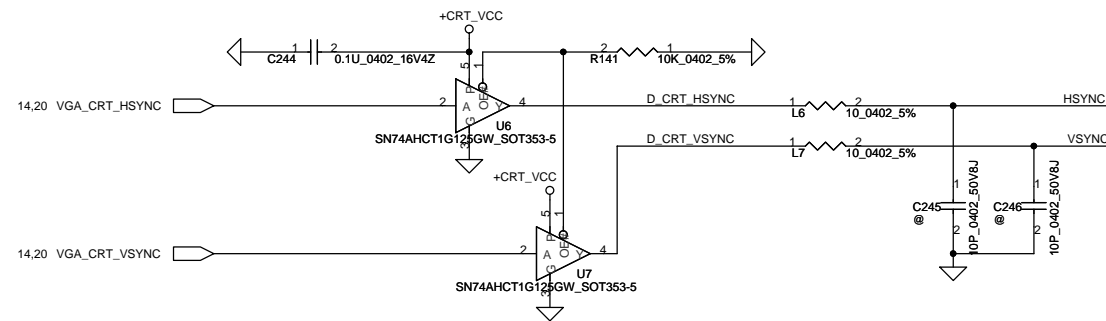
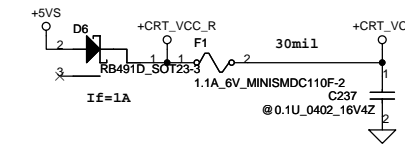
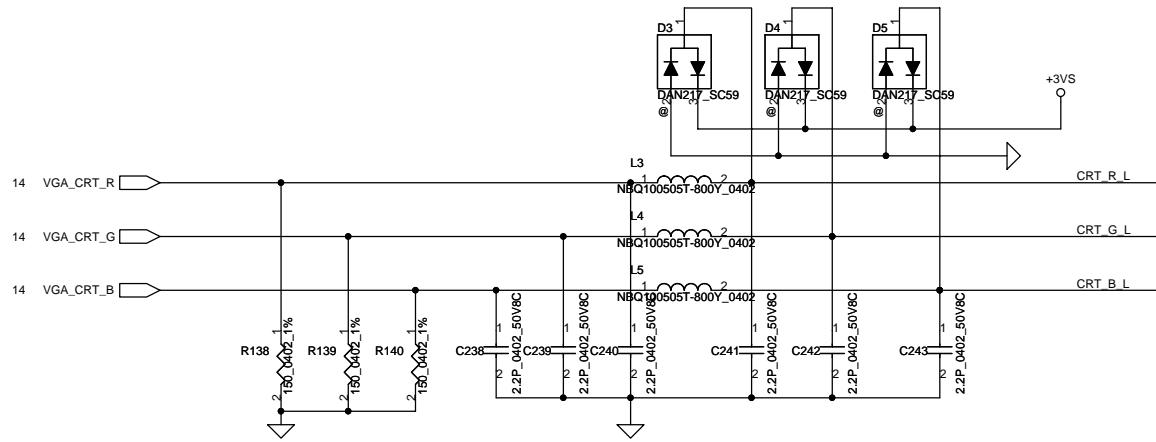


LVDS / Int.Camera / Int.MIC Conn

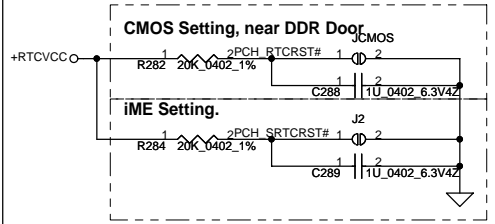


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Size	Document Number	Customer	4019AP	Rev	B
Date:	Tuesday, December 28, 2010	Sheet	21	of	52

CRT CONNECTOR



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				4019AP	
Date: Tuesday, December 28, 2010				Sheet	22 of 52



Integrated SUS 1.05V VRM Enable

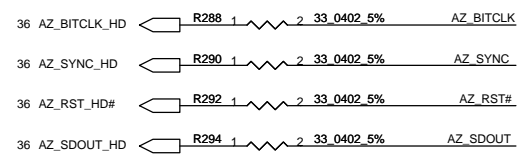
PCH_INTVRMEN	High - Enable Internal VRs (must be always pulled high)
--------------	---

HDA_SYNC
This signal has a weak internal pull down.
H=>On Die PLL is supplied by 1.5V
*L=>On Die PLL is supplied by 1.8V

HDA_SDO
This signal has a weak internal pull down.
This signal can't PU

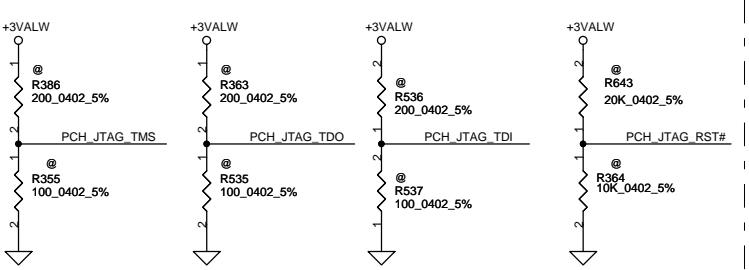
Flash Descriptor Security Override

HDA_DOCK_EN#	Low = Enabled High = Disabled *
--------------	------------------------------------



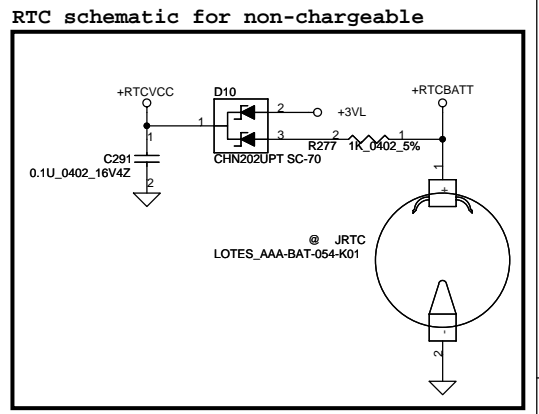
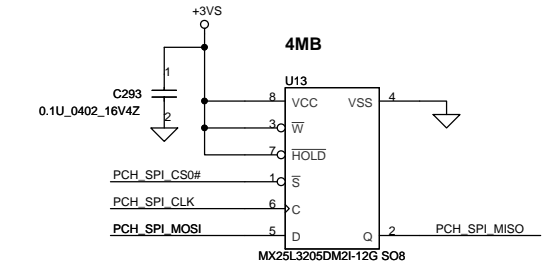
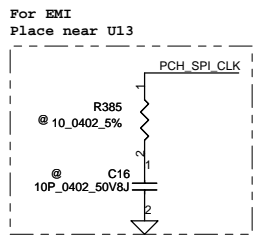
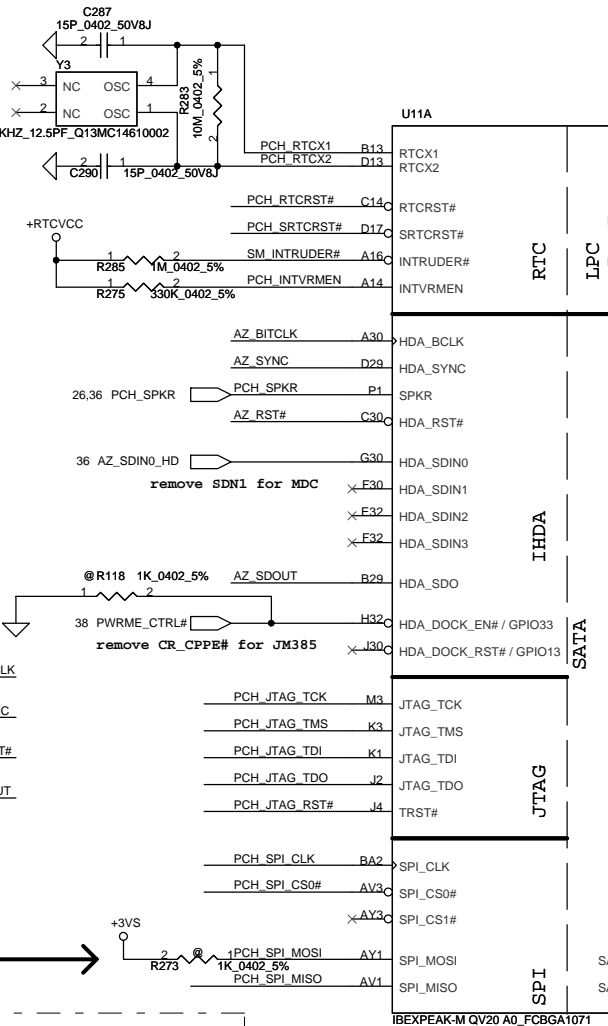
ITPM Enabled Internal: Pull down 20k

SPI_MOSI	High = Enabled Low = Disabled (Default)
----------	--

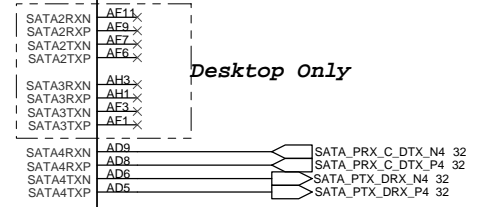


PCH_JTAG TCK
R156 51k 0.402 5%
06/01 change R125 from 4.7K to 51 ohm

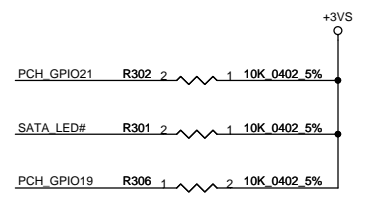
PCH Pin	RefDes	PCH JTAG Enable		PCH JTAG Disable (Default)	
		ES1	ES2	ES1	ES2
PCH_JTAG_TDO	R358	No Install	200ohm	No Install	No Install
PCH_JTAG_TMS	R355	No Install	100ohm	No Install	No Install
PCH_JTAG_TDI	R354	100ohm	100ohm	No Install	No Install
PCH_JTAG_RST#	R536	200ohm	200ohm	20kohm	No Install
	R537	100ohm	100ohm	10kohm	No Install
PCH_JTAG_TCK	R156	51ohm	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R643	20kohm	20kohm	No Install	No Install
	R353	10kohm	10kohm	No Install	No Install



1ST HDD



SATA ODD



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Date:	Tuesday, December 28, 2010	Sheet	23	of	52

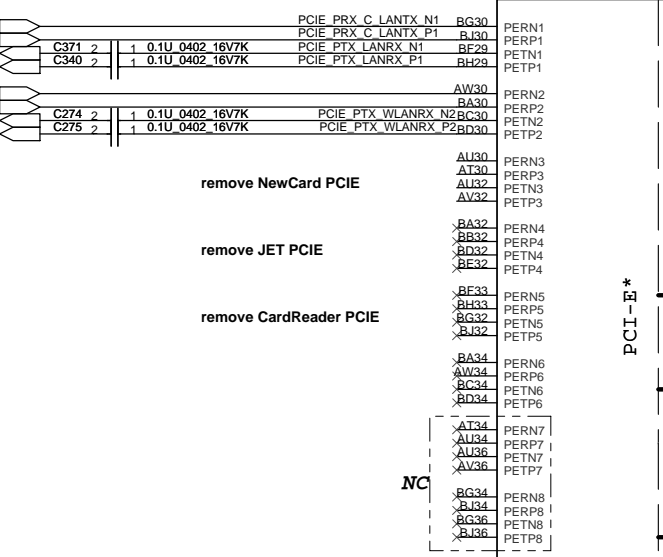


For LAN

34 PCIE_PRX_C_LANTX_N1
34 PCIE_PRX_C_LANTX_P1
34 PCIE_PT_X_C_LANRX_N1
34 PCIE_PT_X_C_LANRX_P1

For WLAN

33 PCIE_PRX_WLANTX_N2
33 PCIE_PRX_WLANTX_P2
33 PCIE_PT_X_C_WLANRX_N2
33 PCIE_PT_X_C_WLANRX_P2



remove NewCard PCIE

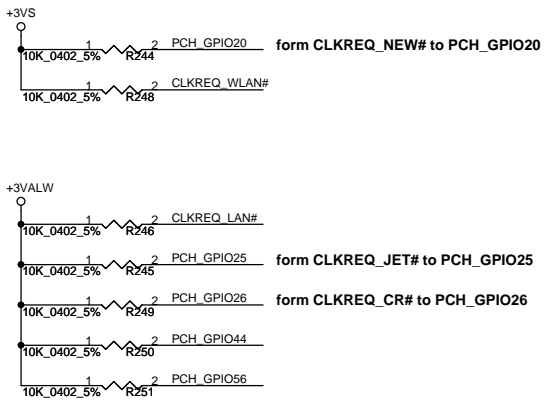
remove JET PCIE

remove CardReader PCIE

NC

LAN

WLAN



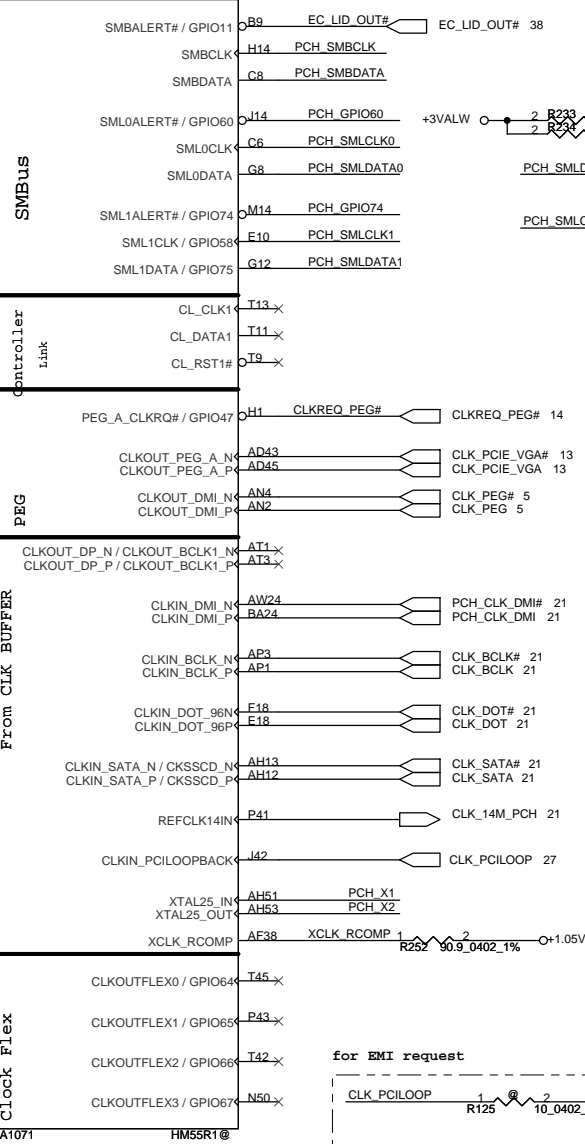
remove NEWCARD CLK

remove JET CLK

form CLKREQ_NEW# to PCH_GPIO20

form CLKREQ_JET# to PCH_GPIO25

form CLKREQ_CR# to PCH_GPIO26



PCI-E*

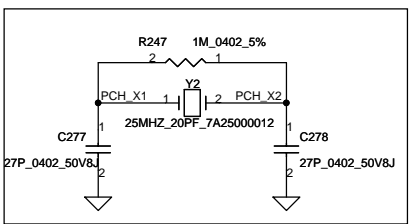
Controller Link

PEG

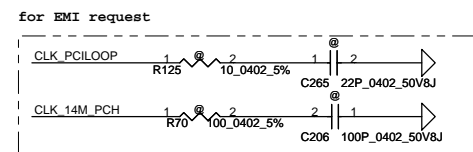
From CLK BUFFER

Clock Flex

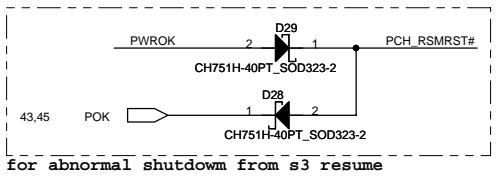
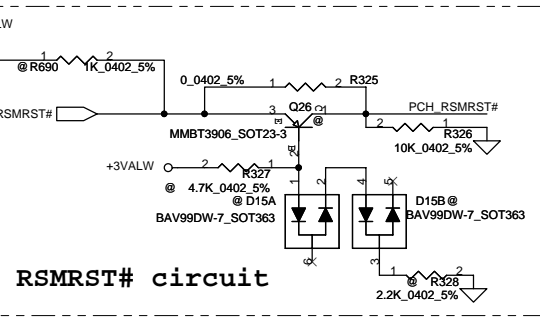
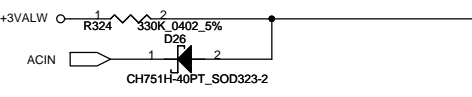
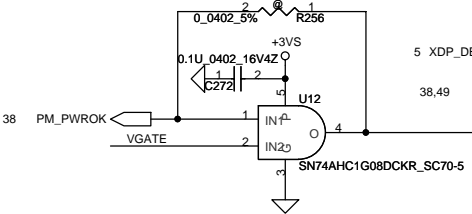
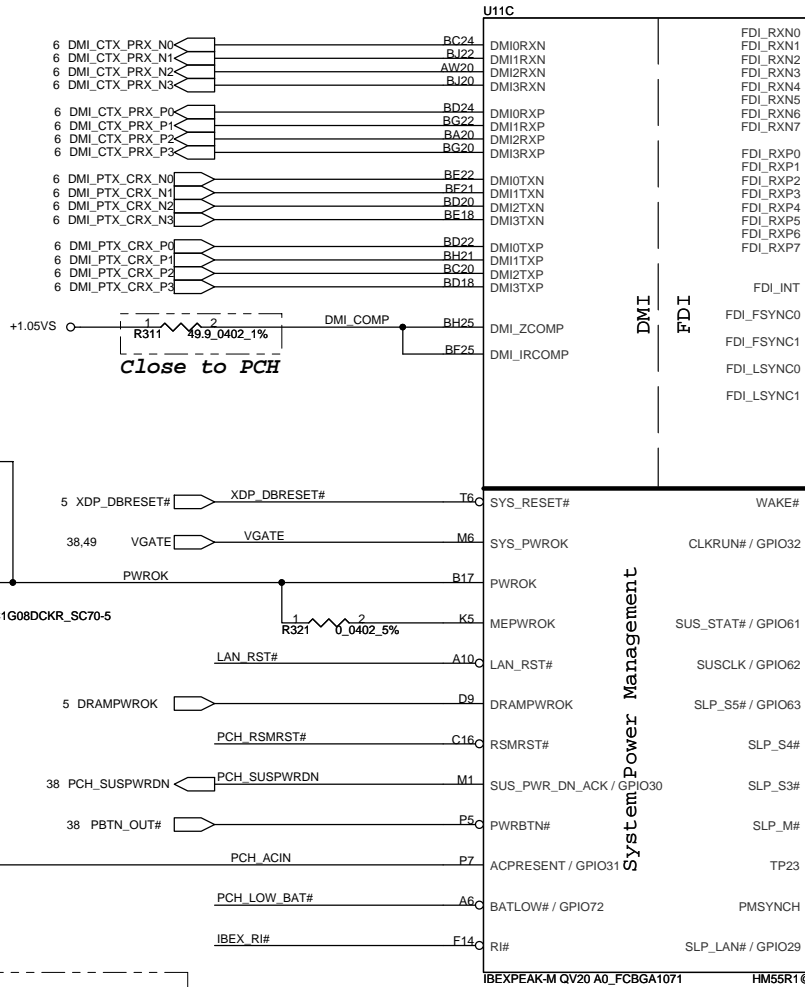
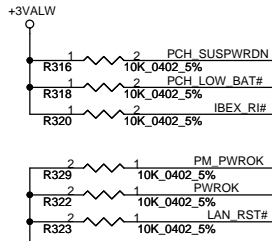
FROM CLK GEN FOR: 133/100/96/14.318 MHZ



Note: Stuff 0 ohm if 25MHz crystal un-stuff



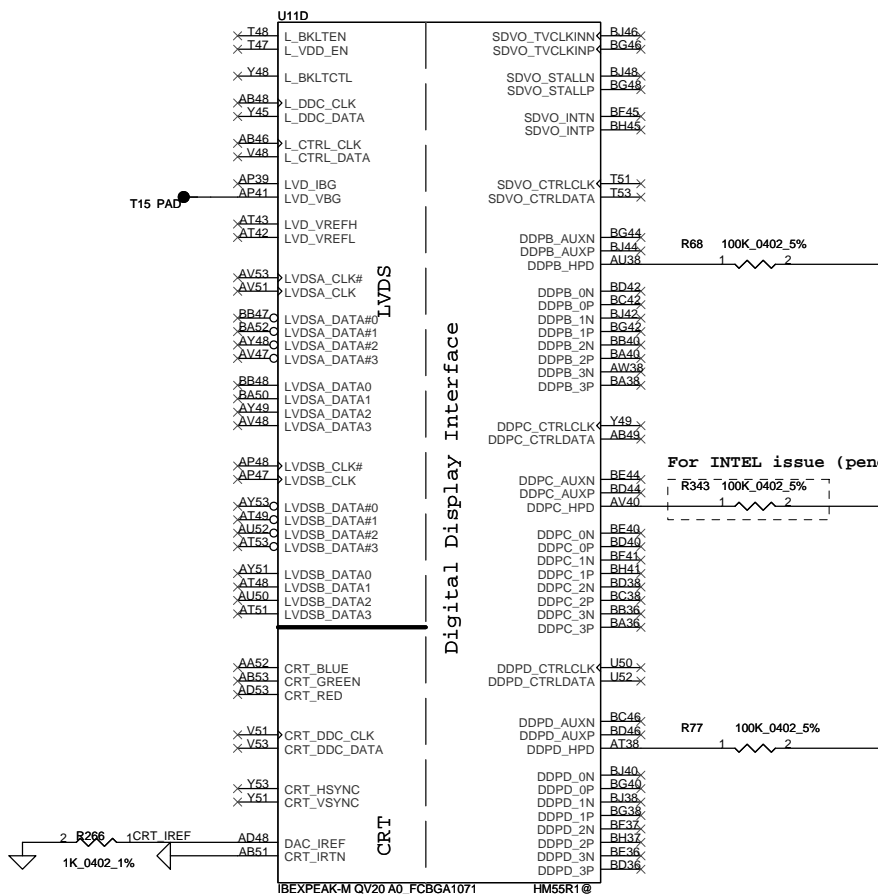
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				4019AP	
Date: Tuesday, December 28, 2010				Sheet	24 of 52



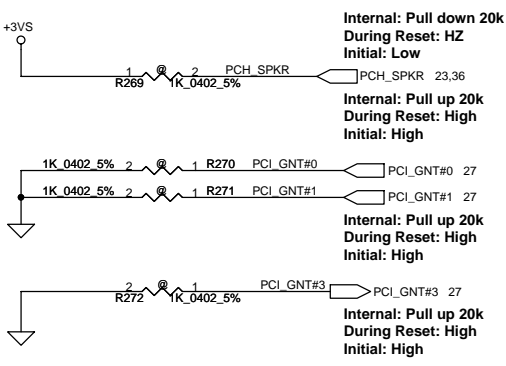
0716 --> Unmount : R327, Q26, D15A, D15B, R328, R690
 Mount : R325, D29, D28

for abnormal shutdown from s3 resume

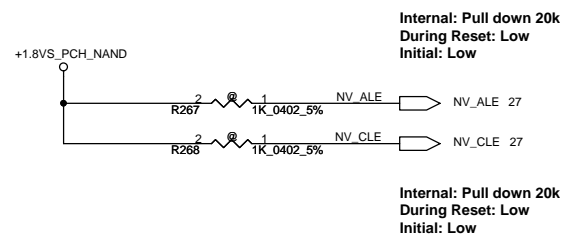
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				4019AP	
Date:				Tuesday, December 28, 2010	Sheet 25 of 52



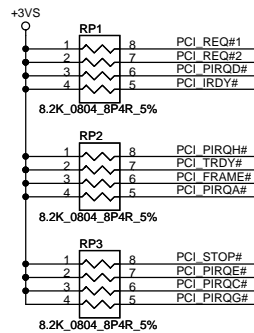
PCH Strap Pin



NO REBOOT Strap		
PCH_SPKR	Low= Disable	High= Enable
Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI (Default)
A16 Swap Override Strap		
PCI_GNT#3	Low= A16 swap override Enable	High= A16 swap override Disable

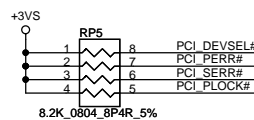
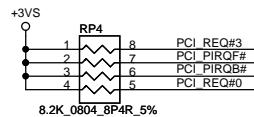


Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled (Default)
DMI Termination Voltage	
NV_CLE	Low= Set to Vss (Default) High= Set to Vcc



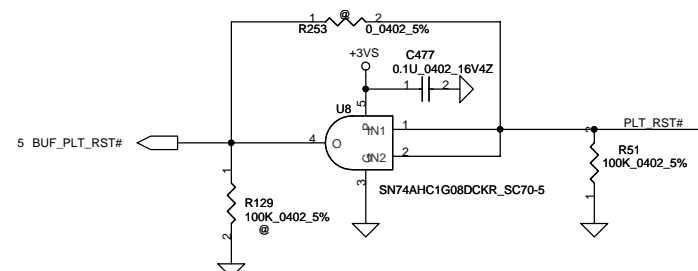
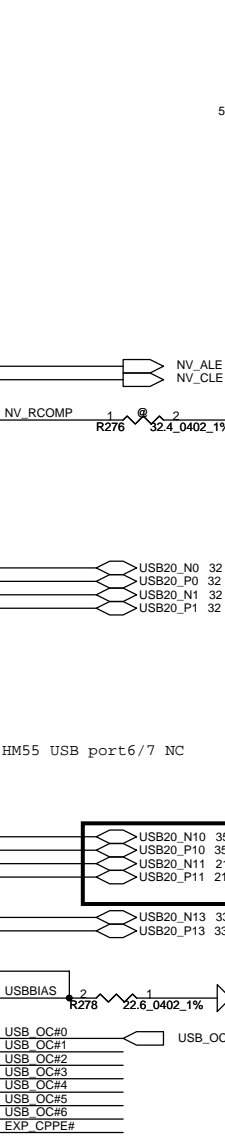
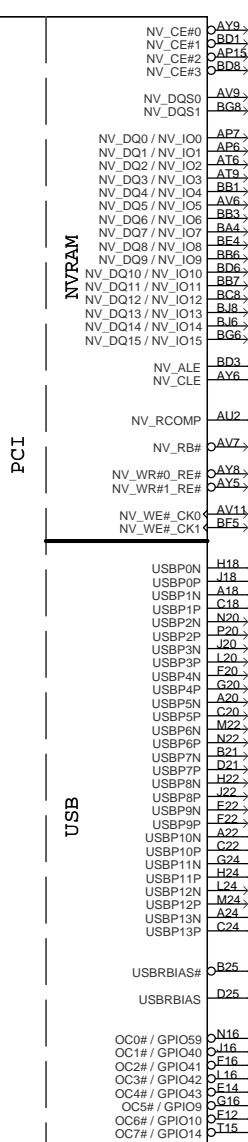
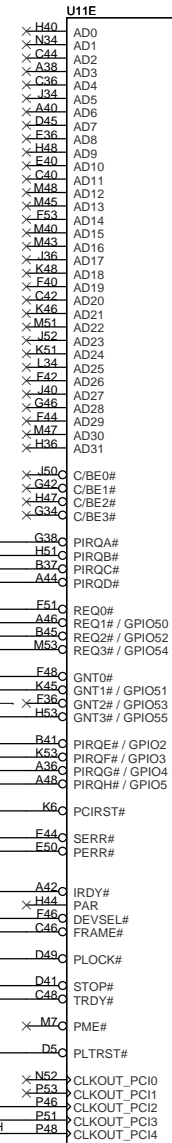
add PCI_REQ#2 for non-ODD_EN#

GNT2#: Not pull low, internal pull up 20K



13,33,34,38,39 PLT_RST#

39 CLK_PCI_DDR
38 CLK_PCI_EC
24 CLK_PCI_LOOP

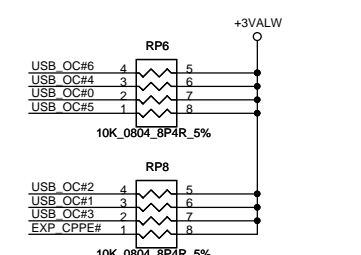


USB-LIGHT1
USB-LIGHT2
USB-Left1
remove eSATA
remove NewCard
remove BT

remove FingerPr
remove FELICA
Card reader(2 in 1)
Int. Camera
remove 3G/TX#1

WLAN

Within 500 mils



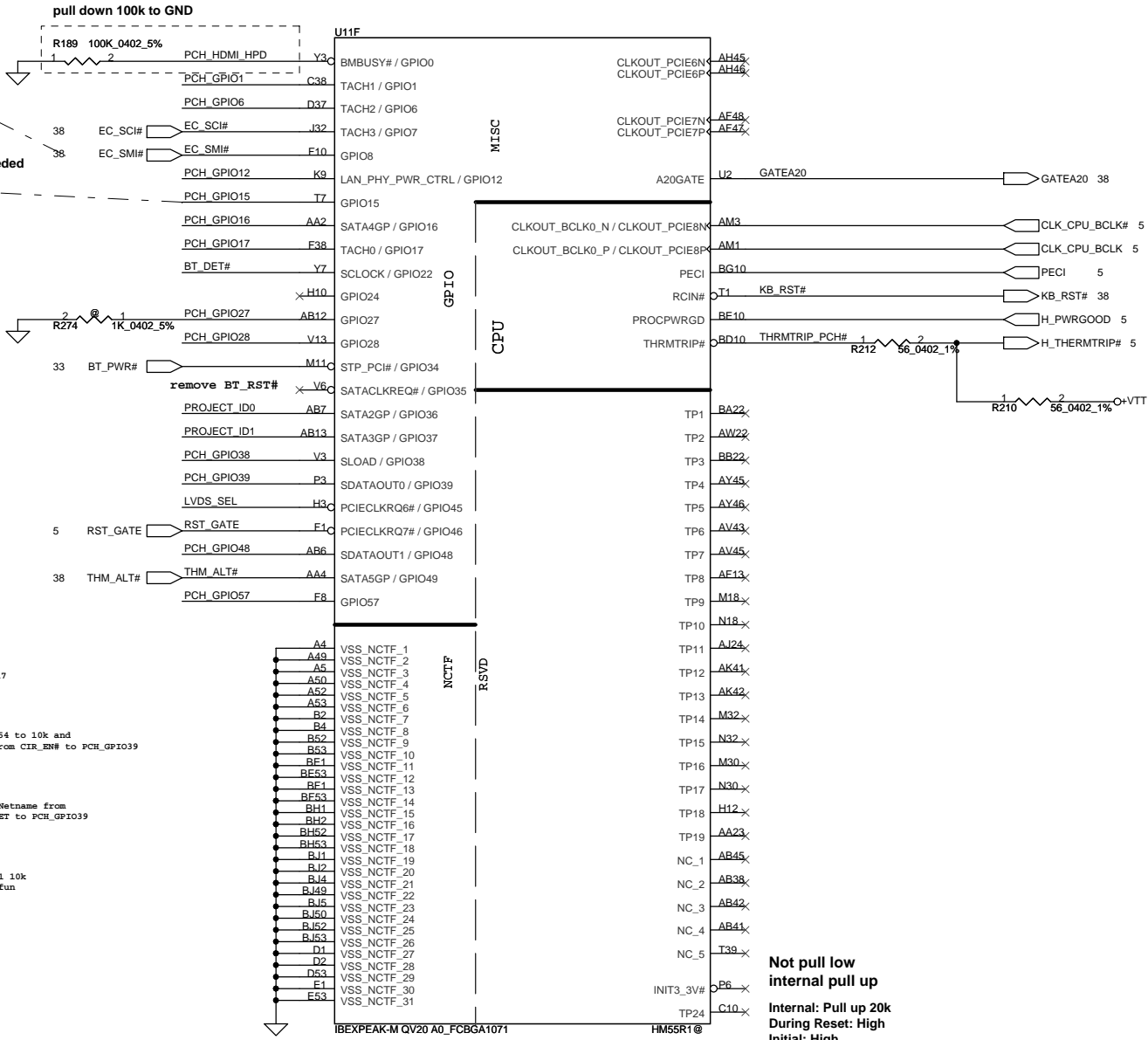
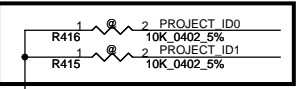
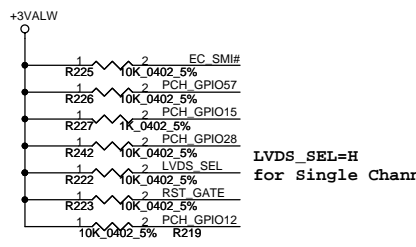
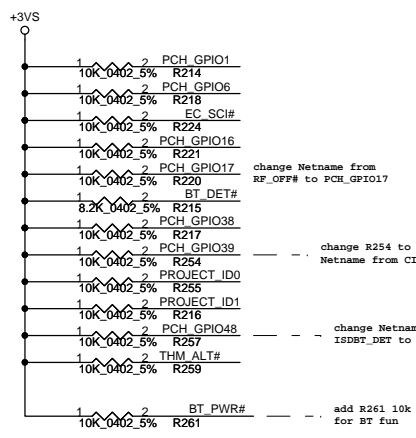
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				4019AP	
Date:	Tuesday, December 28, 2010	Sheet	27	of	52

GPIO8
Not pull down
 Internal: Pull up 20k
 During Reset: High
 Initial: High

GPIO15
 a Strong pull up may be needed
 for GPIO Functionality
 Internal: Pull down 20k
 During Reset: Low
 Initial: Low

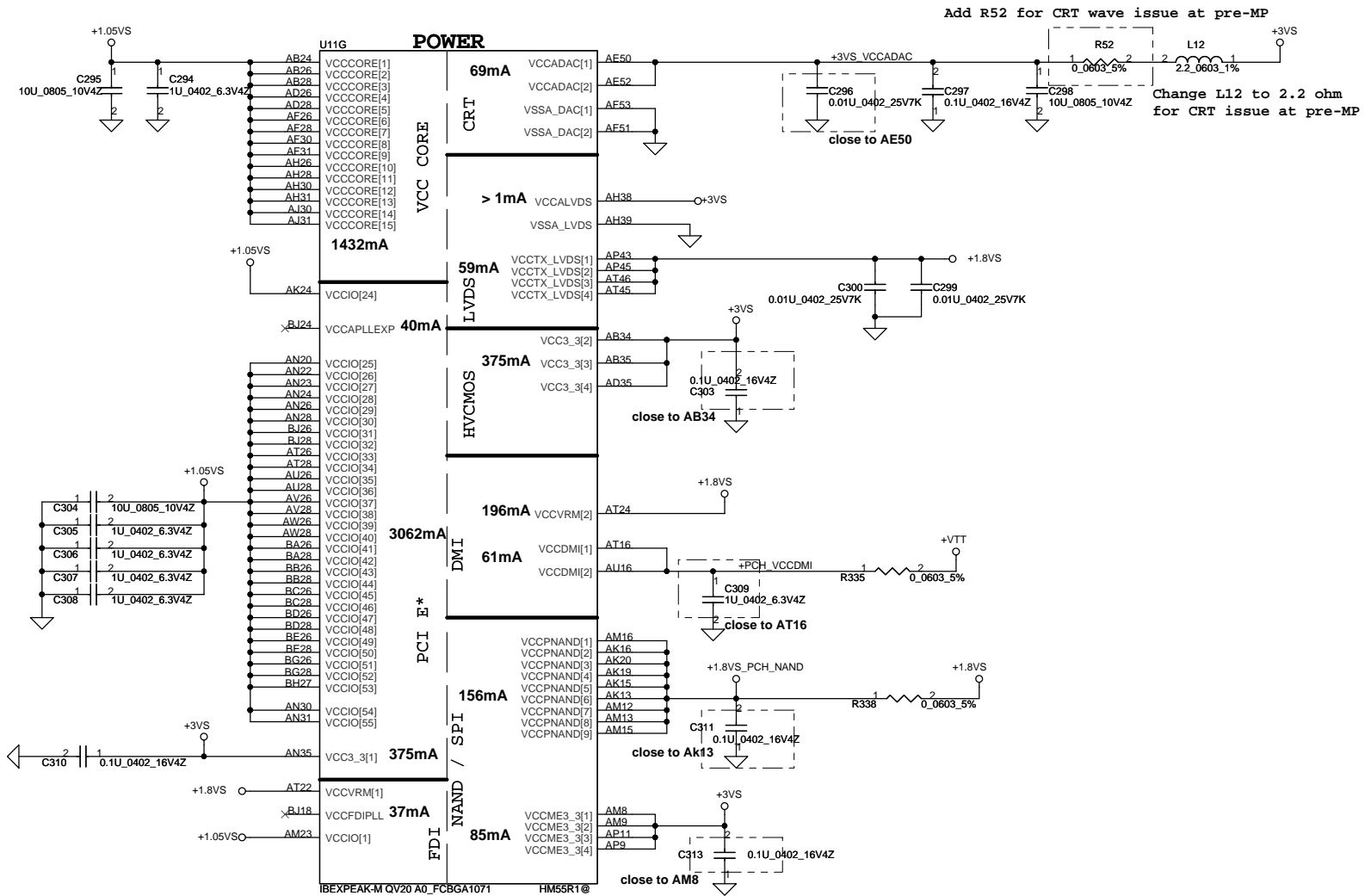
On-Die PLL VR
PCH_GPIO27 High = Enabled (Default)
 Low = Disabled

PROJECT_ID		
Name	ID0	ID1
NBQAA 11.6/13.3"	L	L
NBQAA 14"	L	H
*NBQAA 16"	H	L
NALAA 17.3"	H	H



Not pull low
internal pull up
 Internal: Pull up 20k
 During Reset: High
 Initial: High

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				4019AP	
Date: Tuesday, December 28, 2010				Sheet	28 of 52



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				4019AP	
				Date:	Tuesday, December 28, 2010
				Sheet	29 of 52

VccLAN may be grounded if Intel LAN is disabled

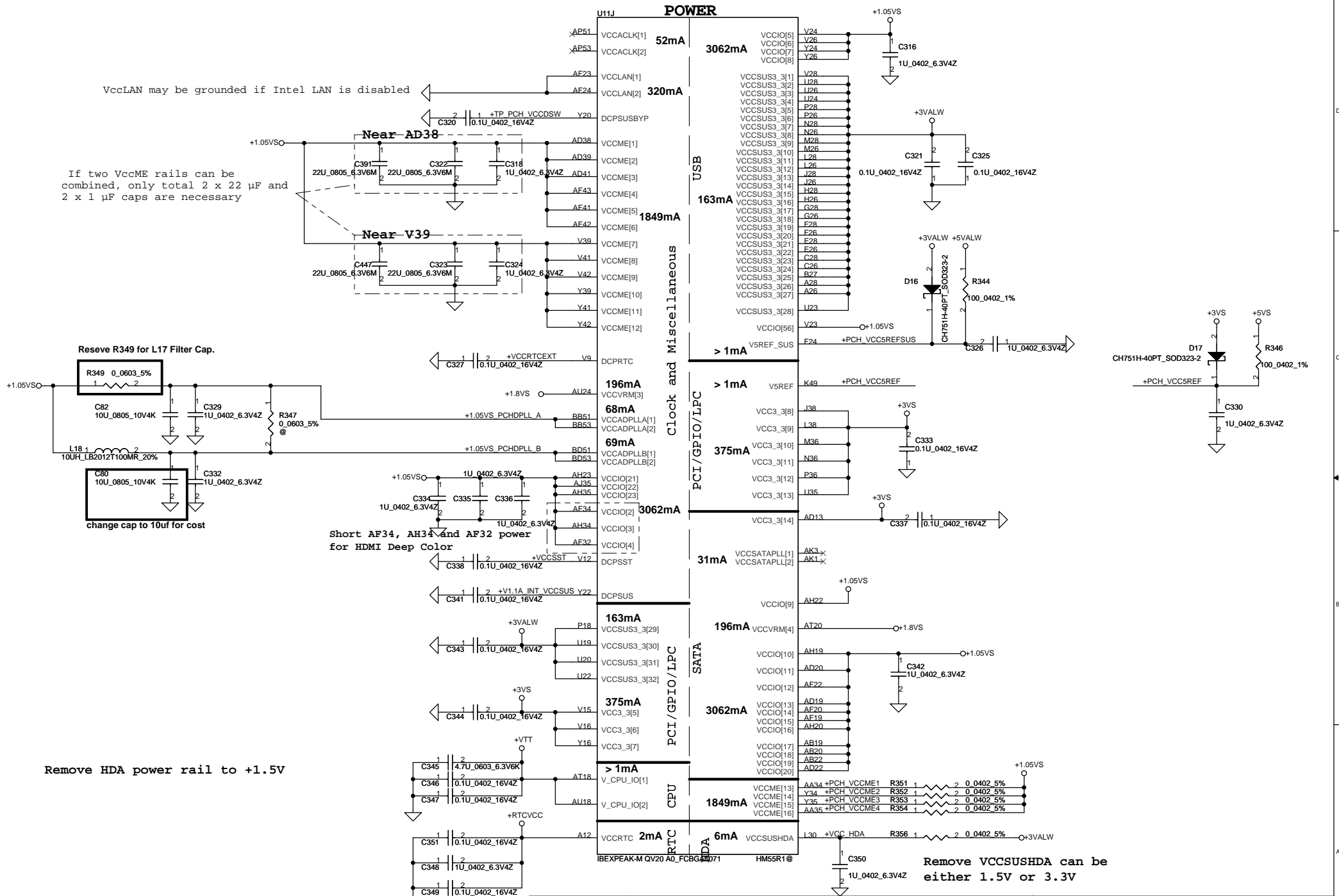
If two VccME rails can be combined, only total 2 x 22 μ F and 2 x 1 μ F caps are necessary

Reserve R349 for L17 Filter Cap.

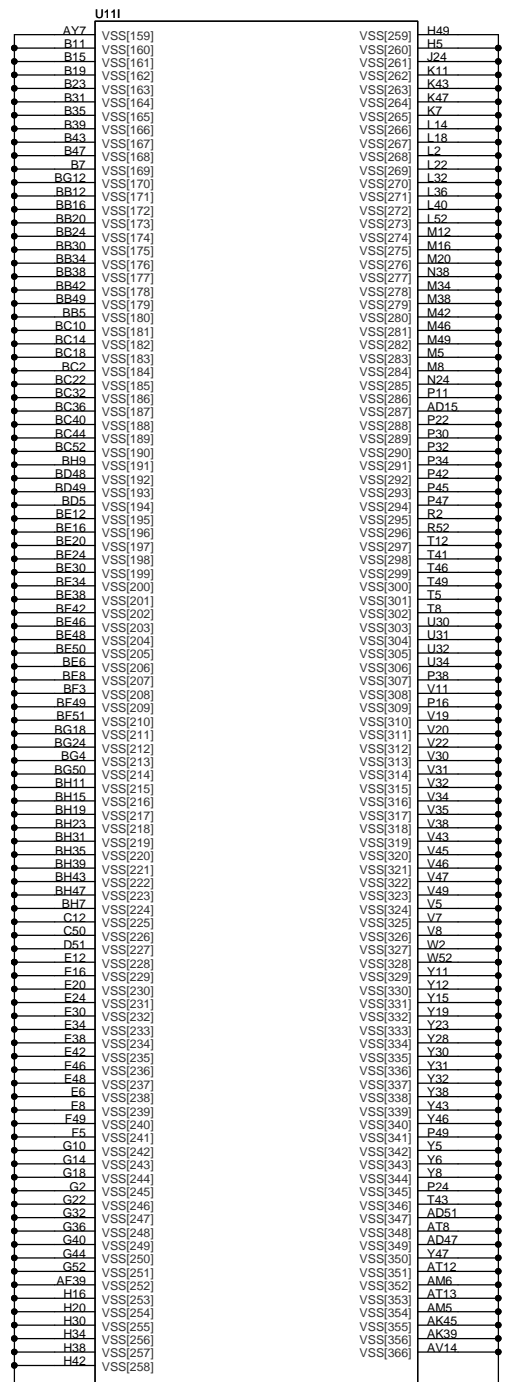
change cap to 10uF for cost

Remove HDA power rail to +1.5V

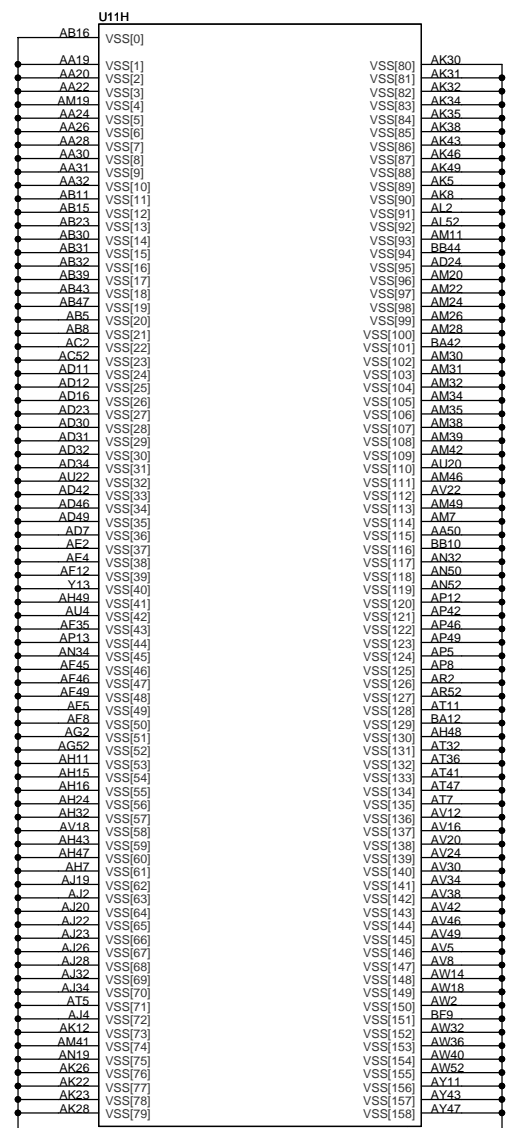
Remove VCCSUSHDA can be either 1.5V or 3.3V



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				Document Number	B
				Custom	4019AP
				Date:	Tuesday, December 28, 2010
				Sheet	30 of 52



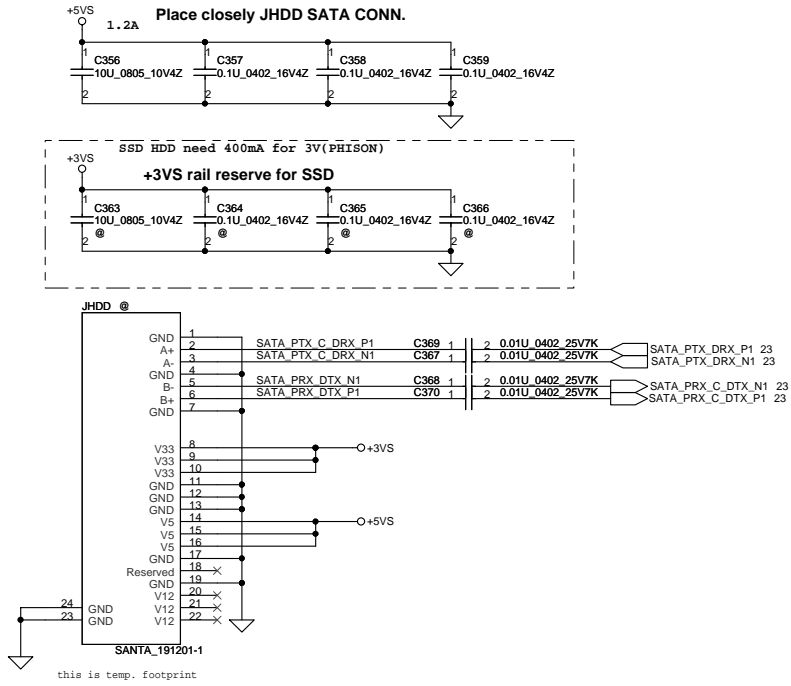
IBEXPEAK-M QV20 A0_FCBGA1071 HM55R1@



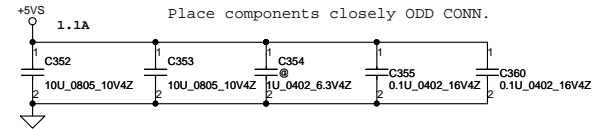
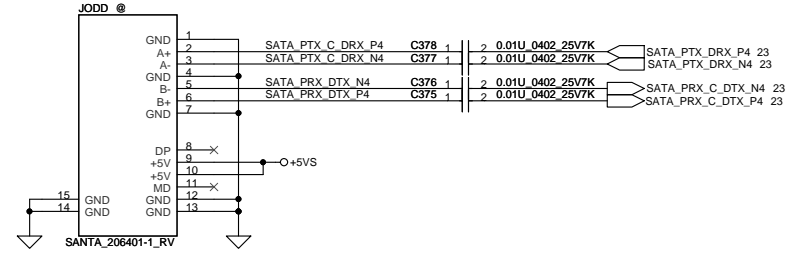
IBEXPEAK-M QV20 A0_FCBGA1071 HM55R1@

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Size	Document Number	Rev	B		
Custom	4019AP	Date:	Tuesday, December 28, 2010	Sheet	31 of 52

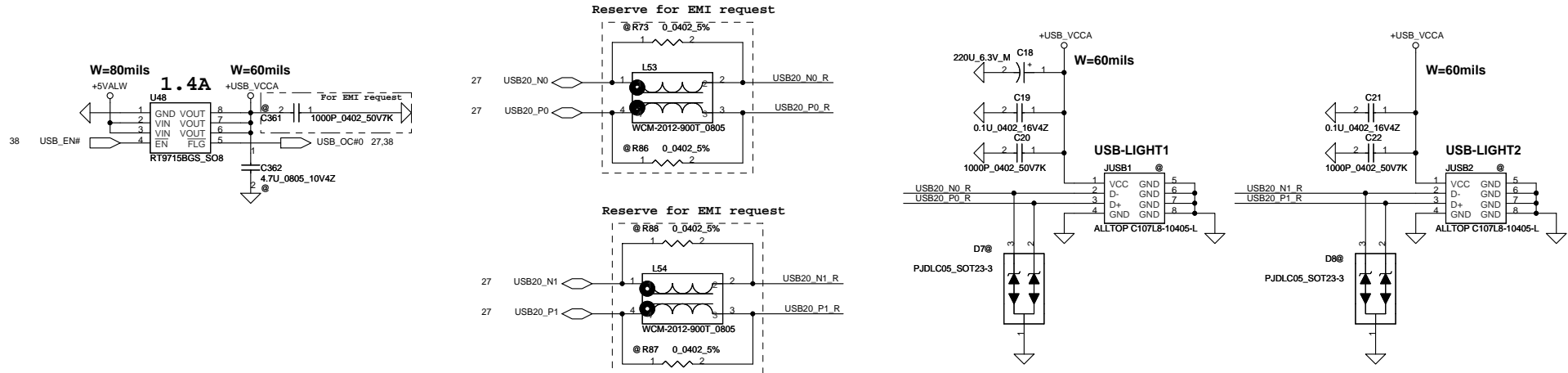
SATA HDD Conn.



SATA ODD Conn

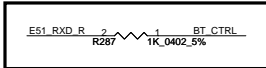
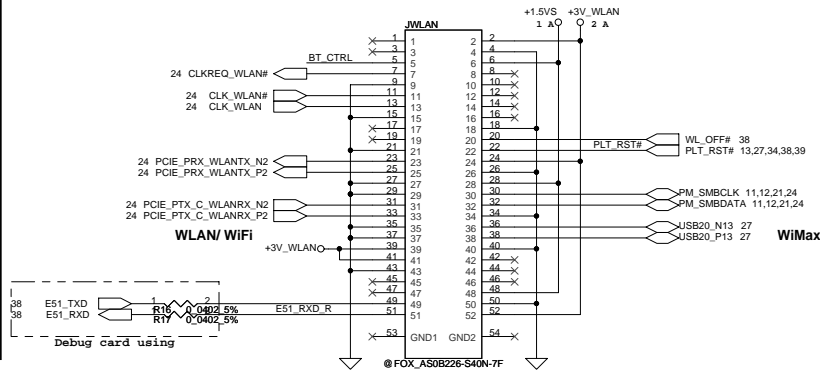
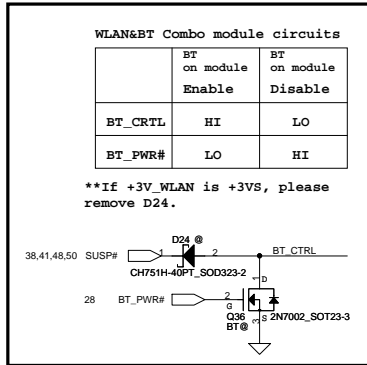


USB Conn. (2 Port)

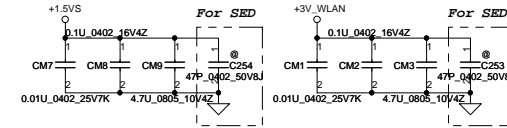
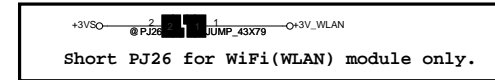


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				4019AP	Rev B
Date:				Tuesday, December 28, 2010	Sheet 32 of 52

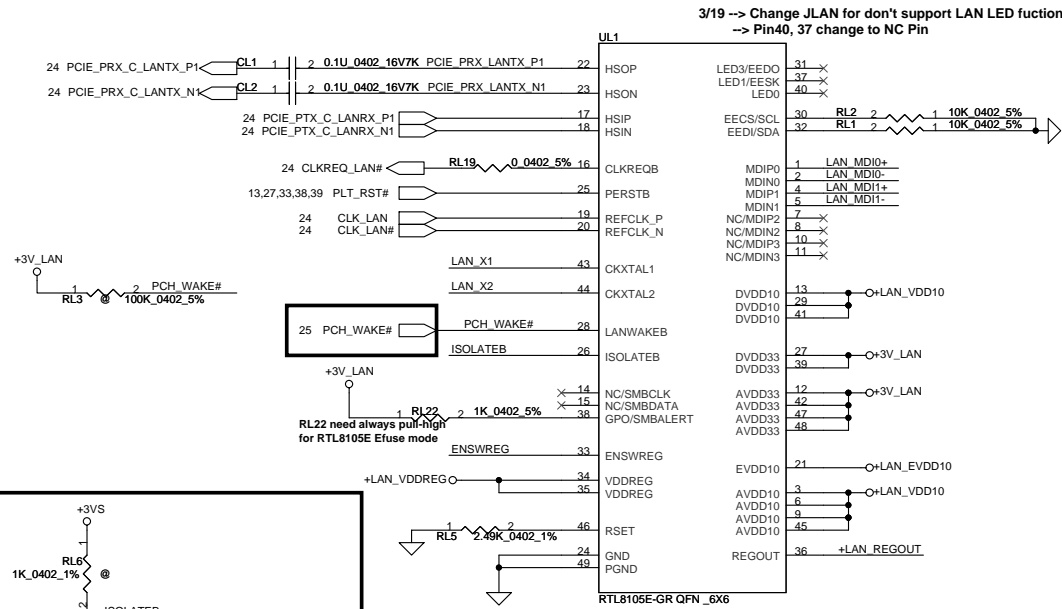
PCIe Mini Card-WLAN/WiMax



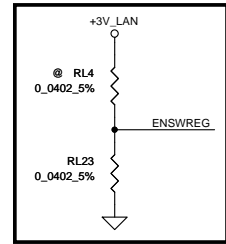
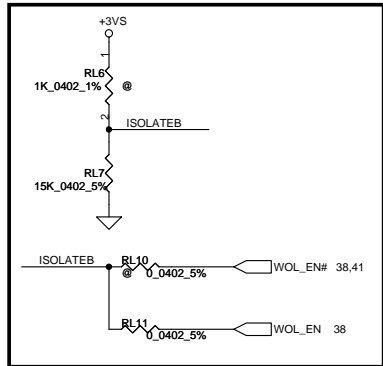
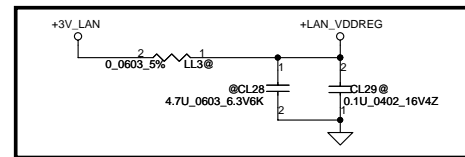
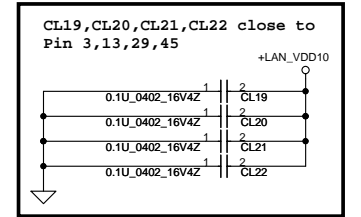
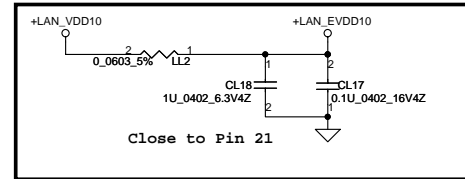
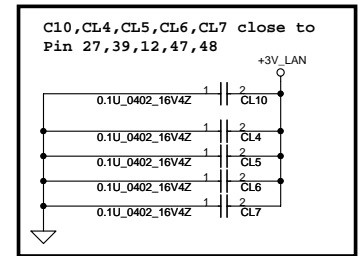
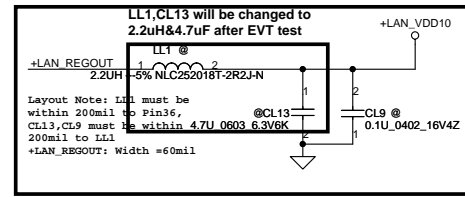
Slot#1 Half PCIe Mini Card-WLAN/WiMax



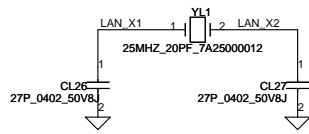
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			4019AP	Rev B
			Date: Tuesday, December 28, 2010	Sheet 33 of 52



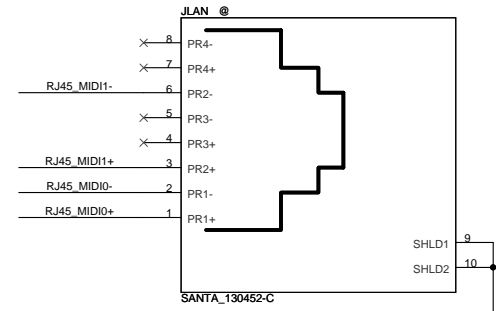
0715 --> LL1, CL13, CL9, LL3, CL28, CL29 are unmount for RTL8105E-VC



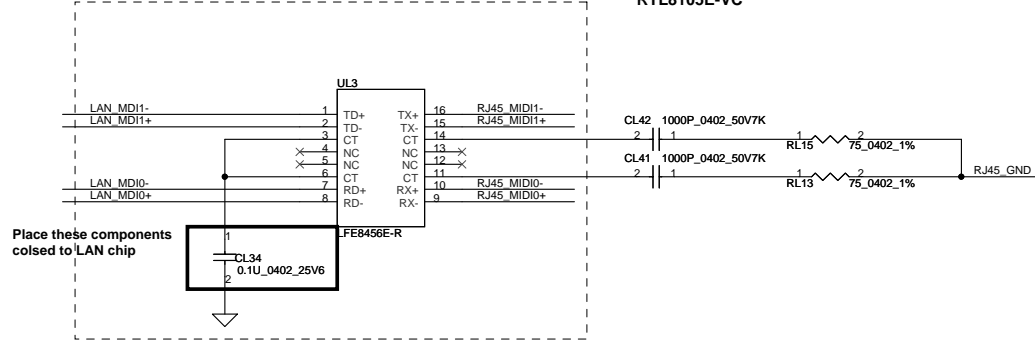
4/2-->remove RL8, RL9, CL11



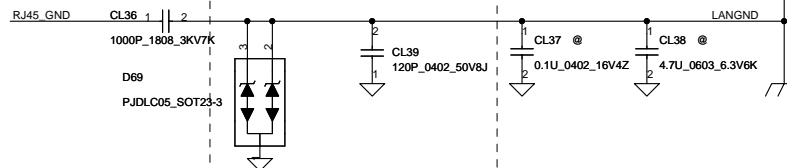
LAN Conn.

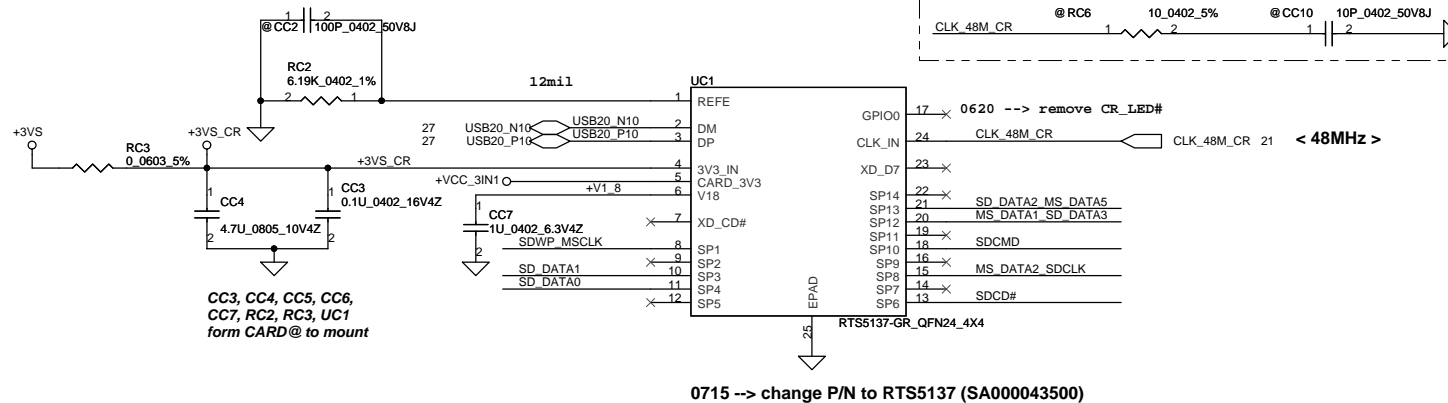


3/29 --> swap Line and PHY signal

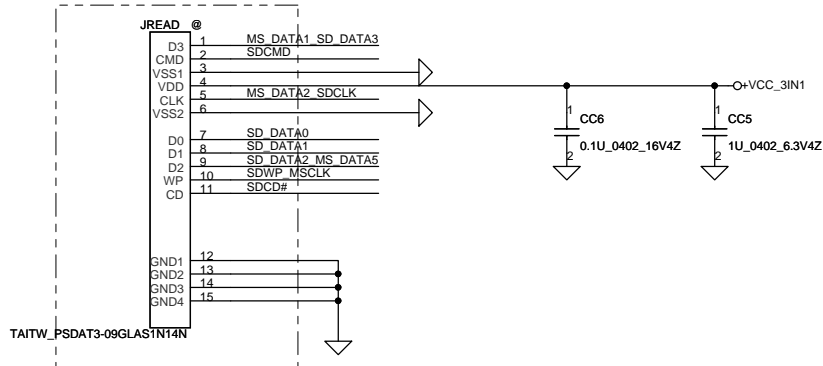


8/16-->Add CL39 for EMI request
Add D69 for ESD

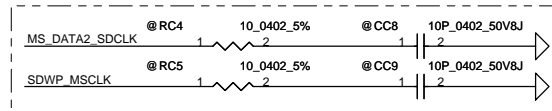




< 2 in 1 Card Reader >
0624 --> change CARDREADER conn.

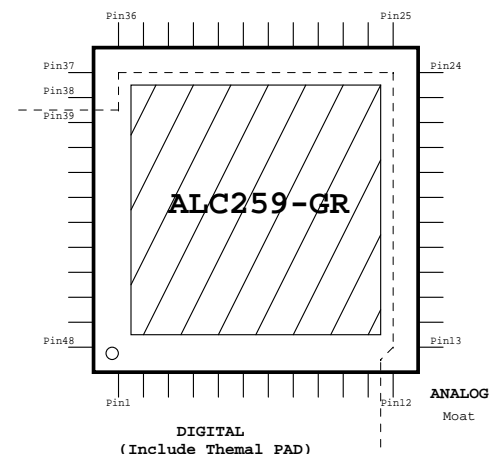
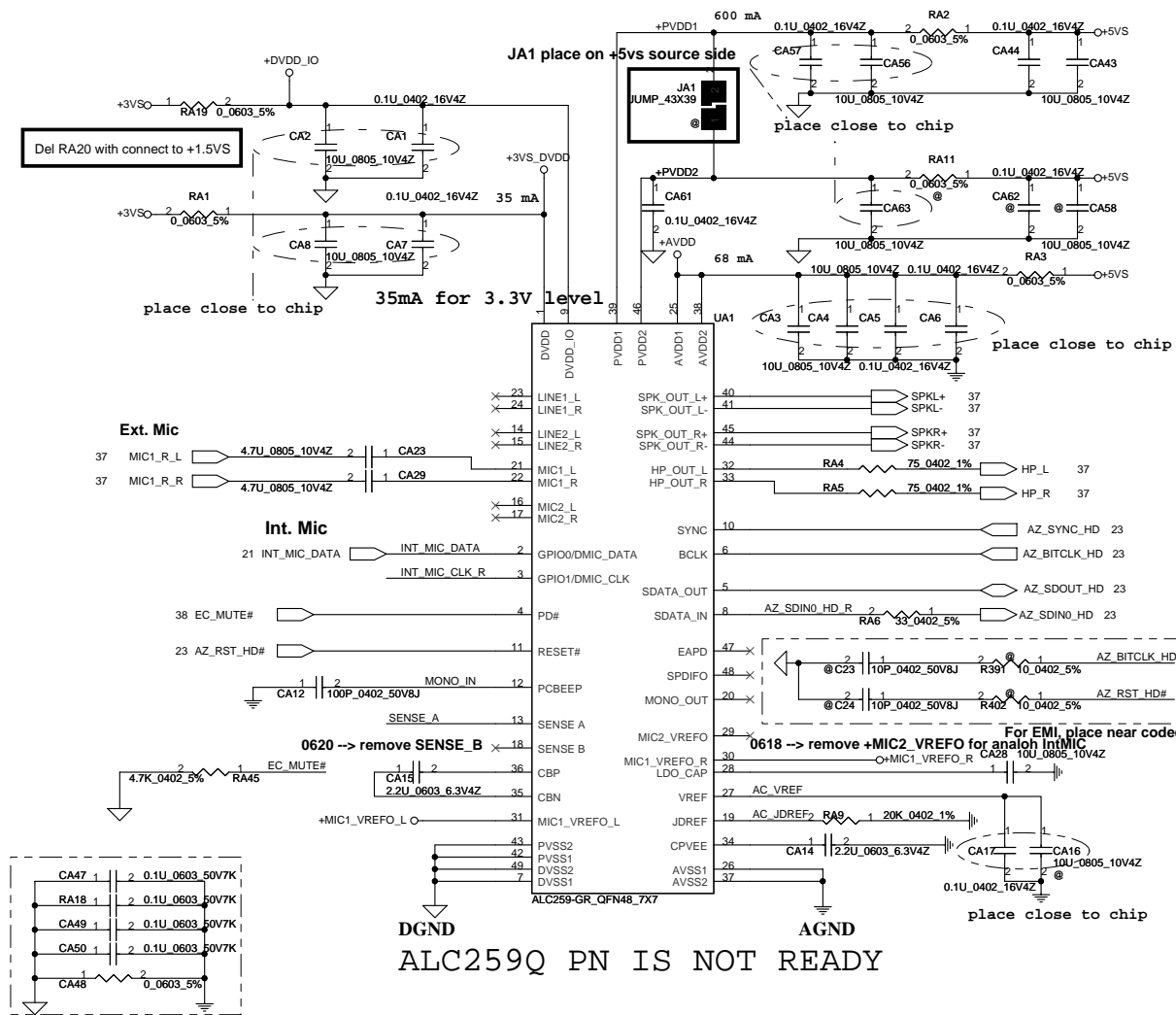


For EMI request

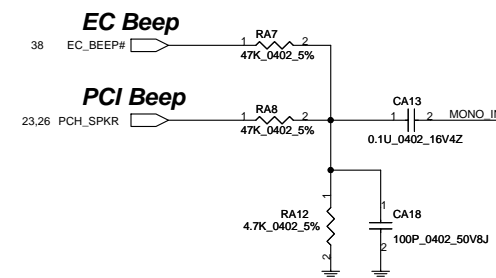


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				4019AP	
Date:		Tuesday, December 28, 2010		Sheet	35 of 52

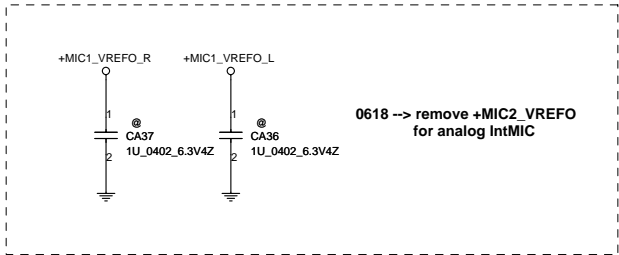
Codec



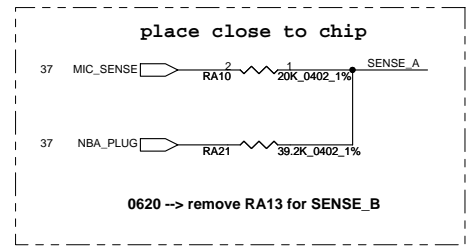
Beep sound



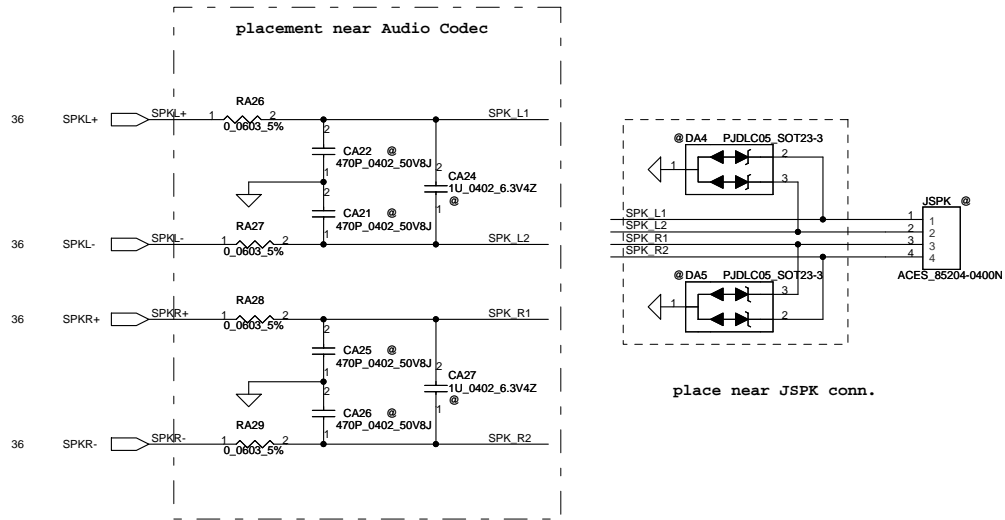
Place close to chip



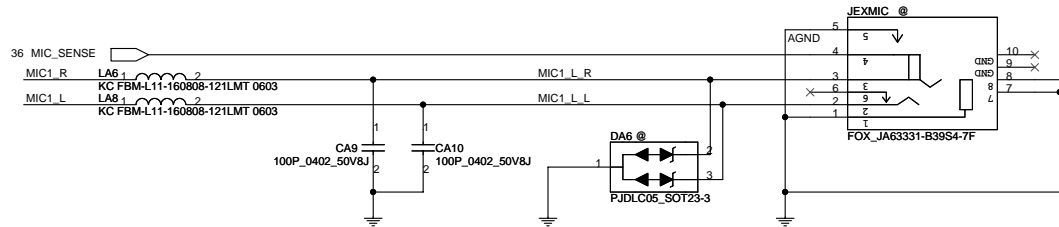
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
	39.2K	PORT-E (PIN 14, 15)	



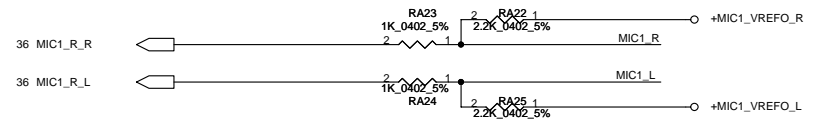
Speaker Connector



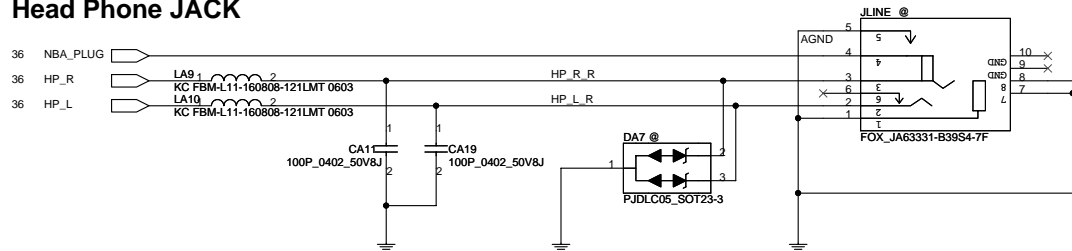
Ex.MIC JACK



Ext.MIC/LINE IN



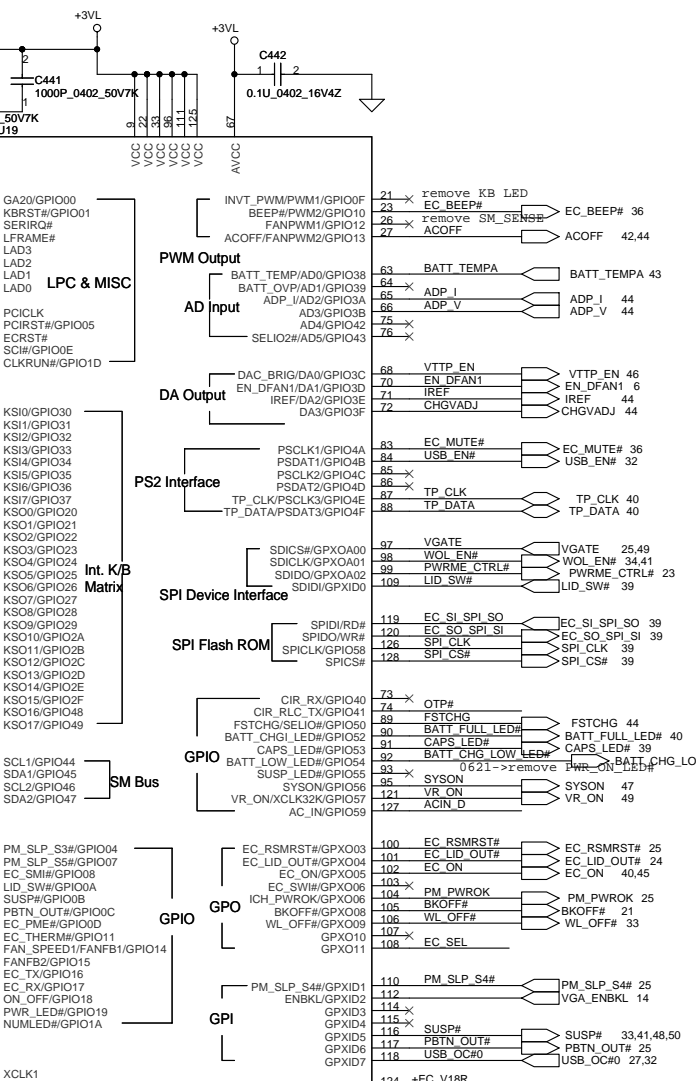
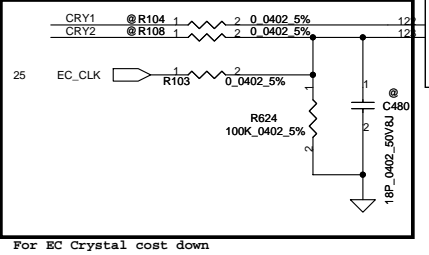
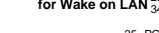
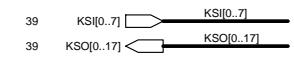
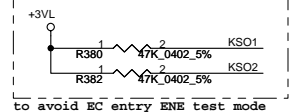
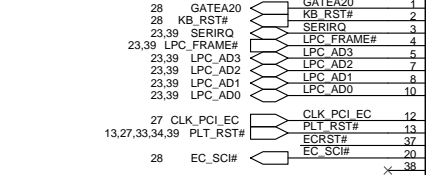
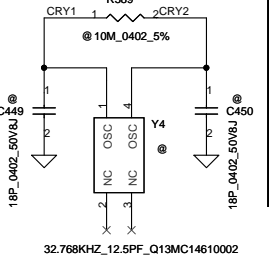
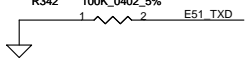
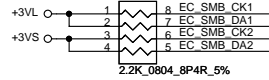
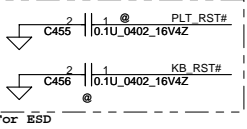
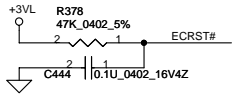
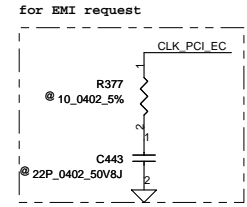
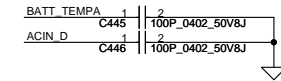
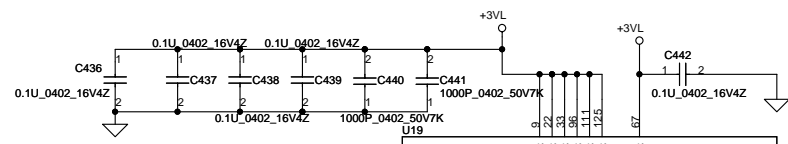
Head Phone JACK



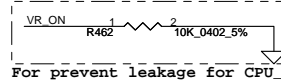
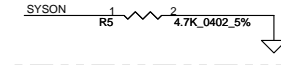
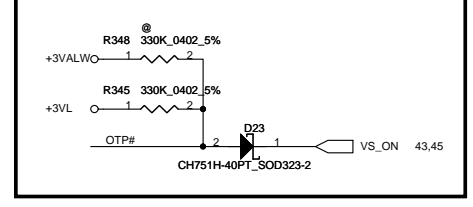
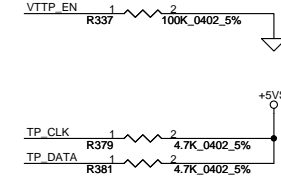
Int. Mic

0618 --> remove Analog IntMIC, and change to DIGITAL MIC

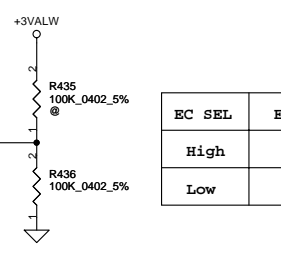
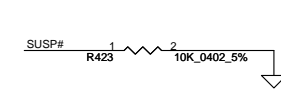
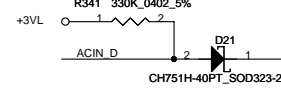
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Issued Date	2010/09/05	Deciphered Date	2011/09/05	SCHEMATICS,MB A6847
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				Rev B Sheet 37 of 52



Remove CEC_INT# pull high



For prevent leakage for CPU_CORE

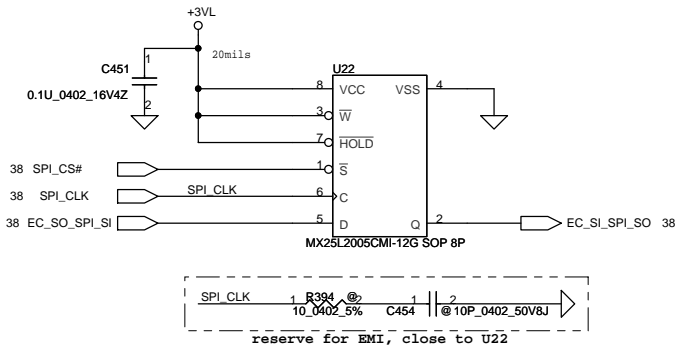


EC SEL	EC Version
High	KB926D3
Low	KB926E0

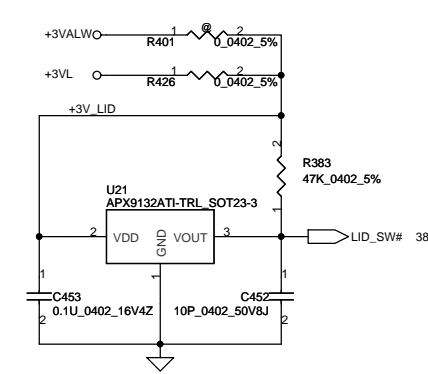
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Date: Tuesday, December 28, 2010				Sheet 38 of 52

Remove PM_SLP_S4#/S5# AND Gate

SPI Flash (256KB)

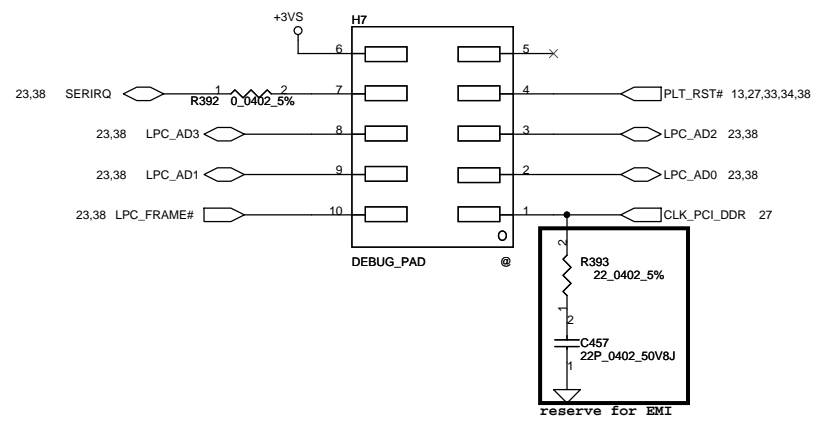


Lid SW

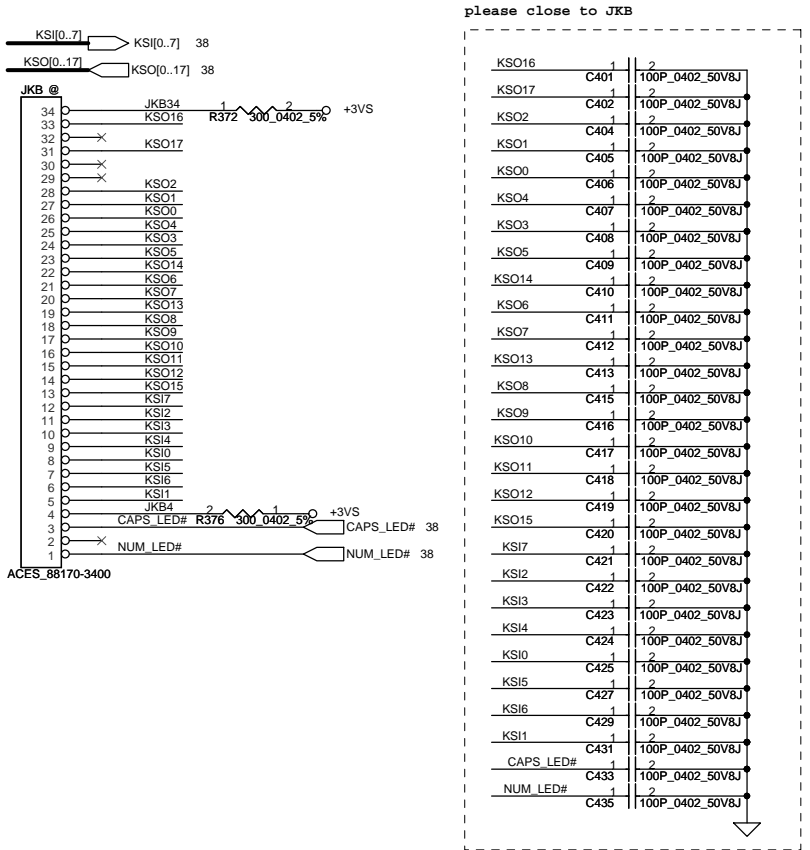


LPC Debug Port

Please place the PAD under DDR DIMM.

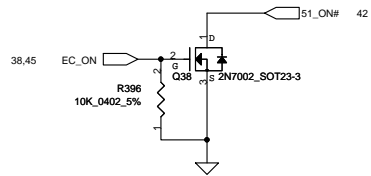
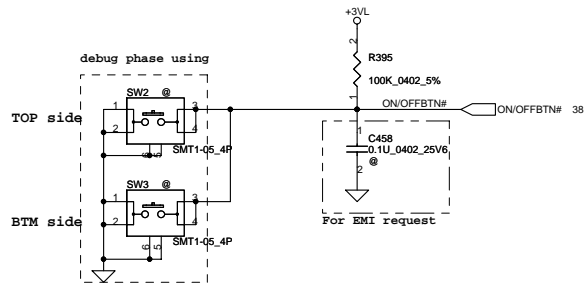


KEYBOARD CONN. Noticed: KB Connector Pin Definition Reversed with KB Membrane Pin Definition

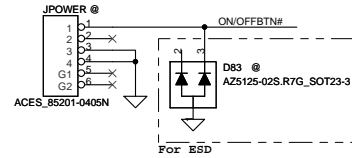


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Date:	Tuesday, December 28, 2010	Sheet	39	of 52

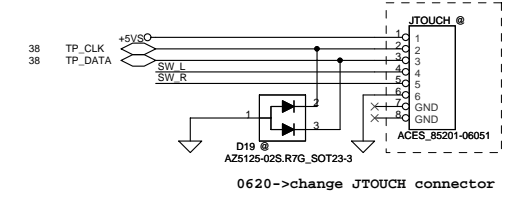
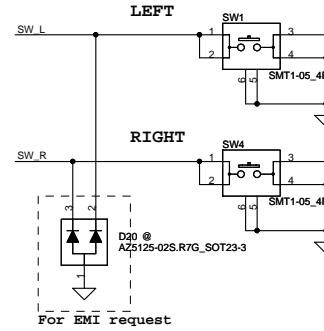
Power Button



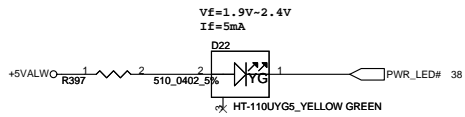
PWR/B to MB Conn.



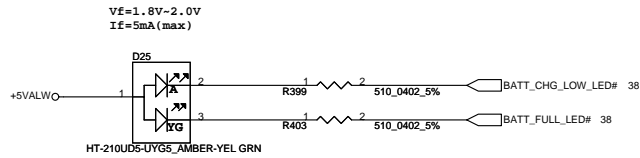
TP Button/Conn.



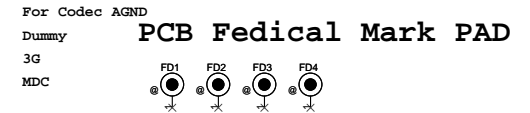
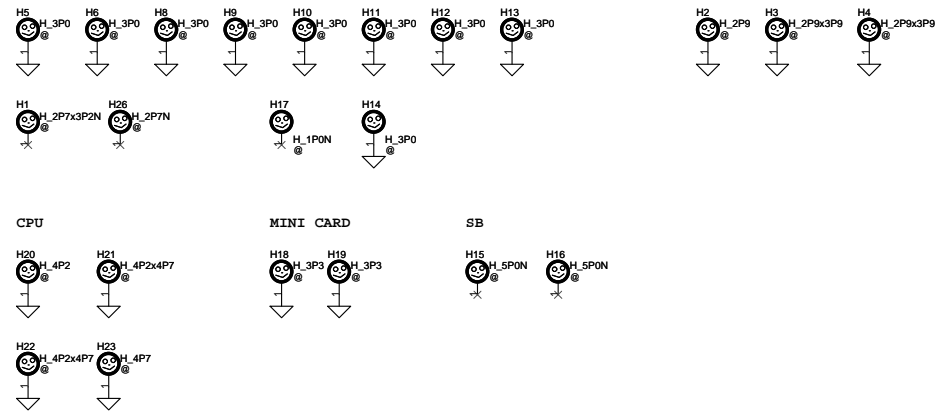
POWER/SUSPEND LED



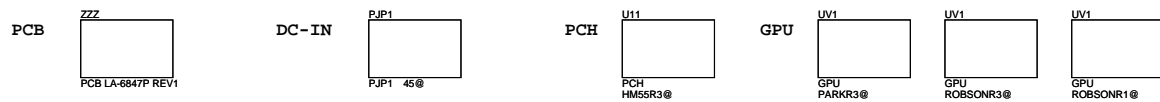
BATT CHARGE/FULL LED



Screw Hole

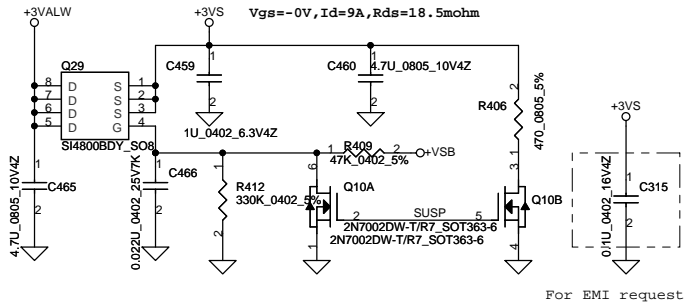


ISPD

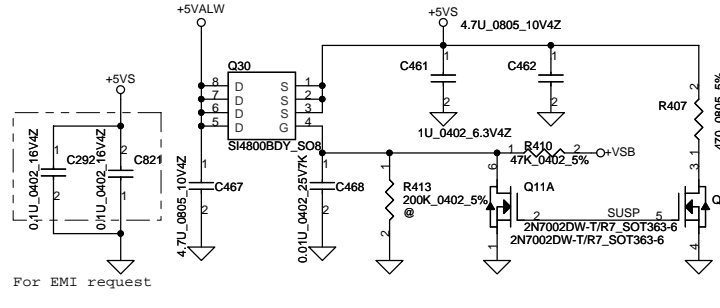


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Size	Document Number	Rev	B	
	4019AP			
Date:	Tuesday, December 28, 2010	Sheet	40	of 52

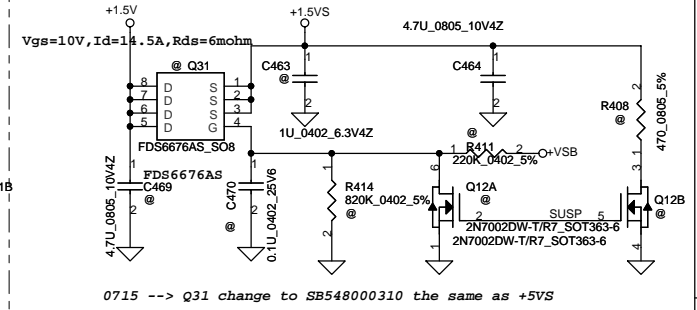
+3VALW TO +3VS



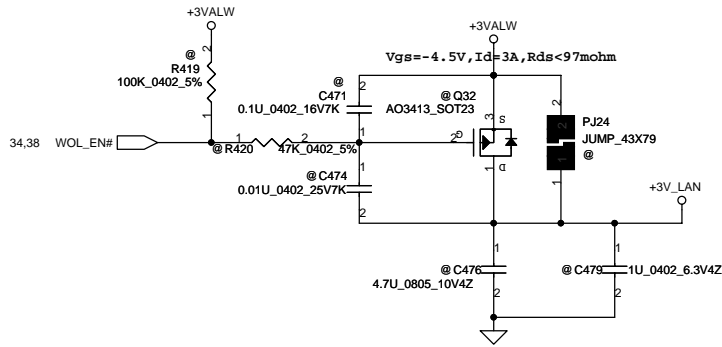
+5VALW TO +5VS



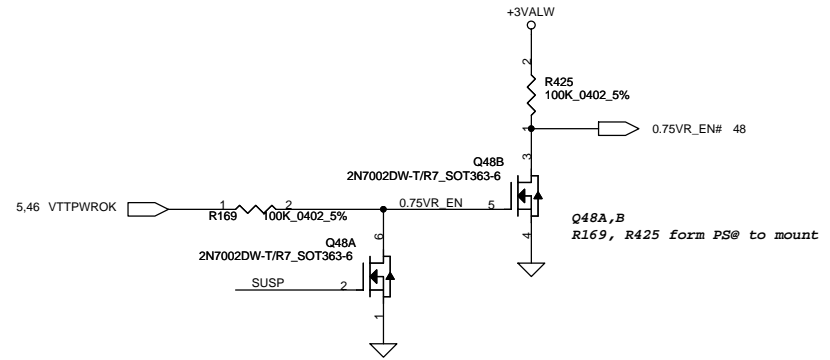
+1.5V to +1.5VS Combine with +1.5V_CPU



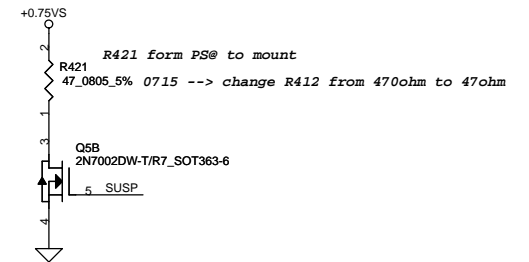
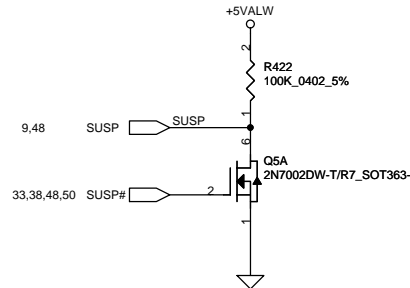
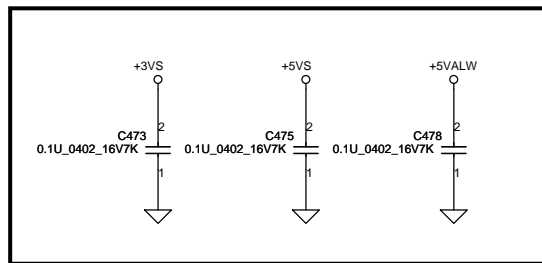
+3VALW TO +3V_LAN



For S3 CPU Power Saving

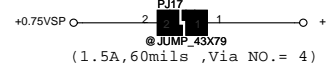
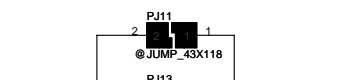
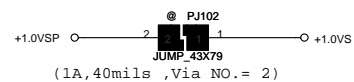
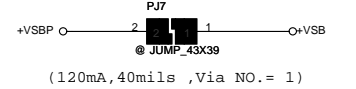
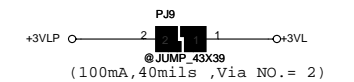
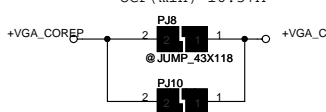
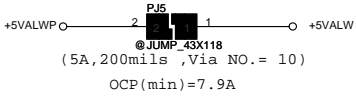
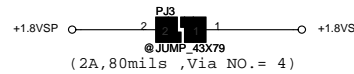
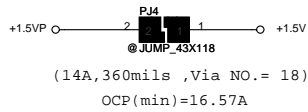
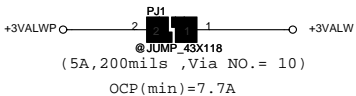
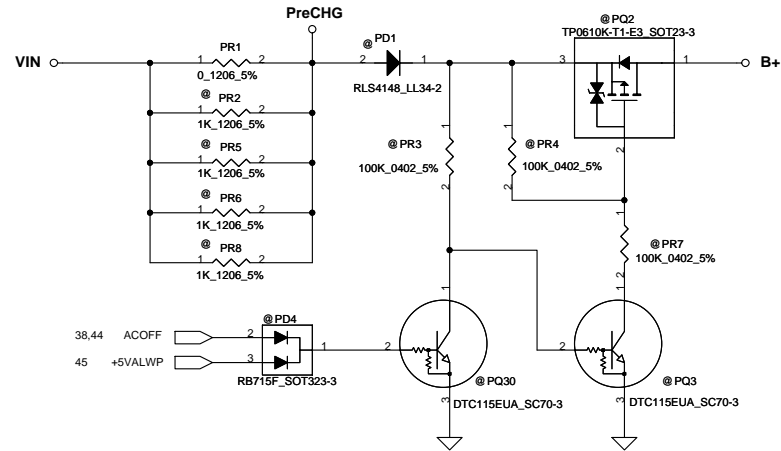
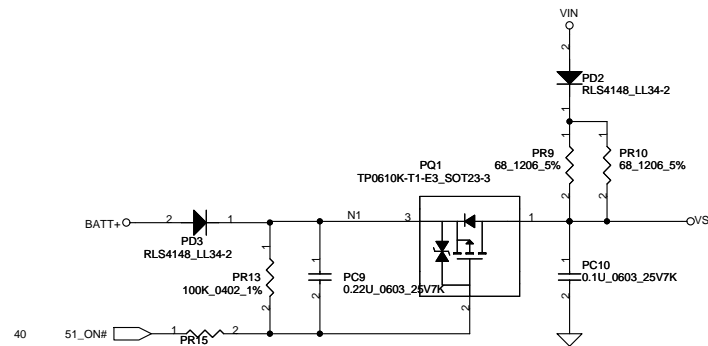
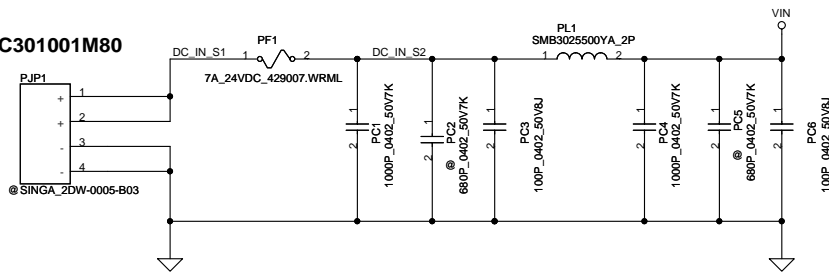


Reserve for EMI test

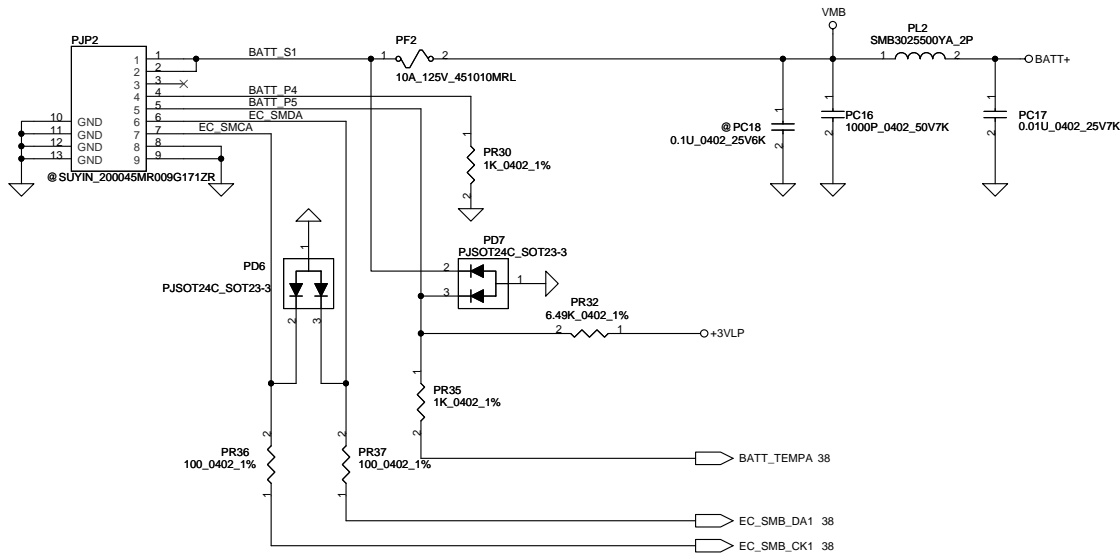


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				4019AP	B
Date: Tuesday, December 28, 2010				Sheet	41 of 52

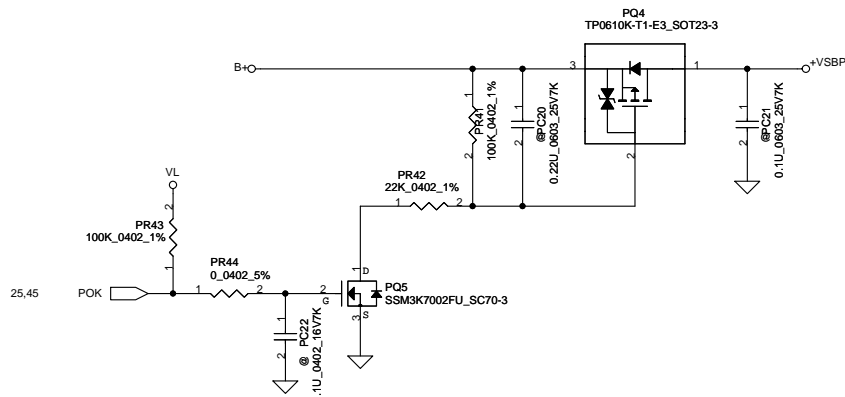
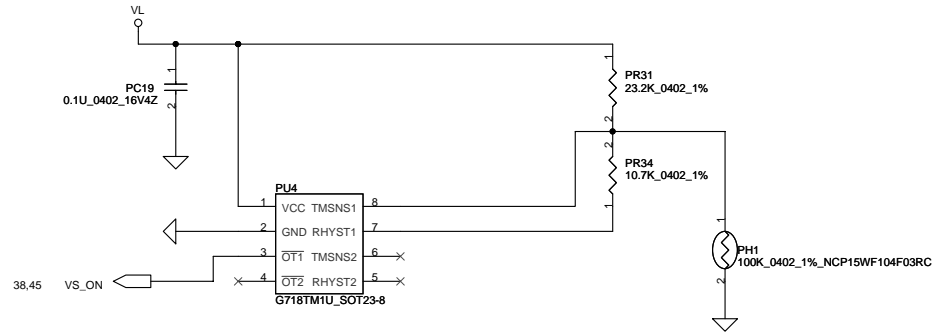
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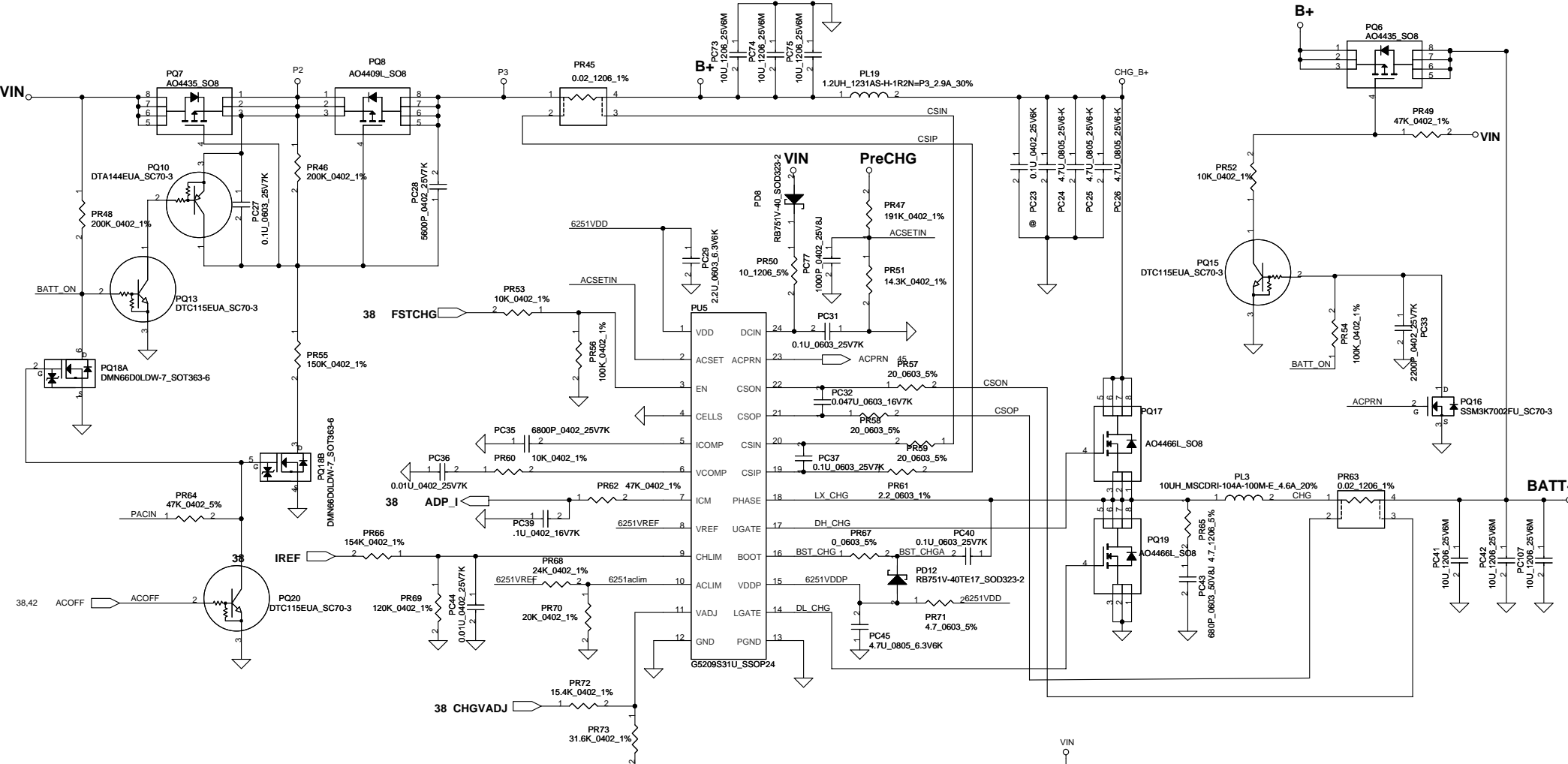
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				4019AP
				Rev B
Date: Tuesday, December 28, 2010				Sheet 42 of 52



PH1 under CPU botten side :
 CPU thermal protection at 90degree C
 Recovery at 56 degree C



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				4019AP	B
				Date: Tuesday, December 28, 2010	Sheet 43 of 52

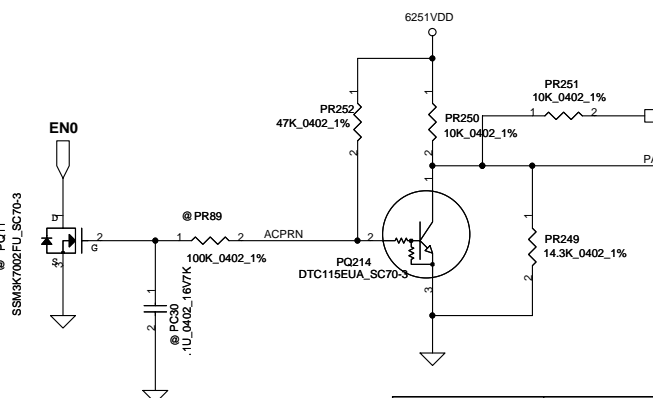


CP mode
 $I_{ada} = 0 - 3.42A (65W)$ $CP = 92\% \cdot I_{ada}$; $CP = 3.147A$
 $V_{ac1im} = 1.08V (65W)$ $PR68 = 75k$ $PR45 = 0.02$

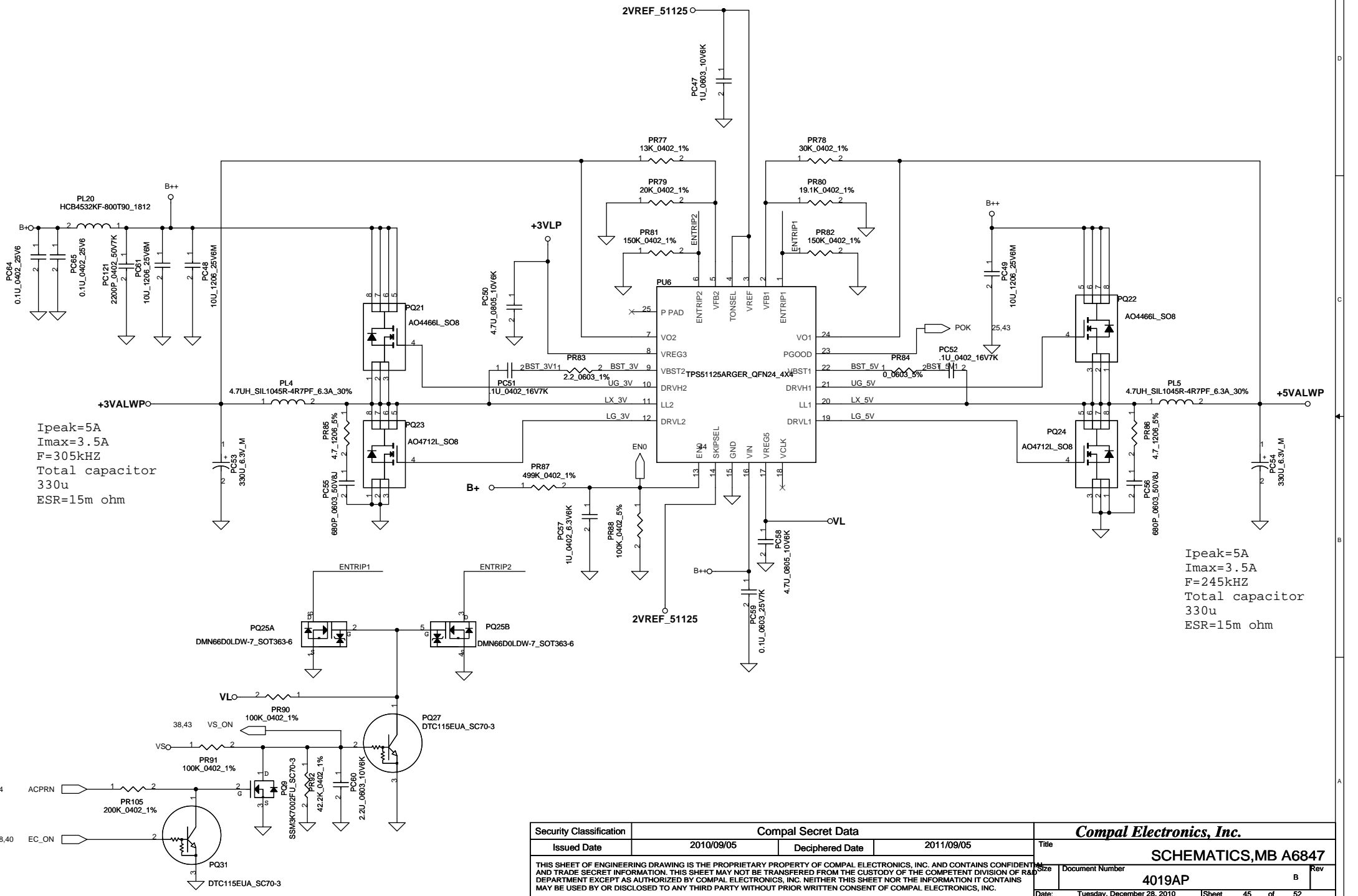
$CC = 0.25A - 3A$
 $I_{REF} = 1.016 \cdot I_{charge}$
 $I_{REF} = 0.254V - 3.048V$
 V_{CHLIM} need over 95mV

$CHGVADJ = (V_{cell} - 4) / 0.10627$	
V _{cell}	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

Vin Detector
 High 18.089V
 Low 17.44V



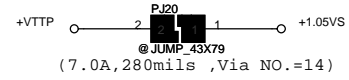
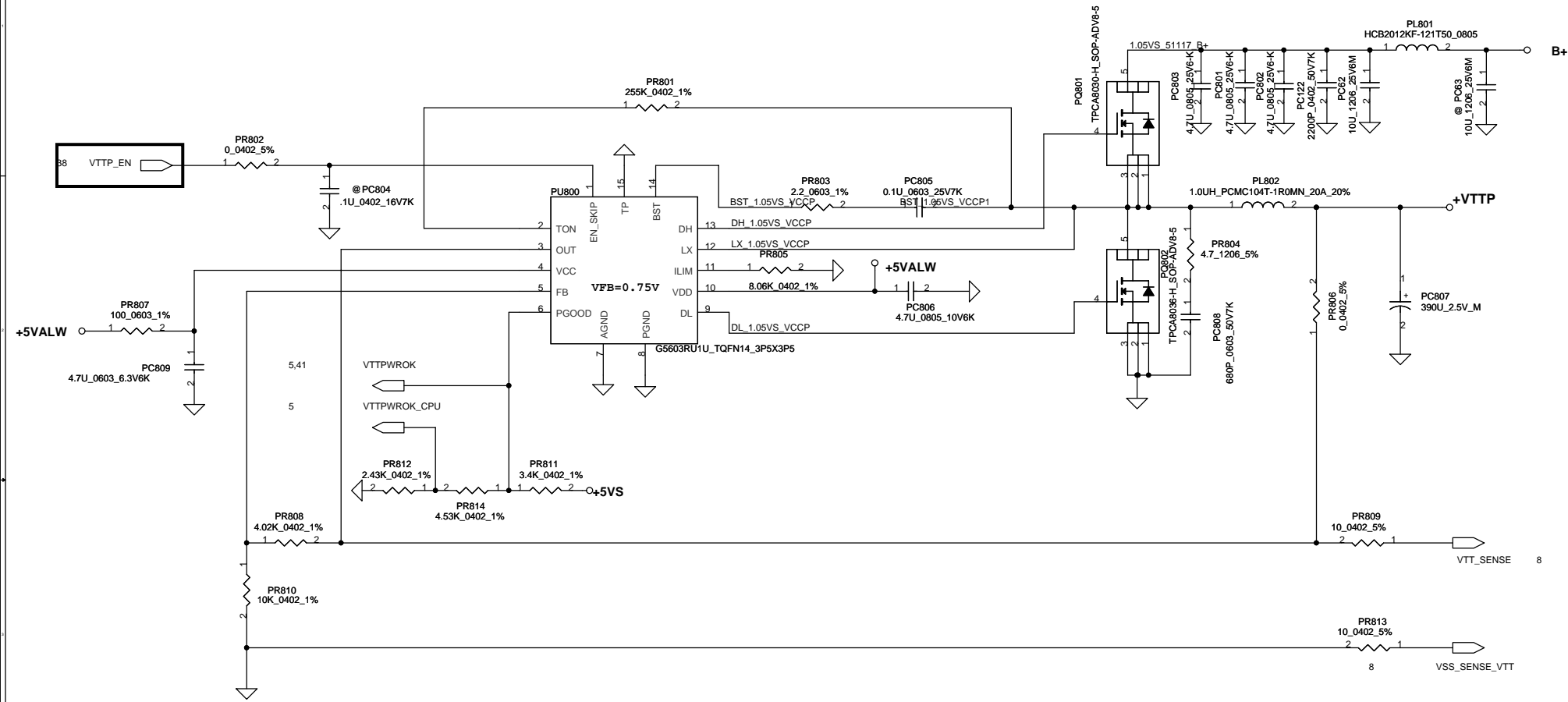
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				4019AP	B
				Date: Tuesday, December 28, 2010	Sheet 44 of 52



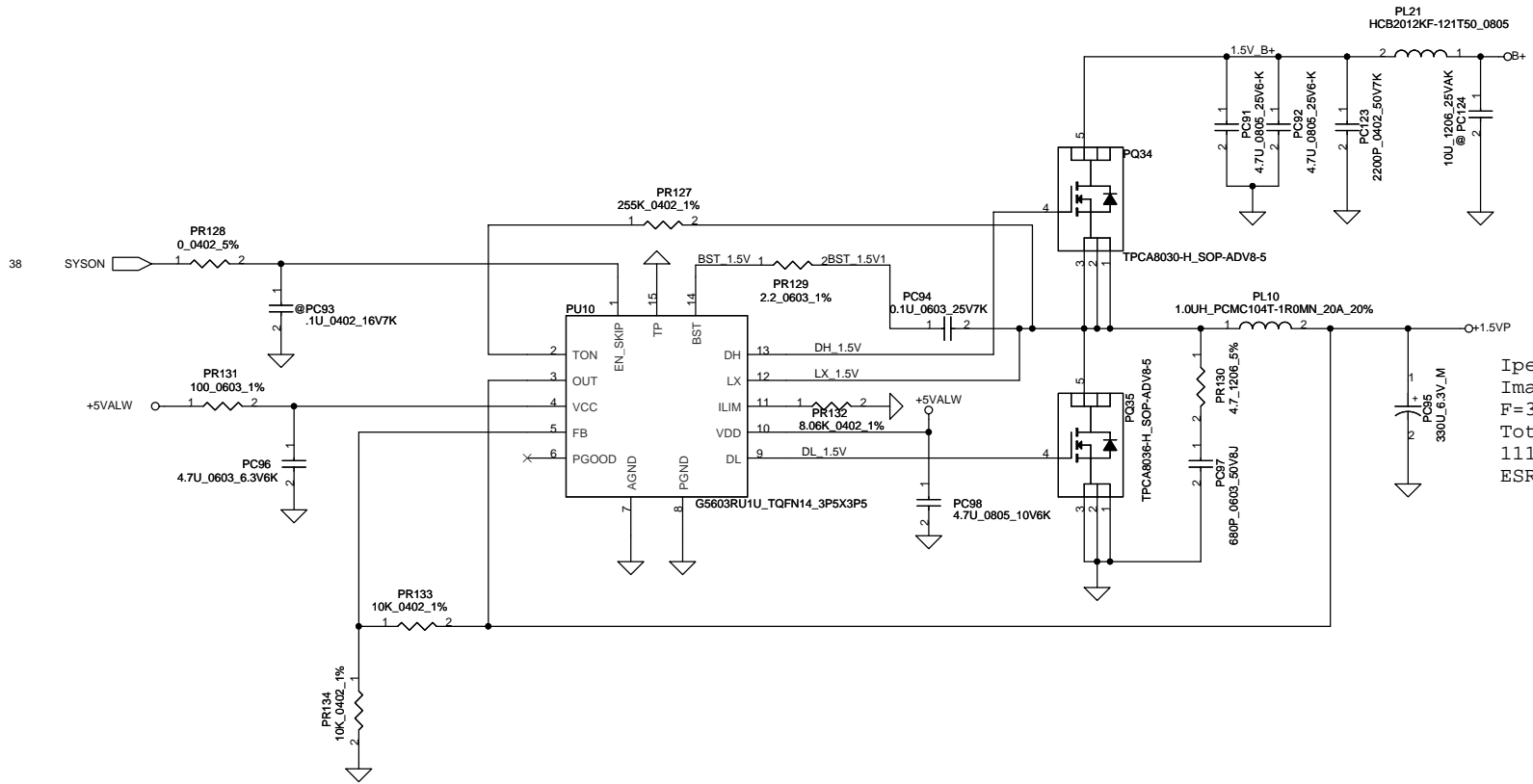
$I_{peak}=5A$
 $I_{max}=3.5A$
 $F=305kHz$
 Total capacitor
 330u
 ESR=15m ohm

$I_{peak}=5A$
 $I_{max}=3.5A$
 $F=245kHz$
 Total capacitor
 330u
 ESR=15m ohm

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				4019AP	B
Date:		Tuesday, December 28, 2010		Sheet	45 of 52

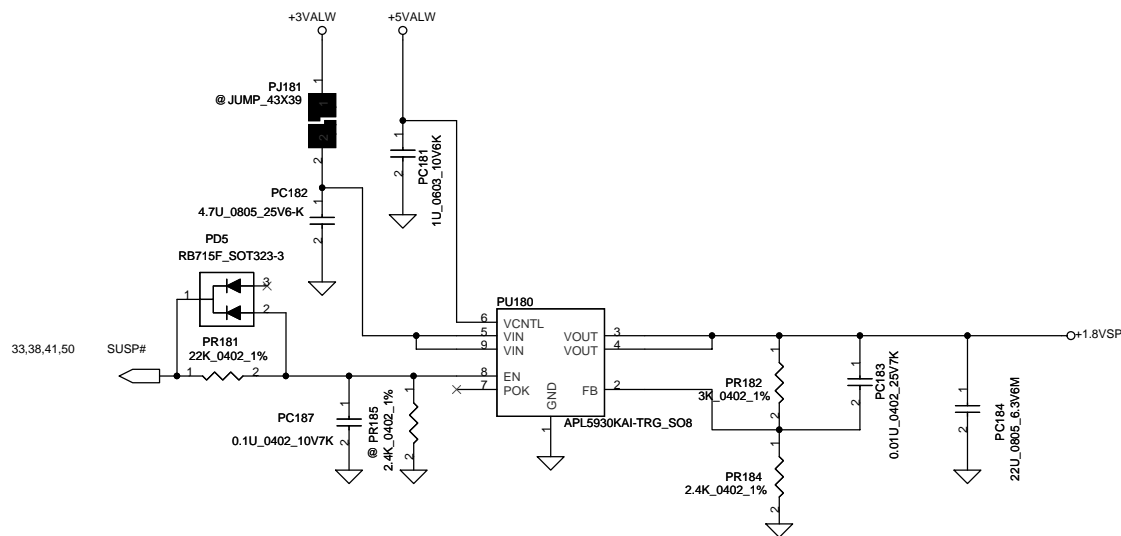
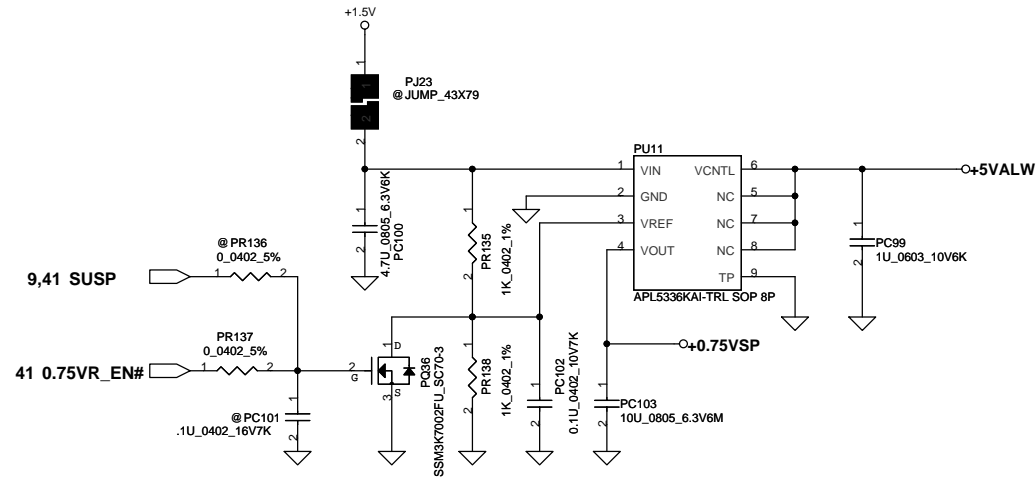


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Document Number	4019AP	Rev	B	
Date:	Tuesday, December 28, 2010	Sheet	46	of 52

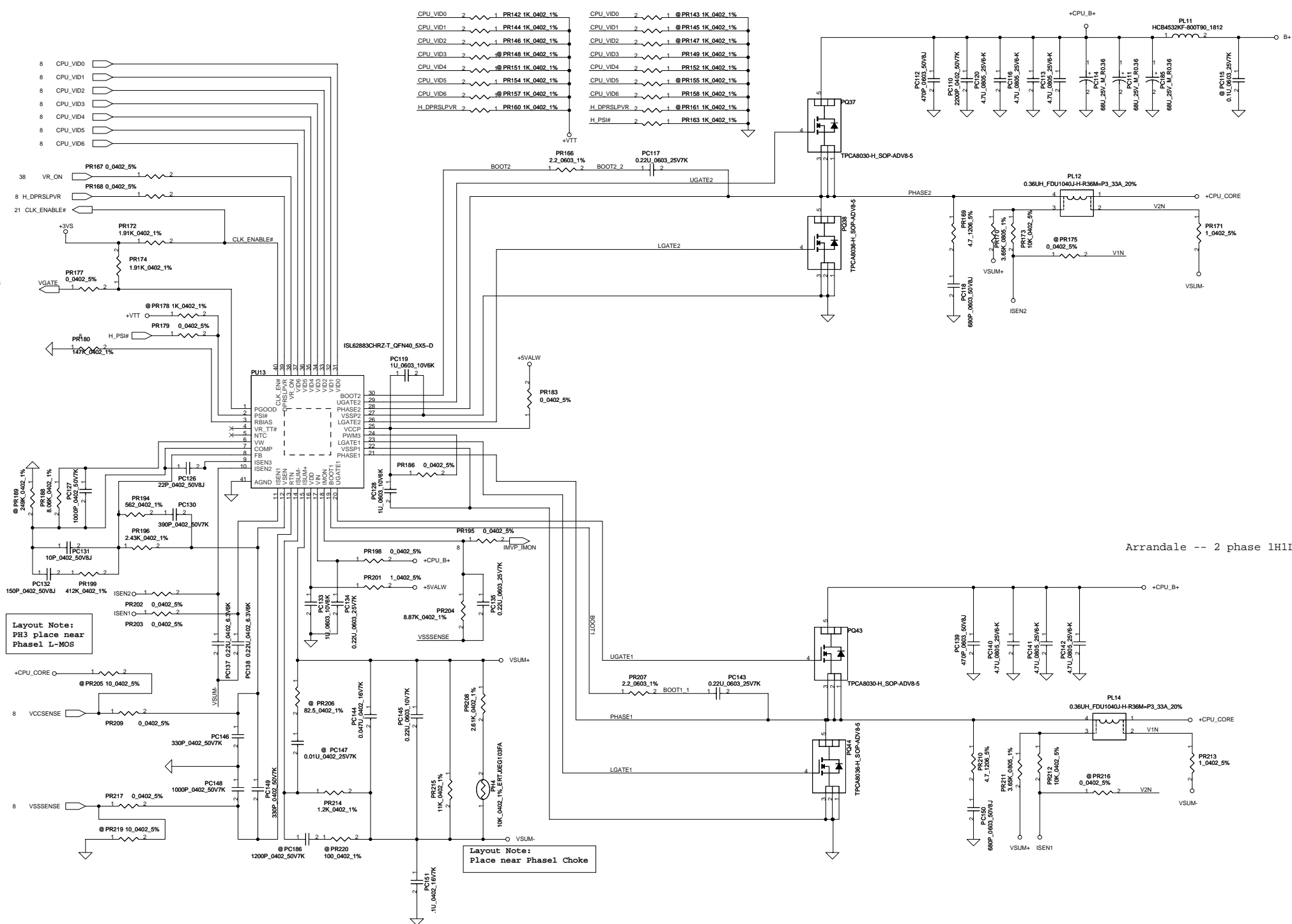


Ipeak=14A
 Imax=9.8A
 F=313kHz
 Total capacitor
 1110u
 ESR=5m ohm

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				Date:	Tuesday, December 28, 2010
				Sheet	47 of 52



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				4019AP	
				Date:	Tuesday, December 28, 2010
				Sheet	48 of 52
				Rev	B

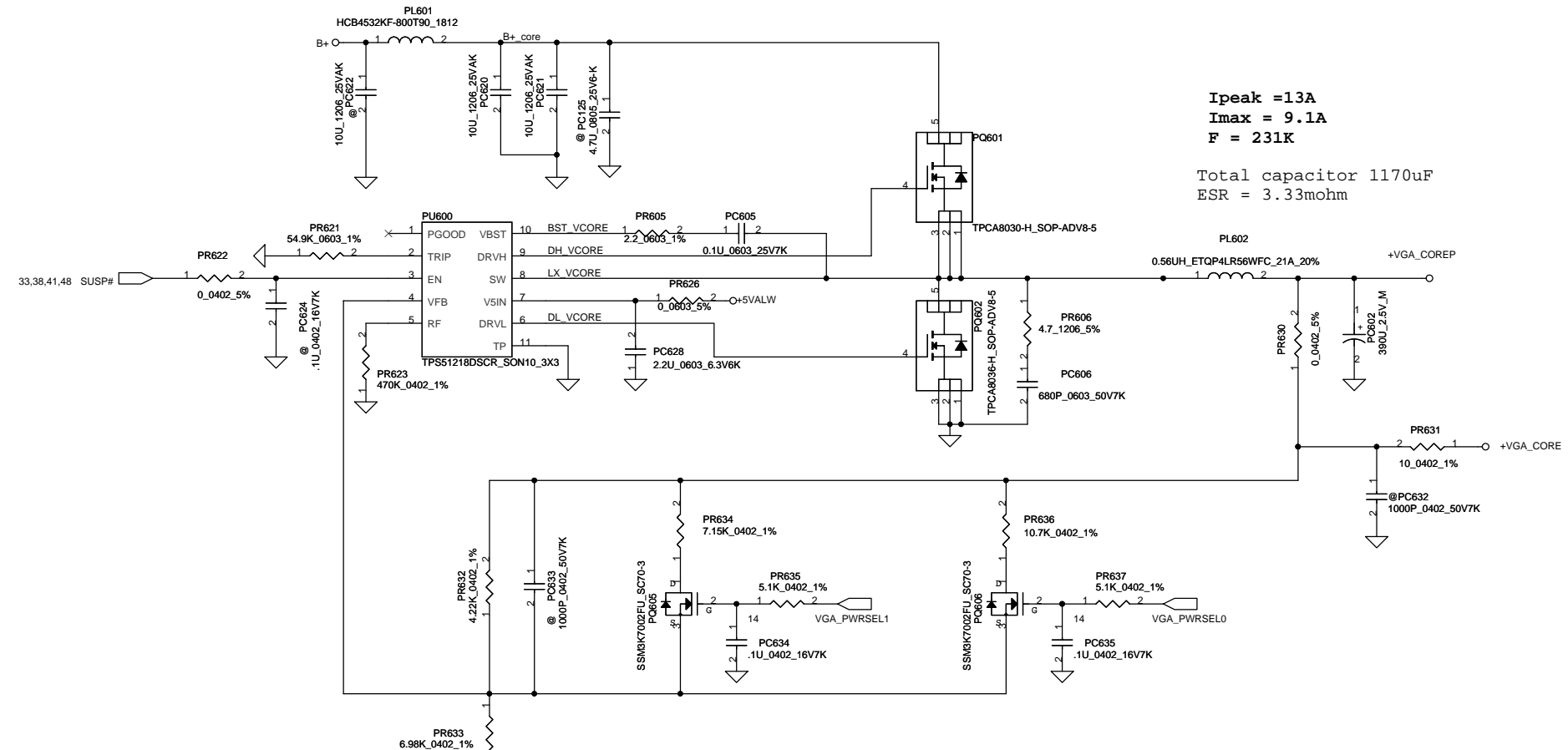


Arrandale -- 2 phase 1H1L

Layout Note:
PH3 place near
Phasel L-MOS

Layout Note:
Place near Phasel Choke

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Size	Document Number	4019AP		Date
C		Tuesday, December 28, 2010		Sheet 49 of 52



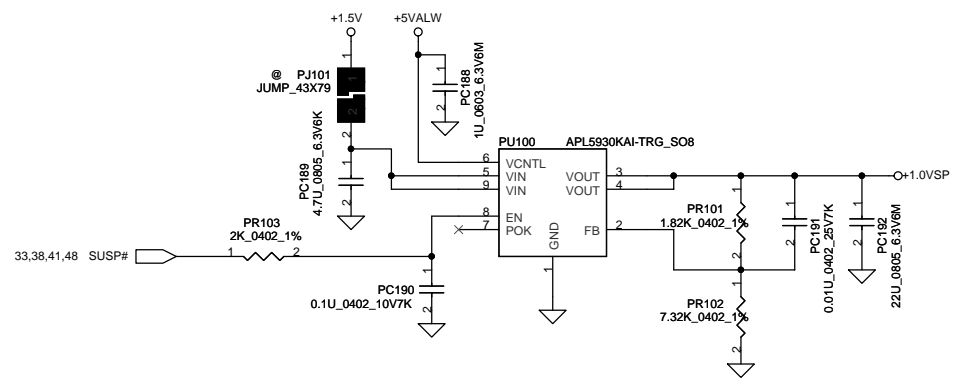
Ipeak = 13A
 Imax = 9.1A
 F = 231K

Total capacitor 1170uF
 ESR = 3.33mohm

Rtrip = 27K, OCP = 24.49A
 Rrf = 470K, FSW = 290KHz

VFB(0.6) = Vout * Rbottom / (Rtop + Rbottom)

SEL1	SEL0	Robson LP	Park XT
L	L		1.12
L	H		
H	L	0.95	
H	H	0.9	0.9



NO DATE	PAGE	MODIFICATION LIST	PURPOSE
2010/10/14	42	Remove PR2,PR3,PR4,PR5,PR6,PR7,PR8,PD1,PD4,PQ2,PQ3,PQ30 Change PR1 to 0_1206_5%	Remove Pre charge
2010/10/14	44	Change PQ8 to AO4409L,remove PR89,PC30,PQ11 Change PR68 to 24K ohm,add PC107	Remove Pre charge
2010/10/14	45	Change PU6 to TPS51125A	Circuit modify
2010/10/14	46	Change PQ802 to TPCA8036	Circuit modify
2010/10/14	48	Change PU11 to APL5336,PR181 to 15K ohm, add PC187(0.22U)	Circuit modify
2010/10/14	50	Change PR621 to 54.9k ohm,Delete PR104,PC622 Add PR606,PC606	Circuit modify
2010/10/21	45	Add PC64(0.1U_0402_25V)	EMI request
2010/10/21	48	Change PR181 to 22k ohm,PC187 to 0.1UF,add PD5	HW request
2010/10/21	50	Change PR605 to 2.2 ohm,PR635,PR637 to 5.1Kohm,PR103 to 2Kohm Add PC190	HW request

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				Document Number
Date:	Tuesday, December 28, 2010	Sheet	51	of 52

PIR (Product Improve Record)

PWWAA LA-6847P SCHEMATIC CHANGE LIST
 REVISION CHANGE: 0.1 TO 1.0

NO DATE PAGE MODIFICATION LIST PURPOSE

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				Rev B
Date: Tuesday, December 28, 2010			Sheet 52 of 52	