

COMPAL CONFIDENTIAL

MODEL NAME : *NCL00 NCL10(ATG)*

PCB NO : *LA-5471P (DA80000G710)*

E2 Rothschild UMA

rPGA Arrandale +
FCBGA PCH IBEXPEAK-M

2010-1-20

REV : 1.0(A00)

@ : Nopop Component

MB Type	BOM P/N	PCMCIA	Express	TCM		TPM				ATG	BOM CONFIG
		1@	2@	W(3@)	W/O(4@)	W(5@)	W/O(6@)	7@	8@	9@	
PCMCIA CARD EN,TPM EN,TCM DIS	43177931L11	*			*	*					1@,4@,5@
EXPRESS CARD EN,TPM EN,TCM DIS	43177931L14		*		*	*					2@,4@,5@
PCMCIA CARD EN,TCM EN,TPM DIS	43177931L12	*		*			*				1@,3@,6@
EXPRESS CARD EN,TCM EN,TPM DIS	43177931L15		*	*			*				2@,3@,6@
PCMCIA CARD EN,ALL TPM DISABLE	43177931L13	*			*		*				1@,4@,6@
EXPRESS CARD EN,ALL TPM DISABLE	43177931L16		*		*		*				2@,4@,6@
PCMCIA CARD EN,TPM EN,TCM DIS	43177931L01	*			*	*				*	1@,4@,5@,9@
PCMCIA CARD EN,TCM EN,TPM DIS	43177931L02	*		*			*			*	1@,3@,6@,9@
PCMCIA CARD EN,ALL TPM DISABLE	43177931L03	*			*		*			*	1@,4@,6@,9@

MB PCB	
Part Number	Description
DA80000G700	PCB 0AY LA-5471P REV0 M/B UMA

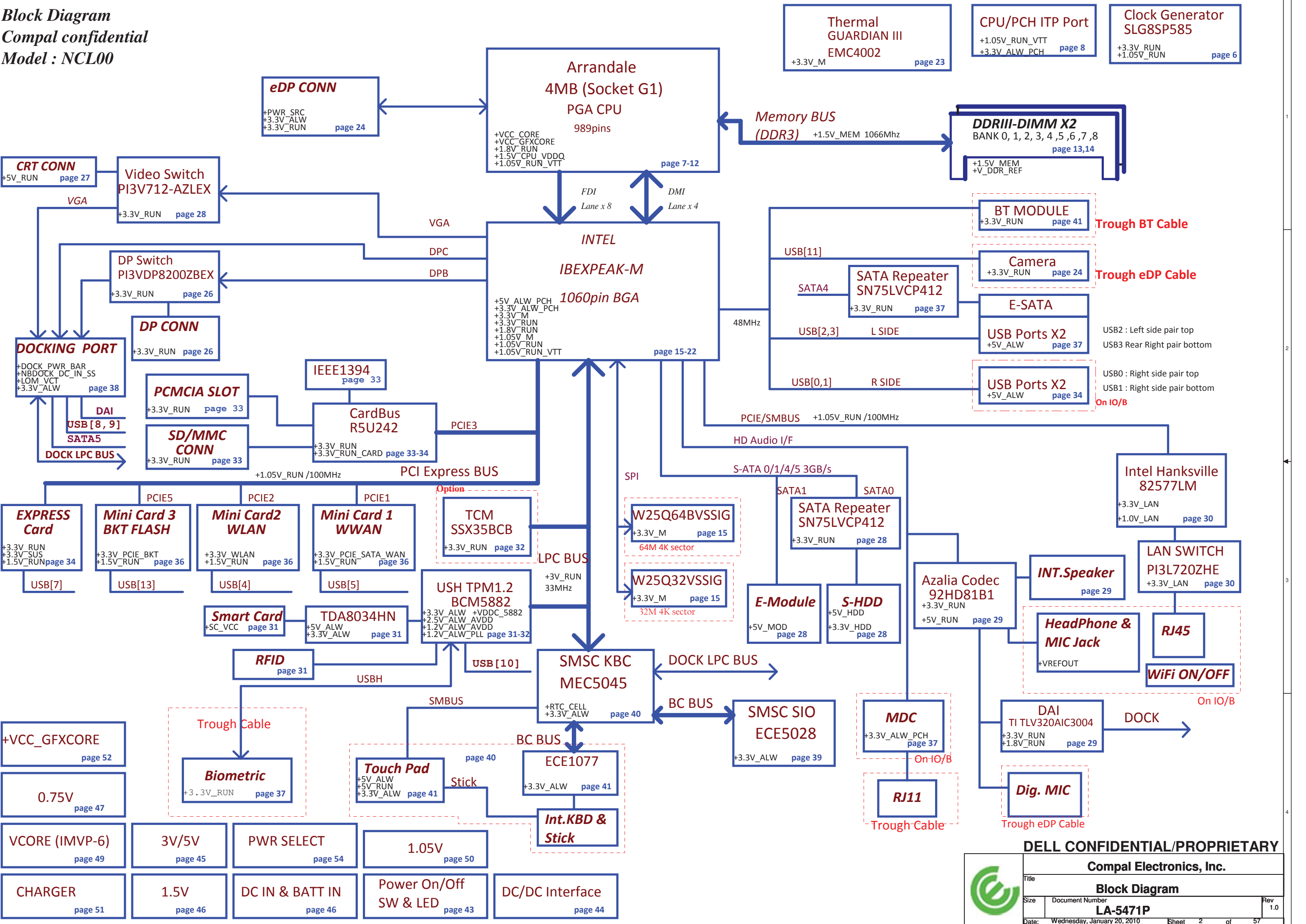
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Block Diagram
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Model : NCL00



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		Block Diagram	
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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

PCH	USB PORT#	DESTINATION
	0	JUSB1 (Ext Right Side Top)
	1	JUSB1 (Ext Right Side Bottom)
	2	JESA1 (Ext Left Side Top)
	3	JESA1 (Ext Left Side Bottom)
	4	WLAN
	5	WWAN
	6	Bluetooth
	7	USH->BIO
	8	DOCKING
	9	DOCKING
	10	Express card
	11	Camera
12	none	
13	JMINI3(PCIE/BKT CARD)	

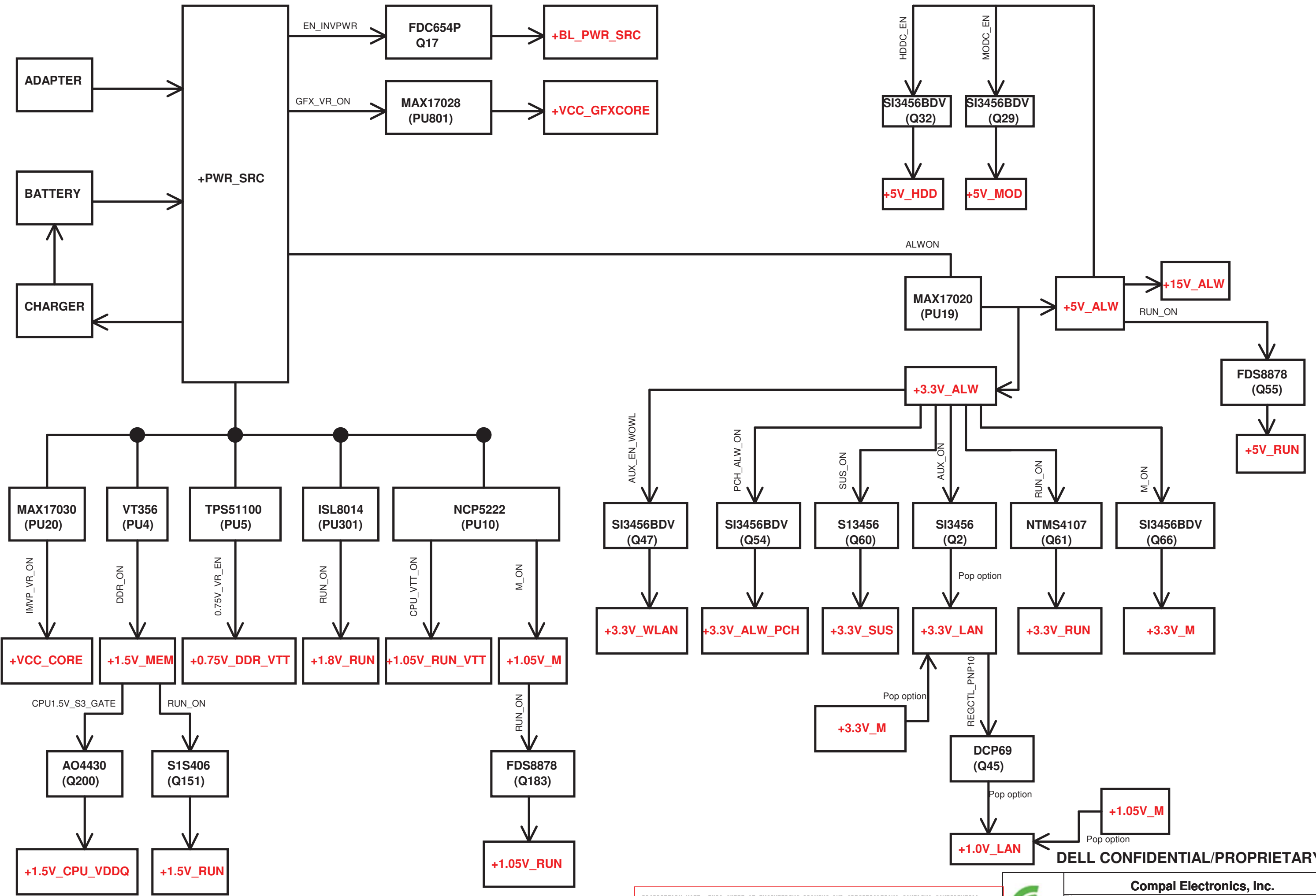
PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	PCMCIA
Lane 4	EXPRESS CARD
Lane 5	MINI CARD-3 PCIE/BKT
Lane 6	10/100/1G LAN
Lane 7	None
Lane 8	None

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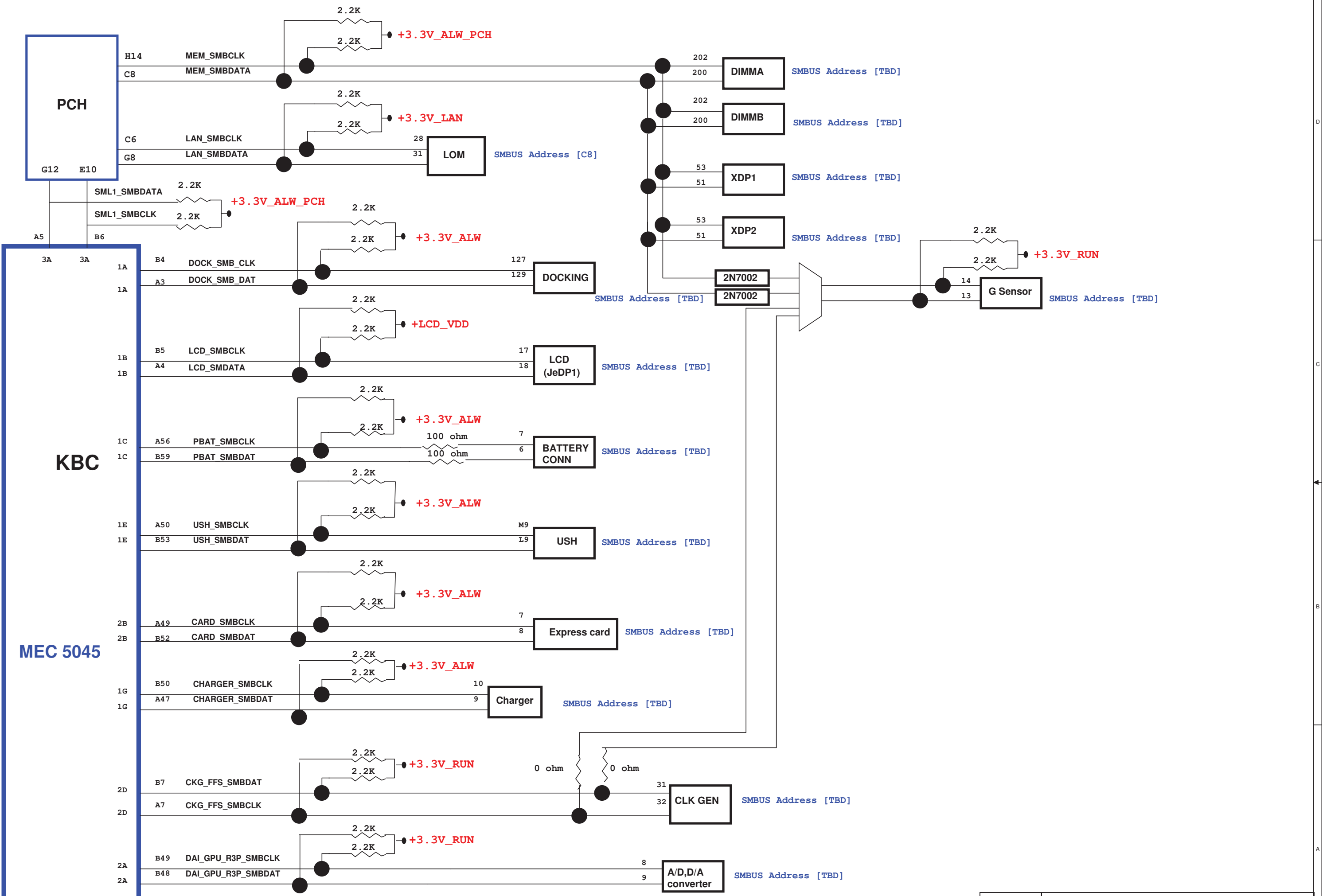


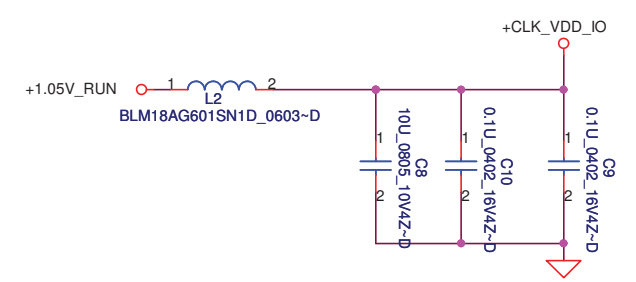
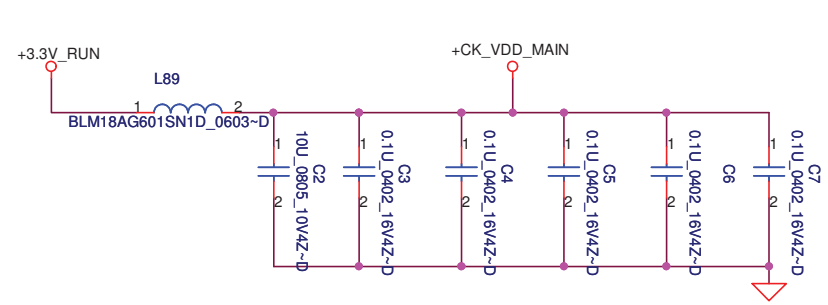
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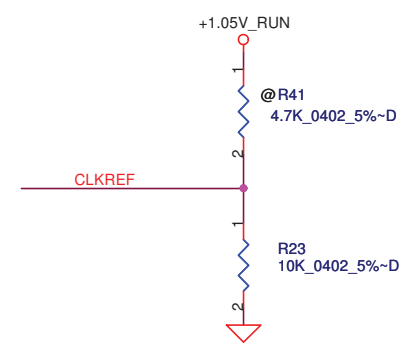
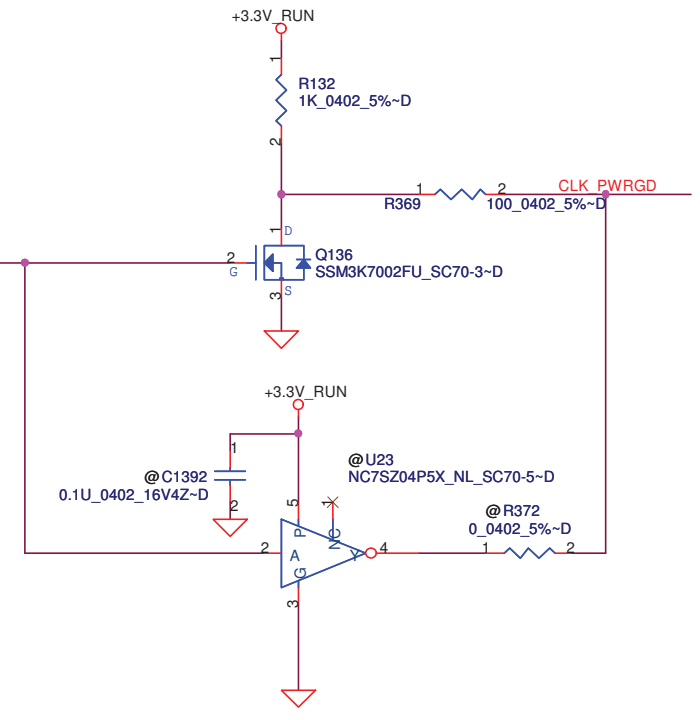
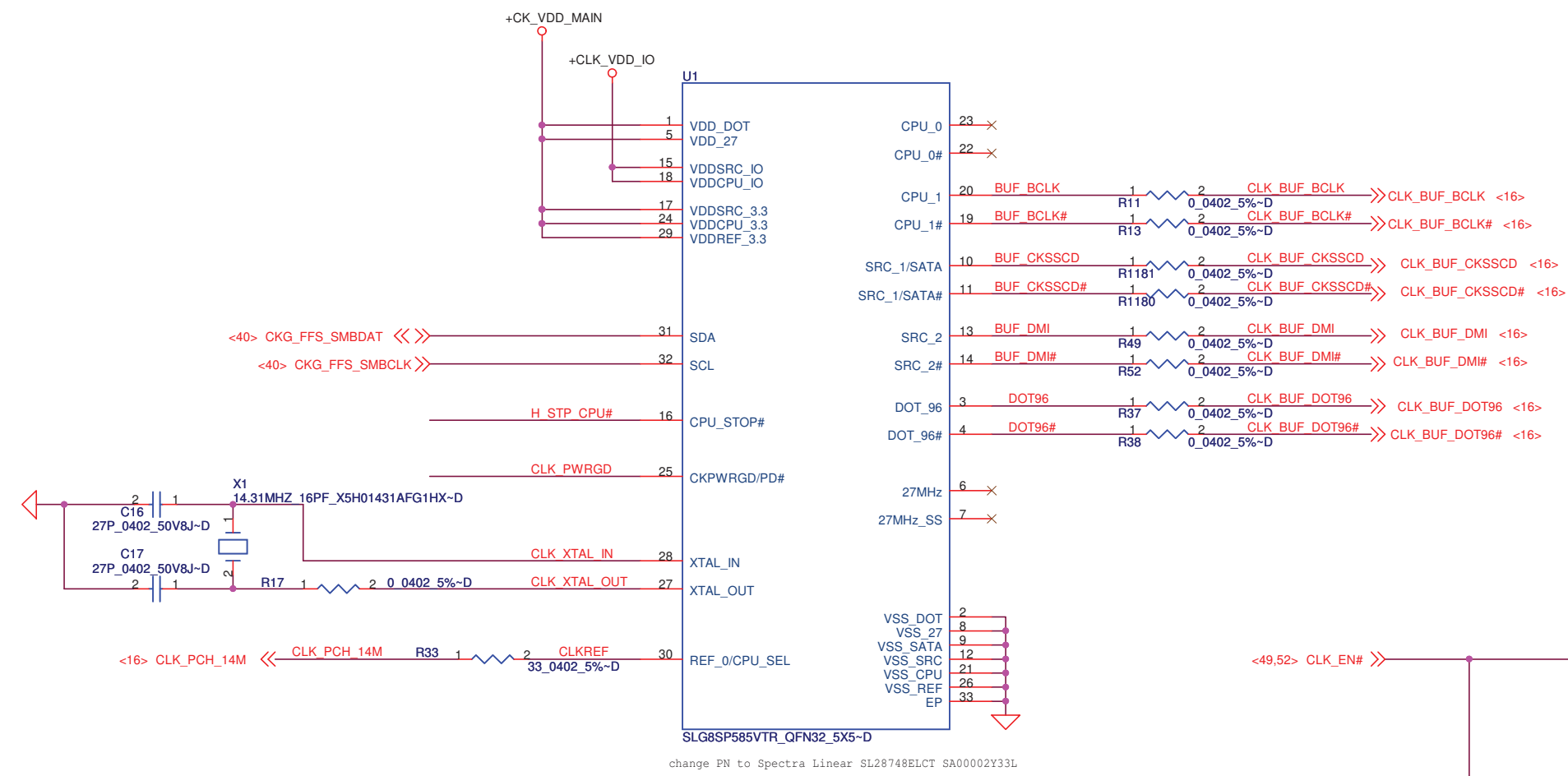
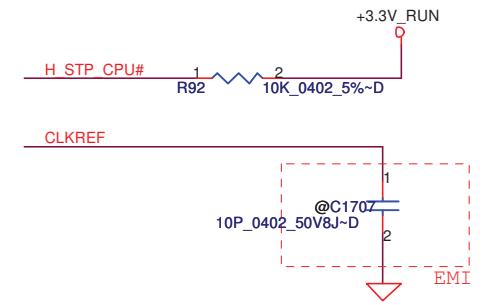


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Title Power Rail			
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+CLK_VDD_IO CAN BE CHANGE FROM 1.05V TO 3V



REF_0/CPU_SEL

PIN 30	CPU0	CPU1
1 (0.7~1.5v)	100MHz	100MHz
0 (DEFAULT)	133MHz	133MHz

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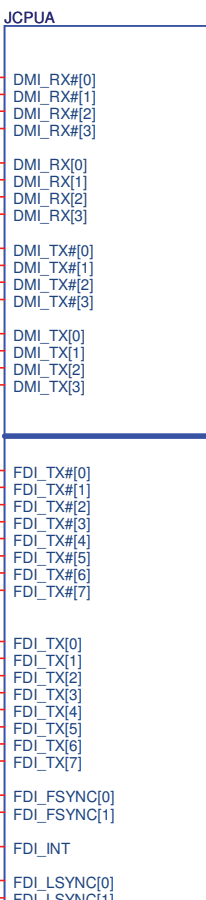
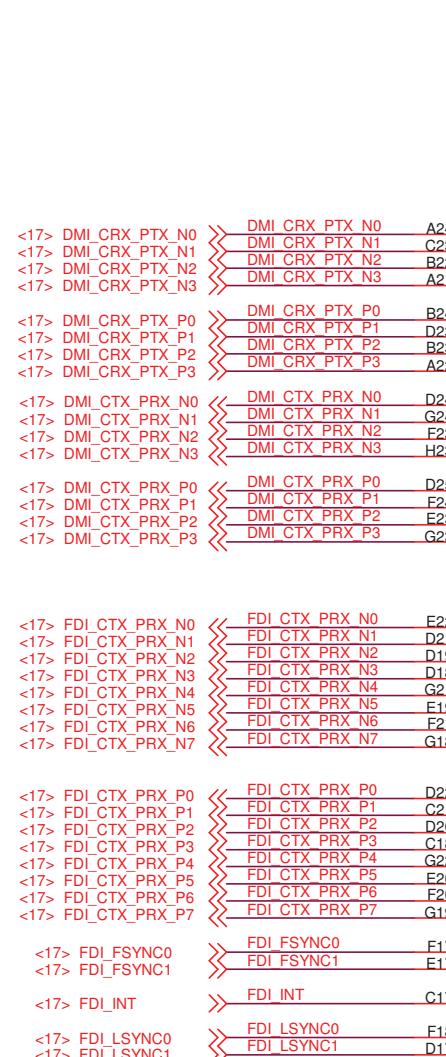
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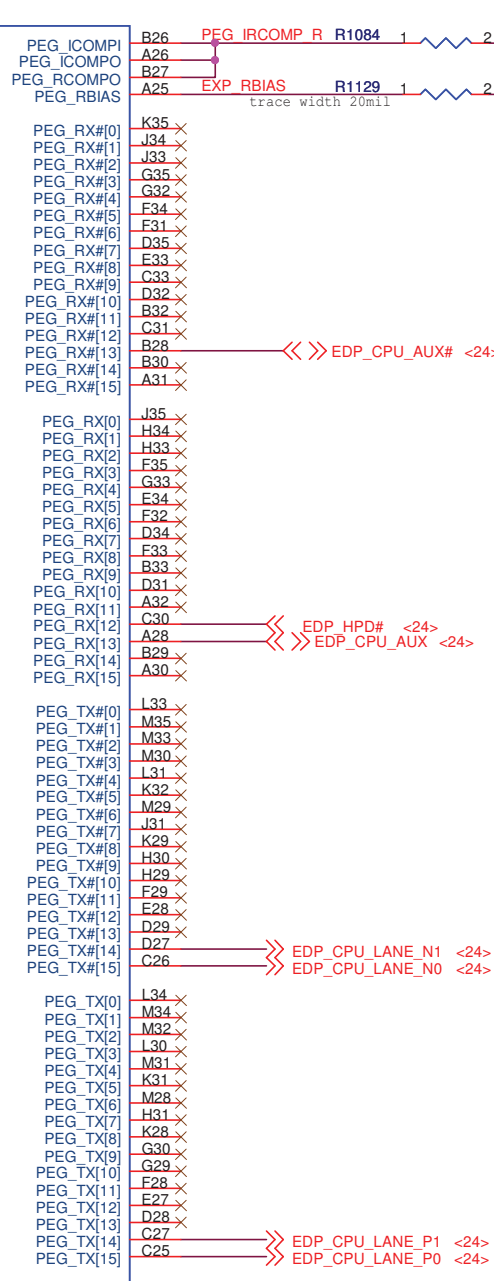
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Size: Document Number **LA-5471P** Rev 1.0

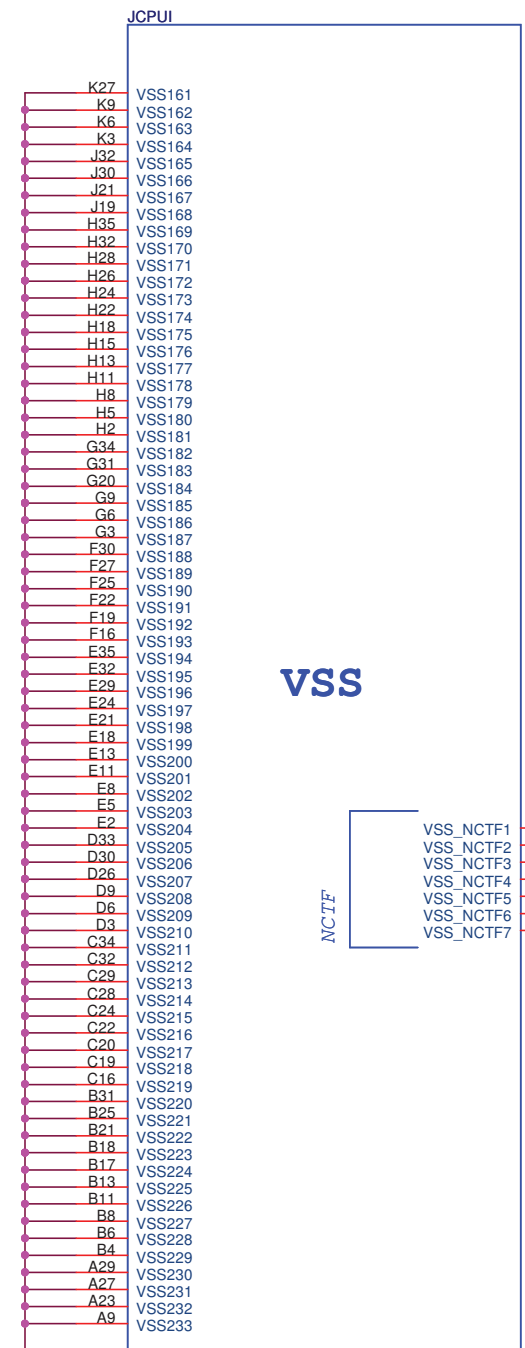
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PCI EXPRESS / GRAPHICS



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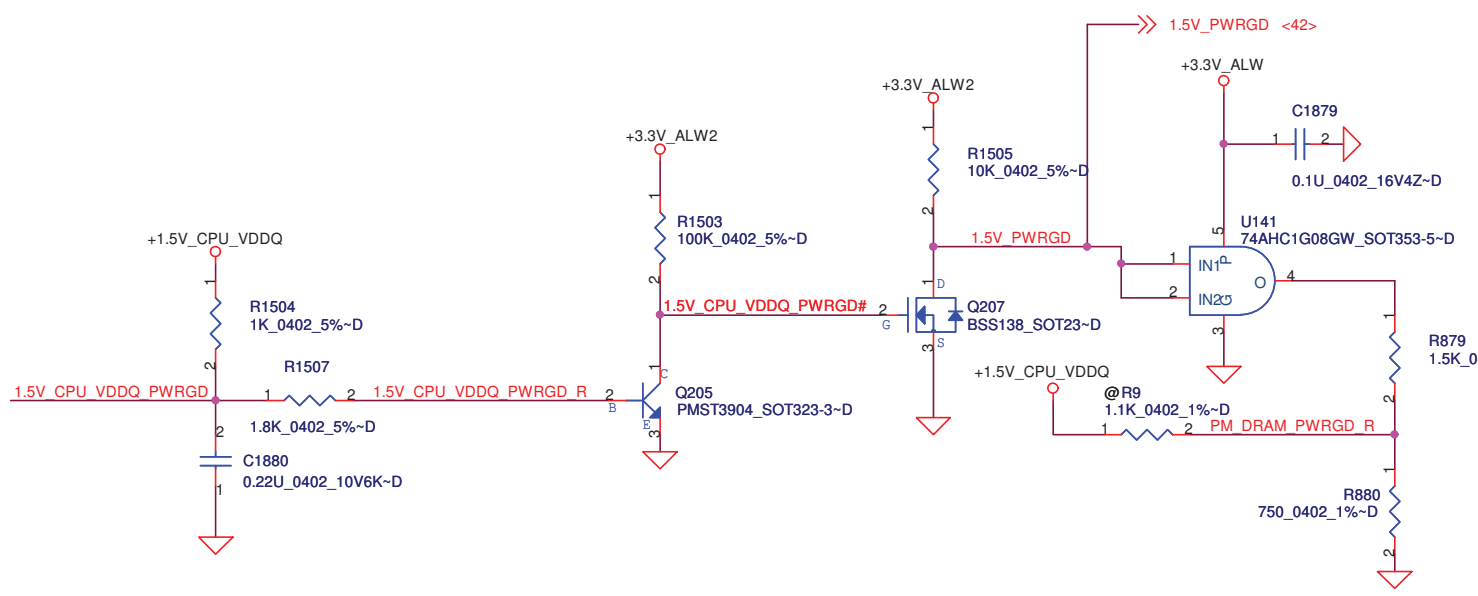
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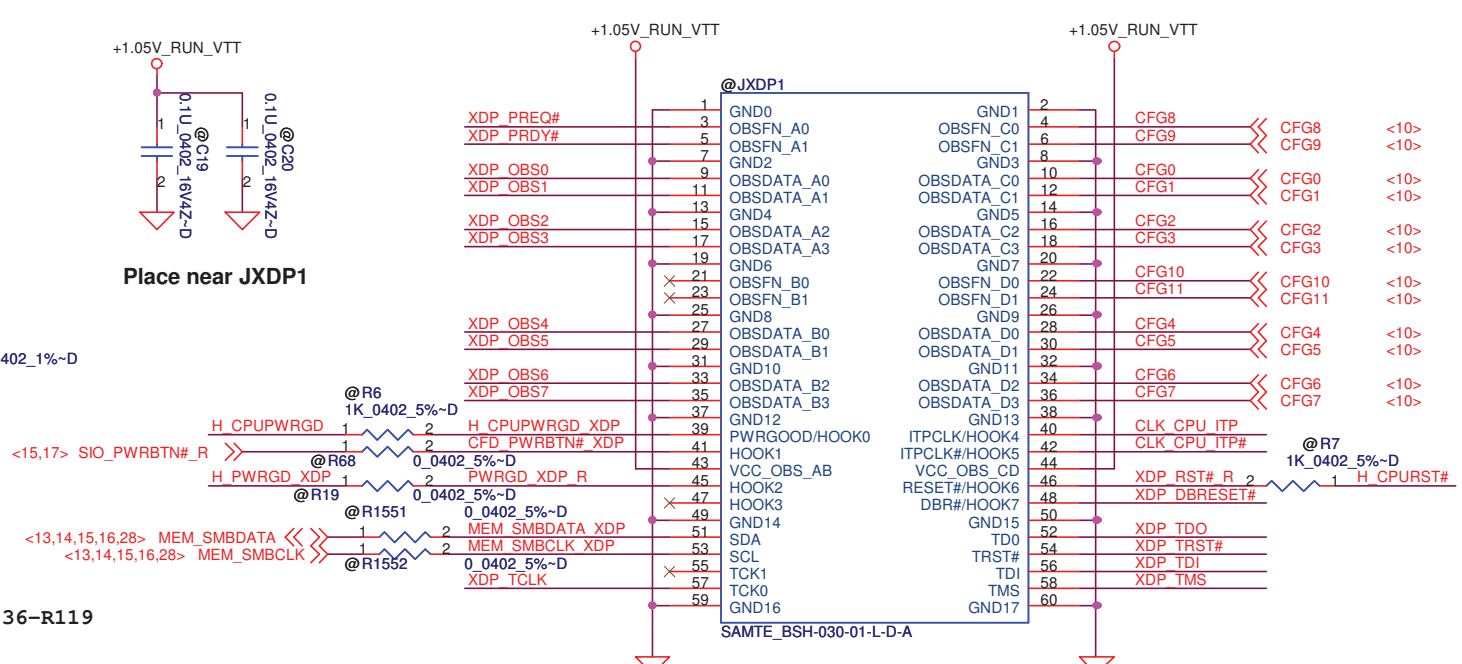
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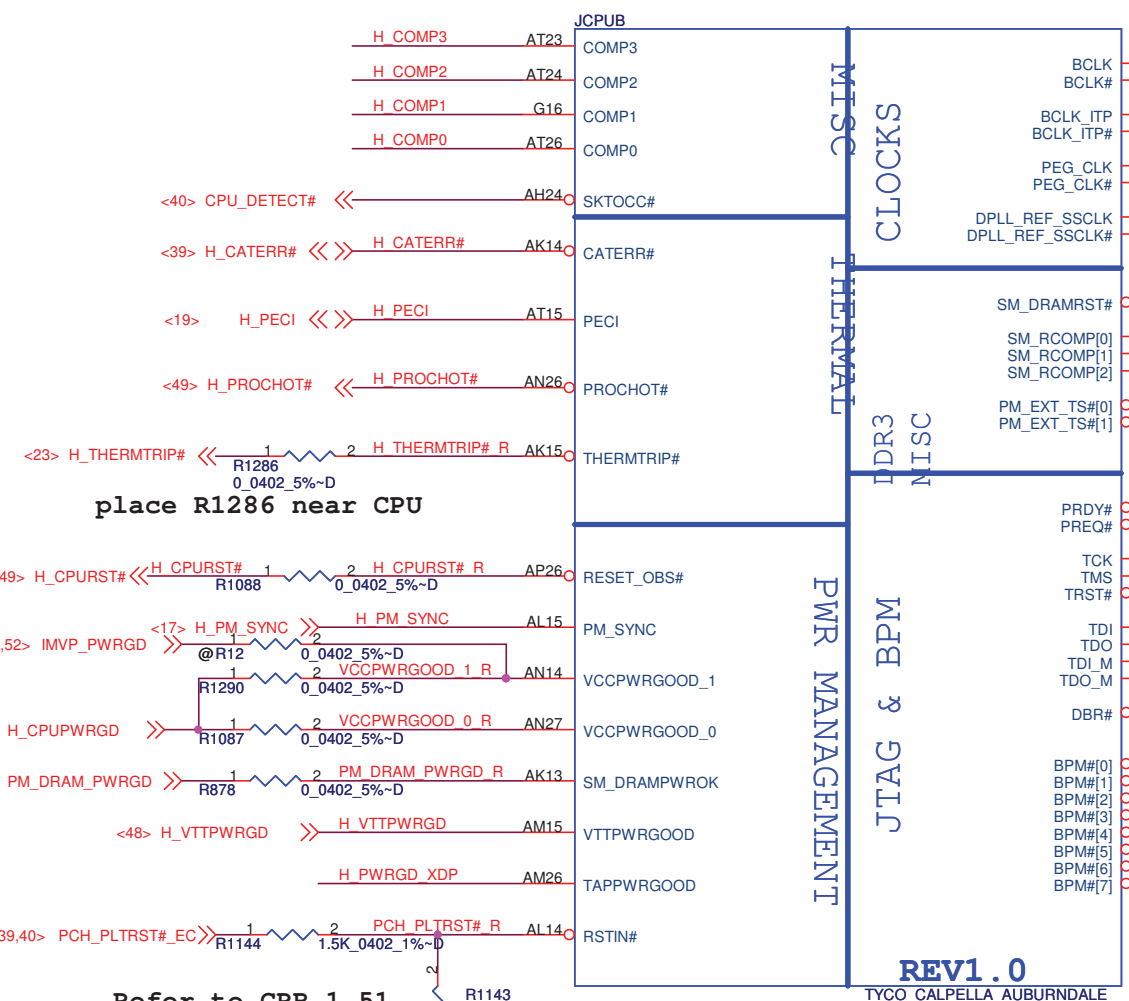
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Place near JXDP1



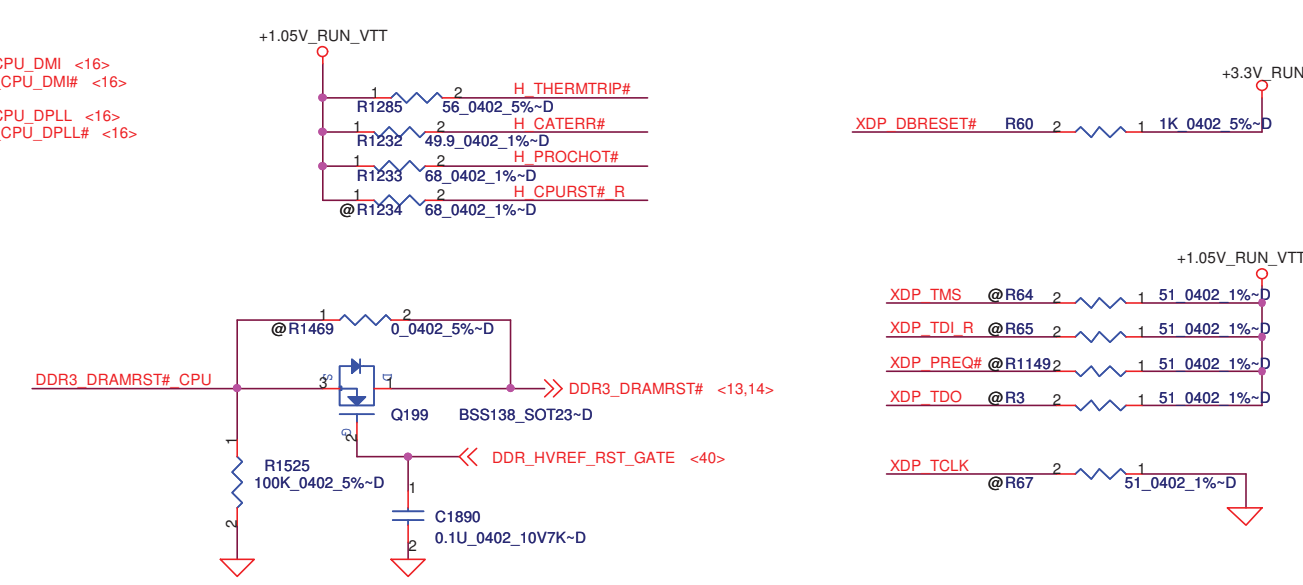
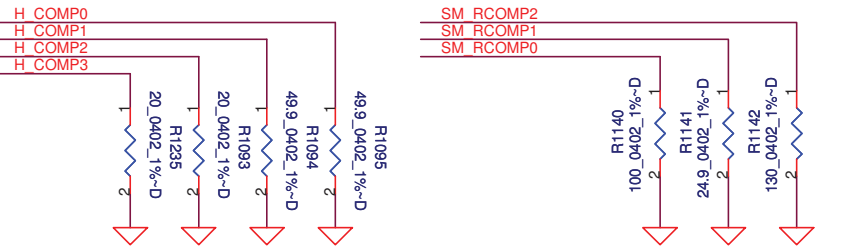
Keep R1132, R1133, R1136-R119 for slew rate control.



place R1286 near CPU

Refer to CRB 1.51

For ESD concern, please put near CPU



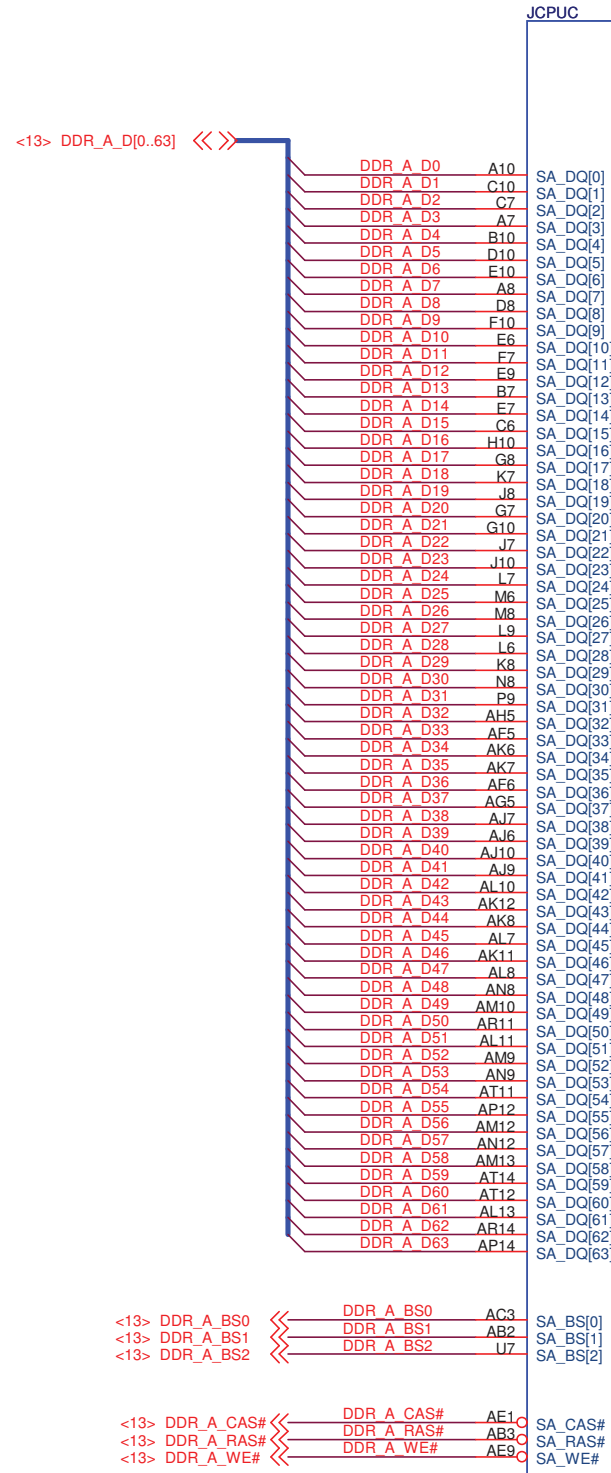
JTAG MAPPING

Scan Chain	Stuff -> R1153,R1156,R1157 (Default)	No stuff -> R1154,R1155
CPU Only	Stuff -> R1153,R1154	No stuff -> R1154,R1155,R1157
PCH Only	Stuff -> R1155,R1156	No stuff -> R1153,R1154,R1157

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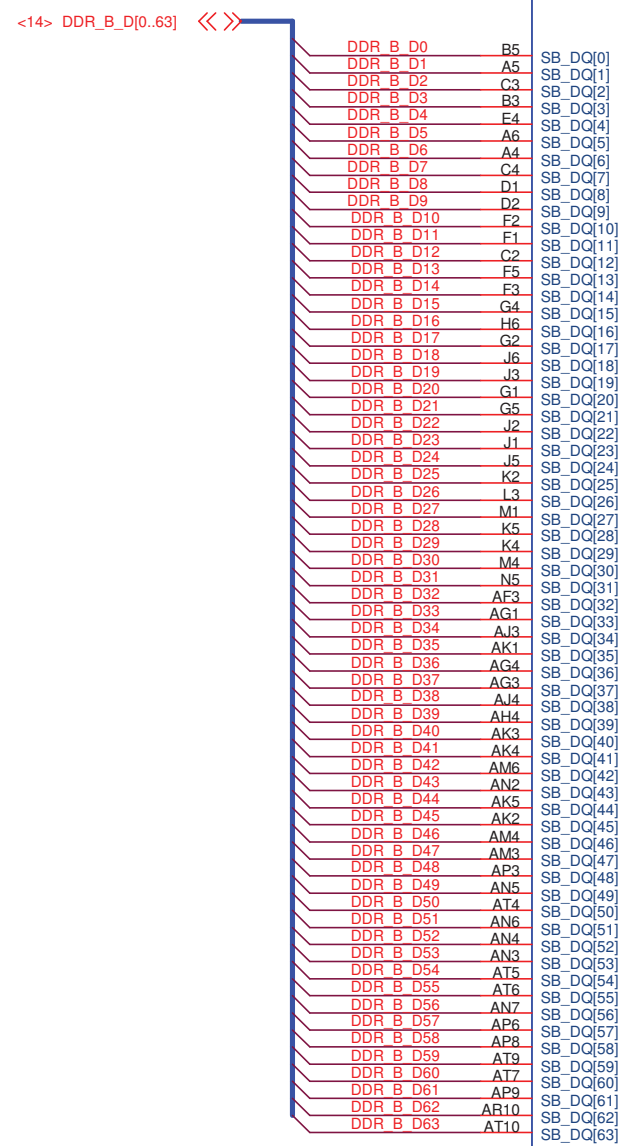


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DDR SYSTEM MEMORY - A

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DDR SYSTEM MEMORY - B

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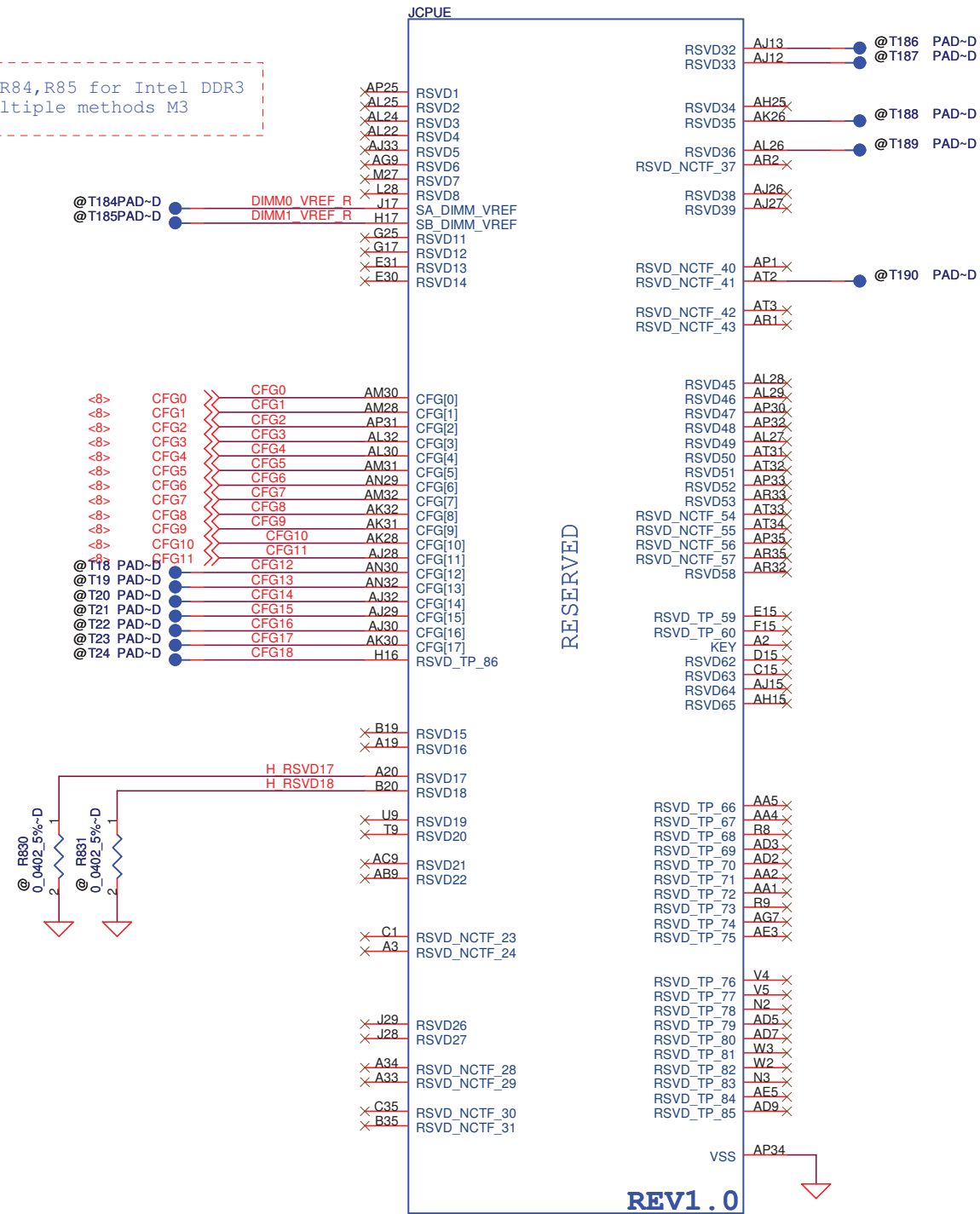


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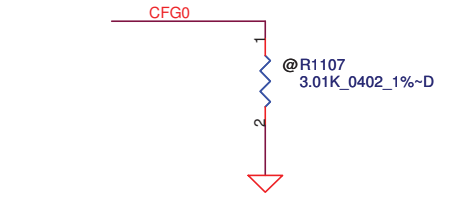
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Populate R84,R85 for Intel DDR3 VREFDQ multiple methods M3

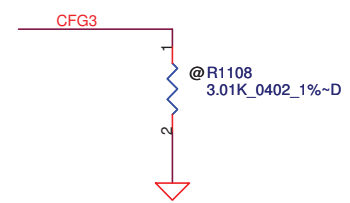


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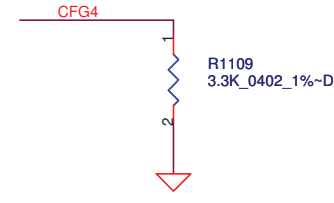
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PCI-Express Configuration Select	
CFG0	1 : Single PEG 0 : Bifurcation enable



PCI-Express Static Lane Reversal	
CFG3	1 : Normal Operation 0 : Lane Number Reversed 15->0, 14->1 ...



Display Port Presence	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

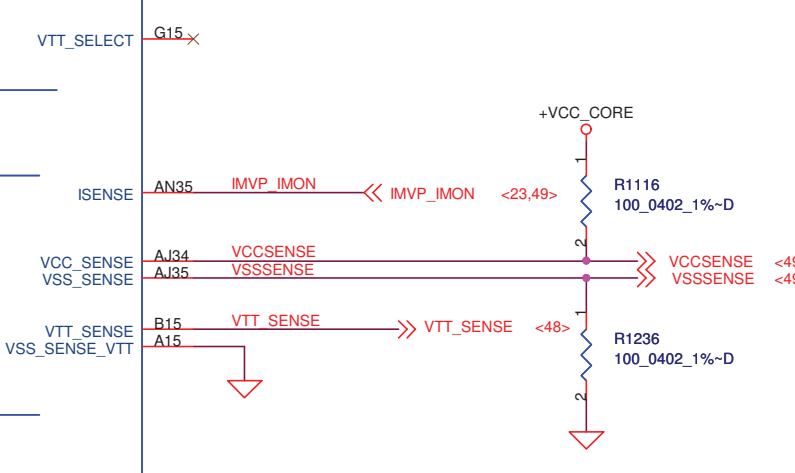
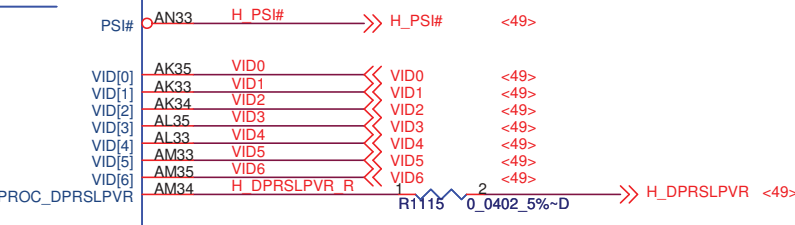
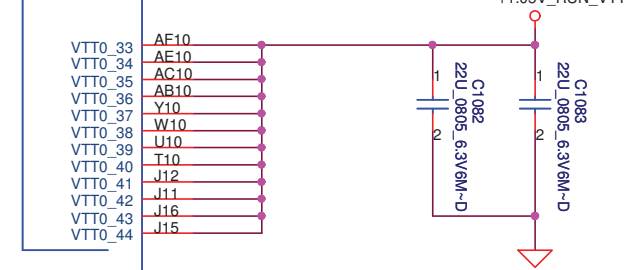
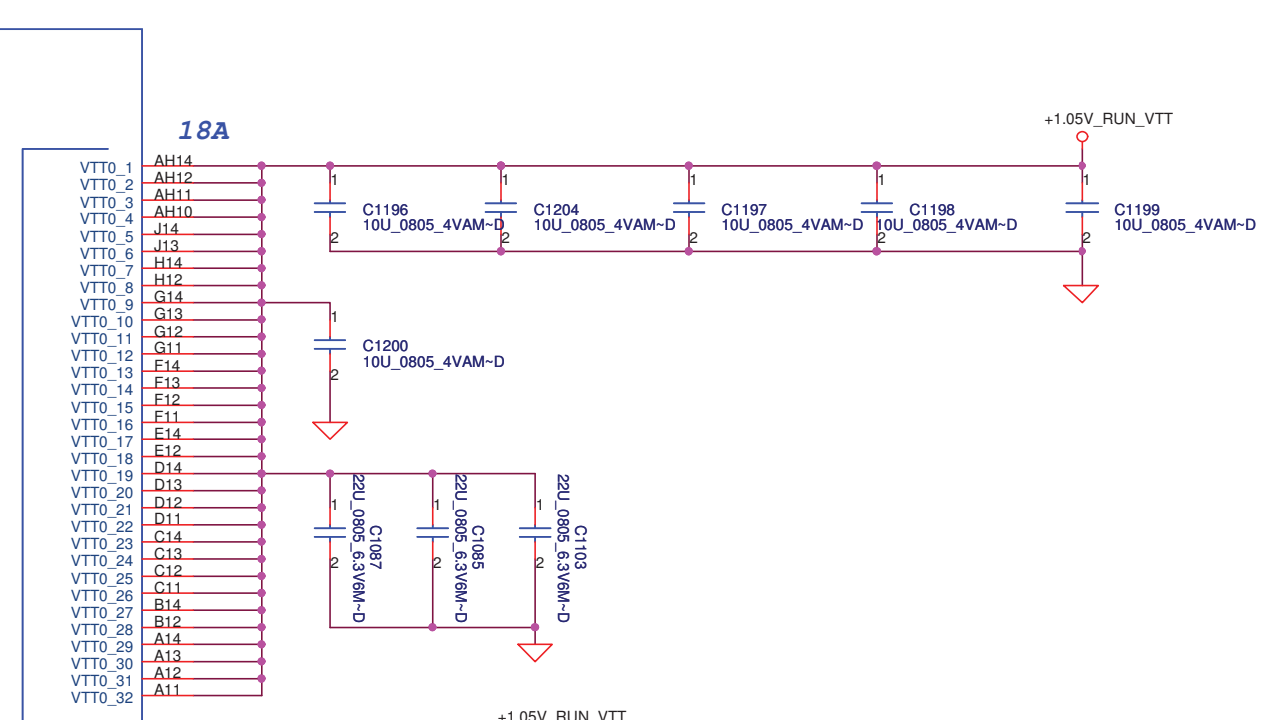
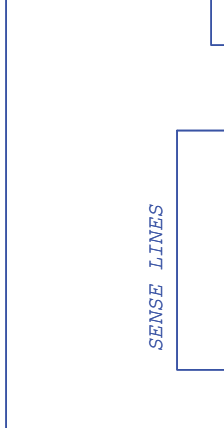
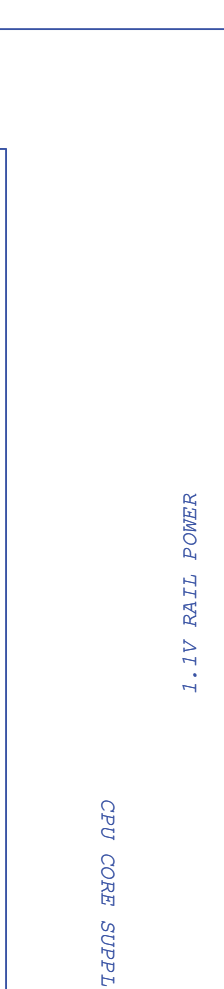
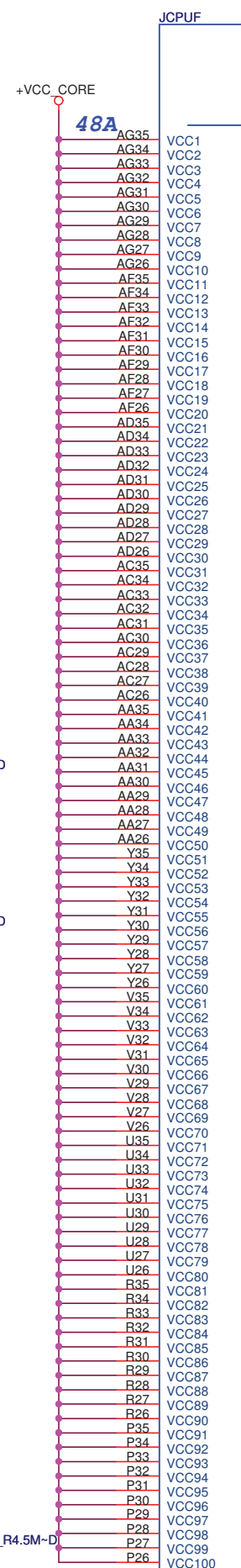
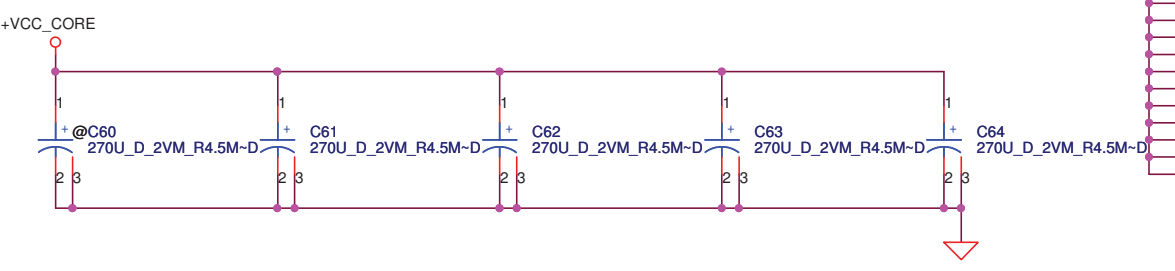
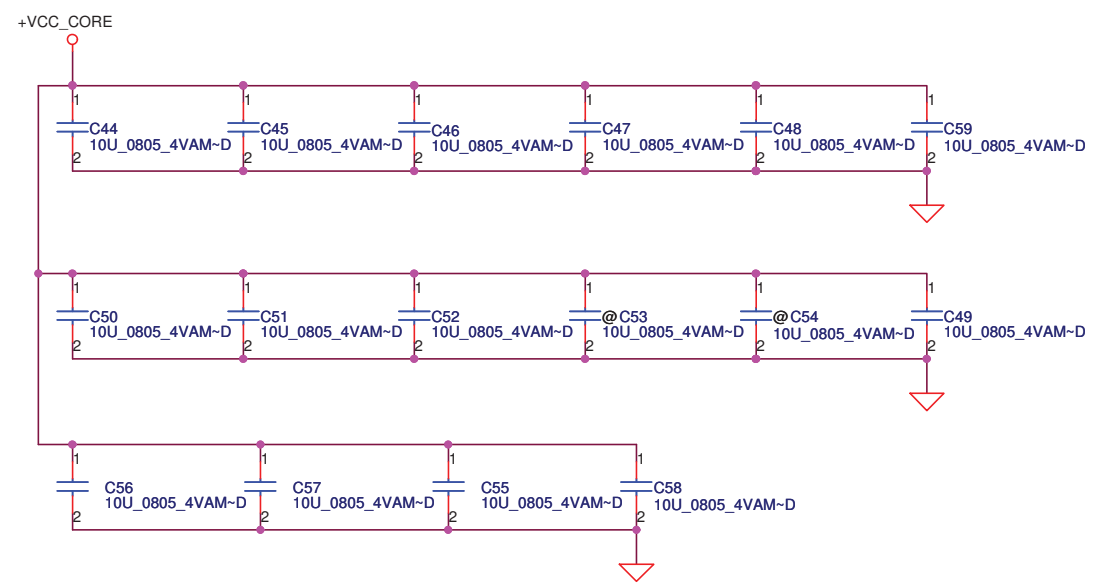
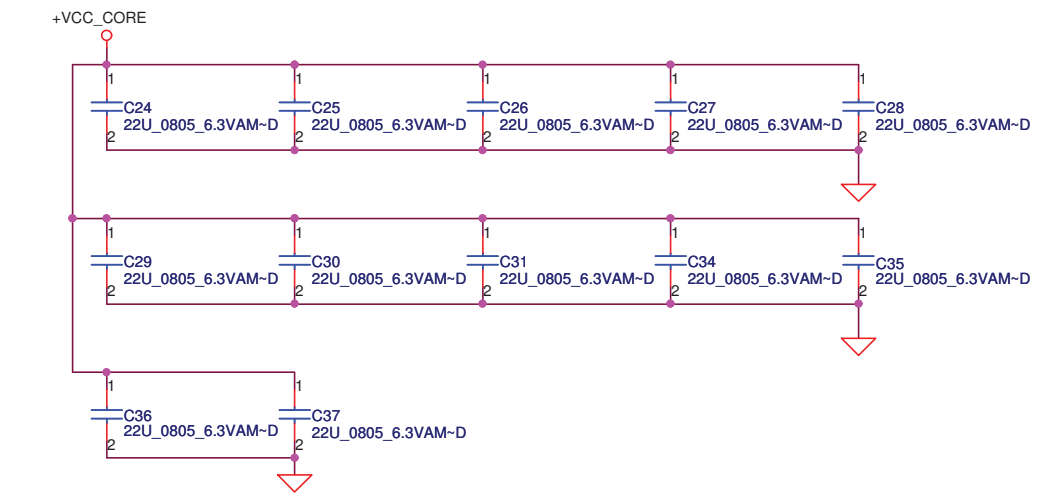
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VTT_SELECT = low, 1.1V
VTT_SELECT = high, 1.05V

Place R1116 and R1236 near CPU
Route VCCSENSE and VSSSENSE trace at 27.4 ohms, 7 mils spacing

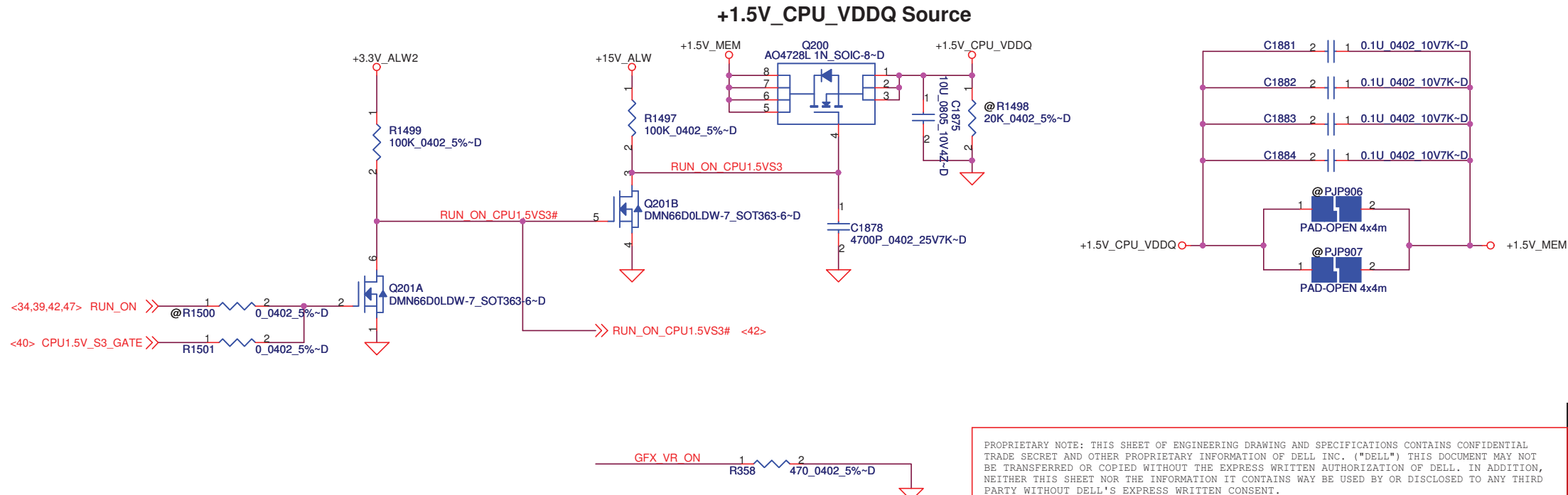
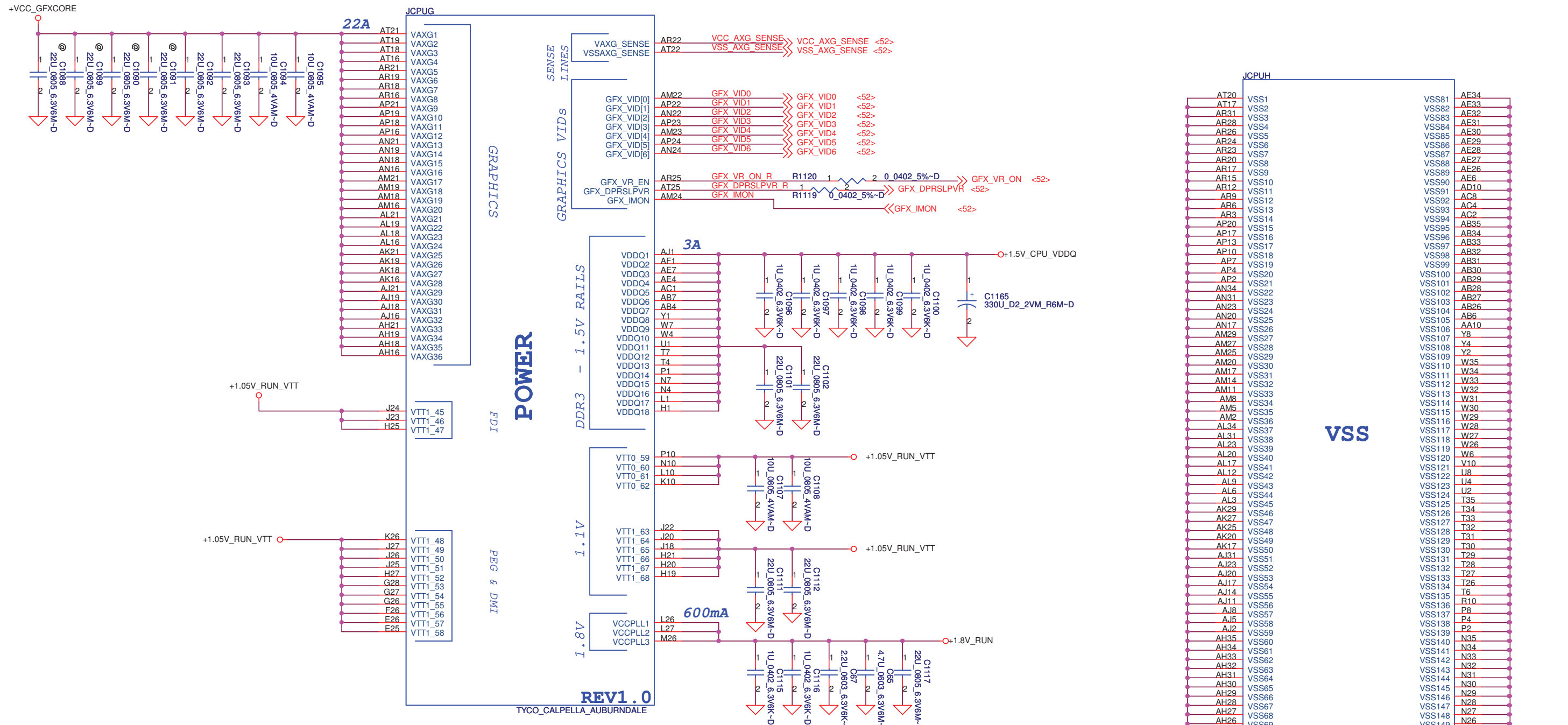
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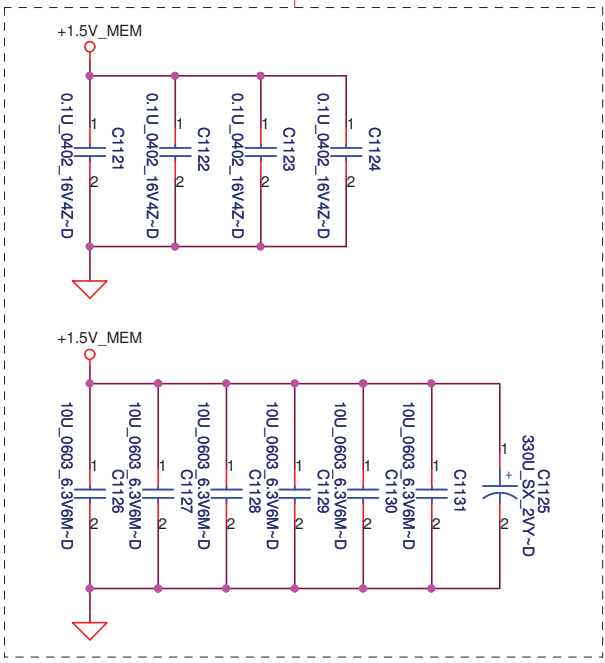
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 <9> DDR_A_MA[0..15] <<>>

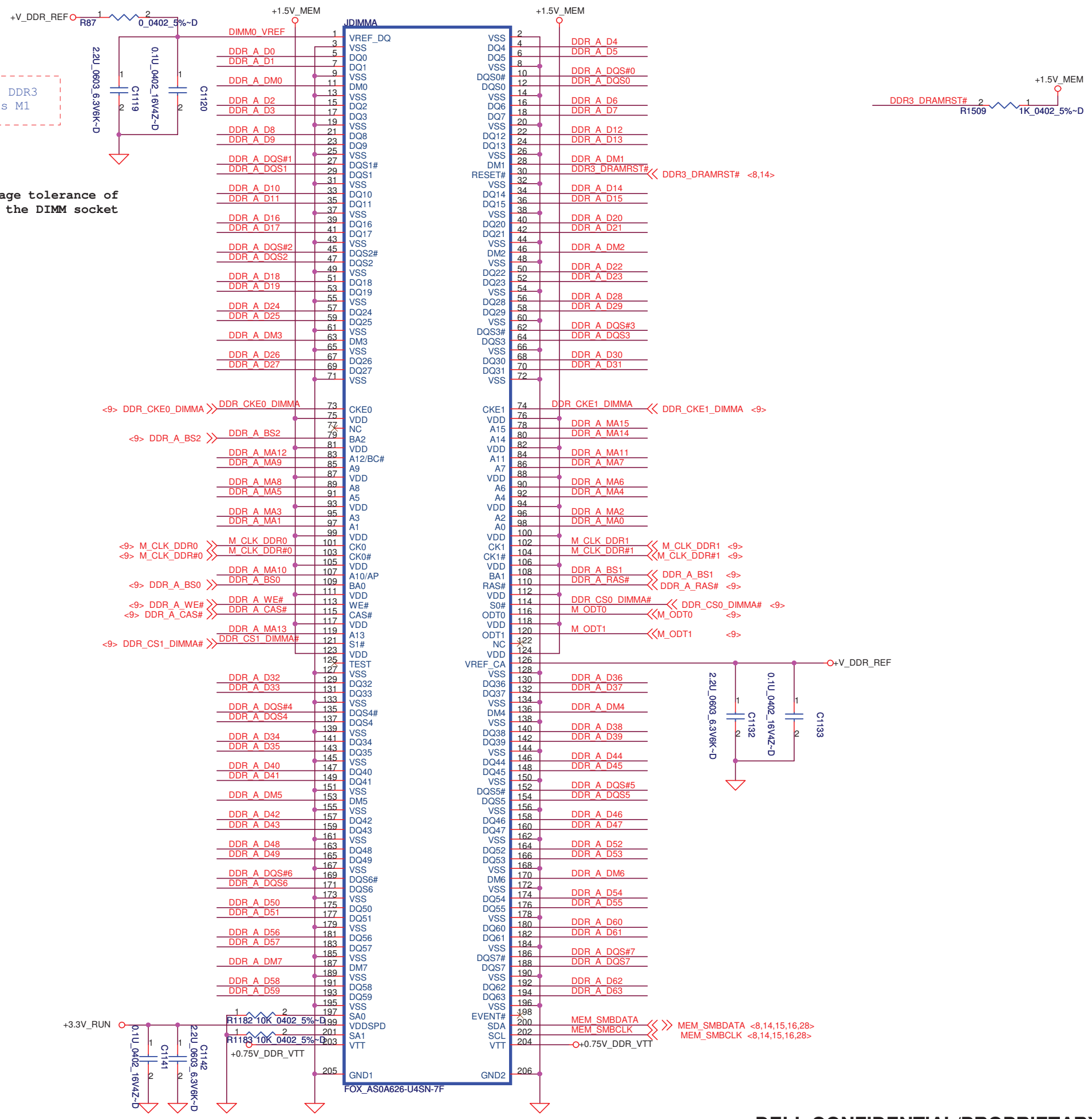
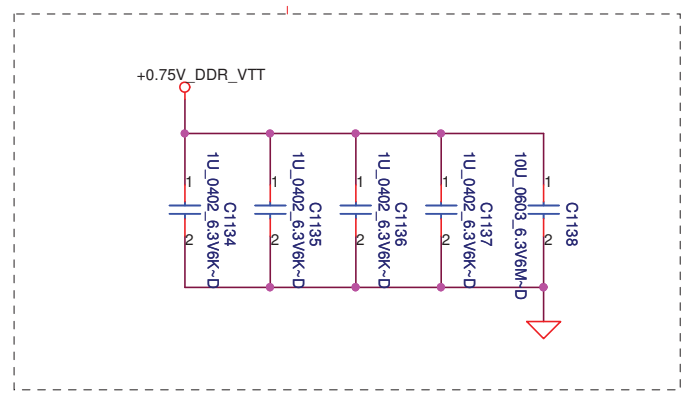
Populate R87 for Intel DDR3 VREFDQ multiple methods M1

Layout Note:
Place near JDIMMA

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket



Layout Note:
Place near JDIMMA.203, 204



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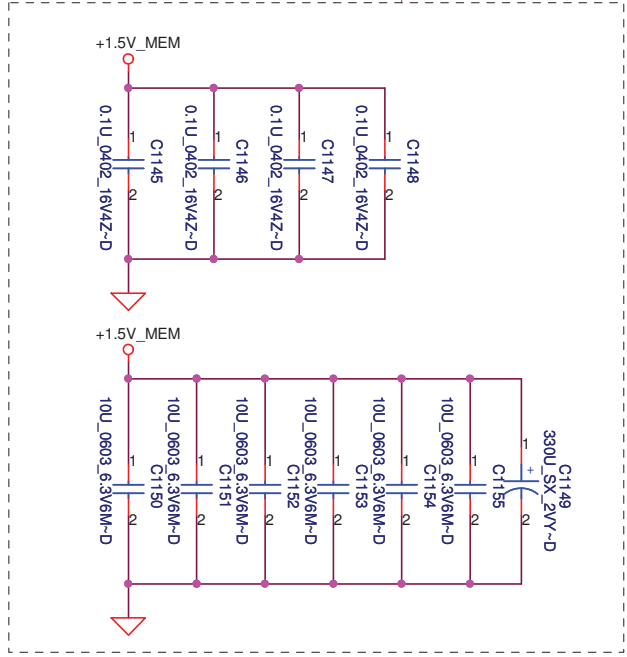
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 <9> DDR_B_D[0..63] <<>>
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 <9> DDR_B_DQS[0..7] <<>>
 <9> DDR_B_MA[0..15] <<>>

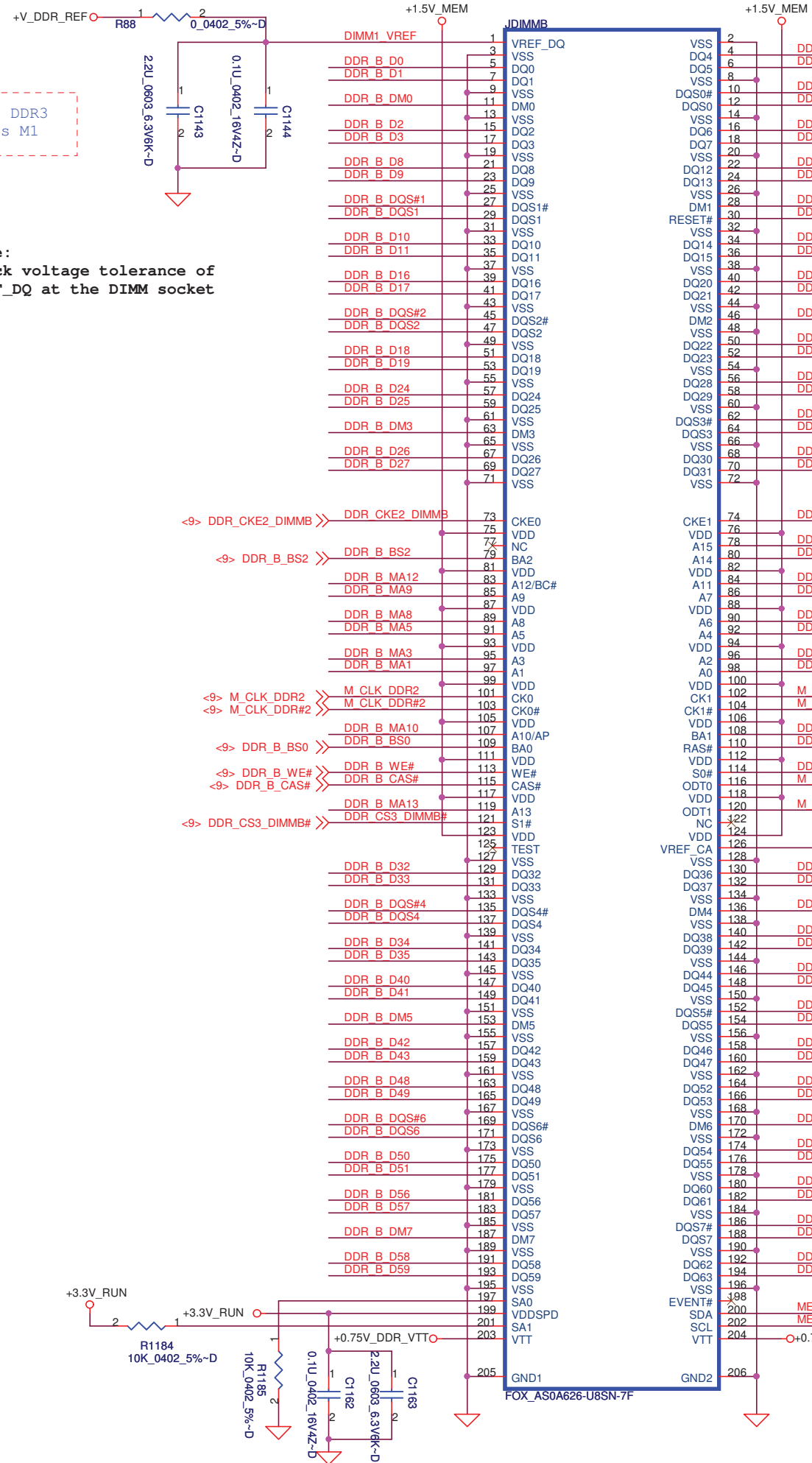
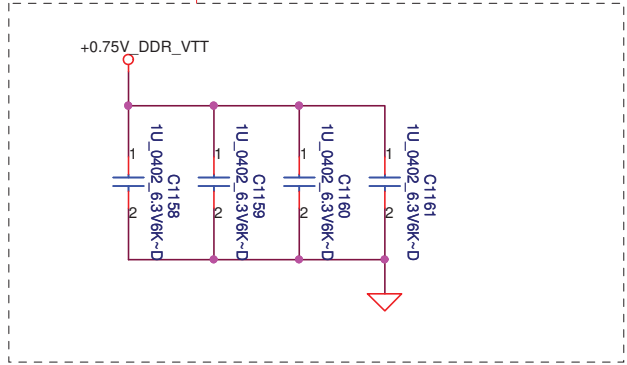
Populate R88 for Intel DDR3
 VREFDQ multiple methods M1

Note:
 Check voltage tolerance of
 VREF_DQ at the DIMM socket

Layout Note:
 Place near JDIMMB



Layout Note:
 Place near JDIMMB.203, 204

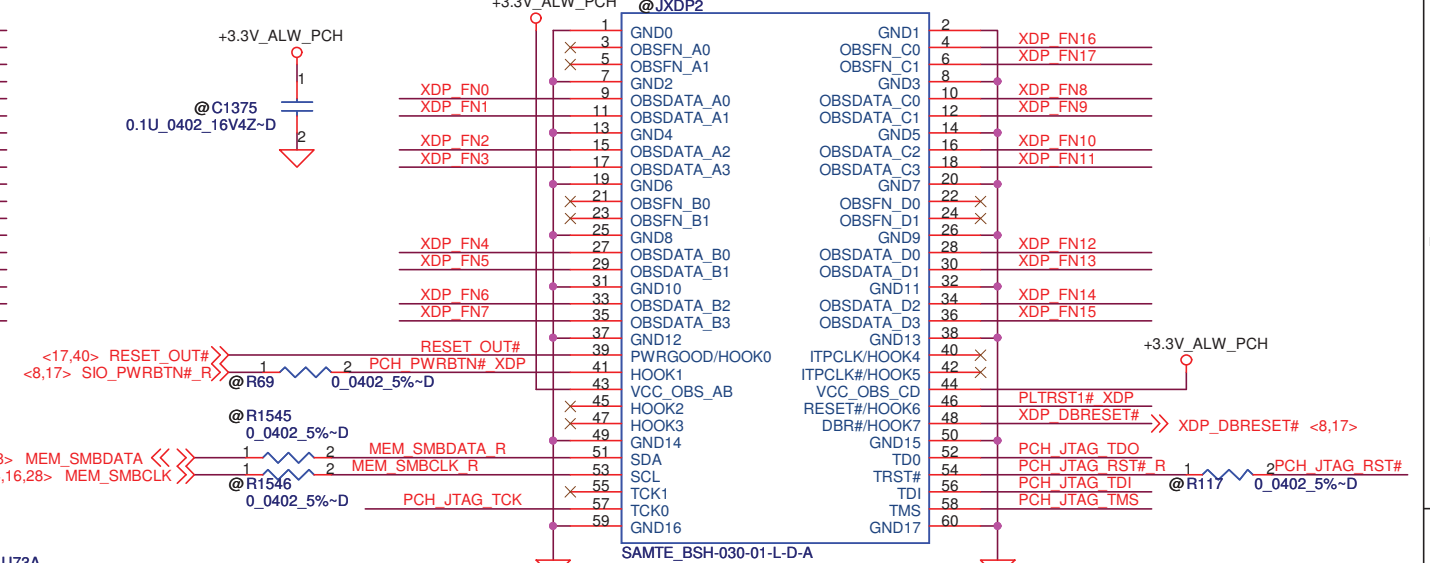
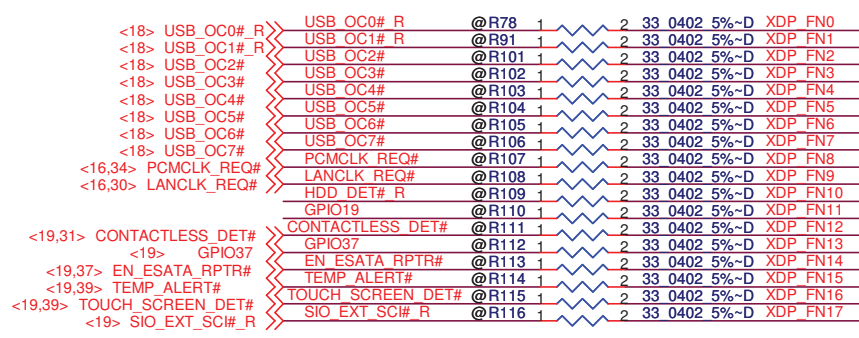


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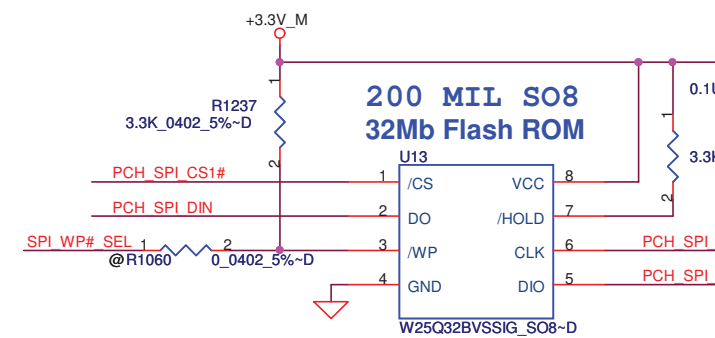
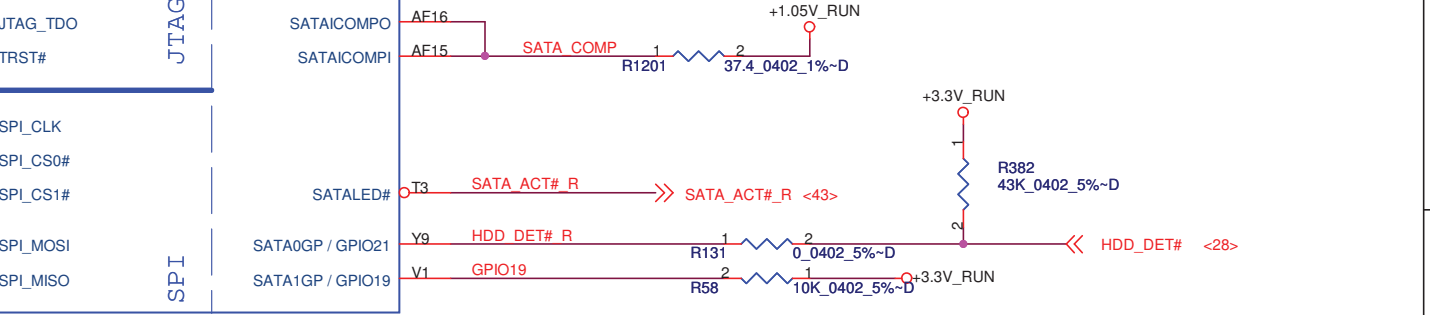
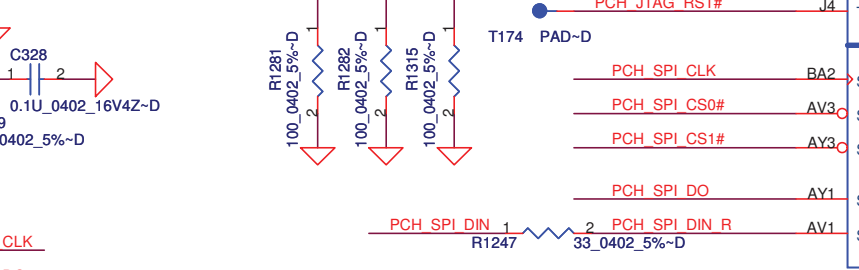
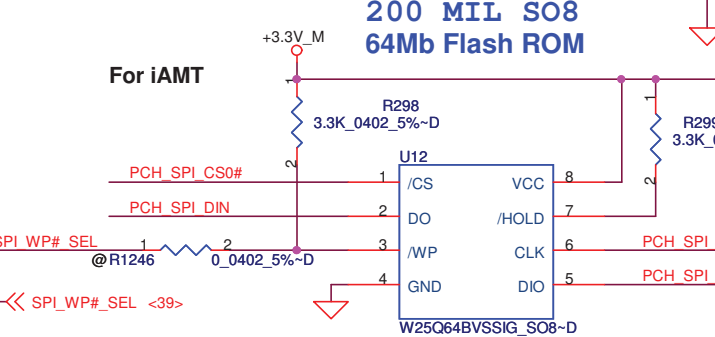
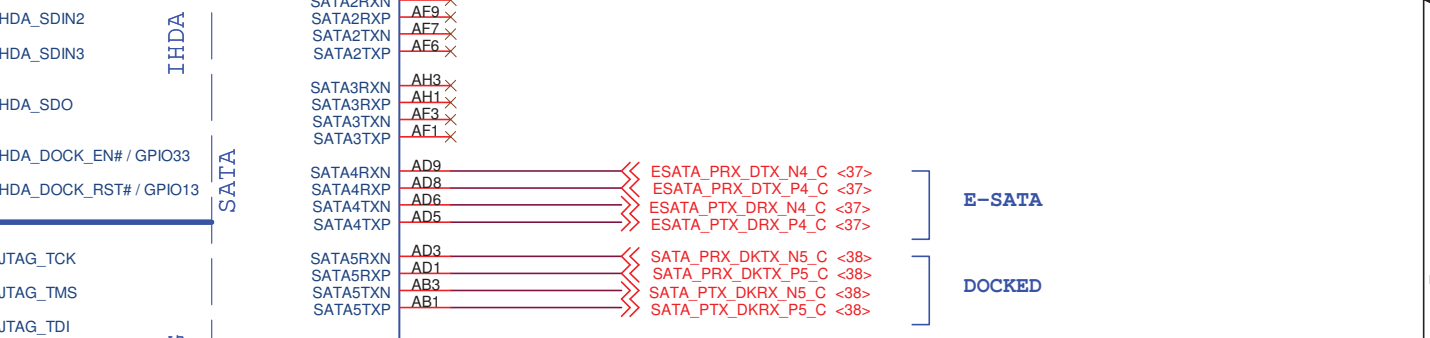
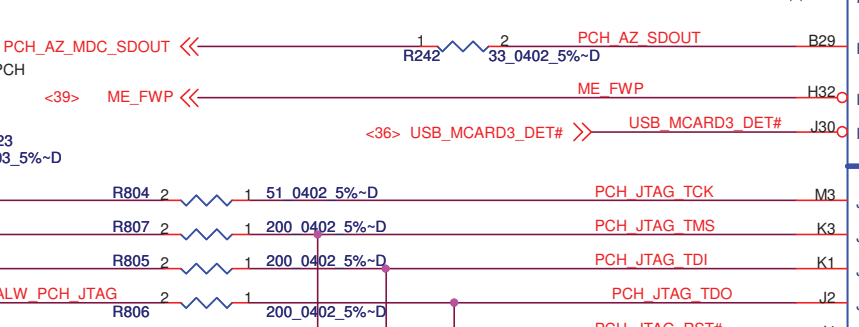
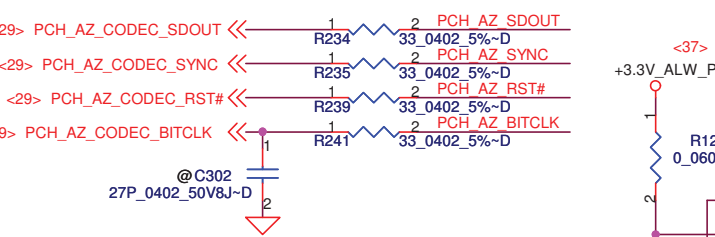
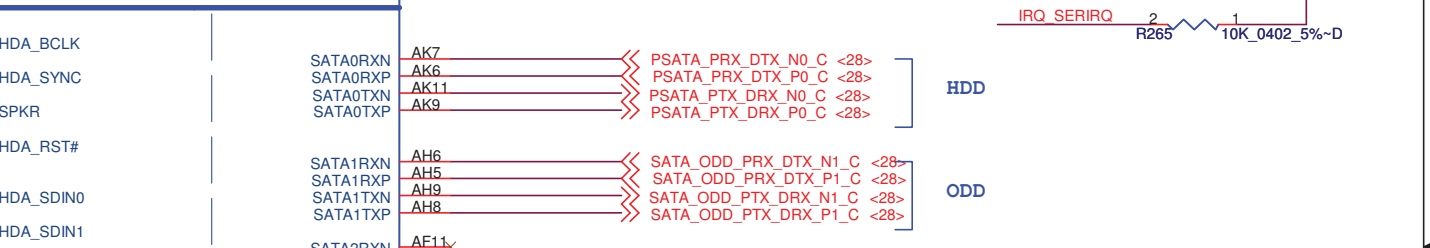
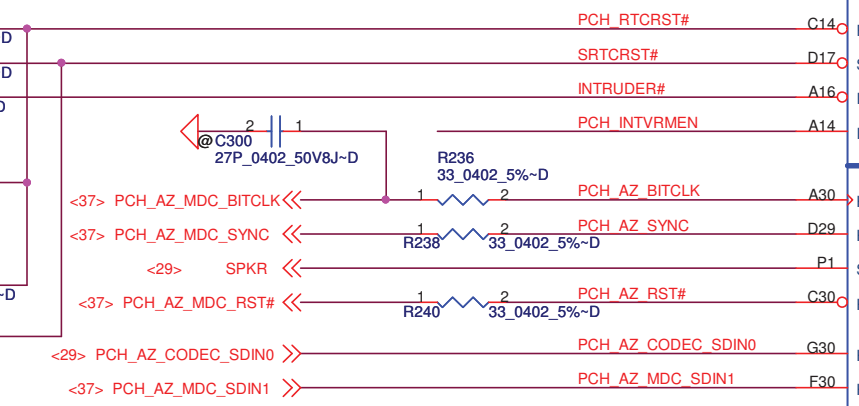
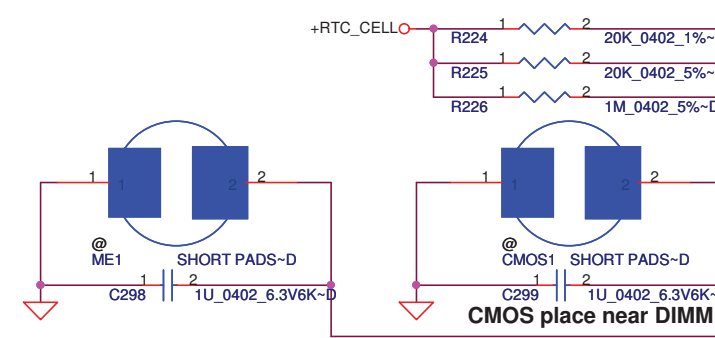
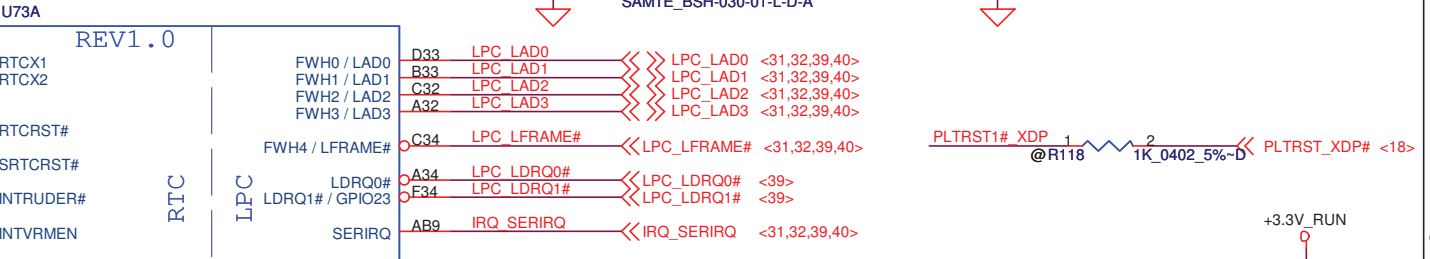
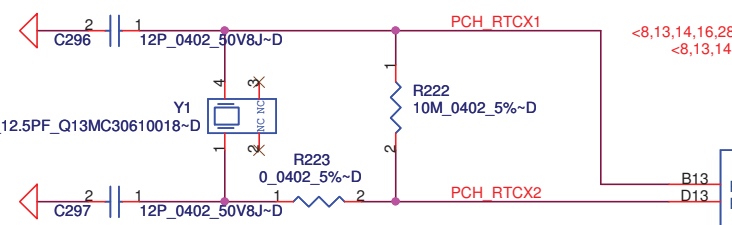
CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

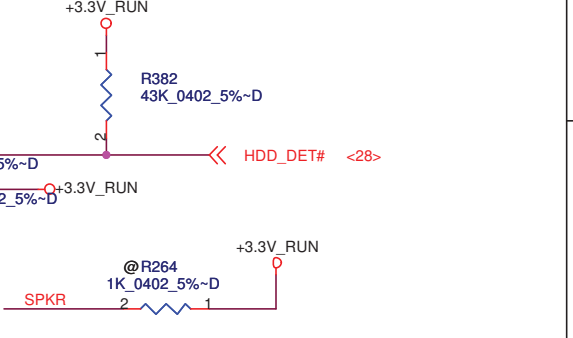


INTVRMEN- Integrated SUS
1.1V VRM Enable
High - Enable Internal VRs

On Die PLL VR is supplied by
1.5V when sampled high, 1.8 V
when sampled low



PCH Pin	Ref.	PCH JTAG Enable		PCH JTAG Disable		Production
		ES1	ES2	ES1	ES2	
TDO	R806	No Stuff	200 ohm	No Stuff	No Stuff	200 ohm
	R1315	No Stuff	100 ohm	No Stuff	No Stuff	100 ohm
TMS	R807	200 ohm	200 ohm	No Stuff	No Stuff	200 ohm
	R1281	100 ohm	100 ohm	No Stuff	No Stuff	100 ohm
TDI	R805	200 ohm	200 ohm	20K ohm	No Stuff	200 ohm
	R1282	100 ohm	100 ohm	10K ohm	No Stuff	100 ohm
TCK	R804	4.7K ohm	4.7K ohm	4.7K ohm	4.7K ohm	51 ohm
	R808	20K ohm	No Stuff	No Stuff	No Stuff	No Stuff
TRST#	R1316	10K ohm	No Stuff	No Stuff	No Stuff	No Stuff



No Reboot Strap
SPKR
Low = Default
High = No Reboot

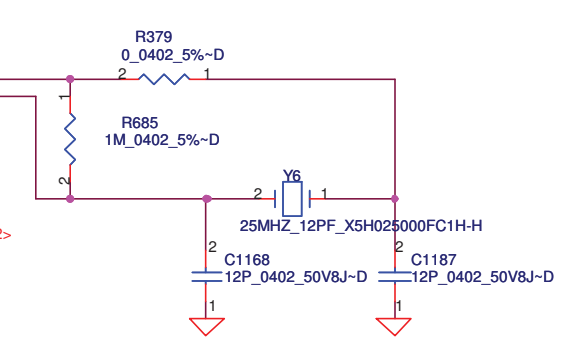
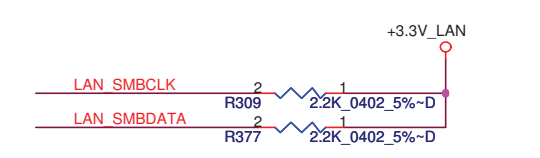
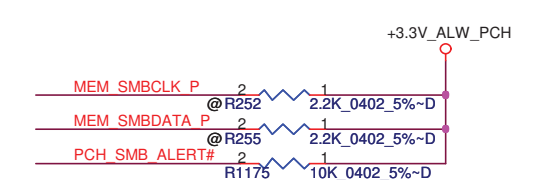
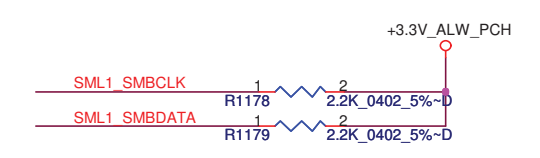
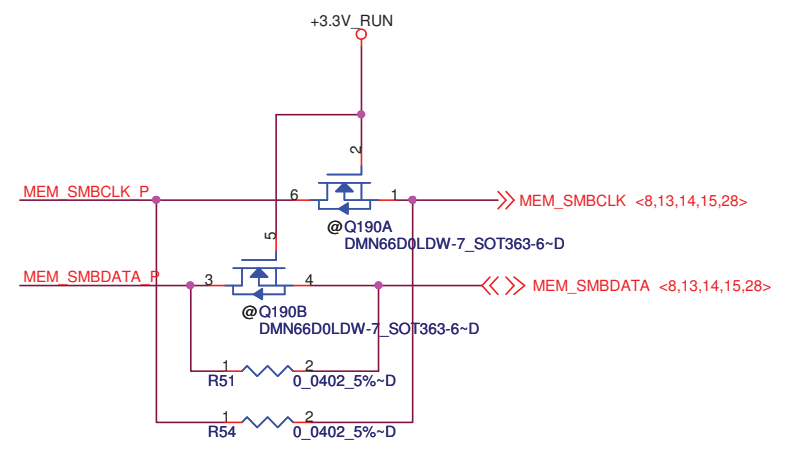
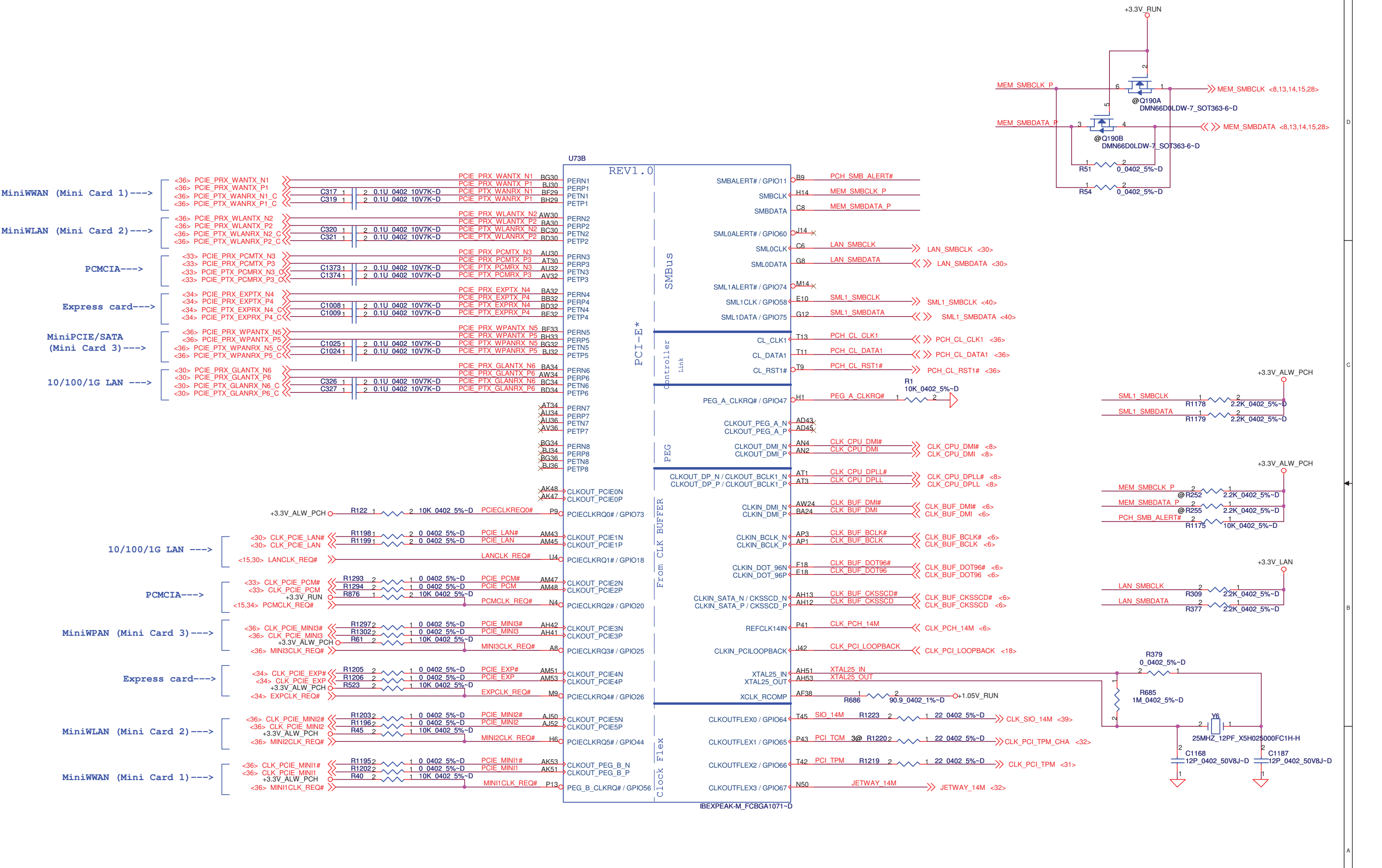
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Size: **LA-5471P**

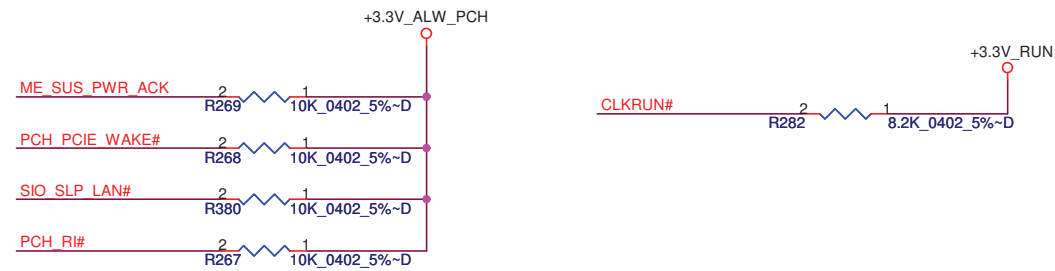
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Title		PCH (2/8)	
Size	Document Number	LA-5471P	
Date:	Wednesday, January 20, 2010	Sheet	16 of 57
		Rev	1.0

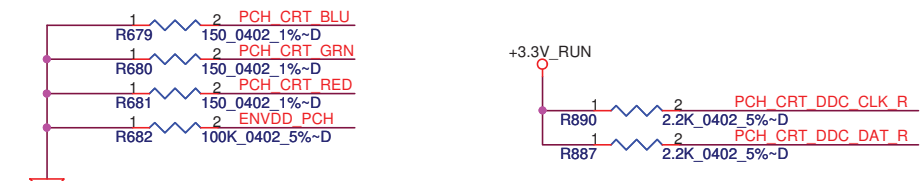
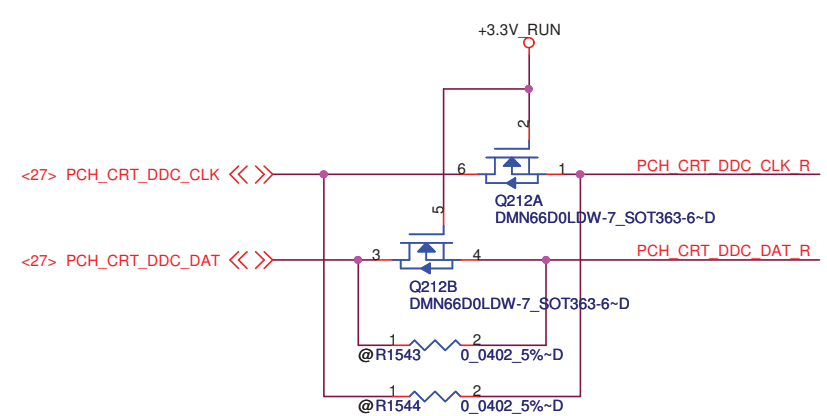
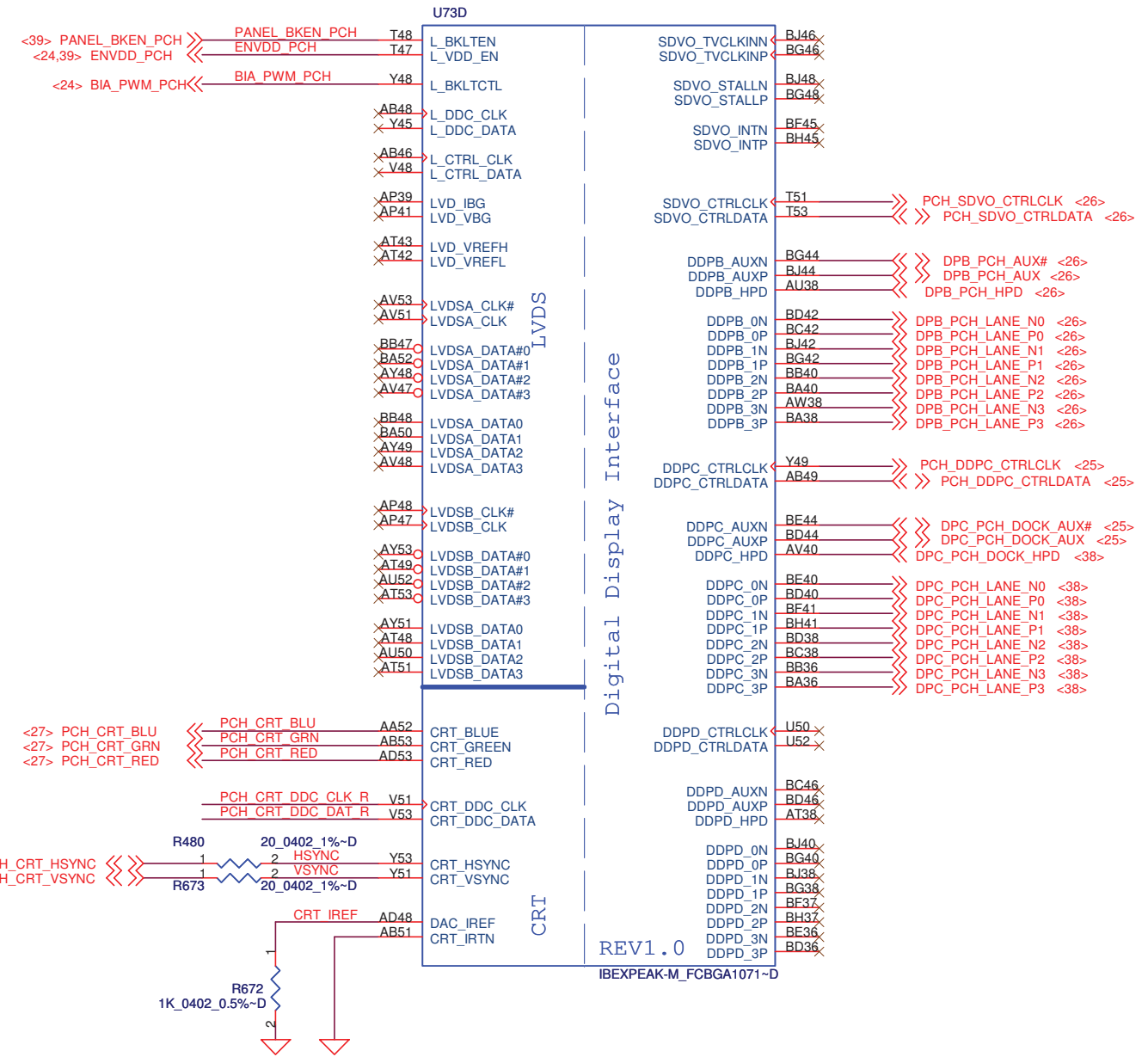
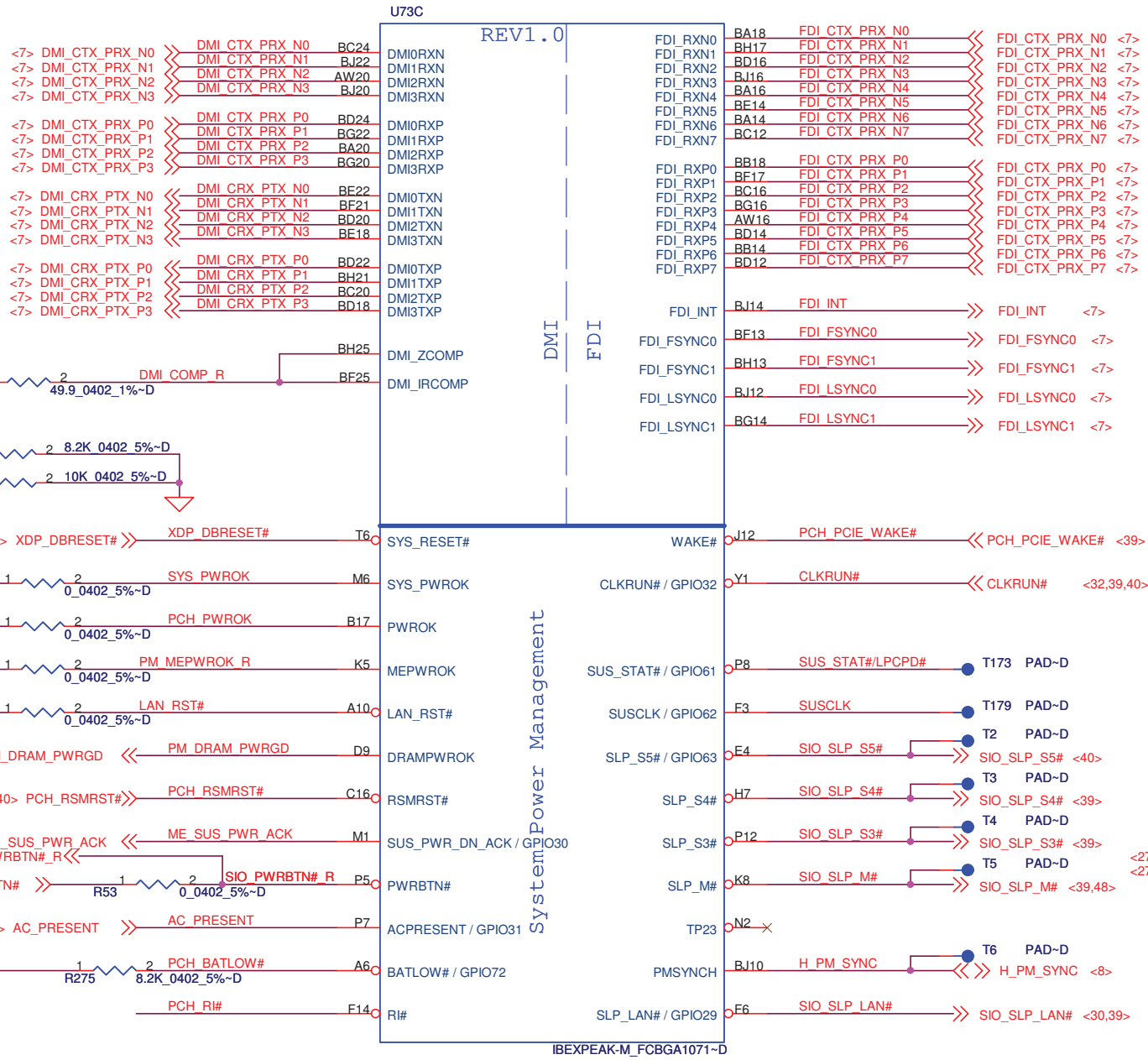
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Intel WW18 Strapping option

PORT	STRAP	ENABLE	DISABLE
LVDS	L_DDC_DATA	PU to 3.3V through 2.2Kohm	NC
PORT B	SDVO_CTRLDATA	PU to 3.3V through 2.2Kohm	NC
PORT B	DDPC_CTRLDATA	PU to 3.3V through 2.2Kohm	NC
PORT B	DDPD_CTRLDATA	PU to 3.3V through 2.2Kohm	NC
eDP on CPU	CFG[4] (at CPU)	PD to GND through 3.3Kohm	NC

Intel request DDPB can not support eDP



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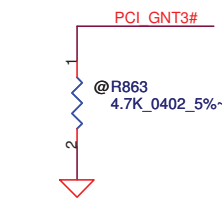
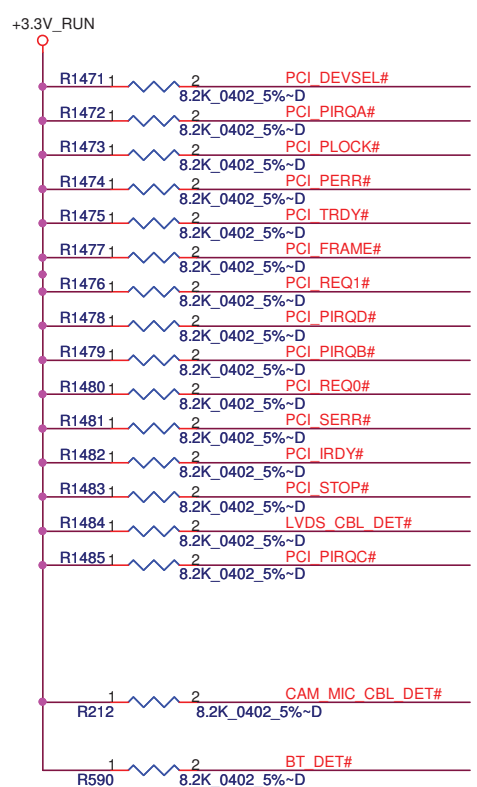
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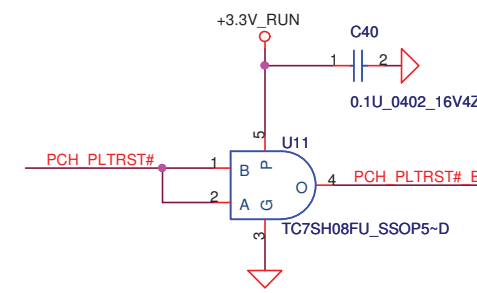
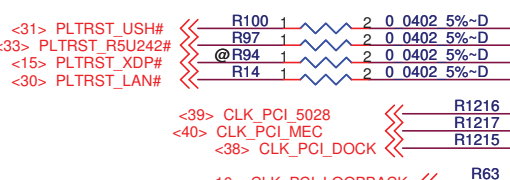
Document Number: **LA-5471P**

Rev: **1.0**

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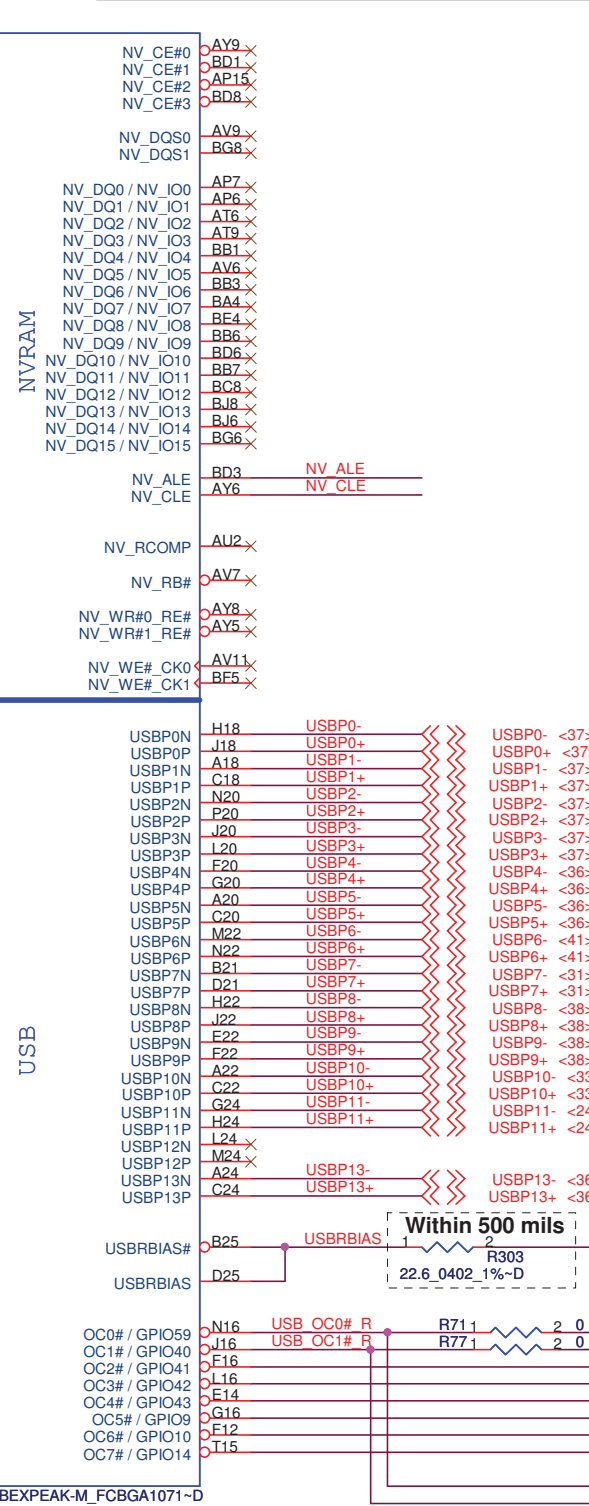
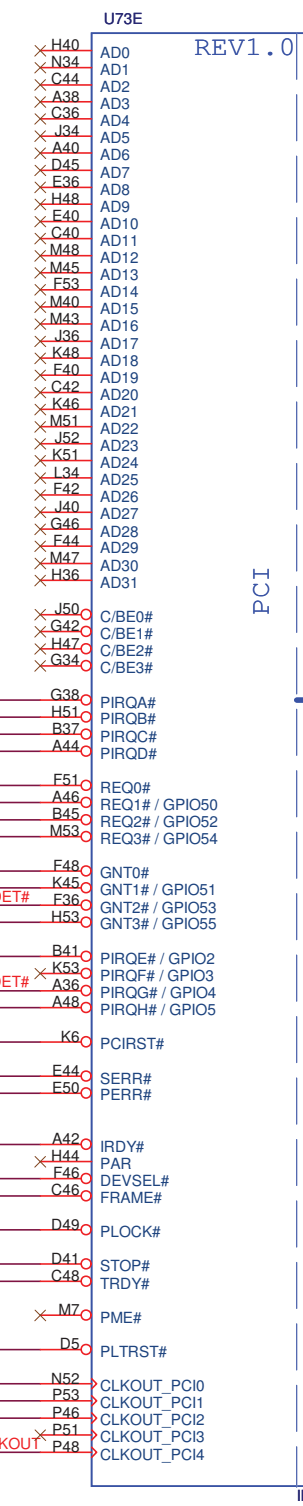


A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default

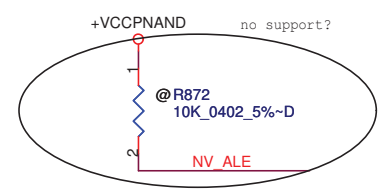
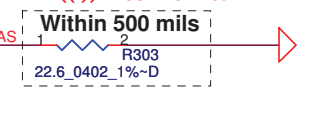


Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

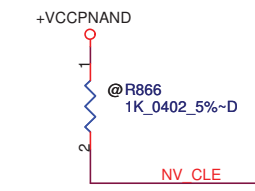
PCH XDP ENABLE	Stuff: R78,R89,R101~R116
	No Stuff: R71,R77,RP1,RP2,R45,R40,R131,R58,R1242,R1243,R1244,R1245,R74,R130
PCH XDP DISABLE	Stuff: R71,R77,RP1,RP2,R45,R40,R131,R58,R1242,R1243,R1244,R1245,R74,R130
	No Stuff: R78,R89,R101~R116



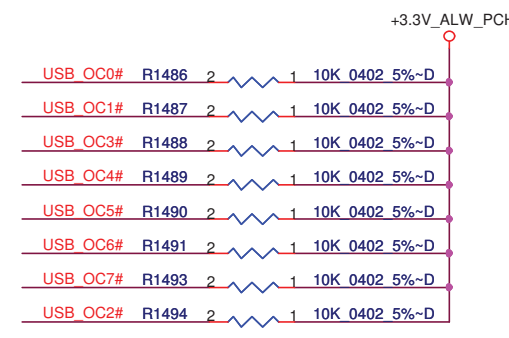
- >Right Side Top
- >USH_BIO
- >Left Side Top
- >Left Side Bottom
- >WLAN
- >WWAN
- >Blue Tooth
- >Express Card
- >DOCK
- >DOCK
- >Right Side Bottom
- >Camera
- >WPAN



Danbury Technology Enabled	
NV_ALE	High = Enabled (Default) Low = Disabled



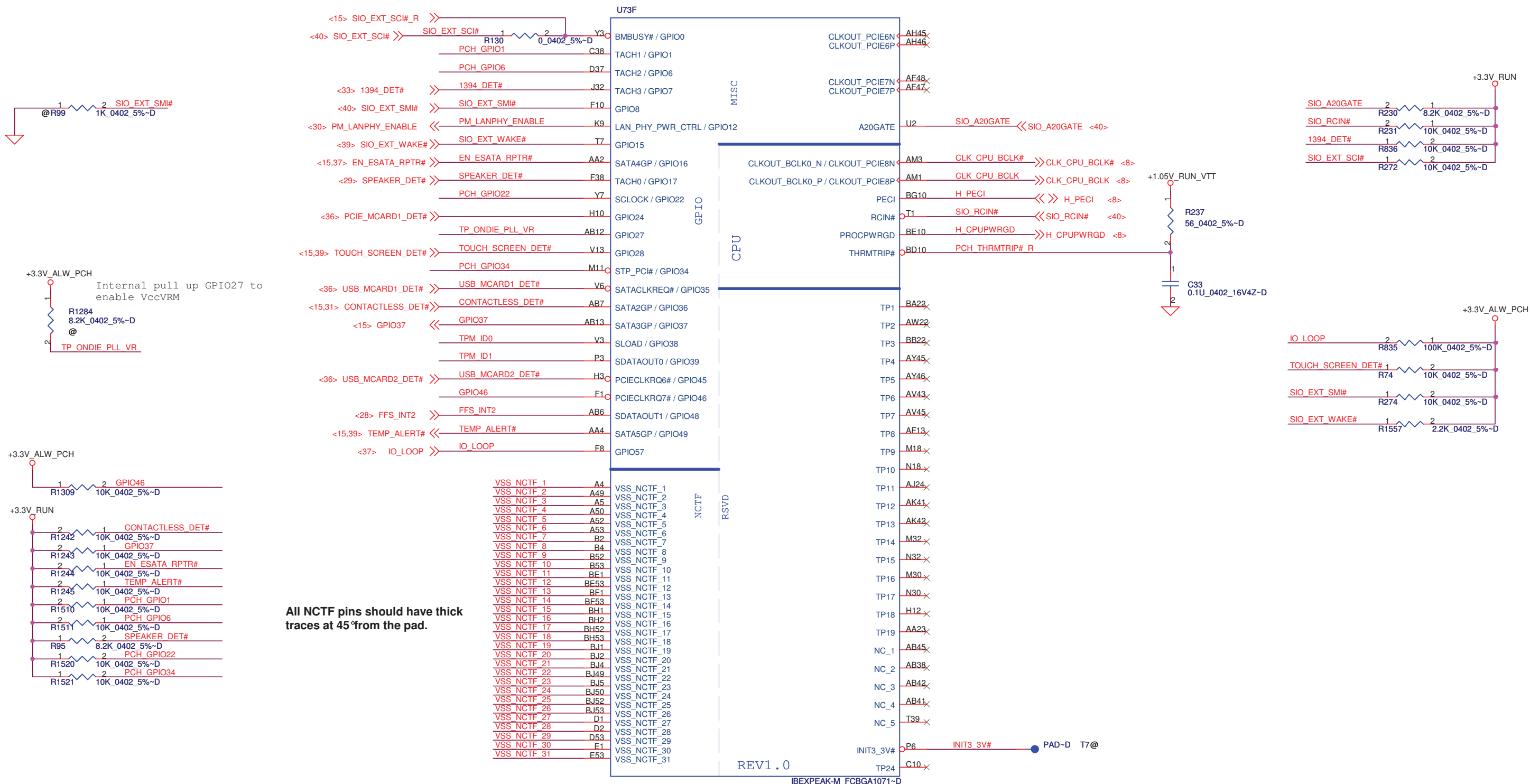
DMI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH



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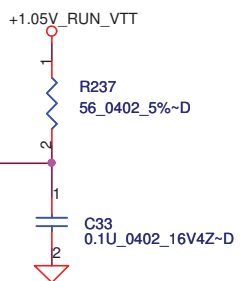
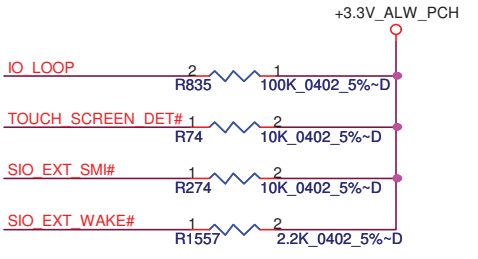
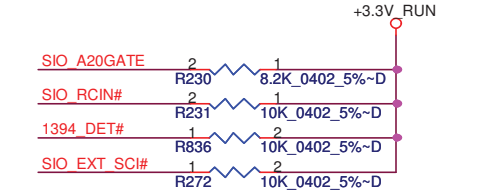
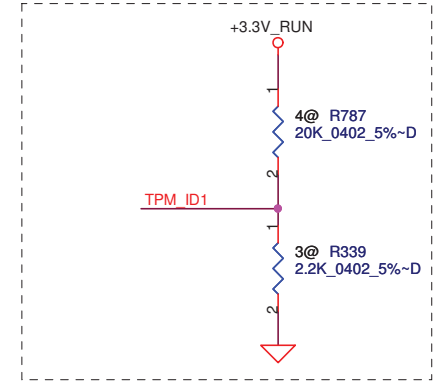
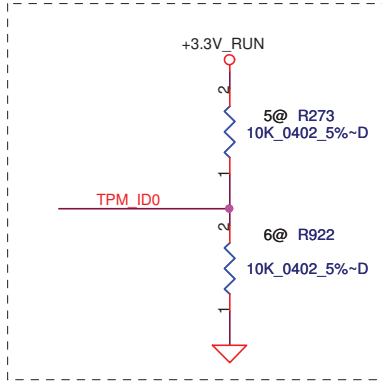
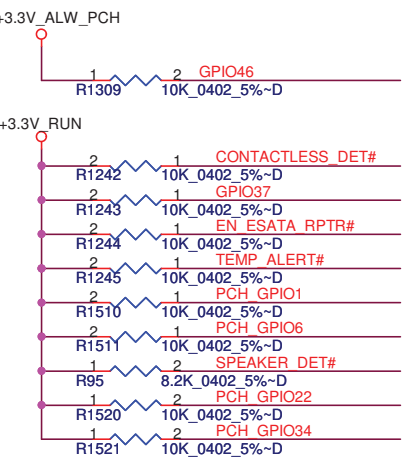
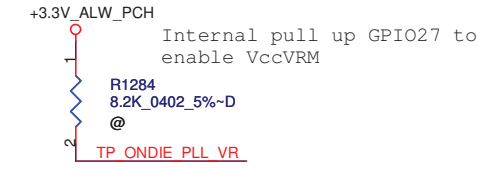
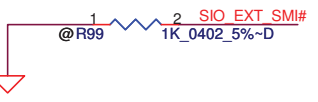


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All NCTF pins should have thick traces at 45° from the pad.

	TPM_ID0	TPM_ID1
China TPM	0	0
No TPM, No China TPM	0	1
Reserved	1	0
TPM	1	1



REV1.0

IBEXPEAK-M_FCBGA1071-D

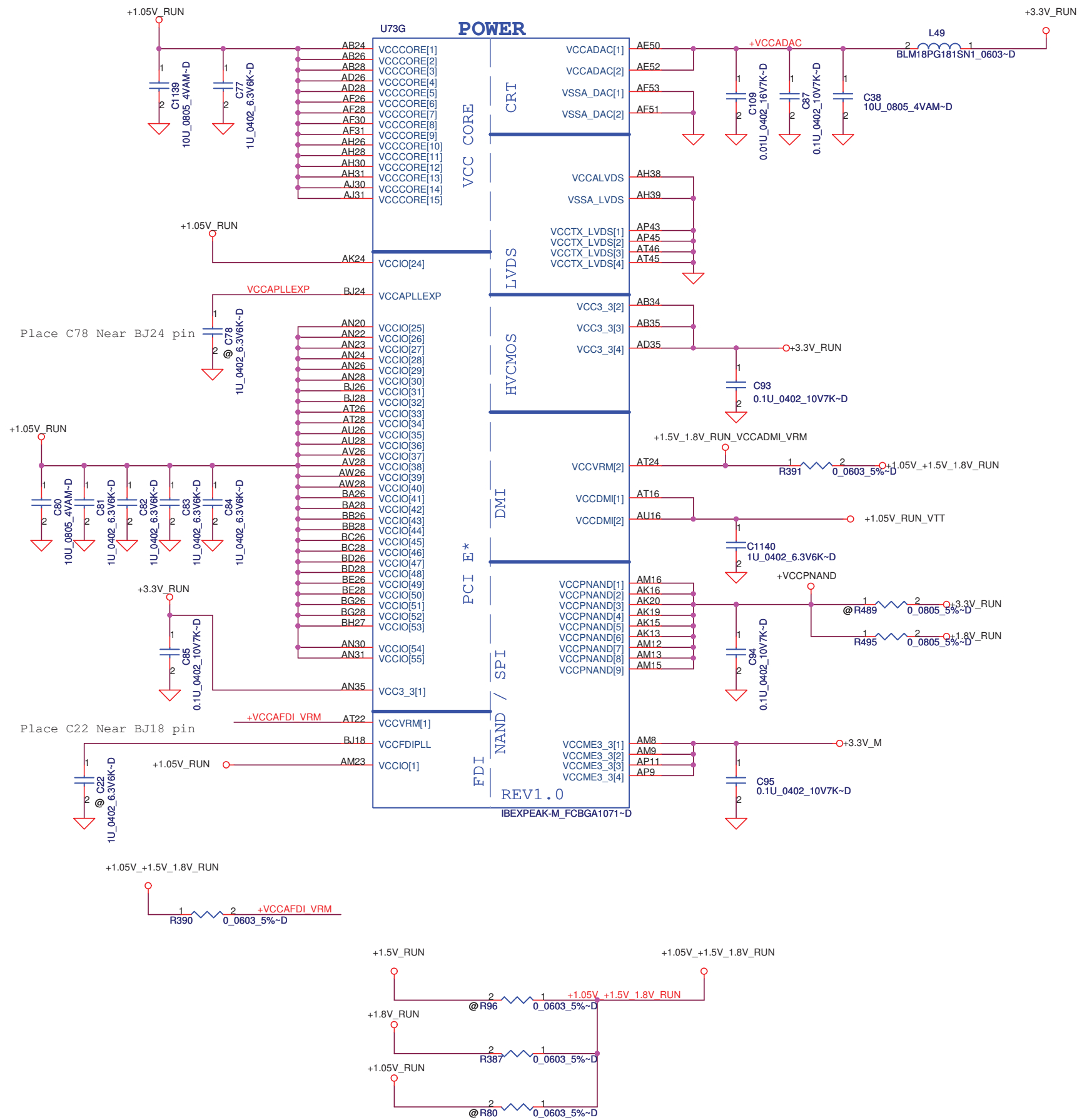


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PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_CPU_IO	1.1/1.05	< 1 (mA)
V5REF	5	< 1 (mA)
V5REF_Sus	5	< 1 (mA)
Vcc3_3	3.3	0.357
VccAClk	1.1	0.052
VccADAC	3.3	0.069
VccADPLL	1.1	0.068
VccADPLLb	1.1	0.069
Vccap1LEXP	1.1	0.04
VccCore	1.1	1.432
VccDMI	1.1	0.058
VccDMI	1.1	0.061
VccFDIPLL	1.1	0.037
VccIO	1.1	3.062
VccLAN	1.1	0.32
VccME	1.1	1.849
VccME3_3	3.3	0.085
VccpNAND	1.8	0.156
VccRTC	3.3	2 (mA)
VccSATAPLL	1.1	0.031
VccSus3_3	3.3	0.163
VccSusHDA	3.3	0.006
VccVRM	1.8 / 1.5	0.196
VccVRM	1.05	< 1 (mA)
VccALVDS	3.3	< 1 (mA)
VccTX_LVDS	1.8	0.059

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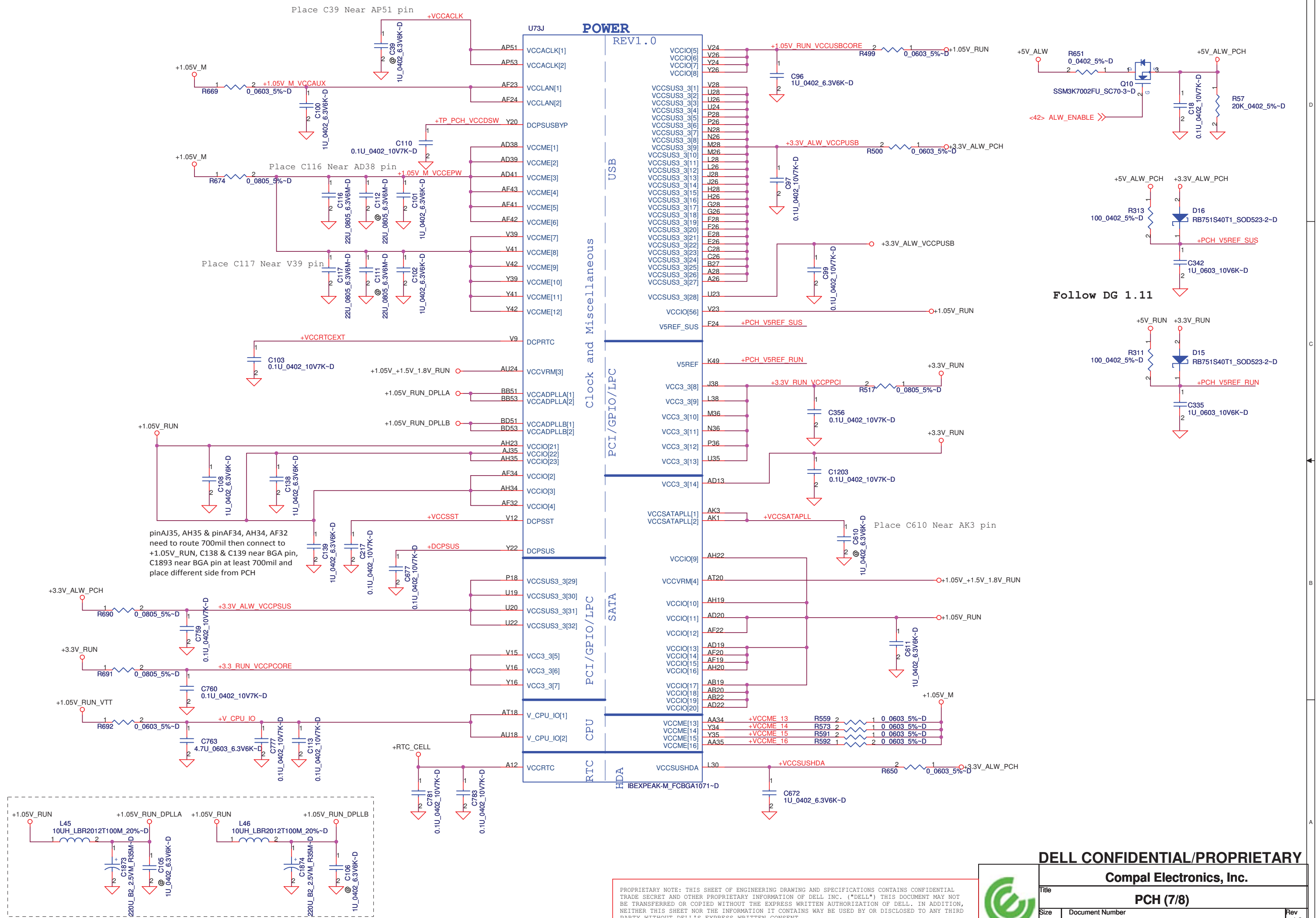
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Follow DG 1.11

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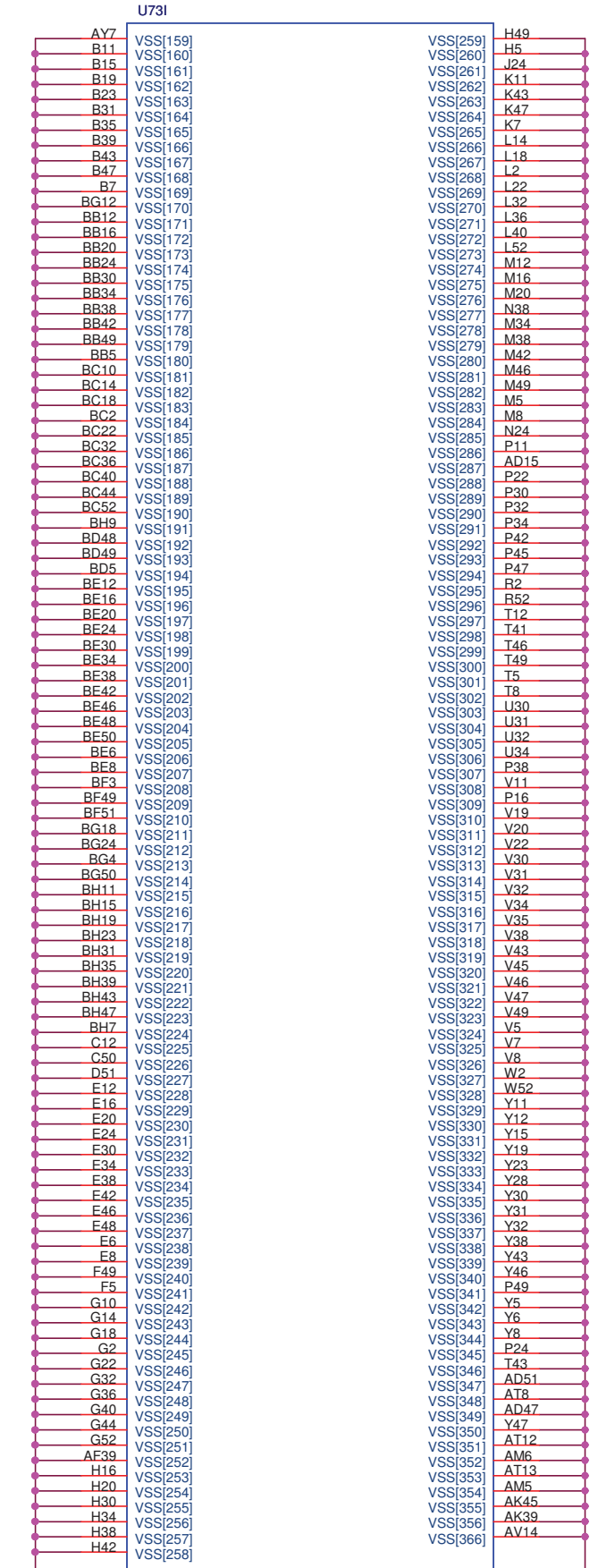
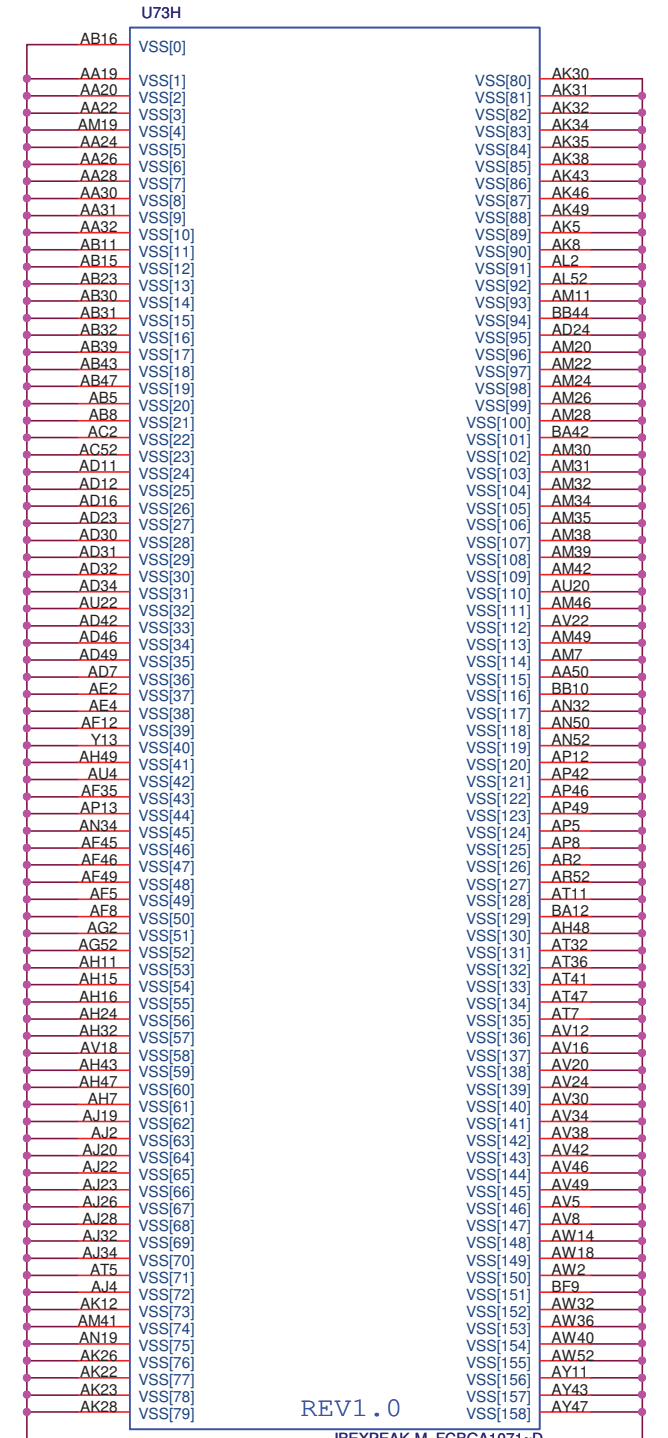
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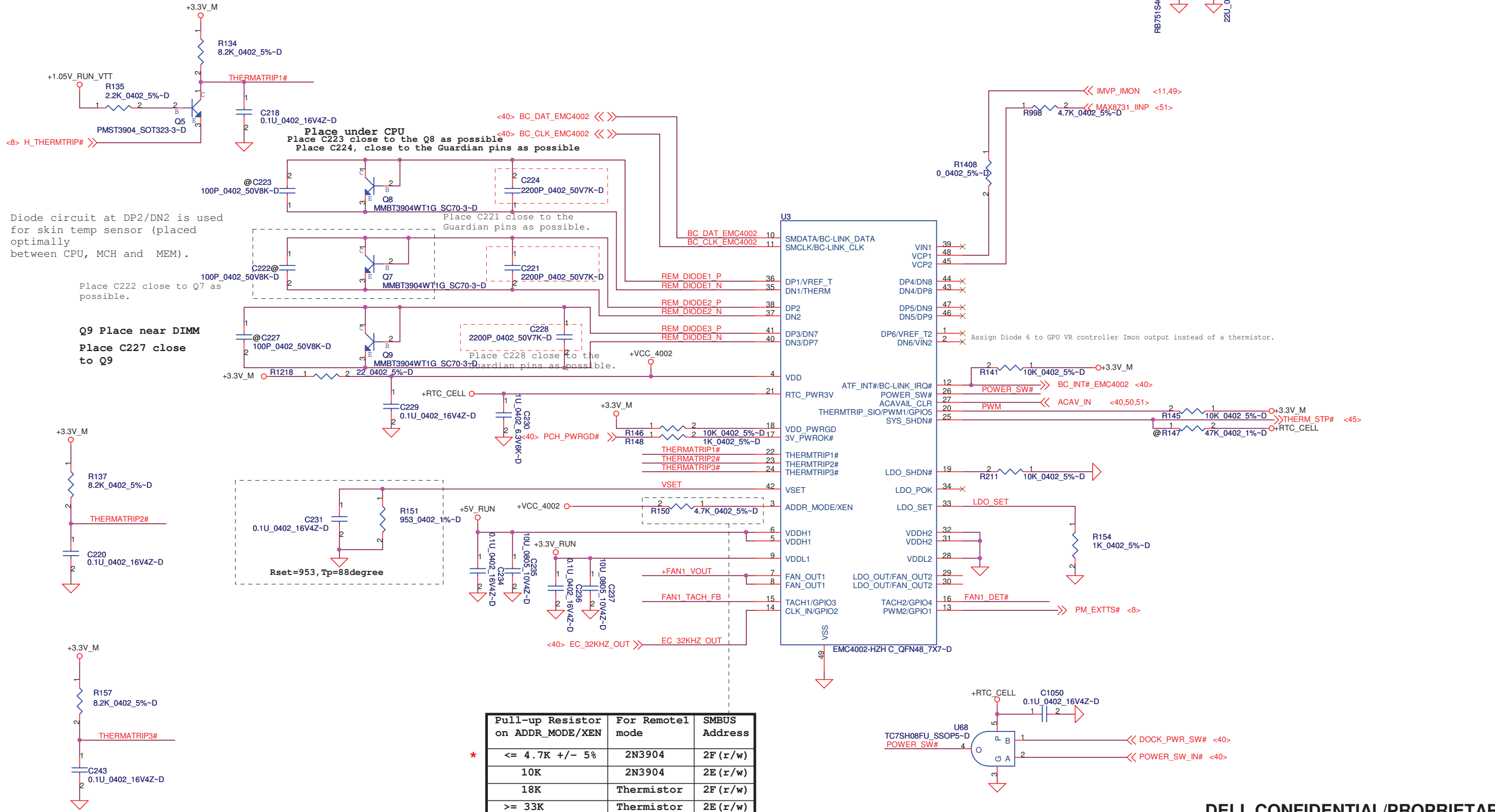


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Diode circuit at DP2/DN2 is used for skin temp sensor (placed optimally between CPU, MCH and MEM).

Place C222 close to Q7 as possible.

Q9 Place near DIMM Place C227 close to Q9

Place under CPU Place C223 close to the Q8 as possible Place C224, close to the Guardian pins as possible

Place C221 close to the Guardian pins as possible.

Rset=953, Tp=88degree

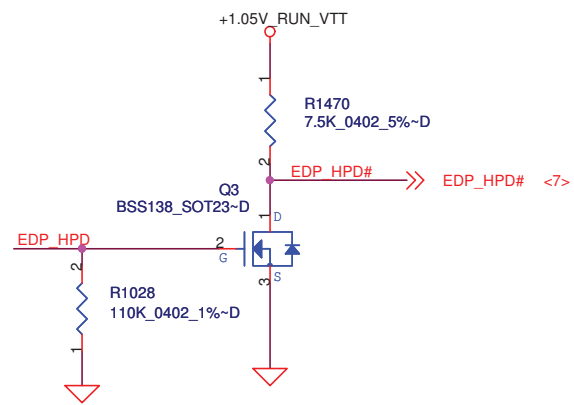
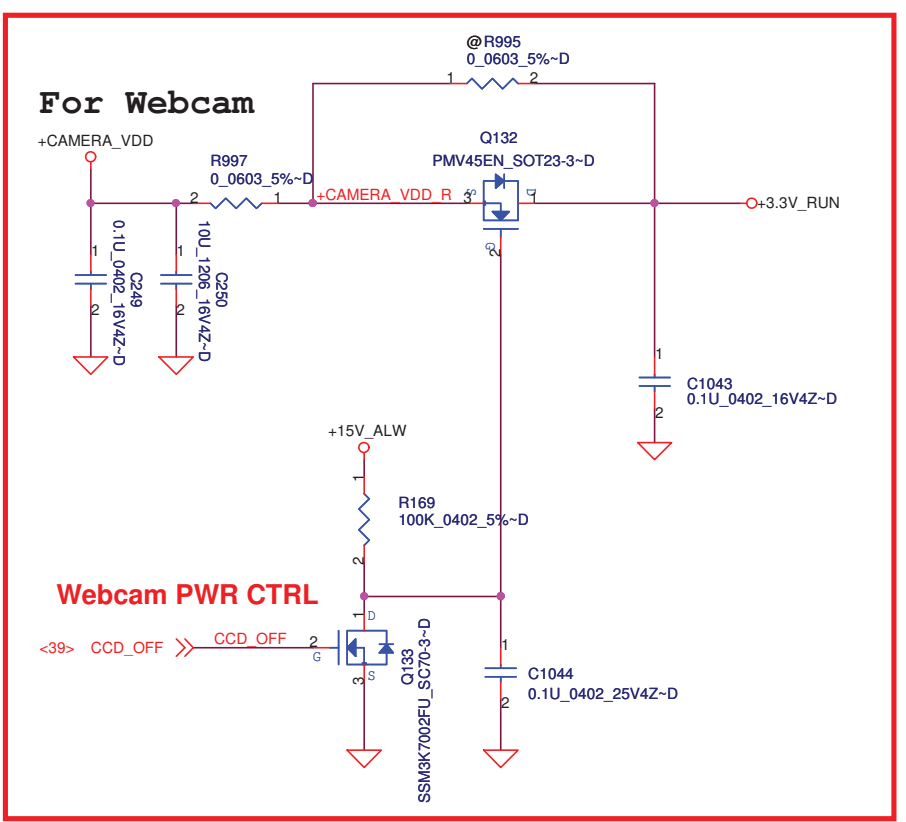
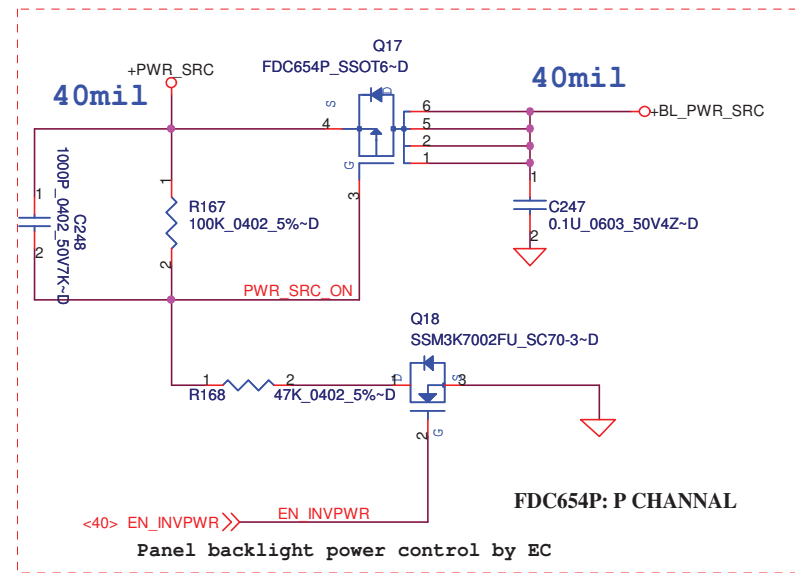
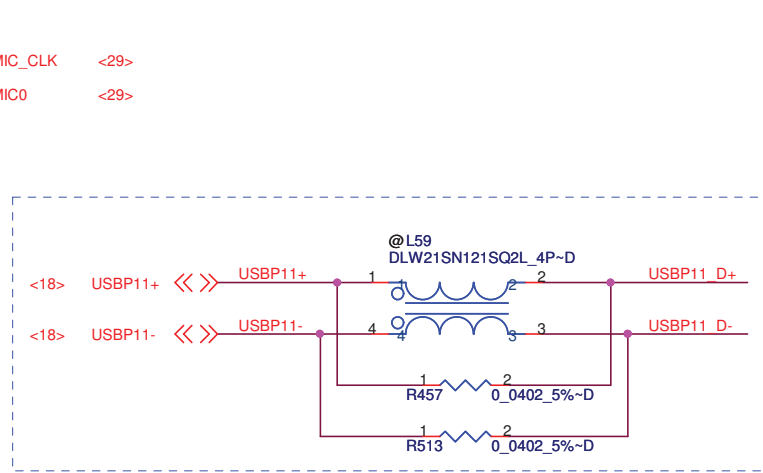
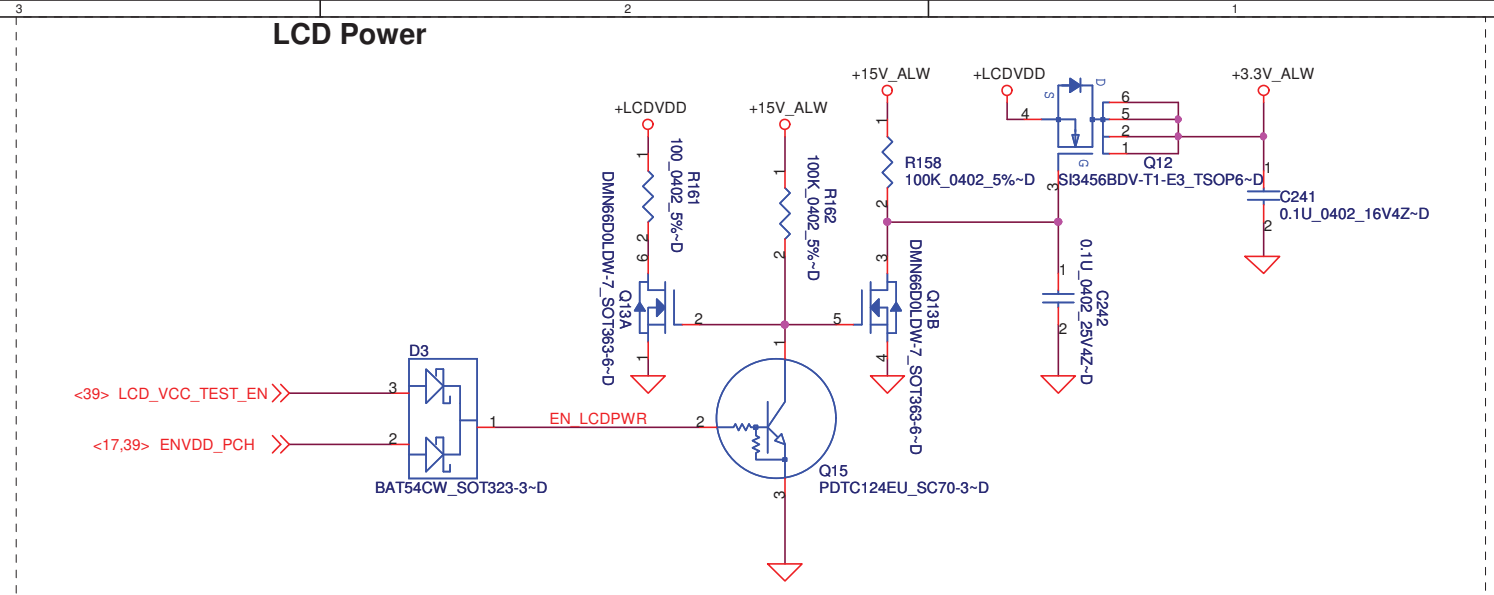
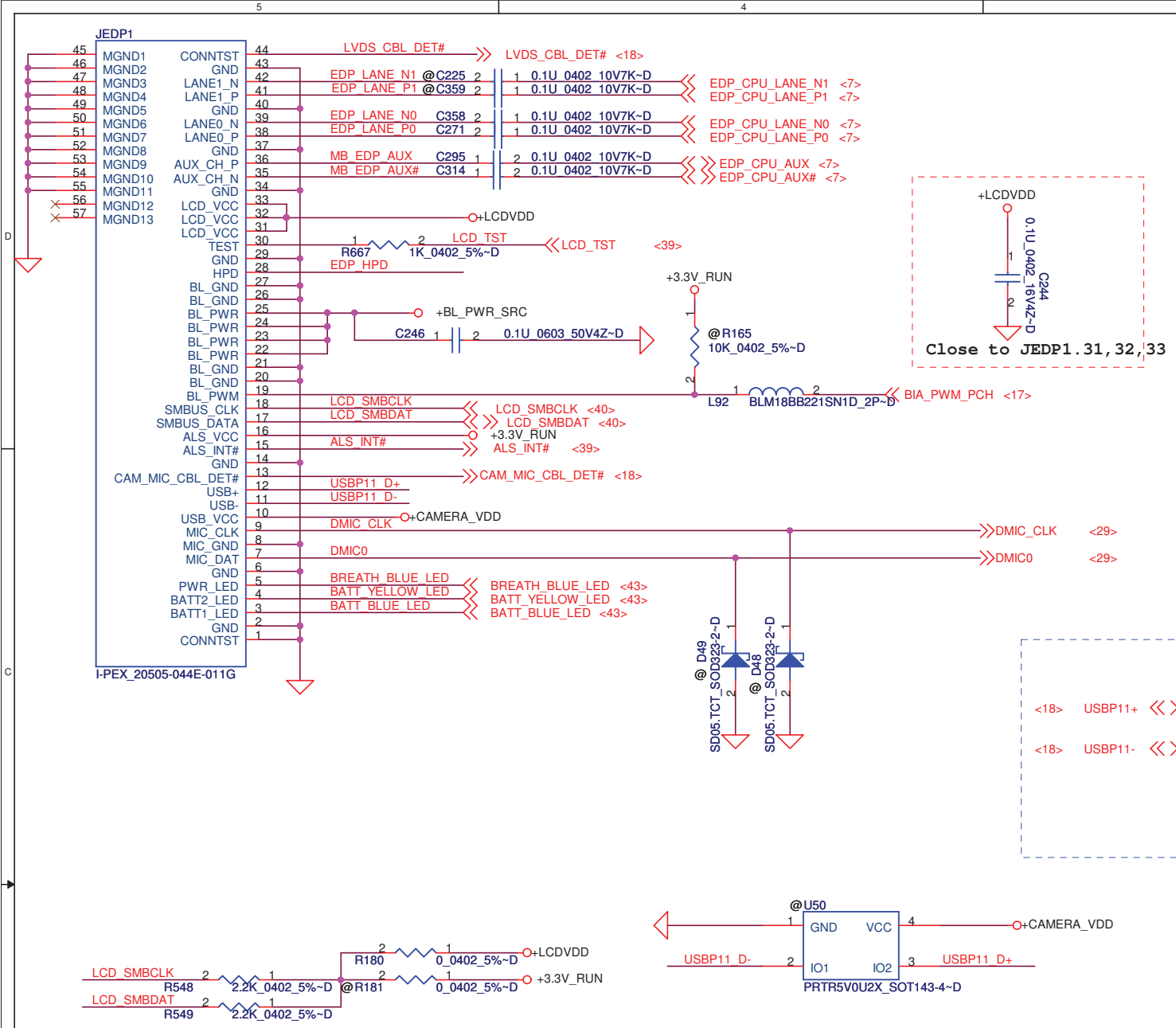
Pull-up Resistor on ADDR_MODE/XEN	For Remote mode	SMBUS Address
<= 4.7K +/- 5%	2N3904	2F (r/w)
10K	2N3904	2E (r/w)
18K	Thermistor	2F (r/w)
>= 33K	Thermistor	2E (r/w)

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Title FAN & Thermal Sensor		
Size	Document Number LA-5471P	Rev 1.0
Date: Wednesday, January 20, 2010	Sheet 23	of 57



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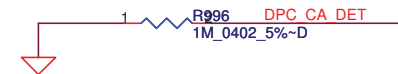
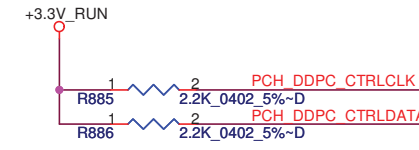
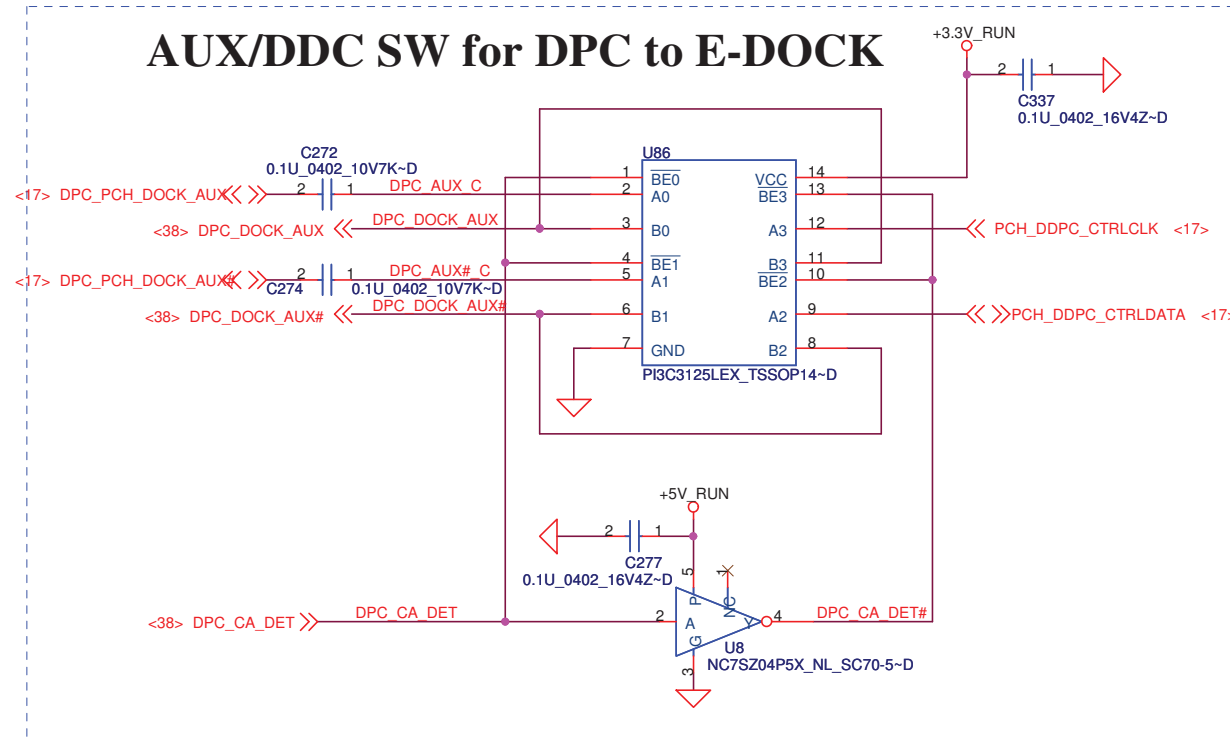
Compal Electronics, Inc.

Title: **eDP & CAM Conn**

Size: Document Number **LA-5471P** Rev 1.0


Date: Wednesday, January 20, 2010 Sheet 24 of 57

AUX/DDC SW for DPC to E-DOCK



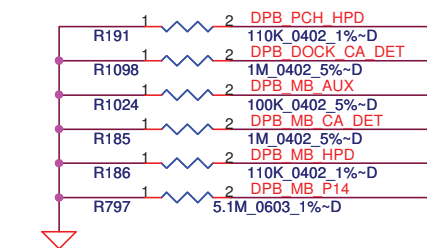
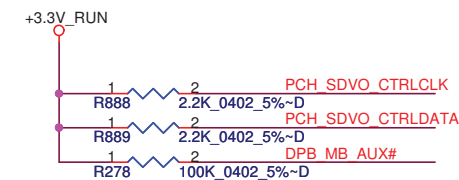
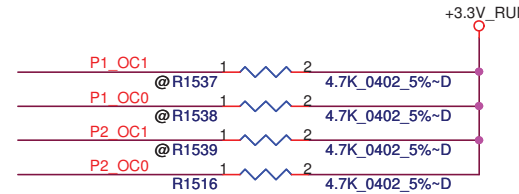
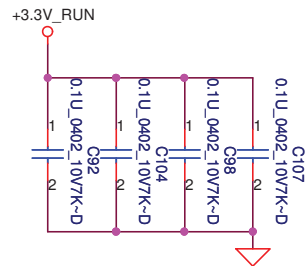
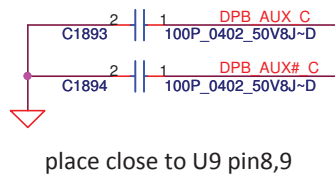
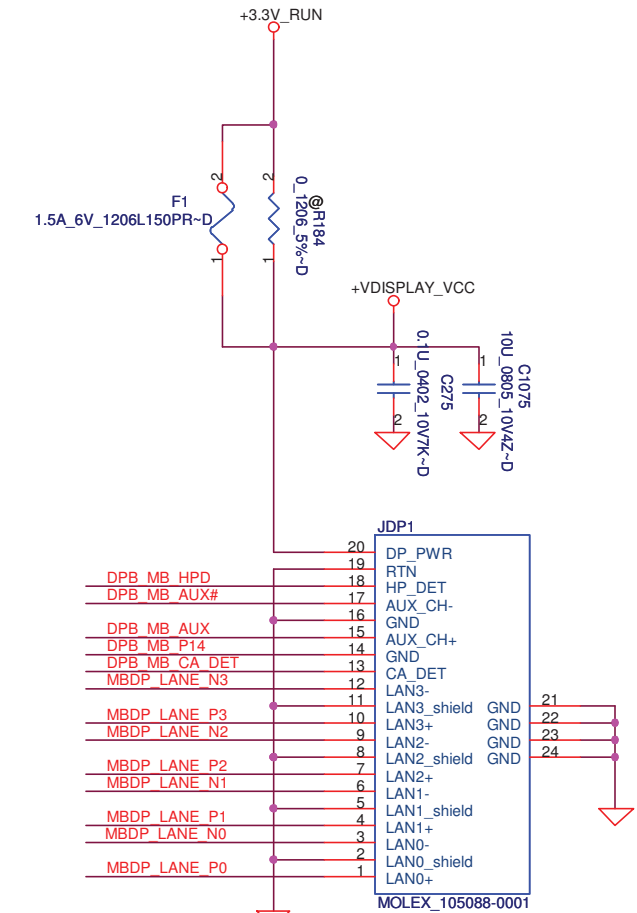
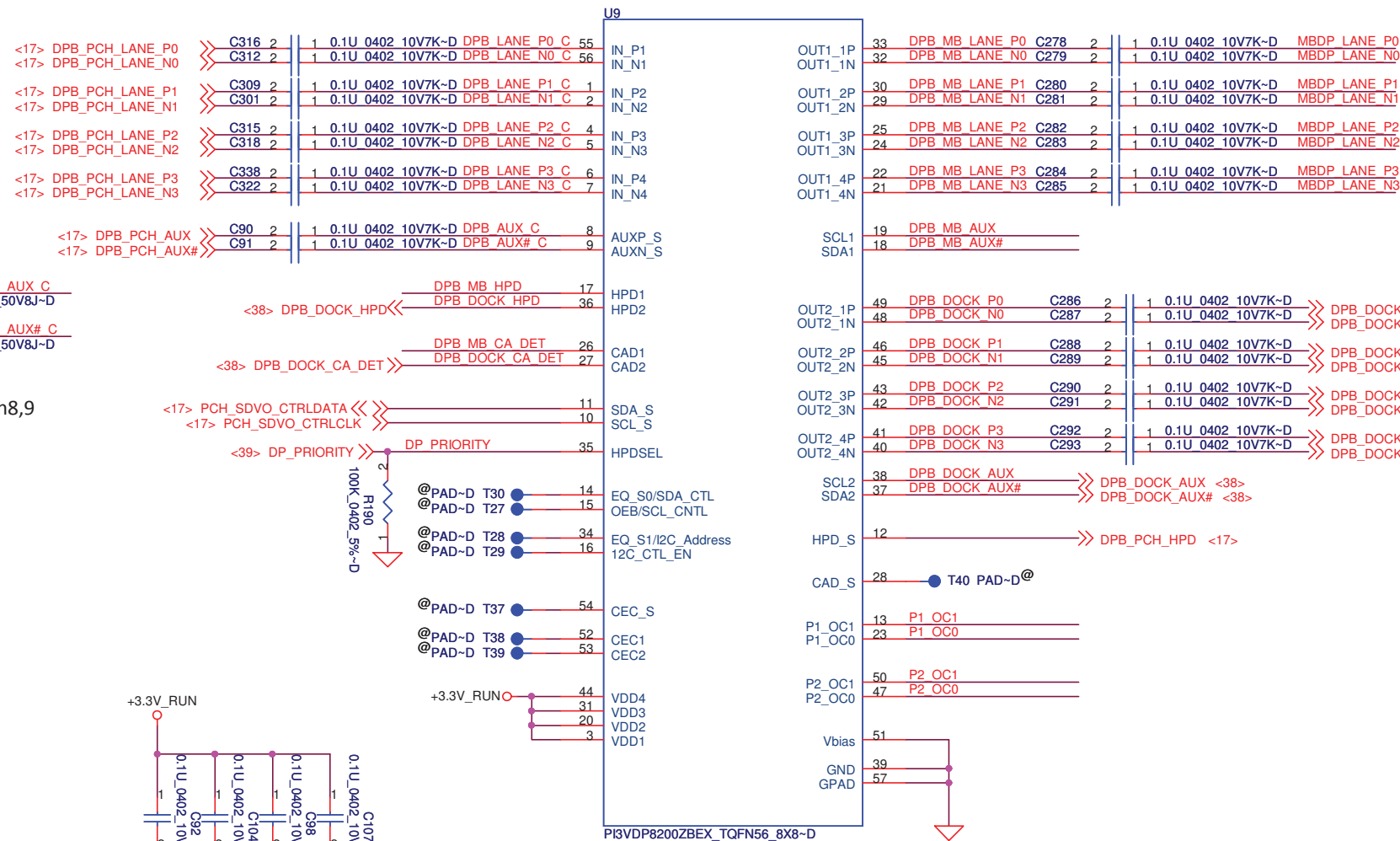
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		Compal Electronics, Inc.	
		DPC DPD SW for DOCK	
Size	Document Number	LA-5471P	
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Display port Connector

DPB SW for MB & DOCK



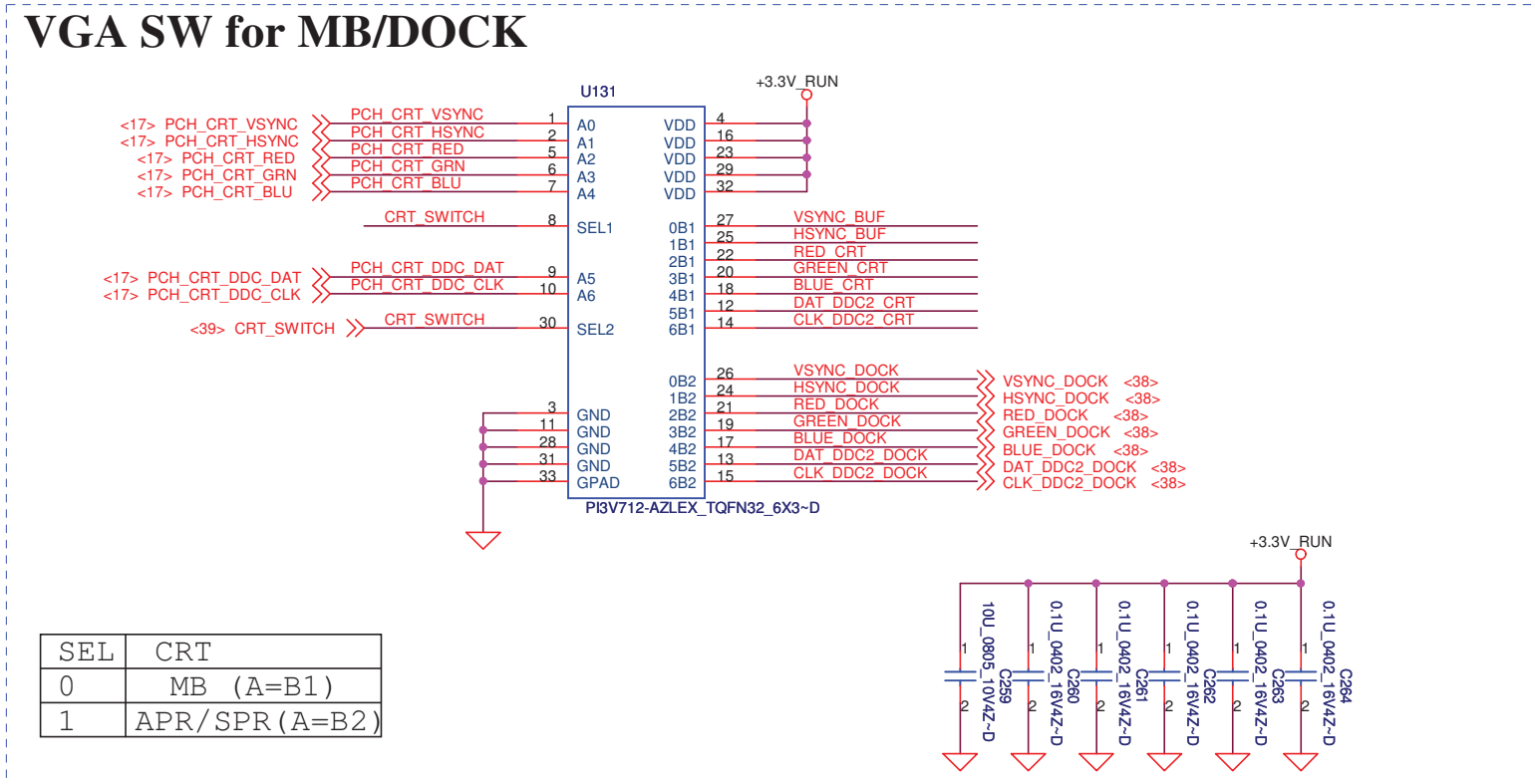
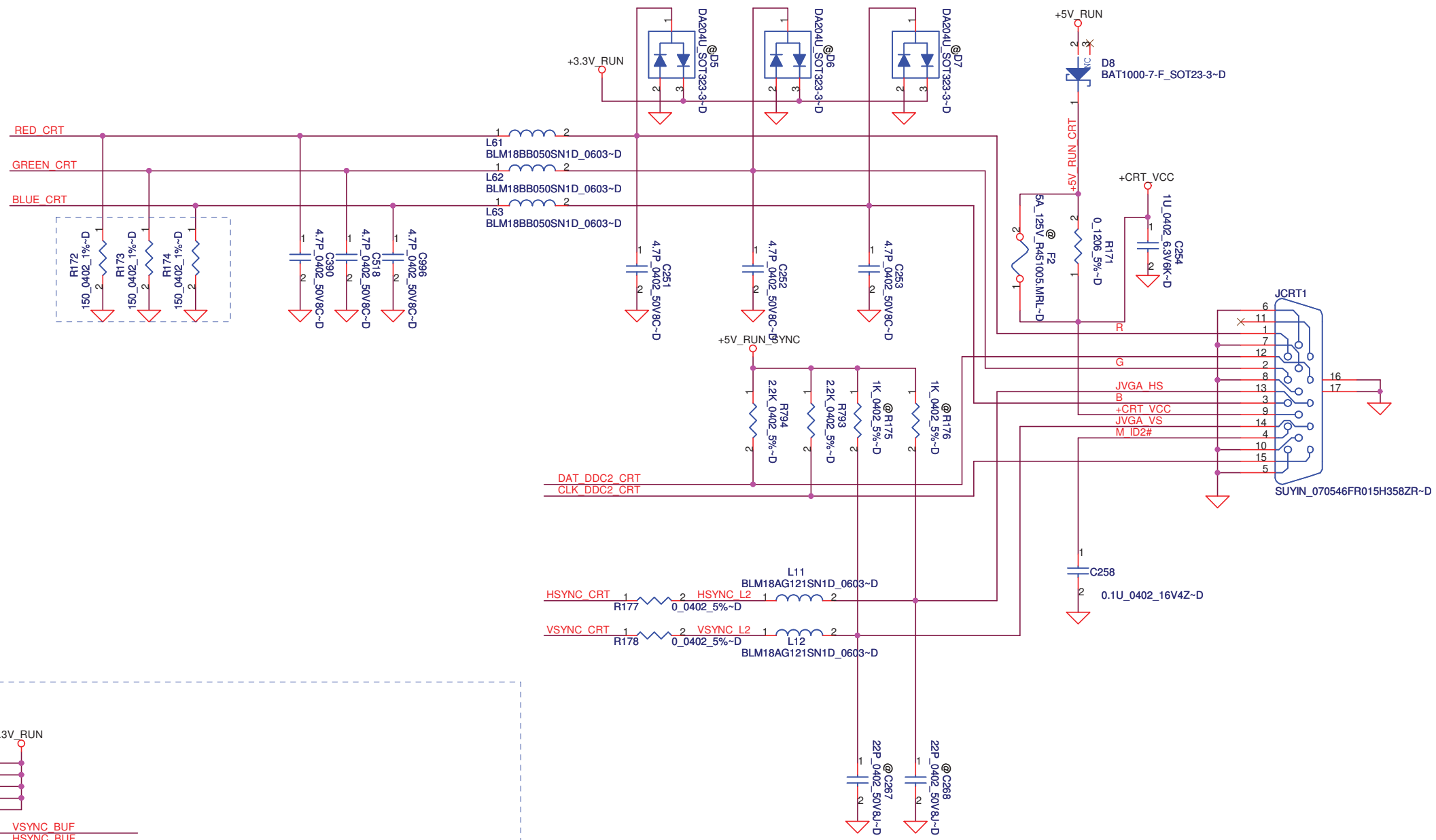
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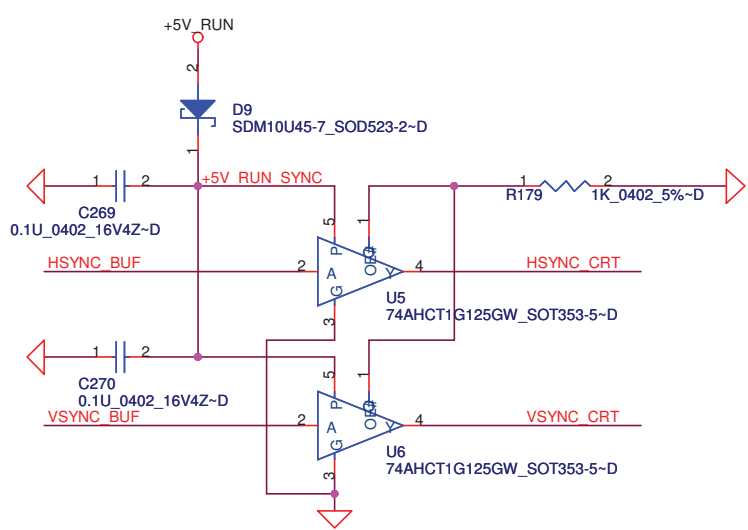


Title		Display port	
Size	Document Number	LA-5471P	
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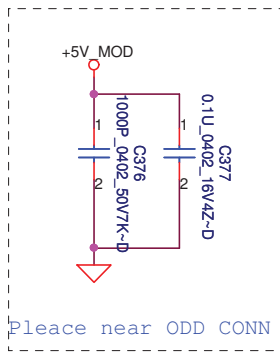
SEL	CRT
0	MB (A=B1)
1	APR/SPR (A=B2)



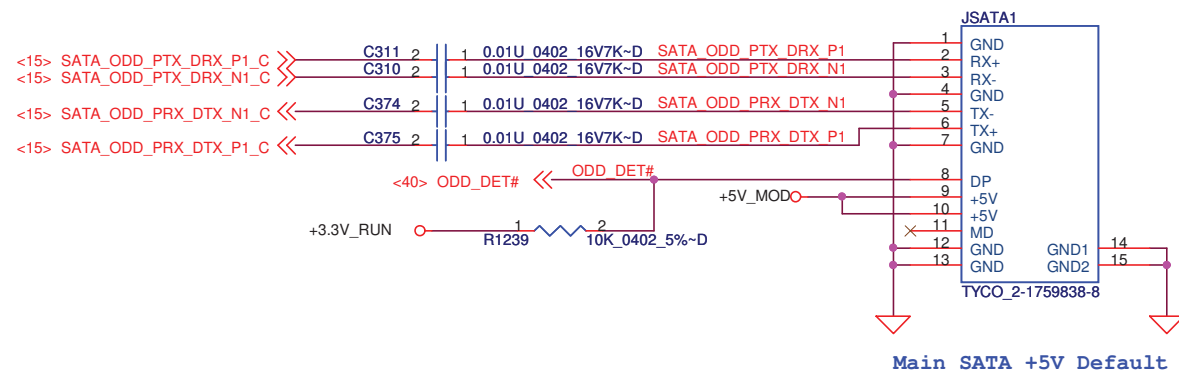
DELL CONFIDENTIAL/PROPRIETARY

		Compal Electronics, Inc.	
		CRT/Video switch	
Size	Document Number	LA-5471P	
Date:	Wednesday, January 20, 2010	Sheet	27 of 57
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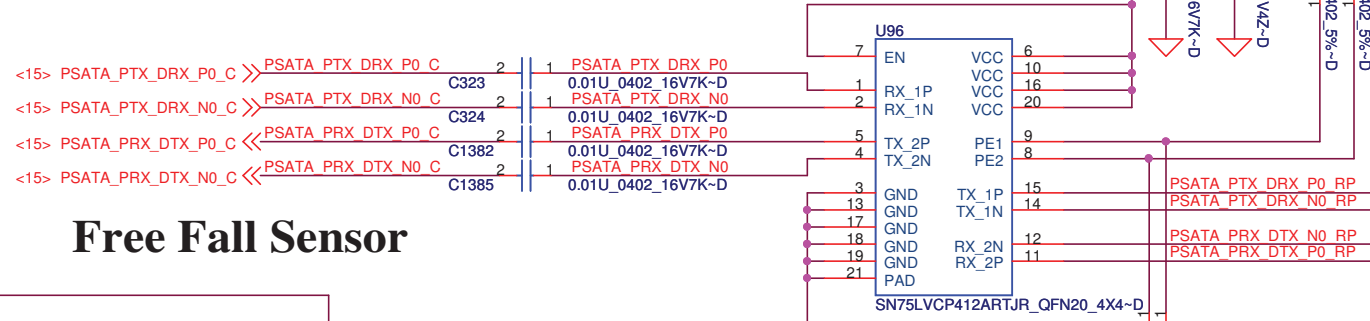


For ODD

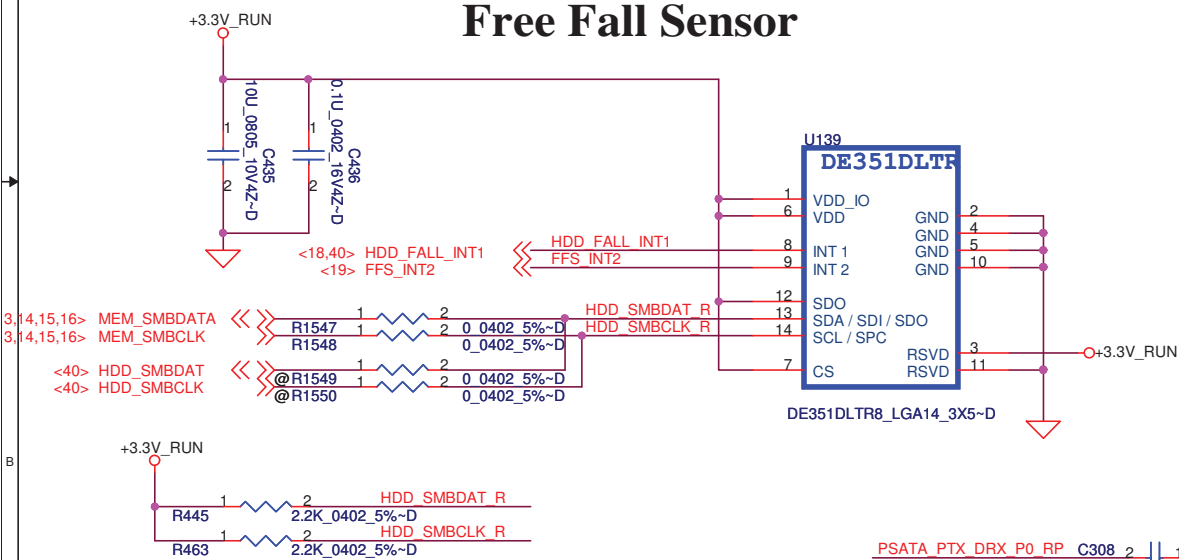


Main SATA +5V Default

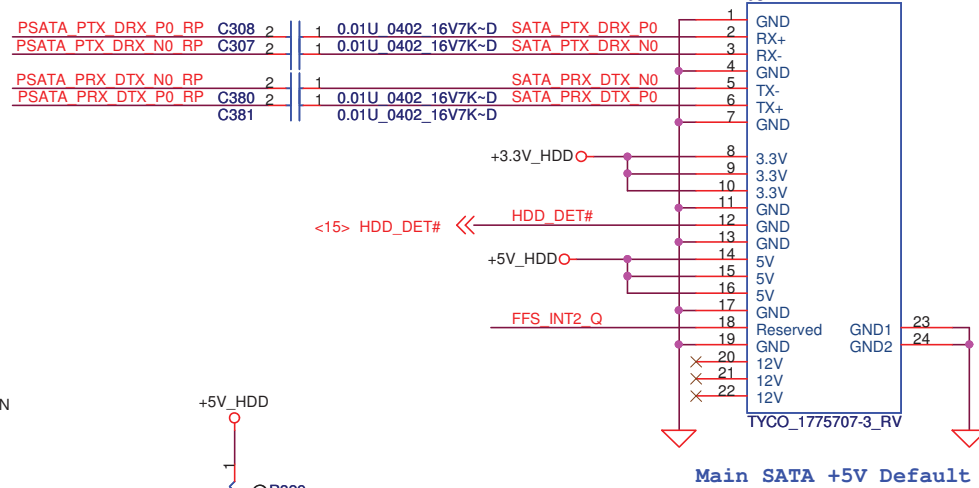
HDD Repeater



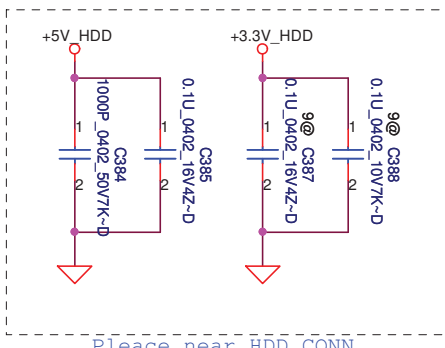
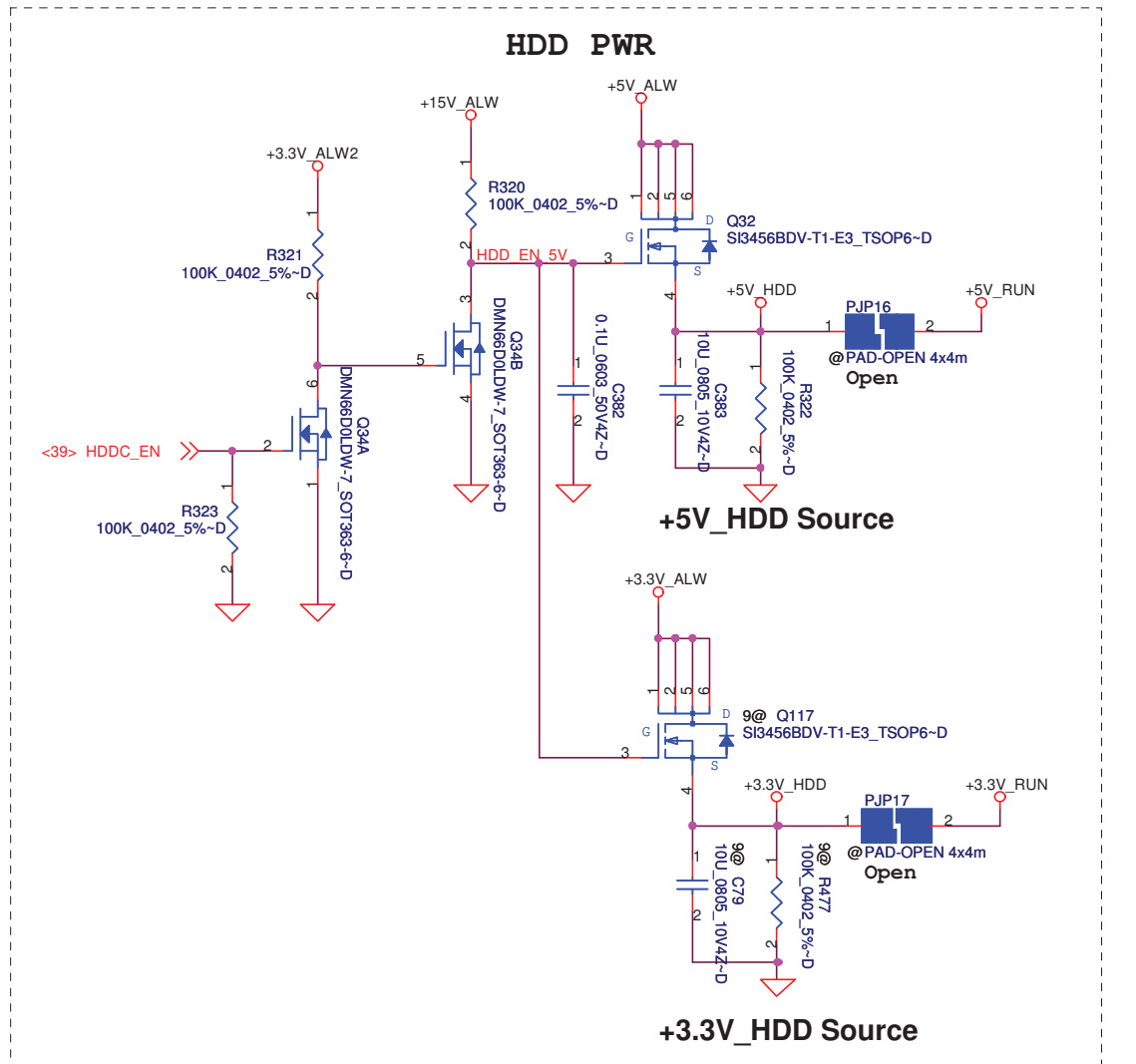
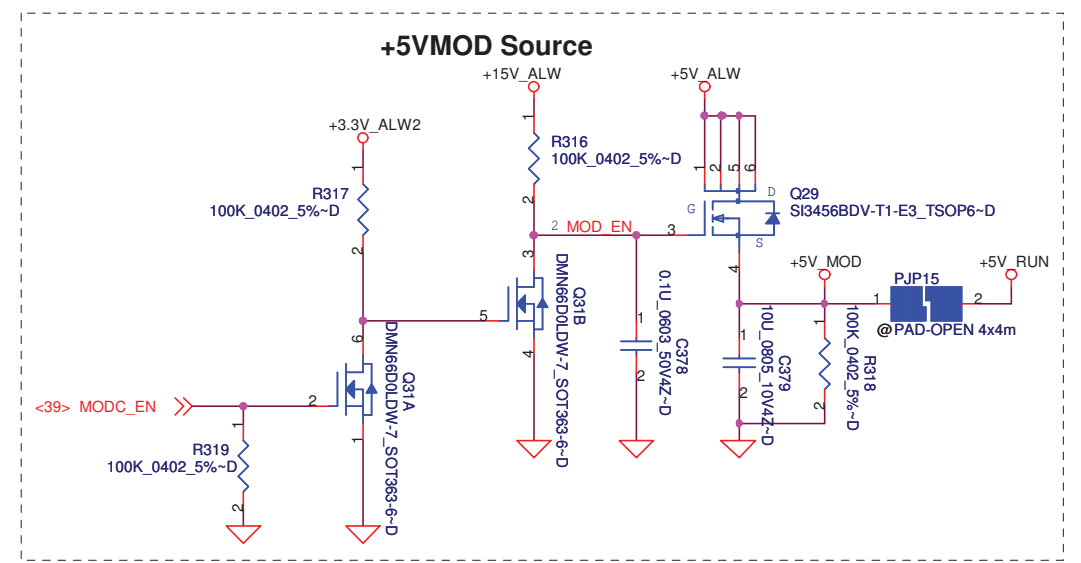
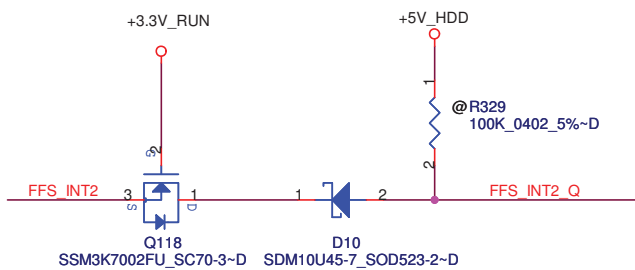
Free Fall Sensor



For HDD



Main SATA +5V Default



Please near HDD CONN

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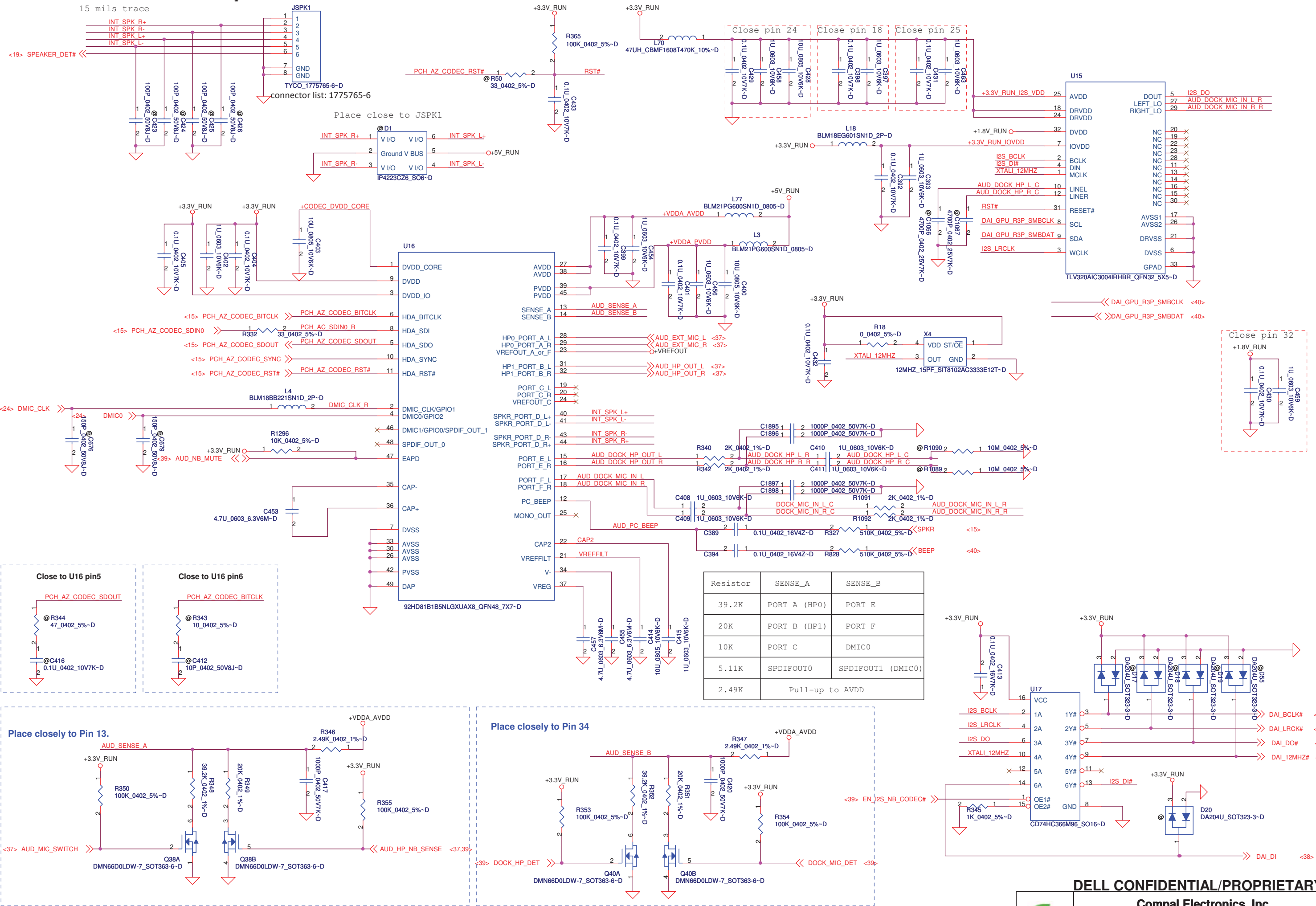
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Title			ODD/HDD CONNECTOR		
Size	Document Number	Rev			1.0
	LA-5471P	Date:	Wednesday, January 20, 2010	Sheet	28 of 57

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Speaker Connector



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Azalia (HD) Codec

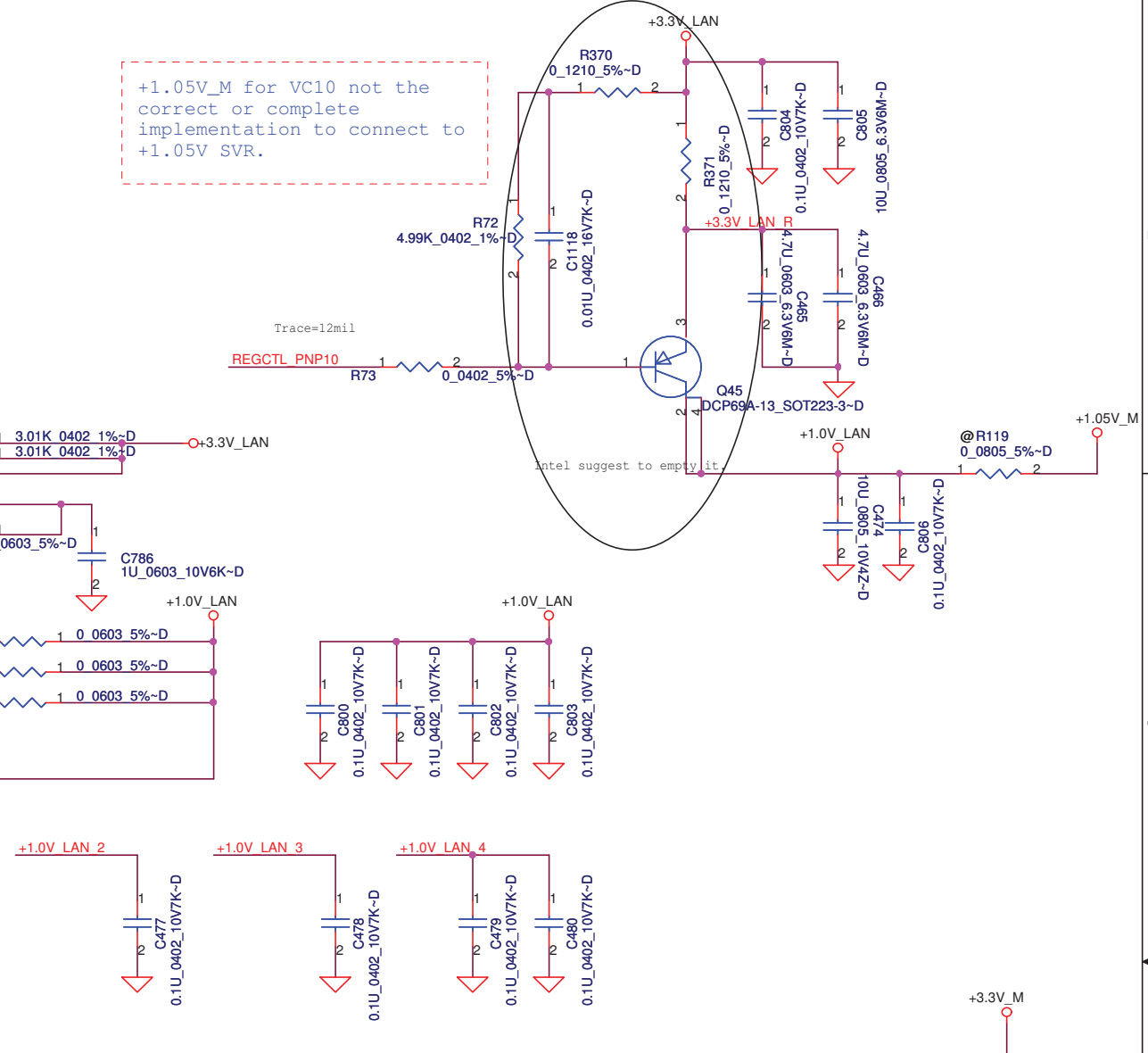
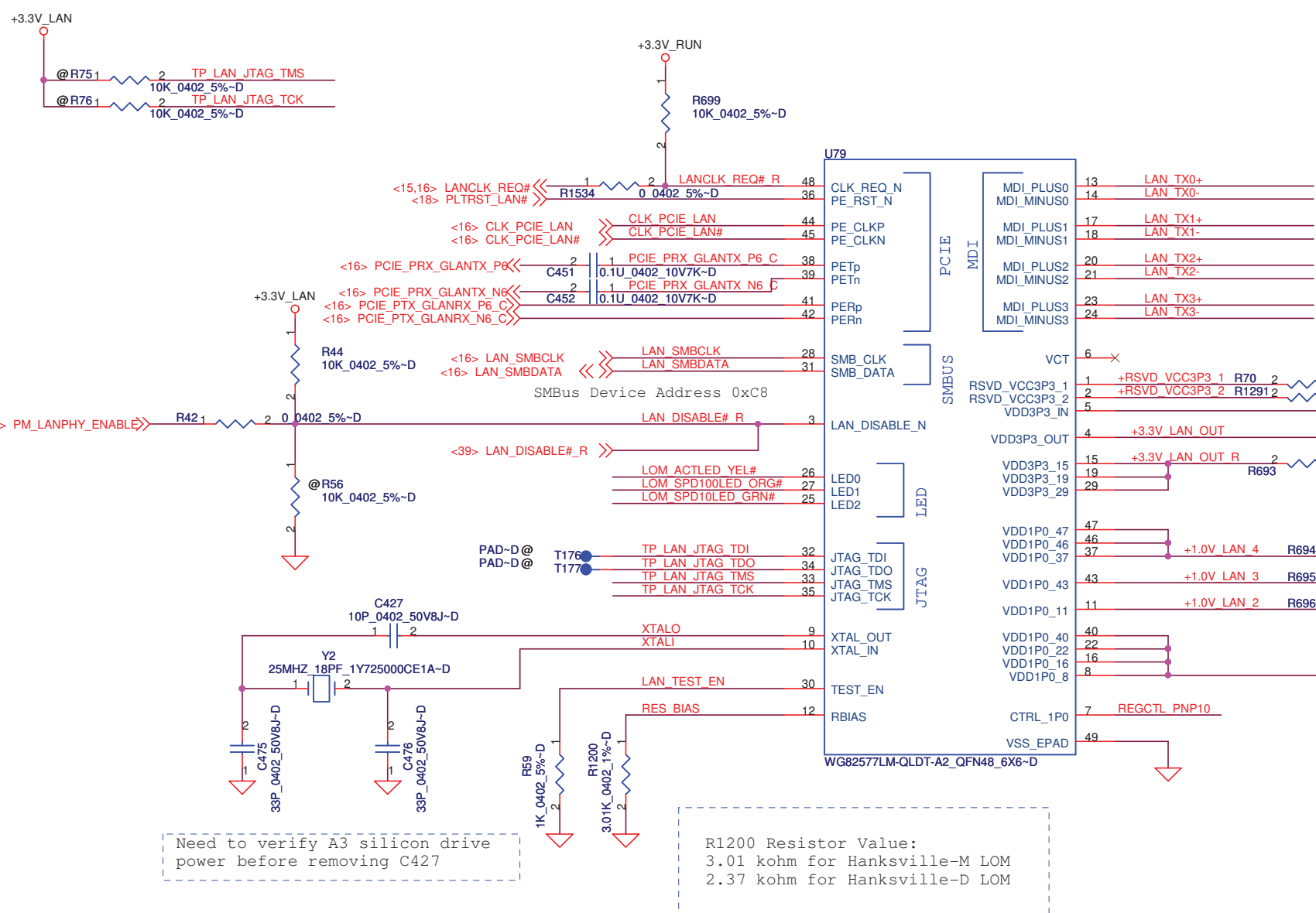
LA-5471P

Rev 1.0

Date: Wednesday, January 20, 2010

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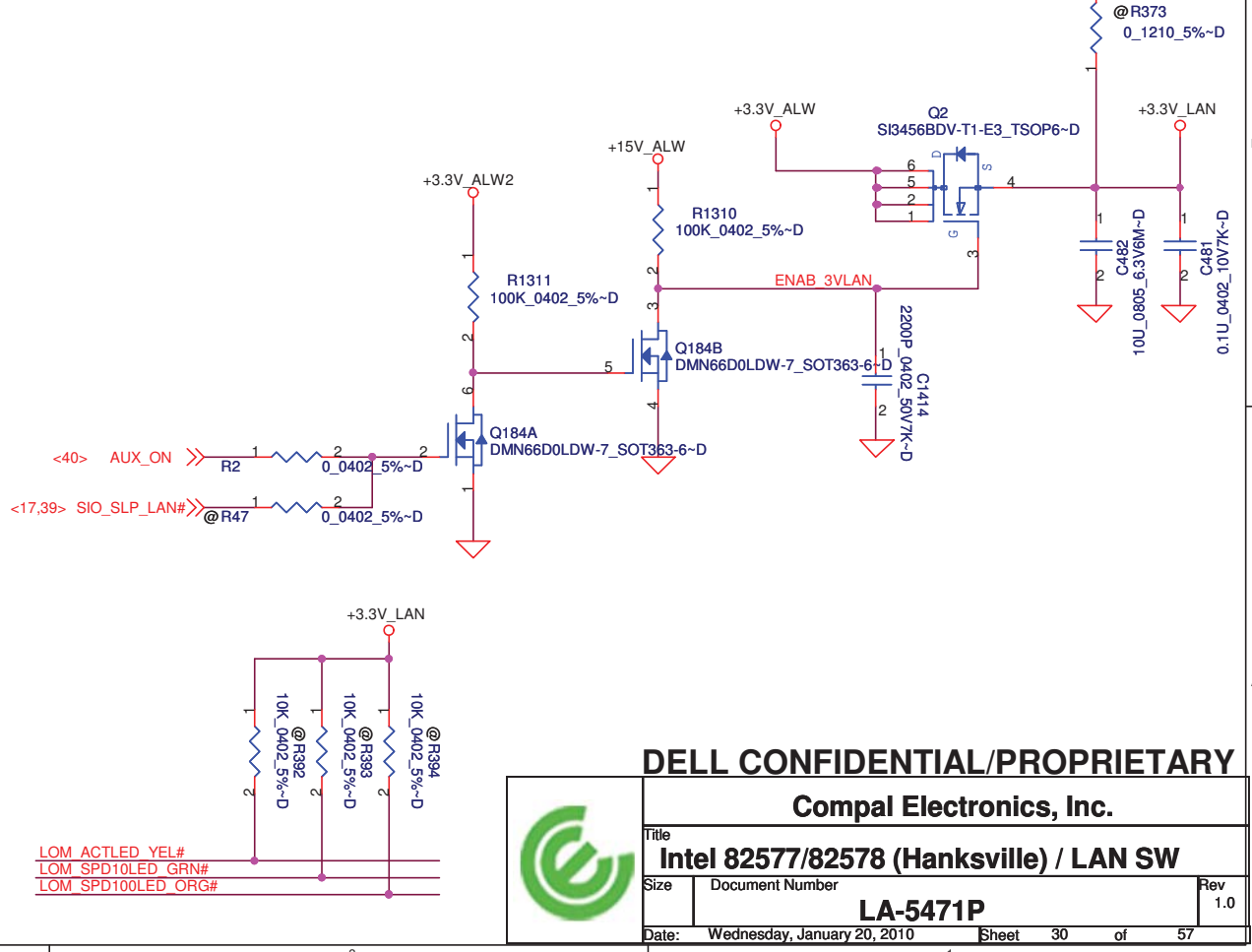
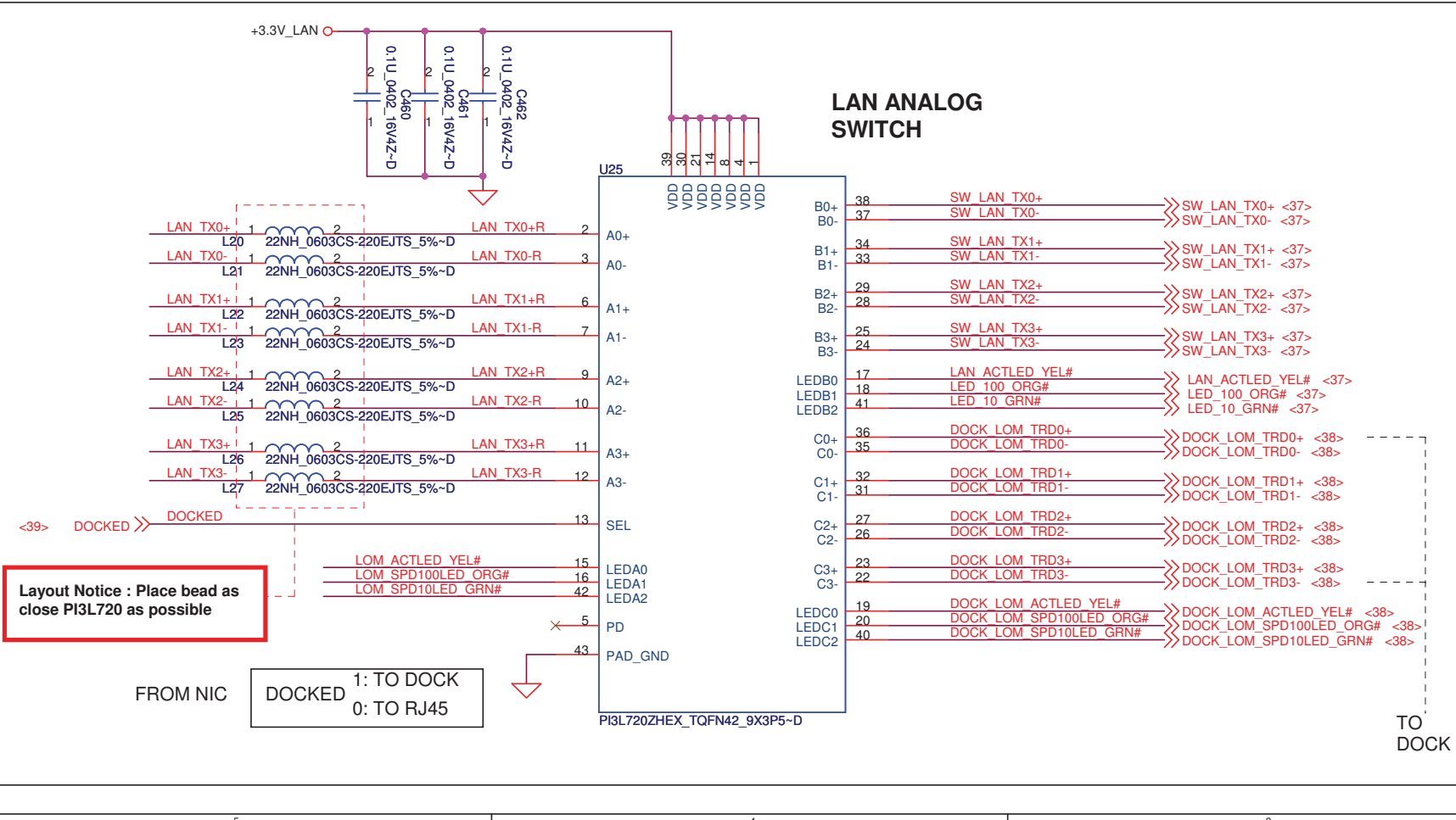
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Need to verify A3 silicon drive power before removing C427

R1200 Resistor Value:
3.01 kohm for Hanksville-M LOM
2.37 kohm for Hanksville-D LOM

+1.05V_M for VC10 not the correct or complete implementation to connect to +1.05V SVR.



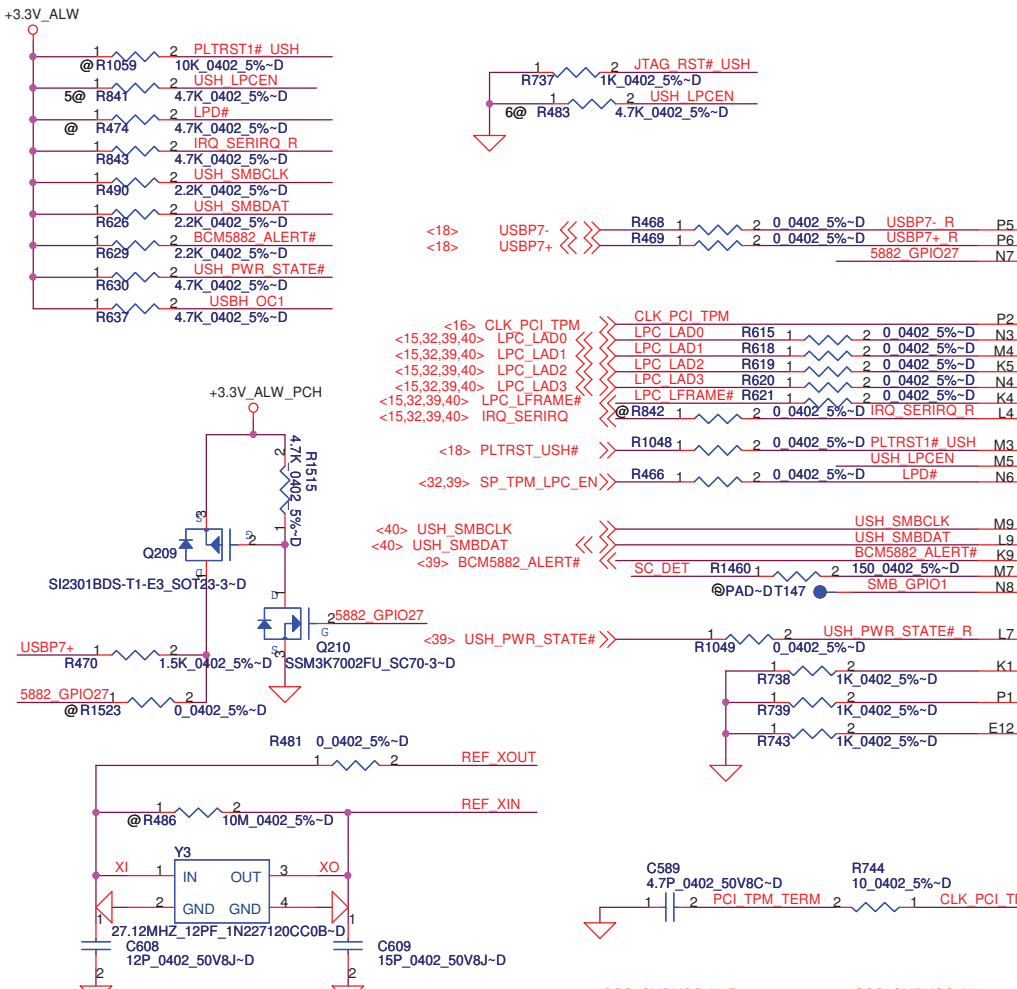
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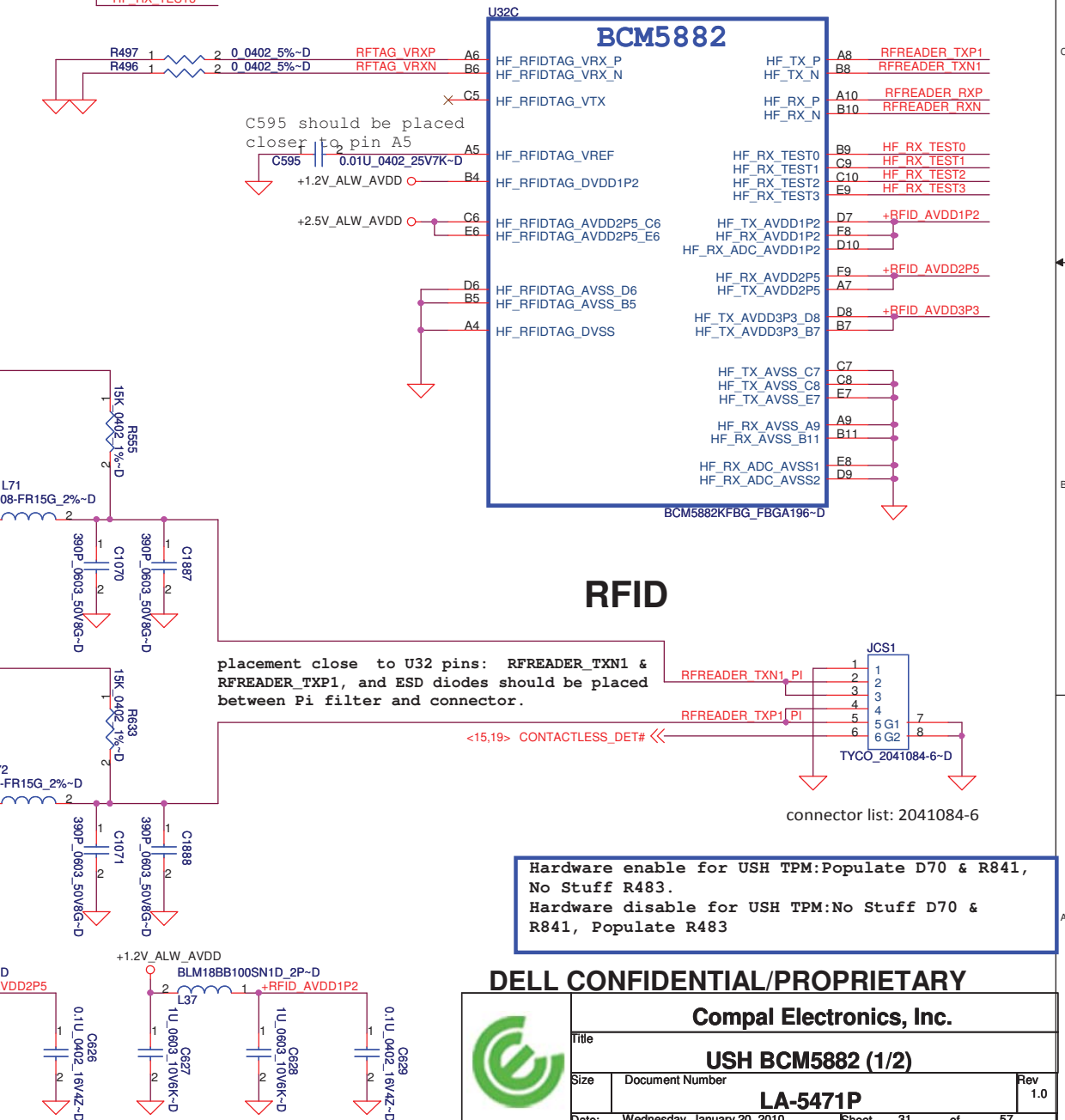
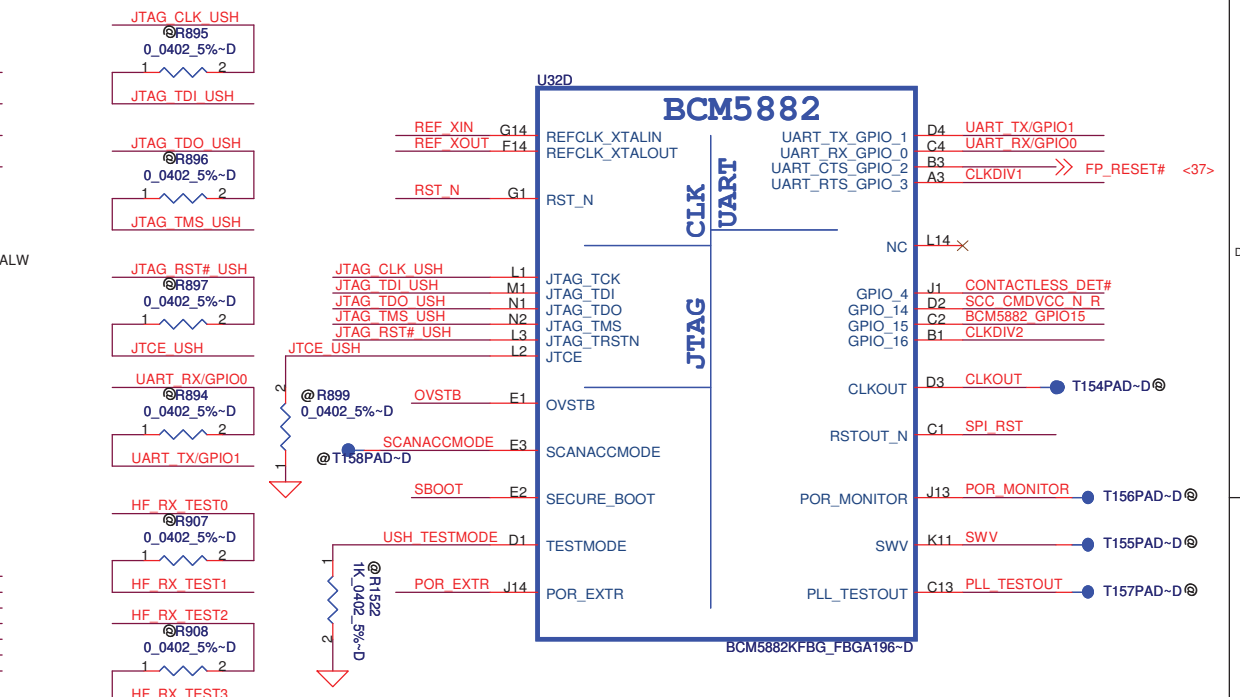
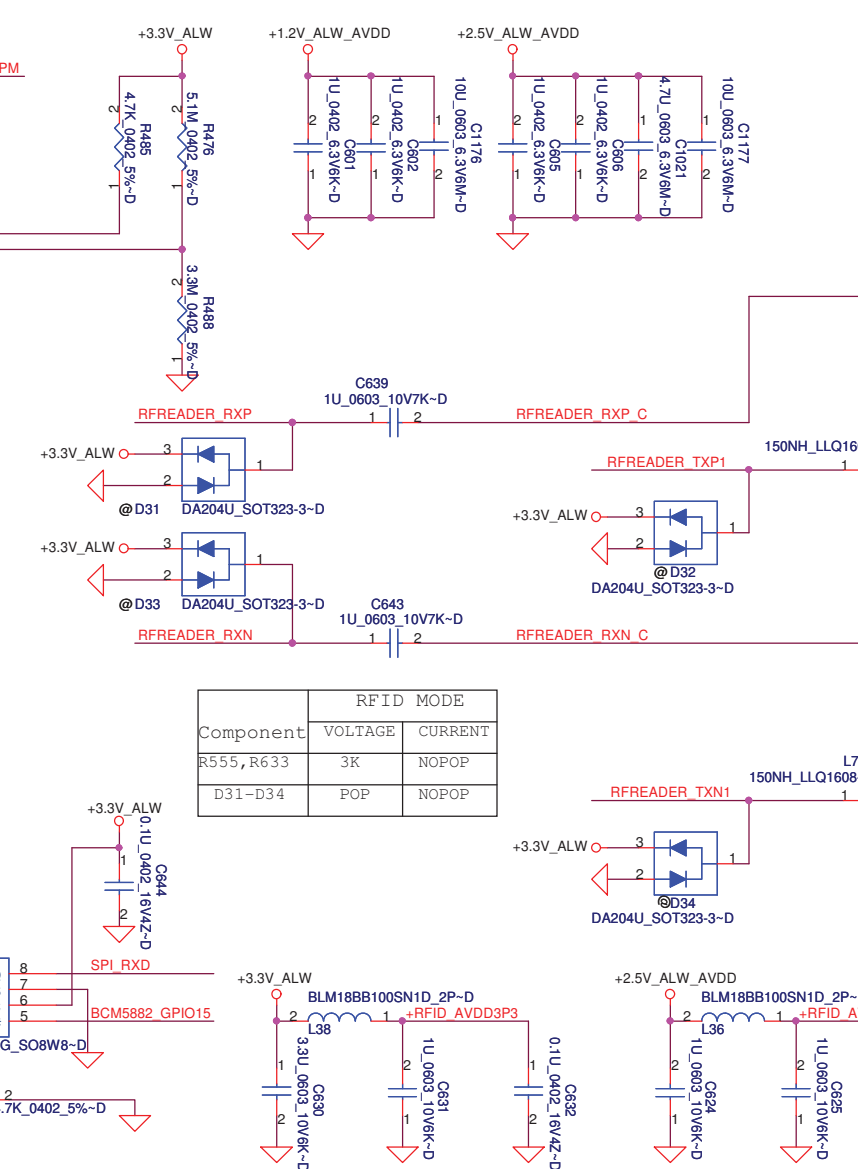
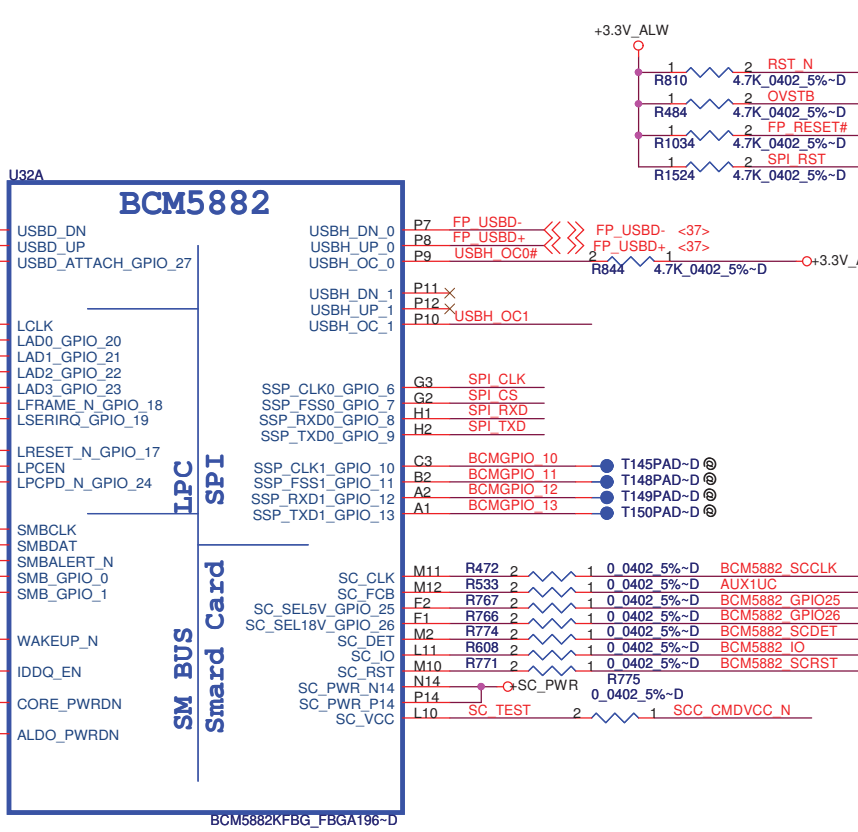
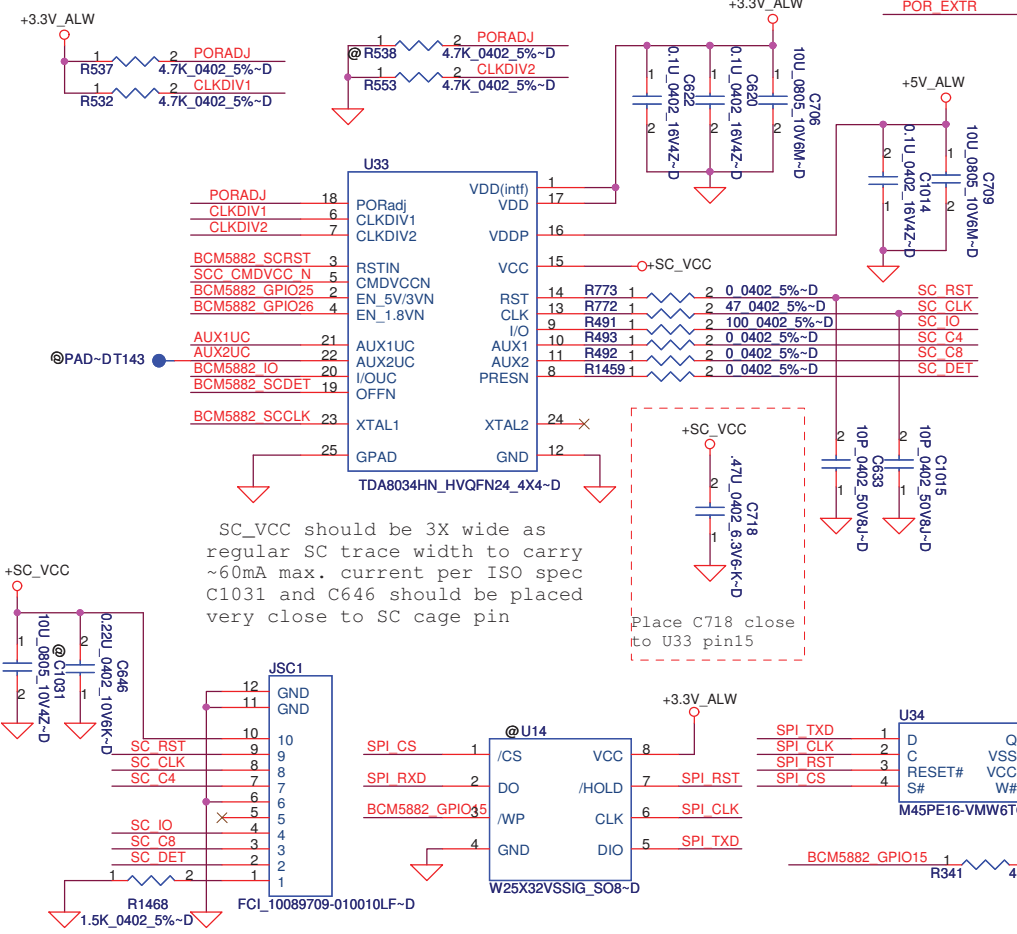
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Size: Document Number LA-5471P

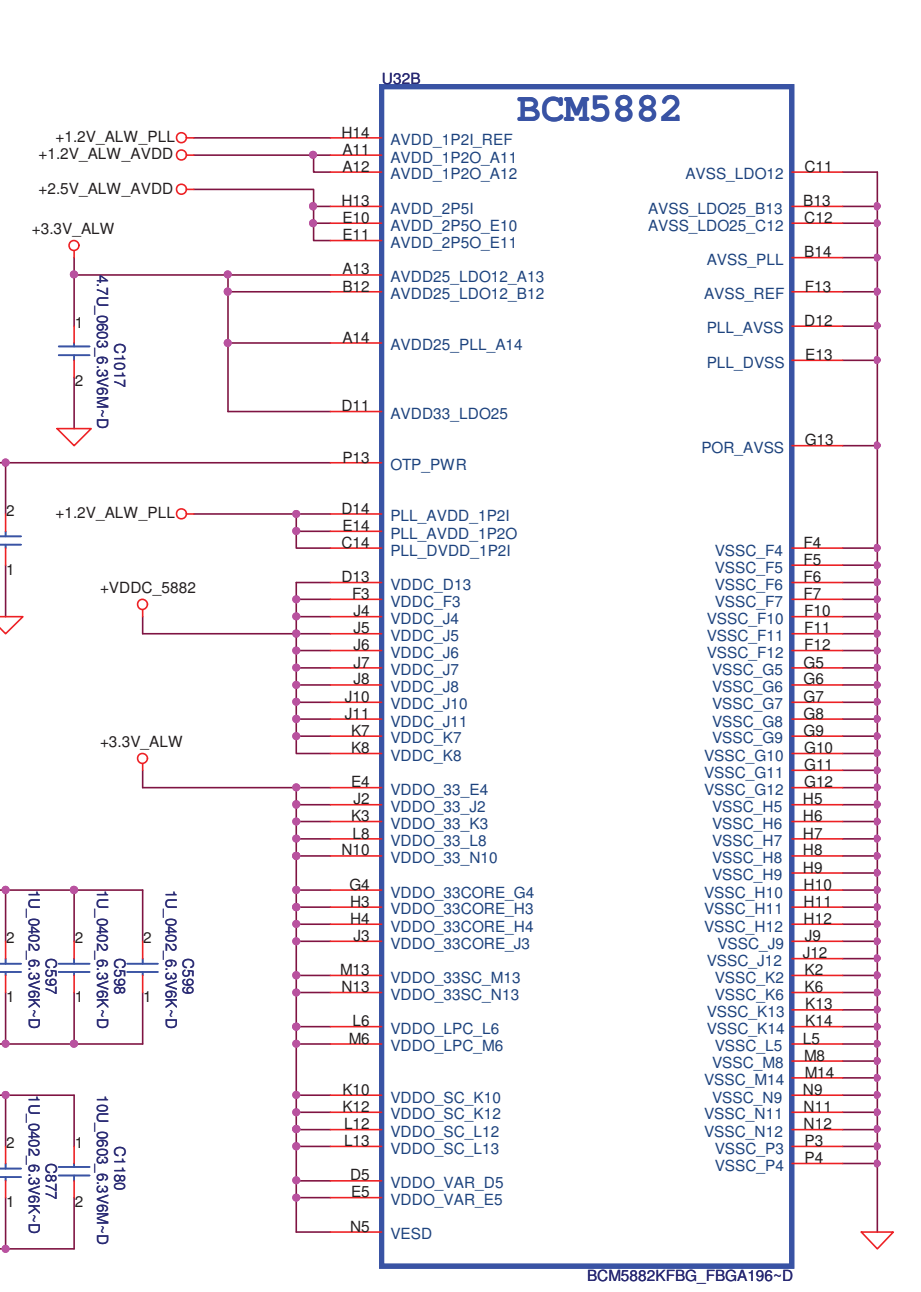
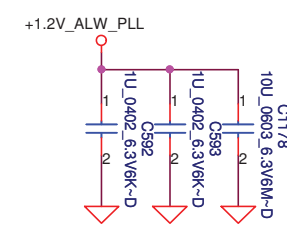
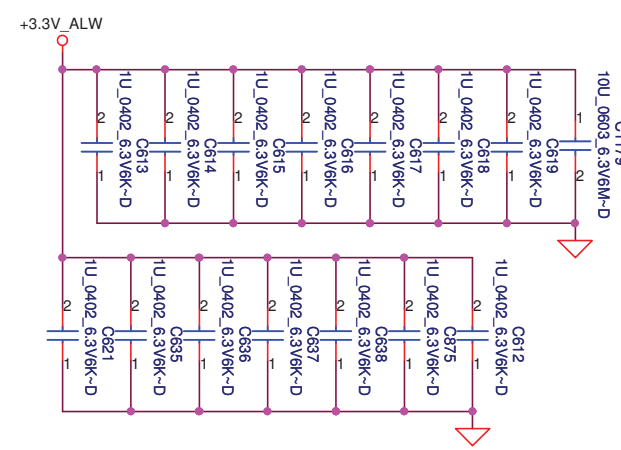
Date: Wednesday, January 20, 2010 Sheet 30 of 57



Smart Card



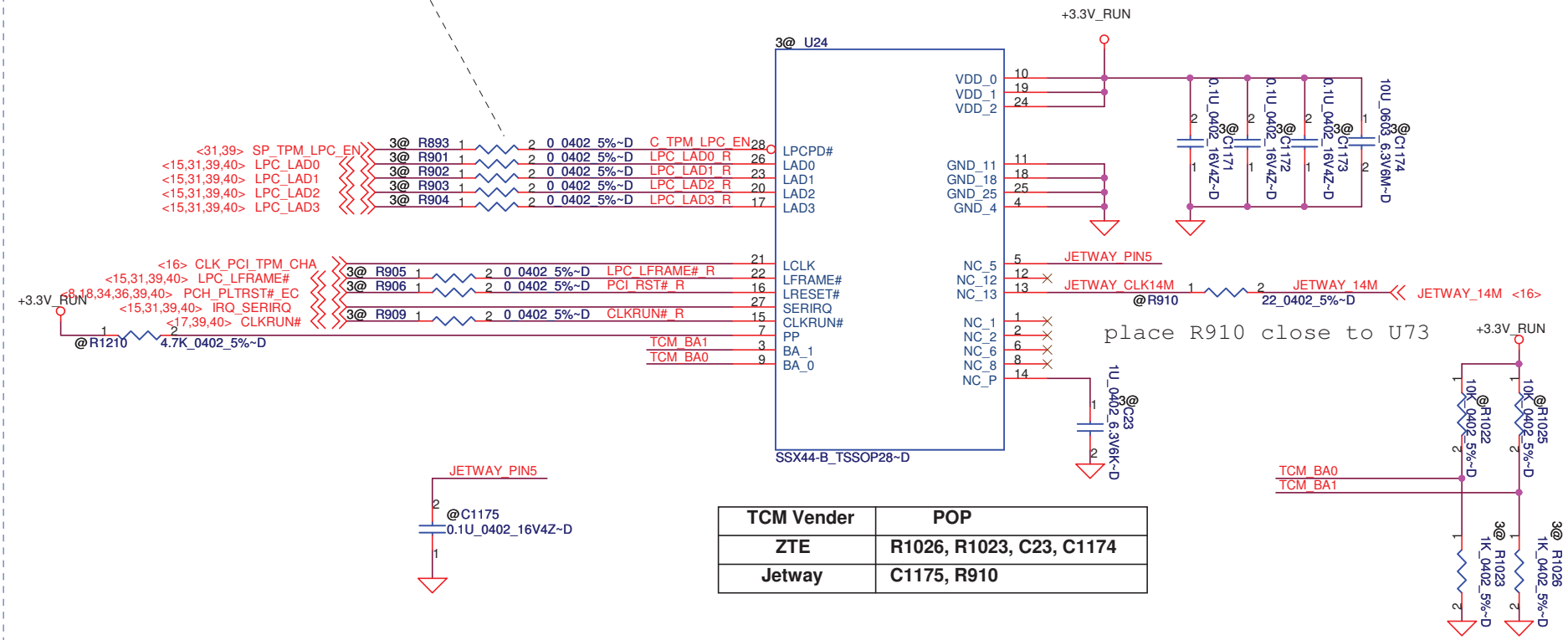
Hardware enable for USH TPM: Populate D70 & R841, No Stuff R483.
 Hardware disable for USH TPM: No Stuff D70 & R841, Populate R483



USH BCM5882 and China TPM Z8H172T Option				
PART/PIN	Ref Des	TCM Enable	TPM Enable	ALL TPM/TCM Disable
TCM circuit	All 3@	POP	@	@
SIO 5028 ->SP_TPM_LPC_EN	PU R841	@	POP	@
	PD R483	POP	@	@
	PU R788	@	@	@
PCH GPIO39 ->TPM_ID1	PU R787	@	@	POP
	PD R339	POP	POP	@
PCH GPIO38 ->TPM_ID0	PU R273	POP	POP	@
	PD R922	@	@	POP

LOW:Power Down Mode
High:Working Mode

China TPM: ZTE & Jetway co-lay



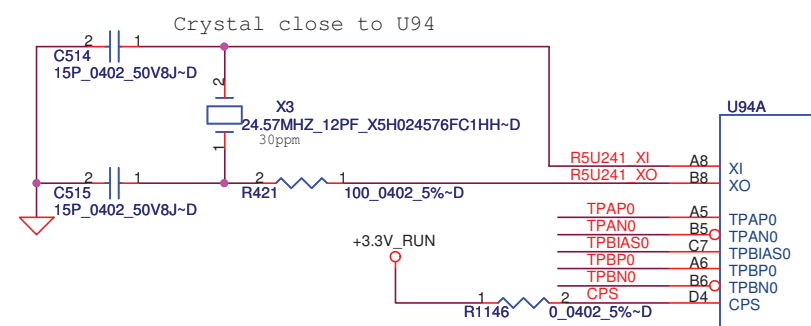
TCM Vender	POP
ZTE	R1026, R1023, C23, C1174
Jetway	C1175, R910

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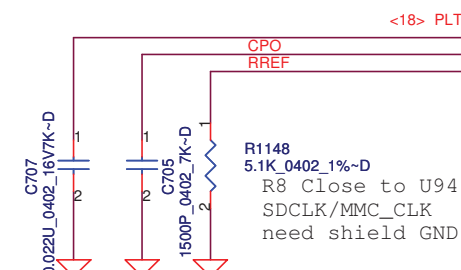
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Compal Electronics, Inc.		
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Size	Document Number	Rev
	LA-5471P	1.0
Date:	Wednesday, January 20, 2010	Sheet 32 of 57

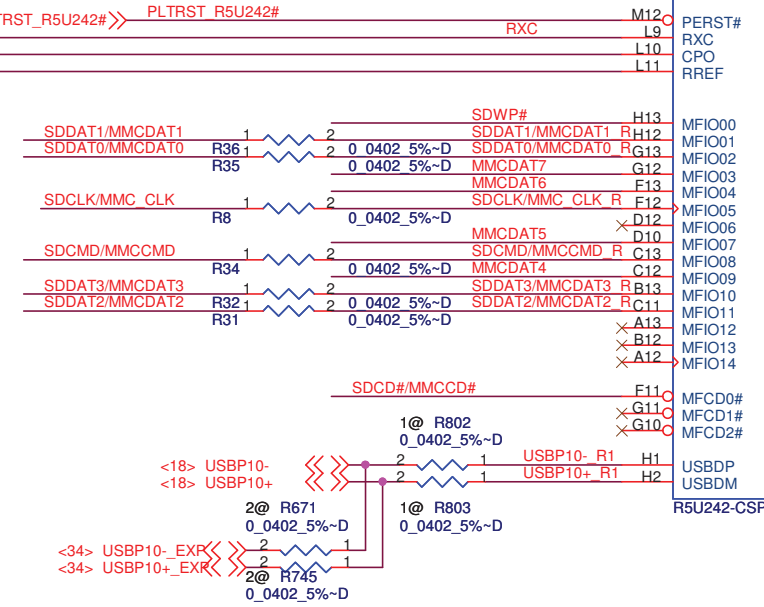


C710, C713 as close as possible to U94

<16> CLK_PCIE_PCM
<16> CLK_PCIE_PCM#
<16> PCIE_PRX_PCMTX_P3
<16> PCIE_PRX_PCMTX_N3
<16> PCIE_PTX_PCMTX_P3_C
<16> PCIE_PTX_PCMTX_N3_C

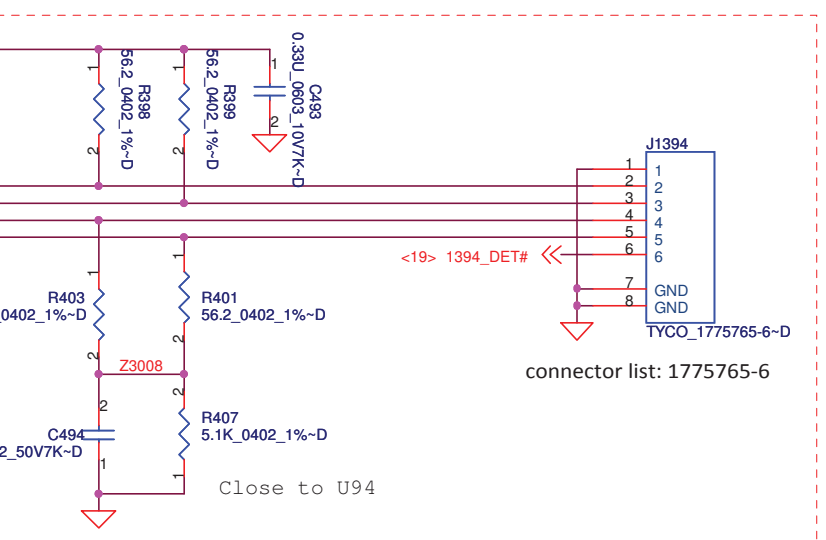
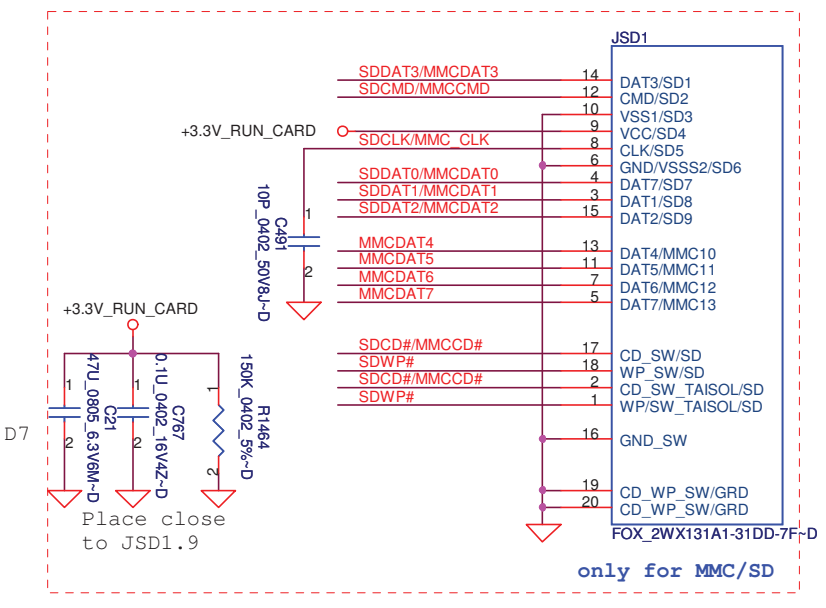
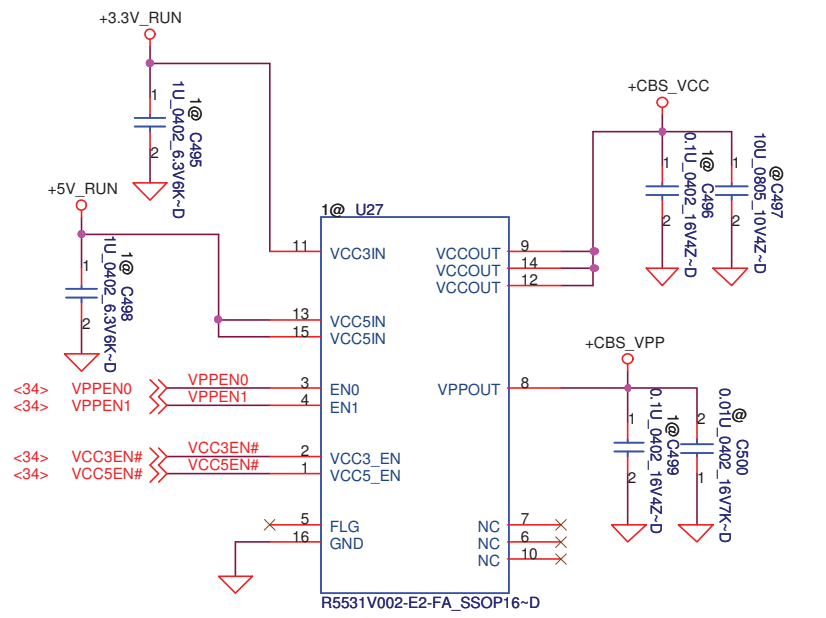
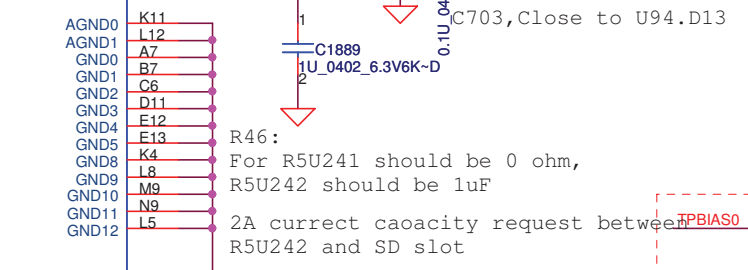
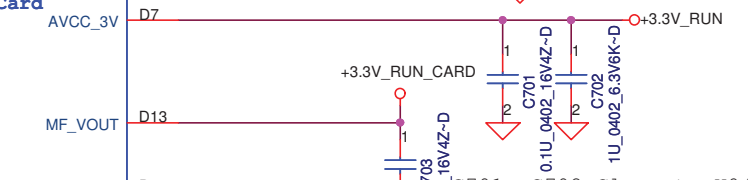
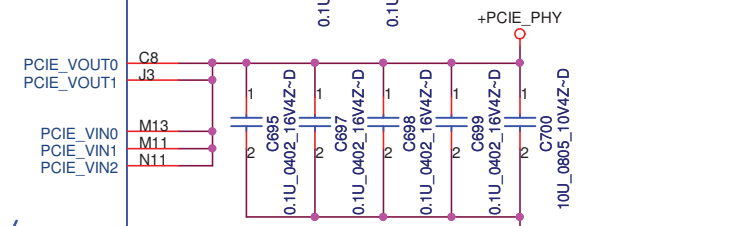
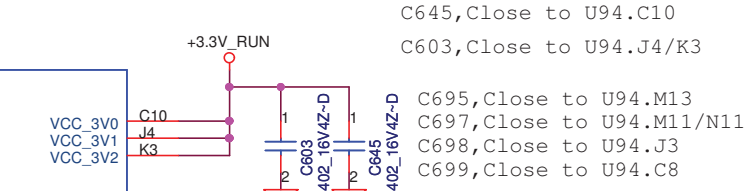


C707, C705, R1148 as close as possible to U94



MFIO Pin Assignment Table

MFIO	SD8	XD	MS8
00	WP	D7	BS
01	D1	D6	-
02	D0	D5	D1
03	D7	D4	-
04	D6	D3	D5
05	CLK	D2	D0
06	-	D1	-
07	D5	D0	D4
08	CMD	WP#	D2
09	D4	WE#	D6
10	D3	ALE	D3
11	D2	CLE	-
12	-	CE#	-
13	-	RE#	D7
14	-	R/B#	CLK



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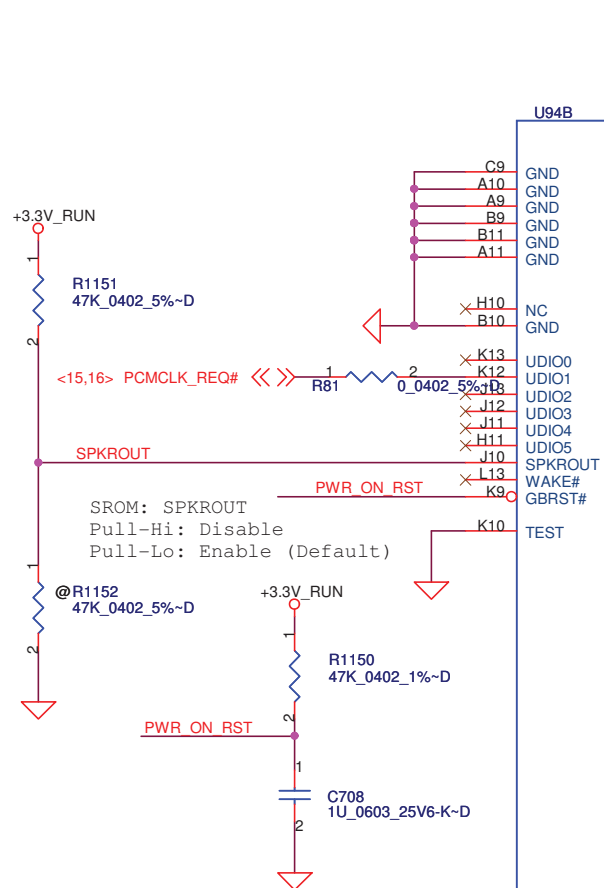
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Title R5U241 (1/2)

Size Document Number LA-5471P

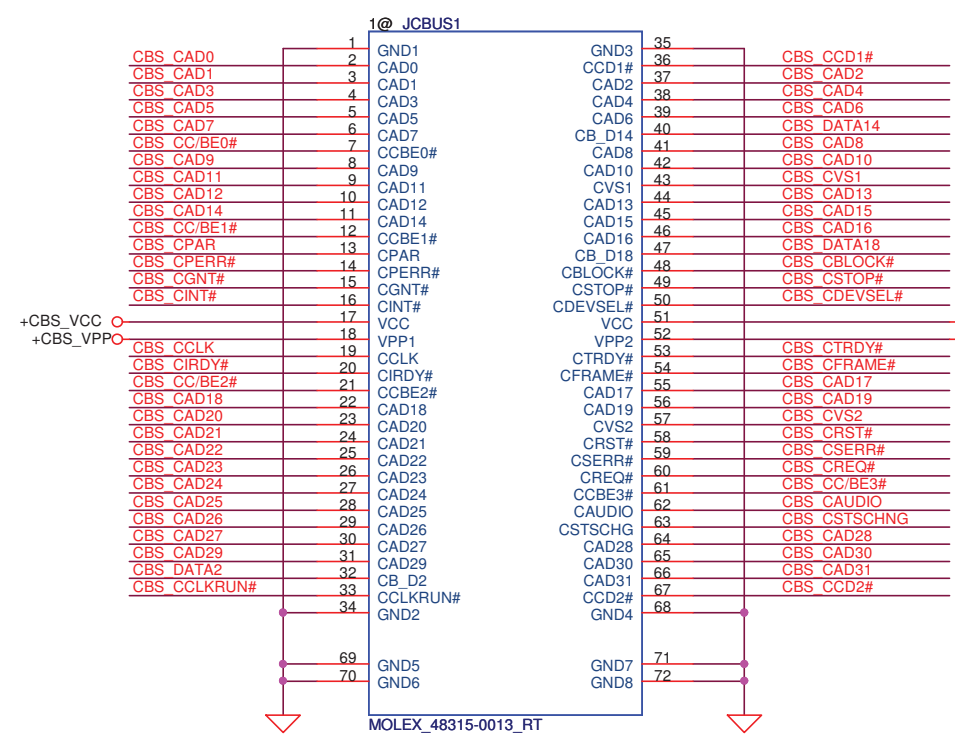
Date: Wednesday, January 20, 2010 Sheet 33 of 57



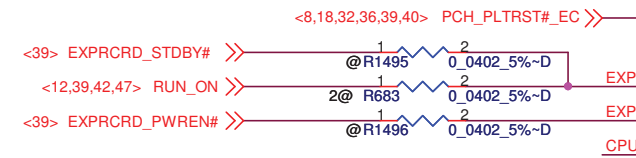
Power-On-Reset: GBRST#
(Global Reset)
Note: De-asserted BEFORE PERST# de-assertion

CADR25	L2	CBS	CAD19
CADR24	K2	CBS	CAD17
CADR23	H4	CBS	CFRAME#
CADR22	J1	CBS	CTRDY#
CADR21	G3	CBS	CDEVSEL#
CADR20	F3	CBS	CSTOP#
CADR19	G2	CBS	CBLOCK#
CADR18	F2	CBS	DATA18
CADR17	H3	CBS	CCLK_R
CADR16	J2	CBS	CIRDY#
CADR15	G1	CBS	CPERR#
CADR14	F1	CBS	CPAR
CADR13	K1	CBS	CC/BE2#
CADR12	C2	CBS	CAD12
CADR11	C3	CBS	CAD9
CADR10	D2	CBS	CAD14
CADR9	E3	CBS	CC/BE1#
CADR8	L1	CBS	CAD18
CADR7	M1	CBS	CAD20
CADR6	M2	CBS	CAD21
CADR5	L3	CBS	CAD22
CADR4	M3	CBS	CAD23
CADR3	N3	CBS	CAD24
CADR2	N4	CBS	CAD25
CADR1	M4	CBS	CAD26
CADR0			
CDATA15	B1	CBS	CAD8
CDATA14	B2	CBS	DATA14
CDATA13	B3	CBS	CAD6
CDATA12	B4	CBS	CAD2
CDATA11	M7	CBS	CAD31
CDATA10	M6	CBS	CAD30
CDATA9	M5	CBS	CAD28
CDATA8	A1	CBS	CAD7
CDATA7	A2	CBS	CAD5
CDATA6	A3	CBS	CAD3
CDATA5	A4	CBS	CAD1
CDATA4	C5	CBS	CAD0
CDATA3	N7	CBS	DATA2
CDATA2	N6	CBS	CAD29
CDATA1	N5	CBS	CAD27
CDATA0			
OE#	C1	CBS	CAD11
WE#	F4	CBS	CGNT#
CE2#	D3	CBS	CAD10
CE1#	D5	CBS	CC/BE0#
REG#	L4	CBS	CC/BE3#
RESET	N1	CBS	CRST#
WAIT#	N2	CBS	CSERR#
WP#/IOIS16#	L7	CBS	CCLKRUN#
RDY/IREQ#	G4	CBS	CINT#
BVD2	K7	CBS	CSTSCHNG
BVD1	K5	CBS	CVS2
VS2#	E4	CBS	CVS1
VS1#	K8	CBS	CCD2#
CD2#	D6	CBS	CCD1#
CD1#	K6	CBS	CREQ#
INPACK#	D1	CBS	CAD13
IORD#	E1	CBS	CAD15
IOWR#			

<33>	VPPEN1	VPPEN1	D9	VPPEN1
<33>	VPPEN0	VPPEN0	E10	VPPEN0
<33>	VCC3EN#	VCC3EN#	F10	VCC3EN#
<33>	VCC5EN#	VCC5EN#	E11	VCC5EN#

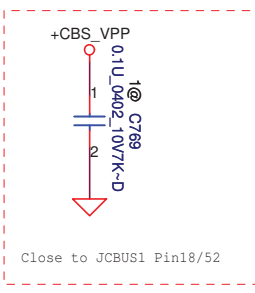
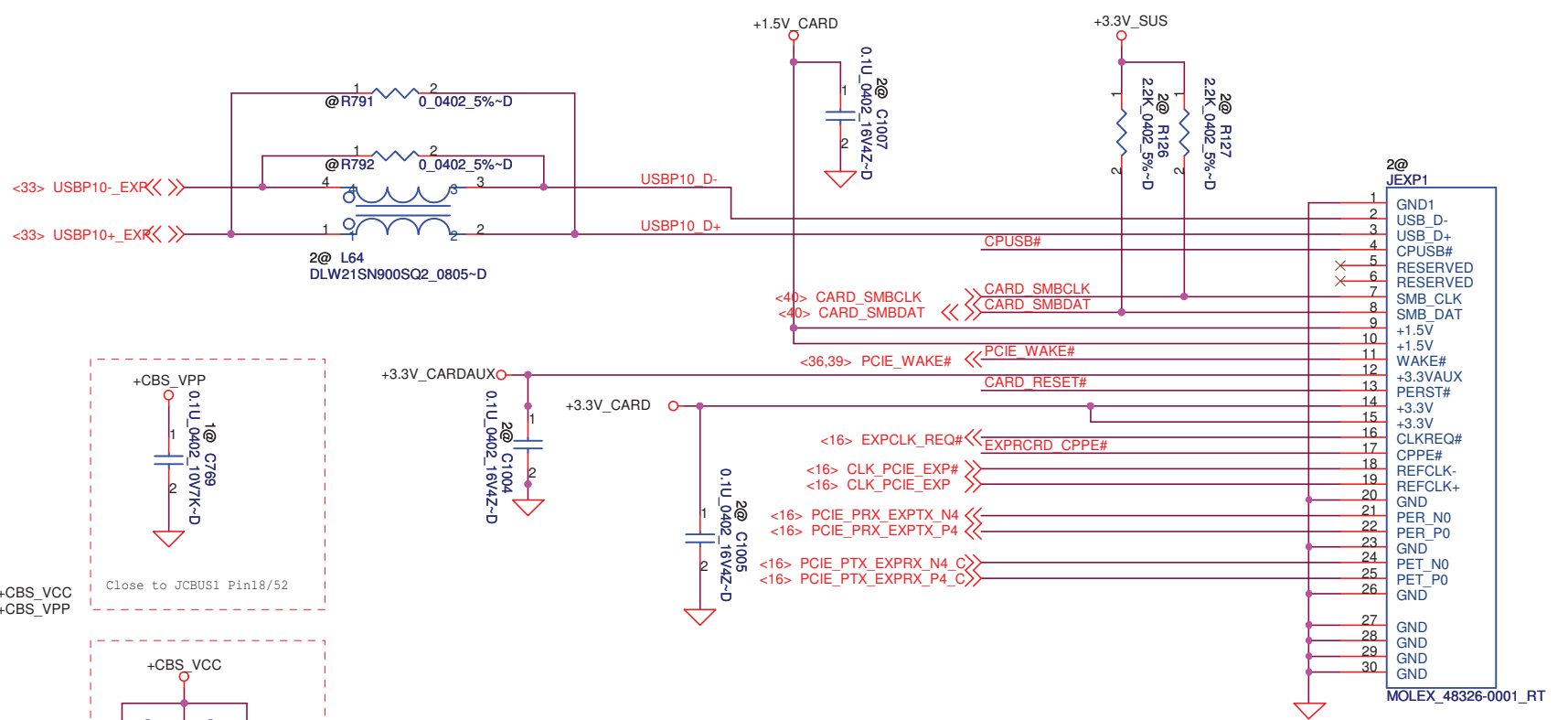


R410 Close to U94, CBS_CCLK need shield GND.



Express Card

+1.5V_CARD: Max. 650mA, Average 500mA
+3.3V_CARD: Max. 1300mA, Average 1000mA



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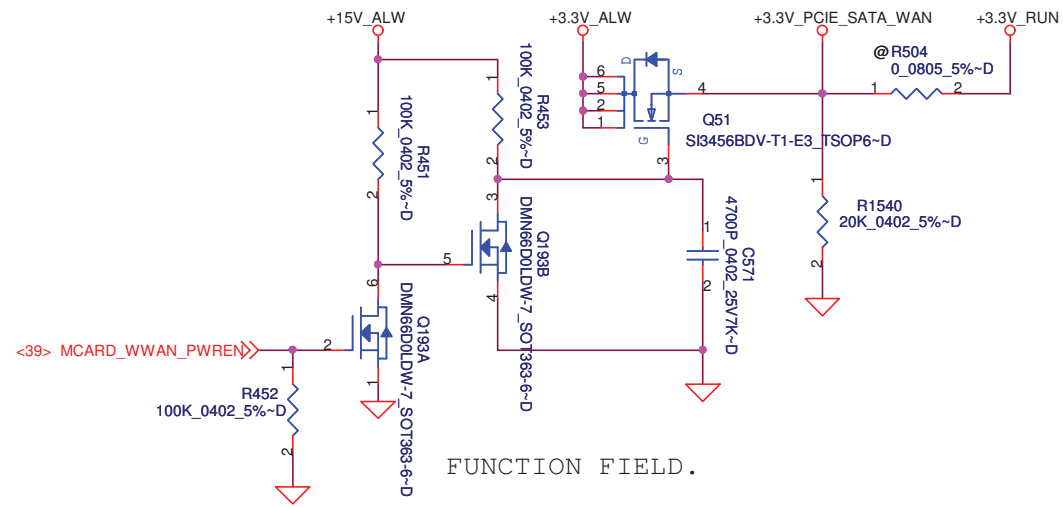
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Size: **LA-5471P**

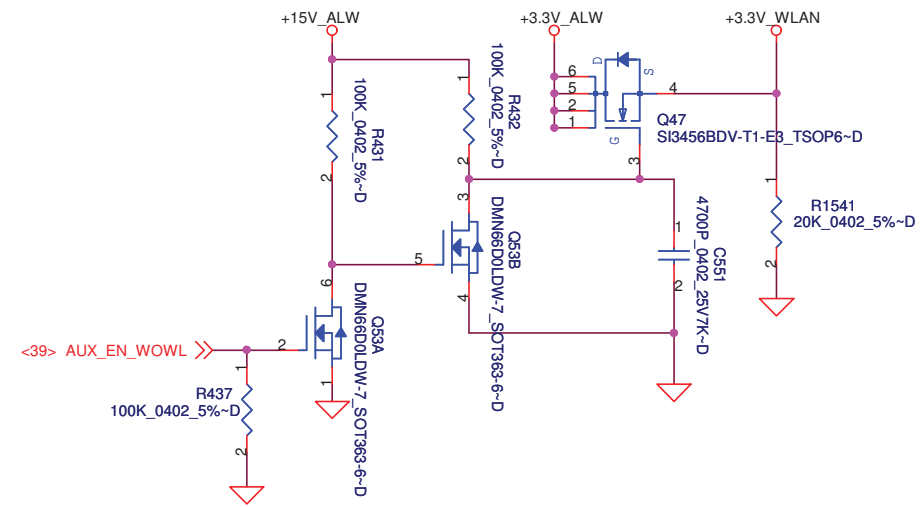
Date: **Wednesday, January 20, 2010** Sheet **34** of **57**

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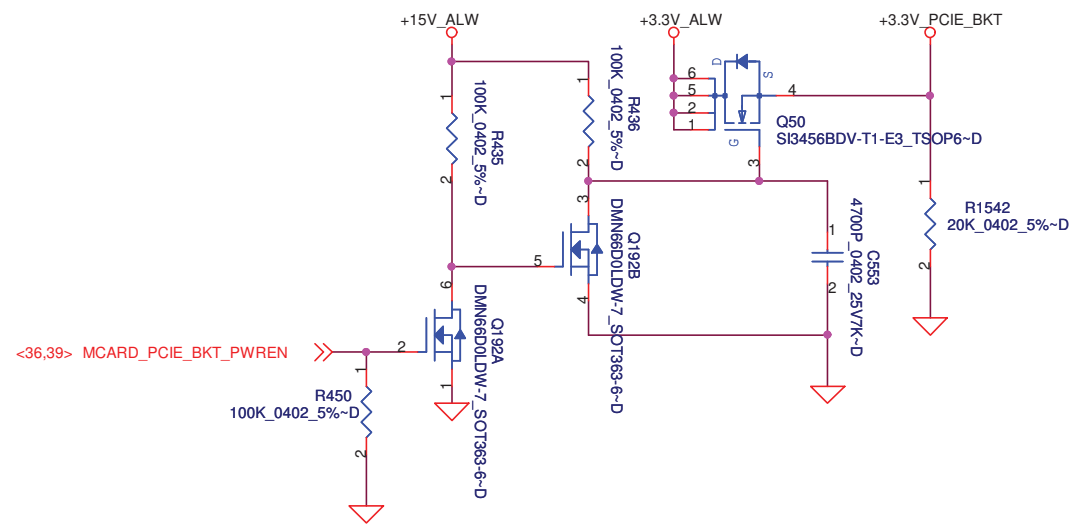
Mini WWAN



Mini WLAN



PCIE/BKT Card



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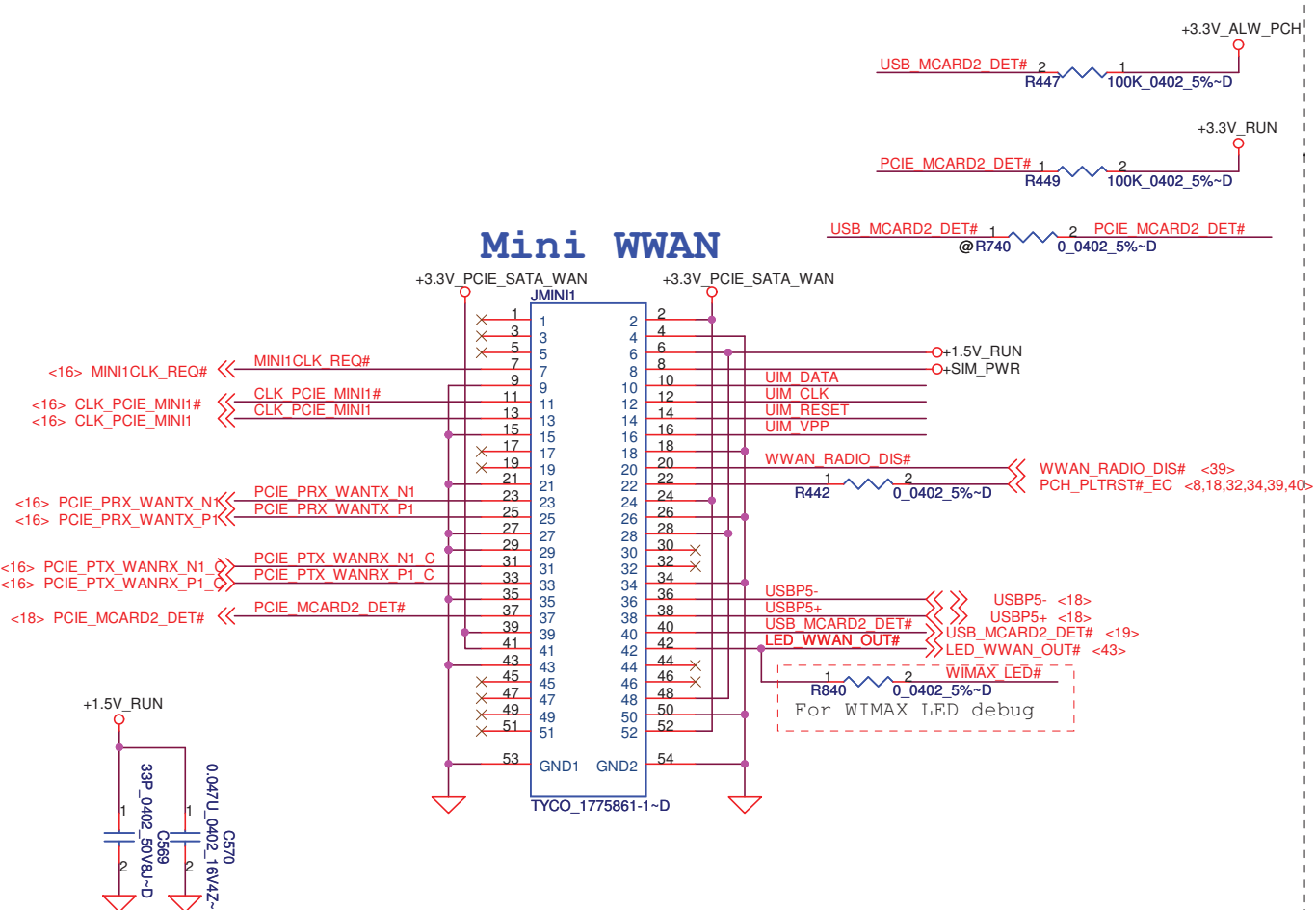
Compal Electronics, Inc.

Title		
PCIE PWR		
Size	Document Number	Rev
	LA-5471P	1.0
Date:	Wednesday, January 20, 2010	Sheet 35 of 57

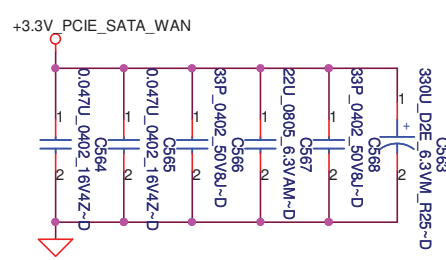
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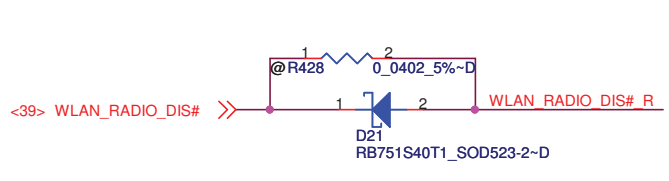
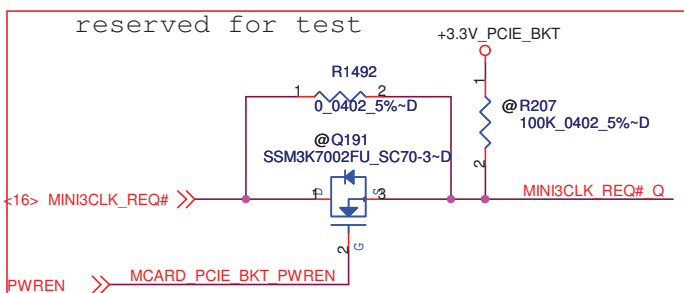
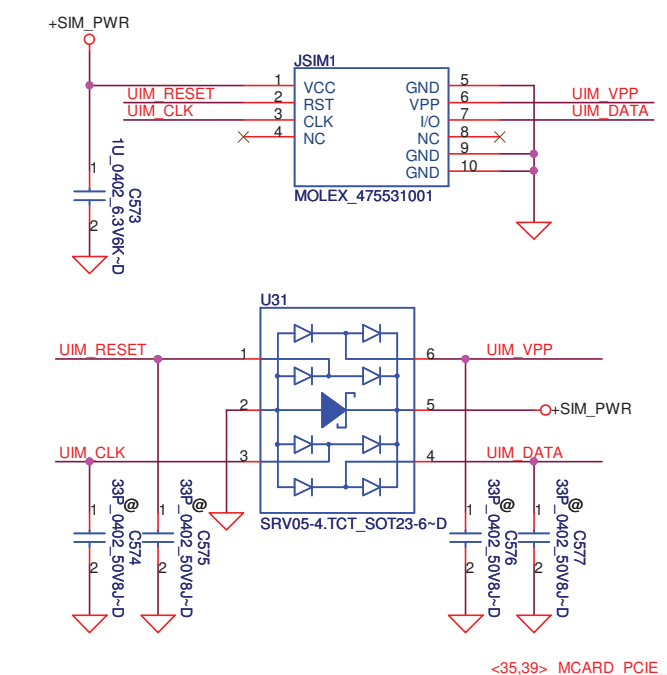
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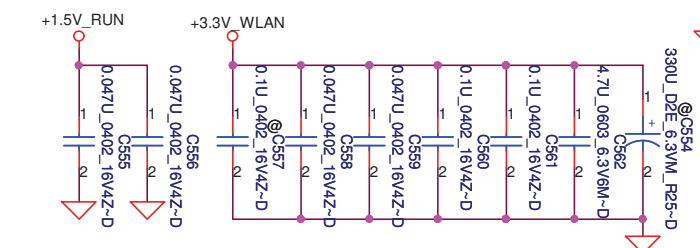
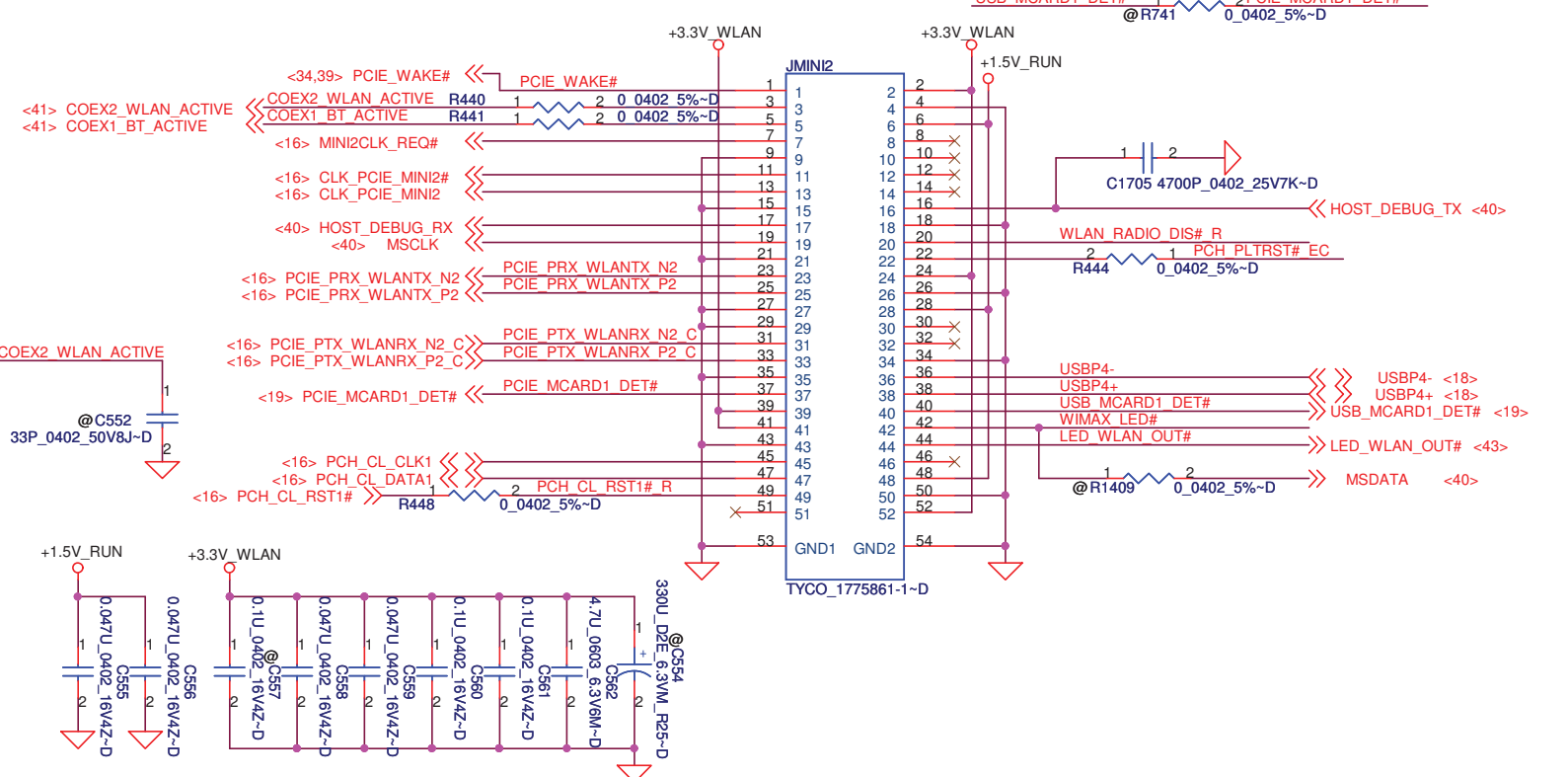
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		Peak	Normal	Normal
+3.3V	+/-9%	1000	750	
+3.3V_PCIE_SATA_WAN	+/-9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+/-5%	500	375	NA



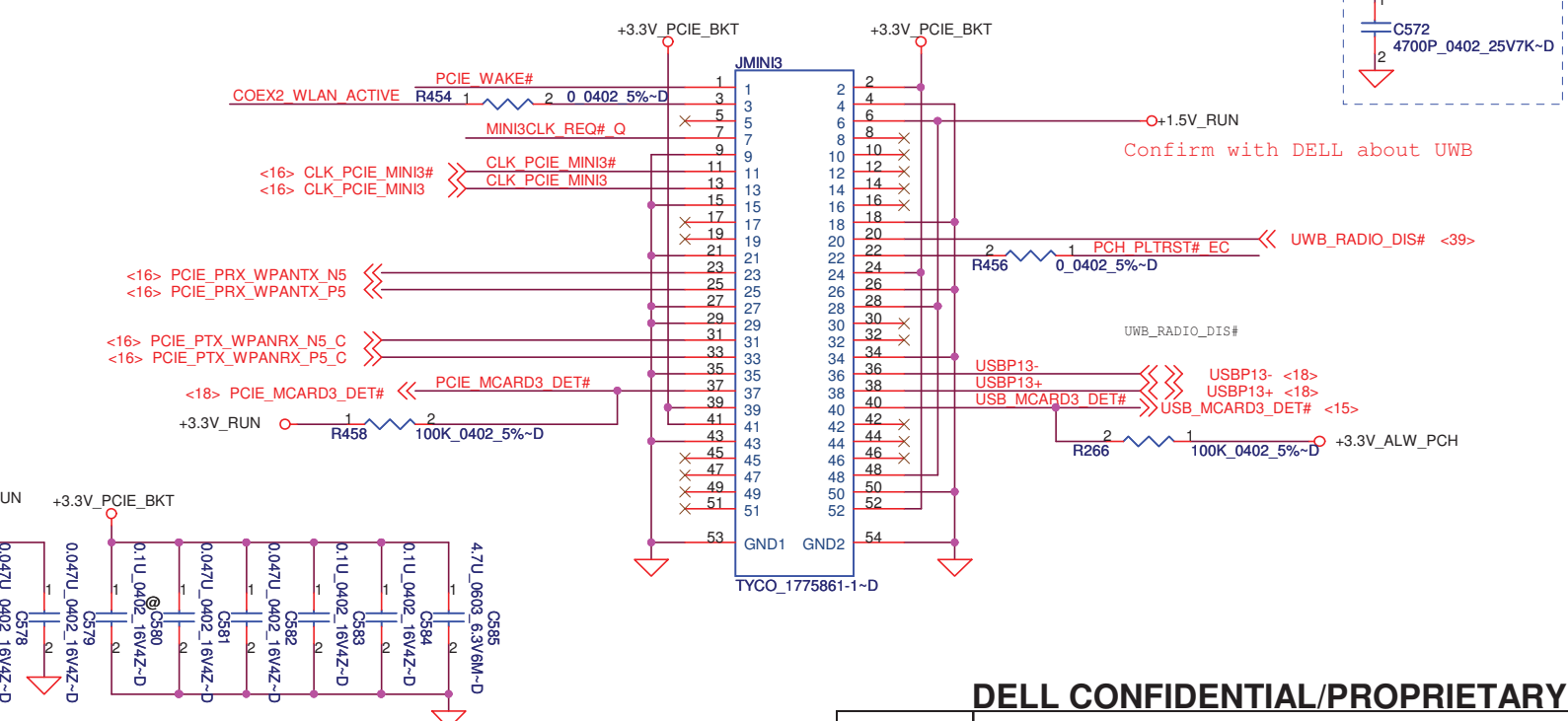
SIM Card



Mini WLAN



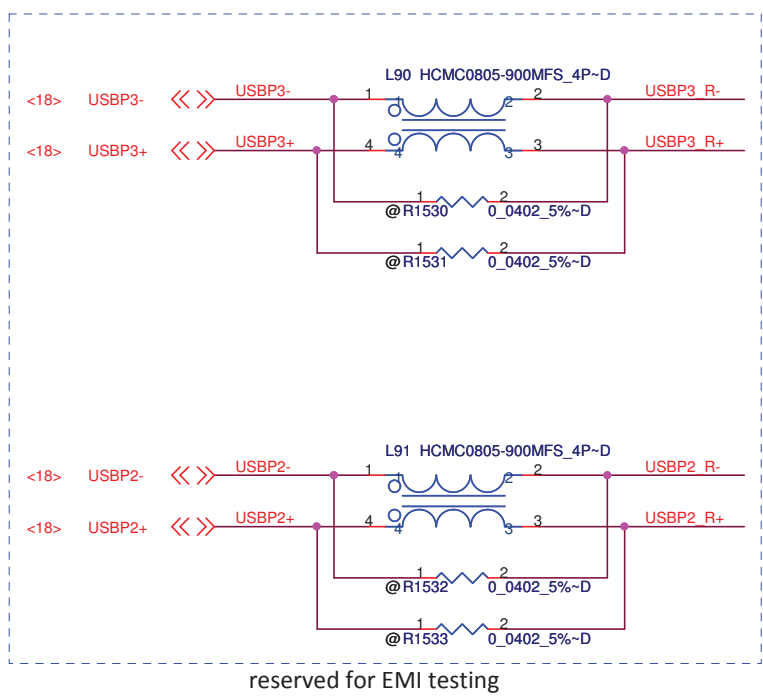
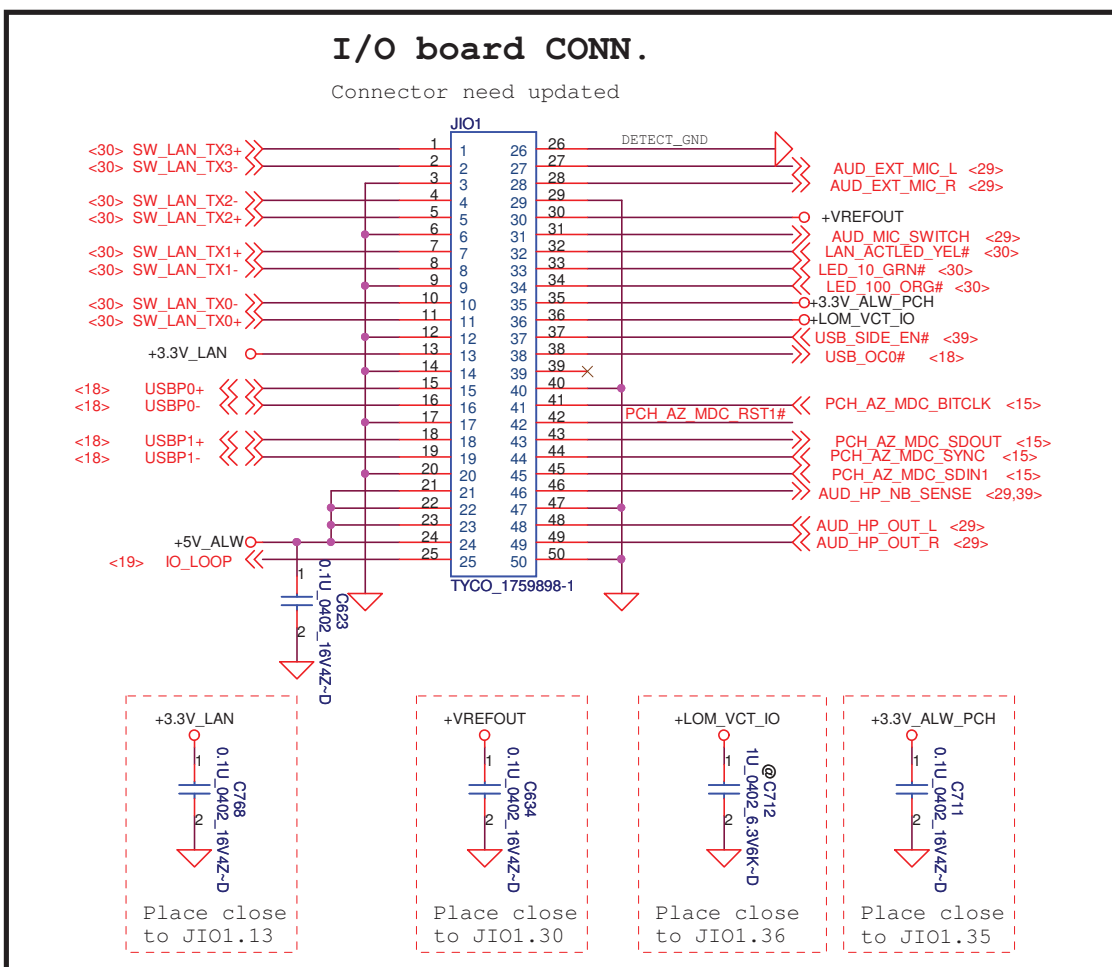
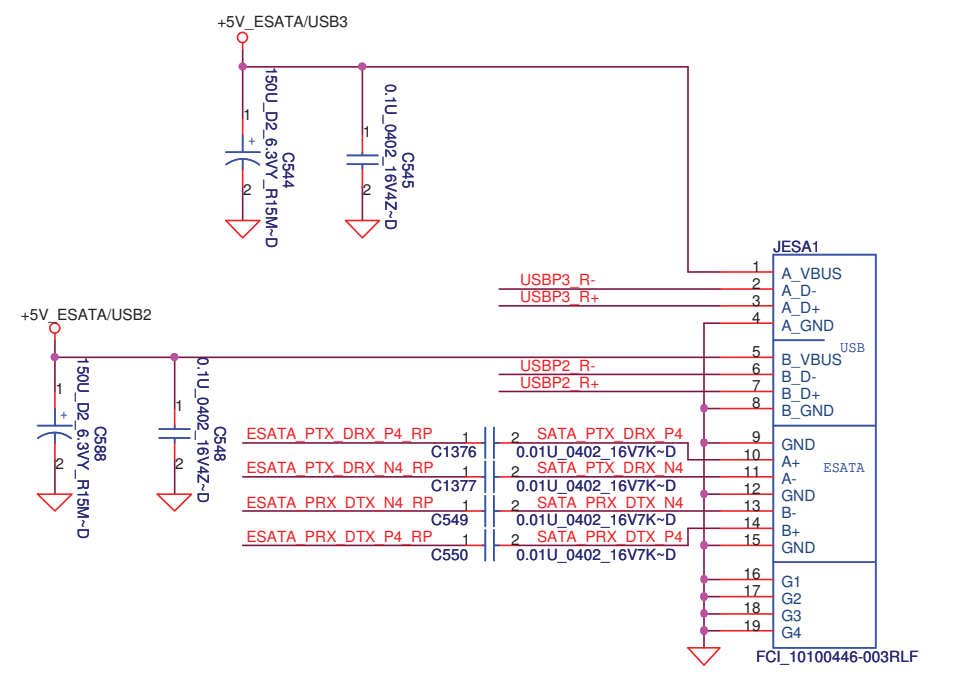
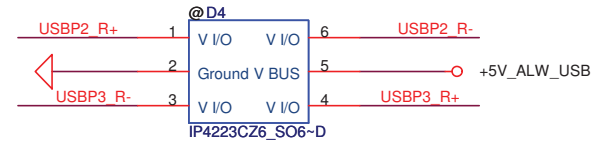
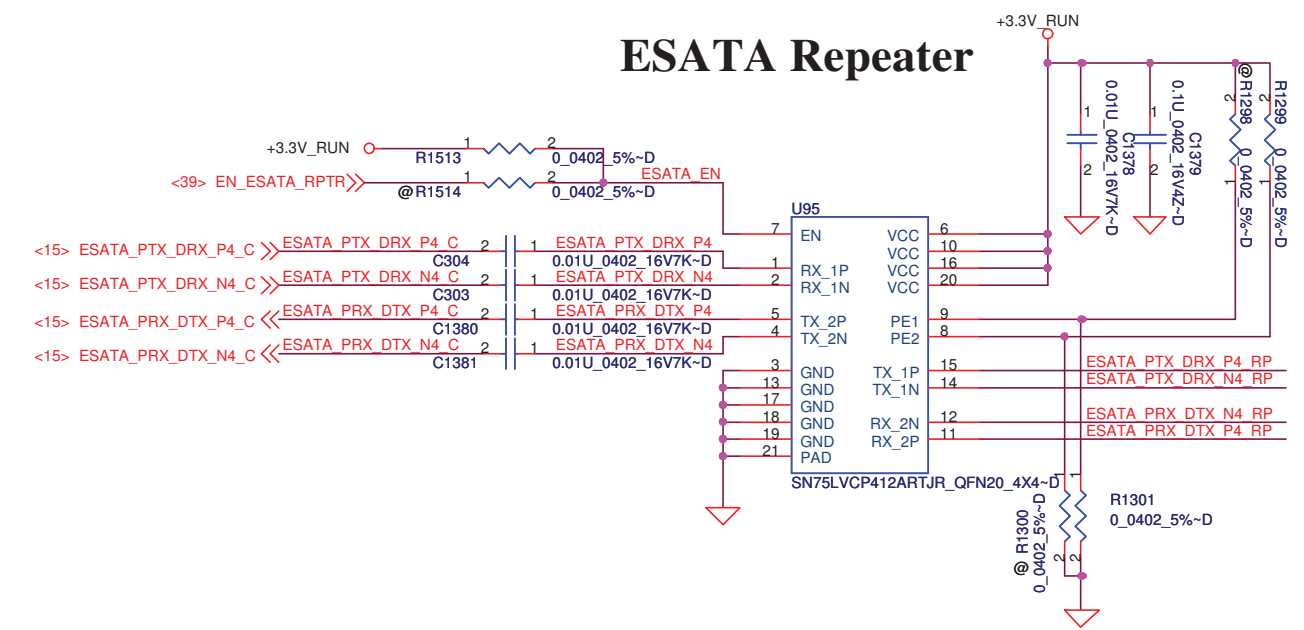
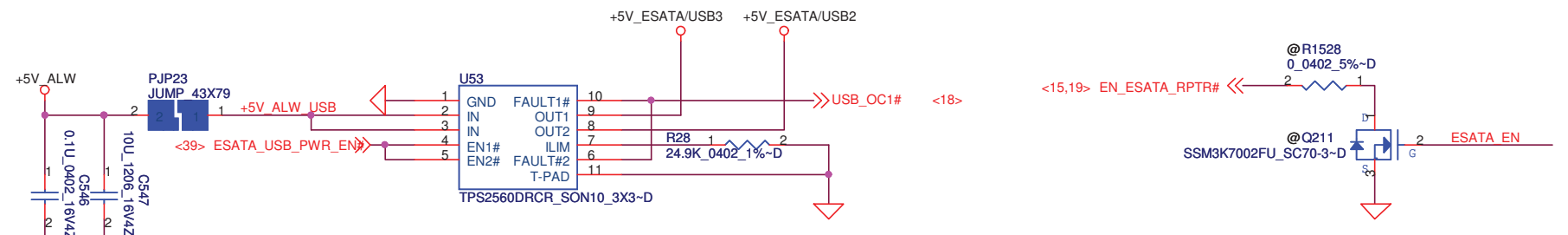
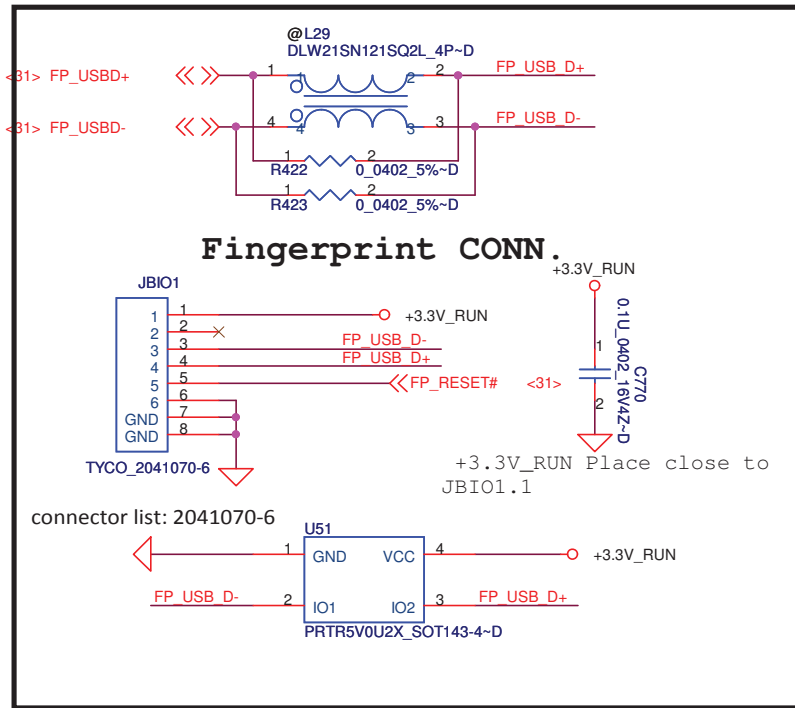
PCIE/BKT Card



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Mini Card		
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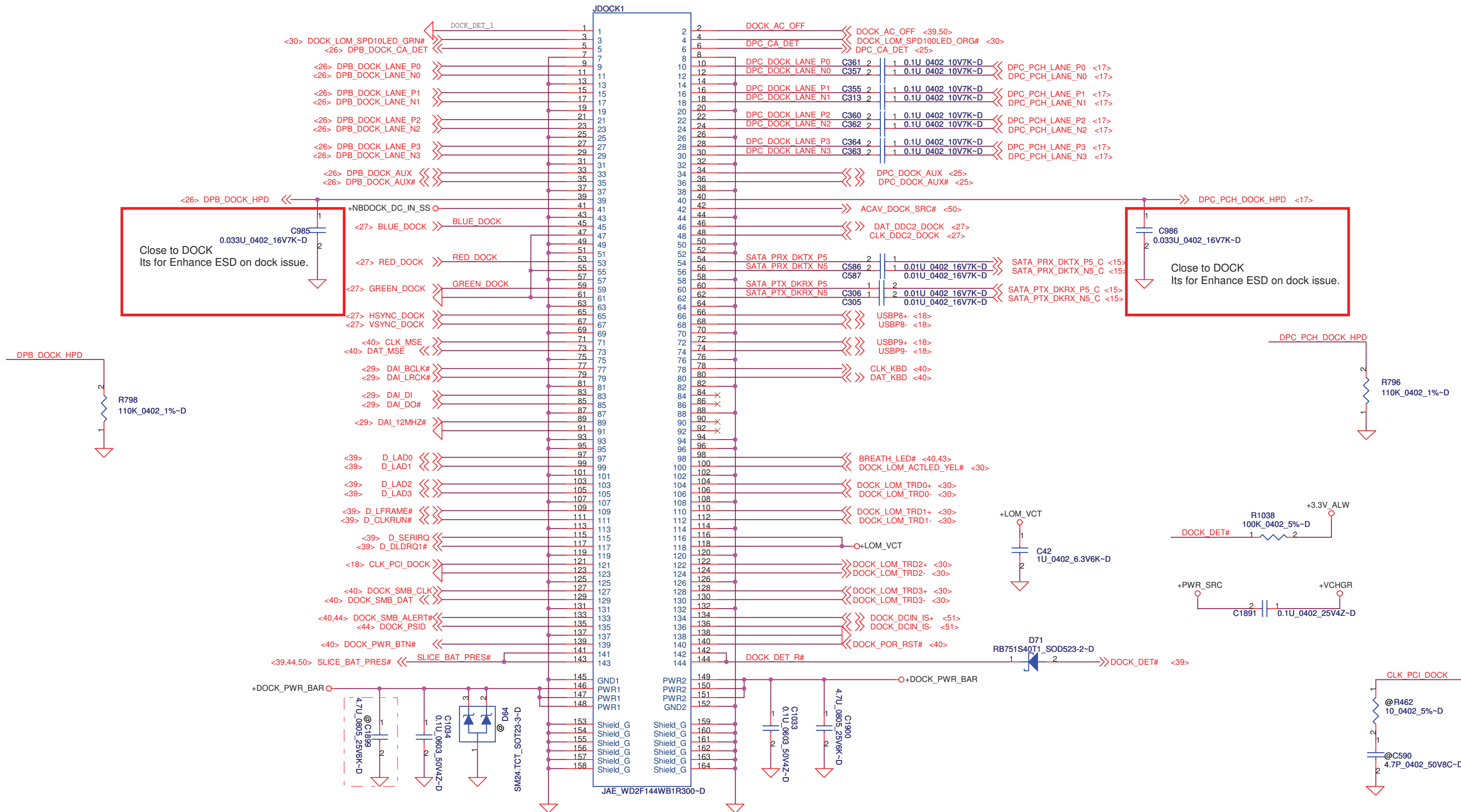
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Compal Electronics, Inc.

USB 2.0 PORT

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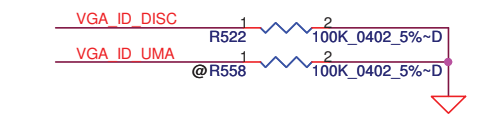
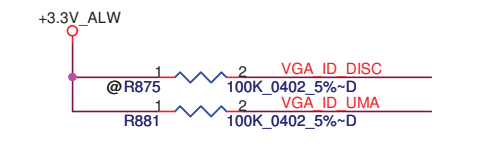
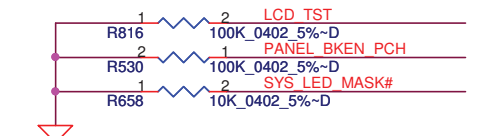
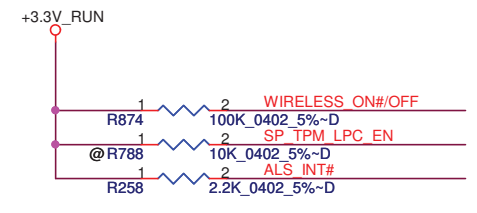
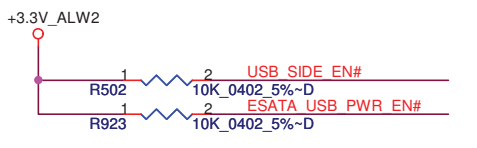
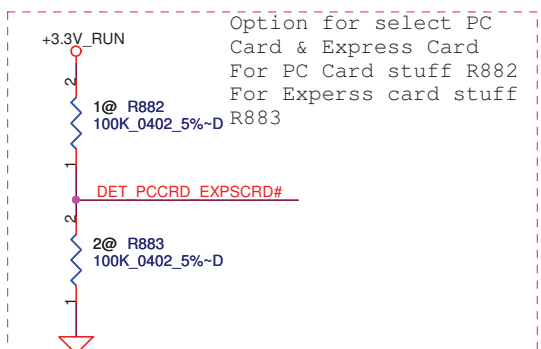
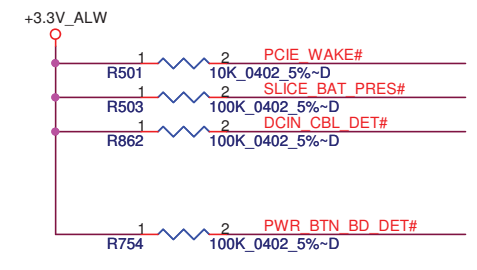
Close to DOCK
Its for Enhance ESD on dock issue.

Close to DOCK
Its for Enhance ESD on dock issue.

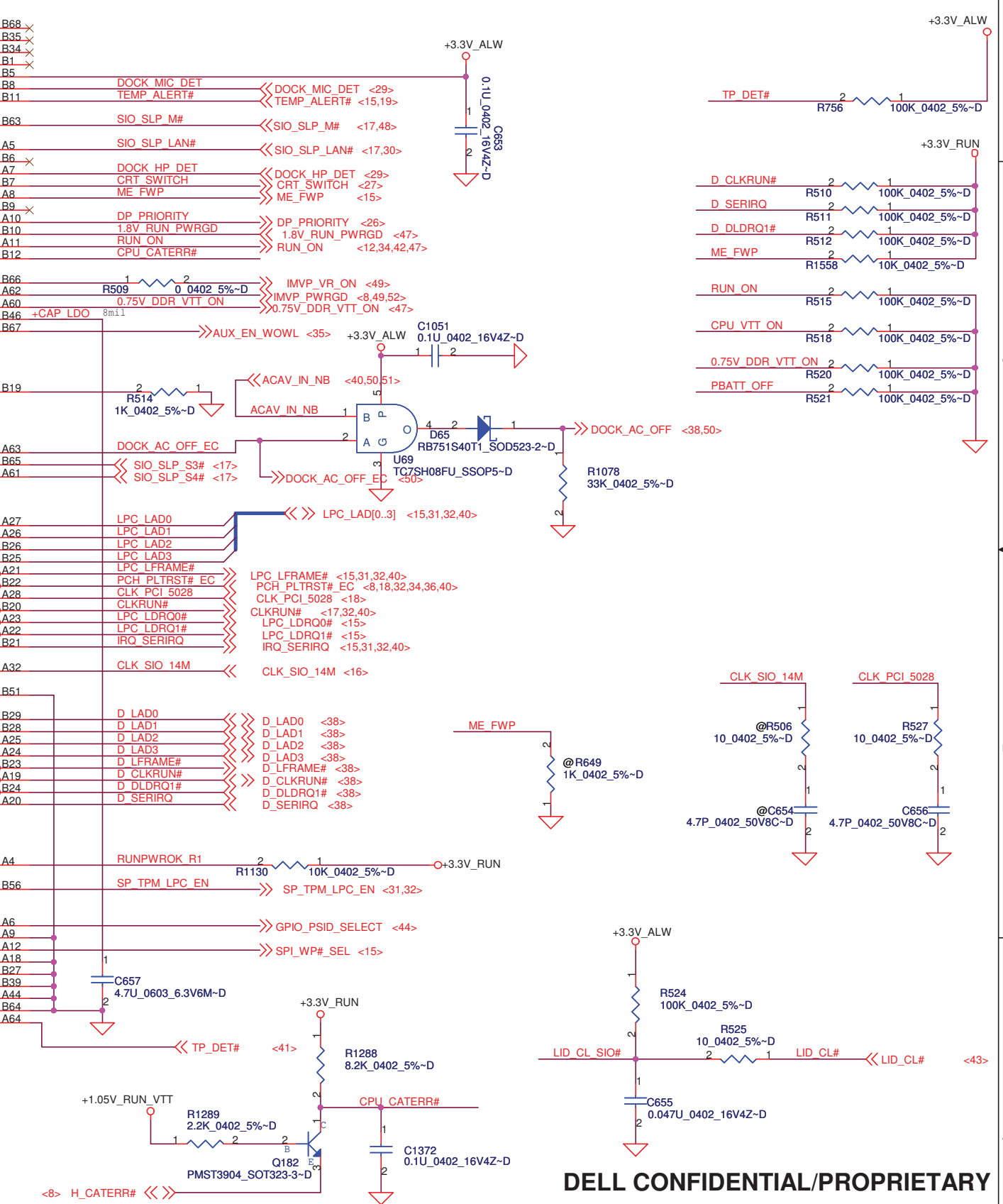
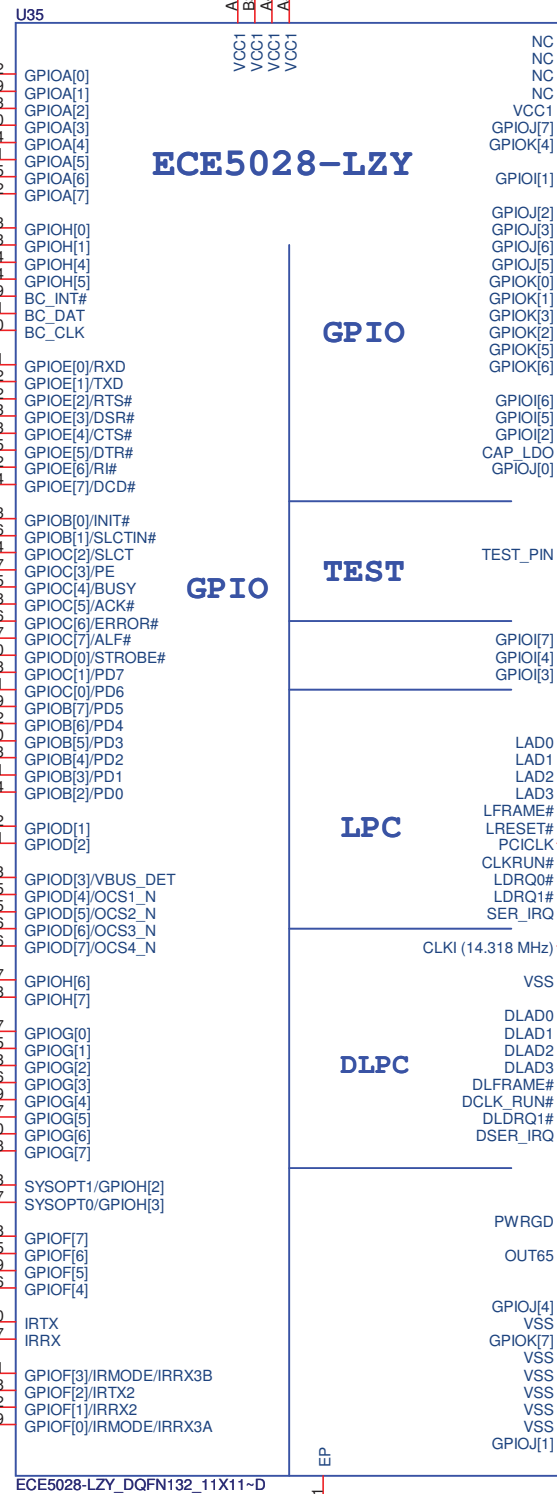
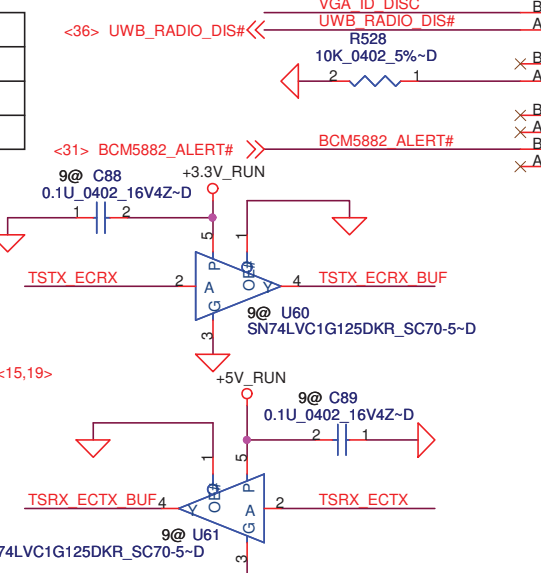
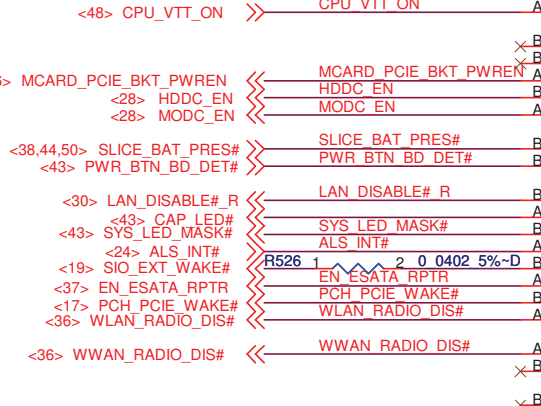
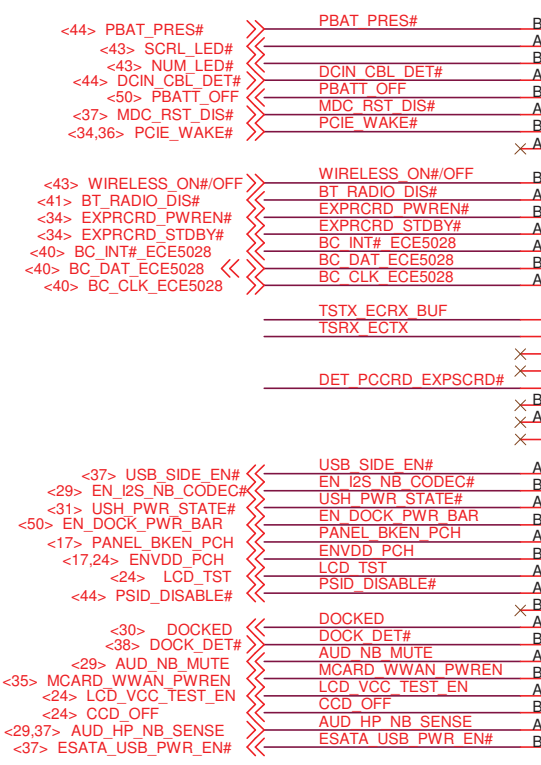
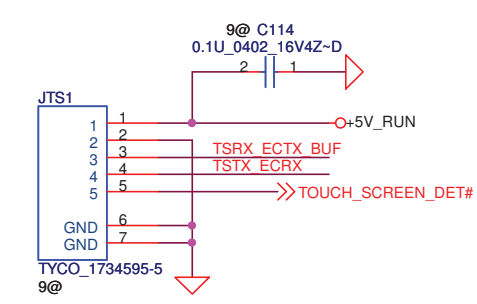
Reserve for EMI test

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DOCKING CONN		Rev 1.0	
LA-5471P	Document Number		
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	VGA_ID_UMA	VGA_ID_DISC
Discrete	0	1
UMA	1	0
SG	1	1



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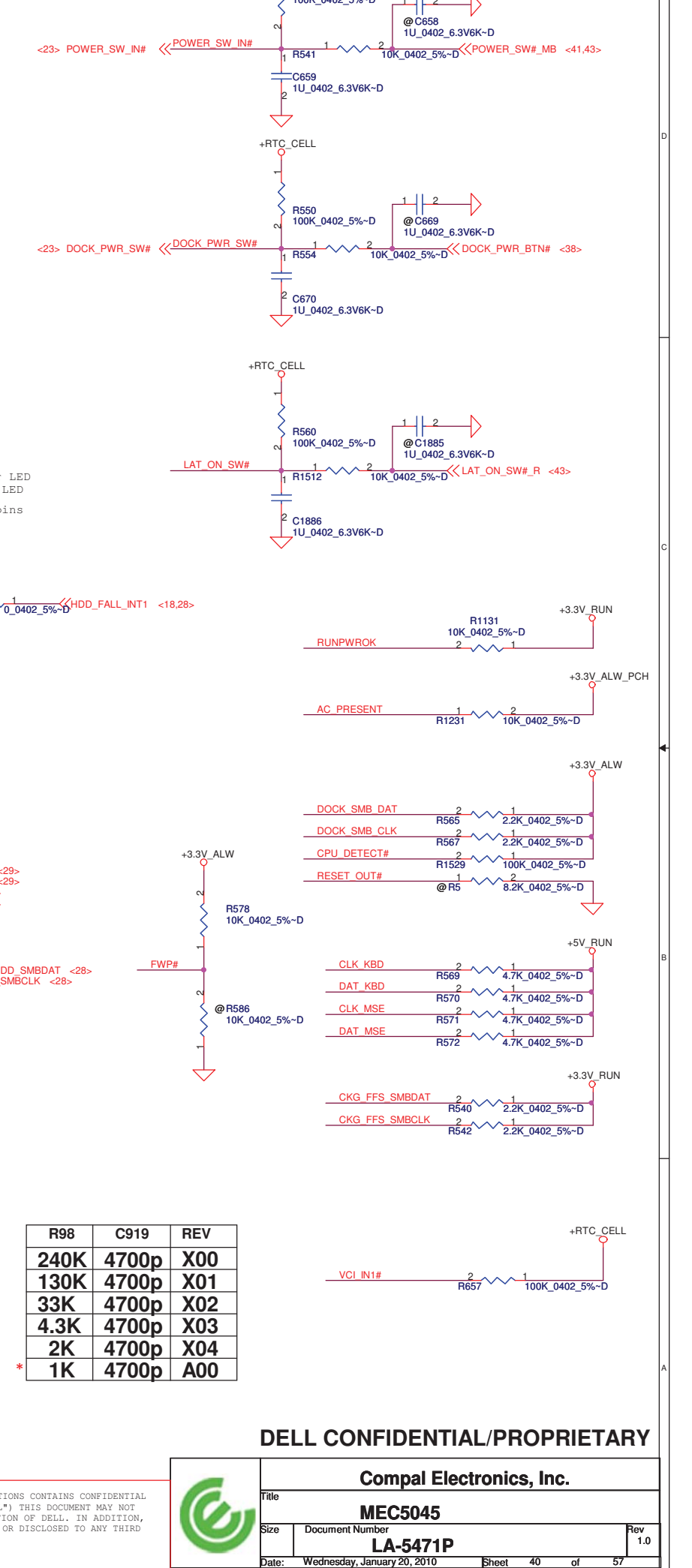
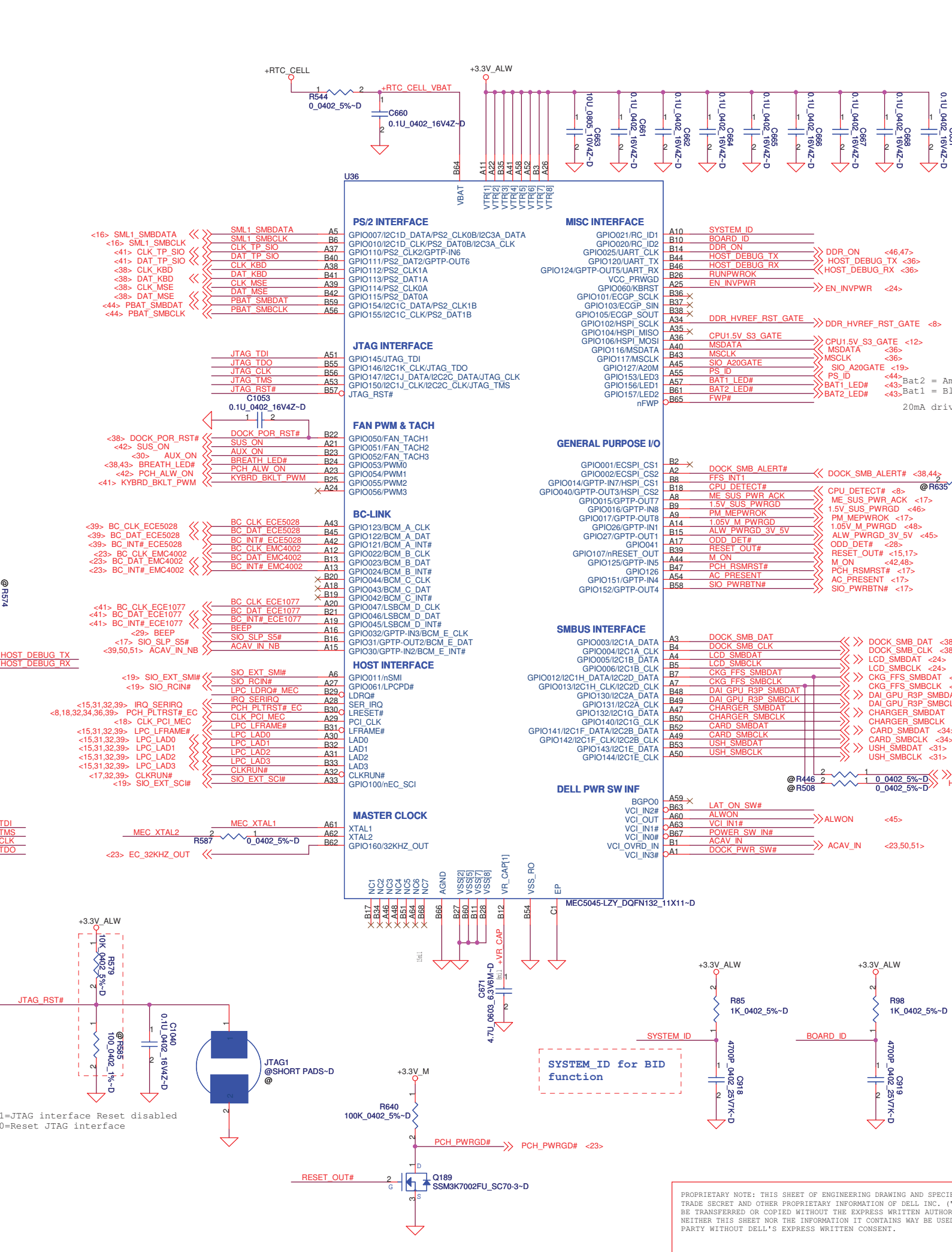
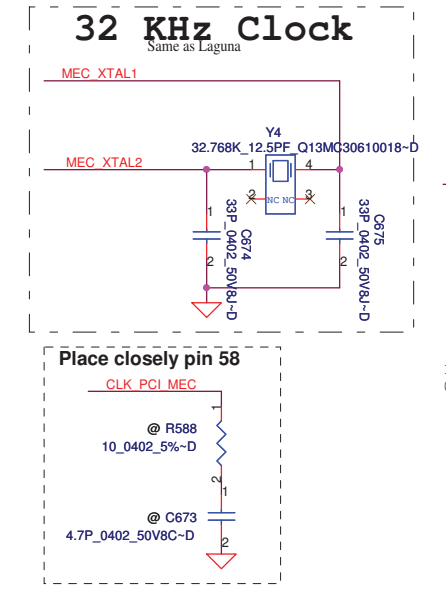
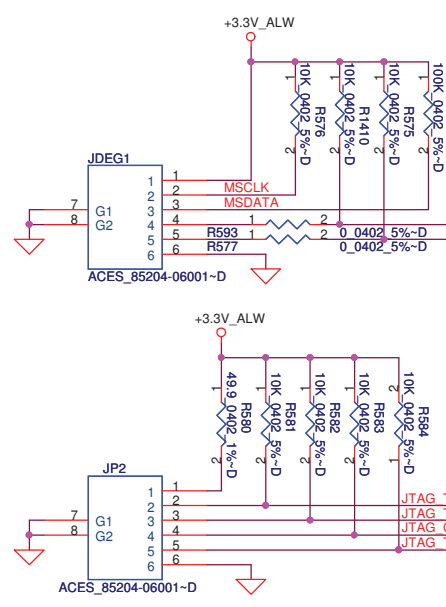
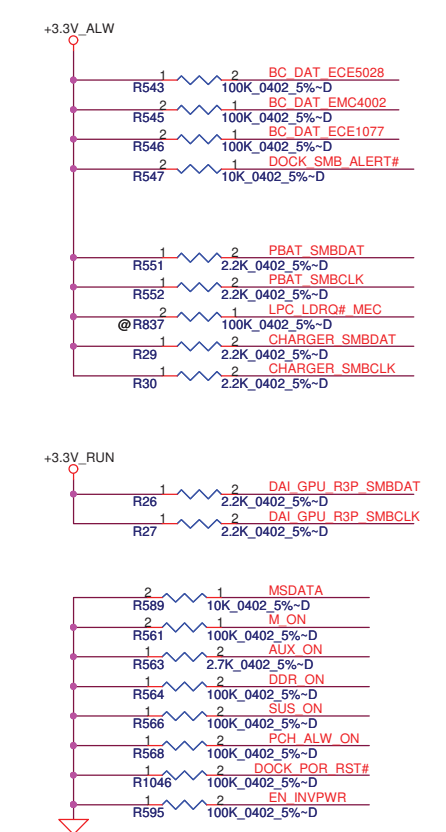
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Size: **LA-5471P**

Document Number: **LA-5471P**

Rev: **1.0**

Date: **Wednesday, January 20, 2010** Sheet **39** of **57**



R98	C919	REV
240K	4700p	X00
130K	4700p	X01
33K	4700p	X02
4.3K	4700p	X03
2K	4700p	X04
1K	4700p	A00

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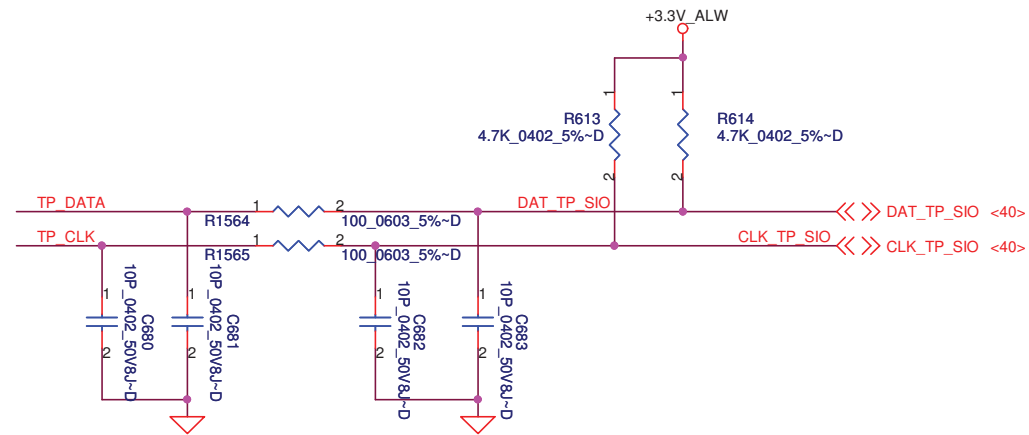
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Size: Document Number: **LA-5471P** Rev: 1.0

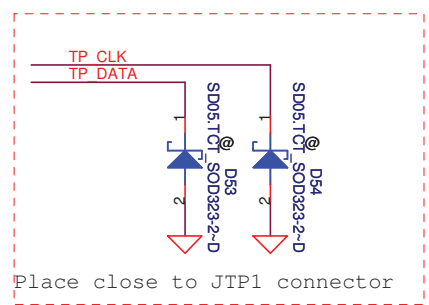
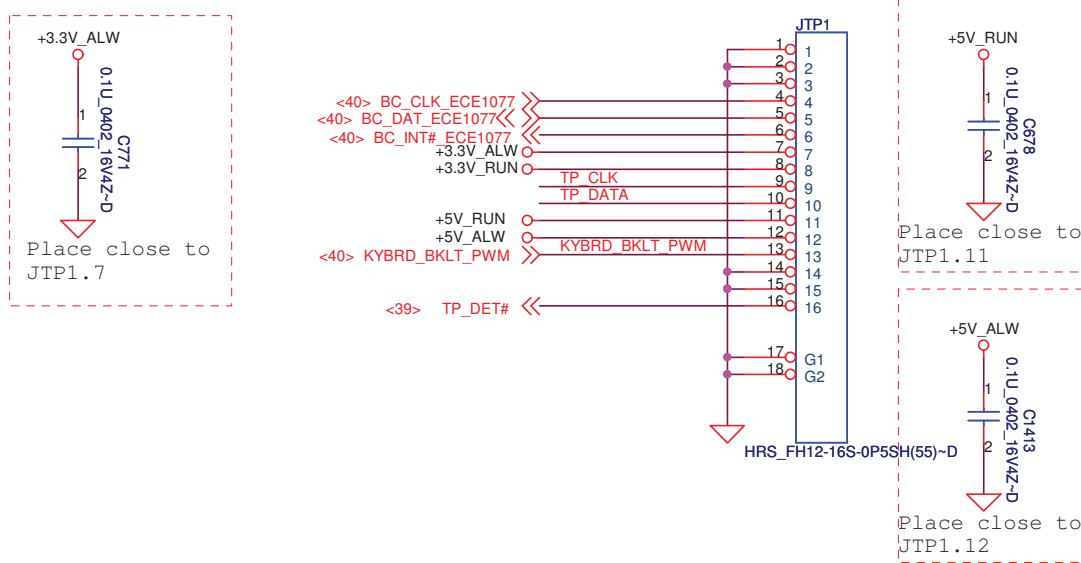
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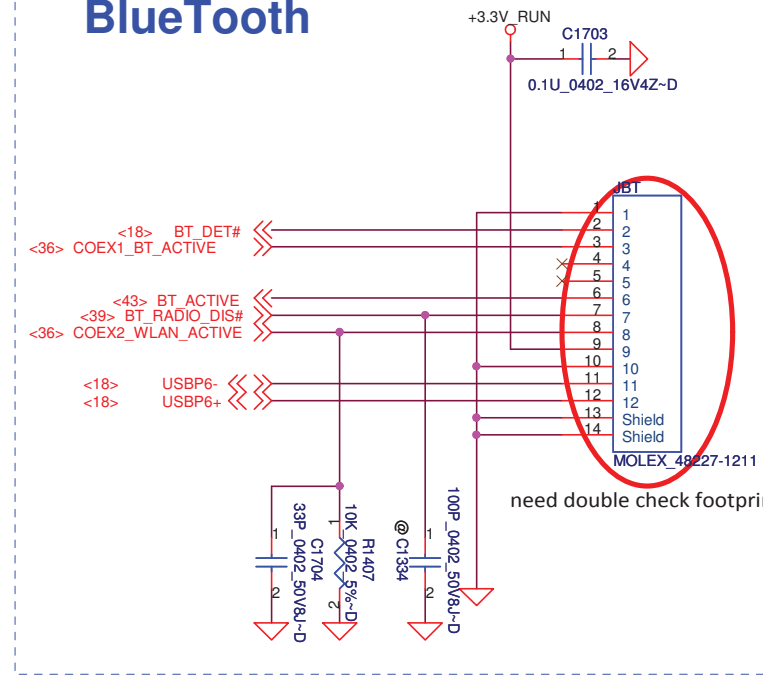
Touch Pad



Touch Pad Conn. Pitch=0.5

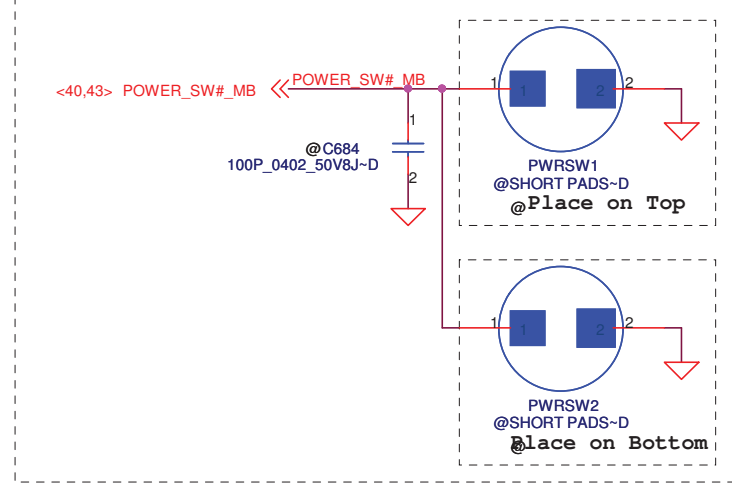


BlueTooth



@FAN	
Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA
@Speak	
Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG
@SM CARD BODY	
Part Number	Description
SP070007V0L	S SOCKET TYCO 1770551-1 10P H5.9 SMART
@PCMCIA BODY	
Part Number	Description
DC000001Q0L	PCMCIA TYCO 1759096-1
@MDC wire set cable	
Part Number	Description
DC02000CS0L	H-CONN SET ZGX MB-MDC
@T/P wire set cable	
Part Number	Description
DC02000840L	H-CONN SET ZJX MB-B/T-TP-FP
@LVDS cable	
Part Number	Description
DC020003Y0L	H-CONN SET ZJX MB-LCD 14 WXGA+ (-1ch)
@LVDS cable	
Part Number	Description
DC02000870L	H-CONN SET ZJX MB-LCD 14 WXGA+ (-2ch)
@RTC BATT	
Part Number	Description
GC20323MX00	BATT CR2032 3V 220MAH MAXELL

Power Switch for debug



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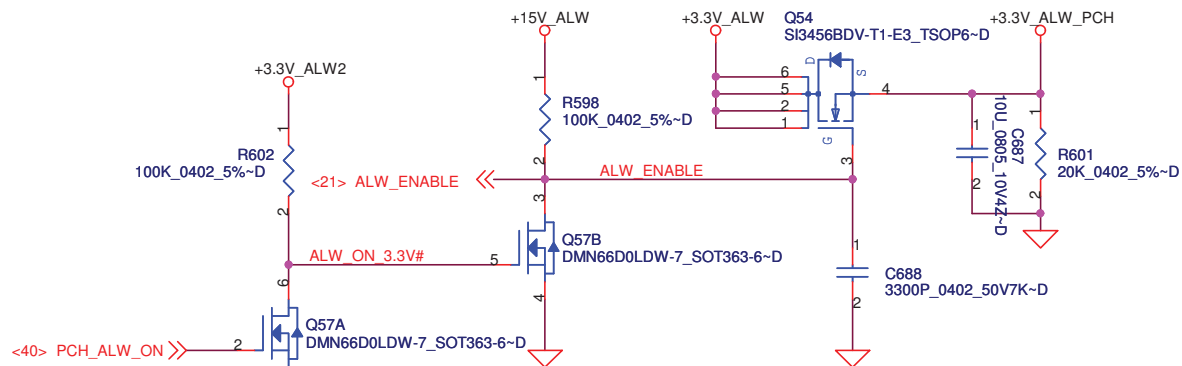
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Size	Document Number	LA-5471P	
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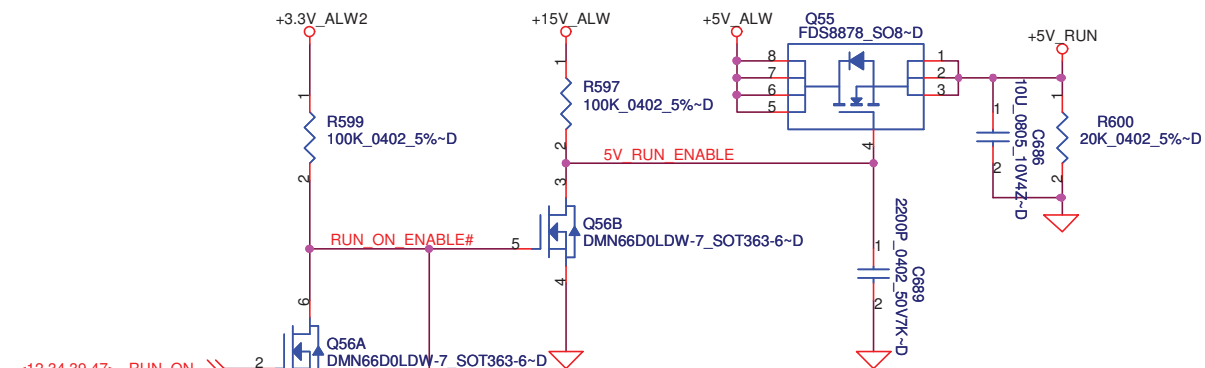


DC/DC Interface

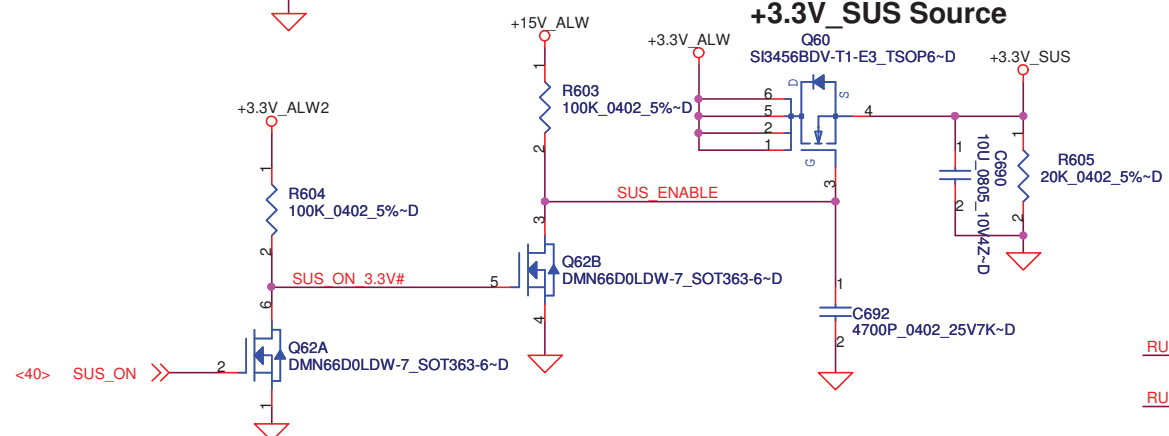
+3.3V_ALW_PCH Source



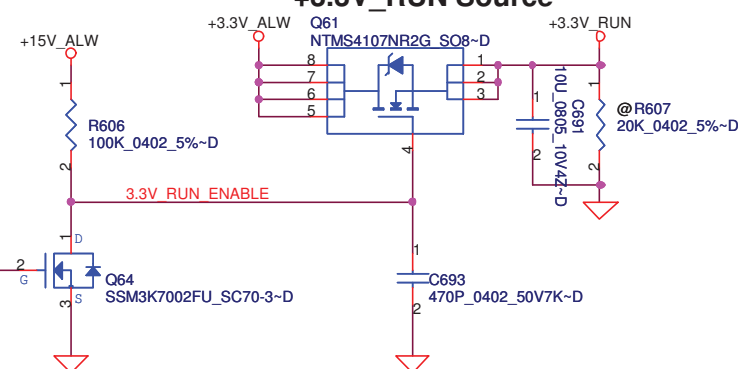
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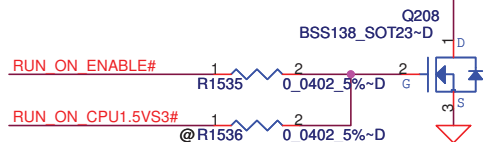
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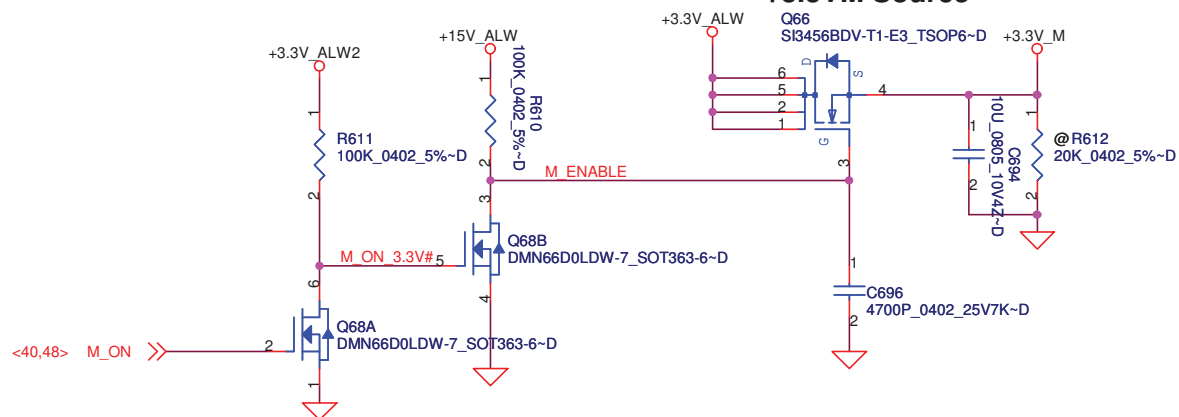
+3.3V_RUN Source



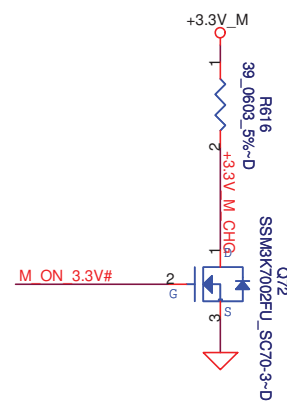
<8> 1.5V_PWRGD >>> R1508 >>> 100K_0402_5%-D >>> 0.75V_VR_EN <47>



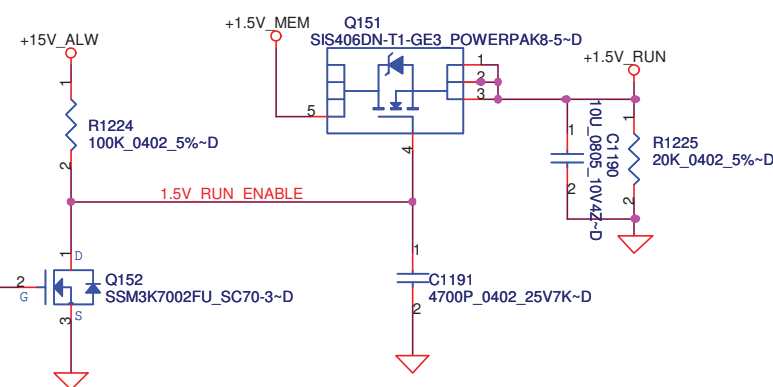
+3.3VM Source



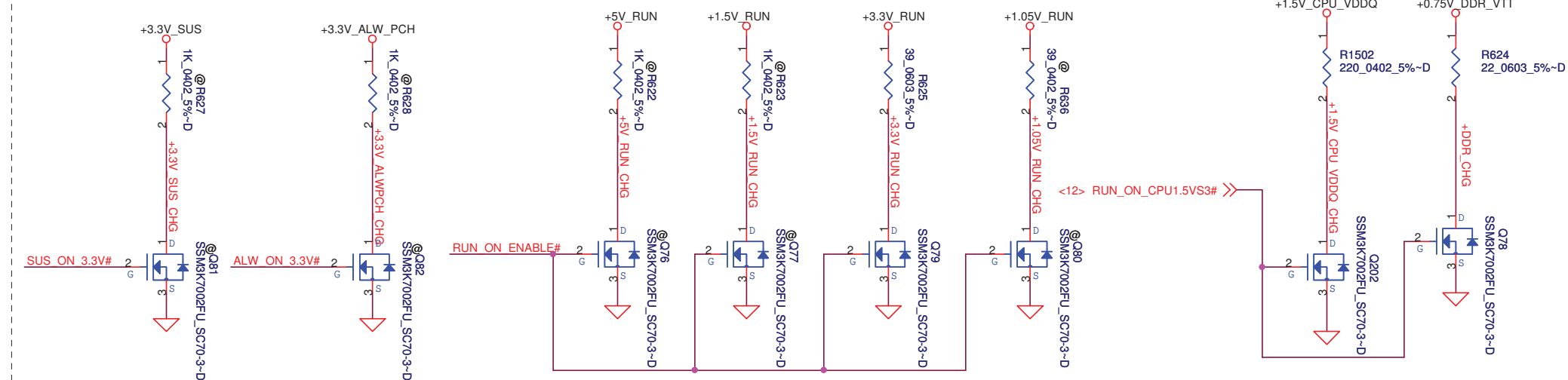
Discharg Circuit



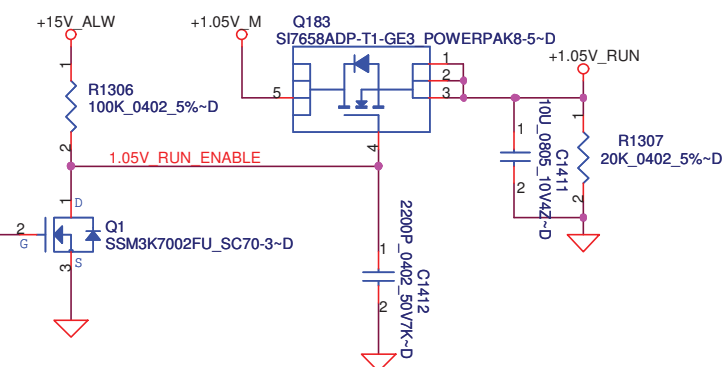
+1.5V_RUN Source



Discharg Circuit



+1.05V_RUN Source

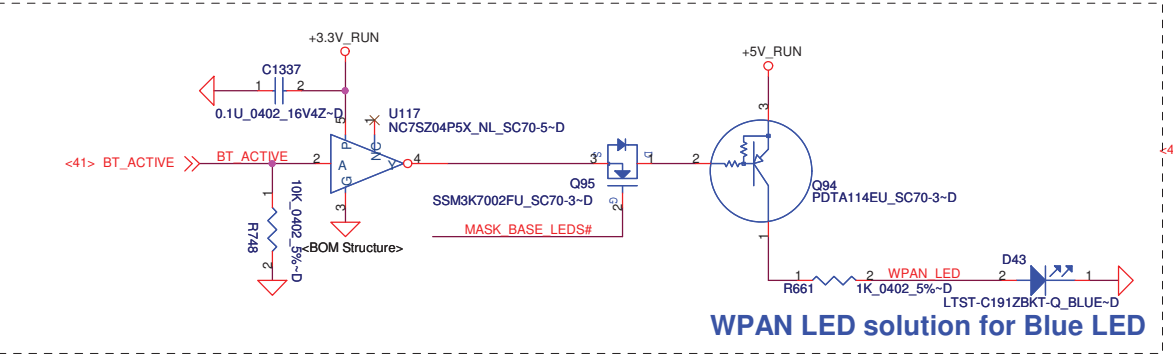
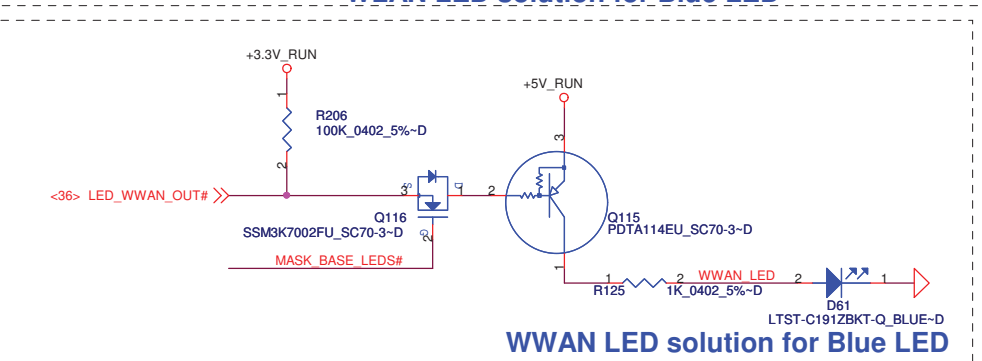
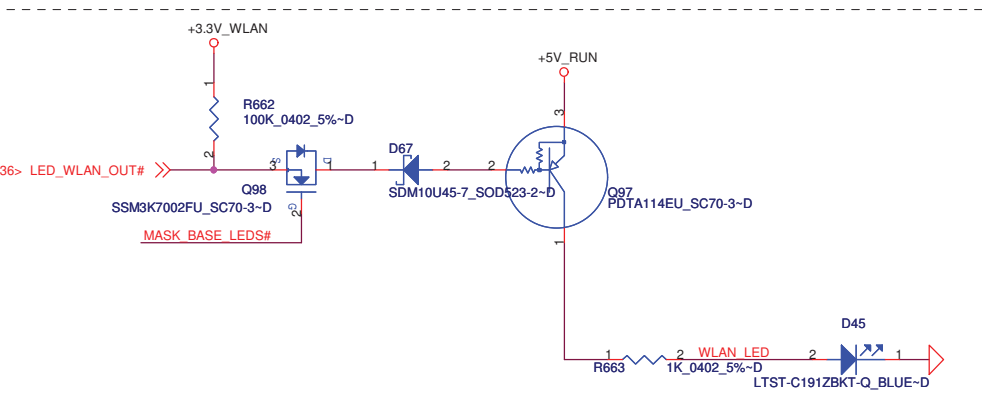
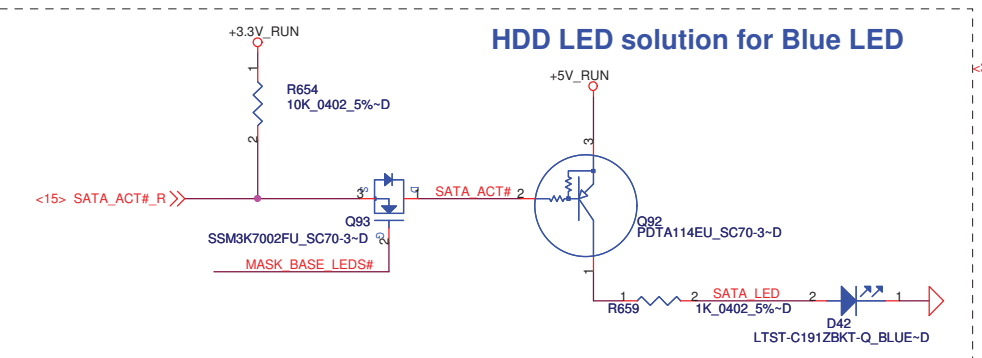


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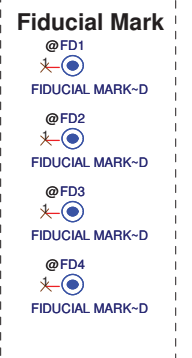
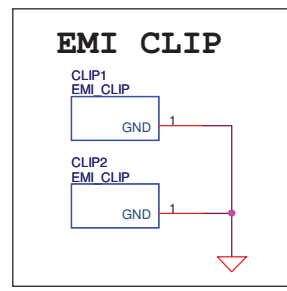
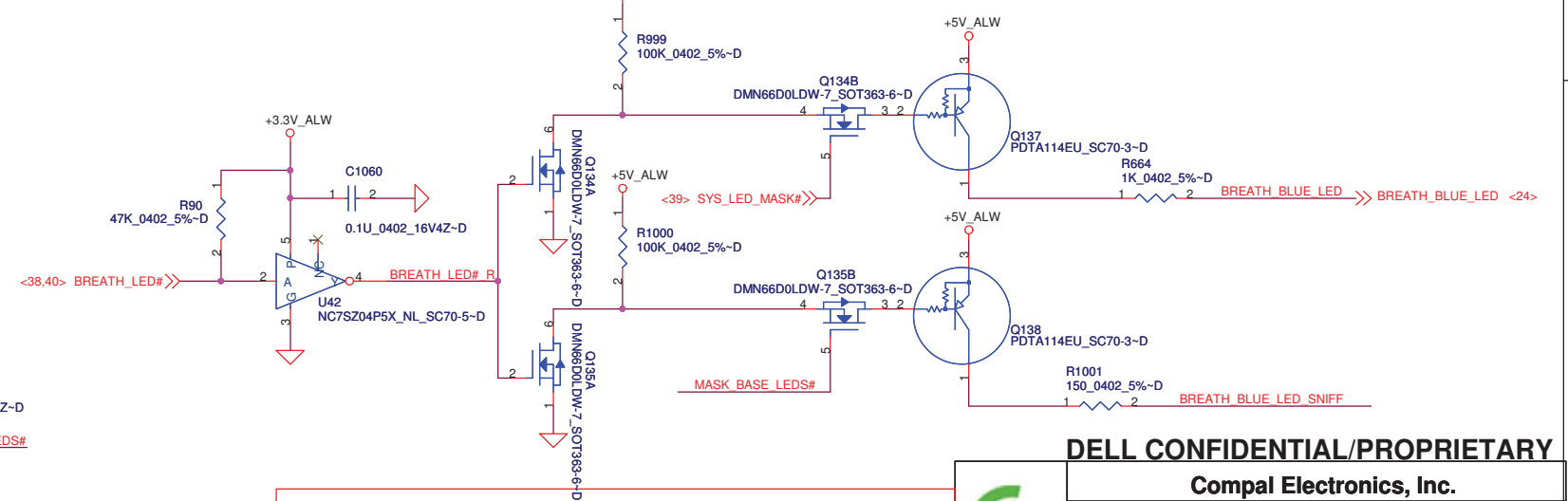
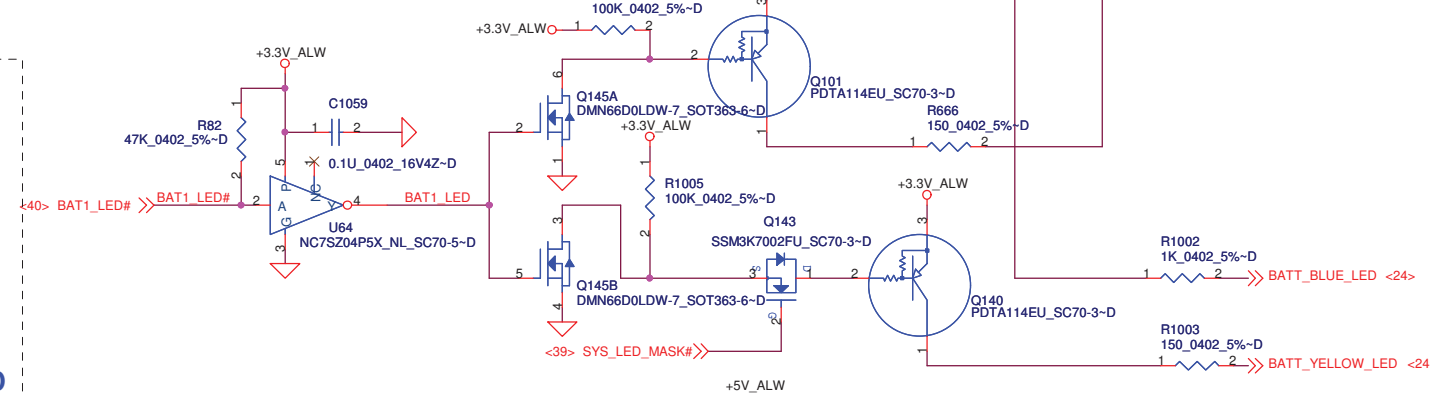
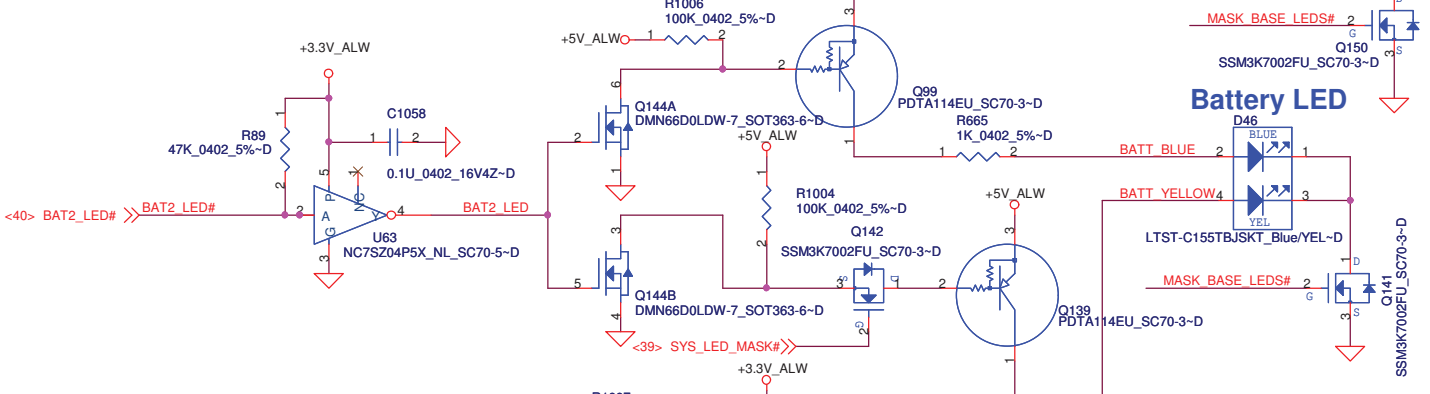
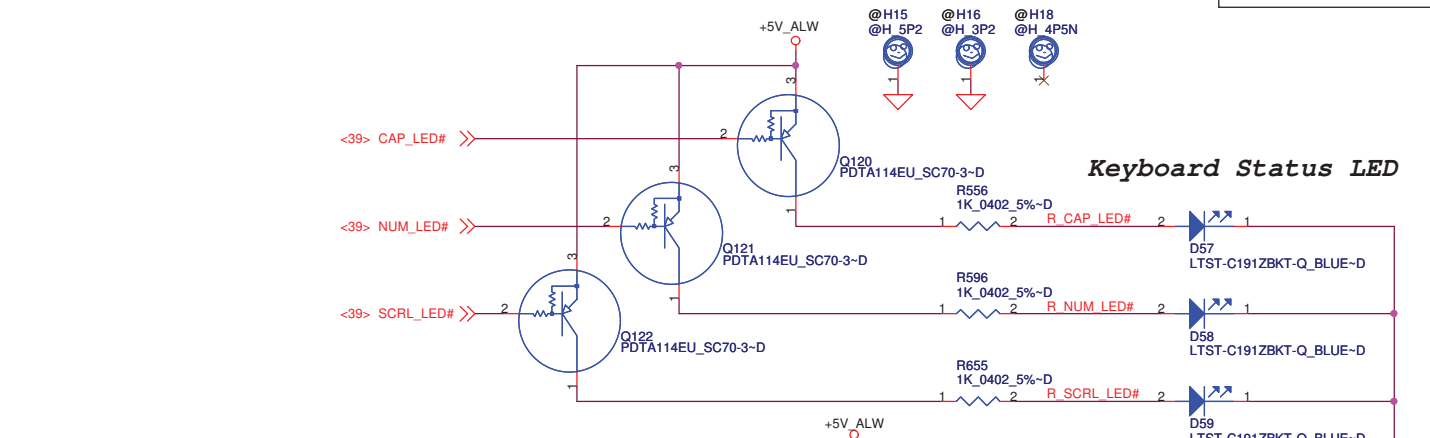
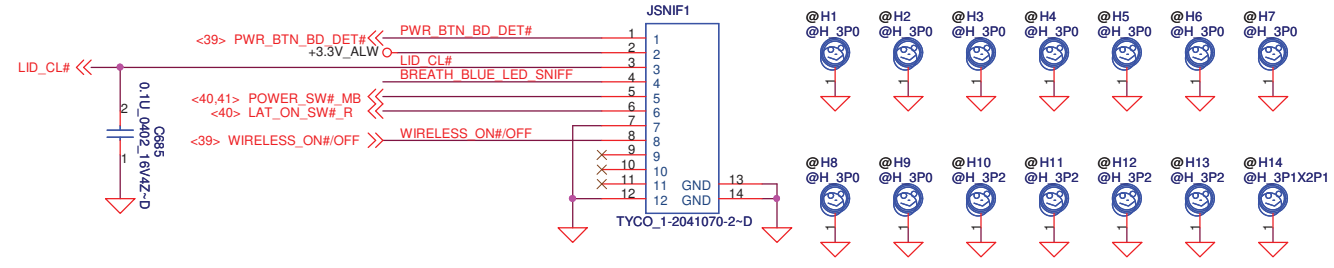
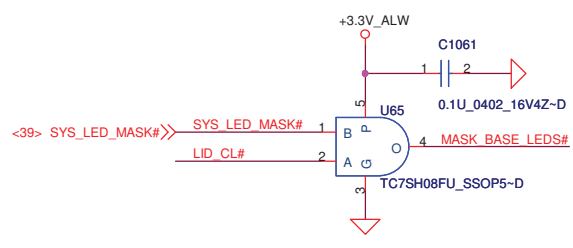
Title			POWER CONTROL
Size	Document Number	Rev	
	LA-5471P	1.0	
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LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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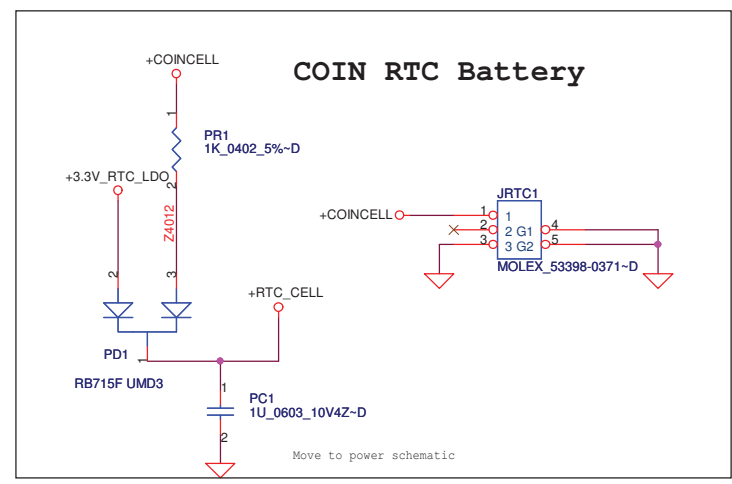
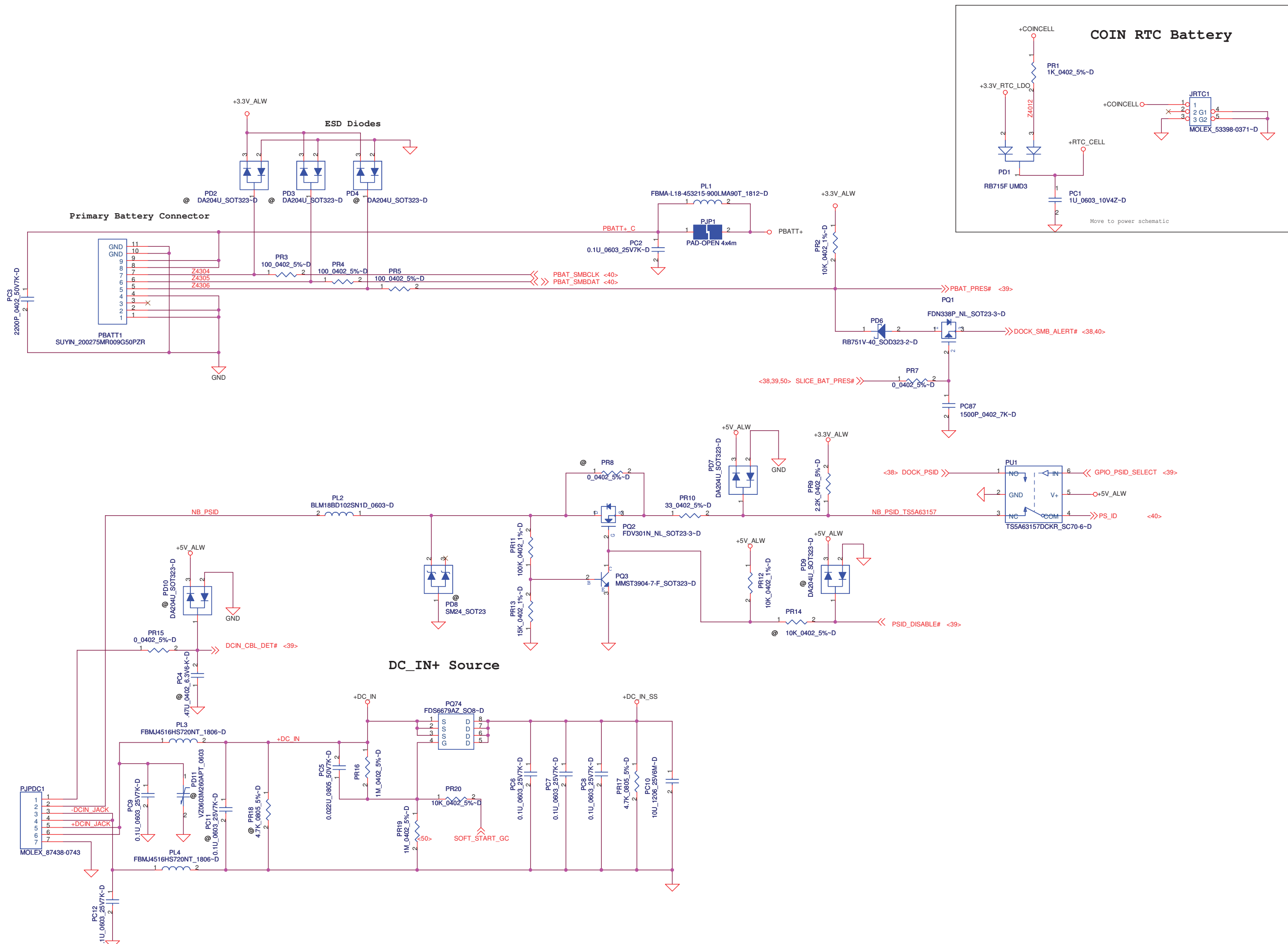
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PAD and Standoff

LA-5471P

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DC_IN+ Source

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Title: +DCIN		
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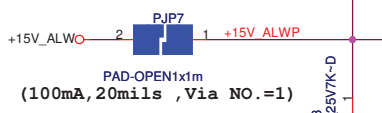
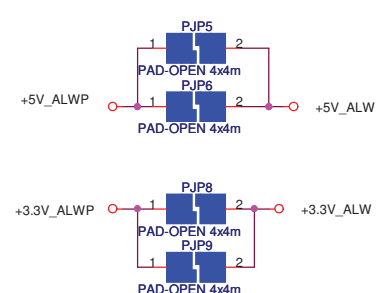
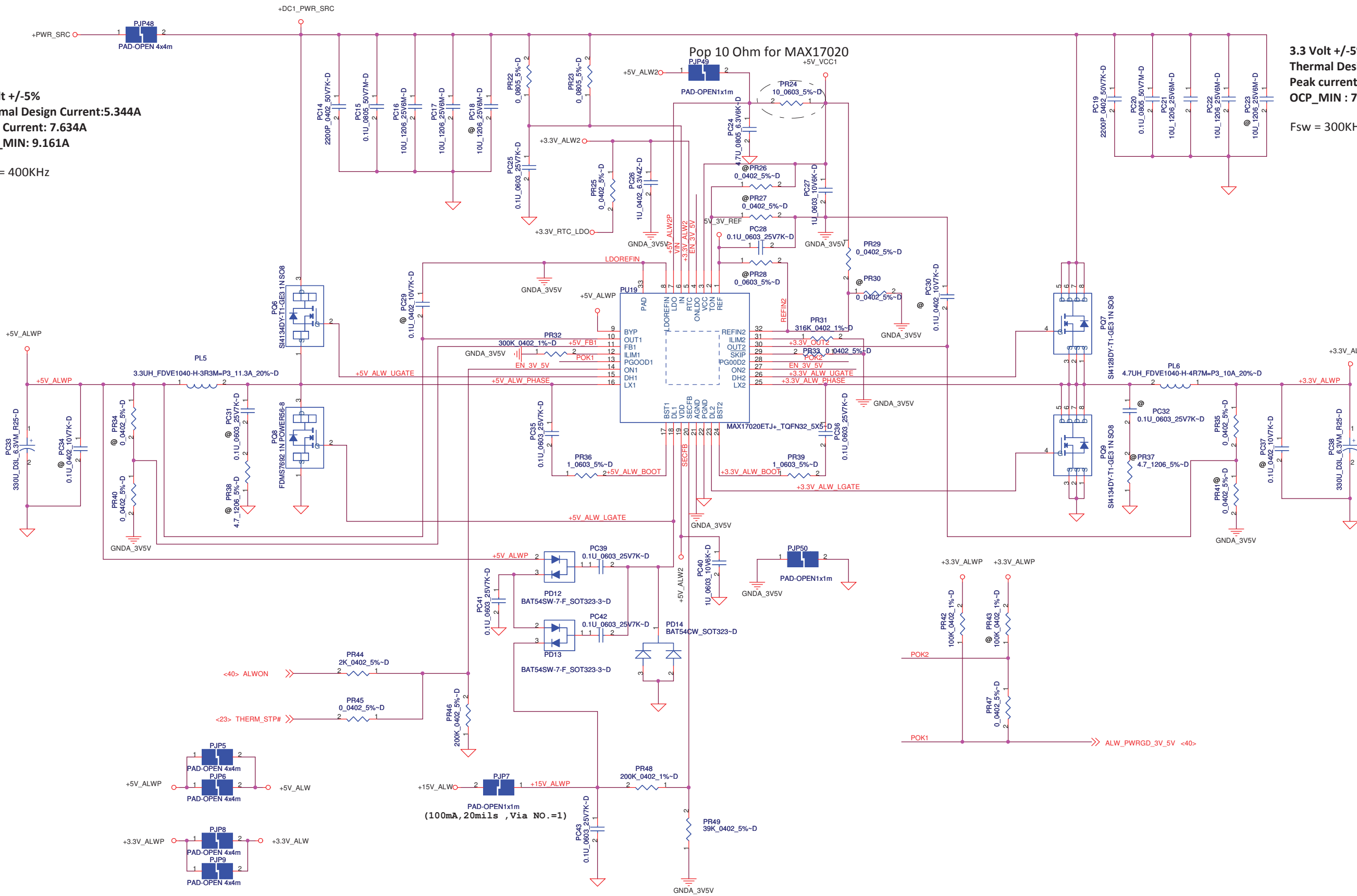
+3.3V_ALWP/ +5V_ALWP/ +5V_ALW2/ +15V_ALWP/ +3.3V_RTC_LDO

5 Volt +/-5%
Thermal Design Current: 5.344A
Peak Current: 7.634A
OCP_MIN: 9.161A

Fsw = 400KHz

3.3 Volt +/-5%
Thermal Design Current : 4.191A
Peak current : 5.988A
OCP_MIN : 7.186A

Fsw = 300KHz

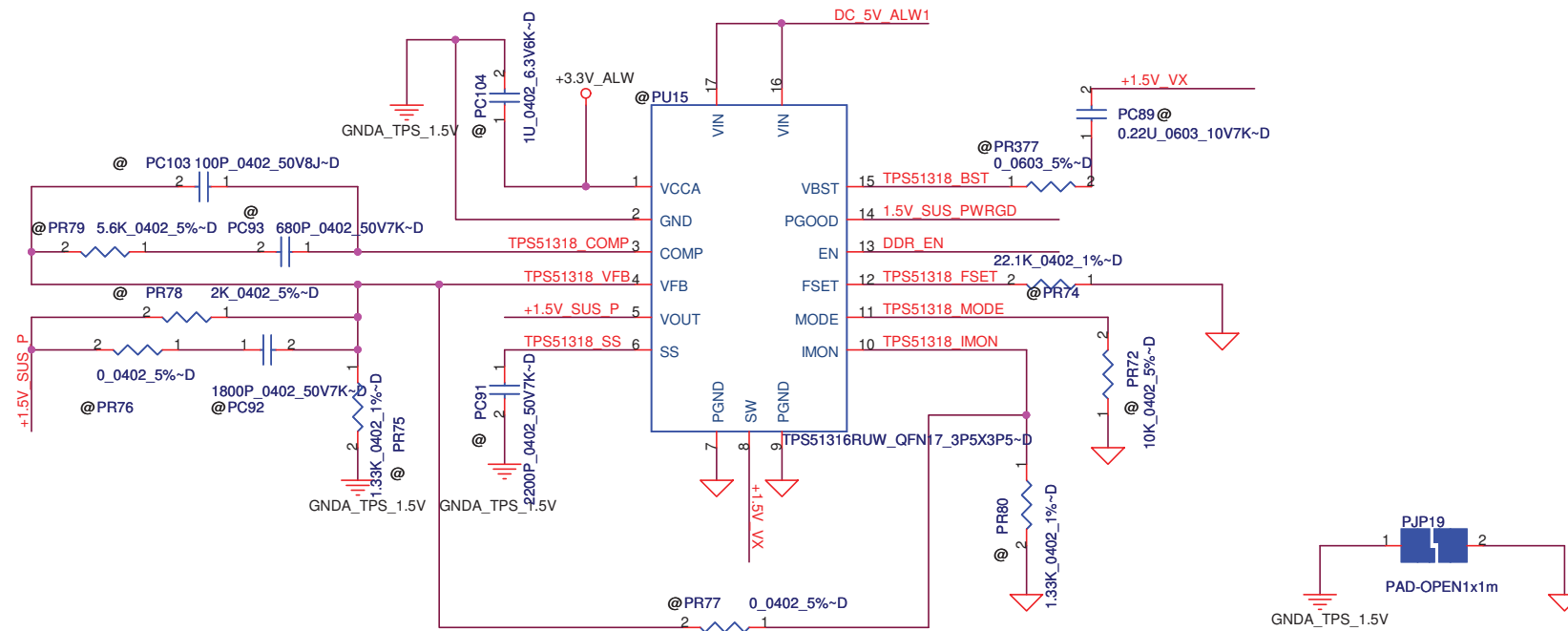


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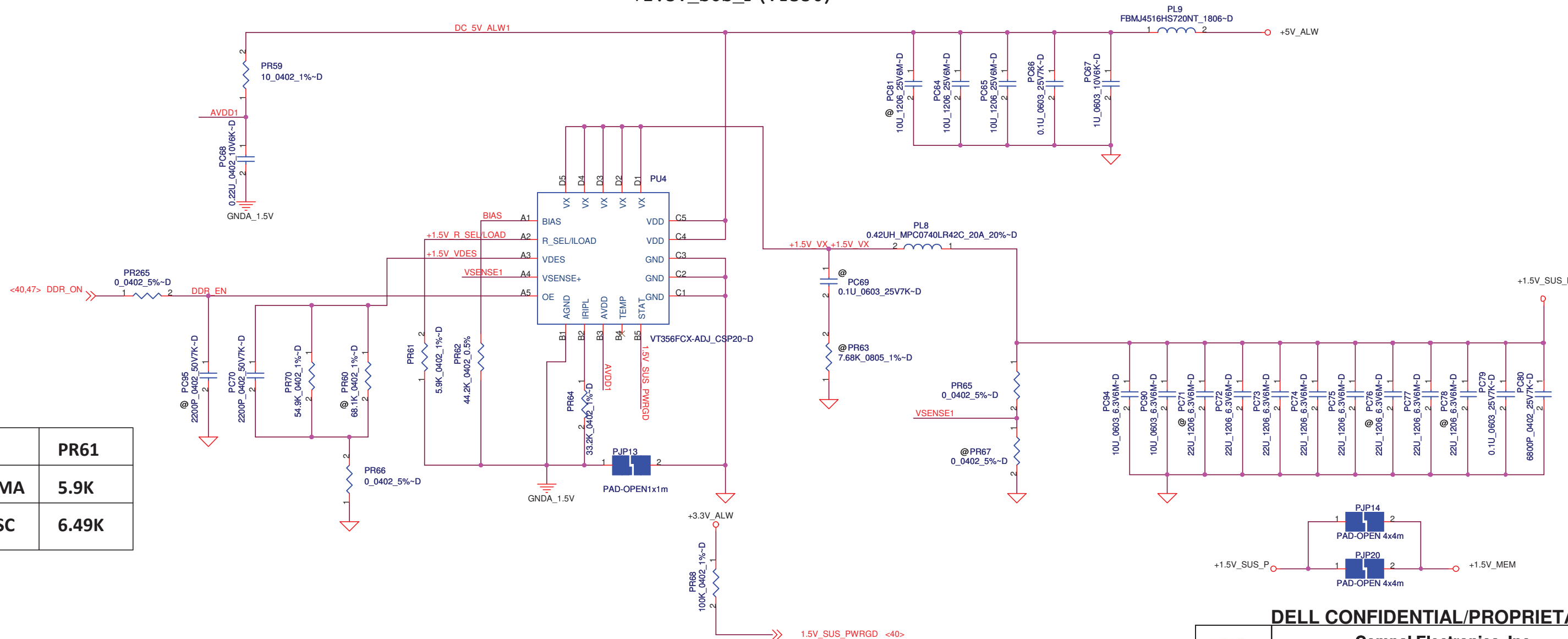
Compal Electronics, Inc.		
DC/DC +3V/ +5V		
Title	Document Number	
	LA-5471P	
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+1.5V_SUS_P (TPS51316)



1.5 Volt +/-5%
 Thermal Design Current : 5.828A
 Peak current : 8.326A
 OCP_MIN :9.991A

+1.5V_SUS_P (VT356)



	PR61
UMA	5.9K
DSC	6.49K

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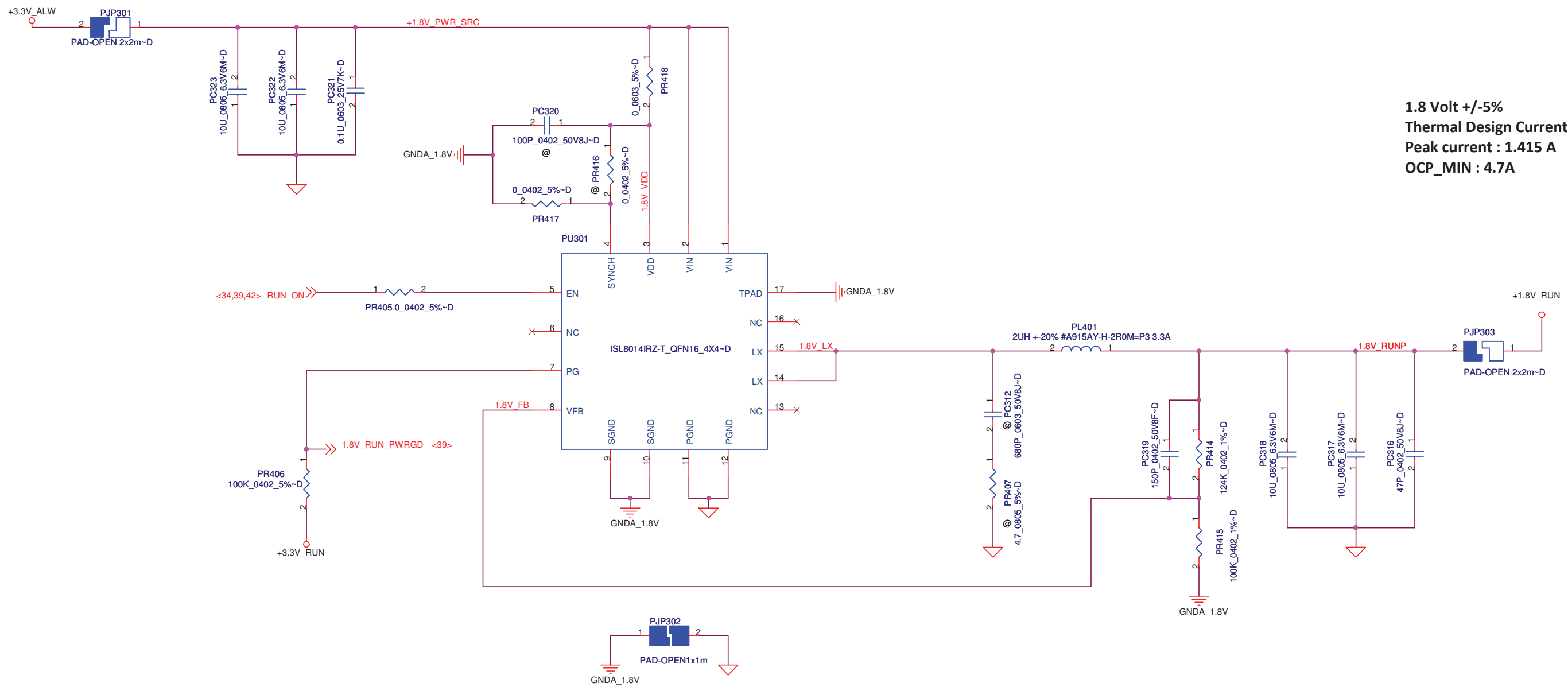
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Title +1.5V MEM	
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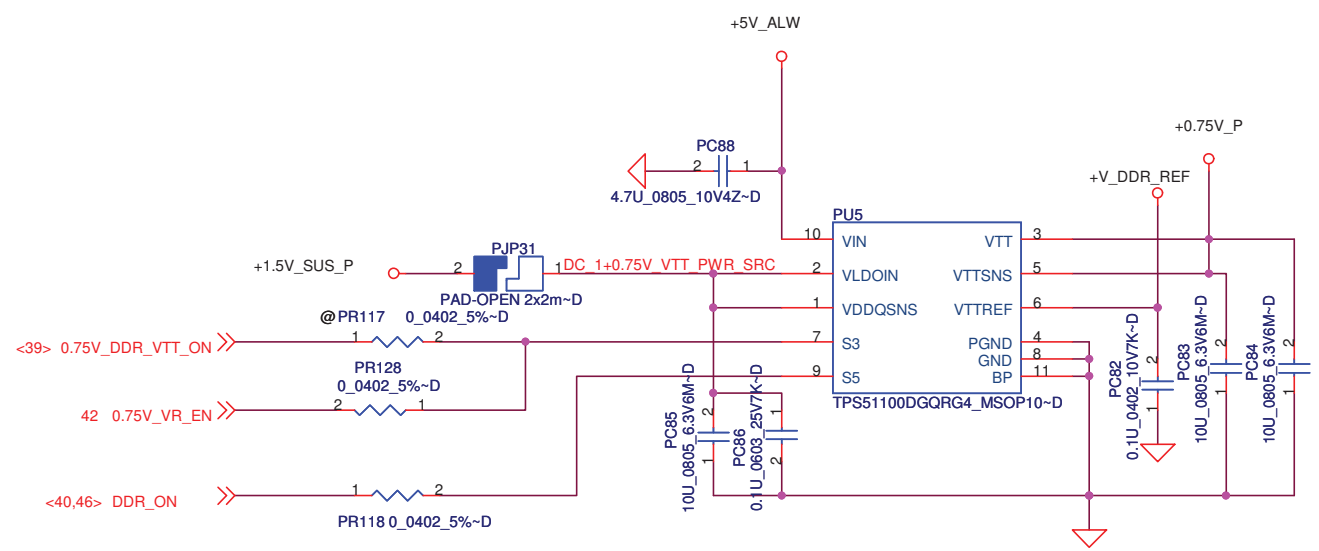
+1.8V_RUN



1.8 Volt +/-5%
Thermal Design Current : 0.99A
Peak current : 1.415 A
OCP_MIN : 4.7A

+0.75V_DDR_VTT

DDR3 Termination



0.75Volt +/-5%
Thermal Design Current: 0.525A
Peak current: 0.750A
OCP mini: 0.900A

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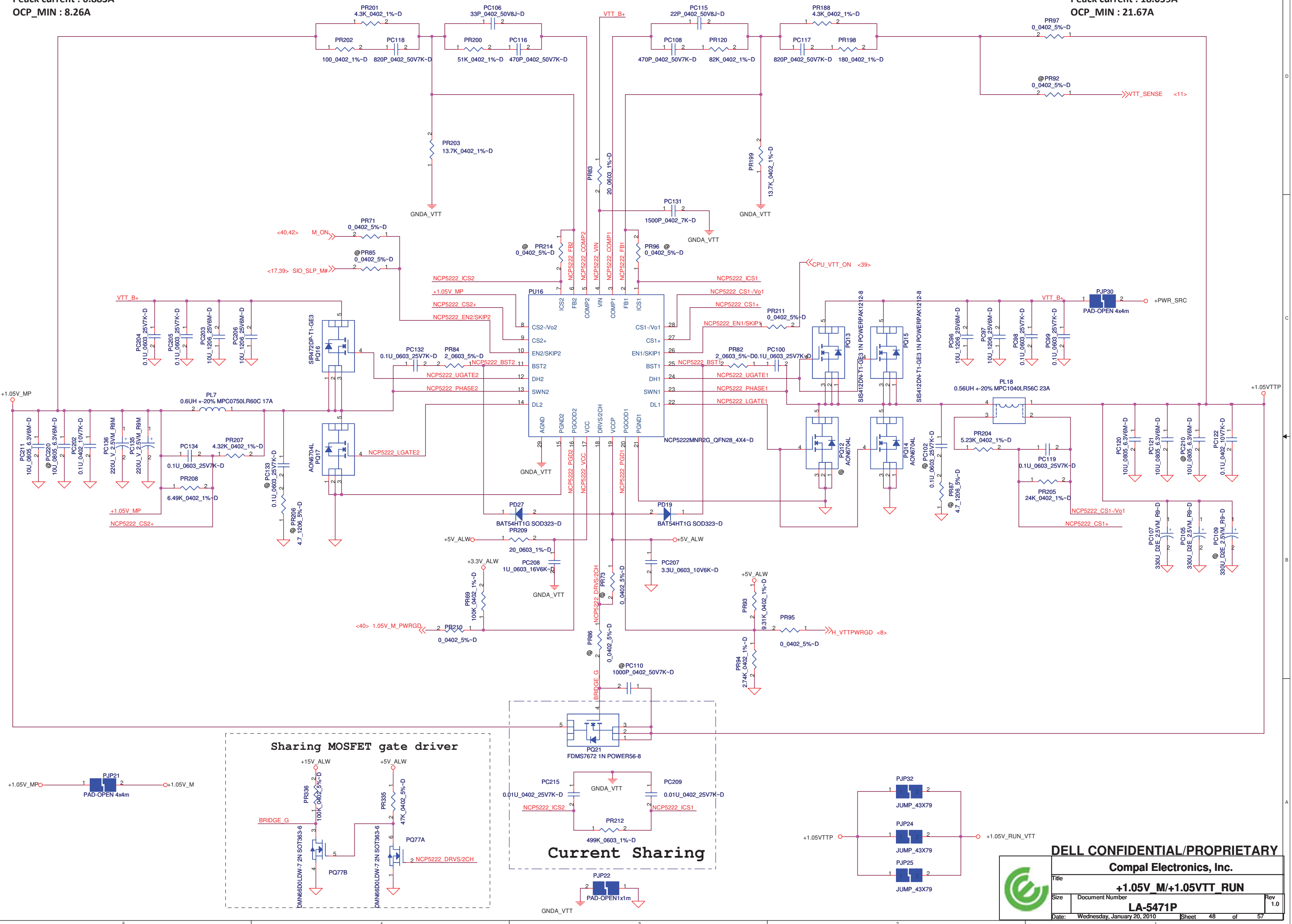
Compal Electronics, Inc.		
+0.75V_DDR_VTT/+1.8V_RUN		
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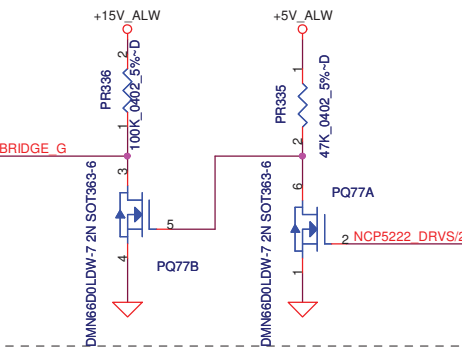
1.05 Volt +/-5%
 Thermal Design Current : 4.818A
 Peack current : 6.883A
 OCP_MIN : 8.26A

+1.05V_M/+1.05VTT_RUN

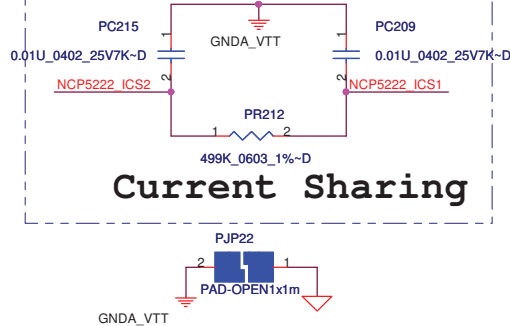
1.05 Volt +/-5%
 Thermal Design Current : 18A
 Peack current : 18.059A
 OCP_MIN : 21.67A



Sharing MOSFET gate driver

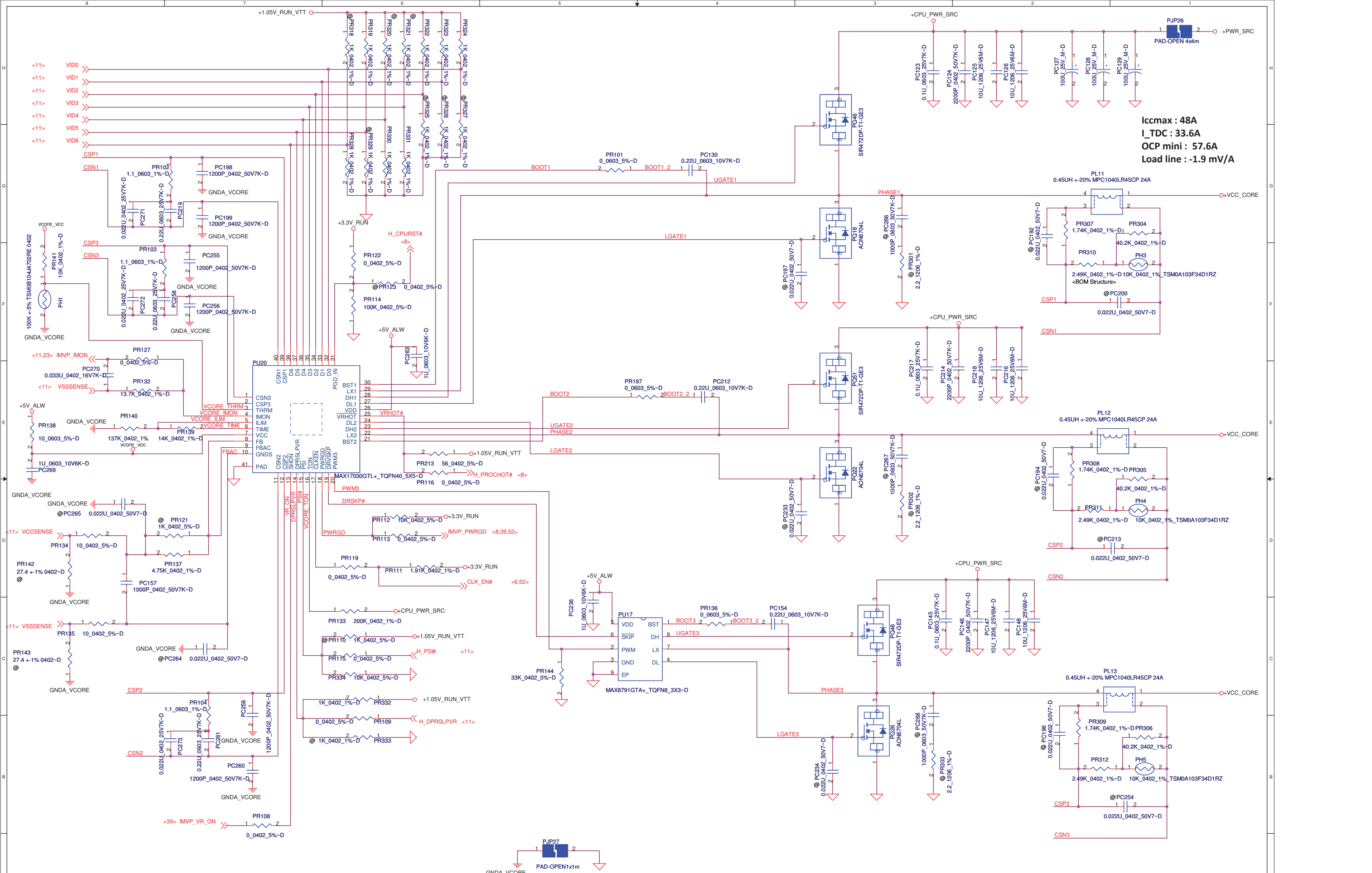


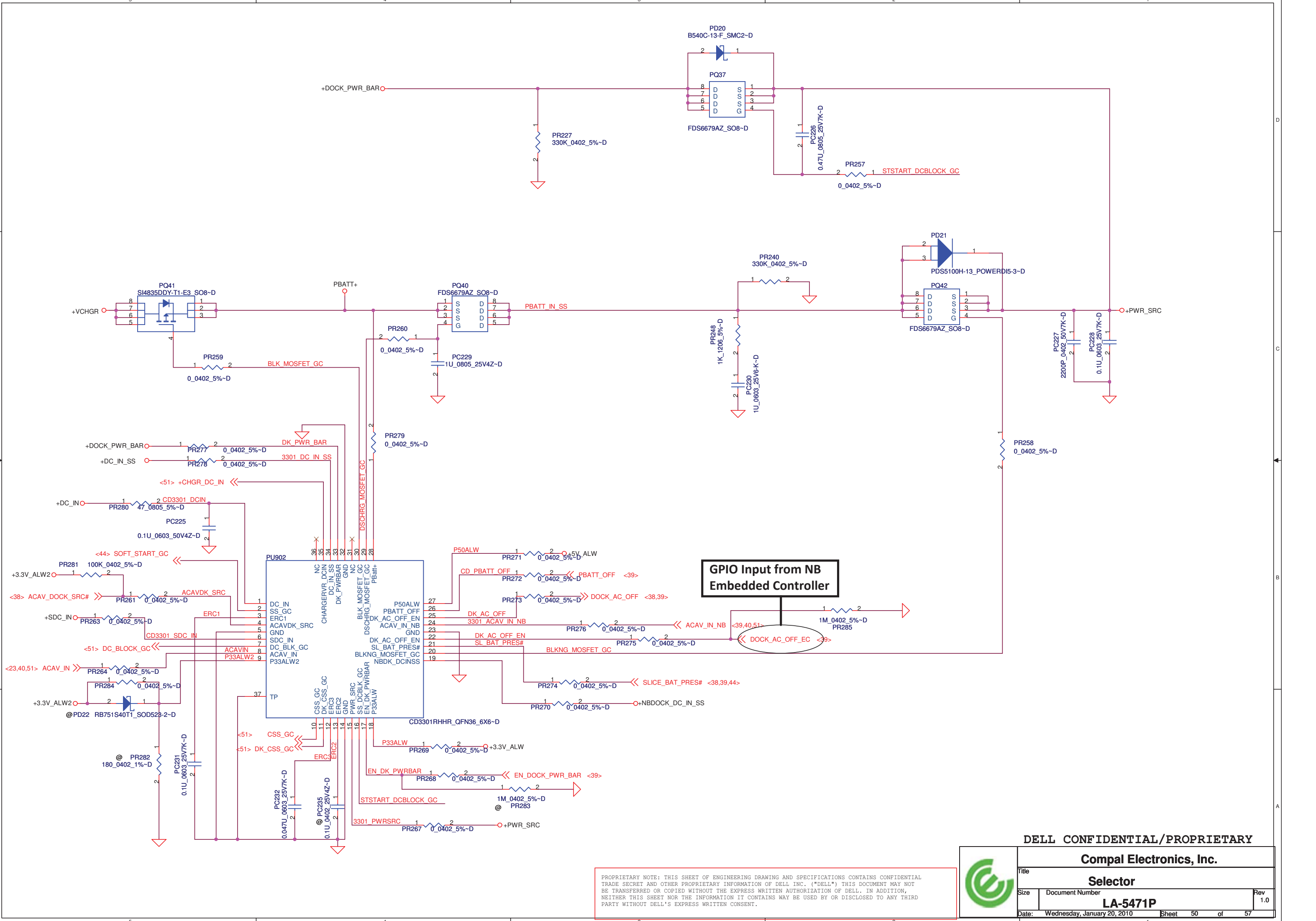
Current Sharing



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+1.05V_M/+1.05VTT_RUN		
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GPIO Input from NB Embedded Controller

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Selector

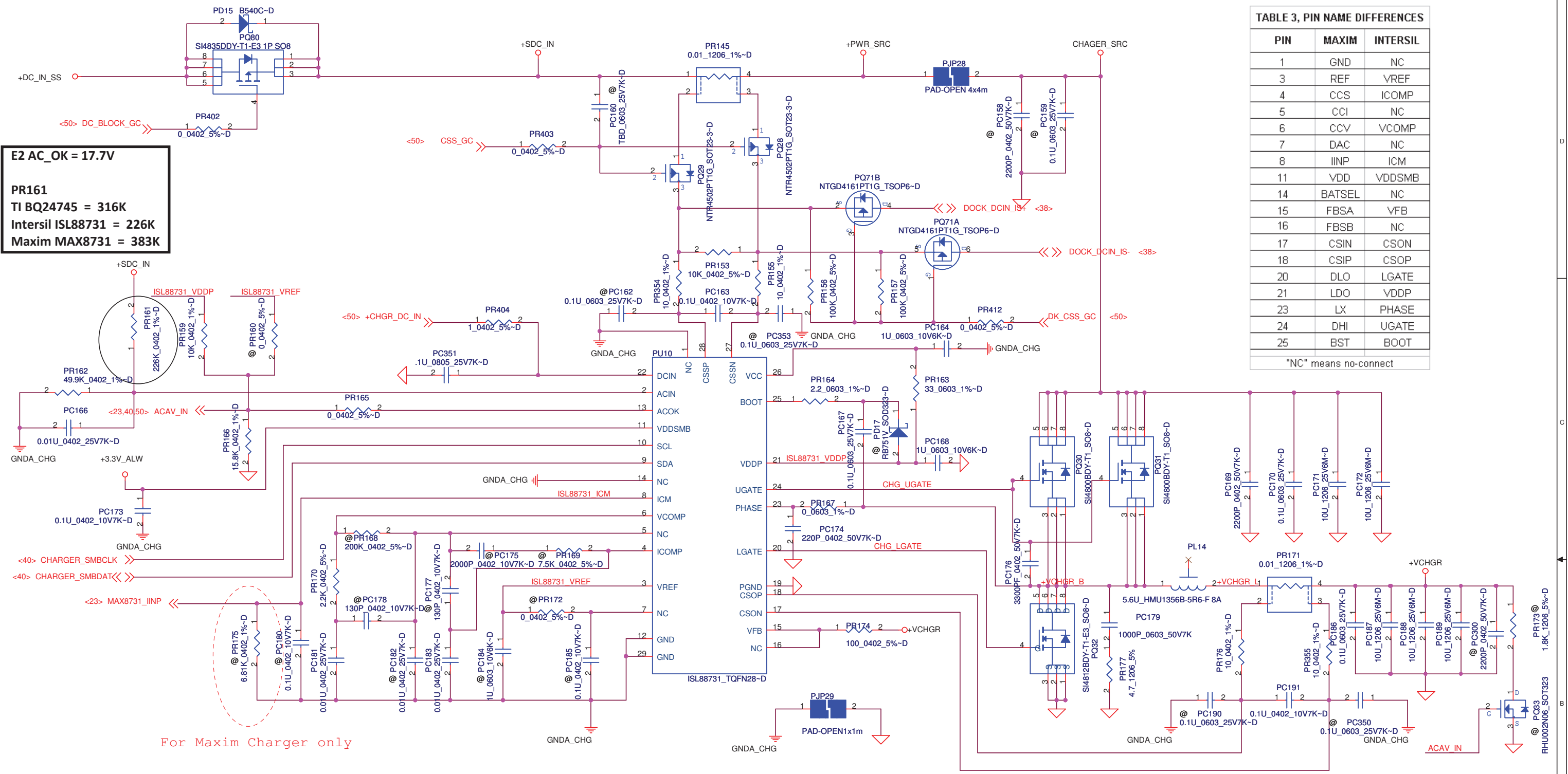
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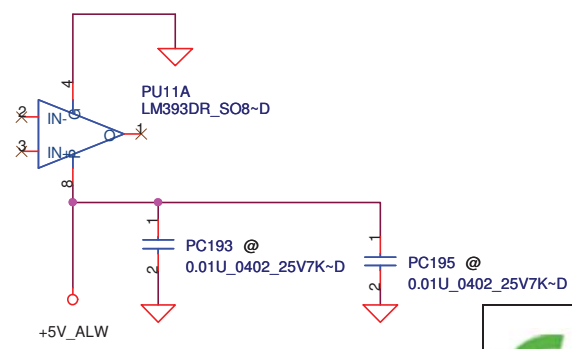
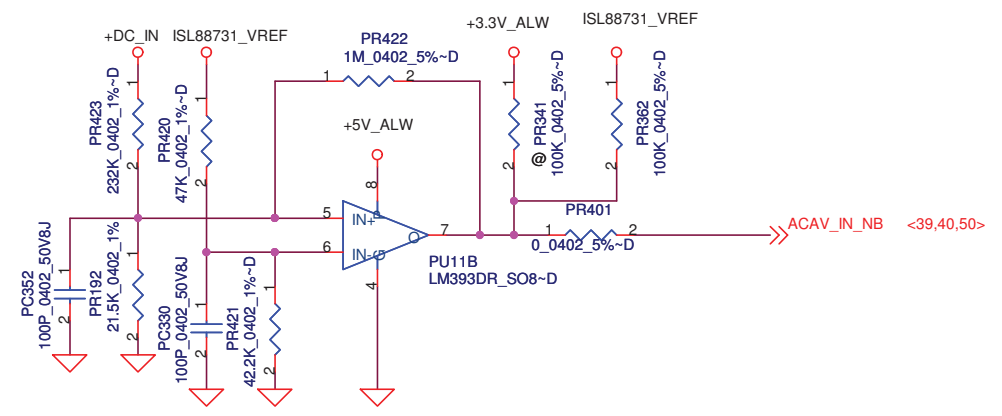
E2 AC_OK = 17.7V
PR161
TI BQ24745 = 316K
Intersil ISL88731 = 226K
Maxim MAX8731 = 383K

TABLE 3, PIN NAME DIFFERENCES		
PIN	MAXIM	INTERSIL
1	GND	NC
3	REF	VREF
4	CCS	ICOMP
5	CCI	NC
6	CCV	VCOMP
7	DAC	NC
8	IINP	ICM
11	VDD	VDDSMB
14	BATSEL	NC
15	FBSA	VFB
16	FBSB	NC
17	CSIN	CSON
18	CSIP	CSOP
20	DLO	LGATE
21	LDO	VDDP
23	LX	PHASE
24	DHI	UGATE
25	BST	BOOT
"NC" means no-connect		



For Maxim Charger only

Maximum charging current is 6.24A



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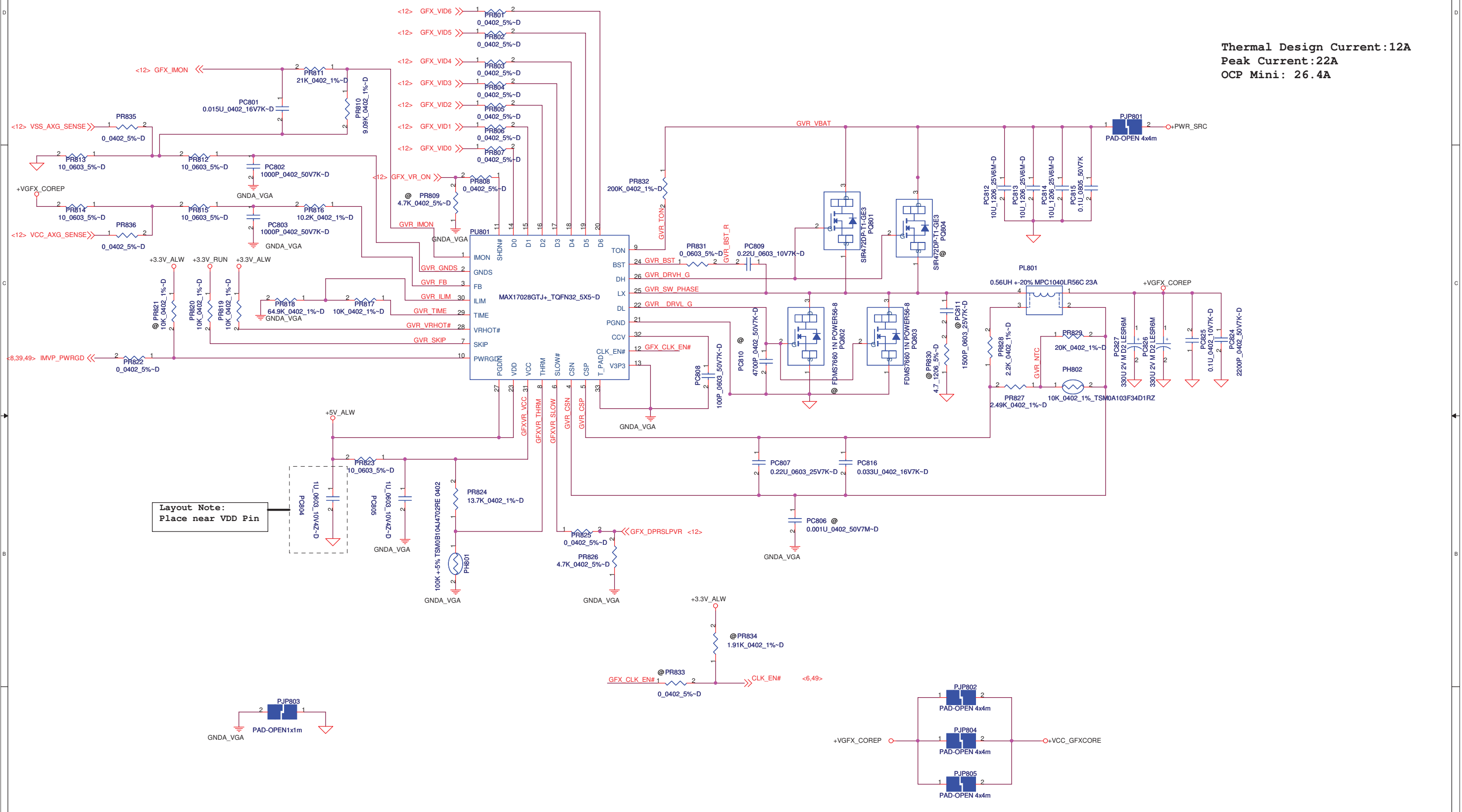
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Charger

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Thermal Design Current:12A
 Peak Current:22A
 OCP Mini: 26.4A



Layout Note:
Place near VDD Pin

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Title: **MAX17028 VGF_X Core**


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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	40	HW	7/13/2009	COMPAL	Board ID	R98 change to 130k ohm	X01
2	30	HW	7/13/2009	COMPAL	follow M09 +3.3V_LAN enable control circuit	depop R47	X01
3	8, 12, 13, 42	HW	7/13/2009	Intel	Intel S3 reduction circuit.	Add R1469, R1497~R1505, R1507~R1509, C1875, C1878~C1884, Q199~Q202, Q205, Q207, Q208, U141, PJP906, PJP907, change R879 to 1.5K, R880 to 750ohm, R624 to 22 ohm, change CPU CDDQ power source from +1.5V_MEM to +1.5V_CPU_VDDQ, change +.075_DDR_VTT discharge gate from RUN_ON_ENABLE# to RUN_ON_CPU1.5VS3#, add +1.5V_CPU_VDDQ discharge circuit, add net "DDR_HVREF_RST_GATE" from U36.A34 to Q119.2, "CPU1.5V_S3_GATE" from U36.A36 to R1501	X01
4	31	HW	7/22/2009	Broadcom	change C718 value	change C718 from .47uF to .22uF	X01
5	23	HW	7/22/2009	DELL	Follow DELL request to remove R3P circuit.	delete U140, R136, R138, R156,R507, R516, R519, R529, R531, R534~R536, R594, R1457, R1458, R1462, R1463, C434, C72, C73, C391, C406, pop R142, D2, C219	X01
6	41, 37	HW	7/22/2009	COMPAL	Per M09 lesson learn request	Re-define JTP1, JBI01	X01
7	19	HW	7/22/2009	Intel	GPIO1, 6, 7 need to PU if no used.	Add R1510, R1511	X01
8	40	HW	7/22/2009	COMPAL	Follow SMSC5045 spec	Add R1512, @C1885, C1886, change R560 to 100Kohm, add net name LAT_ON_SW#_R	X01
9	16	HW	7/22/2009	Intel	Intel Sighting report 3306048 to pop 25MHz crystal.	pop Y6, R685, C1168 (change to 18p), change R381 to C1887(18p)	X01
10	31	HW	7/22/2009	Broadcom	remove RFID disable circuit	remove R1062~R1065	X01
11	24	HW	7/22/2009	COMPAL	CAM Module change from 7pin to 8 pin.	change pin define for JEDP1	X01
12	31	HW	7/22/2009	Broadcom	R898 and R485 pop at the same time.	depop R898	X01
13	29	HW	7/29/2009	COMPAL	EMI solution.	change R1295 to L4 (220ohm) and R1215 from 22ohm to 47ohm.	X01
14	42	HW	7/29/2009	COMPAL	base on de-rating report.	change Q61 from AO4456 to NTMS4107	X01
15	36, 39	HW	7/29/2009	DELL	GPIO MAP update	Add connection from JMINI3.20 to 5028 pin A56, named "UWB_RADIO_DIS#"	X01
16	37, 39	HW	7/29/2009	DELL	GPIO MAP update	Add reserved R1513 between U95.18 and +3.3V_RUN, add R1514 between U95.18 and 5028.A47 named EN_ESATA_RPTR.	X01
17	42	HW	7/29/2009	COMPAL	resolve leakage issue.	Pop R625 and Q79, change R625 to 0603 size.	X01
18	31	HW	7/29/2009	Broadcom	resolve 5882 leakage issue	add R1515, Q209, Q210	X01
19	26	HW	7/29/2009	COMPAL	resolve 8200 DVI can't work issue.	add R1516	X01
20	31	HW	7/29/2009	Broadcom	resolve smart cart can't work problem.	pop R775, R537, depop R776.	X01
21	36	HW	7/29/2009	COMPAL	Correct PU power rail for USB_MCARD1_DET#	change USB_MCARD1_DET# PU to +3.3V_RUN	X01
22	31	HW	7/29/2009	COMPAL	remove R1061 to avoid double PU and provide back-drive path.	remove R1061	X01
23	19	HW	7/29/2009	COMPAL	add PD to prevent floating at PCH GPIO22, GPIO34.	add R1520, R1521	X01
24	21	HW	7/29/2009	COMPAL	Follow the pop option on CRB1.6 to depop C39 for +VCCACLK, C610 for +SATAPLL, C111 and C112 for +1.05V_M_VCCEPW	de-pop C610, C39, C111, C112	X01
25	37	HW	7/31/2009	DELL	correct the connection for EN_ESATA_RPTR. it's not detect function.	change the connection from U95 Pin18 to Pin7	X01
26	27	HW	8/05/2009	COMPAL	base on EA and EMI test result on RGB	change L61~L63 to BLM188B050SN1D and C390, C518, C996, C251~C253 to 4.7p	X01
27	36	HW	8/05/2009	COMPAL	change the PU to +3.3V_RUN refer to the core power rail at PCH side.	change the PU for R458 from +3.3V_ALW_PCH to +3.3V_RUN	X01
28	18, 35, 36	HW	8/05/2009	DELL	Braidwood no longer support on Rothschild.	Delete NVM connection, delete R1411, R1452, R1453, R866, R872 , JBW1, C1851, C1852. Move JMINI1 power circuit to page 36.	X01
29	10	HW	8/06/2009	Intel	Follow Intel recomand to add debug TP.	Add T186~T190	X01
30	28	HW	8/06/2009	COMPAL	Follow M09 to change the PU to +3.3V_RUN	Pop R1239 and change the PU power rail from +5V_MOD to +3.3V_RUN	X01
31	31	HW	8/06/2009	Broadcom	Follow Broadcom request	delete T159, R494, R498, R631, R634, R898, C640, C641, C642 C647, C1026, L73, add R1522, C1887, C1888, change connection for R496, R497 to GND, change connection for JCS1 pin3 and pin4.	X01
32	23	HW	8/12/2009	COMPAL	FAN1_DET# should have 10K PU to +3.3V_M	add R1517	X01
33	40	HW	8/12/2009	SMSC	per AN 19.6 (section 6.7, page 19)	change R541, R554, R1512 from 1K to 10K.	X01
34	23	HW	8/12/2009	SMSC	The pull-up source of the R150 should be changed to +VCC_4002 by SMSC request	change R150 PU from +3.3V_M to +VCC_4002	X01
35	23	HW	8/12/2009	SMSC	Add discharge ckt for+3.3V_M, watch dog timer may not be resetED when EMC4002 VDD_PWRGD is not completely at Logic Low.	pop Q72 and R616, change R616 from 1K(0402) to 39ohm(0603)	X01
36	8	HW	8/12/2009	COMPAL	Follow Margaux to fix S3 power up sequence.	change C1880 from 0.01uF to 0.22uF	X01

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		Title: EE P.I.R (1/1)	
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
37	21	HW	8/12/2009	Intel	WW30 Calpella MoW, Intel request change L45 & L46 to 10uH, DCR=0.36 ohm	change L45, L46 from 10UH_LB2012T100MR_20% to 10UH_LBR2012T100M_20%	X01
38	26, 38	HW	8/12/2009	Intel	Per Intel check list rev1.6, change PD value of HPD signals from 100K to 110K ohm.	change R186, R191, R796, R798 from 100Kohm to 110Kohm	X01
39	39	HW	8/12/2009	COMPAL	VGA_ID_DISC and VGA_ID_UMA should pulled up to +3.3V_ALW	change PU from +3.3V_RUN to +3.3V_ALW for R875, R881	X01
40	31	HW	8/13/2009	Broadcom	Base on Broadcom review for Margaux.	add @R1523, R1524, change C718 to 470nF, C646 to 220nF.	X01
41	15, 30, 33, 40	HW	8/13/2009	COMPAL	Base on EA result for all X'tal and OSC.	change C296, C297 to 12pF, C476 to 33pF, C427 to R1526(200ohm), C674&C675 to 33pF, R421 to 100ohm	X01
42	8	HW	8/13/2009	Intel	Refer to Intel S3PowerReduction_whitePaper_Rev0.9	add R1525 and C1890	X01
43	33, 34	HW	8/13/2009	Ricoh	Correct the Cardbus Controller to R5U242 on PT phase.	change R46 to C1889, C21 from 10uF to 47uF, correct symbol to R5U242	X01
44	30	HW	8/14/2009	Intel	bsae on Intel review result.	remove +LOM_VCT, R562, C41, depop C712 and change the net name to +LOM_VCT_IO, add C1891	X01
45	19, 37	HW	8/14/2009	COMPAL	GPIO MAP update for EN_ESATA_RPTR#.	add @R1528, @Q211, pop R1513, depop R1514, change net name from GPIO16 to EN_ESATA_RPTR#	X01
46	8, 40	HW	8/14/2009	COMPAL	GPIO MAP update for CPU_DETECT#	Add R1529, delete TP1, connect JCPU.AH24 to U36.B18	X01
47	37	HW	8/17/2009	COMPAL	Base on EMI team request to reserve command choke for test	Add L90, L91, @R1530~ @R1533, change L64 to 2@, depop R791, R792.	X01
48	30	HW	8/17/2009	Intel	bsae on Intel review result.	reserved R1534.	X01
49	42	HW	8/18/2009	COMPAL	reserved pop option to improved S3 circuit.	add R1535, @R1536	X01
50	31	HW	8/18/2009	COMPAL	base on Smart card EA result.	R772 to 47 Ohm and C1015 to 10pF	X01
51	28, 37	HW	8/18/2009	COMPAL	base on SATA EA result on HDD and ESATA	depop R1308, R1298, pop R1304, R1031	X01
52	26	HW	8/20/2009	Pericom	Per Pericom: Add 100pf to GND between the source and 8200	add C1893, C1894	X01
53	26	HW	8/20/2009	COMPAL	reserved for dubug.	reserved R1537~R1539	X01
54	16	HW	8/21/2009	COMPAL	Base on EA result on Crystal.	change Y6 to SJ100006M0L (CL=12P)	X01
55	29	HW	8/21/2009	COMPAL	Base on Vender suggestion	change X4 to SiTime 12MHZ_15PF_SIT8102AC3333E12T	X01
56	36	HW	8/23/2009	COMPAL	Follow EA result	add R1540~R1542	X01
57	24	HW	8/23/2009	COMPAL	follow eDP specification.	delete R279 and R1027	X01
58	21	HW	8/24/2009	COMPAL	base on EA result to solve SATA eye.	delete R557	X01
59	13, 14	HW	8/25/2009	COMPAL	Base on EMI request to pop the caps at DDR DIMM for verify.	pop C1121~1124, C1145~C1148	X01
60	42	HW	8/25/2009	COMPAL	Double discharge path on +3.3V_M, +3.3V_RUN and +1.5V_CPU_VDDQ	de-pop R607, R612 and R1498	X01
61	30	HW	8/26/2009	Intel	Follow Intel WW35 '09	Change R1526 to C427 10pF and change C475 to 33pF	X01
62	40	HW	10/06/2009	COMPAL	Board ID	Change R98 to 33K	X02
63	29	HW	10/06/2009	IDT	Follow IDT request to add a filter circuit	Change R340, R342, R1041, R1042 to 2K, add C1895~1898 (1000p), depop C1066, C1067	X02
64	17	HW	10/06/2009	COMPAL	add level shift for CRT DDC signal	add Q212, @1543, @1544	X02
65	32	HW	10/06/2009	COMPAL	Follow Intel DG FLEX clock topology.	change R910 to 22ohm.	X02
66	17	HW	10/06/2009	COMPAL	Follow Schematic check llist rev2.0	change R268 from 1Kohm to 10Kohm, depop C105, C106	X02
67	36	HW	10/06/2009	COMPAL	Correct the PU power rail for USB_MCARD2_DET#	change R447 PU from +3.3V_RUN to +3.3V_ALW +3.3V_ALW_PCH	X02
68	36	HW	10/06/2009	COMPAL	layout request to reduce stub.	add R1545, R1546.	X02
69	16	HW	10/21/2009	COMPAL	Follow X'tal EA. BIT number:DF346635	change C1168 C1187 from 18pF to 12pF.	X02
70	31	HW	10/27/2009	COMPAL	Follow Broadcom RFID final value.BIT number:DF341072	change L71/L72 from 150nH to 68nH, C1070/C1071 from 750pF to 1500pF, C1887/C1888 to 150pF	X02
71	16	HW	10/29/2009	COMPAL	Follow new SMBUS topology to solve AMT Memory issue.	add R1547, R1548	X02
72	41	HW	11/04/2009	COMPAL	Follow new TP spec	change PU for R613 and R614 from +5V_ALW to +3.3V_ALW	X02
73	24	HW	11/04/2009	COMPAL	Solve DF344566 EMI test fail at 200MHz from PCH PCI noise	change R166 to L92 (220ohm 0603 size bead)	X02
74	31	HW	11/04/2009	Broadcom	U34 has been validated to support both Atmel/Numonyx dataflash devices to meet Dell two sources requirement.	remove U14.	X02
75	31	HW	11/05/2009	COMPAL	W25X32VSSIG EOL	change U13 from W25X32VSSIG to W25Q32BVSSIG	X02
76	36	HW	11/05/2009	COMPAL	support WiMAX LED.	pop R840	X02
77	8, 28	HW	11/05/2009	COMPAL	reduce SMBUS stub.	add R1549~R1552 as no pop.	X02
78	40	HW	11/11/2009	COMPAL	solve RTC timing issue and follow the newest EA result.	change C675 from 33pf to 39pf and Y1/4 from 1TJS125DJ4A420P to Q13MC30610018 (10ppm)	X02
79	24	HW	11/11/2009	COMPAL	follloe LCD timing EA result.	change R161 from 470ohm to 100ohm.	X02
80	24	HW	11/11/2009	COMPAL	ME_FWP and SIO_EXT_WAKE# are OD pin.	add R1557 2.2Kohm PU to +3.3V_ALW_PCH , R1558 10K PU to +3.3V_RUN	X02

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
81	21	ESD	11/17/2009	COMPAL	Solve TP ESD issue. DF349471	add R1564, R1565 (100ohm) to replace L41 and L42	X02
82	19	HW	11/17/2009	Intel	Follow check list rev2.0 to add the PU for GPIO22, GPIO34	change the R1520, R1521 from PD to PU +3.3V_RUN	X02
83	31	HW	11/17/2009	COMPAL	use the same solution on Smart card clock.	change R772 from 47ohm to 22ohm.	X02
84	31	HW	11/18/2009	COMPAL	check list rev2.0 requirment	change R224 tolerance from 5% to 1%.	X02
85	40	HW	12/22/2009	COMPAL	Change board ID for X'build	change R98 from 33k ohm to 1k ohm.	A00
86	37	HW	12/22/2009	COMPAL	For DFB concern, change JBIO1 footprint	change JBIO1 footprint from TYCO_1734242-6_6P-T to TYCO_2041070-6_6P.	A00
87	38	EMI	12/22/2009	COMPAL	Solve Simplo battery slice EMI issue	Add C1900 and reserved C1899	A00
88	36	HW	12/22/2009	COMPAL	Solve Wi-max LED abnormal operation	De-pop R1409	A00
89	31	HW	12/22/2009	COMPAL	SC_CLK damping resistor keep PT value	change R772 from 22ohm to 47ohm.	A00
90	12	HW	12/23/2009	COMPAL	Surge voltage on UMA GFX core	change R358 from 4.7k ohm to 470 ohm.	A00
91	31	HW	12/23/2009	BRCOM	By BRCOM recommand	Change L71,L72 from 68nH to 150nH, C1070,C1071 from 1500pF to 390pF,C1887, C1888 from 150pF to 390pF.	A00
92	32	HW	12/23/2009	COMPAL	Change TCM to T1 version	Change TCM from SSX44B-D-T to SSX44-D-T1	A00
93	8, 15	HW	1/5/2010	COMPAL	cost saving for XDP,JTAG	De-pop R780~R785, R22, R24, R1241, R3, R6, R7, R19, R68, R1153, R1156, R1157, R66, C19, C20, R123, R804, R805, R806, R807, R1281, R1282, R1315	A00
94	33, 34	HW	1/5/2010	RICOH	CardBus change from ES2 to ES3	Change U94 from SA00003C21L to SA00003C22L	A00
95	39	HW	1/7/2010	COMPAL	RF team request to add 0.1uF capacitor on +5V_RUN of JTS1 to reduce 1811.5MHz noise	Add C114 on +5V_RUN of JTS1 for ATG configuration	A00
96	28, 37	HW	1/15/2010	COMPAL	Change SATA repeater material to power saving part	Change U95 and U96 part number to SA00003P10L	A00
97	26	HW	1/19/2010	Pericom	Pericom DP SW DP8200 has new silicon W version in stead of Y version	Change U9 to SA00003CD2L	A00
98	11	Acoustic	1/19/2010	COMPAL	To reduce acoustic noise	De-pop C53 and C54	A00

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1	50	Selector	7/20	TI	CSS GC logic wrong issue	Add PR282 180_ohm to GND	X01
2	46	1.5V_MEM	7/20	Compal ADC Guangyong	Add droop resistor for TI solution	Add PR77	X01
3	45	+3.3V/+5V	8/17	Compal ADC Guangyong	Change 3V/5V choke for cost down	change PL5 from SH00000H90L to SH00000FN0L change PL6 from SH00000HB0L to SH00000HR0L	X01
4	50	Selector	8/17	Compal	Add 1M_ohm pull down to fix ACAV_IN_NB oscillation when battery mode S5	Add PR283	X01
5	50	Selector	8/17	TI	new version CD3301 (PG2.1) don't need PD22 and PR282	depop PD22 add PR282, pop PR430	X01
6	50	Selector	8/17	TI	DOCK_AC_OFF_EC floating issue	add PR285	X01
7	49, 52	+VCORE +VGFX_CORE	8/17	Compal	change thermistor package from 0603 to 0402 for cost down	Change PH3,PH4,PH5 and PH802 from SL200000B0L to SL200000W0L	X01
8	47	1.8V_RUN	8/18	MAXIM	Output ripple voltage unstable issue	Change PC314 from SE00000868L(22u/0805) to SE00000000L(100u/1206) Change PR409 from SD03480618L (8.06k) to SD03460418L (6.04k) Change PR410 from SD03440218L(4.02k) to SD03430118L(3.01k) Change PR408 from SD014402A8L(40.2 Ohm) to SD000008H8L(51 Ohm) Change PC315 from SE000003W8L(820pF) to SE076333K8L (3300pF) Change PR411 from SD00000268L(6.98K) to SD03445318L(4.53K) Change PC310 from SE074102K8L(1000P) to SE074472K8L(4700pF) Change PC309 from SE071330J8L (33pF) to SE071560J8L (56pF) Change PC311 from SE042104K8L(.1u/0603/25V) to SE076104K8L(.1u/0402/16V) Add PR413 SD02800008L (0 Ohm)	X01
9	52	Vcc_gfx_core	8/19	Compal	Low side Vds ring over SPEC	Change PQ802 and PQ803 from SB00000KP0L(BSC882N03MS) to SB00000KM0L(FDMS7660)	X01
10	52	Vcc_gfx_core	8/20	Compal	Fine tune Imon time constant meet Intel SPEC 300uS~500uS	Change PC801 from SE068103K8L(0.01uF) to SE076153K8L(0.015uF)	X01
11	52	Vcc_gfx_core	8/20	Maxim	Fine tune transient RC time constant	Add PC816 SE076333K8L (0.033uF)	X01
12	49	+VCORE MAX17030	8/20	Maxim	Vcore FDIM issue	Change PR102, PR103 and PR104 from SD013220B8L(2.2) to SD00000V98L (1.1) Change PR310, PR311 and PR312 from SD03430118L(3.01k) to SD03424918L(2.49k) Change PR307, PR308 and PR309 from SD03422118L(2.21k) to SD03417418L(1.74k) Change PR137 from SD03449910L(4.99k) to SD03447518L(4.75k) Add PC271,PC272 and PC273 SE075223K8L(0.022uF)	X01
13	48	+1.05VM/ +1.05VTT	8/20	ON	Fine tune DC accurcay	Change PR188 and PR201 from SD03451018L(5.1k) to SD00000U28L(4.3k) Change PR199 and PR203 from SD03416228L(16.2k) to SD03413728L(13.7k) Change PR198 from SD03468008L(680 Ohm) to SD03418008L(180 Ohm) Change PR202 from SD03468008L(680 Ohm) to SD03410008L(100 Ohm) Change PC108 and PC116 from SE074331K8L(330p) to SE074471K8L(470p) Change PR200 from SD00000DM0L(200k) to SD03451028L(51k) Change PC115 from SE071300J0L(SE071300J0L) to SE071220J8L(22P) Change PC106 from SE071300J0L(30P) to SE071330J8L(33P) Change PR204 from SD03447518L(4.75K) to SD03452318L(5.23K) Change PR205 from SD03444228L(44.2K) to SD03424028L(24K) Change PR207 from SD00000LZ0L(3.83K) to SD00000J20L(4.32K) Change PR208 from SD03482518L(8.25k) to SD03464918L(6.49k)	X01

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14	47	1.8V_RUN	8/25	DELL	1.8V transient 0.1A ~ 1.6A output voltage over spec	Change PU301 from SA00003B10L(MAX15050) to SA00003CG0L (ISL8014) and support circuit	X01
15	49	Vcore	8/25	MAXIM	Improve DC accuracy	Change exposed pad to PGND from AGND	X01
16	49	Vcore	8/25	MAXIM	Vender recommend PSI# pull down 10k	Change PR334 from SD03410018L (1k) to SD02810028L(10k)	X01
17	51	Charger	8/25	Compal ADC Guangyong	Improve charger choke saturation current at 100 degree C	Change PL14 from SH04856AM8L (5.6u) to SH00000I60L (5.6u)	X01
18	44	DCIN	8/25	Compal	3.3V_ALW2 black driver issue with RTC battery only	Change PD1 from SC100000Q0L(BAT54CW) to SCSB715F08L (RB715F)	X01
19	49	Vcore	8/27	Compal	Reserve resistor pad for debug	Add PR122 and PR123	X01
20	49	Vcore	9/01	MAXIM	Fine tune Imon time constant meet Intel SPEC 300uS~500uS	Change PC270 from SE075223K8L (0.022U) to SE076333K8L (.033U)	X01
21	49	Vcore	9/01	MAXIM	Make sure DPRSLPVE low level under 0.33V	Change PR109 from SD03449908L (499 Ohm) to SD02800008L (0 Ohm)	X01
22	44	DC_IN	10/13	TI	High inrush current on DC_IN when AC adapter plug in	Change PR20 from SD02800008L(0 Ohm) to SD02810028L(10k)	X02
23	49	Vcore	10/20	MAXIM	3 phase overlap issue with 2nd source MOSFET	Add PC198, PC199, PC255, PC256, PC259 and PC260 SE074122K8L (1200pF)	X02
24	48	+1.05VTT	10/28	INTEL	Fine tune H_VTTPWRGD voltage level meet Vih(min) = 0.75 * Vtt	Change PR94 from SD03410028L (10k) to SD03427418L (2.74K) Change PR93 from SD03428728L (28.7k) to SD03493118L (9.31K)	X02
25	49, 52	+V CORE +VGFX_CORE	11/03	Compal	change thermistor package from 0603 to 0402 for cost down	Change PH1 and PH801 from SL20000068L (100K 0603) to SL20000160L (100K 0402)	X02
26	48	+1.05VTT/ +1.05VM	11/16	ON	Bost diode over stress	Change PD19 and PD27 from SC1B751V08L(RB751V) to SCS00003M0L(BAT54HT1G)	X02
27	52	+VGFX_CORE	11/24	MAXIM	Fine tune transient and load line for 2nd and 3rd source choke.	Change PR828 from SD03424918L (2.49k 0402) to SD00000408L (2.2k 0402) Change PR827 from SD03430118L (3.01k 0402) to SD03424918L (2.49k 0402) Change PR816 from SD03411028L (11k 0402) to SD02810228L (10.2k 0402)	X02
28	52	+VGFX_CORE	11/24	MAXIM	Two 4.7k PD on GFX_VR_ON at both EE side and PWR side. Depop PWR side 4.7k PD.	Depop PR809 SD02847018L (4.7K 0402)	X02
29	51	Charger	01/12	Compal	Reduce Pin33,34 and 35 of the CD3301 surge current	Change PC351 from SE00000130L (1u/0805) to SE043104M8L (0.1u/0805) Change PR404 from SD02800008L (0 Ohm) to SD028100B8L (1 Ohm)	A00