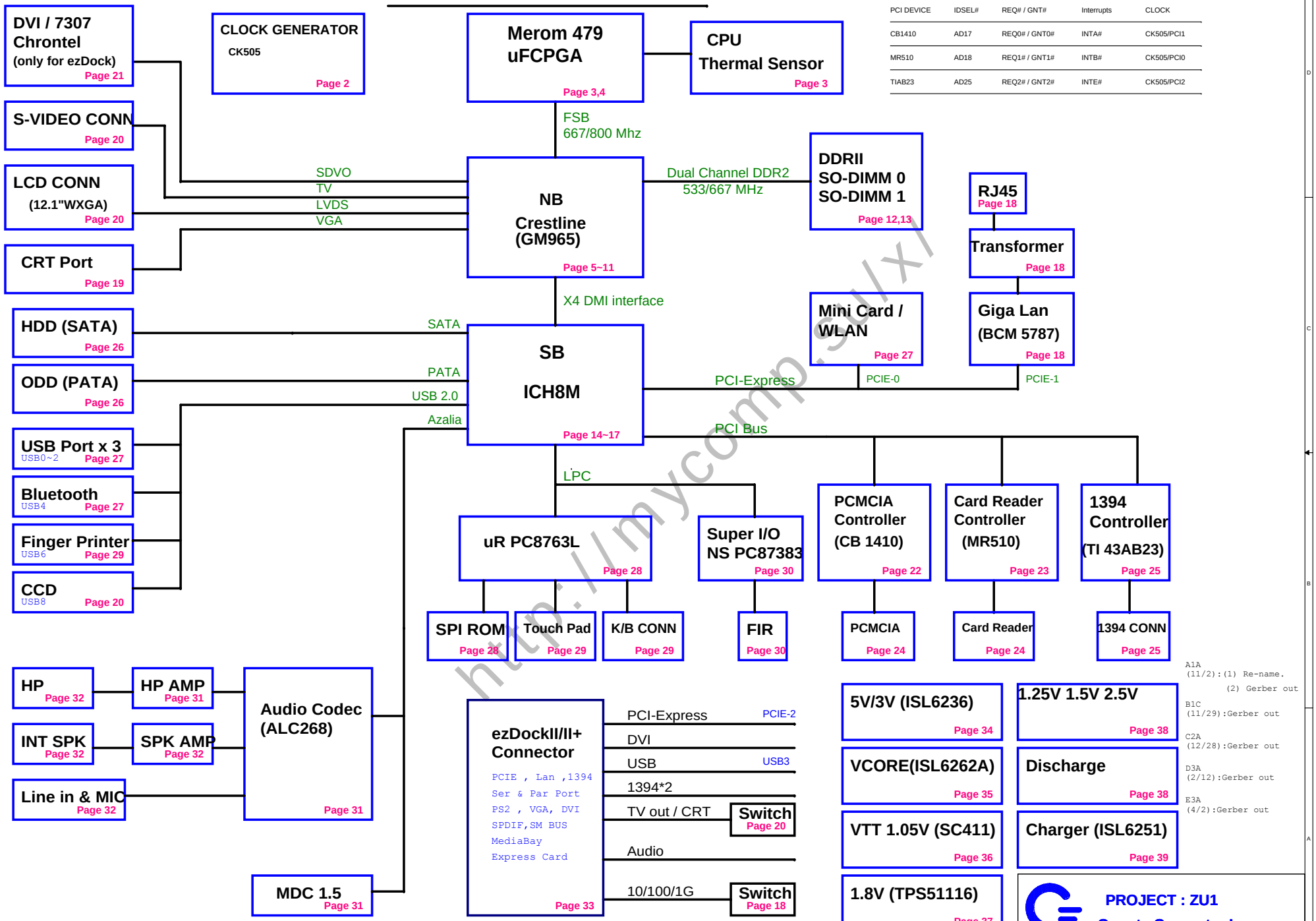
ZU1 SYSTEM BLOCK DIAGRAM



PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts	CLOCK
CB1410	AD17	REQ0# / GNT0#	INTA#	CK505/PCI1
MR510	AD18	REQ1# / GNT1#	INTB#	CK505/PCI0
TIAB23	AD25	REQ2# / GNT2#	INTE#	CK505/PCI2

A1A
(11/2):(1) Re-name.
(2) Gerber out

B1C
(11/29):Gerber out

C2A
(12/28):Gerber out

D3A
(2/12):Gerber out

E3A
(4/2):Gerber out

PROJECT : ZU1
Quanta Computer Inc.

Size	Document Number	Rev
	Block Diagram	3B
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Clock Generator

E3A:(3/16) Change C542 from 0805(CH6102K9A01) to 0603(CH6101M9905) base on ME request(HDD Mylar issue)

A1A:(9/24)
ICS FAE suggest to change
C542,C287 from 4.7uF to 10uF

A1A:(9/28)
Reverse RC0603 footprint for EMI

A1A:(9/20) remove SATACLKREQ function, change R188 value from 475ohm to 22 ohm

A1A:(9/24) FAE : (14M_ICH and SIO_14M) signals trace should be equal length

A1A:(9/24) ICS FAE suggest R change from 22 to 33 ohm
A1A:(9/20) change R186 value from 33ohm to 22 ohm(Intel check list 1.301)

C2A:(12/26) Base on vendor-FCE suggestion,
change C310/C299 from CH03306JBD7 (33p) to CH02706JB06(27p)

<check list>
XTAL length < 500mils

ICS9LPRS365BGLFT
SLG8SP512T: AL8SP512K05

ICS9LPRS365AGLFT/ SLG8SP512T

During initial power-up be used to
sample FSB speed with FSA/B/C

<check list>
(1)PCI2/TME: PU be used, the CK505 cannot over clock any of the clock for Trust Mode security purposes.

(2)PCI4/SRC5_EN: PU be used, the CK505 will be configured to use Pin37/38 to SRC5 clock.
If PD be detect at powe-on,the CK505 will setting Pin 37/38 to PCI_STOP/CUP_SOTP
(Default is setting to PCI_STOP/CUP_SOTP)

(3)PCIF5/ITP_EN: PU be used, the CK505 will be configured to use Pin46/47 to CPU ITP clock.
If PD be detect at powe-on,the CK505 will setting Pin 46/47 to SRC8
(Default is setting to SRC8)

(4)SLG8SP512 Pin 6 select Pin 17, 18 output is LCDCLK or 27 M, PD is LCDCLK, PU is 27 M ,
Pin 37, 38 will fixed be use CPU_Stop and PCI_Stop.

(5)SLG505YC64 CK505 Standar parts follow standar setting

Clock Gen I2C

Pin	Active	Control signal
32	Low	SRC9/9#
33	Low	SRC10/10#

A1A:(9/24) Base on above table, SWAP SRC3 and SRC9

A1A:(9/24) Add PCIE_CLKREQ# PU to +3V

C2A:(12/12)change from +1.05V to +1.25V.
Because VDD_IO will drop out when high loading

Clock Gen Differential IO power

0.1U close to each VDD_IO Power pin

CPU Clock select

A1A: (9/20) Remove 0ohm

C2A: (12/10) no stuff R179,R198,R447 for auto CPU frequence selection (follow ZD1,ZO1)

BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

PROJECT : ZU1
Quanta Computer Inc.

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	CLK. GEN./ CK505	3B
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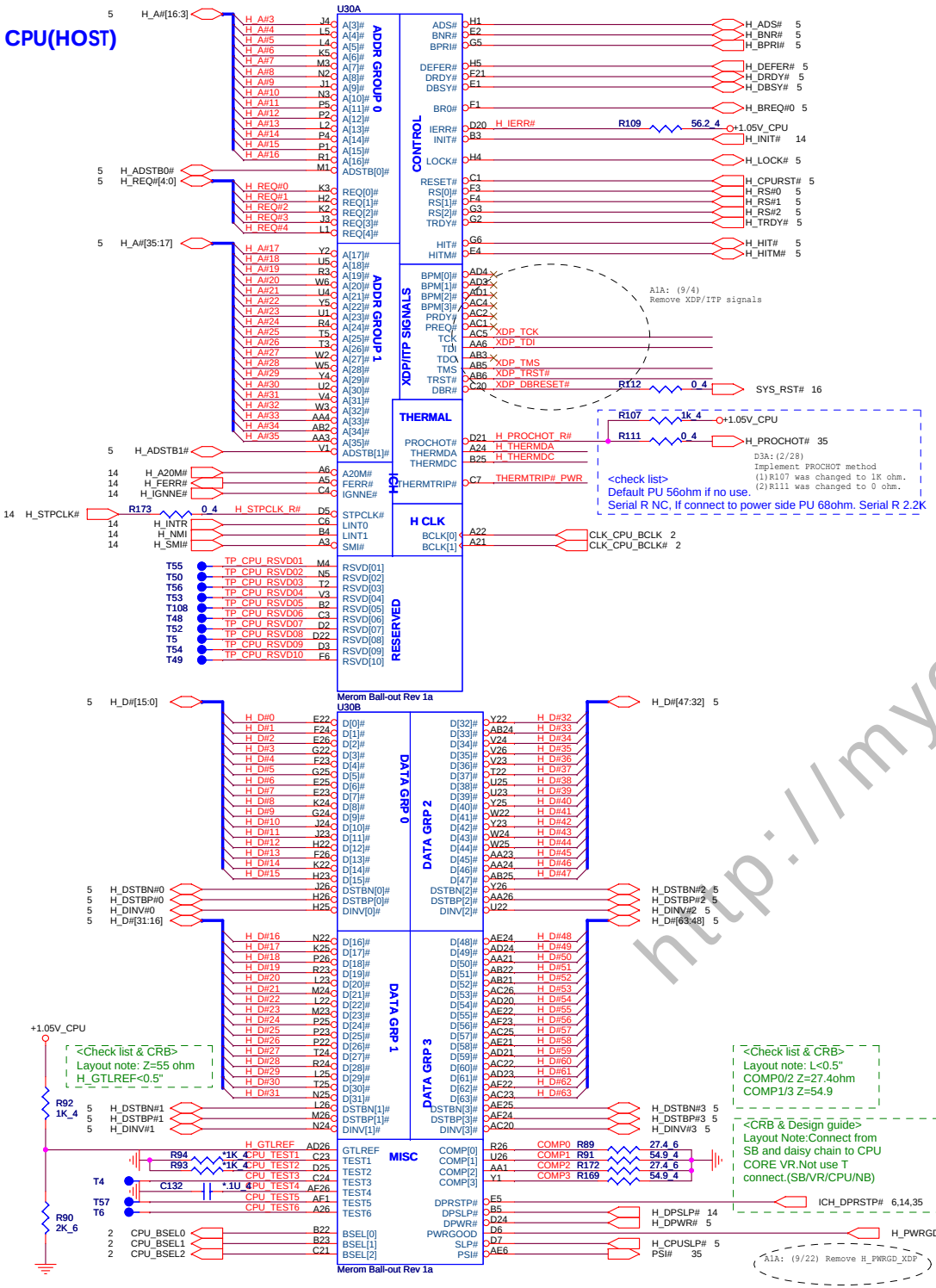
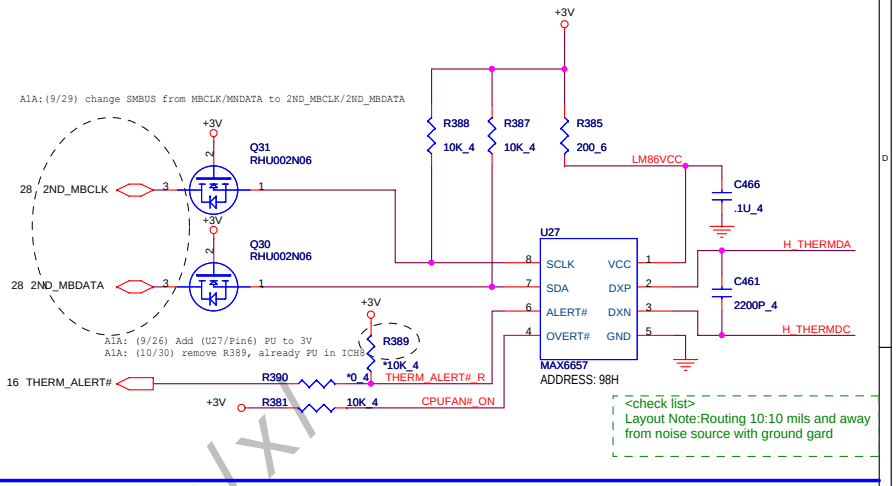
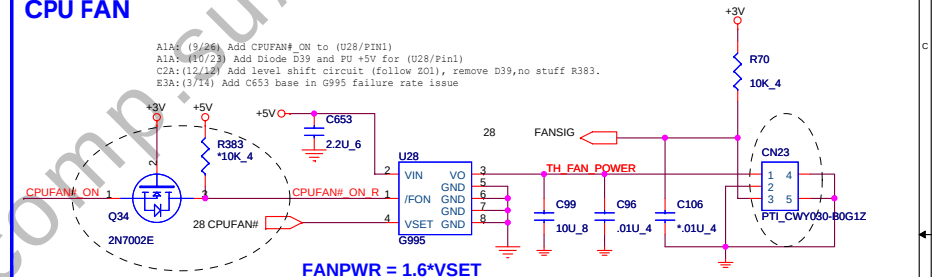
CPU(HOST)



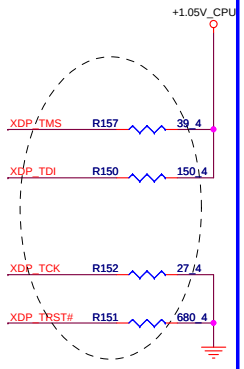
CPU Thermal monitor



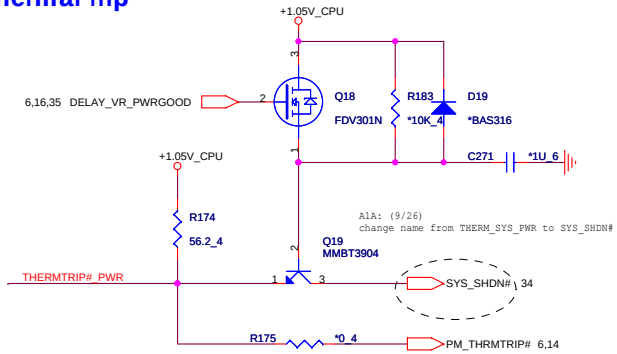
CPU FAN



PU/PD (ITP700)



Thermal Trip



PROJECT : ZU1

Quanta Computer Inc.

Size	Document Number	Rev
	CPU(1 of 2)/FAN/Thermal	3B
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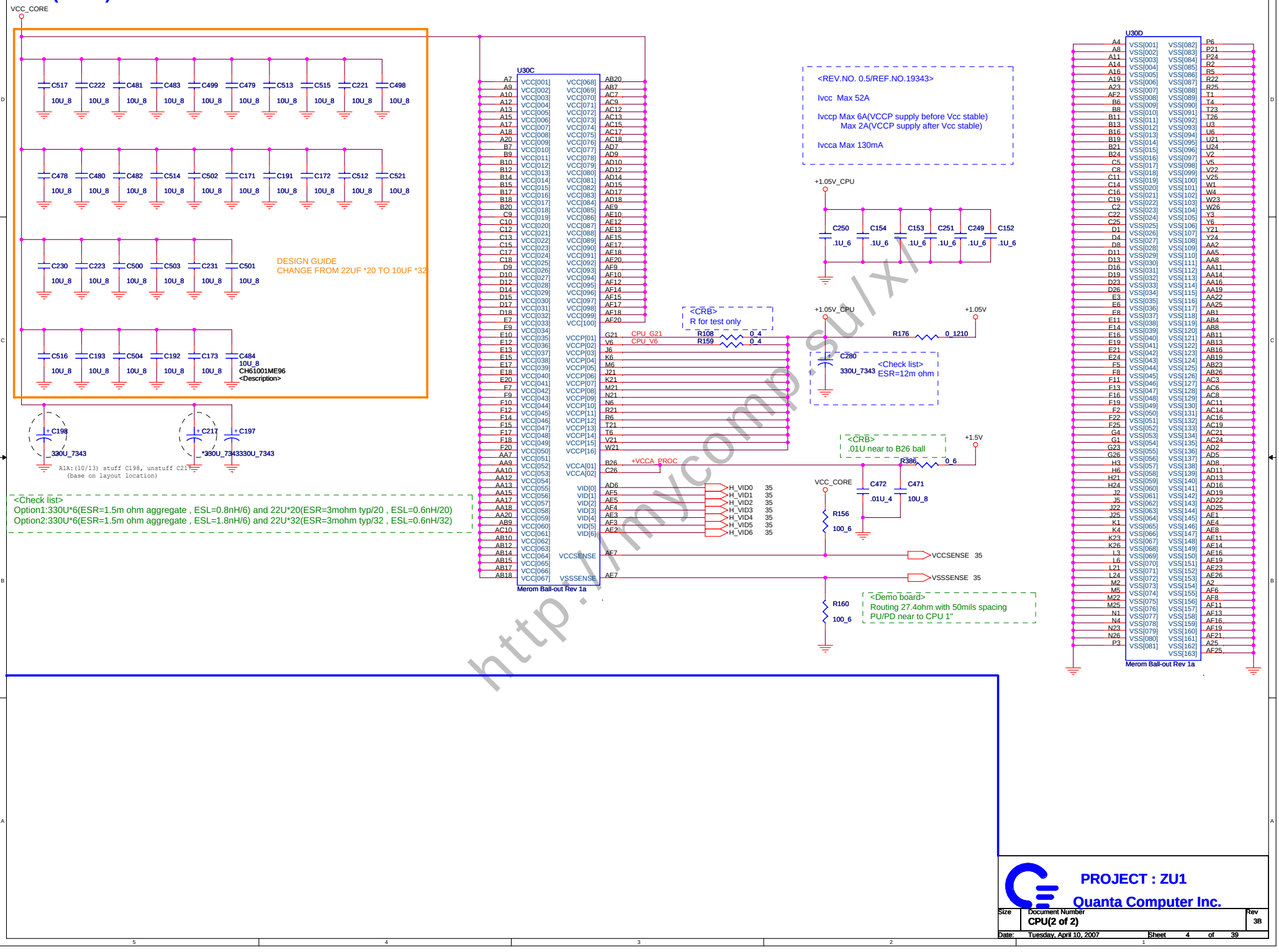
CPU(Power)



PROJECT : ZU1		
Quanta Computer Inc.		
Size	Document Number: CPU(2 of 2)	Rev: 3B
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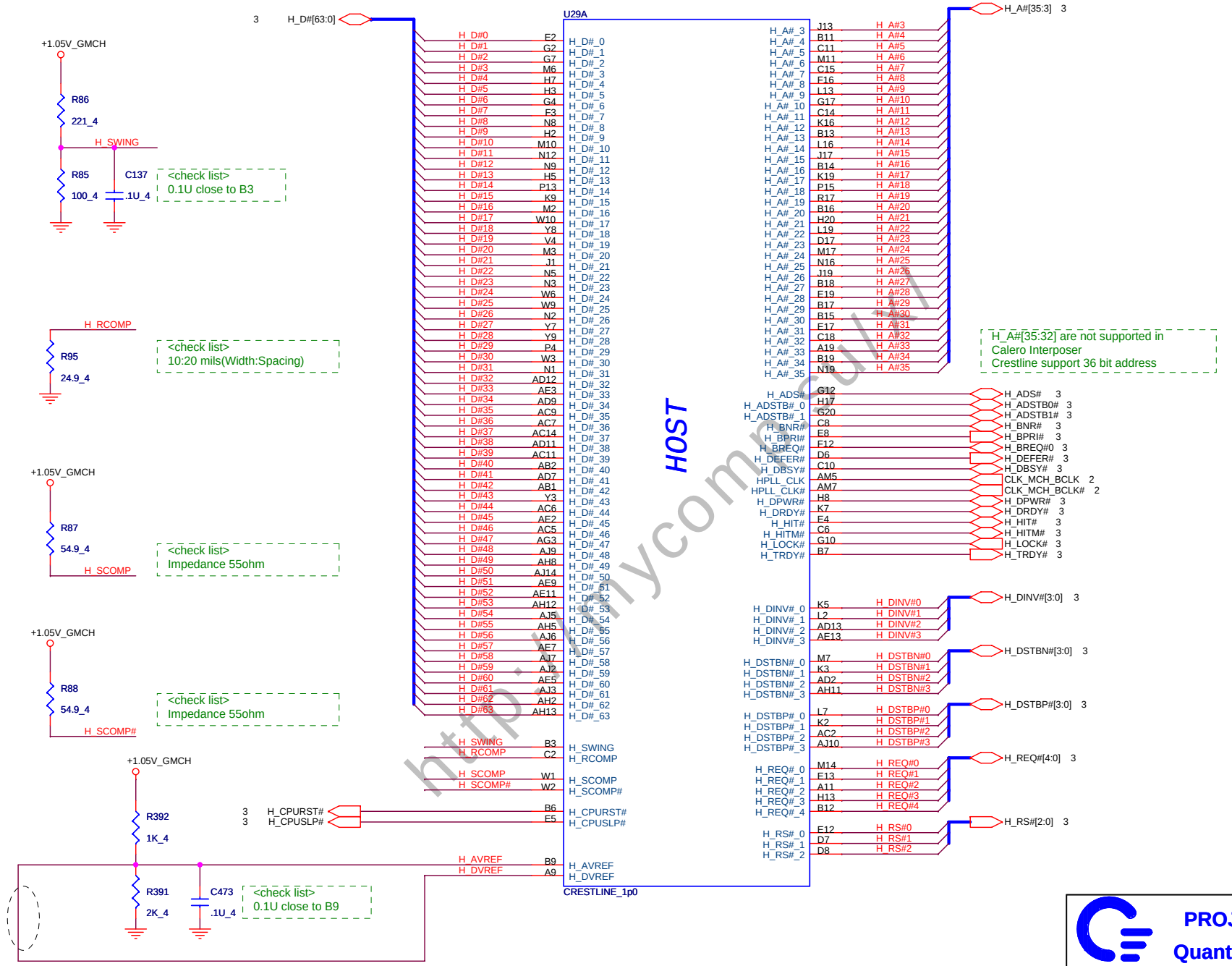
NB(HOST)

D3A:(2/1) Change 965GM from ES sample to QS sample
Change U29 P/N from AJ0QN120T37 to AJ0QP200T09



A1A:(9/20) remove R74 (0 ohm)

PROJECT : ZU1

Quanta Computer Inc.

Size	Document Number	Rev
	GMCH HOST(1 of 7)	3B
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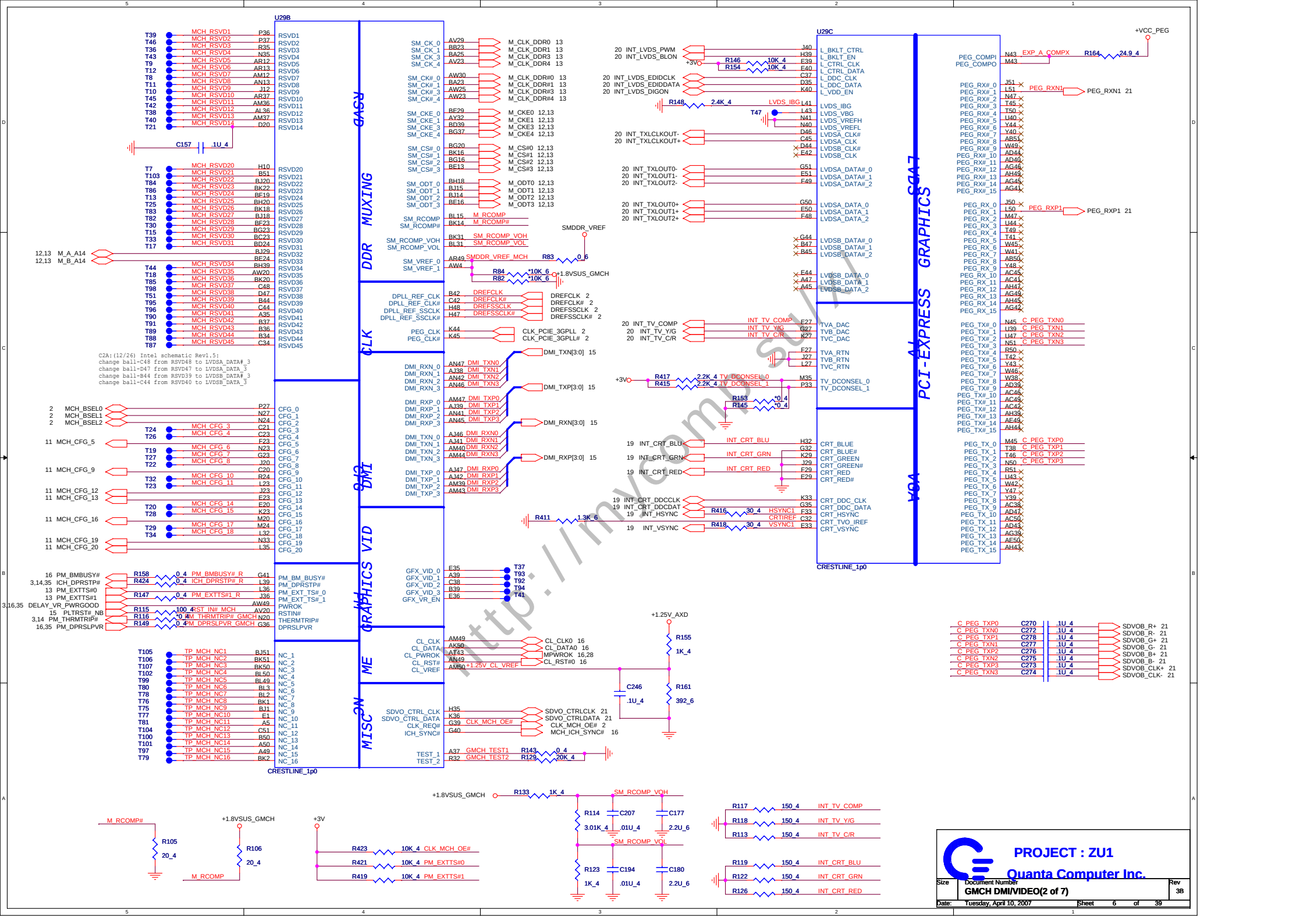
U29B
U29C
CRESTLINE_1p0
CRESTLINE_1p0
DDR MUXING
CLK
DMI
GRAPHICS VID
ME
MISC
GMCH
PCI-EXPRESS GRAPHICS
SDVO
+VCC_PEG
+1.25V_AXD
+1.8VSUS_GMCH
+3V
SMDDR_VREF
C2A:(12/26) Intel schematic Rev1.5:
change ball-C48 from RSVD48 to LVDSA_DATA#_3
change ball-D47 from RSVD47 to LVDSA_DATA_3
change ball-B44 from RSVD39 to LVDSB_DATA#_3
change ball-C44 from RSVD40 to LVDSB_DATA_3
PROJECT : ZU1
Quanta Computer Inc.
GMCH DMI/VIDEO(2 of 7)
Size
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Rev
3B
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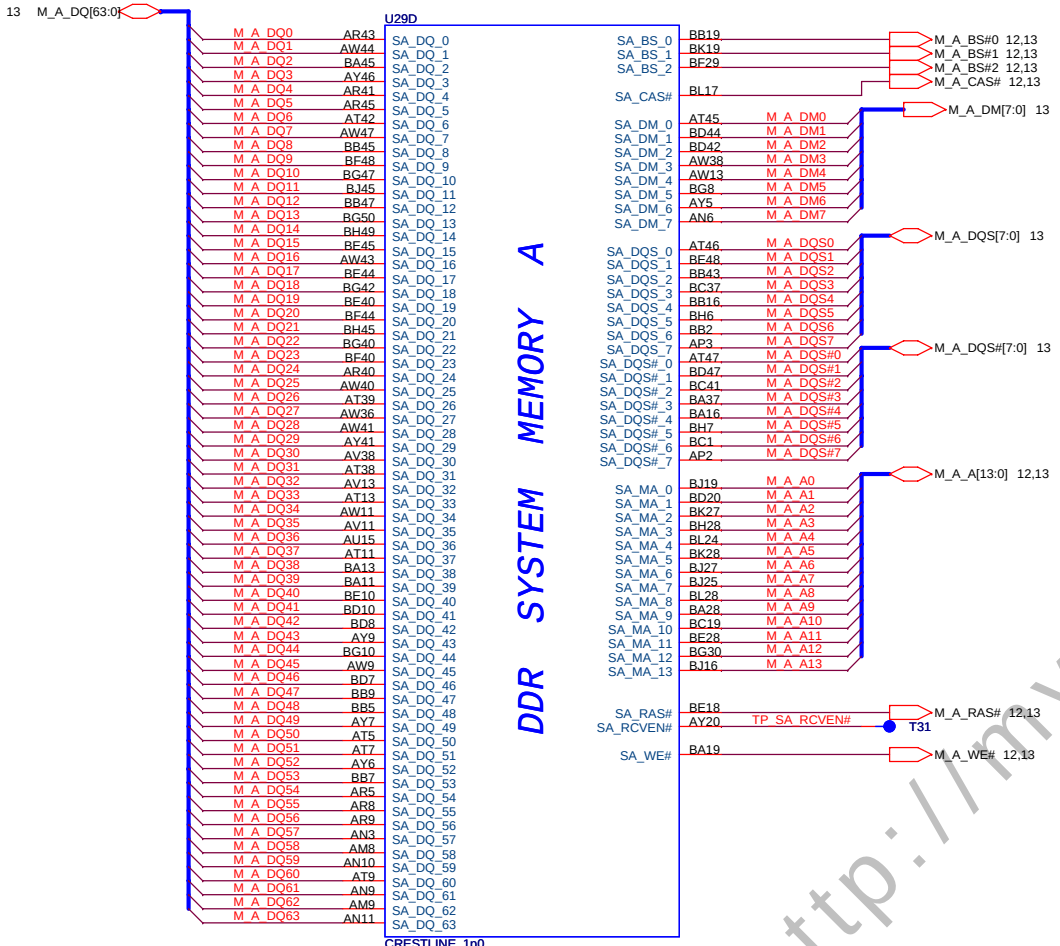
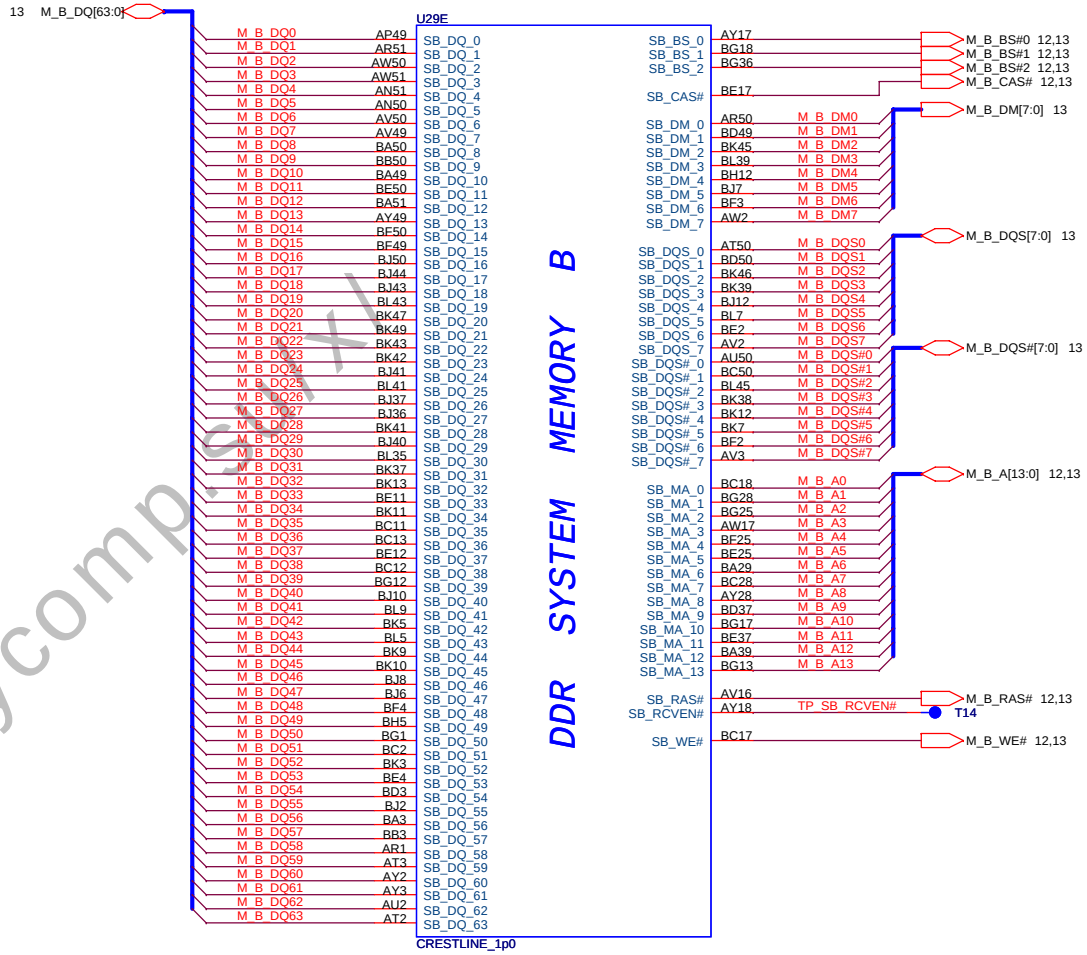
NB(Memory controller)





PROJECT : ZU1

Quanta Computer Inc.

Size	Document Number	Rev
	MCH DDR(3 of 7)	3B
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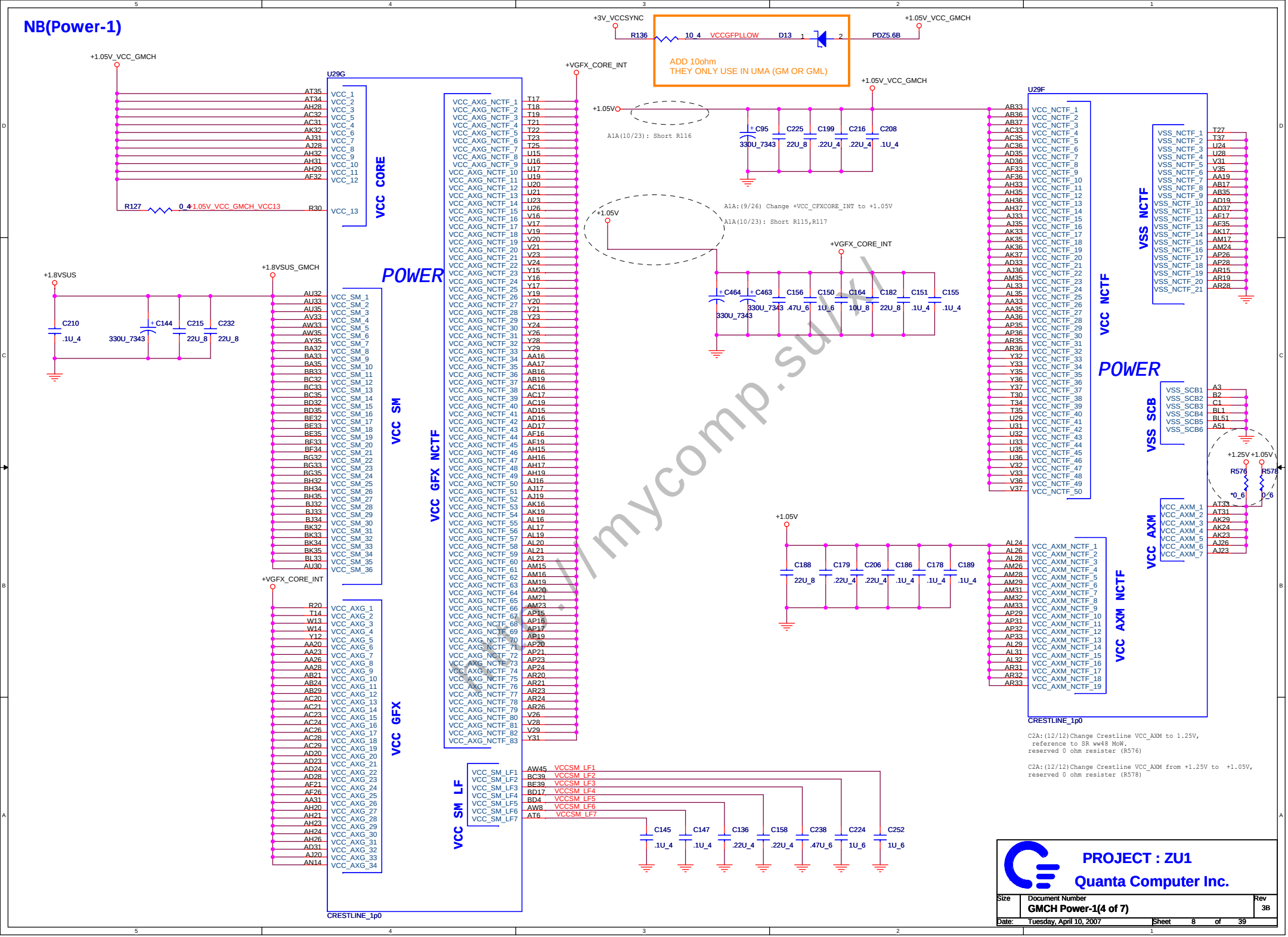
NB(Power-1)



NB(Power-2)

CRT/TV Disable/Enable guideline

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT	3.3V	GND	VCCA_C_TVO	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVO	1.5V	1.5V
VCCDQ_CRT	1.5V	GND	VCCABG_DAC	3.3V	GND
VCCA_A_TVO	3.3V	GND	VSSABG_DAC	GND	GND
VCCA_B_TVO	3.3V	GND	VCC_SYNC	3.3V	GND

LVDS Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If SDVO enable LVDS Disable	If SDVO enable LVDS enable
VCCD_LVDS	GND	1.8V	1.8V
VCCA_LVDS	GND	GND	1.8V
VCCTX_LVDS	GND	GND	1.8V
	EXTERNAL		INTERNAL

<Description>

<FAE>
INT VGA disable
VCCSYNC connect to GND

<Description>

B1D:(12/9) change C143 from CH71002MJC8 to CH7102MT804 (z-limit issue)

A1A:(10/18)
INTEL CRB VCCD_QDAC Filter Modification:
change L13 to R125(100ohm),
change R145(*0 ohm) to C507(1uF)

D3A:(01/02)
R125 shortage issue, Add 2nd source CS11003F953

D3A:(2/13)
Change R125 from CS11003B900 (100 ohm 0.1%) to CS11003J53(100 ohm 1%)

A1A: (9/20) Remove R138 0 ohm

A1A: (9/20) Remove +VCC_RXR_DMI

<FAE>
VCC_RXR_DMI and VCC_PEG
connect to+1.05V

<CRB>
+1.25V AND +1.25M shall be
+1.5V for Calero Interposer

A1A(10/23): Short R122

CRESTLINE_1p0

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Quanta Computer Inc.

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	GMCH Power-2(5 of 7)	3B
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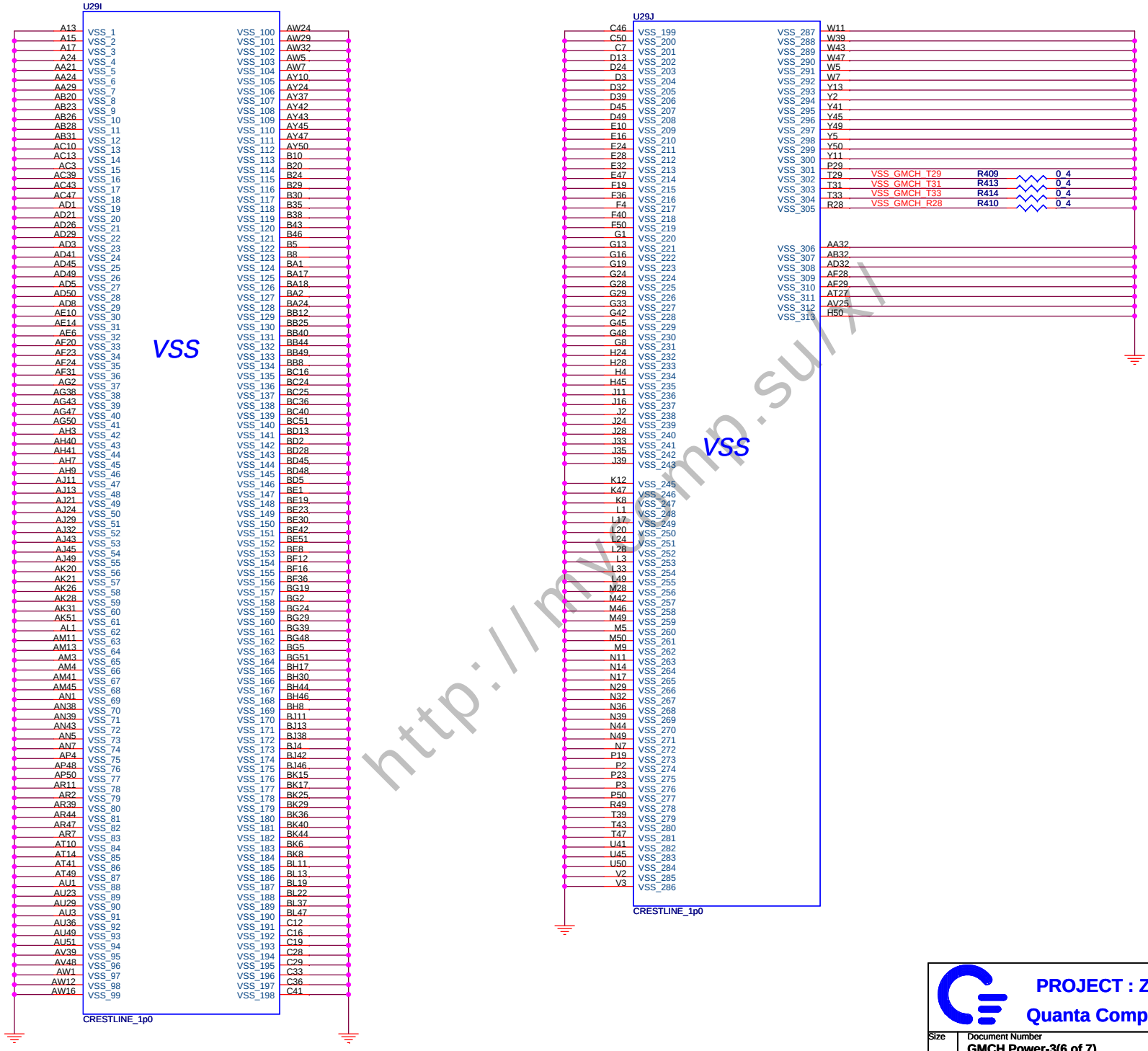
NB(Power-3)



PROJECT : ZU1

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	GMCH Power-3(6 of 7)	3B
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Strap table

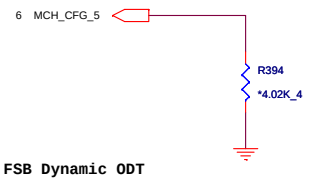
All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

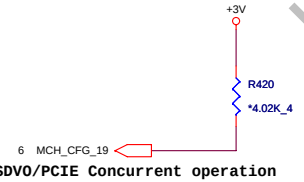
DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)



DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane

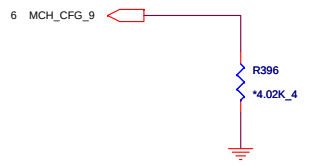


XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)

PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)

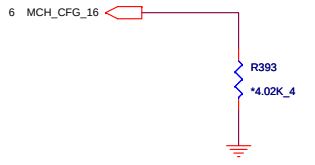


SDVO Present

Strap define at External DVI control page

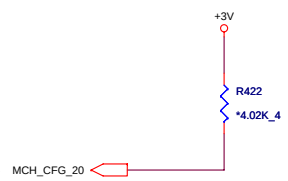
FSB Dynamic ODT

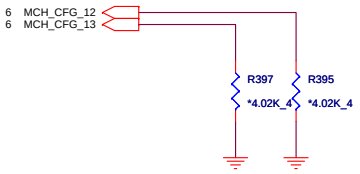
MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port





PROJECT : ZU1
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH Strap(7 of 7)	3B
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DDR2 Dual channel A/B PU

M_A_A[13..0] → M_A_A[13..0] 7,13

M_B_A[13..0] → M_B_A[13..0] 7,13

DDRII A CHANNEL

SMDDR_VTERM

C160 .1U_4, C219 .1U_4, C163 .1U_4, C254 .1U_4, C212 .1U_4, C247 .1U_4, C162 .1U_4, C184 .1U_4, C241 .1U_4, C229 .1U_4, C260 .1U_4, C245 .1U_4, C161 .1U_4

DDRII B CHANNEL

SMDDR_VTERM

C255 .1U_4, C190 .1U_4, C166 .1U_4, C183 .1U_4, C167 .1U_4, C237 .1U_4, C248 .1U_4, C256 .1U_4, C209 .1U_4, C169 .1U_4, C253 .1U_4, C258 .1U_4, C204 .1U_4

Place one cap close to every 2 pull-up resistor terminated to SMDDR_VTERM

M_A_A3	RP16	1 3	2 4	56X2 → SMDDR_VTERM
M_A_A1				
M_A_A7	RP21	1 3	2 4	56X2 → SMDDR_VTERM
M_A_A5				
M_A_A2	RP17	1 3	2 4	56X2 → SMDDR_VTERM
M_A_A4				
M_A_A11	RP26	1 3	2 4	56X2 → SMDDR_VTERM
6,13 M_CKE1				
M_A_A12	RP24	1 3	2 4	56X2 → SMDDR_VTERM
M_A_A9				
	RP27	1 3	2 4	56X2 → SMDDR_VTERM
7,13 M_A_BS#2				
6,13 M_CKE0				
M_A_A0	RP11	1 3	2 4	56X2 → SMDDR_VTERM
7,13 M_A_BS#1				

M_B_A10	RP10	1 3	2 4	56X2 → SMDDR_VTERM
7,13 M_B_BS#0				
M_B_A3	RP13	1 3	2 4	56X2 → SMDDR_VTERM
M_B_A1				
M_B_A0	RP9	1 3	2 4	56X2 → SMDDR_VTERM
7,13 M_B_BS#1				
M_B_A6	RP18	1 3	2 4	56X2 → SMDDR_VTERM
M_B_A11				
M_B_A12	RP19	1 3	2 4	56X2 → SMDDR_VTERM
M_B_A5				
M_B_A2	RP15	1 3	2 4	56X2 → SMDDR_VTERM
M_B_A4				
M_B_A8	RP22	1 3	2 4	56X2 → SMDDR_VTERM
M_B_A9				

M_A_A8	RP20	1 3	2 4	56X2 → SMDDR_VTERM
M_A_A6				
6,13 M_CKE3	RP28	1 3	2 4	56X2
7,13 M_B_BS#2				
7,13 M_A_BS#0	RP4	1 3	2 4	56X2
6,13 M_ODT1				
6,13 M_ODT3	RP1	1 3	2 4	56X2
6,13 M_CS#2				
M_A_A10	RP12	1 3	2 4	56X2
7,13 M_A_CAS#				
7,13 M_A_WE#	RP7	1 3	2 4	56X2
6,13 M_CS#1				
7,13 M_A_RAS#	RP8	1 3	2 4	56X2
6,13 M_CS#0				
7,13 M_B_WE#	RP5	1 3	2 4	56X2
7,13 M_B_CAS#				
M_B_A7	RP25	1 3	2 4	56X2
6,13 M_CKE4				
6,13 M_CS#3	RP6	1 3	2 4	56X2
7,13 M_B_RAS#				
6,13 M_ODT0	RP2	1 3	2 4	56X2
M_A_A13				
6,13 M_ODT2	RP3	1 3	2 4	56X2
M_B_A13				

INTEL FAE (08/17)
ADD MA14 FOR DUAL LAYERS RAM

6,13 M_A_A14 → R144 56_4 → SMDDR_VTERM
6,13 M_B_A14 → R135 56_4 → SMDDR_VTERM

PROJECT : ZU1
Quanta Computer Inc.

Size	Document Number	Rev
	DDR RES. ARRAY	3B
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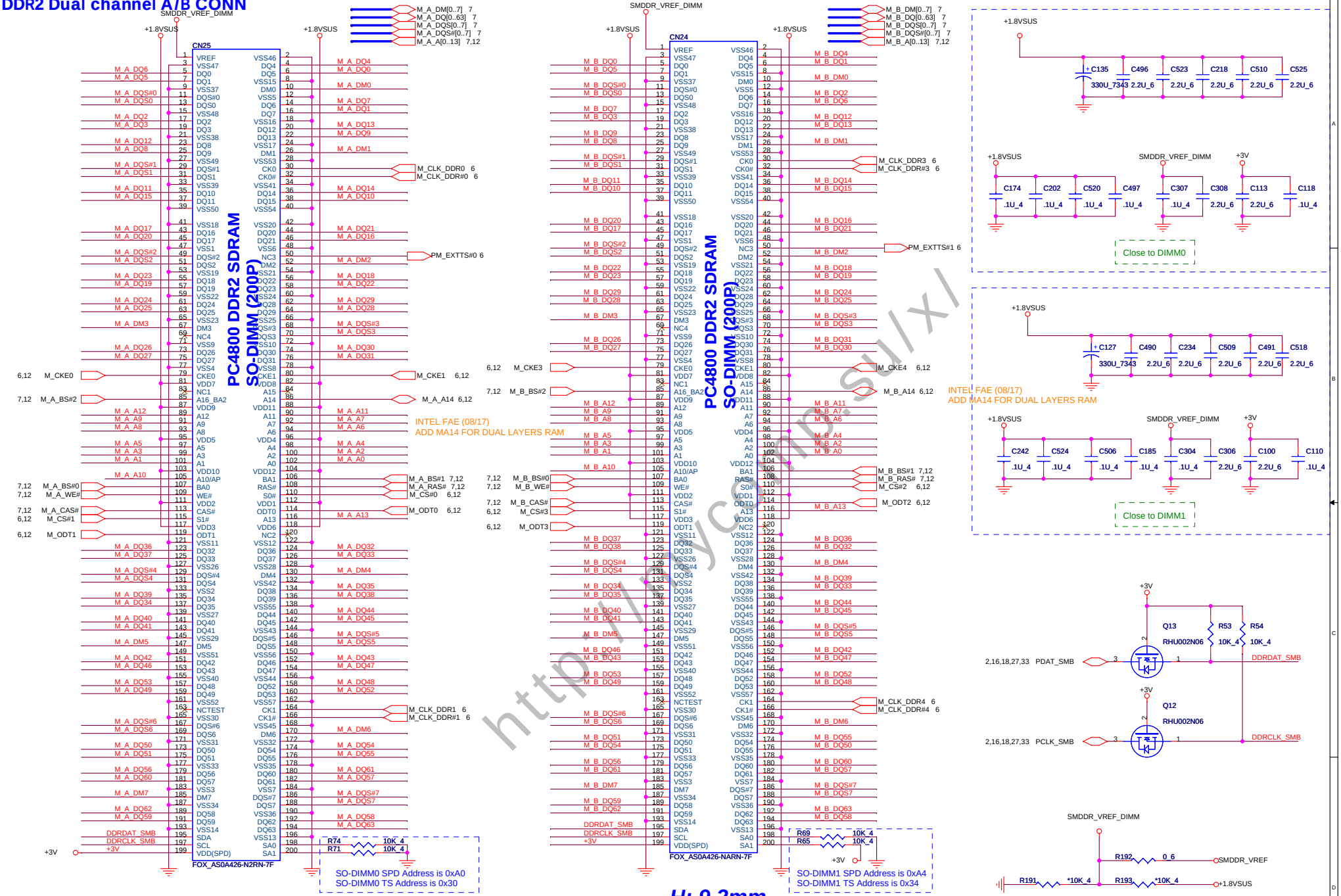
DDR2 Dual channel A/B CONN



H: 5.2mm

CLOCK 0,1
CKE 0,1

H: 9.2mm

CLOCK 3,4
CKE 2,3

A1A:(10/30) no stuff R192, stuff R191,R193
A1A:(11/09) stuff R192, no stuff R191,R193

PROJECT : ZU1		
Quanta Computer Inc.		
Size	Document Number: DDR SO-DIMM(200P)	Rev: 3B
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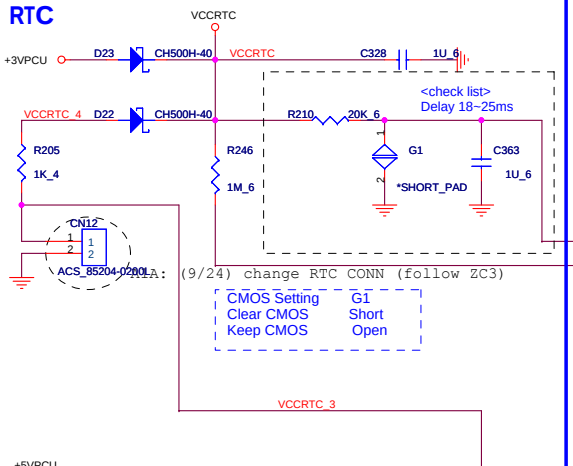
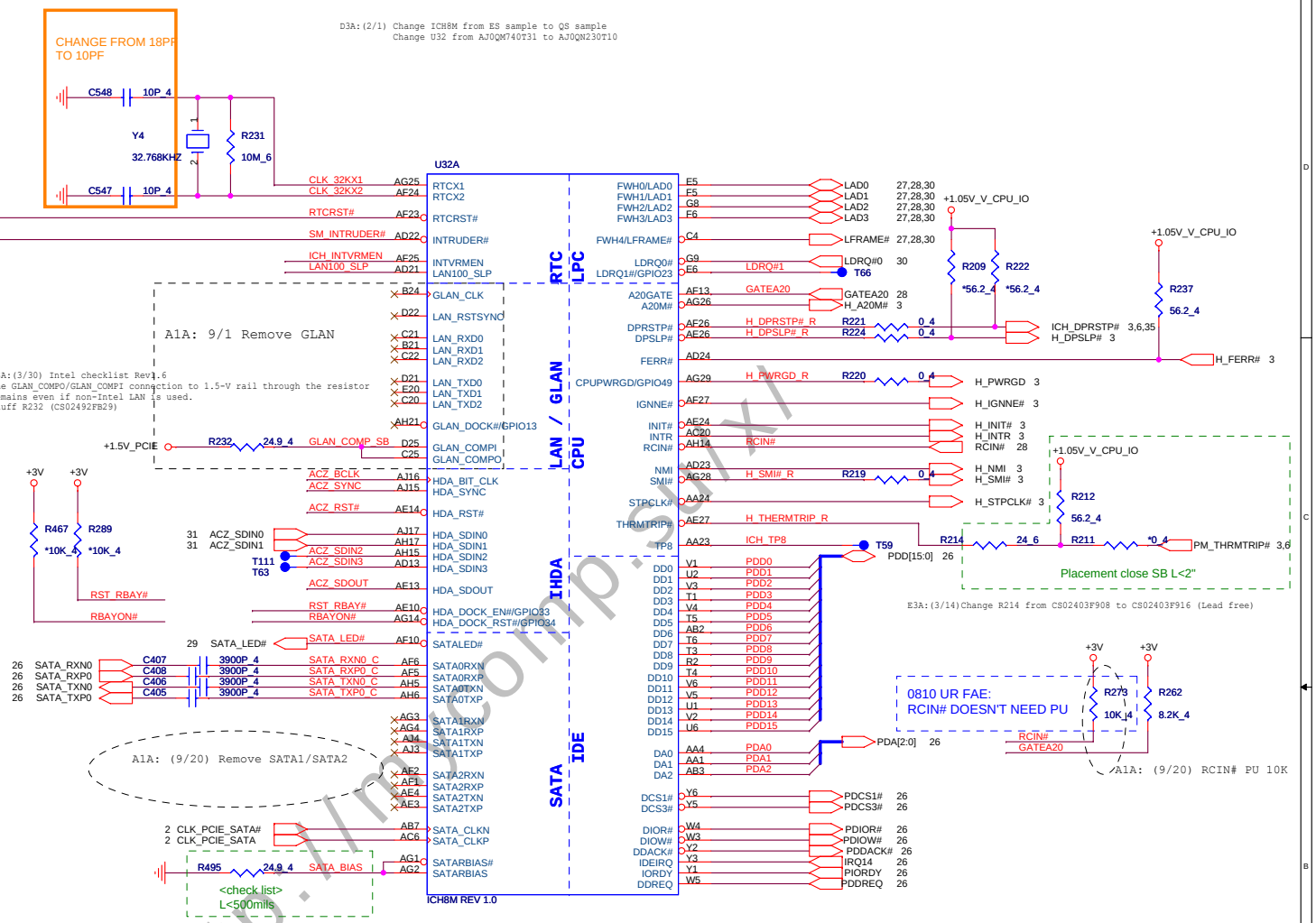
RTC



SATA Disable

1.Connect to GND: SATA[2:0]RXp/n , SATARBIAS , SATARBIAS# , SATA_CLKP , SATACLKN
2.NC: SATA[2:0]TXp/n , SATALED#
3.VccSATAPLL should be connected directly to Vcc1_5,Filter cap are not required
4.BIOS disable



SB Strap

ICH8-M Internal VR Enable strap
(Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

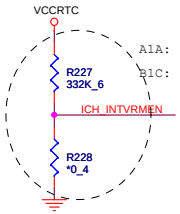
INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH8-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1.05)

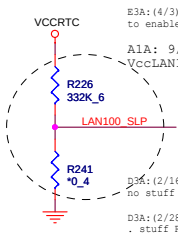
LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1



A1A: (9/20) Change INTVRMEN from PU to PD
B1C: (11/18) Change INTVRMEN from PD to PU

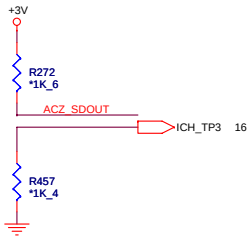


E3A:(4/3)Stuff R226(332K_6) and don't stuff R241
to enable Internal VR for VCCCL1_05 and VCCLAN1_05.

A1A: 9/1 Disable the internal VR powering
VccLAN1_05, and VccCL1_05

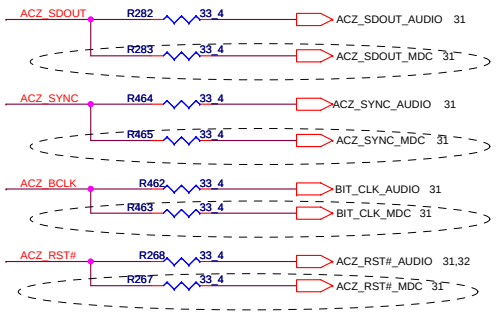
D3A:(2/16)ICH8M Internal VR should not be disabled.
no stuff R241, stuff R226

D3A:(2/28) Battery life issue. Disable ICH8M Internal VR (LAN)
. stuff R241, no stuff R226 for C-build



HDA

A1A: 9/6 base on Intel design guide, add it.



PROJECT : ZU1
Quanta Computer Inc.

Size	Document Number	Rev
	ICH8M HOST(1 of 4)	3B
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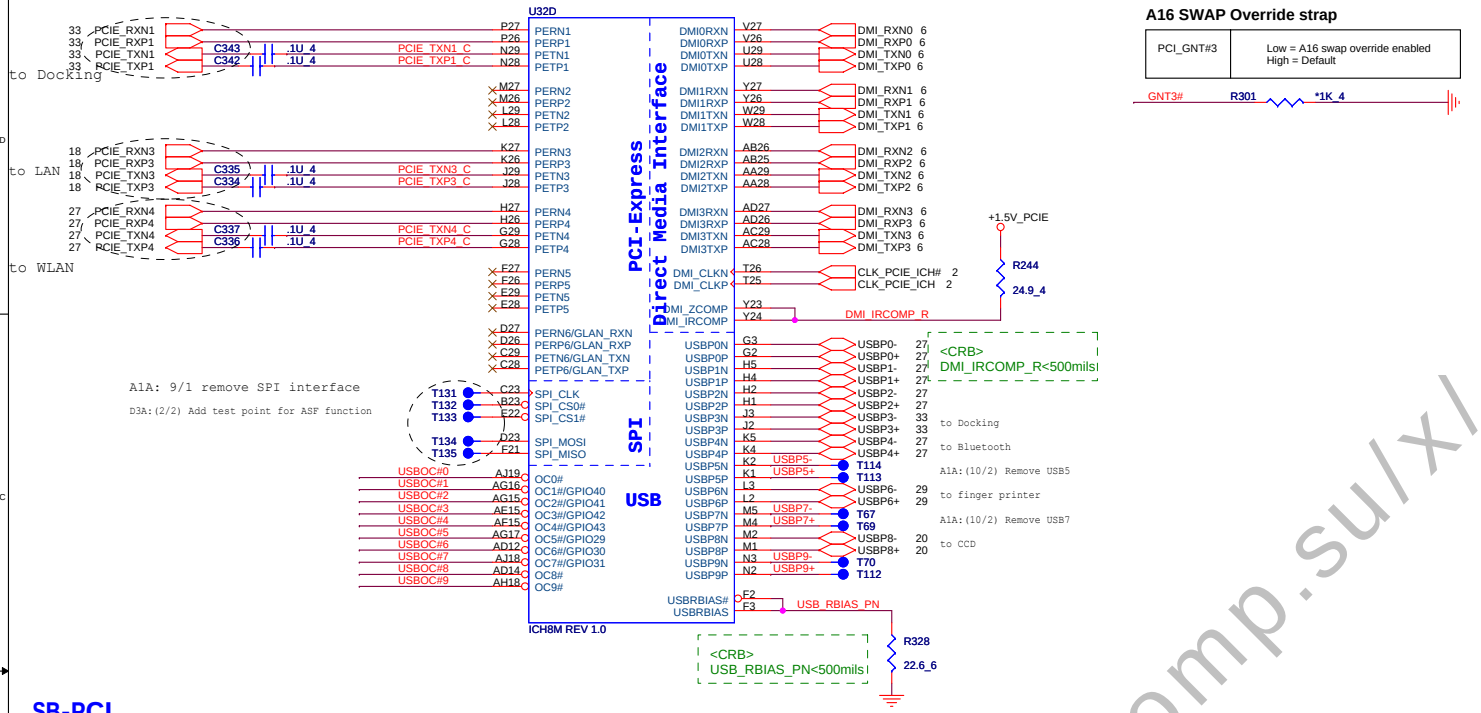
SB-PCIE/USB/DMI

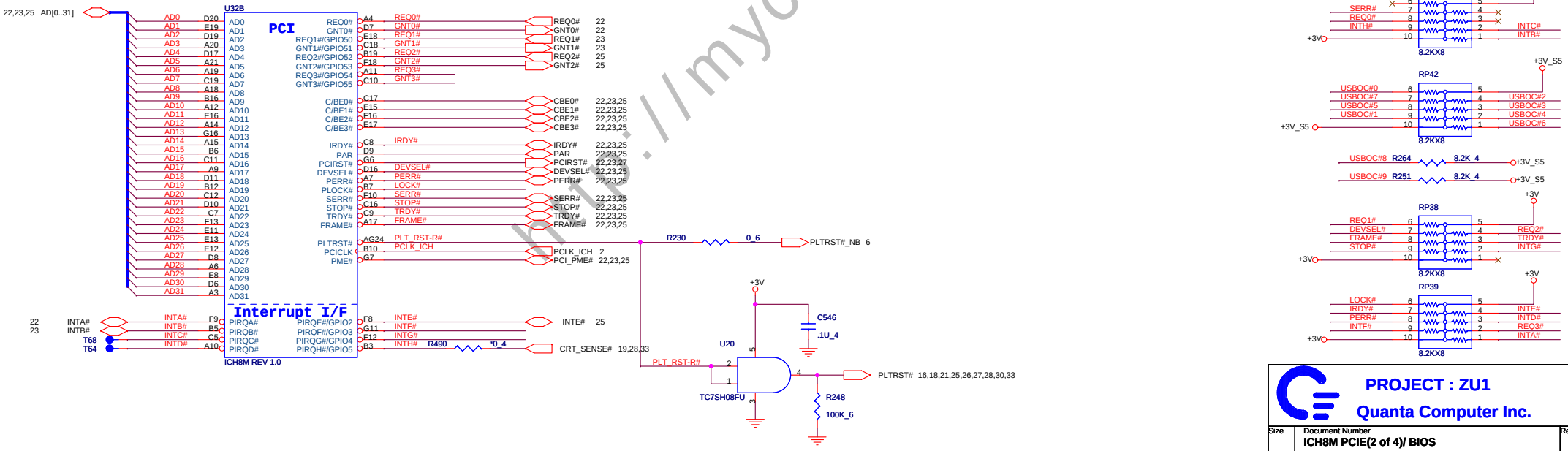


A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default

GNT3# R301 *1K_4

SB-PCI



PROJECT : ZU1

Quanta Computer Inc.

Size	Document Number	Rev
	ICH8M PCIE(2 of 4)/ BIOS	3B
Date: Tuesday, April 10, 2007	Sheet 15 of 39	

SB-GPIO

D3A:(1/31) ASF issue:when iAMT is not implemented, ICH8M SMBus and SMLink should be connected together to support slave mode Connect SMLINK0 to SMBCLK and SMLINK1 to SMBDATA (Add R474,R475 for debug use)

A1A:(9/29) no support iAMT, remove SMB_CLK_ME,SMB_DATA_ME

U32C

SMBCLK SMBDATA LINKALERT# SMLINK0 SMLINK1

PCLK_SMB AJ26
PDAT_SMB AD19
CL_RST#1 AG21
PCLK_SMB R474 0_4 SMLINK0 AC17
PDAT_SMB R475 0_4 SMLINK1 AE19

SMB

RI# AF17

A1A: (9/11) Remove RI#

SUS_STAT#/LPCPD# SYS_RESET#

LPC_PD# F4
SYS_RST# AD15

BMBUSY#/GPIO0

PM_BMBUSY# AG12

SMBALERT#/GPIO11

SMB_ALERT# AG22

STP_PCI#/GPIO15 STP_CPU#/GPIO25

PM_STPPCI_ICH# R459 0_4 AE20
PM_STPCPU_ICH# R460 0_4 AG18

CLKRUN#/GPIO32

CLKRUN# AH11

WAKE# SERIRQ THRM#

PCIE_WAKE# AE17
SERIRQ AF12
THERM_ALERT# AC13

VRMPWRGD

VR_PWRGD_CLKEN AJ20

TP7

ICH_TP7 AJ22

TACH1/GPIO1 TACH2/GPIO6 TACH3/GPIO7 GPIO8 GPIO12 TACH0/GPIO17 GPIO18 GPIO20 SCLOCK/GPIO22 QRT_STATE0/GPIO27 QRT_STATE1/GPIO28 SATACLKREQ#/GPIO35 SLOAD/GPIO38 SDATAOUT0/GPIO39 SDATAOUT1/GPIO48

KBSMI# D43 BAS316 KBSMI#_ICH AJ8
LID591# D44 BAS316 LID591#_ICH AJ9
GPIO7 AH9
SCI# AE16
DOCKIN#_ICH_R AC19
BOARD_ID0 AG8
BOARD_ID1 AH12
BOARD_ID3 AE11
ICH_GPIO22 AG10
ICH_GPIO27 AH25
ICH_GPIO28 AD16
GPIO35 AG13
RST_HDD# AF9
ICH_GPIO39 AJ11
ICH_GPIO48 AD10

SPKR

ACZ_SPKR AD9

MCH_SYNC#

MCH_ICH_SYNC#_R AJ13

TP3

ICH_TP3 AJ21

ICH8M REV 1.0

SATA0GP/GPIO21 AJ12 EMAIL_LED# T145
SATA1GP/GPIO19 AJ10 BOARD_ID2
SATA2GP/GPIO36 AE11 RBAYID0
SATA3GP/GPIO37 AG11 RBAYID1

SATA GPIO

CLK14 AG9 14M_ICH
CLK48 G5 CLKUSB_48

Clocks

SUSCLK D3 ICH8_SIO_32K T71

SIO/ PC87383 DOES NOT NEED 32KHz

SLP_S3# AG23 SLP_S3# R234 100_4 SUSB# 28
SLP_S4# AF21 SLP_S4# R243 100_4 SUSC# 28
SLP_S5# AD18 SLP_S5# T60

S4_STATE#/GPIO26 AH27

A1A: (9/26) Remove S4_STATE#, need be confirm?

PWROK AE23 ICH_PWROK

DPRSLPVR/GPIO16 AJ14 PM_DPRSLPVR_R R466 100_4 PM_DPRSLPVR

PM_DPRSLPVR 6,35

<FAE>
Since your CPU VRM has no DPRSTP# pin, connect PM_DPRSLPVR to IMVP6 is correct

BATLOW# AE21 PM_BATLOW#_R

PWRBTN# C2 DNBSWON# DNBSWON# 28

LAN_RST# AH20 PM_LAN_ENABLE_R R247 0_4 PLTRST#

A1A: 9/1 change to PLTRST#

PLTRST# 15,18,21,25,26,27,28,30,33

RSMRST# AG27 RSMRST#_R

CK_PWRGD E1 CK_PWRGD 2
CLPWROK E3 PWROK_EC 6,28
MPWROK 6,28

B1C:(11/20) short PWROK_EC to MPWROK

SLP_M# AJ25

A1A:(9/16) Remove SUSM# used to control power planes to the Intel AMT sub-system

CL_CLK0 AE18 CL_CLK0 6
CL_CLK1 AF23 CL_CLK1 27
CL_DATA0 AF22 CL_DATA0 6
CL_DATA1 AF19 CL_DATA1 27
CL_VREF0 D24 CL_VREF0_SB
CL_VREF1 AH23 CL_VREF1_SB
CL_RST# AJ23 CL_RST#0 6

MEM_LED/GPIO24 AJ27 ICH_GPIO24
ME_EC_ALERT/GPIO10 AJ24 ICH_GPIO10
EC_ME_ALERT/GPIO14 AF22 ICH_GPIO14
WOL_EN/GPIO9 AG19

A1A: (9/26) Remove (1)ME_EC_ALERT# (2)EC_ME_ALERT

B1C:(11/24) add GPIO10 PU +3V,GPIO14 PD to GND

A1A: (9/11) Remove LAN_WOL_EN circuit

GPIO

Power MGT

SYS

Controller Link

MISC

CLKUSB_48 R335 *10_4 C412 *10P_4

14M_ICH R481 *33_4 C559 *10P_4

E3A:(3/26)
LAN_RST# should be terminated by 8.2-10 kΩ pull down resistor to GND if an Intelk 82566 MM/MC integrated LAN solution is not used.->
(1)Stuff 10k for R204
(2)Don't stuff R456
(3)Don't stuff R247

+3V_S5 R233 *3.24K_6 R229 *453_4 C355 *.1U_4

+3V R453 3.24K_6 R452 453_4 C357 .1U_4

B1C:(11/29) no stuff R229,R233,C355

U31 NC7SZ04

35 VR_PWRGD_CK410# C338 .1U_4 R250 100K_4 VR_PWRGD_CLKEN

A1A: (9/26) change name from VR_PWRGD_CLKEN# to VR_PWRGD_CK410#

B1C: (11/24) add D43,D44 to stop leakage from EC to SB

B1C:(11/28) change DOCKIN# from GPIO7 to GPIO12

18,33 DOCKIN# D24 BAS316

R256 *10K_4 R254 *10K_4

2 PM_STPPCI# 2 PM_STPCPU#

R468 *10K_4

6 MCH_ICH_SYNC# R469 0_4

<check list> internal PD

A1A: (9/26) Remove SATACLKREQ#

26 RST_HDD#

A1A:(9/29) no support iAMT, remove 2ND_MBCLK,2ND_MBDATA,Q11,Q12

3,6,35 DELAY_VR_PWRGOOD R298 100K_4 PWROK_EC

U21 TC7SH08FU

C393 .1U_4 ICH_PWROK

+3VSUS

A1A:(10/12) change from +3V to +3VSUS (Refer to ZC1)

A1A:(9/20) Refer to ZD1, Add ICH_PWROK circuit

+3V_S5

SYS_RST# R263 10K_4

DNBSWON# R329 *10K_4

Internal Pull up

ICH_GPIO24 R454 *10K_4
DOCKIN#_ICH_R R319 8.2K_4

A1A:(10/30) change DOCKIN#_ICH_R PU from +3V to +3V_S5

INTEL CRB: PU +3V

LID591#_ICH R473 10K_4
KBSMI#_ICH R480 10K_4

SCI# R261 10K_4
ICH_GPIO10 R568 10K_4

ICH_GPIO22 R312 10K_4
ICH_GPIO48 R315 10K_4
RST_HDD# R314 10K_4
RBAYID0 R311 8.2K_4
RBAYID1 R300 8.2K_4

ICH_GPIO14 R569 10K_4
PM_DPRSLPVR R269 100K_4

ICH_PWROK R238 10K_4

INTEL CRB NEED THOSE PU & PD.

PM_LAN_ENABLE_R R456 *10K_4

INTEL CRB SHOW IT

ICH_GPIO39 R470 10K_4

INTEL CRB SHOW IT

PM_LAN_ENABLE_R R204 10K_4

DISABLE LAN: STUFF

INTEL FAE (08/17)
"Add RSMRST# isolation (important!!! See ww22 Santa Rosa MoW)"

+3VSUS R207 4.7K_4

Q23 MMBT3906

RSMRST#_R TO ICH8

RSMRST# 28 FROM uR(EC)

R215 10K_4

D21 BAV99

D20 BAV99

R196 2.2K_4

No Reboot strap

HDA_SPKR	Low = Default High = No Reboot

ACZ_SPKR R288 *10K_4

BIOS/ ERIC: UNSTUFF

GPIO35 R265 10K_4
THERM_ALERT# R270 8.2K_4
SERIRQ R299 10K_4
CLKRUN# R305 8.2K_4

ECN 2A
INTEL CRB V1.301
CL_RST# NO NEED PU.

A1A:(9/29) no support iAMT, remove PU +3V_S5 circuit (R259/R258)

RI# R258 10K_4
CL_RST#1 R242 *10K_4
PCLK_SMB R455 2.2K_4
PDAT_SMB R255 2.2K_4
SMB_ALERT# R235 10K_4
PCIE_WAKE# R260 1K_4
PM_BATLOW#_R R245 8.2K_4
GPIO7 R259 *10K_4

C2A:(12/21) no stuff R259 to prevent leakage issue

Board ID	ID3	ID2	ID1	ID0
With EZ Dock	0	0	0	0
W/O EZ Dock	0	0	0	1
RSV	0	0	1	0
RSV	0	0	1	1
RSV	0	1	0	0

R472 *10K_4 BOARD_ID2 R471 10K_4
R310 *10K_4 BOARD_ID1 R304 10K_4
R324 *10K_4 BOARD_ID0 R320 10K_4

C2A:(12/12) Intel Suggest :ICH8M CPIO20 should not be pulled HIGH. Remove BOARD_ID3 circuit(remove R474,R475)

Size	Document Number ICH8M GPIO(3 of 4)		Rev 3B
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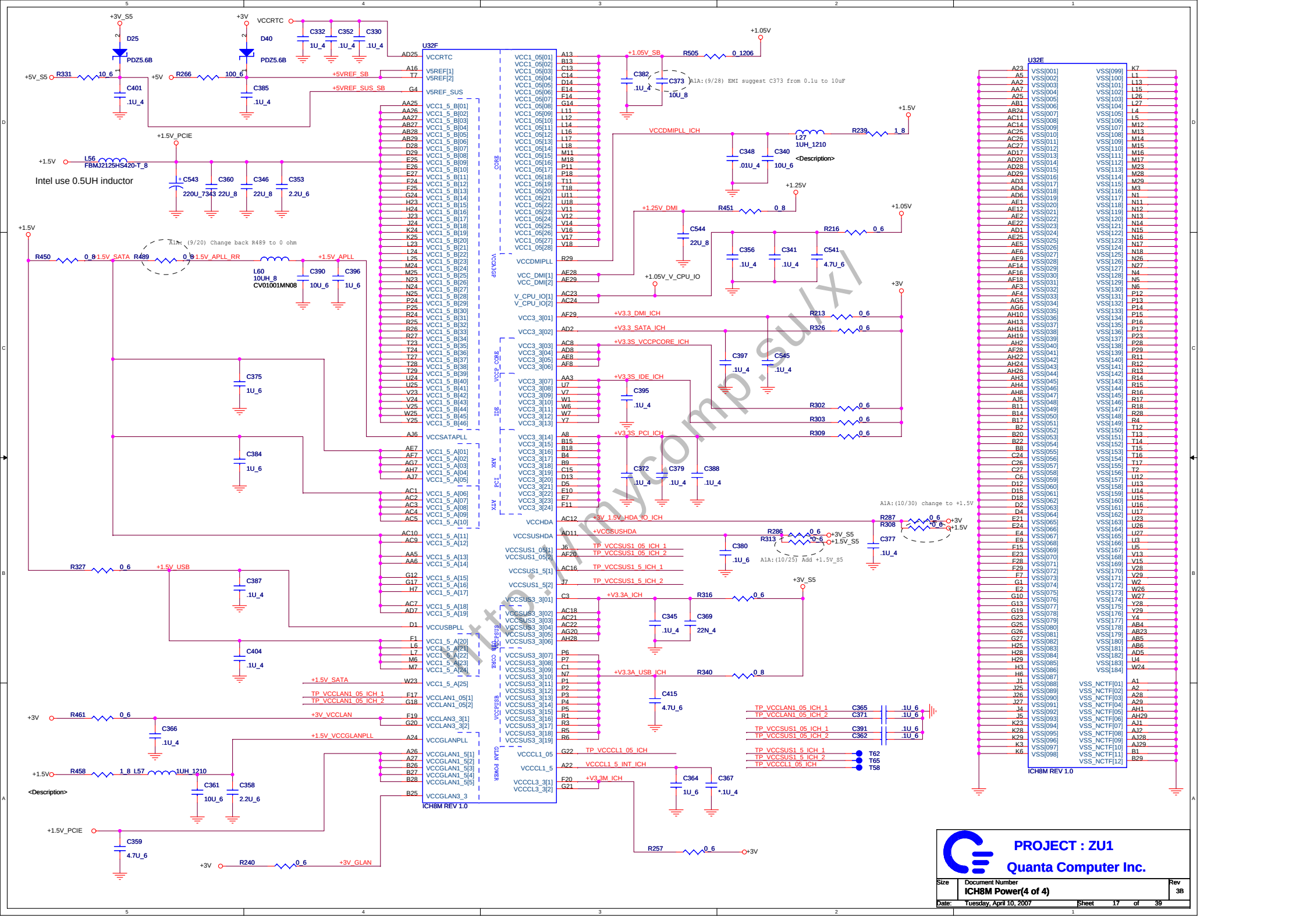
U32F
ICH8M REV 1.0
U32E
ICH8M REV 1.0
Intel use 0.5UH inductor
A1A: (9/20) Change back R489 to 0 ohm
A1A:(9/28) EMI suggest C373 from 0.1u to 10uF
A1A:(10/30) change to +1.5V
A1A:(10/25) Add +1.5V_S5
<Description>
PROJECT : ZU1
Quanta Computer Inc.
ICH8M Power(4 of 4)
Size
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Rev
3B
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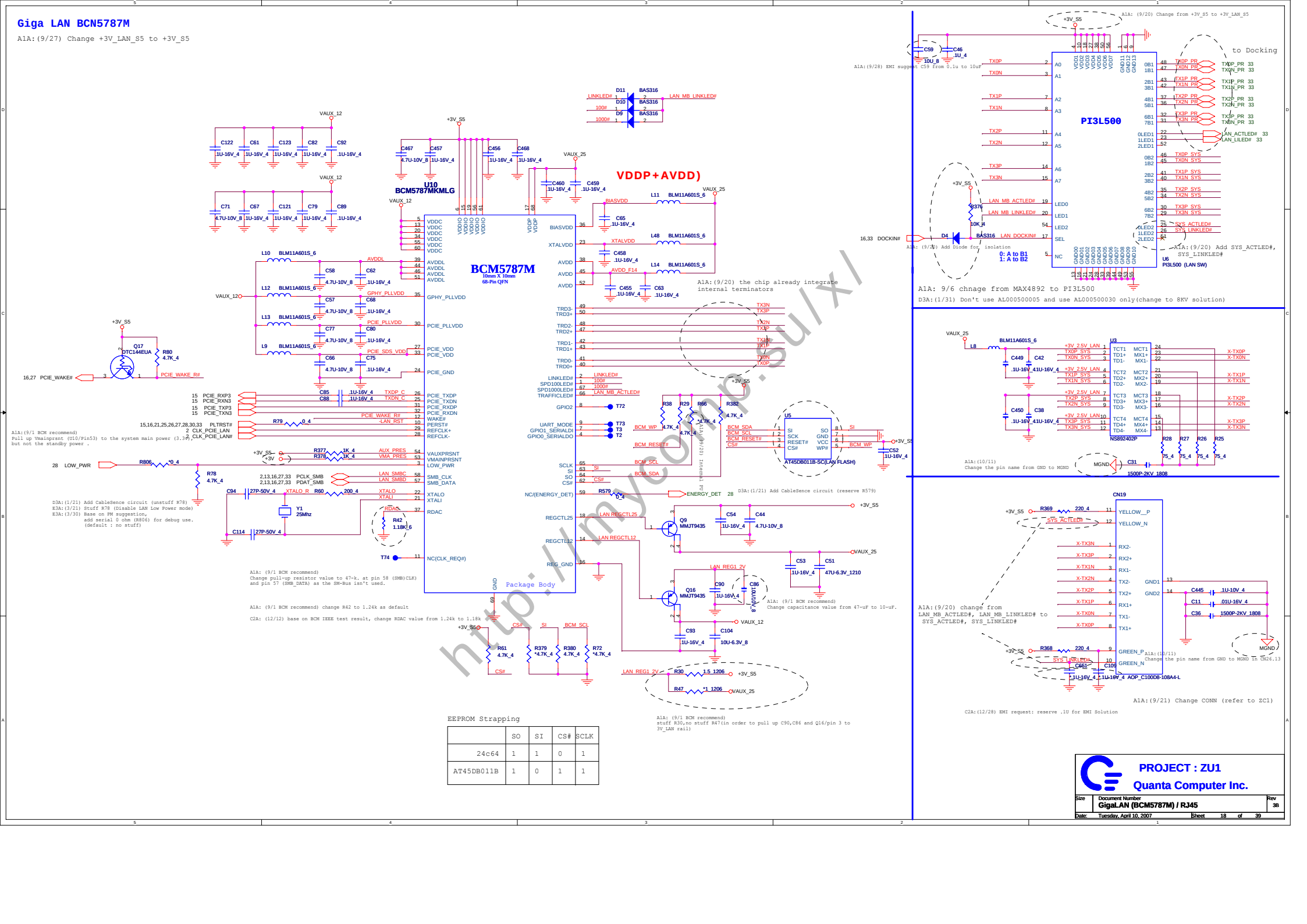
http://mycomp.su/x/

Giga LAN BCN5787M

A1A:(9/27) Change +3V_LAN_S5 to +3V_S5



EEPROM Strapping

	SO	SI	CS#	SCLK
24c64	1	1	0	1
AT45DB011B	1	0	1	1

PROJECT : ZU1

Quanta Computer Inc.

Size	Document Number	Rev
	GigaLAN (BCM5787M) / RJ45	3B

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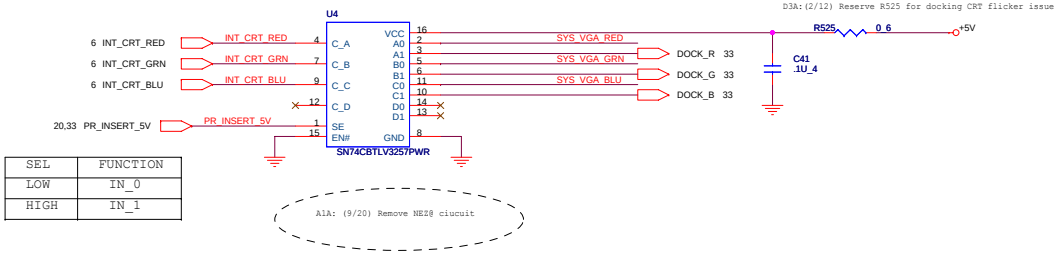
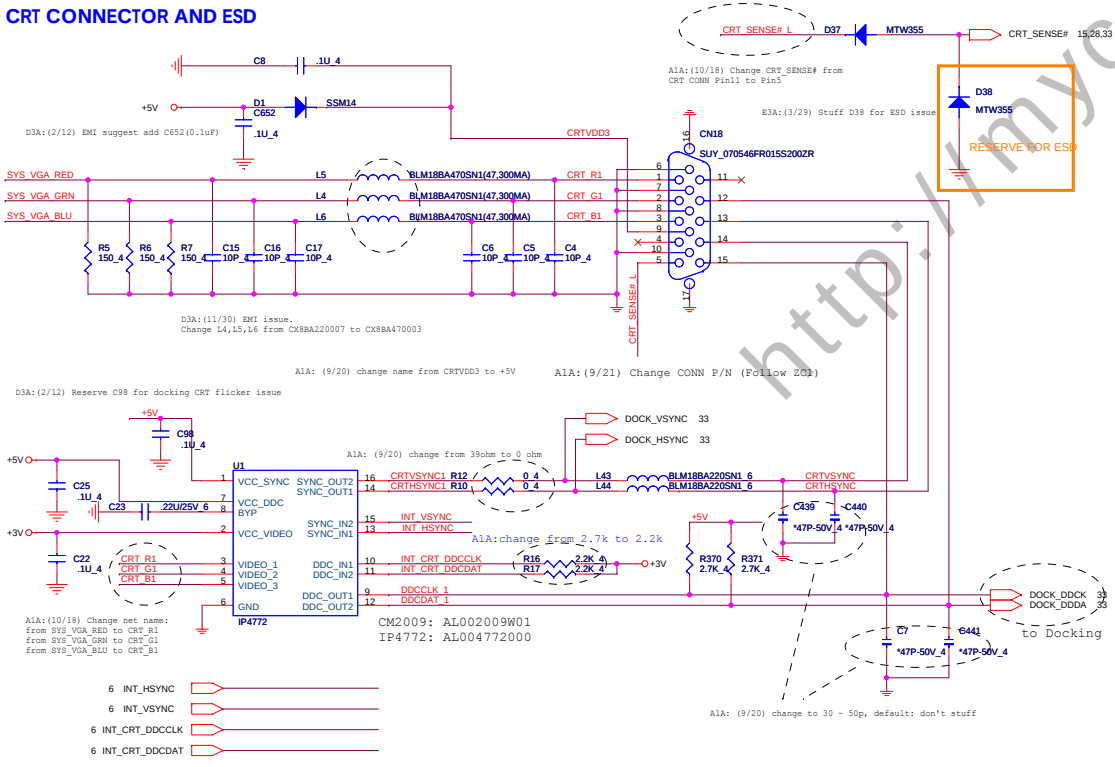
CRT Select



SEL	FUNCTION
LOW	IN_0
HIGH	IN_1

CRT CONNECTOR AND ESD



PROJECT : ZU1
Quanta Computer Inc.

Size	Document Number	Rev
	CRT	3B
Date: Tuesday, April 10, 2007	Sheet 19 of 39	

LVDS

B1C: (11/20)
(1) change PWM control from 965GM to EC
(2) Short L7, un-stuff C28 (L-C filter will impact PWM signal)
(3)stuff R13,no stuff R15

C2A:(12/28) EMI request: reserve L-C footprint for debug use (R52,C650)
D3A:(2/12) Stuff R15, Change PWM control from EC to 965GM
D3A:(2/14) Acer inform no support DPST in C build, remove R15

A1A:(10/2) change from USB7 to USB8

A1A: (9/20) Come from 965GM for PWM control

E3A:(3/15) Link C650 from DMIC-CLK to DMIC-CLK_1

A1A(10/5):Change C12 from CH6102M9900 to CH61004M3E5 (refer to ZC3)
E3A:(4/3) EOL issue change from CH61004M3E5 to CH61004M398

A1A: (9/20) Change LVDS CONN to 30pin
(9/21)change footprint to 88242-3000-30P-RUV

E3A:(3/14)Change MB LCD connector pin define(CN2) and LCD cable pin define to cover production line issue
(Inverter short with signal to burn system)->ZR1 issue
(1)pin 27,29->NC
(2)pin 28,30->INVCC(VIN)->same as C build
(3)pin 8->INT_LVDS_EDIDDATA

<demo circuit>
Crestline suggest 100K
G73 suggest 10K(ZS1 Default)
8/27 change back to 100K

D3A:(2/12)
change U2 from AL004280000(AAT4280IGU-3-T1) to AL004280018(AAT4280IGU-1-T1).
rise time of LCDVCC is >0.5ms and <=10ms.
AL004280018 can meet this spec

CAMERA MODULE

BECAUSE UR'S SUGGESTION,
ACTICE CHANGE FROM LOW TO HIGH.

TV Out (SVHS) MiniDIN 7-pin

SEL	FUNCTION
LOW	IN_0
HIGH	IN_1

A1A: (9/20) Remove "NEZ@" circuit

A1A:(9/21) Change CONN (Follow ZC1)

MR Sensor

D3A:(2/12) Follow ZO1 design,
Remove R24 footprint, DEL D3(BC000316Z07).
Add R73,Q36,Q37

D3A:(2/12) system sometimes will no backlight issue .
For short term solution:
change R22 from 10k(CS31002JB28) to 1K (CS21002FB24)

PROJECT : ZU1
Quanta Computer Inc.

Size	Document Number	Rev
	LVDS/MR senseor/SVIDEO	3B

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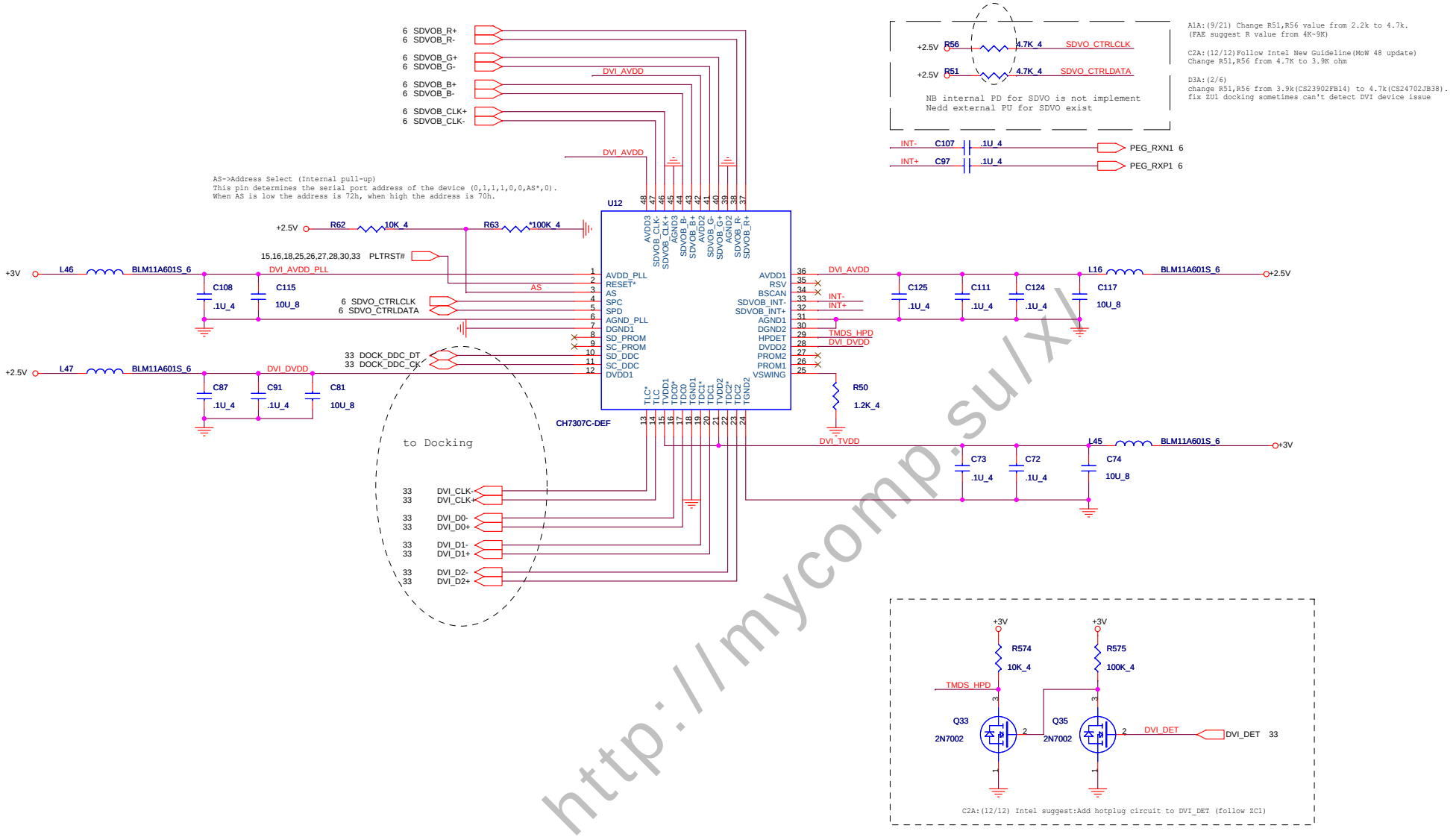
SDVO-DVI



A1A:(9/21) Change R51,R56 value from 2.2k to 4.7k.
(FAE suggest R value from 4K~9K)

C2A:(12/12)Follow Intel New Guideline(MoW 48 update)
Change R51,R56 from 4.7K to 3.9K ohm

D3A:(2/6)
change R51,R56 from 3.9k(CS23902FB14) to 4.7k(CS24702JB38).
fix ZU1 docking sometimes can't detect DVI device issue

D3A:(1/30) remove U13,R68,R75,R73,C98
1/16 confirm with CHRONTEL FAE,
he said we can remove CH9901 (U13),
If ZU1 need support HDCP,
just need change controller from CH7307 to CH7313.
CH7313 already integrated HDCP function, no need external EEPROM.

C2A:(12/22) confrim with FAE ->
Due to Intel VBIOS already integrate the EEPROM function.
ZU1 will remove the U11,R57,R52,C109 to save layout space.

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Quanta Computer Inc.

Size	Document Number	Rev
	DVI (CH7307)	3B
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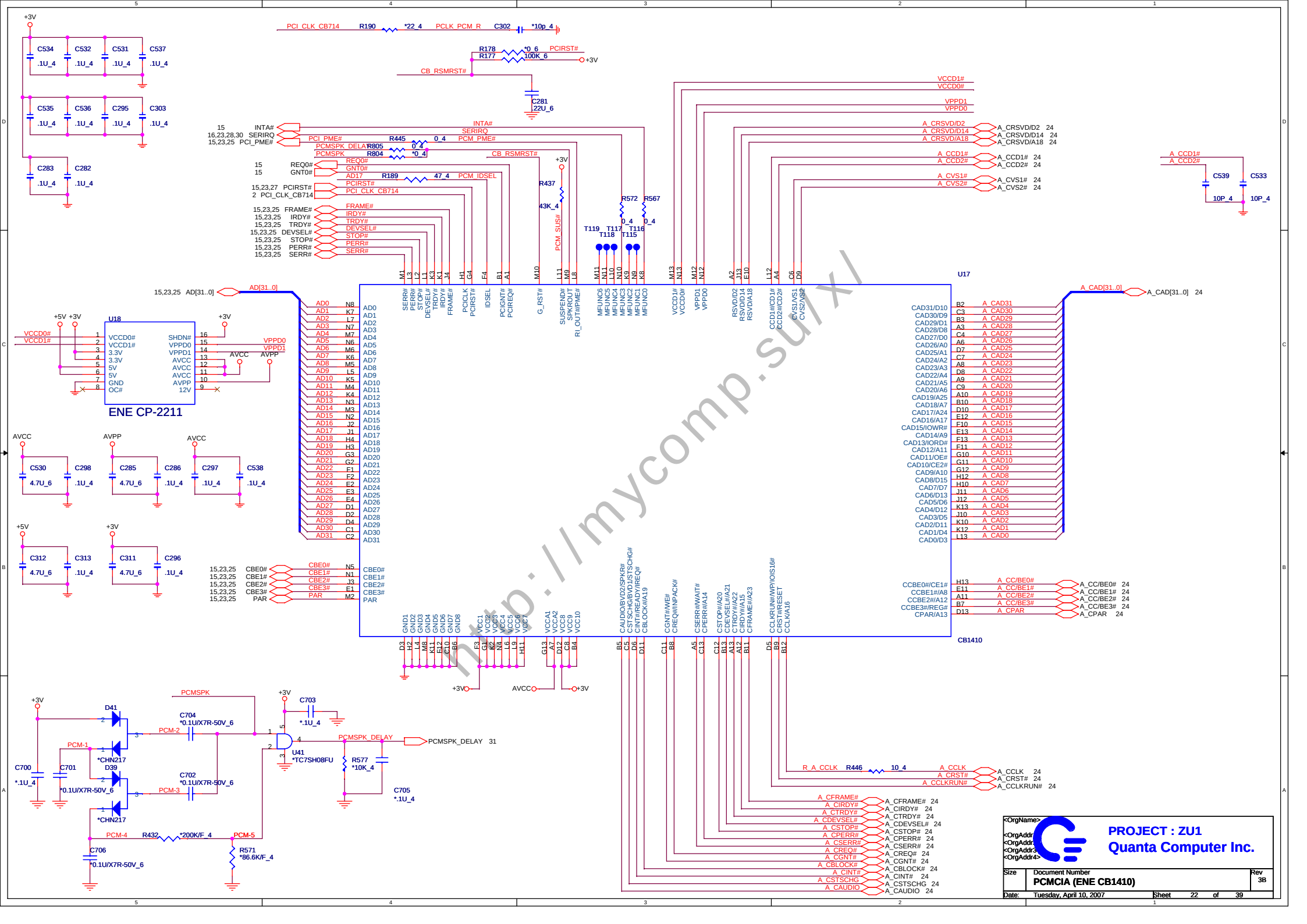
ENE CP-2211
U17
CB1410
U18
U41
*TC7SH08FU
PROJECT : ZU1
Quanta Computer Inc.
PCMCIA (ENE CB1410)
Tuesday, April 10, 2007
http://mycomp.su/x/

ID Select : AD18
Interrupt Pin : INTB#
Request Indicate : REQ1#
Grant Indicate : GNT1#

GRST# should connect to Power On reset if support S3

A1A:(9/22) no stuff R496,R522

48MHz Clock

A1A:(9/26) Add 22ohm for R490 and 10p for C839
Change Y7 from 50MHz to 48MHz

A1A:(9/28) base on EMI suggest: remove R490,C839

A1A:(9/22) XMDAT4B is for 8 bit MMC,remove it.

D3A:(2/12)
(1)no stuff 43K(CS34302JB19):
R562,R527,R533,R538,R539,R565,R561,R540,R498,R497,R500,R552,R555
(2)no stuff 10k(CS31002JB28) : R560
(3) Change R547 from 43k (CS34302JB19) to 8.2k (CS28202JB14)
(4)Change R528 from 10K(CS31002JB28) to 43K(CS34302JB19)

A1A:(9/22) FAE suggest R value under 47 ohm.

A1A:(9/22) Add PU/PD resister

A1A:(9/26) For EMI solution
(close to MR510)

A1A:(9/26) For EMI solution

Size	Document Number: Card Reader (MR510)
Rev	3B
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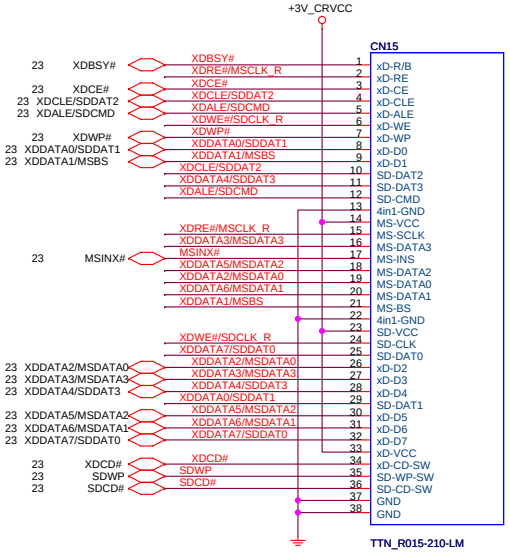
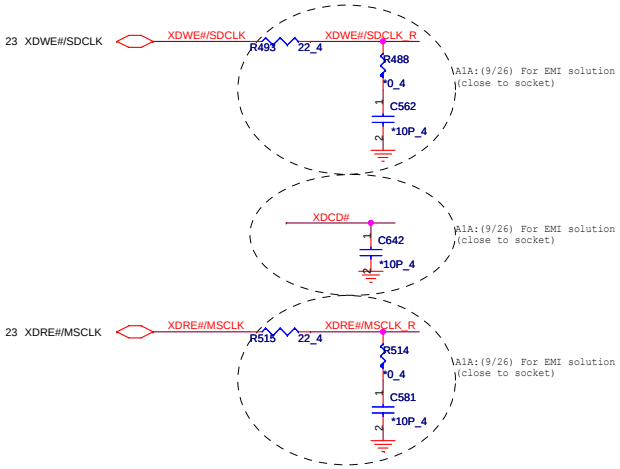
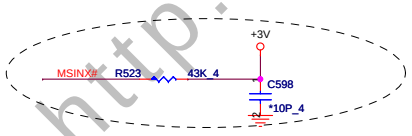
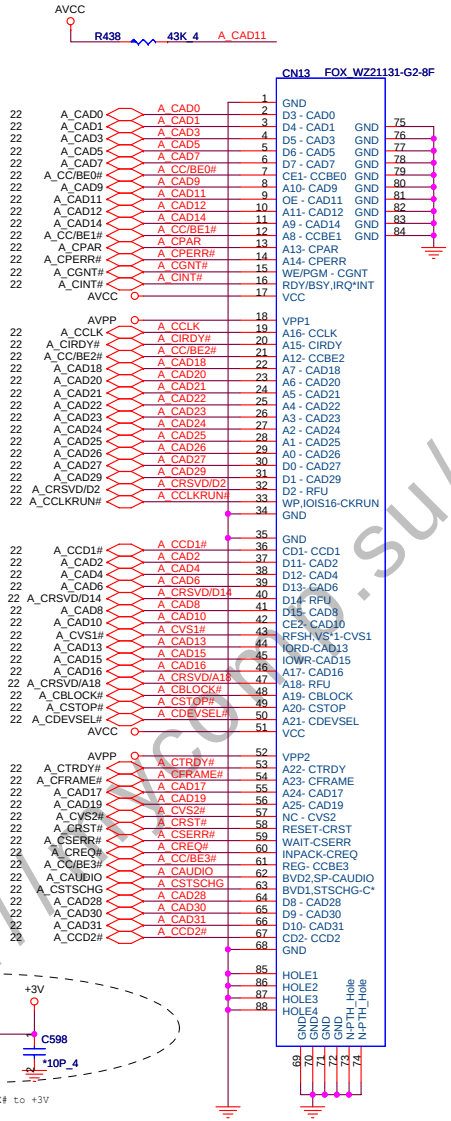
PROJECT : ZU1
Quanta Computer Inc.

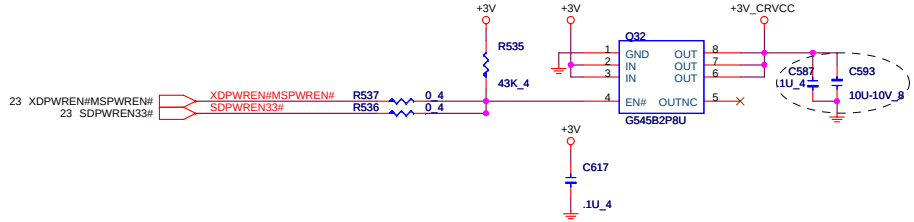
Main Source:TTN DFHD36MR000
2nd Source:NorthStar DFHS36FR003











PROJECT : ZU1
Quanta Computer Inc.

Size	Document Number	Rev
	CARD Reader & PCMCIA SLOT	3B
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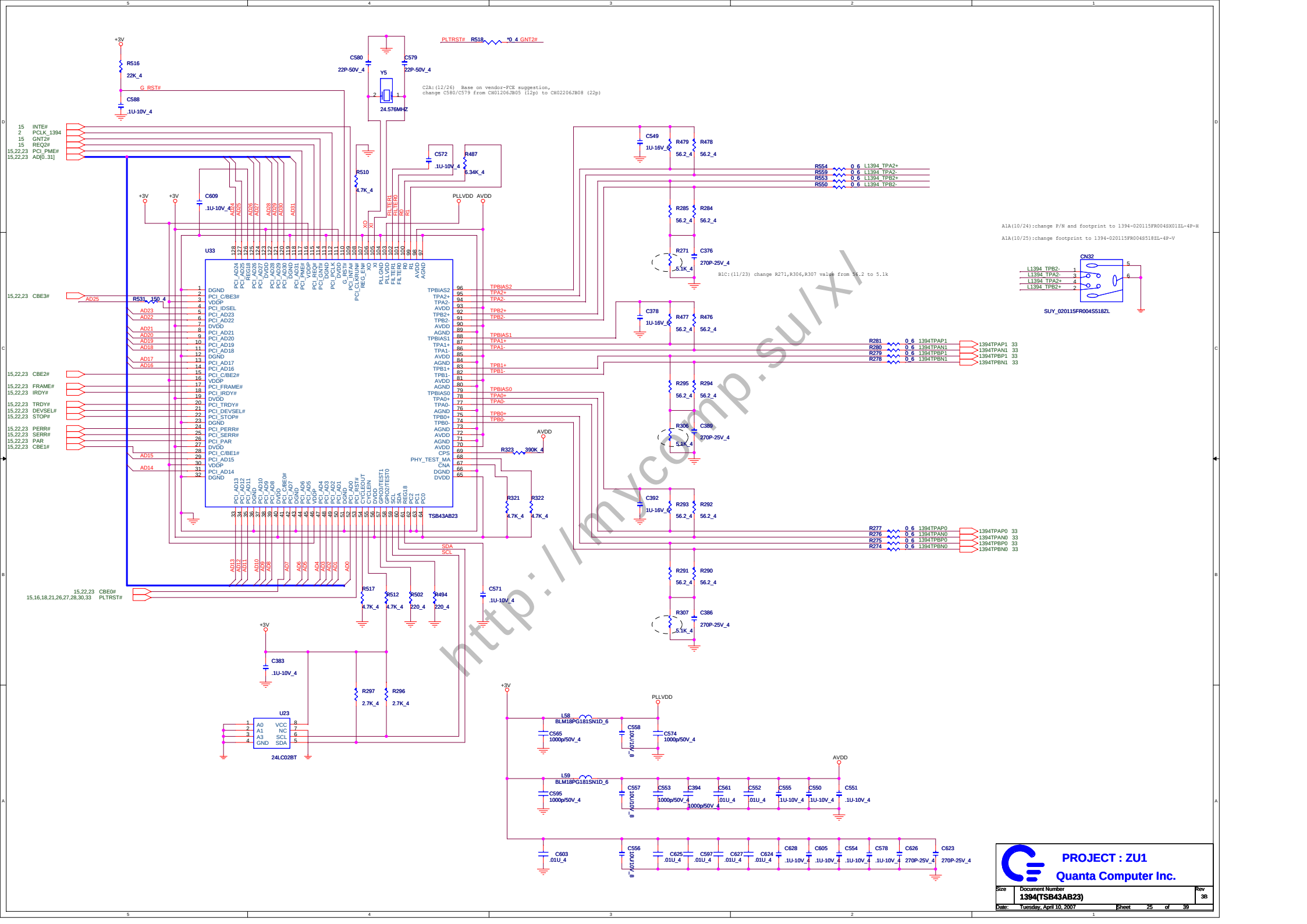
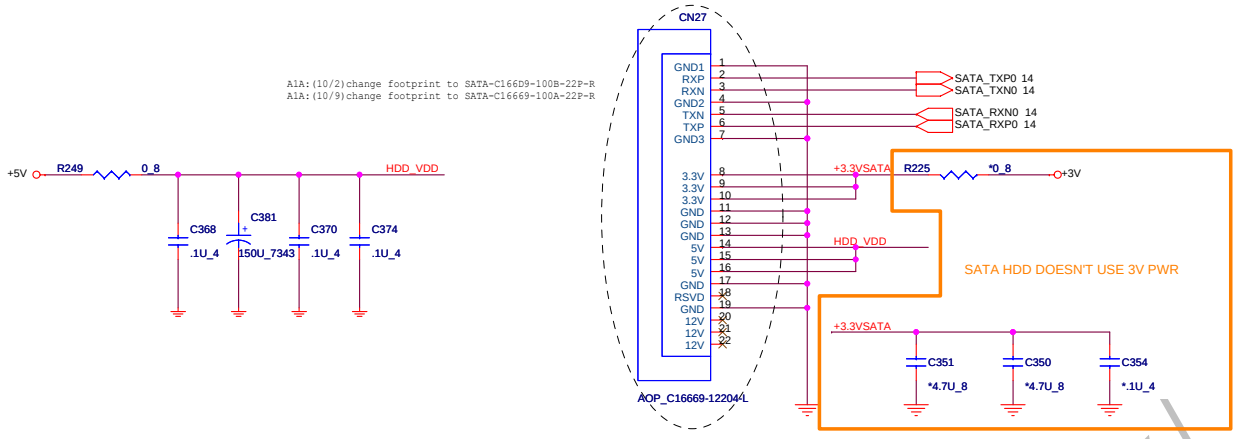
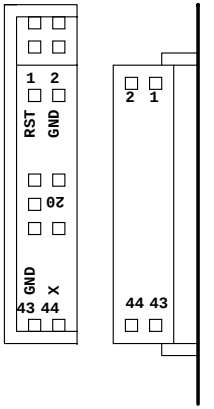
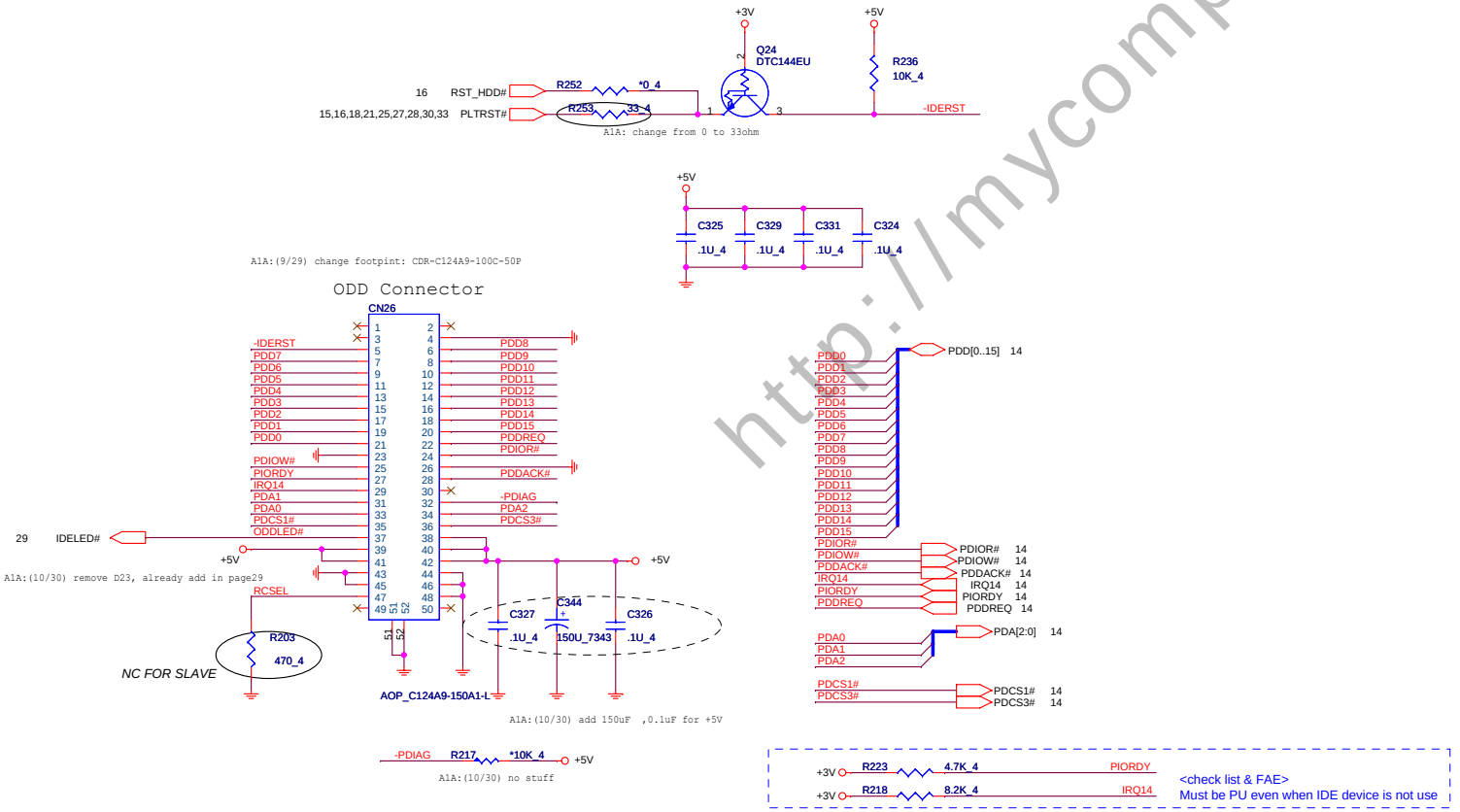

U33
TSB43AB23
U23
24LC02BT
CN32
SUY_020115FR004S518ZL
PROJECT : ZU1
Quanta Computer Inc.
1394(TSB43AB23)
Tuesday, April 10, 2007
Sheet 25 of 39
A1A(10/24):change P/N and footprint to 1394-020115FR004SX012L-4P-H
A1A(10/25):change footprint to 1394-020115FR004S518ZL-4P-V
B1C:(11/23) change R271,R306,R307 value from 56.2 to 5.1k
C2A:(12/26) Base on vendor-FCE suggestion, change C580/C579 from CH01206JB05 (12p) to CH02206JB08 (22p)
http://mycomp.su/xl

SATA HDD





PATA ODD



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	SATA-HDD & PATA-ODD	3B

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MINI-Card

A1A: (9/20) Change from +3V to +3V_WL_VDD
A1A: (10/23)change +3V to +3VSUS
B1C: (10/23)change from +3VSUS to +3V

+3V L28 FBJ3216HS800_1206
C398 10U/10V/X5R_8 C413 .1U_4 C414 .1U_4 C419 .1U_4
+3V_WL_VDD

+1.5V C402 10U_8 C403 .1U_4
POWER DECOUPLING

D3A:(1/21) Stuff R349,R350 for debug use

A1A:9/4 Reserved for debug only

15,22,23 PCIRST#
2,30 PCI_CLK_SIO
PCIRST# R349 0_4 CL_DATA1_CN
PCLK_SIO R350 0_4 CL_CLK1_CN

B1C:(11/29) no stuff R353,R348,R356

16 CL_RST#1 R353 *0_4 CL_RST#0_CN
16 CL_DATA1 R348 *0_4 CL_DATA1_CN
16 CL_CLK1 R356 *0_4 CL_CLK1_CN
R354 0_4 KEDRON_GND_43
R351 0_6 KEDRON_VCC
A1A(10/30): Add (CN28/Pin39,41) to +3V_WL_VDD (follow ZO1)
+3V_WL_VDD R355 0_4 KEDRON_GND_37

15 PCIE_TXP4
15 PCIE_TXN4
15 PCIE_RXP4
15 PCIE_RXN4
PCIE_RXP4
PCIE_RXN4
A1A:(10/30) Remove 0.1uF *2pcs
28 uR_SOUT_CR
28 uR_SWD

+3VSUS 2 CLK_PCIE_MINI1
2 CLK_PCIE_MINI1#
Q25 *DTC144EU R357 *4.7K_4
16,18 PCIE_WAKE#
PCIE_WAKE#_MINI-Card

E3A:(3/16) Base on Acer demand, remove wake on lan for Mini PCIE function.
no stuff Q25,R357

+1.5V 0_4 R336 +1.5V_MINI-Card
+3V_WL_VDD +3V_WL_VDD
A1A:(10/30)change form +3VSUS to +3V_WL_VDD
C424 10U_8 C422 .1U_4

CN28 ACS_88911-5204

51	Reserved	+3.3V	52
49	Reserved	GND	50
47	Reserved	+1.5V	48
45	Reserved	LED_WPAN#	46
43	Reserved	LED_WLAN#	44
41	Reserved	LED_WWAN#	42
39	Reserved	GND	40
37	Reserved	USB_D+	38
35	GND	USB_D-	36
33	PETp0	GND	34
31	PETn0	SMB_DATA	32
29	GND	SMB_CLK	30
27	GND	+1.5V	28
25	PERp0	GND	26
23	PERn0	+3.3Vaux	24
21	GND	PERST#	22
19	Reserved	Reserved	20
17	Reserved	GND	18
15	GND	Reserved	16
13	REFCLK+	Reserved	14
11	REFCLK-	Reserved	12
9	GND	Reserved	10
7	CLKREQ#	Reserved	8
5	Reserved	+1.5V	6
3	Reserved	GND	4
1	WAKE#	+3.3V	2

A1A: (9/26) Remove (CN28/Pin46)BT_LED
WIRELESS_LED# 29
A1A: (9/20) Remove USB_CTRL
MINI_DAT_SMB
MINI_CLK_SMB
B1C:(11/13) Robson ES1 to ES2 change. PIN 37 => GND
B1C:(11/20) need support BCM module PIN 40 => GND
RF_EN_RR R343 0_4 PLTRST# 15,16,18,21,25,26,28,30,33
RF_EN 28
R337 LFRAME# 14,28,30
R345 LAD3 14,28,30
R341 LAD2 14,28,30
R338 LAD1 14,28,30
R339 LAD0 14,28,30
A1A:9/4 Reserved for debug only

B1D:(12/9) change from 9.0mm to 9.9mm (ME request)

+3V Q14 RHU002N06 R48 10K_4 MINI_DAT_SMB
2,13,16,18,33 PDAT_SMB
+3V Q15 RHU002N06 R58 10K_4 MINI_CLK_SMB
2,13,16,18,33 PCLK_SMB

BLUETOOTH MODULE CONNECTOR

A1A: (9/25) change CONN (follow ZH3)

D3A:(2/8)EMI suggest, add common Choke, co-lay R795,R796

15 USBP4+
15 USBP4-
29 BT_LED
BT_POWER
BT_LED
CN5 ACS_88266-05001-06

Q10 AO3413
+3VSUS
BT_POWER_R L15 BK2125HS330_8 BT_POWER
C105 10U_8
C101 1000P_4
C102 .01U_4
BT_POWERON# 28
A1A:(10/25) SI suggest to remove 22pF*2

USB CONN

+5V_S5
U16 TPS2061DGNR
28 USBON#
USBPWR1
R435 *6.34K_4
C305 .1U_4
C279 100U_3528
C289 1000P_4
15 USBP0-
15 USBP0+
CN11 SUY_020133MB004S557ZL
U15 CM1293-04SO
A1A: (9/24)change USB CONN (follow ZC3)
A1A:(10/25) SI suggest to remove 22pF*2

CN21 (B-B) ACS 88028-1210M
15 USBP1-
15 USBP1+
15 USBP2-
15 USBP2+
USBON#
C45 .1U_4
A1A: (10/13) change CONN (follow ZH2 Audio DB)

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A1A:(9/16)Change from WPC8769 to WPC8763

A1A: (9/25) change VBAT from +3VPCU to +A3VPCU

1/13 Comfirm by vendor mail:
VDD must power up after VCC/AVCC

1/13 Comfirm by vendor mail:
VBAT for keep PLL power let power up can quick
If no VBAT will switch to VCCpower.
If PLL no power will cause boot time delay.

A1A: (9/25) place the above capacitors as close to the pins as possible

08/10 FAE: SMI DOESN'T NEED DIODE

FOLLOW INTEL ME-EC INTERFACE SPECIFICATION,
2ND_SMB IS DEDICATED FOR ICH8 CONTROLLER LINK BUS.

08/10 FAE:
ADD ONE GAD PAD UNDER X'TAL,
AND KEEP CLEANCE.

A1A: (9/25)
FAE: PUT Y6 with EC in the same side

A1A:(9/27)change C130,C131 from 6.8p to 5.6p

1/13 Comfirm by vendor mail :
Connect to AGND

C2A:(12/26) Base on vendor-FCE suggestion,
change C130/C131 from CH-5606TB01 (5.6p) to CH0100GJB01 (10p)

A1A: (9/26) Add HWPG_CPUIO

C2A:(12/25) Steven:D16 not necessary if 3V/5V fail, EC can't work.
This monitor circuit is't necessary.

E3A:(3/16)PE request move D15~D18 location for FFC cable issue.Remove D16 footprint and net (HWPG_3/5VPCU) to save layout space.

A1A: (9/26) Add it. Capacitors as close to EC as possible

E3A:(3/15) ICMNT connect to EC pin100(AD pin for power control) , reserve R570 0ohm for debug use

B1C:(10/20)SWAP GPIO1 & GPIO3 (follow EC team)
A1A:(9/29)SWAP GPIO3 & GPIO6 (follow EC team)

A1A: (9/26) Remove BL/C#

08/10 FAE: ADD TP FOR DEBUG

A1A: (9/26) Remove LAN_ON
A1A: (9/26) Remove EC_ME_ALERT

C2A:(12/12)FAE suggest add 22 Ohm dumping resistors on SPI flash interface F_SCK(pin92) and F_SDO(pin87) to avoid potential EMI problem

0~AVCC power for DA pin power reference

08/14 FAE:
Please connect VREF(uRider pin104) to +A3VPCU instead of +3VPCU.

SM BUS PU

I/O ADDRESS SETTING

BADDR1-0	I/O Address	
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

ACER ID

A1A:(9/29) change from MBCLK/MNDATA to 2ND_MBCLK/2ND_MBDATA

D3A:(1/21) Add CableSence circuit

D3A:(1/31) Anda inform: change LAN Low power pin from GPIO47 to GPIO52

SPI FLASH

1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

BUTTON ON KEYBOARD MATRIX

DEBUG PORTS

B1C:(11/28) change CN10/pin1 from +3V to +3VPCU

EC Debug Port

LPC debug card

A1A(10/5):Change LPC debug CONN to DFFC10FR103

E3A:(3/22) confirm with BIOS-CM, no need LPC dedug CONN, Remove CN6,R432 footprint to save space for layout.

INTERNAL KEYBOARD STRIP SET

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Quanta Computer Inc.

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	EC (PC8763LDG)/ FLASH	3B
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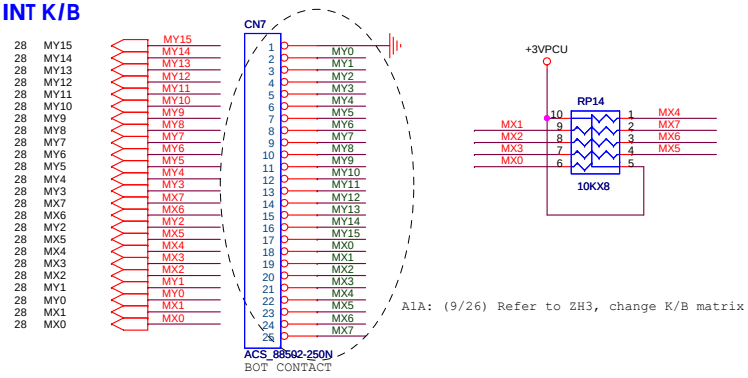
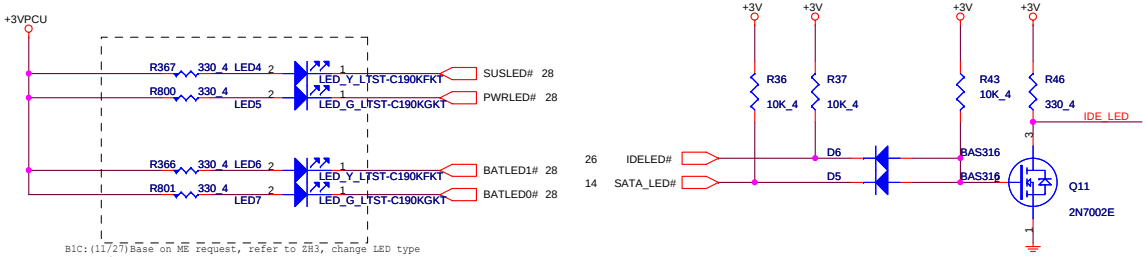
INT K/B



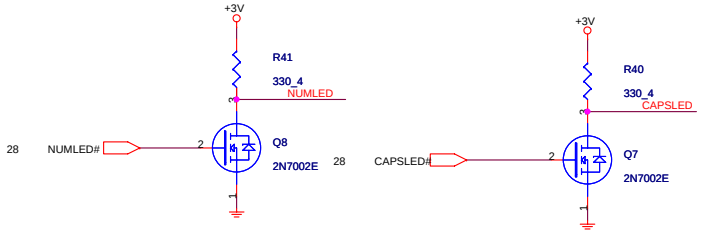
uR REQUEST
MY DOES NOT NEED PU.
MY CAN NOT USE EMI BYPASS CAP, DUE TO FLASH.

A1A: (9/26) Refer to ZH3, change K/B matrix

LED



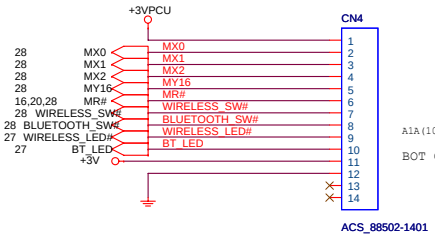
B1C:(11/27)Base on ME request, refer to ZH3, change LED type
B1C:(11/28)Base on ME request, change LED type
D3A:(1/24) Base on SMT-ME request, change LED type to 2 in 1
DEL LED4,LED5,LED6,LED7,R570,R571,Add LED2,LED3
E3A:(3/16)Change LED2, LED3 type base on ME request, Add R800,R801
E3A:(3/30) ESD issue, change LED type (follow B stage)



A1A:(10/30)no stuff (ZU1 no support EMAIL LED)

E3A:(3/30)Remove Q27,R1 footprint to save space for layout
ZU1 no support E-Mail LED

Function Board



A1A(10/5):Change Pin define (Base on Acer ID)

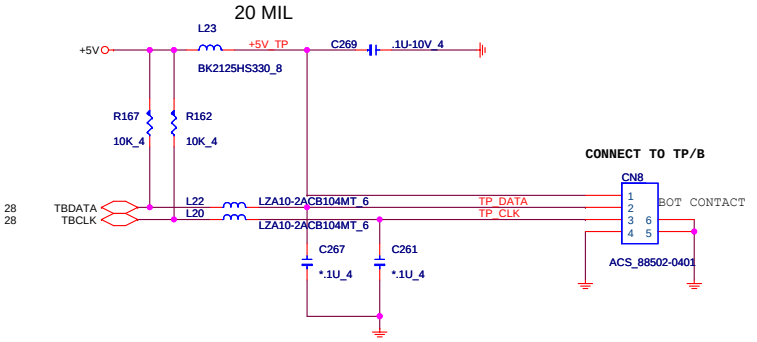
BOT CONTACT

A1A:(9/27) Add Function Board CONN (14pin)

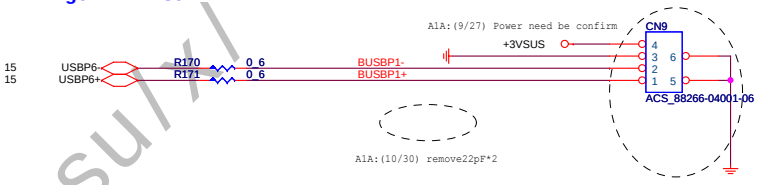
A1A:(10/30) add +3V for Daughter Board use

Keyboard Matrix	Button
MX0/MY16	acer EAP Buttton
MX1/MY16	acer EMAIL Buttton
MX2/MY16	acer WWW Buttton
MX3/MY16	acer EPM Buttton
MX4/MY16	WIRELESS Button
MX5/MY16	BLUETOOTH Button

TOUCH PAD

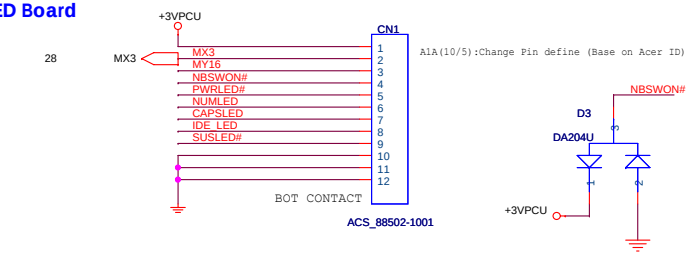


Finger Printer



A1A:(10/30) remove22pF*2

LED Board

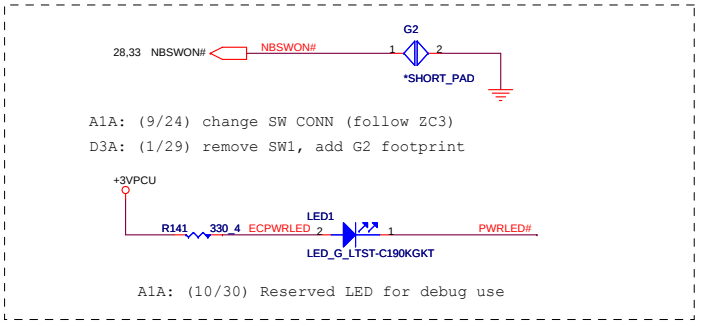


A1A(10/5):Change Pin define (Base on Acer ID)

A1A:(9/27) Add LED Board CONN (10pin)

A1A:(10/26) Add SUSLED#

E3A:(3/30) change ESD protect Diode location from LED/B to MB
(Add D3)



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	SWITCH,LED,KB,Finger,TP	3B
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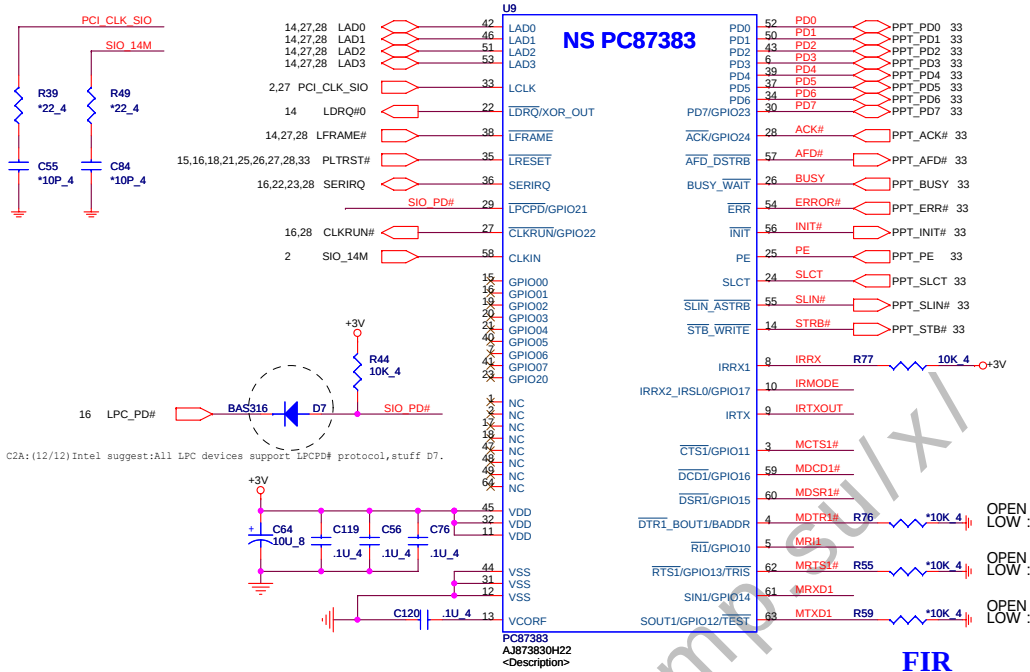
NS SIO PC87383



A1A:(9/20) PPT PU 4.7k circuit exist in Docking. remove it.

OPEN : 164Eh~164Fh
LOW : 2Eh~2Fh

OPEN : normal pin operation
LOW : float device pin

OPEN : normal Device operation
LOW : XOR pin tree

HOLE17 *h-c276d94p2

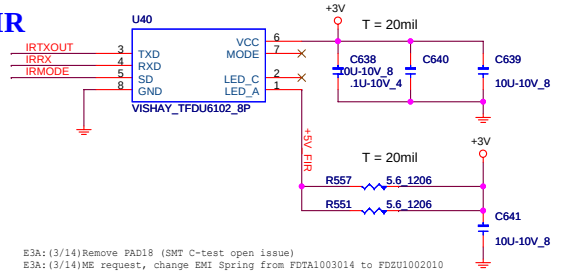
C2A:(12/28) change Hole17 type to improve thermal issue, (change footprint to H-C276D94N-4)

C2A:(12/12)Intel suggest:All LPC devices support LPCPD# protocol,stuff D7.

HOLE

HOLE28 HOLE26 HOLE29 HOLE27 *h-c236d236
HOLE35 HOLE32 HOLE33 HOLE31 *h-c236d236
HOLE37 HOLE38 HOLE34 HOLE36 *h-c236d236
HOLE22 HOLE14 h-c236d138p2
HOLE25 HOLE24 h-c217d59p2

FIR



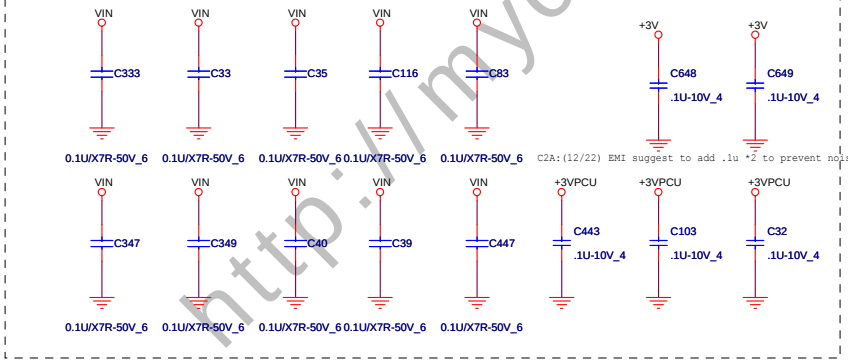
E3A:(3/14)Remove PAD18 (SMT C-test open issue)
E3A:(3/14)ME request, change EMI Spring from FDTA1003014 to FDZU1002010
D3A:(2/14)EMI request add two of clip(FDTA1003014) in PAD17 and PAD19 for EMI issue

PAD19 PAD17 EMIPAD EMIPAD157X79
PAD25 PAD24 PAD23 *EMIPAD EMIPAD157X79

C2A:(12/22) EMI suggest add three clip to contact with CPU cooler's fins (PAD23,24,25)

EMI Cap

A1A:(10/19) EMI suggest :Add the VIN power shape bypass cap 0.1uF x 10pcs
Add the +3VPCU power traces bypass cap 0.1uF x 3pcs



C2A:(12/22) EMI suggest to add .1u *2 to prevent noise (+3V)

HOLE42 *h-o110x94d110x94n Non - PTH Hole

B1C:(11/27)change Hole42 footprint
B1C:(11/23)remove Hole7
D3A:(2/8)Remove hole13

HOLE16 HOLE19 HOLE30 HOLE18 HOLE15 HOLE21 HOLE11 h-c217d122p2

C2A:(12/1) change Hole21 from MBZU1001010 to MBZU1004010

HOLE3 *H-C315D177P2
HOLE9 *h-c276d94p2
HOLE23 HOLE2 HOLE4 HOLE10 HOLE1 HOLE5 HOLE12 HOLE39 HOLE43 HOLE40 HOLE41 *h-c276d94p2
HOLE20 *h-c276i134d94p2
HOLE6 *h-c276d94p2
HOLE8 *h-C276D122P2

D3A:(2/2) change Hole9 footprint

C2A:(12/22) change Hole20 footprint to h-c276i134d94p2

ESDPad

PAD15 PAD5 PAD14 PAD11 PAD13 PAD3 PAD16 PAD10 PAD2 PAD7 PAD1 PAD4 PAD8 PAD12 PAD6 PAD9 *EMIPAD
ADOGND
EMIPAD142X91
PAD20 PAD21 PAD22 MEPAD

C2A:(12/22) Add theree PAD per ME request (fix wire)
D3A:(2/2) change PAD20.PAD21.PAD22 footprint
D3A:(2/12) Add PAD20.PAD21.PAD22 P/N (FDZU1001010)

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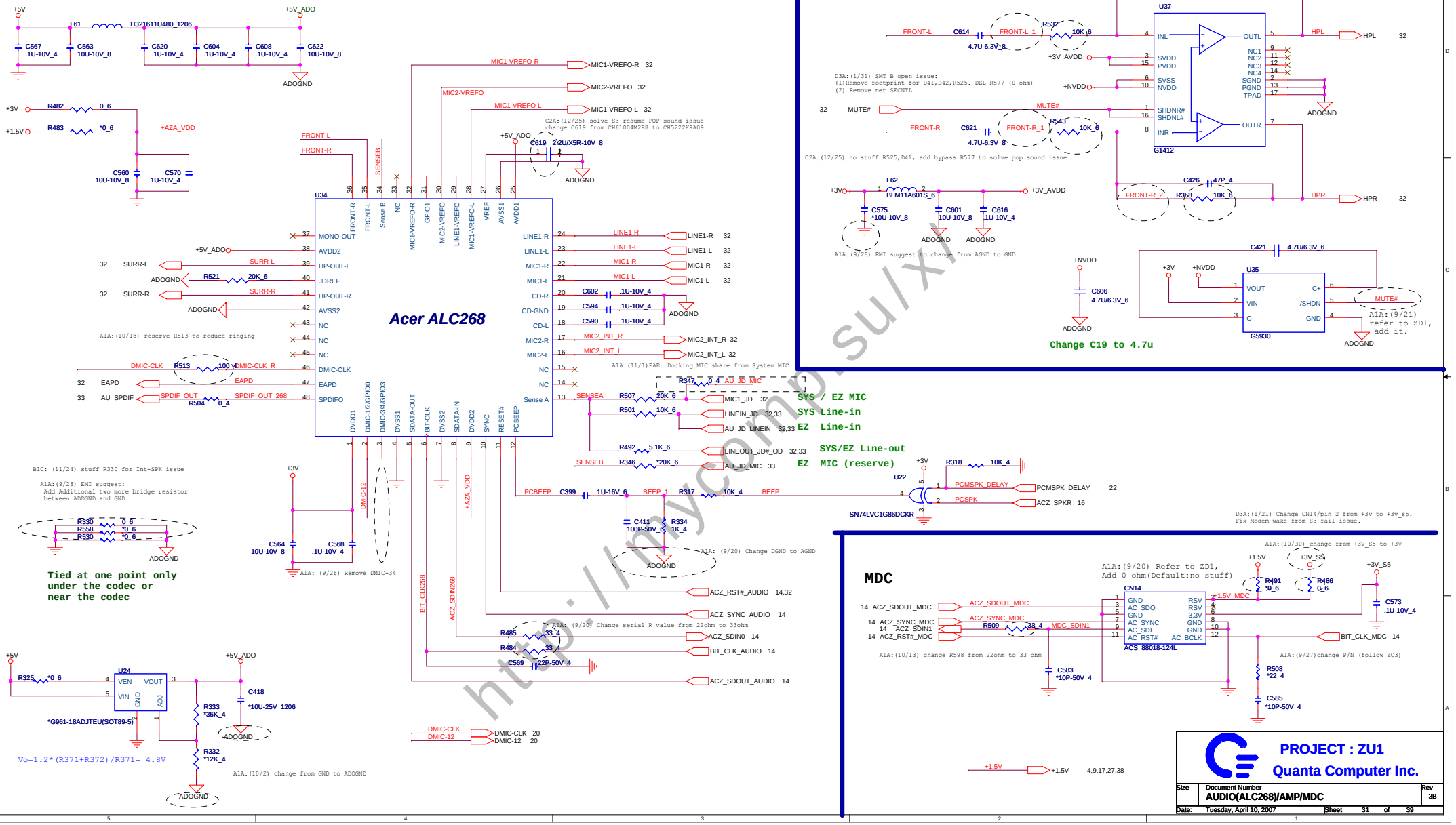
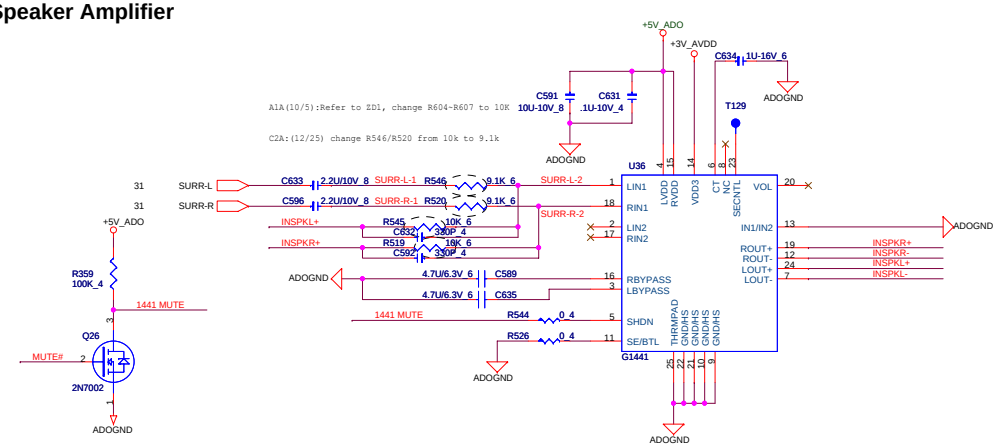
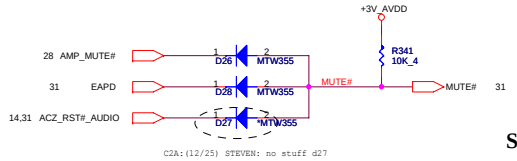
CODEC(ALC268)

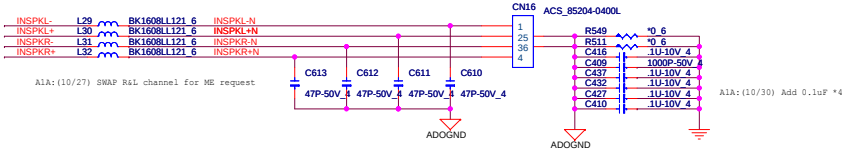


Speaker Amplifier

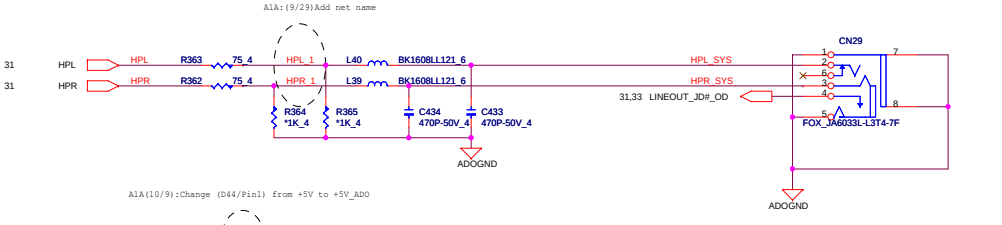




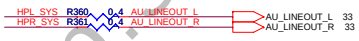
SPEAKER



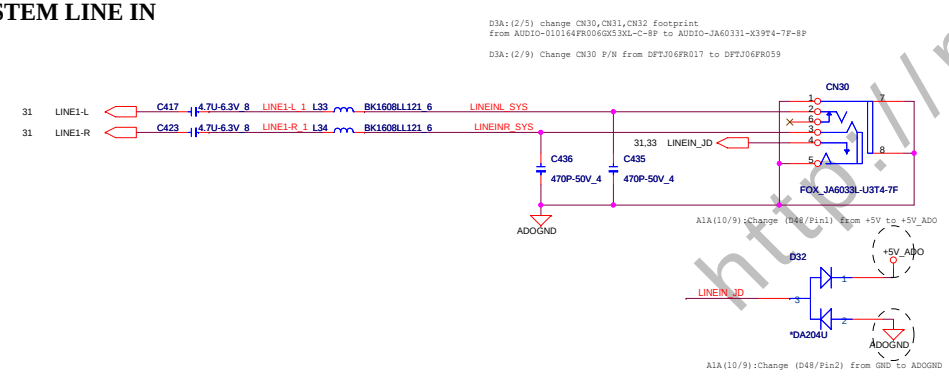
SYSTEM LINE OUT



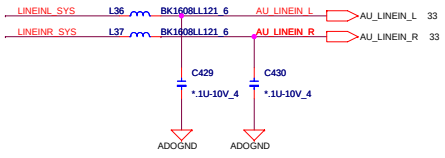
Docking LINE OUT/SPDIF



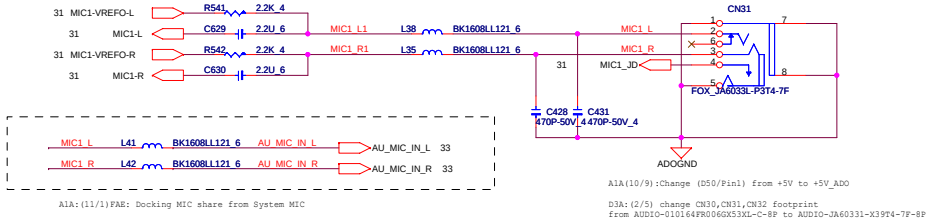
SYSTEM LINE IN



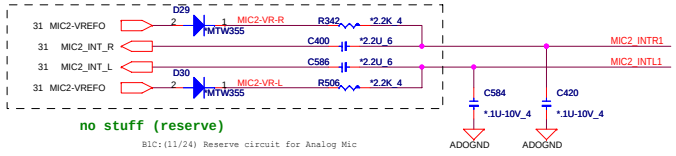
Docking LINE IN

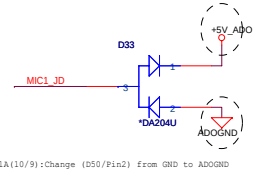


SYSTEM MIC



Analog MIC





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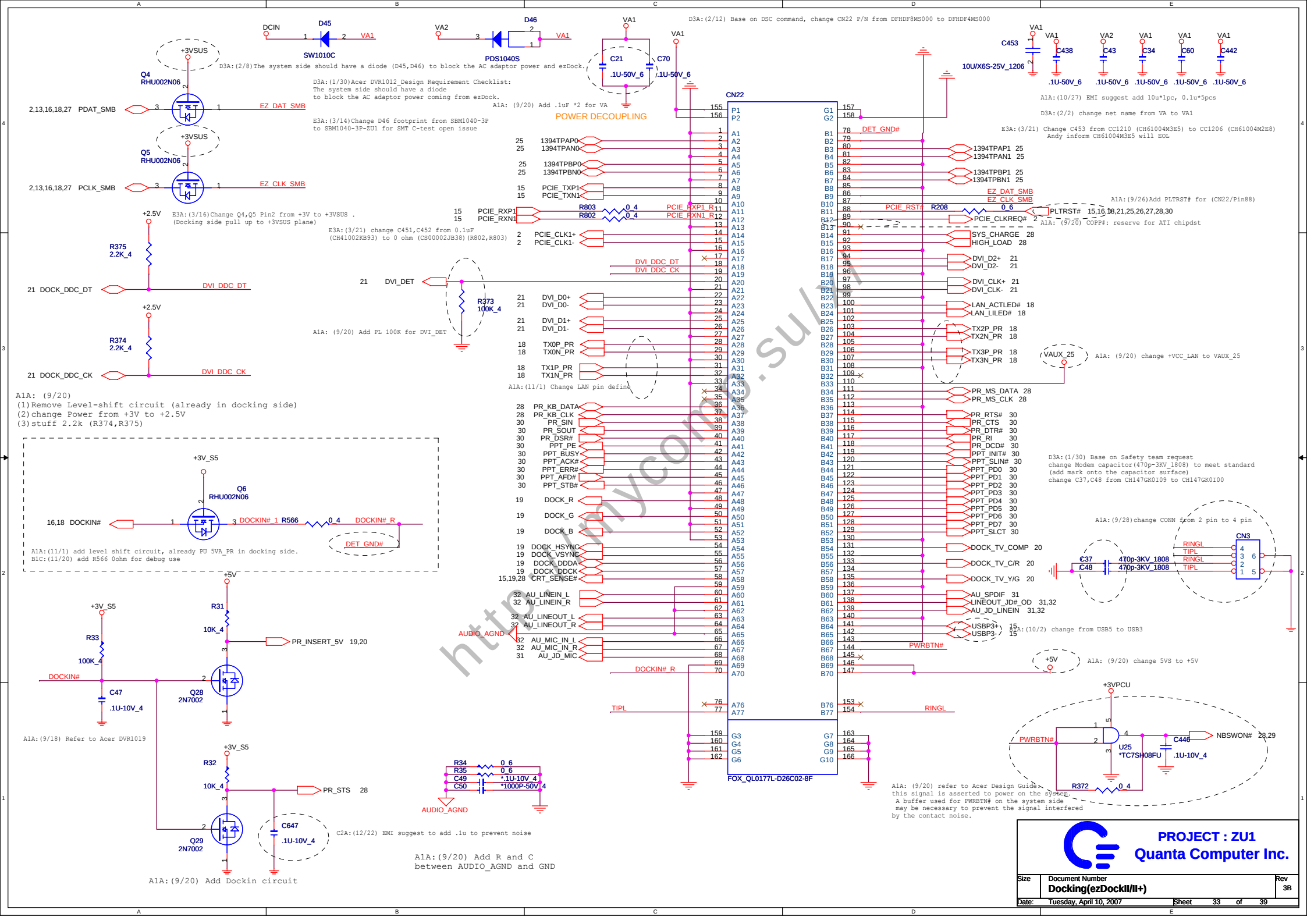
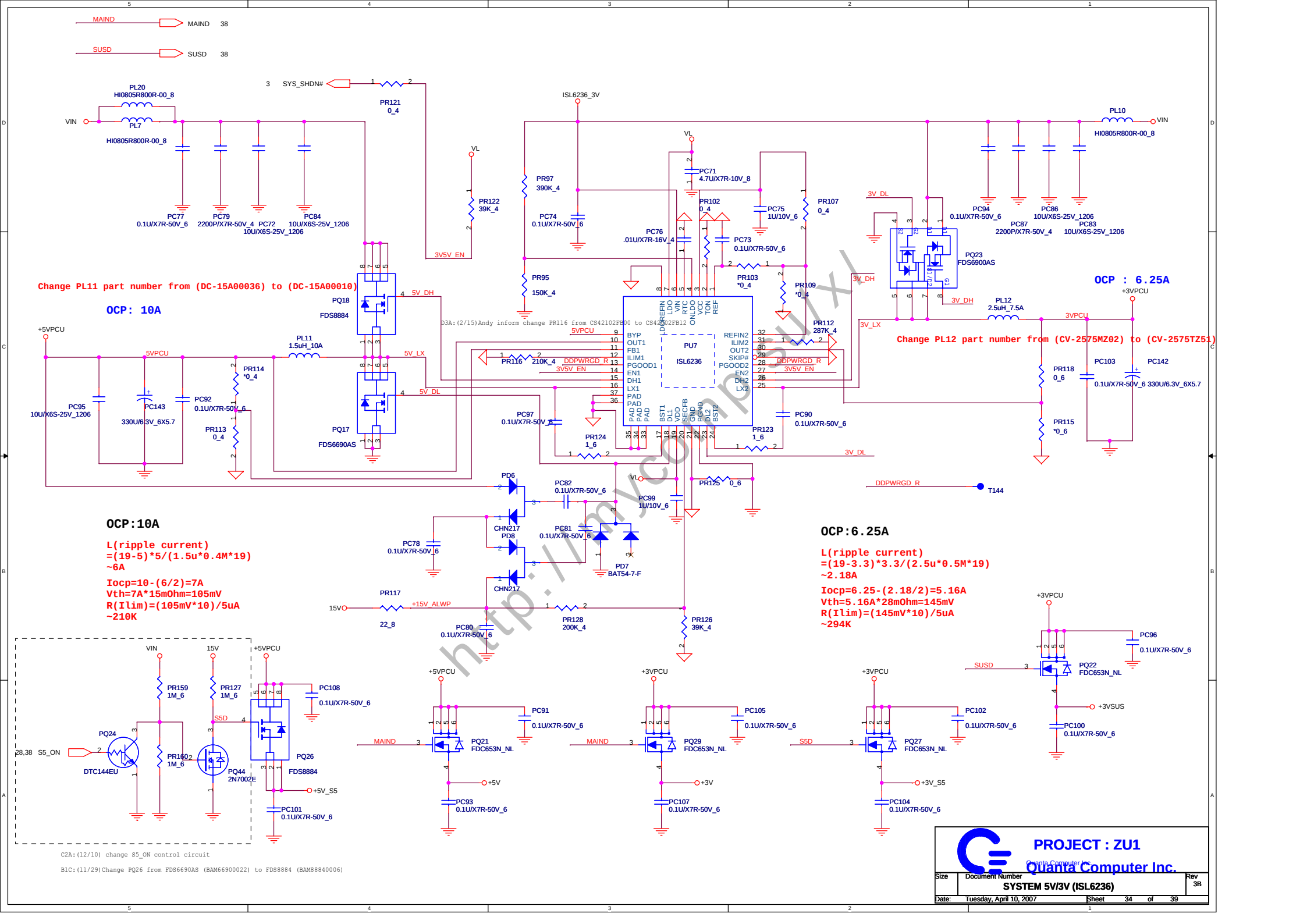
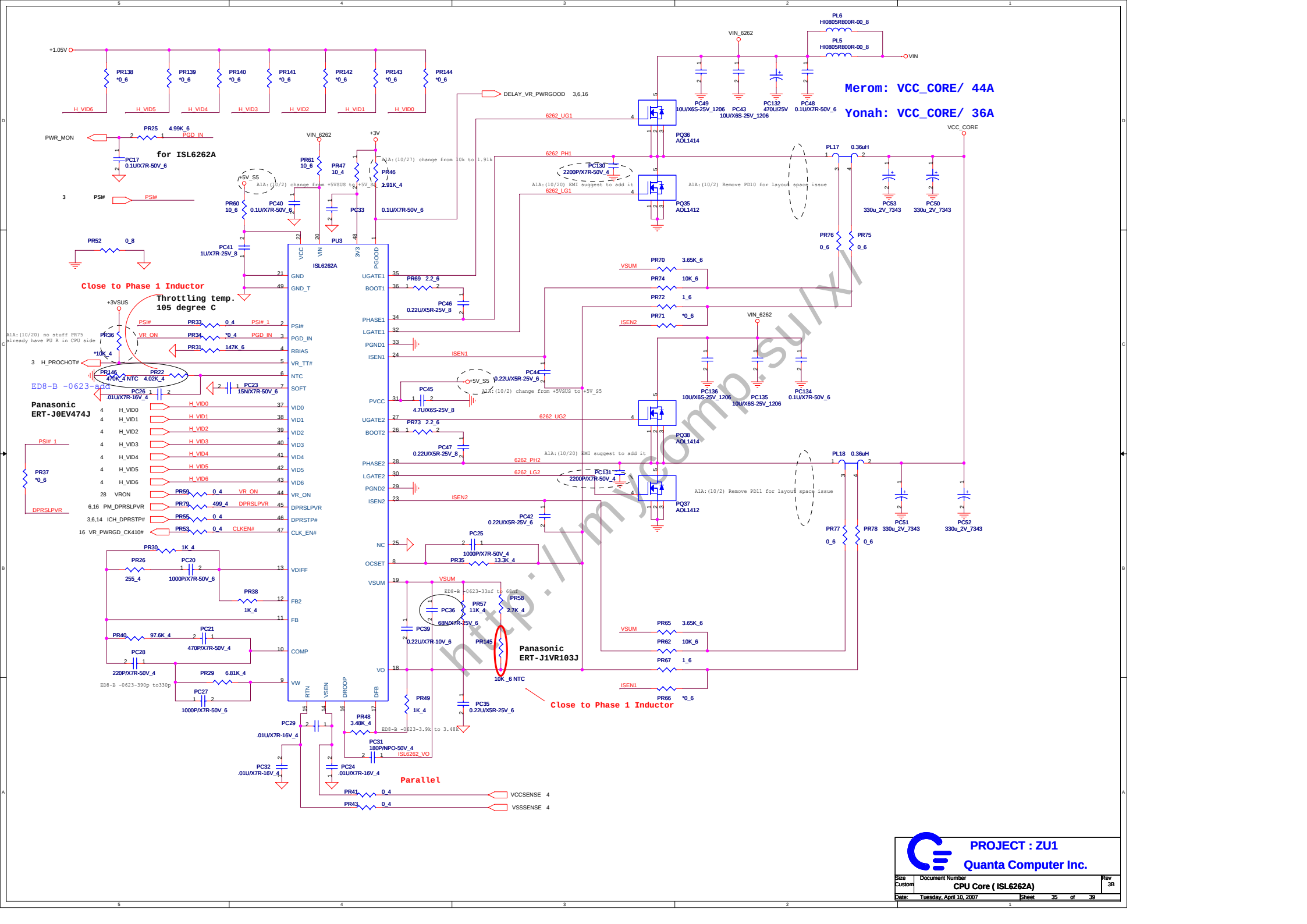
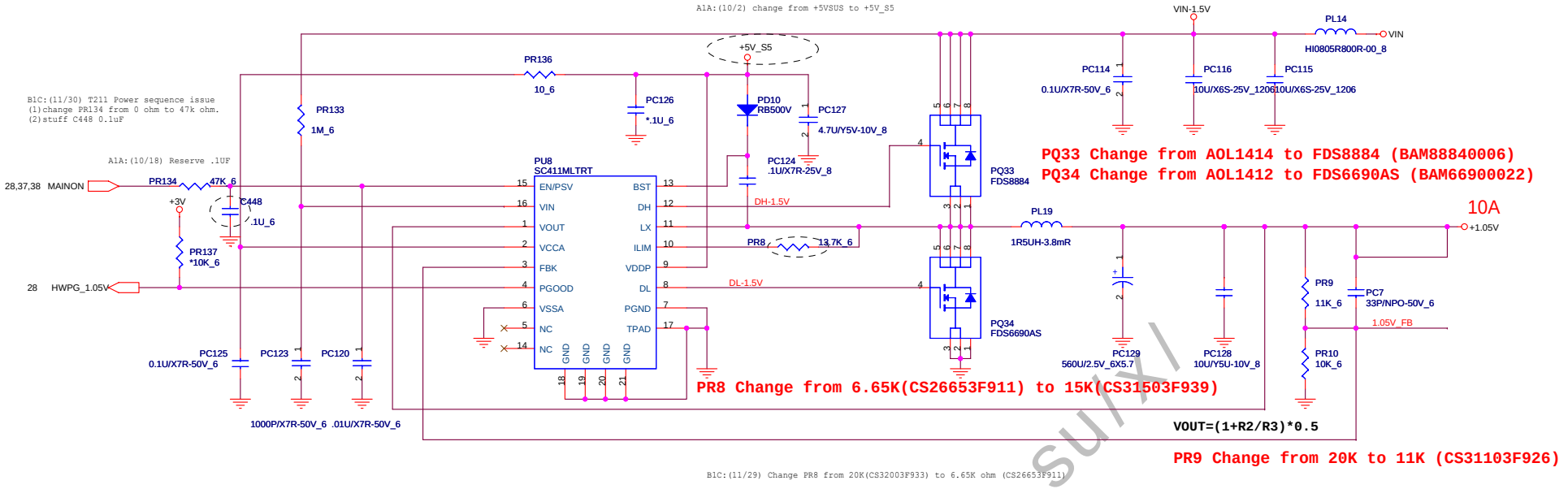


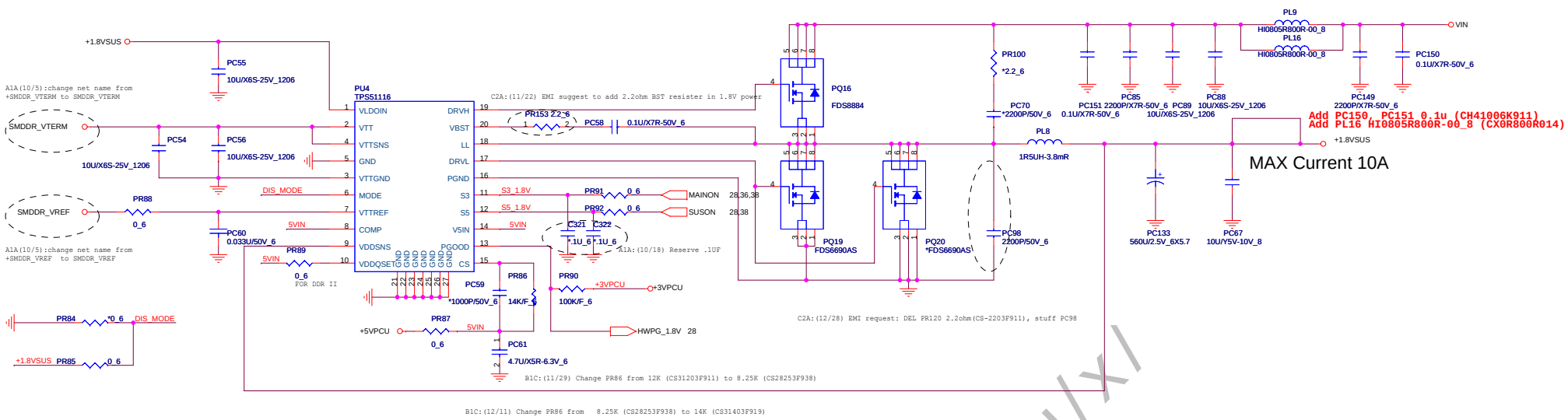

MAIND
MAIND 38
SUSD
SUSD 38
3 SYS_SHDN#
PR121 0_4
PL20 HI0805R800R-00_8
PL7 HI0805R800R-00_8
VIN
PC77 0.1U/X7R-50V_6
PC79 2200P/X7R-50V_4
PC72 10U/X6S-25V_1206
PC84 10U/X6S-25V_1206
VL
PR122 39K_4
3V5V_EN
ISL6236_3V
PR97 390K_4
PC74 0.1U/X7R-50V_6
PR95 150K_4
PC76 .01U/X7R-16V_4
PC71 4.7U/X7R-10V_8
PR102 0_4
PC75 1U/10V_6
PR107 0_4
PR103 *0_4
PR109 *0_4
PL10 HI0805R800R-00_8
PC94 0.1U/X7R-50V_6
PC87 2200P/X7R-50V_4
PC86 10U/X6S-25V_1206
PC83 10U/X6S-25V_1206
3V_DL
PQ23 FDS6900AS
3V_DH
PL12 2.5uH_7.5A
3VPCU
Change PL11 part number from (DC-15A00036) to (DC-15A00010)
OCP: 10A
OCP : 6.25A
Change PL12 part number from (CV-2575MZ02) to (CV-2575TZ51)
+5VPCU
+3VPCU
PQ18 FDS8884
PQ17 FDS6690AS
5V_DH
5V_LX
5V_DL
3V_LX
PL11 1.5uH_10A
PR114 *0_4
PR113 0_4
PC95 10U/X6S-25V_1206
PC143 330U/6.3V_6X5.7
PC92 0.1U/X7R-50V_6
D3A:(2/15)Andy inform change PR116 from CS42102FB00 to CS42102FB12
PU7 ISL6236
BYP OUT1 FB1 ILIM1 PGOOD1 EN1 DH1 LX1 PAD PAD PAD PAD
LDOREFIN LDO VIN RTC ONLDO VCC TON REF
REFIN2 ILIM2 OUT2 SKIP# PGOOD2 EN2 DH2 LX2
BST1 DL1 VDD SECFB GND PGND DL2 BST2
PR116 210K_4
DDPWRGD_R
PR112 287K_4
PC97 0.1U/X7R-50V_6
PR124 1_6
PC90 0.1U/X7R-50V_6
PR123 1_6
PR118 0_6
PR115 *0_6
PC103 0.1U/X7R-50V_6
PC142 330U/6.3V_6X5.7
PR125 0_6
T144
PD6
PC82 0.1U/X7R-50V_6
PC99 1U/10V_6
CHN217
PD8
PC81 0.1U/X7R-50V_6
PD7 BAT54-7-F
PC78 0.1U/X7R-50V_6
OCP:10A
L(ripple current)
=(19-5)*5/(1.5u*0.4M*19)
~6A
Iocp=10-(6/2)=7A
Vth=7A*15mOhm=105mV
R(Ilim)=(105mV*10)/5uA
~210K
OCP:6.25A
L(ripple current)
=(19-3.3)*3.3/(2.5u*0.5M*19)
~2.18A
Iocp=6.25-(2.18/2)=5.16A
Vth=5.16A*28mOhm=145mV
R(Ilim)=(145mV*10)/5uA
~294K
PR117 22_8
15V
+15V_ALWP
PC80 0.1U/X7R-50V_6
PR128 200K_4
PR126 39K_4
VIN
15V
PR159 1M_6
PR127 1M_6
S5D
PQ24 DTC144EU
PR160 1M_6
PQ44 2N7002E
28,38 S5_ON
PC108 0.1U/X7R-50V_6
PQ26 FDS8884
+5V_S5
PC101 0.1U/X7R-50V_6
MAIND
PQ21 FDC653N_NL
PC91 0.1U/X7R-50V_6
+5V
PC93 0.1U/X7R-50V_6
PQ29 FDC653N_NL
PC105 0.1U/X7R-50V_6
+3V
PC107 0.1U/X7R-50V_6
PQ27 FDC653N_NL
PC102 0.1U/X7R-50V_6
+3V_S5
PC104 0.1U/X7R-50V_6
SUSD
PQ22 FDC653N_NL
PC96 0.1U/X7R-50V_6
+3VSUS
PC100 0.1U/X7R-50V_6
C2A:(12/10) change S5_ON control circuit
B1C:(11/29)Change PQ26 from FDS6690AS (BAM66900022) to FDS8884 (BAM88840006)
http://mycompsu.x/
PROJECT : ZU1
Quanta Computer Inc.
Quanta Computer Inc.
Size
Document Number
SYSTEM 5V/3V (ISL6236)
Rev 3B
Date: Tuesday, April 10, 2007
Sheet 34 of 39


Merom: VCC_CORE/ 44A
Yonah: VCC_CORE/ 36A
for ISL6262A
Close to Phase 1 Inductor
Throttling temp.
105 degree C
Panasonic
ERT-J0EV474J
Panasonic
ERT-J1VR103J
Close to Phase 1 Inductor
Parallel
ISL6262A
PROJECT : ZU1
Quanta Computer Inc.
CPU Core (ISL6262A)
Tuesday, April 10, 2007
Sheet 35 of 39
http://mycomp.su/x/



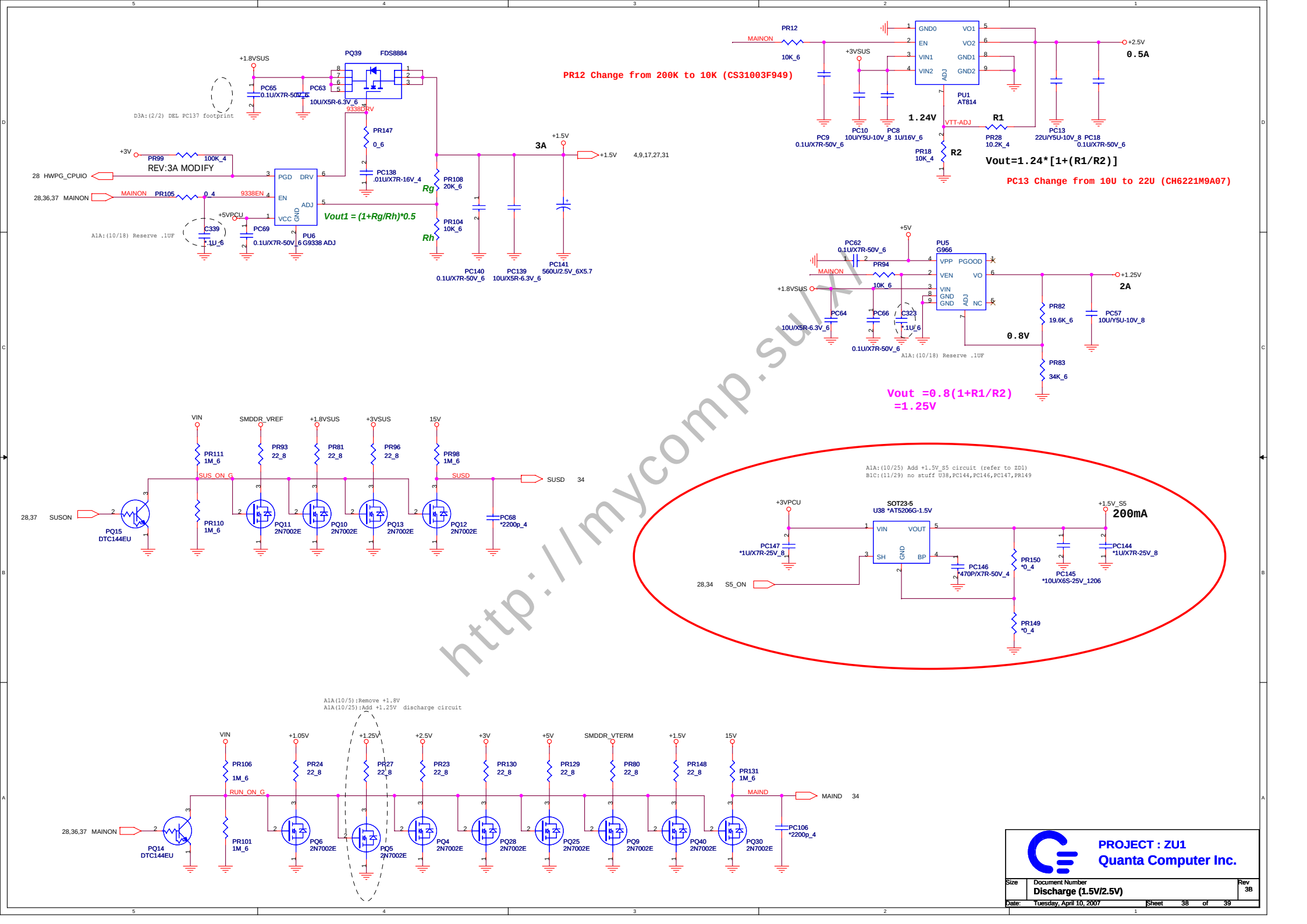
PROJECT : ZU1
Quanta Computer Inc.

Size	Document Number	Rev
	VTT 1.05V (SC411)	3B
Date: Tuesday, April 10, 2007	Sheet 36 of 39	



A1A(10/5):Remove +1.8V circuit

PROJECT : ZU1		
Quanta Computer Inc.		
Size	Document Number: DDR 1.8V(TPS51116)	Rev: 3B
Date: Tuesday, April 10, 2007	Sheet 37 of 39	


PR12 Change from 200K to 10K (CS31003F949)
PC13 Change from 10U to 22U (CH6221M9A07)
Vout1 = (1+Rg/Rh)*0.5
Vout=1.24*[1+(R1/R2)]
Vout =0.8(1+R1/R2)
=1.25V
A1A:(10/25) Add +1.5V_S5 circuit (refer to ZD1)
B1C:(11/29) no stuff U38,PC144,PC146,PC147,PR149
A1A(10/5):Remove +1.8V
A1A(10/25):Add +1.25V discharge circuit
REV:3A MODIFY
D3A:(2/2) DEL PC137 footprint
A1A:(10/18) Reserve .1UF
http://mycomp.su/x/
PROJECT : ZU1
Quanta Computer Inc.
Discharge (1.5V/2.5V)
Tuesday, April 10, 2007
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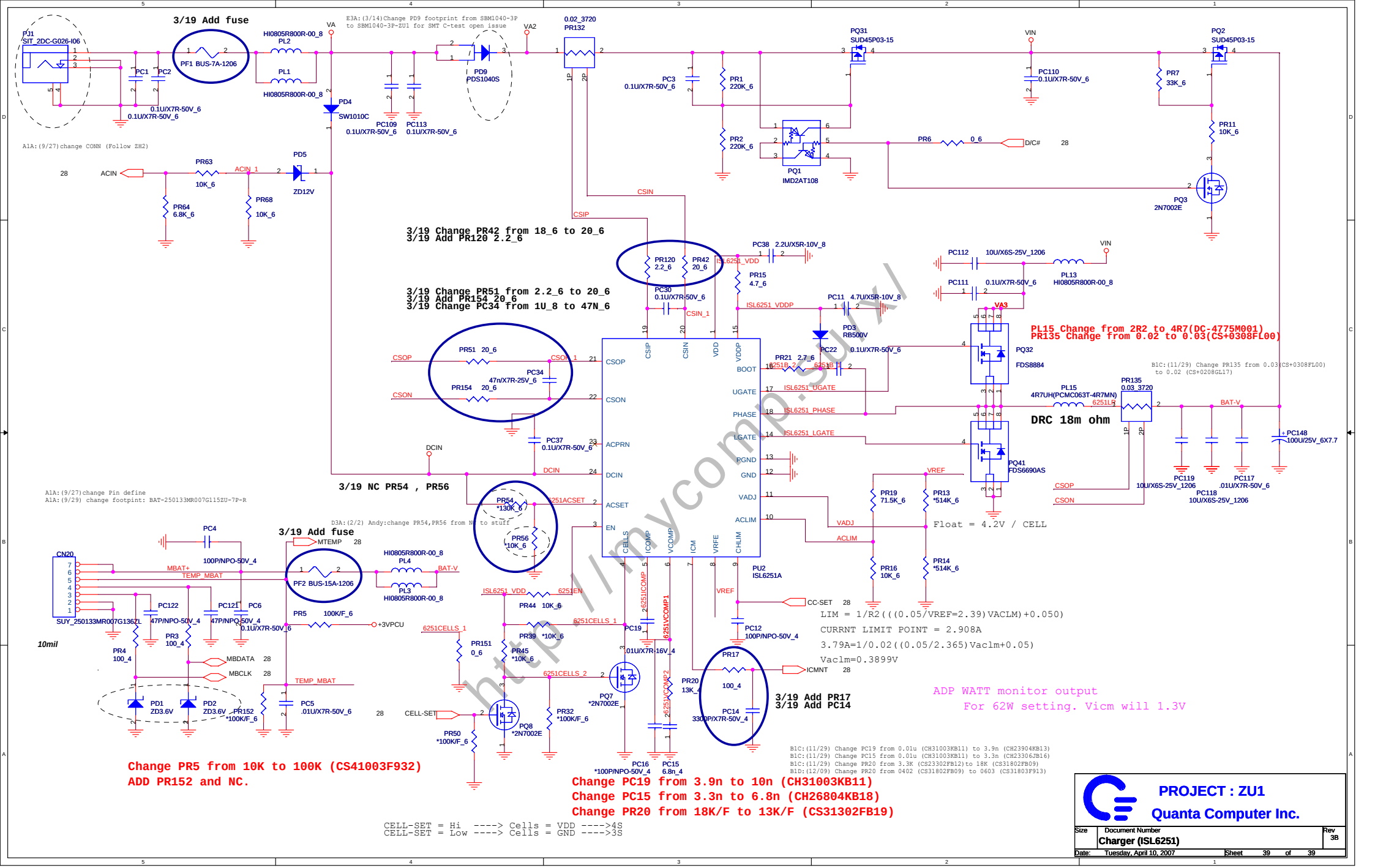
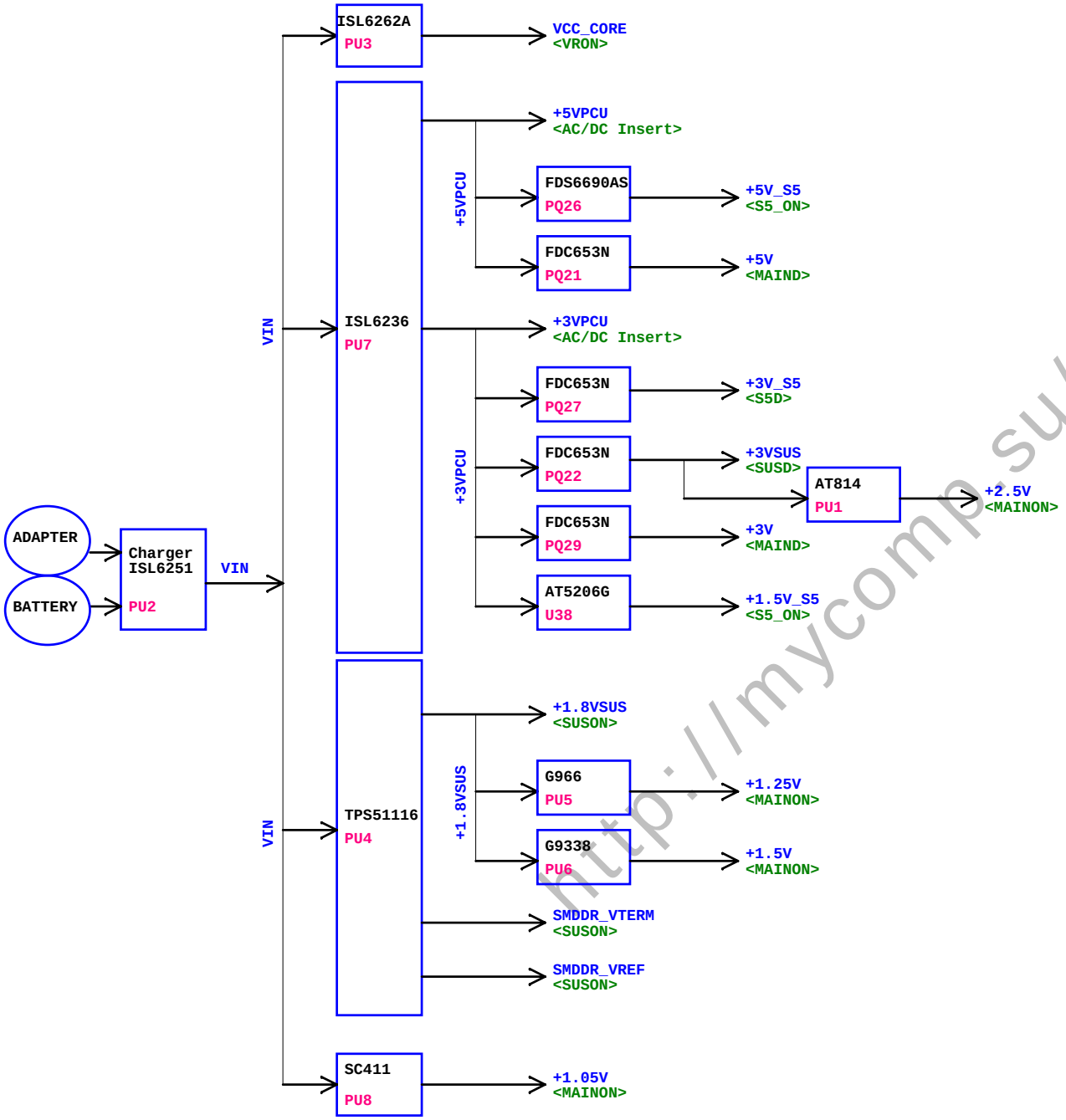
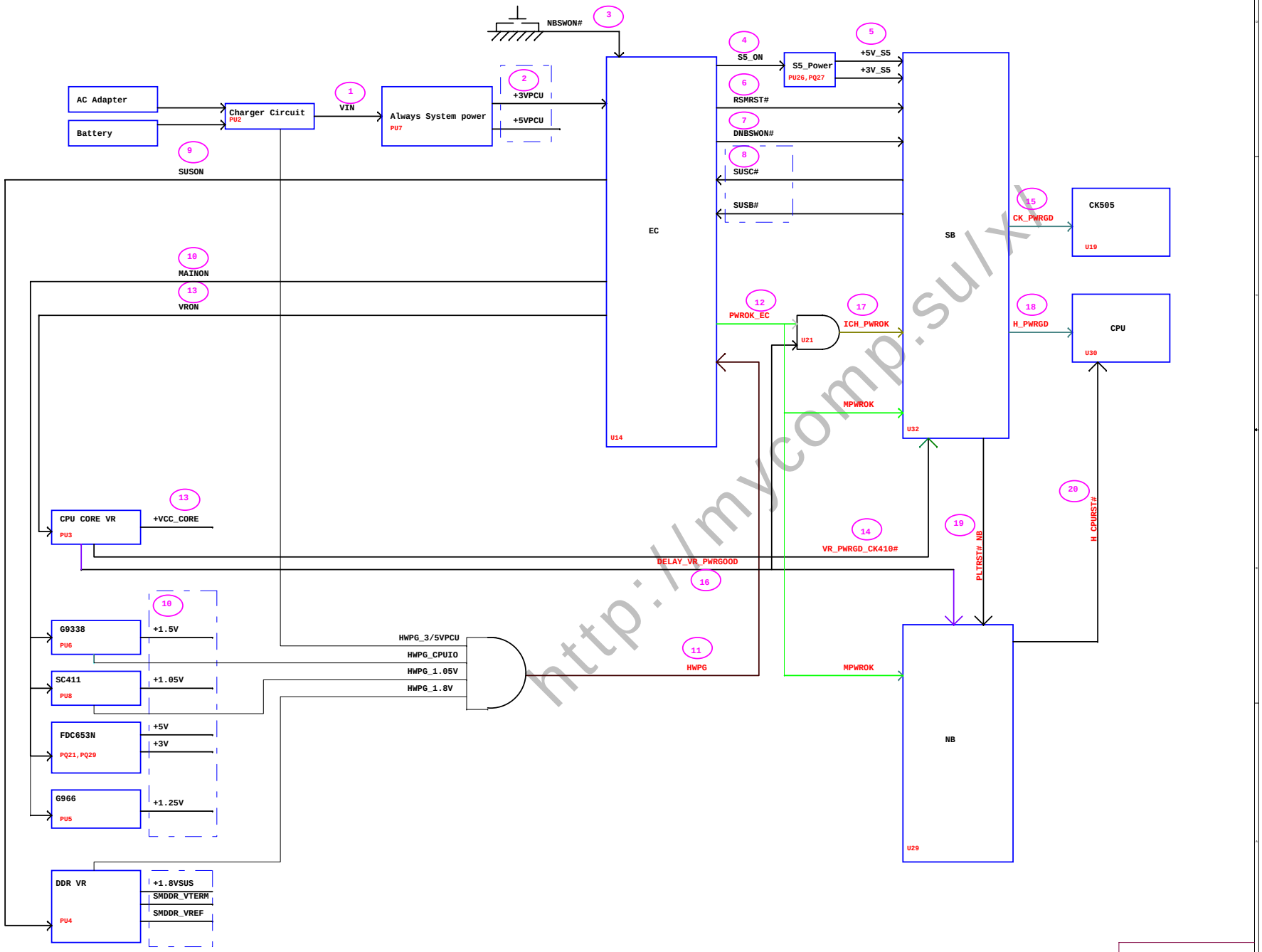

3/19 Add fuse
PF1 BUS-7A-1206
PF2 BUS-15A-1206
3/19 Change PR42 from 18_6 to 20_6
3/19 Add PR120 2.2_6
3/19 Change PR51 from 2.2_6 to 20_6
3/19 Add PR154 20_6
3/19 Change PC34 from 1U_8 to 47N_6
3/19 NC PR54 , PR56
3/19 Add fuse
3/19 Add PR17
3/19 Add PC14
PL15 Change from 2R2 to 4R7(DC-4775M001)
PR135 Change from 0.02 to 0.03(CS+0308FL00)
DRC 18m ohm
Float = 4.2V / CELL
LIM = 1/R2(((0.05/VREF=2.39)VACLM)+0.050)
CURRNT LIMIT POINT = 2.908A
3.79A=1/0.02((0.05/2.365)Vaclm+0.05)
Vaclm=0.3899V
ADP WATT monitor output
For 62W setting. Vicm will 1.3V
Change PR5 from 10K to 100K (CS41003F932)
ADD PR152 and NC.
Change PC19 from 3.9n to 10n (CH31003KB11)
Change PC15 from 3.3n to 6.8n (CH26804KB18)
Change PR20 from 18K/F to 13K/F (CS31302FB19)
CELL-SET = Hi ----> Cells = VDD ----->4S
CELL-SET = Low ----> Cells = GND ----->3S
PROJECT : ZU1
Quanta Computer Inc.
Charger (ISL6251)
Tuesday, April 10, 2007



ZU1 Power Table

SLP_S3#(SUSB#):
Control non-critical power plane when system into S3(Suspend to RAM)/S4(Suspend to Disk)/S5(Soft off).

SLP_S4#(SUSC#):
Control non-critical power plane when system into S4(Suspend to Disk)/S5(Soft off).Used to control DRAM power



Item:	Fixed Issue	Modify List:	Schematic Rev.	Page
1	CPU Clock select issue	Stuff R179,R198,R447 for CPU Clock select issue	A1A	2
2	PCI Clock issue	change R186 value from 33ohm to 22 ohm (refer to Intel check list 1.301)	A1A	2
3	CK505 issue	ICS FAE suggest to change C542,C287 from 4.7u to 10u	A1A	2
4	EMI issue	EMI suggest to reserve R436,R199,R444 for EMI test	A1A	2
5	CK505 issue	Add PCIE_CLKREQ# PU to +3v	A1A	2
6	CK505 issue	SWAP SRC3 and SRC9	A1A	2
7	CK505 issue	Add PCIE_CLKREQ# PU to +3v	A1A	2
8	CK505 issue	Remove U19/Pin48 (no use)	A1A	2
9	CK505 issue	Add PCIE_CLKREQ# PU to +3v	A1A	2
10	CK505 issue	remove SATACLKREQ function, change R188 value from 475ohm to 22 ohm	A1A	2
11	CK505 issue	FAE : (14M_ICH and SIO_14M) signals trace should be equal length	A1A	3
12	CPU issue	Remove XDP/ITP signals (no use)	A1A	3
13	CPU issue	Retain the termination resistors (R157,R150~R152) on these signals even when ITP700 not implemented.	A1A	3
14	Thermal Trip issue	change Q19/Pin3 net name from THERM_SYS_PWR to SYS_SHDN#	A1A	3
15	CPU FAN issue	change CPU FAN CONN (follow ZC3)	A1A	3
16	CPU FAN issue	Add CPUFAN#_ON to (U28/PIN1)	A1A	3
17	CPU FAN issue	Add Diode D39 and PU +5V for (U28/Pin1)	A1A	3
18	CPU Thermal monitor issue	Add (U27/Pin6) PU to 3V	A1A	3
19	CPU Thermal monitor issue	remove R389, already PU in ICH8	A1A	3
20	CPU Thermal monitor issue	change SMBUS from MBCLK/MNDATA to 2ND_MBCLK/2ND_MBDATA (Q30,Q31)	A1A	3
21	CPU Power issue	stuff C198, unstuff C217 (base on layout location)	A1A	4
22	GMCH Power issue	Short R115~R117,change +VCC_CFXCORE_INT to +1.05V	A1A	8
23	GMCH Power issue	Short R122,R138, remove VCC_RXR_DMI circuit (connect to +VCC_PEG directly)	A1A	9
24	GMCH Power issue	INTEL CRB VCCD_QDAC Filter Modification:change L13 to R125(100ohm), change R145(*0 ohm) to C507(1uF)	A1A	9
25	DDR Power issue	stuff R192, no stuff R191,R193 for SMDDR_VREF_DIMM	A1A	13
26	RTC BAT issue	Change RTC BATTERY CONN CN12(follow to ZC3)	A1A	14
27	ICH8-M Strap issue	Stuff R241, no stuff R266 (Disable Internal VR powering VccLAN1_05, VccCL1_05)	A1A	14
28	ICH8-M HDA issue	add R283,R465,R463,R267 for MDC module (base on Intel Design Giude)	A1A	14
29	ICH8-M issue	PU RCIN# to +3V	A1A	14
30	ICH8-M issue	Remove ICH8-M GLAN/SATA1/SATA2 circuit (no use)	A1A	14
31	ICH8-M issue	change net name (U31/Pin2) from VR_PWRGD_CLKEN# to VR_PWRGD_CK410#	A1A	16
32	ICH8-M issue	Remove SATACLKREQ#(U32/Pin:AG13),RI# (U32/Pin:AF17) ;{no use}	A1A	16
33	ICH8-M issue	no support iAMT, remove SMB_CLK_ME,SMB_DATA_ME	A1A	16
34	ICH8-M issue	change DOCKIN#_ICH_R PU from +3V to +3V_S5	A1A	16

PROJECT : ZU1 Quanta Computer Inc.	PROJECT : ZU1	APPROVE BY : James Lu	DRAWING BY:Barry Lee	Stage: A1
	MB ASSY'S P/N : 31ZU1MB0000	PROJECT LEADER:Jack Wu	DOCUMENT NO:	DATE :2006/12/09

CHANGE LIST SHEET 1

Item:	Fixed Issue	Modify List:	Schematic Rev.	Page
35	Power sequence issue	change (U21/Pin5) from +3V to +3VSUS (refer to ZC1)	A1A	16
36	ICH8-M issue	Remove WOL_EN (U32/Pin:AG19) -no use	A1A	16
37	ICH8-M issue	Remove SUSM# (used to control power planes to the Intel AMT sub-system)	A1A	16
38	ICH8-M issue	Remove (1)ME_EC_ALERT# (2)EC_ME_ALERT (no use)	A1A	16
39	ICH8-M issue	connect LAN_RST#(U32/Pin:AH20) to PLTRST# (If no use internal LAN MAC connect LAN_RST# to PLTRST#)	A1A	16
40	ICH8-M issue	change DOCKIN#_ICH_R PU from +3V to +3V_S5	A1A	16
41	EMI issue	EMI suggest C373 from 0.1u to 10uF	A1A	17
42	ICH8-M Power issue	Reserve R308,R313 for +1.5V MDC module	A1A	17
43	LAN Power issue	change LAN power from +3V_LAN_S5 to +3V_S5	A1A	18
44	LAN Power issue	BCM FAE: Pull up Vmainprsnt (U10/Pin53) to the system main power (3.3v), but not the standby power	A1A	18
45	LAN Power issue	BCM FAE: Change capacitance value from 47-uF to 10-uF.	A1A	18
46	LAN Power issue	BCM FAE:stuff R30,no stuff R47(in order to pull up C90,C86 and Q16/pin 3 to 3V_LAN rail)	A1A	18
47	LAN Switch issue	EMI suggest C59 from 0.1u to 10uF	A1A	18
48	LAN Switch issue	Add Diode D4 for isolation (Dockin#)	A1A	18
49	LAN Switch issue	change LAN Switch from MAX4892 to PI3L500	A1A	18
50	LAN Transformer issue	change TRANSFORMER GND(U3/Pin15,18,21,24) to MGND	A1A	18
51	LAN CONN issue	Change CONN P/N (follow ZC1)	A1A	18
52	LAN CONN issue	change CONN GND(CN19/Pin13,14) to MGND	A1A	18
53	CRT issue	change C439, C440,C7,C441 to 30~50pF(default :no stuff)	A1A	19
54	CRT issue	Change CRT_SENSE# from CRT CONN Pin11 to Pin5 (follow Acer define)	A1A	19
55	CRT issue	Change CRT CONN P/N(follow ZC1)	A1A	19
56	CRT issue	change R16,R17 from 2.7k to 2.2k ; R10,R12 from 39 to 0 ohm	A1A	19
57	CRT issue	change U1 from CM2009 to IP4772	A1A	19
58	LVDS issue	change CCD function from USB7 to USB8	A1A	20
59	LVDS issue	Change C12 from CH6102M9900 to CH61004M3E5 (refer to ZC3)	A1A	20
60	TV issue	Change CN17 CONN P/N (follow ZC1)	A1A	20
61	SDVO issue	Change R51,R56 value from 2.2k to 4.7k (FAE suggest R value from 4K~9K)	A1A	21
62	PCMCIA issue	refer to BL3. Add G_RST# circuit.	A1A	22
63	PCMCIA issue	FAE suggest R189's value under 47 ohm.	A1A	22
64	Card reader issue	no stuff R496,R522	A1A	23
65	Card reader issue	FAE suggest R503's value under 47 ohm.	A1A	23
66	Card reader issue	Remove U39/Pin99, no use (XMDAT4B is for 8 bit MMC,remove it.)	A1A	23
67	Card reader issue	Change C593 from 0.1u to 10uF,EMI suggest add C587 0.1uF	A1A	24
68	PCMCIA issue	change PCMCIA CONN (follow BH1)	A1A	24

Item:	Fixed Issue	Modify List:	Schematic Rev.	Page
69	PATA ODD issue	change R253 from 0 to 33ohm	A1A	26
70	PATA ODD issue	Add C326,C327,C344 for +5V	A1A	26
71	PATA ODD issue	Remove D23, already add in page29	A1A	26
72	Mini Card issue	Reserve R349,R350,R337,R345,R344,R338,R339 for debug card use	A1A	27
73	Mini Card issue	Add (CN28/Pin39,41) to +3V_WL_VDD (follow ZO1)	A1A	27
74	Mini Card issue	Remove (CN28/Pin36,38) USB circuit	A1A	27
75	Mini Card issue	Remove (CN28/Pin46) BT LED	A1A	27
76	Mini Card issue	Remove 0.1uF (CN28/Pin23,25), already in WL module	A1A	27
77	Bluetooth issue	SI suggest to remove 22pF*2 (CN5/Pin3,4)	A1A	27
78	USB CONN issue	SI suggest to remove 22pF*2 (CN11/Pin2,3)	A1A	27
79	EC issue	Change EC from WPC8769 to WPC8763	A1A	28
80	EC issue	change U7/Pin5,6 from MBCLK/MNDATA to 2ND_MBCLK/2ND_MBDATA	A1A	28
81	EC issue	Remove ME_EC_ALERT#	A1A	28
82	EC issue	FAE:Change U14/Pin80 from +3VPCU to +A3VPCU	A1A	28
83	EC issue	change C130,C131 from 6.8p to 5.6p	A1A	28
84	EC issue	Add D18 for HWPG_CPUIO	A1A	28
85	Finger Printer issue	SI suggest to remove 22pF*2 (CN9/Pin2,3)	A1A	29
86	SuperIO issue	Remove PPT PU 4.7K circuit (already in docking)	A1A	30
87	Audio issue	Change Serial resister R484,R485 value from 22 ohm to 33 ohm	A1A	31
88	Audio issue	reserve R513 to reduce ringing	A1A	31
89	Audio issue	Refer to ZD1, change R546,R520,R545,R519 to 10k	A1A	32
90	Docking issue	(CN22/Pin18,Pin19):(1)Remove Level-shift circuit (2)change Power from +3V to +2.5V (3)stuff 2.2k	A1A	33
91	Docking Power issue	Add .1u*7 , 10U*1 for VA	A1A	33
92	Docking issue	Reserve U25 for docking PWRBTN#	A1A	33
93	Docking issue	Change Docking Pin141/142 from USB5 to USB3	A1A	33
94	Docking issue	PL DVI_DET 100k to GMD (CN22/Pin20)	A1A	33
95	Docking issue	Change LAN pin define	A1A	33
96	Audio issue	Change CN29,CN30,CN31 P/N (Base on Acer request)	A1B	32
97	ICH8-M Strap issue	Change INTVRMEN from PD to PU	B1C	14
98	Leakage issue	add D43,D44 to stop leakage from EC to SB	B1C	16
99	ICH8-M issue	change DOCKIN# from GPIO7 to GPIO12	B1C	16
100	Power sequence issue	short PWROK_EC to MPWROK	B1C	16
101	ICH8-M issue	PU GPIO10 to +3V, PD GPIO14 to GND	B1C	16
102	ICH8-M issue	remove R229,R233,C355	B1C	16

Item:	Fixed Issue	Modify List:	Schematic Rev.	Page
103	PCMCIA issue	Reserve R572 for debug use	B1C	22
104	1394 issue	Change R271,R306,R307 from 56.2 to 5.1k ohm (fix 1394 can't detect issue)	B1C	25
105	Mini Card issue	no stuff R353,R348,R356	B1C	27
106	Mini Card issue	need support BCM WL Module, Connect CN28/Pin40 to GND	B1C	27
107	EC issue	SWAP GPIO1 and GPIO3	B1C	28
108	EC issue	Change CN10/Pin1 from +3V to +3VPCU	B1C	28
109	LED issue	Base on Me request, change PWR/SUS/BAT LED type	B1C	29
110	Audio issue	Stuff R330 to fix Internal SPK issue (floating GND issue)	B1C	27
111	Docking issue	Add R566 for Debug use	B1C	33
112	Mini Card issue	ME request :change CN28 P/N from DFHD52MS049 to DFHS52FR082 (9.0mm to 9.9mm)	B1D	27
113	GMCH Power issue	Change C143 from CH71002MJC8 to CH7102MT804 (Z-limit issue,H2.9mm to H1.5mm)	B1D	9
114	CPU Clock issue	Set CPU Frequency to auto selection (no stuff R179,R198,R447)	C2A	2
115	S5_ON issue	Change S5_ON control circuit (follow ZO1/ZD1)	C2A	34
116	CK505 issue	change CK505 VDD_IO from +1.05V to +1.25V. Because VDD_IO will drop out when high loading	C2A	2
117	G995 issue	Add level shift circuit (follow ZO1), remove D39,no stuff R383.	C2A	3
118	BIOS EMI issue	FAE suggest add 22 Ohm dumping resistors R596,R597 to avoid potential EMI problem	C2A	28
119	LAN issue	Base on BCM IEEE test result, change RDAC value (R42) from 1.24k to 1.18k	C2A	18
120	Audio issue	Acer change internal Mic solution to Fortemedia,Remove CN33,D29,D30,R342,R506,C400,C586	C2A	32
121	DVI Detect issue	Intel suggest:Add hotplug circuit to DVI_DET (follow ZC1)	C2A	21
122	ICH8M issue	Intel Suggest :ICH8M CPIO20 should not be pulled HIGH.Remove BOARD_ID3 circuit(remove R474,R475)	C2A	16
123	SDVO issue	Intel Suggest :Follow Intel New Guideline(MoW 48 update) Change R51,R56 from 4.7K to 3.9K ohm	C2A	21
124	GMCH Power issue	Change Crestline VCC_AXM to 1.25V, reference to SR ww48 MoW.reserved 0 ohm resister (R576)	C2A	8
125	SuperIO issue	Intel Suggest :All LPC devices support LPCPD# protocol, stuff D7	C2A	30
126	ICH8M issue	no stuff R259 to prevent leakage issue	C2A	16
127	EMI issue	EMI suggest add C647 to prevent noise for PR_STS	C2A	33
128	EMI issue	EMI suggest to add .1u *2 to prevent noise (+3V)	C2A	30
129	EMI issue	EMI suggest to add 2.2ohm BST resister (PR153) in 1.8V power	C2A	37
130	EMI issue	EMI suggest add three clip to contact with CPU cooler's fins (PAD23,24,25)	C2A	30
131	ME issue	ME request add three pad for fix wire (PAD20,21,22)	C2A	30
132	DVI issue	remove the U11,R57,R52,C109 to save layout space.	C2A	21
133	Power monitor issue	D16 not necessary if 3V/5V fail, EC can't work.	C2A	28
134	S3 resume POP sound issue	change C619 from CH61004M2E8 to CH5222K9A09 to solve S3 resume POP sound issue	C2A	31
135	POP sound issue	no stuff R525,D41, add bypass R577 to solve pop sound issue	C2A	31
136	AUDIO issue	no stuff D27	C2A	32

Item:	Fixed Issue	Modify List:	Schematic Rev.	Page
137	Audio issue	change R546/R520 from 10k to 9.1k	C2A	32
138	GMCH POWER issue	Change Crestline VCC_AXM from +1.25V to +1.05V, reserved 0 ohm resister (R578)	C2A	8
139	XTAL issue	Base on vendor-FCE suggestion, change C580/C579 from CH01206JB05 (12p) to CH02206JB08 (22p)	C2A	25
140	XTAL issue	Base on vendor-FCE suggestion, change C310/C299 from CH03306JBD7 (33p) to CH02706JB06 (27p)	C2A	2
141	XTAL issue	Base on vendor-FCE suggestion, change C130/C131 from CH-5606TB01 (5.6p) to CH01006JBD1 (10p)	C2A	28
142	EMI issue	EMI request: DEL PR120 2.2ohm(CS-2203F911), stuff PC98	C2A	37
143	EMI issue	EMI request: reserve .1U for (CN19/pin9,10)	C2A	18
144	EMI issue	EMI request: reserve L-C footprint for debug use (R52,C650)	C2A	20
145	debug issue	Stuff R349 , R350 for debug use	D3A	27
146	Modem wake from S3 fail issue	Change CN14/pin 2 from +3v to +3v_s5.	D3A	31
147	CableSence circuit issue	Add CableSence circuit (unstuff R78)	D3A	18
148	CableSence circuit issue	Add CableSence circuit (reserve R579)	D3A	18
149	LED type issue	Base on SMT-ME request, change LED type to 2 in 1,DEL LED4,LED5,LED6,LED7,R570,R571,Add LED2,LED3	D3A	29
150	SW button issue	Base on ASSEMBLY -Line request, remove SW1, add G2 footprint	D3A	29
151	change Modem capacitor to meet safety standard	change C37,C48 from CH147GK0I09 to CH147GK0I00	D3A	33
152	Power issue	The system side should have a diode (D45,D46) to block the AC adaptor power and ezDock.	D3A	33
153	EMI issue	Change L4,L5,L6 from CX8BA220007 to CX8BA470003	D3A	19
154	DVI issue	remove U13,R68,R75,R73,C98 for layout space issue	D3A	21
155	ASF issue	Connect SMLINK0 to SMBCLK and SMLINK1 to SMBDATA (Add R474,R475 for debug use)	D3A	16
156	SMT B open issue	(1)Remove footprint for D41,D42,R525. DEL R577 (0 ohm) (2) Remove net SECNTL	D3A	31
157	CableSence circuit issue	change LAN Low power pin from GPIO47 to GPIO52	D3A	28
158	LAN switch issue	Change U6 from AL000500005 to AL000500030 (change to 8KV solution)	D3A	18
159	Change 965GM from ES sample to QS sample	Change U29 P/N from AJ0QN120T37 to AJ0QP200T09	D3A	5~11
160	Change ICH8M from ES sample to QS sample	Change U32 from AJ0QM740T31 to AJ0QN230T10	D3A	14~17
161	Audio Jack issue	change CN30,CN31,CN32 footprint from AUDIO-010164FR006GX53XL-C-8P to AUDIO-JA60331-X39T4-7F-8P	D3A	32
162	docking sometimes can't detect DVI device issue	change R51,R56 from 3.9k(CS23902FB14) to 4.7k(CS24702JB38).	D3A	21
163	EMI issue	EMI suggest, add common Choke, co-lay R795,R796	D3A	27
164	Audio Jack issue	Change CN30 P/N from DFTJ06FR017 to DFTJ06FR059	D3A	32
165	Audio Jack issue	Change CN29 P/N from DFTJ06FR019 to DFTJ06FR061	D3A	32
166	Audio Jack issue	Change CN31 P/N from DFTJ06FR018 to DFTJ06FR060	D3A	32
167	backlight control issue	Follow ZO1 design,Remove R24 footprint, DEL D3(BC000316Z07).Add R73,Q36,Q37	D3A	20
168	docking CRT flicker issue	Reserve C98,R525 for docking CRT flicker issue	D3A	19
169	EMI issue	EMI suggest add C652(0.1uF)	D3A	19
170	system sometimes will no backlight issue .	For short term solution:change R22 from 10k(CS31002JB28) to 1K (CS21002FB24)	D3A	

Item:	Fixed Issue	Modify List:	Schematic Rev.	Page
171	Quanta DSC Team issue	Base on DSC command, change CN22 P/N from DFHDF8MS000 to DFHDF4MS000	D3A	33
172	rise time of LCDVCC is >0.5ms and <=10ms.	change U2 from AL004280000(AAT4280IGU-3-T1) to AL004280018(AAT4280IGU-1-T1).	D3A	23
173	Card reader issue	no stuff 43K(CS34302JB19):R562,R527,R533,R538,R539,R565,R561,R540,R498,R497,R500,R552,R555	D3A	23
174	Card reader issue	no stuff 10k(CS31002JB28) : R560	D3A	23
175	Card reader issue	Change R547 from 43k (CS34302JB19) to 8.2k (CS28202JB14)	D3A	23
176	Card reader issue	Change R528 from 10K(CS31002JB28) to 43K(CS34302JB19)	D3A	23
177	Shortage issue	Change R125 from CS11003B900 (100 ohm 0.1%) to CS11003F953(100 ohm 1%)	D3A	9
178	EMI issue	EMI request add two of clip(FDTA1003014) in PAD17 and PAD19 for EMI issue	D3A	30
179	DPST issue	Acer inform no support DPST in C build, remove R15	D3A	20
180	Shortage issue	Andy inform change PR116 from CS42102FB00 to CS42002FB12	D3A	34
181	ICH8M Power issue	ICH8M Internal VR should not be disabled.no stuff R241, stuff R226	D3A	14
182	implement it for CPU protect in C build.	Change R111 from *2.2k to 0ohm,Change R107 from 56.2(CS05622FB22) to 1k(CS21002FB24)	D3A	3
183	Battery life issue.	Battery life issue. Disable ICH8M Internal VR (LAN). stuff R241, no stuff R226 for C-build	D3A	14
184	Change EMI Spring Material	ME request, change EMI Spring from FDTA1003014 to FDZU1002010	E3A	30
185	C-Test SMT open issue	C-test SMT open issue, remove PAD18	E3A	30
186	ZR1 issue	Change CN2 Pin define to cover production line issue(Inverter short with signal to burn system)	E3A	20
187	C-Test SMT open issue	Change PD9,D46 footprint from SBM1040-3P to SBM1040-3P-ZU1 for SMT C-test open issue	E3A	33 & 39
188	Change NB P/N for RAMP	Change U29 P/N form AJ0QP200T09 to AJSLA5T0T05	E3A	5~11
189	Change SB P/N for RAMP	Change U32 P/N from AJ0QN230T10 to AJSLA5Q0T05	E3A	14~17
190	Material Lead issue	Change R214 from CS02403F908 to CS02403F916 (Lead free)	E3A	14
191	G995 failure rate issue	Add C653 base on G995 failure rate issue	E3A	3
192	Run-in auto shot down issue	ICMNT connect to EC pin100 , reserve R570 0ohm for debug use, Add C654 to avoid noise	E3A	28 & 39
193	remove wake on lan for Mini PCIE function.	Base on Acer demand, remove wake on lan for Mini PCIE function.no stuff Q25,R357	E3A	27
194	move D15~D18 location for FFC cable issue	Remove footprint (D16), Remove net (HWPG_3/5VPCU),no stuff PR119	E3A	28 & 34
195	LED issue	Change LED2, LED3 type base on ME request, Add R800,R801	E3A	29
196	HDD Mylar issue	Change C542 from 0805(CH6102K9A01) to 0603(CH6101M9905) base on ME request(HDD Mylar issue)	E3A	2
197	Docking issue	Change Q4,Q5 Pin2 from +3V to +3VSUS .(Docking side pull up to +3VSUS plane)	E3A	33
198	Docking issue	change C451,C452 from 0.1uF (CH41002KB93) to 0 ohm (CS00002JB38)(R802,R803)	E3A	33
199	Disable LAN Low Power mode	Stuff R78(CS24702JB38)	E3A	18
200	EOL issue	Change C453 from CC1210 (CH61004M3E5) to CC1206 (CH61004M2E8)	E3A	33
201	LPC CONN issue	confirm with BIOS-CM, no need LPC dedug CONN,Remove CN6,R432 footprint to save space for layout.	E3A	28
202	LAN_RST# issue	(1)Stuff 10k for R204(2)Don't stuff R456(3)Don't stuff R247	E3A	16
203	PO" sounds when insert PCMCIA card	Add 0 ohm (R804) for PCMSPK	E3A	22
204	ESD issue	Stuff D38 for CRT port	E3A	19

PROJECT : ZU1 Quanta Computer Inc.	PROJECT : ZU1	APPROVE BY : Kin Wang	DRAWING BY:Barry Lee	Stage: C / Ramp
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CHANGE LIST SHEET 6

Item:	Fixed Issue	Modify List:	Schematic Rev.	Page
205	PCMCIA POP SOUND issue	Refer to BU1, add circuit for POP sound issue	E3A	24
206	GLAN issue	Stuff R232 (CS02492FB29), The GLAN_COMPO/GLAN_COMPI connection to 1.5-V rail through the resistor remains	E3A	14
207	ESD issue	change LED type (follow B stage) DEL LED2,LED3, Add LED4~7	E3A	29
208	ESD issue	change ESD protect Diode from location LED/B to MB	E3A	29
209	Disable LAN Low power mode	Base on PM suggestion, add serial 0 ohm (R806) for debug use.(no stuff)	E3A	18
210			E3A	
211			E3A	
212			E3A	
213			E3A	
214			E3A	
215			E3A	
216			E3A	
217			E3A	
218			E3A	
219			E3A	
220			E3A	
221			E3A	
222			E3A	
223			E3A	
224			E3A	
225			E3A	
226			E3A	
227			E3A	
228			E3A	
229			E3A	
230			E3A	
231			E3A	
232			E3A	
233			E3A	
234			E3A	
235			E3A	
236			E3A	
237			E3A	
238			E3A	