

Compal Confidential

Model Name : ZIUS6/S7

File Name : LA-A321PR01

BOM P/N:4319OP38L5x -- ZIUS7

4319OP38L0x -- ZIUS6

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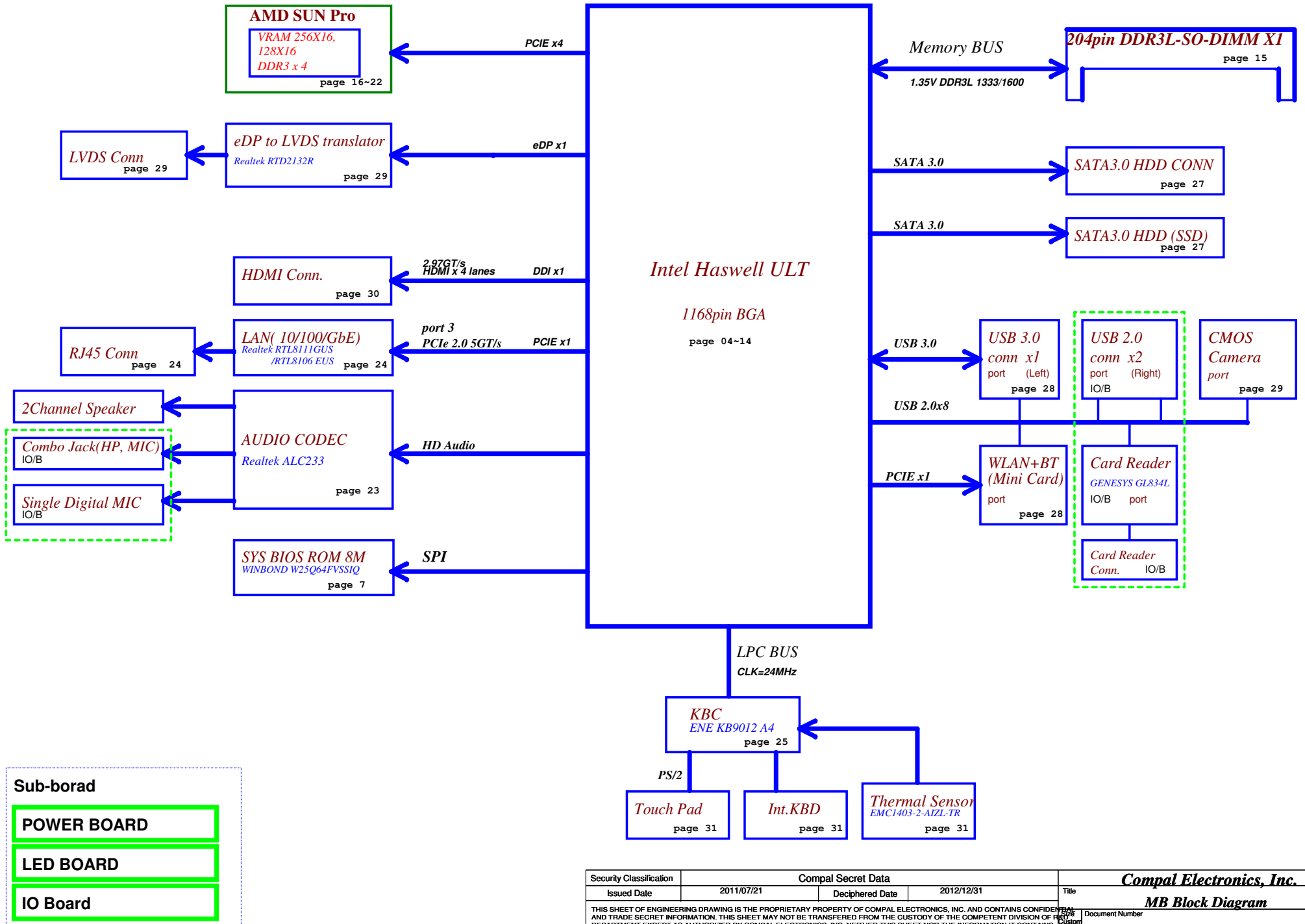
ZIUS6/S7 M/B Schematics Document

Intel SharyBay ULT Processor + AMD SUN Pro

2013-03-14

REV: 0.2

Security Classification	Compal Secret Data		Title	
Issued Date	2011/06/24	Deciphered Date	2012/07/12	Compal Electronics, Inc. Cover Page
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Voltage Rails

power plane	B+	+5VALW	+1.35V	
State		+3VALW		+5VS +3VS +1.5VS +1.05VS_VTT +CPU_CORE +0.675VS +VGA_CORE (PX) +0.95VS_VGA (PX) +3.3VS_VGA (PX) +1.8VS_VGA (PX) +1.5VS_VGA (PX)
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	✗	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

STATE	SIGNAL	SLP_S0#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOM Structure Table

BTO Item	BOM Structure
Connector	ME@
45 LEVEL	45@
Unpop	@
CPU OPTION	CPU1@
INTEL UMA	UMA@
AMD SUN Pro	PX@
VRAM Option	S1G@ M1G@ H1G@ S2G@ M2G@
LAN RTL8111GUS	8111@ SWR@
LAN RTL8106EUS	8106@ SWR@
USB3.0	USB3@
EMI PART	EMI@
ESD PART	ESD@

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	0.2
3	0.1
4	
5	
6	
7	

EC SM Bus1 address

Device	Address
Smart Battery Charger	0xA0

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2-AIZL-TR	1001_101xb
Panel - eDP to LVDS translator	
SharkBay ULT	
AMD SUN Pro	

CPU SM Bus address

Device	Address
DDR DIMM0	0xA0
WALN	
Touch Pad	

CPU SML0 Bus address

Device	Address

USB 2.0 Port Table

Port	3 External USB Port
0	USB 2.0 Port (I/O Board)
1	USB 3.0/2.0 Port (MB)
2	USB 2.0 Port (I/O Board)
3	Card Reader
4	Touch Screen (reserve)
5	Camera
6	Mini Card (WLAN/BT)
7	

USB 3.0 Port Table

Port	
1	
2	USB 3.0 Port (MB)
3	
4	

PCIe Port Table

Port	Lane	
1		
2		LAN
3		WLAN
4		
5	0	
	1	
	2	GPU
	3	
6	0	
	1	
	2	
	3	

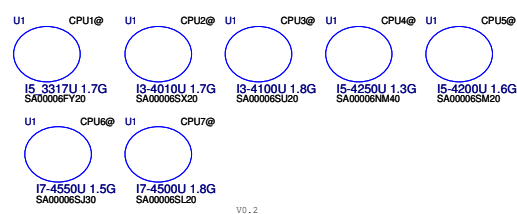
SATA Port Table

Port	
3	
2	
1	mSATA SSD
0	HDD

SMBUS Control Table

	HOST	VGA	BATT	KB9012	SODIMM	WLAN	PANEL sensor ADM1032	Thermal sensor EMC1403	VGA sensor ADM1032	CPU Sensor	Touch Pad	Security ROM	NFC
EC_SMB_CK1	KB9012	X	V	X	X	X	X	X	X	X	X	X	X
EC_SMB_DA1	+3VLP		+3VLP										
EC_SMB_CK2	KB9012	V	X	X	X	X	V	V	V	V	X	X	X
EC_SMB_DA2	+3VS	+3VS					+3VS	+3VS	+3VS	+3VALW			
SMBCLK	CPU	X	X	X	X	X	X	X	X	X	+3VS	+3VS	+3VS
SMBDATA	+3VALW												
SML0CLK	CPU	X	X	X	X	X	X	X	X	X	X	X	X
SML0DATA	+3VALW												
SML1CLK	KB9012	X	X	V	X	X	X	X	X	V	X	X	X
SML1DATA	+3VS			+3VS						+3VALW			

CPU part



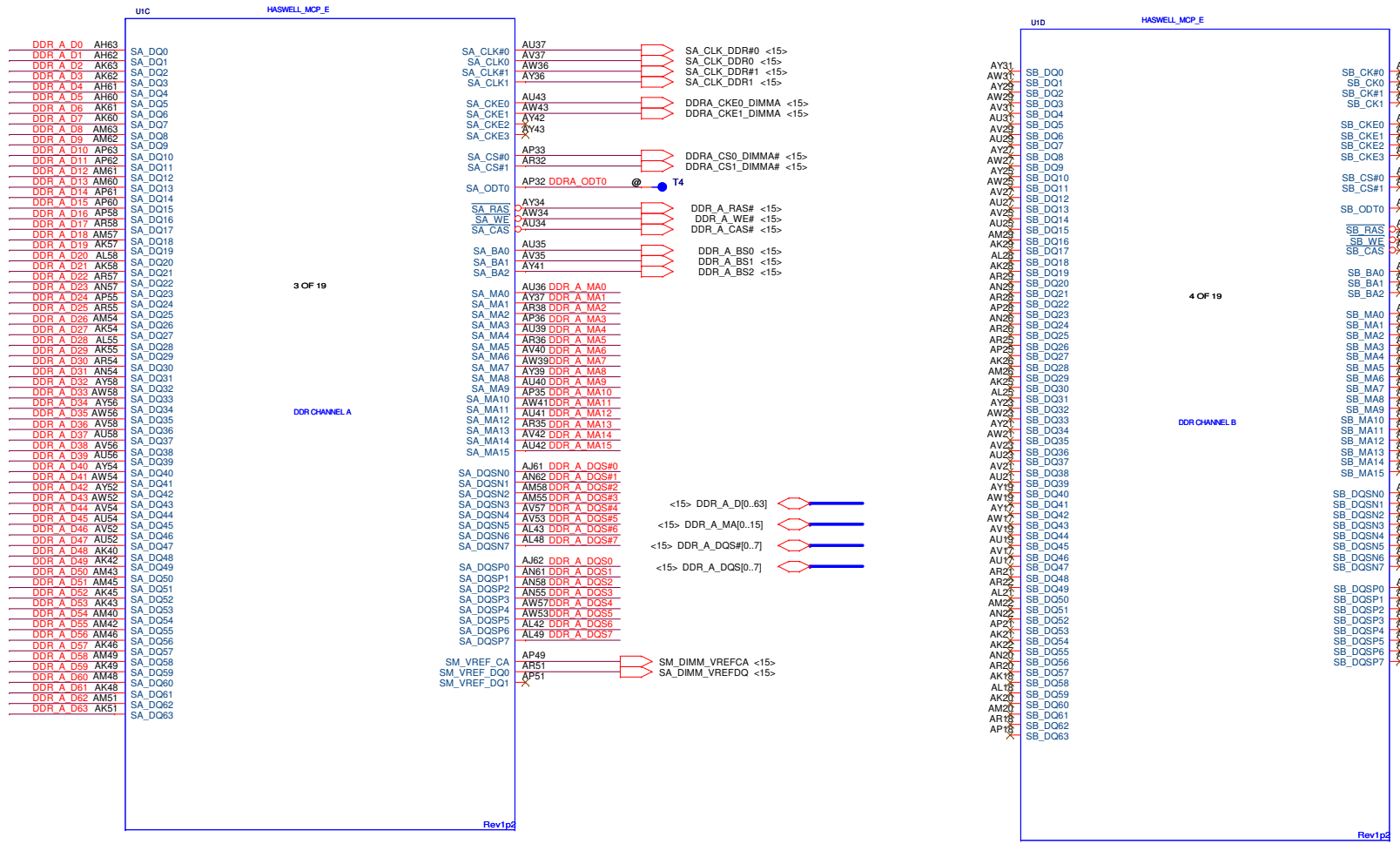
PCB part



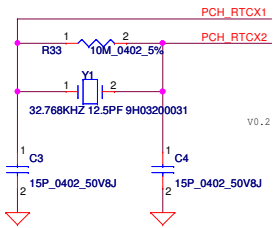
VRAM



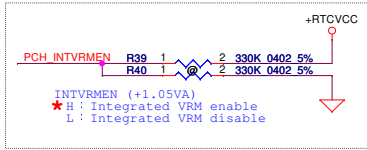
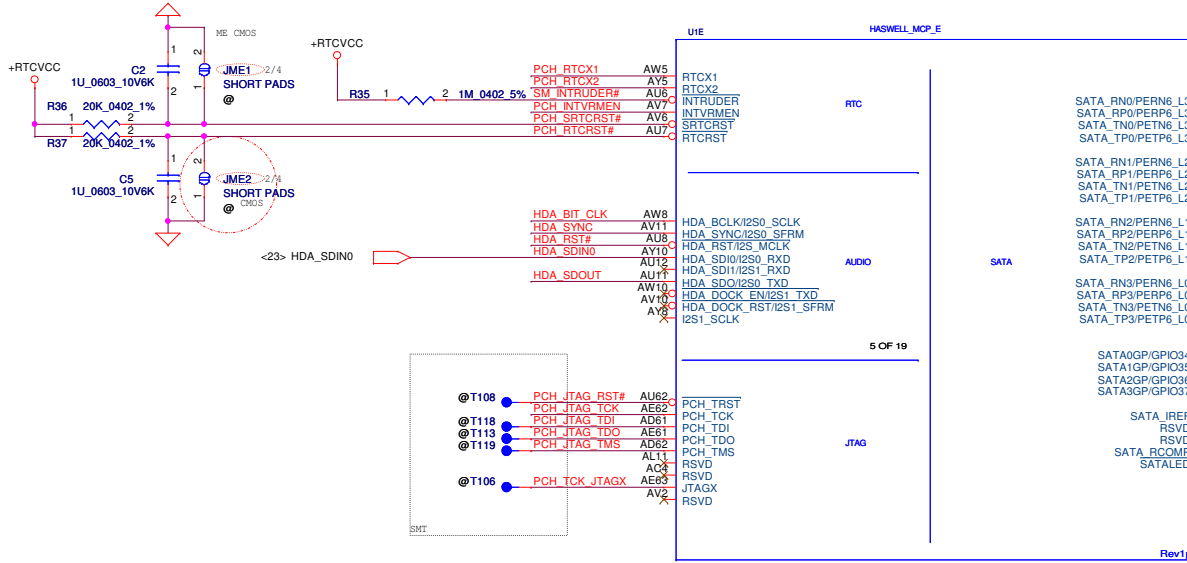
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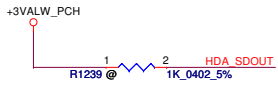
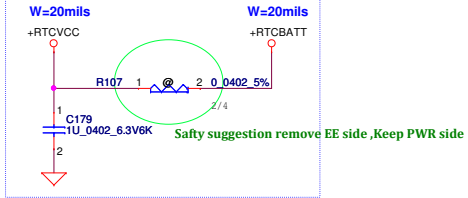
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Issued Date	2011/12/13	Deciphered Date	2012/12/13	Compal Electronics, Inc. HSW MCP(2/11) DDRIII	
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JME2 Short PAD placement to Bottom side.

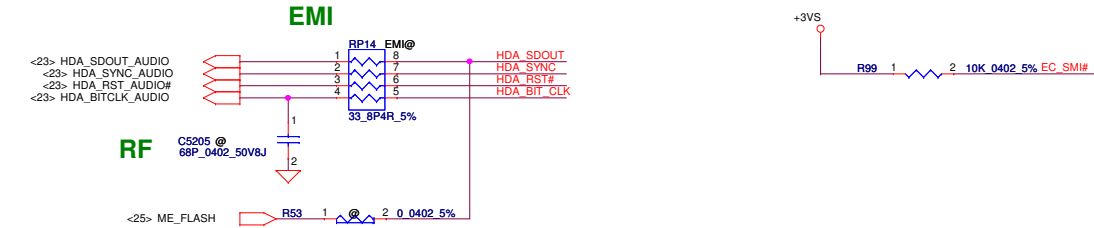
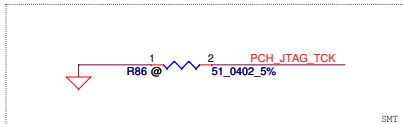


RTC Battery



HDA_SDOUT
ME debug mode, this signal has a weak internal PD
* Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Override]

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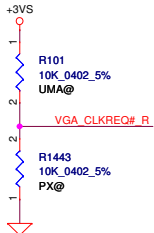
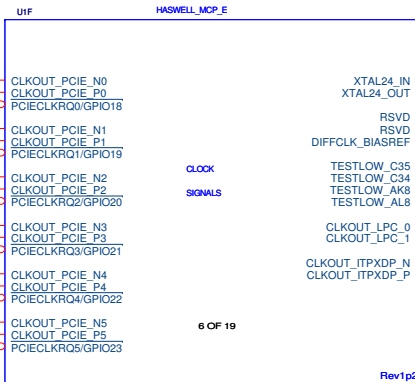


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GLAN

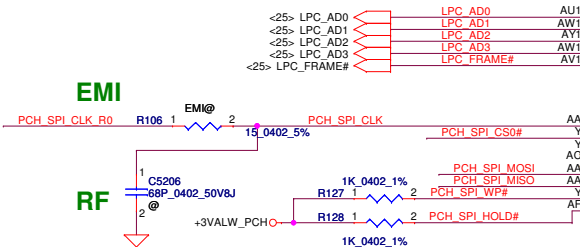
WLAN

dGPU

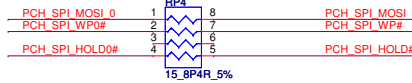


EMI

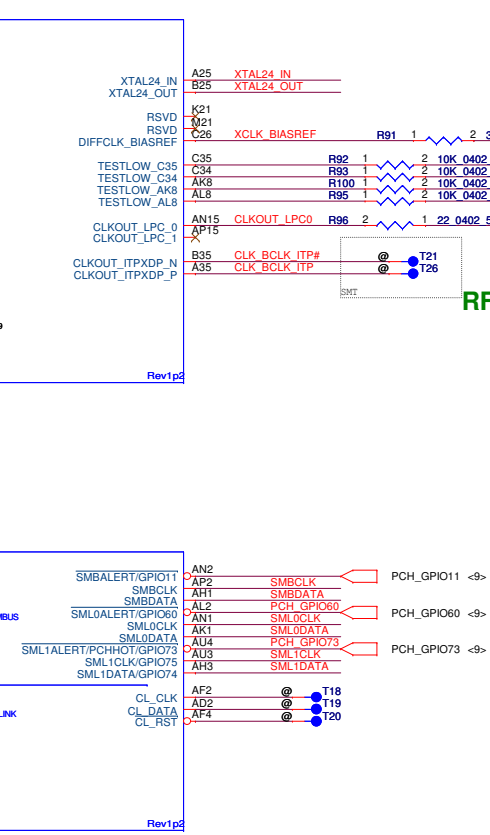
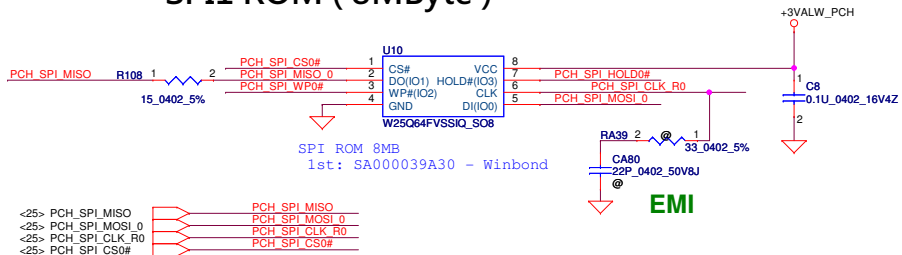
RF



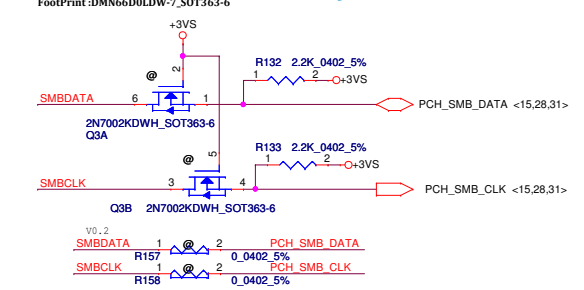
CHKLIST1.0
 2 SPI Device = 33 ohm
 1 SPI Device = 15 ohm



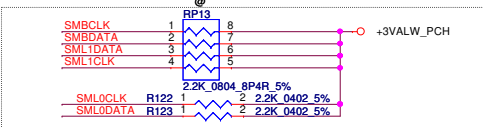
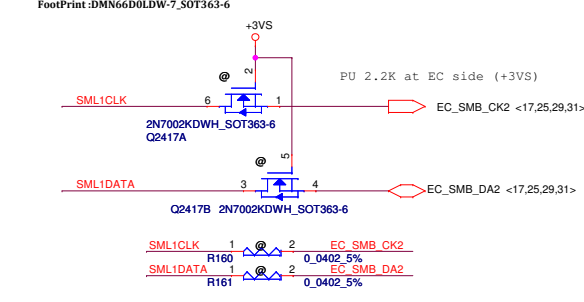
SPI1 ROM (8MByte)



SMBus :SPD/PCIe/Security/TP



SML1 Bus :EC/Sensors



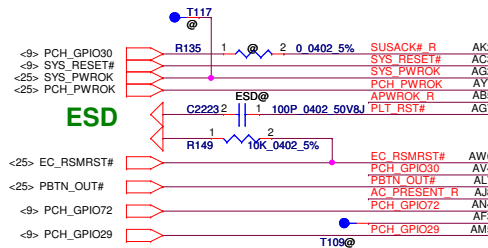
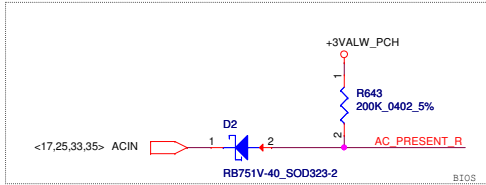
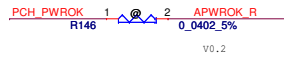
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Note: SUSACK# and SUSWRN# can be tied together if EC does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit

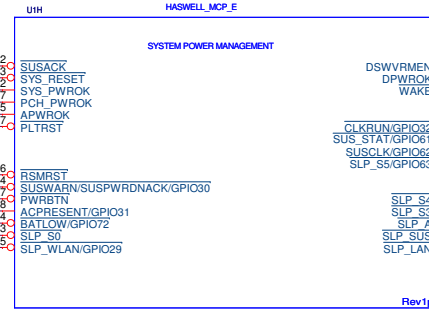
CAN be NC ,if not support Deep Sx

DPWROK: Tired togher with RSMRST# that do not support Deep Sx

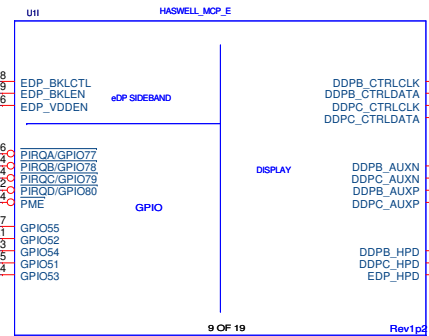
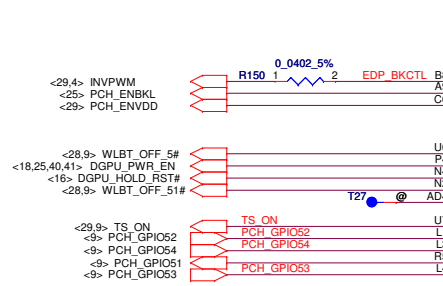
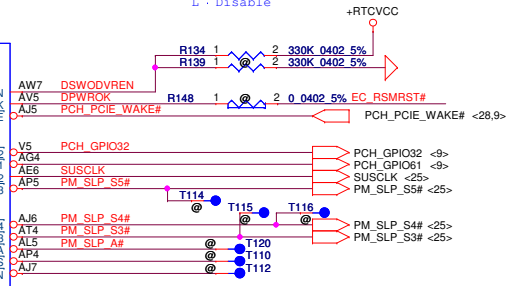
DSWODVREN - On Die DSW VR Enable
 * H : Enable (DEFAULT)
 L : Disable



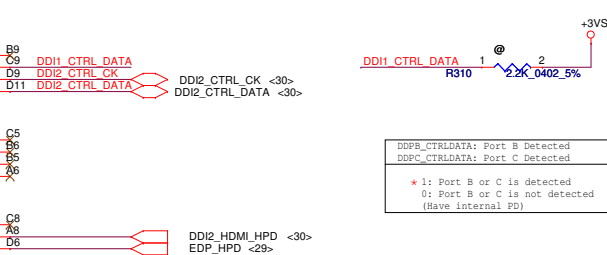
PCH_BATLOW# Need pull high to VCCDSW3_3 (If no deep Sx , connect to VCCSUS3_3)



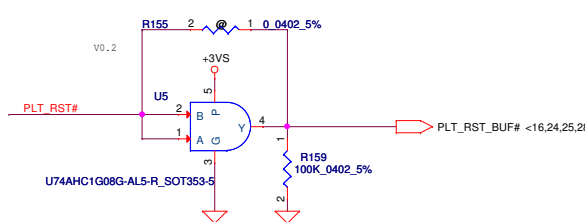
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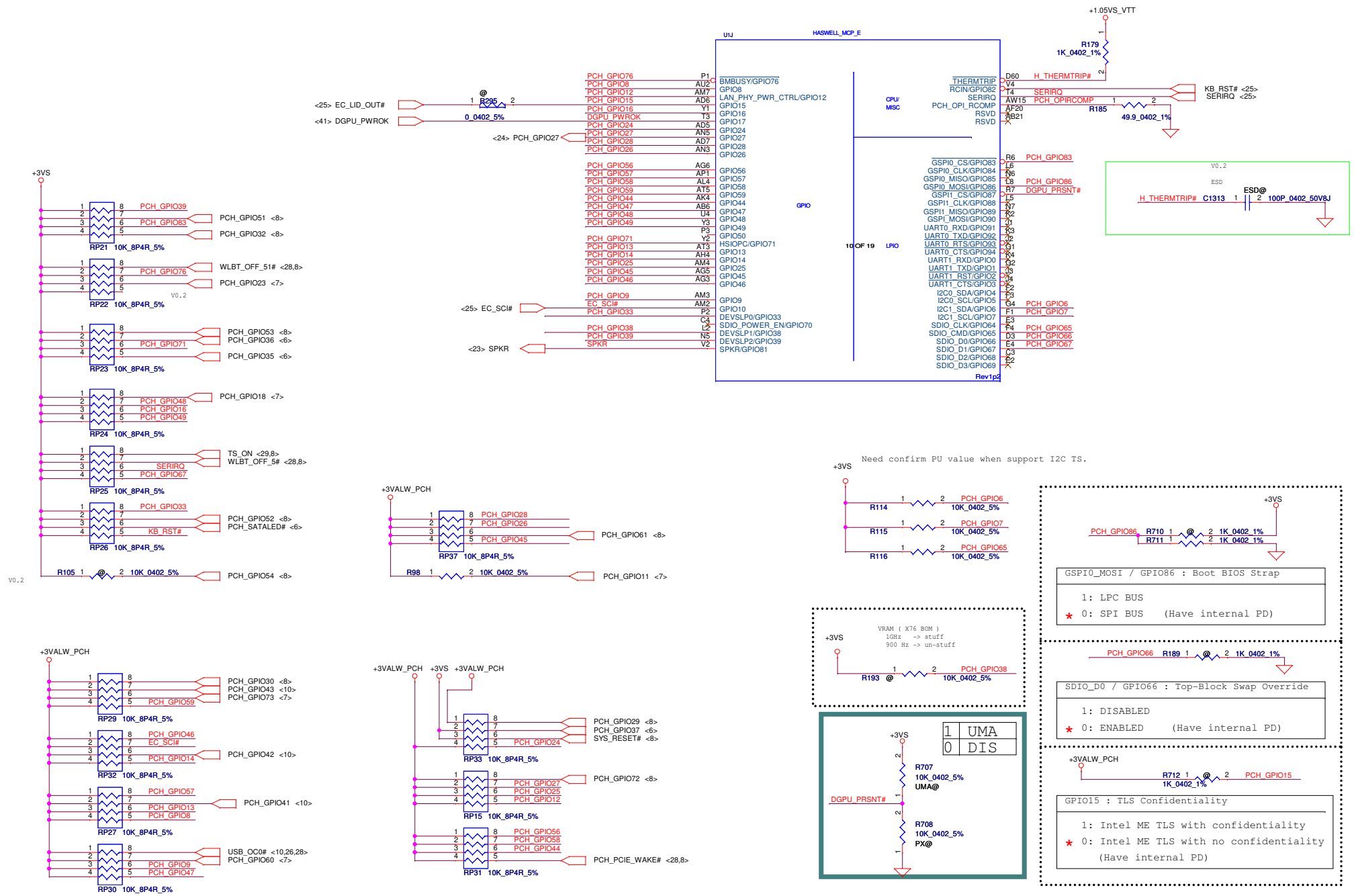
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DDPB_CTRLDATA: Port B Detected
 DDPC_CTRLDATA: Port C Detected
 * 1: Port B or C is detected
 0: Port B or C is not detected
 (Have internal PD)



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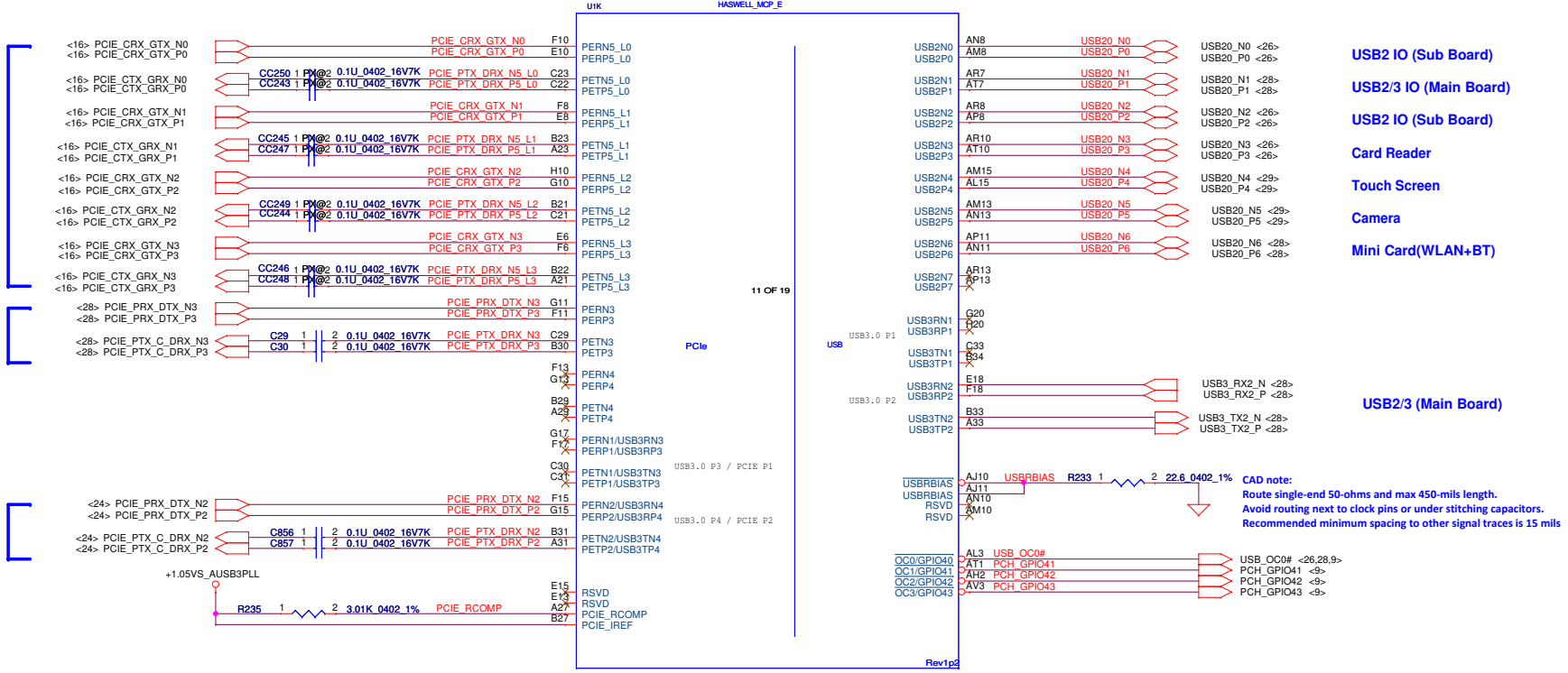


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dGPU

WLAN

LAN



USB2 IO (Sub Board)

USB2/3 IO (Main Board)

USB2 IO (Sub Board)

Card Reader

Touch Screen

Camera

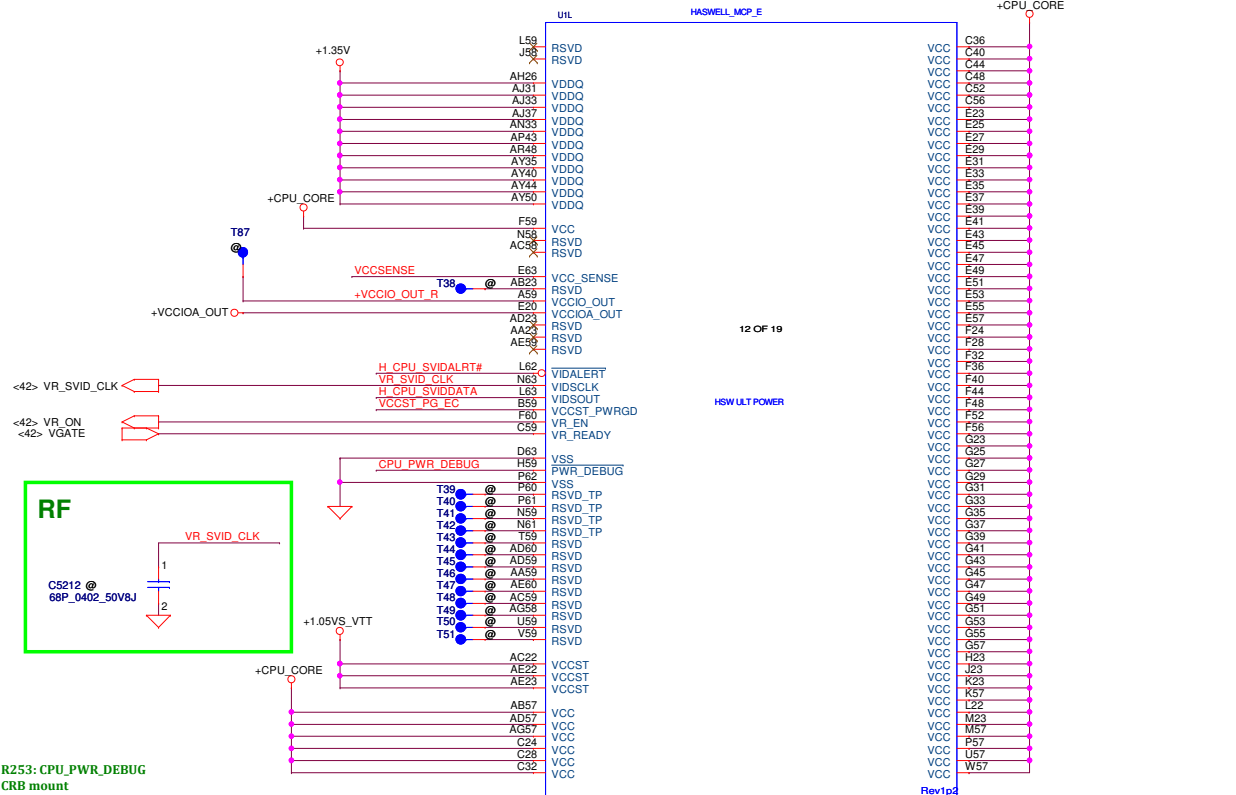
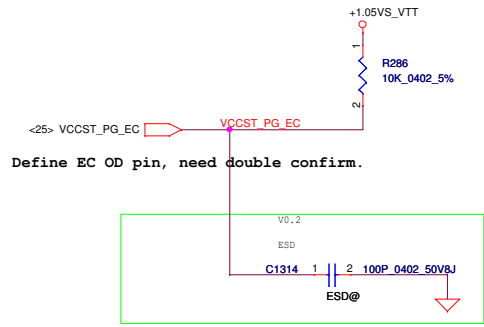
Mini Card(WLAN+BT)

USB2/3 (Main Board)

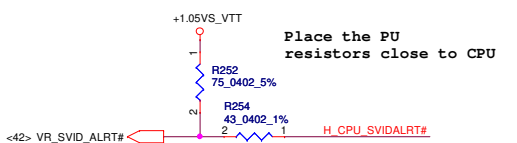
CAD note:
 Route single-end 50-ohms and max 450-mils length.
 Avoid routing next to clock pins or under stitching capacitors.
 Recommended minimum spacing to other signal traces is 15 mils

Rev1p2

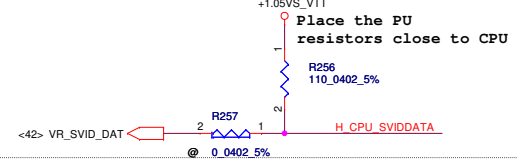
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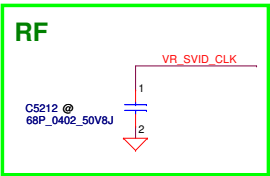
SVID ALERT



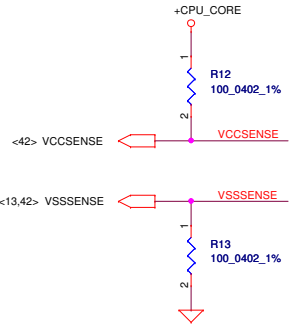
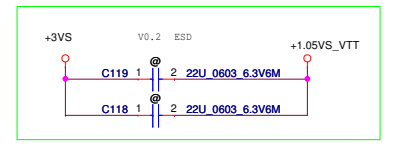
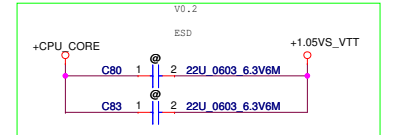
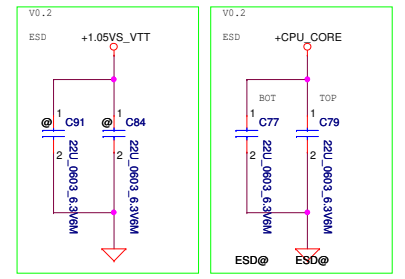
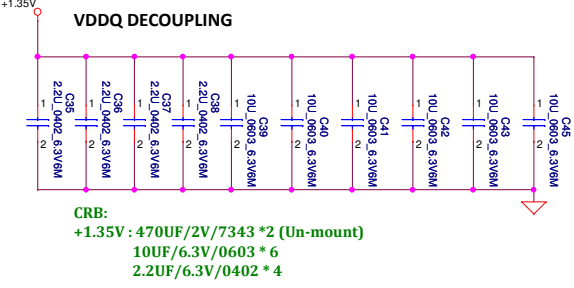
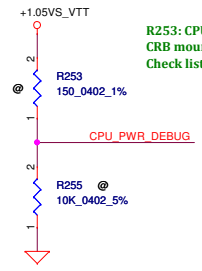
SVID DATA



R256:
CRB r0.7 changed from 130 Ohms to 110 Ohms



R253: CPU_PWR_DEBUG
CRB mount
Check list, XDP use only

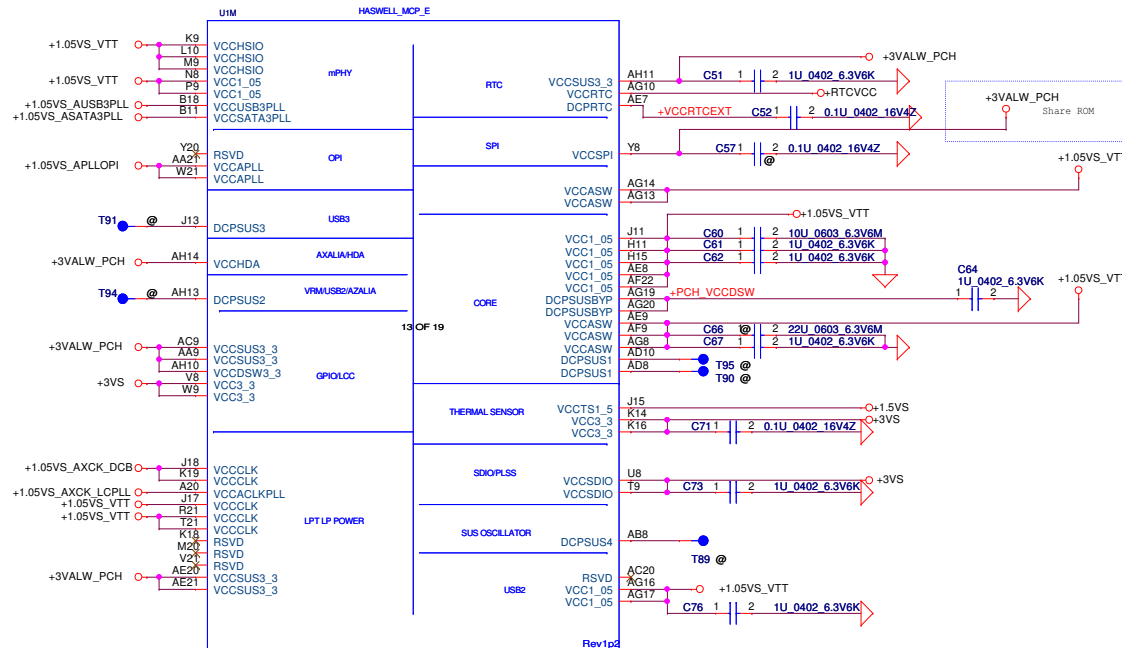
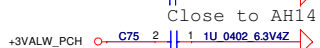
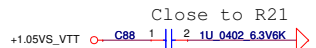
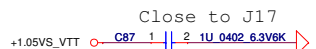
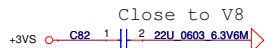
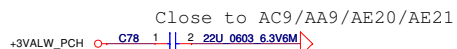
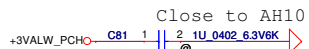
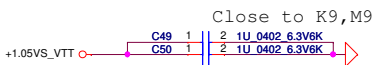
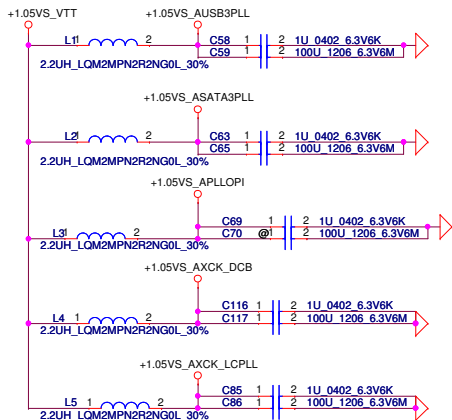


CAD Note: PU resistor should be close to CPU

CAD Note: PD resistor should be close to CPU

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/12/13	Deciphered Date	2012/12/13	Title HSW MCP(8/11) Power	
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Date	Thursday, March 14, 2013			Sheet	11 of 46

Check Power Source Close to N8
 +1.05VS_VTT C53 @ 1 2 1U 0402 6.3V6K

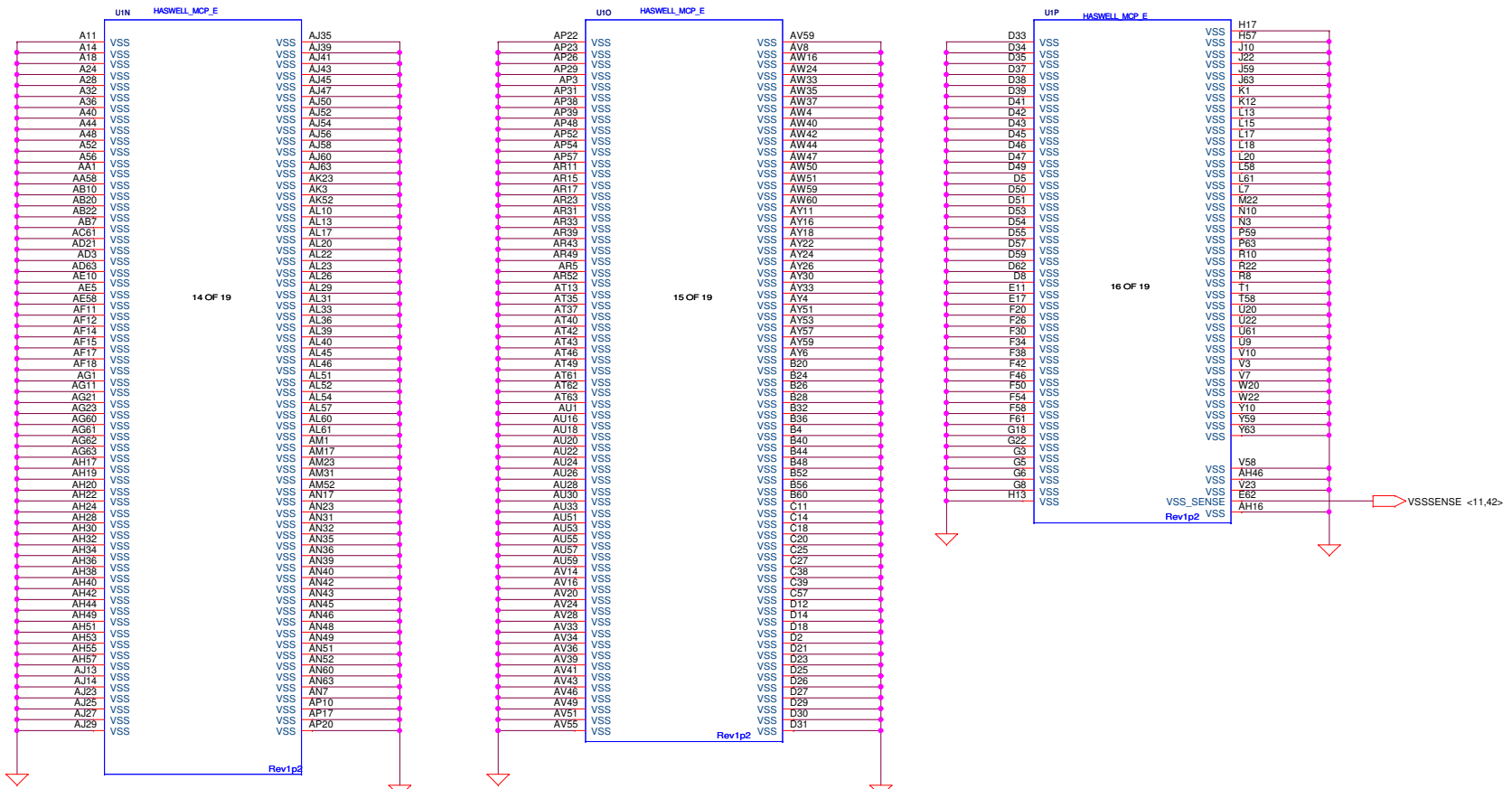


18mA

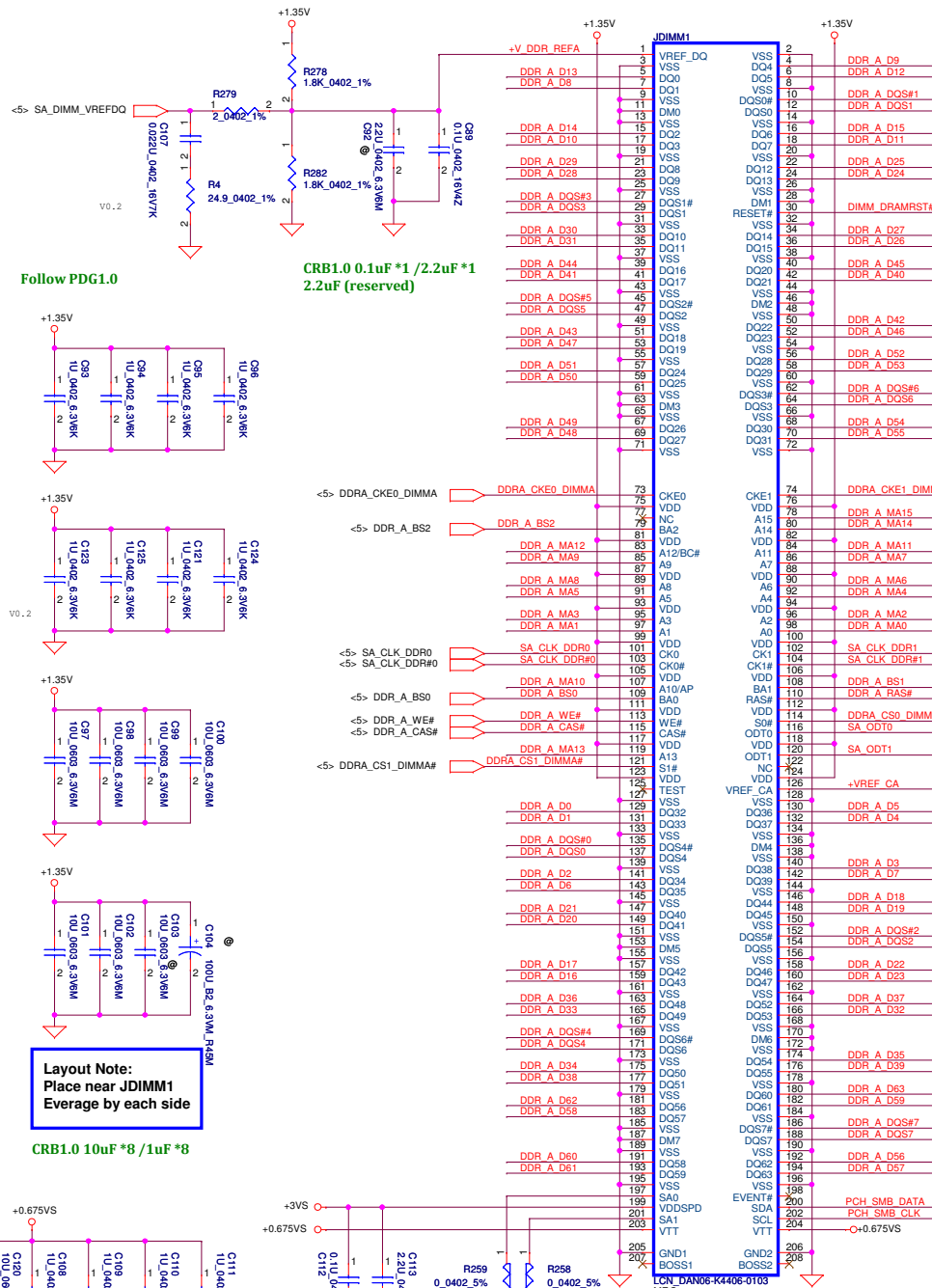
658mA

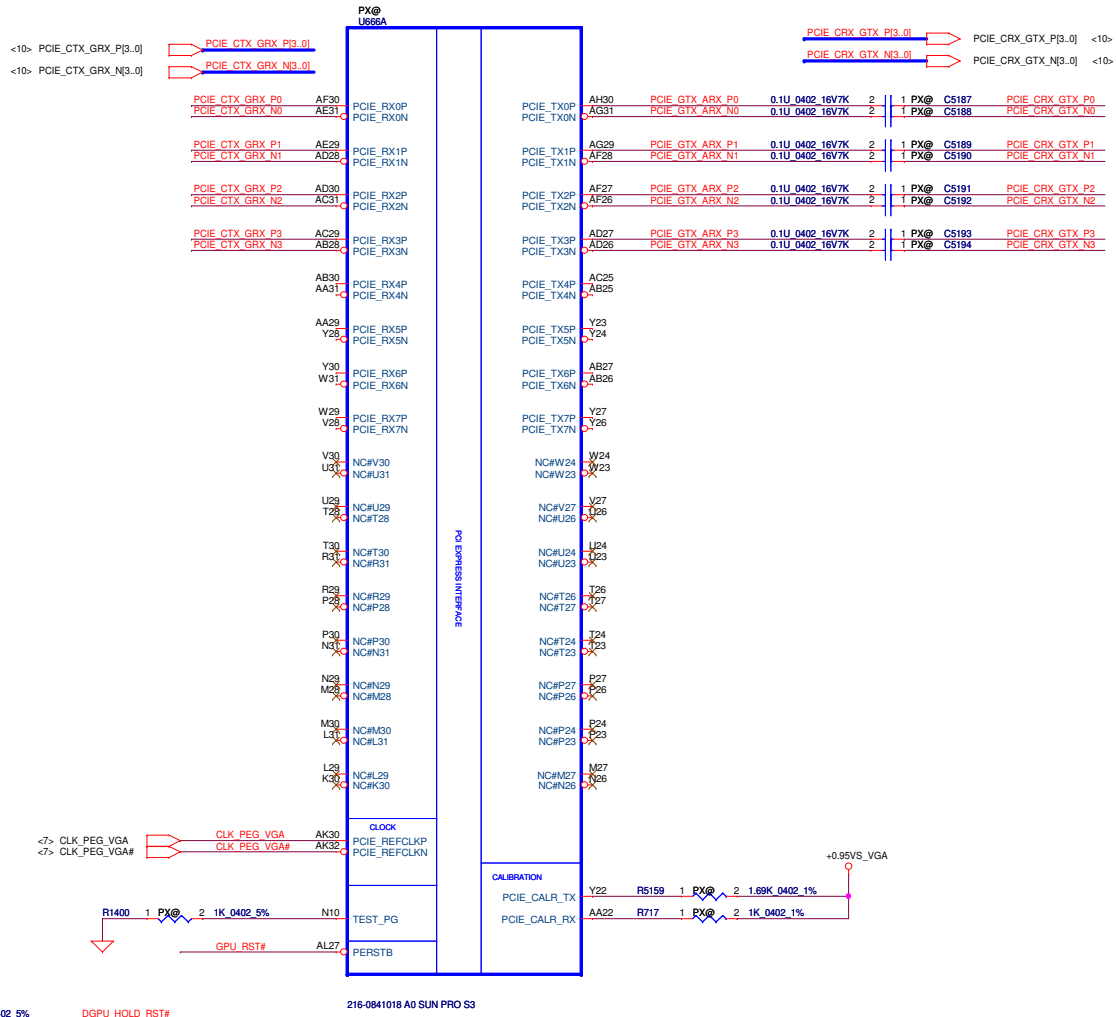
+RTCVCC
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			Sheet 12 of 46	Rev 0.2

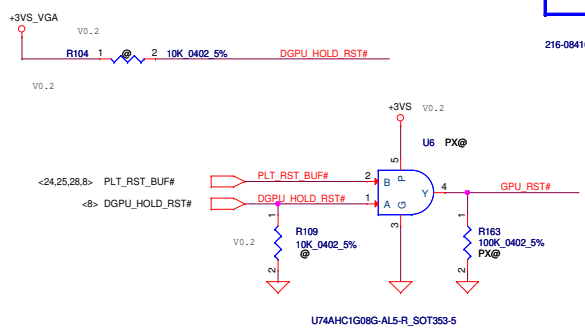
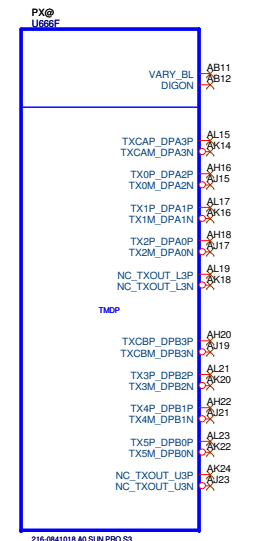


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				LA-A321PR02	0.2
Date: Thursday, March 14, 2013				Sheet	13 of 46



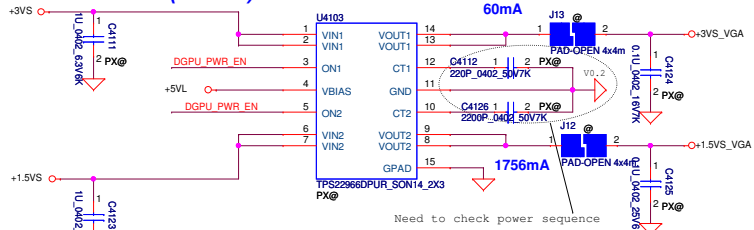


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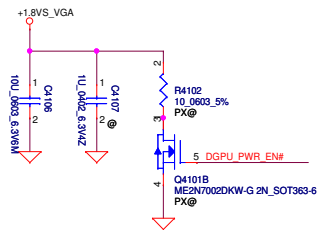


Security Classification	Compal Secret Data		Title	
Issued Date	2013/01/11	Deciphered Date	2013/12/31	SUN_PCIE/DP
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Date: Thursday, March 14, 2013				Rev 0.2
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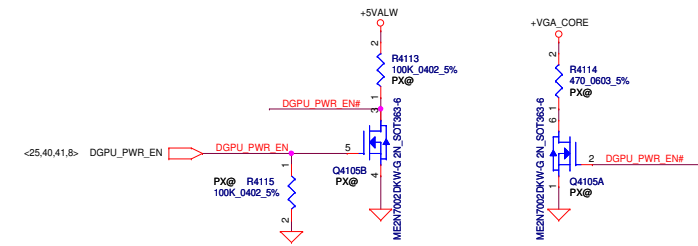
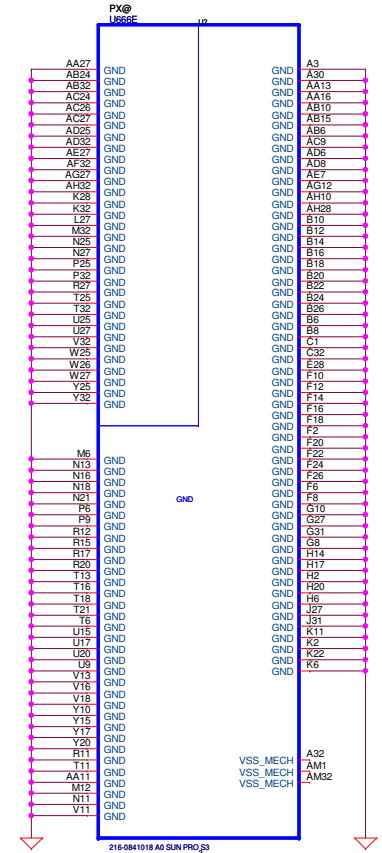
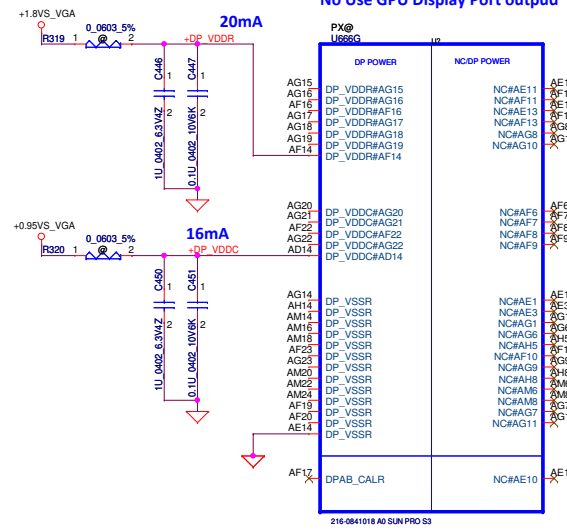
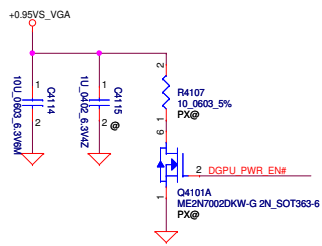
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+1.5V to +1.5VSG (2.096A)



+1.8VALW to +1.8VSG (818mA)

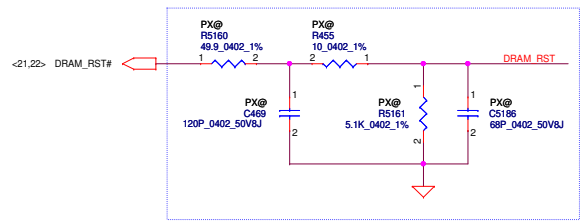
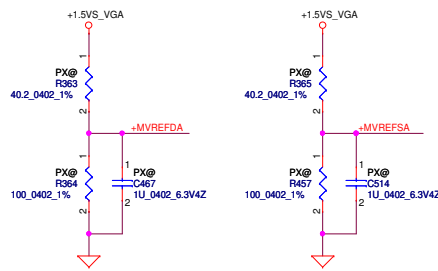


+0.95VALW to +0.95VSG (4.016A)



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Issued Date	2013/01/11	Deciphered Date	2013/12/31	SUN Power/GND	
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Size	Custom	Document Number	LA-A321PR02		Rev 0.2
Date:	Tuesday, March 19, 2013		Sheet	18	of 46

- <21,22> M_DA[63..0] M_DA[63..0]
- <21,22> M_MA[15..0] M_MA[15..0]
- <21,22> M_DQM[7..0] M_DQM[7..0]
- <21,22> M_DQS[7..0] M_DQS[7..0]
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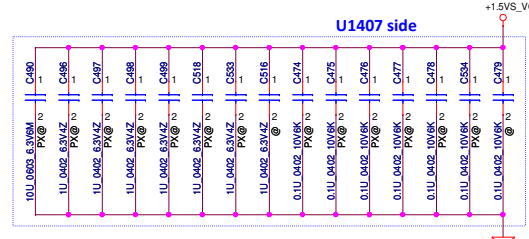
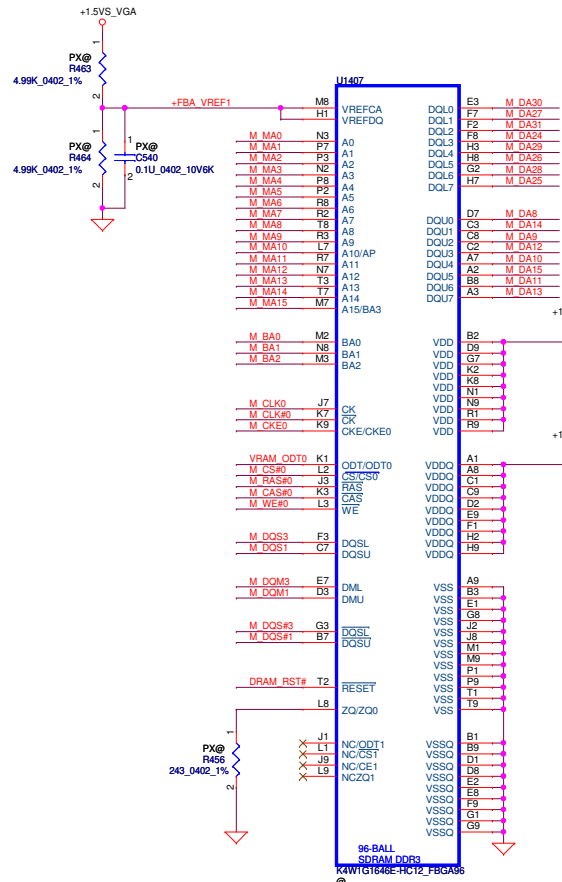
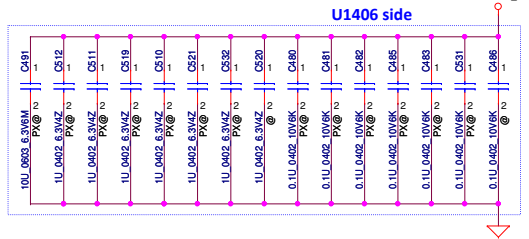
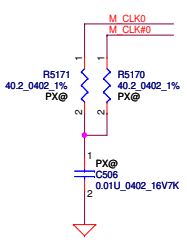
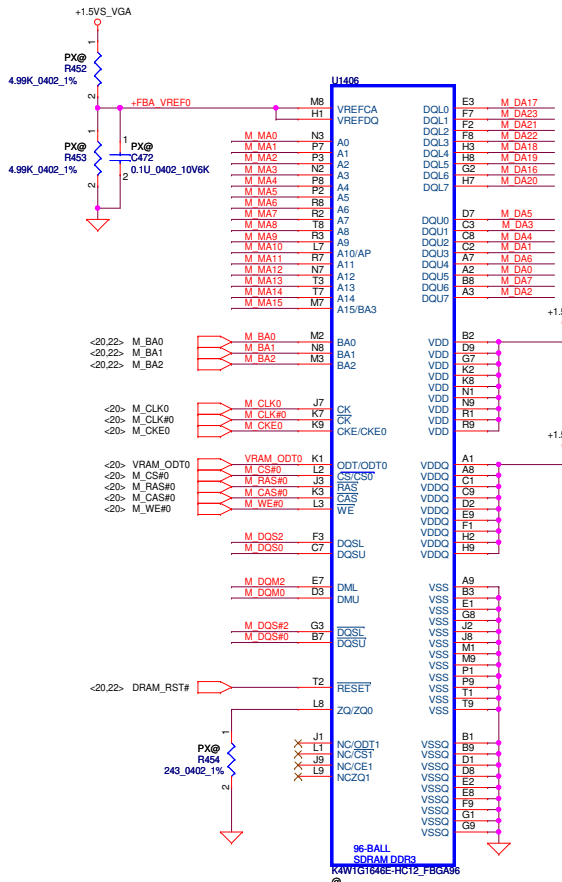
Place close to GPU (within 25mm)
and place component close to each other



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Issued Date	2013/01/11	Deciphered Date	2013/12/31	SUN MEM	
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Size	Custom	Document Number	LA-A321PR02		Rev 0.2
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Memory Partition A - Lower 32 bits

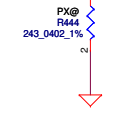
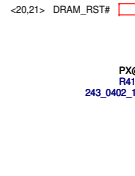
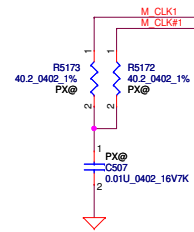
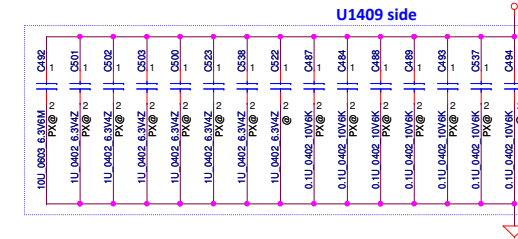
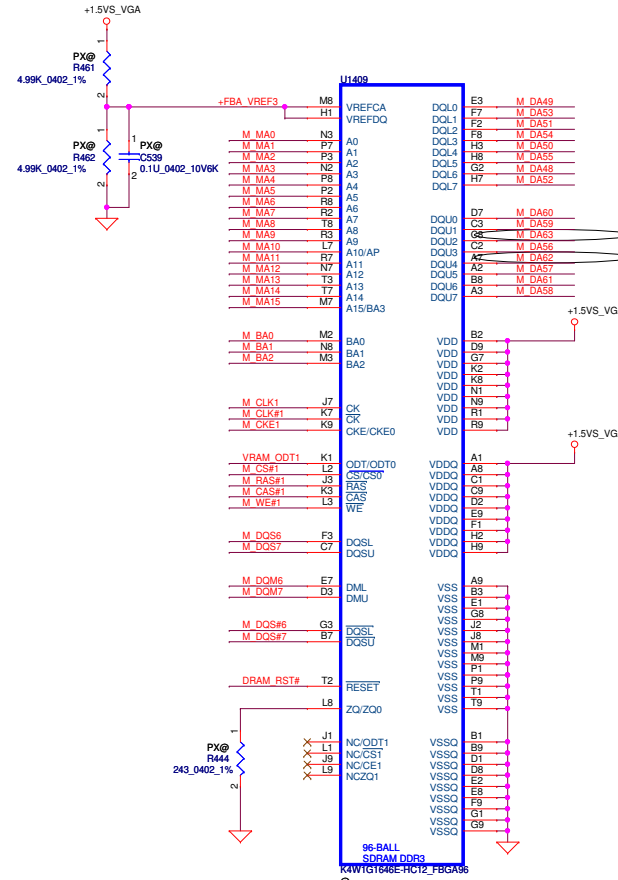
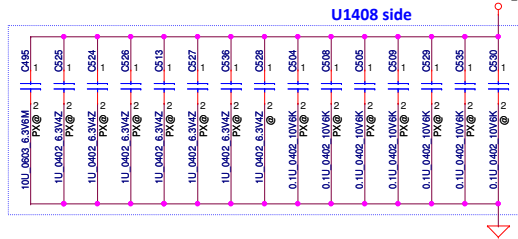
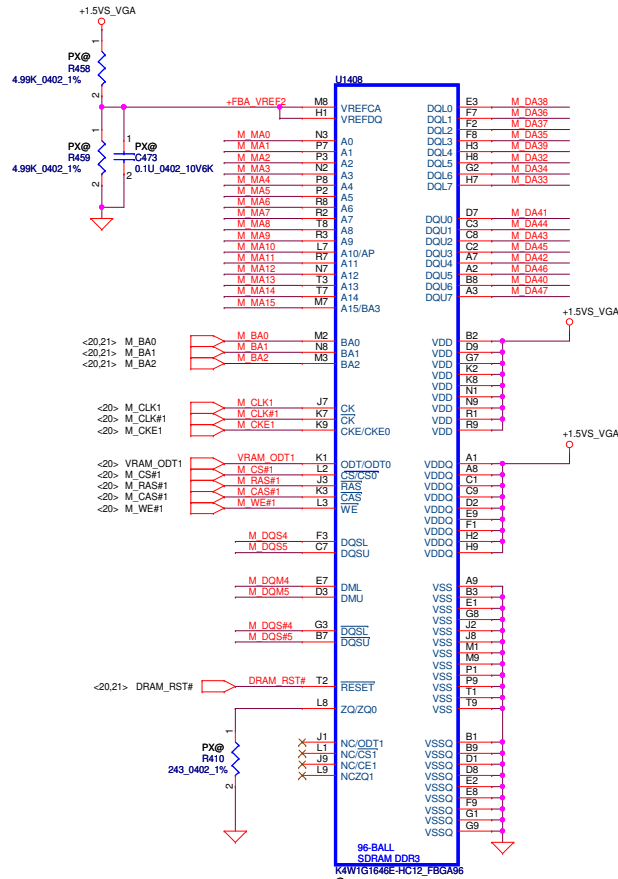
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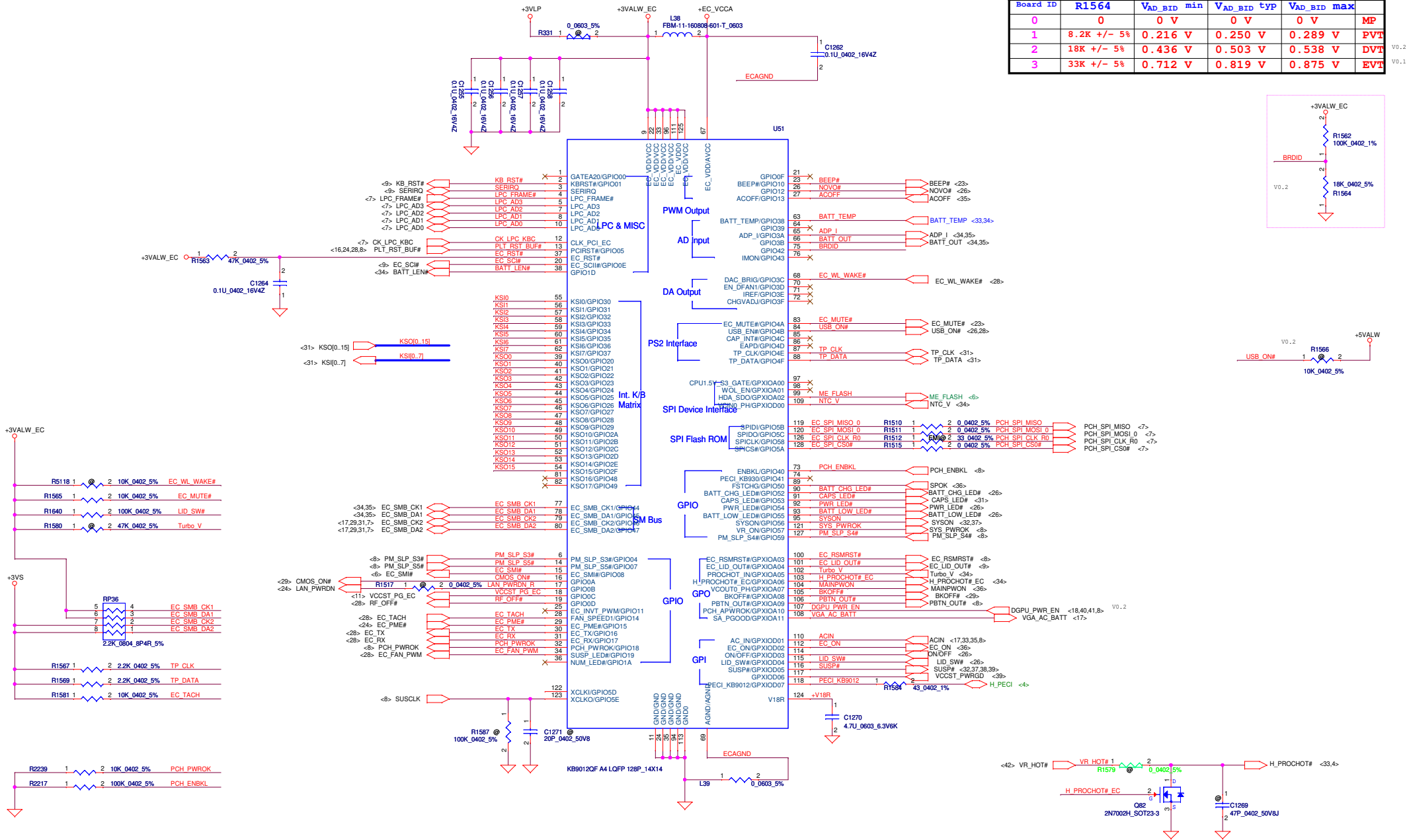
Security Classification	Compal Secret Data		Title
Issued Date	2013/01/11	Deciphered Date	
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Memory Partition A - Upper 32 bits

- <20.21> M_DA[63..0] M_DA[63..0]
- <20.21> M_MA[15..0] M_MA[15..0]
- <20.21> M_DQM[7..0] M_DQM[7..0]
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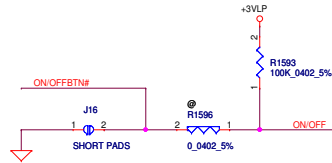
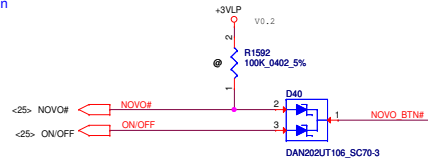
Vcc	3.3V +/- 5%				
R1562	100K +/- 5%				
Board ID	R1564	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	
0	0	0 V	0 V	0 V	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	EVT



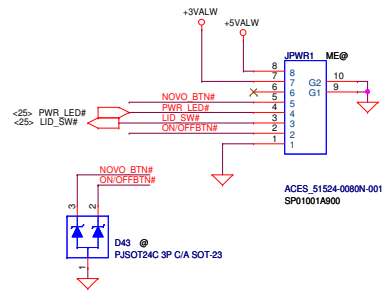
Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		BIOS & EC I/O Port	
2011/06/15		2012/07/11		Rev 0.2	
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Size Custom	Document Number	LA-A321PR02		Date	Thursday, March 14, 2013
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I/O Board CONN.

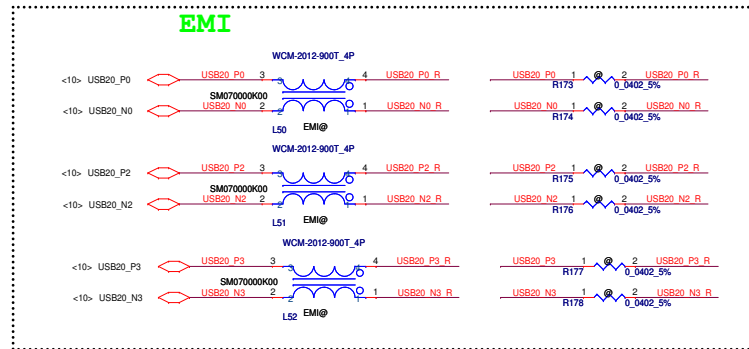
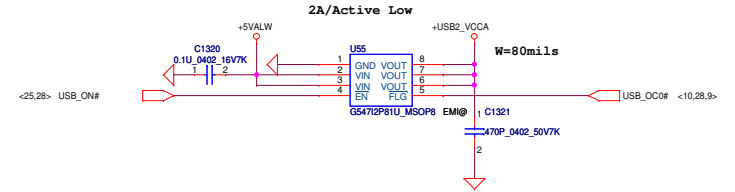
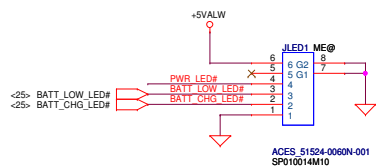
Connector: 0.3A / pin



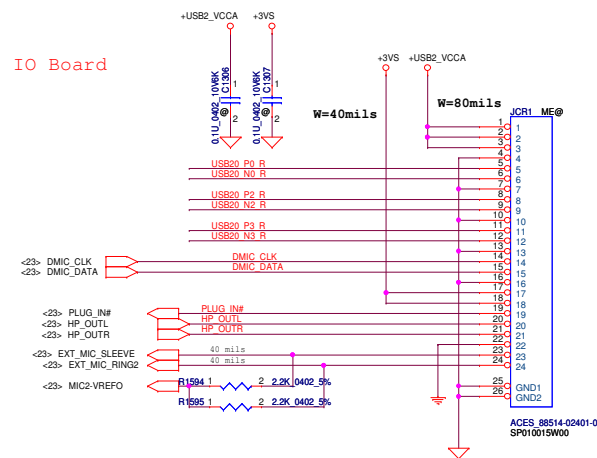
Power Board



LED Board

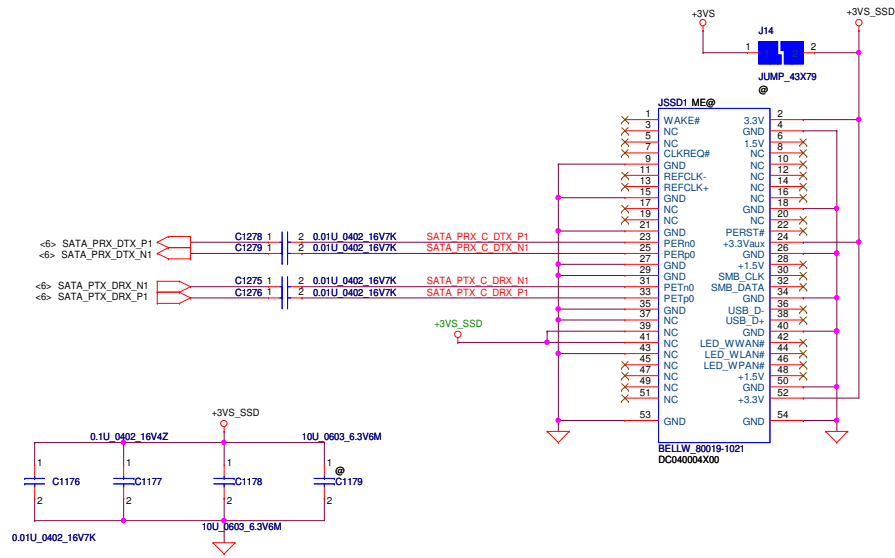


IO Board

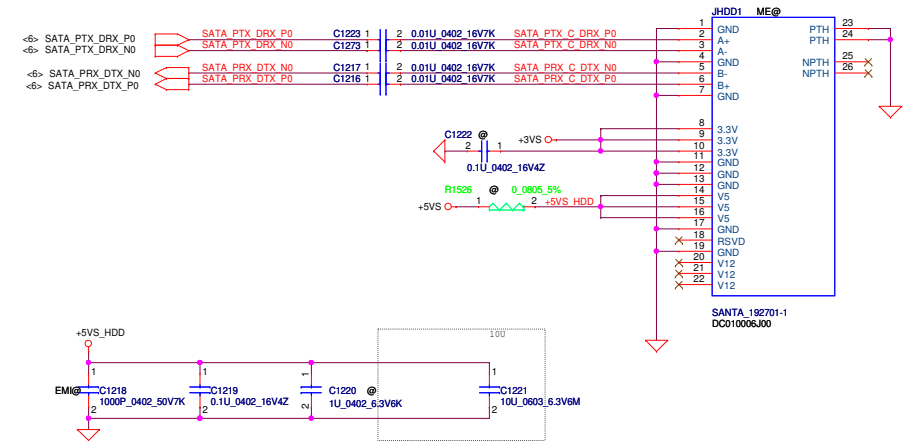


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Size	Document Number		Rev
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msATA CONN.

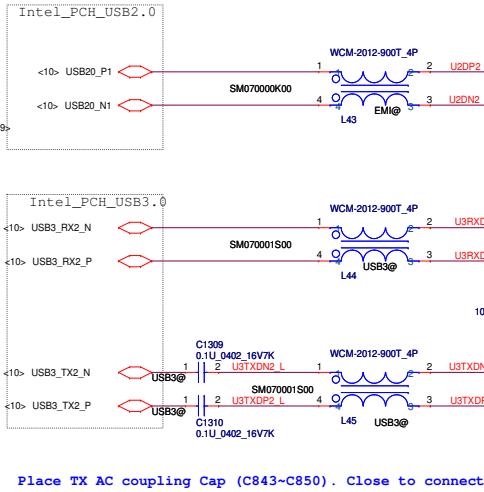
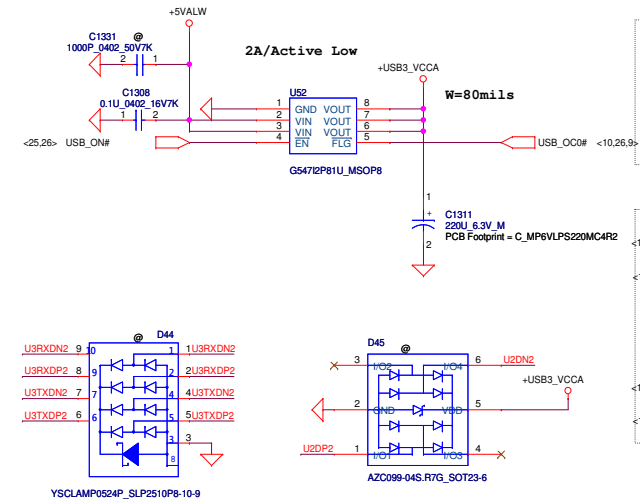


SATA HDD CONN.

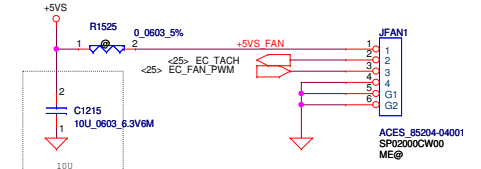
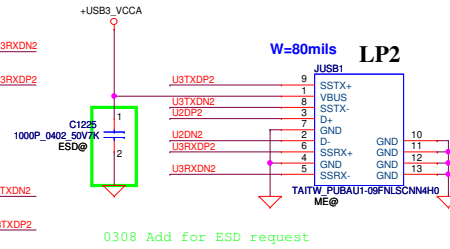


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Issued Date	2011/06/15	Deciphered Date	2012/07/11	HDD/ODD/IBT Connector	
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			Date:	Thursday, March 14, 2013	Sheet 27 of 46

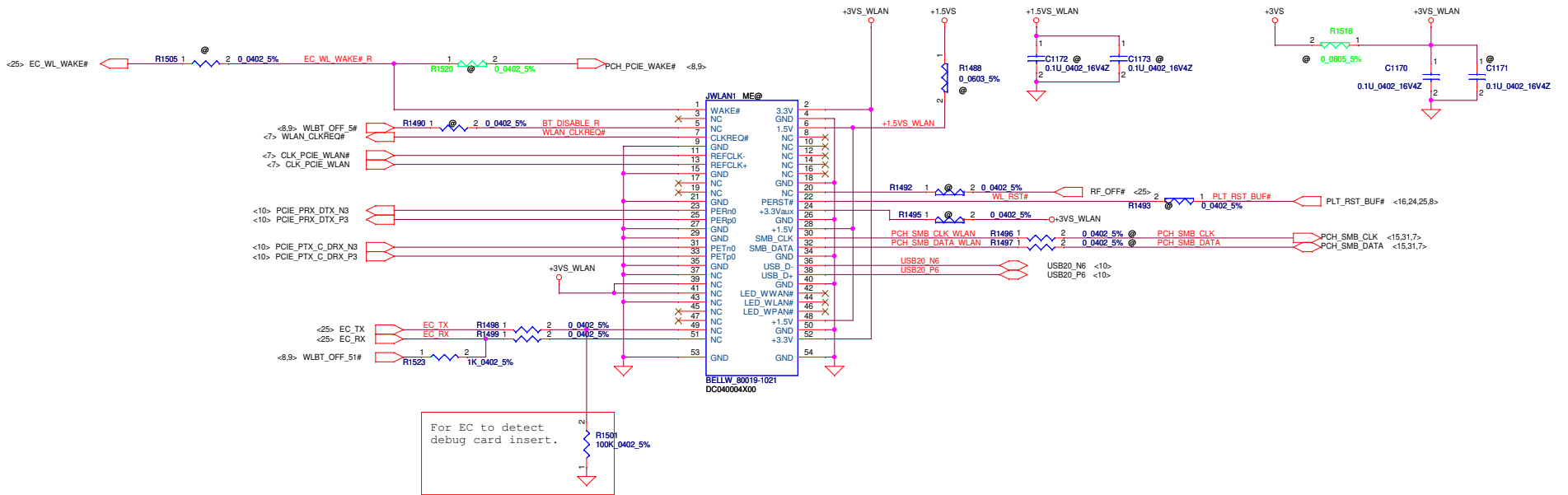
USB 3.0 Charger & Conn.



FAN CONN.

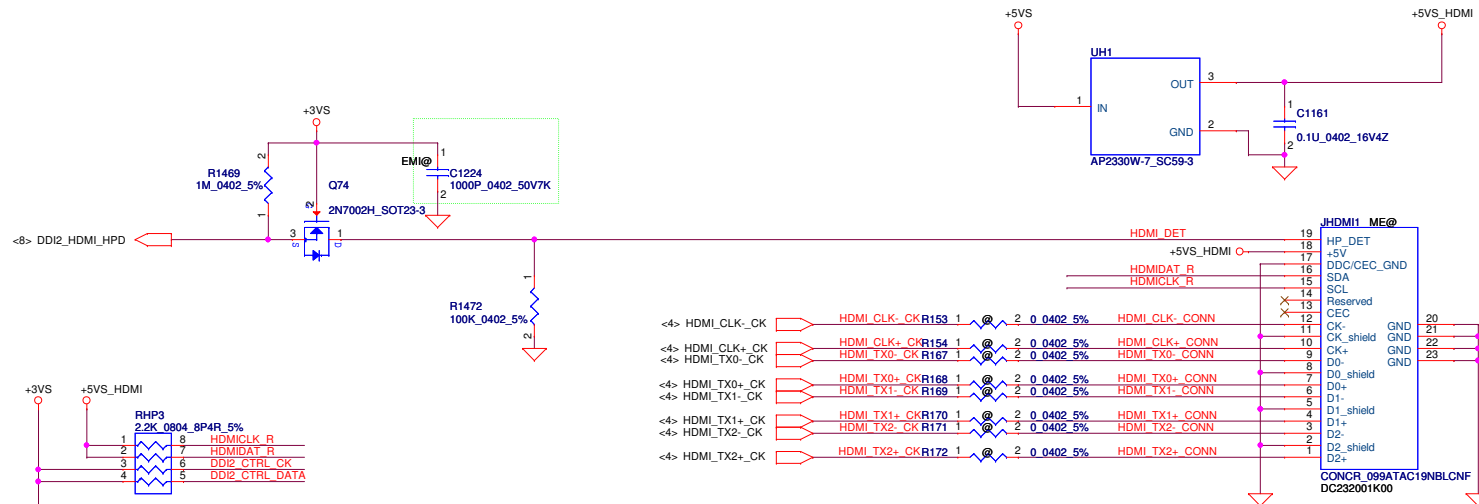


Mini-Express Card for WLAN(Half)

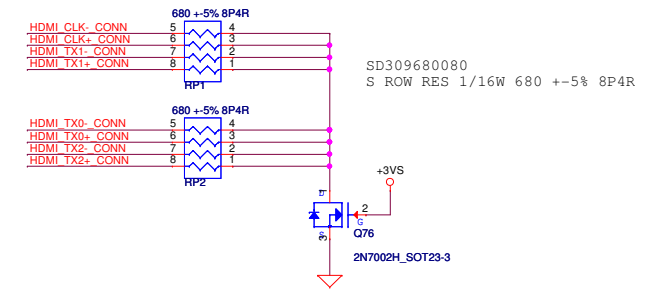
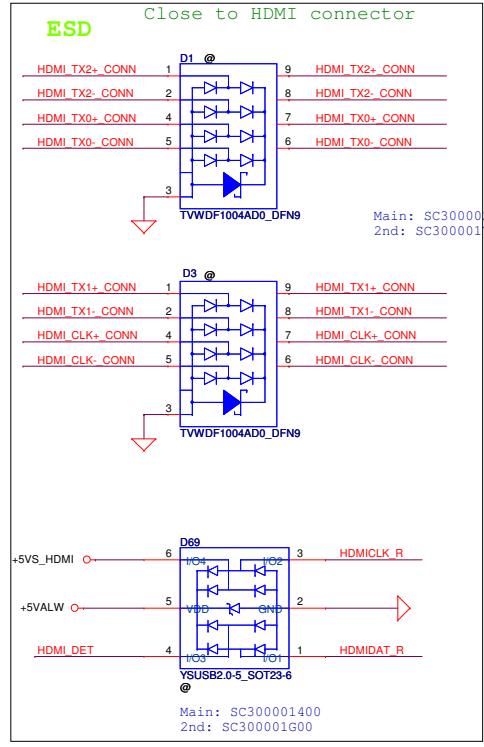
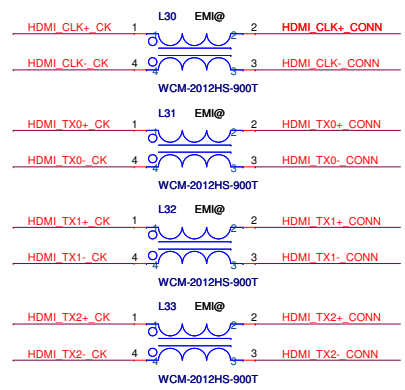
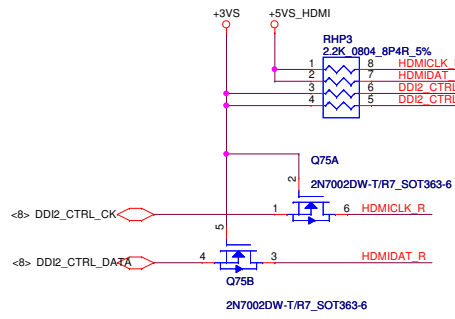


Note: The real behavior of BT_DISABLE are
 BT_DISABLE=LOW, BT=OFF
 BT_DISABLE=HIGH, BT=ON

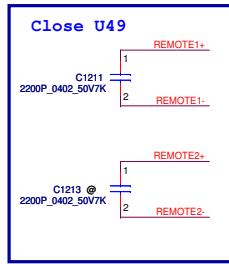
Security Classification	Compal Secret Data		Title
Issued Date	2011/07/21	Deciphered Date	
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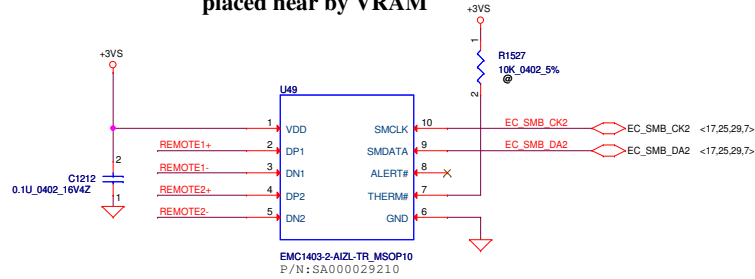
Change Symbol to main source 02/24



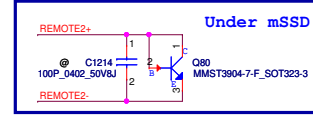
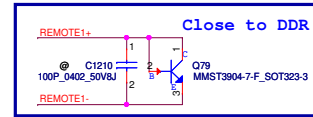
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title
				HDMI CONN
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				Rev 0.2 Sheet 30 of 46



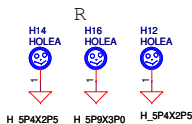
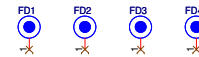
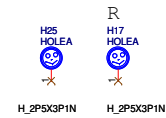
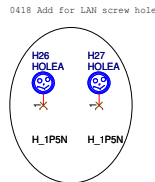
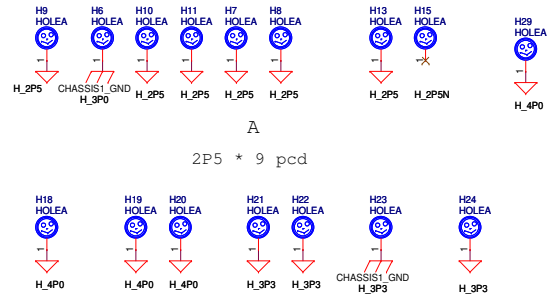
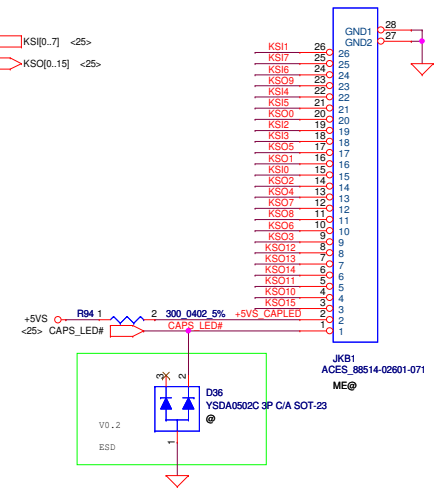
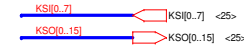
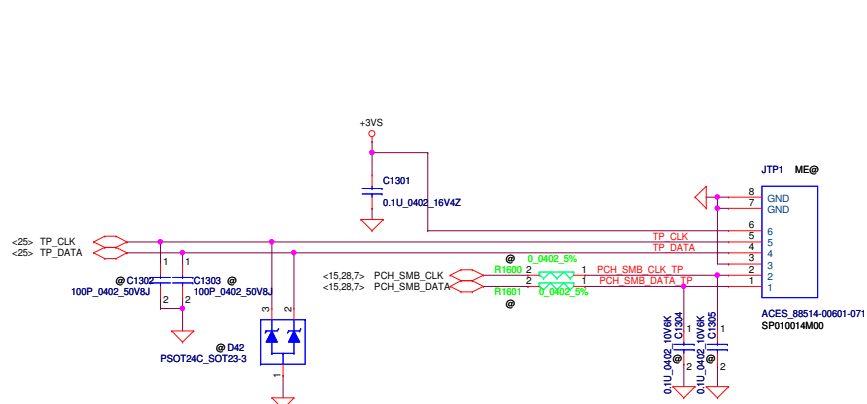
SMSC thermal sensor placed near by VRAM



Address 1001_101xb P/N:SA000029210 F75303M P/N:SA000046C00



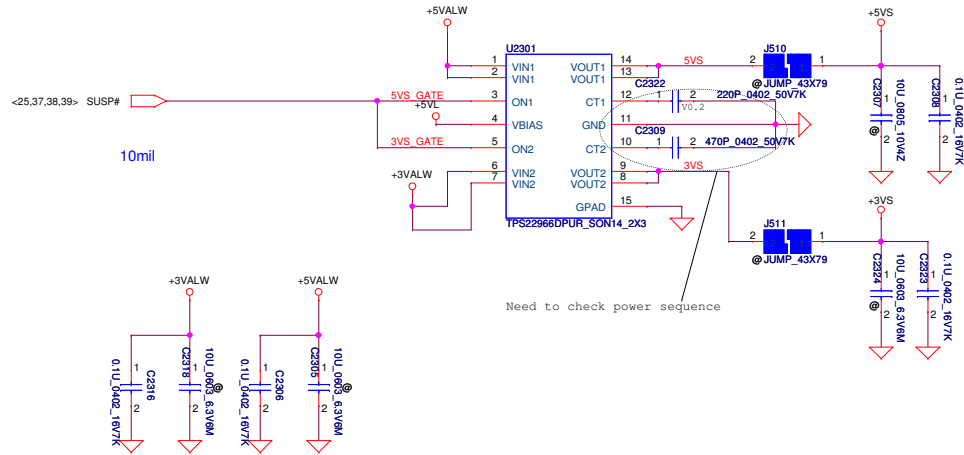
REMOTE1, 2+/-:
Trace width/space:10/10 mil
Trace length:<8"



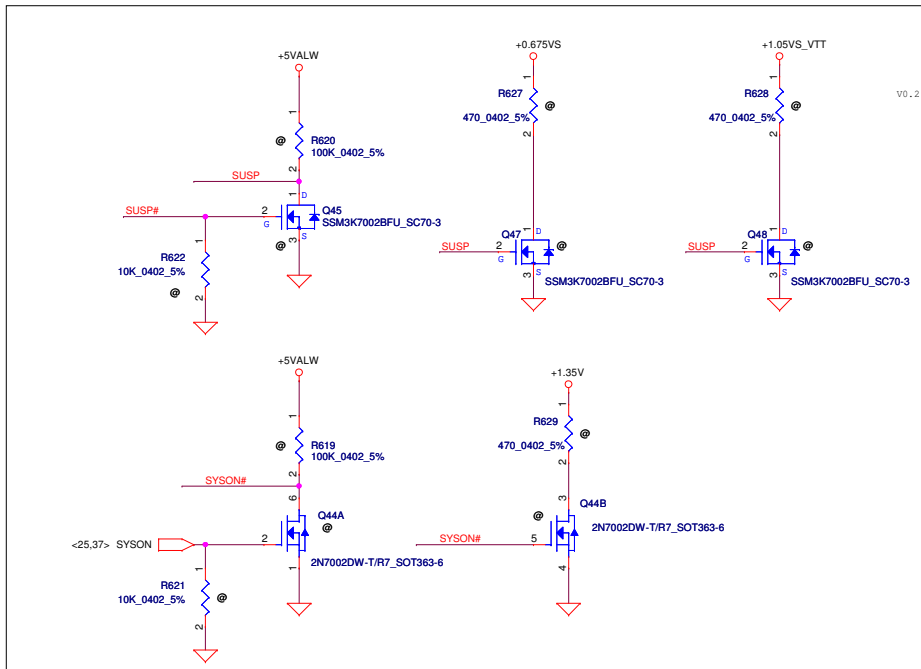
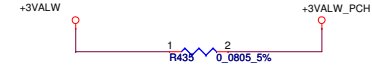
M/B 橢圓孔 M/B KB 橢圓孔

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Size Custom	Document Number	Date: Tuesday, March 19, 2013		Rev 0.2
LA-A321PR02			Sheet 31 of 46	

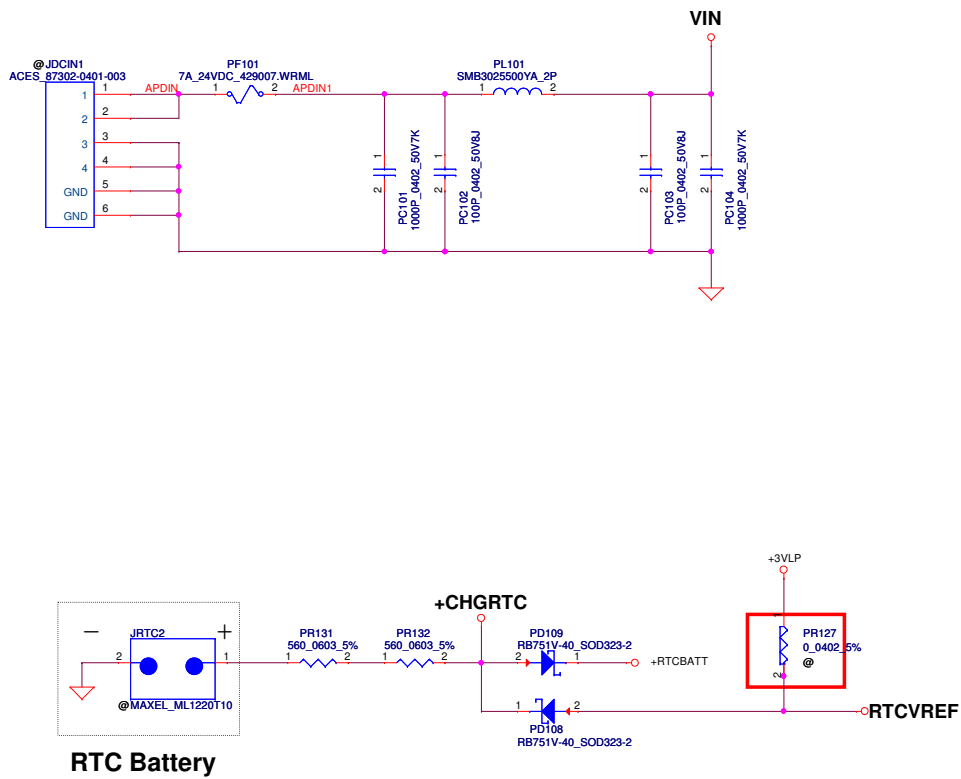
+5VALW TO +5VS
+3VALW TO +3VS



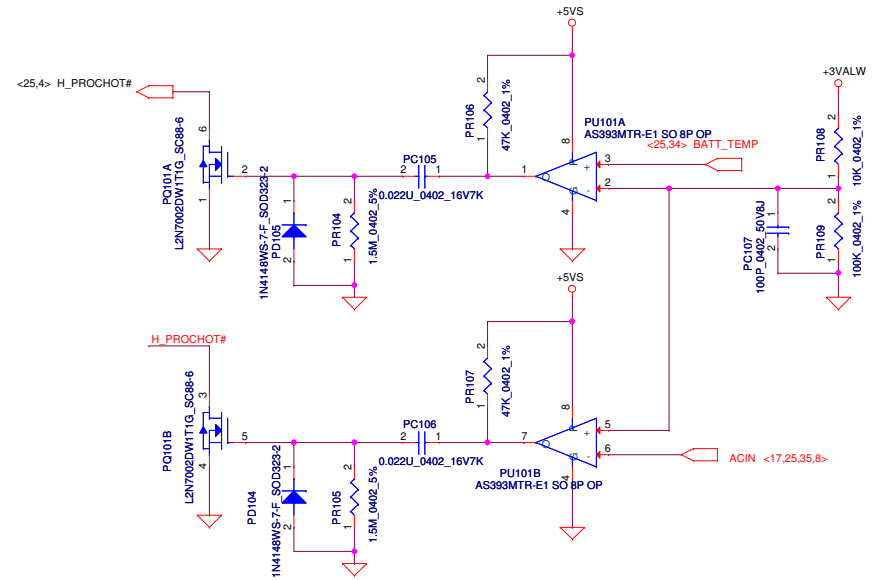
+3VALW TO +3VALW(PCH AUX Power)
+5VALW TO +5VALW(PCH AUX Power)



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				Custom	LA-A321PR02
				Date:	Thursday, March 14, 2013
				Sheet	32 of 46

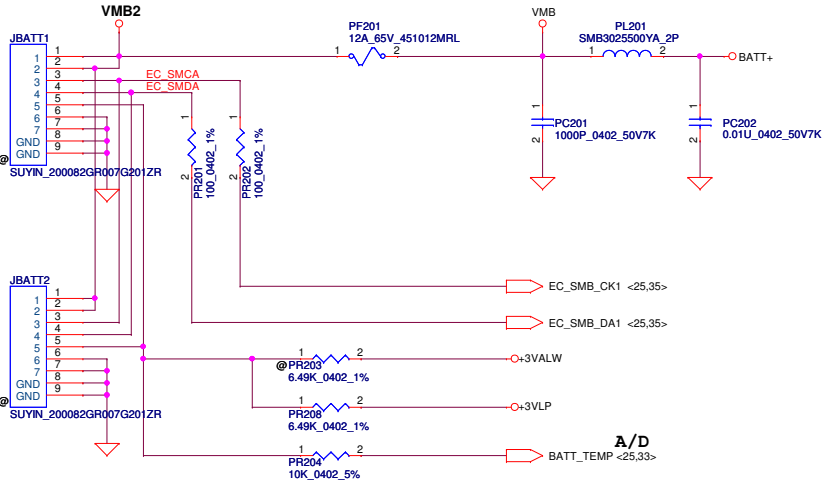


RTC Battery



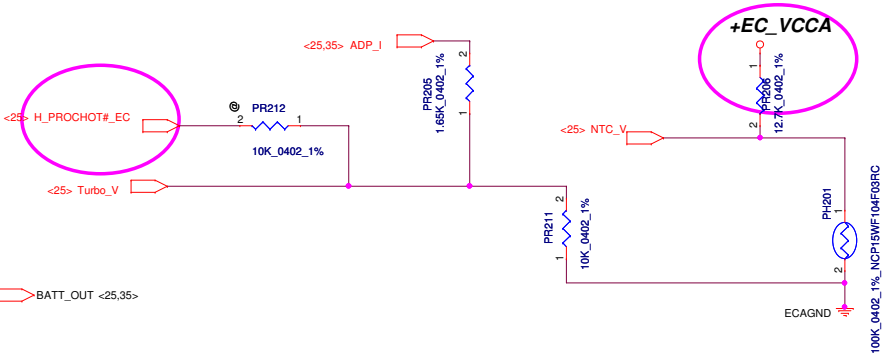
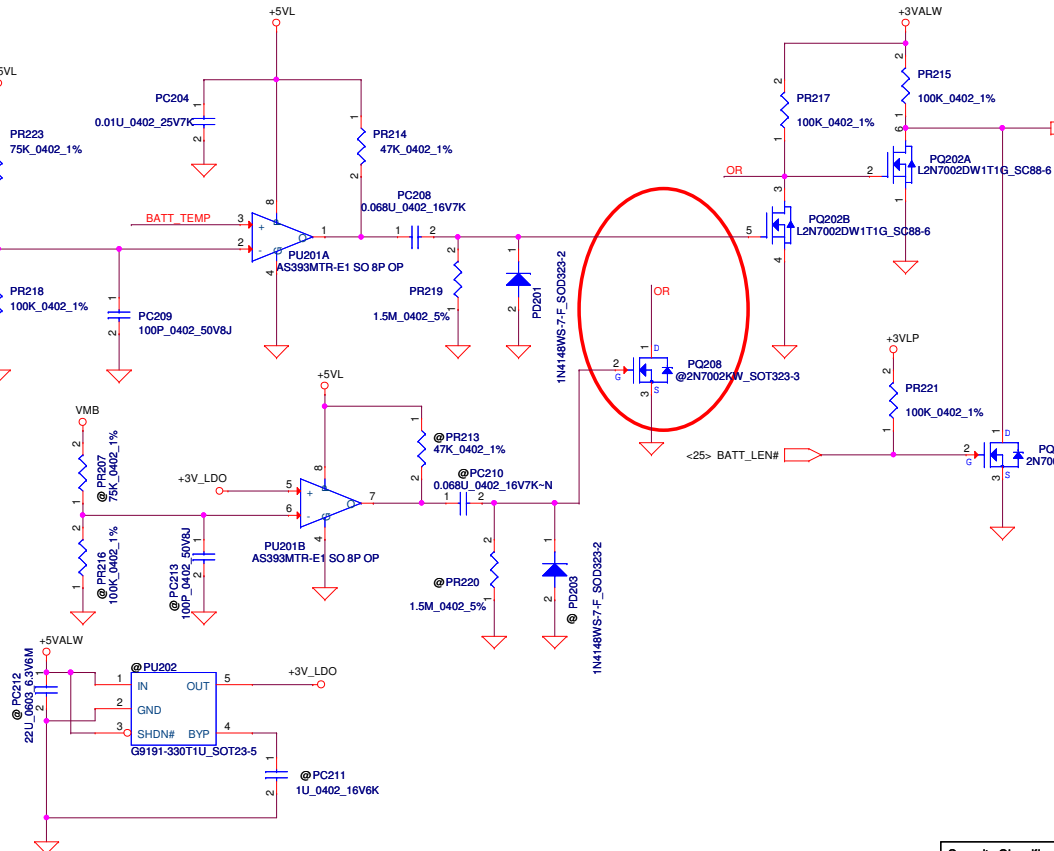
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				LA-A321PR01	0.2
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JBATT1 Just for 13.3"
JBATT2 Just for 14"

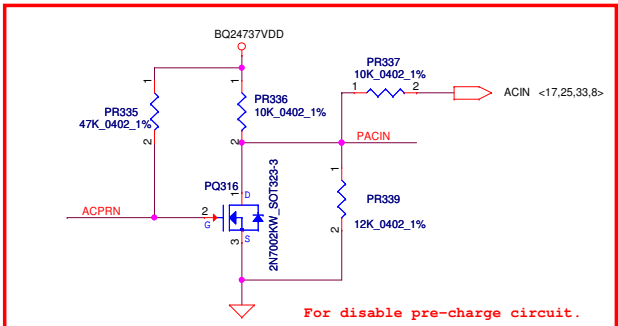
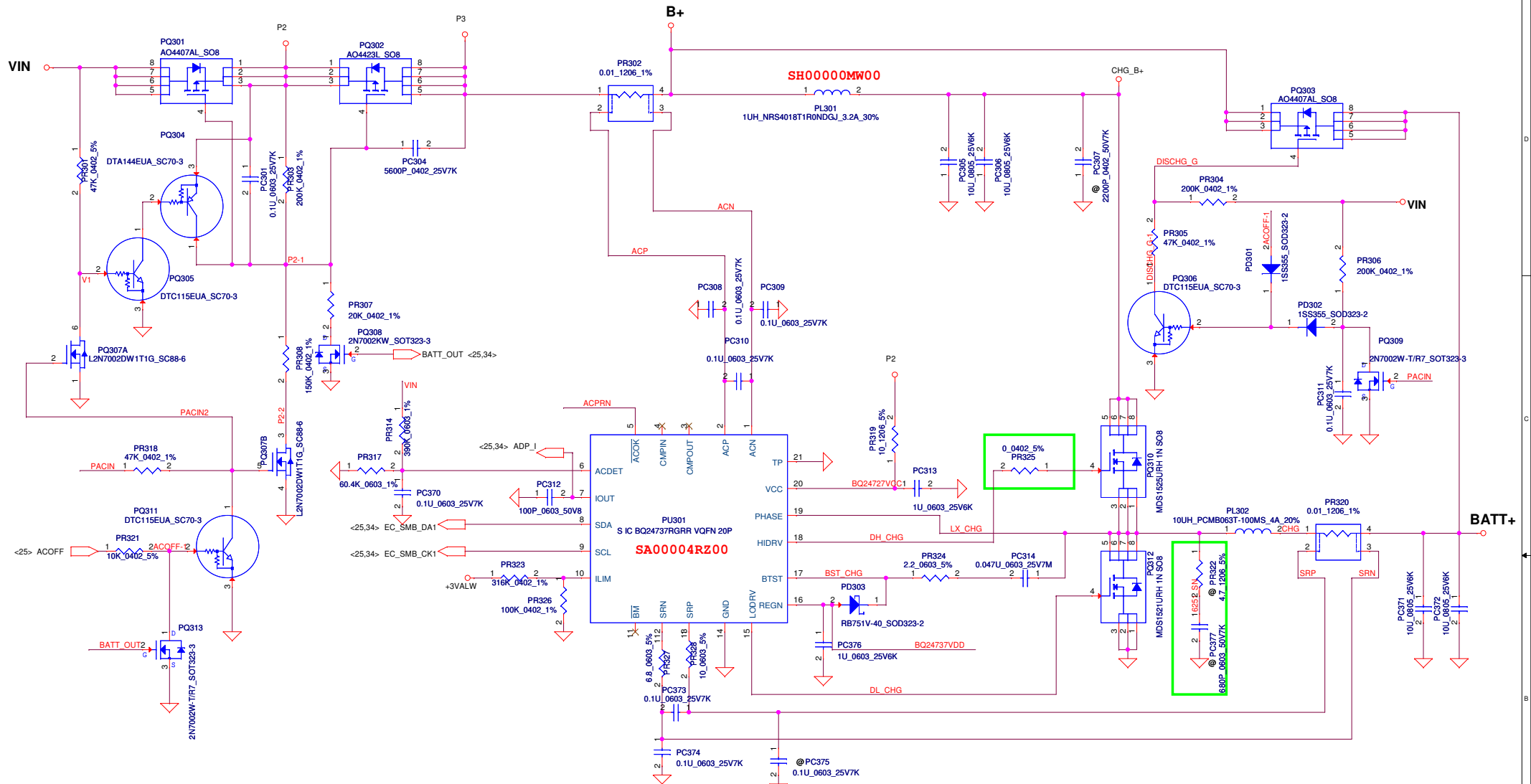


PH1 under CPU bottom side :
CPU thermal protection at 93 +3 degree C
Recovery at 56 +3 degree C

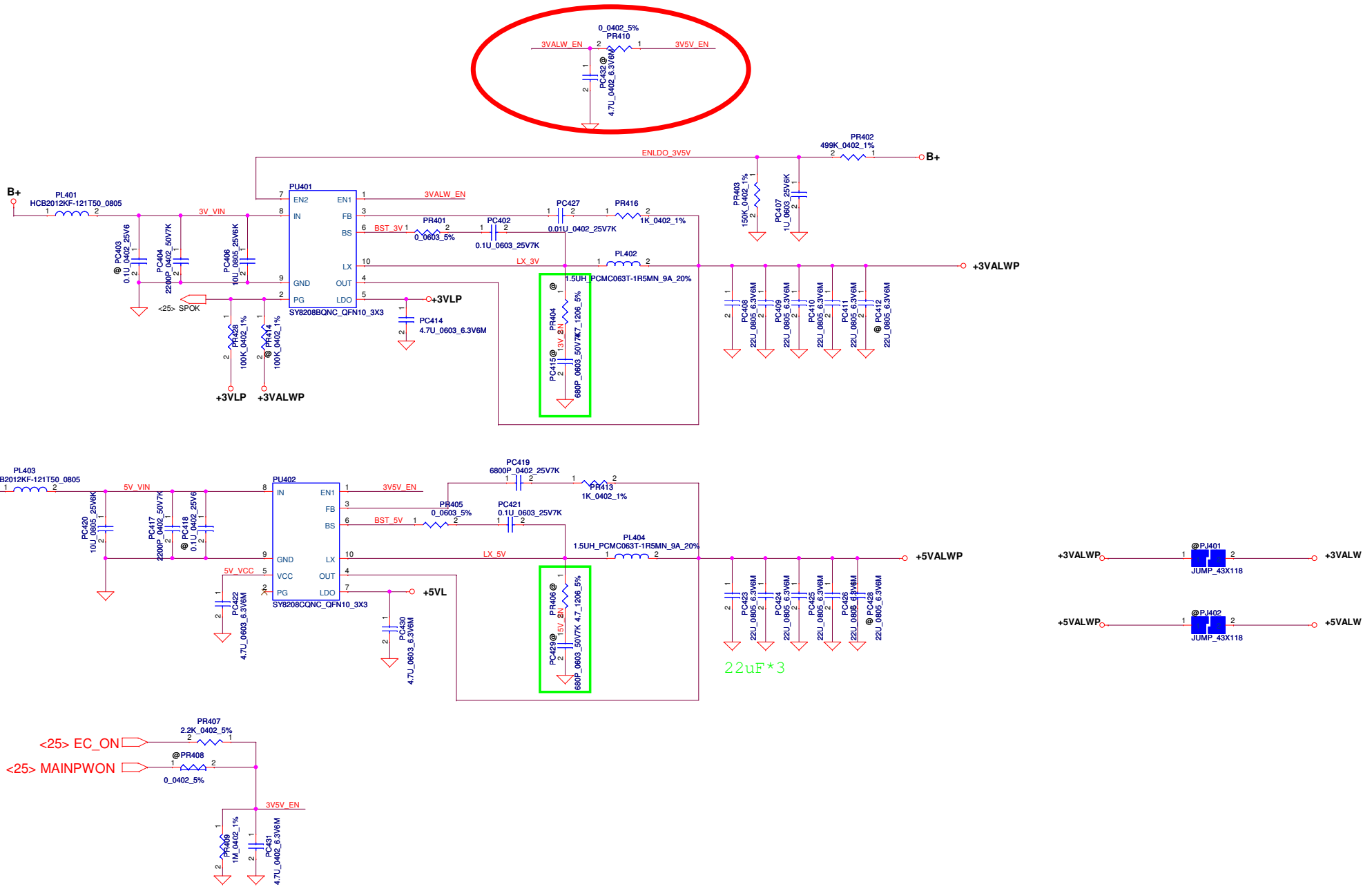
65W(UMA) : PR205=1.65K(SD034165180)



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				LA-A321PR01	0.2
				Date: Thursday, March 14, 2013	Sheet 34 of 46



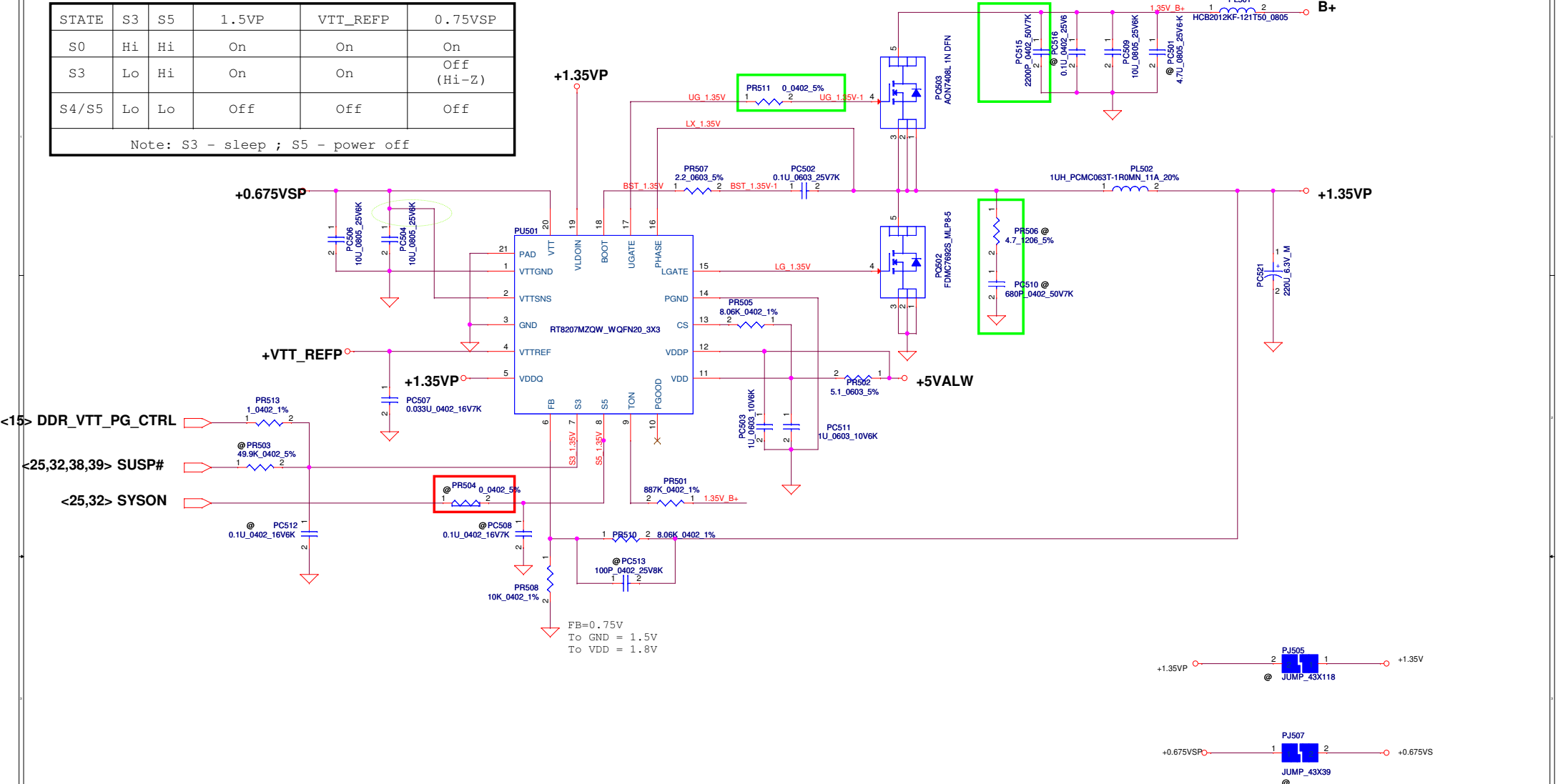
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Issued Date	2010/01/13	Deciphered Date	2012/07/11	Title
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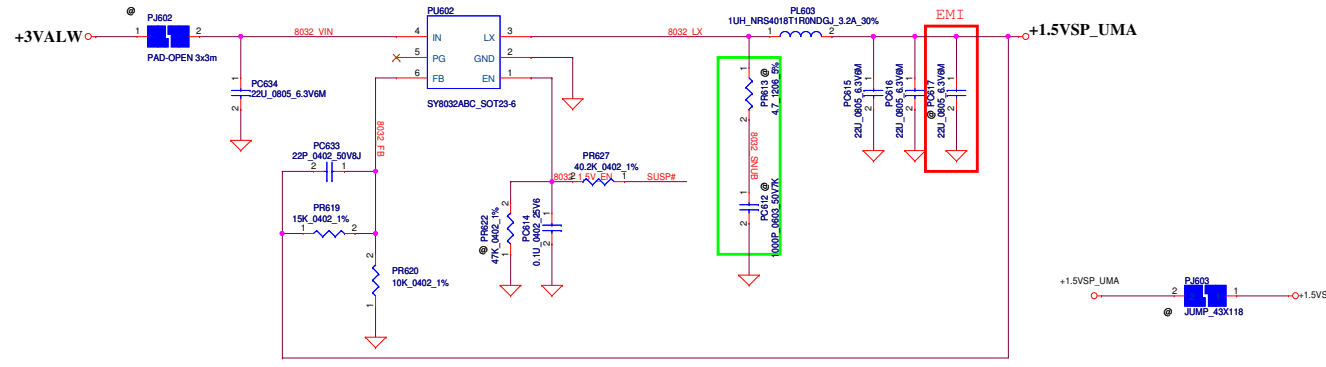
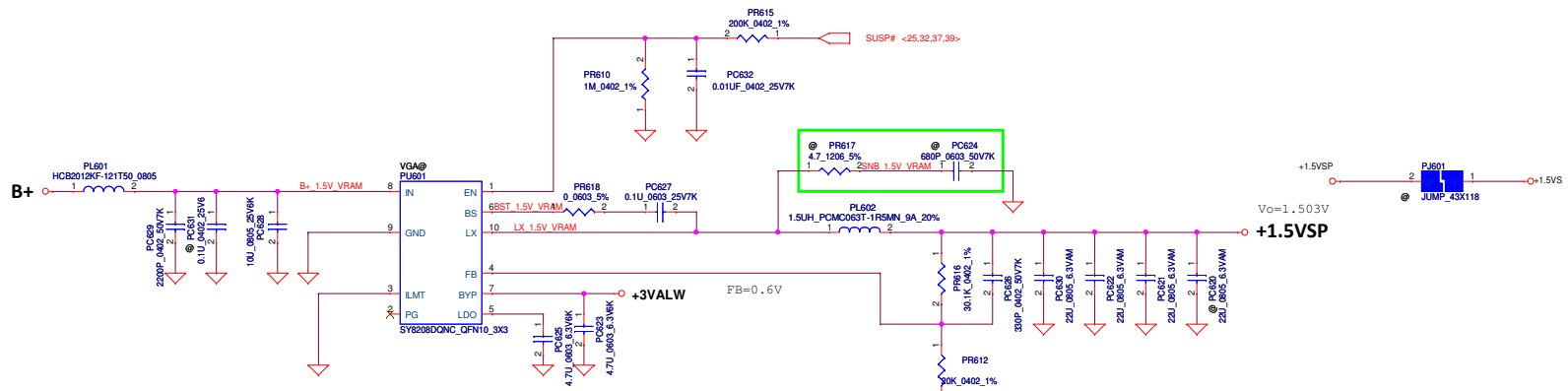
STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off

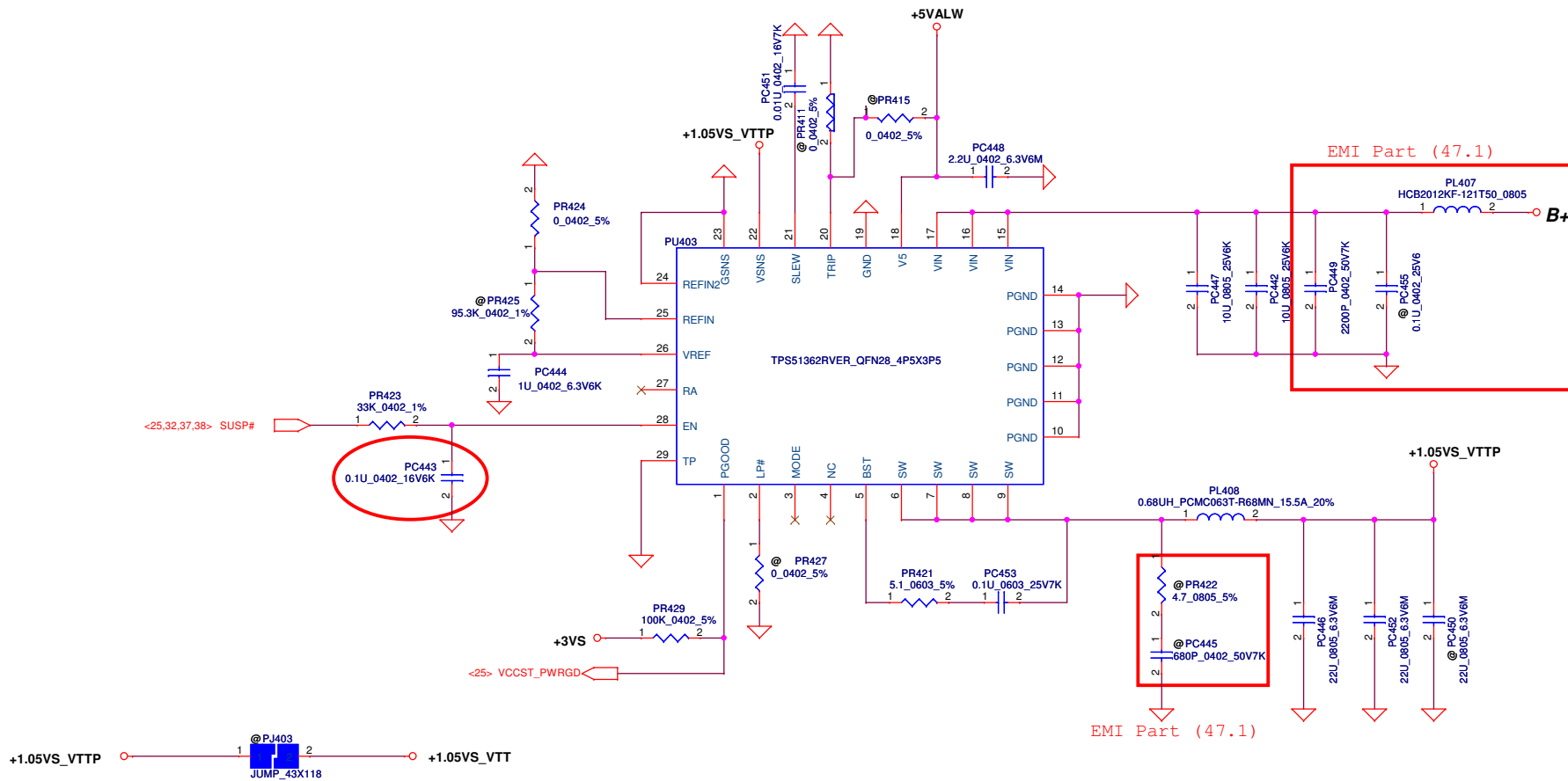


PB=0.75V
 To GND = 1.5V
 To VDD = 1.8V

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				Custom	LA-A321PR01
				Date	Thursday, March 14, 2013
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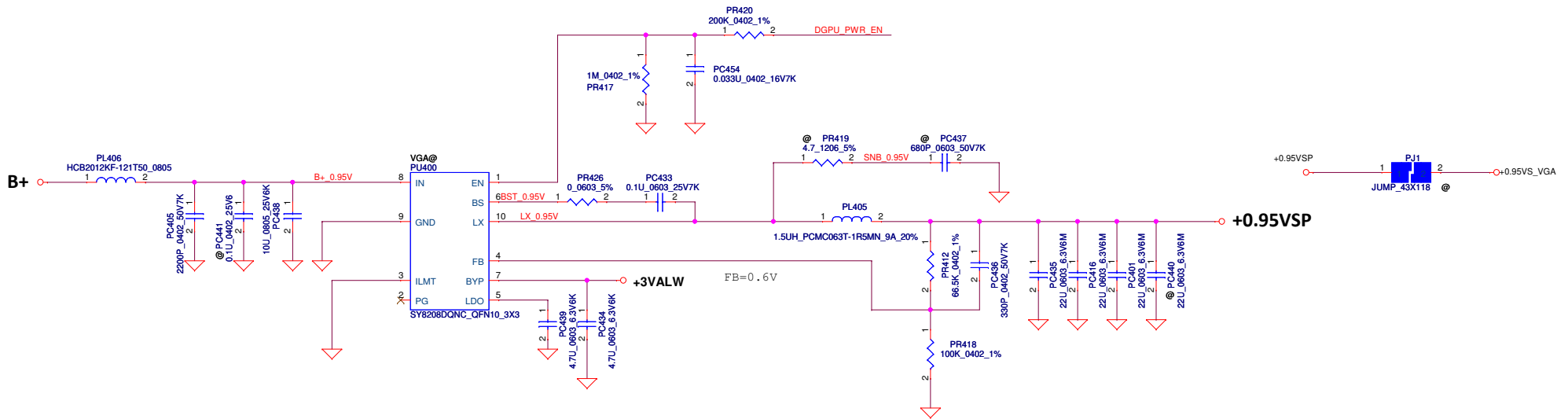
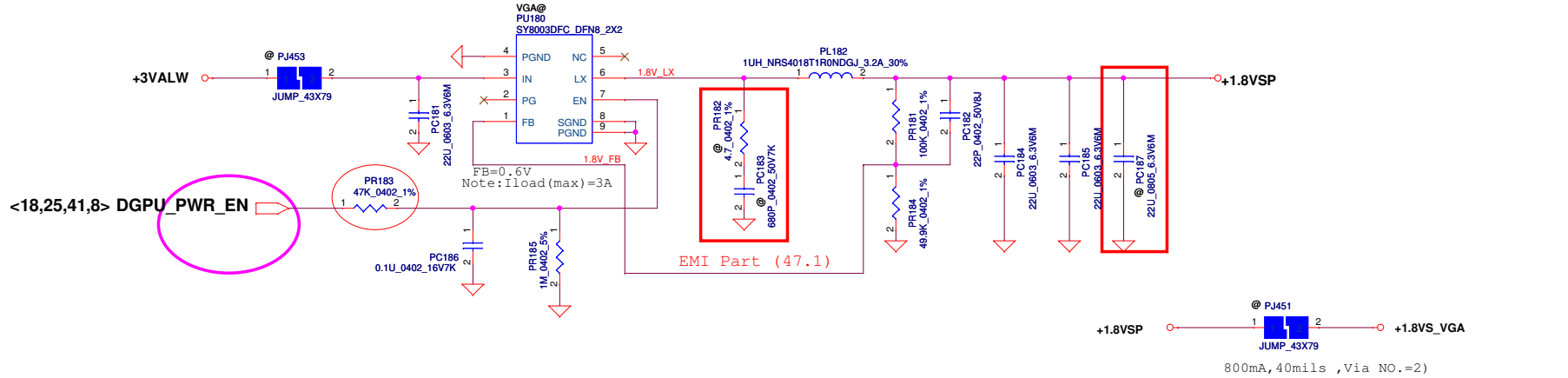


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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title
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Date:	Thursday, March 14, 2013	Sheet	38	of 46

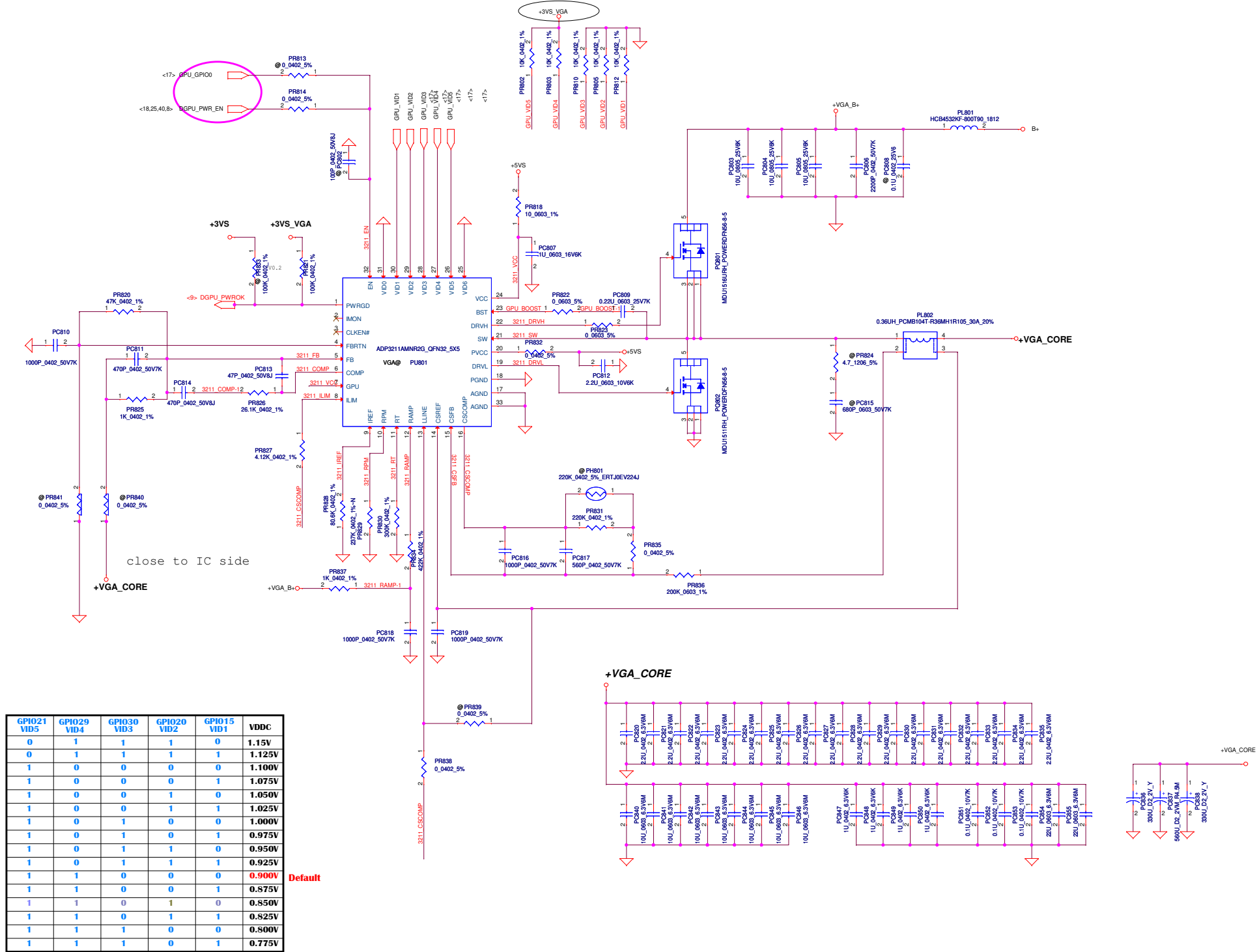


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1.8V controller (35.15), Support component (35.16)



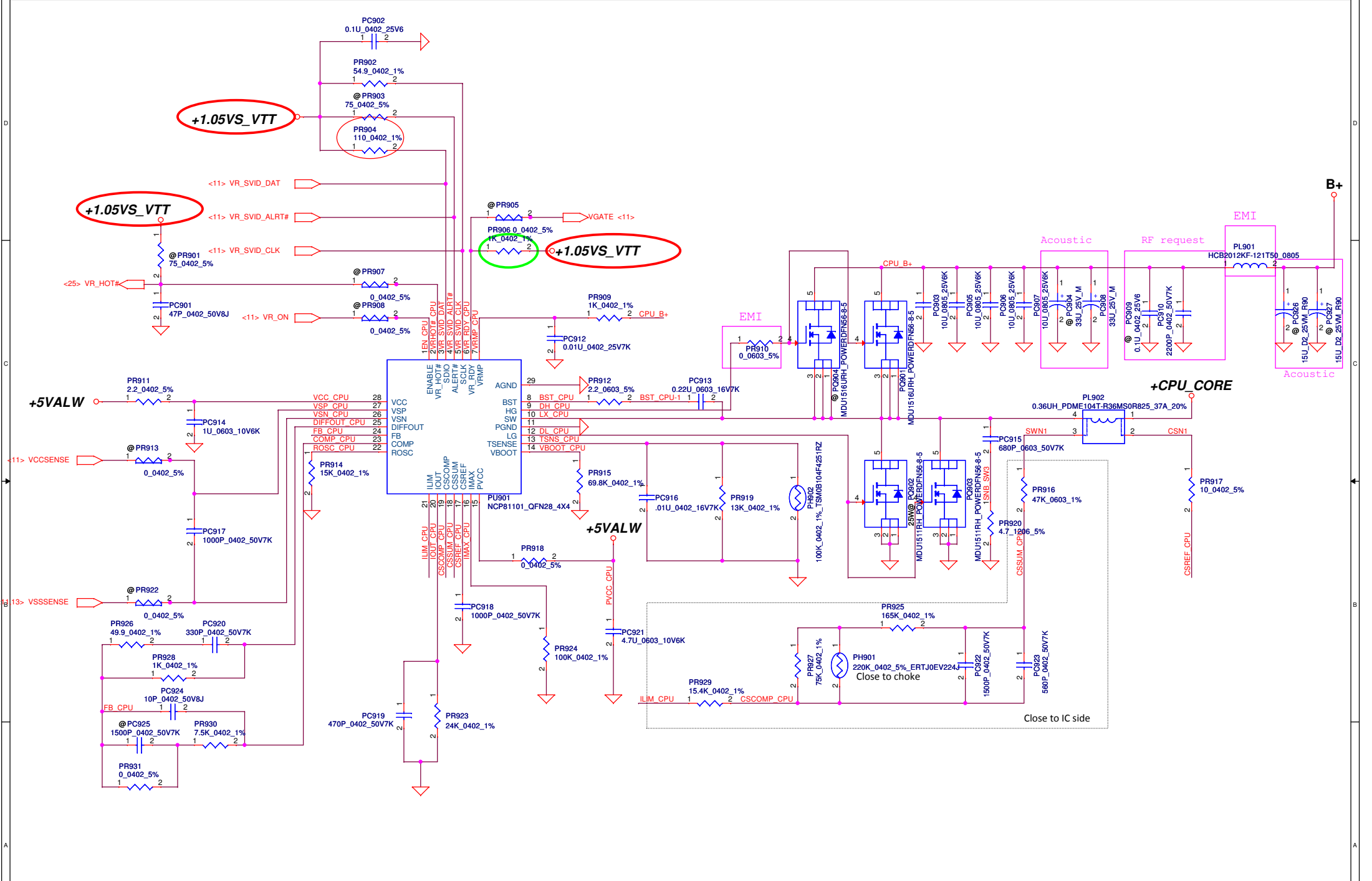
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GPIO21 VID5	GPIO29 VID4	GPIO30 VID3	GPIO20 VID2	GPIO15 VID1	VDDC
0	1	1	1	0	1.15V
0	1	1	1	1	1.125V
1	0	0	0	1	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	1	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Default

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C	LA-A321PRO1	0.2		Thursday, March 14, 2013	
				Sheet	41 of 46

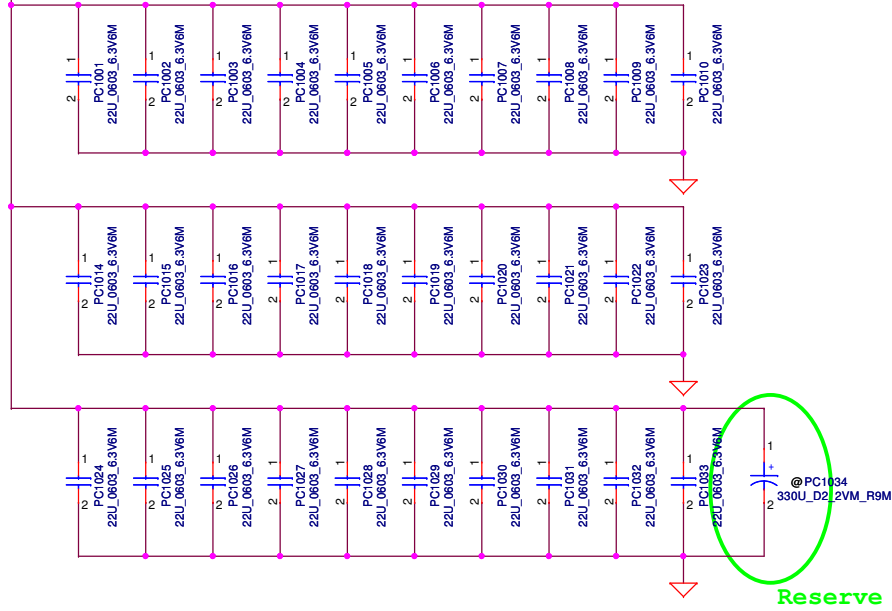


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+CPU_CORE

30 X 22u/0805

RF request



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Version change list (P.I.R. List)

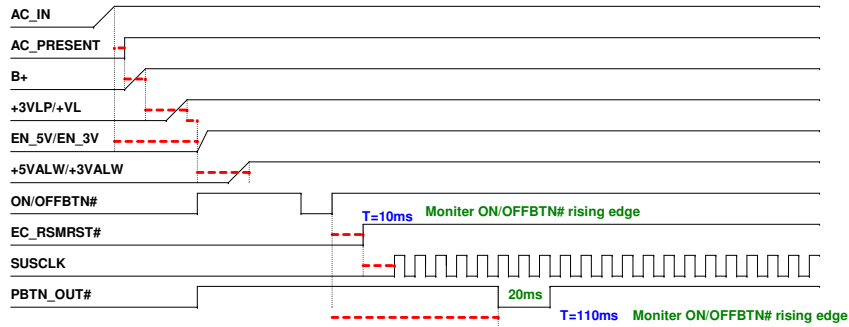
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1	For HW sequence	44	ADD PR821 100K ohm pull high +VS_VGA	3/11	SDV
2	For HW sequence	37	Remove PC512 0.1U_0402	3/11	SDV
3	For HW sequence	39	Change PC443 to 0.1U_0402	3/11	SDV
4	For HW sequence	40	Change PC186 to 0.1uf	2/7	SDV
5	For HW sequence	40	Change PC454 to 0.033uf	2/7	SDV
6	For HW sequence	40	Change PR183 to 47K ohm	2/7	SDV
7					
9					
10					
11					
12					
13					
14					
15					
16					
17					

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				Custom	0.2
				Date: Thursday, March 14, 2013	
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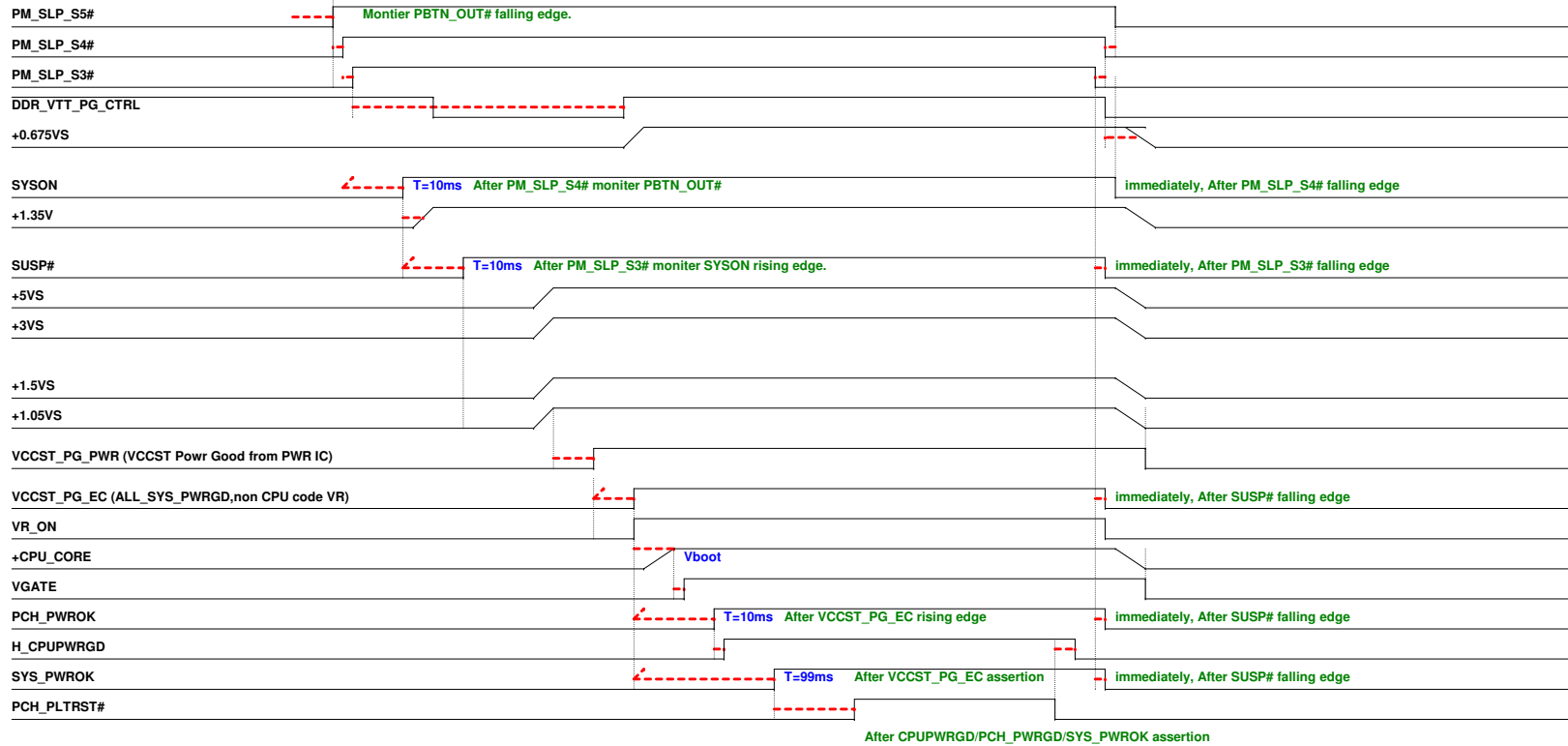
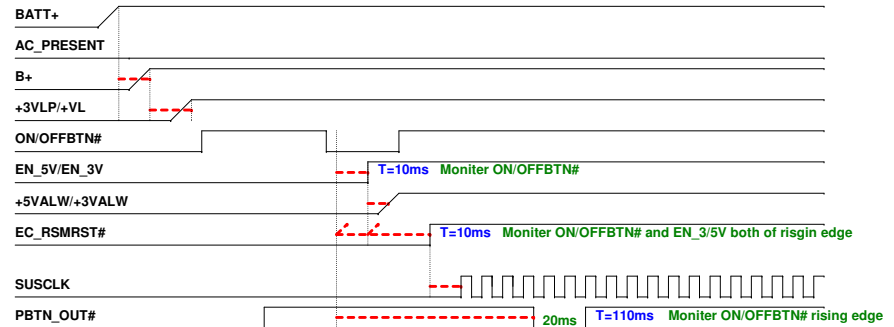
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2					
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4					
5					
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7					
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14					
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16					
17					

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[AC Mode]



[DC Mode]



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