Compal Confidential

Model Name : VIUS3/S4
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BOM P/N:43

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VIUS3/S4 M/B Schematics Document

Intel Ivy Bridge ULV Processor + Panther Point PCH
AMD Seymour XT

2011-12-28

REV:0.1

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.		
Title: Cover Page		
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Compal confidential
File Name :VIUS3/VIUS4

Chief River

AMD Seymour XT
23mm *23mm
VRAM 128MB*16
gDDR3*4

PCI-E X16
Gen 2
UP TO 1G

Intel
IVY Bridge SV/ULV
(Sandy Bridge)
Processor
BGA1023

DDR3-SO-DIMM X1
BANK 0, 1

Dual Channel
DDR3-1066/1333(1.5V) for Sandy Bridge
DDR3-1600(1.5V) for Ivy Bridge

FDI *8
100MHz
2.7GT/s

DMI2 *4
100MHz
5GT/s

Std HDMI
Connector

HDMI 1.4a

LVDS
Connector

PX 5.0

Intel
Panther Point
HM77/HM70
FCBGA 989 Balls
25mm*25mm

6*SATA
(port0,1 Support SATA3)

SATA3.0 HDD CONN

SATA3.0 HDD (SSD)

4*USB3.0

14*USB2.0

USB PORT 3.0 x1 (Left)

USB PORT 2.0 x2 (Right)
IO Board

Card Reader RTS 5178 (2in1)
IO Board

CMOS Camera

BlueTooth CONN

WLAN/WiMAX

WWAN

PCI Express (Half)
Mini card Slot 1
WLAN/WiMAX

USB(WiMAX)

PCI-E(WLAN)

PCI Express (Full)
Mini card Slot 2
SSD

mSATA(SSD)

Gen 2

6*PCI-E x1

HD Audio

SPI ROM
BIOS
4MB*1
2MB*1

LPC BUS

EC
ENE KB9012

WLAN/WiMAX

LAN(10/100/Giga)
Realtek
8105E-VD (10/100)
8111F-VL (Giga)

RJ45 CONN

Touch Pad

Int.KBD

Thermal Sensor
EMC1403

Audio Codec
RealTek
ALC259-VC2

2Channel Speaker

Single Digital MIC

Audio Combo Jack
(APPLE type)
HeadPhone Output
Microphone Input
IO Board

Sub-borad

POWER BOARD

LED BOARD

IO Board

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Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V +1.5V_IO	+5VS +3VS +1.5VS +1.05VS_VTT +CPU_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	Porject	Phase
0	0	0 V	0 V	0 V	G-series	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	G-series	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	G-series	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	G-series	EVT
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	Y-series	EVT
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	Y-series	DVT
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	Y-series	PVT
7	NC	2.500 V	3.300 V	3.300 V	Y-series	MP

EC SM Bus1 address

Address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor F75303M	1001_101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

AMD-GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111Xb (0x9E)

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X

USB Port Table

USB 3.0	USB 2.0		Port	3 External USB Port
xHCI1	EHCI1	UHCI0	0	
xHCI2			1	USB 3.0 Port (Left Side)
xHCI3		UHCI1	2	Mini Card(WLAN)
xHCI4			3	
		UHCI2	4	X (USB PORT disabled on HM70)
			5	X (USB PORT disabled on HM70)
		UHCI3	6	X (USB PORT disabled on HM70)
			7	X (USB PORT disabled on HM70)
	EHCI2	UHCI4	8	USB/B (Right Side USB-BD)
			9	USB/B (Right Side USB-BD)
		UHCI5	10	USB Port (Right Side CR-BD)
			11	Camera (LVDS)
		UHCI6	12	X (USB PORT disabled on HM70)
			13	X (USB PORT disabled on HM70)

HM70 Disable xHCI3,xHCI4

BOM Structure Table

BTO Item	BOM Structure
INTEL UMA only	UMA@
GPU:Seymour XT	PX@ PX5@
HDMI	HDMI@
HDD1 (HM77 SATA 3.0)	HDD1@
HDD2 (HM70 SATA 2.0)	HDD2@
Interna-Intel-USB3.0	IU3@
Interna-Intel-USB2.0	IU2@
Blue Tooth	BT@
10/100 LAN	8105E@
GIGA LAN	8111F@
Connector	ME@
45 LEVEL	45@
Unpop	@

SATA Port Table

	HM77	HM70	
SATA P0	GEN3/2/1	GEN3/2/1	SSD
SATA P1	GEN3/2/1	Disable	HDD (HM77)
SATA P2	GEN2/1	GEN2/1	HDD (HM70)
SATA P3	GEN2/1	Disable	
SATA P4	GEN2/1	GEN2/1	
SATA P5	GEN2/1	GEN2/1	

HM70 Disable P1,P3

PCIe Port Table

	HM77	HM70	
PCIe P1	Enable	Enable	LAN
PCIe P2	Enable	Enable	WLAN
PCIe P3	Enable	Enable	
PCIe P4	Enable	Enable	
PCIe P5	Enable	Disable	
PCIe P6	Enable	Disable	
PCIe P7	Enable	Disable	
PCIe P8	Enable	Disable	

HM70 Disable P5,P6,P7,P8

Power-Up/Down Sequence

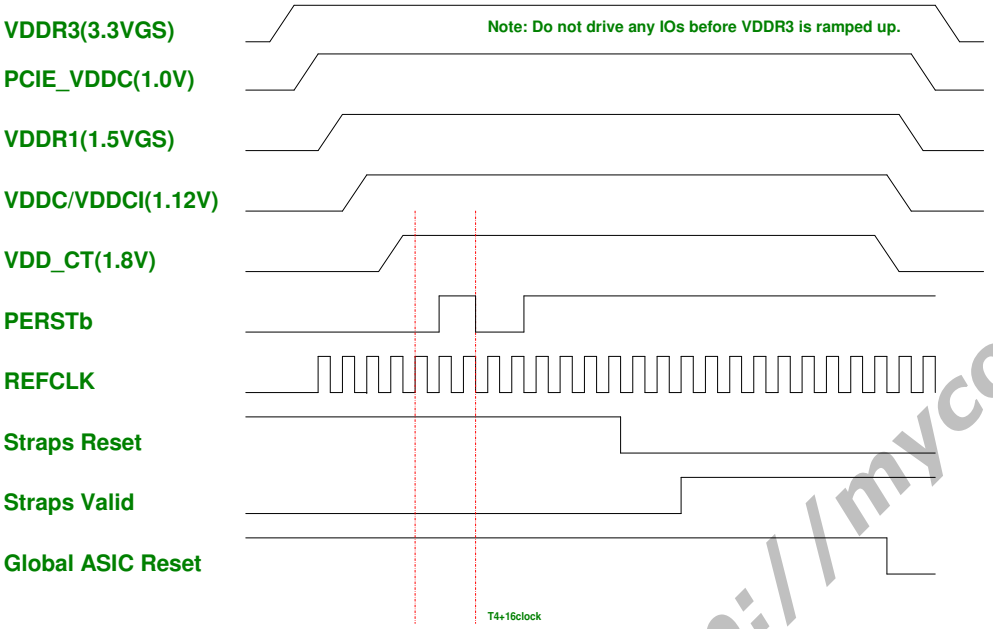
1. All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.

2. VDDR3 should ramp-up before or simultaneously with VDDC.

3. For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.

4. The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.

5.VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)



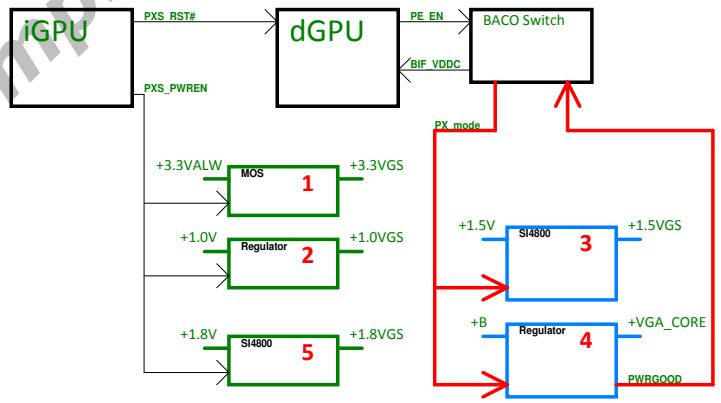
Without BACO option :

PXS_RST# : Low -> Reset dGPU ; High ->Normal operation
PXS_PWREN : Low -> dGPU Power OFF ; High -> dGPU Power ON

BACO option :

PXS_RST# : High ->Normal operation (dGPU is not reset on BACO mode)
PXS_PWREN : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode) BIF_VDDC=VGA_CORE When GPU enable BIF_VDDC=1.0V When BACO	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A



CPU part

UCPU1 CPU1@ — I3_3217 1.8G — SA00005L510
UCPU1 CPU2@ — I5_3427 1.8G — SA00005L900
UCPU1 CPU3@ — I5_2557 1.4G — SA00004VZ00
UCPU1 CPU4@ — 977 1.4G — SA00005BJ40

PCB part

ZZZ5 — PCB 0R LA-8951P REV0 M/B — DA60000TO00

ZZZ2 — Hynix S512@ — X7641338L01
ZZZ1 — Hynix H512@ — X7641338L02
ZZZ3 — Hynix S1G@ — X7641338L03
ZZZ4 — Hynix H1G@ — X7641338L04

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PEG_ICOMPI and RCOMPO signals should be shorted and routed
with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils
- typical impedance = 14.5 mohms

Layout placement: Place close to U8 (GPU)

+1.05VS_VTT

R249 24.9_0402_1%

W=12mil L=500mil S=15mil

PEG_COMP

UCPU1A

PEG_ICOMPI
PEG_ICOMPO
PEG_RCOMPO

DMI

[15] DMI_CRX_PTX_N0 M2 DMI_RX#[0]
[15] DMI_CRX_PTX_N1 P6 DMI_RX#[1]
[15] DMI_CRX_PTX_N2 P1 DMI_RX#[2]
[15] DMI_CRX_PTX_N3 P10 DMI_RX#[3]

[15] DMI_CRX_PTX_P0 N3 DMI_RX[0]
[15] DMI_CRX_PTX_P1 P7 DMI_RX[1]
[15] DMI_CRX_PTX_P2 P3 DMI_RX[2]
[15] DMI_CRX_PTX_P3 P11 DMI_RX[3]

[15] DMI_CTX_PRX_N0 K1 DMI_TX#[0]
[15] DMI_CTX_PRX_N1 M8 DMI_TX#[1]
[15] DMI_CTX_PRX_N2 N4 DMI_TX#[2]
[15] DMI_CTX_PRX_N3 R2 DMI_TX#[3]

[15] DMI_CTX_PRX_P0 K3 DMI_TX[0]
[15] DMI_CTX_PRX_P1 M7 DMI_TX[1]
[15] DMI_CTX_PRX_P2 P4 DMI_TX[2]
[15] DMI_CTX_PRX_P3 T3 DMI_TX[3]

Intel(R) FDI

U7
[15] FDI_CTX_PRX_N0 W11 FDI0_TX#[0]
[15] FDI_CTX_PRX_N1 W1 FDI0_TX#[1]
[15] FDI_CTX_PRX_N2 AA6 FDI0_TX#[2]
[15] FDI_CTX_PRX_N3 W6 FDI0_TX#[3]
[15] FDI_CTX_PRX_N4 V4 FDI1_TX#[0]
[15] FDI_CTX_PRX_N5 Y2 FDI1_TX#[1]
[15] FDI_CTX_PRX_N6 AC9 FDI1_TX#[2]
[15] FDI_CTX_PRX_N7 FDI1_TX#[3]

U6
[15] FDI_CTX_PRX_P0 W10 FDI0_TX[0]
[15] FDI_CTX_PRX_P1 W3 FDI0_TX[1]
[15] FDI_CTX_PRX_P2 AA7 FDI0_TX[2]
[15] FDI_CTX_PRX_P3 W7 FDI0_TX[3]
[15] FDI_CTX_PRX_P4 T4 FDI1_TX[0]
[15] FDI_CTX_PRX_P5 AA3 FDI1_TX[1]
[15] FDI_CTX_PRX_P6 AC8 FDI1_TX[2]
[15] FDI_CTX_PRX_P7 FDI1_TX[3]

[15] FDI_FSYNC0 AA11 FDI0_FSYNC
[15] FDI_FSYNC1 AC12 FDI1_FSYNC

U11
[15] FDI_INT FDI_INT

[15] FDI_LSYNC0 AA10 FDI0_LSYNC
[15] FDI_LSYNC1 AG8 FDI1_LSYNC

PCI EXPRESS -- GRAPHICS

PEG_RX#[0] H22 PEG_GTX_C_HRX_N0
PEG_RX#[1] J21 PEG_GTX_C_HRX_N1
PEG_RX#[2] B22 PEG_GTX_C_HRX_N2
PEG_RX#[3] D21 PEG_GTX_C_HRX_N3
PEG_RX#[4] A19 PEG_GTX_C_HRX_N4
PEG_RX#[5] D17 PEG_GTX_C_HRX_N5
PEG_RX#[6] B14 PEG_GTX_C_HRX_N6
PEG_RX#[7] D13 PEG_GTX_C_HRX_N7
PEG_RX#[8] A11 PEG_GTX_C_HRX_N8
PEG_RX#[9] B10 PEG_GTX_C_HRX_N9
PEG_RX#[10] G8 PEG_GTX_C_HRX_N10
PEG_RX#[11] A8 PEG_GTX_C_HRX_N11
PEG_RX#[12] B6 PEG_GTX_C_HRX_N12
PEG_RX#[13] H8 PEG_GTX_C_HRX_N13
PEG_RX#[14] E5 PEG_GTX_C_HRX_N14
PEG_RX#[15] K7 PEG_GTX_C_HRX_N15

PEG_RX[0] K22 PEG_GTX_C_HRX_P0
PEG_RX[1] K19 PEG_GTX_C_HRX_P1
PEG_RX[2] C21 PEG_GTX_C_HRX_P2
PEG_RX[3] D19 PEG_GTX_C_HRX_P3
PEG_RX[4] C19 PEG_GTX_C_HRX_P4
PEG_RX[5] D16 PEG_GTX_C_HRX_P5
PEG_RX[6] C13 PEG_GTX_C_HRX_P6
PEG_RX[7] D12 PEG_GTX_C_HRX_P7
PEG_RX[8] C11 PEG_GTX_C_HRX_P8
PEG_RX[9] C9 PEG_GTX_C_HRX_P9
PEG_RX[10] F8 PEG_GTX_C_HRX_P10
PEG_RX[11] C8 PEG_GTX_C_HRX_P11
PEG_RX[12] C5 PEG_GTX_C_HRX_P12
PEG_RX[13] H6 PEG_GTX_C_HRX_P13
PEG_RX[14] F6 PEG_GTX_C_HRX_P14
PEG_RX[15] K6 PEG_GTX_C_HRX_P15

PEG_TX#[0] G22 PEG_HTX_GRX_N0
PEG_TX#[1] C23 PEG_HTX_GRX_N1
PEG_TX#[2] D23 PEG_HTX_GRX_N2
PEG_TX#[3] F21 PEG_HTX_GRX_N3
PEG_TX#[4] H19 PEG_HTX_GRX_N4
PEG_TX#[5] C17 PEG_HTX_GRX_N5
PEG_TX#[6] K15 PEG_HTX_GRX_N6
PEG_TX#[7] F17 PEG_HTX_GRX_N7
PEG_TX#[8] F14 PEG_HTX_GRX_N8
PEG_TX#[9] A15 PEG_HTX_GRX_N9
PEG_TX#[10] J14 PEG_HTX_GRX_N10
PEG_TX#[11] H13 PEG_HTX_GRX_N11
PEG_TX#[12] M10 PEG_HTX_GRX_N12
PEG_TX#[13] F10 PEG_HTX_GRX_N13
PEG_TX#[14] D9 PEG_HTX_GRX_N14
PEG_TX#[15] J4 PEG_HTX_GRX_N15

PEG_TX[0] F22 PEG_HTX_GRX_P0
PEG_TX[1] A23 PEG_HTX_GRX_P1
PEG_TX[2] D24 PEG_HTX_GRX_P2
PEG_TX[3] E21 PEG_HTX_GRX_P3
PEG_TX[4] G19 PEG_HTX_GRX_P4
PEG_TX[5] B18 PEG_HTX_GRX_P5
PEG_TX[6] K17 PEG_HTX_GRX_P6
PEG_TX[7] G17 PEG_HTX_GRX_P7
PEG_TX[8] E14 PEG_HTX_GRX_P8
PEG_TX[9] C15 PEG_HTX_GRX_P9
PEG_TX[10] K13 PEG_HTX_GRX_P10
PEG_TX[11] G13 PEG_HTX_GRX_P11
PEG_TX[12] K10 PEG_HTX_GRX_P12
PEG_TX[13] G10 PEG_HTX_GRX_P13
PEG_TX[14] D8 PEG_HTX_GRX_P14
PEG_TX[15] K4 PEG_HTX_GRX_P15

G3 G1 G4

C259 C276 C257 C274 C254 C272 C252 C270 C250 C268 C248 C267 C246 C264 C244 C262
C258 C277 C256 C275 C255 C273 C253 C271 C251 C269 C249 C266 C247 C265 C245 C263
C562 C582 C564 C584 C566 C587 C568 C589 C570 C591 C572 C593 C574 C594 C576 C597
C561 C583 C563 C585 C565 C586 C567 C588 C569 C590 C571 C592 C573 C595 C575 C596

1 2 PX@ 0.22U_0402_6.3V6K

PEG_GTX_HRX_N0 PEG_GTX_HRX_N1 PEG_GTX_HRX_N2 PEG_GTX_HRX_N3 PEG_GTX_HRX_N4 PEG_GTX_HRX_N5 PEG_GTX_HRX_N6 PEG_GTX_HRX_N7 PEG_GTX_HRX_N8 PEG_GTX_HRX_N9 PEG_GTX_HRX_N10 PEG_GTX_HRX_N11 PEG_GTX_HRX_N12 PEG_GTX_HRX_N13 PEG_GTX_HRX_N14 PEG_GTX_HRX_N15
PEG_GTX_HRX_P0 PEG_GTX_HRX_P1 PEG_GTX_HRX_P2 PEG_GTX_HRX_P3 PEG_GTX_HRX_P4 PEG_GTX_HRX_P5 PEG_GTX_HRX_P6 PEG_GTX_HRX_P7 PEG_GTX_HRX_P8 PEG_GTX_HRX_P9 PEG_GTX_HRX_P10 PEG_GTX_HRX_P11 PEG_GTX_HRX_P12 PEG_GTX_HRX_P13 PEG_GTX_HRX_P14 PEG_GTX_HRX_P15
PEG_HTX_C_GRX_N0 PEG_HTX_C_GRX_N1 PEG_HTX_C_GRX_N2 PEG_HTX_C_GRX_N3 PEG_HTX_C_GRX_N4 PEG_HTX_C_GRX_N5 PEG_HTX_C_GRX_N6 PEG_HTX_C_GRX_N7 PEG_HTX_C_GRX_N8 PEG_HTX_C_GRX_N9 PEG_HTX_C_GRX_N10 PEG_HTX_C_GRX_N11 PEG_HTX_C_GRX_N12 PEG_HTX_C_GRX_N13 PEG_HTX_C_GRX_N14 PEG_HTX_C_GRX_N15
PEG_HTX_C_GRX_P0 PEG_HTX_C_GRX_P1 PEG_HTX_C_GRX_P2 PEG_HTX_C_GRX_P3 PEG_HTX_C_GRX_P4 PEG_HTX_C_GRX_P5 PEG_HTX_C_GRX_P6 PEG_HTX_C_GRX_P7 PEG_HTX_C_GRX_P8 PEG_HTX_C_GRX_P9 PEG_HTX_C_GRX_P10 PEG_HTX_C_GRX_P11 PEG_HTX_C_GRX_P12 PEG_HTX_C_GRX_P13 PEG_HTX_C_GRX_P14 PEG_HTX_C_GRX_P15

PEG_GTX_HRX_N[0..15] [22]
PEG_GTX_HRX_P[0..15] [22]
PEG_HTX_C_GRX_N[0..15] [22]
PEG_HTX_C_GRX_P[0..15] [22]

Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIE Gen3 (8GT/s)

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms
can't be left floating
,even if disable eDP function...

+1.05VS_VTT

R247 24.9_0402_1%

W=12mil L=500mil S=15mil

EDP_COMP

eDP

AF3 eDP_COMPIO
AD2 eDP_ICOMPO
AG11 eDP_HPD#

AG4 AF4 eDP_AUX#
eDP_AUX

AC3 AC4 AE11 AE7 eDP_TX#[0] eDP_TX#[1] eDP_TX#[2] eDP_TX#[3]

AC1 AA4 AE10 AE6 eDP_TX[0] eDP_TX[1] eDP_TX[2] eDP_TX[3]

IVY-BRIDGE_BGA1023

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Title: PROCESSOR(1/7) DMI,FDI,PEG

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PCH->CPU
UNCOREPWRGOOD:非CORE外的電OK
SM_DRAMPWROK:DRAM power ok
RESET#:部ok後請CPU做reset

Follow DG 1.5& Tacoma_Fall2 1.0

reserve

C614 2 1 0.1U_0402_16V4Z H_CPUPWRGD_R

R292 2 1 10K_0402_5%

PROC_SELECT#
PH VCPLL and connect to PCH DF_TVS

偵測CPU有無安裝

XBOX 三紅功能

follow Checklist 1.5

+1.05VS_VTT R534 2 1 62_0402_5%

H_PROCHOT# R533 56_0402_5%

UNCOREPWRGOOD:非CORE外的電OK

SM_DRAMPWROK:DRAM power ok

+1.05VS_VTT

CLK_CPU_DPLL# R517 2 1 1K_0402_5%

CLK_CPU_DPLL R516 2 1 1K_0402_5%

Checklist1.5 P.67 Graphis Disable Guide
DIS only SKU eDP disable
DPLL_REF_SSCLK PD 1K_5% to GND
DPLL_REF_SSCLK# PH 1K_5% to +1.05VS_VTT

UCPU1B

MISC THERMAL
CLOCKS
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM

PROC_SELECT#
PROC_DETECT#
CATERR#
PECI
PROCHOT#
THERMTRIP#
PM_SYNC
UNCOREPWRGOOD
SM_DRAMPWROK
RESET#

BCLK
BCLK#
DPLL_REF_CLK
DPLL_REF_CLK#
SM_DRAMRST#
SM_RCOMP[0]
SM_RCOMP[1]
SM_RCOMP[2]
PRDY#
PREQ#
TCK
TMS
TRST#
TDI
TDO
DBR#
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]
BPM#[4]
BPM#[5]
BPM#[6]
BPM#[7]

IVY-BRIDGE_BGA1023

SM_RCOMP0,SM_RCOMP1
W=20mil L=500mil S=13mil

SM_RCOMP2
W=15mil L=500mil S=13mil

DDR3 Compensation Signals

SM_RCOMP0 R272 140_0402_1%
SM_RCOMP1 R273 25.5_0402_1%
SM_RCOMP2 R267 200_0402_1%

@ C82 100P_0402_50V8J

ESD
C Reserve

PU/PD for JTAG signals

XDP_TMS R20 51_0402_5%
XDP_TDI R39 51_0402_5%
XDP_TDO R37 51_0402_5%
XDP_TCK R40 51_0402_5%
XDP_TRST# R28 51_0402_5%

XDP_DBRESET# R312 1K_0402_5%

Tacoma_Fall2 1.0 PH 1K +3VS
Check list 1.5 PH 1K +3VS
Debug port DG1.1-1.3 50~5K ohm

+3VALW
+3VS
+1.5V_CPU_VDDQ
C228 0.1U_0402_16V4Z
R34 10K_0402_5%
R35 @ 10K_0402_5%
U22
74AHC1G09GW_TSSOP5
R238 200_0402_5%
R38 39_0402_5%
Q4 2N7002K_SOT23-3
[15] SYS_PWROK
[15] PM_DRAM_PWRGD
[10] RUN_ON_CPU1.5VS3#

Buffered reset to CPU

+3VS
+1.05VS_VTT
C617 0.1U_0402_16V4Z
R546 75_0402_5%
R544 43_0402_5%
U45
SN74LVC1G07DCKR_SC70-5
C43 0.1U_0402_16V4Z
BUF_CPU_RST#
BUFO_CPU_RST#
PCH_PLTRST#
PCH_PLTRST# [17]

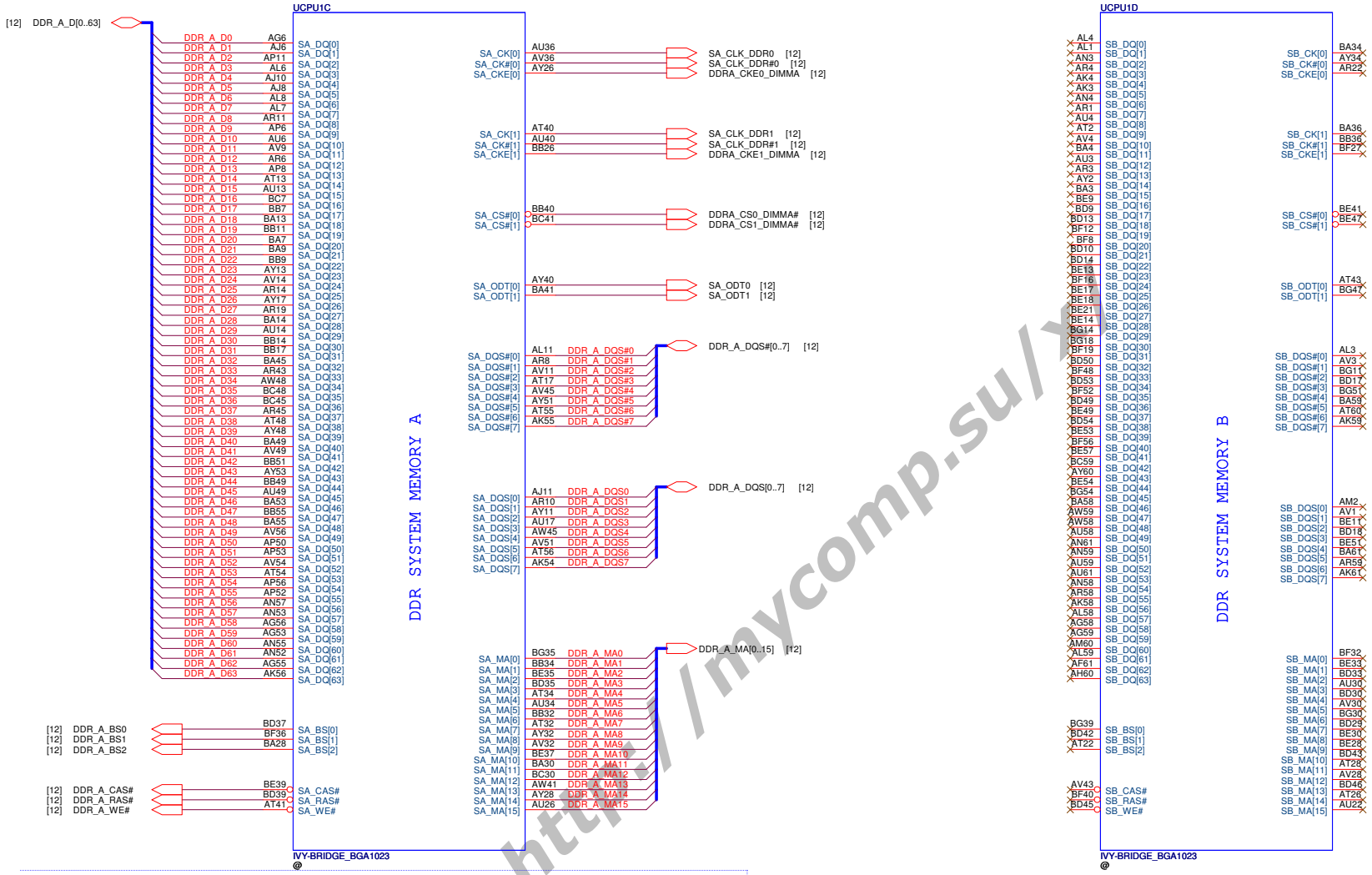
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

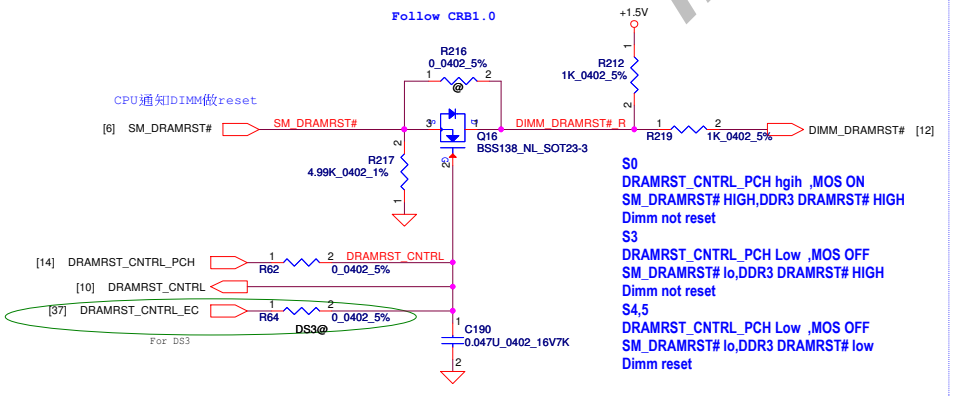
Compal Electronics, Inc.

Title: PROCESSOR(3/7) DDRIII

Size: Custom | Document Number: Sherry and Royal | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 6 of 55





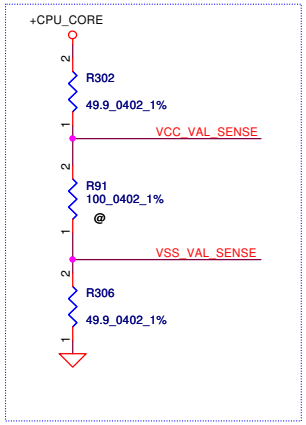
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

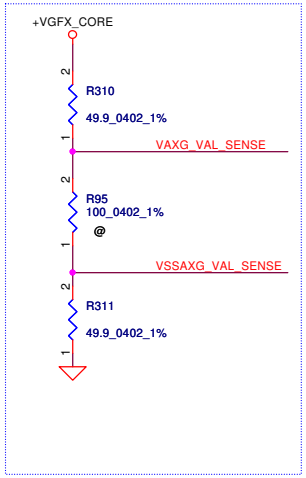
Compal Electronics, Inc.

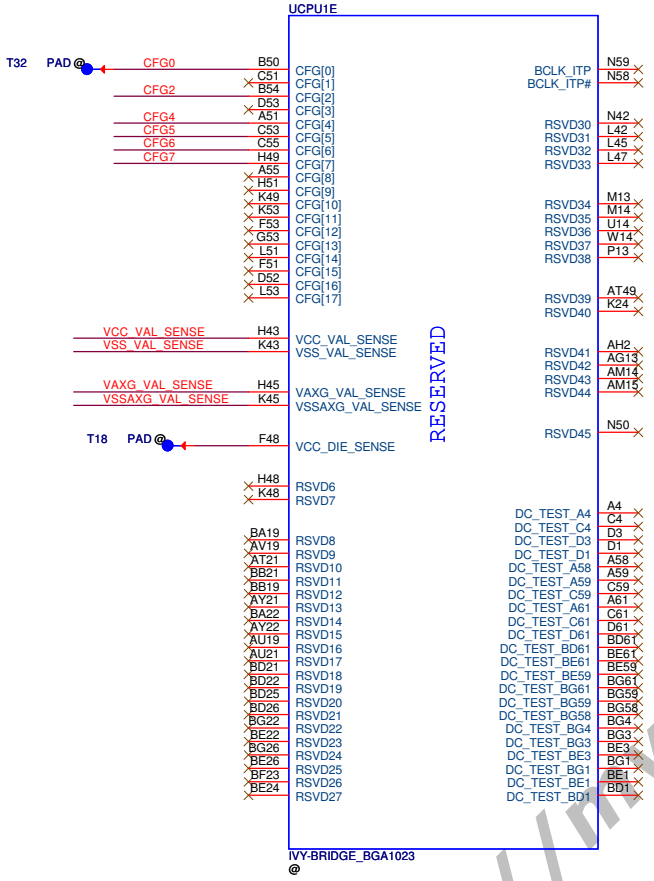
Title: PROCESSOR(3/7) DDRIII

Size: Custom | Document Number: Sherry and Royal | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 7 of 55

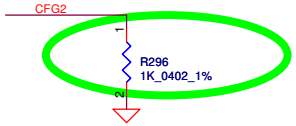






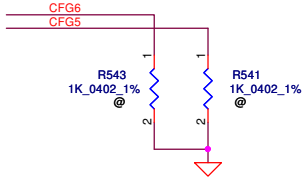
These pins are for solder joint reliability and non-critical to function. For BGA only.

CFG Straps for Processor

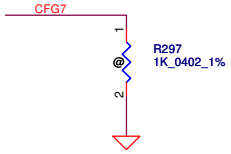


PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

eDP enable	
CFG4	* 1:Disable 0:Enable



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) 1x16 PCI Express 10: 2x8 PCI Express 01: Reserved 00: 1x8,2x4 PCI Express



PEG DEFER TRAINING	Tacoma_Fall2 1.0 P.12
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

Size: Custom | Document Number: Sherry and Royal | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 8 of 55

POWER

UCPU1F

ULV type
DC 33A

8.5A

+CPU_CORE

INTEL Recommend VCC
4*470UF,12*22uF(0805) and 35*2.2uF(0402)
PD0.8
CAP at Power side

CORE SUPPLY

VCC[1] A26, A29, A31, A34, A35, A38, A39, A42, C26, C27, C32, C34, C37, C39, C42, D27, D32, D34, D37, D39, D42, E26, E28, E32, E34, E37, E38, F25, F26, F28, F32, F34, F37, F38, F42, G42, H25, H26, H28, H29, H32, H34, H35, H37, H38, H40, J25, J26, J28, J29, J32, J34, J35, J37, J38, J40, J42, K26, K27, K29, K32, K34, K35, K37, K39, K42, L25, L28, L33, L36, L40, N26, N30, N34, N38
VCC[2] … VCC[76]

PEG IO AND DDR IO

+1.05VS_VTT

For DDR

VCCIO[1] AF46, VCCIO[3] AG48, VCCIO[4] AG50, VCCIO[5] AG51, VCCIO[6] AJ17, VCCIO[7] AJ21, VCCIO[8] AJ25, VCCIO[9] AJ43, VCCIO[10] AJ47, VCCIO[11] AK50, VCCIO[12] AK51, VCCIO[13] AL14, VCCIO[14] AL15, VCCIO[15] AL16, VCCIO[16] AL20, VCCIO[17] AL22, VCCIO[18] AL26, VCCIO[19] AL45, VCCIO[20] AL48, VCCIO[21] AM16, VCCIO[22] AM17, VCCIO[23] AM21, VCCIO[24] AM43, VCCIO[25] AM47, VCCIO[26] AN20, VCCIO[27] AN42, VCCIO[28] AN45, VCCIO[29] AN48

INTEL Recommend VCCIO
2*330UF,10*10uF(0603) and 26*1uF(0402)
PD0.8
CAP at Power side

For PEG

VCCIO[30] AA14, VCCIO[31] AA15, VCCIO[32] AB17, VCCIO[33] AB20, VCCIO[34] AC13, VCCIO[35] AD16, VCCIO[36] AD18, VCCIO[37] AD21, VCCIO[38] AE14, VCCIO[39] AE15, VCCIO[40] AF16, VCCIO[41] AF18, VCCIO[42] AF20, VCCIO[43] AG15, VCCIO[44] AG16, VCCIO[45] AG17, VCCIO[46] AG20, VCCIO[47] AG21, VCCIO[48] AJ14, VCCIO[49] AJ15

+1.05VS_VTT

VCCIO[50] W16, VCCIO[51] W17

+3VS

R521 10K_0402_5%

VCCIO_SEL

R522 10K_0402_5% @

VCCIO_SEL after Ivy bridge ES2 Voltage support		
BC22	*	1/NC : (Default) +1.05VS_VTT 0: +1.0VS_VTT

VCCIO_SEL

BC22 VCCIO_SEL

QUIET RAILS

+1.05VS_VTT

VCCPQE[1] AM25, VCCPQE[2] AN22

C553 1U_0402_6.3V6K

+1.05VS_VTT

R531 130_0402_5%

+1.05VS_VTT

R529 75_0402_5%

Place the PU resistors close to CPU

SVID

VIDALERT# A44 H_CPU_SVIDALRT#
VIDSCLK B43 H_CPU_SVIDCLK
VIDSOUT C44 H_CPU_SVIDDAT

R528 43_0402_1% → VR_SVID_ALRT# [50]
R527 0_0402_5% → VR_SVID_CLK [50]
R530 0_0402_5% → VR_SVID_DAT [50]

Place the PU resistors close to VR

+CPU_CORE

R79 100_0402_1% @

R281 100_0402_1%

SENSE LINES

VCC_SENSE F43 VCCSENSE_R
VSS_SENSE G43 VSSSENSE_R

R282 0_0402_5%
R289 0_0402_5%

VCCSENSE [50]
VSSSENSE [50]

R288 100_0402_1%

R513 10_0402_5% +1.05VS_VTT

VCCIO_SENSE AN16 VCCIO_SENSE
VSS_SENSE_VCCIO AN17 VSSIO_SENSE_L

VCCIO_SENSE [47]
VSSIO_SENSE_L [47]

R512 10_0402_5%

Check list 1.5

Should change to connect form power circuit & layout differential with VCCIO_SENSE.

IVY-BRIDGE_BGA1023

@

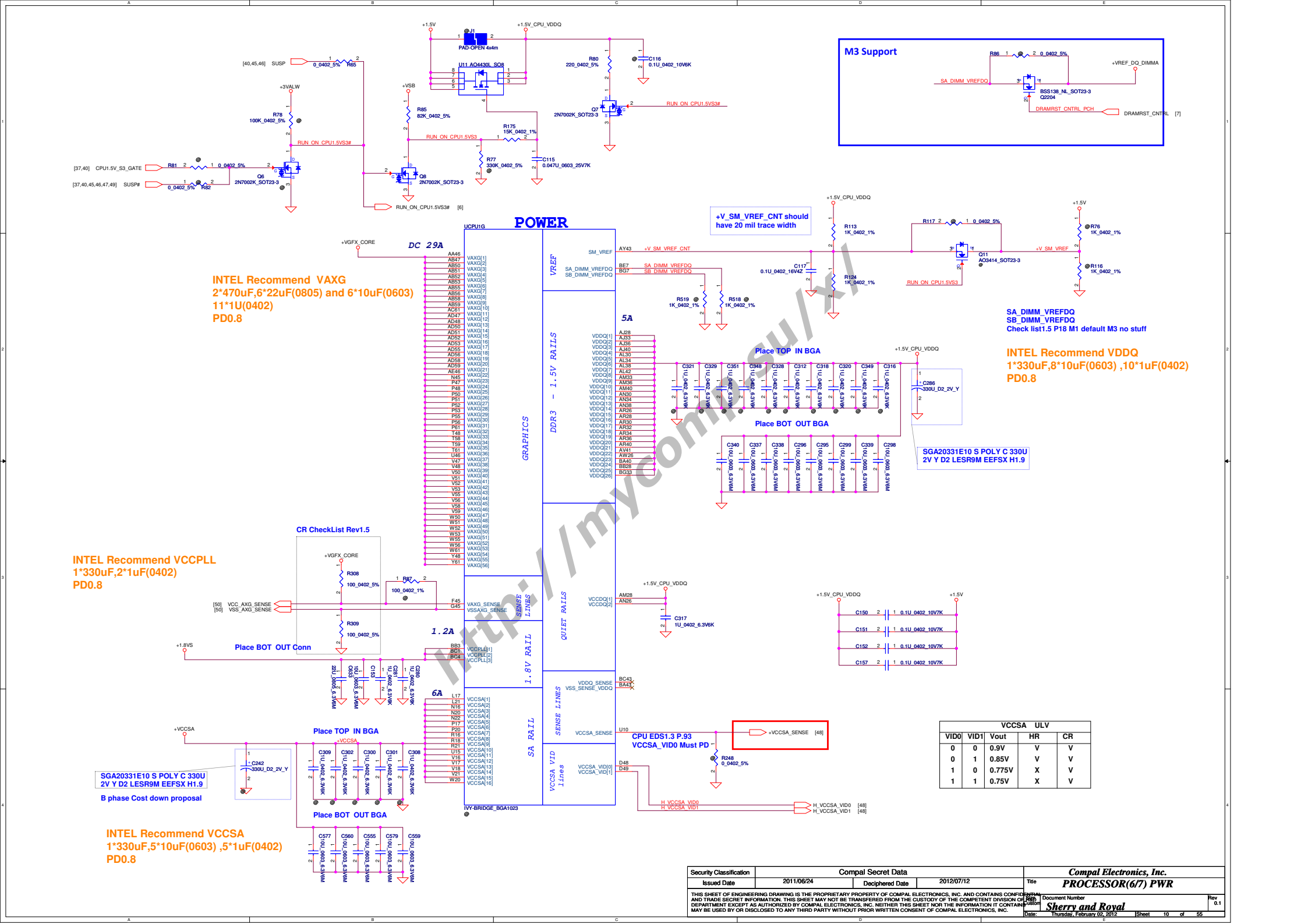
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

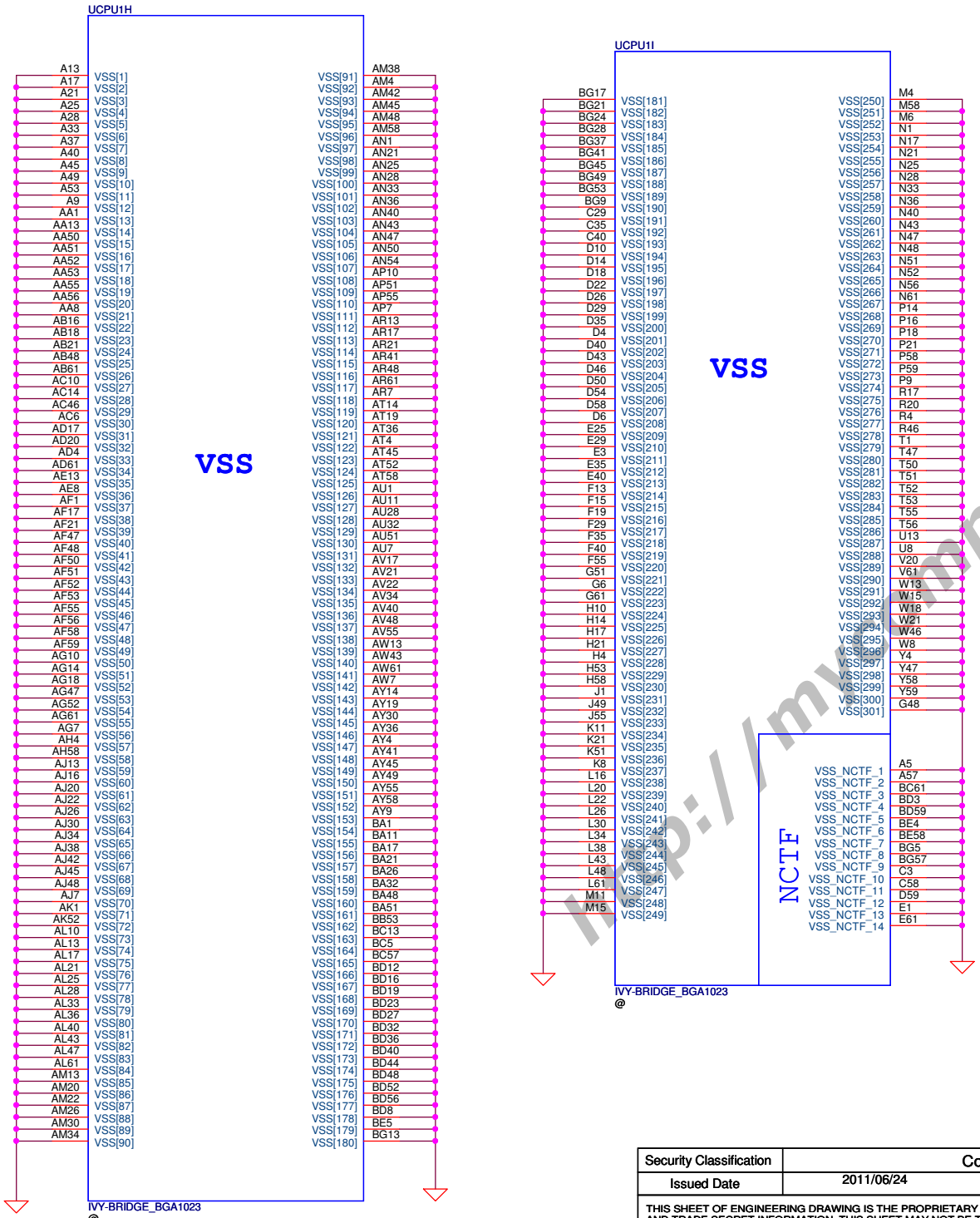
Compal Electronics, Inc.

Title: PROCESSOR(5/7) PWR,BYPASS

Size	Document Number	Rev
Custom	Sherry and Royal	0.1

Date: Thursday, February 02, 2012 Sheet 9 of 55





Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

Size: Custom | Document Number: Sherry and Royal | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 11 of 55

All VREF traces should have 10 mil trace width

DDR_A_DQS#[0..7] [7]
DDR_A_DQS[0..7] [7]
DDR_A_D[0..63] [7]
DDR_A_MA[0..15] [7]

Layout Note:
Place near JDIMM1

Layout Note:
Place near JDIMM1.203,204

DDR_A_DM0
DDR_A_DM1
DDR_A_DM2
DDR_A_DM3
DDR_A_DM4
DDR_A_DM5
DDR_A_DM6
DDR_A_DM7

JDIMM1
TYCO_2-2013022-1
ME@

Channel A

DIMM_1 Standard H:4.0mm

<Address: SA1:SA0=00>

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: DDRIII DIMMB

Size: Custom | Document Number: Sherry and Royal | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 12 of 55

RTCRST close to RAM door

+RTCBATT
C439 1U_0402_6.3V6K
R501 0_0603_5%
R356 20K_0402_5%
R357 20K_0402_5%
PCH_RTCRST#
PCH_SRTCRST#
C440 1U_0402_6.3V6K
R372 0_0603_5%

+RTCBATT
R358 1M_0402_5% SM_INTRUDER#
R355 330K_0402_5% PCH_INTVRMEN

INTVRMEN
★ H : Integrated VRM enable
L : Integrated VRM disable
(INTVRMEN should always be pull high.)

+3VS
R109 1K_0402_5% HDA_SPKR
HIGH= Enable (No Reboot)Disable TCO timer system reboot feature
★ LOW= Disable (Default internal PD)

+3V_PCH
R46 1K_0402_5%
R73 0_0402_5%
[37] ME_FLASH
HDA_SDOUT_PCH

HDA_SDO
ME debug mode,this signal has a weak internal PD
★ Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Overide]

+3V_PCH
R47 1K_0402_5% HDA_SYNC_PCH
This signal has a weak internal pull-down

On Die PLL VR Select is supplied by
★1.5V when sampled high
1.8V when sampled low
Needs to be pulled High for Huron River platfrom

R75 33_0402_5% [36] HDA_BITCLK_AUDIO HDA_BITCLK_PCH
R30 33_0402_5% [36] HDA_SYNC_AUDIO HDA_SYNC_PCH_R
R74 33_0402_5% [36] HDA_RST_AUDIO# HDA_RST_PCH#
R72 33_0402_5% [36] HDA_SDOUT_AUDIO HDA_SDOUT_PCH

+3V_PCH
R134 200_0402_5% PCH_JTAG_TDO
R143 200_0402_5% PCH_JTAG_TMS
R137 200_0402_5% PCH_JTAG_TDI
R141 100_0402_1%
R140 100_0402_1%
R142 100_0402_1%

PCH_RTCX1
R406 10M_0402_5%
PCH_RTCX2
Y2 32.768KHZ_12.5PF_9H032000019
C452 18P_0402_50V8J
C451 18P_0402_50V8J

Prevent back drive issue.
+5VS
Q3 BSS138_NL_SOT23-3
R48 0_0402_5%
R29 1M_0402_5%
HDA_SYNC_PCH_R
[36] HDA_SPKR
[36] HDA_SDIN0

U13A
PCH_RTCX1 A20 RTCX1
PCH_RTCX2 C20 RTCX2
PCH_RTCRST# D20 RTCRST#
PCH_SRTCRST# G22 SRTCRST#
SM_INTRUDER# K22 INTRUDER#
PCH_INTVRMEN C17 INTVRMEN
RTC

HDA_BITCLK_PCH N34 HDA_BCLK
HDA_SYNC_PCH L34 HDA_SYNC
HDA_SPKR T10 SPKR
HDA_RST_PCH# K34 HDA_RST#
HDA_SDIN0 E34 HDA_SDIN0
G34 HDA_SDIN1
C34 HDA_SDIN2
A34 HDA_SDIN3
HDA_SDOUT_PCH A36 HDA_SDO
PCH_GPIO33 C36 HDA_DOCK_EN# / GPIO33
PCH_GPIO13 N32 HDA_DOCK_RST# / GPIO13
IHDA

R162 1K_0402_1%
R341 10K_0402_5%
+3V_PCH
R100 51_0402_5%
PCH_JTAG_TCK J3 JTAG_TCK
PCH_JTAG_TMS H7 JTAG_TMS
PCH_JTAG_TDI K5 JTAG_TDI
PCH_JTAG_TDO H1 JTAG_TDO
JTAG

SPI_CLK_PCH_R T3 SPI_CLK
SPI_SB_CS0# Y14 SPI_CS0#
SPI_SB_CS1# T1 SPI_CS1#
SPI_SI V4 SPI_MOSI
SPI_SO_R U3 SPI_MISO
SPI

PANTHER_FCBGA999
<BOM Structure>

LPC
FWH0 / LAD0 C38 LPC_AD0 — LPC_AD0 [31,37]
FWH1 / LAD1 A38 LPC_AD1 — LPC_AD1 [31,37]
FWH2 / LAD2 B37 LPC_AD2 — LPC_AD2 [31,37]
FWH3 / LAD3 C37 LPC_AD3 — LPC_AD3 [31,37]
FWH4 / LFRAME# D36 LPC_FRAME# — LPC_FRAME# [31,37]
LDRQ0# E36
LDRQ1# / GPIO23 K36
SERIRQ V5 SERIRQ — SERIRQ [37]

+3VS
SERIRQ R118 10K_0402_5%

SATA 6G
SATA0RXN AM3
SATA0RXP AM1
SATA0TXN AP7 SATA_PTX_DRX_C_N0 2 — 1 C1185 0.01U_0402_16V7K SATA_PRX_DTX_C_N0 [31]
SATA0TXP AP5 SATA_PTX_DRX_C_P0 2 — 1 C1208 0.01U_0402_16V7K SATA_PRX_DTX_C_P0 [31]
SATA_PTX_DRX_N0 [31]
SATA_PTX_DRX_P0 [31]
SSD

SATA1RXN AM10 SATA_DTX_C_R_PRX_N1 R148 HDD1@ 2 — 1 0_0402_5%
SATA1RXP AM8 SATA_DTX_C_R_PRX_P1 R149 HDD1@ 2 — 1 0_0402_5%
SATA1TXN AP11 SATA_PTX_DRX_N1 R150 HDD1@ 2 — 1 0_0402_5% SATA_PTX_R_DRX_N1 HDD1@ 2 — 1 C1209 0.01U_0402_16V7K
SATA1TXP AP10 SATA_PTX_DRX_P1 R151 HDD1@ 2 — 1 0_0402_5% SATA_PTX_R_DRX_P1 HDD1@ 2 — 1 C1223 0.01U_0402_16V7K
SATA_DTX_C_PRX_N1 [35]
SATA_DTX_C_PRX_P1 [35]
SATA_PTX_R_DRX_N1 [35]
SATA_PTX_R_DRX_P1 [35]
HDD0 w/ HM77
Disable w/ HM70

SATA2RXN AD7 SATA_DTX_C_R_PRX_N2 R154 HDD2@ 2 — 1 0_0402_5% SATA_DTX_C_PRX_N1
SATA2RXP AD5 SATA_DTX_C_R_PRX_P2 R157 HDD2@ 2 — 1 0_0402_5% SATA_DTX_C_PRX_P1
SATA2TXN AH5 SATA_PTX_DRX_N2 R160 HDD2@ 2 — 1 0_0402_5% SATA_PTX_R_DRX_N1_CO
SATA2TXP AH4 SATA_PTX_DRX_P2 R161 HDD2@ 2 — 1 0_0402_5% SATA_PTX_R_DRX_P1_CO
HDD1 w/ HM70

SATA3RXN AB8
SATA3RXP AB10
SATA3TXN AF3
SATA3TXP AF1
Disable w/ HM70

SATA4RXN Y7
SATA4RXP Y5
SATA4TXN AD3
SATA4TXP AD1

SATA5RXN Y3
SATA5RXP Y1
SATA5TXN AB3
SATA5TXP AB1

SATAICOMPO Y11 — L=500mil S=15mil — +1.05VS_VTT
SATAICOMPI Y10 SATA_COMP — R121 37.4_0402_1%

SATA3RCOMPO AB12 — L=500mil S=15mil — +1.05VS_VTT
SATA3COMPI AB13 SATA3_COMP — R126 49.9_0402_1%

SATA3RBIAS AH1 RBIAS_SATA3 — R440 750_0402_1%

SATALED# P3 PCH_SATALED#
SATA0GP / GPIO21 V14 PCH_GPIO21 — No use PH 10K +3VS
SATA1GP / GPIO19 P1 BBS_BIT0_R

GPIO19 has internal Pull up
GPIO21 Debug Port DG 1.2 PH 4.7K +3VS
+3VS
BBS_BIT0_R R466 10K_0402_5%
PCH_SATALED# R429 10K_0402_5%
PCH_GPIO21 R136 10K_0402_5%

Boot BIOS Strap		
Boot BIOS	GPIO51	GPIO19
LPC	0	0
Reserved	0	1
–	1	0
★ SPI	1	1

8MB SPI ROM FOR ME
& Non-share ROM.

+3VS
R266 2_SPI_WP#1 3.3K_0402_5%
R221 2SPI_HOLD#1 3.3K_0402_5%
R127 2_SPI_WP# 3.3K_0402_5%
R171 2SPI_HOLD# 3.3K_0402_5%

R172 0_0402_5%
SPI_SB_CS1# — CS1#
SPI_SO_R — SPI_SO1
SPI_WP#1
R188 33_0402_5%
U46
CS# VCC
SO HOLD# SPI_HOLD#1
WP# SCLK SPI_CLK1
GND SI SPI_SI1
16M W25Q16BVSSIG SOIC 8P
+3VS
0_0402_5% R199 SPI_CLK_PCH_R
SPI_SI
R196 33_0402_5%

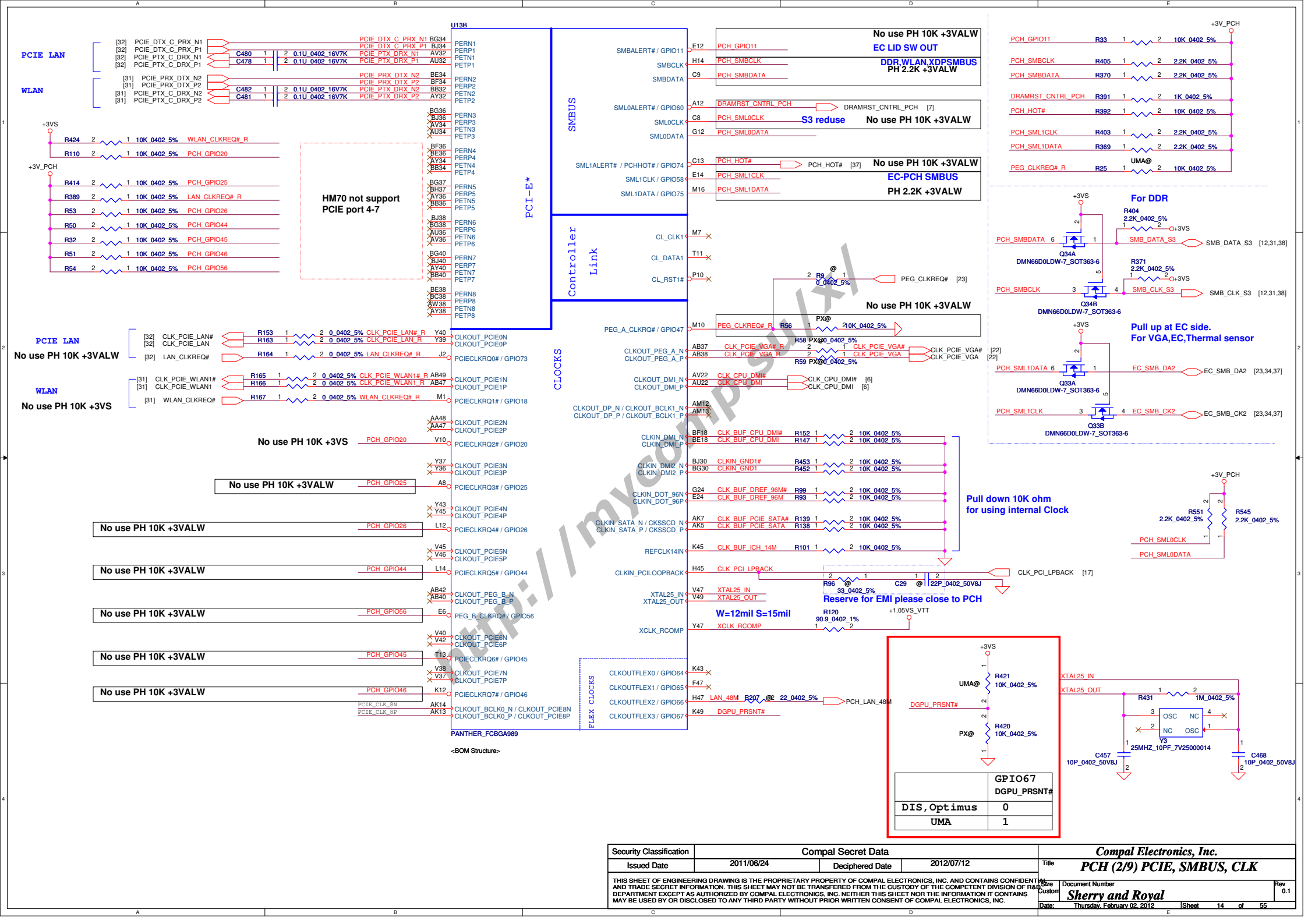
Reserve for EMI
C459 10P_0402_50V8J
R434 SPI_CLK_PCH_R 33_0402_5%

U6 Rersver 4M+2M Solution

+3VS
C191 0.1U_0402_16V4Z
R173 0_0402_5%
SPI_SB_CS0#2 — CS#
SPI_SO_R — SPI_SO_L
SPI_WP#
R169 33_0402_5%
U44
CS# VCC
SO HOLD# SPI_HOLD#
WP# SCLK SPI_CLK_PCH
GND SI SPI_SI_R
32M W25Q32BVSSIG SOIC 8P
0_0402_5% R168 SPI_CLK_PCH_R
SPI_SI
R170 33_0402_5%

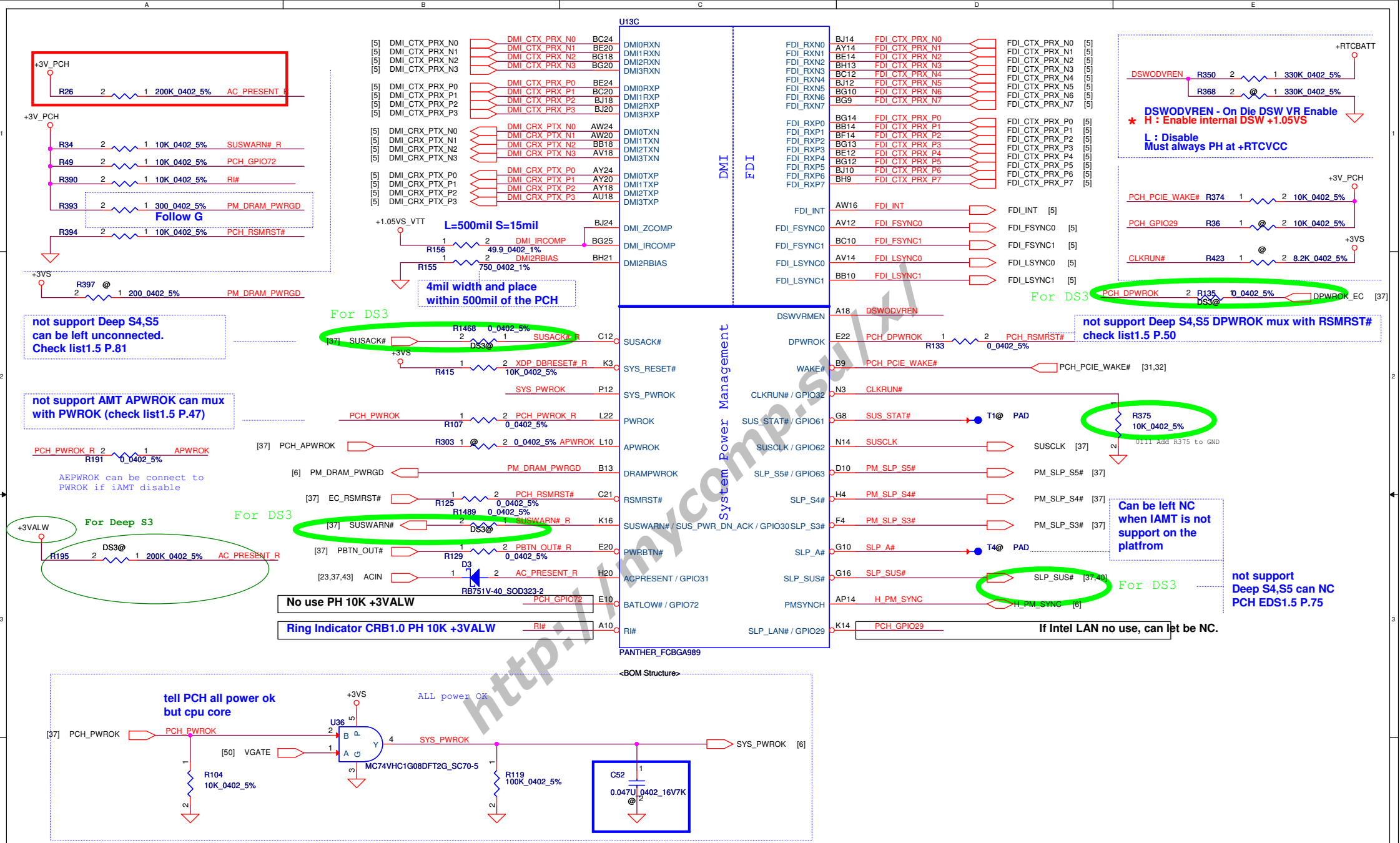
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.
Title: PCH (1/9) SATA,HDA,SPI, LPC, XDP
Size: Custom | Document Number: Sherry and Royal | Rev: 0.1
Date: Thursday, February 02, 2012 | Sheet 13 of 55



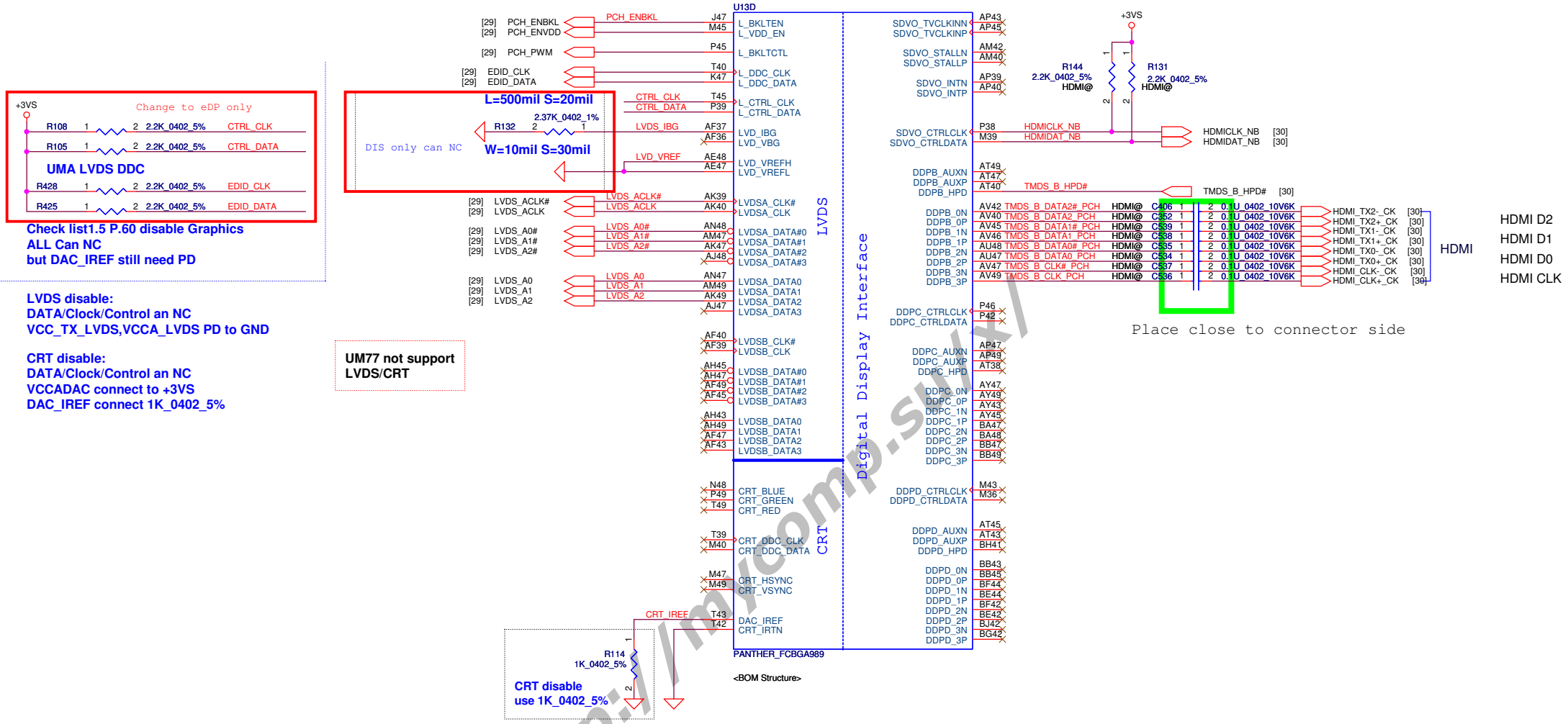
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.	
Title	PCH (2/9) PCIE, SMBUS, CLK
Size: Custom	Document Number: Sherry and Royal
Rev: 0.1	
Date: Thursday, February 02, 2012	Sheet 14 of 55



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.			
Title: PCH (3/9) DMI,FDI,PM			
Size: Custom	Document Number: Sherry and Royal		Rev: 0.1
Date: Thursday, February 02, 2012	Sheet 15 of 55		



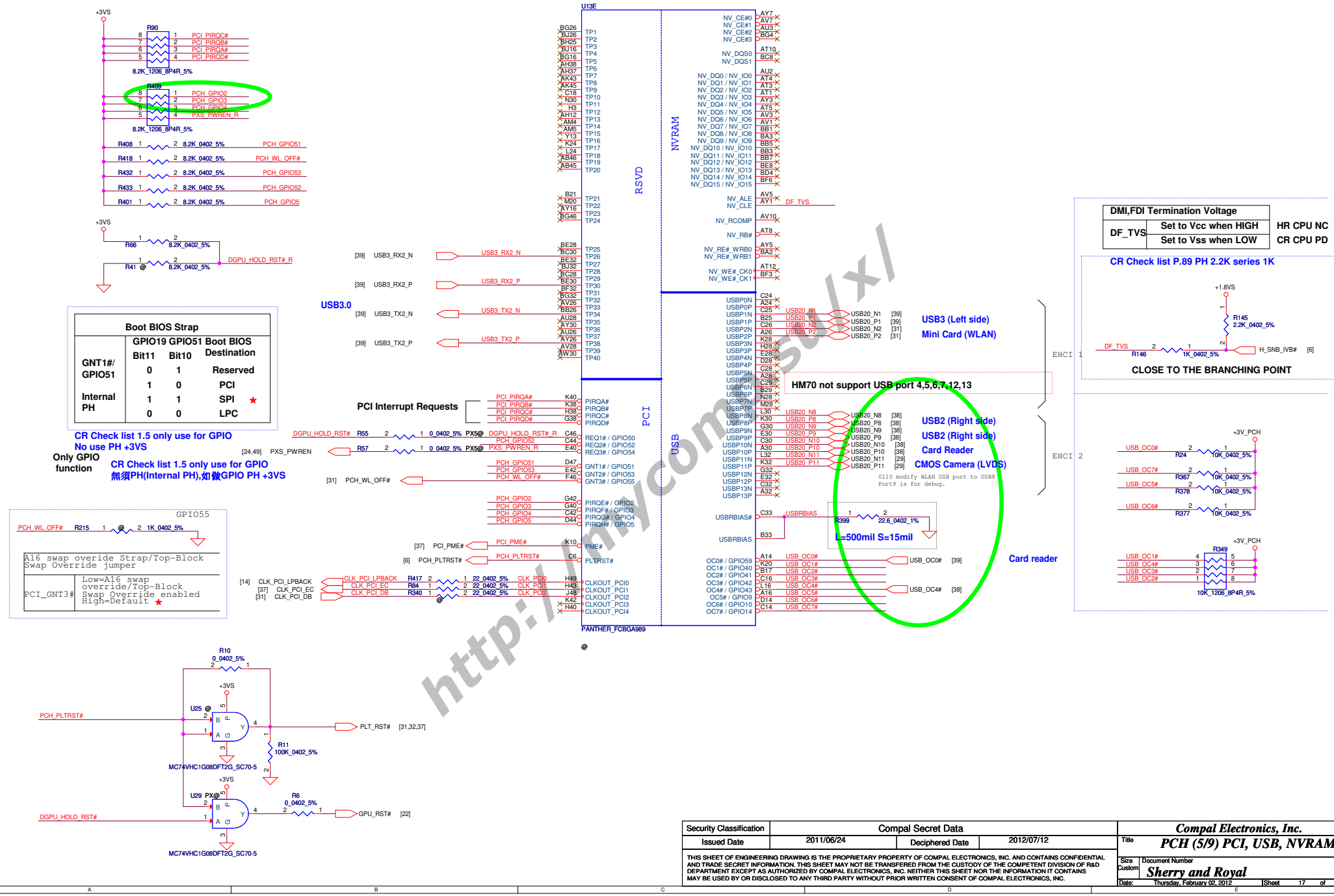
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: PCH (4/9) LVDS,CRT,DP,HDMI

Size: Custom | Document Number: Sherry and Royal | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 16 of 55



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, NVRAM

Size: Custom | Document Number: Sherry and Royal | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 17 of 55

HDA_SYNC PH(PLL =+1.5VS)

GPIO28

On-Die PLL Voltage Regulator

This signal has a weak internal pull up

★ H : On-Die PLL voltage regulator enable
L : On-Die PLL Voltage Regulator disable

+3V_PCH
R411 10K_0402_5%
PCH_GPIO28
R413 1K_0402_5%
Debug Port DG 1.2 PH 4.7K +3VALW_PCH

Deep S4,S5 wake event signal
RTC alarm,Power BTN,GPIO27
PCH_GPIO27 (Have internal Pull-High)
Deep S4,S5 wake event signal

+3VALW
For DS3
R208 DS3@ 10K_0402_5%
R83 @ 10K_0402_5%
PCH_GPIO27

+3V_PCH
R261 @ 1K_0402_5% EC_SMI#

SATA2GP/GPIO36 & SATA3GP/GPIO37
Sampled at Rising edge of PWROK.
Weak internal pull-down.
(weak internal pull-down is disabled
after PLTRST# de-asserts)
NOTE: This signal should NOT be
pulled high when strap is sampled

+3VS
R112 10K_0402_5% PCH_GPIO0
R402 10K_0402_5% PCH_GPIO1
R70 10K_0402_5% PCH_GPIO6
R115 10K_0402_5% MSATA_DET#
R71 10K_0402_5% VGA_PWRGD_R
R419 10K_0402_5% PCH_GPIO39
R97 10K_0402_5% BT_DISABLE
R416 10K_0402_5% PCH_BT_ON#
R128 10K_0402_5% PCH_GPIO48
R111 10K_0402_5% PCH_GPIO49

+3V_PCH
R376 10K_0402_5% PCH_GPIO12
R412 1K_0402_5% PCH_GPIO15
R52 10K_0402_5% PCH_GPIO57
R92 10K_0402_5% PCH_GPIO24
For DDR3L control
[46] DDR3L_EN# R63 @ 0_0402_5% PCH_GPIO24

GPIO24 Unmultiplexed
NOTE: GPIO24 configuration
register bits are not cleared by
CF9h reset event.
CRB1.0 PH10K to +3VALW

Fan Tachometer Inputs
TACH1~7 only on server
can insted to GPIO

No use PH 10K +3VS			PCH_GPIO0	T7
No use PH 10K +3VS			PCH_GPIO1	A42
No use PH 10K +3VS			PCH_GPIO6	H36
No use PH 10K +3VS		[37] EC_SCI#	EC_SCI#	E38
No use PH 10K +3VALW		[37] EC_SMI#	EC_SMI#	C10
No use PH +3VALW			PCH_GPIO12	C4
No use PH +3VALW		[37] EC_LID_OUT#	EC_LID_OUT# @ R60 0_0402_5% PCH_GPIO15	G2
No use PH +3VS		[31] mSATA_DET#	mSATA_DET#	U2
No use PH +3VS		[22,49] VGA_PWRGD	R45 0_0402_5% VGA_PWRGD_R	D40
No use PH 10K +3VS	Blue Booth	[31] BT_DISABLE	BT_DISABLE	T5
No use PH +3VALW	DDR3		PCH_GPIO24	E8
No use PD 10K to GND		EC_LID_OUT#	R61 0_0402_5% PCH_GPIO27	E16
No use PH 10K +3VALW			PCH_GPIO28	P8
No use PH 10K +3VS	BT ON/OFF	[31] PCH_BT_ON#	PCH_BT_ON#	K1
No use can NC		R243 0_0402_5%	PCH_GPIO35	K4
Can't PH			PCH_GPIO36	V8
Can't PH			PCH_GPIO37	M5
No use PH 10K +3VS	Optimus(L)/ non optimus(H)		OPTIMUS_EN#	N2
No use PH 10K +3VS			PCH_GPIO39	M3
No use PH 10K +3VS			PCH_GPIO48	V13
SATA5GP&TEMP_ALERT# CRB PH 10K +3VS			PCH_GPIO49	V3
No use PH +3VALW			PCH_GPIO57	D6

+3VS
R427 UMA@ 10K_0402_5% OPTIMUS_EN#
R426 PX@ 10K_0402_5%

	GPIO38 OPTIMUS_EN#
* Muxless	0
nonMuxless	1

+3VS
R244 10K_0402_5% @ PCH_GPIO37
R881 10K_0402_5%
R245 10K_0402_5% @ PCH_GPIO36
R552 10K_0402_5%

GPIO36/GPIO37 is Strap functionality
that requires internal pull down to be sampled at rising PWROK.
When uses as SATA2GP/SATA3GP for mechanical presence detect
-use a external pull up 150K-200K ohm to Vcc3_3
When used as GP input
-ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA*GP
-use 8.2K-10K pull-down
check list page 47

U13F

GPIO: BMBUSY# / GPIO0, TACH1 / GPIO1, TACH2 / GPIO6, TACH3 / GPIO7, GPIO8, LAN_PHY_PWR_CTRL / GPIO12, GPIO15, SATA4GP / GPIO16, TACH0 / GPIO17, SCLOCK / GPIO22, GPIO24 / MEM_LED, GPIO27, GPIO28, STP_PCI# / GPIO34, GPIO35, SATA2GP / GPIO36, SATA3GP / GPIO37, SLOAD / GPIO38, SDATAOUT0 / GPIO39, SDATAOUT1 / GPIO48, SATA5GP / GPIO49, GPIO57

TACH4 / GPIO68 C40 PCH_GPIO68
TACH5 / GPIO69 B41 PCH_GPIO69
TACH6 / GPIO70 C41 PCH_GPIO70
TACH7 / GPIO71 A40 PCH_GPIO71

CPU/MISC: A20GATE P4 GATEA20 [37]; PECI AU16 PCH_PECI_R 0_0402_5% R158 H_PECI [37,6]; RCIN# P5 EC_KBRST# KBRST# [37]; PROCPWRGD AY11 H_CPUPWRGD [6]; THRMTRIP# AY10 PCH_THRMTRIP#_R R159 390_0402_5% H_THERMTRIP# [6]; INIT3_3V# T14

R106 10K_0402_5%

PECI CPU-EC
CTRL+ALT+DEL
non CPU power ok
130c shut down

INIT3_3V Checklist1.5 P.69
This signal has weak internal
PU, can't pull low,leave NC

NC_1 AH8, NC_2 AK11, NC_3 AH10, NC_4 AK10, NC_5 P37

TS_VSS1~4
PD to GND

EC_KBRST# R103 10K_0402_5%
PCH_GPIO68 R400 10K_0402_5%

NCTF: VSS_NCTF_1 A4, VSS_NCTF_2 A44, VSS_NCTF_3 A45, VSS_NCTF_4 A46, VSS_NCTF_5 A5, VSS_NCTF_6 A6, VSS_NCTF_7 B3, VSS_NCTF_8 B47, VSS_NCTF_9 BD1, VSS_NCTF_10 BD49, VSS_NCTF_11 BE1, VSS_NCTF_12 BE49, VSS_NCTF_13 BF1, VSS_NCTF_14 BF49; VSS_NCTF_15 BG2, VSS_NCTF_16 BG48, VSS_NCTF_17 BH3, VSS_NCTF_18 BH47, VSS_NCTF_19 BJ4, VSS_NCTF_20 BJ44, VSS_NCTF_21 BJ45, VSS_NCTF_22 BJ46, VSS_NCTF_23 BJ5, VSS_NCTF_24 BJ6, VSS_NCTF_25 C2, VSS_NCTF_26 C48, VSS_NCTF_27 D1, VSS_NCTF_28 D49, VSS_NCTF_29 E1, VSS_NCTF_30 E49, VSS_NCTF_31 F1, VSS_NCTF_32 F49

9/15 Layout
request remove
Test point
They will route
by itself

9/15 Layout
request remove
Test point
They will route
by itself

PANTHER_FCBGA989

<BOM Structure>

+3VS
R67 @ 10K_0402_5% PCH_GPIO69
R42 @ 10K_0402_5%
R69 10K_0402_5%@ PCH_GPIO70
R44 200K_0402_5%

PCH_GPIO70	Function
0	13/14"
1	NA
PCH_GPIO71	
0	USB3.0 by PCH
1	USB3.0 by NEC

Need?

+3VS
R68 10K_0402_5% @ PCH_GPIO71
R43 200K_0402_5%

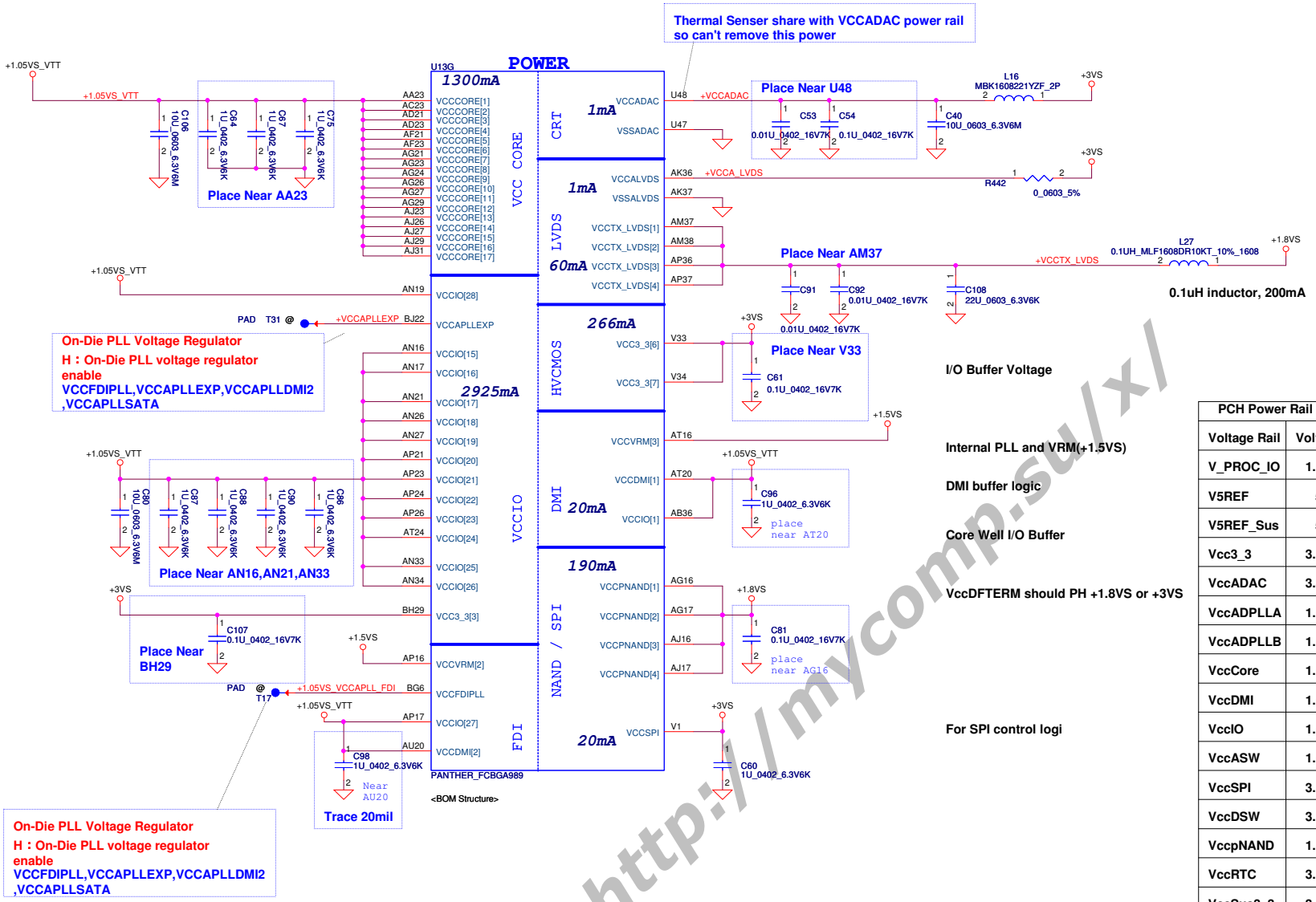
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: Sherry and Royal | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 18 of 55



PCH Power Rail Table			
Voltage Rail	Voltage	S0 Iccmax Current(A)	
V_PROC_IO	1.05	0.001	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltag
Vcc3_3	3.3	0.266	I/O Buffer Voltage
VccADAC	3.3	0.001	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.08	Display PLL A power
VccADPLLB	1.05	0.08	Display PLL B power
VccCore	1.05	1.3	Internal Logic Voltage
VccDMI	1.05	0.042	DMI Buffer Voltage
VccIO	1.05	2.925	Core Well I/O buffers
VccASW	1.05	1.01	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.02	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.19	1.8V power supply for DF_TVS
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.266	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.16	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.02	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.06	Analog power supply for LVDS (Mobile Only)

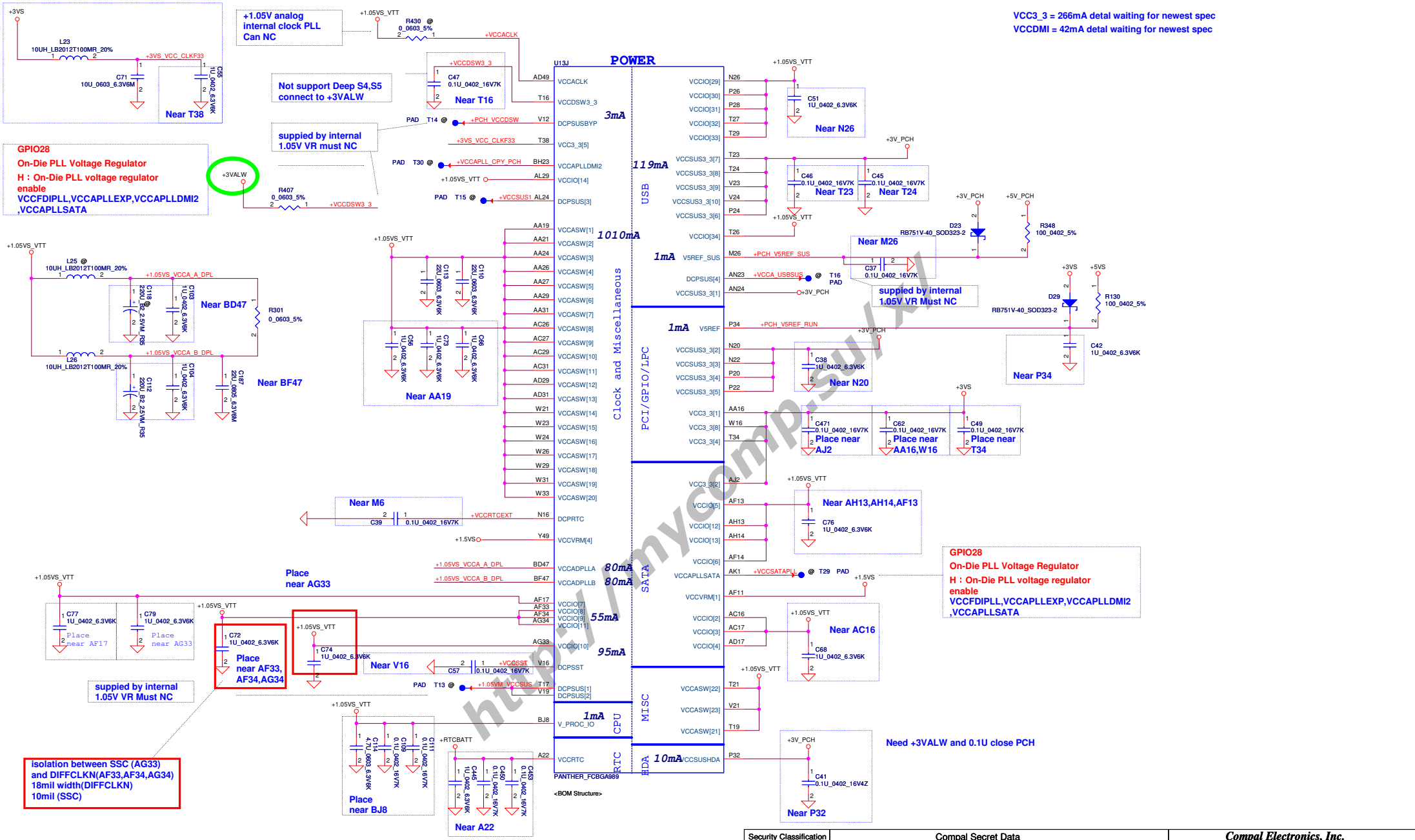
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

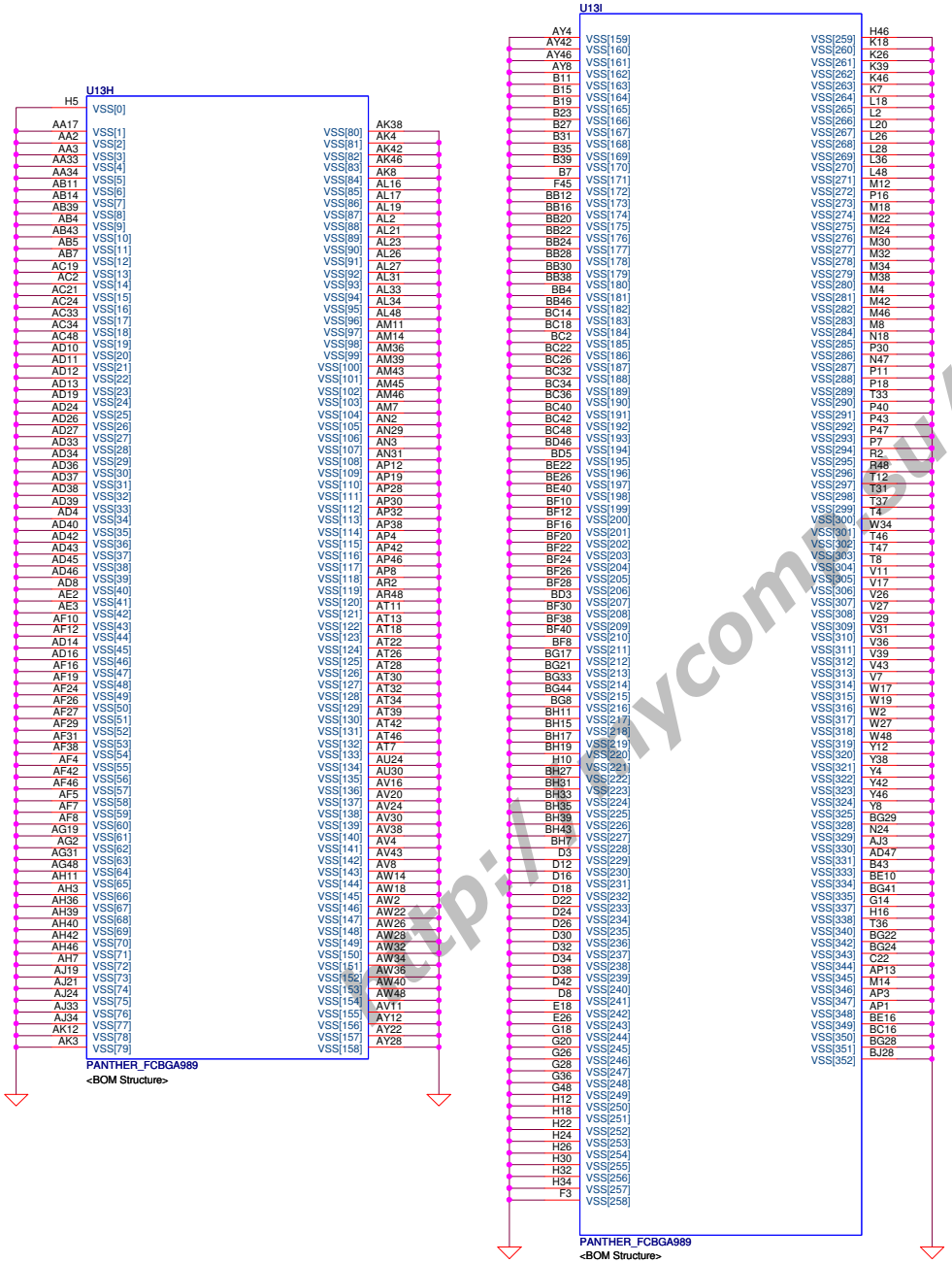
Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: Sherry and Royal | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 19 of 55





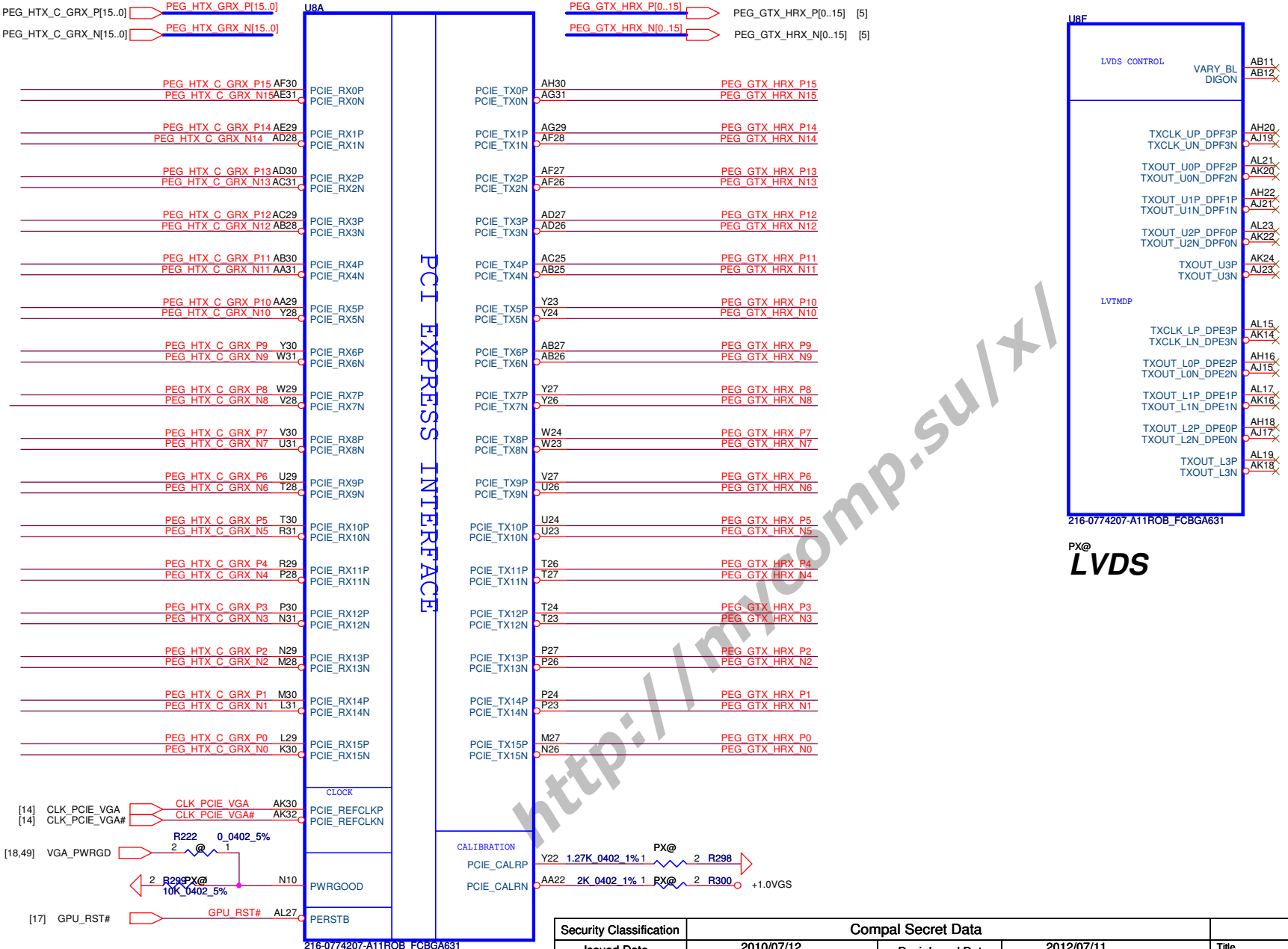
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: PCH (9/9) VSS

Size: Custom | Document Number: Sherry and Royal | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 21 of 55



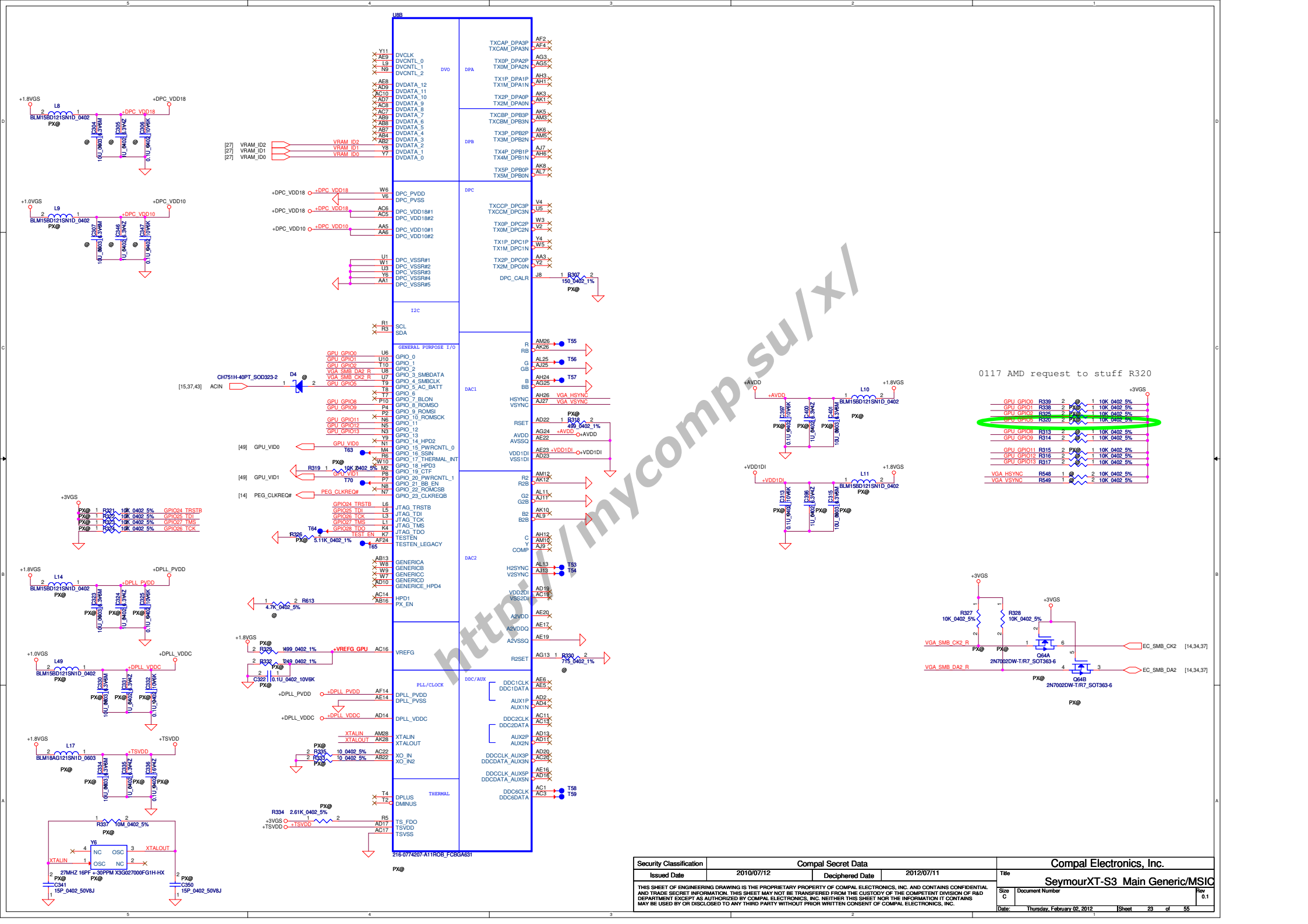
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: SeymourXT-S3 PCIE/LVDS

Size	Document Number	Rev
B		0.1

Date: Thursday, February 02, 2012 Sheet 22 of 55



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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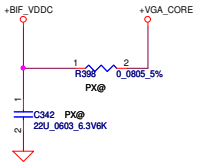
Compal Electronics, Inc.

Title: SeymourXT-S3 Main Generic/MSIC

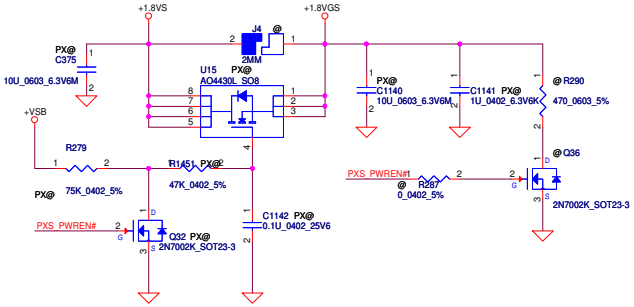
Size	Document Number	Rev
C		0.1

Date: Thursday, February 02, 2012 | Sheet 23 of 55

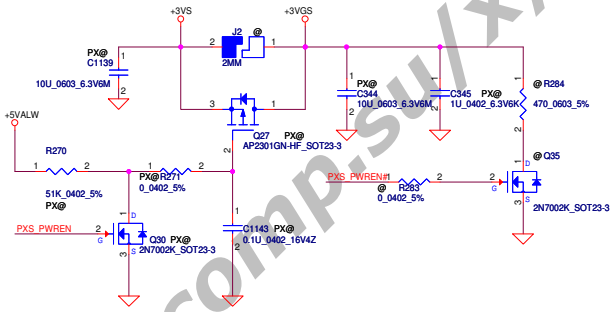
55mA@1.0V, in BACO mode

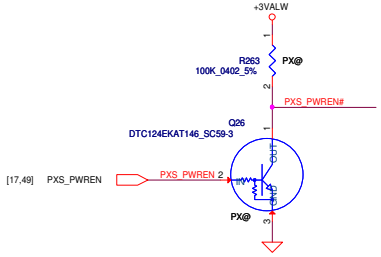


+1.8VS TO +1.8VGS

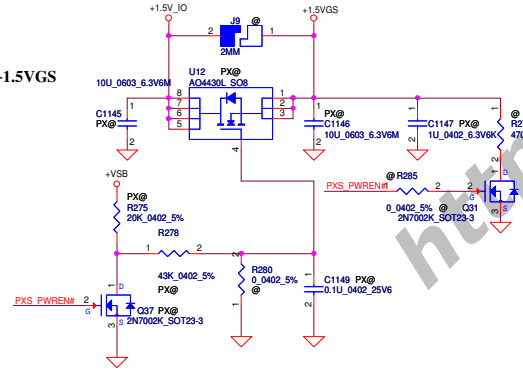


+3.3VS TO +3.3VGS





+1.5V TO +1.5VGS



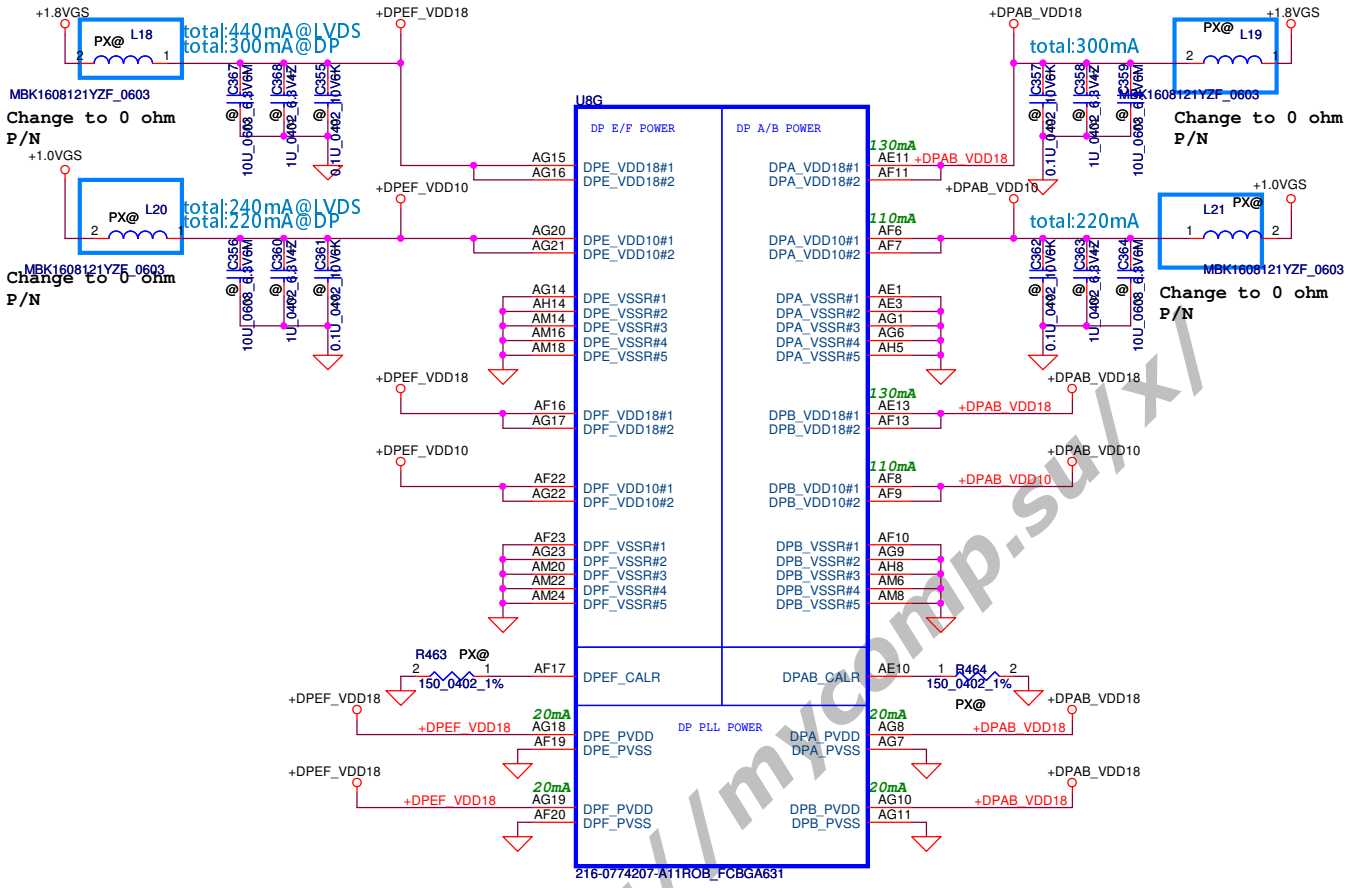
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: SeymourXT_S3_BACO POWER

Size	Document Number	Rev
C	Sherry and Royal	0.1

Date: Thursday, February 02, 2012 Sheet 24 of 55



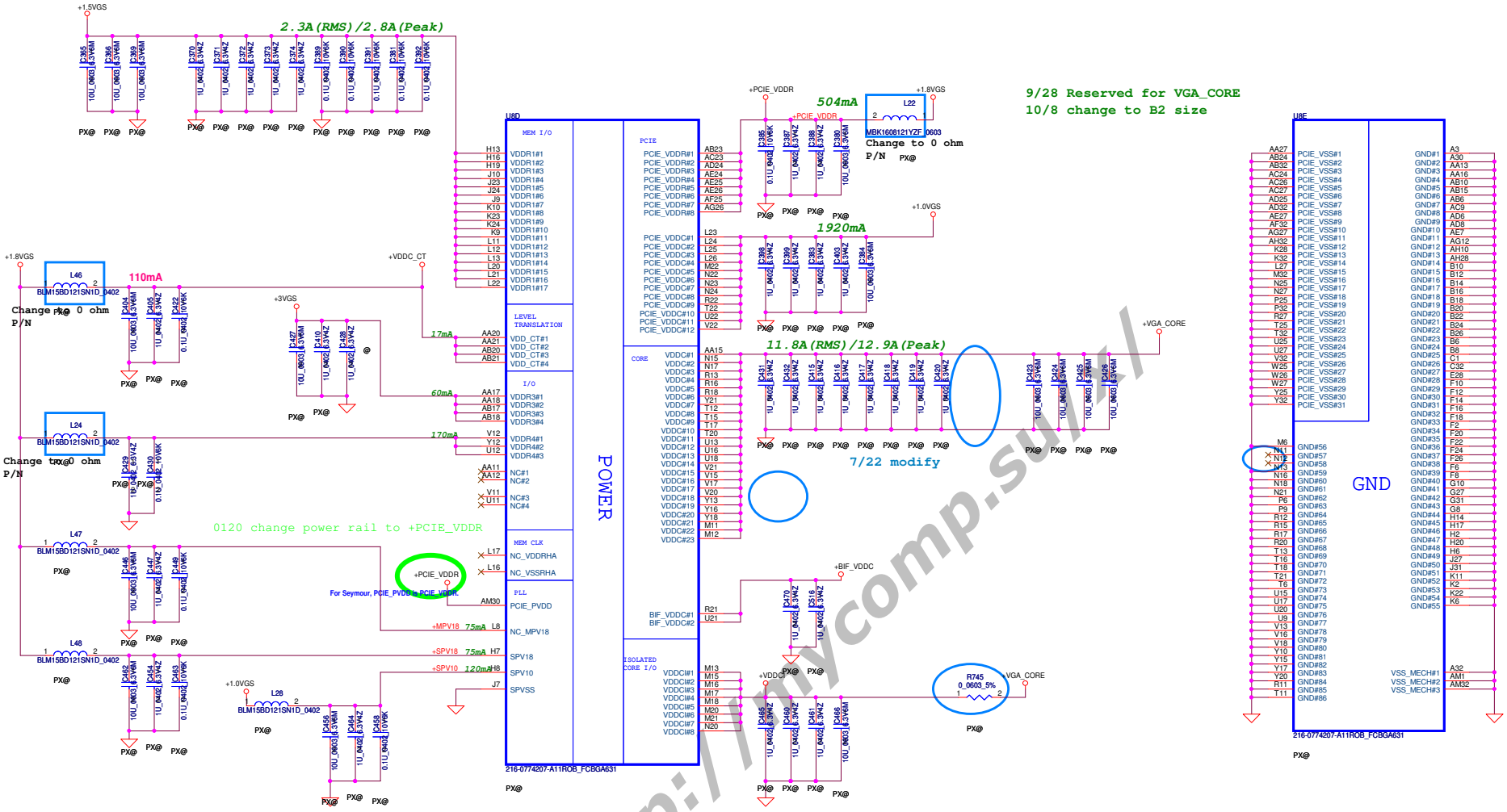
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: SeymourXT-S3 DP PWR

Size	Document Number	Rev
B		0.1

Date: Thursday, February 02, 2012 Sheet 25 of 55



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/07/12	Deciphered Date	2012/07/11
Title	SeymourXT-S3 PWR/GND		
Size C	Document Number		Rev 0.1
Date: Thursday, February 02, 2012	Sheet 26 of 55		

[28] M_DA[63..0] — M_DA[63..0]
[28] M_MA[13..0] — M_MA[13..0]
[28] M_DQM[7..0] — M_DQM[7..0]
[28] M_DQS[7..0] — M_DQS[7..0]
[28] M_DQS#[7..0] — M_DQS#[7..0]

PARK SCL has different recommand

9/28 change P/N to SD034100A80

[28] DRAM_RST# — R366 51.1_0402_1% PX@ — R455 10_0402_1% — DRAM_RST
C469 120P_0402_50V8J — PX@ — R456 4.99K_0402_1% — PX@ — PX@

+1.5VGS — R363 40.2_0402_1% — +MVREFDA — R364 100_0402_1% PX@ — C467 0.1U_0402_16V4Z PX@ — PX@

+1.5VGS — R365 40.2_0402_1% — +MVREFSA — R457 100_0402_1% PX@ — C514 0.1U_0402_16V4Z PX@ — PX@

U8C

MEMORY INTERFACE

	GDDR5/DDR3		GDDR5/DDR3		
M_DA0	DQA0_0/DQA_0	K27	MAA0_0/MAA_0	K17	M_MA0
M_DA1	DQA0_1/DQA_1	J29	MAA0_1/MAA_1	J20	M_MA1
M_DA2	DQA0_2/DQA_2	H30	MAA0_2/MAA_2	H23	M_MA2
M_DA3	DQA0_3/DQA_3	H32	MAA0_3/MAA_3	G23	M_MA3
M_DA4	DQA0_4/DQA_4	G29	MAA0_4/MAA_4	G24	M_MA4
M_DA5	DQA0_5/DQA_5	F28	MAA0_5/MAA_5	H24	M_MA5
M_DA6	DQA0_6/DQA_6	F32	MAA0_6/MAA0_6	J19	M_MA6
M_DA7	DQA0_7/DQA_7	F30	MAA0_7/MAA0_7	K19	M_MA7
M_DA8	DQA0_8/DQA_8	C30	MAA1_0/MAA_8	J14	M_MA8
M_DA9	DQA0_9/DQA_9	F27	MAA1_1/MAA_9	K14	M_MA9
M_DA10	DQA0_10/DQA_10	A28	MAA1_2/MAA_10	J11	M_MA10
M_DA11	DQA0_11/DQA_11	C28	MAA1_3/MAA_11	J13	M_MA11
M_DA12	DQA0_12/DQA_12	E27	MAA1_4/MAA_12	H11	M_MA12
M_DA13	DQA0_13/DQA_13	G26	MAA1_5/MAA_13/BA2	G11	M_BA2 → M_BA2 [28]
M_DA14	DQA0_14/DQA_14	D26	MAA1_6/MAA_14/BA0	J16	M_BA0 → M_BA0 [28]
M_DA15	DQA0_15/DQA_15	F25	MAA1_7/MAA_15/BA1	L15	M_BA1 → M_BA1 [28]
M_DA16	DQA0_16/DQA_16	A25			
M_DA17	DQA0_17/DQA_17	C25	WCKA0_0/DQMA_0	E32	M_DQM0
M_DA18	DQA0_18/DQA_18	E25	WCKA0B_0/DQMA_1	E30	M_DQM1
M_DA19	DQA0_19/DQA_19	D24	WCKA0_1/DQMA_2	A21	M_DQM2
M_DA20	DQA0_20/DQA_20	E23	WCKA0B_1/DQMA_3	C21	M_DQM3
M_DA21	DQA0_21/DQA_21	F23	WCKA1_0/DQMA_4	E13	M_DQM4
M_DA22	DQA0_22/DQA_22	D22	WCKA1B_0/DQMA_5	D12	M_DQM5
M_DA23	DQA0_23/DQA_23	F21	WCKA1_1/DQMA_6	E3	M_DQM6
M_DA24	DQA0_24/DQA_24	E21	WCKA1B_1/DQMA_7	F4	M_DQM7
M_DA25	DQA0_25/DQA_25	D20			
M_DA26	DQA0_26/DQA_26	F19	EDCA0_0/RDQSA_0	H28	M_DQS0
M_DA27	DQA0_27/DQA_27	A19	EDCA0_1/RDQSA_1	C27	M_DQS1
M_DA28	DQA0_28/DQA_28	D18	EDCA0_2/RDQSA_2	A23	M_DQS2
M_DA29	DQA0_29/DQA_29	F17	EDCA0_3/RDQSA_3	E19	M_DQS3
M_DA30	DQA0_30/DQA_30	A17	EDCA1_0/RDQSA_4	E15	M_DQS4
M_DA31	DQA0_31/DQA_31	C17	EDCA1_1/RDQSA_5	D10	M_DQS5
M_DA32	DQA1_0/DQA_32	E17	EDCA1_2/RDQSA_6	D6	M_DQS6
M_DA33	DQA1_1/DQA_33	D16	EDCA1_3/RDQSA_7	G5	M_DQS7
M_DA34	DQA1_2/DQA_34	F15			
M_DA35	DQA1_3/DQA_35	A15	DDBIA0_0/WDQSA_0	H27	M_DQS#0
M_DA36	DQA1_4/DQA_36	D14	DDBIA0_1/WDQSA_1	A27	M_DQS#1
M_DA37	DQA1_5/DQA_37	F13	DDBIA0_2/WDQSA_2	C23	M_DQS#2
M_DA38	DQA1_6/DQA_38	A13	DDBIA0_3/WDQSA_3	C19	M_DQS#3
M_DA39	DQA1_7/DQA_39	C13	DDBIA1_0/WDQSA_4	C15	M_DQS#4
M_DA40	DQA1_8/DQA_40	E11	DDBIA1_1/WDQSA_5	E9	M_DQS#5
M_DA41	DQA1_9/DQA_41	A11	DDBIA1_2/WDQSA_6	C5	M_DQS#6
M_DA42	DQA1_10/DQA_42	C11	DDBIA1_3/WDQSA_7	H4	M_DQS#7
M_DA43	DQA1_11/DQA_43	F11			
M_DA44	DQA1_12/DQA_44	A9	ADBIA0/ODTA0	L18	VRAM_ODT0 → VRAM_ODT0 [28]
M_DA45	DQA1_13/DQA_45	C9	ADBIA1/ODTA1	K16	VRAM_ODT1 → VRAM_ODT1 [28]
M_DA46	DQA1_14/DQA_46	F9			
M_DA47	DQA1_15/DQA_47	D8	CLKA0	H26	M_CLK0 → M_CLK0 [28]
M_DA48	DQA1_16/DQA_48	E7	CLKA0B	H25	M_CLK#0 → M_CLK#0 [28]
M_DA49	DQA1_17/DQA_49	A7			
M_DA50	DQA1_18/DQA_50	C7	CLKA1	G9	M_CLK1 → M_CLK1 [28]
M_DA51	DQA1_19/DQA_51	F7	CLKA1B	H9	M_CLK#1 → M_CLK#1 [28]
M_DA52	DQA1_20/DQA_52	A5			
M_DA53	DQA1_21/DQA_53	E5	RASA0B	G22	M_RAS#0 → M_RAS#0 [28]
M_DA54	DQA1_22/DQA_54	C3	RASA1B	G17	M_RAS#1 → M_RAS#1 [28]
M_DA55	DQA1_23/DQA_55	E1			
M_DA56	DQA1_24/DQA_56	G7	CASA0B	G19	M_CAS#0 → M_CAS#0 [28]
M_DA57	DQA1_25/DQA_57	G6	CASA1B	G16	M_CAS#1 → M_CAS#1 [28]
M_DA58	DQA1_26/DQA_58	G1			
M_DA59	DQA1_27/DQA_59	G3	CSA0B_0	H22	M_CS#0 → M_CS#0 [28]
M_DA60	DQA1_28/DQA_60	J6	CSA0B_1	J22	
M_DA61	DQA1_29/DQA_61	J1			
M_DA62	DQA1_30/DQA_62	J3	CSA1B_0	G13	M_CS#1 → M_CS#1 [28]
M_DA63	DQA1_31/DQA_63	J5	CSA1B_1	K13	
+MVREFDA	MVREFDA	K26	CKEA0	K20	M_CKE0 → M_CKE0 [28]
+MVREFSA	MVREFSA	J26	CKEA1	J17	M_CKE1 → M_CKE1 [28]
	MEM_CALRN0	K25	WEA0B	G25	M_WE#0 → M_WE#0 [28]
	MEM_CALRP0	K24	WEA1B	H10	M_WE#1 → M_WE#1 [28]
			GDDR5 MAA1_8 / MAA0_8	G14 / G20	M_MA13
DRAM_RST	DRAM_RST	L10			
	CLKTESTA	K8			
	CLKTESTB	L7			

64MX16 (512MB)
64MX16 (512MB)
128M16 (1GB)
128M16 (1GB)

216-0774207-A11ROB_FCBGA631

+1.5VGS — +MVREFDA — R458 1 PX@ 2 240_0402_1% — MEM_CALRN0
+MVREFSA — R459 1 PX@ 2 240_0402_1% — MEM_CALRP0

R460@51.1_0402_1% — C515@0.1U_0402_16V4Z
R373@51.1_0402_1% — C517@0.1U_0402_16V4Z

Route 50ohms single-ended/100ohm diff and keep short

debug only, for clock observation,if not need, DNI.

+1.8VGS

R461 1	X76@ 2	10K_0402_5%	VRAM_ID0	VRAM_ID0 [23]
R462 1	X76@ 2	10K_0402_5%		
R359 1	X76@ 2	10K_0402_5%	VRAM_ID1	VRAM_ID1 [23]
R360 1	X76@ 2	10K_0402_5%		
R361 1	X76@ 2	10K_0402_5%	VRAM_ID2	VRAM_ID2 [23]
R362 1	X76@ 2	10K_0402_5%		

Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
K4W1G1646G-BC11 Samsung 128MB PN:SA00004GS00	R461 1	R360 0	R362 0
H5TQ1G63DFR-11C Hynix 128MB PN:SA000041S20	R462 0	R359 1	R362 0
K4W2G1646C-HC11 Samsung 256MB PN:SA000047O00	R461 1	R360 0	R361 1
H5TQ2G63BFR-11C/H5TQ2G63DFR-11C Hynix 256MB PN:SA00003YO10/ SA00003YOA0	R462 0	R359 1	R361 1

ZZZ
Hynix H1G@ X7639238L02

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

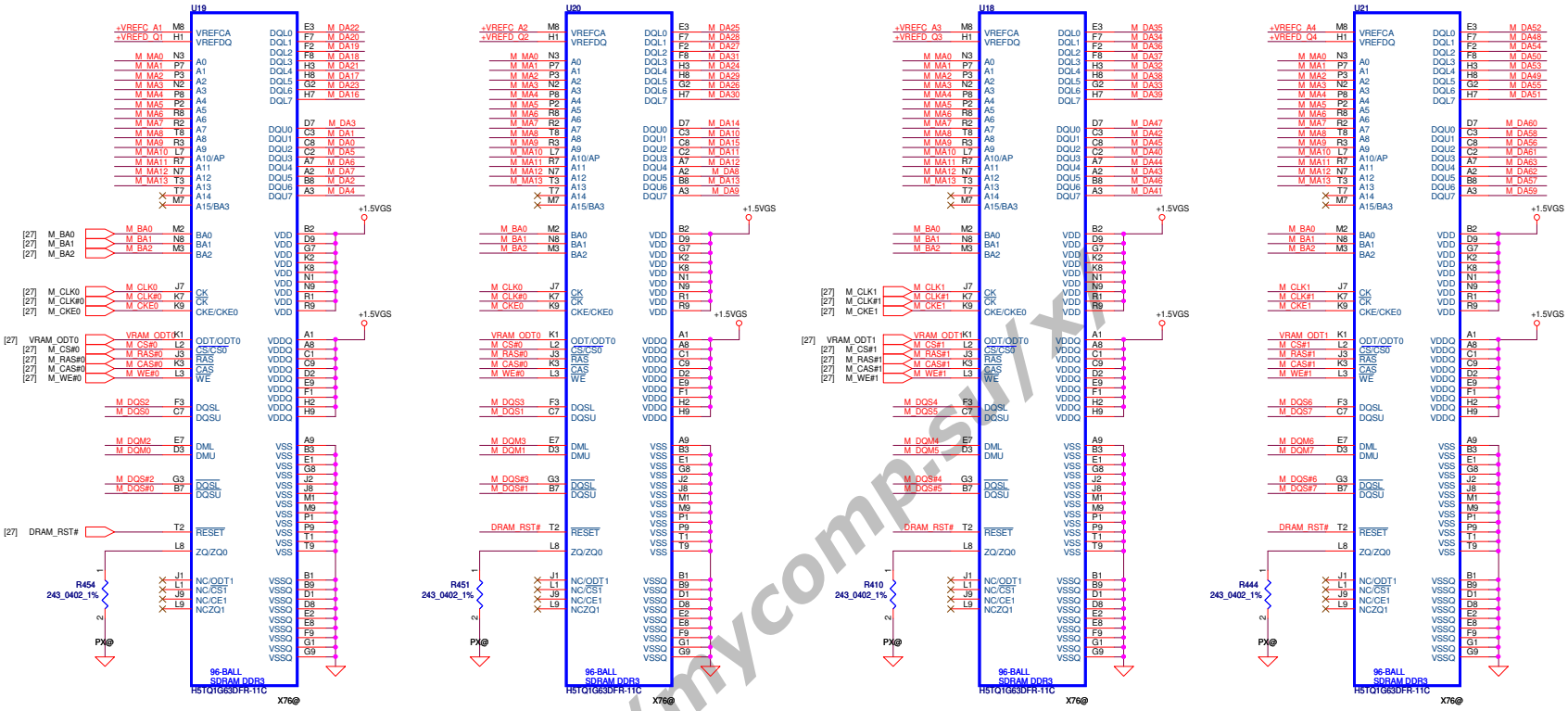
Compal Electronics, Inc.

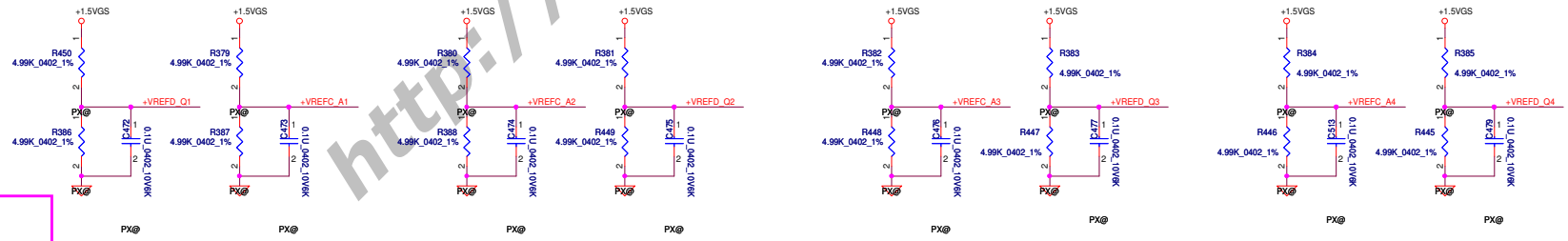
Title: SeymourXT-S3 MEM Interface

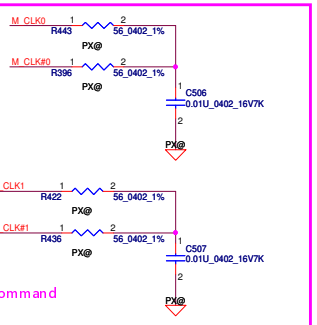
Size: B | Document Number | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 27 of 55

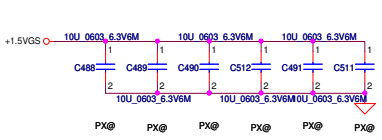
[27] M_DA[63..0] — M_DA[63..0]
[27] M_MA[13..0] — M_MA[13..0]
[27] M_DQM[7..0] — M_DQM[7..0]
[27] M_DQS[7..0] — M_DQS[7..0]
[27] M_DQS#[7..0] — M_DQS#[7..0]

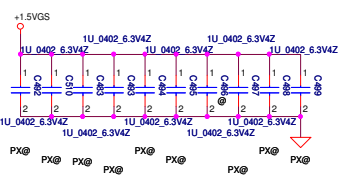


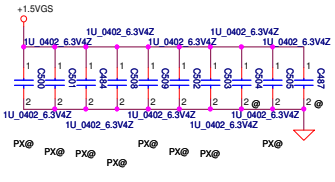




ref 139-02 recommand
add off page
Park SCL recommand pu 60.4 ohm to +1.5VGS
0619 update





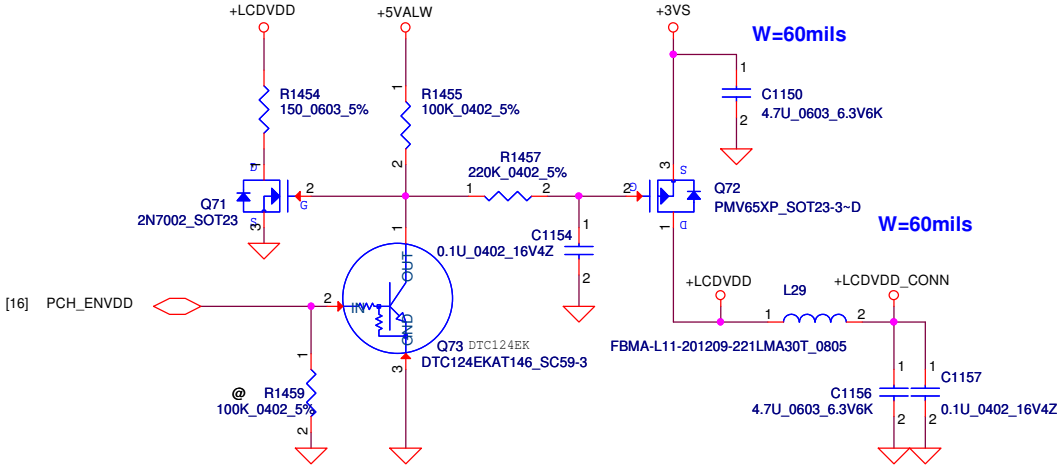


VRAM P/N :
Hynix : SA000041S10 (S IC D3 64MX16 H5TQ1G63BFR-11C FBGA C38!)
Samsung : SA000041T10 (S IC D3 64MX16 K4W1G1646E-HC11 FBGA C38!)
update VRAM PN 0619 update

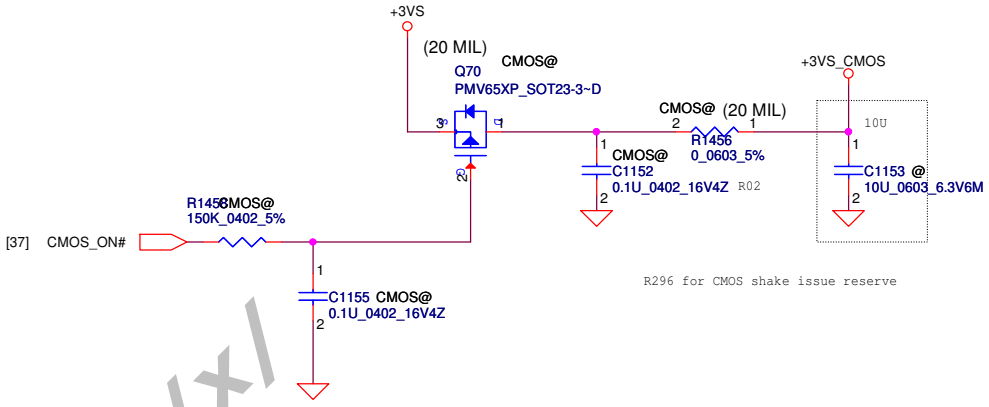
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.
Title: SeymourXT-S3 VRAM
Size: C | Document Number | Rev: 0.1
Date: Thursday, February 02, 2012 | Sheet 28 of 55

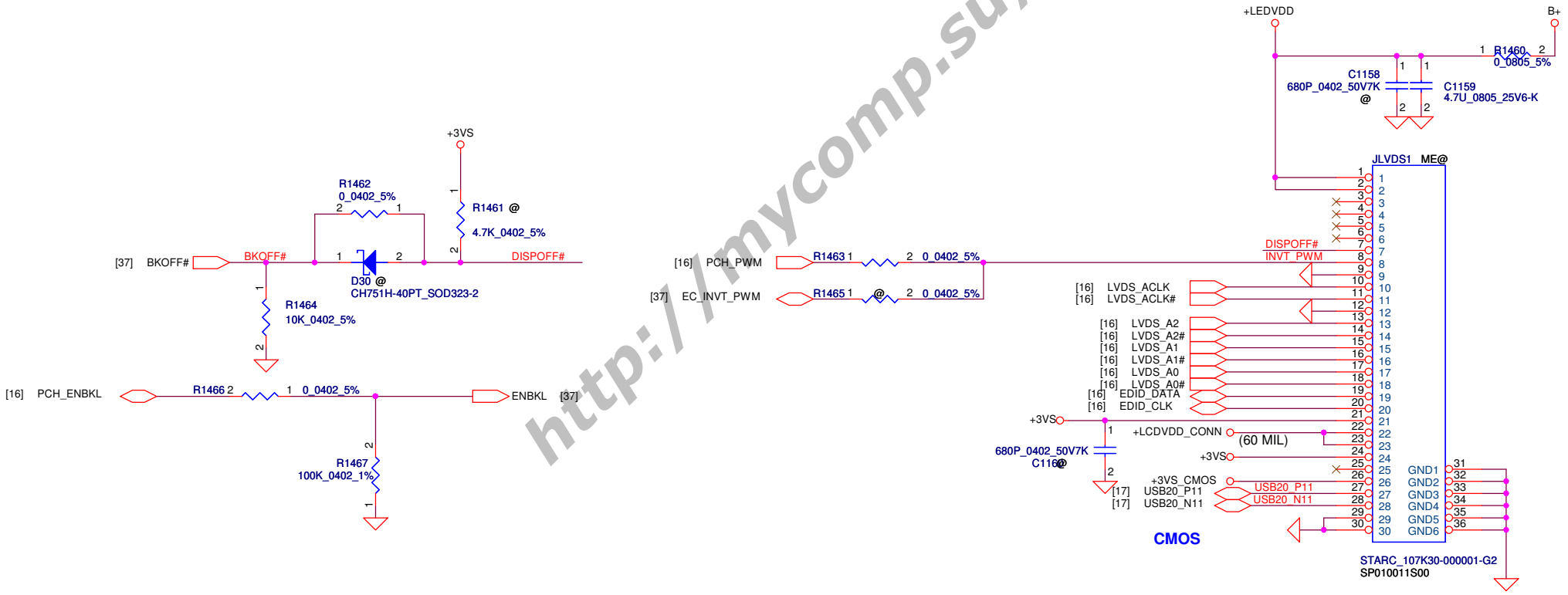
LCD POWER CIRCUIT



CMOS Camera



VGA LCD/PANEL BD. Conn.



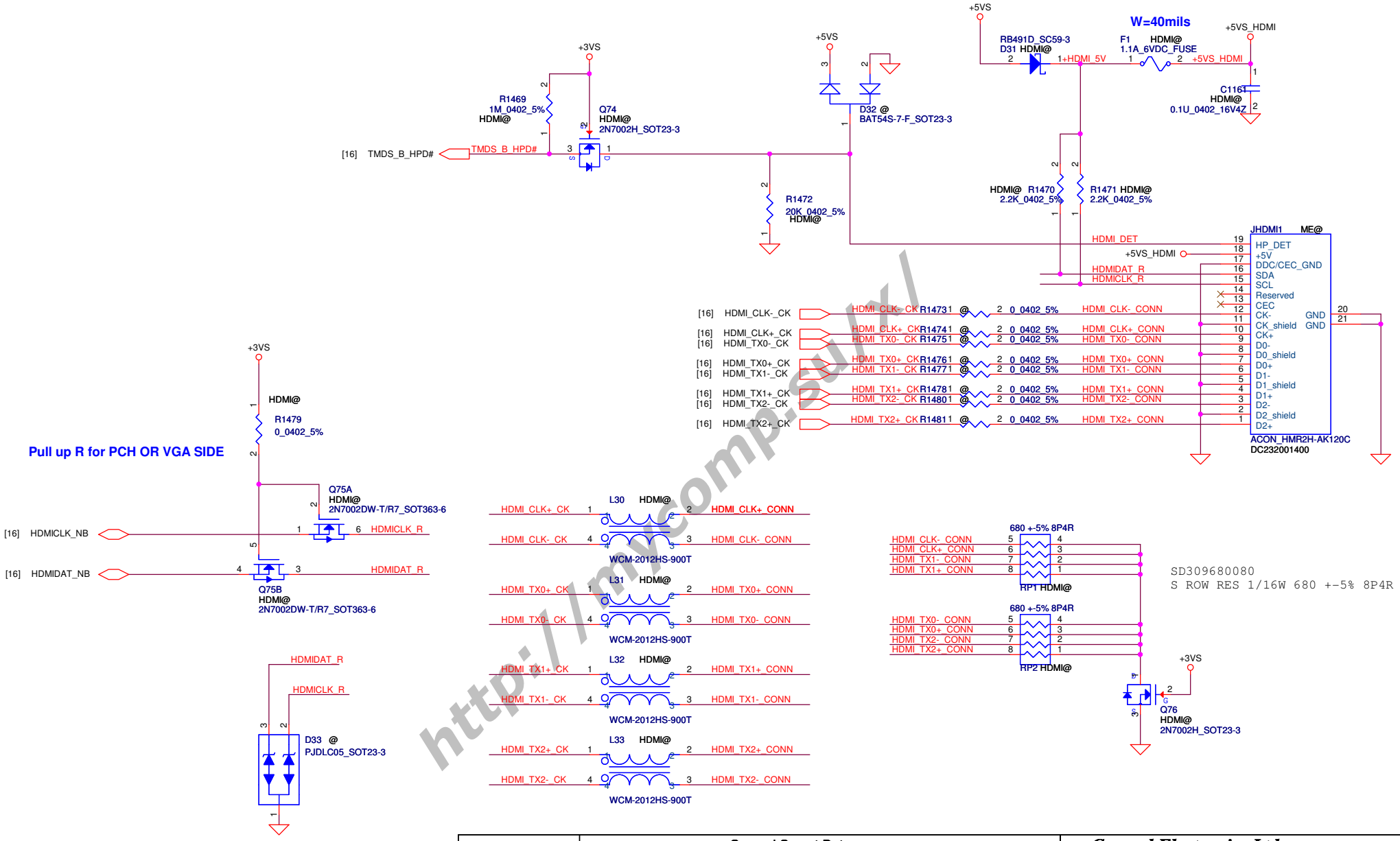
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **LVDS/CAMERA**

Size	Document Number	Rev
Custom	Sherry and Royal	0.1

Date: Thursday, February 02, 2012 | Sheet 29 of 55



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics,Ltd.

Title: HDMI CONN

Size: B | Document Number: Sherry and Royal | Rev: 0.1

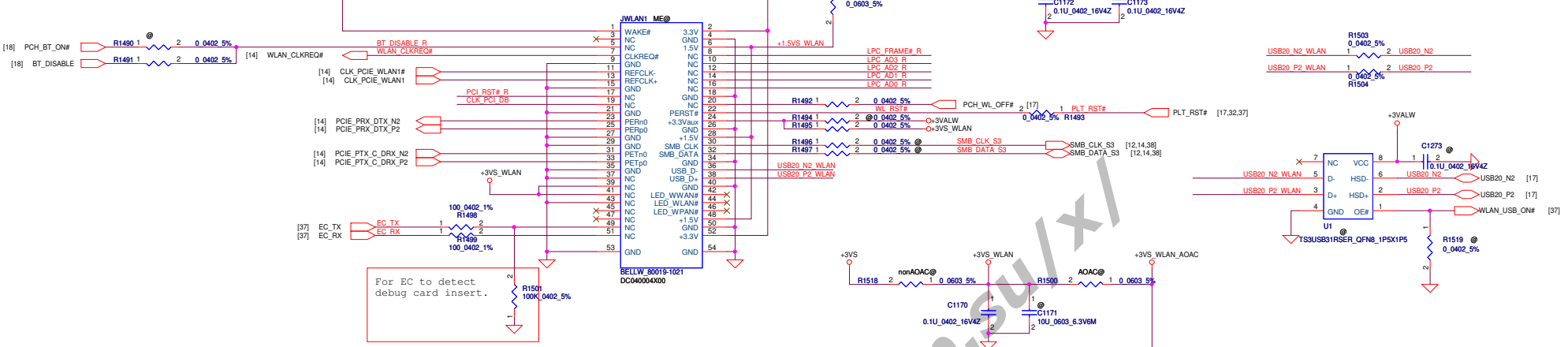
Date: Thursday, February 02, 2012 | Sheet 30 of 55

Mini-Express Card for WLAN/WiMAX(Half)
Mini-Express Card for SSD(Full)

Mini-Express Card(WLAN/WiMAX)

9/18 JP1 Pin2,24,52 contact to +3VS_WLAN for AOAC function

Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

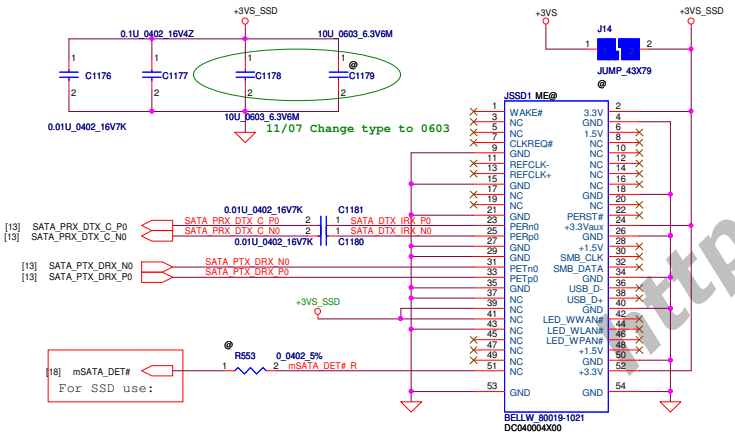


Mini-Express Card(SSD)

SSD Active:4.5W(1.5A)

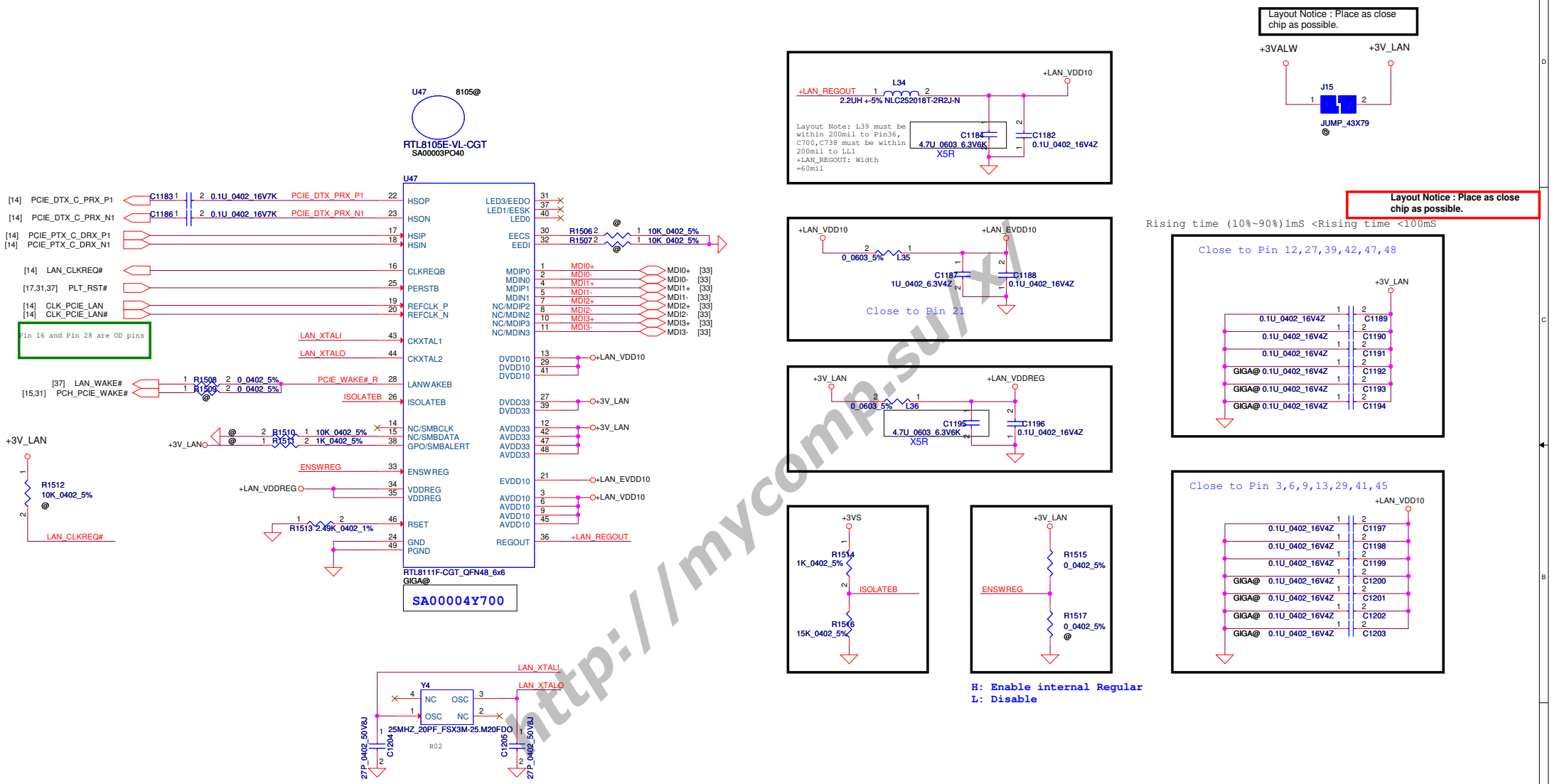
11/07 Change type to 0603

9/18 Increase for Intel AOAC function



Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title	Mini-Card		
Size	Document Number	Sherry and Royal	Rev 0.1
Date: Thursday, February 02, 2012	Sheet 31 of 55		



H: Enable internal Regular
L: Disable

Layout Notice : Place as close chip as possible.

Layout Notice : Place as close chip as possible.

Rising time (10%~90%)1mS <Rising time <100mS

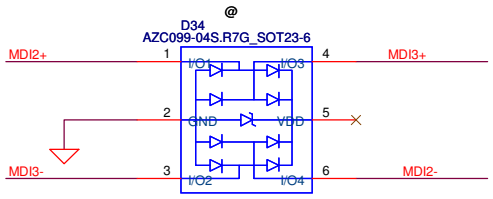
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

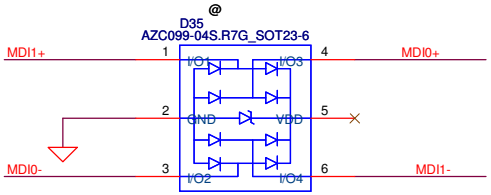
Title: LAN-RTL8111F/8105E

Size: Custom | Document Number: Sherry and Royal | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 32 of 55



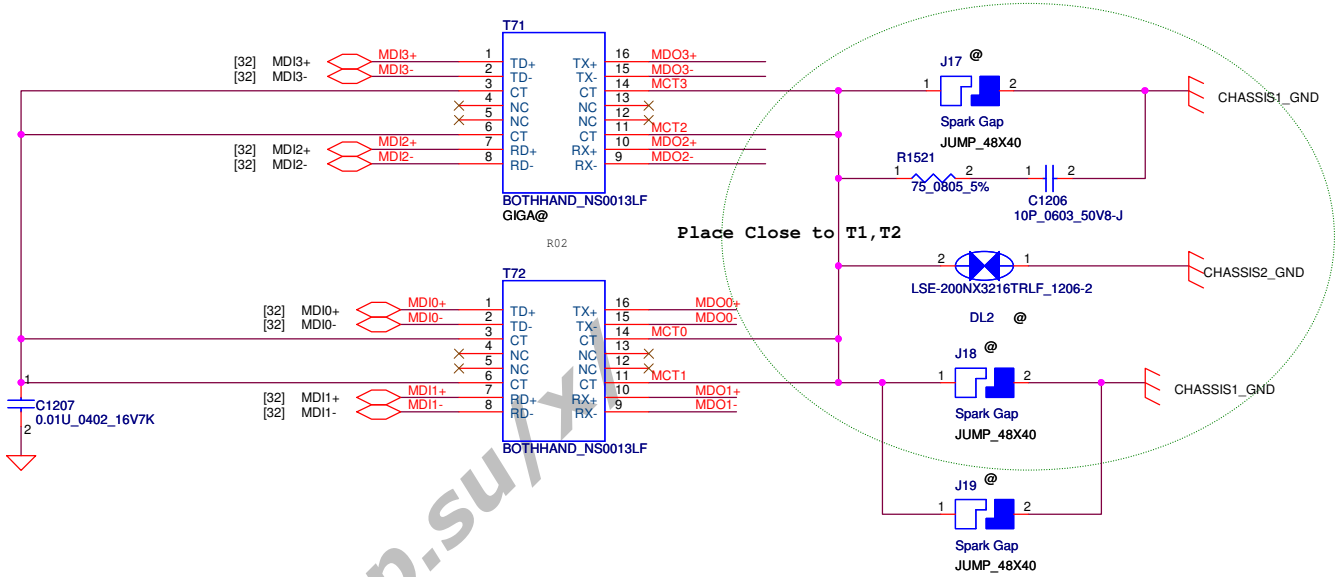
Place Close to T71

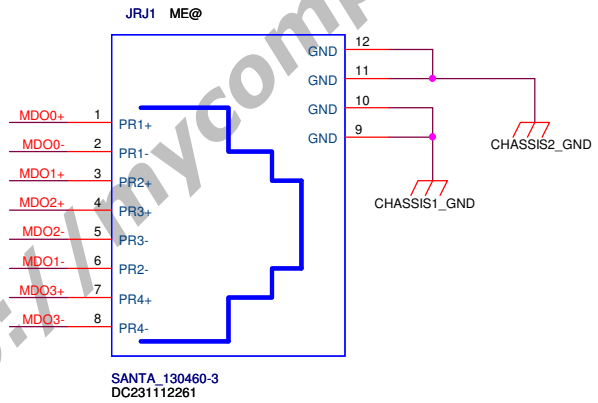


Place Close to T72

D34/D35
1'S PN:SC300001G00
2'S PN:SC300002E00

Reserve gas tube for EMI go rural solution





Reserve for EMI go rural solution

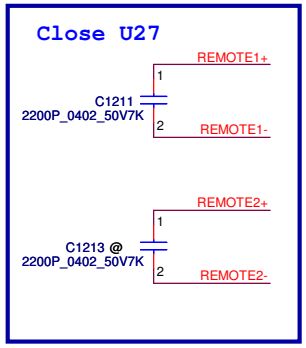
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

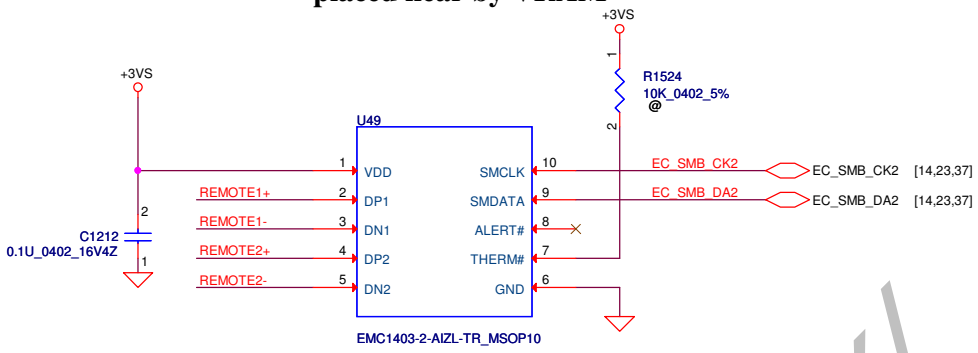
Title: LAN_Transformer

Size: B | Document Number: Sherry and Royal | Rev: 0.1

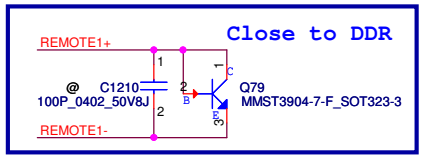
Date: Thursday, February 02, 2012 | Sheet 33 of 55

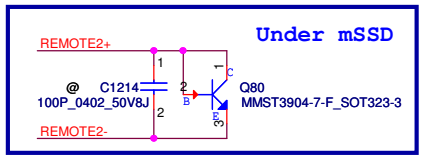


SMSC thermal sensor placed near by VRAM



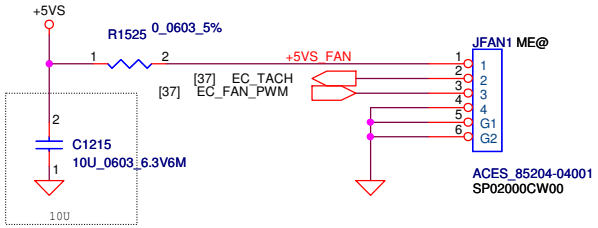
Address 1001_101xb



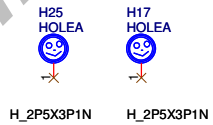


REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN1 Conn

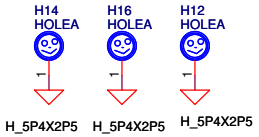


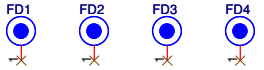
R



E

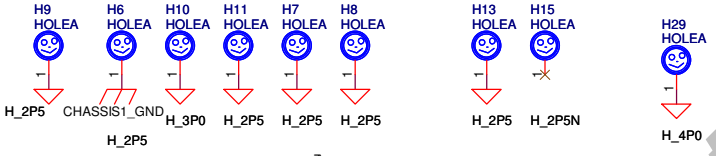
R





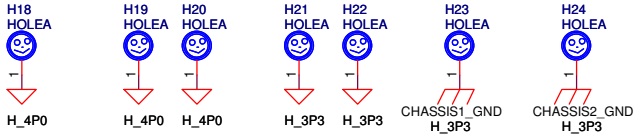
M/B 橢圓孔

M/B KB 橢圓孔



A

2P5 * 9 pcd



B CPU C GPU D LAN

F G

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics,Ltd.

Title: **Fintek-Thermal IC/FAN/screw**

Size: B | Document Number: **Sherry and Royal** | Rev: 0.1

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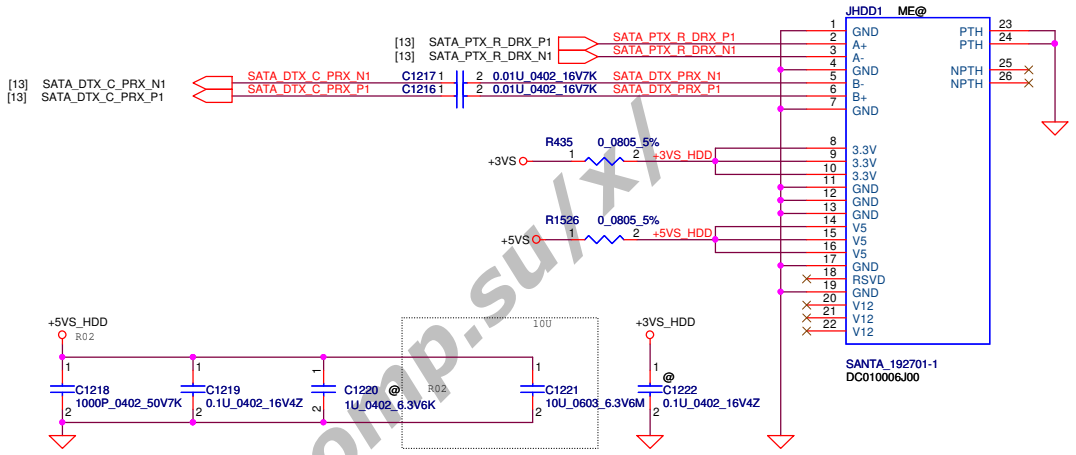
SATA HDD Conn.



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **HDD/ODD/BT Connector**

Size	Document Number	Rev
Custom	Sherry and Royal	0.1

Date: Thursday, February 02, 2012 | Sheet 35 of 55

600ohms @100MHz 1A
P/N: SM01000BU00

600ohms @100MHz 2A
P/N: SM01000EE00

Power down (PD#) power stage for save power
0V: Power down power stage
3.3V: Power up power stage

U50 ALC259Q-VC2-GR_QFN48_6X6

MIC Sense
R939 place near pin13

Capless HP Sense
R940 place near pin34

Vendor recommend. 2.2K

Vendor recommend. 2.2u

external MIC

Internal Speaker

Headphone

Place near Pin25

Place near Pin38

Place near Pin1

Place near Pin9

Place next to pin 27

0110 delete R1539

Pin Assignment	Location	Function
SPK-OUT (Pin40/41/44/45)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
MIC1(Pin21/22)	External	Mic in

wide 25MIL

JSPK1 ME@ ACES_88266-04001 SP02000K200

Reserve for ESD request.

Combo Jack detect (normal open)

EMI

PC Beep

EC Beep [37] BEEP#

PCH Beep [13] HDA_SPKR

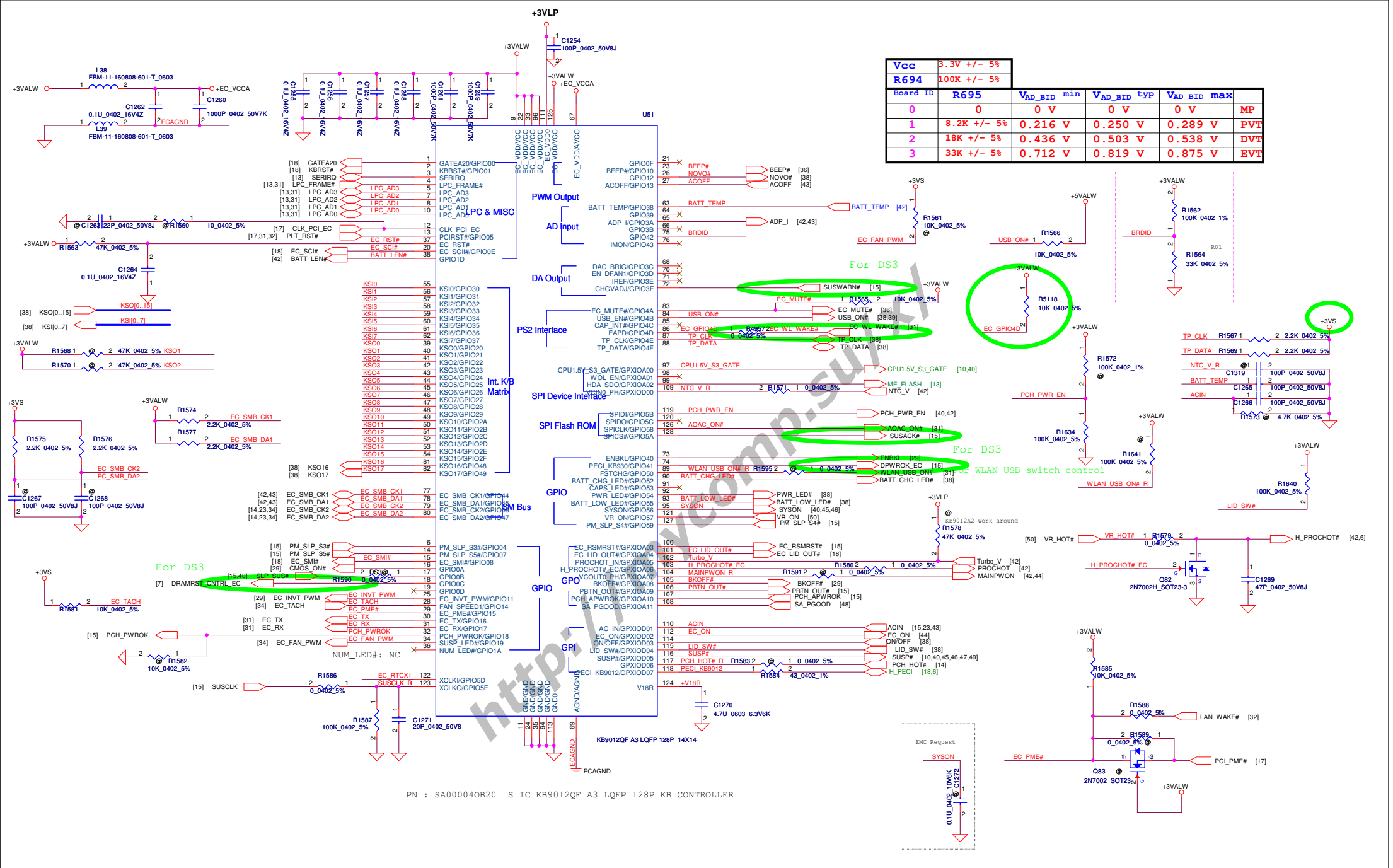
Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics,Ltd.

Title: HD Audio Codec_ALC259Q-VC

Size: C | Document Number: Sherry and Royal | Rev: 0.1

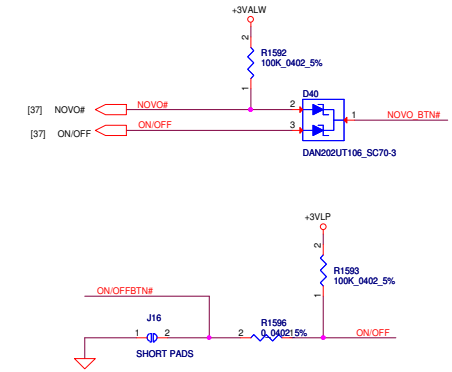
Date: Thursday, February 02, 2012 | Sheet 36 of 55

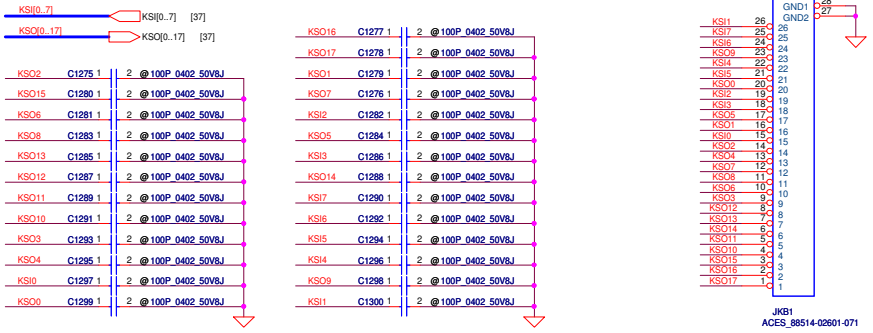


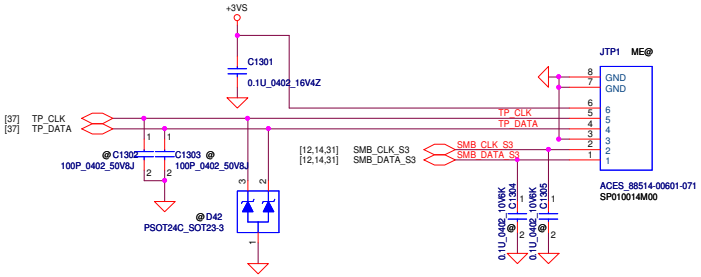
Vcc	3.3V +/- 5%				
R694	100K +/- 5%				
Board ID	R695	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	
0	0	0 V	0 V	0 V	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	EVT

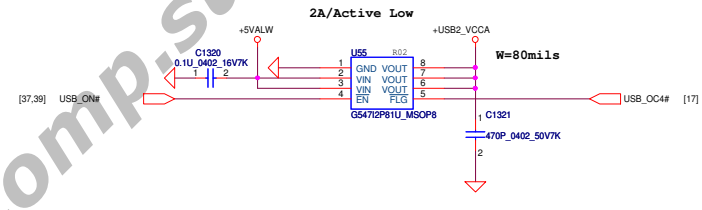
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title	BIOS & EC I/O Port		
Size	Document Number	Rev	
Custom	Sherry and Royal	0.1	
Date: Thursday, February 02, 2012	Sheet 37 of 55		

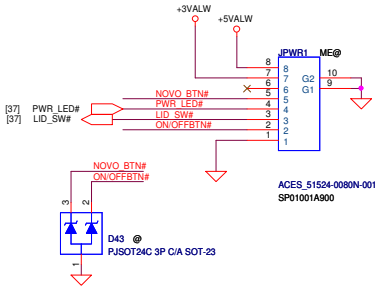




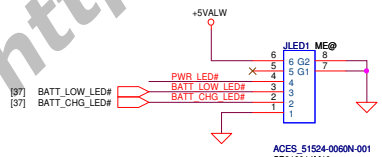




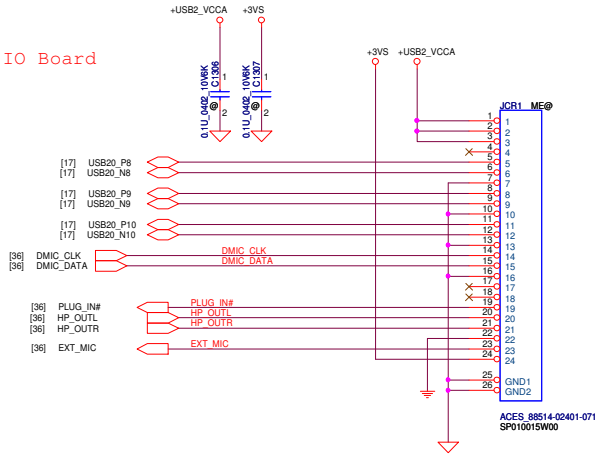
Power Board



LED Board

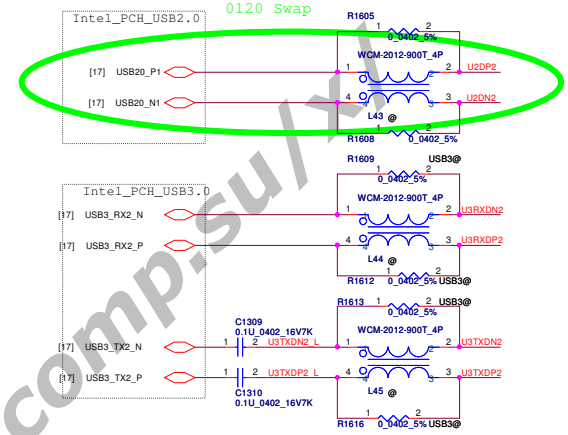


IO Board

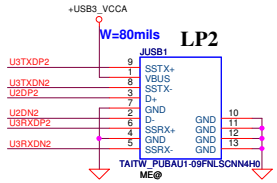


Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

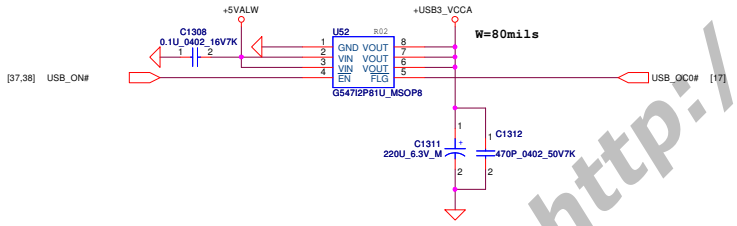
Title	Compal Electronics, Inc. ROM/KBD/PWR/CR/LED/TP Conn.		
Size C	Document Number Sherry and Royal		Rev 0.1
Date: Thursday, February 02, 2012	Sheet 38 of 55		

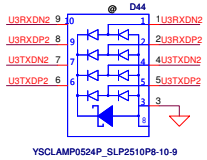


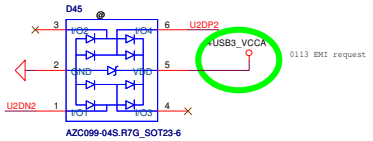
Place TX AC coupling Cap (C843~C850). Close to connector



2A/Active Low







For EMI request

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: USB3.0/Left USB Ports

Size	Document Number	Rev
Custom		0.1

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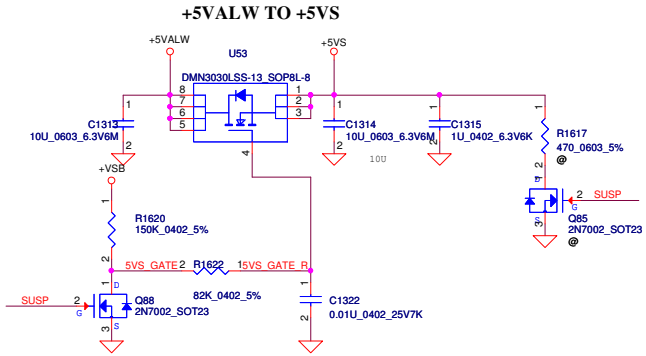
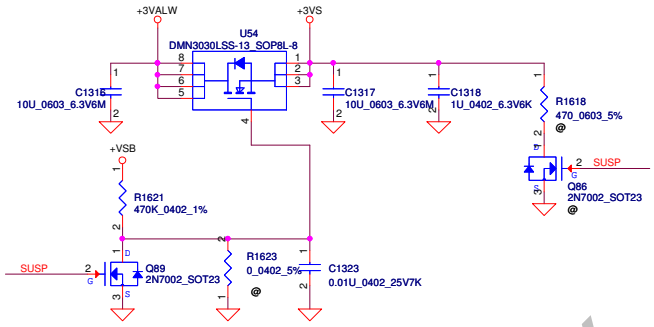
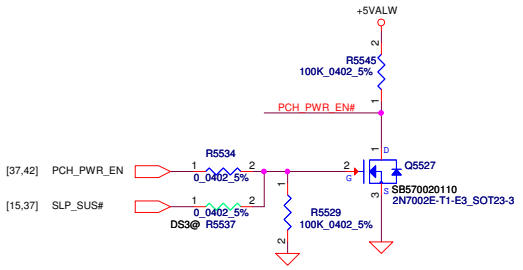
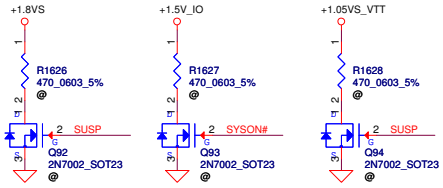
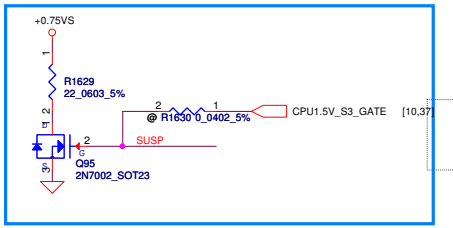


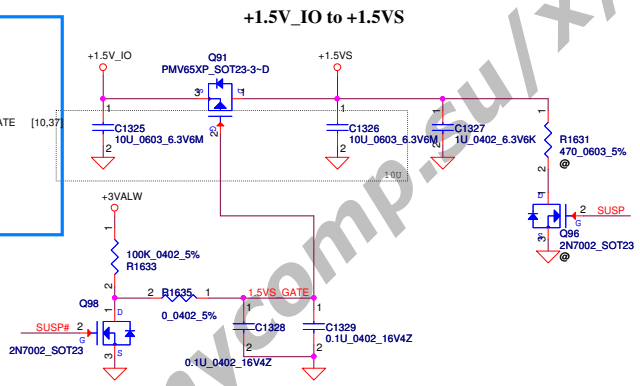


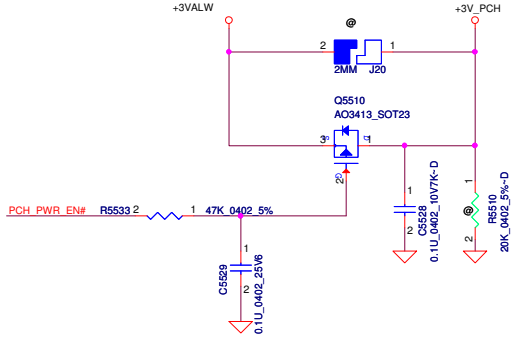


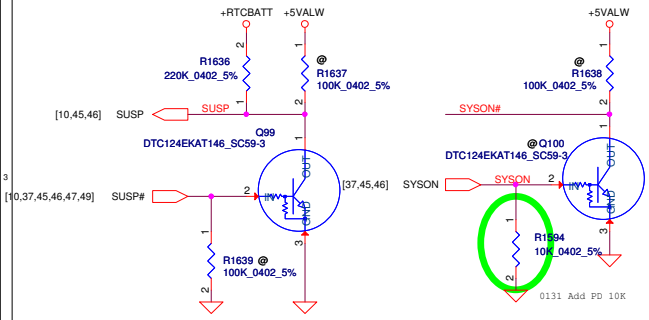


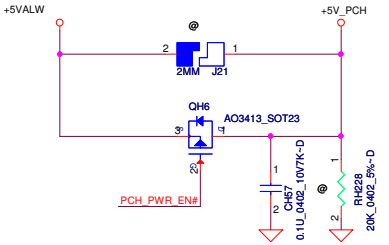


For Intel S3 Power Reduction.









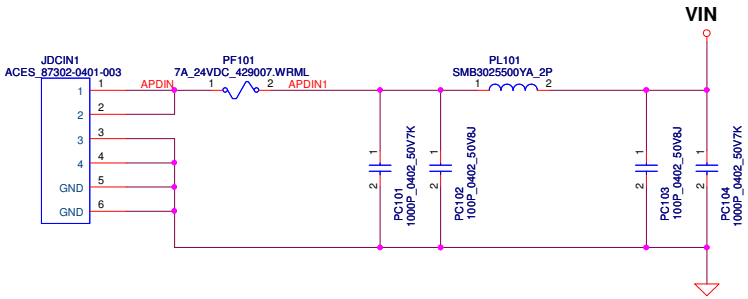
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

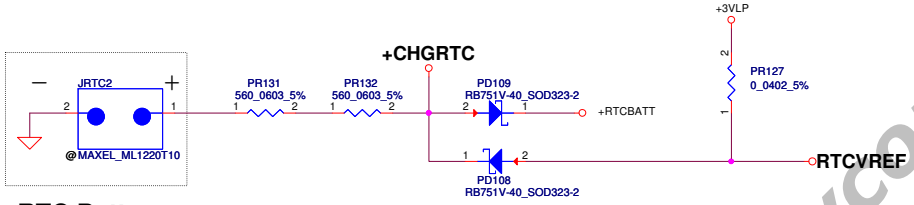
Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: Sherry and Royal | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 40 of 55





RTC Battery

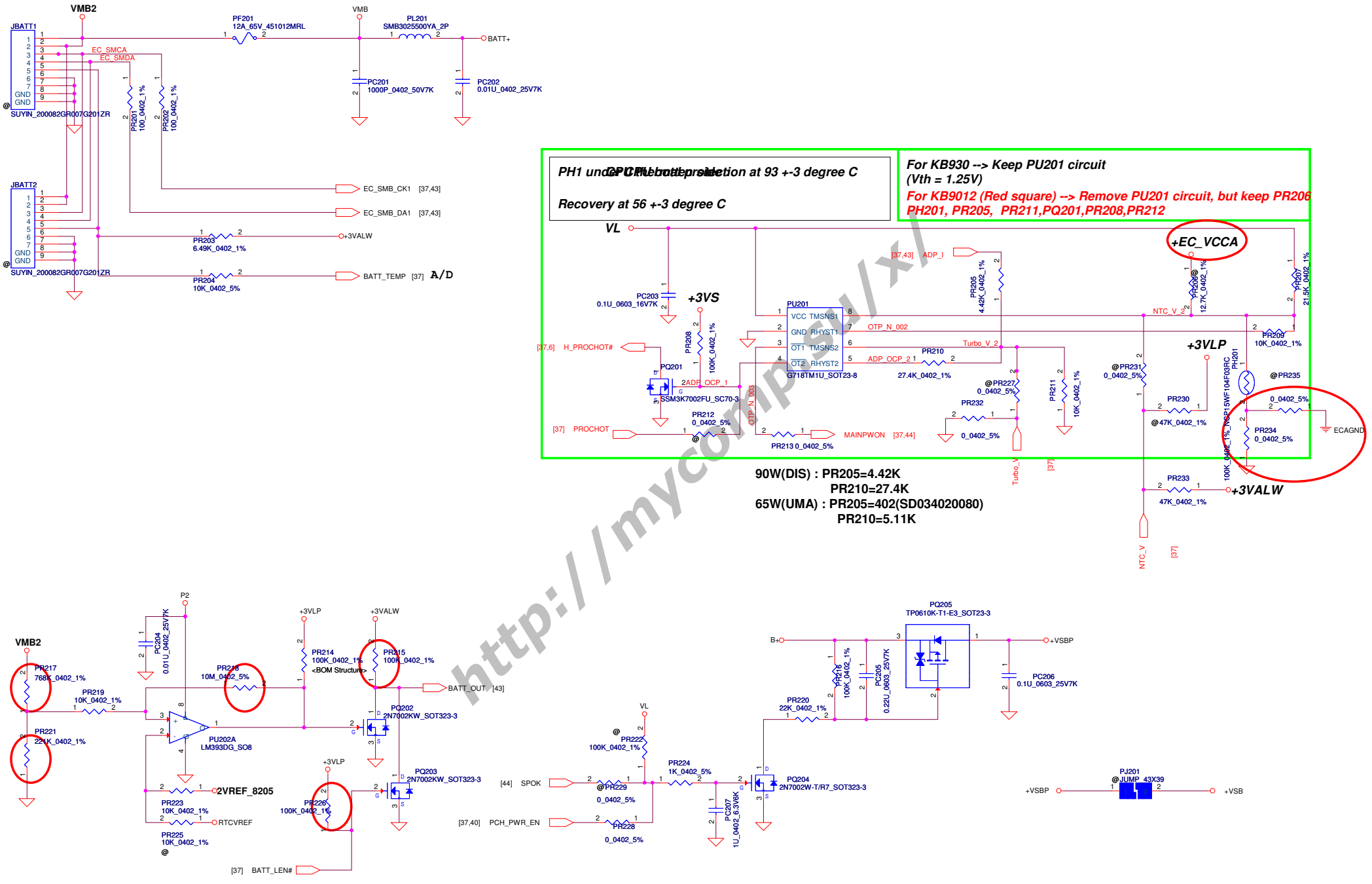
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR DCIN

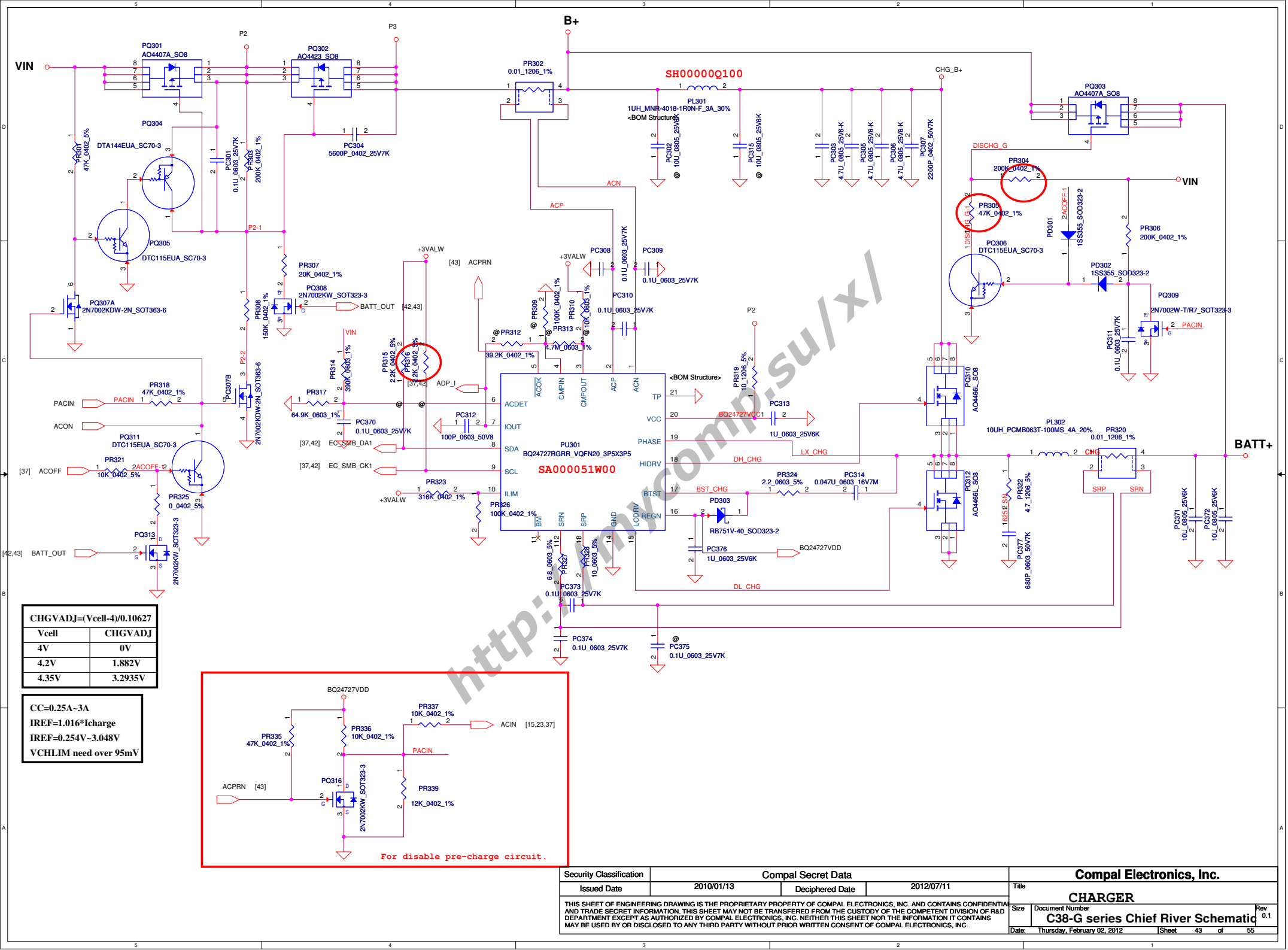
Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 41 of 55



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.	
Title	PWR-BATTERY CONN/OTP
Size: Custom	Document Number: C38-G series Chief River Schematic
Rev: 0.1	
Date: Thursday, February 02, 2012	Sheet 42 of 55



CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2012/07/11

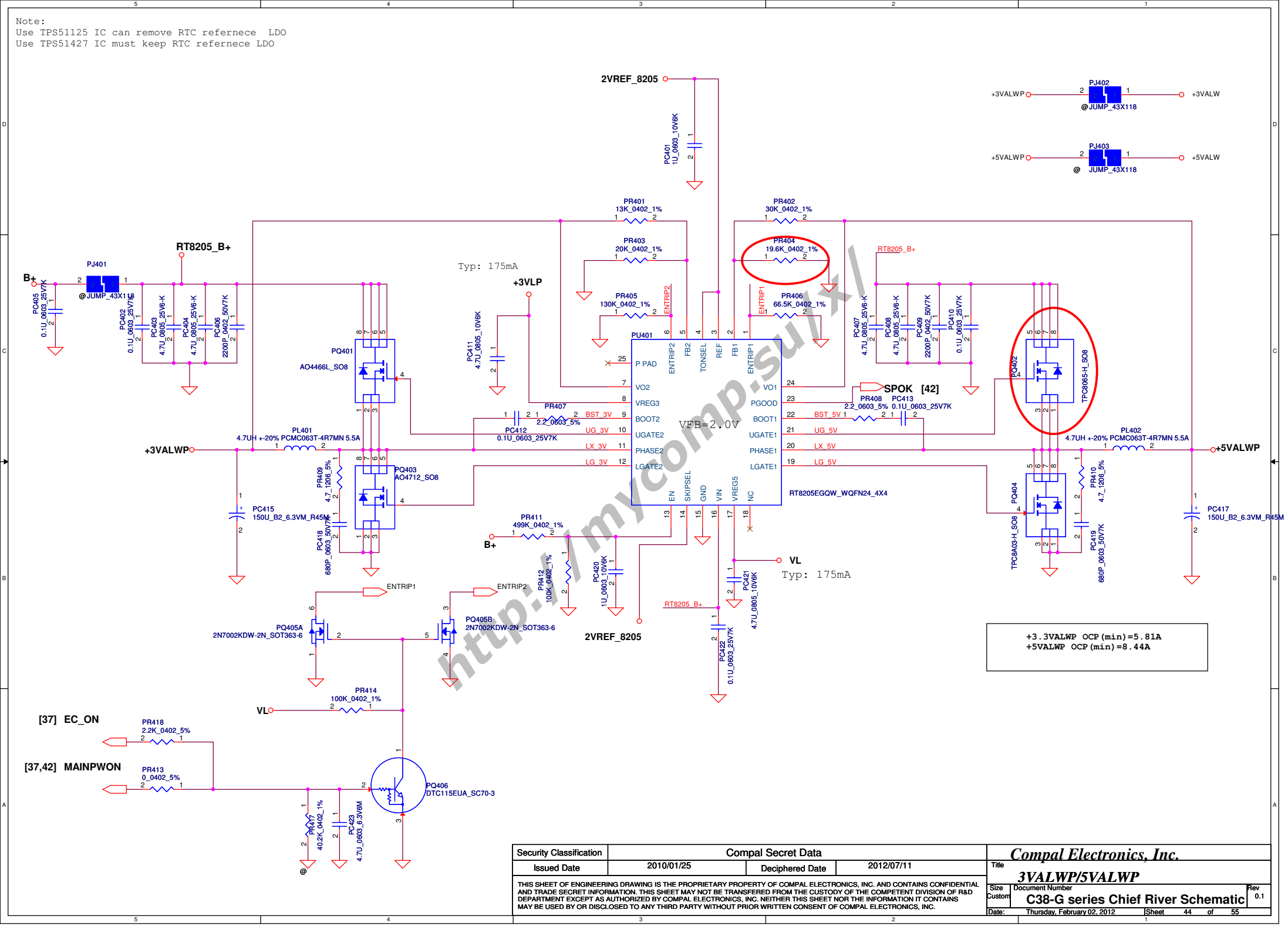
Compal Electronics, Inc.

Title: CHARGER

Size | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 43 of 55

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

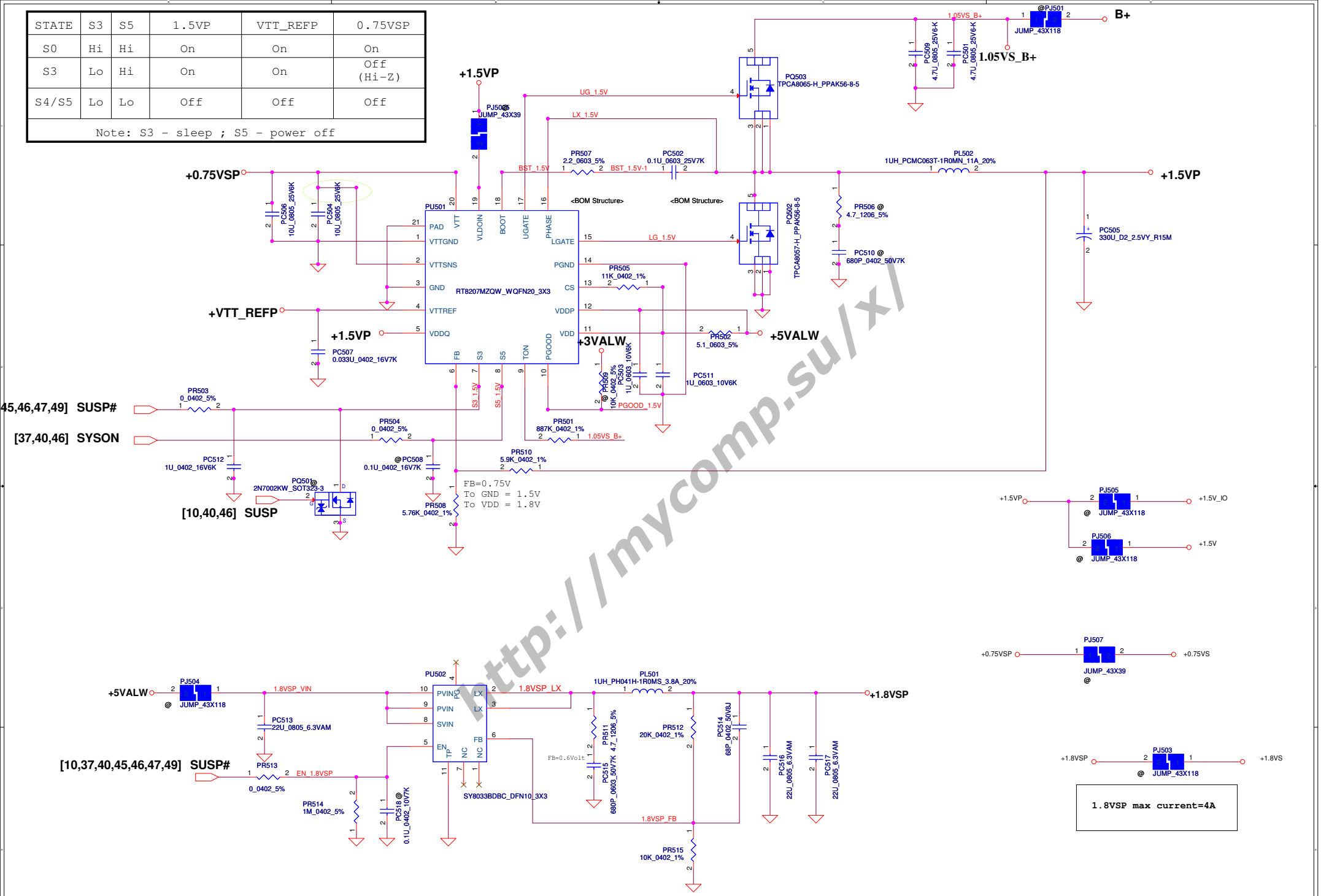
Title: 3VALWP/5VALWP

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 44 of 55

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

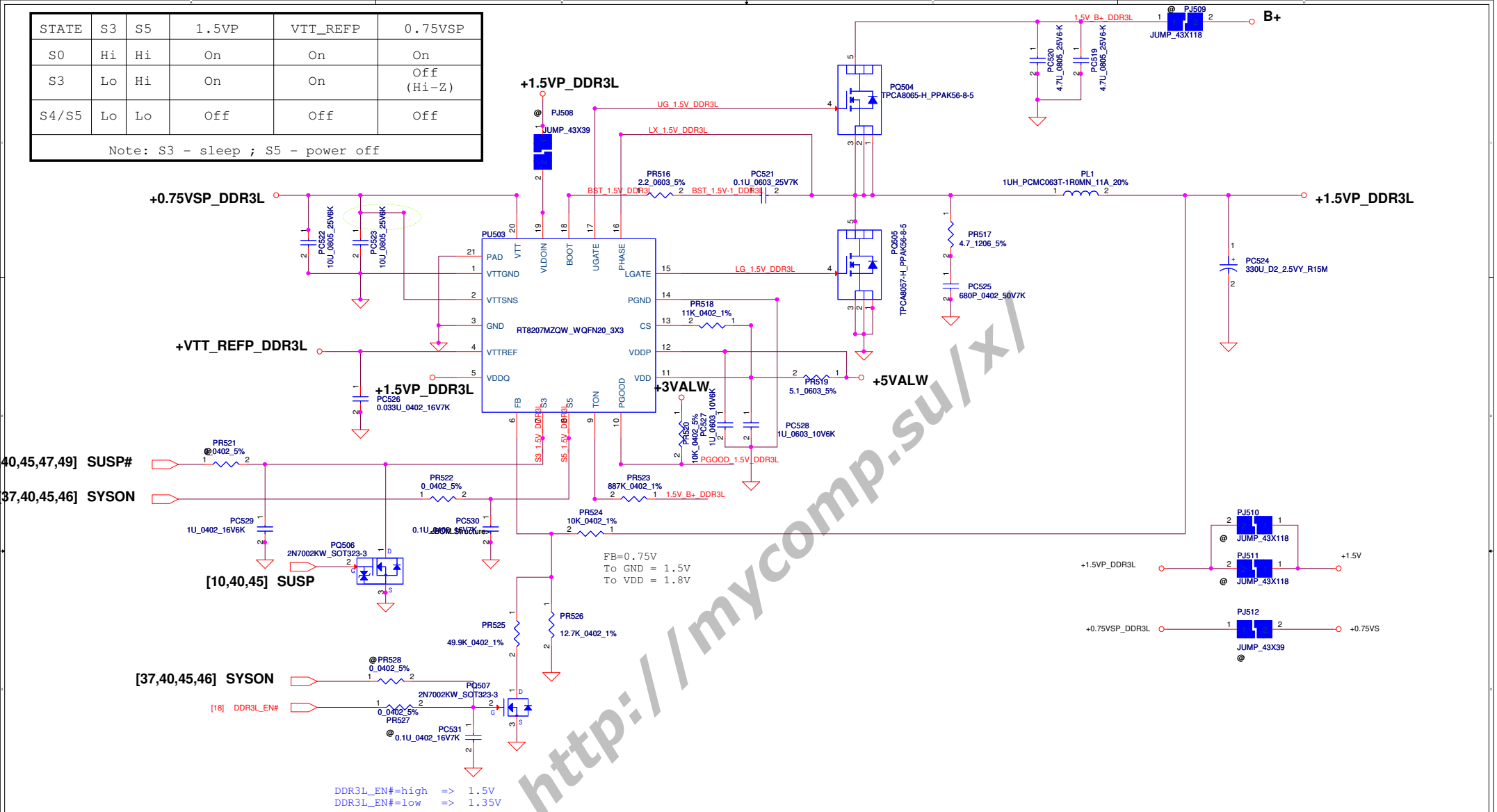
Title: PWR-+1.5VP/+1.8VSP

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 45 of 55

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off



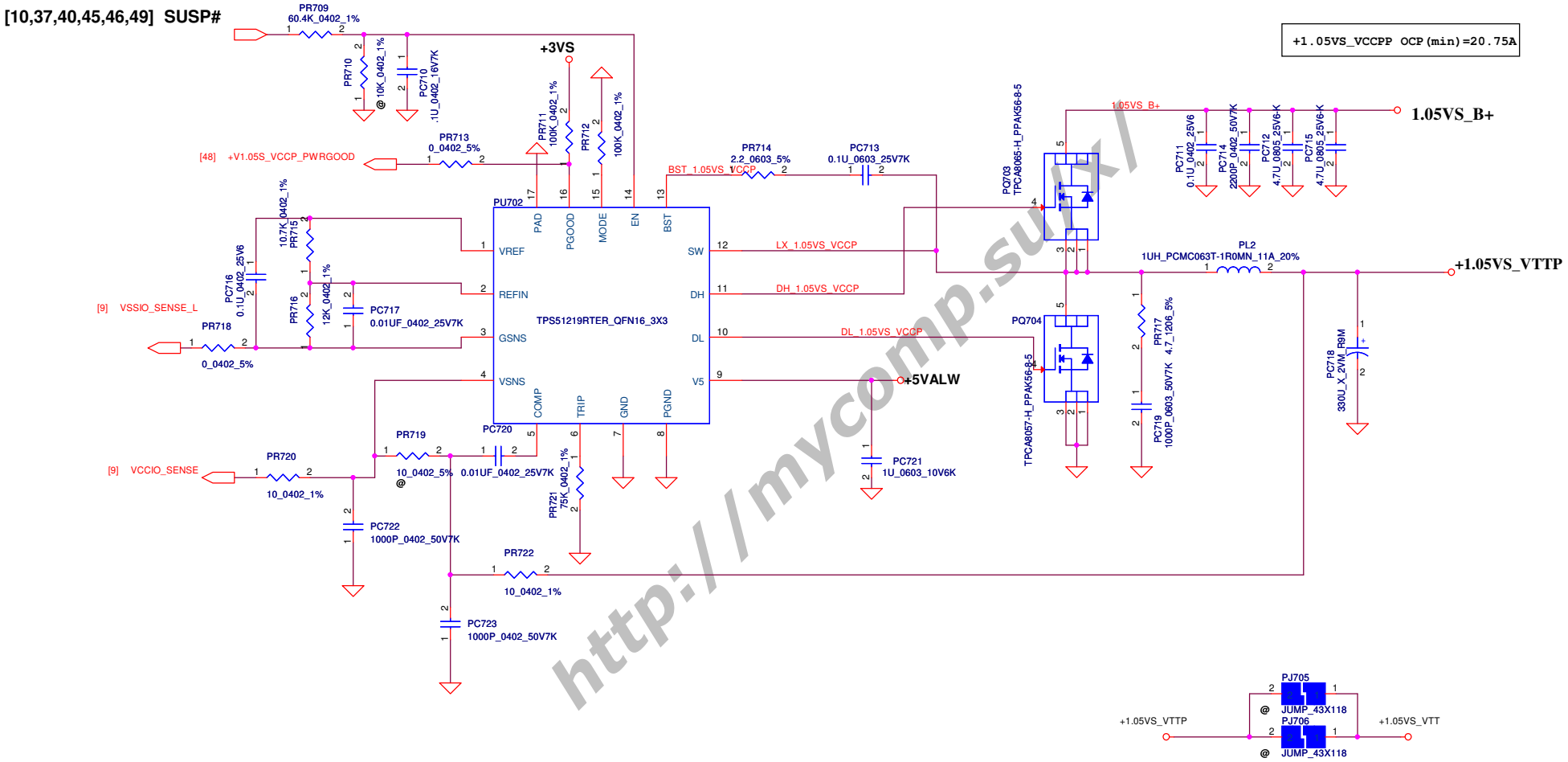
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR-+1.5VP/+1.8VSP

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 46 of 55



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR +1.05VS_VCCPP/

Size	Document Number	Rev
Custom	C38-G series Chief River Schematic	0.1

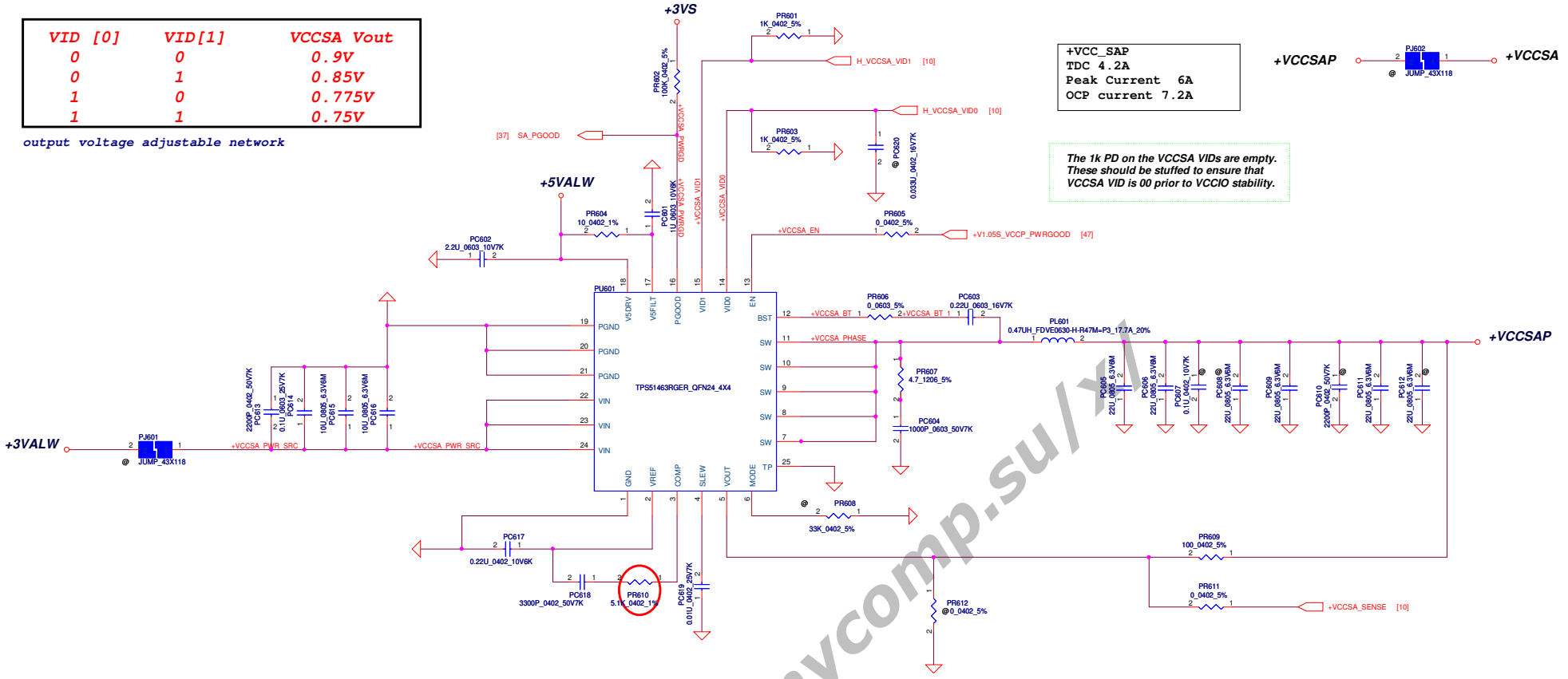
Date: Thursday, February 02, 2012 Sheet 47 of 55

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



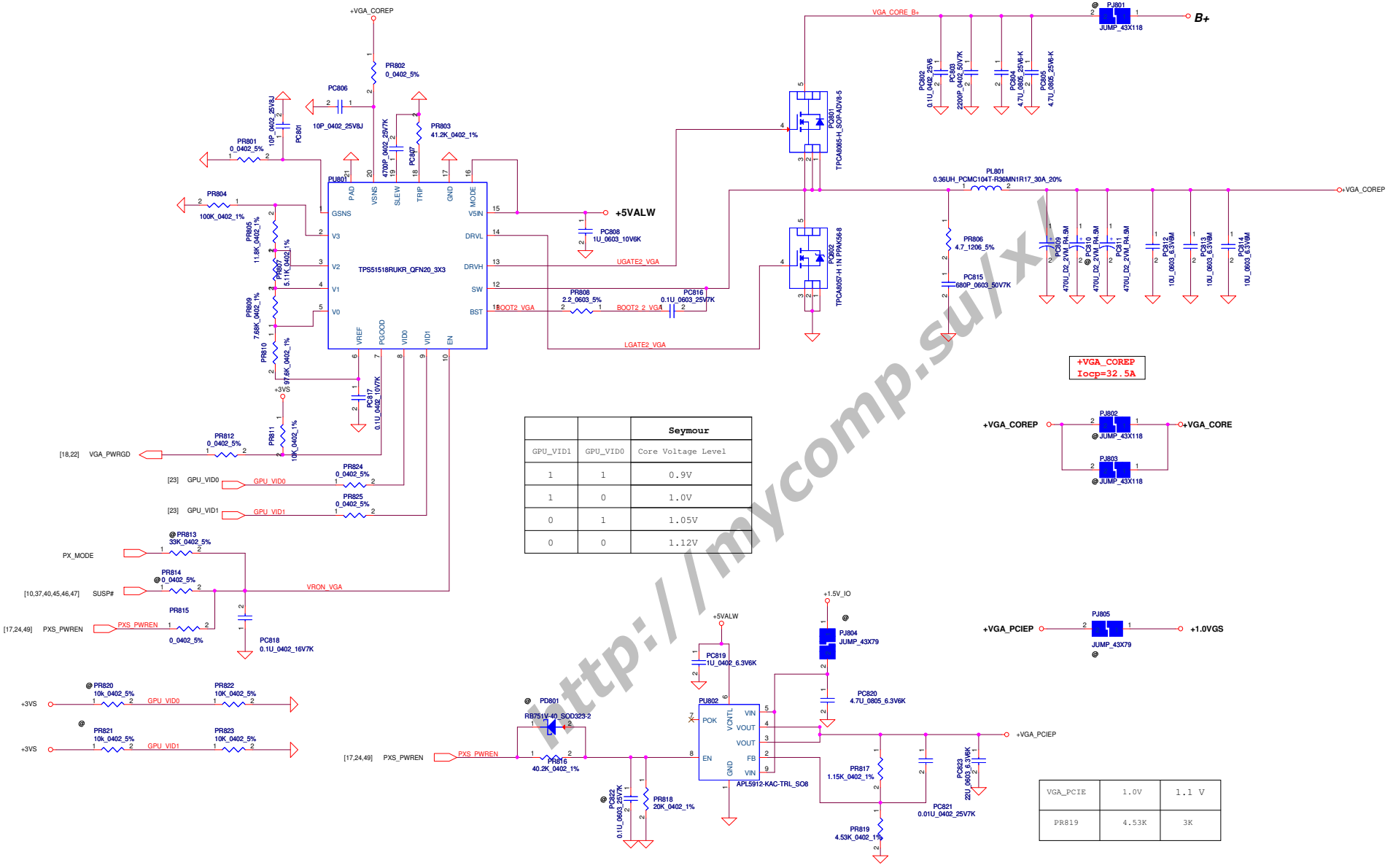
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR +VCCSAP

Size	Document Number	Rev
C	C38-G series Chief River Schematic	0.1

Date: Thursday, February 02, 2012 Sheet 48 of 55



		Seymour
GPU_VID1	GPU_VID0	Core Voltage Level
1	1	0.9V
1	0	1.0V
0	1	1.05V
0	0	1.12V

VGA_PCIE	1.0V	1.1 V
PR819	4.53K	3K

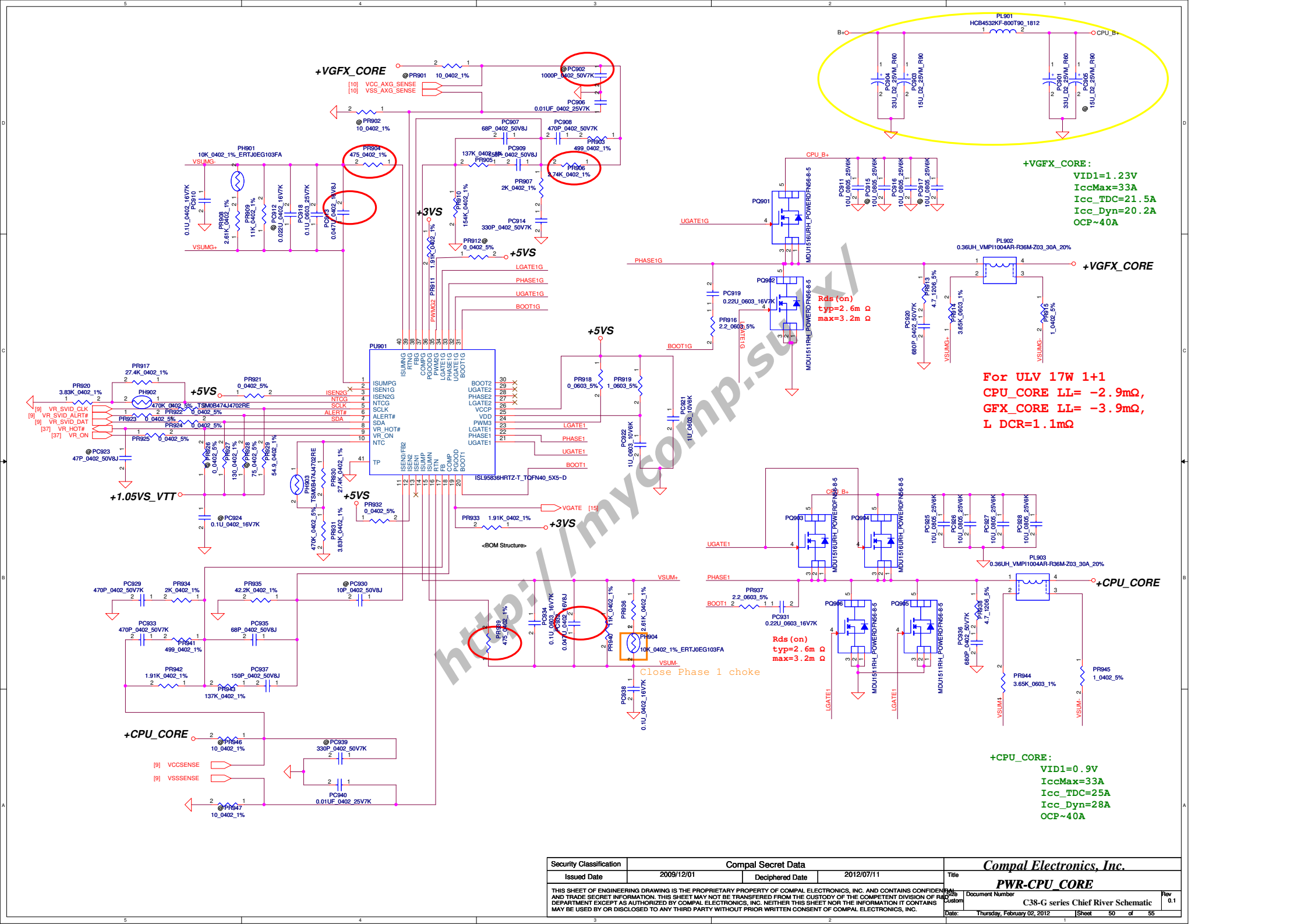
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: **PWR-VGA_CORE/VGA_PCIE**

Size	Document Number	Rev
		0.1

Date: Thursday, February 02, 2012 | Sheet 49 of 55



Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2012/07/11

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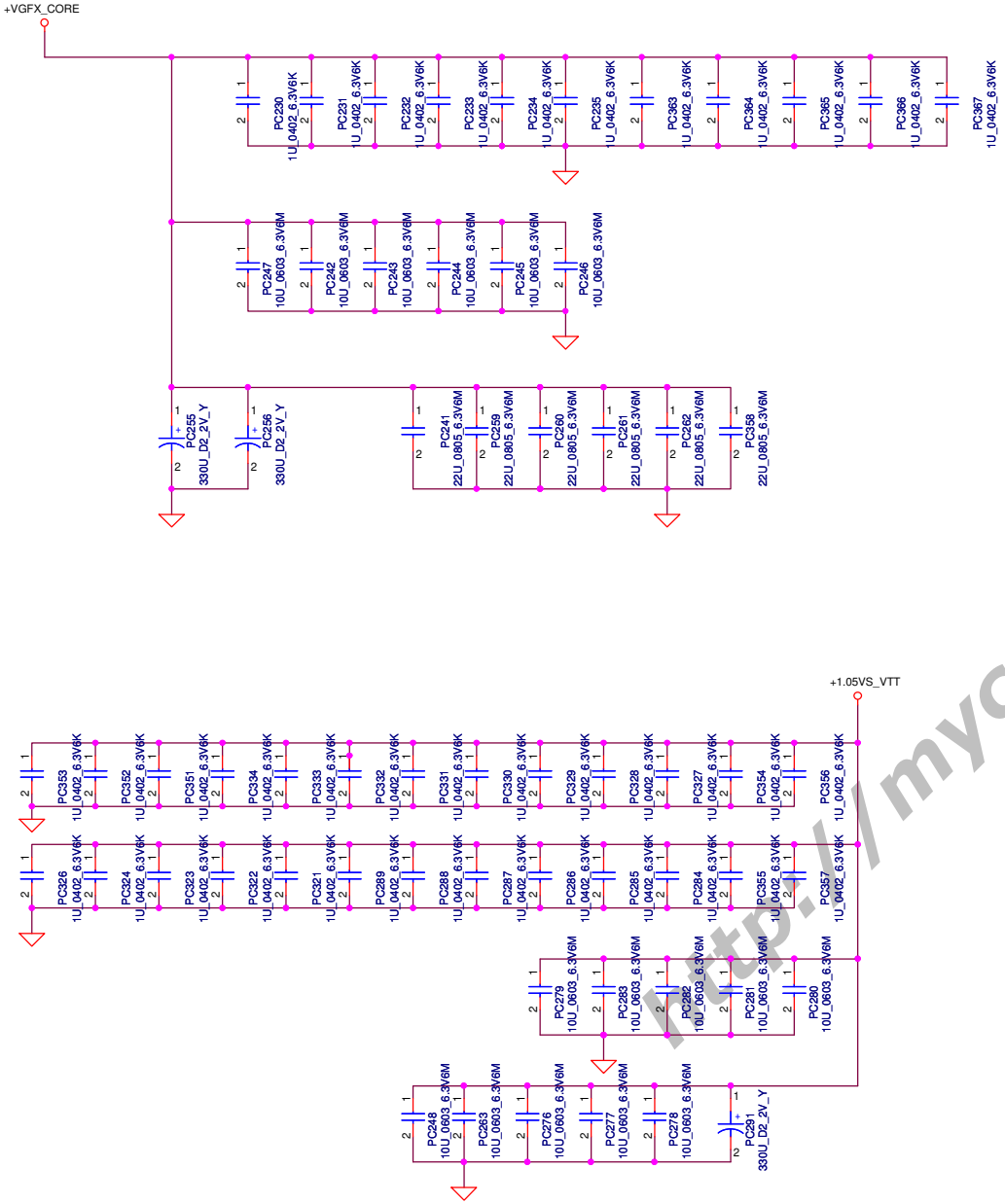
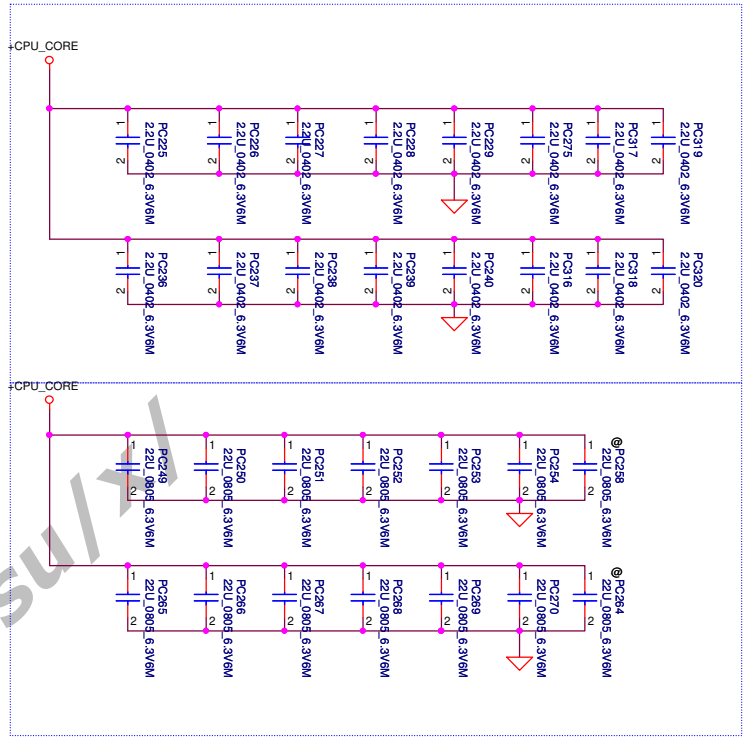
Compal Electronics, Inc.

Title: PWR-CPU_CORE

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 50 of 55





Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: CPU_CORE_CAP

Size	Document Number	Rev
Custom		0.1

Date: Thursday, February 02, 2012 Sheet 51 of 55

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2012/07/11

Compal Electronics, Inc.

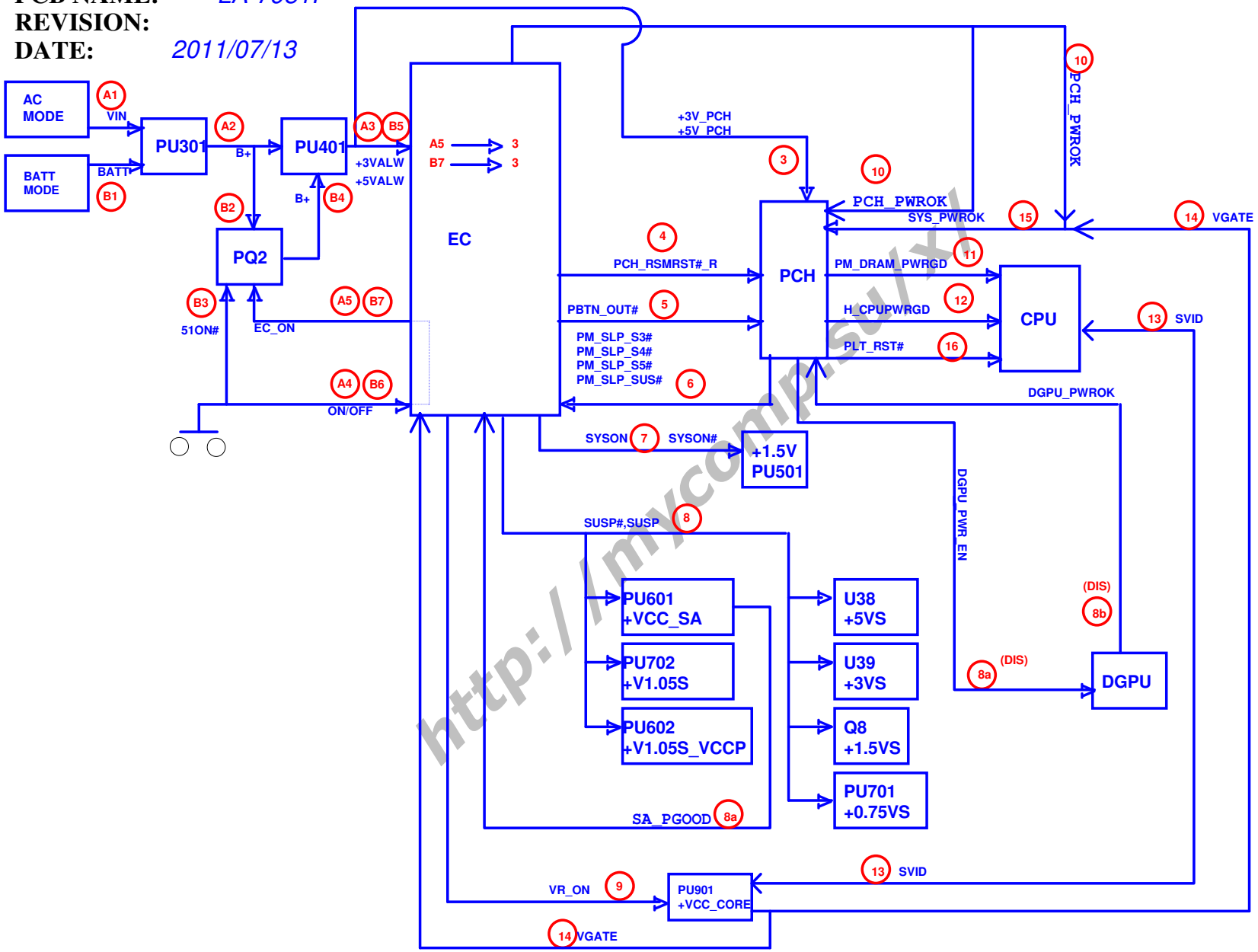
Title: **PIR (PWR)**

Size	Document Number	Rev
Custom	C38-G series Chief River Schematic	0.1

Date: Thursday, February 02, 2012 | Sheet 52 of 55

COMPAL CONFIDENTIAL

MODEL NAME: *Power Sequence Block Diagram*
PCB NAME: *LA-7981P*
REVISION:
DATE: *2011/07/13*



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: ***Power sequence***

Size: Custom | Document Number: ***Sherry and Royal*** | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 53 of 55

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Initial				DVT
2					
3					
4					
5					
6					
7					
8					
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10					
11					
12					
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