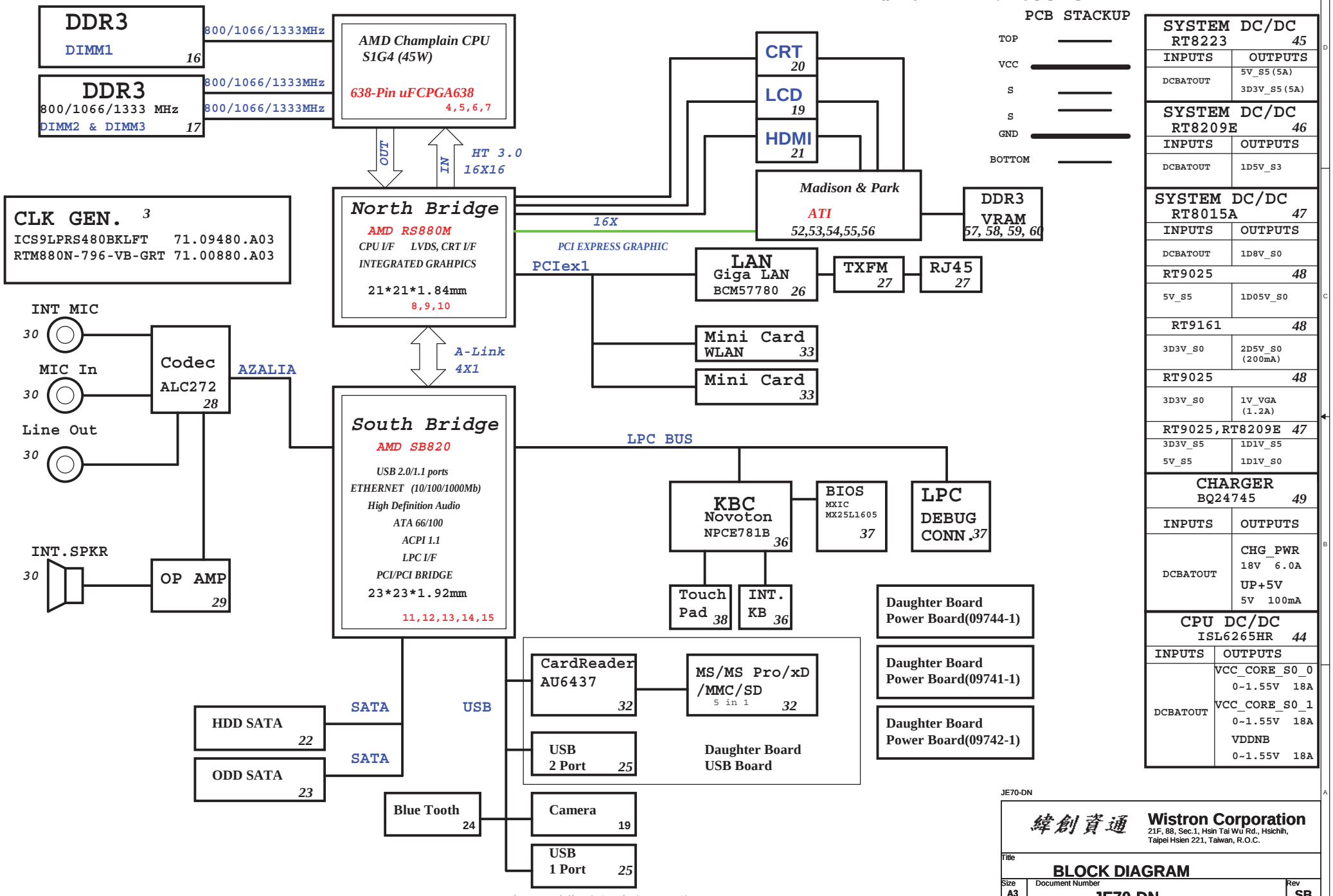
JE70-DN/SJV71-DN/HM72-DN Block Diagram

Project code: 91.4HP01.001
PCB P/N : 48.4HP01.011
REVISION : 09929-1



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC RT8223 45

INPUTS	OUTPUTS
DCBATOUT	5V_S5(5A) 3D3V_S5(5A)

SYSTEM DC/DC RT8209E 46

INPUTS	OUTPUTS
DCBATOUT	1D5V_S3

SYSTEM DC/DC RT8015A 47

INPUTS	OUTPUTS
DCBATOUT	1D8V_S0

RT9025 48

5V_S5	1D05V_S0

RT9161 48

3D3V_S0	2D5V_S0 (200mA)

RT9025 48

3D3V_S0	1V_VGA (1.2A)

RT9025,RT8209E 47

3D3V_S5	1D1V_S5
5V_S5	1D1V_S0

CHARGER BQ24745 49

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265HR 44

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A VCC_CORE_S0_1 0~1.55V 18A VDDNB 0~1.55V 18A

JE70-DN

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Title: BLOCK DIAGRAM
Size: A3 | Document Number: JE70-DN | Rev: SB
Date: Wednesday, March 31, 2010 | Sheet 1 of 63

page36

EC Functional Strap Definitions

Signal	Comment
TEST# pin110	Test Mode Select. Sampled at VCC Power-Up reset or VCC_POR Input reset, to determine the device operation mode as follows: **No pull-down resistor: Normal operation mode (XORTR and TRIST strap pins are ignored).** 10 KΩ external pull-down resistor:Test mode (ICT or XOR-Tree Test mode, according to XORTR and TRIST strap pins).
XORTR# pin111	XOR-Tree Mode Select. Sampled at VCC Power-Up reset or VCC_POR Input reset, to select the XOR-Tree Test mode, if TEST is strapped low: No pull-down resistor: Not allowed if TEST pin is strapped low. **10 KΩ external pull-down resistor:XOR-Tree Test mode .Note: TRIST strap pin must be left unconnected.**
TRIST# pin112	ICT Mode Select. Sampled at VCC Power-Up reset or VCC_POR Input reset, to select the ICT Test mode, if TEST is strapped low: **No pull-down resistor: Not allowed if TEST pin is strapped low.** 10 KΩ external pull-down resistor:ICT Test mode (see Section 3.4.1 on page 53), forces the device to float its output and I/O pins.Note: XORTR strap pin must be left unconnected.
JEN0#, JENK# pin49,53	JTAG Select. Sampled at VCC Power-Up reset or VCC_POR Input reset, to select the JTAG signals to device pins (see Table 4 on page 35 for details). **Both JEN0 and JENK, are pulled to 1 by an internal resistor** The external 10 KΩ pull-down resistor must be connected to GND.
SHBM pin83	Shared Host BIOS Memory. Sampled at VCC Power-Up reset or VCC_POR Input reset, to determine the state of the shared BIOS memory. **No pull-down resistor:Disable the shared BIOS memory.** 10 KΩ external pull-down resistor:Enable the shared BIOS memory
SDP_VIS# pin41	Port80 (SDP) Visibility Mode Select. Sampled at VCC Power-Up reset or VCC_POR Input reset, to select the Visibility mode for the Port80 (SDP). **No pull-down resistor: SDP in Normal mode** 10 KΩ external pull-down resistor:SDP in Visibility mode.
XOR_OUT pin35	XOR-Tree Output. The device pins are internally connected in a XOR-tree structure

page9

STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
*1 :Disable 0 : Enable

RS780: Enables Side port memory (RS880 use HSYNC#)

*1 :Disable 0 : Enable

SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected

page15

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Note: SB820 has 15K internal PU FOR PCI_AD[27:23]

page15

	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	AZ_SDOUT	GPIO200 GPIO199
PULL HIGH	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	LOW POWER MODE	H,H = Reserved H,L = SPI ROM
PULL LOW	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	PERFORMANCE MODE DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM

NOTE: SB820 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

page12

	USB Pair	USB Device
	12	MINI2 CARD
	11	NC
	10	NC
	9	CCD
	8	NC
	7	Bluetooth
	6	USB3
OCP3#	5	USB2
	4	CardReader
	3	NC
OCP2#	2	USB4
	1	MINI1 CARD
OCP0#	0	USB1

JE70-DN

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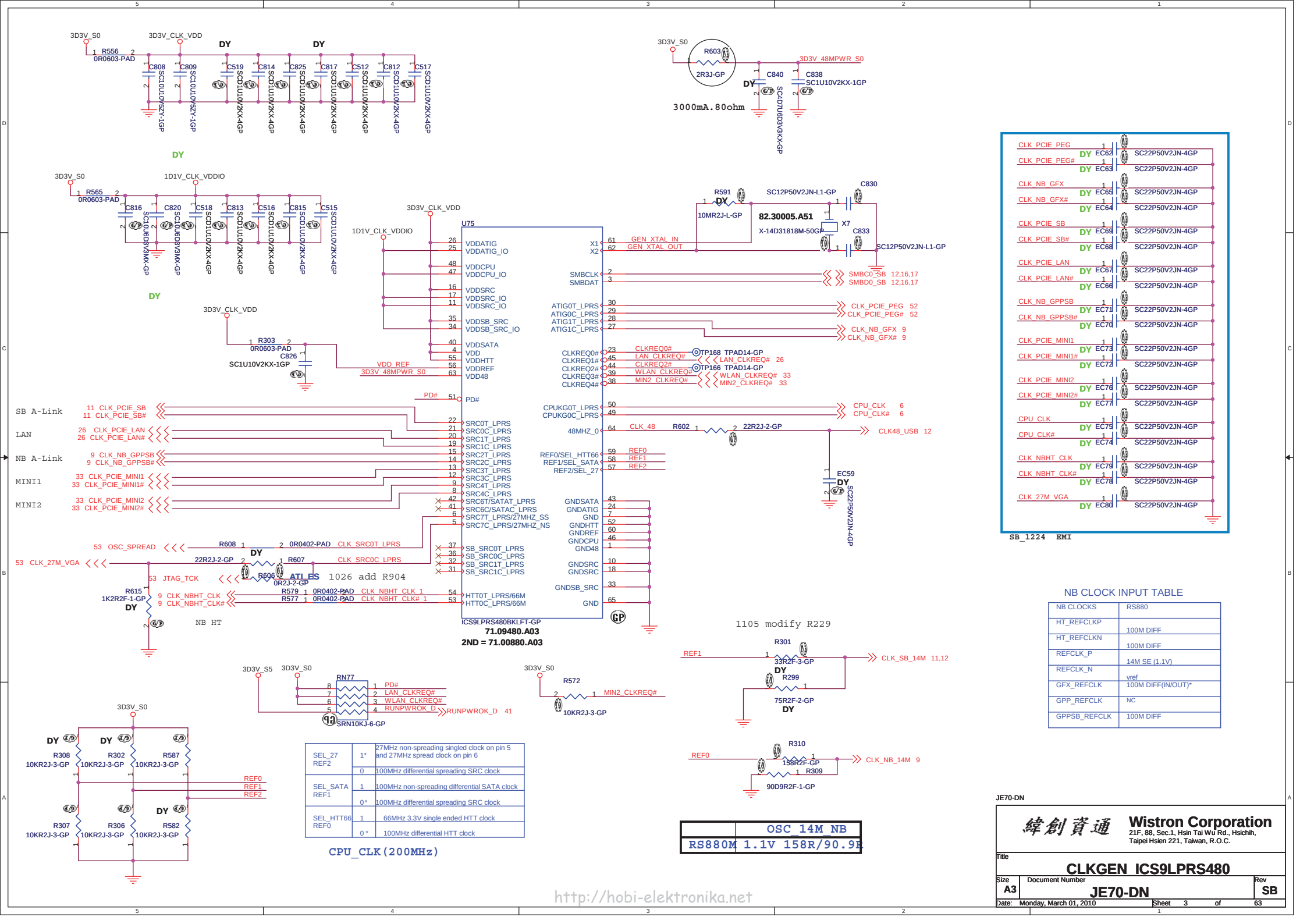
Title: Reference

Size	Document Number	Rev
A3	JE70-DN	SB

Date: Thursday, November 19, 2009 Sheet 2 of 63


3D3V_S0
3D3V_CLK_VDD
R556
0R0603-PAD
C808 SC10U10V5ZY-1GP
C809 SC10U10V5ZY-1GP
C519 SCD1U10V2KX-4GP
C814 SCD1U10V2KX-4GP
C825 SCD1U10V2KX-4GP
C817 SCD1U10V2KX-4GP
C512 SCD1U10V2KX-4GP
C812 SCD1U10V2KX-4GP
C517 SCD1U10V2KX-4GP
DY
3D3V_S0
R603
2R3J-GP
3D3V_48MPWR_S0
C840
DY
C838 SC1U10V2KX-1GP
SC4D7U6D3V3KX-GP
3000mA.80ohm
3D3V_S0
1D1V_CLK_VDDIO
R565
0R0603-PAD
C816 SC10U6D3V3MX-GP
C820 SC10U6D3V3MX-GP
C518 SCD1U10V2KX-4GP
C813 SCD1U10V2KX-4GP
C516 SCD1U10V2KX-4GP
C815 SCD1U10V2KX-4GP
C515 SCD1U10V2KX-4GP
DY
3D3V_CLK_VDD
1D1V_CLK_VDDIO
U75
VDDATIG
VDDATIG_IO
VDDCPU
VDDCPU_IO
VDDSRC
VDDSRC_IO
VDDSRC_IO
VDDSB_SRC
VDDSB_SRC_IO
VDDSATA
VDD
VDDHTT
VDDREF
VDD48
PD#
SRC0T_LPRS
SRC0C_LPRS
SRC1T_LPRS
SRC1C_LPRS
SRC2T_LPRS
SRC2C_LPRS
SRC3T_LPRS
SRC3C_LPRS
SRC4T_LPRS
SRC4C_LPRS
SRC6T/SATAT_LPRS
SRC6C/SATAC_LPRS
SRC7T_LPRS/27MHZ_SS
SRC7C_LPRS/27MHZ_NS
SB_SRC0T_LPRS
SB_SRC0C_LPRS
SB_SRC1T_LPRS
SB_SRC1C_LPRS
HTT0T_LPRS/66M
HTT0C_LPRS/66M
GNDSB_SRC
X1
X2
GEN_XTAL_IN
GEN_XTAL_OUT
SMBCLK
SMBDAT
ATIG0T_LPRS
ATIG0C_LPRS
ATIG1T_LPRS
ATIG1C_LPRS
CLKREQ0#
CLKREQ1#
CLKREQ2#
CLKREQ3#
CLKREQ4#
CPUKG0T_LPRS
CPUKG0C_LPRS
48MHZ_0
REF0/SEL_HTT66
REF1/SEL_SATA
REF2/SEL_27
GNDSATA
GNDATIG
GND
GNDHTT
GNDREF
GNDCPU
GND48
GNDSRC
GNDSRC
GND
ICS9LPRS480BKLFT-GP
71.09480.A03
2ND = 71.00880.A03
R591
DY
10MR2J-L-GP
SC12P50V2JN-L1-GP
C830
82.30005.A51
X7
X-14D31818M-50GP
C833
SC12P50V2JN-L1-GP
SMBC0_SB 12,16,17
SMBD0_SB 12,16,17
CLK_PCIE_PEG 52
CLK_PCIE_PEG# 52
CLK_NB_GFX 9
CLK_NB_GFX# 9
CLKREQ0#
LAN_CLKREQ#
TP168 TPAD14-GP
LAN_CLKREQ# 26
CLKREQ2#
TP166 TPAD14-GP
WLAN_CLKREQ#
WLAN_CLKREQ# 33
MIN2_CLKREQ#
MIN2_CLKREQ# 33
CPU_CLK 6
CPU_CLK# 6
CLK_48
R602
22R2J-2-GP
CLK48_USB 12
EC59
DY
SC22P50V2JN-4GP
REF0
REF1
REF2
3D3V_CLK_VDD
R303
0R0603-PAD
C826
SC1U10V2KX-1GP
VDD_REF
3D3V_48MPWR_S0
PD#
SB A-Link
11 CLK_PCIE_SB
11 CLK_PCIE_SB#
LAN
26 CLK_PCIE_LAN
26 CLK_PCIE_LAN#
NB A-Link
9 CLK_NB_GPPSB
9 CLK_NB_GPPSB#
MINI1
33 CLK_PCIE_MINI1
33 CLK_PCIE_MINI1#
MINI2
33 CLK_PCIE_MINI2
33 CLK_PCIE_MINI2#
53 OSC_SPREAD
R608
DY
22R2J-2-GP
0R0402-PAD
CLK_SRC0T_LPRS
53 CLK_27M_VGA
R607
CLK_SRC0C_LPRS
53 JTAG_TCK
R606
0R2J-2-GP
ATI_ES
1026 add R904
R615
1K2R2F-1-GP
DY
9 CLK_NBHT_CLK
9 CLK_NBHT_CLK#
R579
R577
0R0402-PAD
CLK_NBHT_CLK_1
CLK_NBHT_CLK#_1
NB HT
3D3V_S5
3D3V_S0
RN77
SRN10KJ-6-GP
PD#
LAN_CLKREQ#
WLAN_CLKREQ#
RUNPWROK_D
RUNPWROK_D 41
3D3V_S0
R572
MIN2_CLKREQ#
10KR2J-3-GP
1105 modify R229
REF1
R301
33R2F-3-GP
CLK_SB_14M 11,12
DY
R299
75R2F-2-GP
DY
REF0
R310
158R2F-GP
CLK_NB_14M 9
R309
90D9R2F-1-GP
3D3V_S0
DY
R308
10KR2J-3-GP
R302
10KR2J-3-GP
R587
10KR2J-3-GP
REF0
REF1
REF2
R307
10KR2J-3-GP
R306
10KR2J-3-GP
R582
10KR2J-3-GP
SEL_27 REF2
1* 27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
0 100MHz differential spreading SRC clock
SEL_SATA REF1
1 100MHz non-spreading differential SATA clock
0* 100MHz differential spreading SRC clock
SEL_HTT66 REF0
1 66MHz 3.3V single ended HTT clock
0* 100MHz differential HTT clock
CPU_CLK(200MHz)
OSC_14M_NB
RS880M 1.1V 158R/90.9R
CLK_PCIE_PEG
DY EC62 SC22P50V2JN-4GP
CLK_PCIE_PEG#
DY EC63 SC22P50V2JN-4GP
CLK_NB_GFX
DY EC65 SC22P50V2JN-4GP
CLK_NB_GFX#
DY EC64 SC22P50V2JN-4GP
CLK_PCIE_SB
DY EC69 SC22P50V2JN-4GP
CLK_PCIE_SB#
DY EC68 SC22P50V2JN-4GP
CLK_PCIE_LAN
DY EC67 SC22P50V2JN-4GP
CLK_PCIE_LAN#
DY EC66 SC22P50V2JN-4GP
CLK_NB_GPPSB
DY EC71 SC22P50V2JN-4GP
CLK_NB_GPPSB#
DY EC70 SC22P50V2JN-4GP
CLK_PCIE_MINI1
DY EC73 SC22P50V2JN-4GP
CLK_PCIE_MINI1#
DY EC72 SC22P50V2JN-4GP
CLK_PCIE_MINI2
DY EC76 SC22P50V2JN-4GP
CLK_PCIE_MINI2#
DY EC77 SC22P50V2JN-4GP
CPU_CLK
DY EC75 SC22P50V2JN-4GP
CPU_CLK#
DY EC74 SC22P50V2JN-4GP
CLK_NBHT_CLK
DY EC79 SC22P50V2JN-4GP
CLK_NBHT_CLK#
DY EC78 SC22P50V2JN-4GP
CLK_27M_VGA
DY EC80 SC22P50V2JN-4GP
SB_1224 EMI
NB CLOCK INPUT TABLE
NB CLOCKS | RS880
HT_REFCLKP | 100M DIFF
HT_REFCLKN | 100M DIFF
REFCLK_P | 14M SE (1.1V)
REFCLK_N | vref
GFX_REFCLK | 100M DIFF(IN/OUT)*
GPP_REFCLK | NC
GPPSB_REFCLK | 100M DIFF
JE70-DN
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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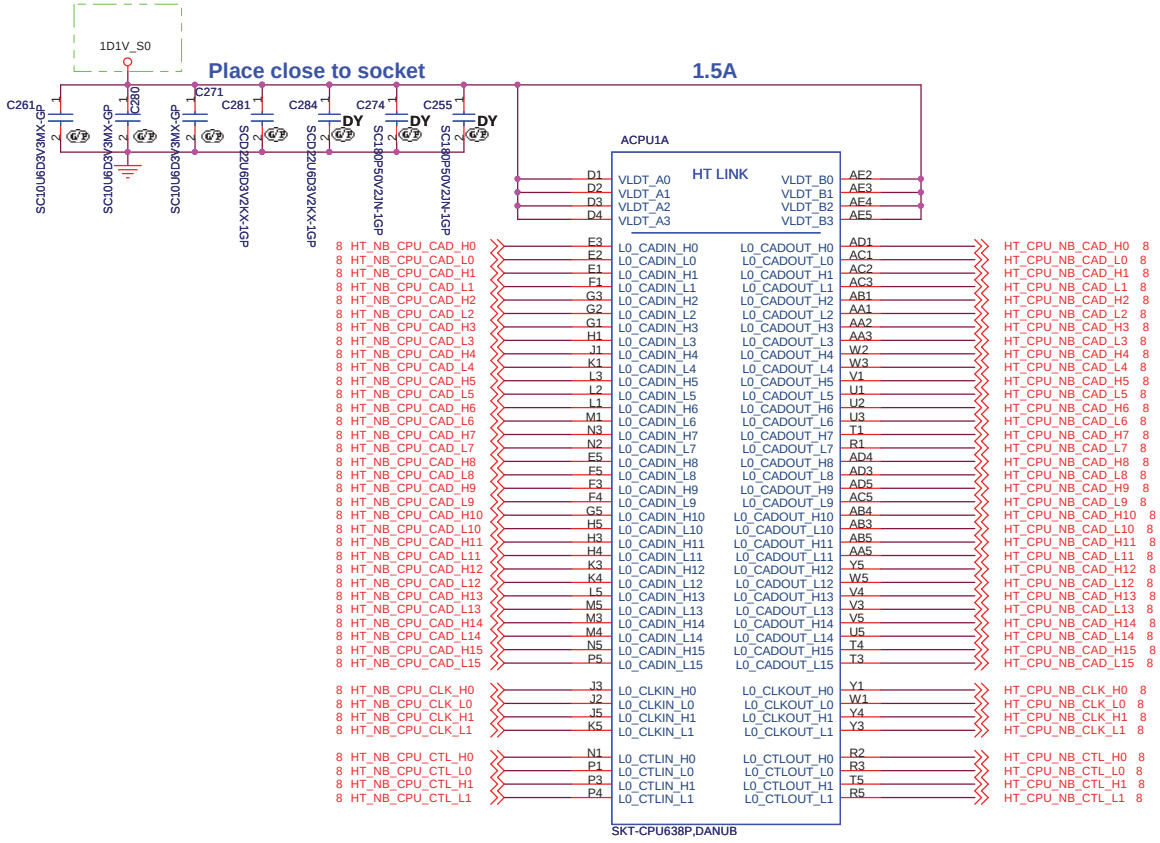
Title
CLKGEN ICS9LPRS480
Size A3
Document Number JE70-DN
Rev SB
Date: Monday, March 01, 2010
Sheet 3 of 63
http://hobi-elektronika.net



62.10055.111

SKT-BGA638H176

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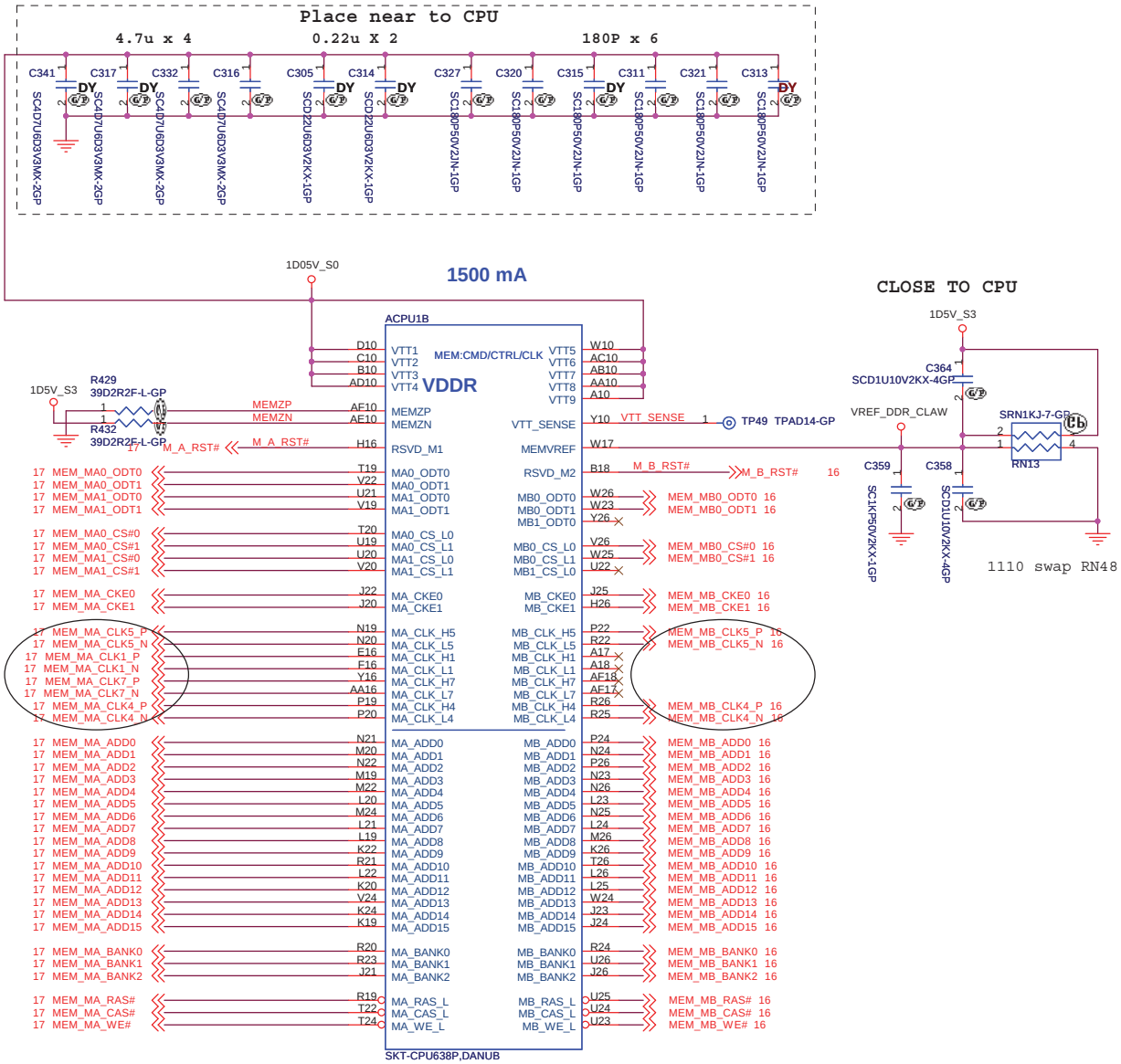
Title: **CPU HT LINK I/F (1/4)**

Size	Document Number	Rev
A3	JE70-DN	SB

Date: Monday, March 01, 2010 Sheet 4 of 63



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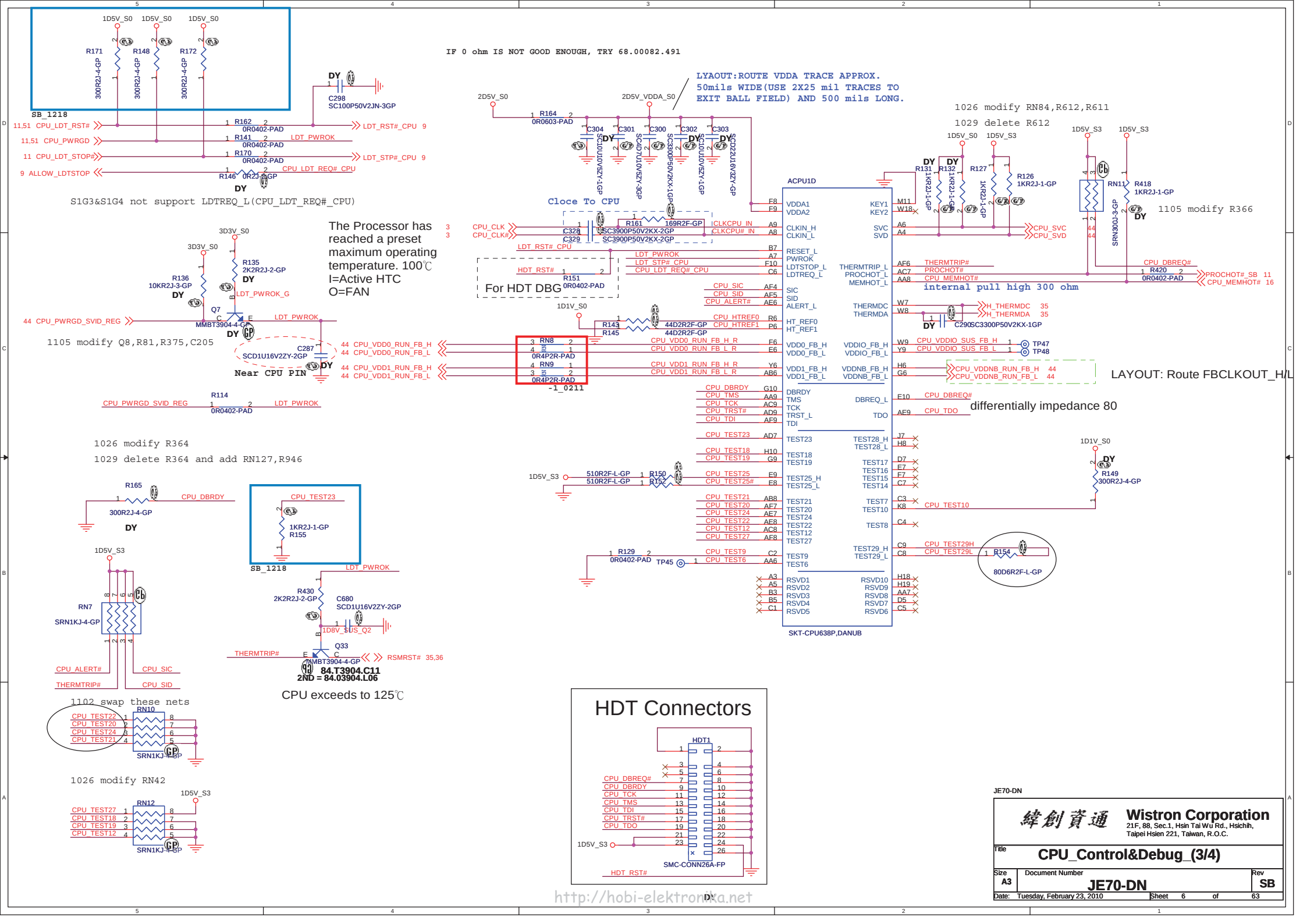
Title: **CPU_DDR_(2/4)**

Size	Document Number	Rev
A3	JE70-DN	SB

Date: Monday, March 01, 2010 Sheet 5 of 63


IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491
LYAOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.
1026 modify RN84,R612,R611
1029 delete R612
1105 modify R366
SB_1218
S1G3&S1G4 not support LDTREQ_L(CPU_LDT_REQ#_CPU)
The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN
Cloce To CPU
For HDT DBG
internal pull high 300 ohm
1105 modify Q8,R81,R375,C205
Near CPU PIN
differentially impedance 80
LAYOUT: Route FBCLKOUT_H/L
1026 modify R364
1029 delete R364 and add RN127,R946
1102 swap these nets
1026 modify RN42
CPU exceeds to 125℃
84.T3904.C11
2ND = 84.03904.L06
ACPU1D
SKT-CPU638P,DANUB
HDT Connectors
SMC-CONN26A-FP
http://hobi-elektronika.net
JE70-DN
Wistron Corporation
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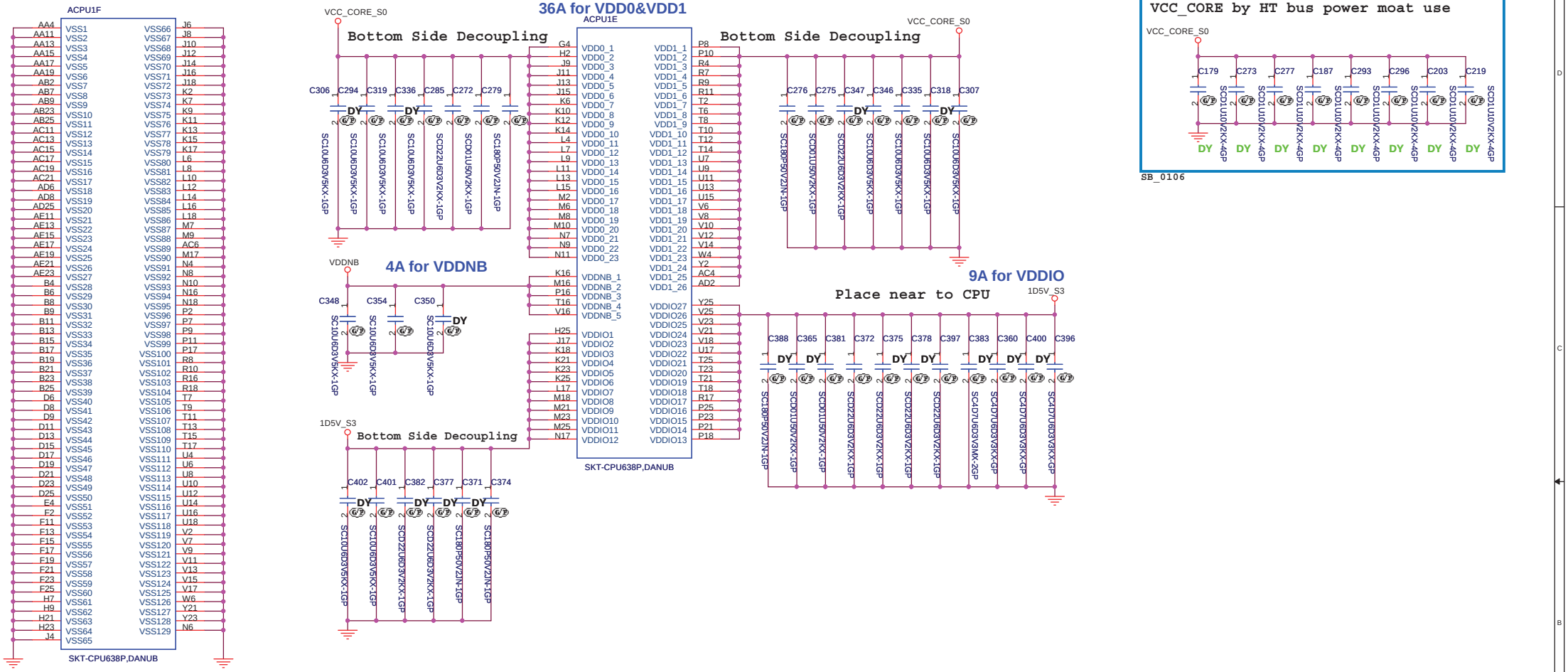
CPU_Control&Debug_(3/4)
Size A3
Document Number JE70-DN
Rev SB
Date: Tuesday, February 23, 2010
Sheet 6 of 63



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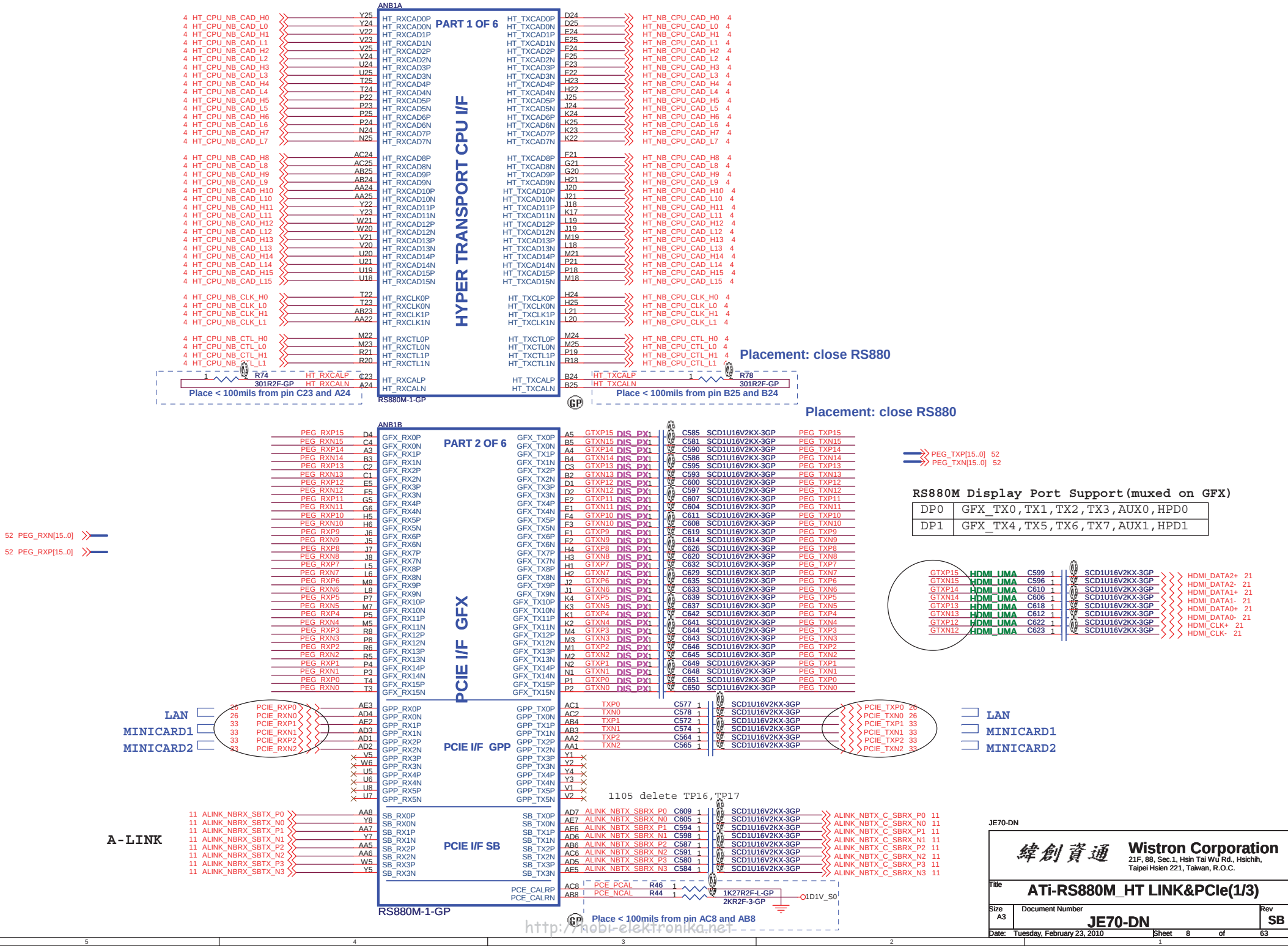
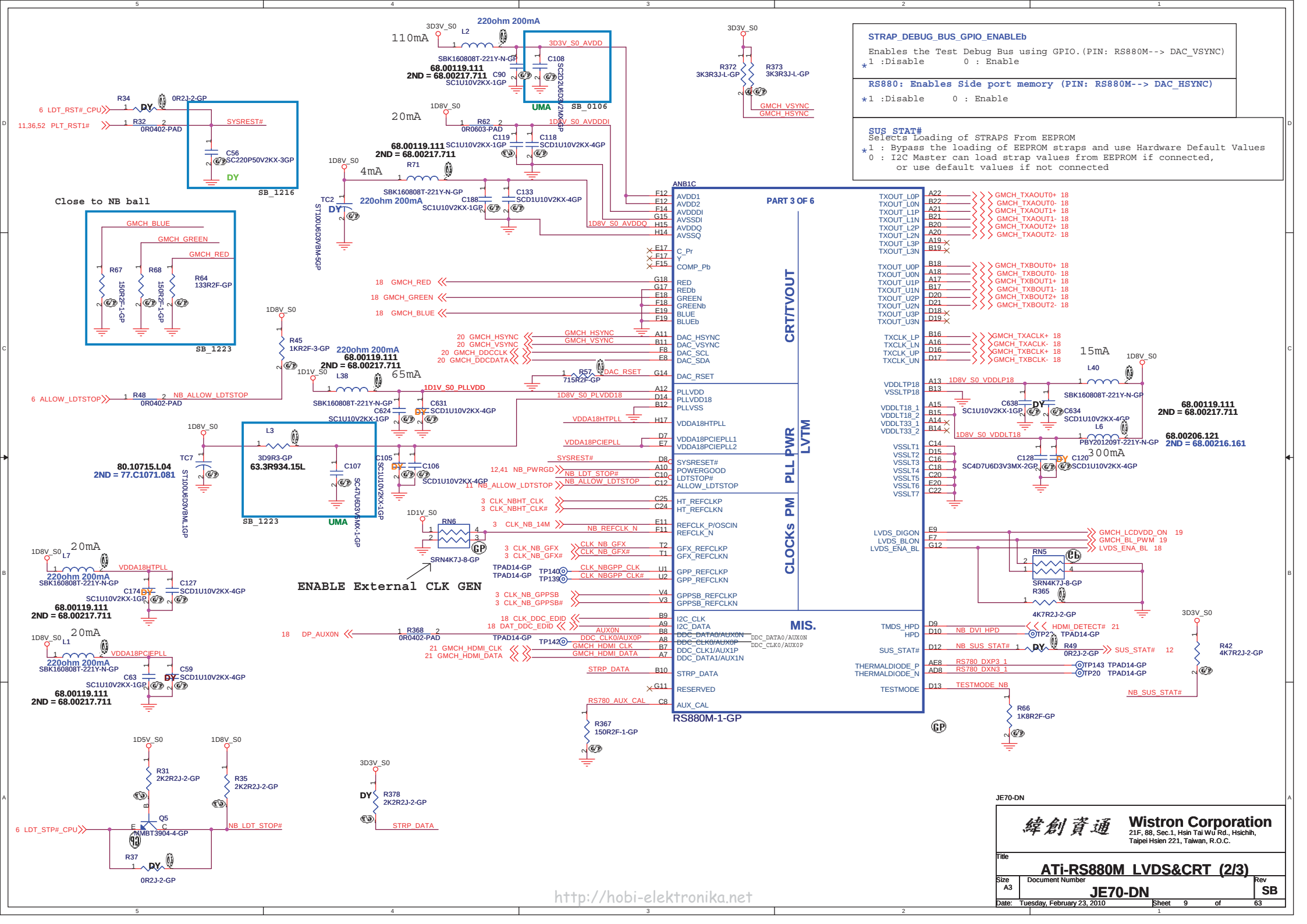
Title	CPU_Power_(4/4)	
Size A3	Document Number JE70-DN	Rev SB
Date: Wednesday, January 06, 2010	Sheet 7 of 63	




STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS880M--> DAC_VSYNC)
*1 :Disable 0 : Enable
RS880: Enables Side port memory (PIN: RS880M--> DAC_HSYNC)
*1 :Disable 0 : Enable
SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected
ANB1C
PART 3 OF 6
CRT/TVOUT
PLL PWR
LVTM
CLOCKs PM
MIS.
RS880M-1-GP
Close to NB ball
ENABLE External CLK GEN
220ohm 200mA
SB_1216
SB_1223
SB_0106
UMA
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
ATi-RS880M LVDS&CRT (2/3)
JE70-DN
Rev SB
Tuesday, February 23, 2010
Sheet 9 of 63
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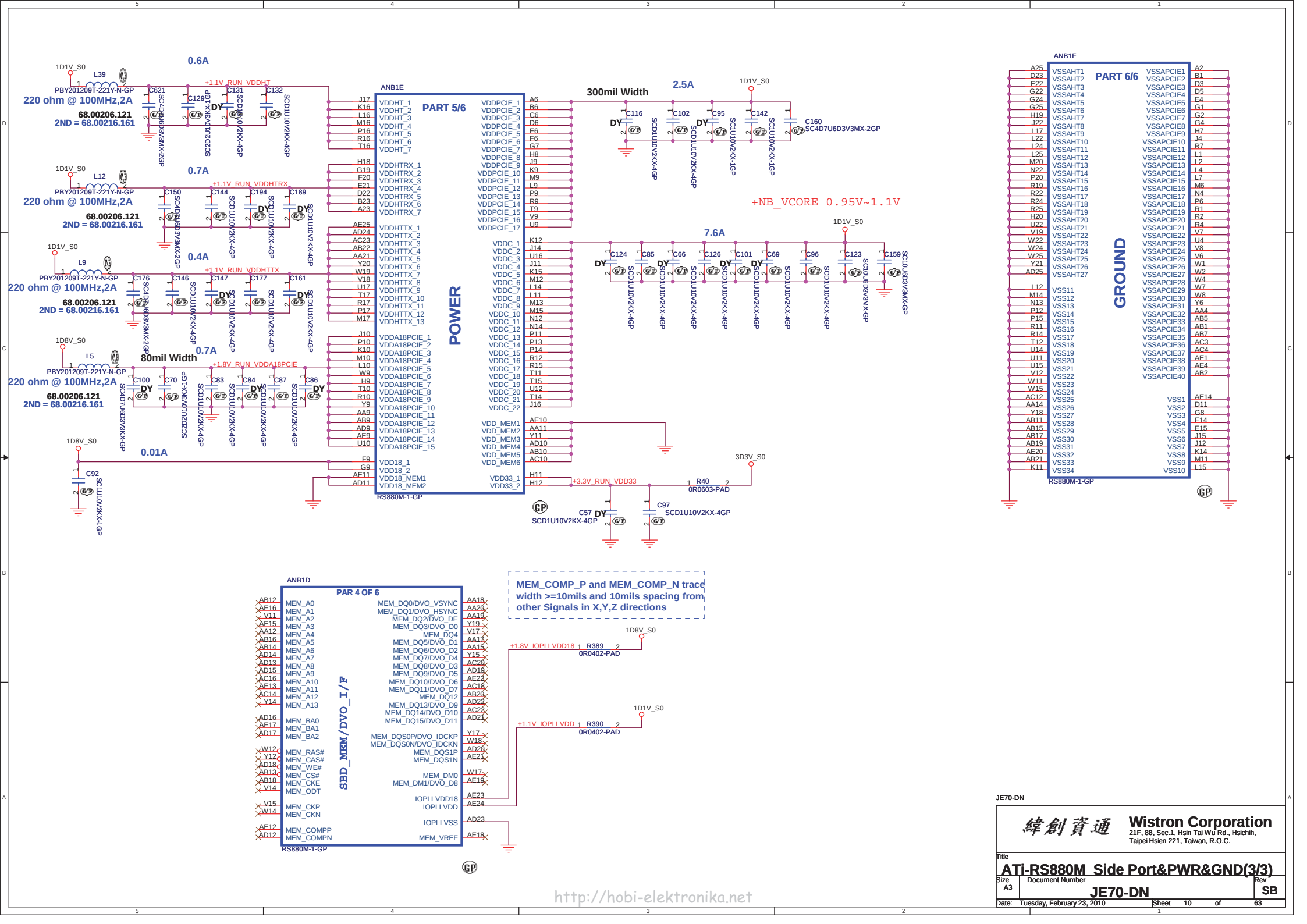

JE70-DN

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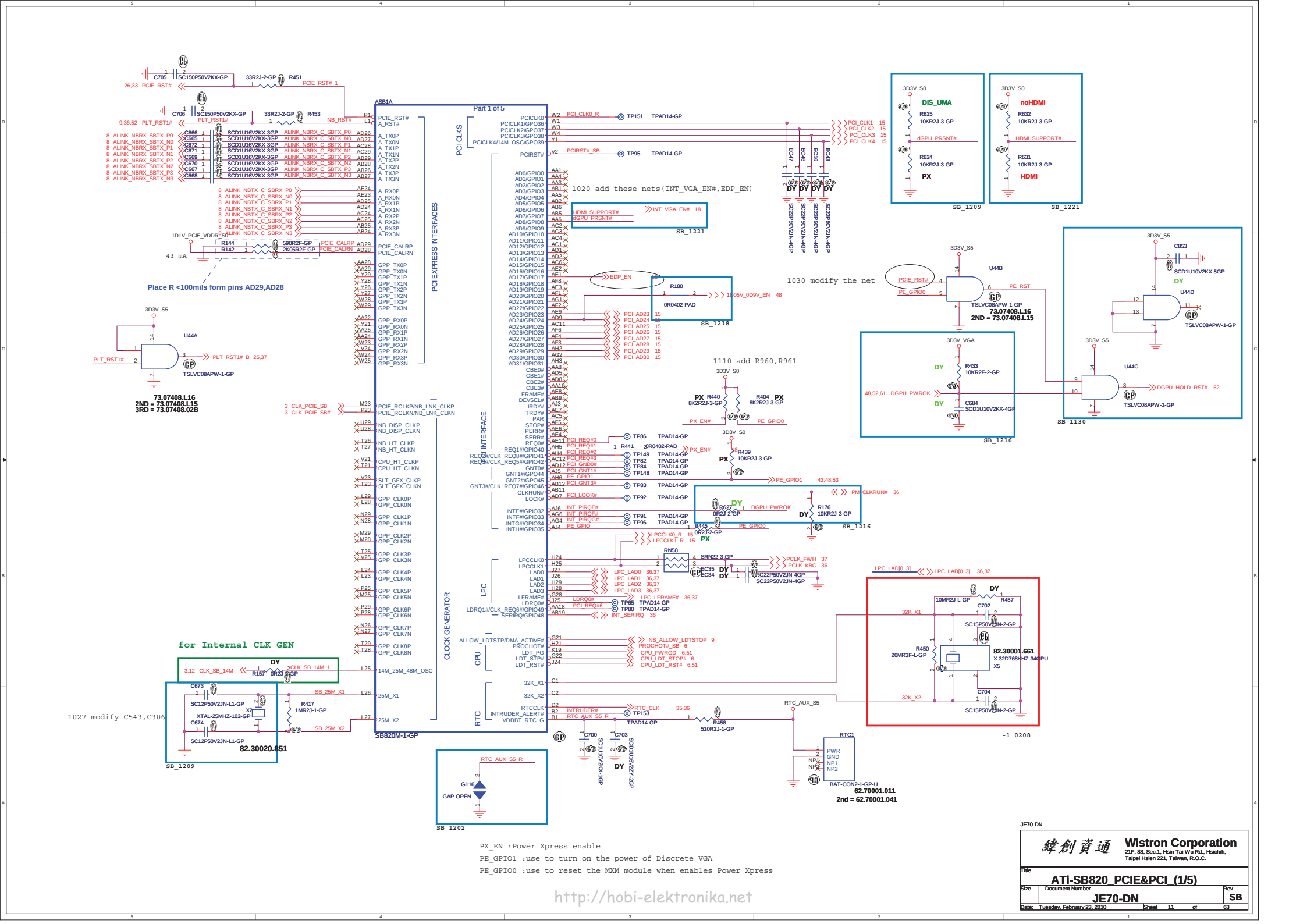
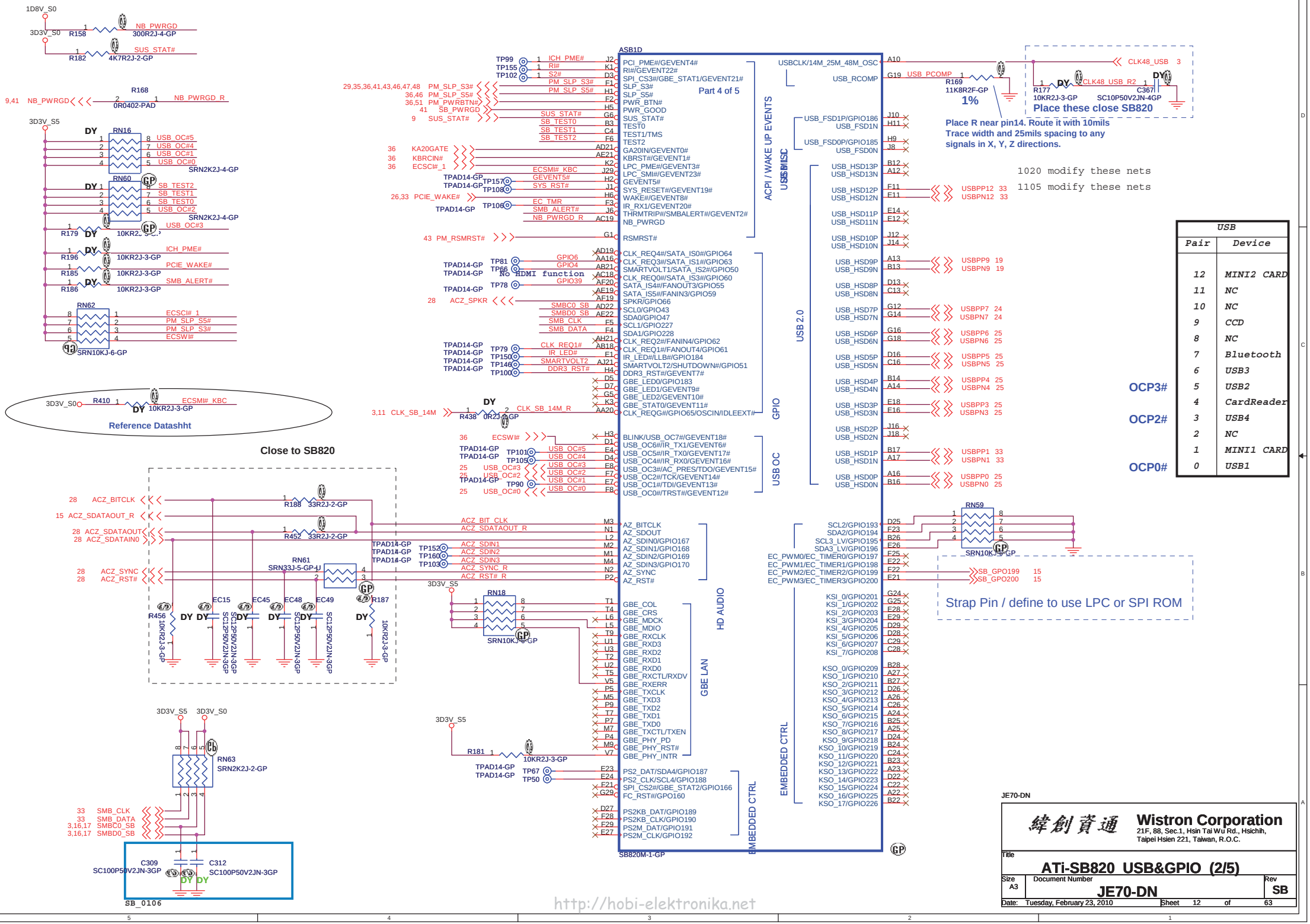
Taipei Hsien 221, Taiwan, R.O.C.

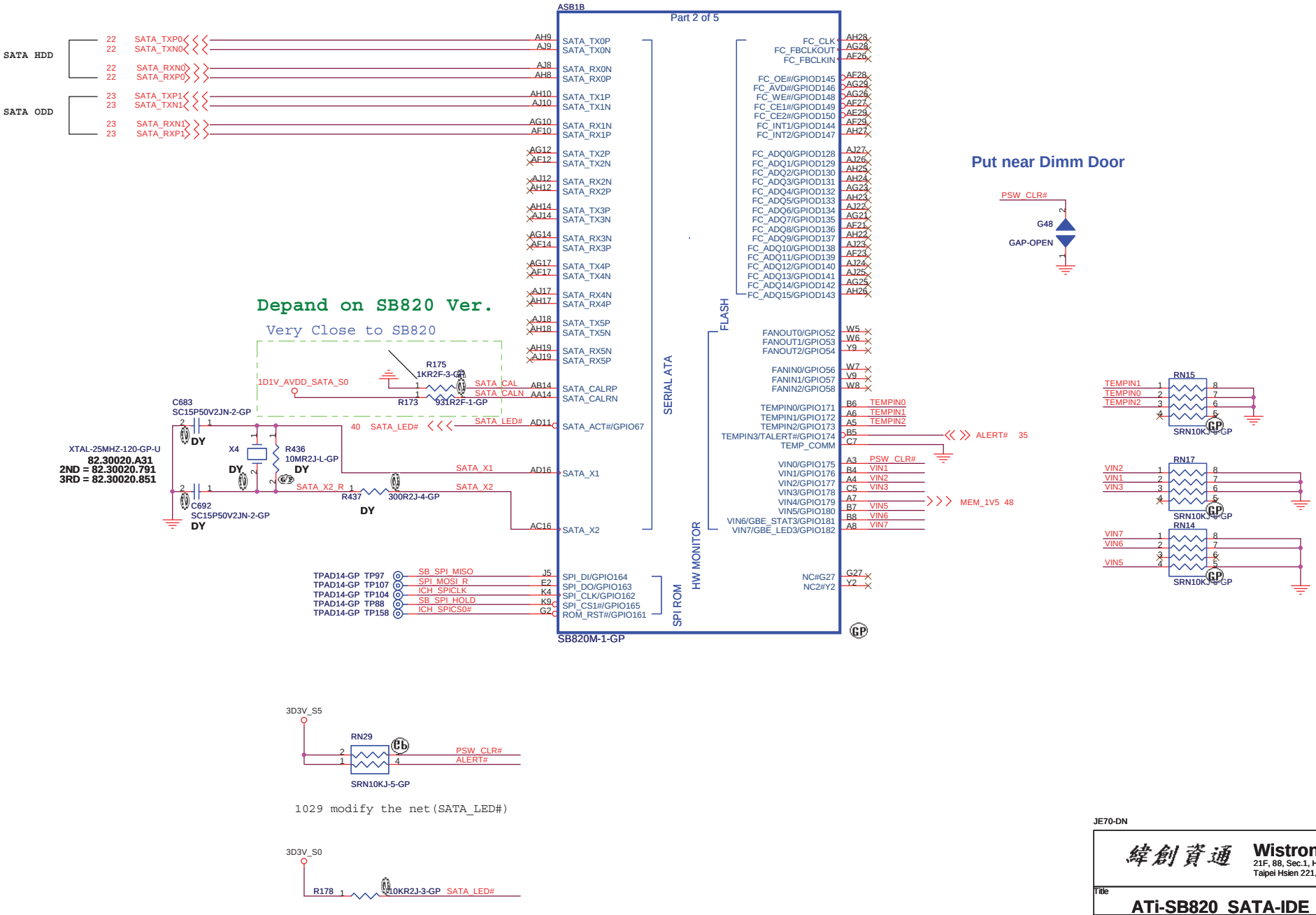
Title: ATi-RS880M_Side Port&PWR&GND(3/3)

Size	Document Number	Rev
A3	JE70-DN	SB

Date: Tuesday, February 23, 2010 Sheet 10 of 63


ASB1A
Part 1 of 5
SB820M-1-GP
PCI EXPRESS INTERFACES
PCI CLKS
PCI INTERFACE
CLOCK GENERATOR
LPC
CPU
RTC
1020 add these nets(INT_VGA_EN#,EDP_EN)
SB_1221
SB_1218
1030 modify the net
1110 add R960,R961
SB_1216
SB_1130
SB_1209
SB_1202
Place R <100mils form pins AD29,AD28
for Internal CLK GEN
1027 modify C543,C306
82.30020.851
82.30001.661
73.07408.L16
2ND = 73.07408.L15
3RD = 73.07408.02B
62.70001.011
2nd = 62.70001.041
PX_EN :Power Xpress enable
PE_GPIO1 :use to turn on the power of Discrete VGA
PE_GPIO0 :use to reset the MXM module when enables Power Xpress
http://hobi-elektronika.net
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
JE70-DN
ATi-SB820_PCIE&PCI_(1/5)
Size
Document Number
JE70-DN
Rev
SB
Date: Tuesday, February 23, 2010
Sheet 11 of 63


ASB1D
Part 4 of 5
SB820M-1-GP
ACPI / WAKE UP EVENTS
USB MISC
USB 2.0
GPIO
USB OC
HD AUDIO
GBE LAN
EMBEDDED CTRL
Close to SB820
Reference Datashht
Strap Pin / define to use LPC or SPI ROM
Place these close SB820
Place R near pin14. Route it with 10mils
Trace width and 25mils spacing to any
signals in X, Y, Z directions.
1020 modify these nets
1105 modify these nets
OCP3#
OCP2#
OCP0#
USB
Pair | Device
12 | MINI2 CARD
11 | NC
10 | NC
9 | CCD
8 | NC
7 | Bluetooth
6 | USB3
5 | USB2
4 | CardReader
3 | USB4
2 | NC
1 | MINI1 CARD
0 | USB1
JE70-DN
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB820 USB&GPIO (2/5)
Size A3
Document Number JE70-DN
Rev SB
Date: Tuesday, February 23, 2010
Sheet 12 of 63
http://hobi-elektronika.net



JE70-DN

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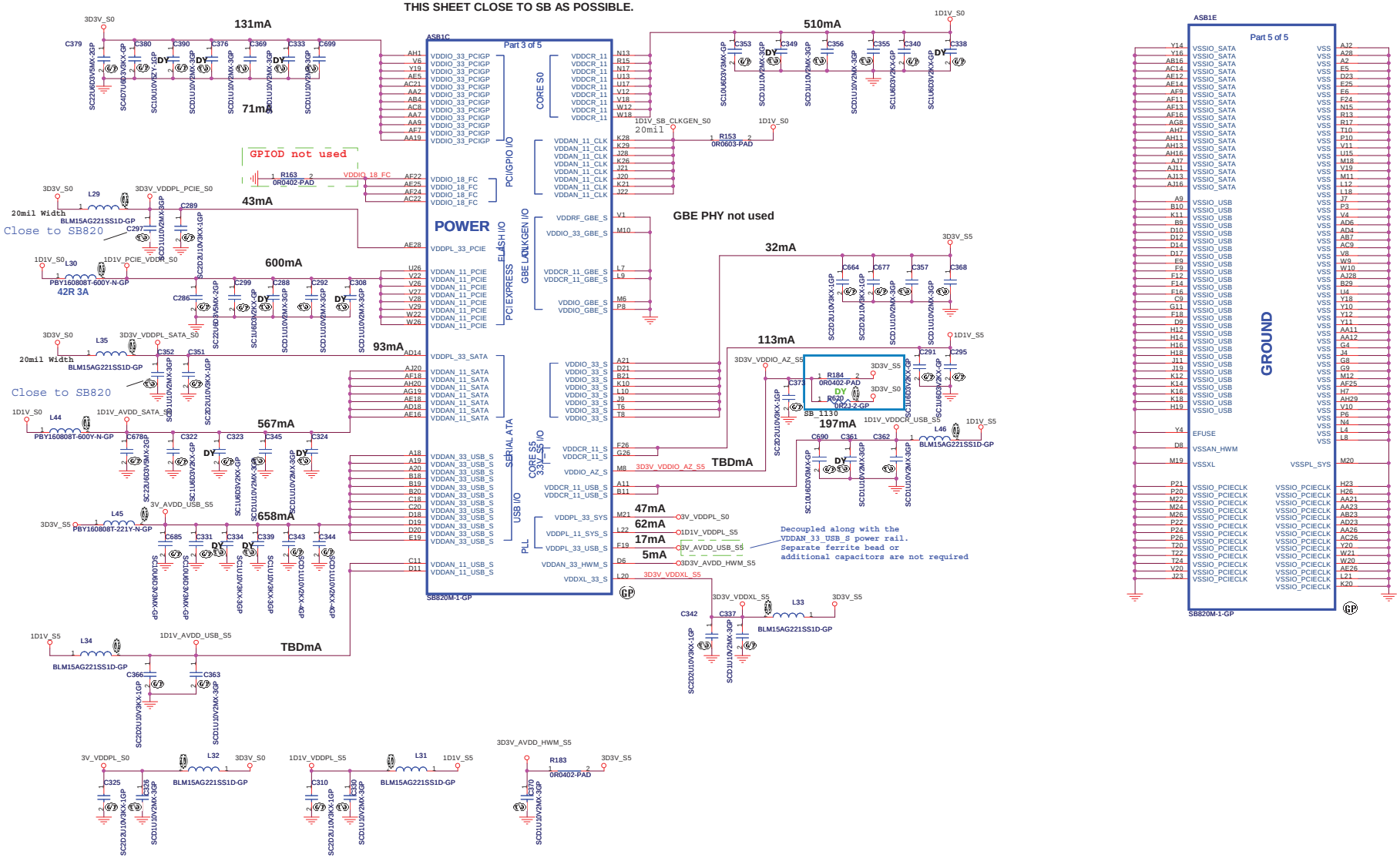
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB820 SATA-IDE (3/5)

Size: A3 | Document Number: JE70-DN | Rev: SB

Date: Tuesday, February 23, 2010 | Sheet 13 of 63

PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.



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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

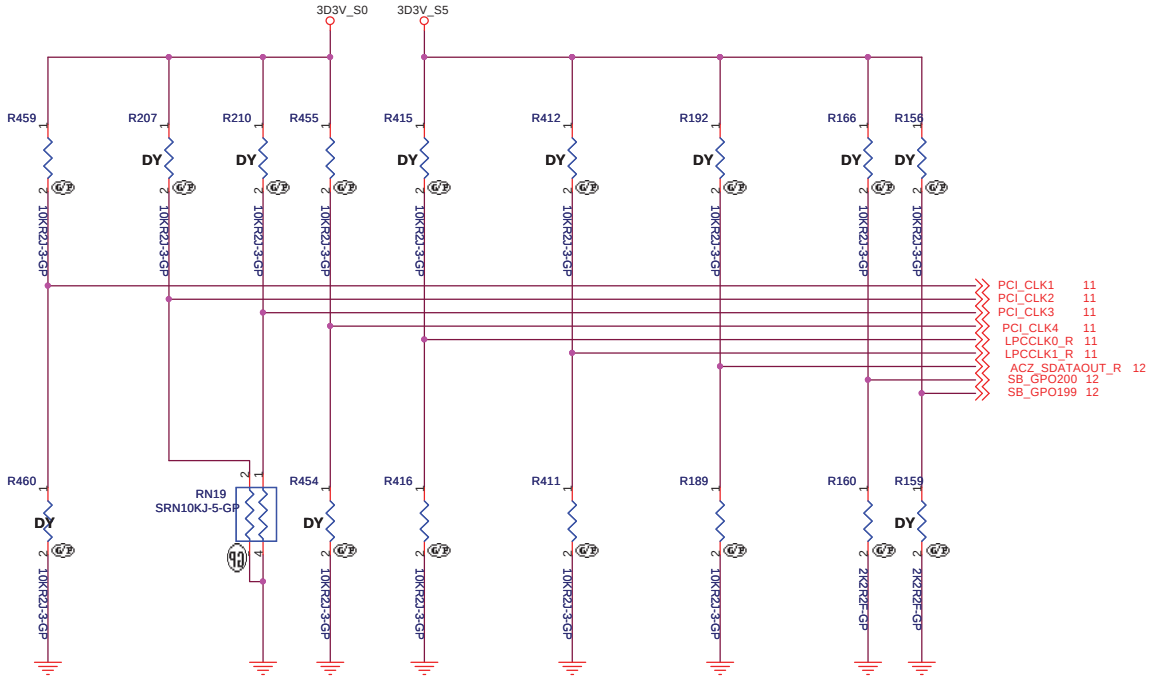
Title: ATi-SB820_POWER&GND_(4/5)

Size	Document Number	Rev
Custom	JE70-DN	SB

Date: Friday, February 12, 2010 Sheet 14 of 63

REQUIRED STRAPS

REQUIRED SYSTEM STRAPS

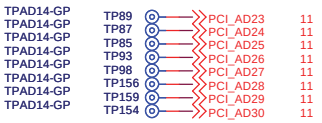


1118 modify R412,R411

	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	AZ_SDOUT	GPIO200 GPIO199
PULL HIGH	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED	LOW POWER MODE	H,H = Reserved H,L = SPI ROM
PULL LOW	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	PERFORMANCE MODE DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM

NOTE: SB820 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Note: SB820 has 15K internal PU FOR PCI_AD[27:23]

JE70-DN

緯創資通 Wistron Corporation
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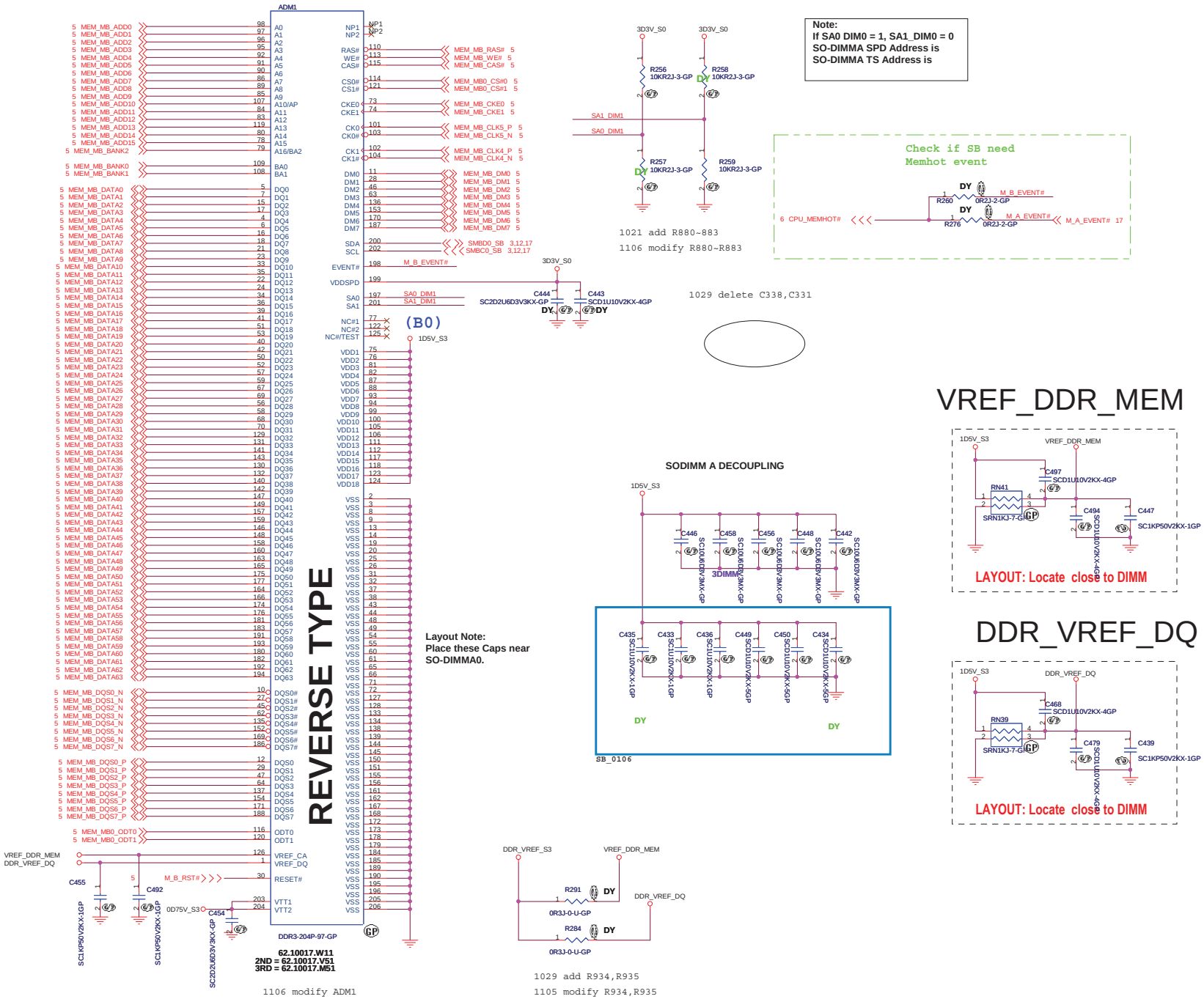
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB820 STRAPPING (5/5)

Size	Document Number	Rev
A3	JE70-DN	SB

Date: Tuesday, February 23, 2010 Sheet 15 of 63



VREF_DDR_MEM

DDR_VREF_DQ

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRIII_SO-DIMM SKT_1

Size	Document Number	Rev
Custom	JE70-DN	SB

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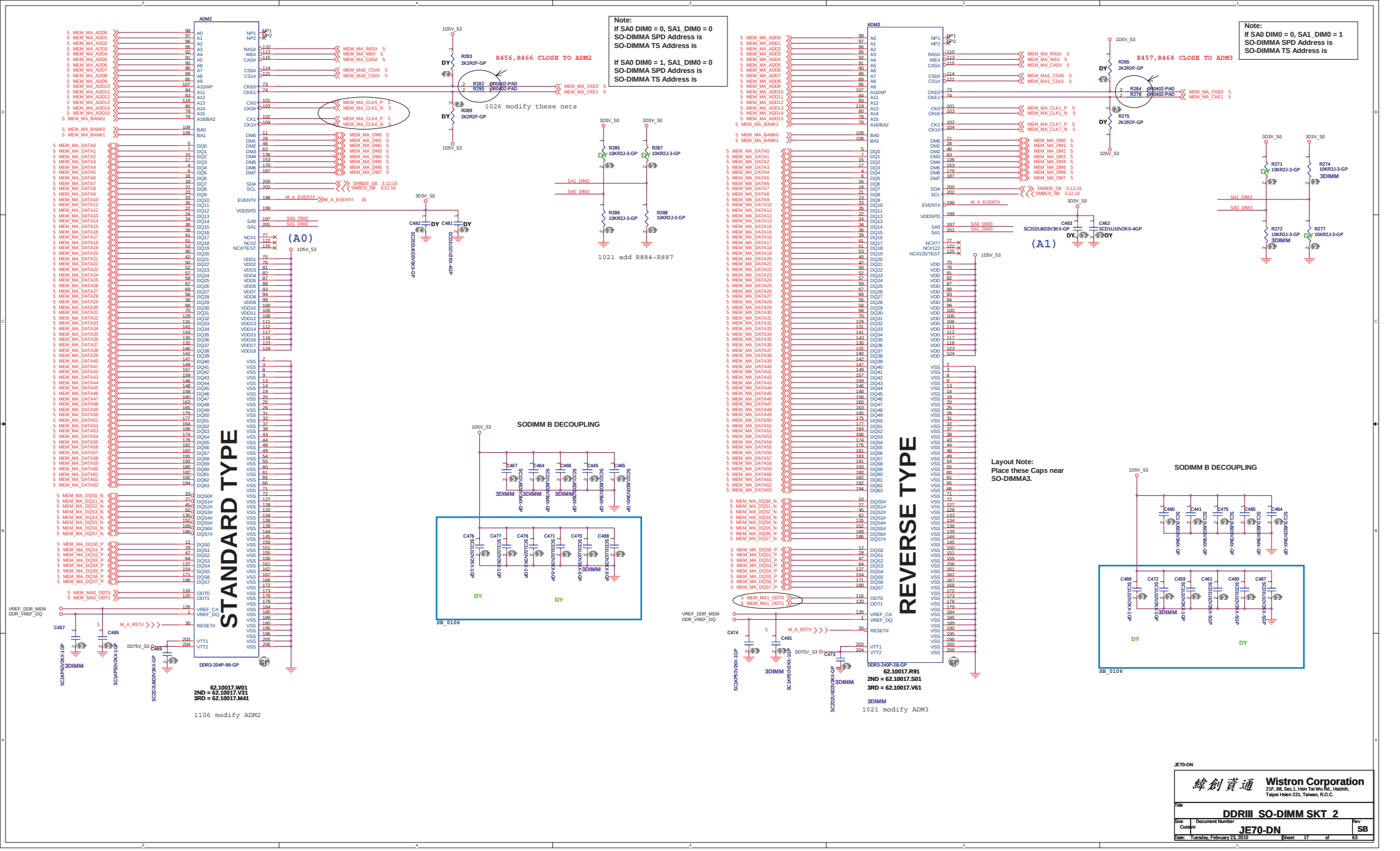

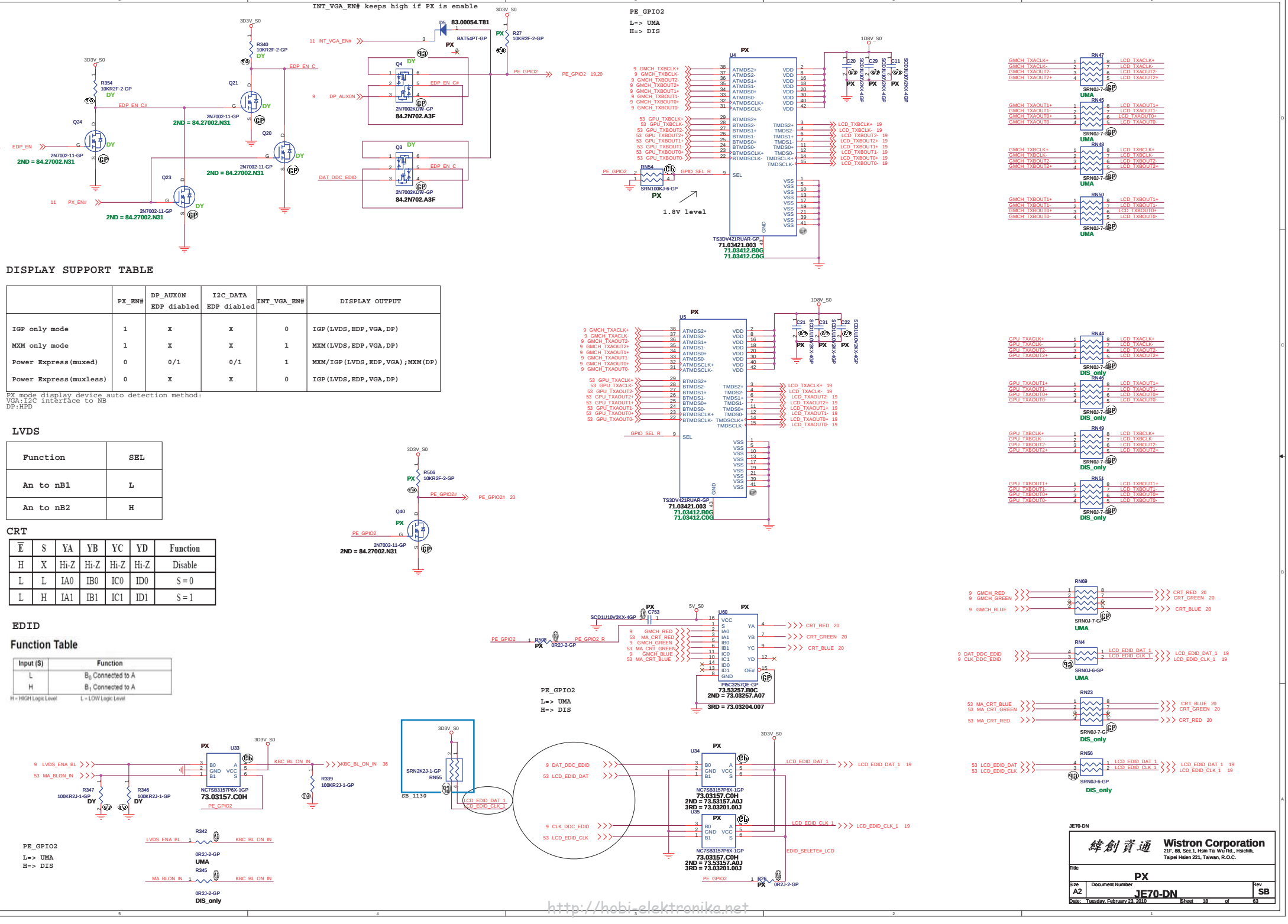

DISPLAY SUPPORT TABLE

	PX_EN#	DP_AUX0N EDP diabled	I2C_DATA EDP diabled	INT_VGA_EN#	DISPLAY OUTPUT
IGP only mode	1	X	X	0	IGP(LVDS,EDP,VGA,DP)
MXM only mode	1	X	X	1	MXM(LVDS,EDP,VGA,DP)
Power Express(muxed)	0	0/1	0/1	1	MXM/IGP(LVDS,EDP,VGA);MXM(DP)
Power Express(muxless)	0	X	X	0	IGP(LVDS,EDP,VGA,DP)

PX mode display device auto detection method:
VGA:I2C interface to NB
DP:HPD

LVDS

Function	SEL
An to nB1	L
An to nB2	H

CRT

$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

EDID

Function Table

Input (S)	Function
L	B_0 Connected to A
H	B_1 Connected to A

H = HIGH Logic Level L = LOW Logic Level

JE70-DN	
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Title	PX
Size: A2	Document Number: JE70-DN
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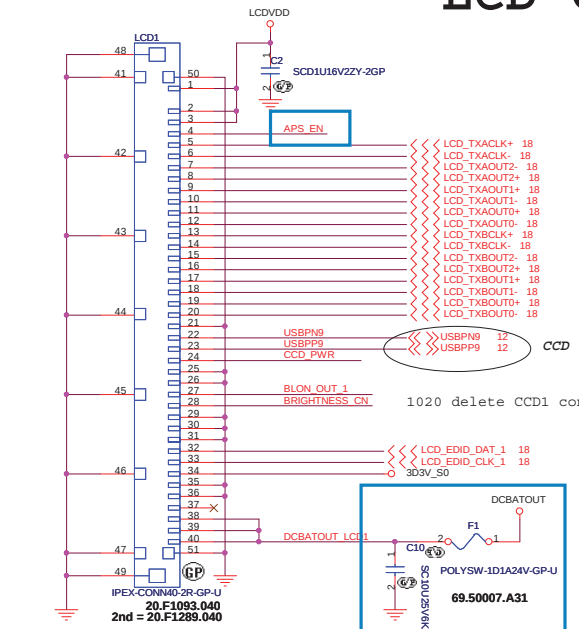
LCD CONN

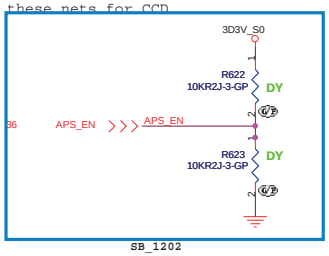
Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

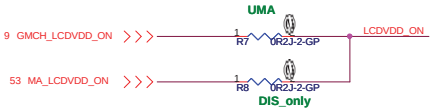
CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

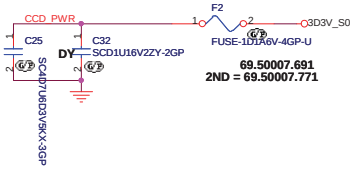


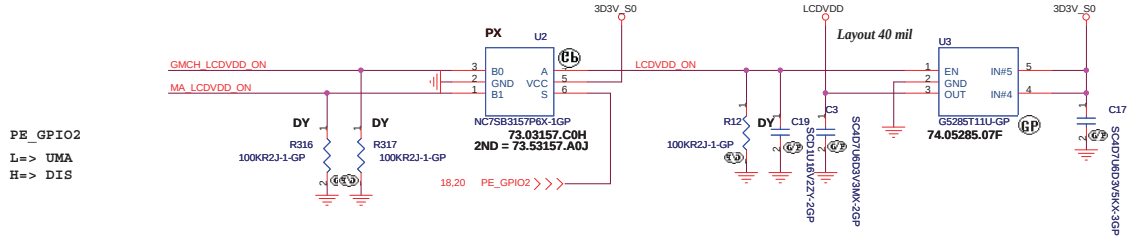
1029 add EC99,EC100

1020 delete CCD1 conn and modify these nets for CCD

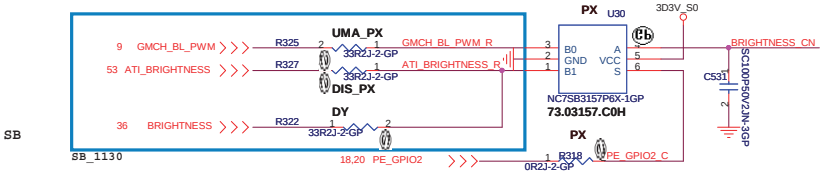


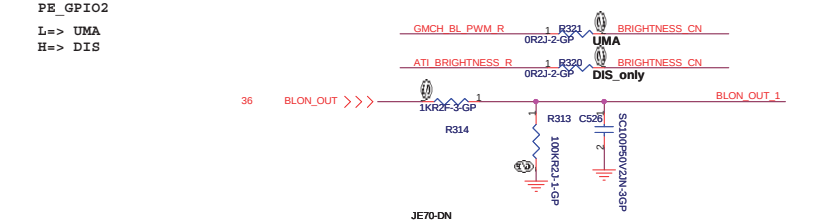






Reserve direct connector to KBC





JE70-DN

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Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN

Size	Document Number	Rev
Custom	JE70-DN	SB

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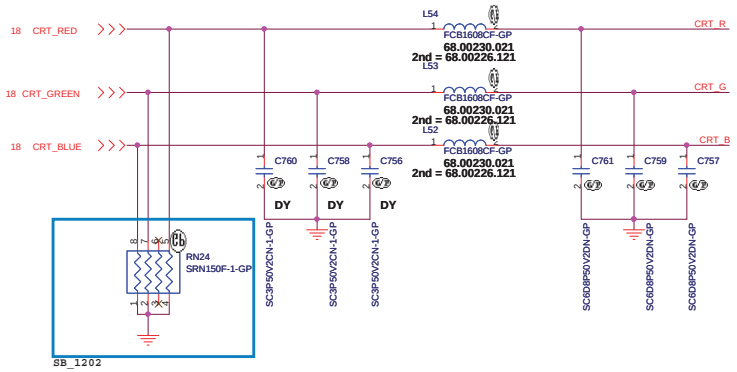
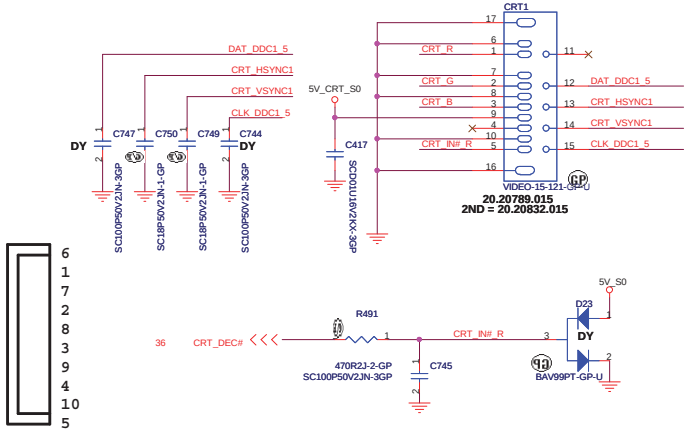
Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 10 ohm@100MHz



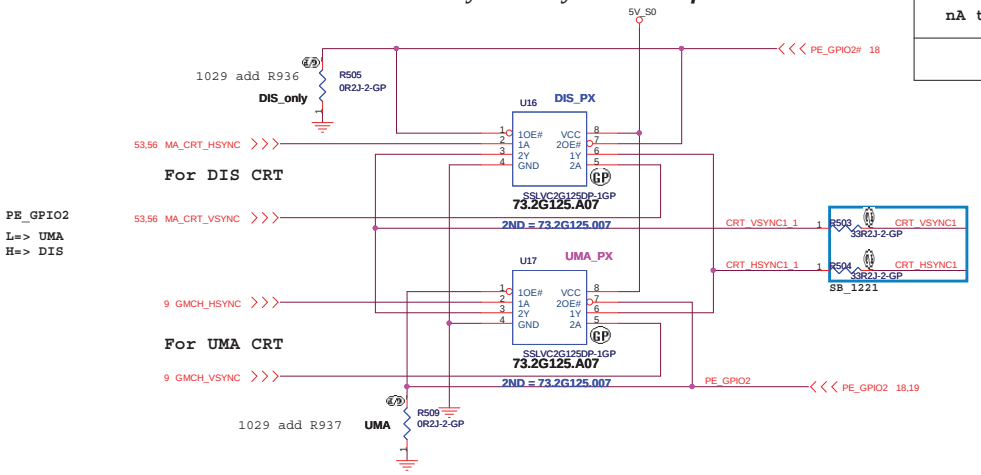
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT I/F & CONNECTOR

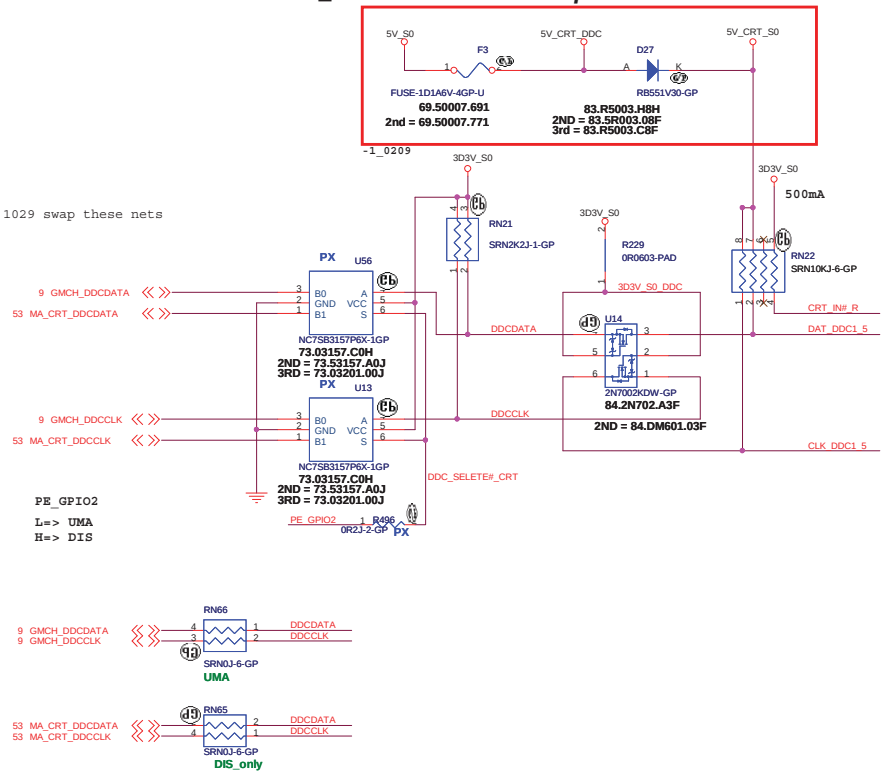


Function	OE#
nA to nY	L
X	H

Hsync & Vsync level shift



DDC_CLK & DATA level shift



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Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

Size	Document Number	Rev
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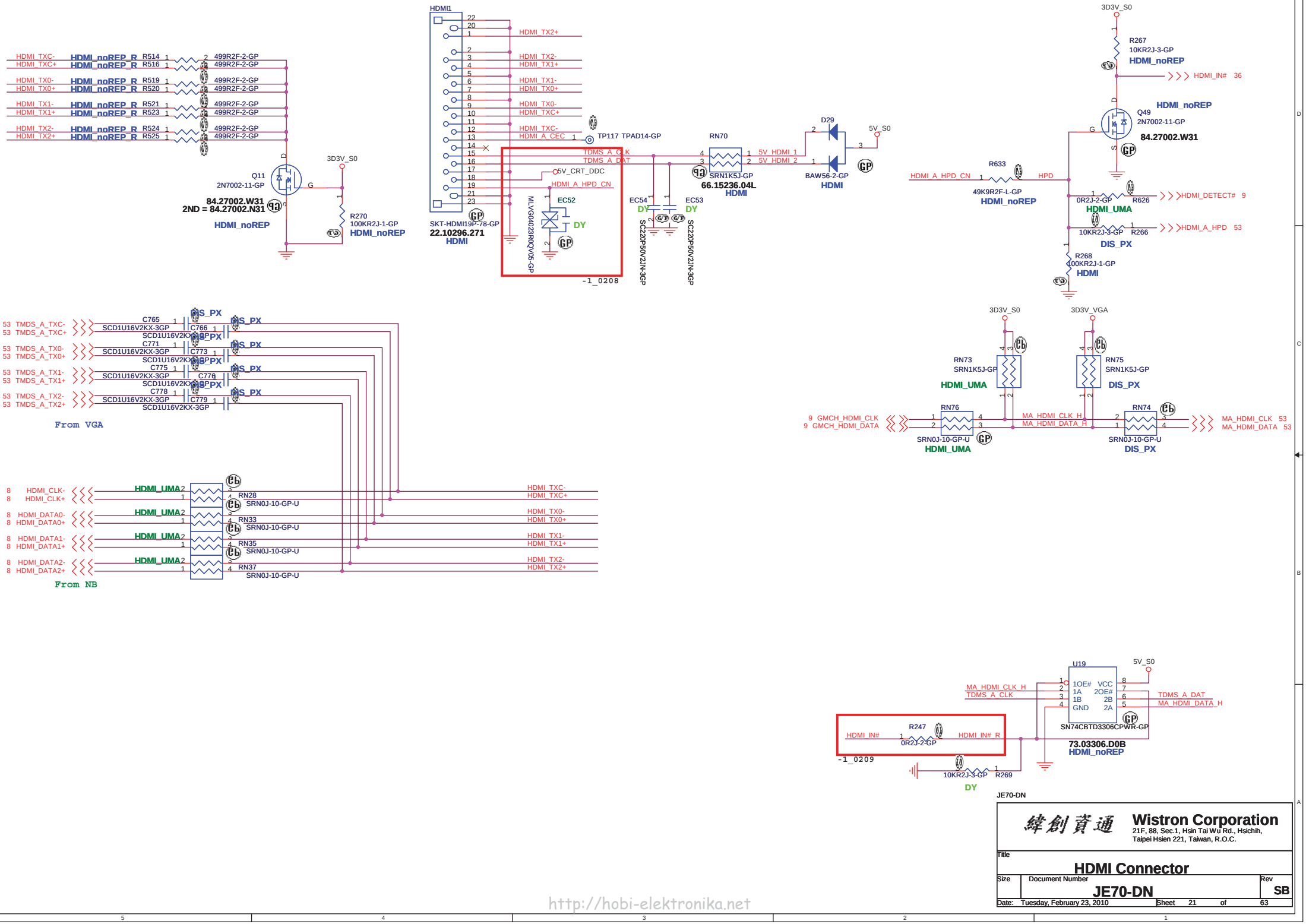

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDMI Connector**

Size	Document Number	Rev
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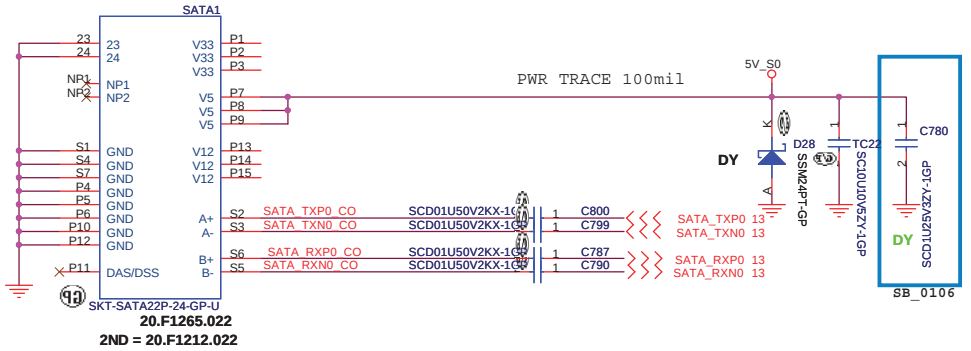
SATA Connector



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Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDD**

Size | Document Number: **JE70-DN** | Rev: **SB**

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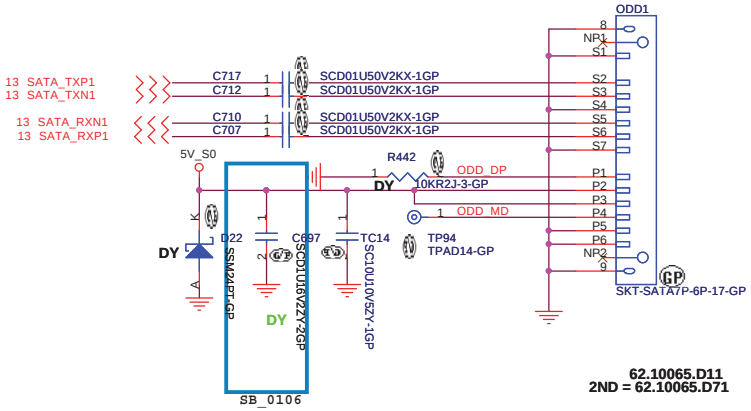
ODD Connector



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Title		
ODD		
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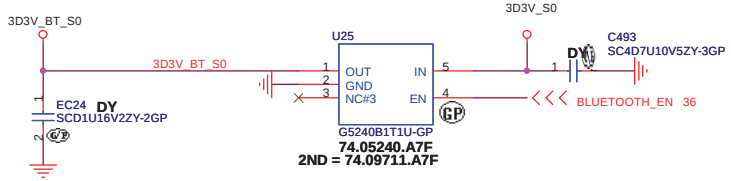
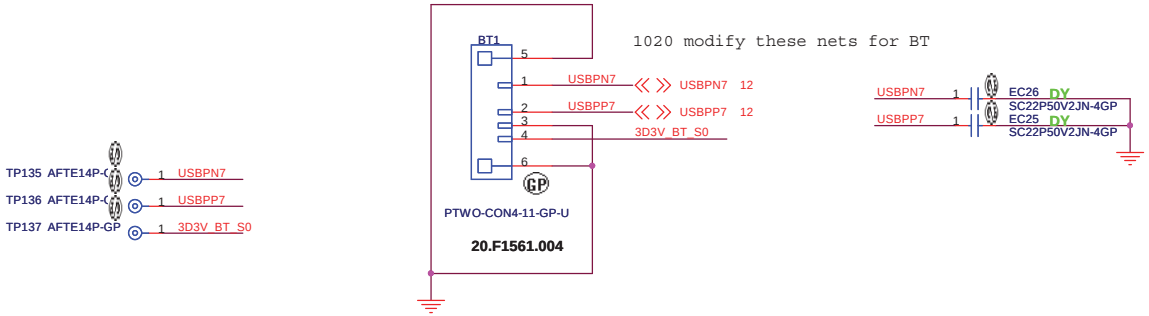
BLUETOOTH MODULE

1.5A / High Active Voltage 2V





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Title	**BLUETOOTH**
Size / Document Number	**JE70-DN** / Rev **SB**
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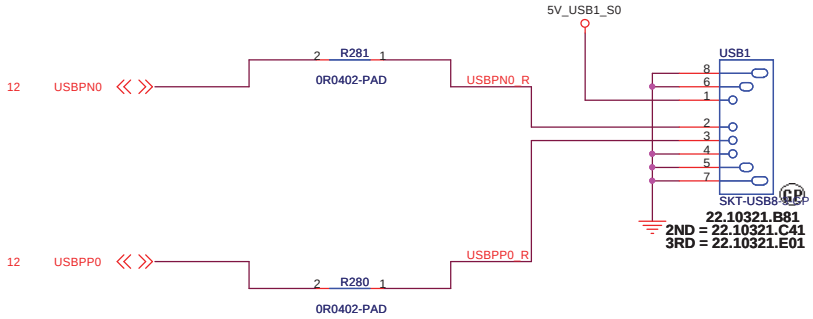

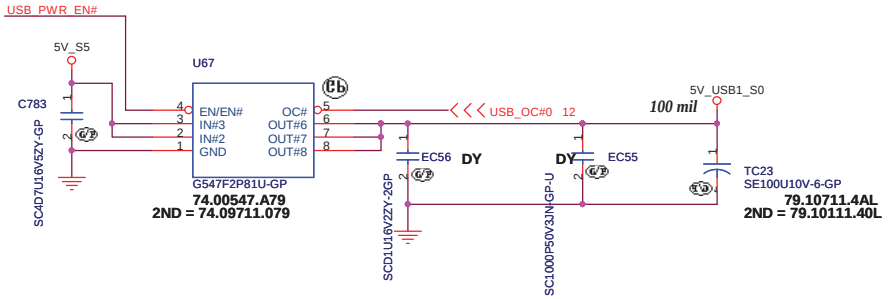

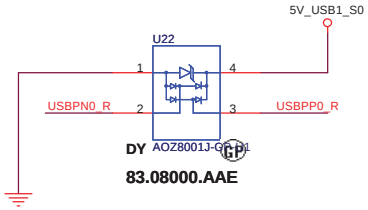

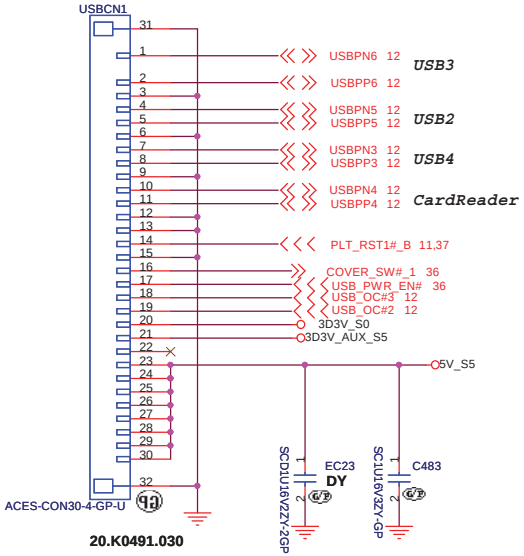

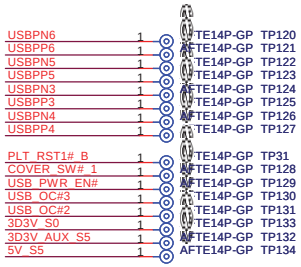

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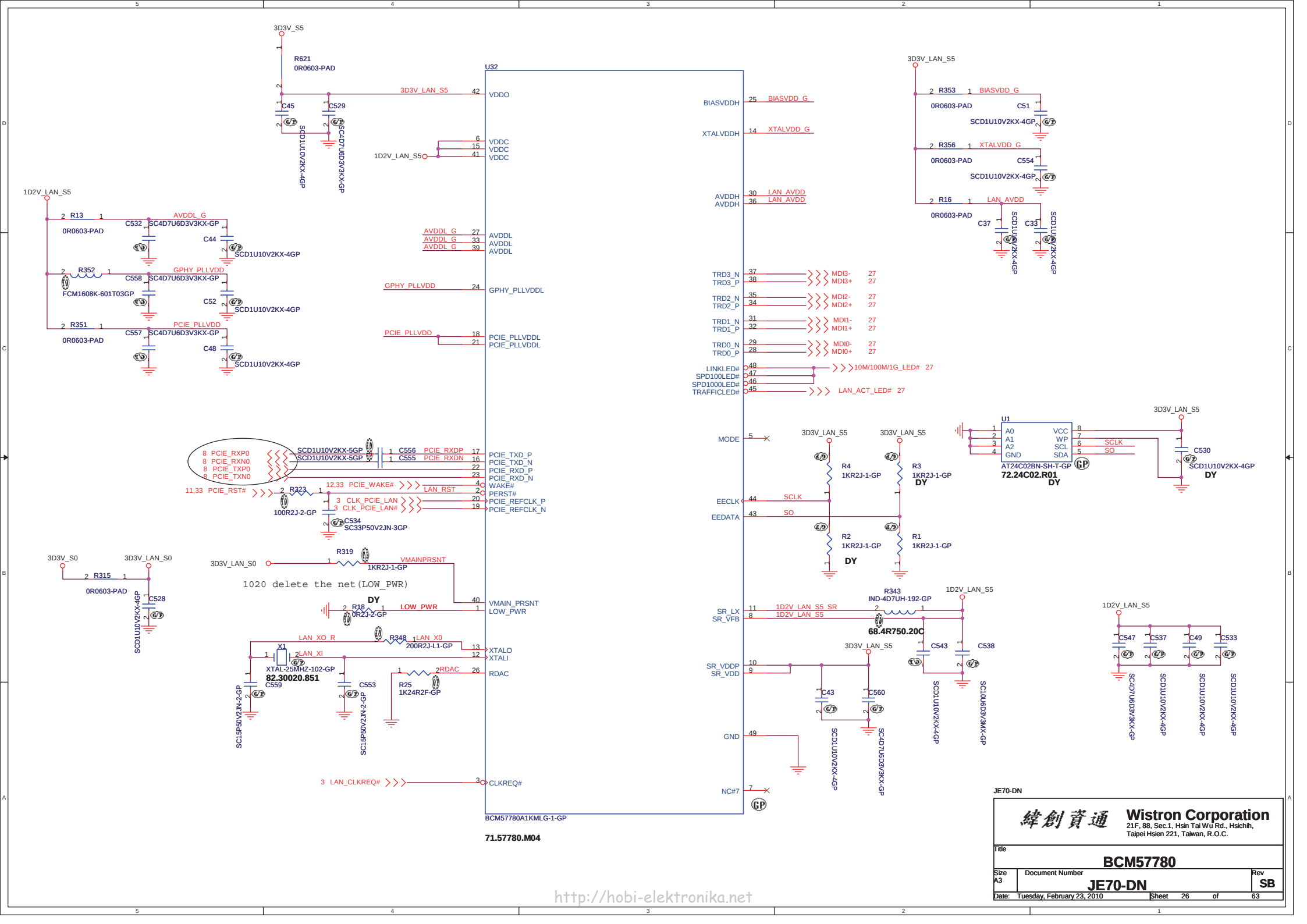
Title	USB	
Size	Document Number: JE70-DN	Rev: SB
Date: Tuesday, February 23, 2010	Sheet 25 of 63	



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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	BCM57780	
Size A3	Document Number JE70-DN	Rev SB
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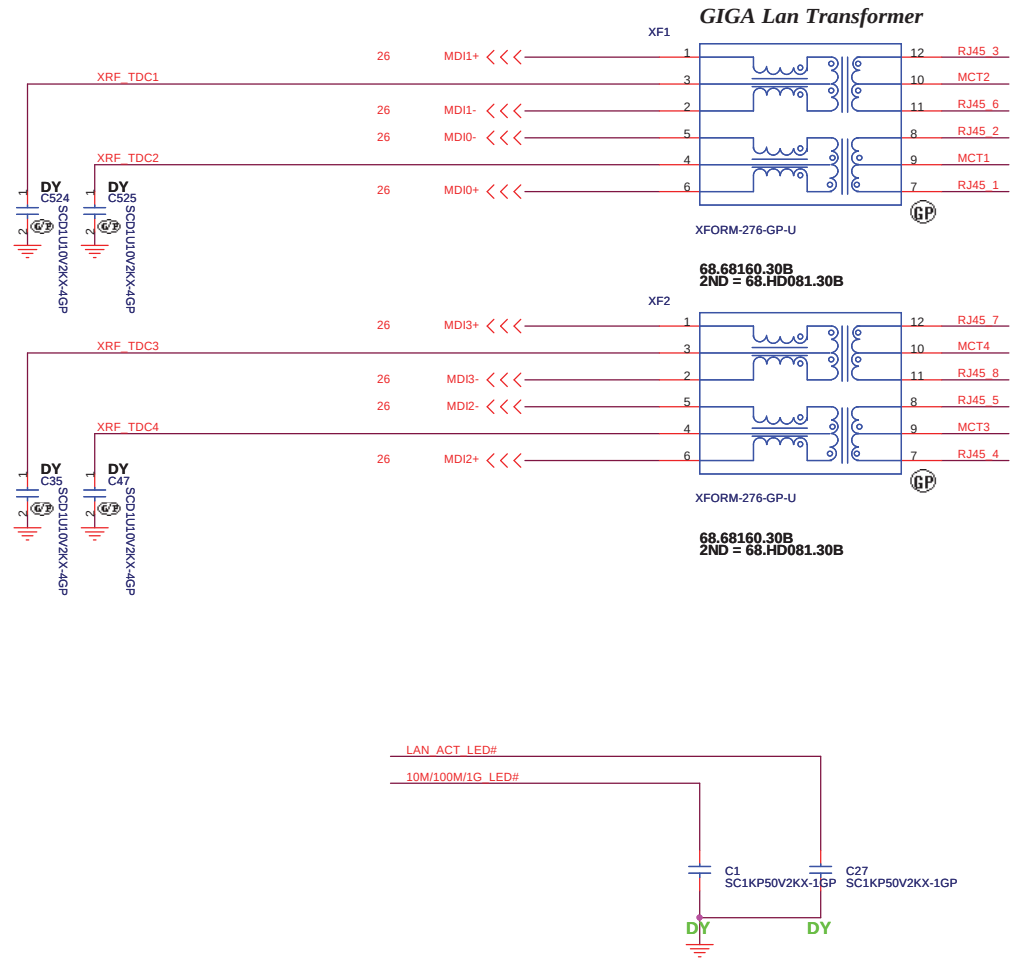
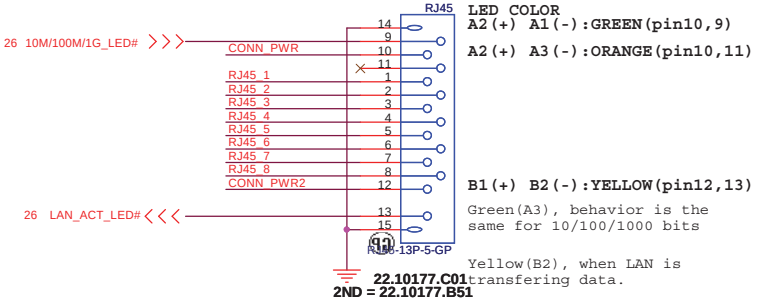
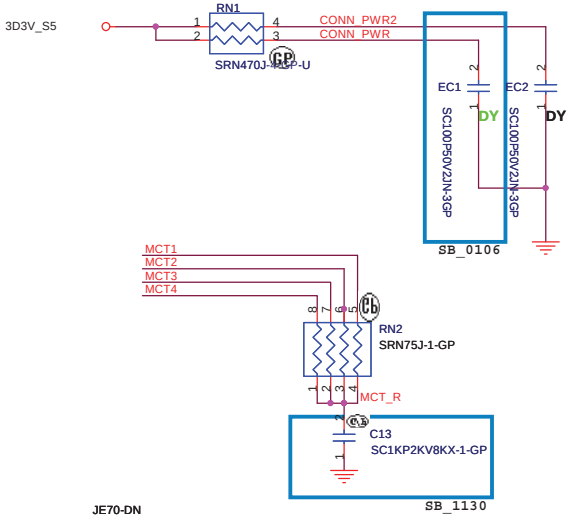
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

LAN Connector

LAN Connector

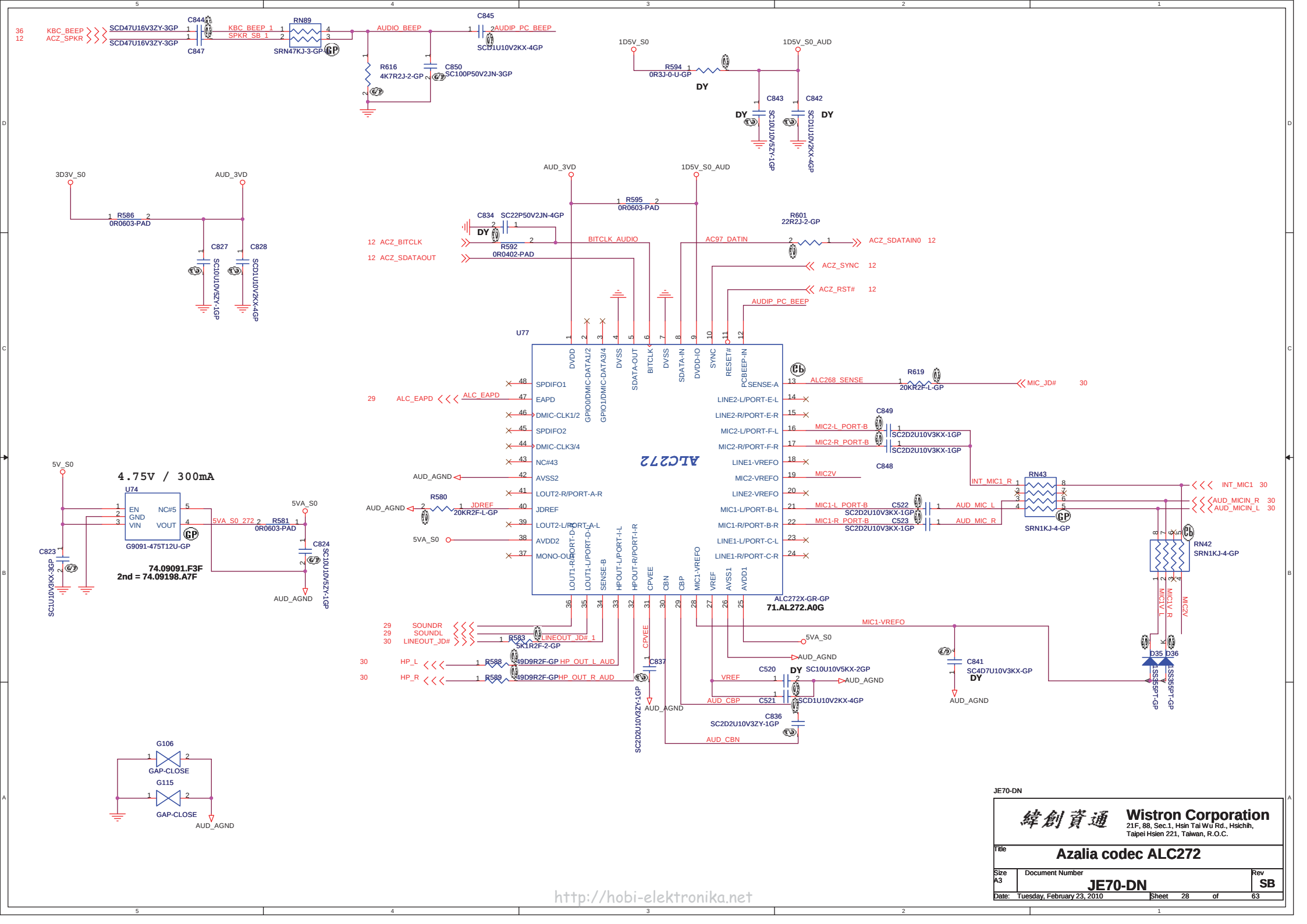






JE70-DN

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LAN CONN		
Size: A3	Document Number: JE70-DN	Rev: SB
Date: Monday, March 01, 2010	Sheet 27 of 63	



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緯創資通 **Wistron Corporation**
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Title: **Azalia codec ALC272**

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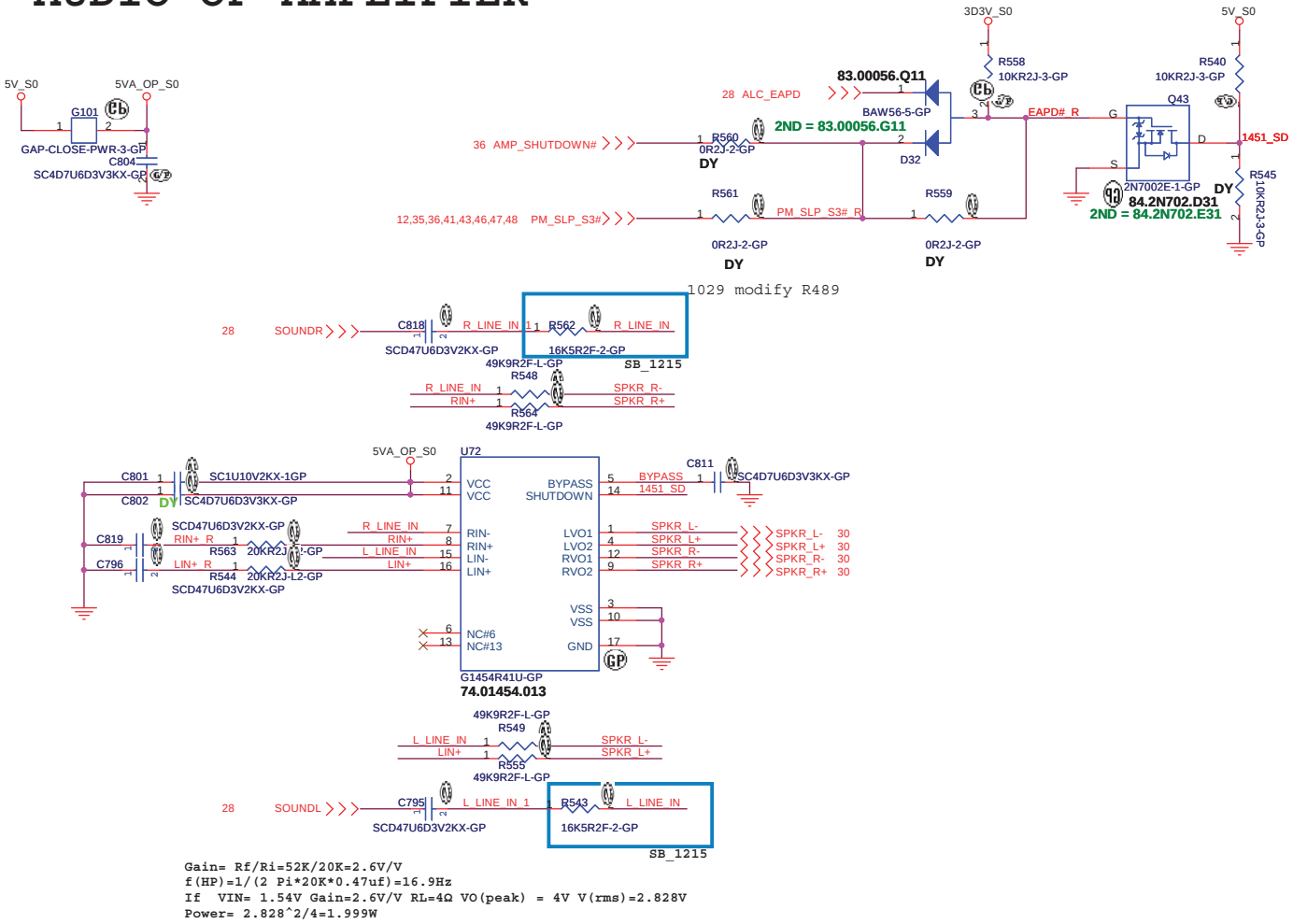
AUDIO OP AMPLIFIER




```
Gain= Rf/Ri=52K/20K=2.6V/V
f(HP)=1/(2 Pi*20K*0.47uf)=16.9Hz
If  VIN= 1.54V Gain=2.6V/V RL=4Ω VO(peak) = 4V V(rms)=2.828V
Power= 2.828^2/4=1.999W
```


JE70-DN

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	AUDIO AMP
Size	Document Number: JE70-DN — Rev: SB
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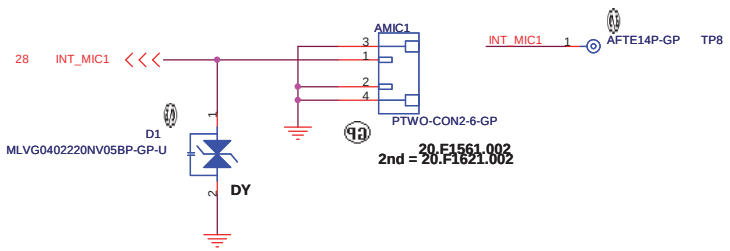
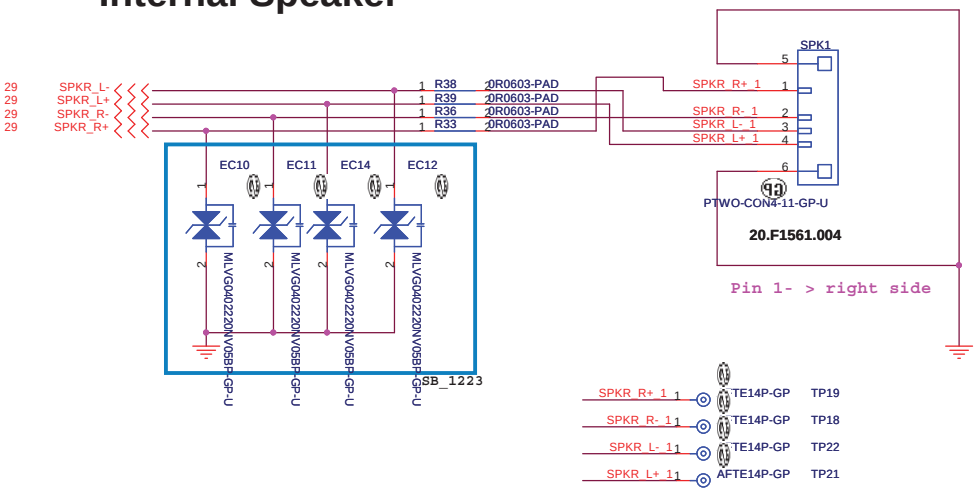
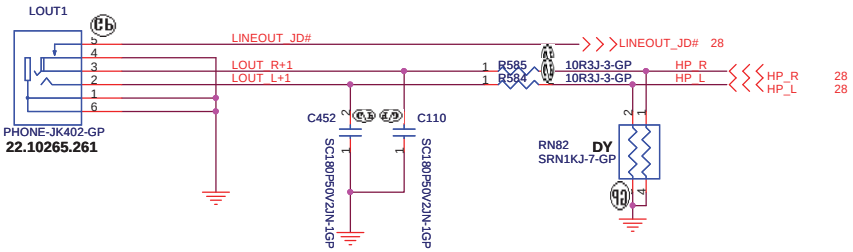
Internal Mic

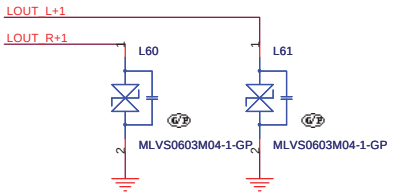


Internal Speaker

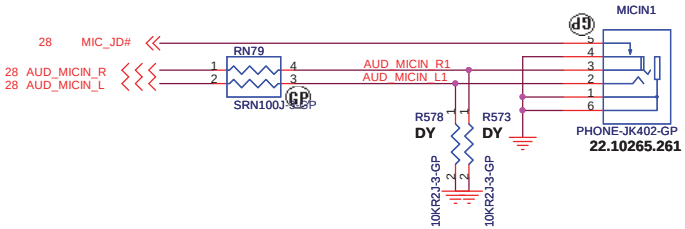


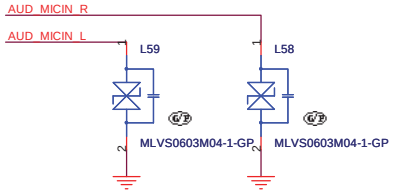
LINE OUT





MIC IN





JE70-DN

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AUDIO JACK	
Size	Document Number JE70-DN	Rev SB
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No Modem Function

JE70-DN

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MDC		
Size	Document Number: JE70-DN	Rev: SB
Date: Thursday, November 19, 2009	Sheet 31 of 63	

5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD) on USB board

JE70-DN

緯創資通 **Wistron Corporation**
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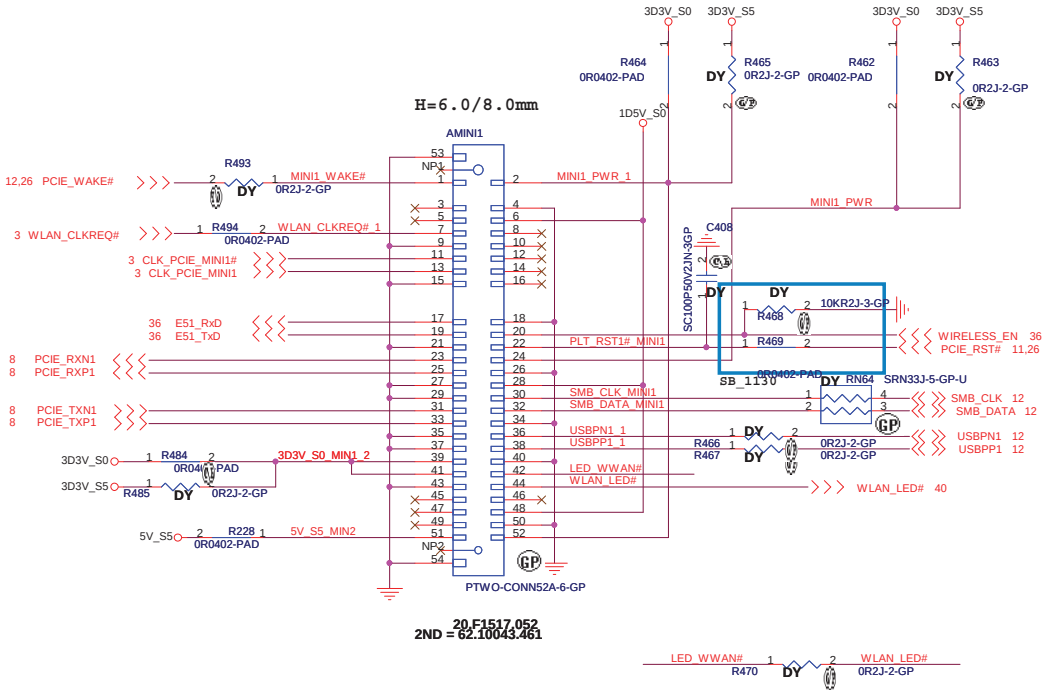
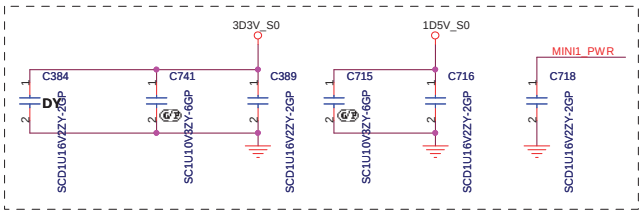
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CARDREADER**		
Size	Document Number: **JE70-DN**	Rev: **SB**
Date: Thursday, November 19, 2009	Sheet 32 of 63	

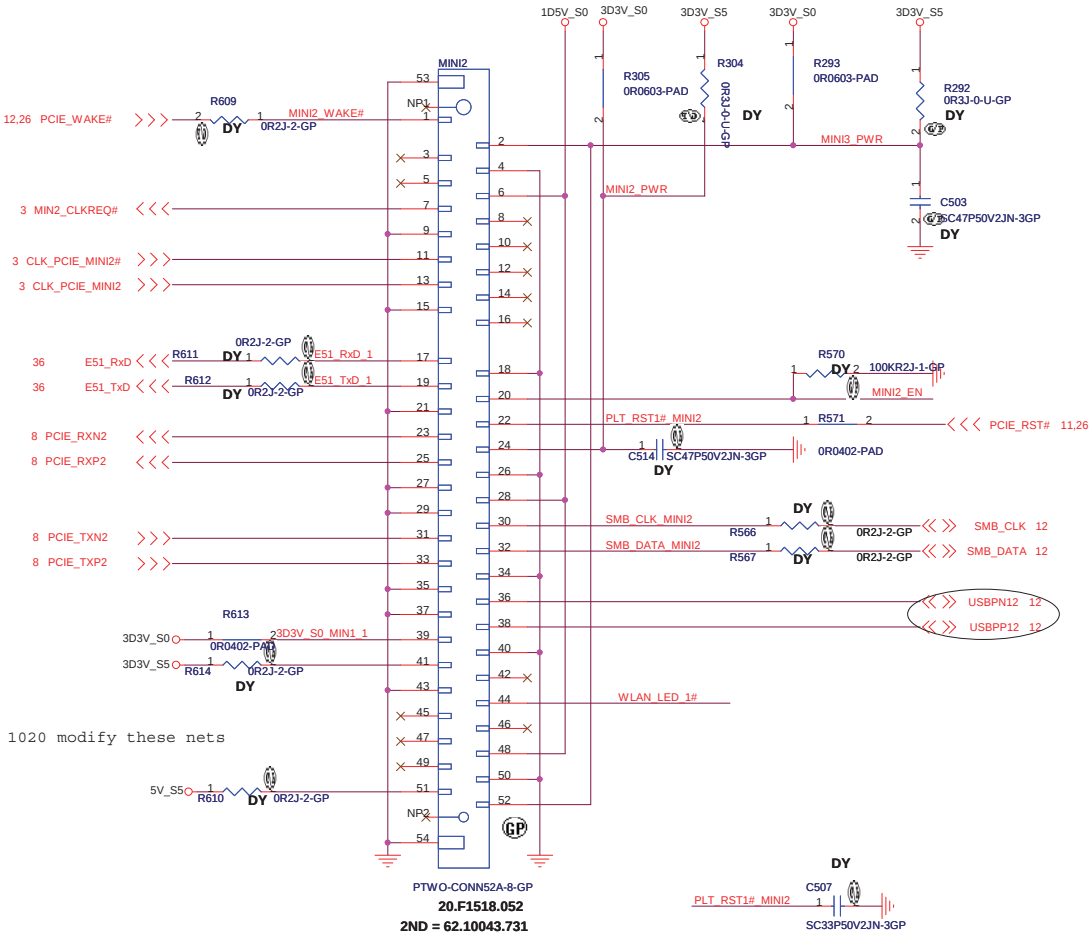
Mini Card Connector(WLAN)



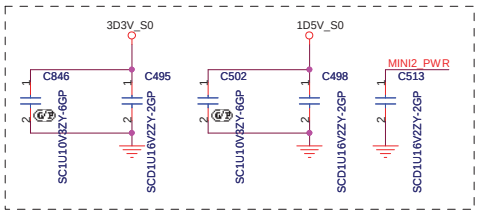
Place near AMINI1

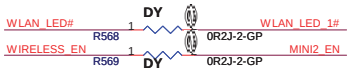


Mini Card Function



Place near MINIC2





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Title	MINI CARD	
Size	Document Number: JE70-DN	Rev: SB
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No NEWCARD Function

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Title		
NEW CARD		
Size	Document Number	Rev
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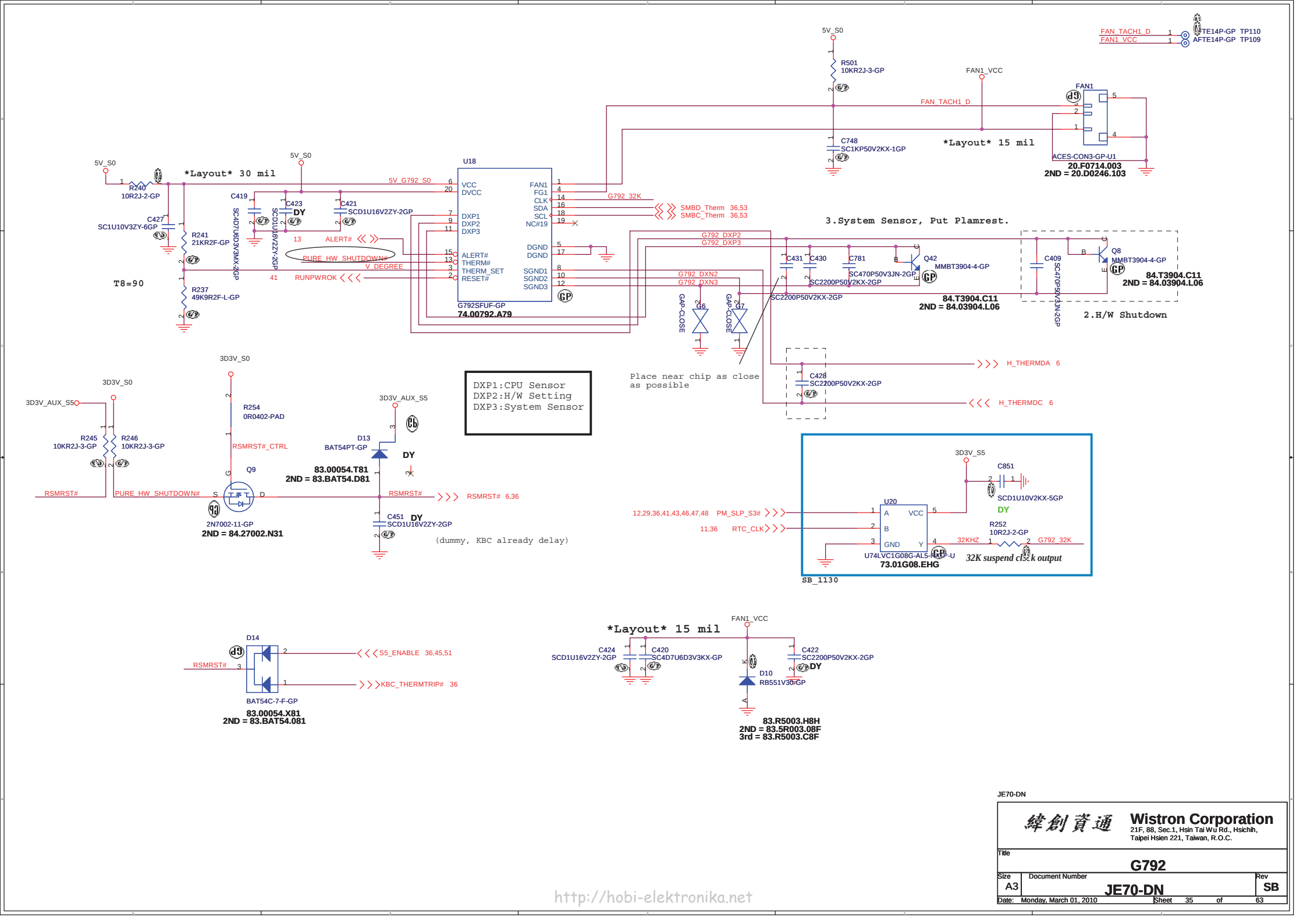

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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**G792**
Size: A3	Document Number: **JE70-DN** Rev: **SB**
Date: Monday, March 01, 2010	Sheet 35 of 63

1020 add R134

1029 modify the net(KBC_BL_ON_IN)

1023 delete R892,R483,R497,R478 and add RN123

1023 swap these nets(KBRCIN#,KA20GATE)

1023 add U101

1023 modify RN89

1111 delete CRT_DEC#

Prevent BIOS data loss solution

FOR KBC DEBUG

Model ID

14": PH 10K 3D3V_AUX_S5

17": PL 10K GND

SB 1126 add TP174

Change to 71.00773.00G

1023 delete R258 and RN122

PCB VER

SA: R250-->1.0K

SB: R250-->2.0K

SC: R250-->3.0K

1 : R250-->4.7K

65W UMA

90W DIS_PX

High:65W Low : 90W

High: UMA Low : DIS_PX

83.R0304.A8H

2ND = 83.R2002.B8E

84.T3906.A11

2ND = 84.03906.F11

THERMAL-----> BATTERY----->

Internal KeyBoard Connector

AKB1 20.K0320.026 ACES-CON26-6GP-U

U61A GPIO41 VDD AVCC VCC VCC VCC VCC VCC

A/D LPC D/A SMB SP SPI GPIO SER/IR

GPIO10/LPCPD# LRESET# LCLK LFRAME# LAD0 LAD1 LAD2 LAD3 SERIRQ GPIO11/CLKRUN# KBRST# GA20 ECSCI#/GPIO54 GPIO65/SMI# GPIO67/PWUREQ#

VREF GPI90/AD0 GPI91/AD1 GPI92/AD2 GPI93/AD3 GPIO05 GPIO04

GPIO74/SDA2 GPIO73/SCL2 GPIO22/SDA1 GPIO17/SCL1

GPIO66/G_PWM

GPIO77 GPIO76/SHBM GPIO75 GPIO81

GPO83/SOUT_CR/BADDR1 GPIO87/SIN_CR GPO84/BADDR0

GPIO16 GPIO34 GPIO36

VCORF

GPI94 GPI95 GPI96 GPI97

GPIO01/TB2 GPIO03 GPIO06 GPIO07 GPIO23 GPIO24 GPIO30 GPIO31 GPIO32/D_PWM GPIO33/H_PWM GPIO40/F_PWM GPIO42/TCK GPIO43/TMS GPIO44/TDI GPIO45/E_PWM GPIO46/TRST# GPIO47 GPIO50/TDO GPIO51 GPIO52/RDY# GPIO53 GPIO70 GPIO71 GPIO72 GPO82/TRIS#

AGND GND GND GND GND GND

NPCE781BA0DX-GP

U61B 2 OF 2 KBC PS/2 FIU

32KX1/32KCLKIN 32KX2 GPIO55/CLKOUT GPIO14/TB1 GPIO20/TA2 GPIO56/TA1 GPIO15/A_PWM GPIO21/B_PWM GPIO13/C_PWM GPIO12/PSDAT3 GPIO25/PSCLK3 GPIO27/PSDAT2 GPIO26/PSCLK2 GPIO35/PSDAT1 GPIO37/PSCLK1 F_SDI F_SDO F_CS0# F_SCK

KBSOUT0/JENK# KBSOUT1/TCK KBSOUT2/TMS KBSOUT3/TDI KBSOUT4/JEN0# KBSOUT5/TDO KBSOUT6/RDY# KBSOUT7 KBSOUT8 KBSOUT9 KBSOUT10 KBSOUT11 KBSOUT12/GPIO64 KBSOUT13/GPIO63 KBSOUT14/GPIO62 KBSOUT15/GPIO61/XOR_OUT GPIO60/KBSOUT16 GPIO57/KBSOUT17

KCOL0 KCOL1 KCOL2 KCOL3 KCOL4 KCOL5 KCOL6 KCOL7 KCOL8 KCOL9 KCOL10 KCOL11 KCOL12 KCOL13 KCOL14 KCOL15 KCOL16 KCOL17

KBSIN0 KBSIN1 KBSIN2 KBSIN3 KBSIN4 KBSIN5 KBSIN6 KBSIN7

KROW1 KROW2 KROW3 KROW4 KROW5 KROW6 KROW7 KROW8

VCC_POR# ECRST#

NPCE781BA0DX-GP

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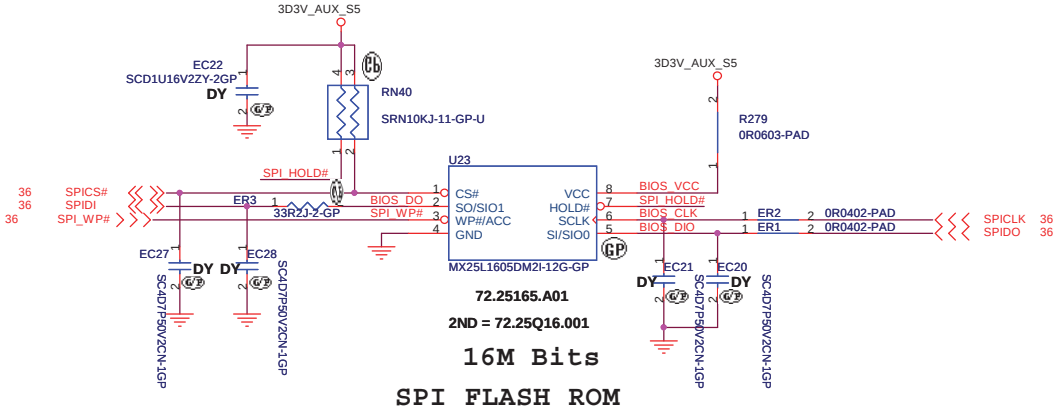
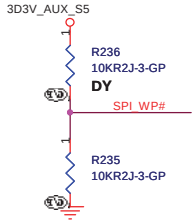
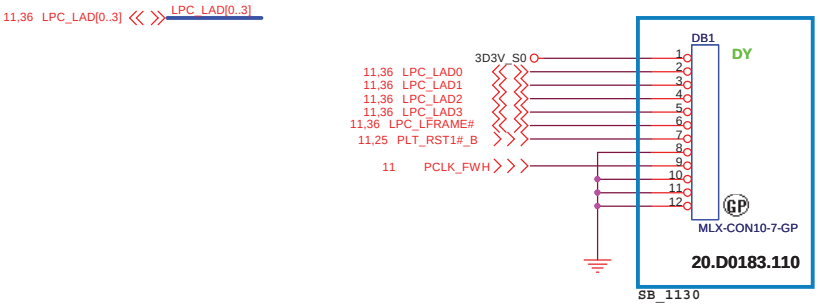
Title: KBC NPCE781B	
Size: A3	Document Number: JE70-DN
Rev: SB	
Date: Monday, March 01, 2010	Sheet 36 of 63

JE70-DN





GOLDEN FINGER FOR DEBUG BOARD



JE70-DN

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Title: **BIOS**

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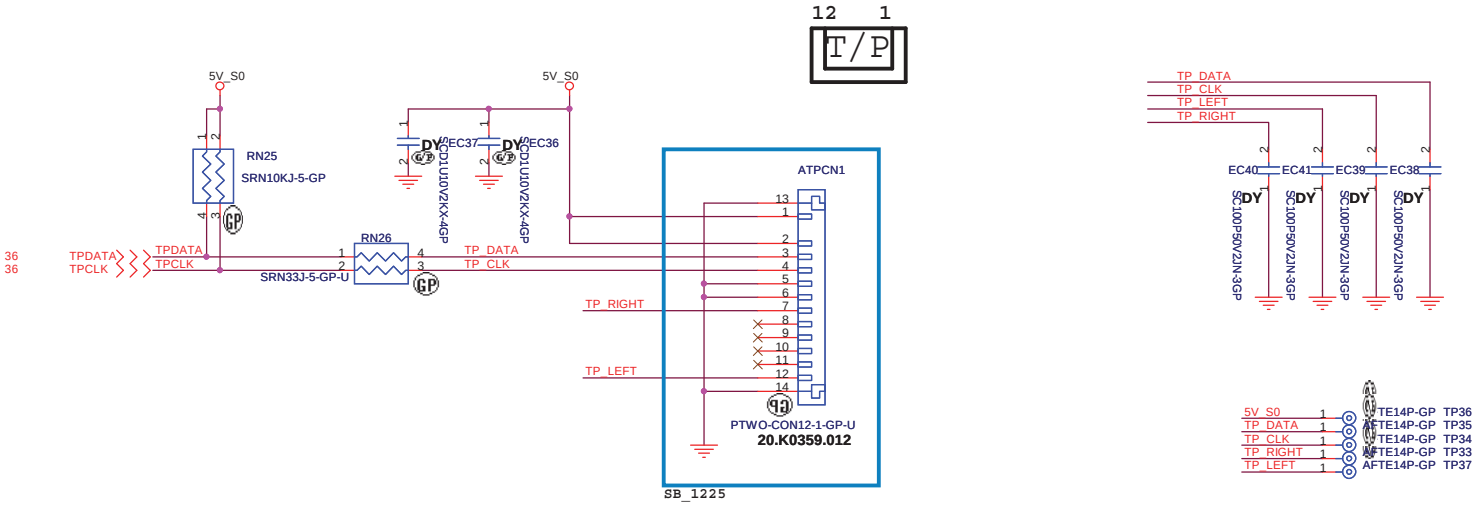

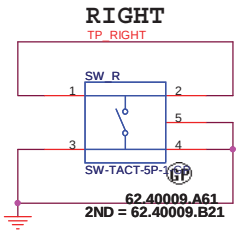

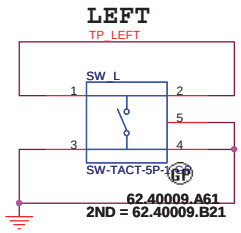

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Title: **Touch PAD**		
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NONE BOARD

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Title: NONE BOARD

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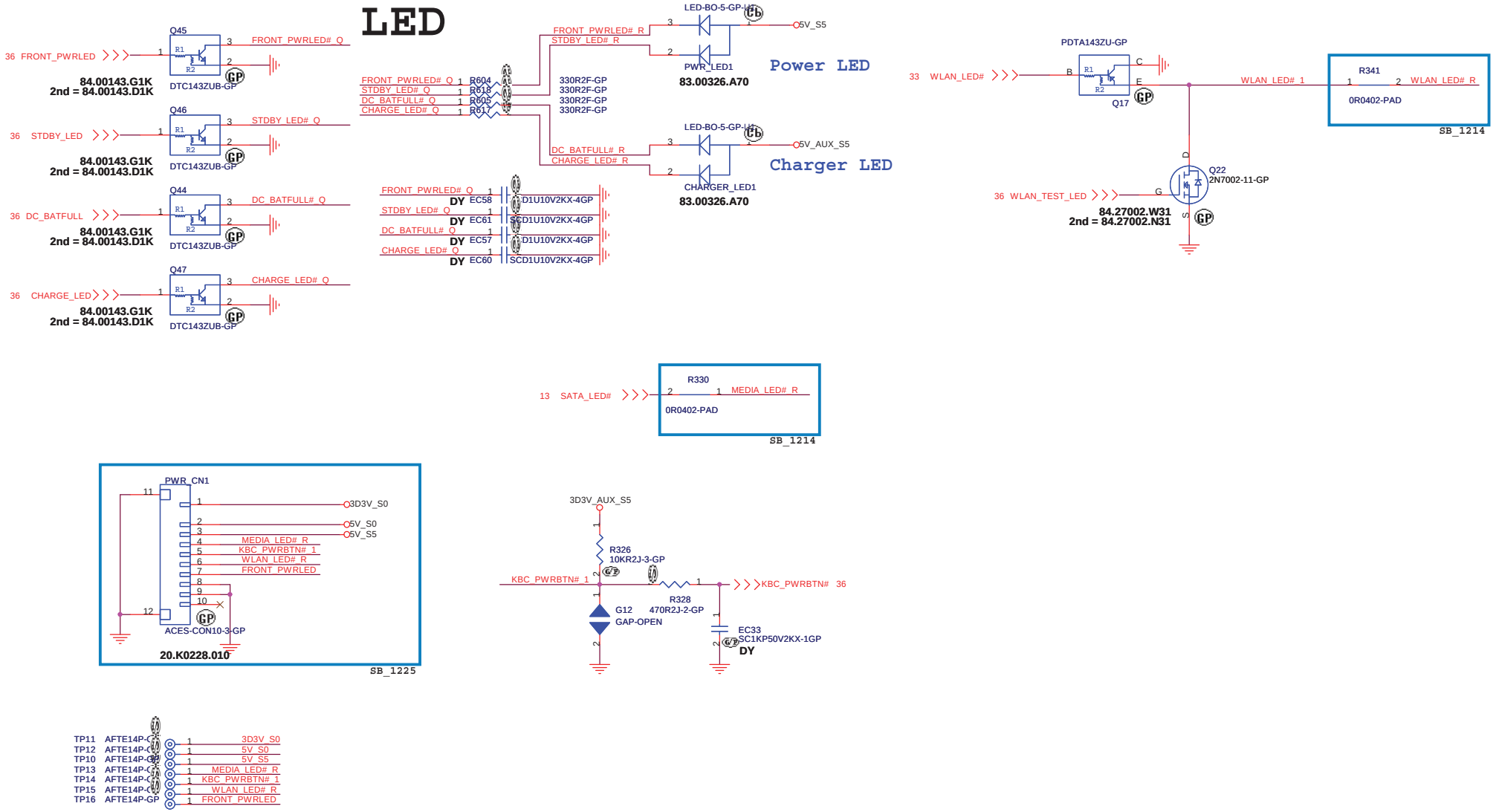
LED



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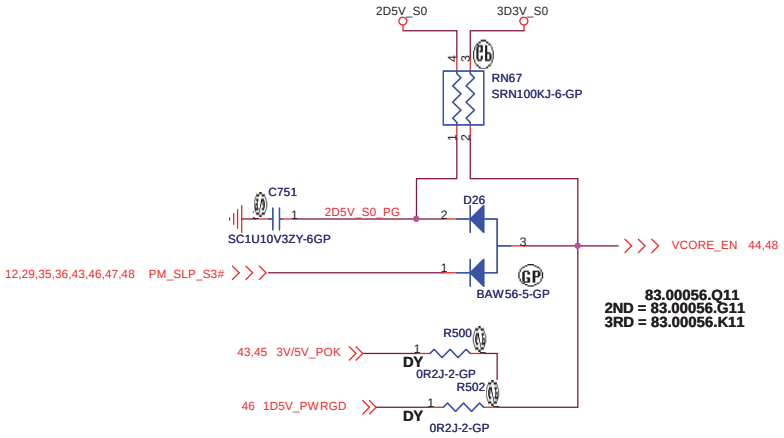
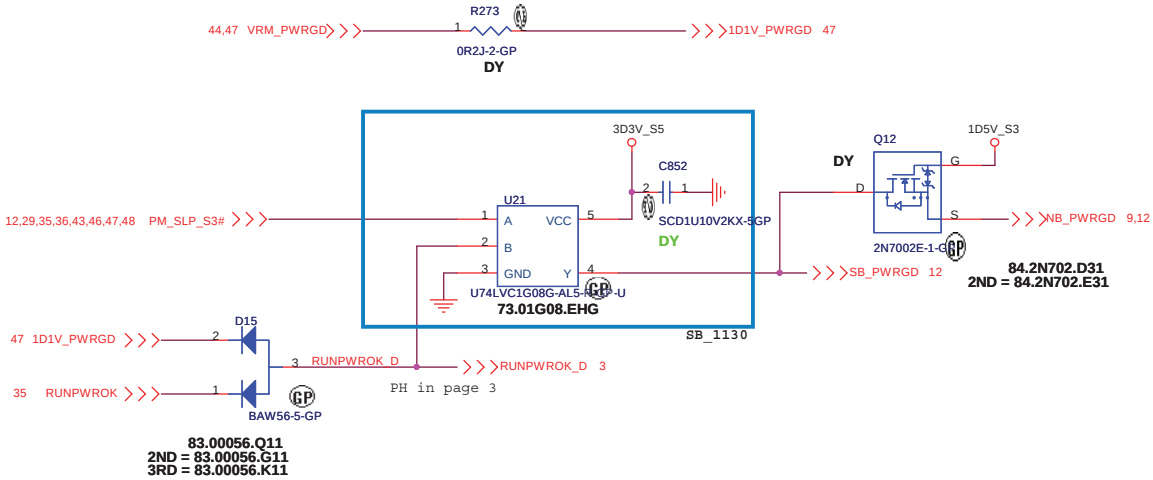
Title: LED		
Size: A3	Document Number: JE70-DN	Rev: SB
Date: Tuesday, February 23, 2010	Sheet 40 of 63	



1D5V_S3_PWRGD

P/H @ 1D8V_S3 PAGE



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Title: **POWER ON LOGIC**

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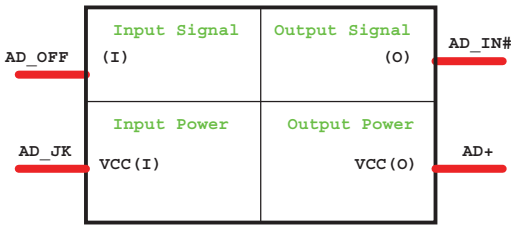
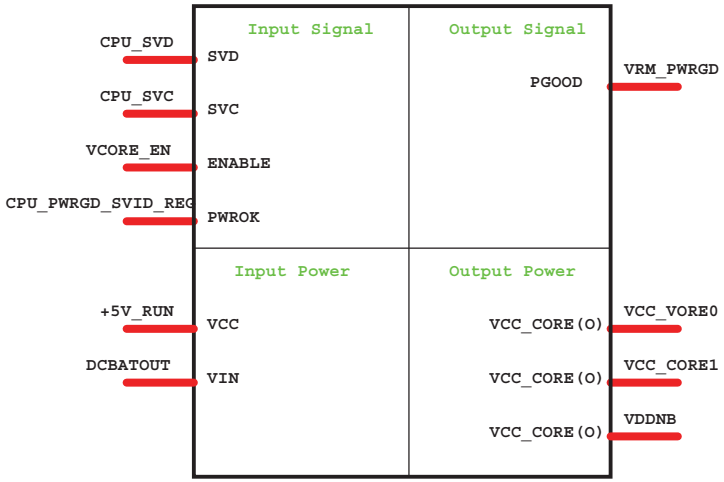
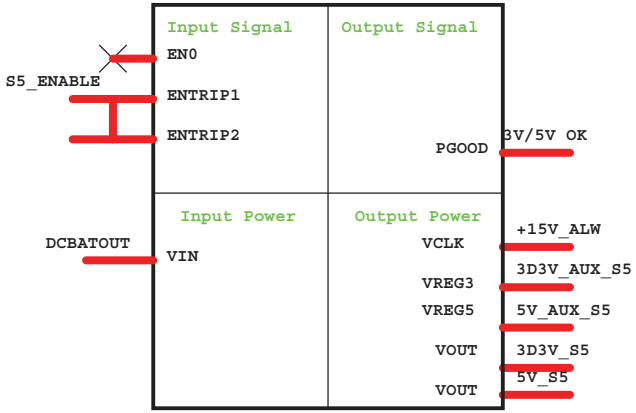
Adapter



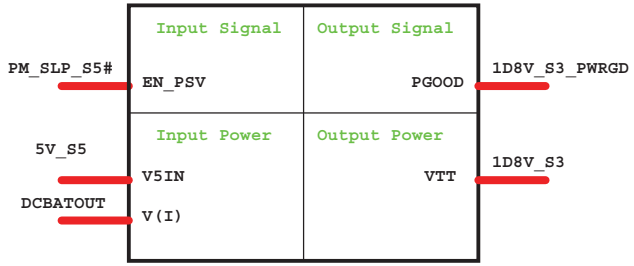
CPU_CORE
ISL6265HRTZ



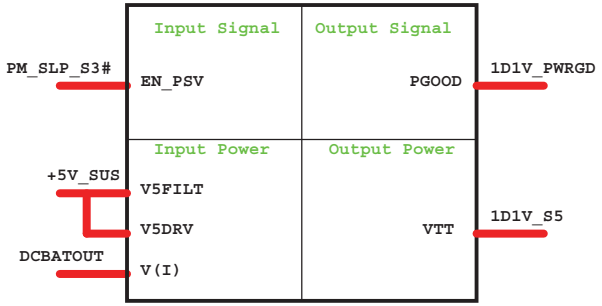
DCDC 5V/3D3V(RT8205A)



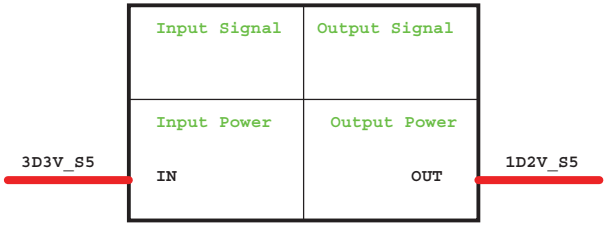
DCDC 1D8V(RT8209B)



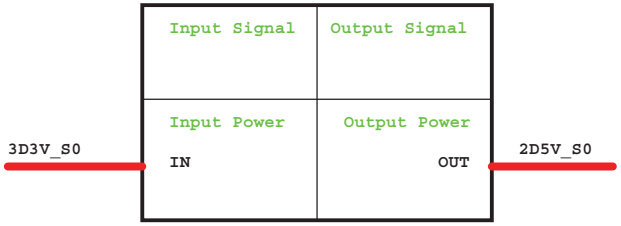
DCDC 1D1V(RT8209)



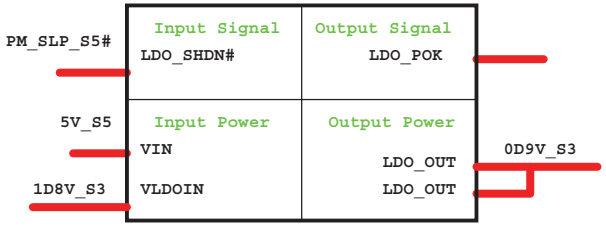
1D2V LDO G9161



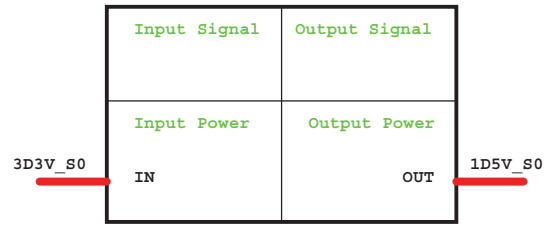
2D5V LDO R9161



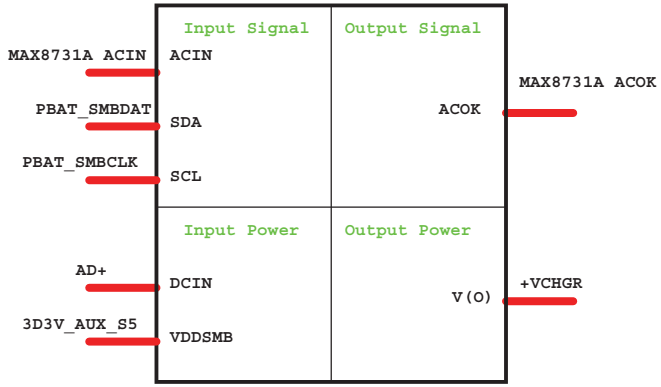
0D9V LDO RT9026



1D5V LDO G9571



CHARGER MAX8731



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Title: Power Block Diagram

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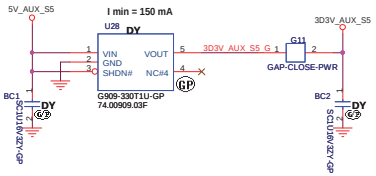
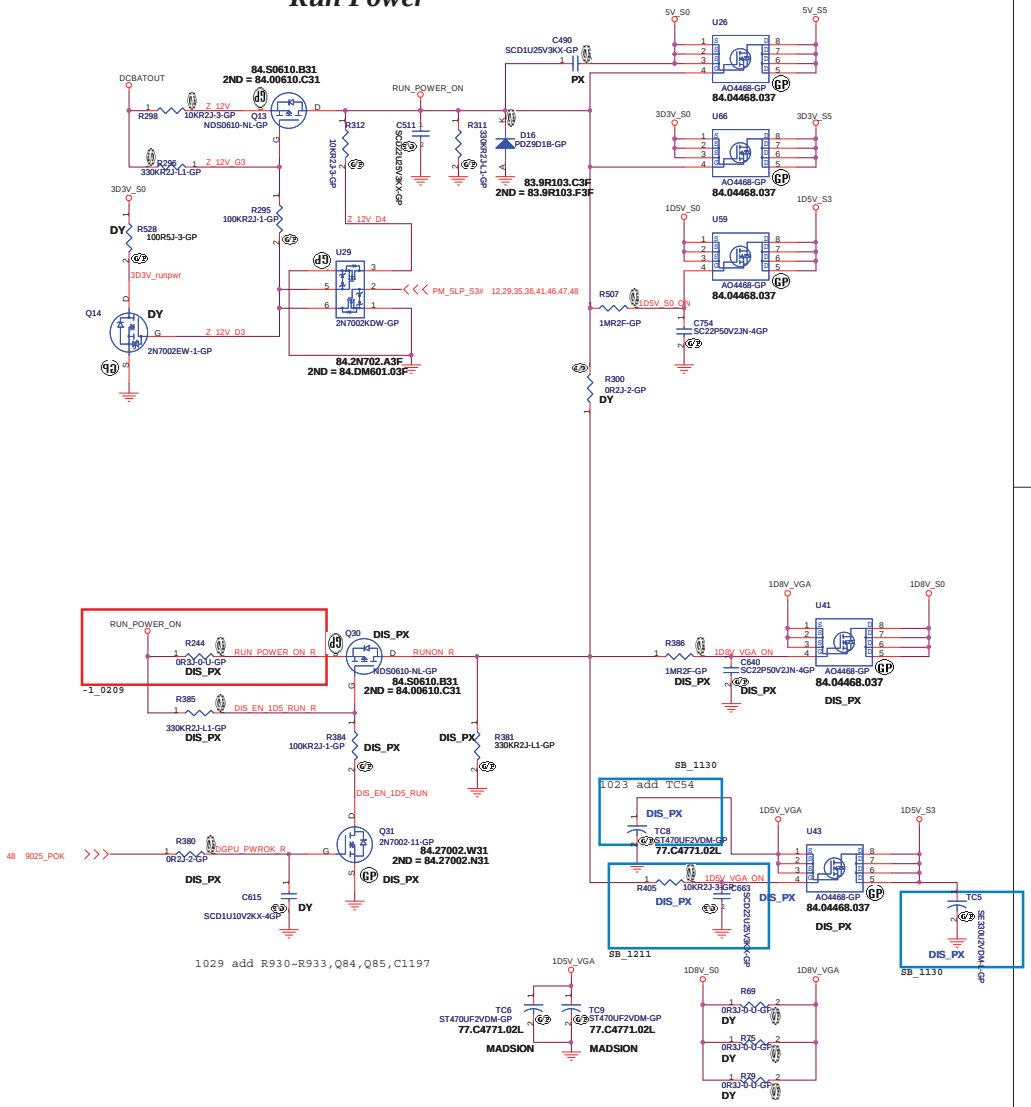
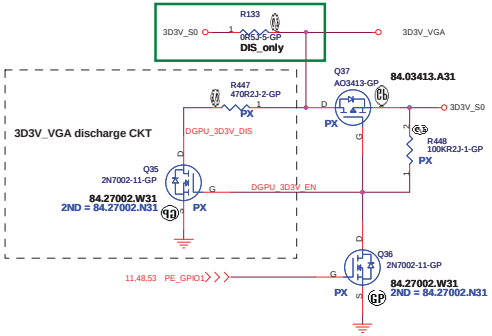
Aux Power 3D3V_AUX_S5

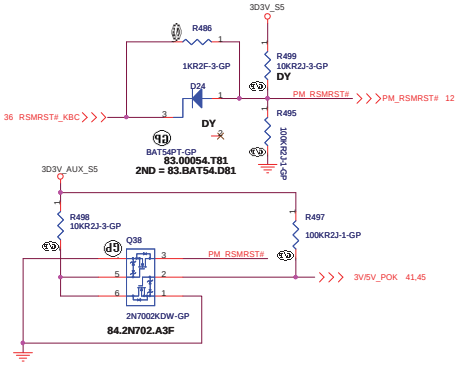


Run Power



+3VS to 3.3V_DELAY Transfer





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Title: RUN AND AUX POWER

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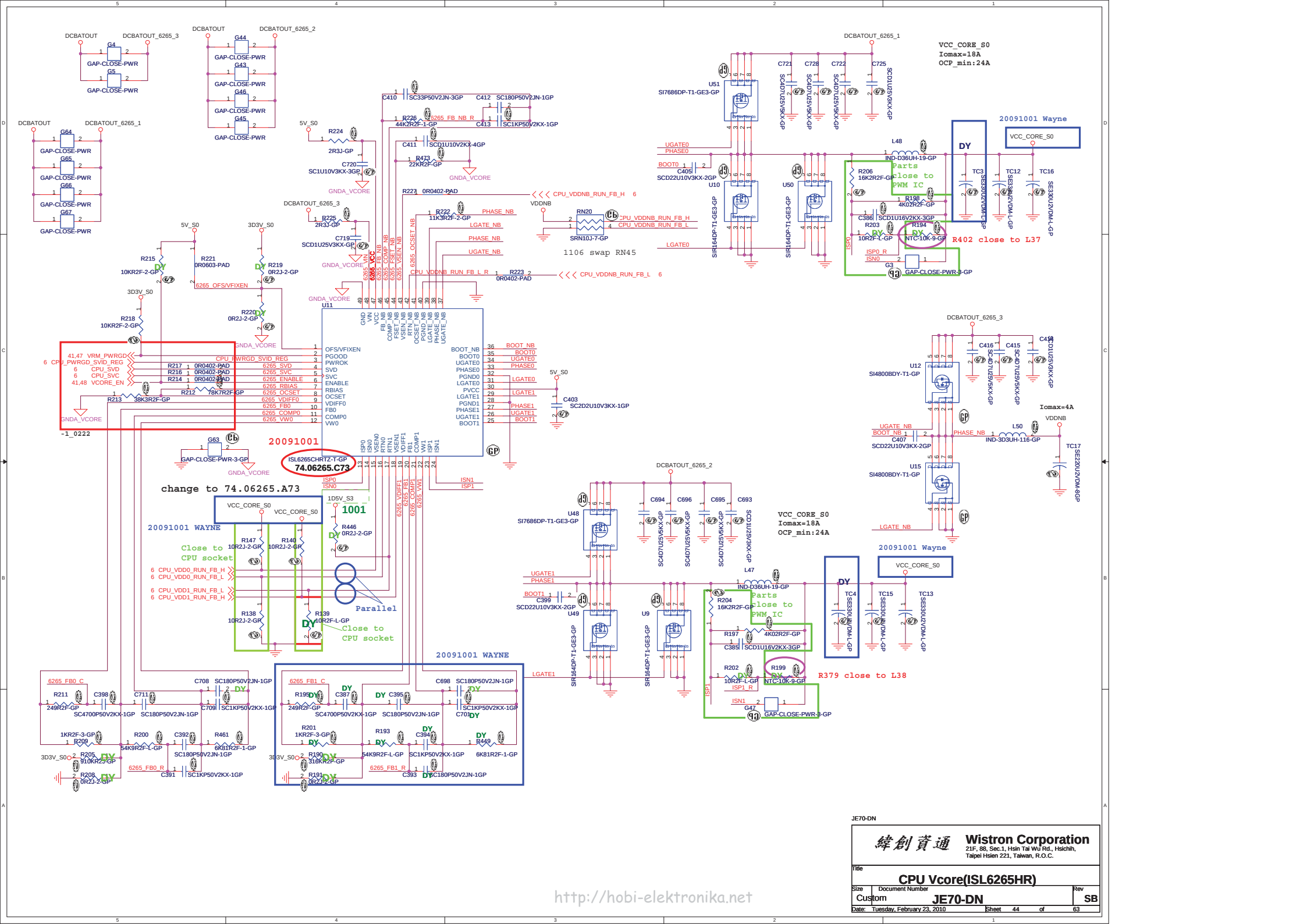
VCC_CORE_S0
Iomax=18A
OCP_min:24A
20091001 Wayne
R402 close to L37
R379 close to L38
1106 swap RN45
change to 74.06265.A73
20091001
ISL6265CHRTZ-T-GP
74.06265.C73
20091001 WAYNE
Close to CPU socket
Parallel
Parts close to PWM IC
Wistron Corporation
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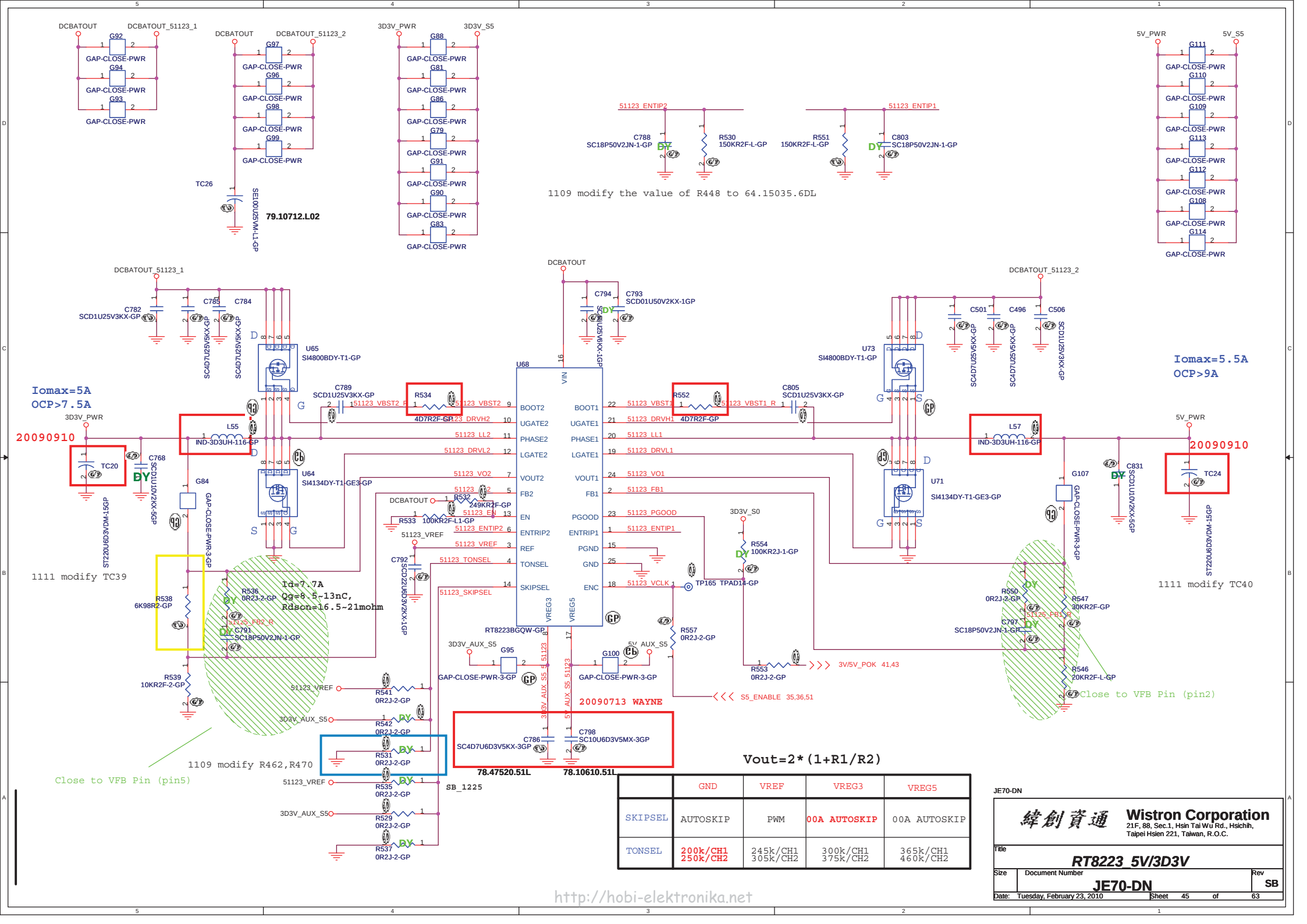
CPU Vcore(ISL6265HR)
JE70-DN
Tuesday, February 23, 2010
http://hobi-elektronika.net



	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

JE70-DN

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Title: RT8223_5V/3D3V

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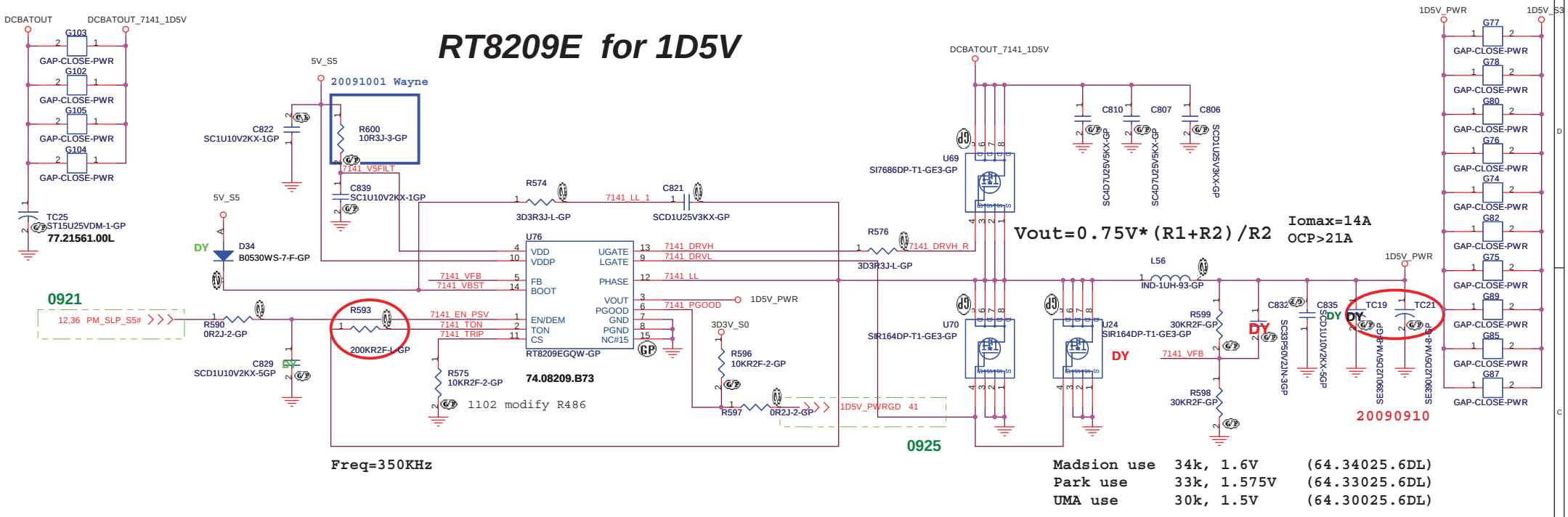
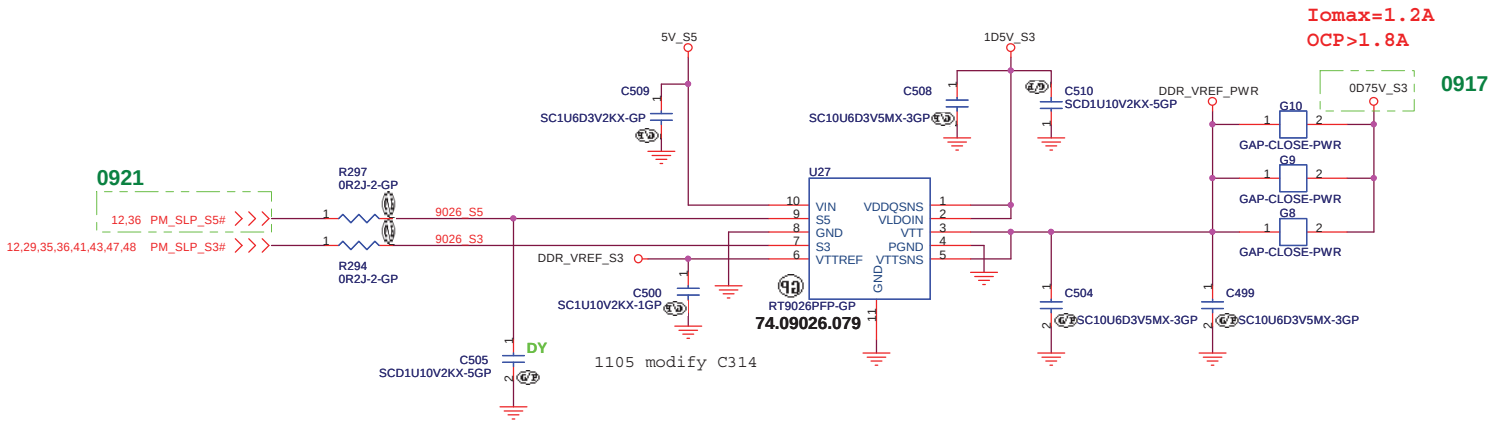
RT8209E for 1D5V



RT9026 for 0D75V_S3



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Title	RT8209E 1D5V	
Size	Document Number JE70-DN	Rev SB
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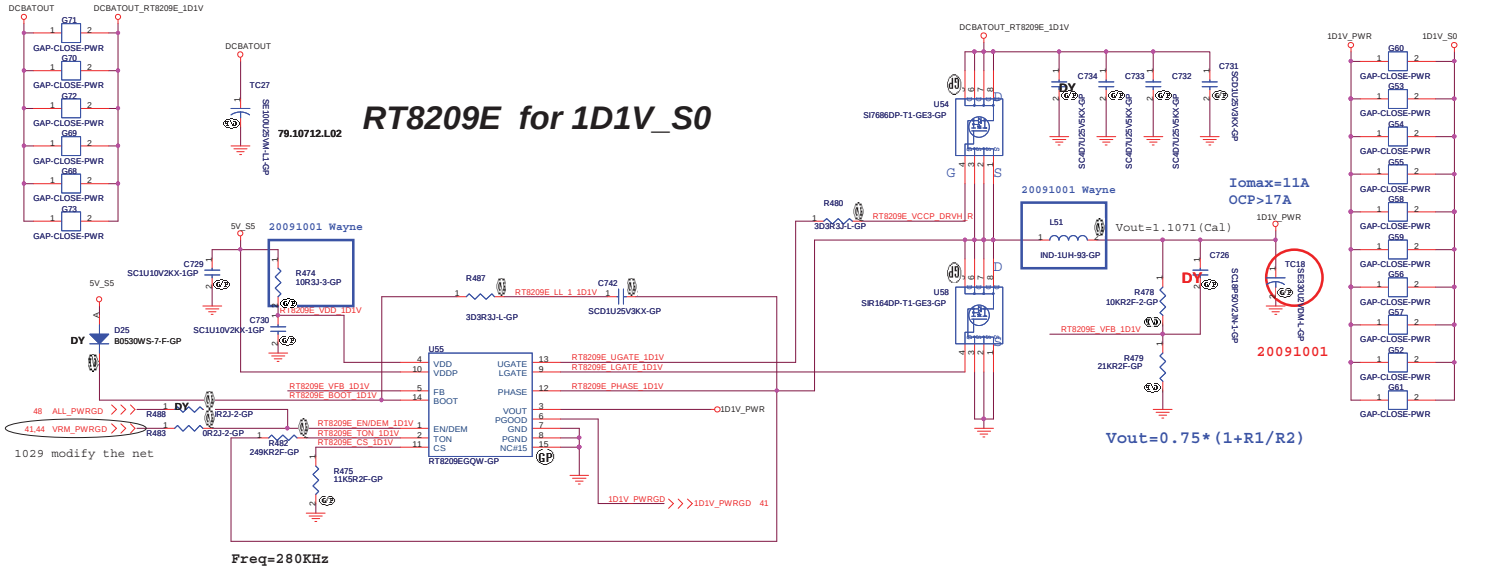

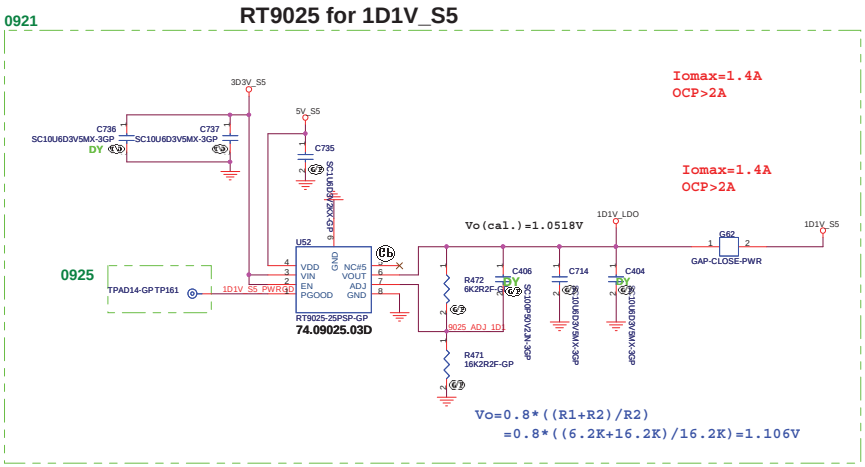

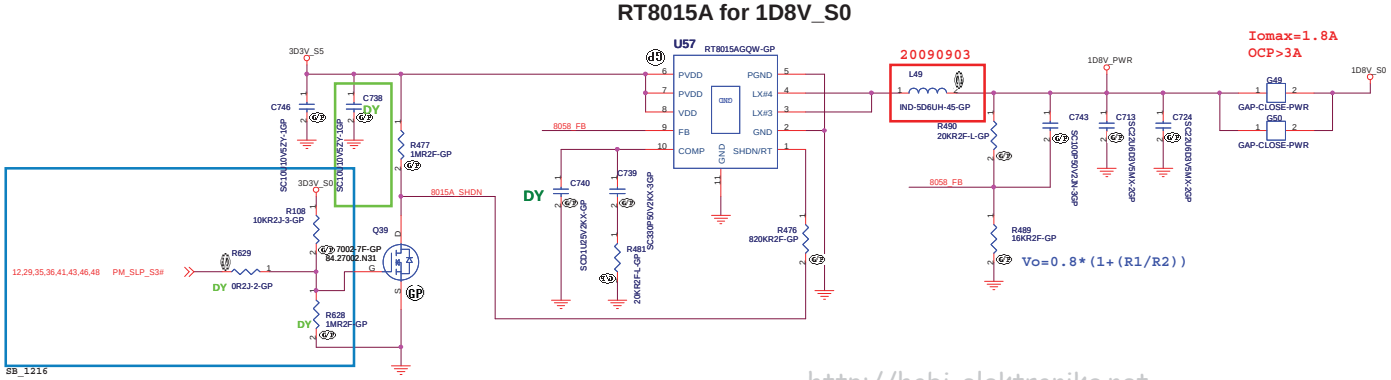

JE70-DN

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Title: 1D1V_S0 & 1D1V_S5 & 1D8V_S0

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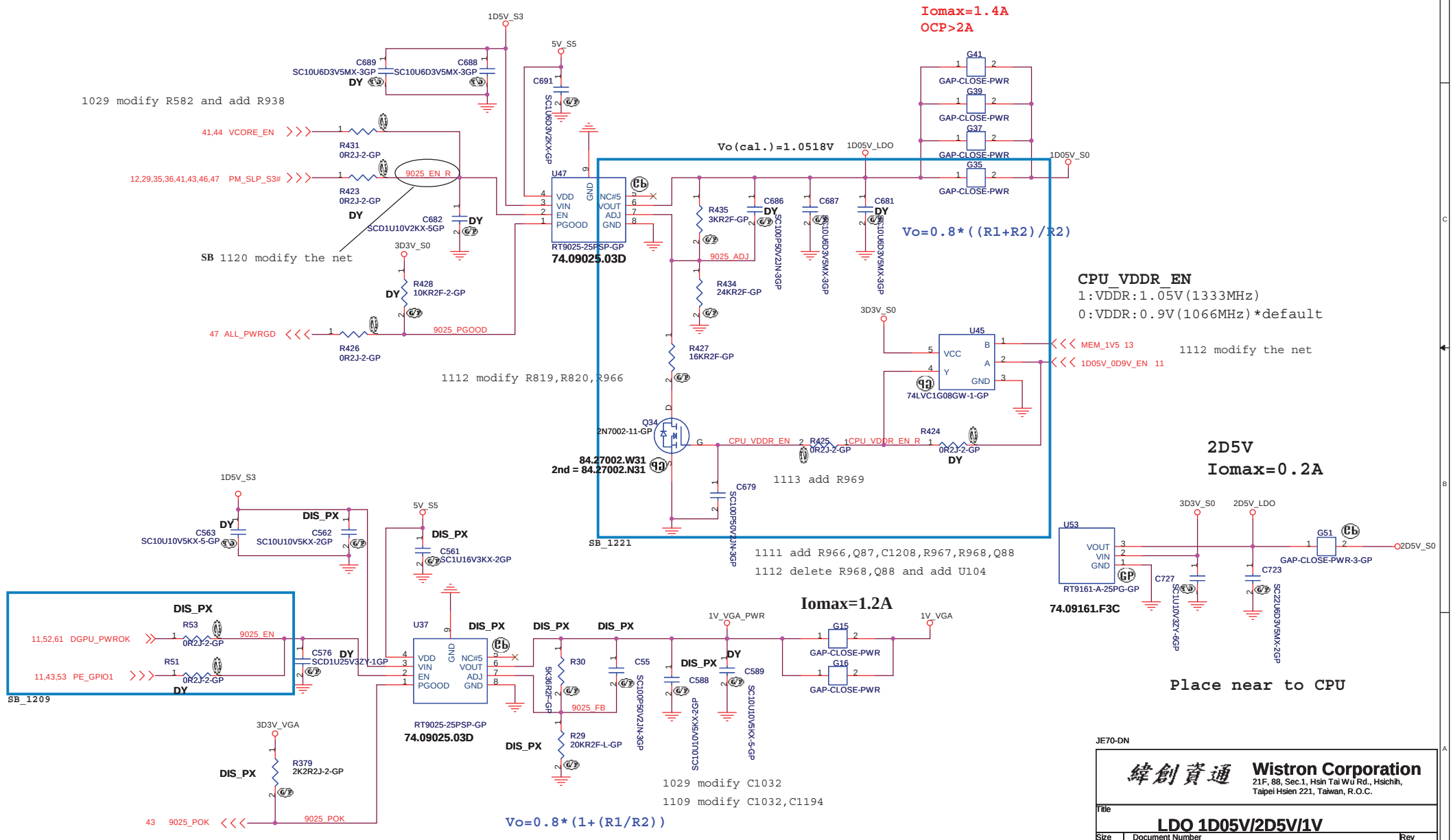
RT9025 for 1D05V_S0



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Title: LDO 1D05V/2D5V/1V

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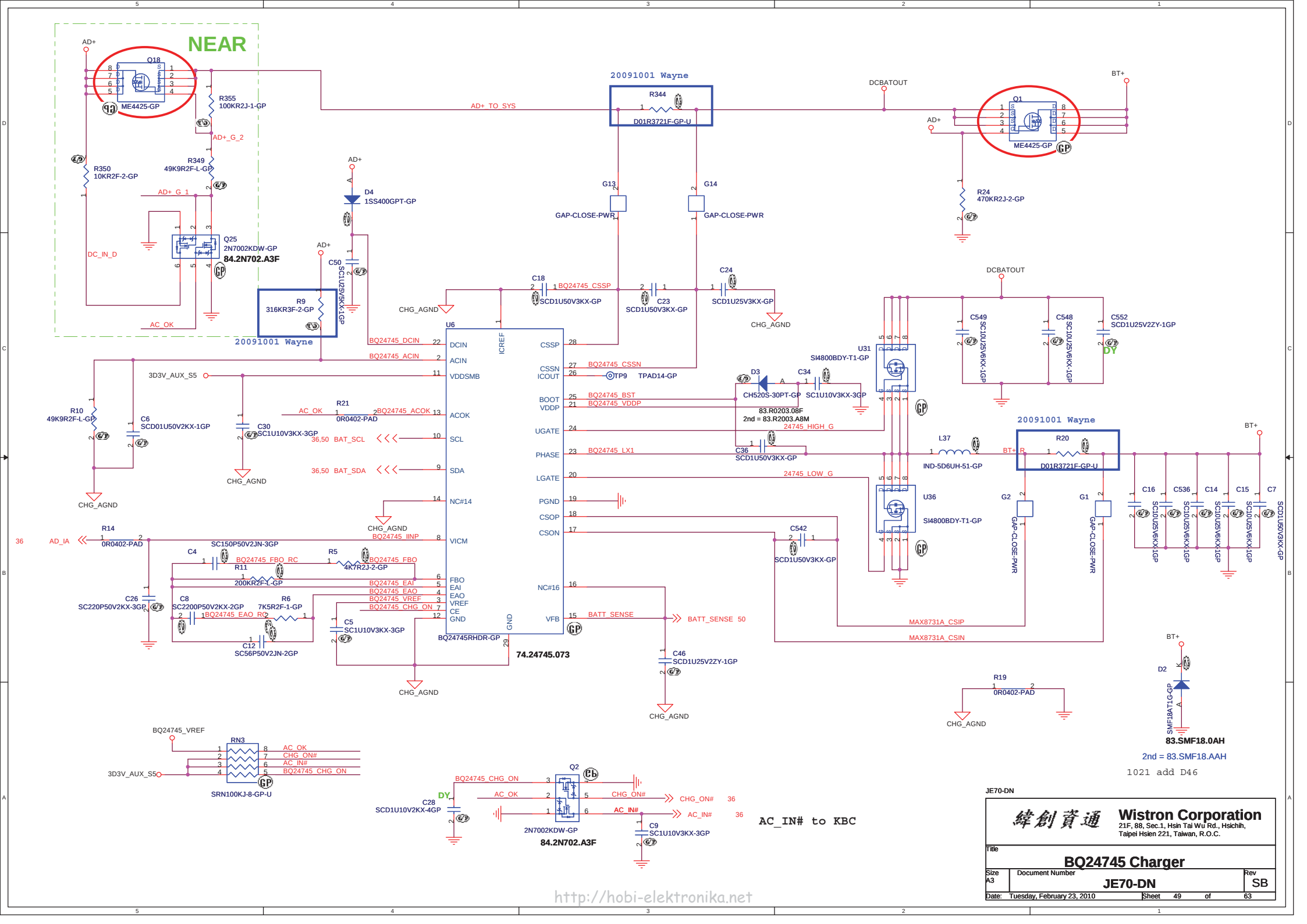
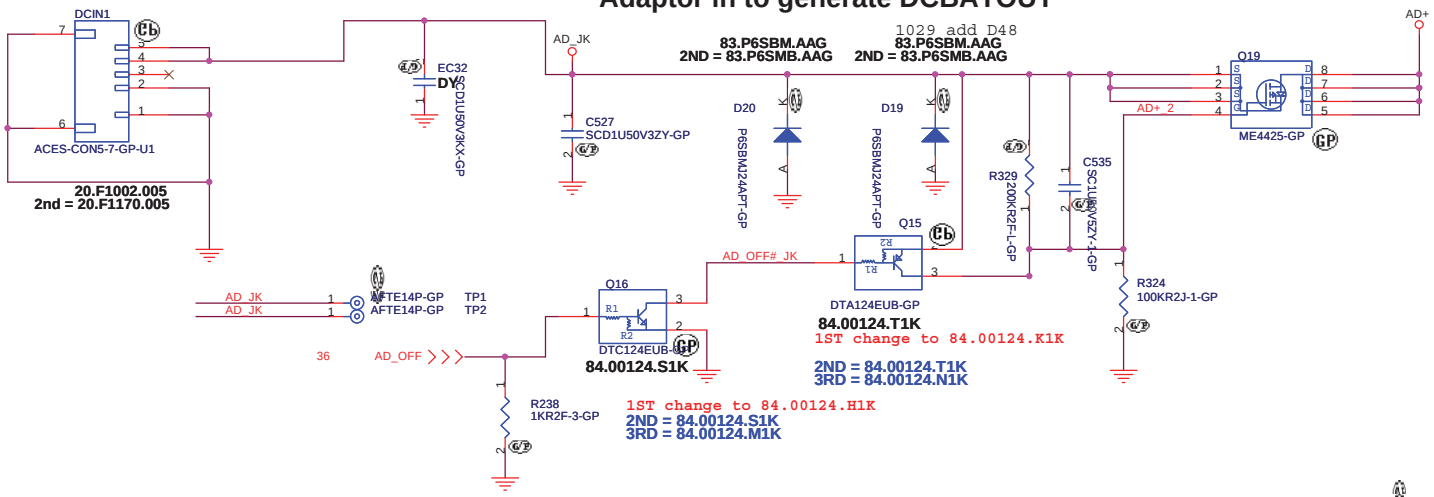

NEAR
20091001 Wayne
20091001 Wayne
20091001 Wayne
Q18
ME4425-GP
R355
100KR2J-1-GP
AD+_G_2
R350
10KR2F-2-GP
R349
49K9R2F-L-GP
AD+_G_1
Q25
2N7002KDW-GP
84.2N702.A3F
DC_IN_D
AC_OK
R9
316KR3F-2-GP
D4
1SS400GPT-GP
C50
SCD1U28V3KX-1GP
AD+_TO_SYS
R344
D01R3721F-GP-U
G13
G14
GAP-CLOSE-PWR
GAP-CLOSE-PWR
DCBATOUT
Q1
ME4425-GP
R24
470KR2J-2-GP
C18
SCD1U50V3KX-GP
C23
SCD1U50V3KX-GP
C24
SCD1U25V3KX-GP
CHG_AGND
U6
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
VICM
FBO
EAI
EAO
VREF
CE
GND
ICREF
CSSP
CSSN
ICOUT
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
BQ24745RHDR-GP
74.24745.073
BQ24745_DCIN
BQ24745_ACIN
BQ24745_CSSN
BQ24745_BST
BQ24745_VDDP
24745_HIGH_G
BQ24745_LX1
24745_LOW_G
BQ24745_IINP
BQ24745_FBO_RC
BQ24745_FBO
BQ24745_EAI
BQ24745_EAO
BQ24745_VREF
BQ24745_CHG_ON
BATT_SENSE
BATT_SENSE 50
MAX8731A_CSIP
MAX8731A_CSIN
3D3V_AUX_S5
R10
49K9R2F-L-GP
C6
SCD01U50V2KX-1GP
C30
SC1U10V3KX-3GP
R21
0R0402-PAD
36,50 BAT_SCL
36,50 BAT_SDA
R14
0R0402-PAD
AD_IA
SC150P50V2JN-3GP
C4
R11
200KR2F-L-GP
R5
4K7R2J-2-GP
C26
SC220P50V2KX-3GP
C8
SC2200P50V2KX-2GP
R6
7K5R2F-1-GP
C5
SC1U10V3KX-3GP
C12
SC56P50V2JN-2GP
C542
SCD1U50V3KX-GP
C46
SCD1U25V2ZY-1GP
D3
CH520S-30PT-GP
C34
SC1U10V3KX-3GP
83.R0203.08F
2nd = 83.R2003.A8M
C36
SCD1U50V3KX-GP
U31
SI4800BDY-T1-GP
U36
SI4800BDY-T1-GP
L37
IND-5D6UH-51-GP
R20
D01R3721F-GP-U
C549
SC10U25V6KX-1GP
C548
SC10U25V6KX-1GP
C552
SCD1U25V2ZY-1GP
DY
C16
C536
C14
C15
C7
SCD1U50V3KX-GP
R19
0R0402-PAD
D2
SMF18AT1G-GP
83.SMF18.0AH
2nd = 83.SMF18.AAH
1021 add D46
RN3
SRN100KJ-8-GP-U
AC_OK
CHG_ON#
AC_IN#
BQ24745_CHG_ON
Q2
2N7002KDW-GP
84.2N702.A3F
C28
SCD1U10V2KX-4GP
C9
SC1U10V3KX-3GP
CHG_ON#
AC_IN#
AC_IN# to KBC
JE70-DN
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BQ24745 Charger
Size A3
Document Number
JE70-DN
Rev SB
Date: Tuesday, February 23, 2010
Sheet 49 of 63
http://hobi-elektronika.net

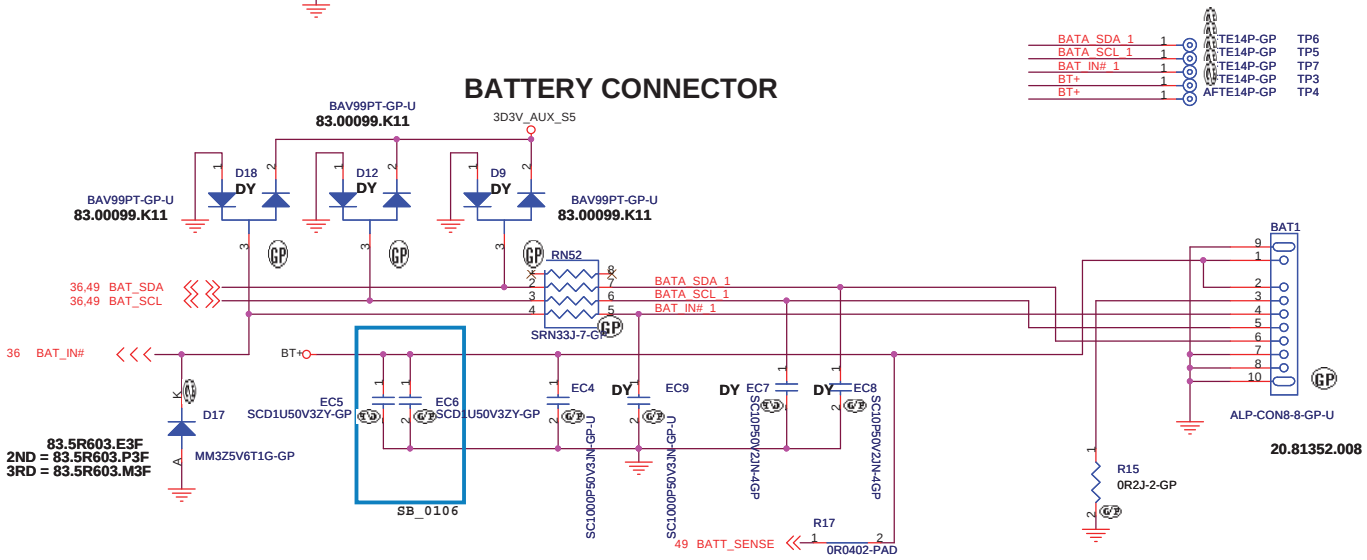
1021 modify DCIN1

1Pin=3A

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



Pin NO	Symbol
1	GND
2	GND
3	SMD
4	SMC
5	TS
6	B/I
7	BT+
8	BT+

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Title: **AD/BATT CONN**

Size | Document Number: **JE70-DN** | Rev: **SB**

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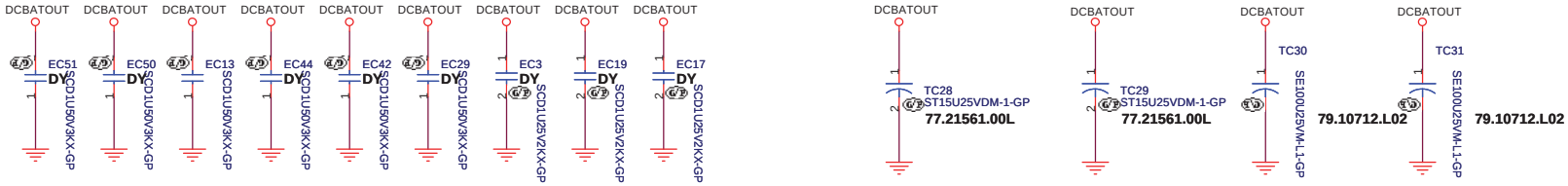
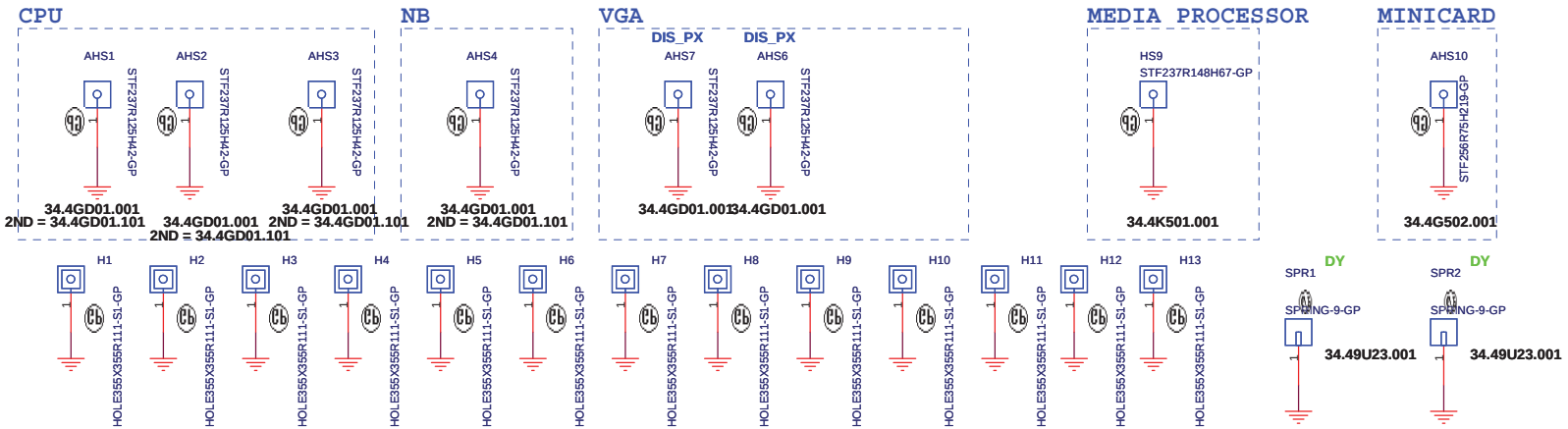
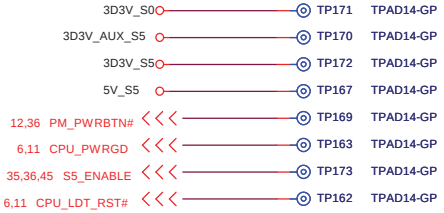




Check test point



Test Point放在Dimm Door打開可量測處

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Taipei Hsien 221, Taiwan, R.O.C.

Title: EMI/Spring/Boss

Size | Document Number: JE70-DN | Rev: SB

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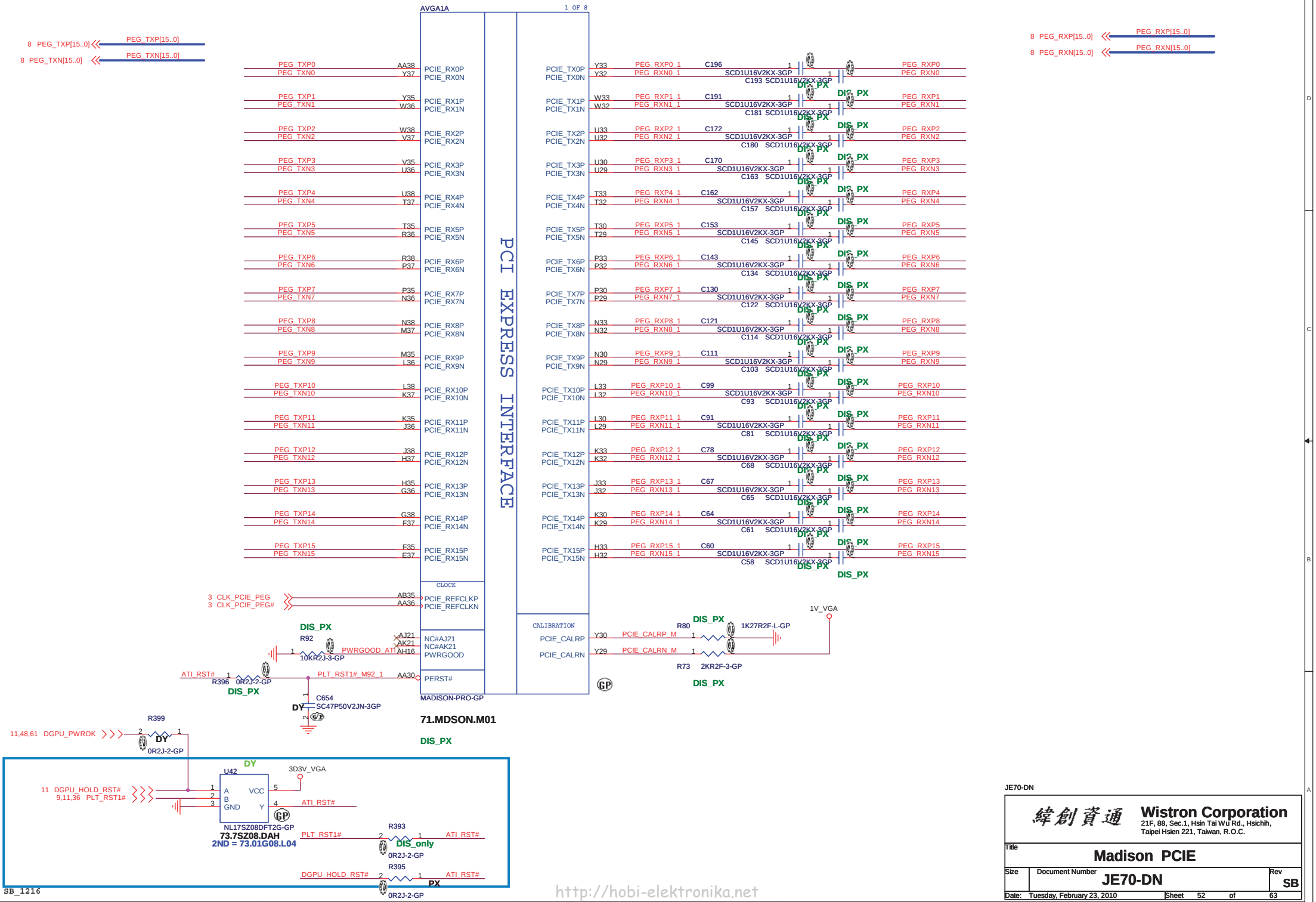

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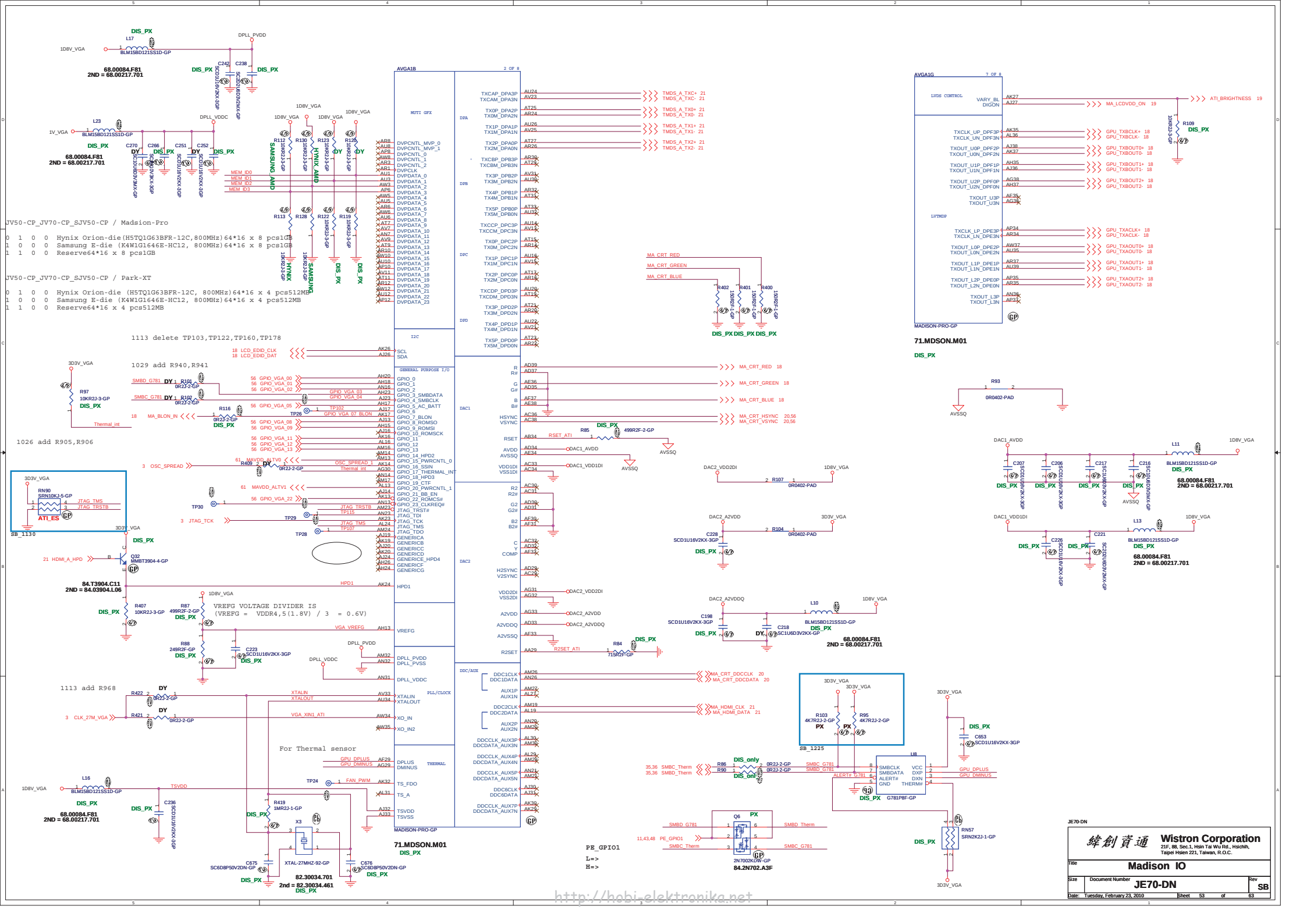
Title	Madison PCIE	
Size	Document Number: JE70-DN	Rev: SB
Date: Tuesday, February 23, 2010	Sheet 52 of 63	


JV50-CP_JV70-CP_SJV50-CP / Madsion-Pro
0 1 0 0 Hynix Orion-die(H5TQ1G63BFR-12C,800MHz)64*16 x 8 pcs1GB
1 0 0 0 Samsung E-die (K4W1G1646E-HC12, 800MHz)64*16 x 8 pcs1GB
1 1 0 0 Reserve64*16 x 8 pcs1GB
JV50-CP_JV70-CP_SJV50-CP / Park-XT
0 1 0 0 Hynix Orion-die (H5TQ1G63BFR-12C, 800MHz)64*16 x 4 pcs512MB
1 0 0 0 Samsung E-die (K4W1G1646E-HC12, 800MHz)64*16 x 4 pcs512MB
1 1 0 0 Reserve64*16 x 4 pcs512MB
1113 delete TP103,TP122,TP160,TP178
1029 add R940,R941
1026 add R905,R906
1113 add R968
VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)
For Thermal sensor
PE_GPIO1
L=>
H=>
71.MDSON.M01
84.T3904.C11
82.30034.701
84.2N702.A3F
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Madison IO
JE70-DN
Tuesday, February 23, 2010
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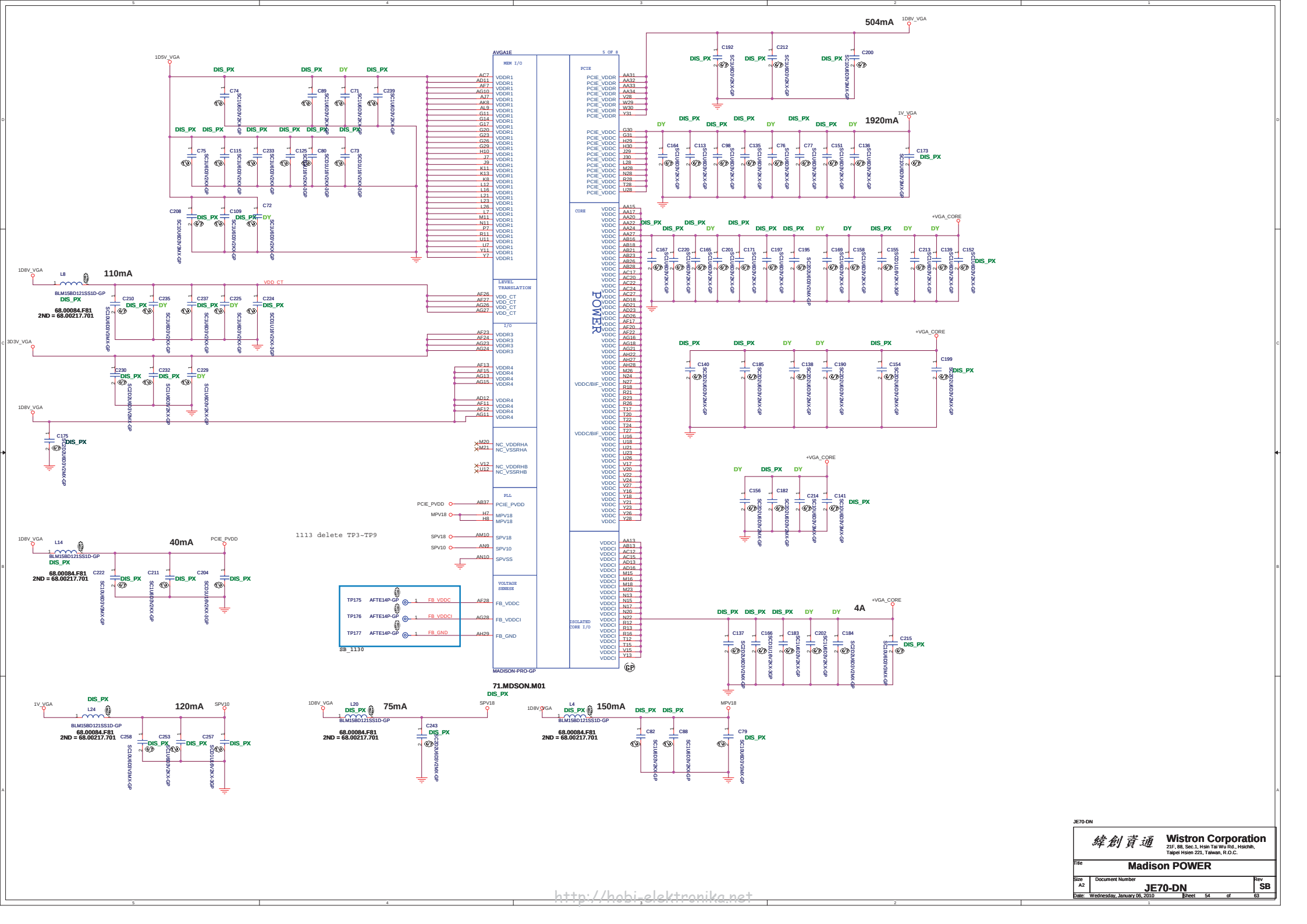
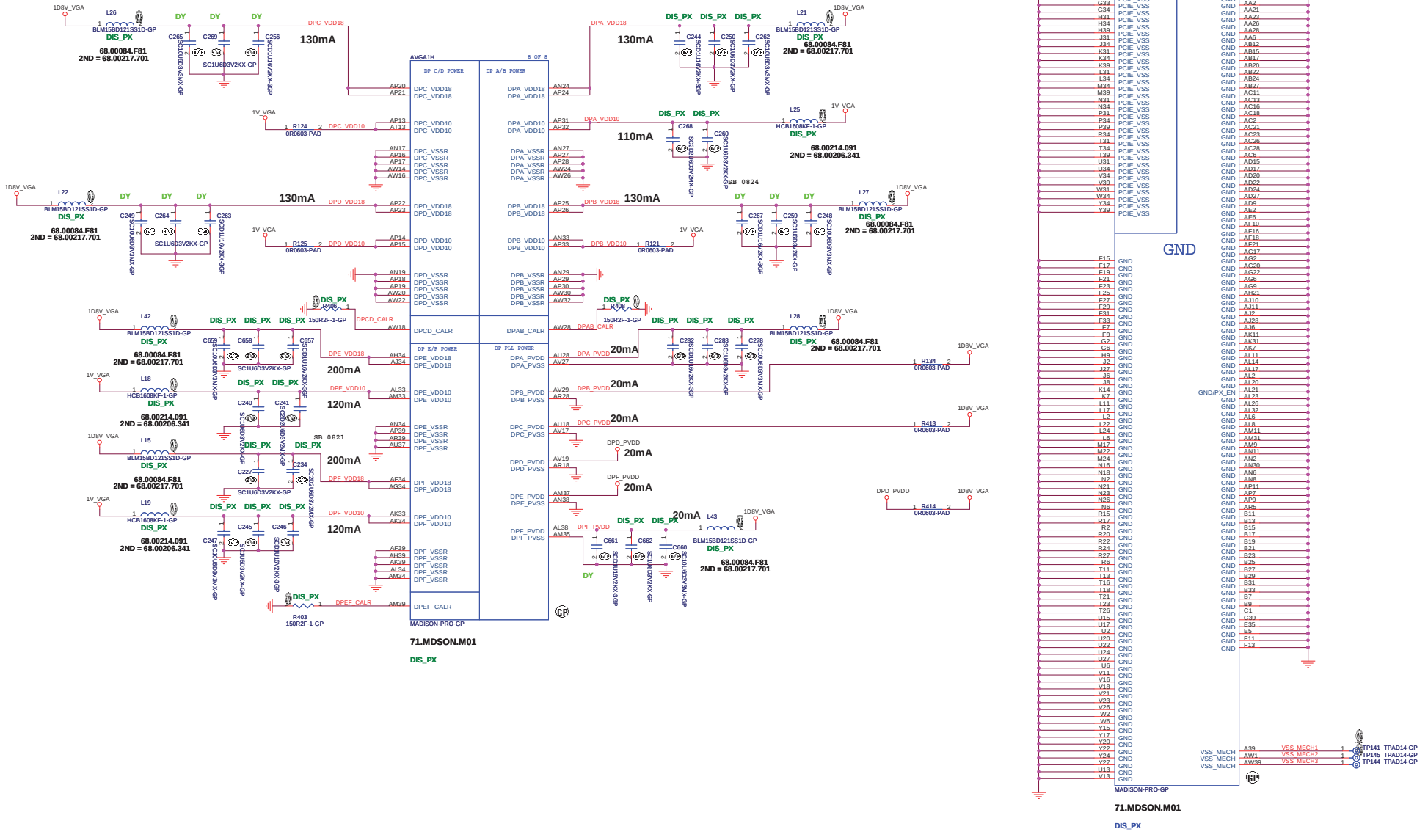

504mA
1920mA
110mA
40mA
120mA
75mA
150mA
4A
1113 delete TP3~TP9
71.MDSON.M01
MADISON-PRO-GP
POWER
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Madison POWER
JE70-DN
Wednesday, January 06, 2010
http://hobi-elektronika.net



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Title: DP POWER_GND

Size	Document Number	Rev
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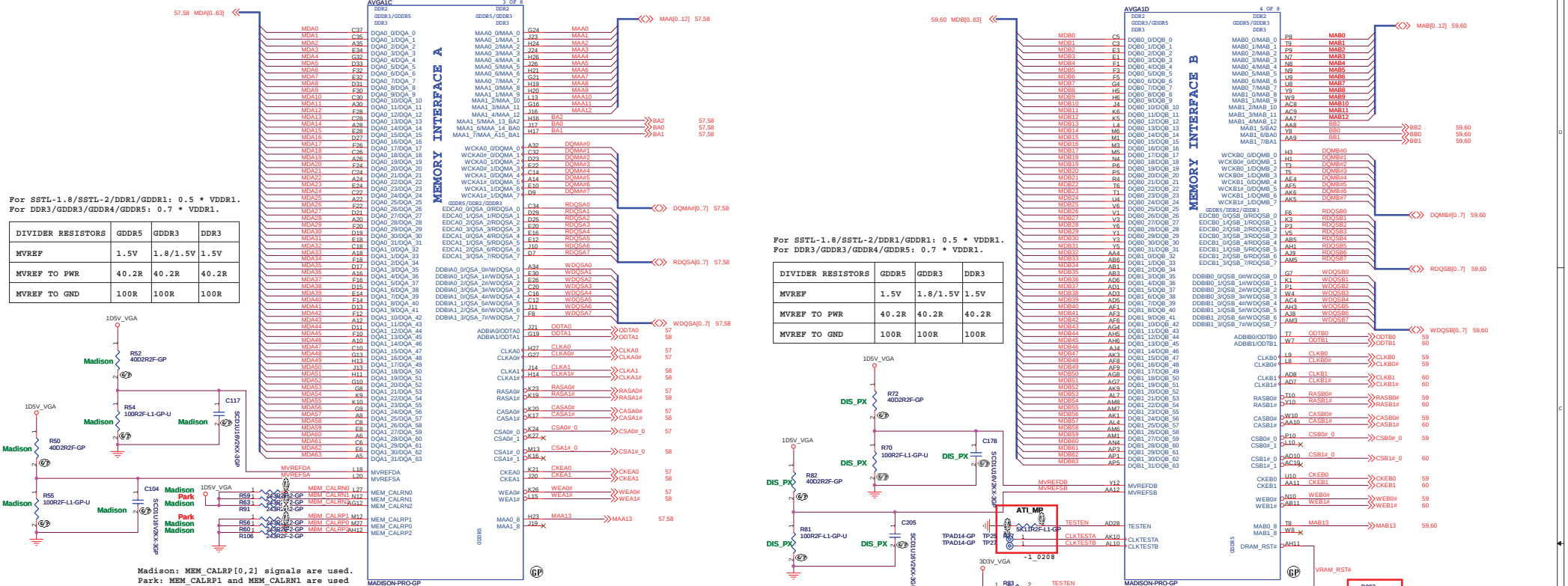
Date: Tuesday, February 23, 2010 Sheet 55 of 63



DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R

Designator	For M97-M2	For Mannhatton
R_MEM_1	10K	10K
R_MEM_2	40R/Short	680R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	X
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC, GPIO2, GPIO21

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V 128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

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Title: Madison Memory / Straps

Size: Custom | Document Number: JE70-DN | Rev: SB

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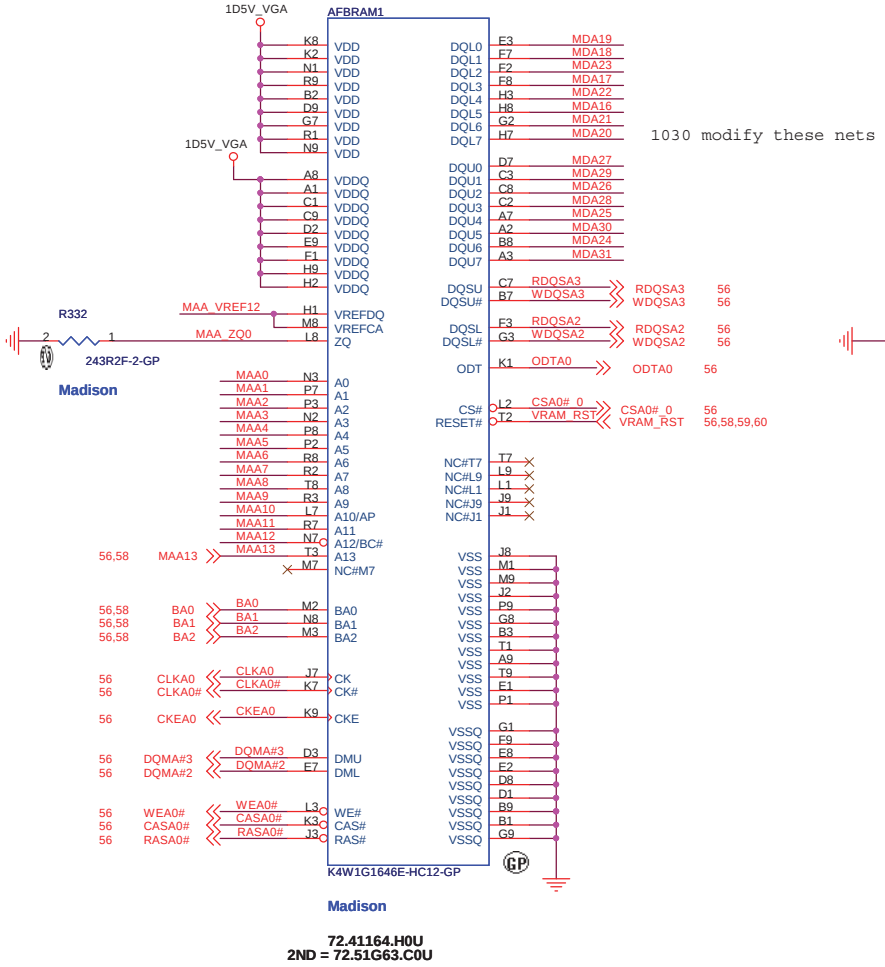
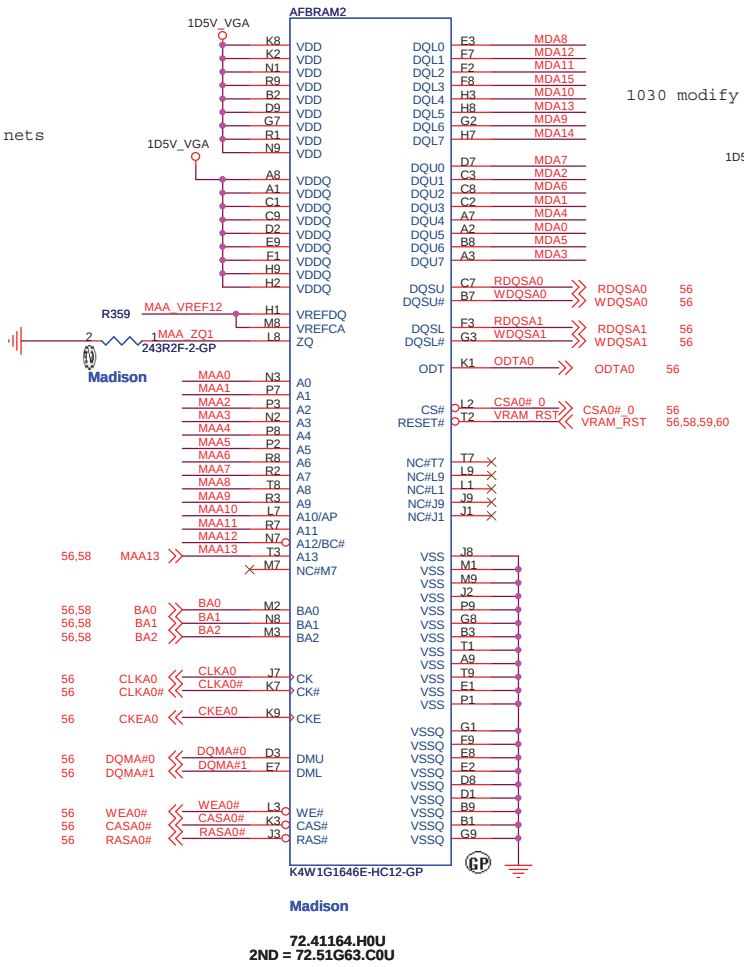
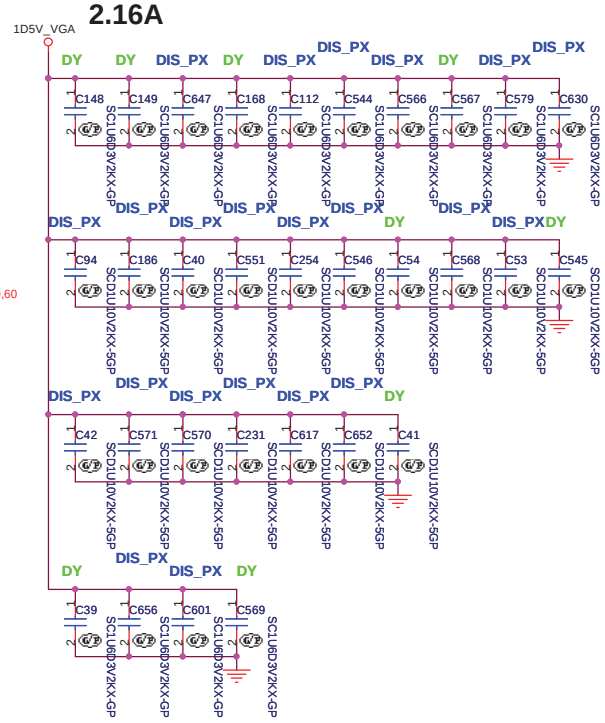
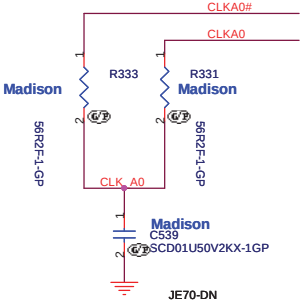
DDR3

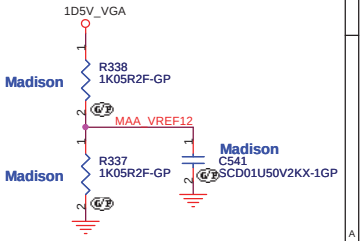






SAMSUNG: 72.41164.H0U(VR.1GB0B.006)
HYNIX: 72.51G63.C0U(VR.1GB0G.004)





56,58 DQMA#[0..7]

56,58 RDQSA[0..7]

56,58 WDQSA[0..7]

56,58 MAA[0..12] MAA[0..12]

56,58 MDA[0..63] MDA[0..63]

JE70-DN

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *VRAM(1/4)*		
Size: A3	Document Number: JE70-DN	Rev: SB
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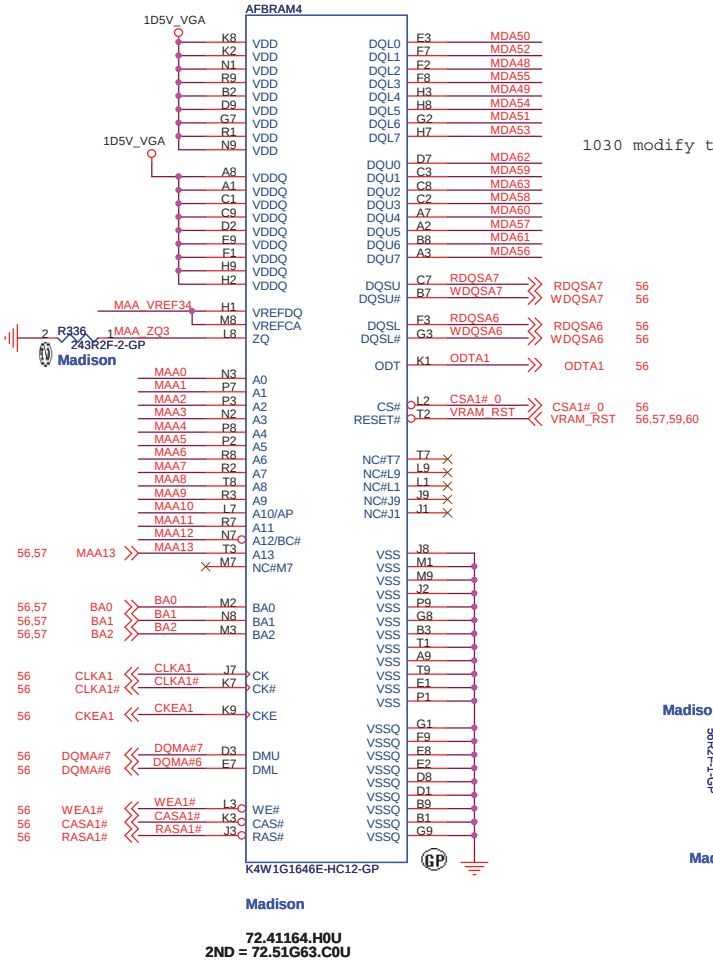
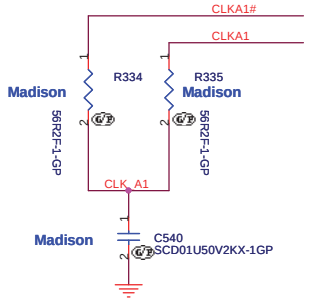
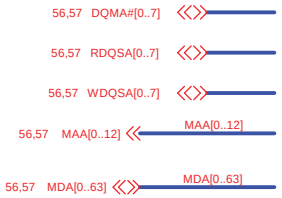
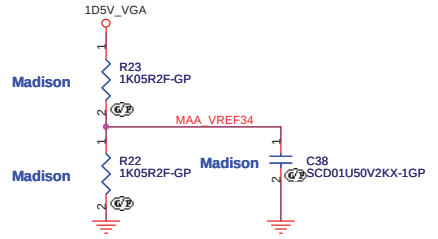
DDR3





SAMSUNG: 72.41164.H0U(VR.1GB0B.006)
HYNIX: 72.51G63.C0U(VR.1GB0G.004)





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Title: VRAM(2/4)

Size	Document Number	Rev
A3	JE70-DN	SB

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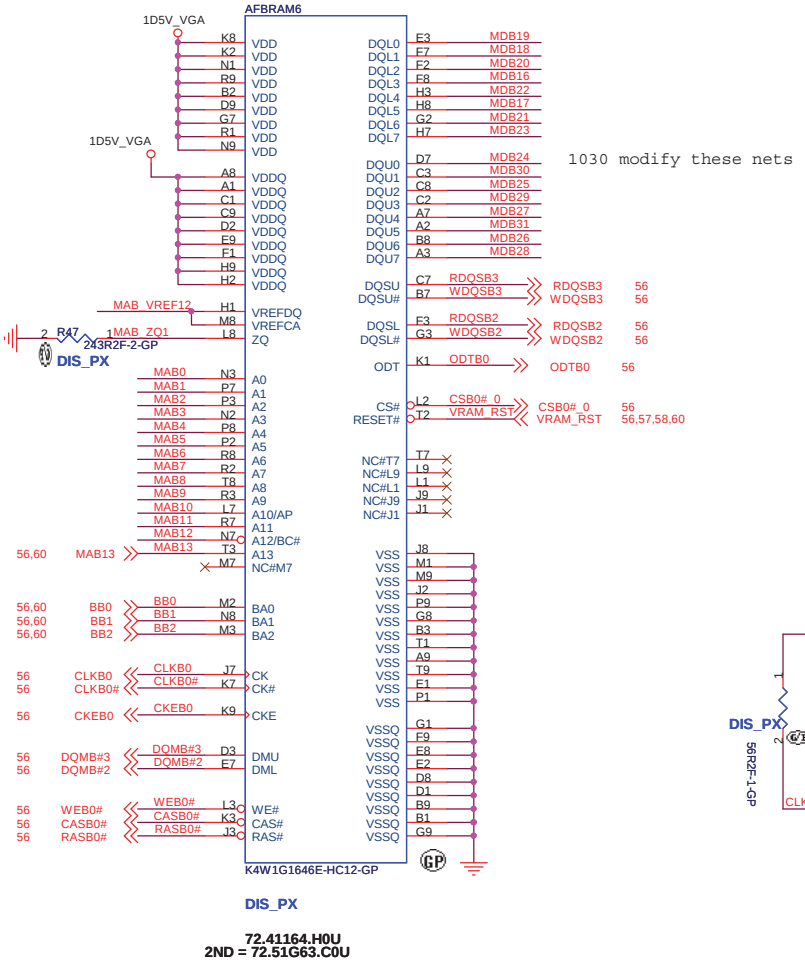
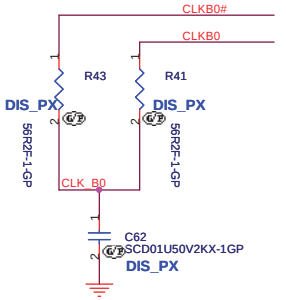
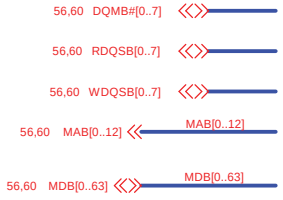
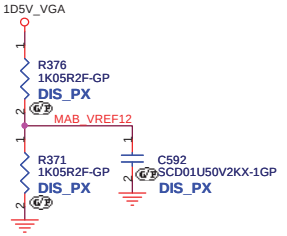
DDR3





SAMSUNG: 72.41164.H0U(VR.1GB0B.006)
HYNIX: 72.51G63.C0U(VR.1GB0G.004)





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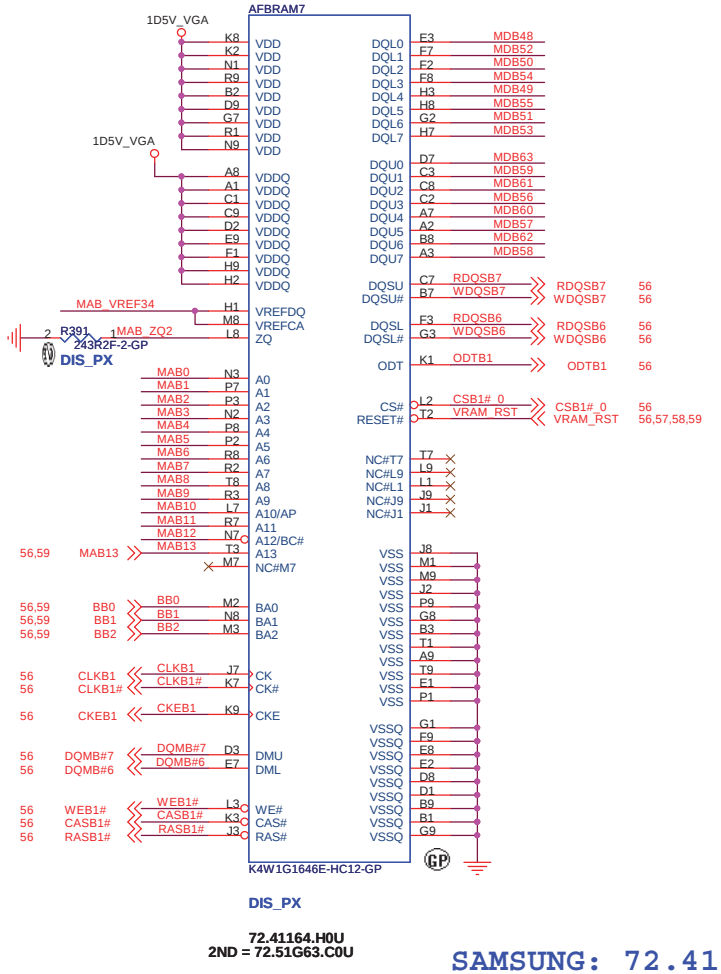
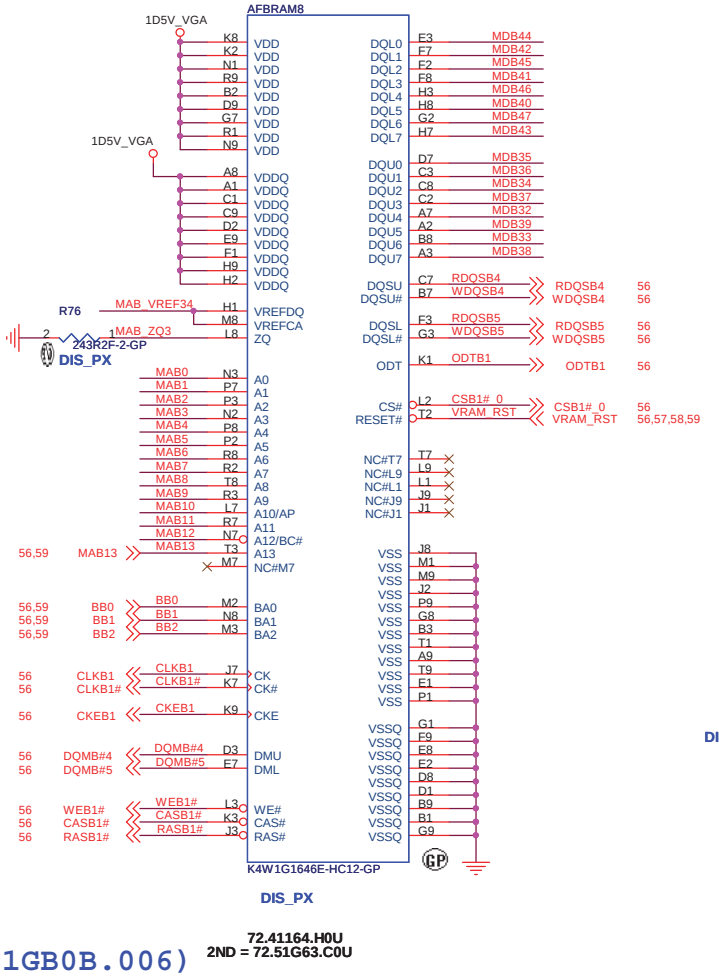
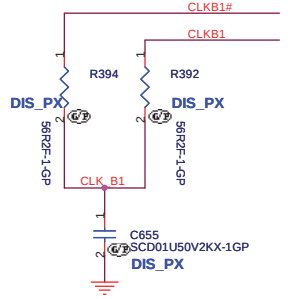
Title: VRAM(3/4)		
Size: A3	Document Number: JE70-DN	Rev: SB
Date: Tuesday, February 23, 2010	Sheet 59 of 63	

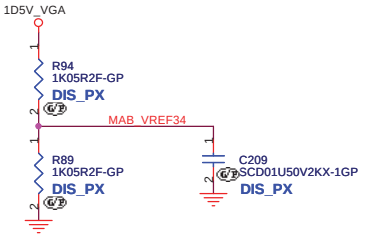
DDR3





SAMSUNG: 72.41164.H0U(VR.1GB0B.006)
HYNIX: 72.51G63.C0U(VR.1GB0G.004)





56,59 DQMB#[0..7]
56,59 RDQSB[0..7]
56,59 WDQSB[0..7]
56,59 MAB[0..12] MAB[0..12]
56,59 MDB[0..63] MDB[0..63]

JE70-DN

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *VRAM(4/4)*

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A3	JE70-DN	SB

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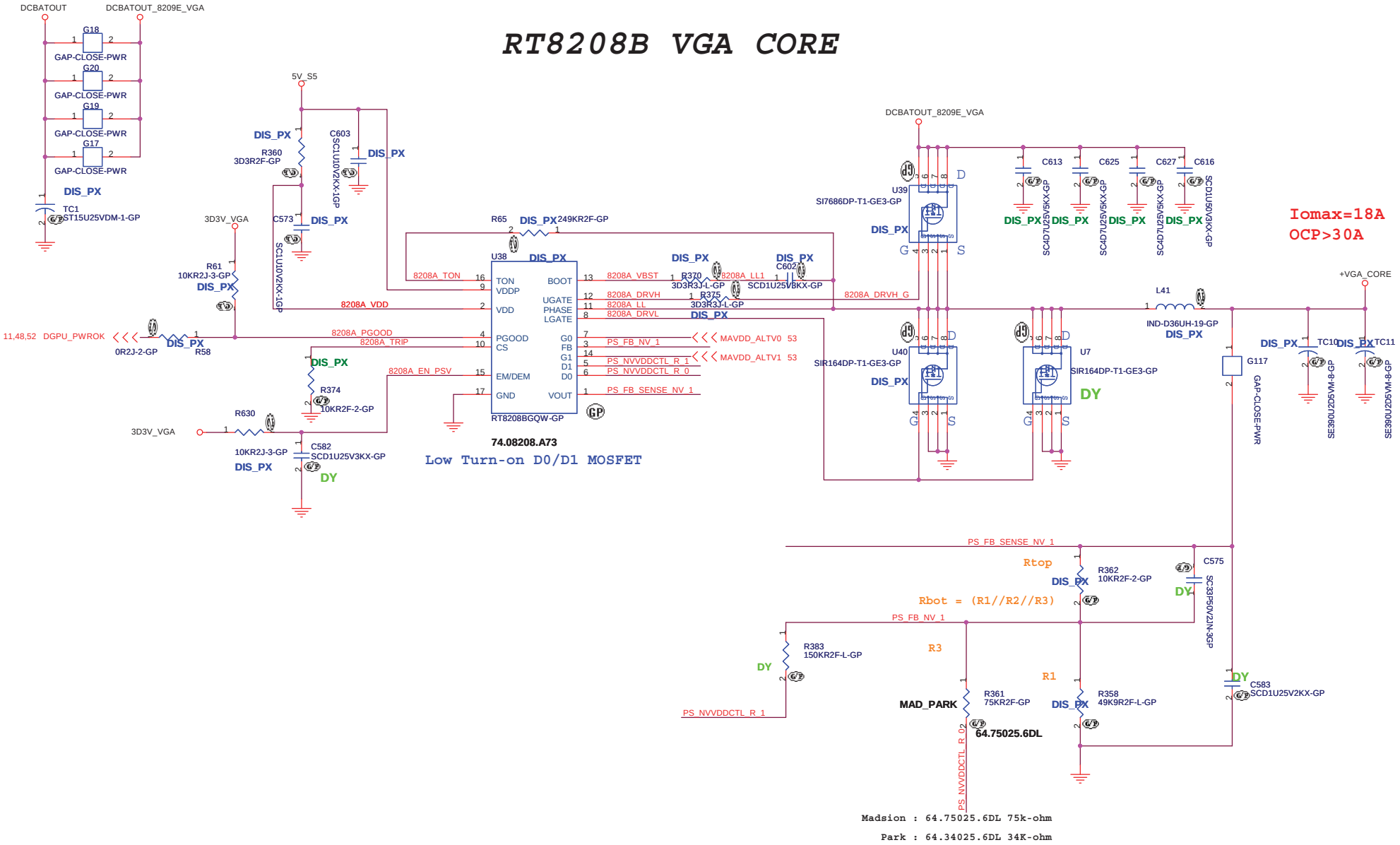
RT8208B VGA CORE



MAVDD_ALTV0	Madison Pro	Park XT
0	1.00V	1.12V
1	0.90V	0.90V

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Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8209E_VGA_CORE

Size: A3 | Document Number: JE70-DN | Rev: SB

Date: Monday, March 01, 2010 | Sheet 61 of 63

1020

Page8: modify these nets for PCIE ports
Page11:add these nets(INT_VGA_EN#,EDP_EN)
Page11:add the net(PX_EN#) and R861
Page11:delete D41,R437,R435
Page12:modify these nets for USB ports
Page14:modify L45,L48,L52,L57,L58,L60
Page18:delete RN95,R423 and add Q73~Q76,R862~R864,D45
Page19:delete CCD1 conn and modify these nets for CCD
Page19:add R865,R866,U100
Page20:add Q77,R867
Page24:add modify these nets for BT
Page25:add modify these nets for USB board
Page26:modify these nets for PCIE port(LAN)
Page26:delete the net(LOW_PWR)
Page33:modify these nets for PCIE ports(MINI1,MINI2)
Page33:modify these part's names
Page33:modify these nets for USB port(MINI2)
Page40:1020 modify PWR_LED1,CHARGER_LED1
Page51:add screw holes

1021

Page5:modify these nets
Page6:delete HDT1 conn and add TP246~255
Page16:modify these nets of ADM1
Page16:add R880~883
Page17:modify these nets of ADM2 and ADM3
Page17:add R884~R891
Page18:add RN114~117
Page23:modify ODD1
Page25:modify the net(COVER_SW#_1)
Page30:modify LOUT1,AMIC1 and MICIN1
Page33:modify AMINI1 and MINI2
Page36:modify these nets and add R873~878
Page38:modify these devices(ATPCN1,SW_R,SW_L)
Page40:modify PWR_LED1,CHARGER_LED1
Page49:add D46
Page50:modify DCIN1, BAT1 and add R879

1021

Page26:modify U6(LAN IC)

1023

Page12:delete R538,R539 and add RN118
Page12:delete R442,R443,R445 and add RN119
Page12:delete R570~R572 and add RN120
Page12:delete C368~C371,C446,C449,C686,C687
Page18:swap these nets
Page21:add R892~R900,Q78
Page25:delete TC29,TC24,EC79,EC83
Page25:modify the net of USBCN1 pin32
Page36:delete R258 and RN89,RN122
Page36:delete R382 and add U101
Page36:delete R892,R483,R497,R478 and add RN123
Page36:delete R410,R416 and add RN121,R892
Page37:add R901,R902
Page40:modify the pin5 define of PWR_CN1 and Q11
Page43:add TC53,TC54,U44
Page61:modify TC52, R295 and add R903,Q79

1026

Page3: add R904 and modify C509,R232,R235
Page6: add R913,RN124
Page6: modify RN42,RN84,R612,R611,R364
Page17:modify these nets
Page19:modify R588
Page21:modify U73 and delete R504
Page22:modify SATA1
Page35:delete R311 and modify FAN1
Page36:modify RN121
Page36:modify AKB1
Page37:modify RN94 and the net(SPI_WP#)
Page43:add R097~R911,D47,Q80
Page53:add R905,R906

1027

Page10:delete C651,R320,R316
Page11:modify C543,C306,C424,C433
Page11:delete R148
Page12:modify the net(PM_RSMRST#)
Page43:modify the net(PM_RSMRST#)

1028

Page3:add the net(LAN_CLKREQ#)to RN70
Page4:modify C704~C706
Page4:modify R401
Page9:delete R576,R578
Page10:modify C62,C91
Page11:delete R207,C337,D5,R208
Page11:delete the net(PCI_REQ#6)
Page12:delete RN120 and add R570
Page13:modify the net(SATA_LED#)
Page14:add C1198,C1199 and modify C815,C811
Page16:add R934,R935
Page18:add U102,R915~R919
Page18:modify R432,U3,U8
Page19:add U103,R920~R922 and delete D35
Page20:add R936,R937 and modify R325,R323,R354
Page21:delete RN8,RN13,RN15,RN19
Page21:modify C819~C821,C823,C824,C826~C828
Page25:add L82,R924,R925
Page29:modify R489
Page30:modify R622,R619 and add RN125
Page36:delete R384 and modify the net(KBC_BL_ON_IN)
Page36:add R926
Page43:delete R583,D33,U74,R340,Q34,R584
Page43:add R930~R933,Q84,Q85,C1197
Page43:add R927~R929,Q8~Q83
Page43:delete R591~R595
Page48:modify these nets(DGPU_PWROK,9025_POK)

1029

Page6:delete R364,R612 and add RN127,R946
Page16:delete C331,C338
Page17:delete C348,C340,C350,C342
Page18:modify these nets
Page19:add EC99,EC100
Page24:add EC101,EC102
Page25:add L82,R924,R925,R939,EC103
Page35:delete D17,D18,U39,U43,R298,R322,R330,R338,R337,C646,C656
Page35:delete U38,R321,R308,R309,R314,C645
Page36:add R945,RN126
Page43:delete U44,R342,C675
Page47:modify the net
Page48:modify R582 and add R938
Page50:add D48
Page53:add R940~R943
Page61:add R944,Q86

1030

Page3:modify these nets
Page8:modify these nets
Page11:modify the net
Page12:add R949
Page14:delete C760,C721,C805,C800,C769,L64 and add R948
Page18:modify these nets
Page30:add R950~R953 and modify EC24,EC51
Page57:swap these nets
Page58:swap these nets
Page59:swap these nets
Page60:swap these nets

1102

Page3:swap these nets
Page6:swap these nets
Page12:swap these nets
Page13:swap these nets
Page18:swap these nets
Page25:modify USBCN1
Page30:modify these names of these nets

1103

Page3:modify X5,C508,C509
Page11:modify R164
Page14:modify L51,L59
Page21:modify these names of nets
Page21:add RN8,RN13,RN15,RN19
Page36:add the net(A_MIC_SUPPORT#)

1104

Page6:delete TP246~255 and add HDT1
Page9:modify the value of RN11
Page24:add AFTP(TP256~TP258)
Page24:add AFTP(TP259~TP263)
Page25:add AFTP(TP264~TP280)
Page35:add AFTP(TP281,TP282)
Page36:add AFTP(TP283~TP307)
Page38:add AFTP(TP308~TP312)
Page40:add AFTP(TP313~TP319)
Page56:modify these values of R724,R725

1105

Page3:delete R191~R194,R198~R200,R204~R206
Page3:delete R214,R213,R187~R190,R220,R222
Page3:add RN128~RN136
Page3:modify R215,R197,R238,R229
Page6:delete R104,R105,R108,R110
Page6:add RN137,RN138,R954
Page6:modify R366
Page6:modify Q8,R81,R375,C205
Page8:delete TP16,TP17,TP20,TP21
Page9:add R955,R956 and modify R29
Page11:delete R144,R141,R137,R138
Page12:add the net(SUS_STAT#) and R957
Page12:modify these nets
Page21:swap these nets
Page28:modify C713,R634 and delete R626
Page33:modify these nets
Page33:modify R879

1106

Page3:modify these values of R169,R170
Page12:add R957,R958
Page12:add these nets(USB_OC#0,USB_OC#2,USB_OC#3)
Page16:modify R880~R883,ADM1
Page17:modify R888,R890,ADM2
Page21:add R959
Page35:modify FAN1
Page35:modify PWR_CN1
Page35:modify ATPCN1
Page36:swap these nets(KBRCIN#,KA20GATE)
Page37:swap RN94
Page44:swap RN45
Page51:add EC104~EC112 for EMI demand

1107

Page3:swap RN129,RN130,RN132
Page6:swap RN137
Page51:add EC104~EC112 for EMI demand

1109

Page45:modify the value of R448 to 64.15035.6DL for Power team demand
Page45:modify R462,R470 for Power team demand
Page46:modify L25 for Power team demand
Page48:modify C1032,C1194

1110

Page5:swap RN48
Page7:add C1200~C1207
Page11:add R960,R961
Page25:modify USB1
Page43:add TC55,TC56
Page52:add R962

1111

Page11:add R965
Page21:modify HDMI1
Page28:add R626
Page33:delete C550,C549 and add R963
Page36:delete RN121 and add R964
Page45:modify TC39,TC40
Page48:add R966,Q87,C1208,R967,R968,Q88

1112

Page13:modify the net
Page48:delete R968,Q88
Page48:modify R819,R820,R966
Page48:modify the net

1113

Page3:delete R170,EC50
Page25:delete R939,TP272,EC103
Page46:modify TC43
Page48:add R969
Page53:add R968
Page53:delete TP103,TP122,TP160,TP178
Page53:delete these TP(TP157,TP145...)
Page54:delete TP3~TP9

1117(Rename)

Page18:swap these nets
Page22:delete D29~D31,D33
Page36:modify RN31
Page61:delete G24~G29
Page61:modify the net

1118

Page14:add R620 and modify R184
Page15:modify R412,R411
Page36:swap AKB1 pin1~pin26

JE70-DN

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1120

Page19: modify these nets
Page48: modify the net(9025_EN)

1124

Page38: modify ATPCN1

1126

Page25: modify these nets
Page36: add TP174

JE70-DN

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Title: *HISTORY(2/2)*

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