Compal Confidential

QAWGH Schematics Document

AMD APU Trinity FS1r2 + FCH Hudson-M3 + GPU Seymourr XT

2011-10-07

REV:0.1

Security Classification	Compal Secret Data		
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ZZZ
LA8611P
DA_PCB
DA80000S600

QAWGH

LS7986P CardReader/B
LS7982P USB/B
LS7983P PWR/B
LS8612P LED/B
LS7985P ODD/B
LS8617P Cap Sensor/B

AMD Seymour XT
VRAM
64M16/128M16
DDR3 x 4
page 17 ~ 23

PCIE x 16 Gen2

AMD FS1r2 APU
Trinity
uPGA 722 pin
35mm x 35mm
page 5,~9

Memory BUS(DDRIII)
Dual Channel
1.5V DDRIII 1866

204pin DDRIII-SO-DIMM X2
BANK 0, 1, 2
page 10,11

LVDS translator
RTDS2132S
page 24

DP Port0

HDMI Conn.
page 26

DP Port2

DP Port1

LVDS Conn.
page 25

4 * x1 PCI-E 2.0

x4 UMI Gen. 1
2.5GT/s per lane

GPP1

GPP0

LAN
AR8161/8162
page 28~29

Hudson M3
uFCBGA-656
24.5mm x 24.5mm
page 12~16

AZALIA

Audio Codec
CX20671-21Z
page 30

2Channel Speaker
page 30

Internal MIC
page 30

Audio Jacks
Sub-board

PCI Express
Mini Card Slot 1
WLAN/WiMAX
page 32

USB(WiMAX)

CRT Conn.
page 27

FCH CRT (VGA DAC)

4 * x1 PCI-E 2.0

4*USB3.0,10*USB2.0

6*SATA serial

CMOS Camera
page 25

BlueTooth Conn
page 31

USB Port 3.0 x2(Left)
page 37,38

USB Port 2.0 x 1 (Right)
Sub-board

Card Reader
RTS5178
USB 2.0 x 1
Sub-board

2 in 1 Conn.
SD/SDXC/MMC

SPI ROM
page 13

LPC Bus

Cap Sensor
Sub-board

EC
ENE KB930/ KB9012
page 34

Touch Pad
page 35

Int. KBD
page 35

SATA0

SATA 3.0 HDD Conn.
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SATA1

SATA ODD Conn.
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Thermal Sensor
EMC1403
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Title: Block Diagrams

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+1.5V	1.5V power rail for APU VDDIO and DDR	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.2VS	1.2V (VDDR, VDDP) switched power rail for APU	ON	OFF	OFF
+2.5VS	2.5V for APU VDDA	ON	OFF	OFF
+1.1VALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VGS	1.5V switched power rail	ON	OFF	OFF
+1.8VGS	1.8V switched power rail	ON	OFF	OFF
+1.0VGS	1.0V switched power rail for VGA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

FCH Hudson-M2/3 SATA Port List

SATA0	NC
SATA1	HDD
SATA2	ODD
SATA3	NC
SATA4	NC
SATA5	NC

Comal PCIE Port List

APU	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	NC
	PCIE3	NC
FCH	PCIE0	NC
	PCIE1	NC
	PCIE2	NC
	PCIE3	NC

FCH Hudson-M2/3 USB Port List

USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	Right USB1
Port1	Right USB2
Port2	Mini PCIE
Port3	USB Camera
Port4	BT
Port5	Card Reader
Port6	NC
Port7	NC
Port8	NC
Port9	NC
Port10	USB3.0 LP1
Port11	USB3.0 LP2
Port12	NC
Port13	NC

FCH Hudson-M2/3 USB OC PIN

USB_OC0#	USB3.0 (LP1, LP2)
USB_OC1#	USB2.0 (RP1)
USB_OC2#	USB2.0 (RP2)
USB_OC3#	NC
USB_OC4#	NC
USB_OC5#	NC
USB_OC6#	NC
USB_OC7#	NC

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001-011xb	15H

EC SM Bus2 address

Device	Address	HEX
EMC1403(VGA, DDR,WLAN)	1001-101xb	9AH
SB-TSI (default)	1001-100xb	98H
VGA Thermal	1000-001xb	82H
Cap Sensor	1000-0000b	80H
RTDS2132S-E	1010-1000b	A8H

SM Bus Controller 0

(FCH_SMB1 ~ FCH_SMB4, SMB_ALERT#)

Device	Address	HEX

SM Bus Controller 1

(FCH_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90H
DDR DIMM2 (FCH_SMB0)	1001-001xb	92H
WLAN (FCH_SMB0)		

BOM Structure

```
UMA@  : UMA only
PX@   : DIS muxluss
CMOS@ : USB camera
HDMI@ : HDMI function
nonHDMI@ : w/o HDMI function
BT@   : BT function
ME@   : ME components
X76@  : VRAM
45@   : 45 Level
PX4@  : PX4
PX5@  : PX5
8162@ : 10/100 LAN
GIGA@ : giga LAN
14@   : G 14"
15@   : G 15"
BBH@  : Best Buy high-end
nonBBH@ : non Best Buy high-end
AN@   : Apple & Nokia combo
A@    : Apple only
```


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Title: Notes List

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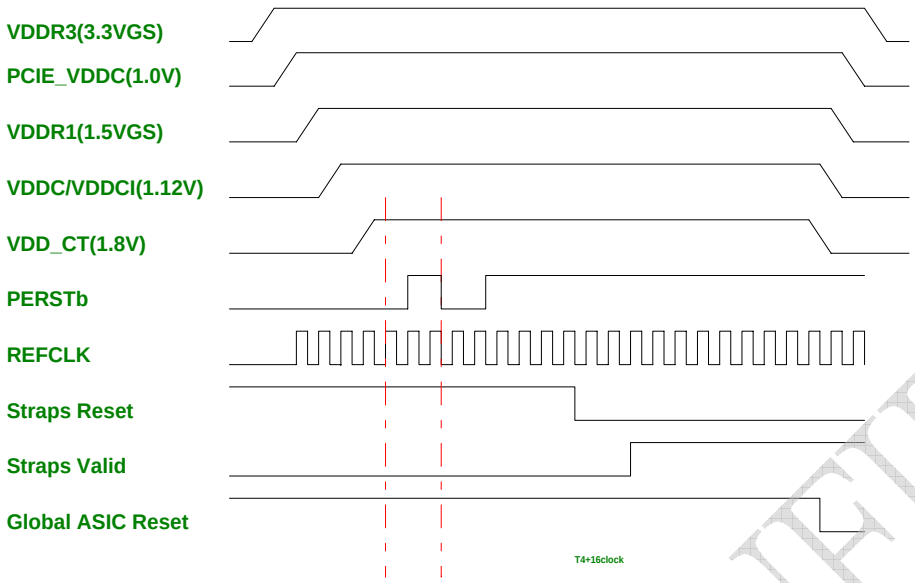
Power-Up/Down Sequence

"Seymour" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies, except for VDDR3, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. There is no timing requirement on the ramp up of VDDR3 relative to other power rails.
- The external pull-up resistors on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa). For BACO enabled designs, VDDC must ramp up before VDD_CT at system power up.
- For power down, reversing the ramp-up sequence is recommended



Without BACO option :

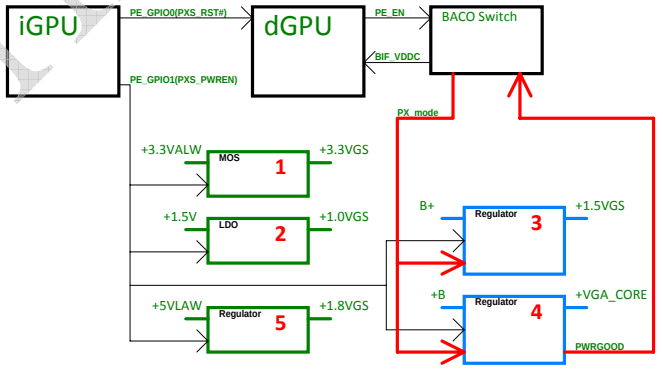
PE_GPIO0 (PXS_RST#) : Low -> Reset dGPU ; High ->Normal operation
PE_GPIO1 (PXS_PWREN) : Low -> dGPU Power OFF ; High -> dGPU Power ON

BACO option :

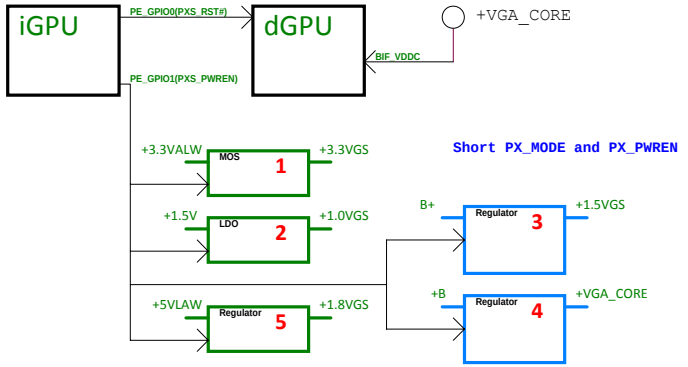
PE_GPIO0 (PXS_RST#) : High ->Normal operation (dGPU is not reset on BACO mode)
PE_GPIO1 (PXS_PWREN) : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	775mA
PCIE_VDDC	1.0V	OFF	ON	1.1A
VDDR3	3.3V	OFF	ON	60mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	1.2A
VDDC/VDDCI	TBD	OFF	OFF	28

PX4.0



PX5.0



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Title: **dGPU Notes List**

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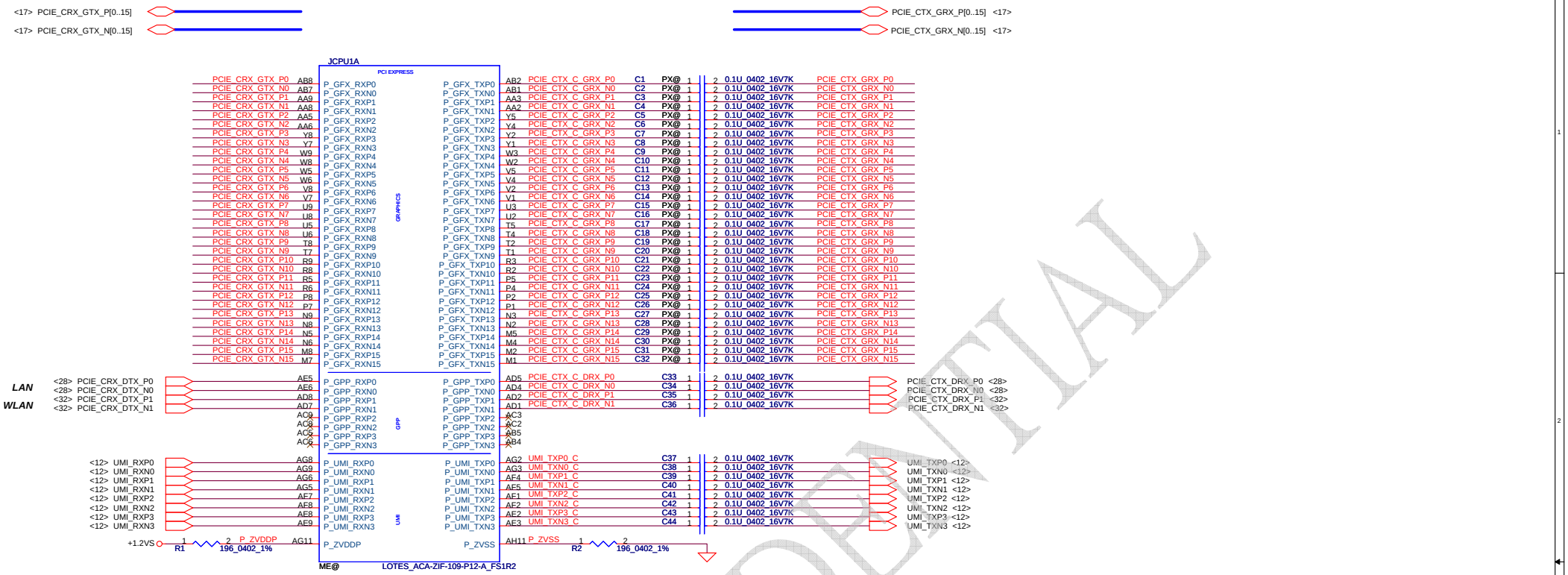
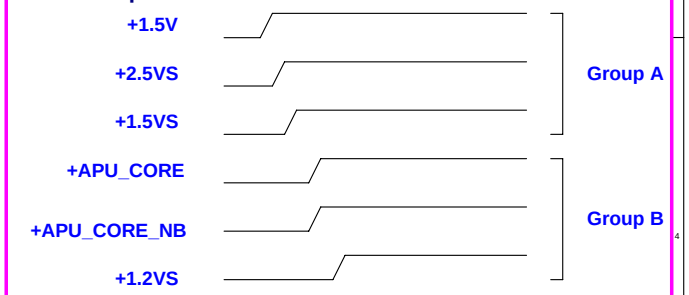


Power Sequence of APU



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: FS1r2 PCIE/UMI

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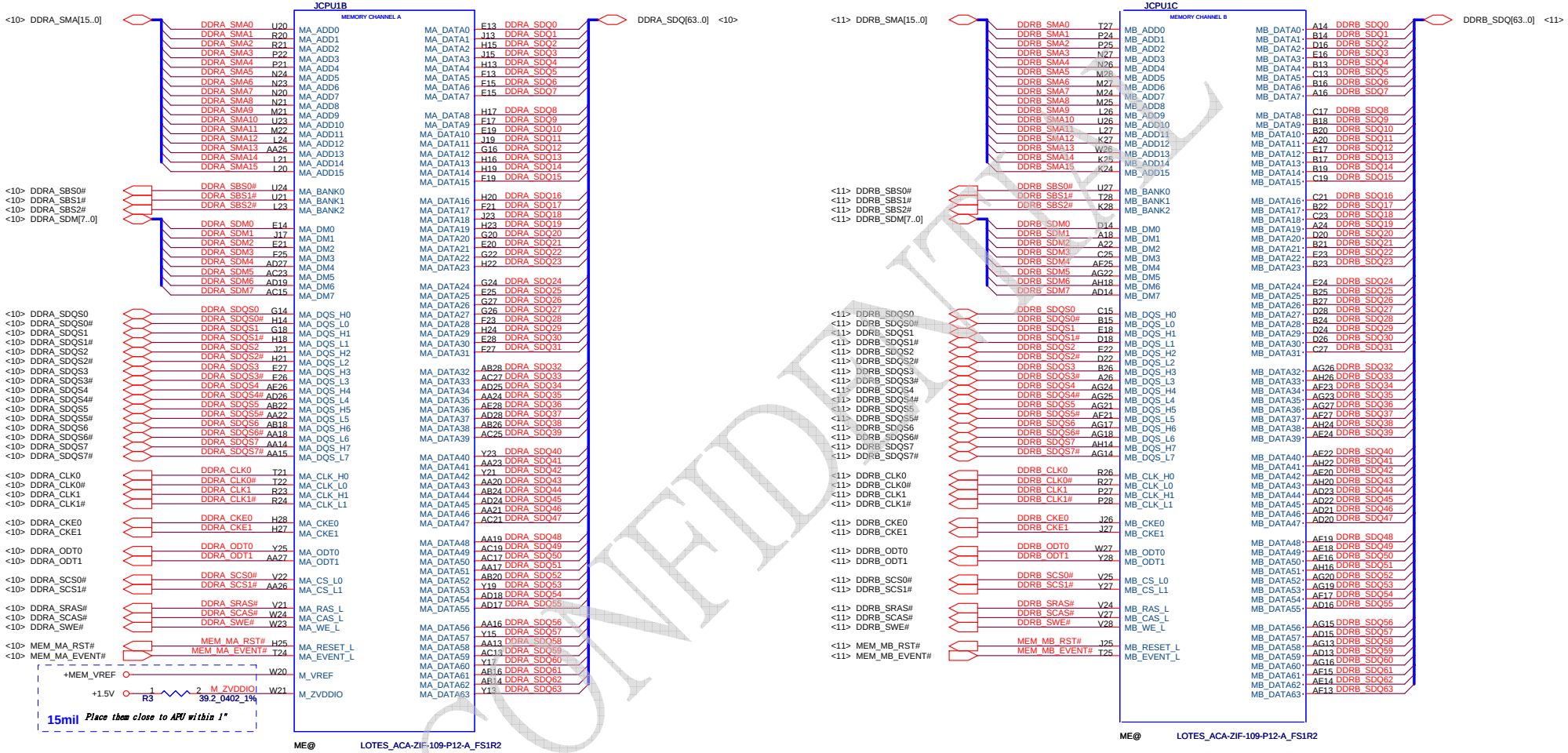

Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: FS1r2 DDRIII Memory I/F

Size	Document Number	Rev
Custom	LA8611P	0.1

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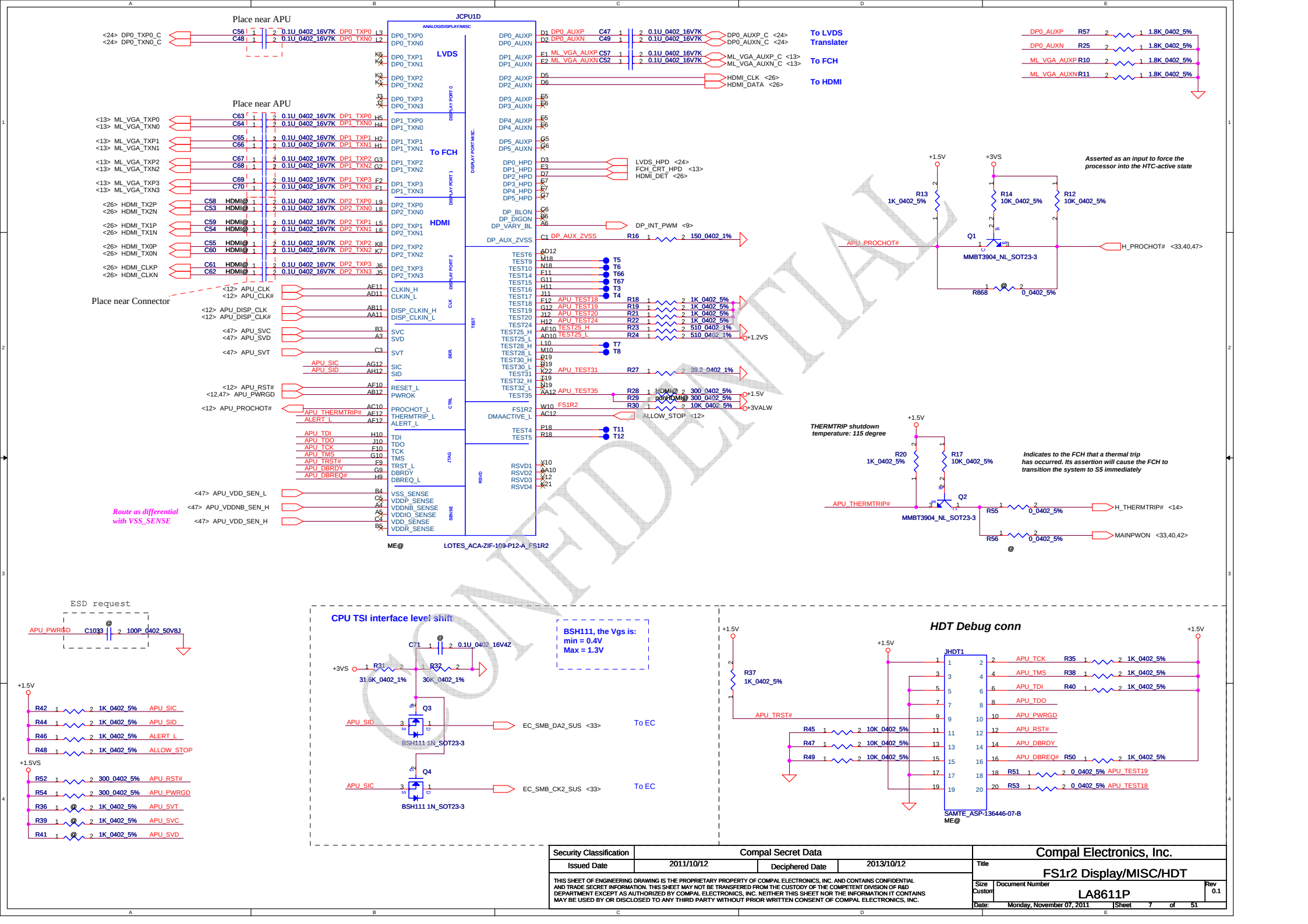

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Compal Electronics, Inc.	
Title	FS1r2 Display/MISC/HDT
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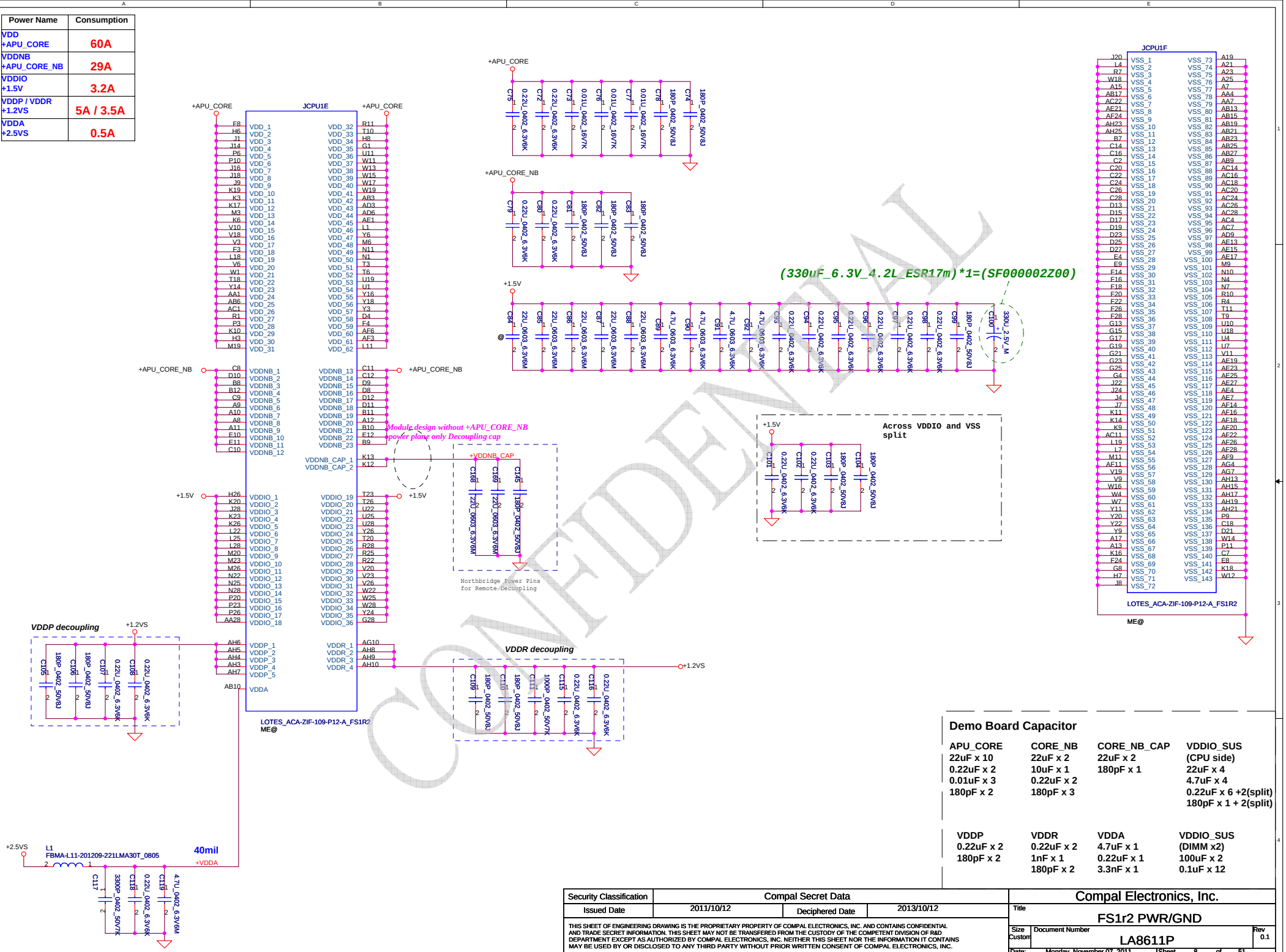
Power Name	Consumption
VDD +APU_CORE	60A
VDDNB +APU_CORE_NB	29A
VDDIO +1.5V	3.2A
VDDP / VDDR +1.2VS	5A / 3.5A
VDDA +2.5VS	0.5A



Demo Board Capacitor

APU_CORE	CORE_NB	CORE_NB_CAP	VDDIO_SUS
22uF x 10	22uF x 2	22uF x 2	(CPU side)
0.22uF x 2	10uF x 1	180pF x 1	22uF x 4
0.01uF x 3	0.22uF x 2		4.7uF x 4
180pF x 2	180pF x 3		0.22uF x 6 +2(split)
			180pF x 1 + 2(split)

VDDP	VDDR	VDDA	VDDIO_SUS
0.22uF x 2	0.22uF x 2	4.7uF x 1	(DIMM x2)
180pF x 2	1nF x 1	0.22uF x 1	100uF x 2
	180pF x 2	3.3nF x 1	0.1uF x 12

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Title: FS1r2 PWR/GND

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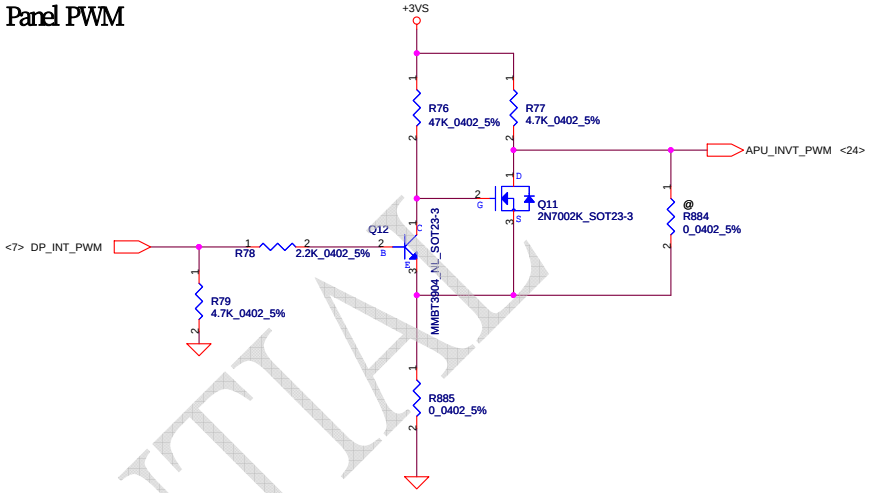
Panel PWM



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: FS1r2 Signal Level Shifter

Size	Document Number	Rev
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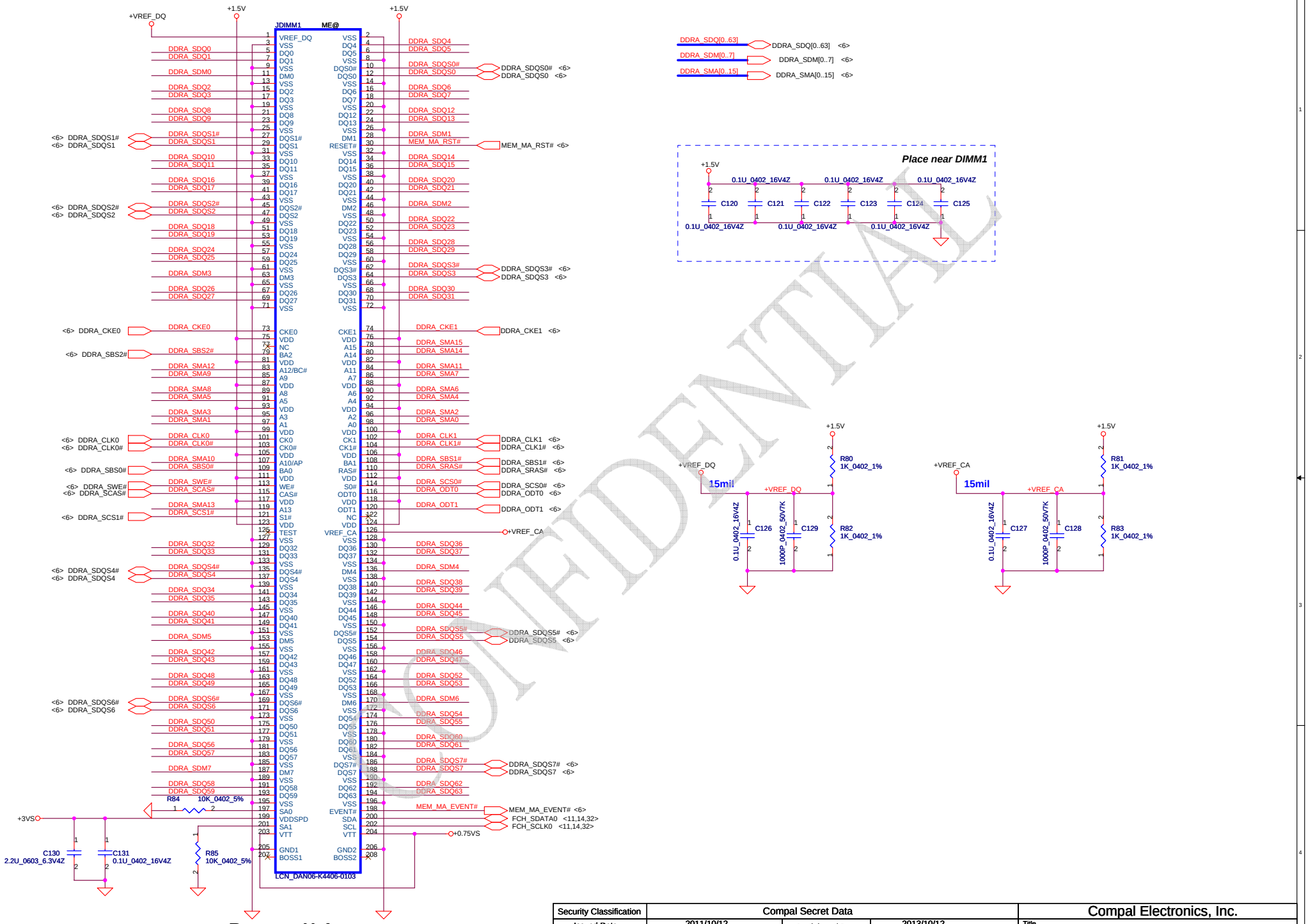

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Title: DDRIII SO-DIMM 1

Size	Document Number	Rev
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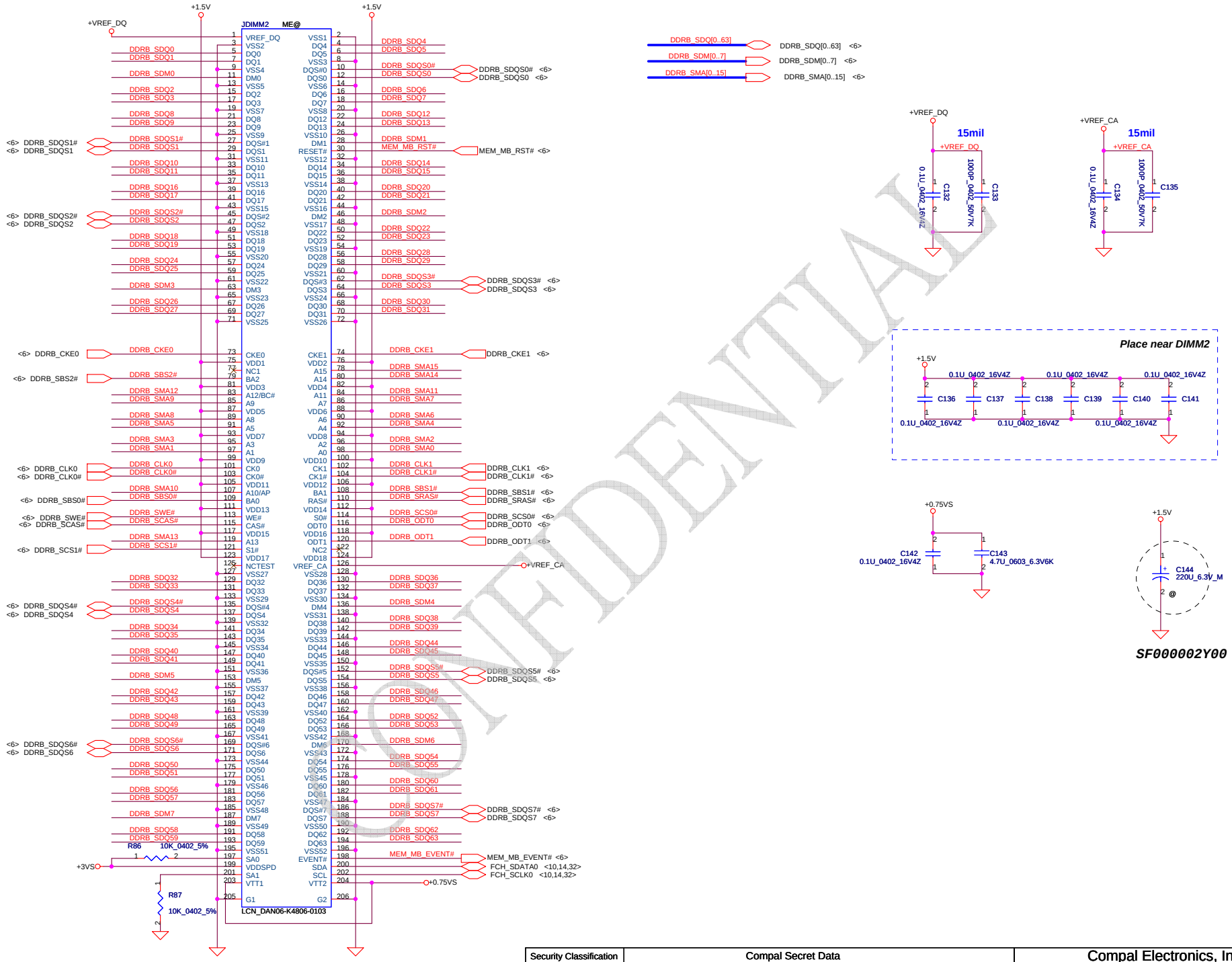

Reserve H:8mm

<Address: 01>

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: DDRIII SO-DIMM 2

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C146 place close to FCH

C146 1 2 150P_0402_50V8J

PLT_RST# 1 R89 2 33_0402_5% APU_PCIE_RST#_C A_RST#

U2A

HUDSON-2

PCIE_RST# AE2
A_RST# AD5

UMI_TX0P AE30
UMI_TX0N AE32
UMI_TX1P AD33
UMI_TX1N AD31
UMI_TX2P AD28
UMI_TX2N AD29
UMI_TX3P AC30
UMI_TX3N AC32

<5> UMI_RXP0 C147 1 2 0.1U_0402_16V7K UMI_RXP0_C
<5> UMI_RXN0 C148 1 2 0.1U_0402_16V7K UMI_RXN0_C
<5> UMI_RXP1 C149 1 2 0.1U_0402_16V7K UMI_RXP1_C
<5> UMI_RXN1 C150 1 2 0.1U_0402_16V7K UMI_RXN1_C
<5> UMI_RXP2 C151 1 2 0.1U_0402_16V7K UMI_RXP2_C
<5> UMI_RXN2 C152 1 2 0.1U_0402_16V7K UMI_RXN2_C
<5> UMI_RXP3 C153 1 2 0.1U_0402_16V7K UMI_RXP3_C
<5> UMI_RXN3 C154 1 2 0.1U_0402_16V7K UMI_RXN3_C

UMI_RX0P AB33
UMI_RX0N AB31
UMI_RX1P AB28
UMI_RX1N AB29
UMI_RX2P Y33
UMI_RX2N Y31
UMI_RX3P Y28
UMI_RX3N Y29

<5> UMI_TXP0
<5> UMI_TXN0
<5> UMI_TXP1
<5> UMI_TXN1
<5> UMI_TXP2
<5> UMI_TXN2
<5> UMI_TXP3
<5> UMI_TXN3

PCI EXPRESS INTERFACES

+VDDAN_11_PCIE

R94 1 2 590_0402_1% PCIE_CALRP AE29
R88 1 2 2K_0402_1% PCIE_CALRN AE31

PCIE_CALRP
PCIE_CALRN

GPP_TX0P V33
GPP_TX0N V31
GPP_TX1P W30
GPP_TX1N W32
GPP_TX2P AB26
GPP_TX2N AB27
GPP_TX3P AA24
GPP_TX3N AA23

GPP_RX0P AA27
GPP_RX0N AA26
GPP_RX1P W27
GPP_RX1N V27
GPP_RX2P V26
GPP_RX2N W26
GPP_RX3P W24
GPP_RX3N W23

+1.1VS_CKVDD

R95 1 2 2K_0402_1% CLK_CALRN F27

CLK_CALRN

PCIE_RCLKP G30
PCIE_RCLKN G28

<7> APU_DISP_CLK R26 DISP_CLKP
<7> APU_DISP_CLK# T26 DISP_CLKN

DISP2_CLKP H33
DISP2_CLKN H31

<7> APU_CLK T24 APU_CLKP
<7> APU_CLK# T23 APU_CLKN

<17> CLK_PCIE_VGA R98 1 PX@ 2 0_0402_5% CLK_PCIE_VGA_R J30 SLT_GFX_CLKP
<17> CLK_PCIE_VGA# R99 1 PX@ 2 0_0402_5% CLK_PCIE_VGA#_R K29 SLT_GFX_CLKN

GPP_CLK0P H27
GPP_CLK0N H28

GPP_CLK1P J27
GPP_CLK1N K26

WLAN

<32> CLK_PCIE_WLAN R102 1 2 0_0402_5% CLK_PCIE_WLAN_R F33 GPP_CLK2P
<32> CLK_PCIE_WLAN# R103 1 2 0_0402_5% CLK_PCIE_WLAN#_R F31 GPP_CLK2N

LAN

<28> CLK_PCIE_LAN R100 1 2 0_0402_5% CLK_PCIE_LAN_R E33 GPP_CLK3P
<28> CLK_PCIE_LAN# R101 1 2 0_0402_5% CLK_PCIE_LAN#_R E31 GPP_CLK3N

GPP_CLK4P M23
GPP_CLK4N M24

GPP_CLK5P M27
GPP_CLK5N M26

GPP_CLK6P N25
GPP_CLK6N N26

GPP_CLK7P R23
GPP_CLK7N R24

GPP_CLK8P N27
GPP_CLK8N R27

CLOCK GENERATOR

<28> CLK_LAN_48M R680 1 @ 2 22_0402_5% CLK_LAN_25M_R J26 14M_25M_48M_OSC

25M_X1 C31 25M_X1

25M_X2 C33 25M_X2

21807-A13-HUDSON-M3_FCBGA656

PCI CLKS

PCICLK0 AF3 PCI_CLK1 <16>
PCICLK1/GPO36 AF1
PCICLK2/GPO37 AF5 PCI_CLK3 <16>
PCICLK3/GPO38 AG2 PCI_CLK4 <16>
PCICLK4/14M_OSC/GPO39 AF6

PCIRST# AB5

PCI INTERFACE

AD0/GPIO0 AJ3
AD1/GPIO1 AL5
AD2/GPIO2 AG4
AD3/GPIO3 AL6
AD4/GPIO4 AH3
AD5/GPIO5 AJ5
AD6/GPIO6 AL1
AD7/GPIO7 AN5
AD8/GPIO8 AN6
AD9/GPIO9 AJ1
AD10/GPIO10 AL8
AD11/GPIO11 AL3
AD12/GPIO12 AM7
AD13/GPIO13 AJ6
AD14/GPIO14 AK7
AD15/GPIO15 AN8
AD16/GPIO16 AG9
AD17/GPIO17 AM11
AD18/GPIO18 AJ10
AD19/GPIO19 AL12
AD20/GPIO20 AK11
AD21/GPIO21 AN12
AD22/GPIO22 AG12
AD23/GPIO23 AE12 PCI_AD23 <16>
AD24/GPIO24 AC12 PCI_AD24 <16>
AD25/GPIO25 AE13 PCI_AD25 <16>
AD26/GPIO26 AF13 PCI_AD26 <16>
AD27/GPIO27 AH13 PCI_AD27 <16>
AD28/GPIO28 AH14
AD29/GPIO29 AD15
AD30/GPIO30 AC15
AD31/GPIO31 AE16
CBE0# AN3
CBE1# AJ8
CBE2# AN10
CBE3# AD12
FRAME# AG10
DEVSEL# AK9
IRDY# AL10
TRDY# AF10
PAR AE10
STOP# AH1
PERR# AM9
SERR# AH8
REQ0# AG15
REQ1#/GPIO40 AG13
REQ2#/CLK_REQ8#/GPIO41 AE15
REQ3#/CLK_REQ5#/GPIO42 AM17 T14
GNT0# AD16
GNT1#/GPO44 AD13
GNT2#/SD_LED/GPO45 AD21
GNT3#/CLK_REQ7#/GPIO46 AK17 T69
CLKRUN# AD19
LOCK# AH9

INTE#/GPIO32 AF18
INTF#/GPIO33 AE18
INTG#/GPIO34 AC16
INTH#/GPIO35 AD18

Module design have reserve GPIO44,45 for VGA power enable and reset

LPC

LPCCLK0 B25 R891 1 2 0_0402_5% CLK_PCI_EC <16,33>
CLK_PCI_DB <32>
R670 @ 0_0402_5%

LPCCLK1 D25 LPC_CLK1 <16>
LAD0 D27 LPC_AD0 <32,33>
LAD1 C28 LPC_AD1 <32,33>
LAD2 A26 LPC_AD2 <32,33>
LAD3 A29 LPC_AD3 <32,33>
LFRAME# A31 LPC_FRAME# <32,33>
LDRQ0# B27
LDRQ1#/CLK_REQ6#/GPIO49 AE22
SERIRQ/GPIO48 AF19 SERIRQ <33>

APU

DMA_ACTIVE# G25
PROCHOT# E28 APU_PROCHOT# R R15 1 @ 2 0_0402_5% ALLOW_STOP <7>
APU_PG E26 APU_PWRGD <7,47>
LDT_STP# G26
APU_RST# E26 APU_RST# <7>

S5 PLUS

S5_CORE_EN H7
RTCCLK F1 RTC_CLK <16,33>
INTRUDER_ALERT# F3
VDDBT_RTC_G E6

W=20mils R105 1 2 510_0402_5% +RTCBATT

32K_X1 G2 32K_X1
32K_X2 G4 32K_X2

C156 1U_0402_6.3V6K

CLRP1 @ SHORT PADS

for Clear CMOS

APU_PCIE_RST #: Reset PCIE device on APU

+3VALW

C789 @ 0.1U_0402_16V4Z

MC74VHC1G08DFT2G SC70 5P U43

APU_PCIE_RST# C @R692 1 2 33_0402_5%

@ C790 150P_0402_50V8J

@ R693 8.2K_0402_5%

@R695 0_0402_5%

R866 0_0402_5%

APU_PCIE_RST# <17,28,32>

PLT_RST# <33>

R692/ C790 close to FCH

25M_X1
25M_X2
R106 1M_0402_5%
OSC NC NC OSC
Y4 25MHZ_20PF_FSX3M-25.M20FDO
C157 22P_0402_50V8J
C155 22P_0402_50V8J

C158 22P_0402_50V8J 32K_X1
R107 20M_0402_5%
Y1 32.768KHZ_12.5PF_CM31532768DZFT
C159 22P_0402_50V8J 32K_X2

Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

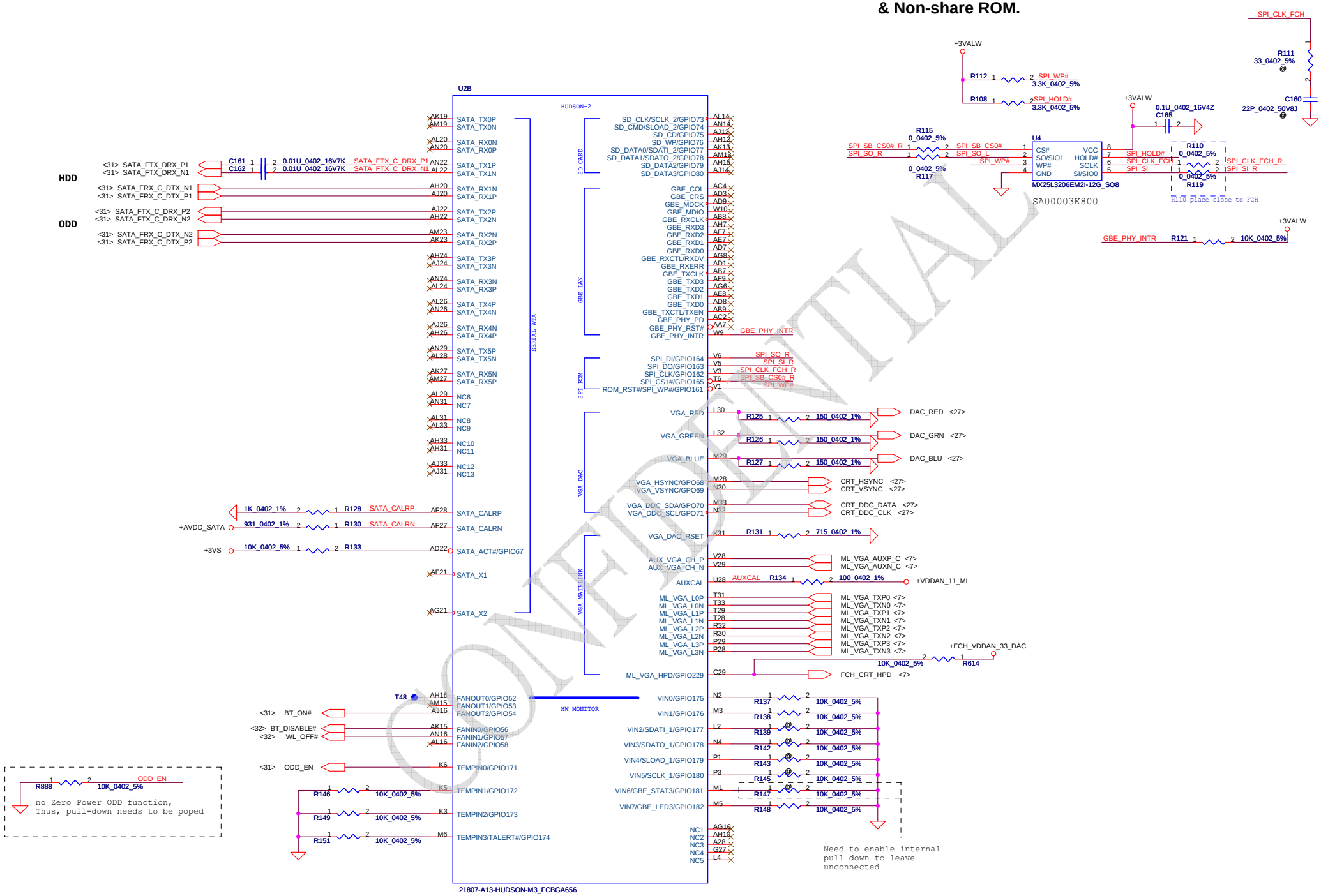
Compal Electronics, Inc.

Title: FCH PCIE/CLK/PCI/LPC/RTC

Size: Custom | Document Number: LA8611P | Rev: 0.1

Date: Monday, November 07, 2011 | Sheet 12 of 51

4MB SPI ROM & Non-share ROM.



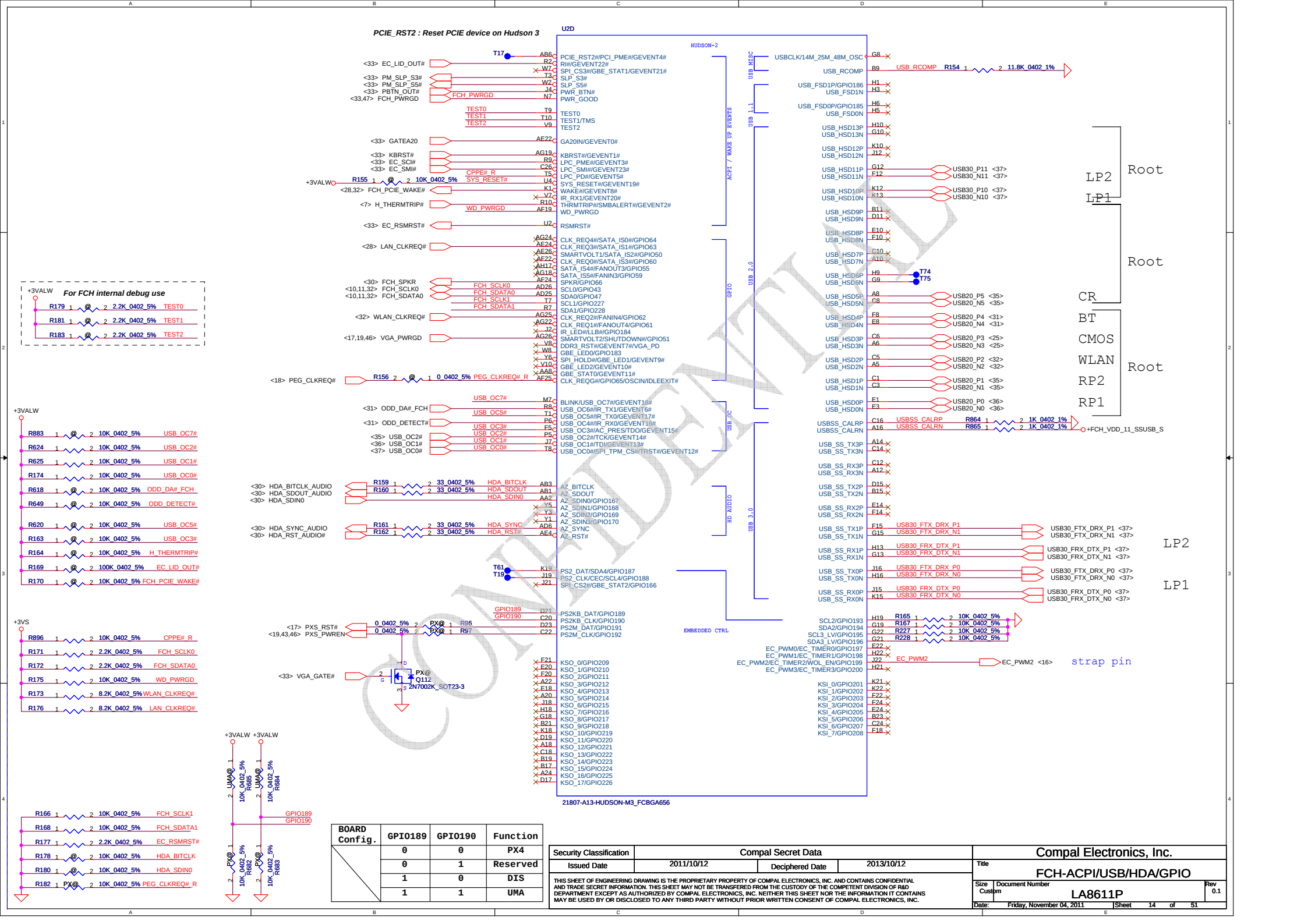
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: FCH SATA/SPI/VGA/HWM/SD

Size	Document Number	Rev
Custom	LA8611P	0.1

Date: Friday, November 04, 2011 Sheet 13 of 51



BOARD Config.	GPIO189	GPIO190	Function
	0	0	PX4
	0	1	Reserved
	1	0	DIS
	1	1	UMA

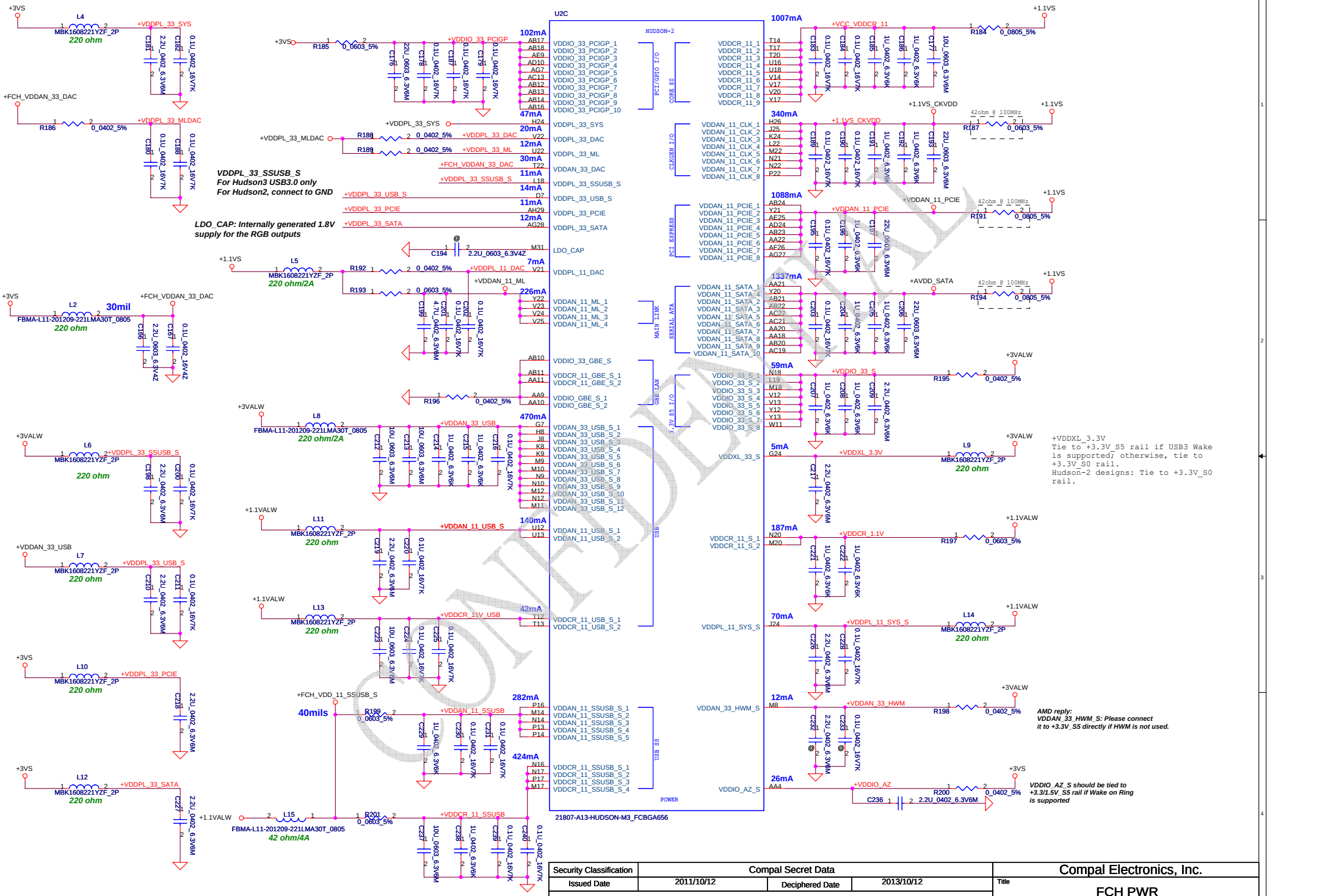
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: FCH-ACPI/USB/HDA/GPIO

Size	Document Number	Rev
Custom	LA8611P	0.1

Date: Friday, November 04, 2011 | Sheet 14 of 51



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

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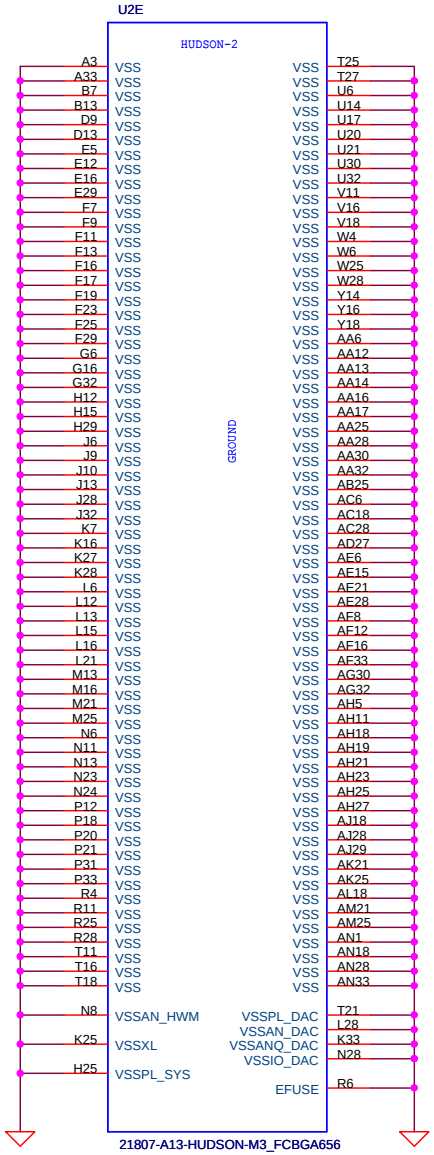
Compal Electronics, Inc.

Title: FCH PWR

Size: Custom | Document Number: LA8611P | Rev: 0.1

Date: Friday, November 04, 2011 | Sheet 15 of 51



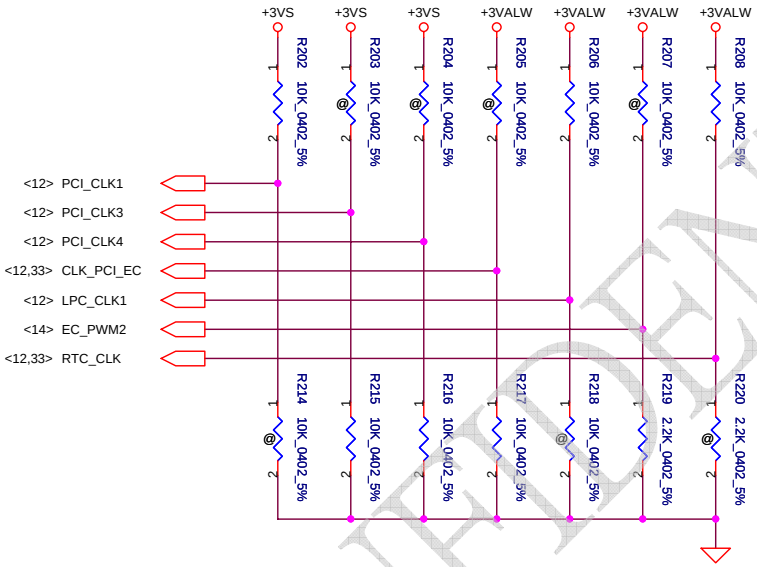
STRAP PINS

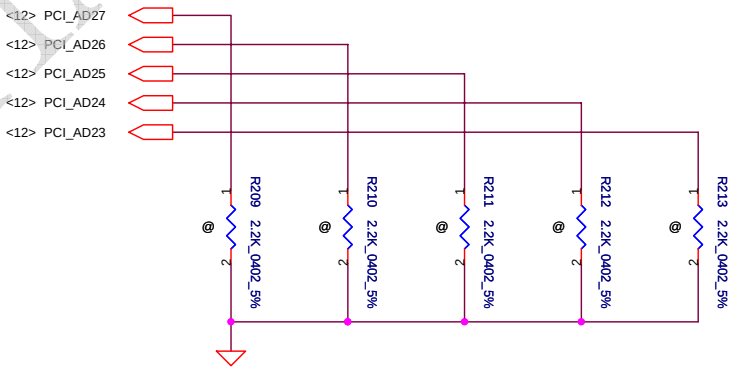
	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT





Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: FCH-VSS/Strap

Size	Document Number	Rev
B	LA8611P	0.1

Date: Friday, November 04, 2011 Sheet 16 of 51

LVDS Interface

Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_PCIE/LVDS

Size	Document Number	Rev
B	LA8611P	0.1

Date: Friday, November 04, 2011 Sheet 17 of 51

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0: 50% swing 1: Full swing	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS 0: disable 1: enable	X
RSVD	GPIO2	Advertises PCIE speed when compliance test 0: 2.5GT/s 1: 5GT/s	0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0: disable 1: enable	X
ROMIDCFG[2:0]	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VIP_DEVICE_STRAP_ENA	VSYNC	IGNORE VIP DEVICE STRAPS	0
RSVD	H2SYNC		0
RSVD	GENERICC		0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21	H2SYNC	GENERICC	GPIO2	GPIO8

TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)

STRAPS

Internal VGA Thermal Sensor

XTALIN
Voltage Swing: 1.8 V

0.60 V level, Please VREFG Divider ans cap close to ASIC

Reserve as AMD request

Security Classification	Compal Secret Data			
Issued Date	2011/10/12	Deciphered Date	2013/10/12	

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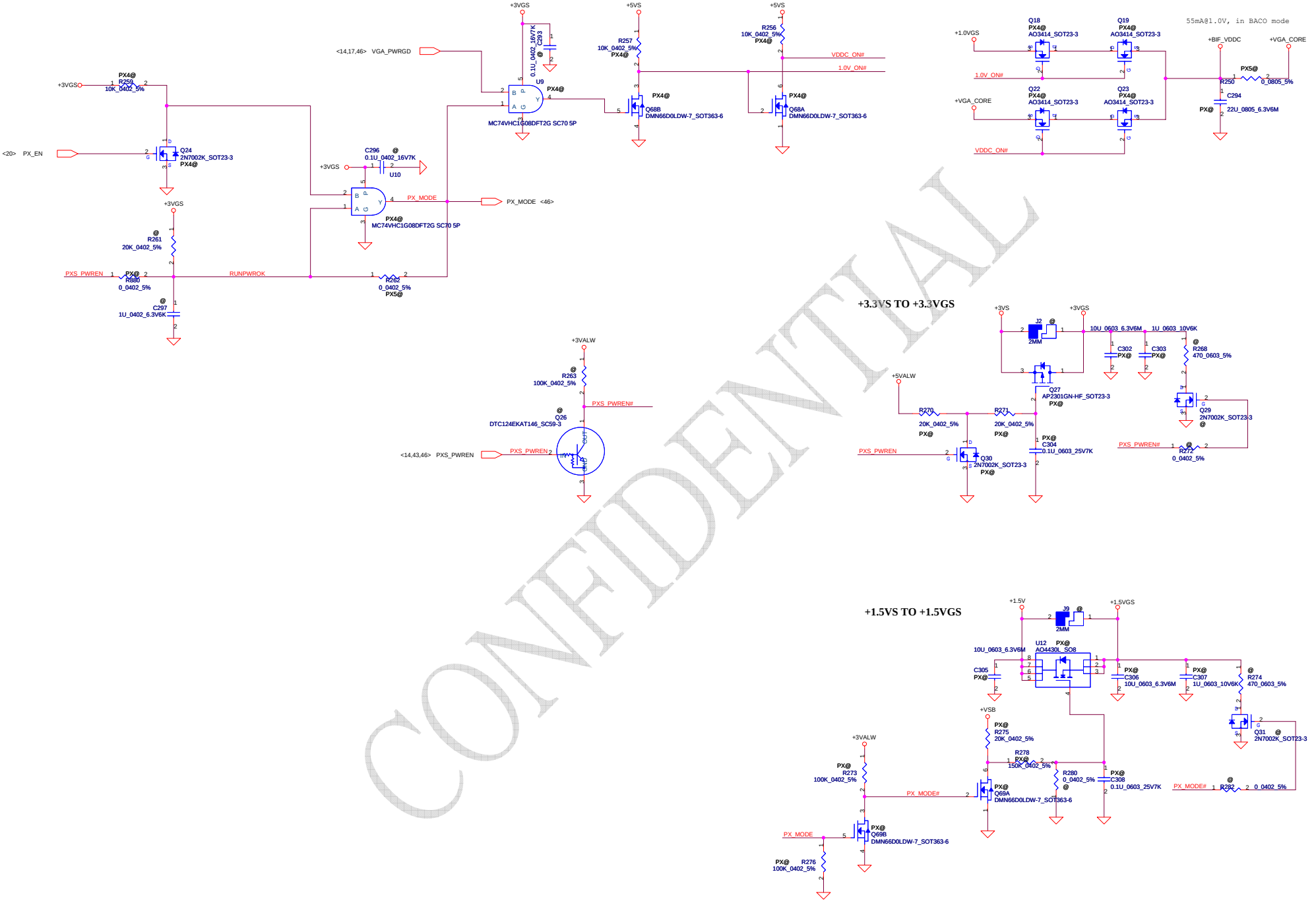
Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_Main_MSIC

Size: C | Document Number: LA8611P | Rev: 0.1

Date: Friday, November 04, 2011 | Sheet 18 of 51



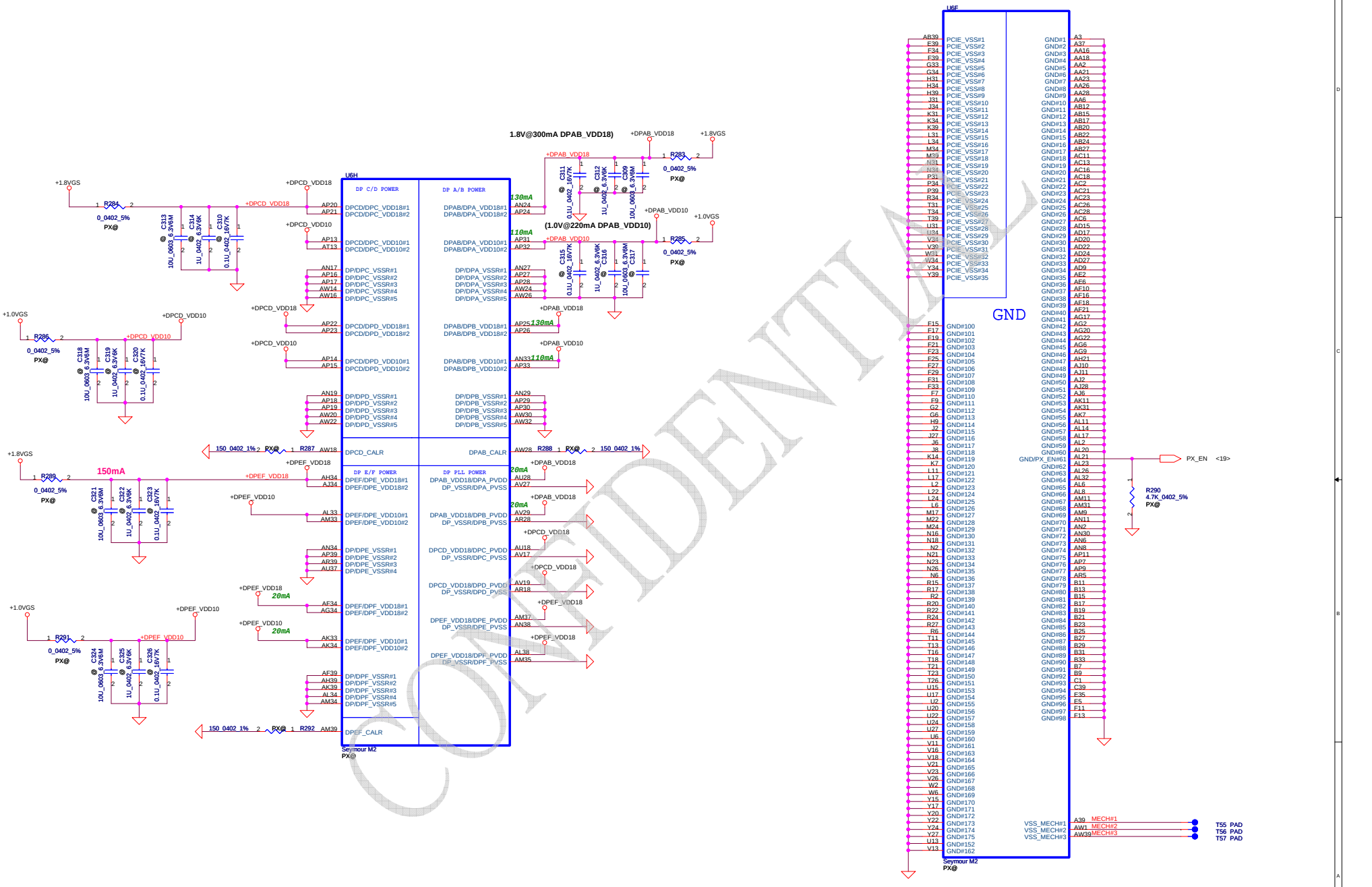
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_BACO POWER

Size	Document Number	Rev
C	LA8611P	0.1

Date: Friday, November 04, 2011 | Sheet 19 of 51



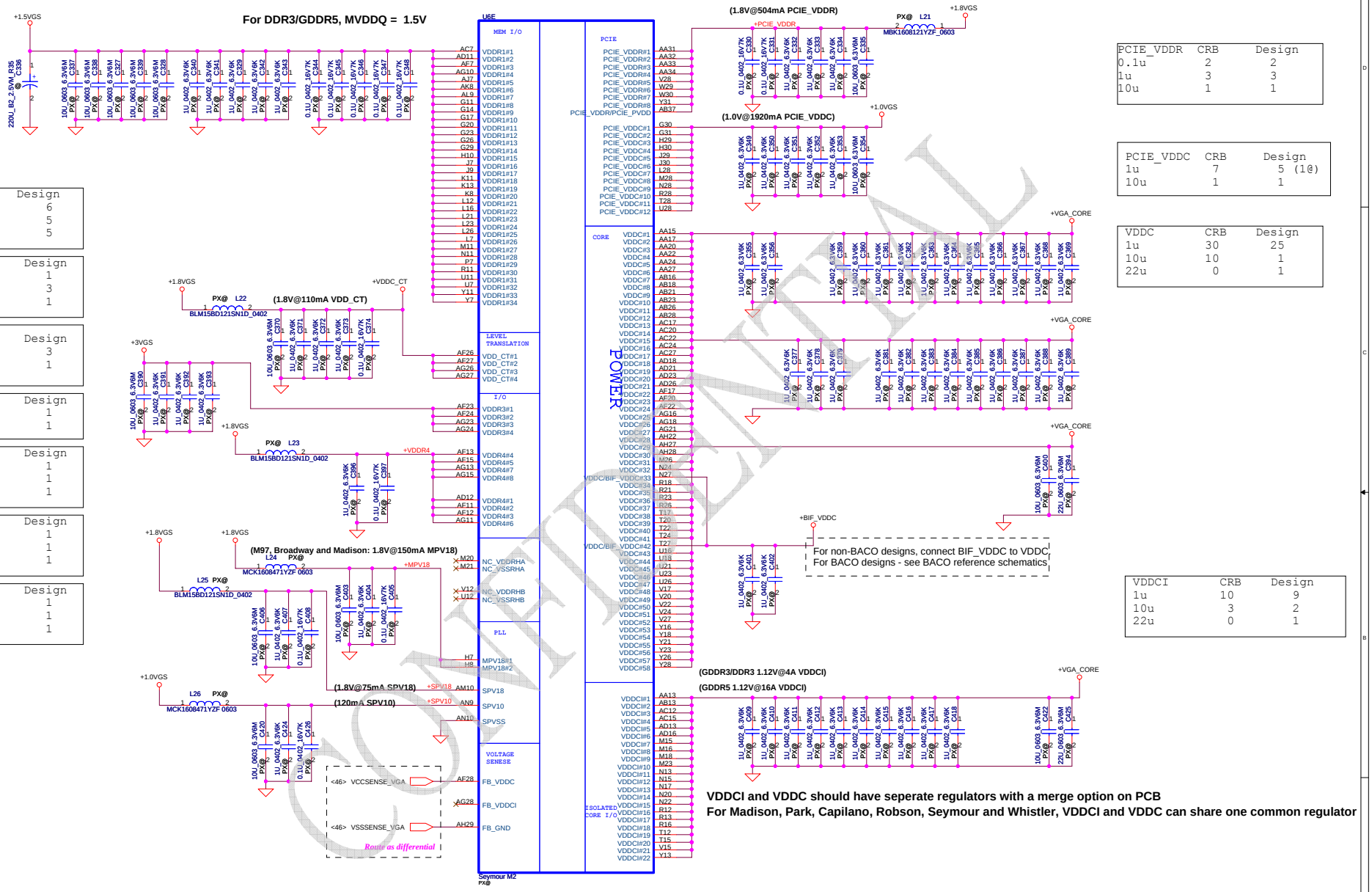
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: ATI_SetmourXT_M2_PWR_GND

Size	Document Number	Rev
C	LA8611P	0.1

Date: Friday, November 04, 2011 Sheet 20 of 51



VDDR1	CRB	Design
0.1u	6	6
1u	10	5
10u	6	5

VDD_CT	CRB	Design
0.1u	1	1
1u	3	3
10u	1	1

VDDR3	CRB	Design
1u	3	3
10u	1	1

VDDR4	CRB	Design
0.1u	1	1
1u	1	1

MPV18	CRB	Design
0.1u	2	1
1u	2	1
10u	1	1

SPV18	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1

SPV10	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1

PCIE_VDDR	CRB	Design
0.1u	2	2
1u	3	3
10u	1	1

PCIE_VDDC	CRB	Design
1u	7	5 (1@)
10u	1	1

VDDC	CRB	Design
1u	30	25
10u	10	1
22u	0	1

VDDCI	CRB	Design
1u	10	9
10u	3	2
22u	0	1

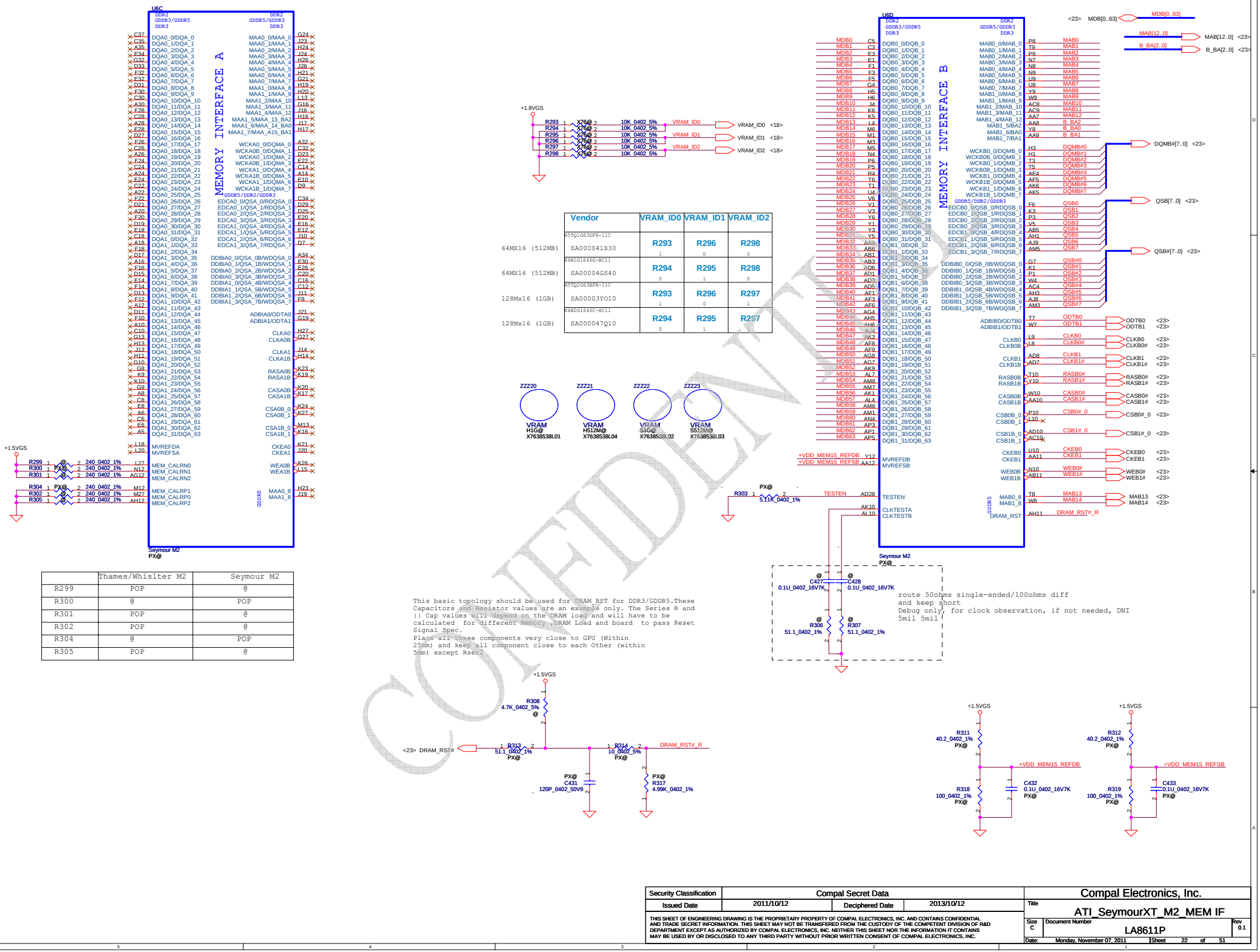
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_Power

Size	Document Number	Rev
C	LA8611P	0.1

Date: Friday, November 04, 2011 Sheet 21 of 51



	Thames/Whistler M2	Seymour M2
R299	POP	@
R300	@	POP
R301	POP	@
R302	POP	@
R304	@	POP
R305	POP	@

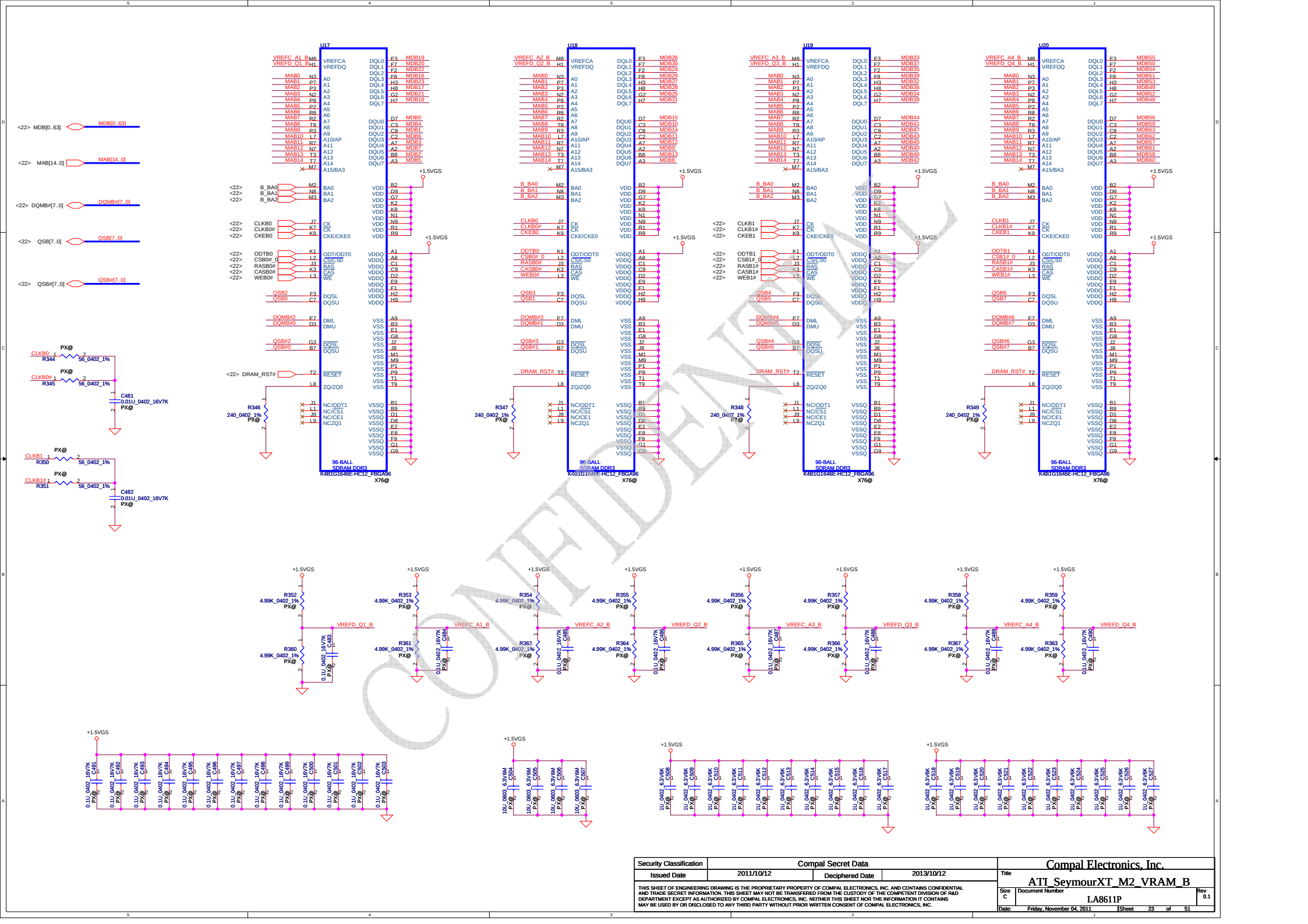
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_MEM IF

Size	Document Number	Rev
C	LA8611P	0.1

Date: Monday, November 07, 2011 | Sheet 22 of 51



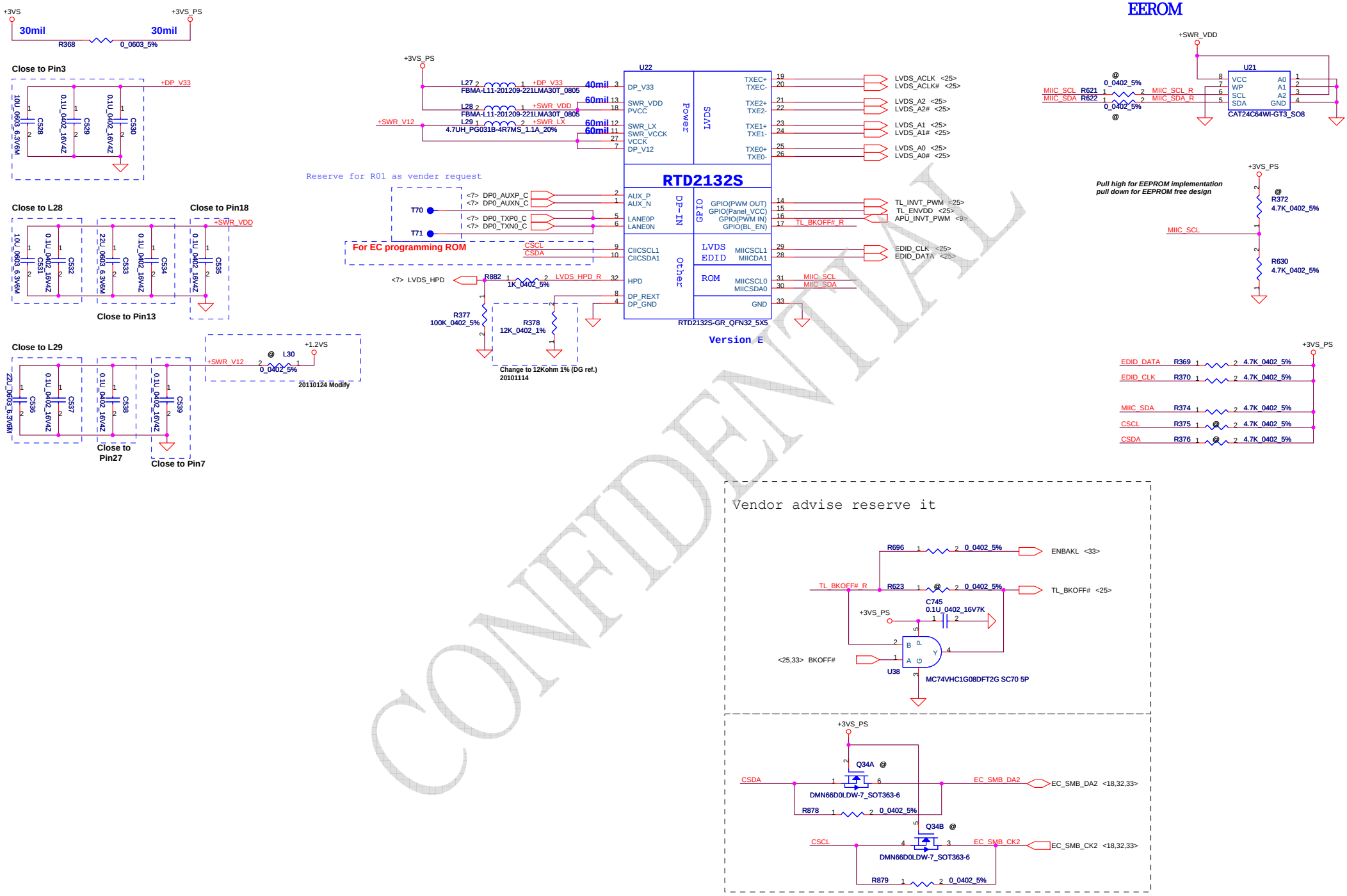
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_VRAM_B

Size	Document Number	Rev
C	LA8611P	0.1

Date: Friday, November 04, 2011 | Sheet 23 of 51



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

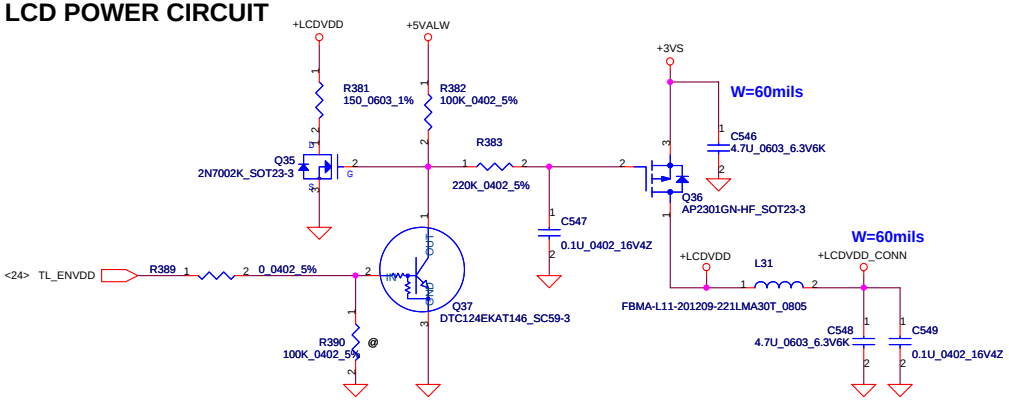
Compal Electronics, Inc.

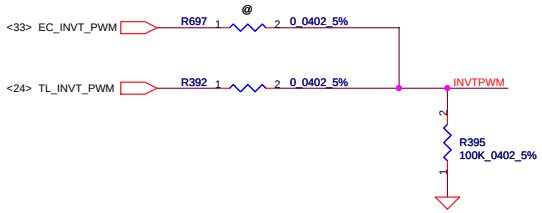
Title: LVDS Translator - RTD2132S

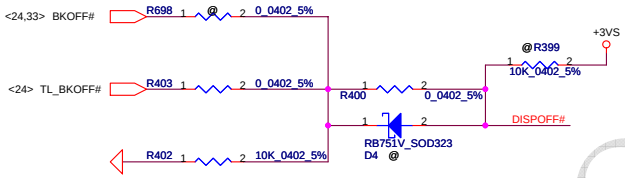
Size	Document Number	Rev
Custom	LA8611P	0.1

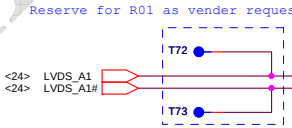
Date: Monday, November 07, 2011 Sheet 24 of 51

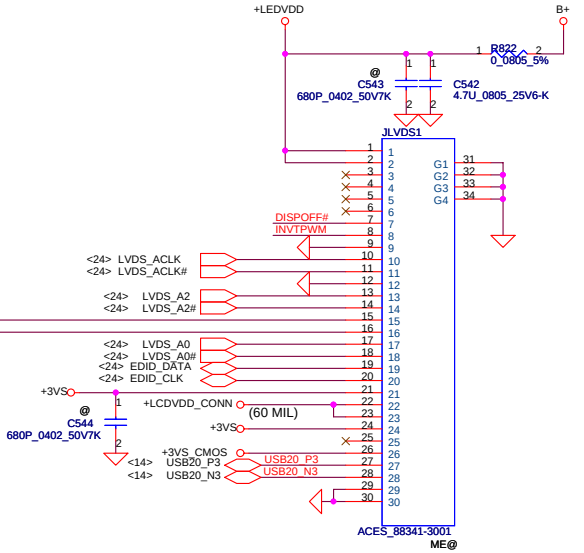
LCD POWER CIRCUIT



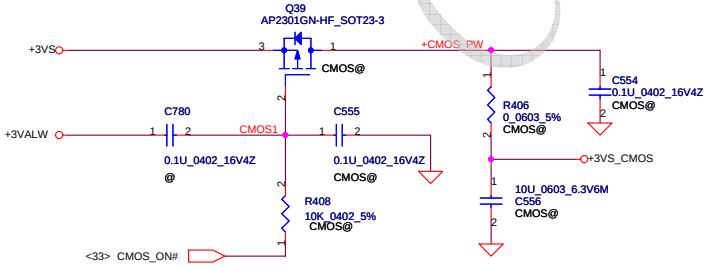








CMOS Camera



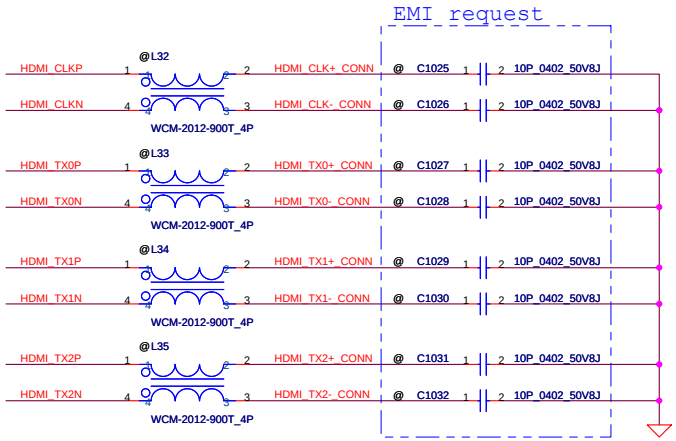
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

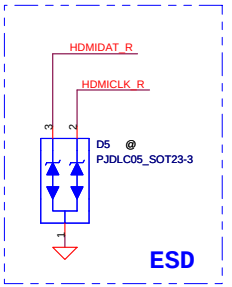
Compal Electronics, Inc.

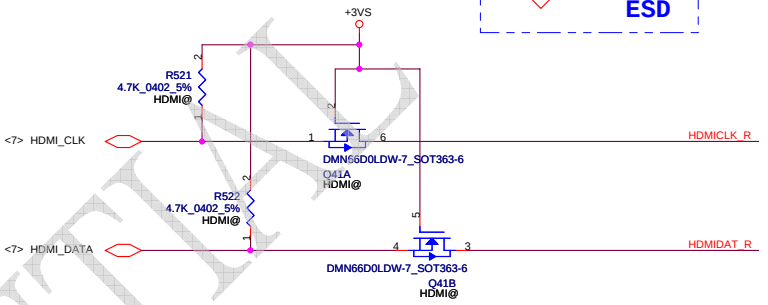
Title: LVDS/CAMERA

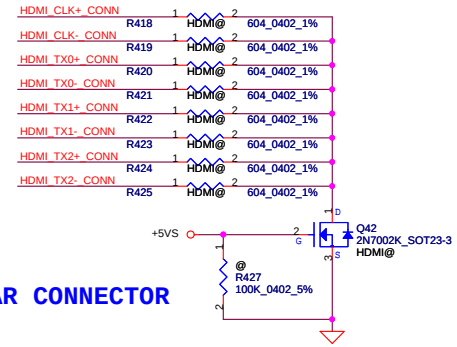
Size	Document Number	Rev
B	LA8611P	0.1

Date: Friday, November 04, 2011 | Sheet 25 of 51

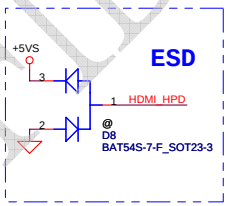


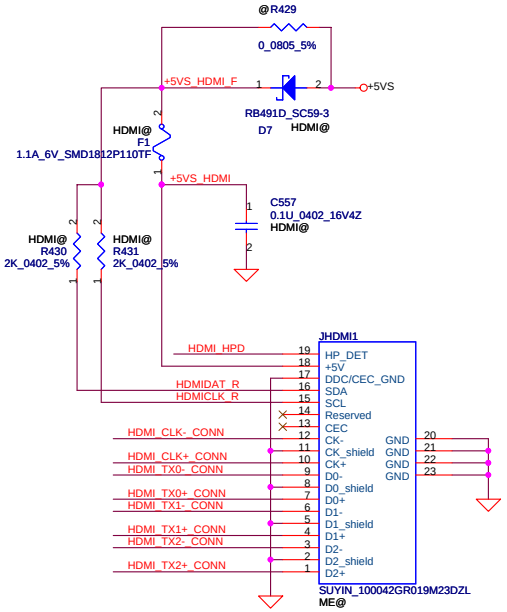


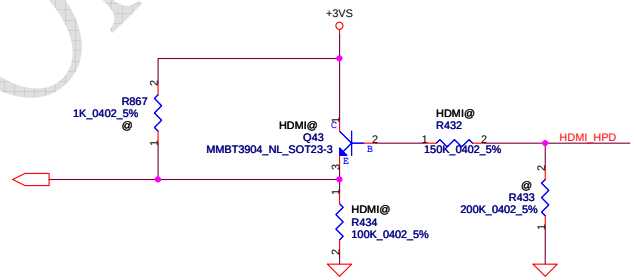




NEAR CONNECTOR







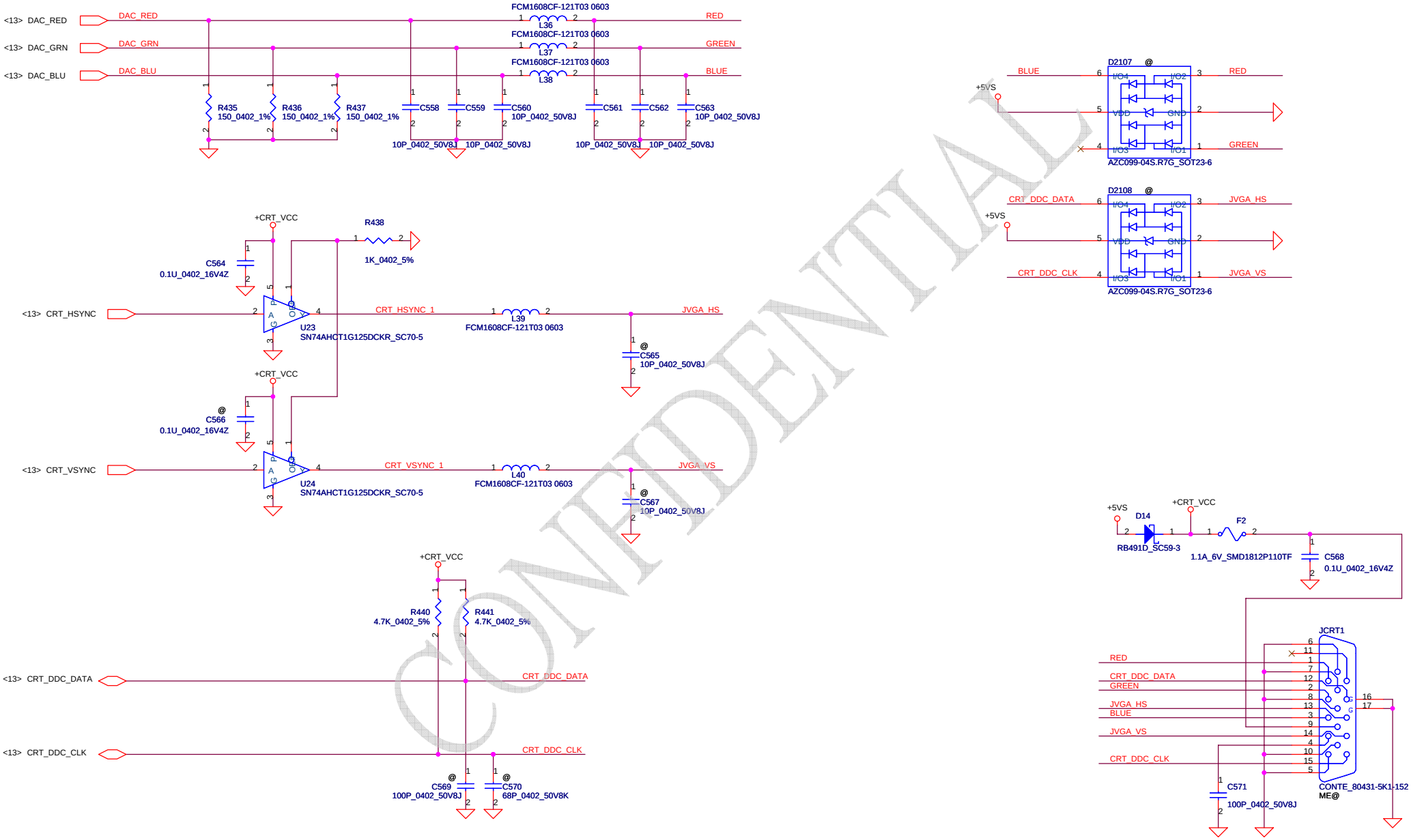
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: HDMI Connector

Size	Document Number	Rev
Custom	LA8611P	0.1

Date: Friday, November 04, 2011 Sheet 26 of 51



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title	CRT Connector	
Size: Custom	Document Number: LA8611P	Rev: 0.1
Date: Friday, November 04, 2011	Sheet 27 of 51	

Switching Mode only

+3VALW

+3V_LAN

J11

JUMP_43X79

Layout Notice : Place as close chip as possible.

Atheros request can't disable LAN power

Close together

+LX

R772 0_0402_5%

+1.1_DVDDL

+LX_R

L60 4.7UH_SIA4012-4R7M_20%

C854 1000P_0402_50V7K

C855 0.1U_0402_16V4Z

C859 10U_0603_6.3V6M

Note: Place Close to LAN chip
L39 DCR< 0.15 ohm
Rate current > 1A

Close to Pin40

L61 FBMA-L11160808601LMA10T_2P

L62 FBMA-L11160808601LMA10T_2P

+1.1_AVDDL_L

+1.1_AVDDL

+1.1_DVDDL

C856 0.1U_0402_16V4Z

C857 1U_0402_6.3V4Z

C858 4.7U_0603_6.3V6K

Place close to Pin34

Vendor recommand reseve the PU resistor close LAN chip

+3V_LAN

R773 4.7K_0402_5%

@

<12,17,32> APU_PCIE_RST#

APU_PCIE_RST#

U41 8162@

AR8162-AL3A-R

SA000050E00_S IC AR8161-AL3A-R QFN 40P E-LAN CTRL

SA000052J10_S IC AR8162-AL3A-R QFN 40P E-LAN CTRL

H --> Overclocking mode
L --> Not overclocking mode
Overclocking mode stick

+3V_LAN

+AVDDH_AVDD3.3

R774 0_0402_5%

C860 0.1U_0402_16V4Z

C862 1U_0402_6.3V4Z

Place close to Pin16

Place Close to Chip

U41 GIGA@

Atheros AR8151/AR8161

<5> PCIE_CRX_DTX_N0

C861 .1U_0402_16V7K

PCIE_PRX_C_DTX_N0

<5> PCIE_CRX_DTX_P0

C863 .1U_0402_16V7K

PCIE_PRX_C_DTX_P0

<5> PCIE_CTX_DRX_N0

<5> PCIE_CTX_DRX_P0

<12> CLK_PCIE_LAN#

<12> CLK_PCIE_LAN

APU_PCIE_RST#

<14,32> FCH_PCIE_WAKE#

<33> LAN_WAKE#

R777 0_0402_5%

R778 0_0402_5%

PCIE_WAKE#_R

+3V_LAN

R780 4.7K_0402_5%

Vendor recommand reseve the PU resistor close LAN chip

+3V_LAN

R781 4.7K_0402_5%

<14> LAN_CLKREQ#

LAN_XTALO

LAN_XTALI

TX_N TX_P RX_N RX_P REFCLK_N REFCLK_P PERST# WAKE# SMCLK SMDATA NC TESTMODE XTLO XTLI CLKREQ# AVDDL AVDDL AVDDL AVDDL AVDDL_REG/AVDDL GND

LED_0 LED_1 LED_2 VDD33 LX VDDCT/ISOLAN DVDDL/PPS DVDDL_REG/DVDDL AVDDH/AVDDL3 AVDDH AVDDH_REG RBIAS

ACTIVITY LAN_LINK# LAN_CLK_SEL

R881 @ 10K_0402_5%

R775 @ 10K_0402_5%

ACTIVITY <29>

LAN_LINK# <29>

For 48MHz CLK need to pull down, keep floating for cystal

TRXN0 TRXP0 TRXN1 TRXP1 TRXN2 TRXP2 TRXN3 TRXP3

MDI0- MDI0+ MDI1- MDI1+ MDI2- MDI2+ MDI3- MDI3+

MDI0 <29> MDI0+ <29> MDI1- <29> MDI1+ <29> MDI2- <29> MDI2+ <29> MDI3- <29> MDI3+ <29>

LAN_RBIAS

R779 2.37K_0402_1%

Place Close to PIN1

+3V_LAN

+1.7_VDDCT

R782 30K_0402_1%

+3VS

+1.1_DVDDL

+2.7_AVDDH

+AVDDH_AVDD3.3

+2.7_AVDDH

+2.7_AVDDH

AR8161-AL3A-R_QFN40_5X5

Place Close to PIN1

+3V_LAN

C864 1000P_0402_50V7K

C865 0.1U_0402_16V4Z

C866 1U_0402_6.3V4Z

C867 10U_0603_6.3V6M

C868 10U_0603_6.3V6M

C869 0.1U_0402_16V4Z

C870 0.1U_0402_16V4Z

C871 0.1U_0402_16V4Z

C872 1U_0402_6.3V4Z

C873 0.1U_0402_16V4Z

C874 0.1U_0402_16V4Z

C875 1U_0402_6.3V4Z

C876 0.1U_0402_16V4Z

C877 0.1U_0402_16V4Z

C878 1U_0402_6.3V4Z

Near Pin13

Near Pin19

Near Pin31

Near Pin6

Near Pin9

Near Pin22

Near Pin37

<12> CLK_LAN_48M

C879 @ 5P_0402_50V8

Place Close to C881

LAN_XTALI

LAN_XTALO

Y3

NC OSC OSC NC

25MHZ_20PF_FSX3M-25.M20FDO

C881 27P_0402_50V8J

C882 27P_0402_50V8J

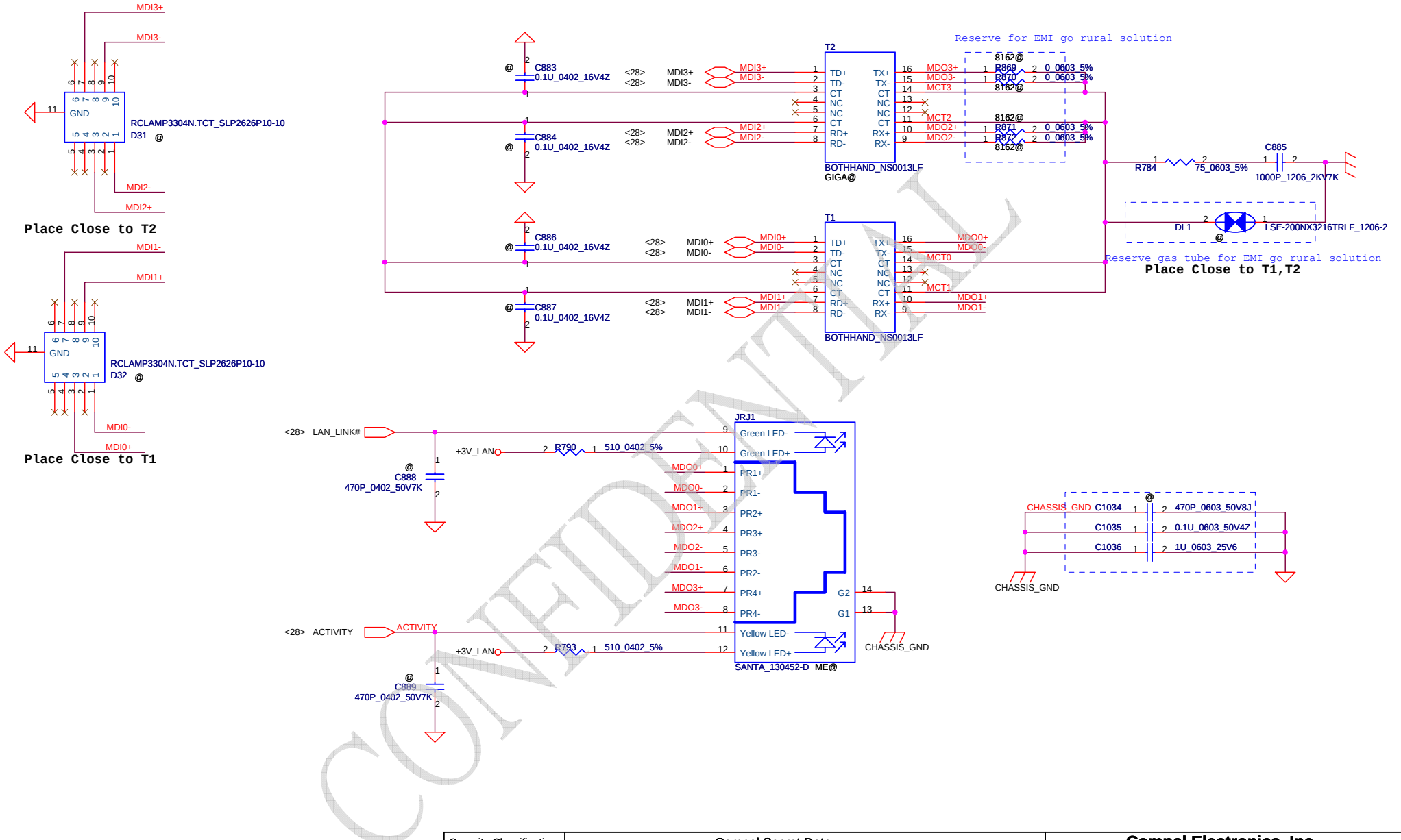
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: LAN-AR8151/8161

Size: Custom | Document Number: LA8611P | Rev: 0.1

Date: Tuesday, November 08, 2011 | Sheet 28 of 51



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

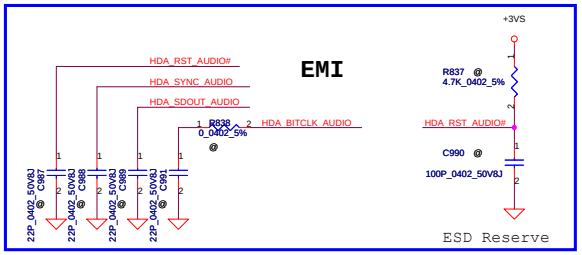
Compal Electronics, Inc.

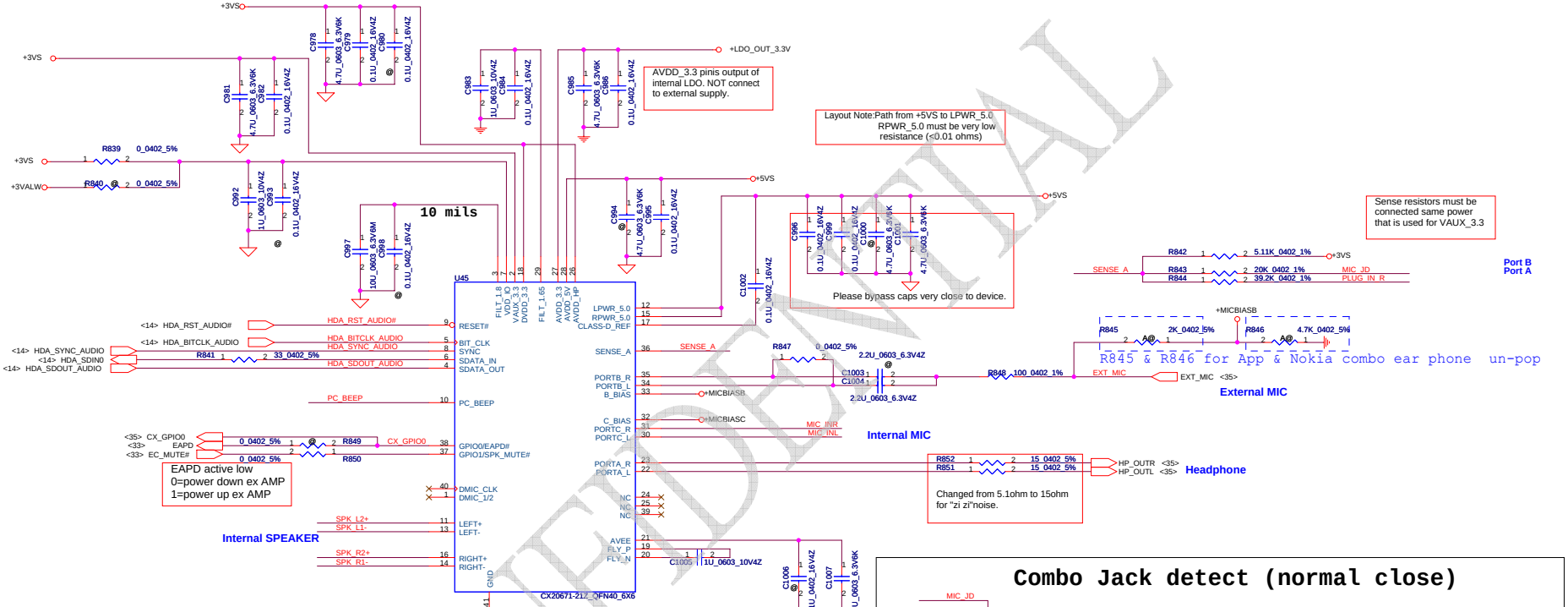
Title: LAN_Transformer

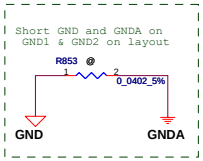
Size	Document Number	Rev
B	LA8611P	0.1

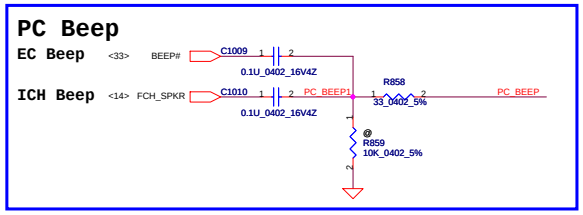
Date: Tuesday, November 08, 2011 Sheet 29 of 51

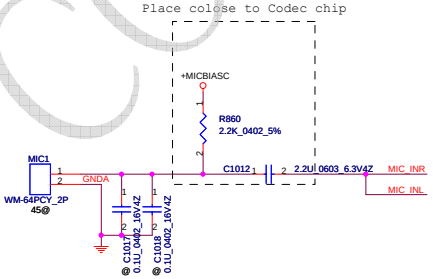
CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).

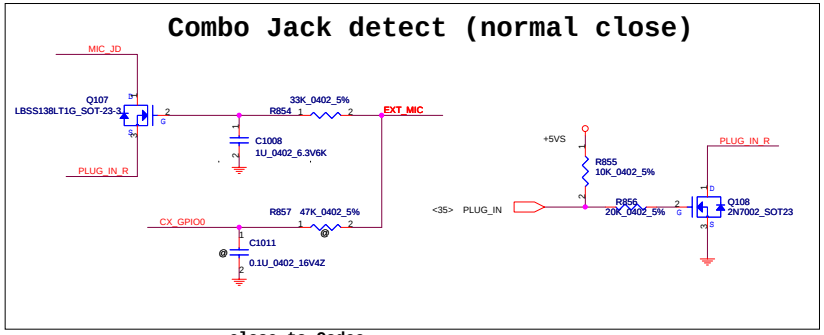








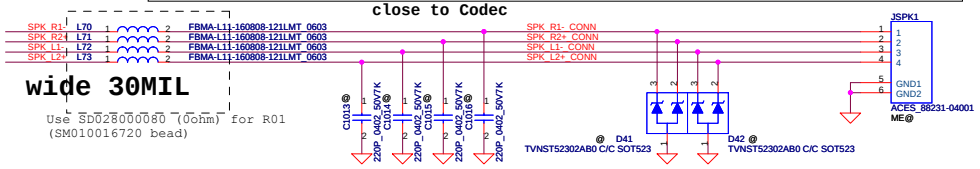




close to Codec

wide 30MIL

Use SD028000080 (0ohm) for R01 (SM010016720 bead)



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

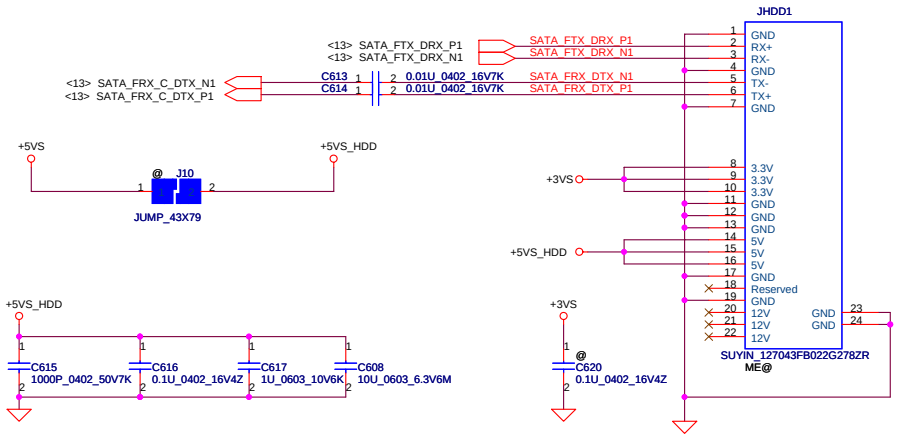
Compal Electronics, Inc.

Title: CX20671 Codec

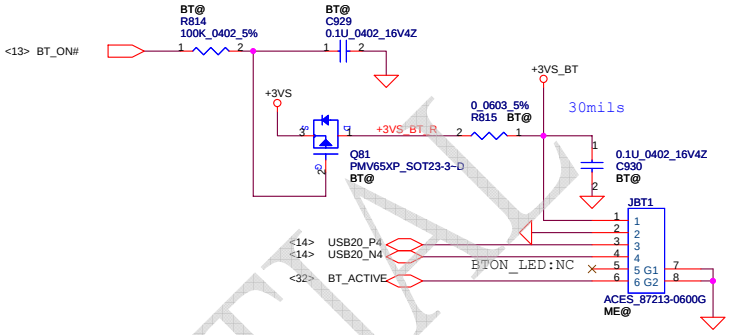
Size: Custom | Document Number: LA8611P | Rev: 0.1

Date: Monday, November 07, 2011 | Sheet 30 of 51

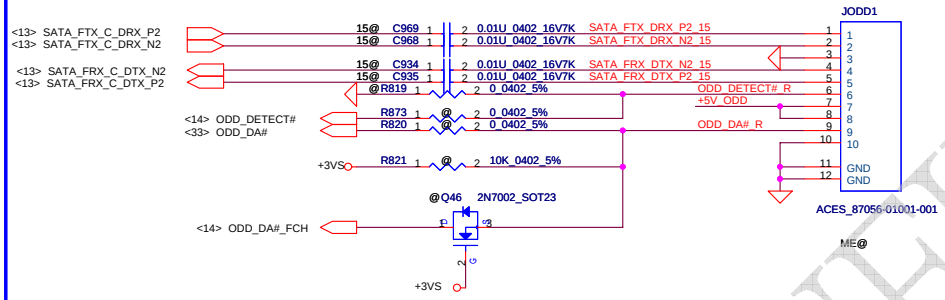
HDD CONN



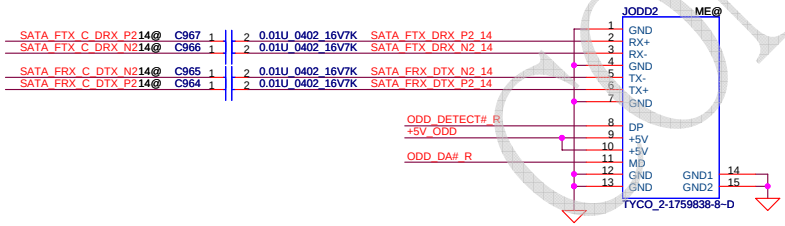
BT MODULE CONN



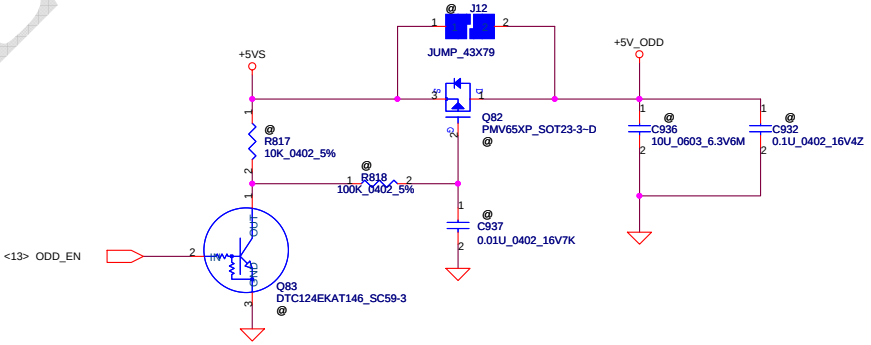
ODD CONN 15''



ODD CONN 14''



short J12, no zero power ODD function

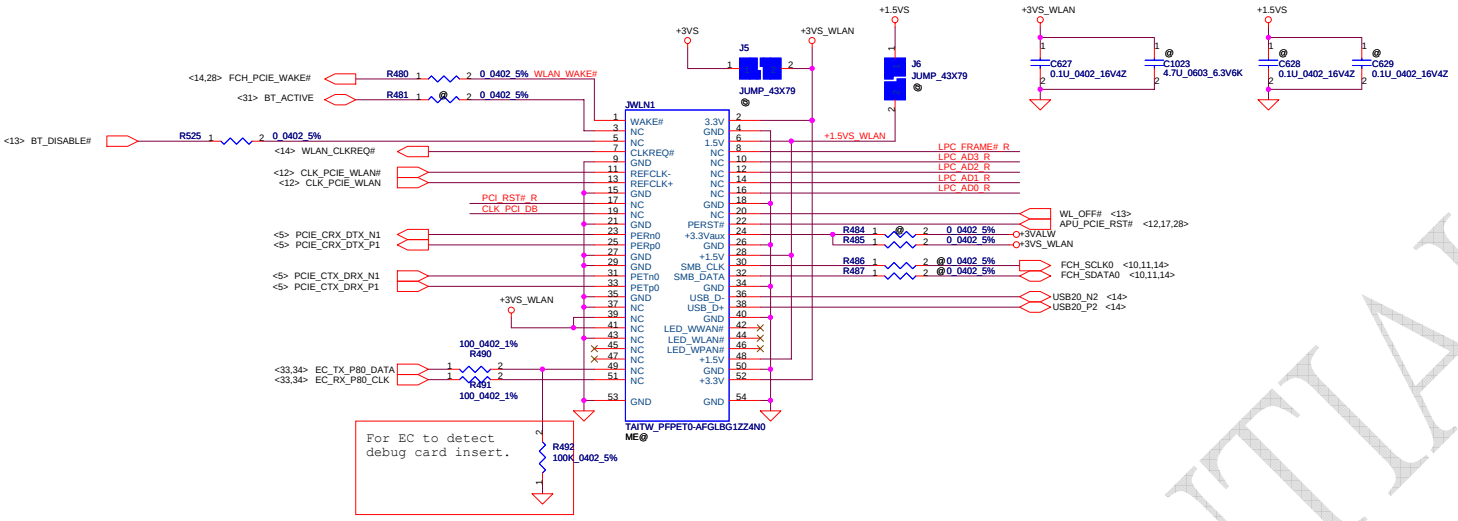


Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

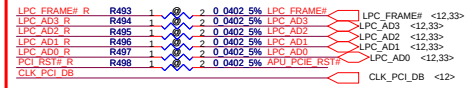
Compal Electronics, Inc.

Title	HDD/ODD/BT	
Size B	Document Number LA8611P	Rev 0.1
Date: Friday, November 04, 2011	Sheet 31 of 51	

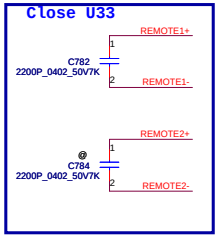
Mini-Express Card for WLAN/WiMAX(Half)



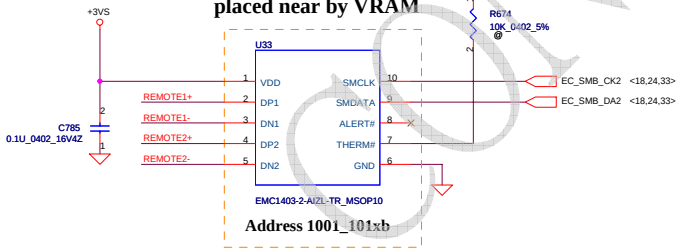
Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.



Close U33



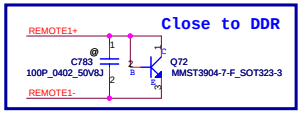
SMSC thermal sensor placed near by VRAM



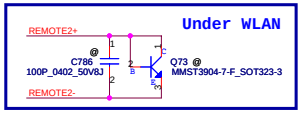
Address 1001_101xb

Change from SA000029210 to SA000046C00 for main source

Close to DDR



Under WLAN

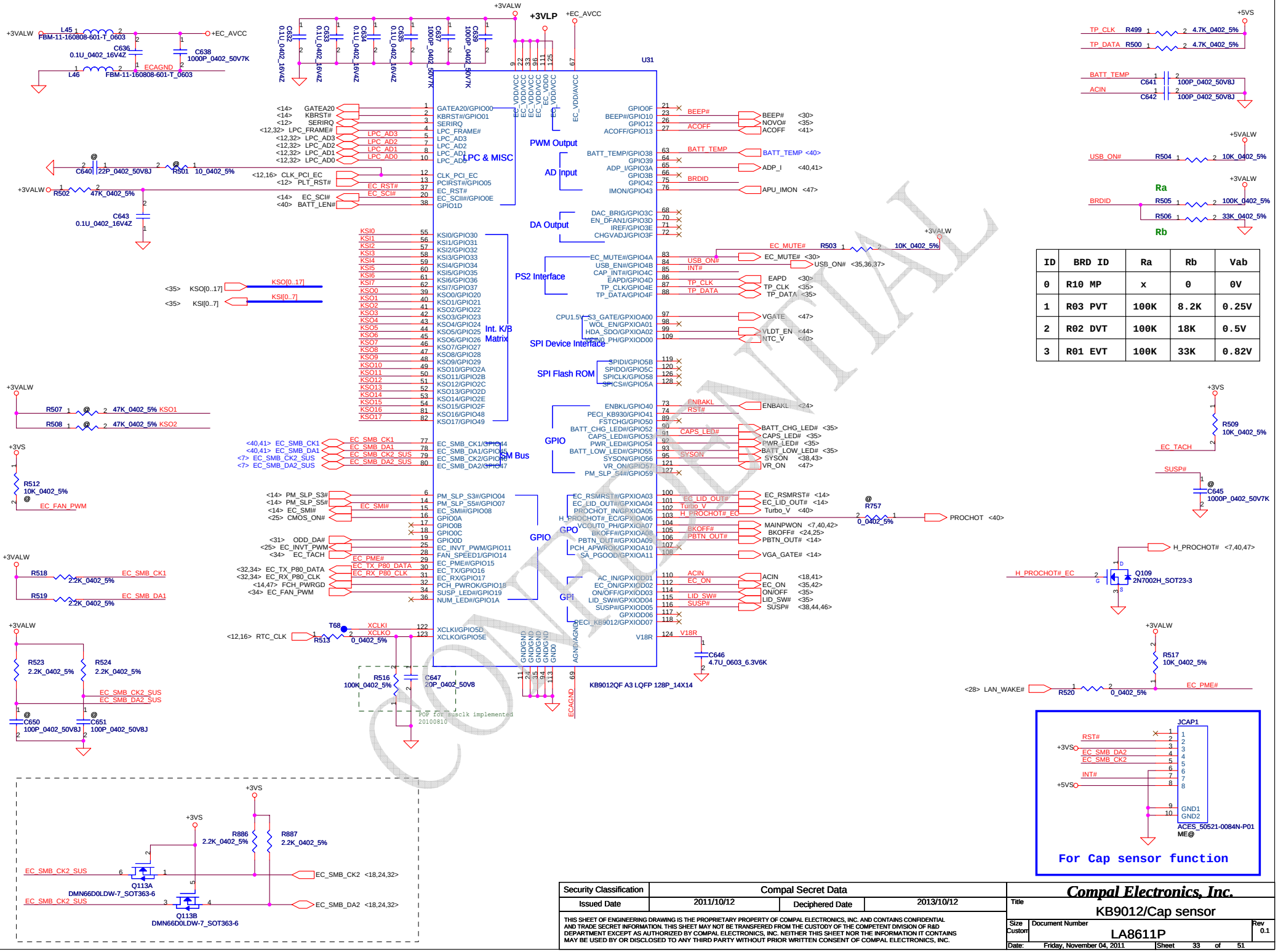


REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title	Mini PCIE/Thermal IC	
Size	Document Number	Rev
	LA8611P	0.1
Date: Friday, November 04, 2011	Sheet 32 of 51	



ID	BRD ID	Ra	Rb	Vab
0	R10 MP	x	0	0V
1	R03 PVT	100K	8.2K	0.25V
2	R02 DVT	100K	18K	0.5V
3	R01 EVT	100K	33K	0.82V

Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

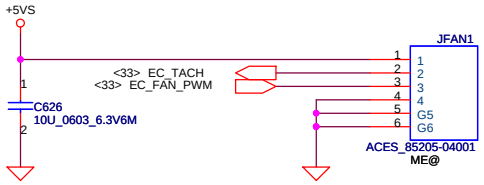
Compal Electronics, Inc.

Title: KB9012/Cap sensor

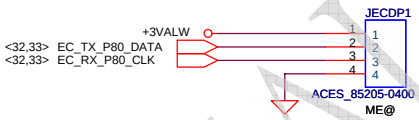
Size	Document Number	Rev
Custom	LA8611P	0.1

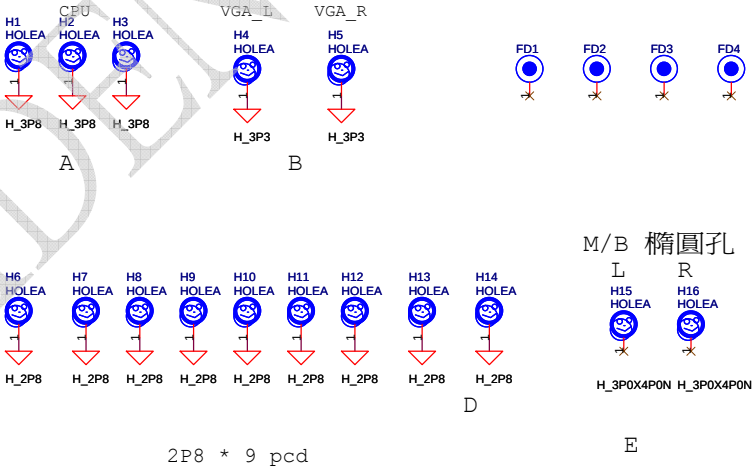
Date: Friday, November 04, 2011 | Sheet 33 of 51

FAN CONN



EC DEBUG PORT





Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

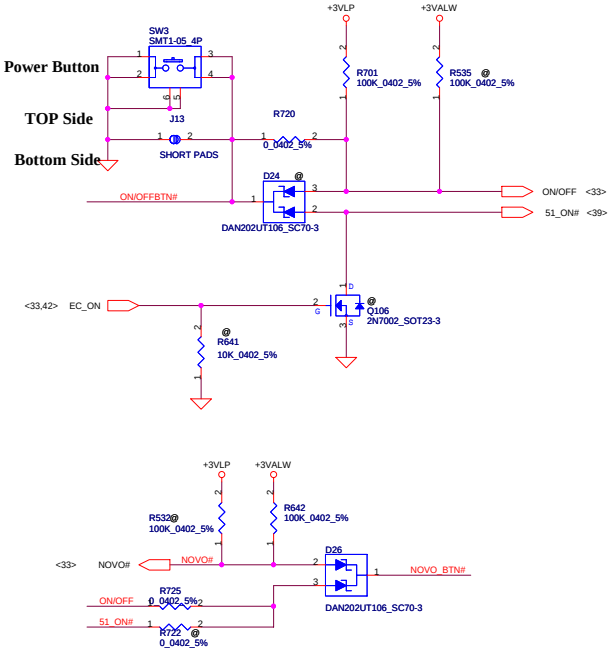
Compal Electronics, Inc.

Title: FAN/SCREW/EC Debug

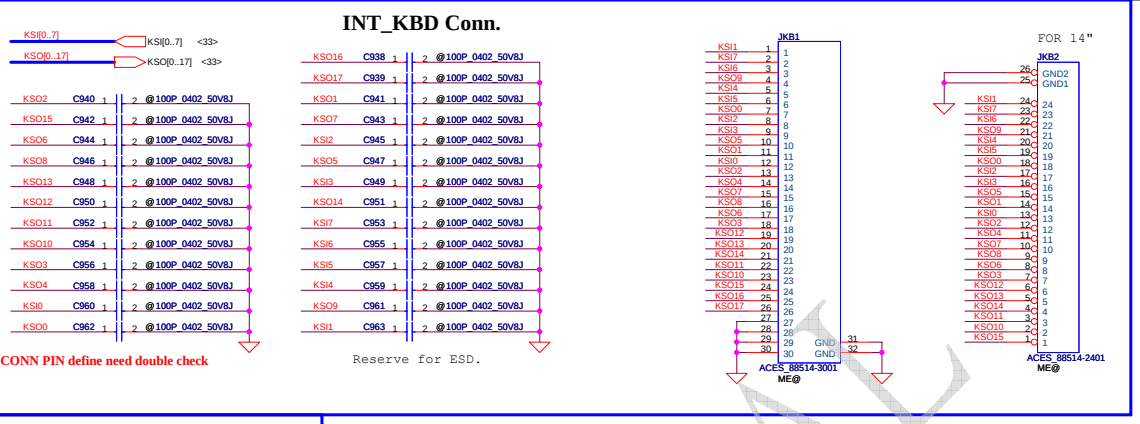
Size	Document Number	Rev
B	LA8611P	0.1

Date: Friday, November 04, 2011 | Sheet 34 of 51

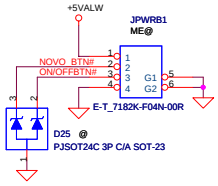
ON/OFF switch



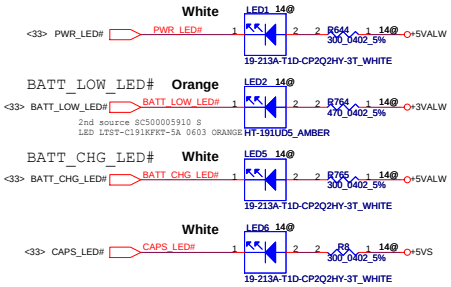
INT_KBD Conn.

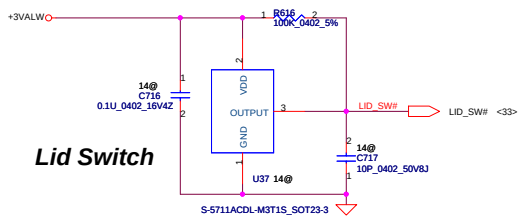


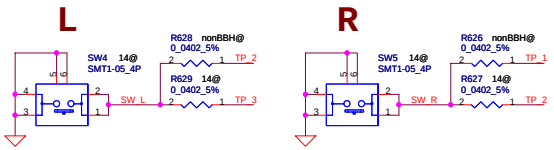
Power Button Board Conn. 8pin



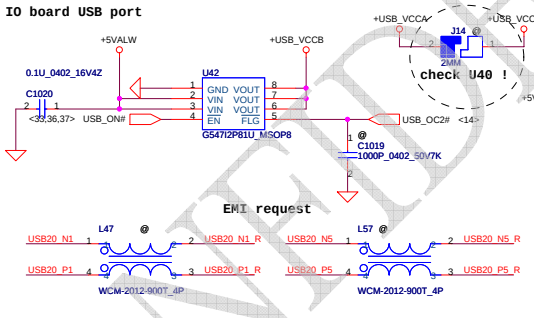
FOR 14"



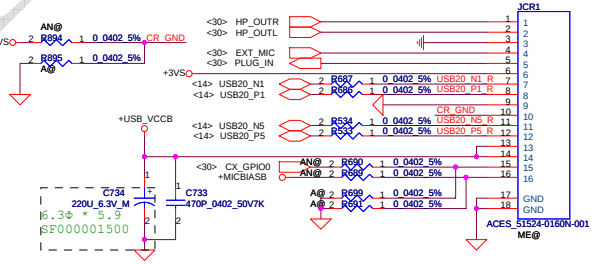




IO board USB port

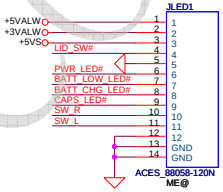


Card Reader/Audio Jack SB CONN



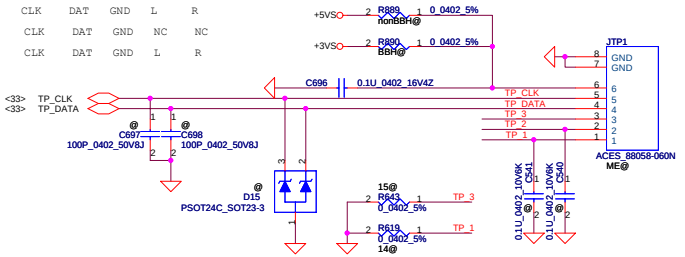
FOR 15"

LED B/D Conn



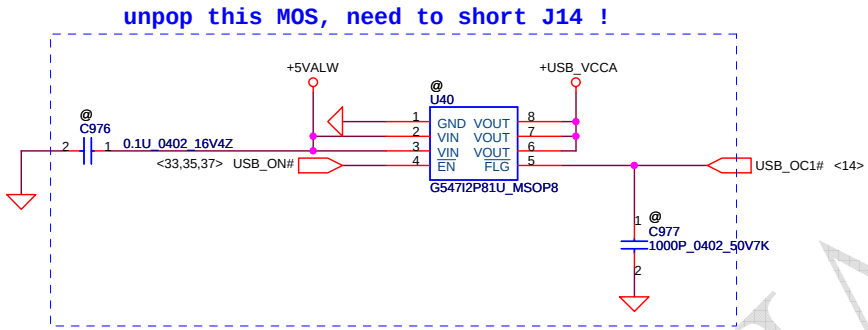
To TP/B Conn.

pin	6	5	4	3	2	1
14	VDD	CLK	DAT	L	R	GND
15	VDD	CLK	DAT	GND	L	R
BB-H	VDD	CLK	DAT	GND	NC	NC
BB-L	VDD	CLK	DAT	GND	L	R

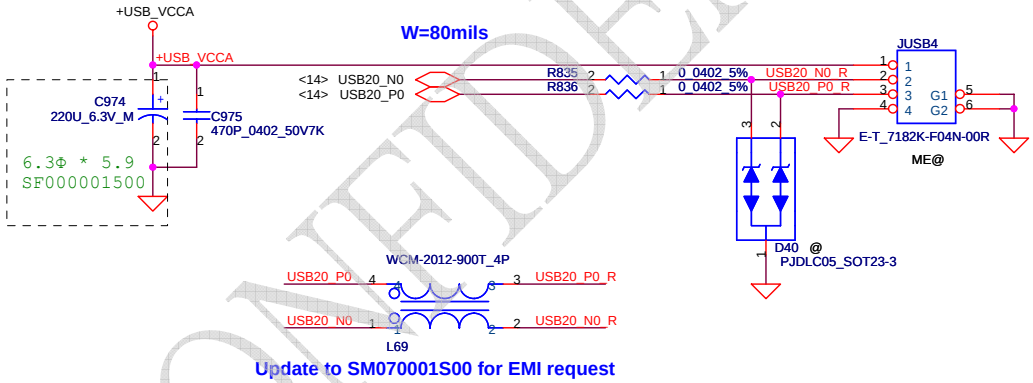


Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Title	Compal Electronics, Inc. KBD/PWR/CR/LED/TP Conn.		
Size C	Document Number LA8611P		Rev 0.1
Date: Monday, November 07, 2011	Sheet 35 of 51		



Right Ext.USB FFC Conn.



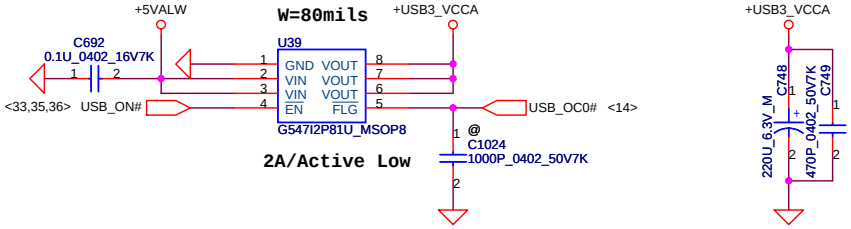
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

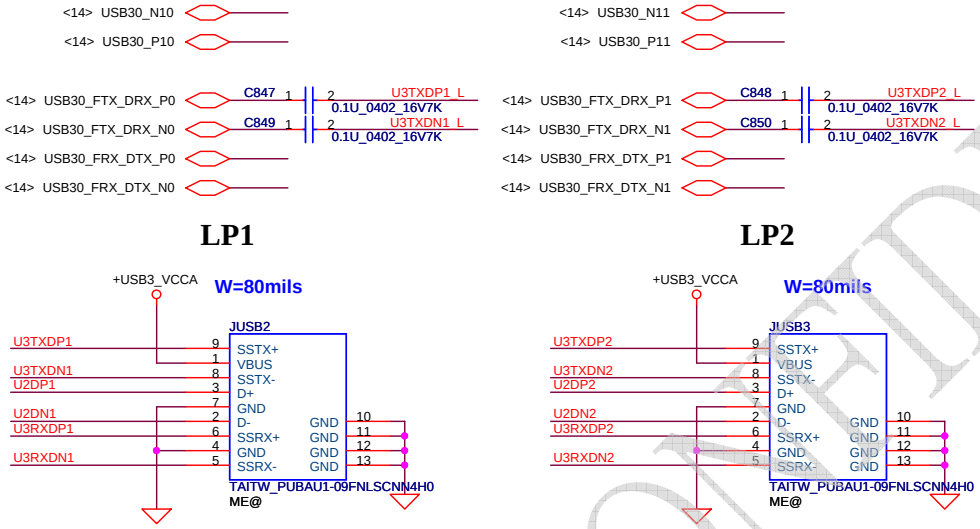
Compal Electronics, Inc.

Title: USB cable port

Size	Document Number	Rev
B	LA8611P	0.1

Date: Monday, November 07, 2011 Sheet 36 of 51

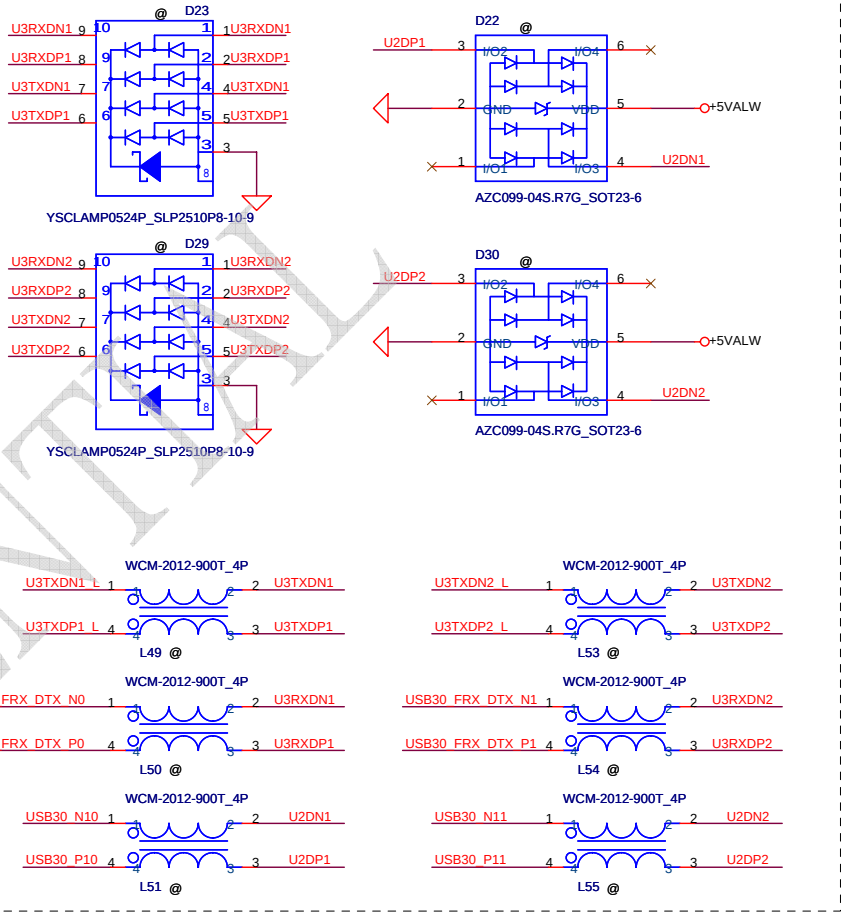


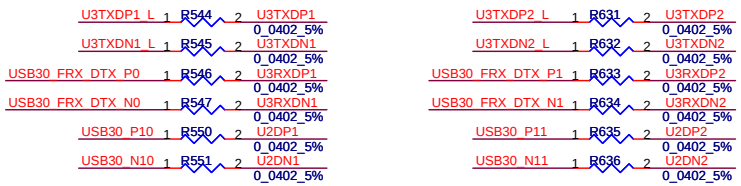


LP1

LP2

For EMI/ESD request





Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: Left USB3.0

Size	Document Number	Rev
B	LA8611P	0.1

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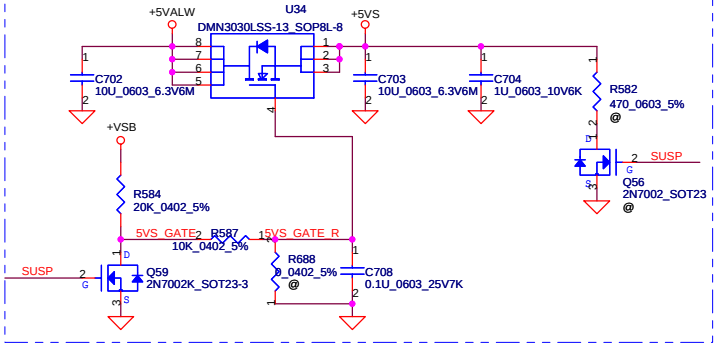
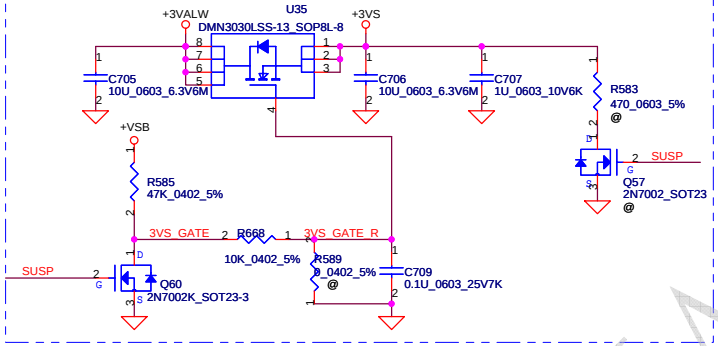
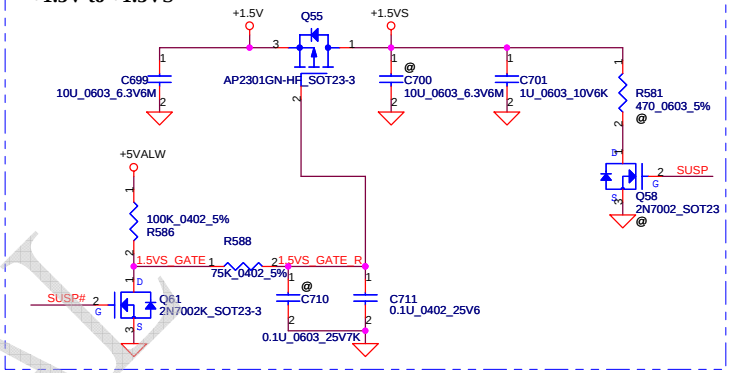
+5VALW TO +5VS



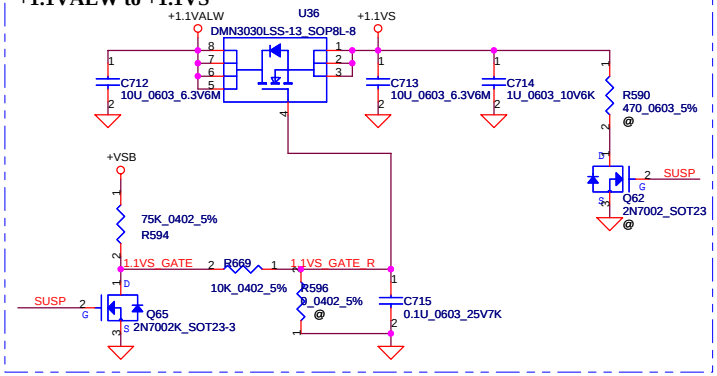
+3VALW TO +3VS

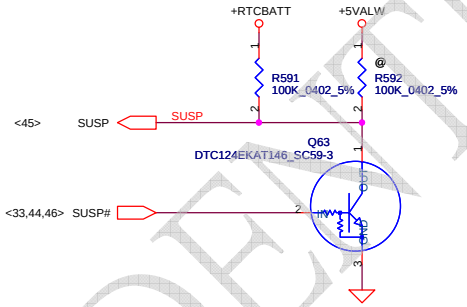


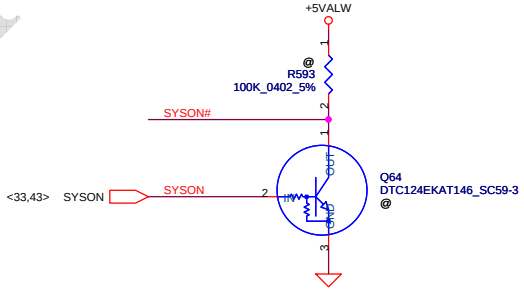
+1.5V to +1.5VS

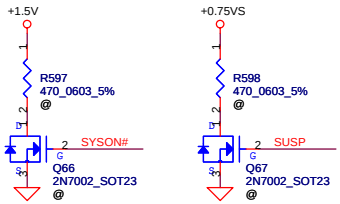


+1.1VALW to +1.1VS









Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	LA8611P	0.1

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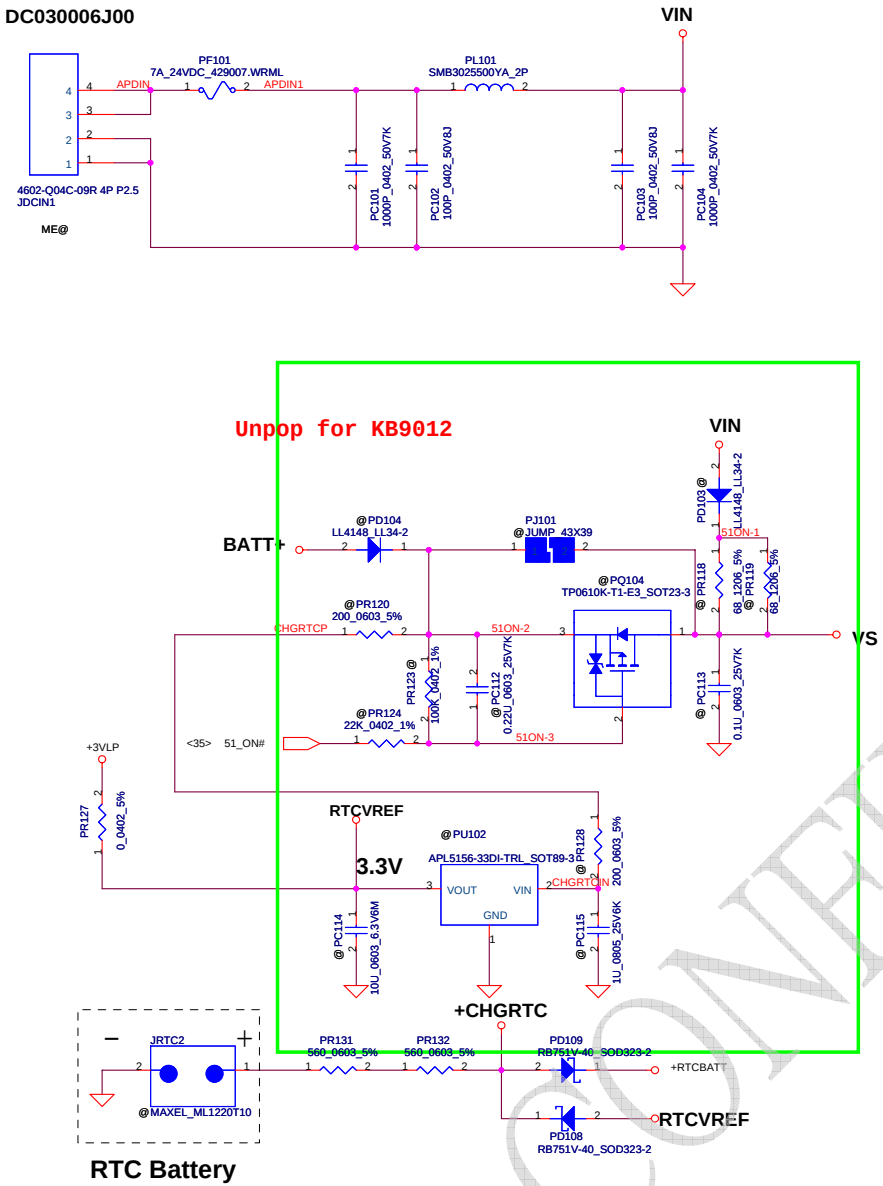


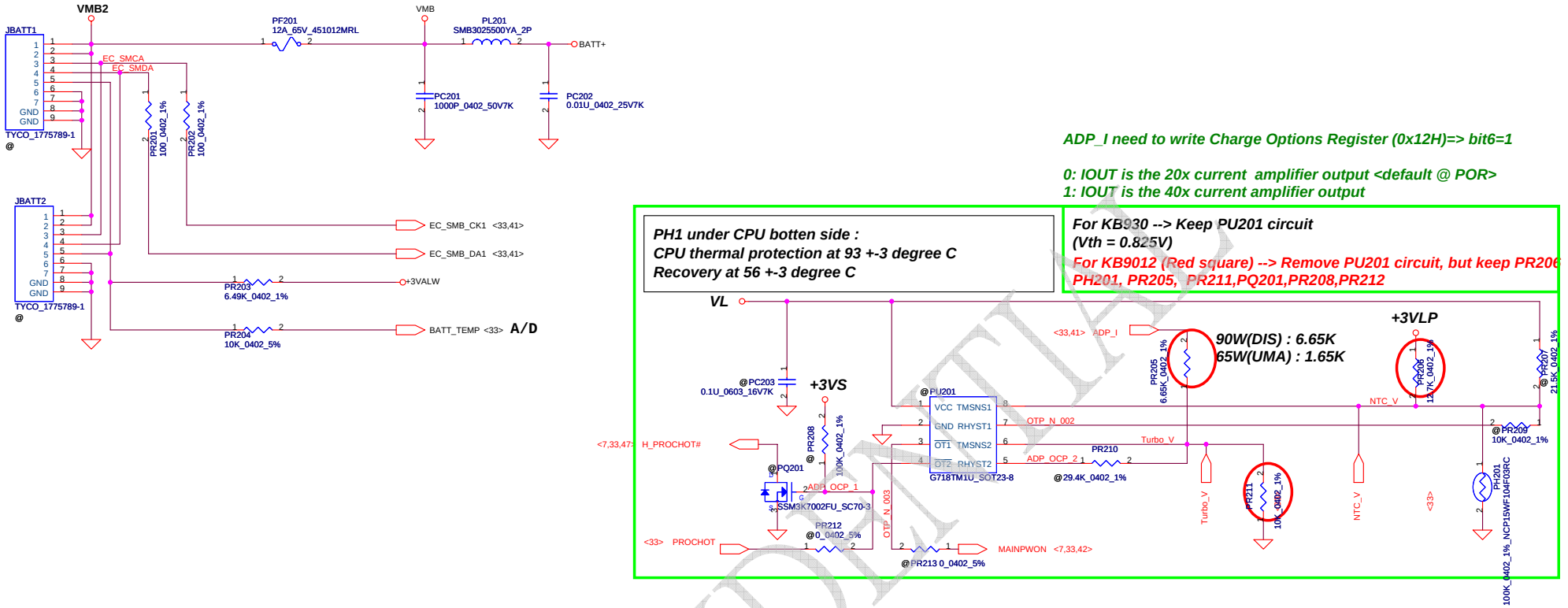
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: PWR DCIN / Vin Detector /Pre-charge

Size	Document Number	Rev
Custom	LA8611P	0.1

Date: Friday, November 04, 2011 Sheet 39 of 51



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: LA8611P | Rev: 0.1

Date: Friday, November 04, 2011 | Sheet 40 of 51

Need EC write ChargeOption() bit[8]=0
Setting (ACP to PHASE Rising Threshold)=1350mV(min)

SH00000AA00

SH000005Y80

SA000051W00

CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

For disable pre-charge circuit.

Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: CHARGER

Size | Document Number: LA8611P | Rev: 0.1

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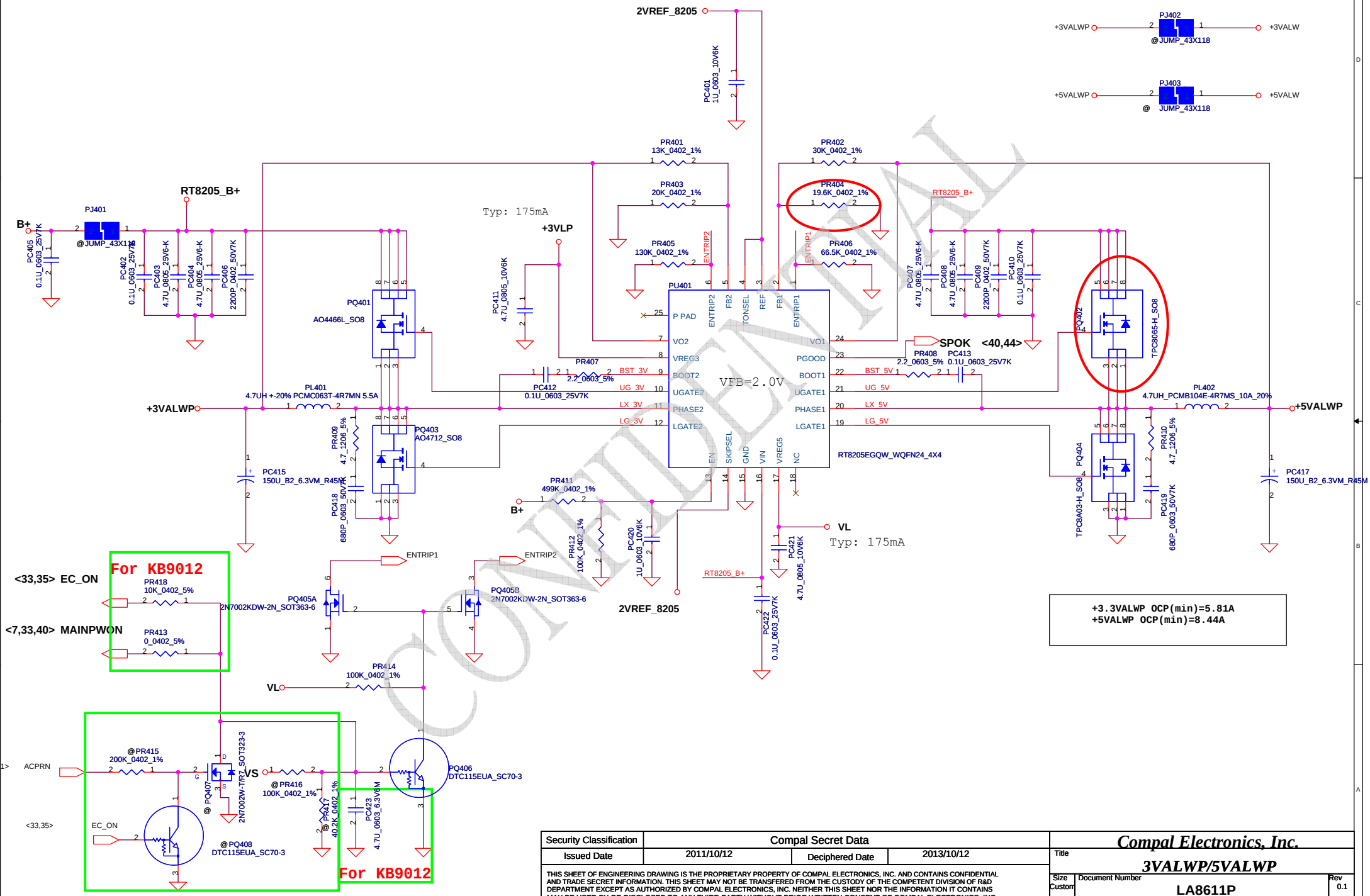
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



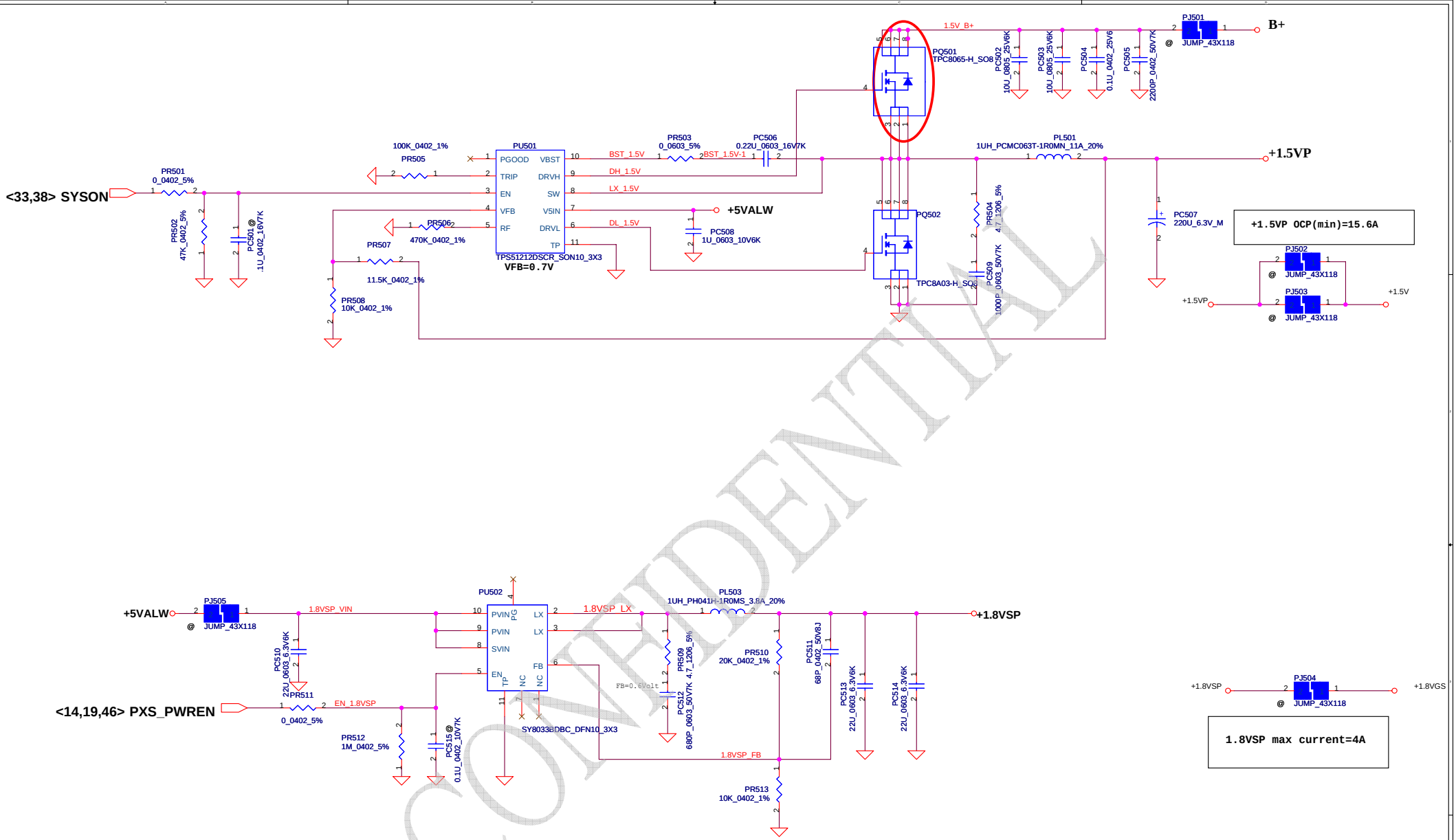
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

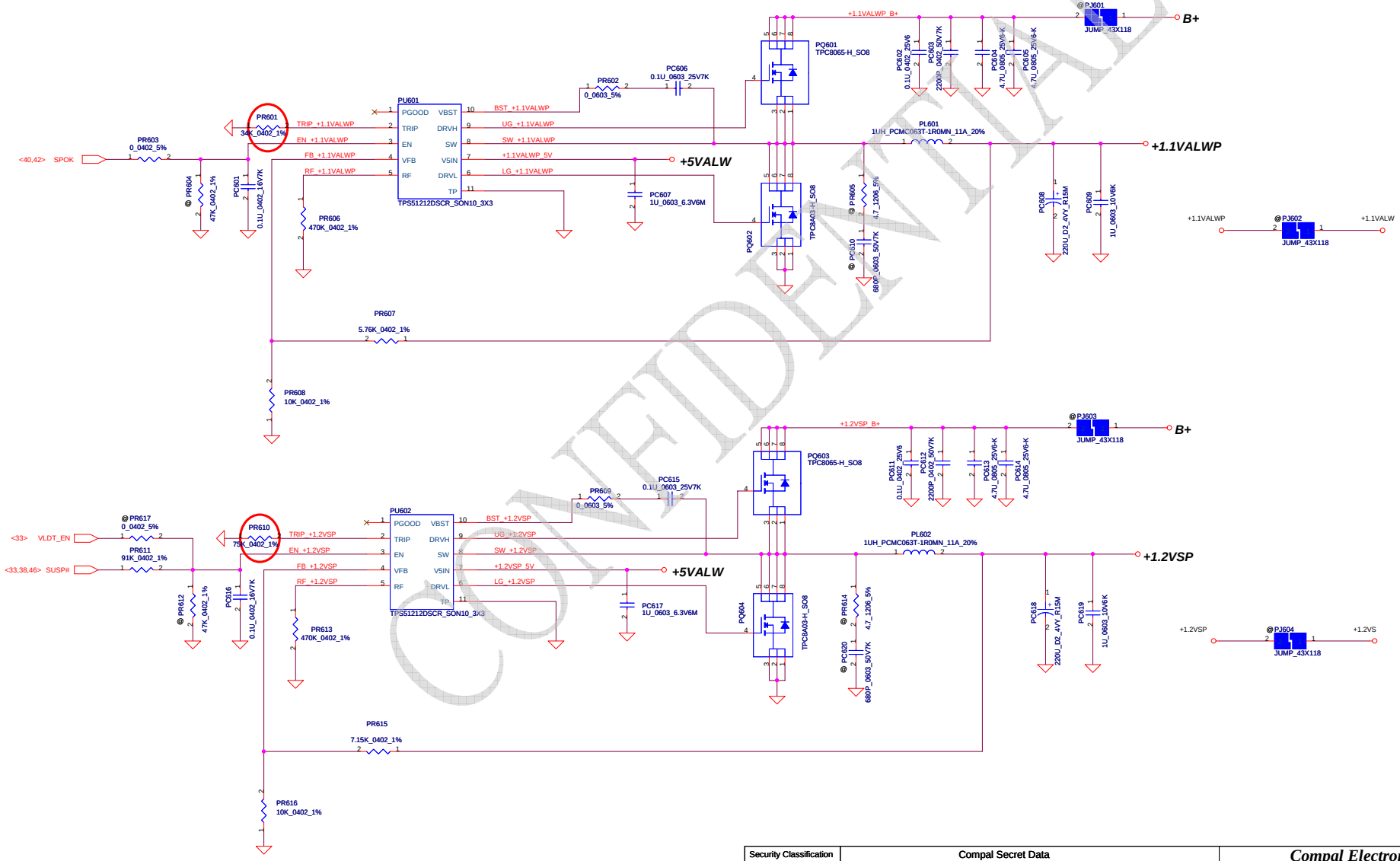
Size	Document Number	Rev
Custom	LA8611P	0.1

Date: Friday, November 04, 2011 Sheet 42 of 51



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.			
Title	PWR-+1.5VP/+1.8VSP		
Size: Custom	Document Number: LA8611P		Rev: 0.1
Date: Friday, November 04, 2011	Sheet 43 of 51		



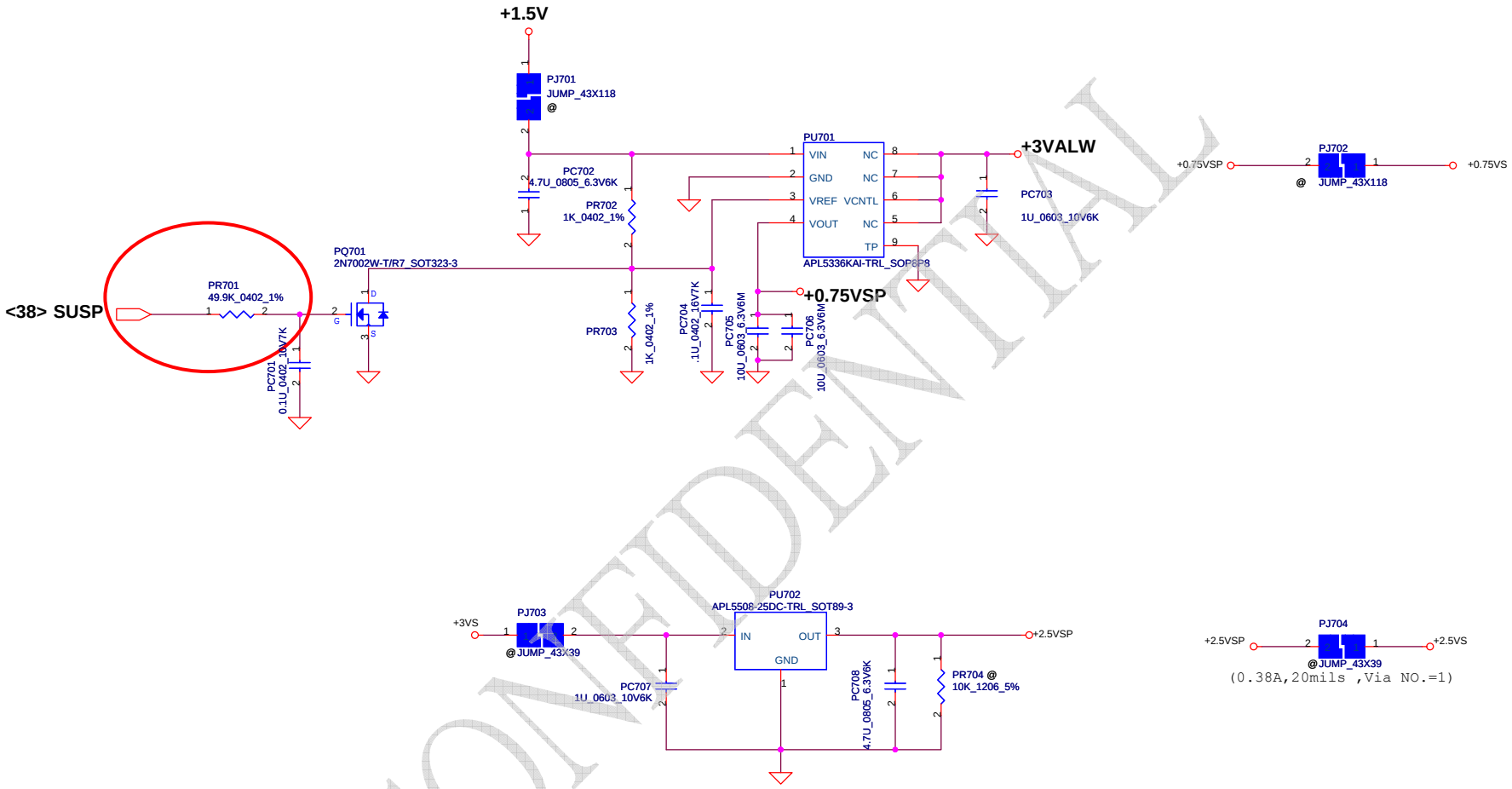
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: PWR +1.1VALWP/+1.2VSP

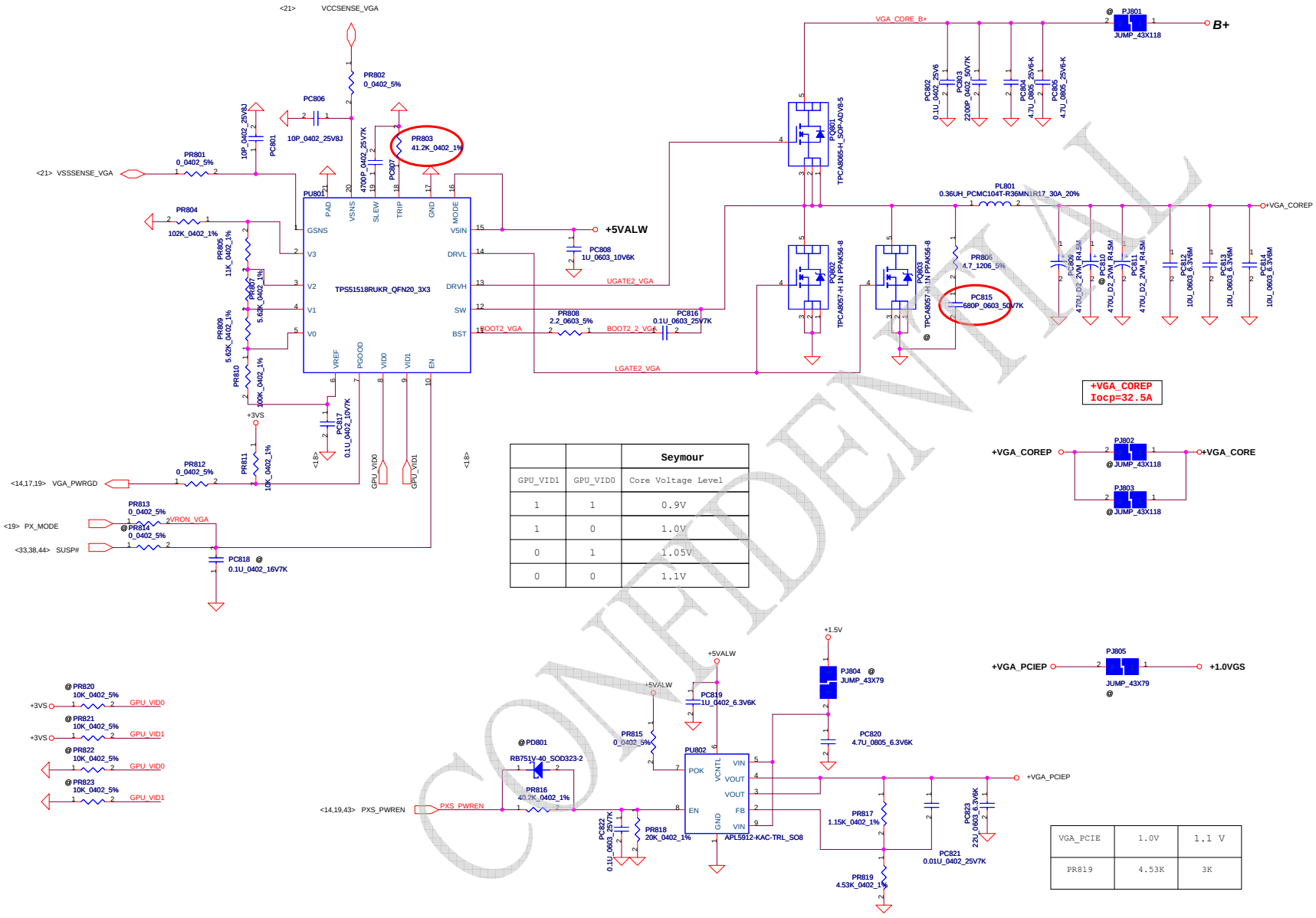
Size	Document Number	Rev
C	LA8611P	0.1

Date: Friday, November 04, 2011 | Sheet 44 of 51



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.		
Title	PWR +0.75VSP/2.5VSP	
Size: Custom	Document Number: LA8611P	Rev: 0.1
Date: Friday, November 04, 2011	Sheet 45 of 51	



		Seymour
GPU_VID1	GPU_VID0	Core Voltage Level
1	1	0.9V
1	0	1.0V
0	1	1.05V
0	0	1.1V

VGA_PCIE	1.0V	1.1 V
PR819	4.53K	3K

Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: **PWR-VGA_CORE/VGA_PCIE**

Size	Document Number	Rev
	LA8611P	0.1

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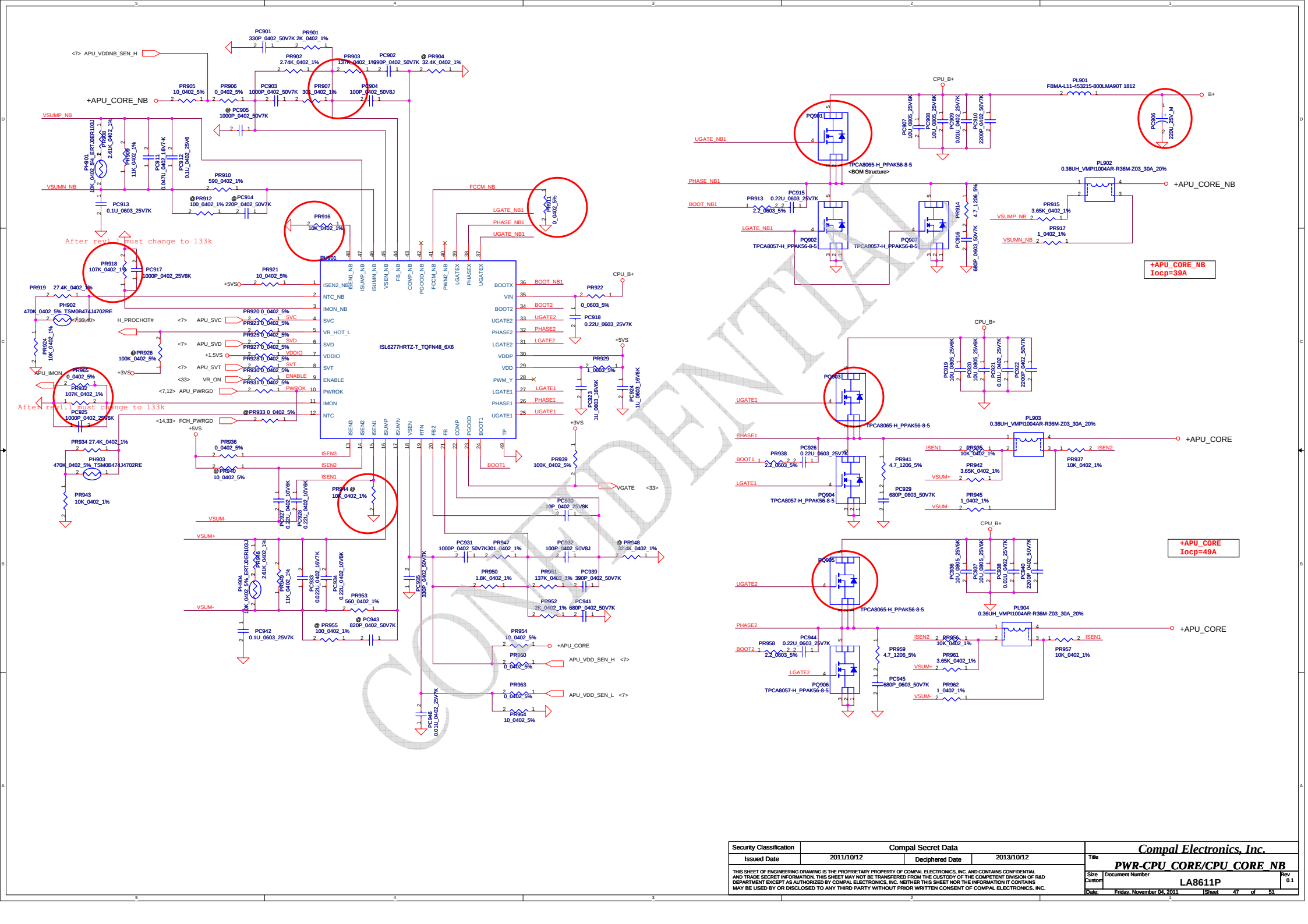

Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

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Compal Electronics, Inc.

Title: PWR-CPU_CORE/CPU_CORE_NB

Size	Document Number	Rev
Custom	LA8611P	0.1

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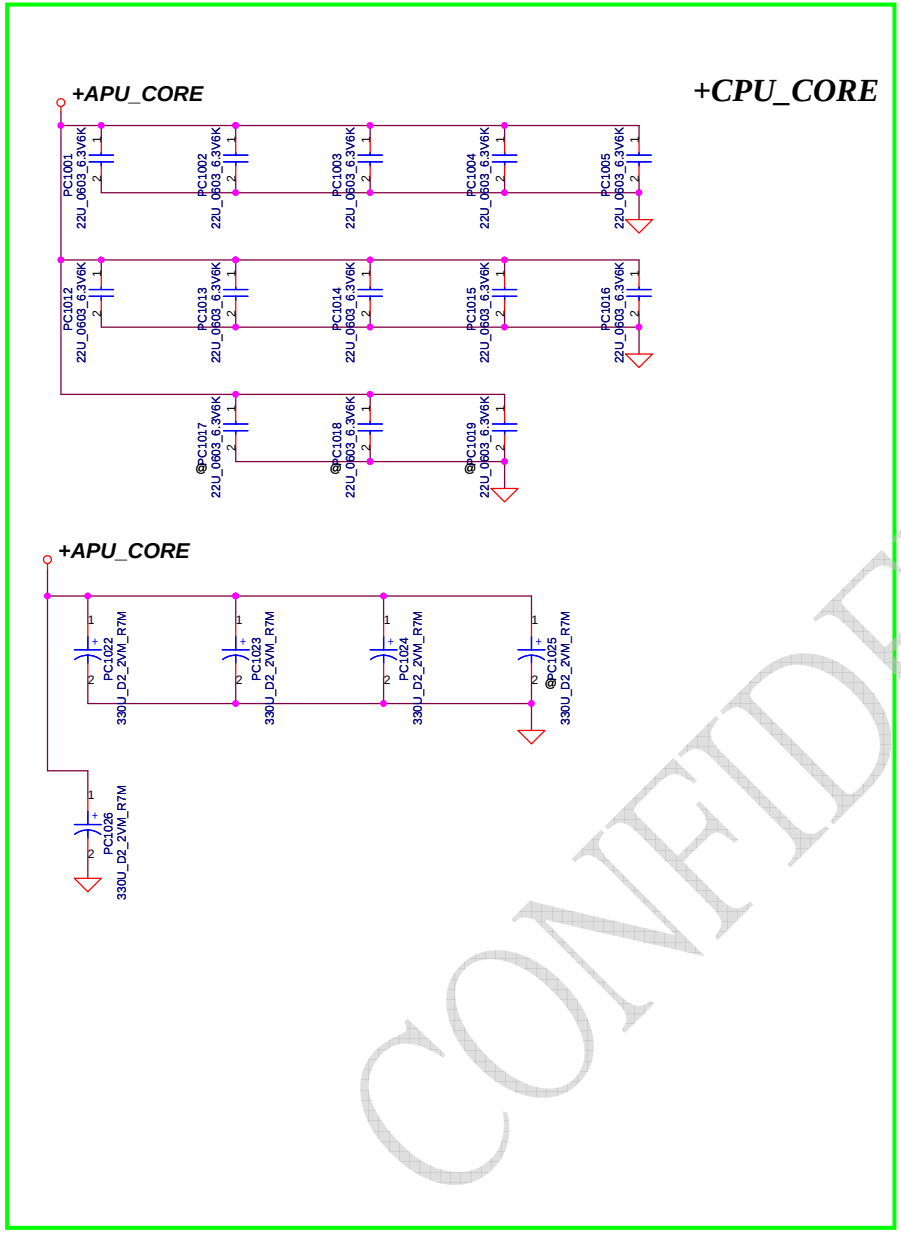
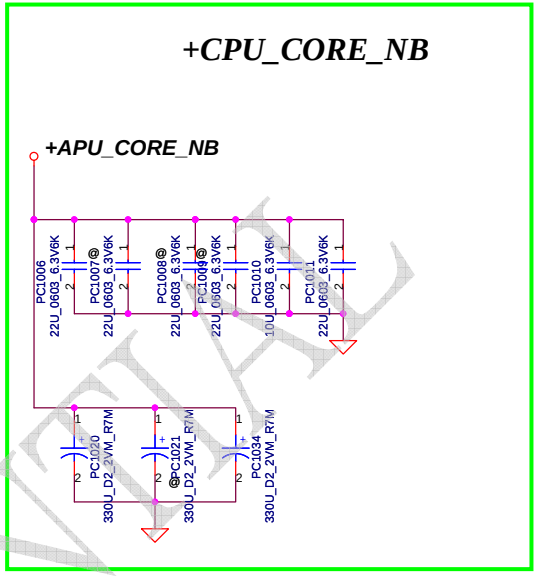
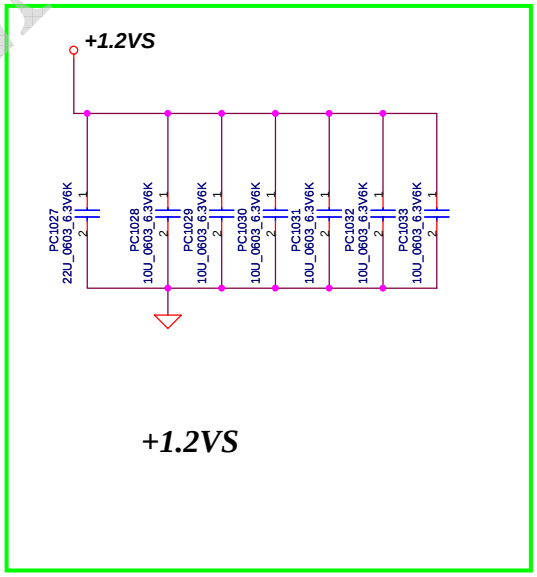






Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.		
Title: PWR - PROCESSOR DECOUPLING		
Size	Document Number: LA8611P	Rev: 0.1
Date: Friday, November 04, 2011	Sheet 48 of 51	

Version change list (P.I.R. List)

for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

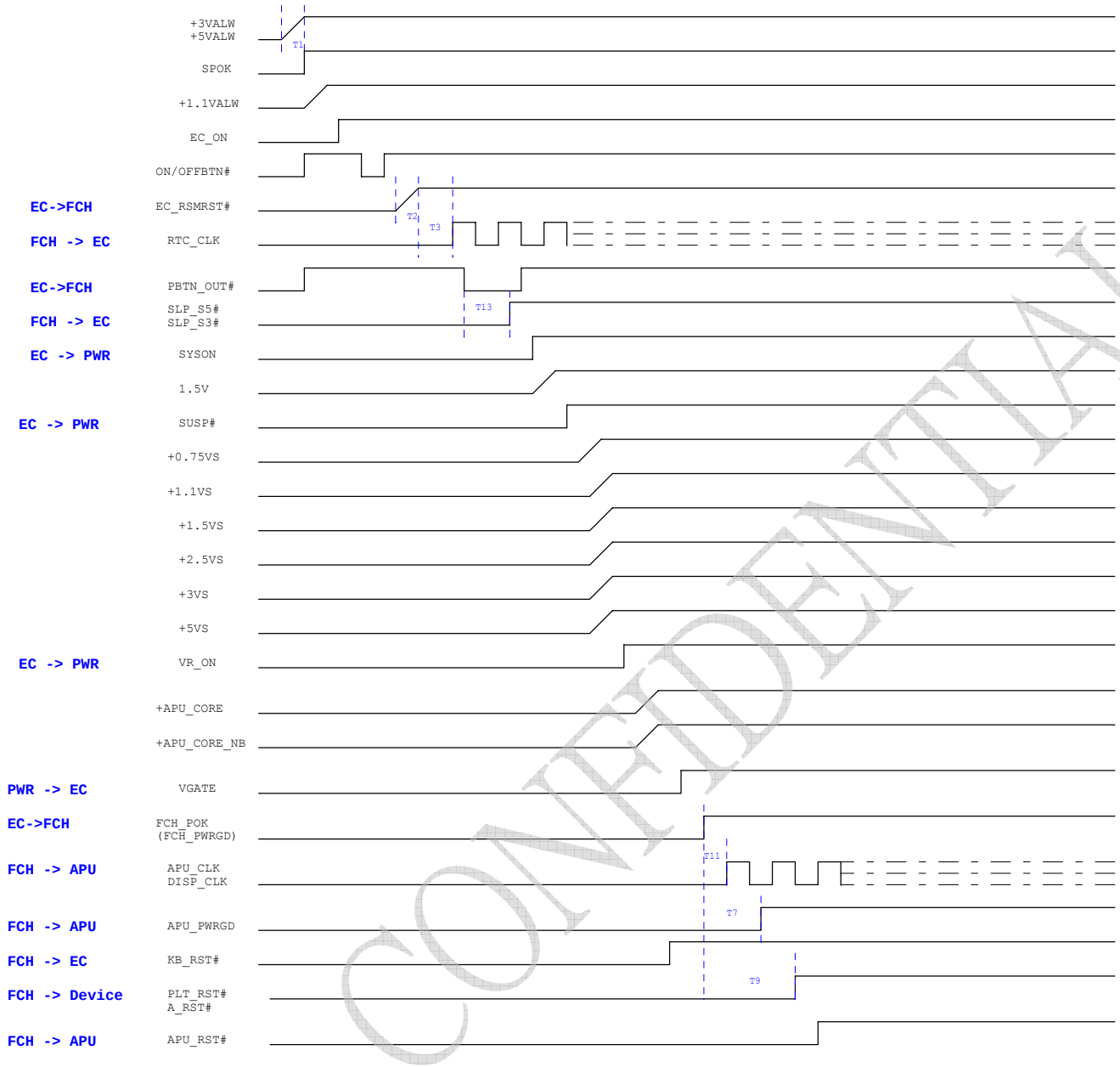
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: **PIR (PWR)**

Size	Document Number	Rev
Custom	LA8611P	0.1

Date: Friday, November 04, 2011 | Sheet 49 of 51



1ms< T1 < 100ms : +3VALW rising time, for LAN chip request

+3VALW need rampe up before +1.1VALW or at the same time.

T2 < 50ms : EC_RSMRST# rising time

+3VALW need rampe up before EC_RSMRST# de-assertion at least 10ms

+1.1VALW need rampe up before EC_RSMRST# de-assertion

T3 > 16ms : EC_RSMRST# de-assert to start RTCCLK

T13 > 200ns : PBTN_OUT# to SLP_S3#/S5# de-assertion

T11< 32ms : FCH_POK assertion to clock out

98ms< T7< 150ms : FCH_POK assertion to APU_PWRGD

KB_RST# should be de-asserted before FCH_POK

101ms< T9< 113ms : FCH_POK assertion to A_RST# de-assertion

Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: Power sequence

Size	Document Number	Rev
A3	LA8611P	0.1

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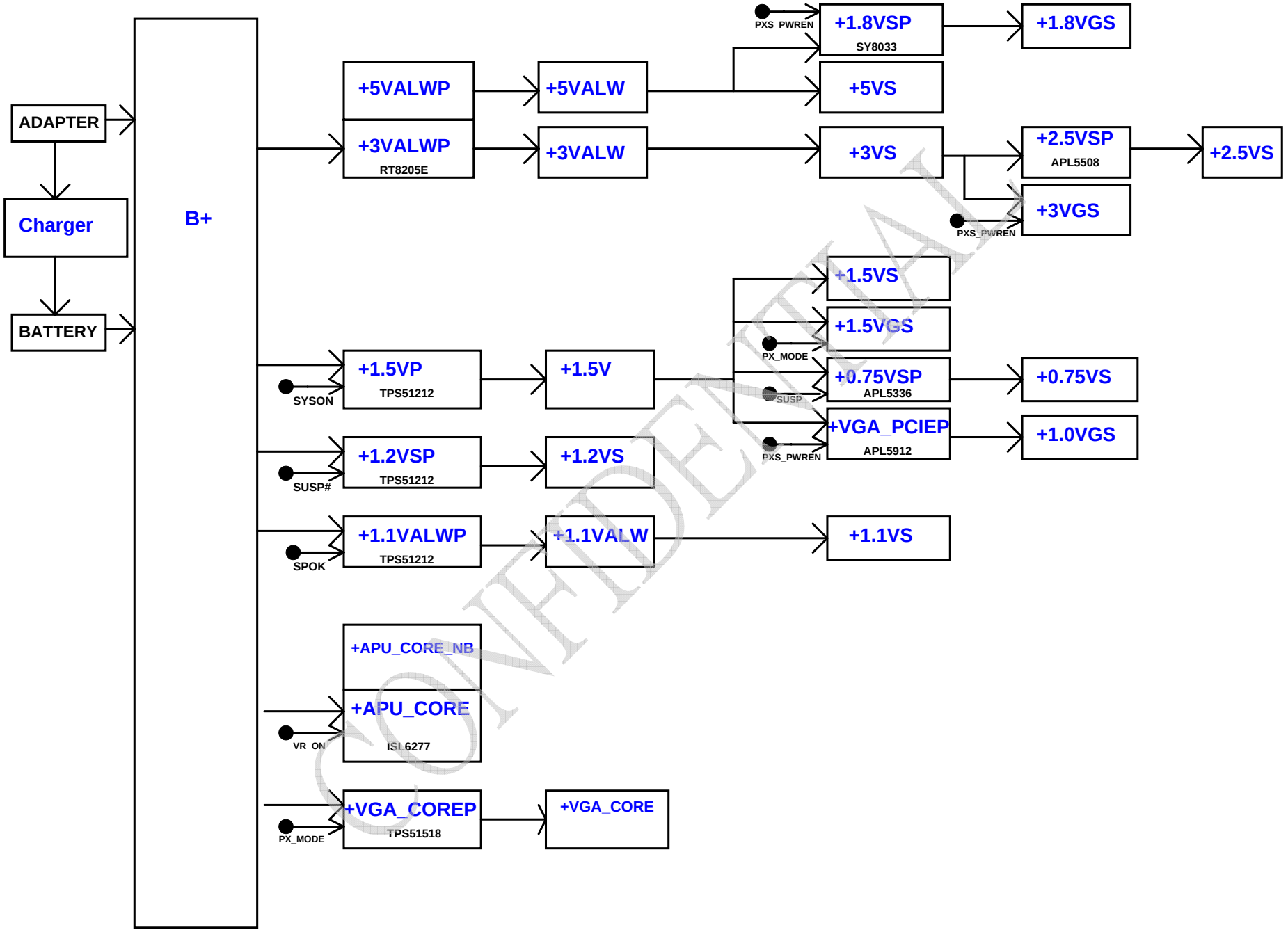

Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: Power diagram

Size	Document Number	Rev
C	LA8611P	0.1

Date: Wednesday, November 09, 2011 Sheet 51 of 51