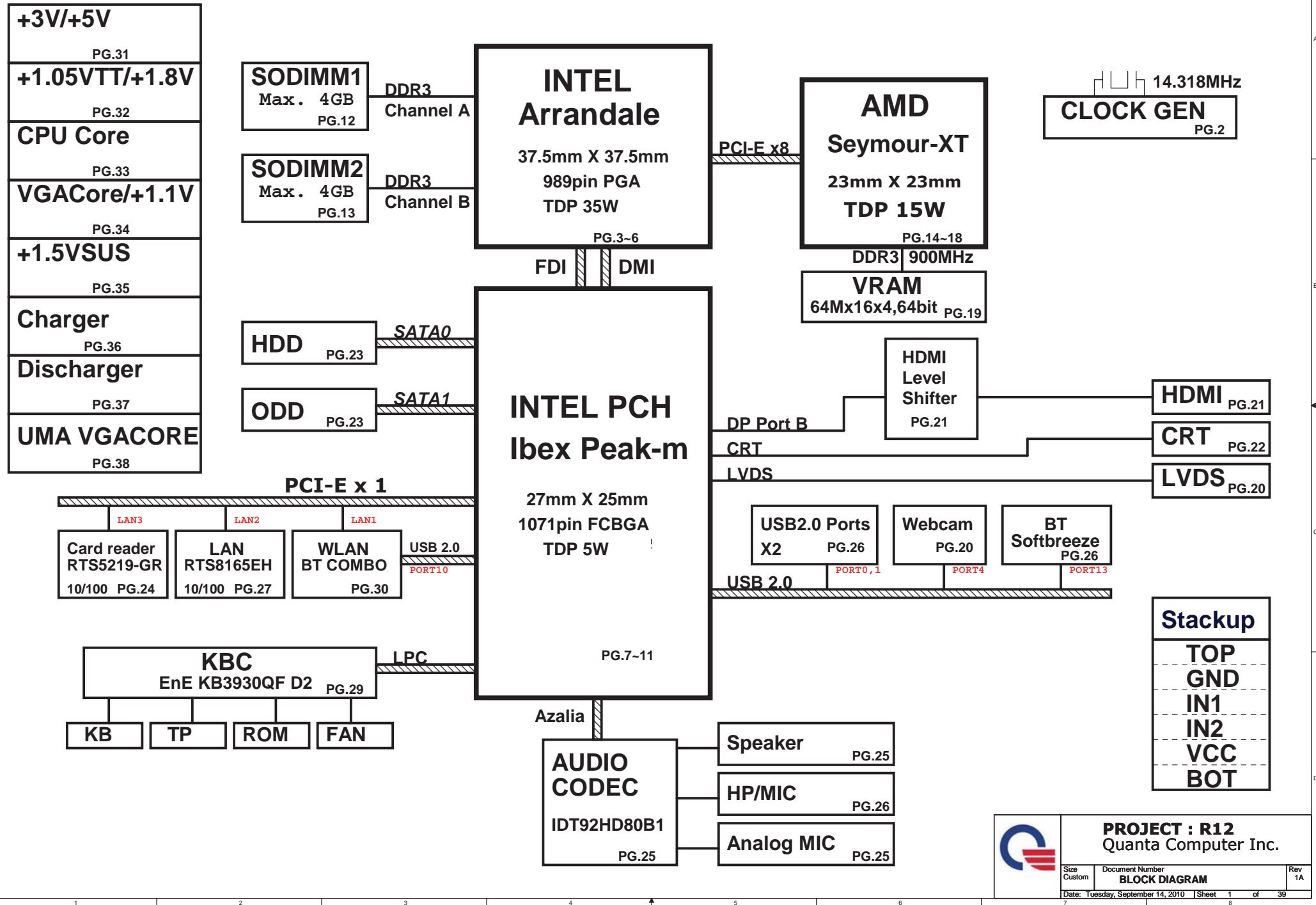
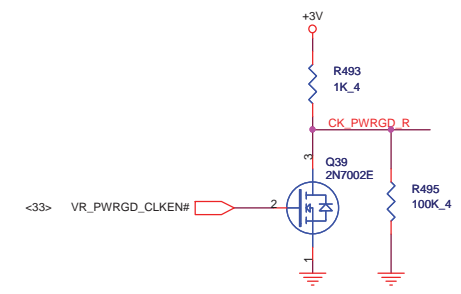
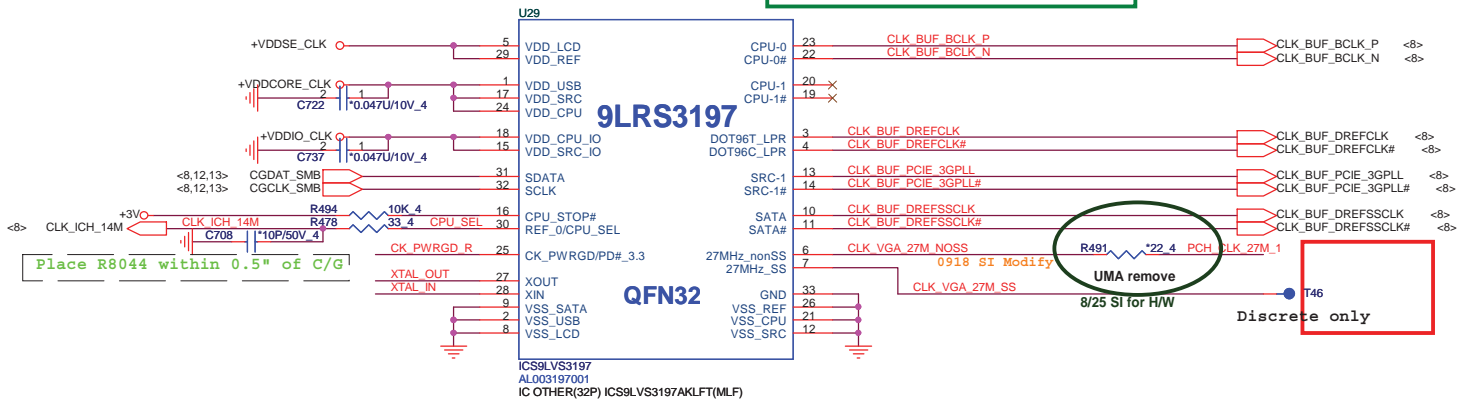
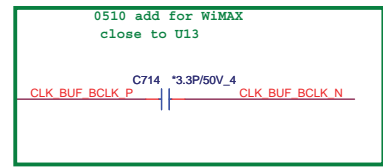
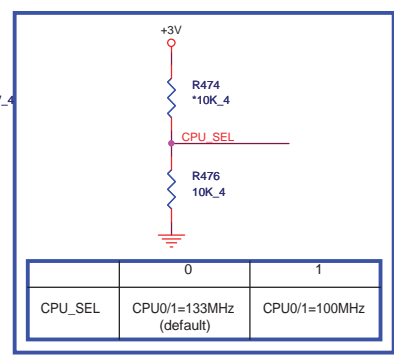
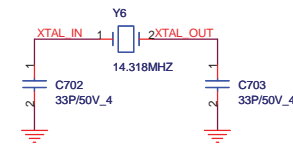
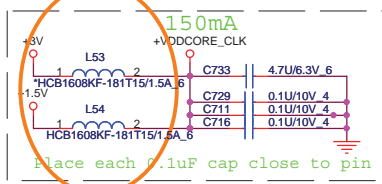
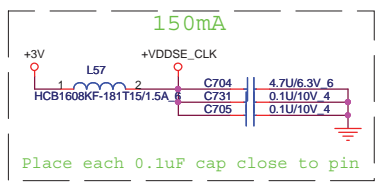
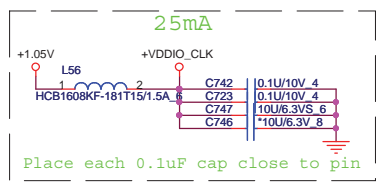


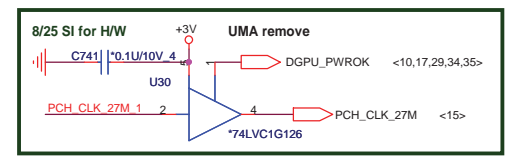
R12 INTEL UMA/DISCRETE SYSTEM DIAGRAM



PROJECT : R12
Quanta Computer Inc.

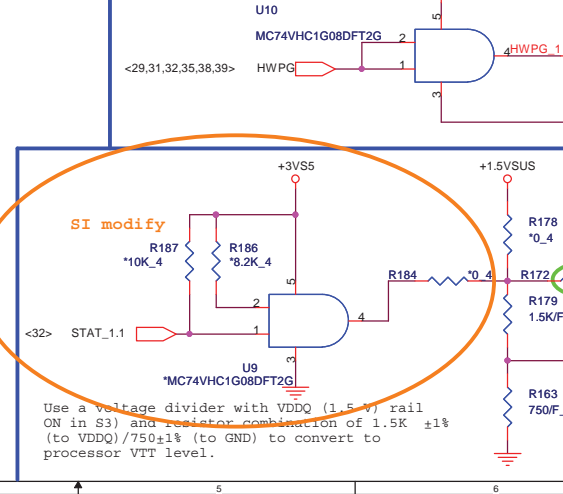
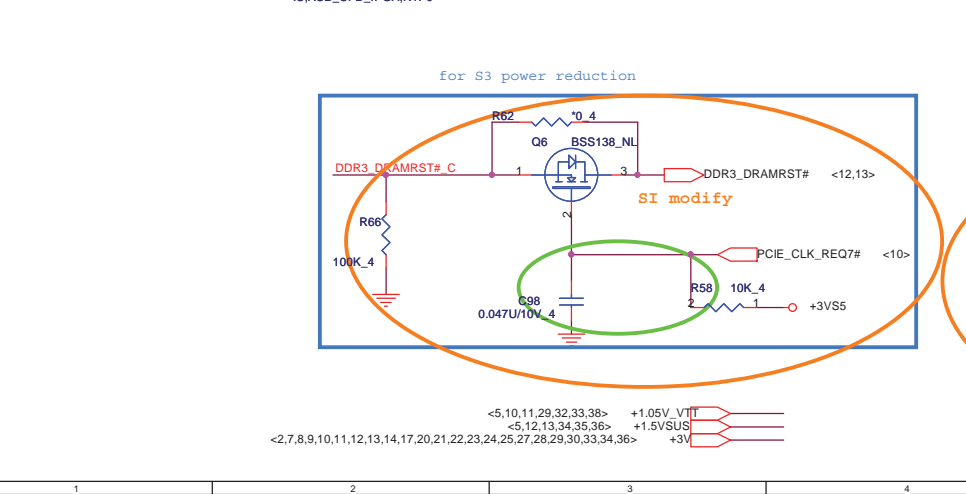
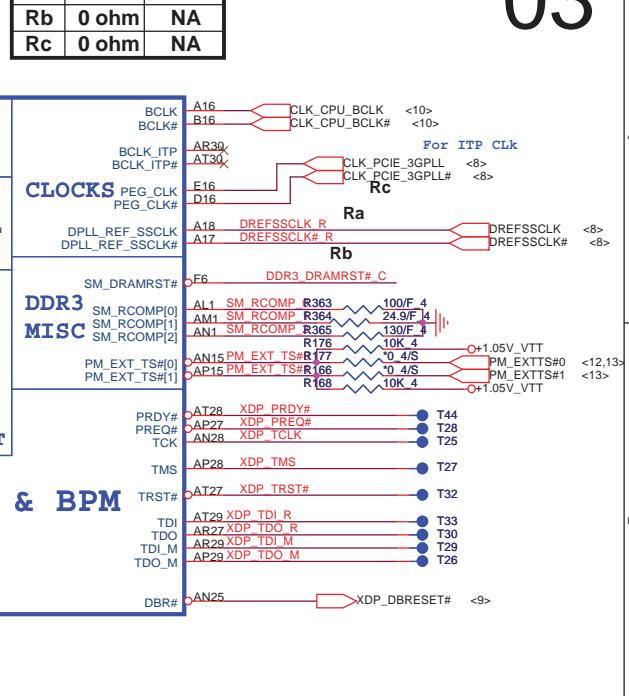
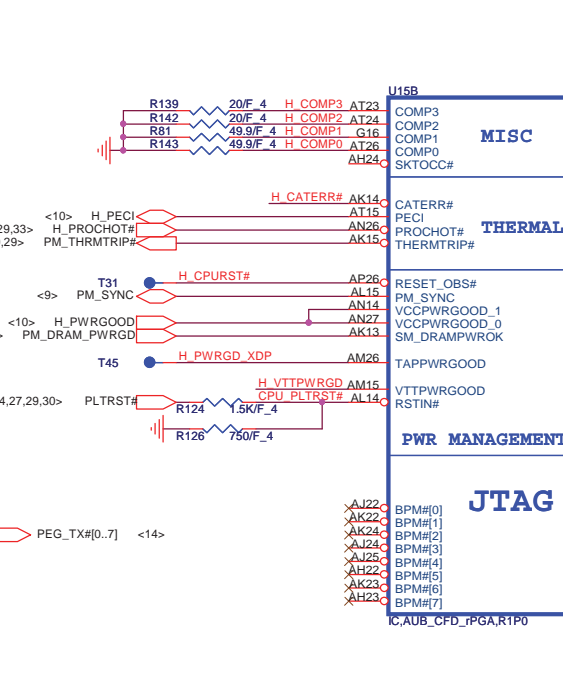
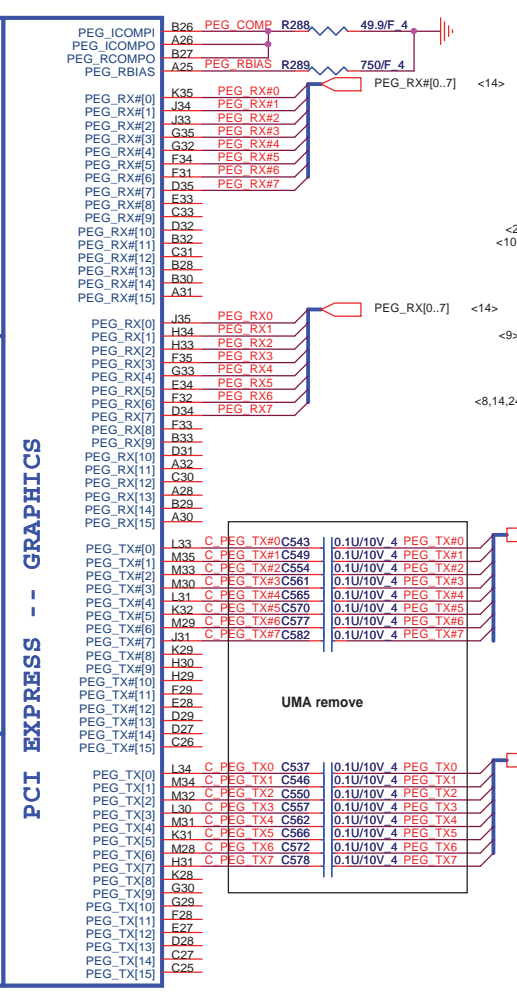
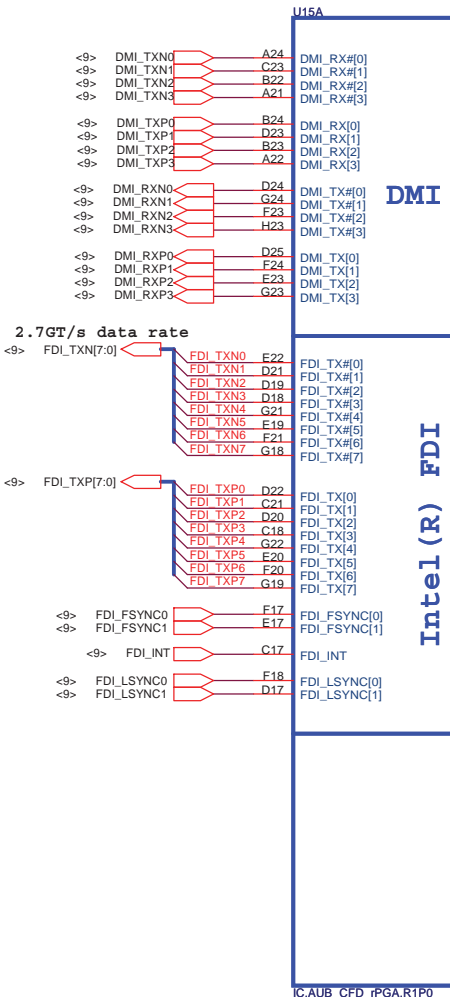


Vender	Part	Part Number	Part Description
ICS	ICS9LVS3197	AL003197000	IC OTHER(32P) ICS9LVS3197AKLFT(MLF)
Realtek	RTM890N-632	AL000890000	IC OTHER(32P) RTM890N-632-GRT(QFN)
Silego	SLG8LV595VTR	AL000595000	IC OTHER(32P)SLG8LV595VTR(QFN)



+1.05V <7,8,9,11,39>
 +1.5V <5,30>
 +3V <3,7,8,9,10,11,12,13,14,17,20,21,22,23,24,25,27,28,29,30,33,34,36>

Ra	DIS	UMA
Rb	0 ohm	NA
Rc	0 ohm	NA



JTAG MAPPING

XDP_TDI R Ra

XDP_TDO M Rb

XDP_TDI M Rd

XDP_TDO R Re

XDP_TRST# R147

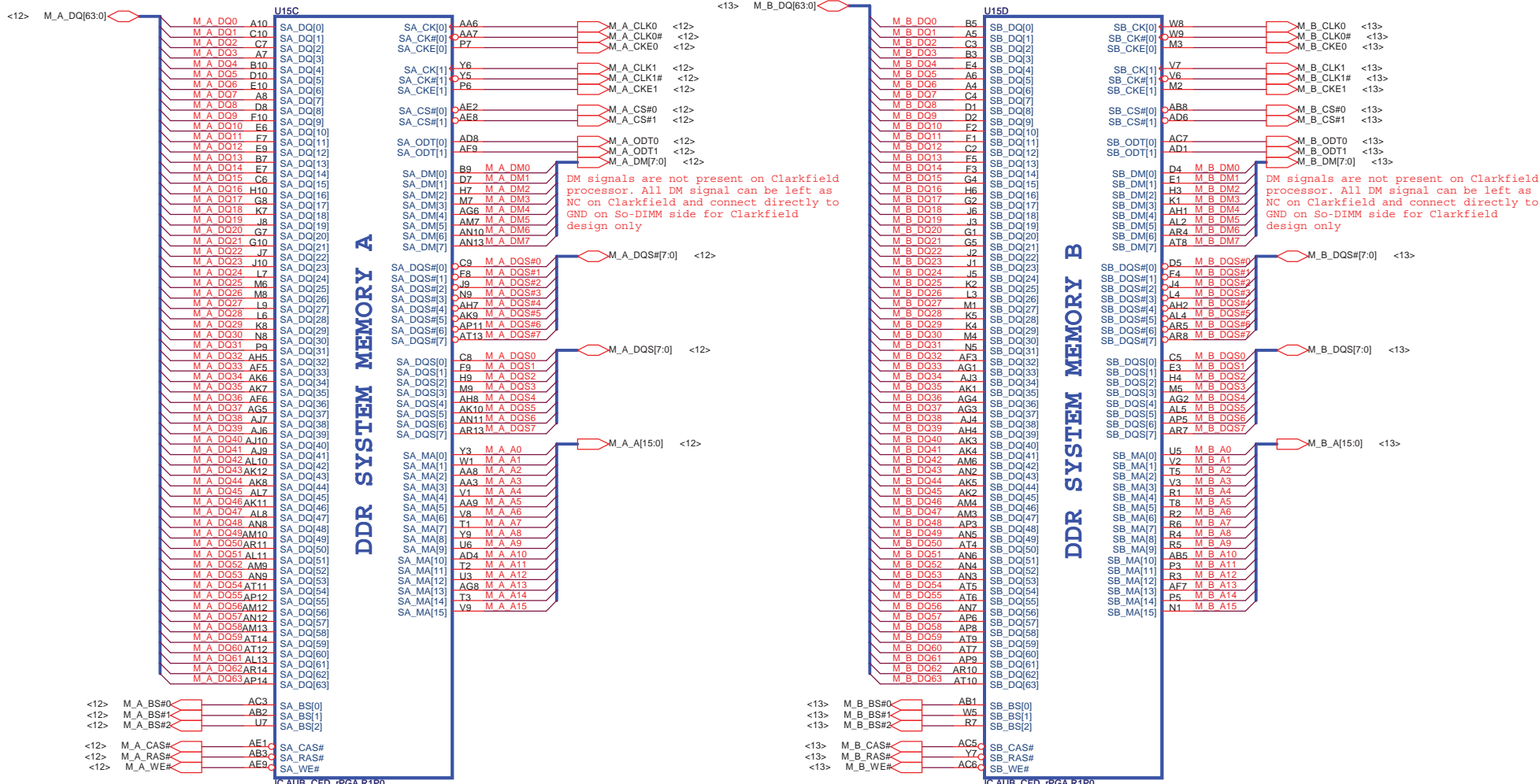
Scan Chain (Default)	STUFF -> Ra, Rc, Re NO STUFF -> Rb, Rd
CPU Only	STUFF -> Ra, Rb NO STUFF -> Rc, Rd, Re
GMCH Only	STUFF -> Rd, Re NO STUFF -> Ra, Rb, Rc

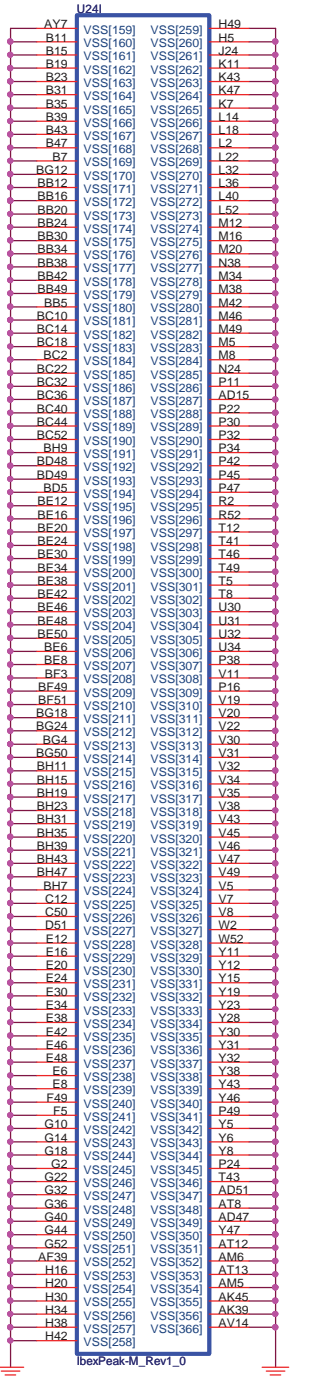
PROJECT : R12
Quanta Computer Inc.

Size Custom Document Number PROCESSOR 1/4(HOST&PEX) Rev 1A

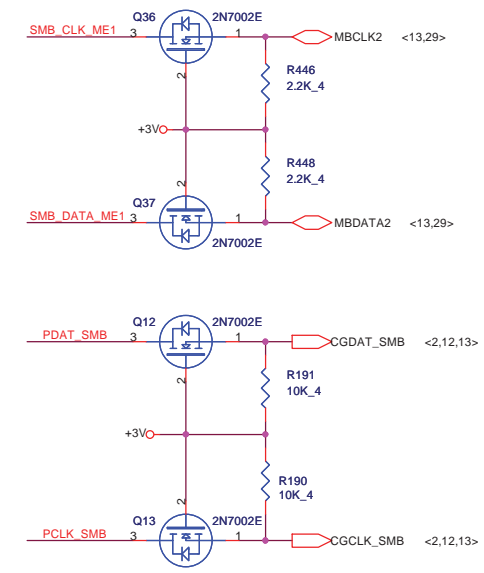
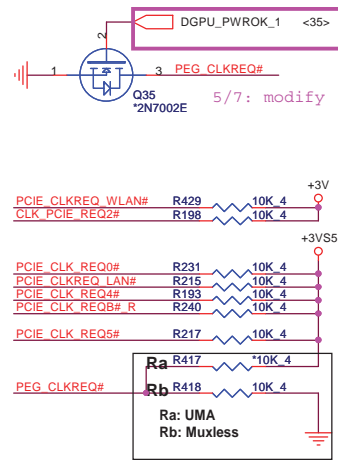
Date: Sunday, September 19, 2010 Sheet 3 of 39

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

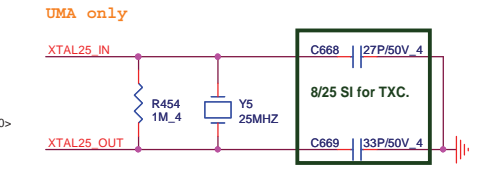
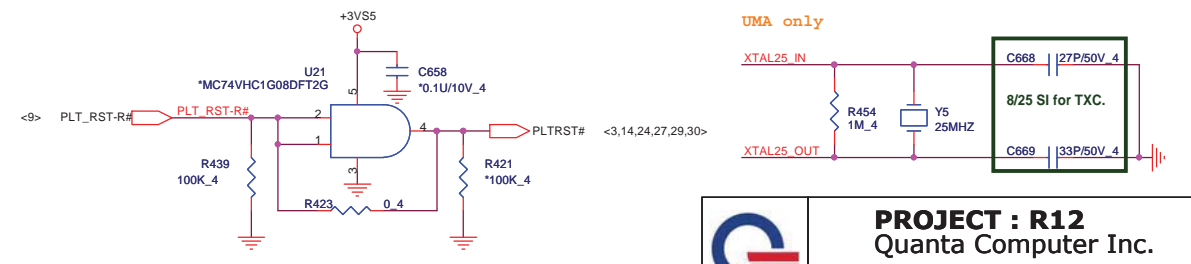
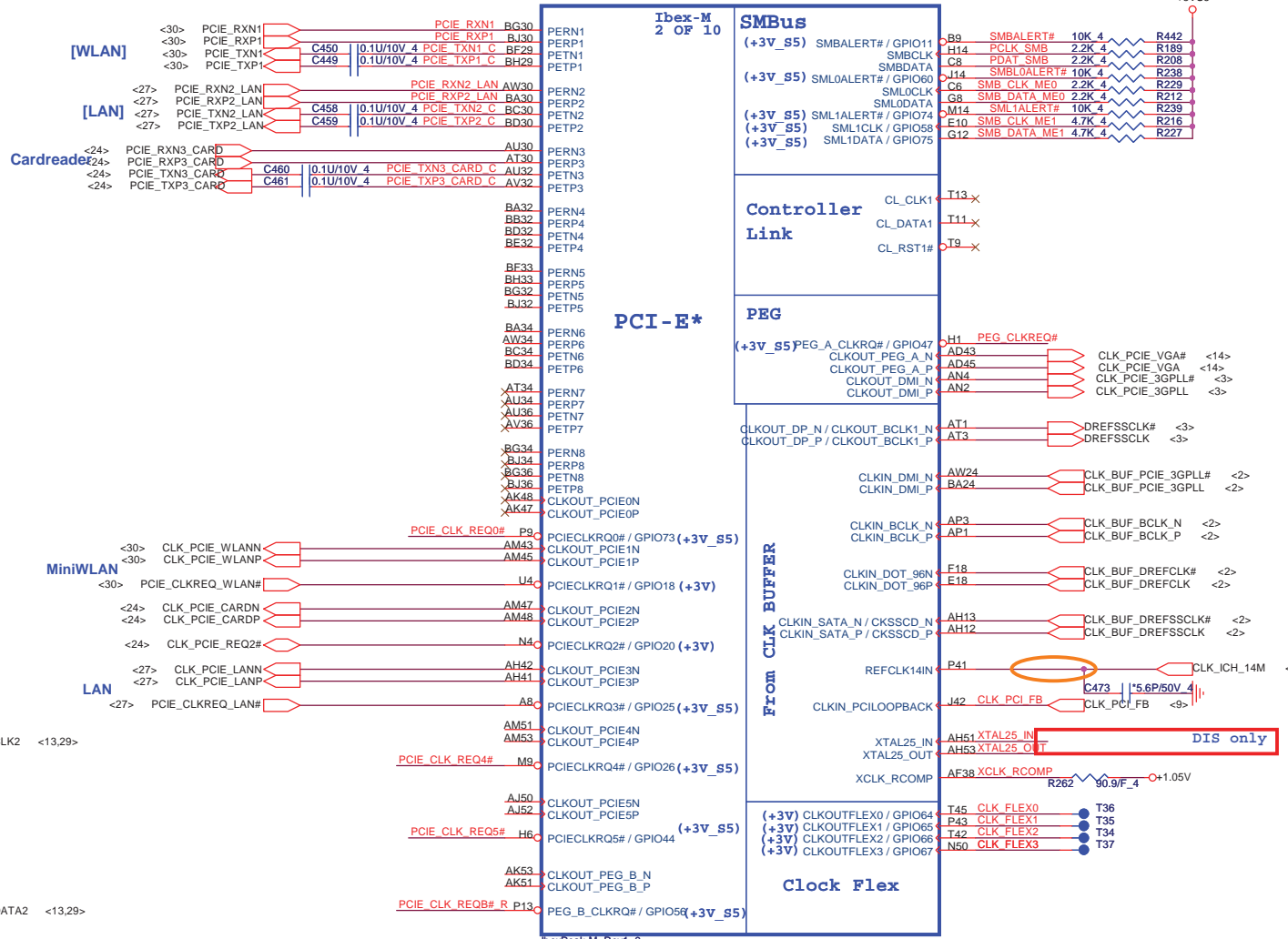




PEG Clock detect (SG only)



IBEX PEAK-M (PCI-E,SMBUS,CLK)



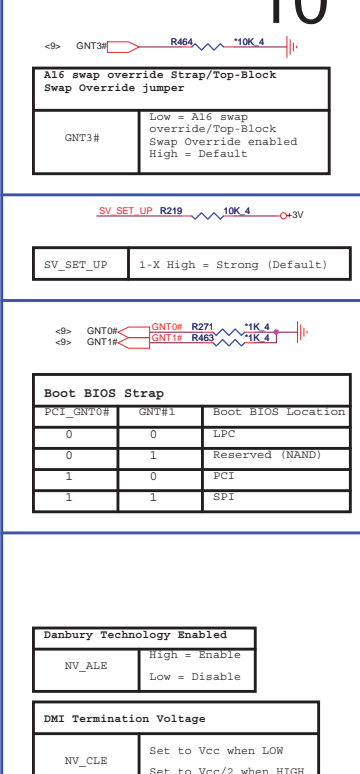
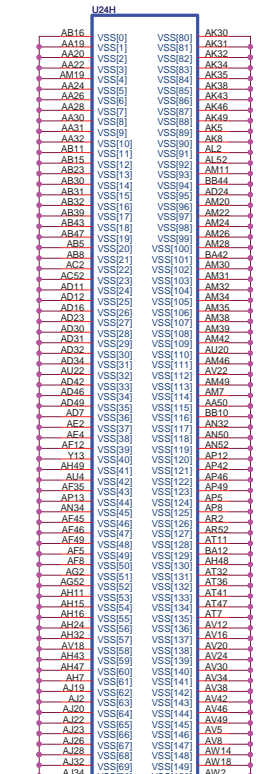
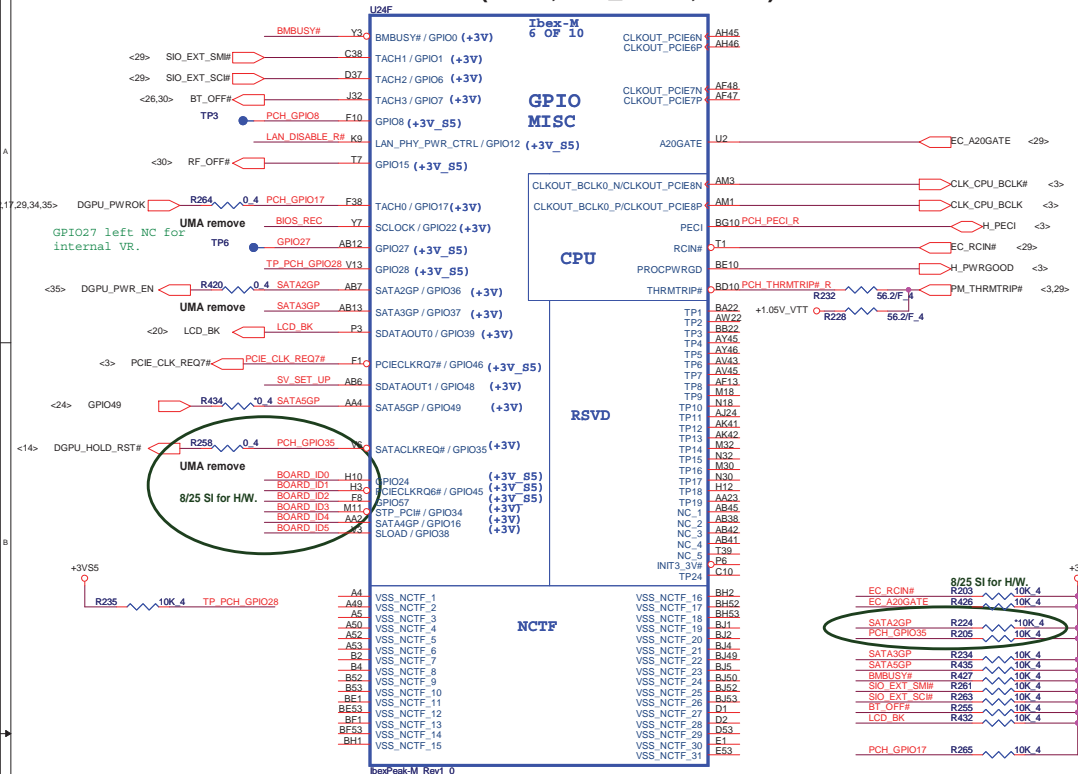
PROJECT : R12
Quanta Computer Inc.

Size Custom	Document Number PCH 2/5 (PCI-E, SMBUS, CK)	Rev 1A
Date: Sunday, September 19, 2010 Sheet 8 of 39		

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

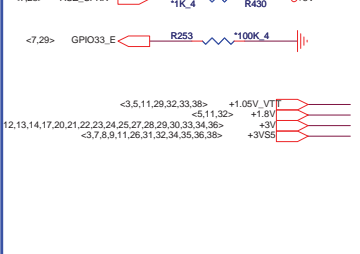
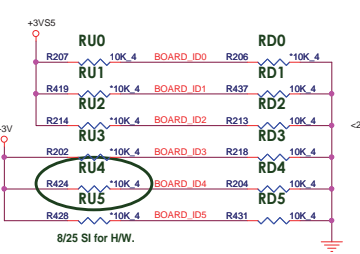
IBEX PEAK-M (GND)

10



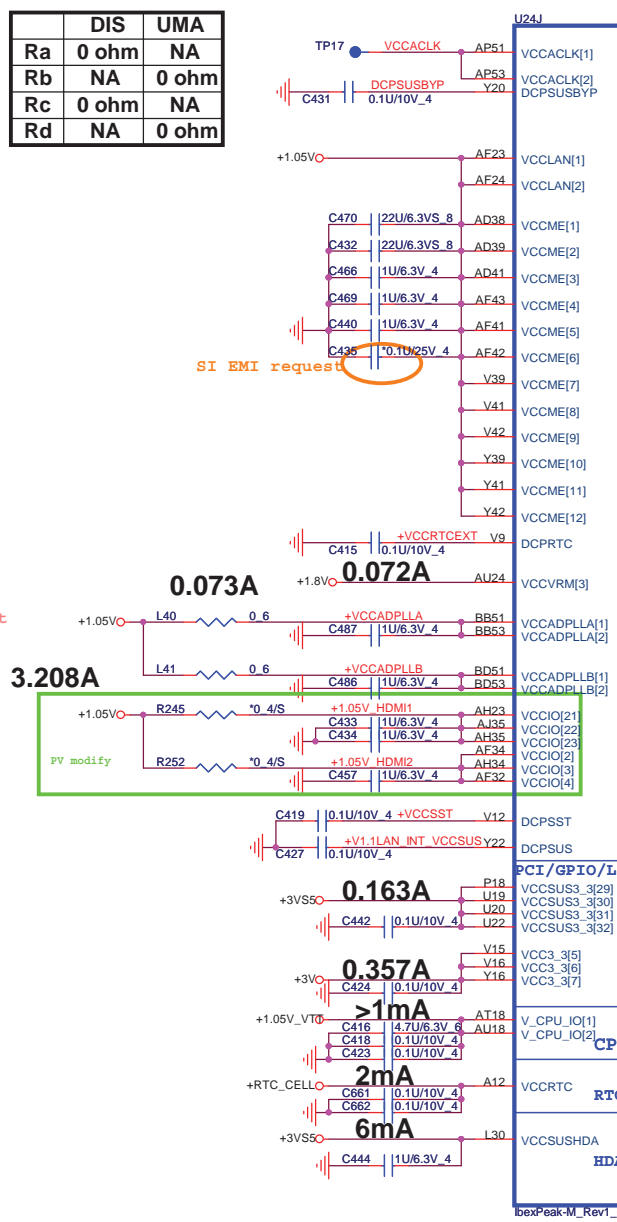
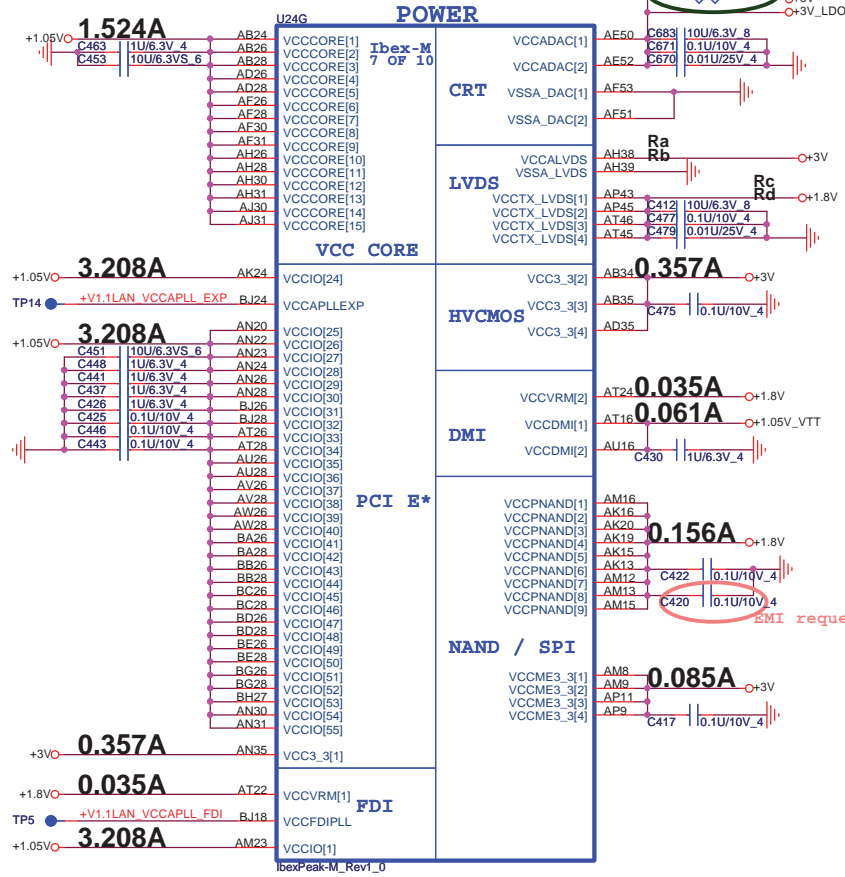
R12.MB P/N	ID0	ID1	ID2	ID3	ID4	ID5
UMA						
31R12MB0000 (PIM)	0	0	0	0	0	0
31R12MB0010 (PDT)	0	0	0	0	0	0
Seymour XT						
Hynix 512						
31R12MB0020 (PIM)	1	0	0	0	0	0
31R12MB0030 (PDT)	1	0	0	0	0	0
Samsung 512						
Hynix 1G						
31R12MB0060 (PIM)	1	0	0	0	0	0
31R12MB0070 (PDT)	1	0	0	0	0	0
Samsung 1G						
Hynix 1G						
31R12MB0080 (PIM)	1	0	0	0	0	0
31R12MB0090 (PDT)	1	0	0	0	0	0

Board ID	ID0	ID1	ID2	ID3	ID4	ID5
UMA						
UMA/DIS	0=UMA 1=Dis.					
Reserve						
Reserve		0=No 1=Yes				
Reserve			0=No 1=Yes			
Reserve				0=No 1=Yes		
Reserve					0=No 1=Yes	

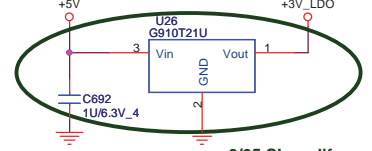


8/25 SI modify
Uninstall on UMA
Install on DIS

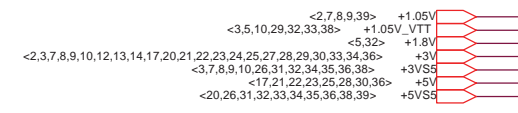
	DIS	UMA
Ra	0 ohm	NA
Rb	NA	0 ohm
Rc	0 ohm	NA
Rd	NA	0 ohm



UMA Only, If have power noise issue then stuff it.

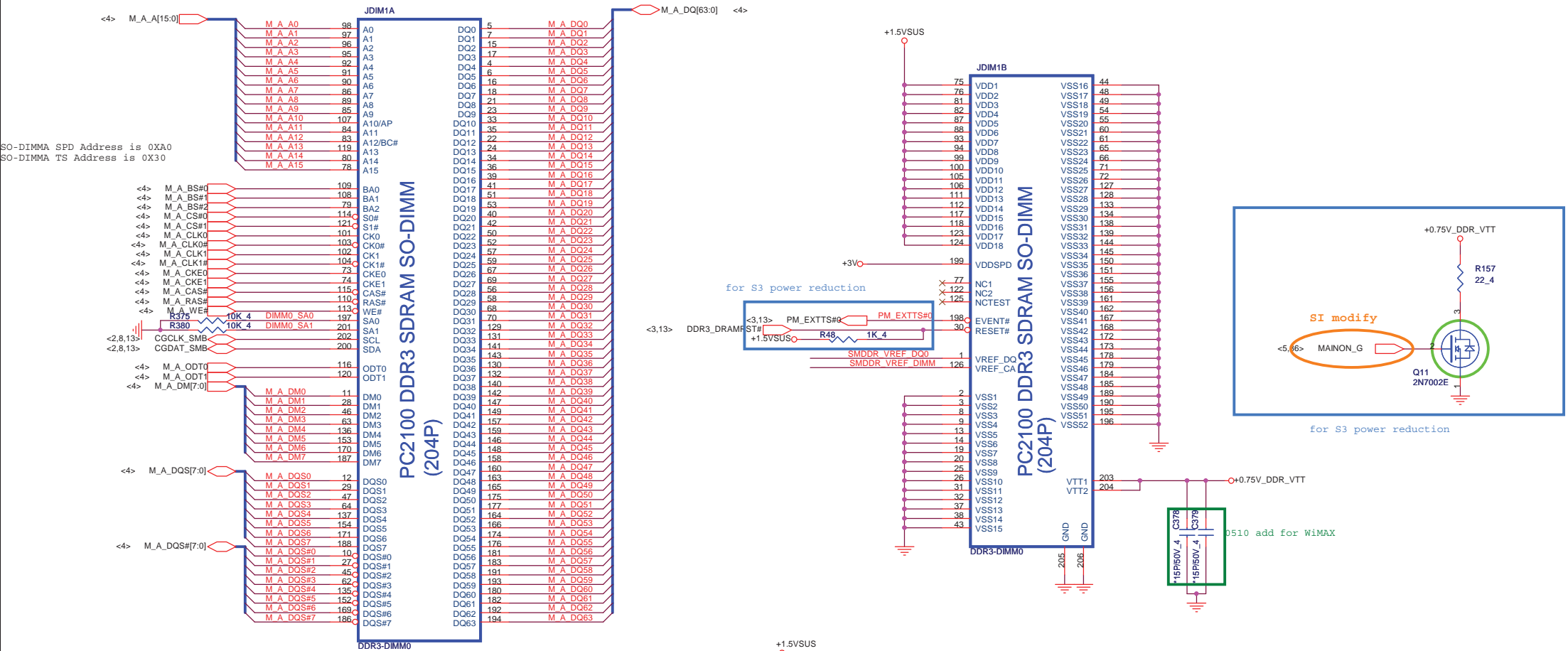


8/25 SI modify
Install LDO when UMA

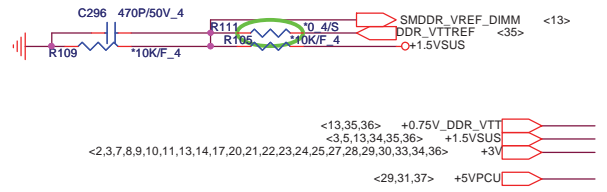
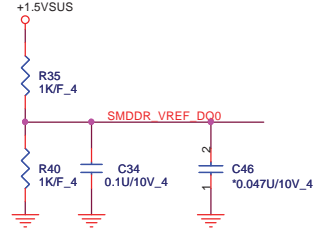
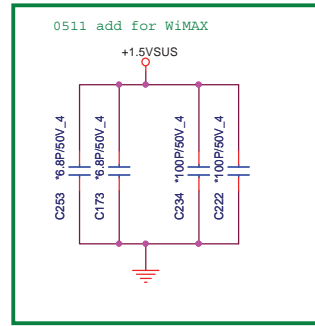
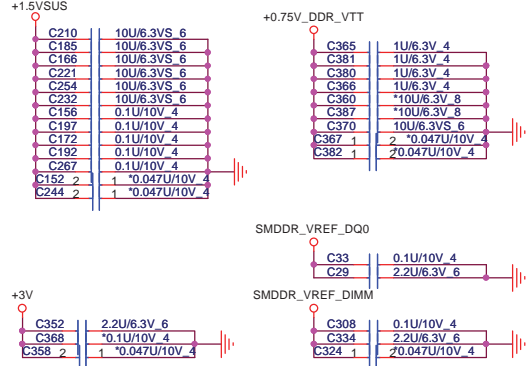


PROJECT : R12
Quanta Computer Inc.

Size Custom	Document Number PCH 5/5 (POWER)	Rev 1A
Date: Sunday, September 19, 2010 Sheet 11 of 39		

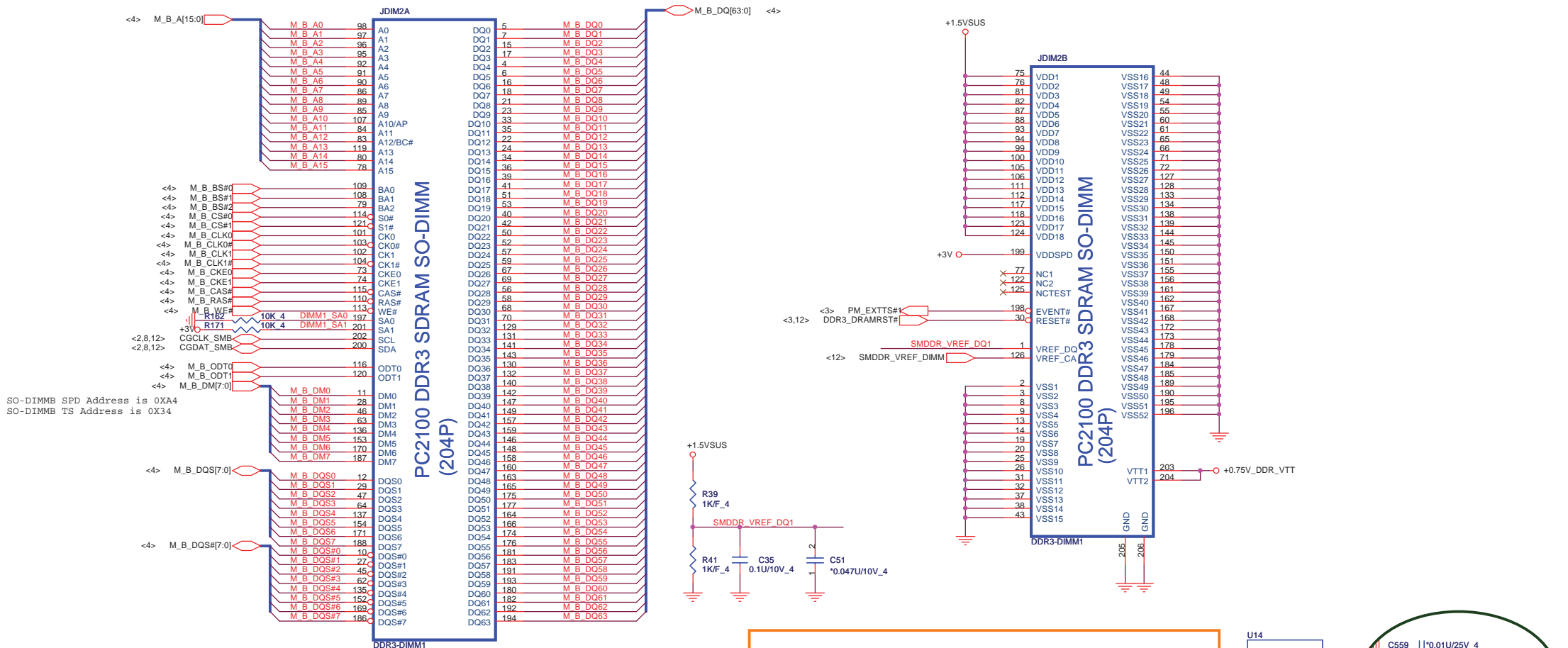


Place these Caps near So-Dimm0.
 Some Projects replace 10UF 0805 by 4.7UF 0603
 It can cost down 30%



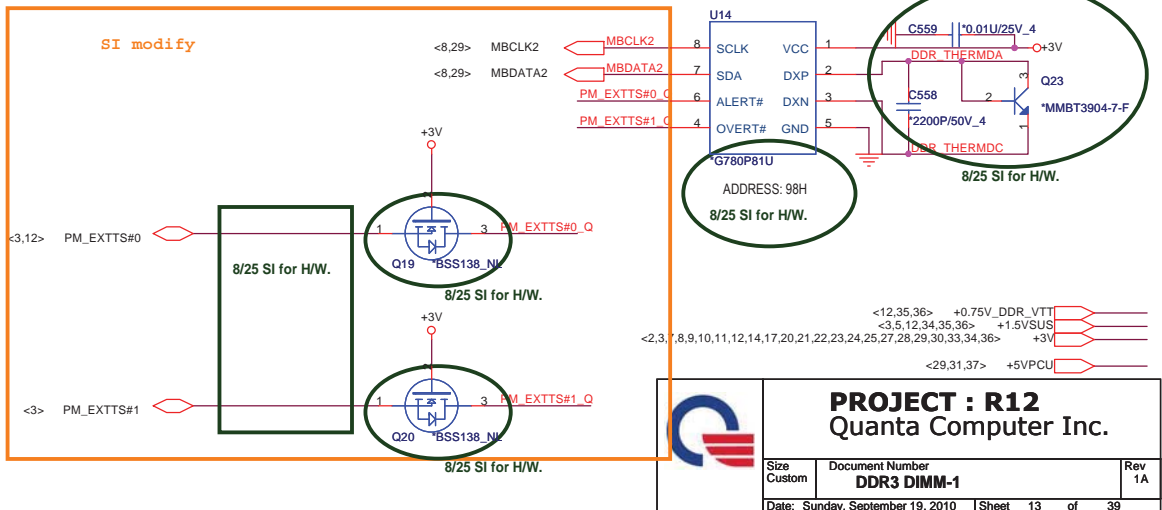
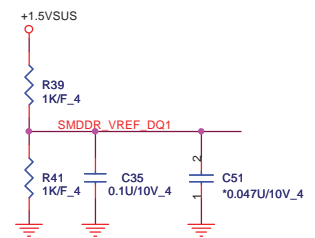
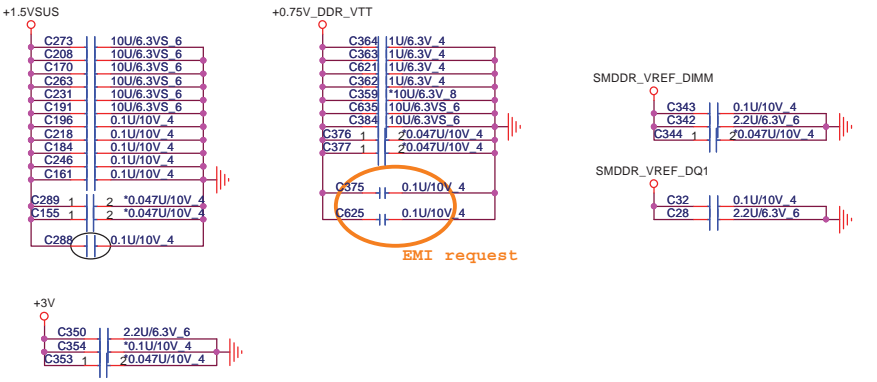
PROJECT : R12
Quanta Computer Inc.

Size Custom	Document Number DDR3 DIMM-0	Rev 1A
Date: Sunday, September 19, 2010 Sheet 12 of 39		



SO-DIMM SPD Address is 0XA4
SO-DIMM TS Address is 0X34

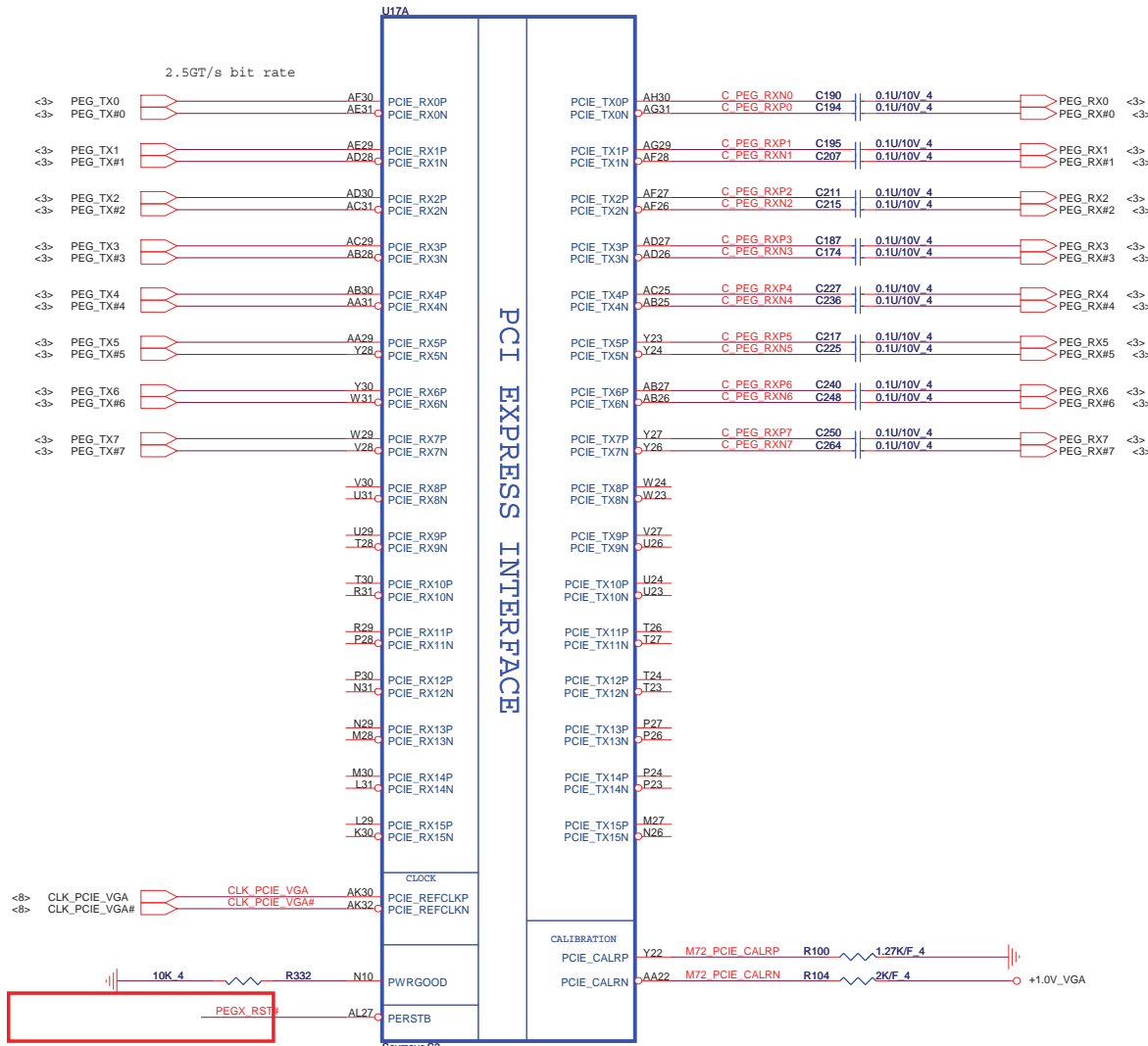
Place these Caps near So-Dimm1.
Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%



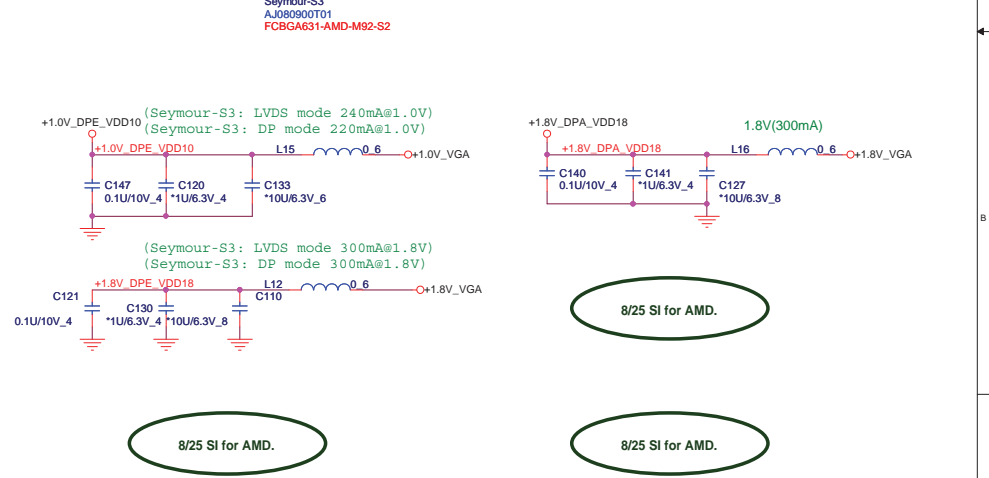
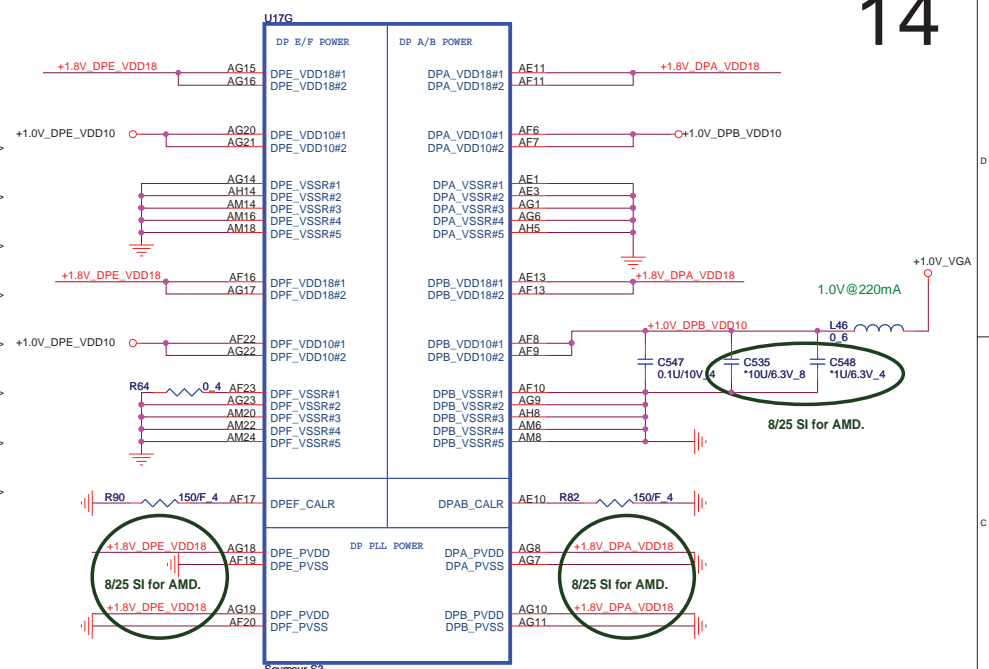
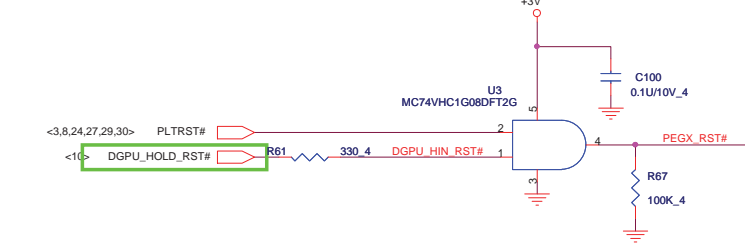
PROJECT : R12
Quanta Computer Inc.

Size Custom Document Number **DDR3 DIMM-1** Rev 1A

Date: Sunday, September 19, 2010 Sheet 13 of 39

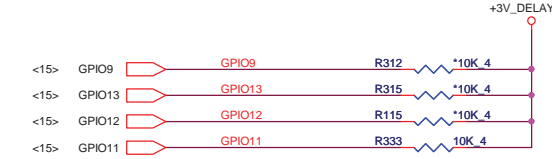
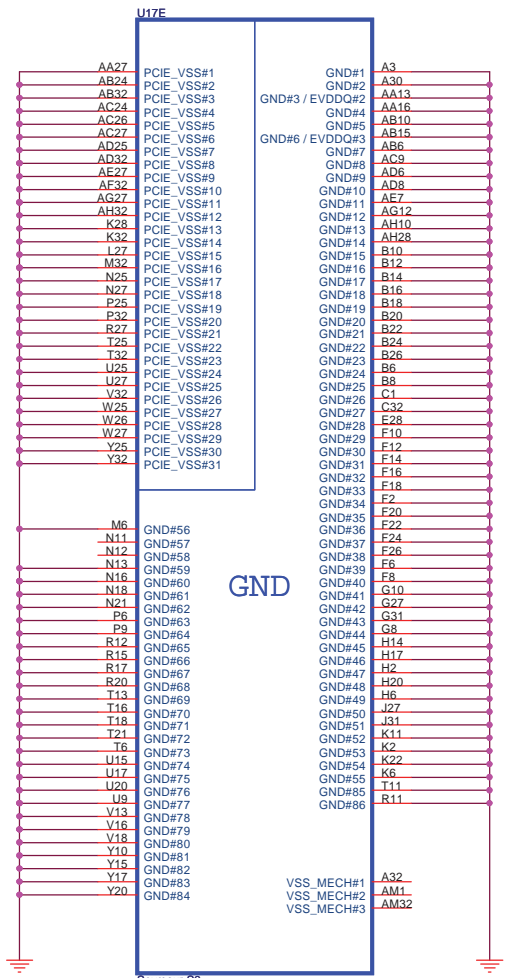


100MHz (+/-300ppm) input frequency,
0-0.7V single-ended swing



PROJECT : R12
Quanta Computer Inc.

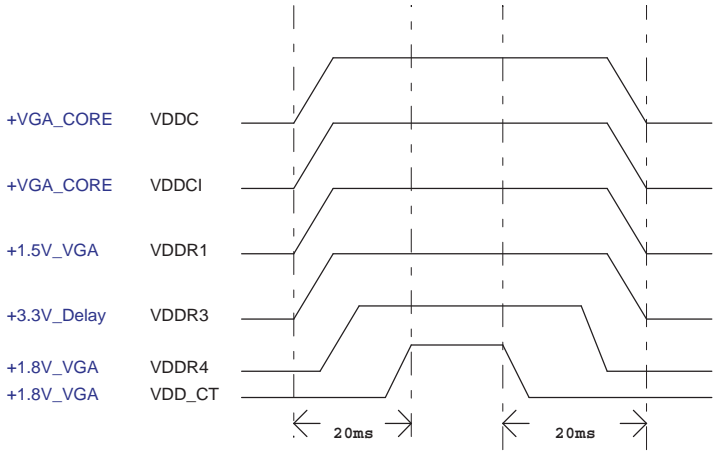
Size Custom	Document Number Seymour PCIe Interface	Rev 1A
Date: Sunday, September 19, 2010		Sheet 14 of 39



CONFIGURATION STRAPS			RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS		
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET		
H2SYNC	GENERICC	
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET		
GPIO21_BB_EN		

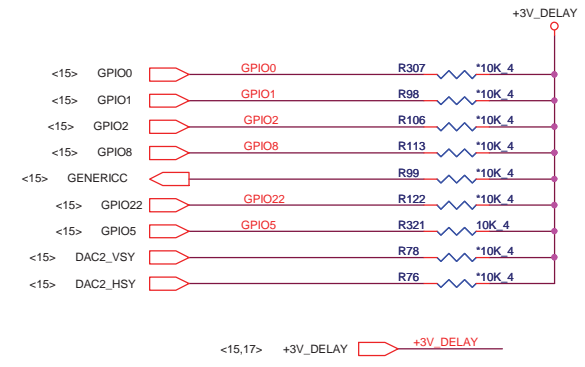
Power Up/Down Sequence



Memory Aperture size

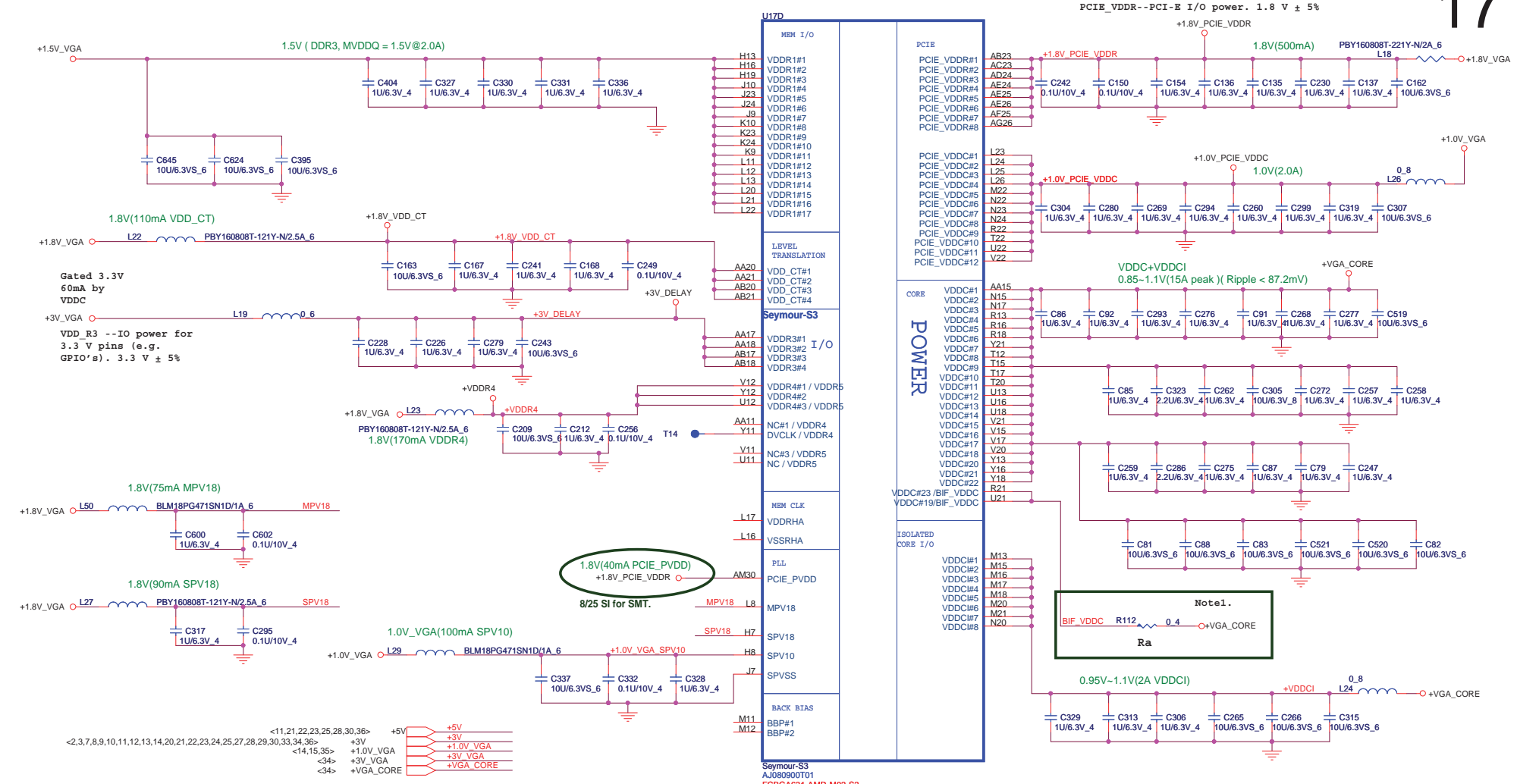
GPIO9 BIOSROM	GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0
0	256M	0	1
0	64M	0	1
0	32M	0	1
0	512M	1	0
0	1G	1	0
0	2G	1	1
0	4G	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

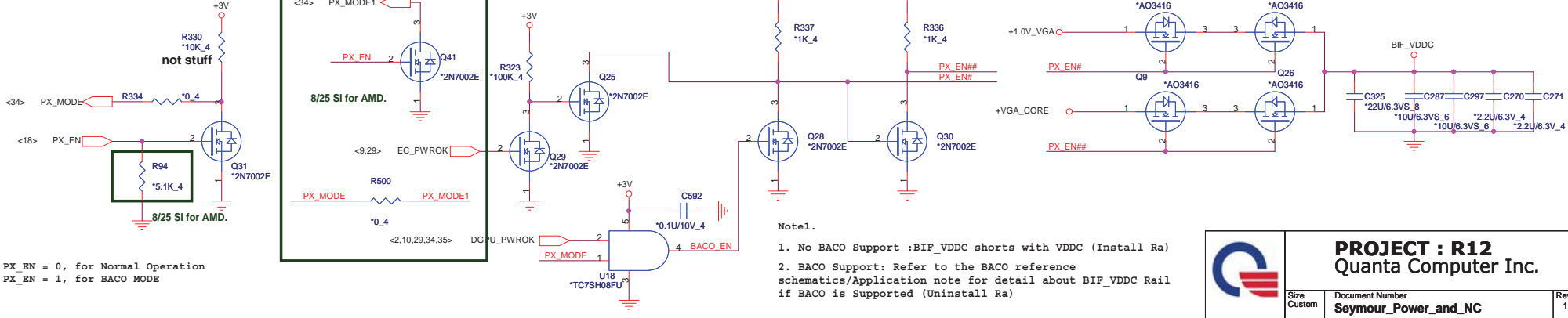


PROJECT : R12
 Quanta Computer Inc.

Size Custom Document Number Seymour GND / LVDS/ Straps Rev 1A
 Date: Sunday, September 19, 2010 Sheet 16 of 39

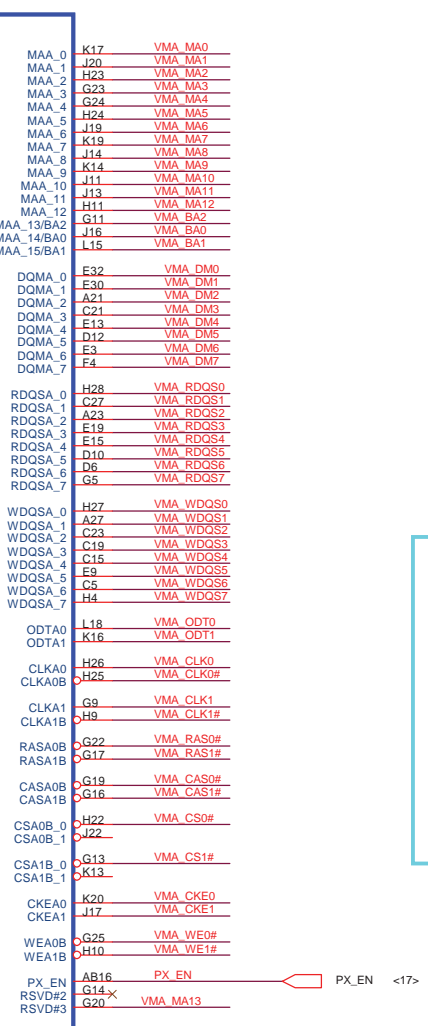
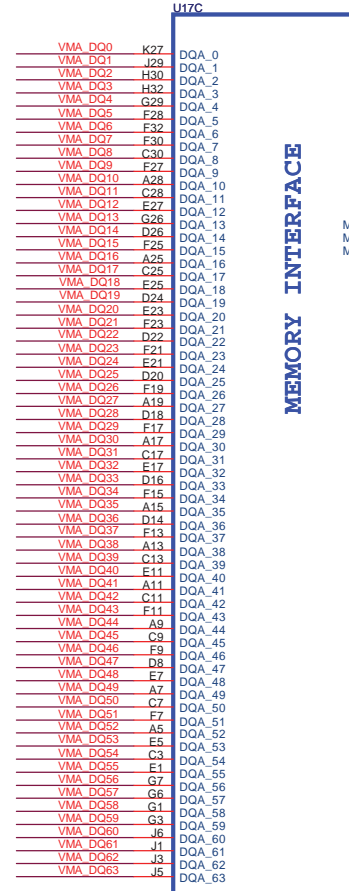
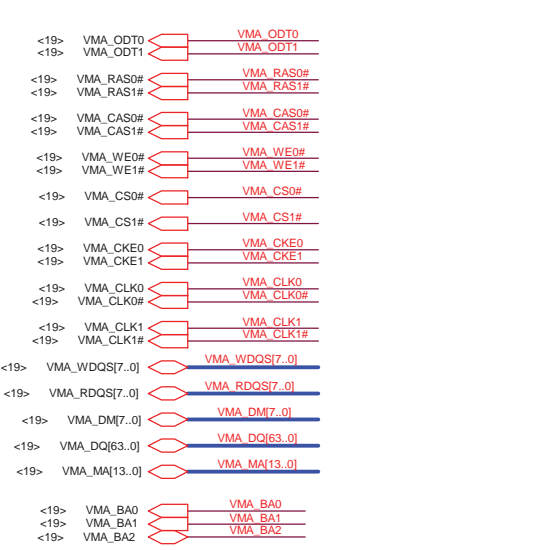


Support BACO Mode



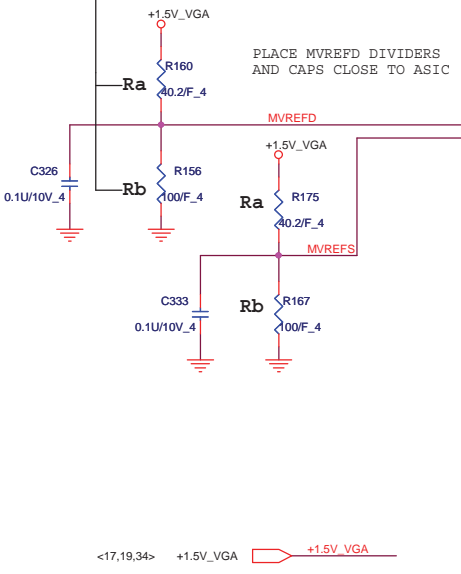
	PROJECT : R12 Quanta Computer Inc.	
	Size Custom Document Number Seymour_Power_and_NC	Date: Sunday, September 19, 2010 Sheet 17 of 39

MEMORY INTERFACE

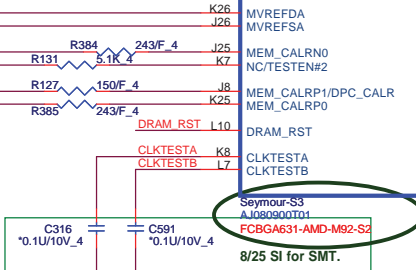


support 1Gbit
VRAM (64M X 16)

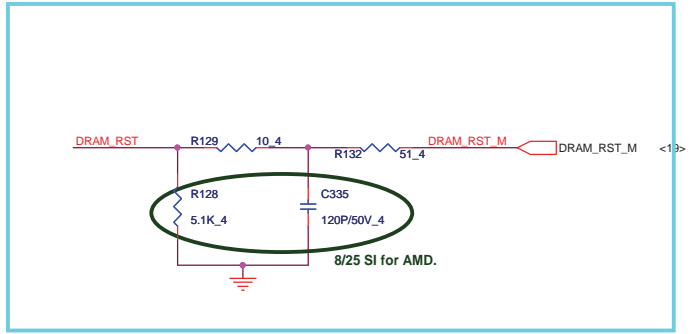
DIVIDER RESISTORS	GDDR5	DDR3
MVREF TO 1.8V (Ra)	40.2R	40.2R
MVREF TO GND (Rb)	100R	100R



PLACE MVREFD DIVIDERS
AND CAPS CLOSE TO ASIC

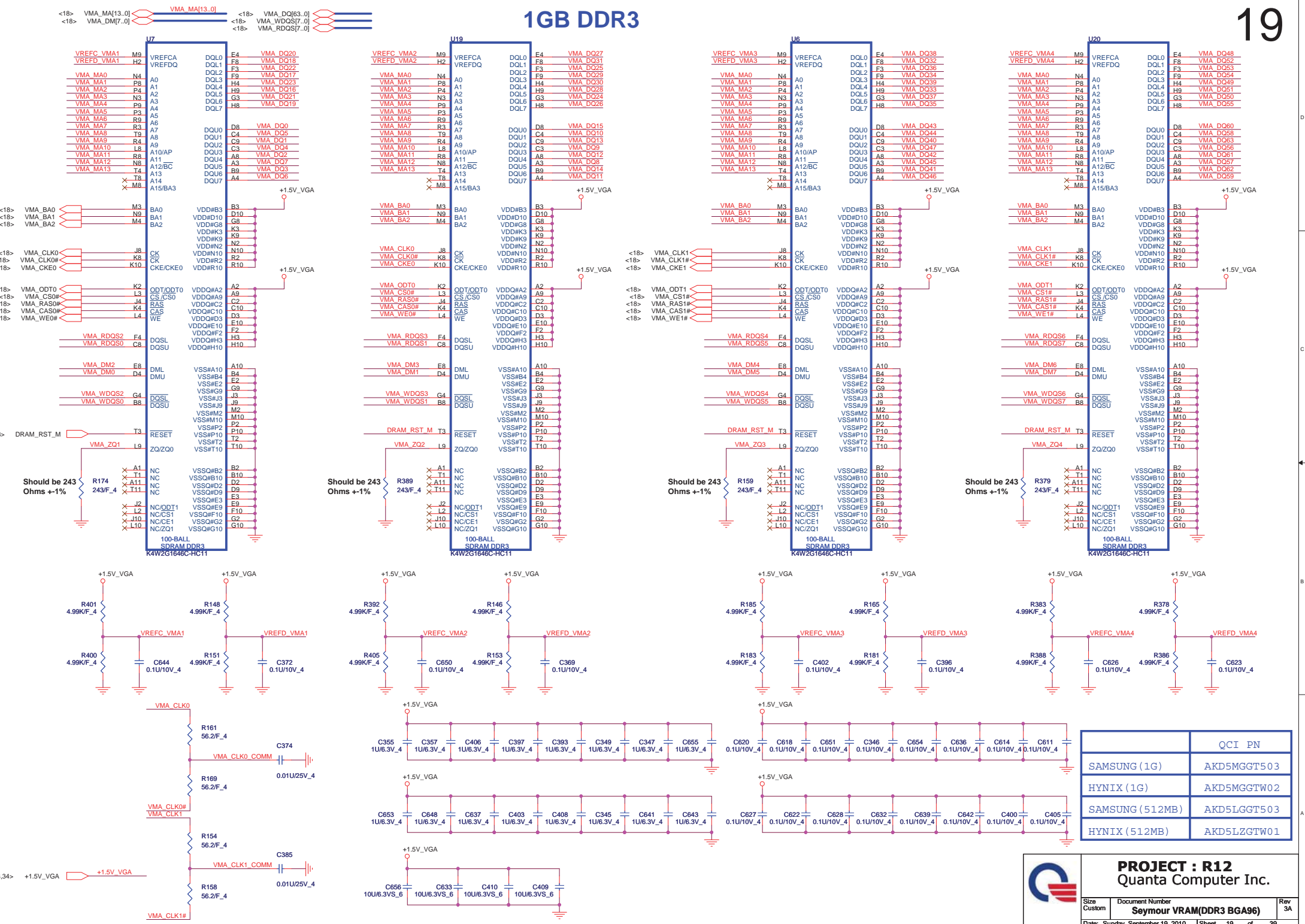


route 50ohms
single-ended/100ohms diff
and keep short
Debug only, for clock observation,
if not needed, DNI



PROJECT : R12
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1GB DDR3

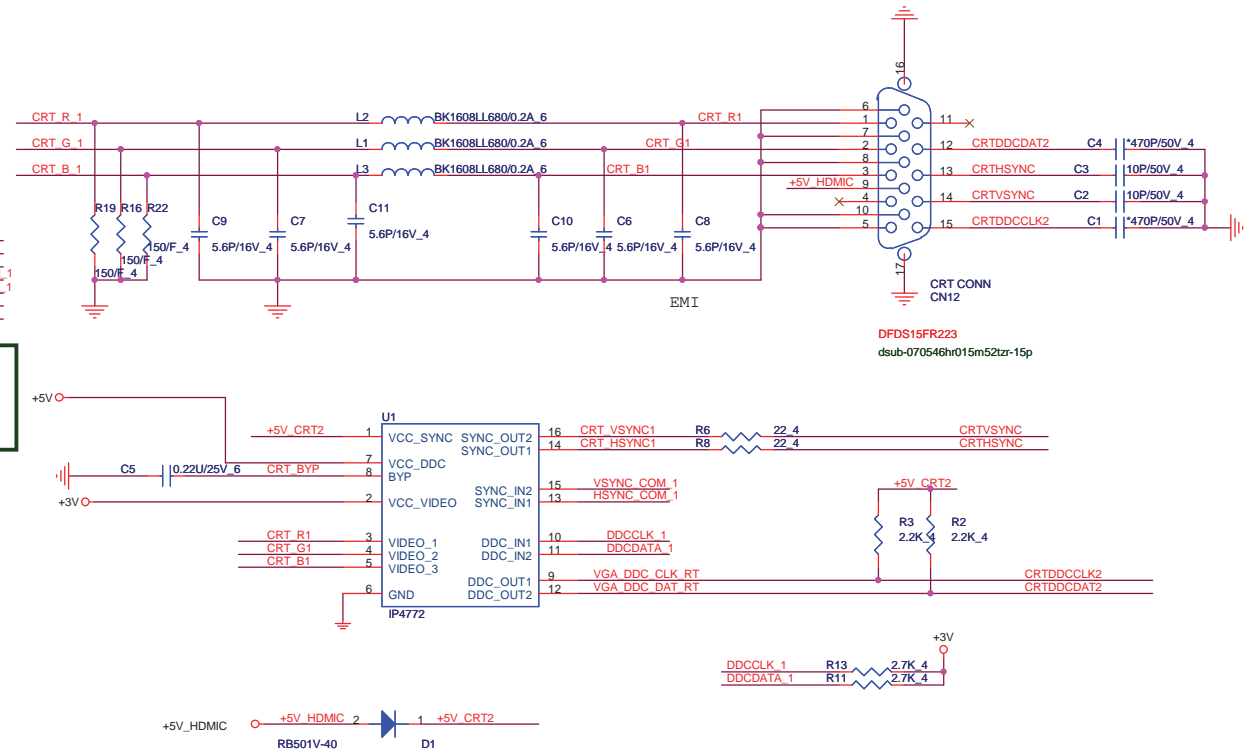
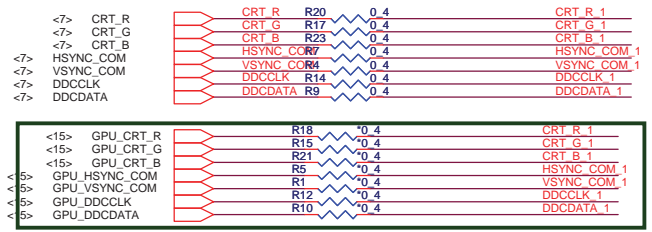


QCI PN	
SAMSUNG (1G)	AKD5MGGT503
HYNIX (1G)	AKD5MGGTW02
SAMSUNG (512MB)	AKD5LGGT503
HYNIX (512MB)	AKD5LZGTW01

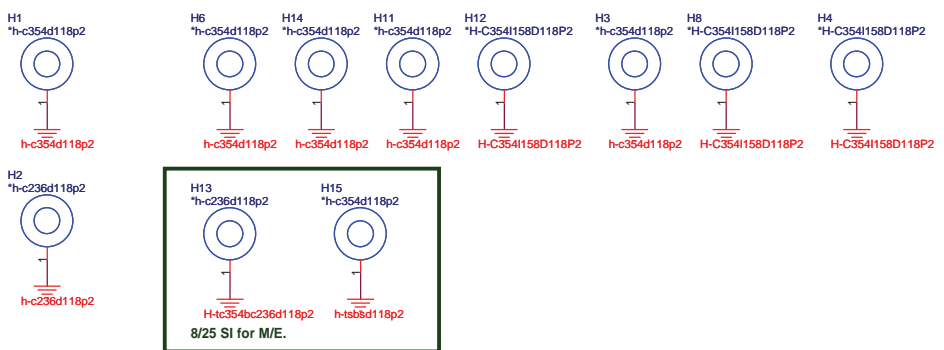


PROJECT : R12
Quanta Computer Inc.

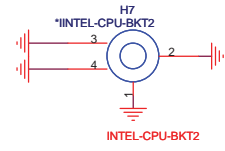
CRT PORT



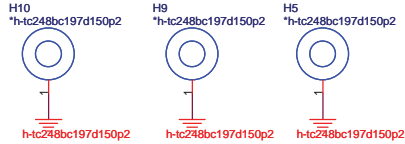
HOLE



CPU

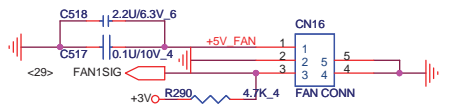


VGA

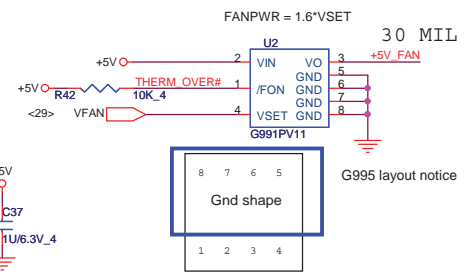


	PROJECT : R12 Quanta Computer Inc.	
	Size Custom Document Number CRT.Hole	Rev 1A
Date: Sunday, September 19, 2010 Sheet 22 of 39		

CPU FAN

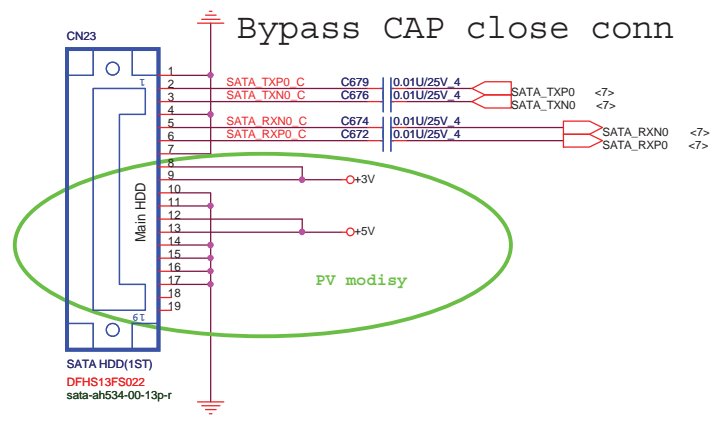


DFHD03MR029
53398-0310-3P-L

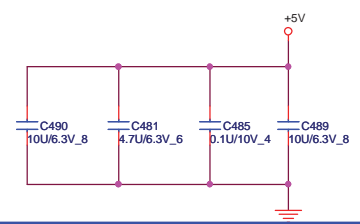


G995 layout notice

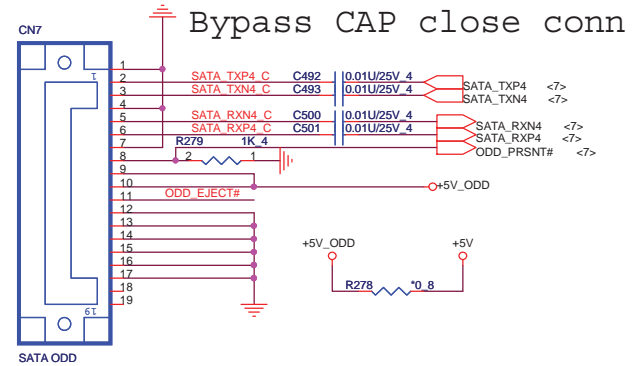
SATA HDD CONNECTOR



Bypass CAP close conn



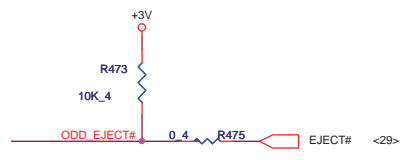
SATA ODD CONNECTOR



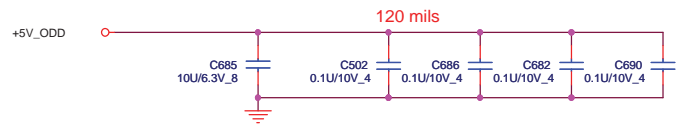
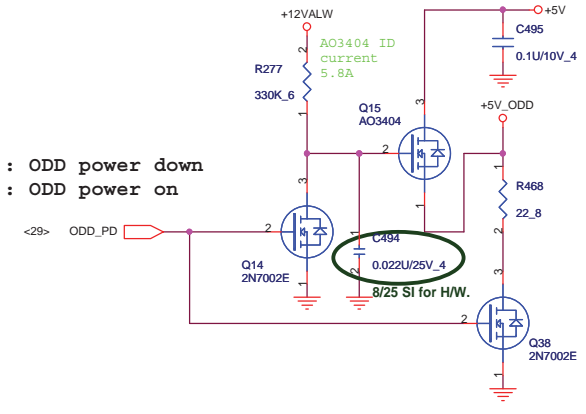
Bypass CAP close conn

DFHS13FS022
sata-ah534-00-13p-r

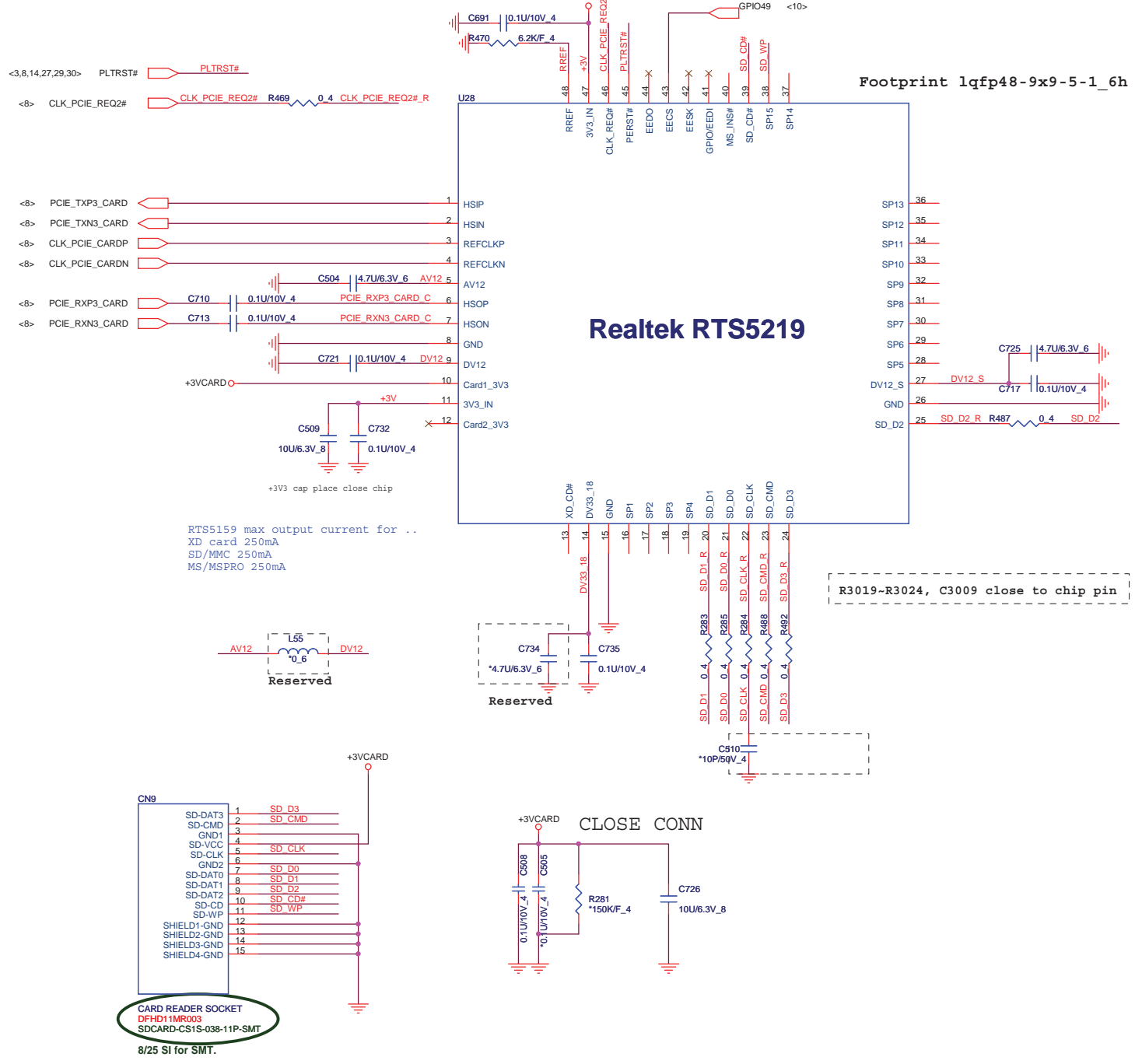
follow INTEL DG change eject PU to +3V.



High : ODD power down
Low : ODD power on



120 mils

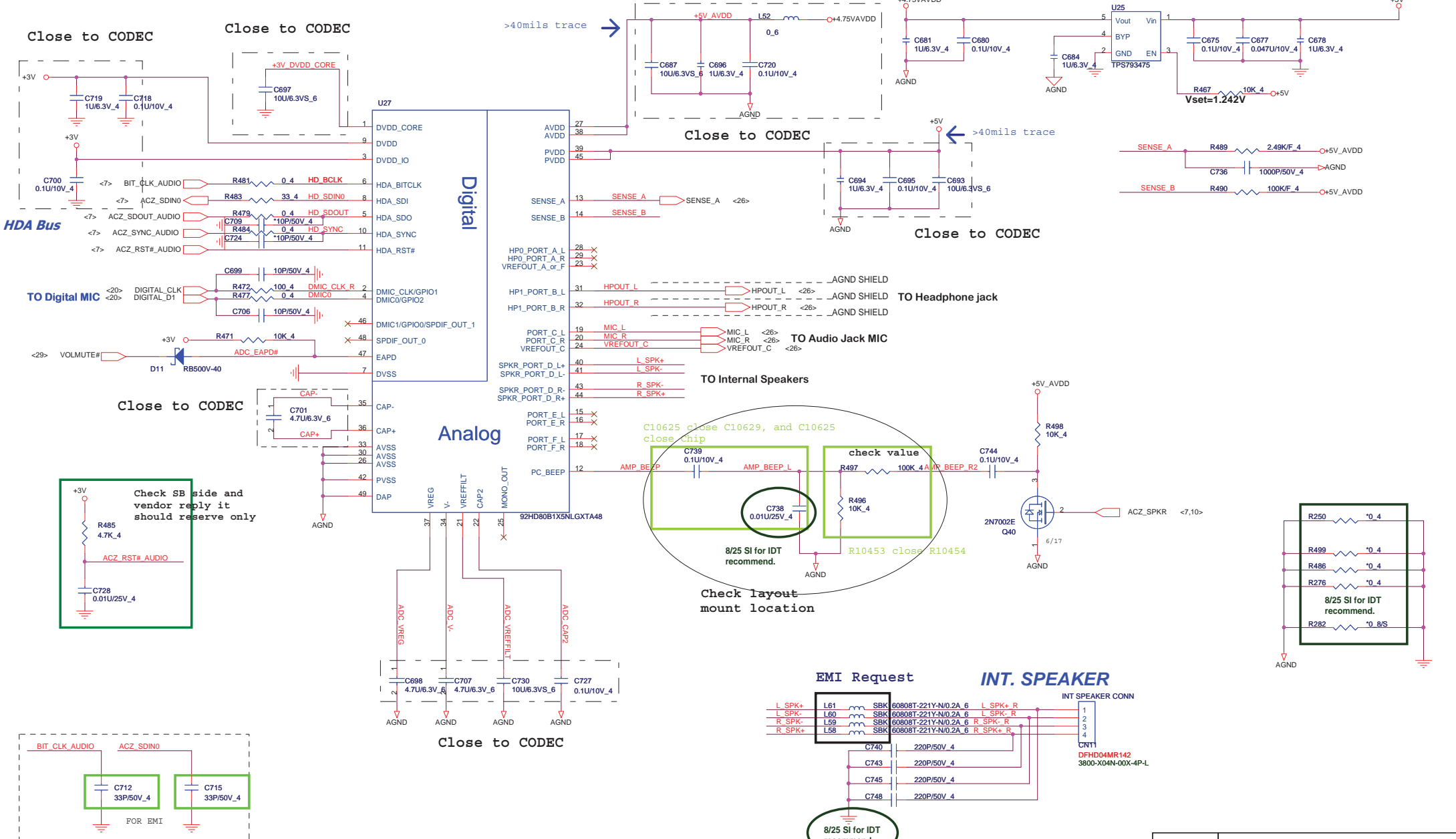


RTS5159 max output current for ..
 XD card 250mA
 SD/MMC 250mA
 MS/MSPRO 250mA

R3019-R3024, C3009 close to chip pin

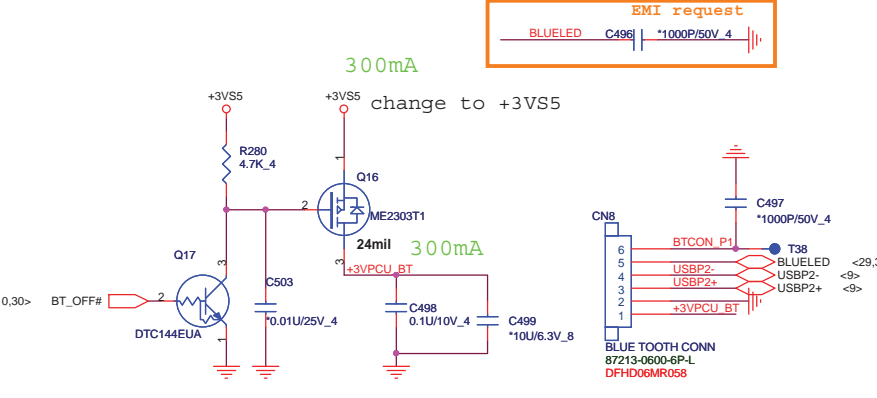
CARD READER SOCKET
 DFHD11MR003
 SDCARD-CS1S-038-11P-SMT
 8/25 SI for SMT.

<2,3,7,8,9,10,11,12,13,14,17,20,21,22,23,24,27,28,29,30,33,34,36> +3V
<11,17,21,22,23,28,30,36> +5V



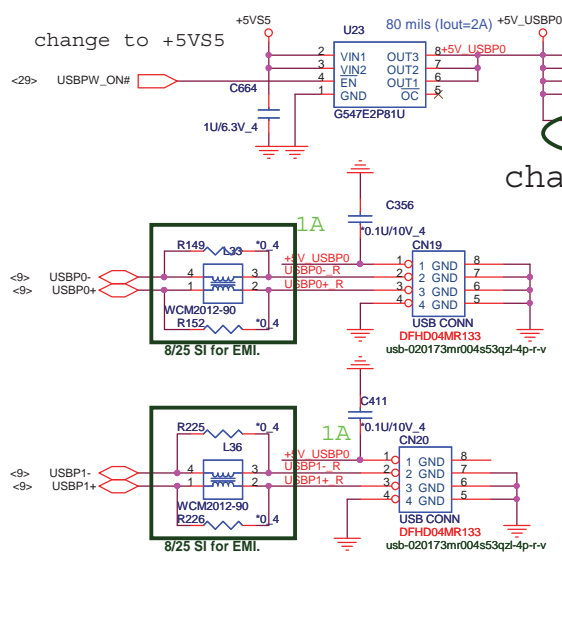
			PROJECT : R12		
			Quanta Computer Inc.		
Size	Document Number	Rev			
Custom	Azalia 92HD80	1A			
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BLUETOOTH

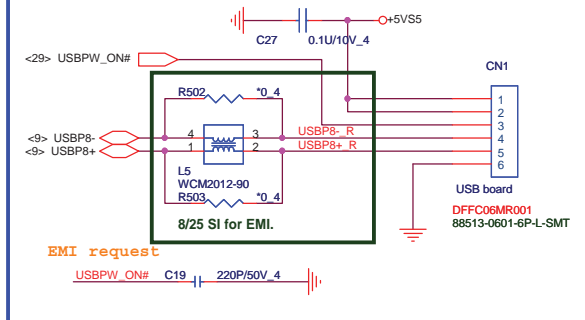


LEFT SIDE USB2

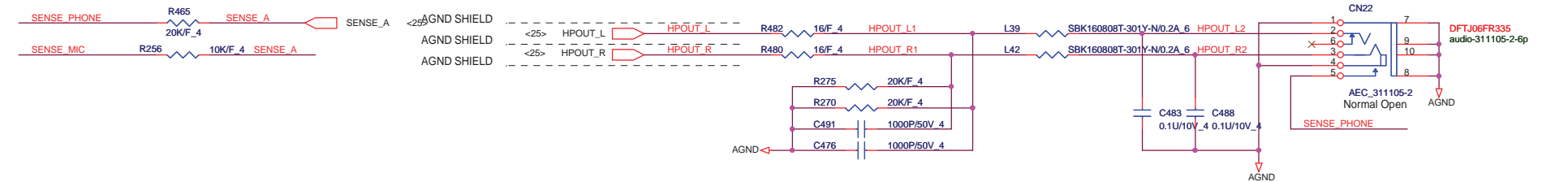
change to AL000547005
change to +5VS5



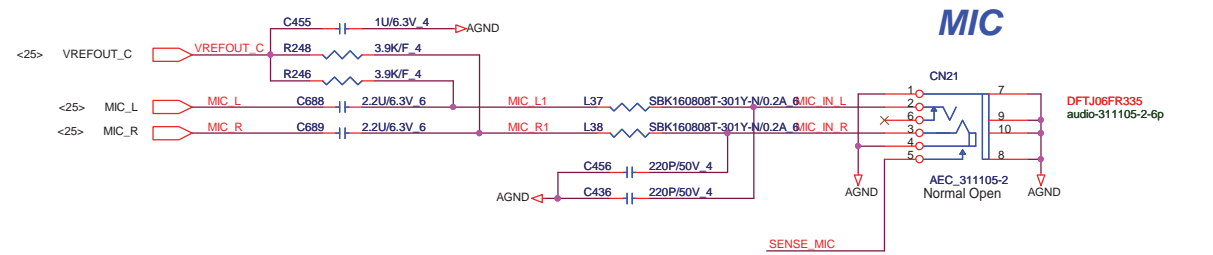
Right SIDE USB1



Line out

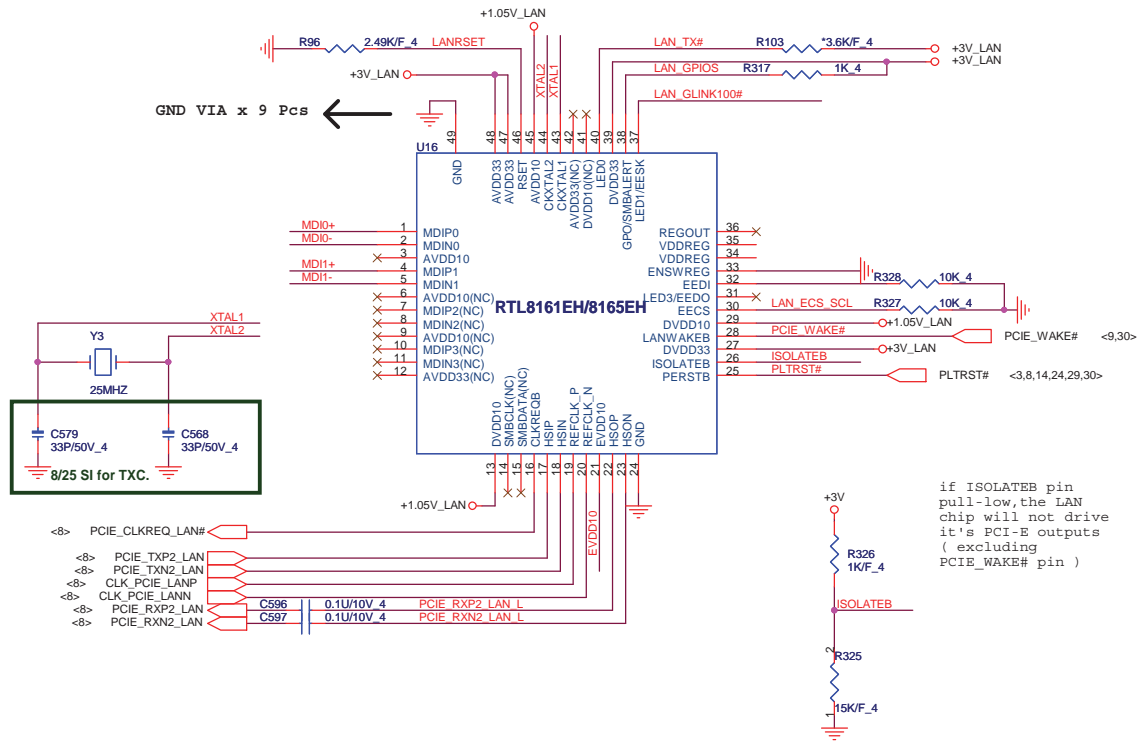


MIC



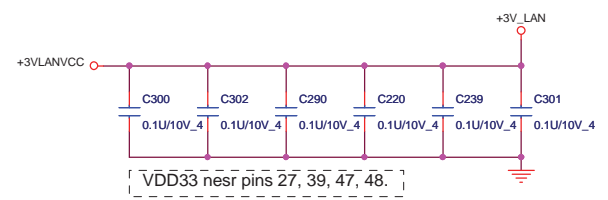
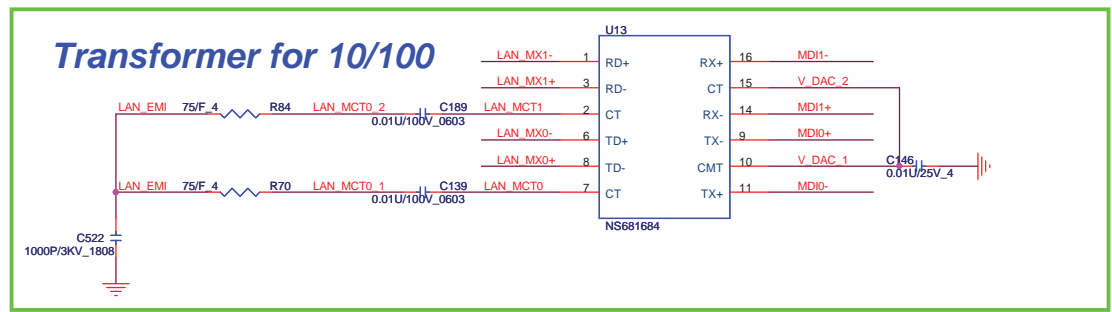
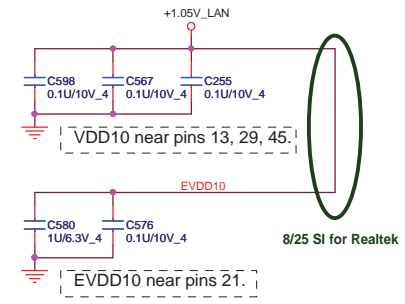
PROJECT : R12
Quanta Computer Inc.

Size Custom	Document Number USB/BT/Audio Jack	Rev 1A
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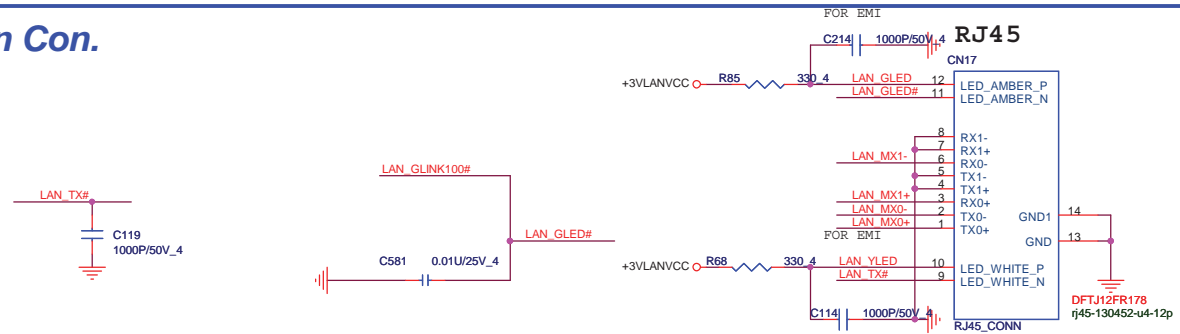


IND SMD 4.7UH +/-20% 680MA (CBC2518T4R7M)
CV-4707MZ00

Power trace Layout 寬度 > 60mil
>60mil



Lan Con.

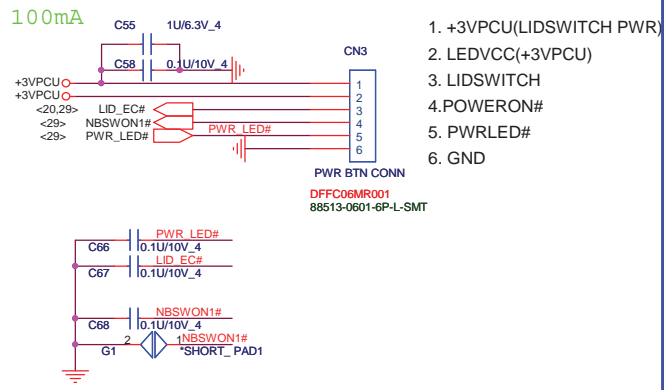


<2,3,7,8,9,10,11,12,13,14,17,20,21,22,23,24,25,28,29,30,33,34,36> +3VLANVCC
+3V

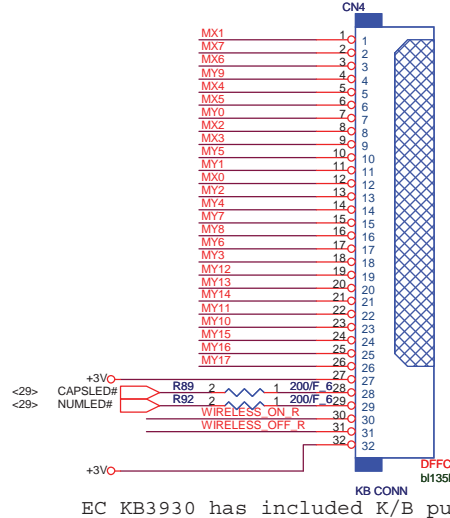
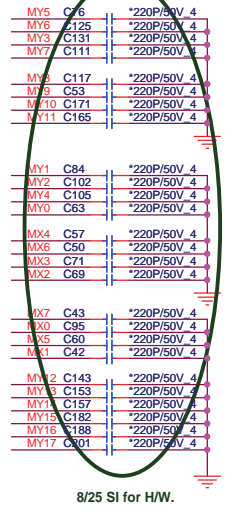
PROJECT : R12
Quanta Computer Inc.

Size Custom	Document Number RTL8165EH	Rev 1A
Date: Sunday, September 19, 2010		Sheet 27 of 39

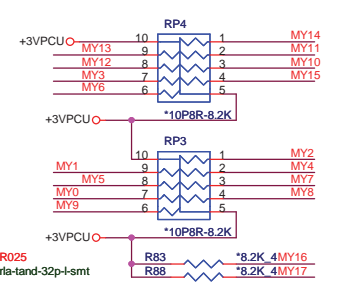
POWER BOTTON CONNECT



KEYBOARD Con.



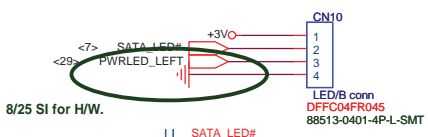
KEYBOARD PULL-UP



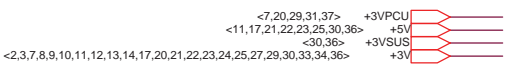
SI Modify



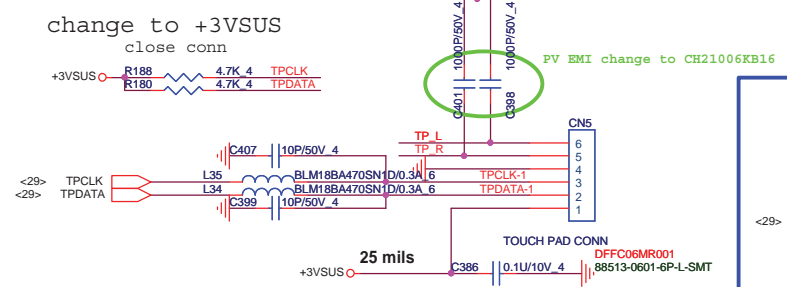
LED Con.



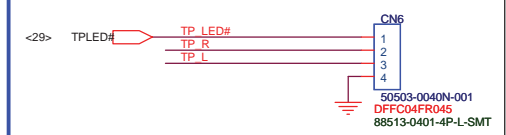
1. +3V
2. SATA_LED#
3. PWR_LED#
4. GND



TOUCH PAD Con.



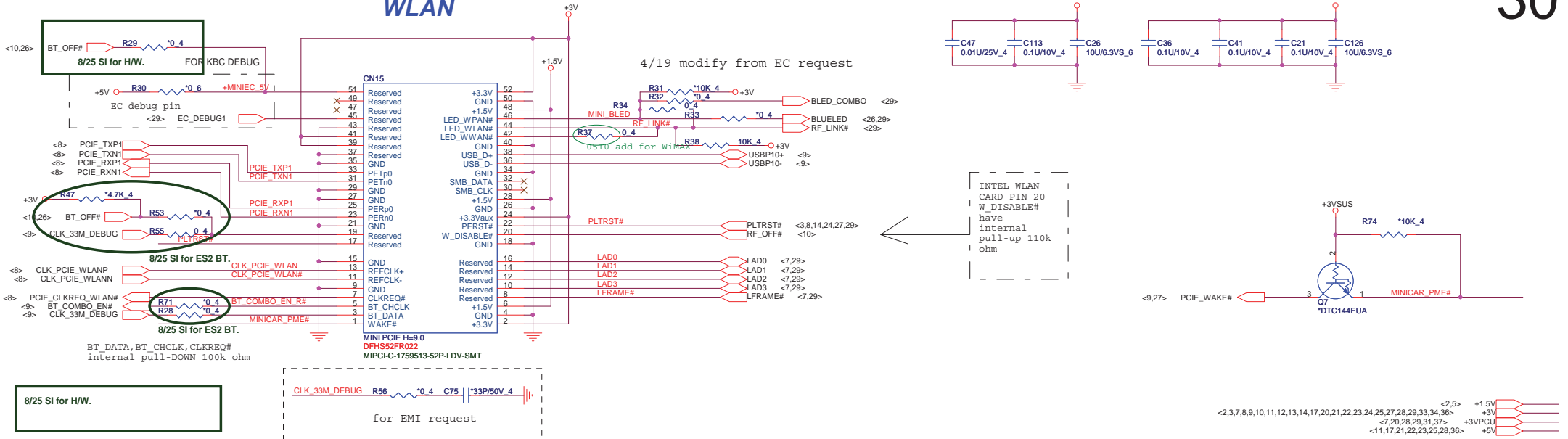
To TOUCH PAD SW board



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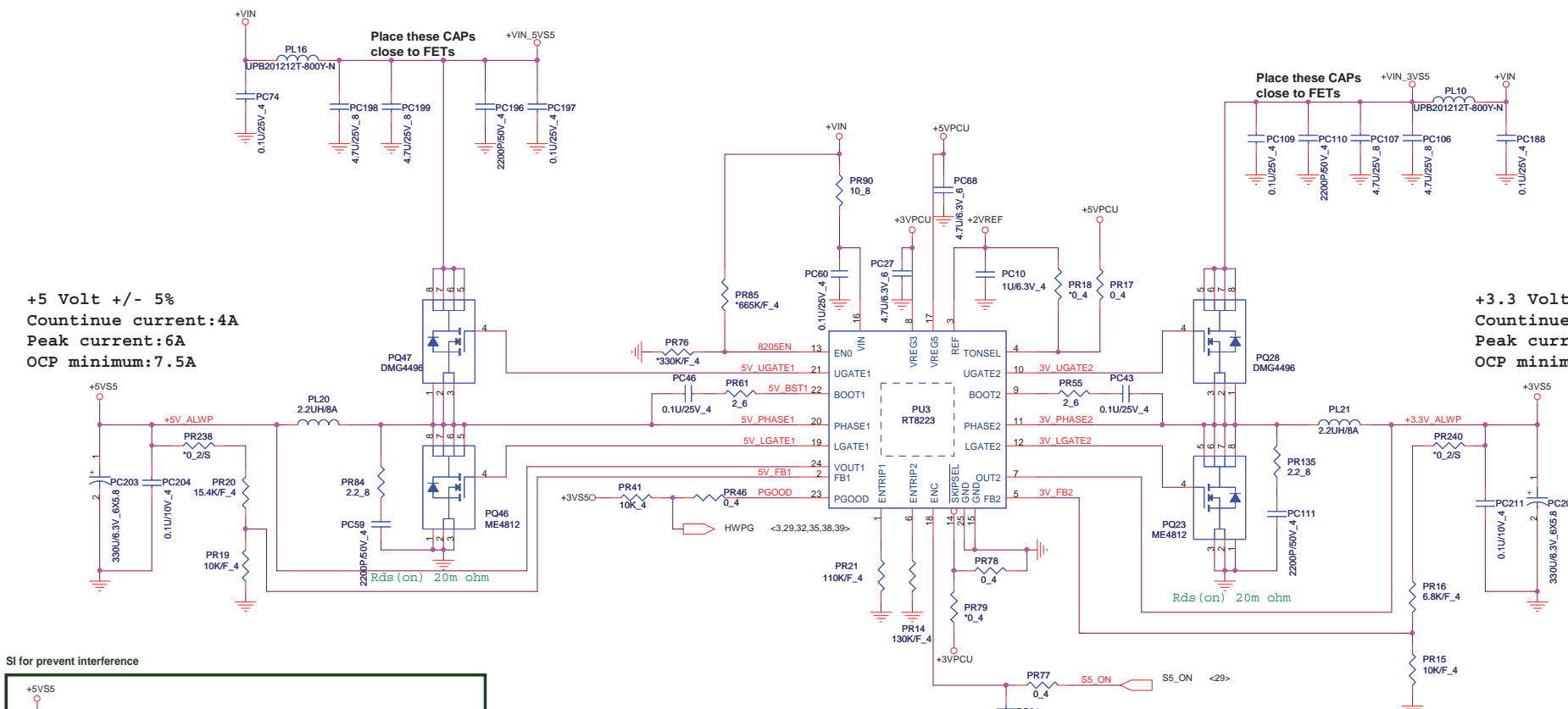
Mini PCI-E Card 1

WLAN

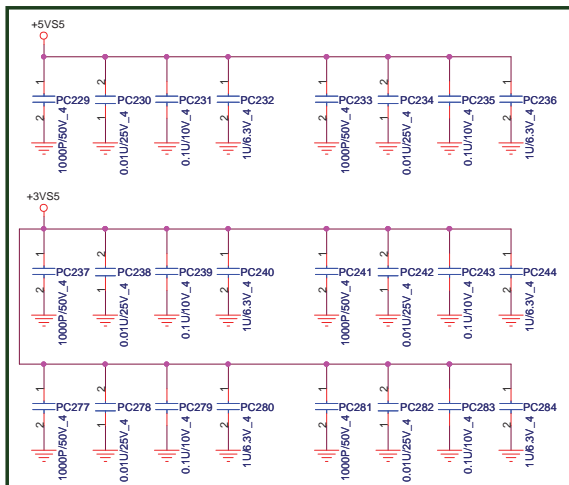



+5 Volt +/- 5%
 Countinue current:4A
 Peak current:6A
 OCP minimum:7.5A

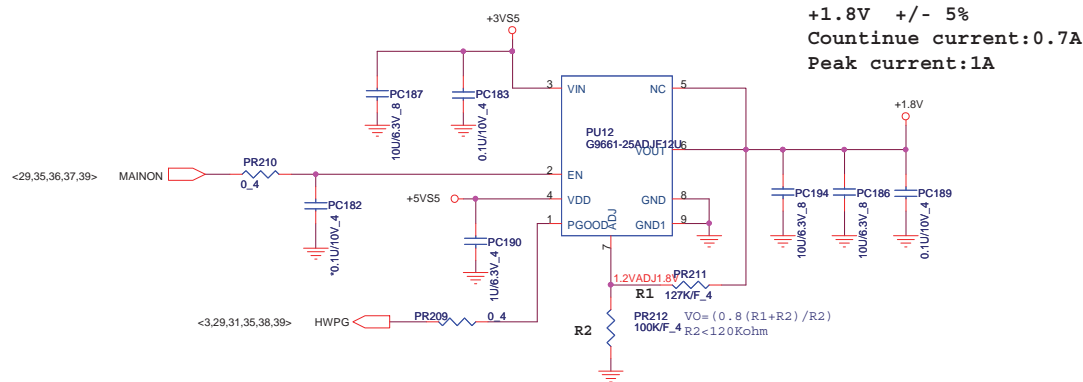
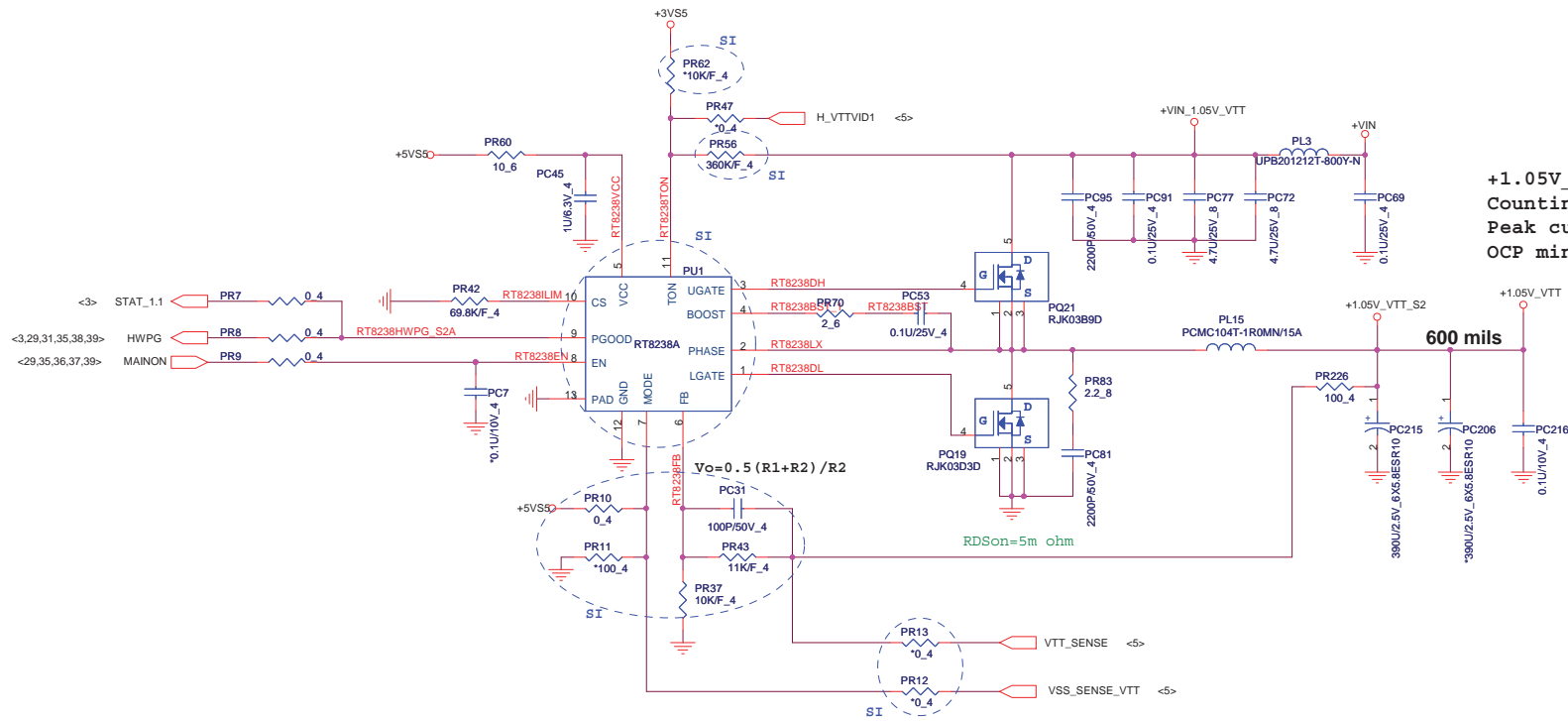
+3.3 Volt +/- 5%
 Countinue current:4A
 Peak current:6A
 OCP minimum:7.5A



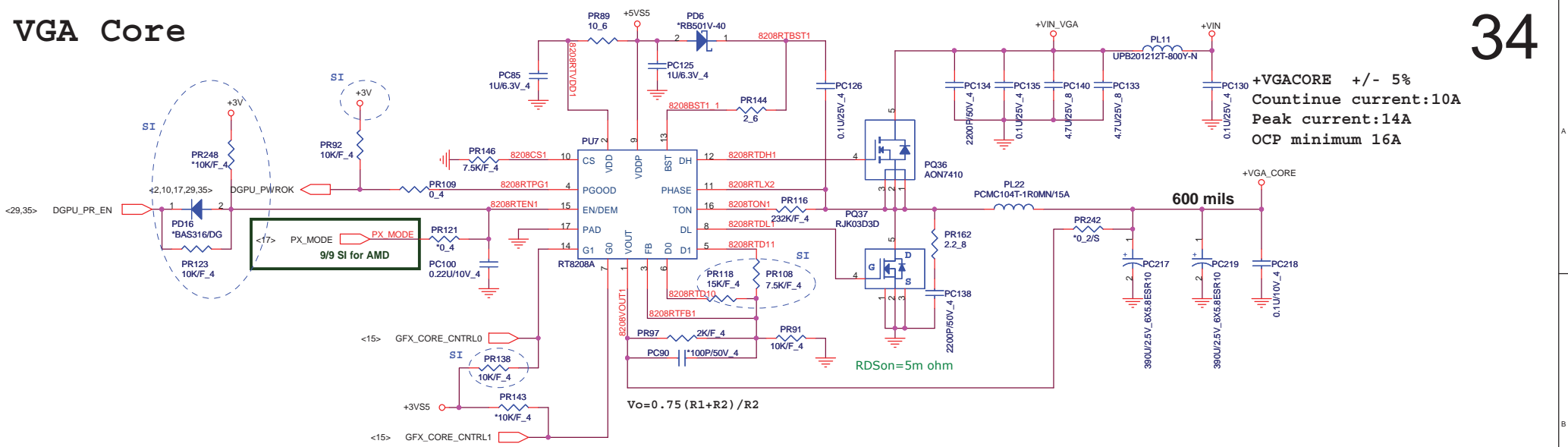
SI for prevent interference



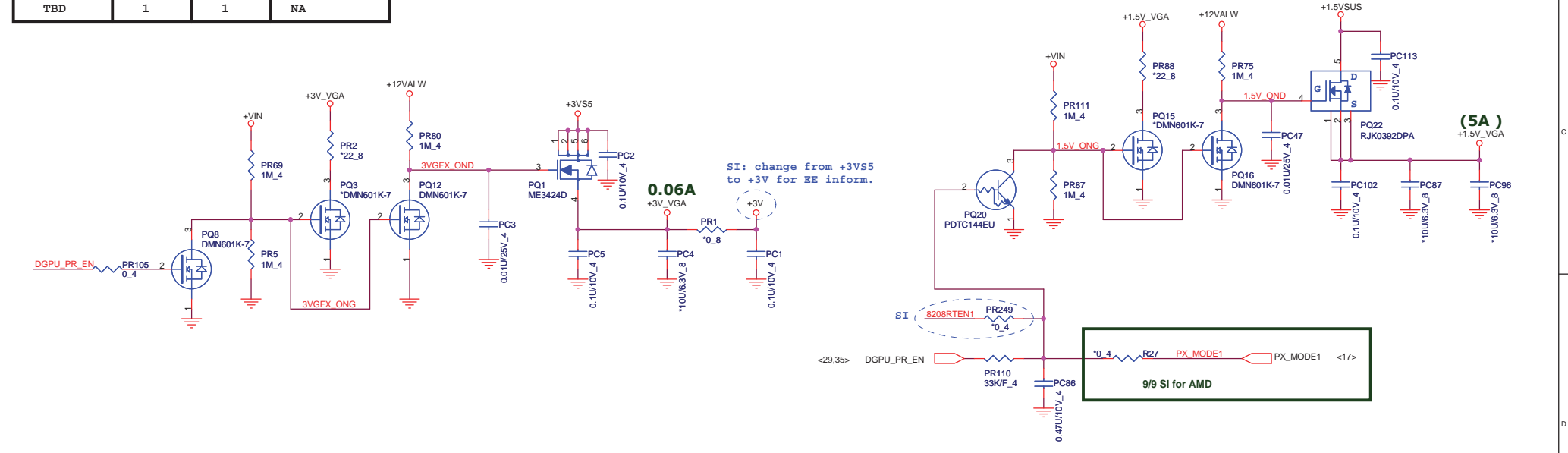
			PROJECT : R12	
			Quanta Computer Inc.	
Size Custom	Document Number	+5V/+3V (RT8206B)		Rev 1A
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VGA Core

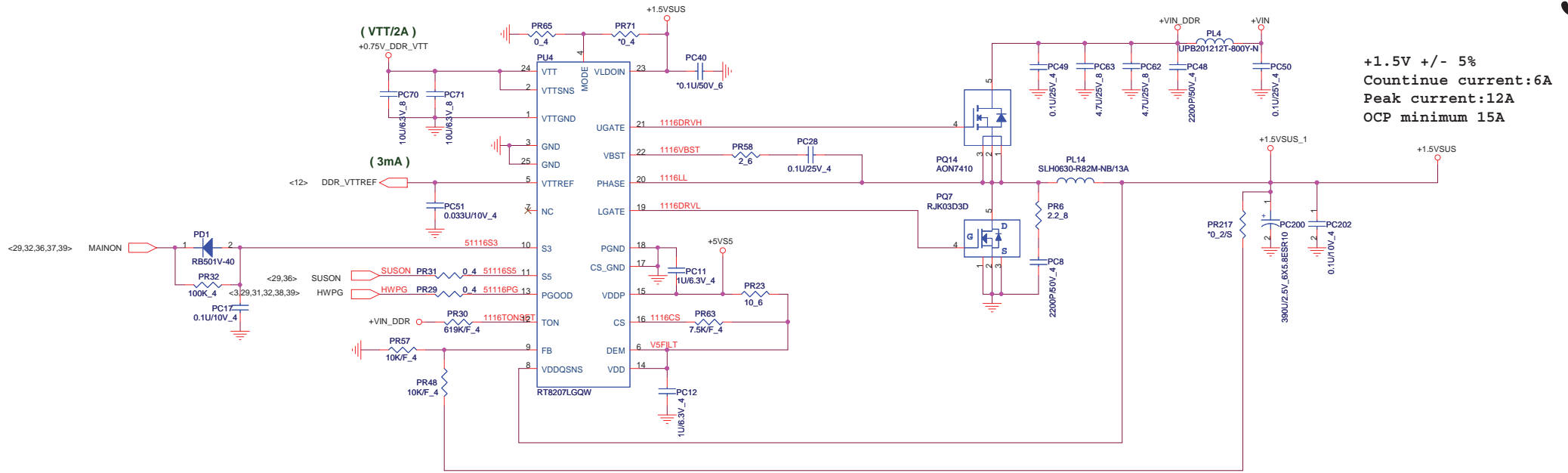


Seymour-XT	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	1V
H	1	0	1.1V (Default)
TBD	1	1	NA

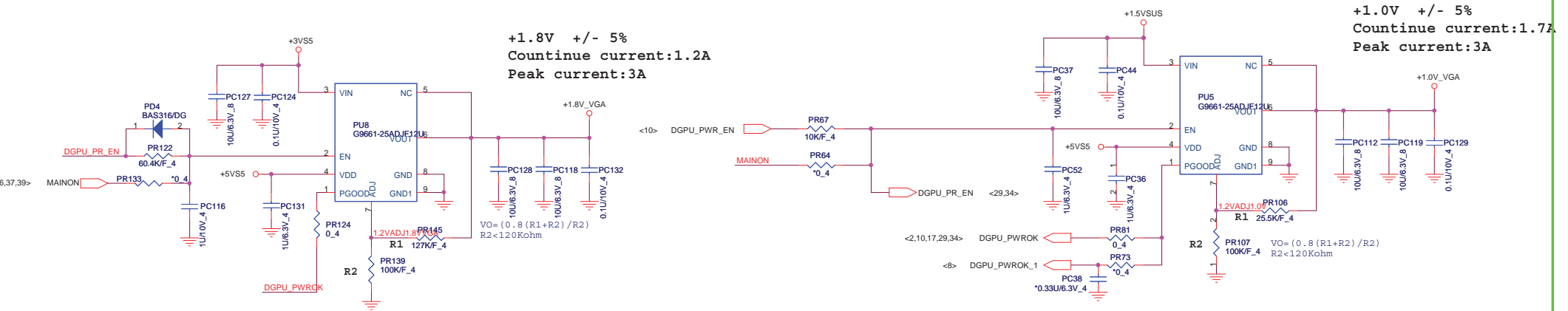


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Quanta Computer Inc.

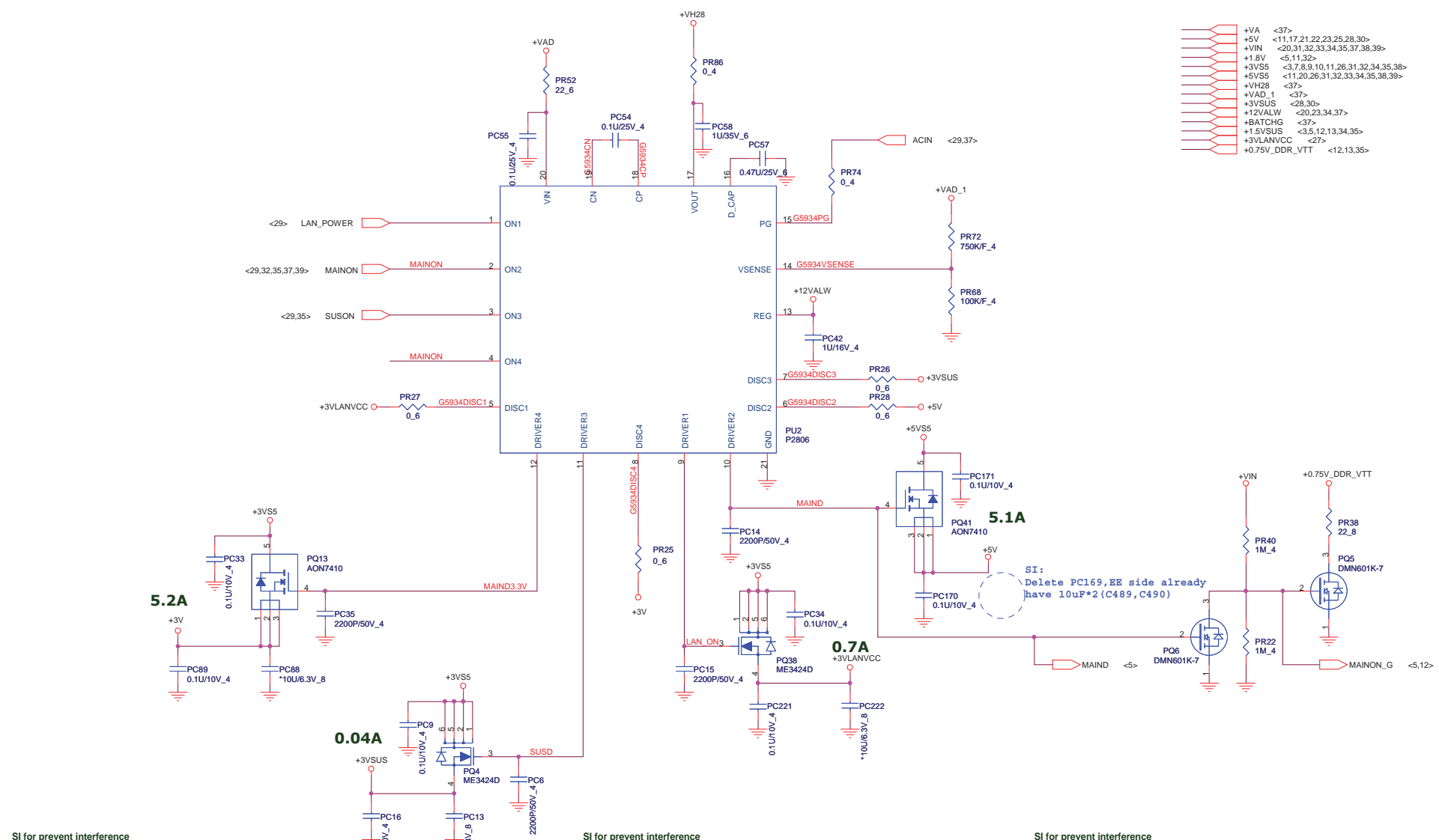
Size Custom	Document Number +VGACORE (RT8208/1.8V)	Rev 1A
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SG & Discrete Only



- +VA <37>
- +5V <11,17,21,22,23,25,28,30>
- +VIN <20,31,32,33,34,35,37,38,39>
- +1.8V <5,11,32>
- +3VS5 <3,7,8,9,10,11,26,31,32,34,35,38>
- +5VS5 <11,20,26,31,32,33,34,35,38,39>
- +VH28 <37>
- +VAD_1 <37>
- +3VSUS <28,30>
- +12VALW <20,23,34,37>
- +BATCHG <37>
- +1.5VSUS <3,5,12,13,34,35>
- +3VLNVCC <27>
- +0.75V_DDR_VTT <12,13,35>



5.2A

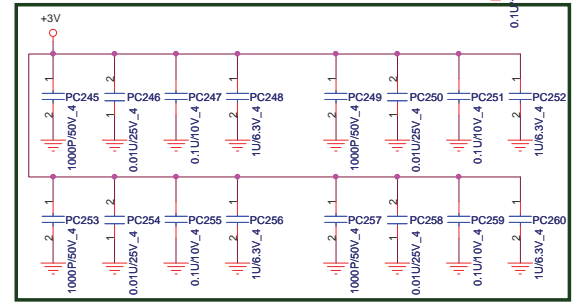
0.04A

0.7A

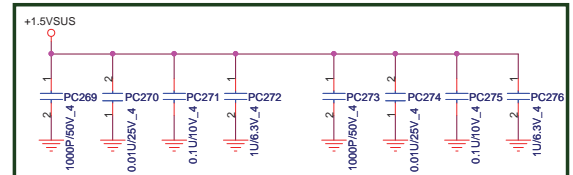
5.1A

SI: Delete PC169, EE side already have 10uF*2 (C489, C490)

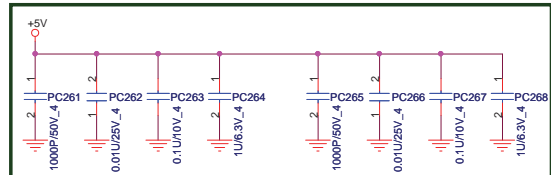
SI for prevent interference



SI for prevent interference



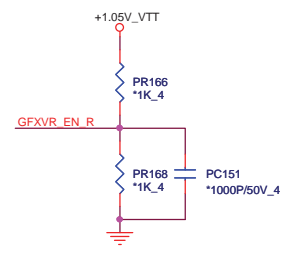
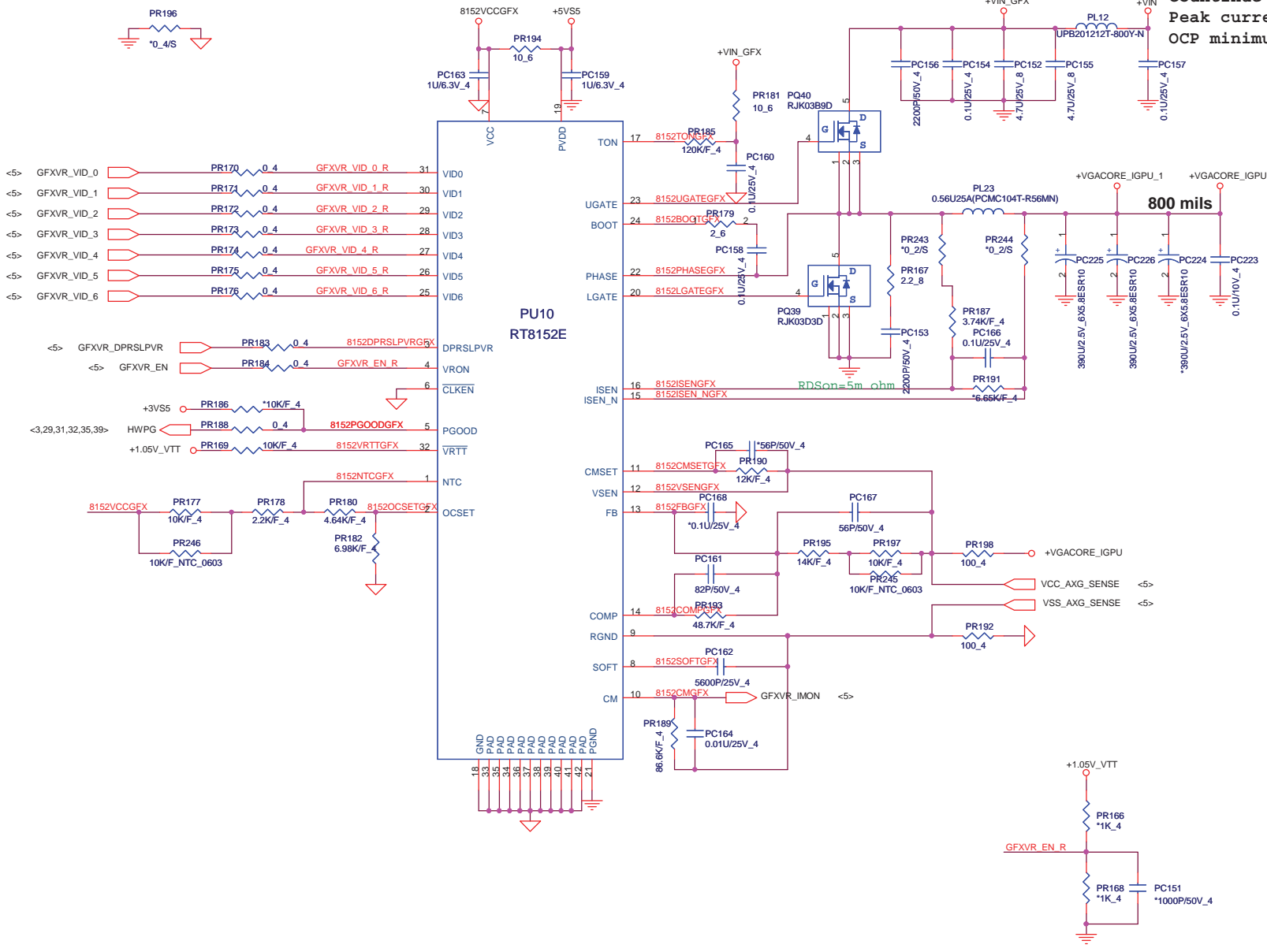
SI for prevent interference




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Quanta Computer Inc.

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+VGA_UMA +/- 5%
 Continue current:12A
 Peak current:18A
 OCP minimum 22A



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	Size Custom	Document Number UMA GPU CORE (RT8152C)
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