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Z5WAE Schematics Document

AMD "Beema" Platform

AMD 25W APU With Puma+ Core and 25W DGPU with Jet

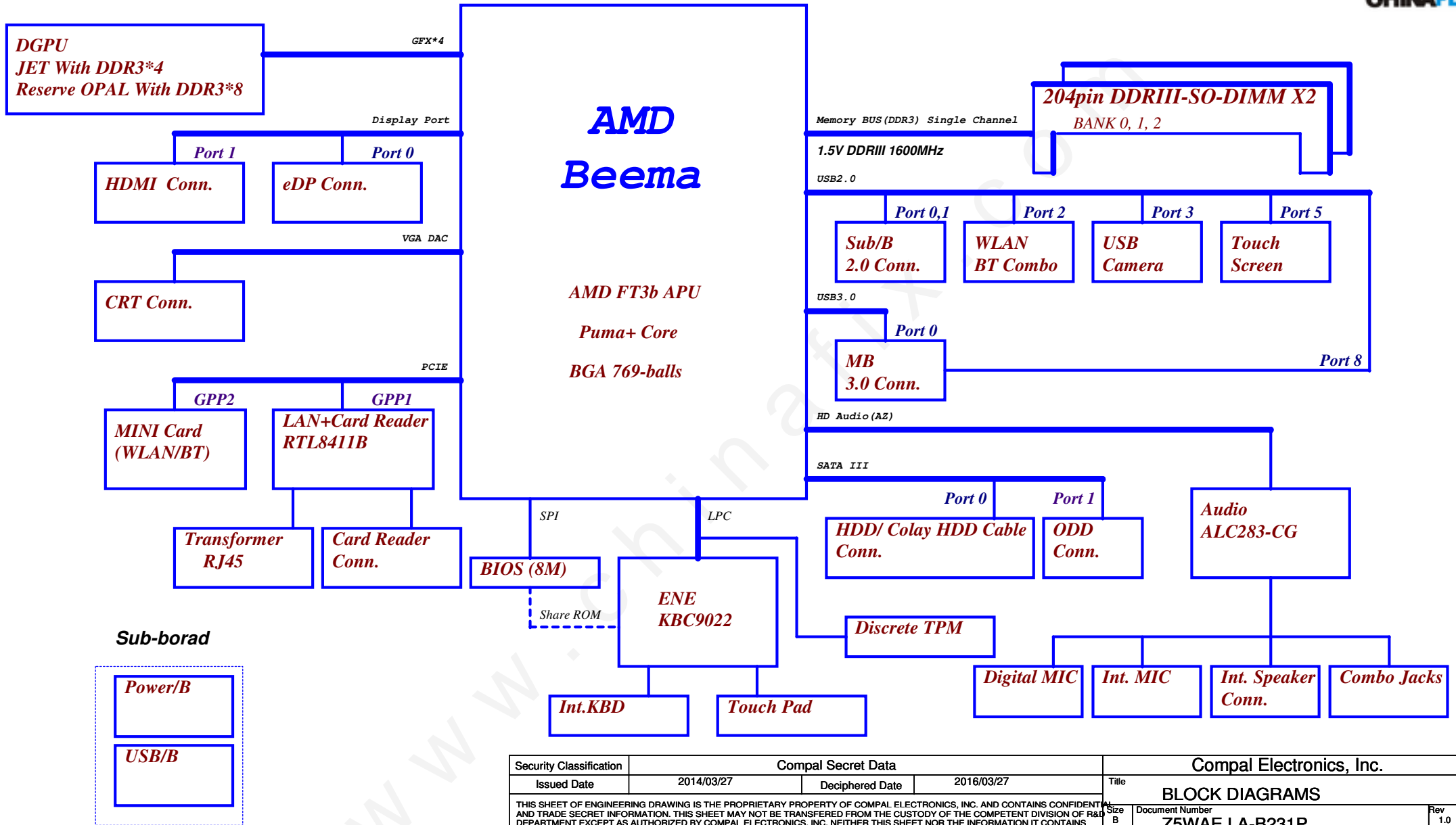
LA-B231P REV: 1.0

2014-03-27

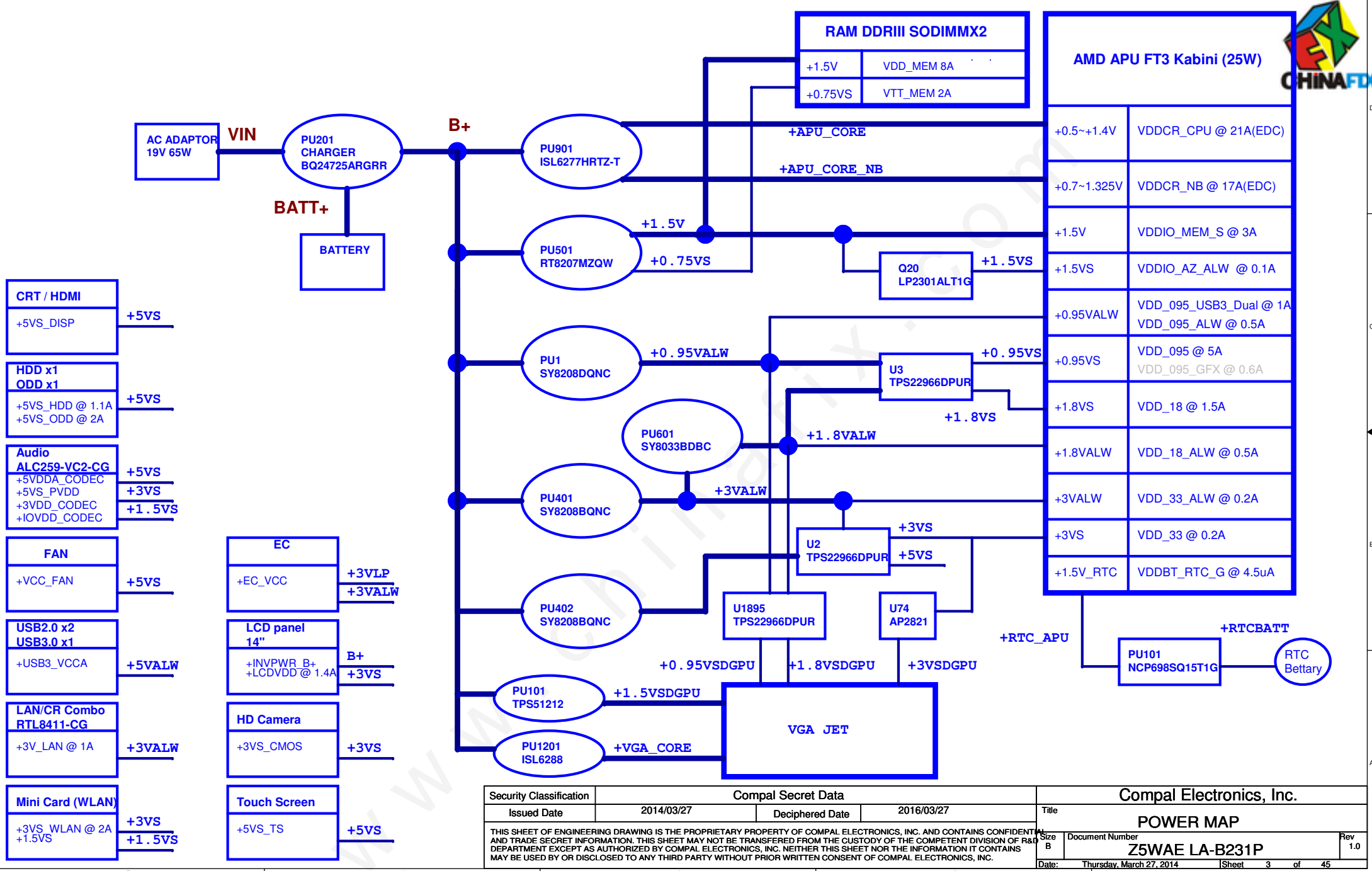
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Model Name : Z5WAE



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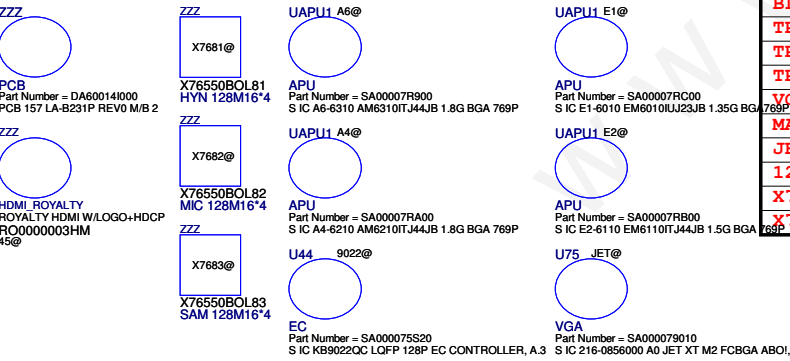
Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+0.95VALW	0.95V always on power rail	ON	ON	ON
+0.95VS	0.95V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for APU and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_APU	RTC power	ON	OFF	OFF
+3VSDGPU	VGA power	ON	OFF	OFF
+1.8VSDGPU	VGA power	ON	OFF	OFF
+1.5VSDGPU	VGA power	ON	OFF	OFF
+0.95VSDGPU	VGA power	ON	OFF	OFF
+VGA_CORE	VGA power	ON	OFF	OFF

SMBus List

EC SMBus Port1 (+3VALW)			EC SMBus Port2 (+3VS)		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	SB-TSI (APU)	1001 100X b	98H
			VGA Temp.		41H

APU SMBus Port0 (+3VS)			APU SMBus Port1(+3VALW)		
Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1010 000Xb	A0H			
DDR DIMM2	1010 001Xb	A2H			
Mini Card (DNI)					



Board ID / SKU ID Table for AD channel

Vcc	3.3V				
Ra	100K +/- 1%				
Board ID	Rb	V min	V typ	V max	EC AD
0	0		0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V		0xE7 - 0xFF

BOARD ID Table

Board ID	PCB Revision
0	EVT
1	DVT
2	PVT
3	
4	
5	
6	
7	

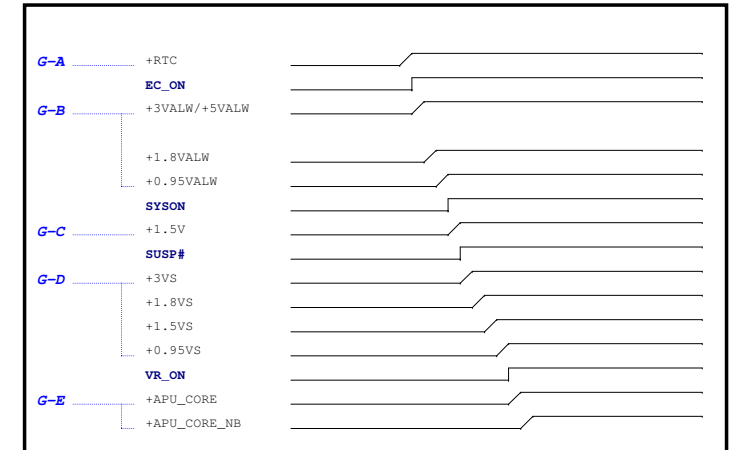


BOM Structure Table

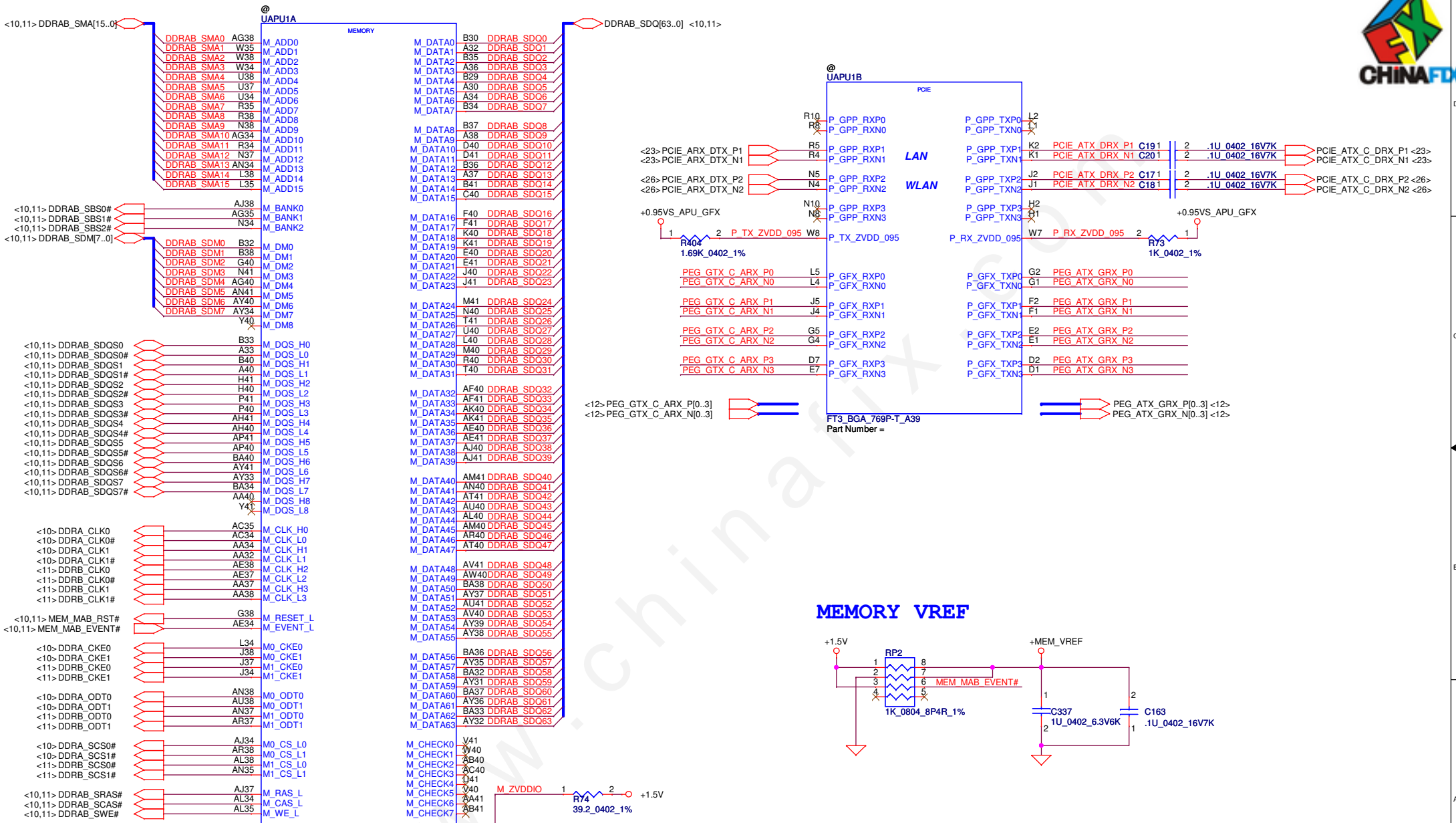
BOM Structure	BTO Item
@	Unpop
CONN@	Connector part control by ME
EMI@	EMI pop component
@EMI@	EMI unpop component
ESD@	ESD pop component
@ESD@	ESD unpop component
AL@	Auto Load EC ROM
RS@	R-short
JP@	Jump
TP@	Test point
SP@	Short pad for clear CMOS
1DMIC@	Use 1 DMIC
2DMIC@	Use 2 DMIC
45@	HDMI royalty
9012@	Use KBC9012
9022@	Use KBC9022
A6@	Use A6 APU
E1@	Use E1 APU
BL@	Keyboard backlight
TPM@	Use discrete TPM module
TPUSB@	Use USB to I2C IC for T/P
TPSM@	Use APU SMBus for T/P
VGA@	Have discrete graphic
MARS@	Use Opal
JET@	Use Jet
128@	Dual channel VRAM, pop with MARS@
X76@	VRAM type select, control by X76XX@
X76XX@	VRAM type select, control level X76

STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	ON	OFF	OFF	OFF

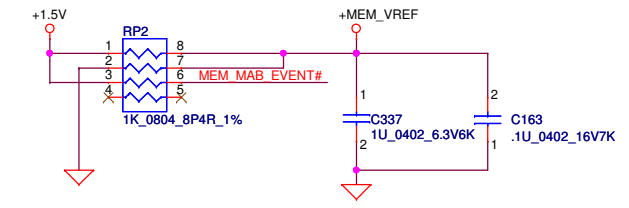
APU POWER SEQUENCE



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MEMORY VREF



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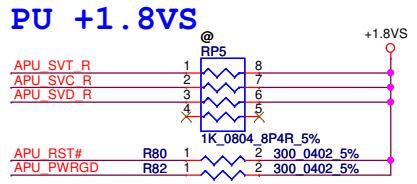
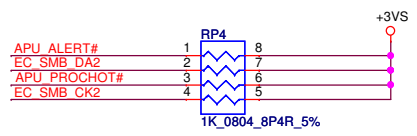
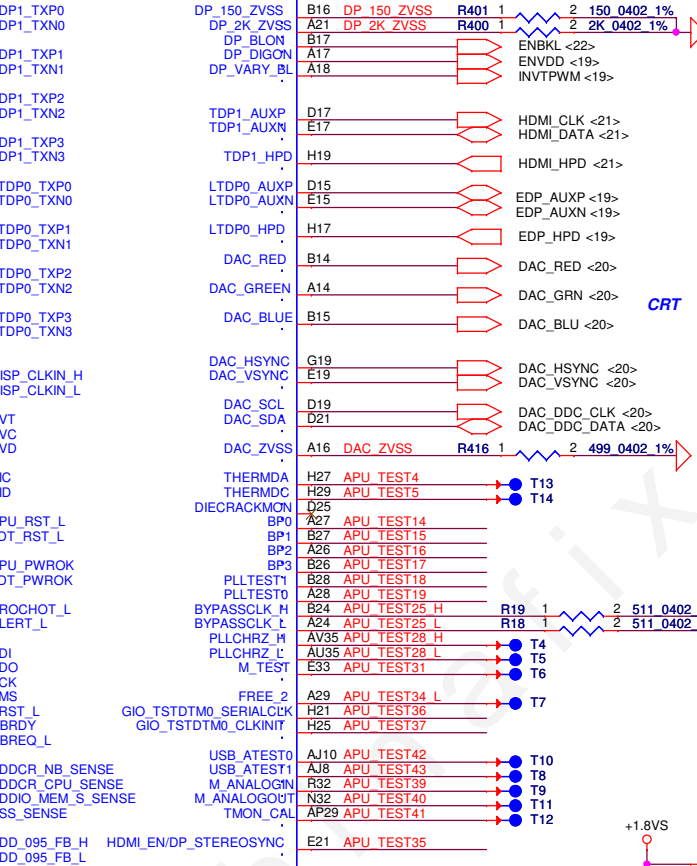
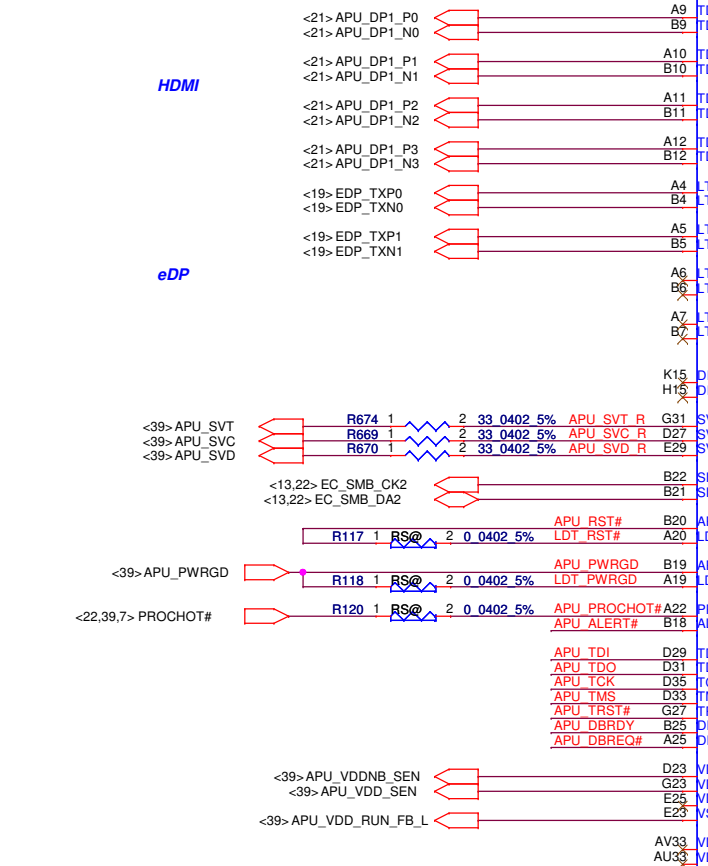


HDMI

eDP

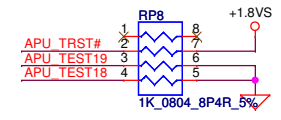
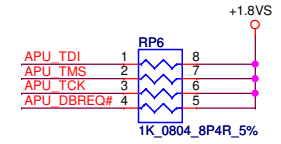
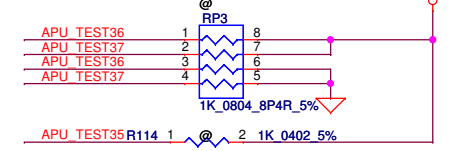
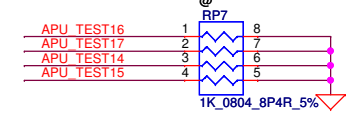
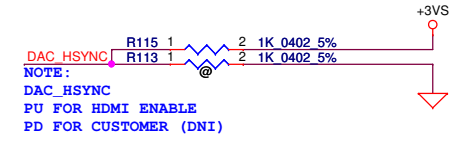
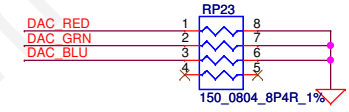
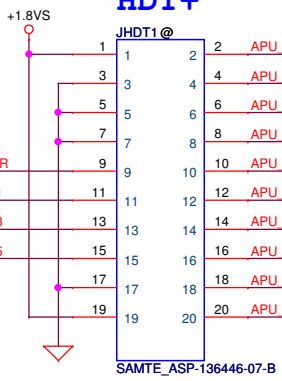
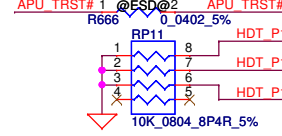
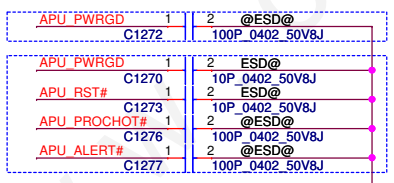
CRT

HDT+

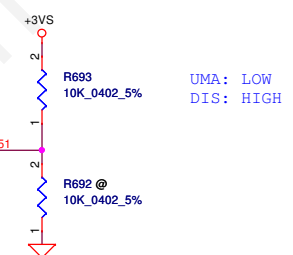
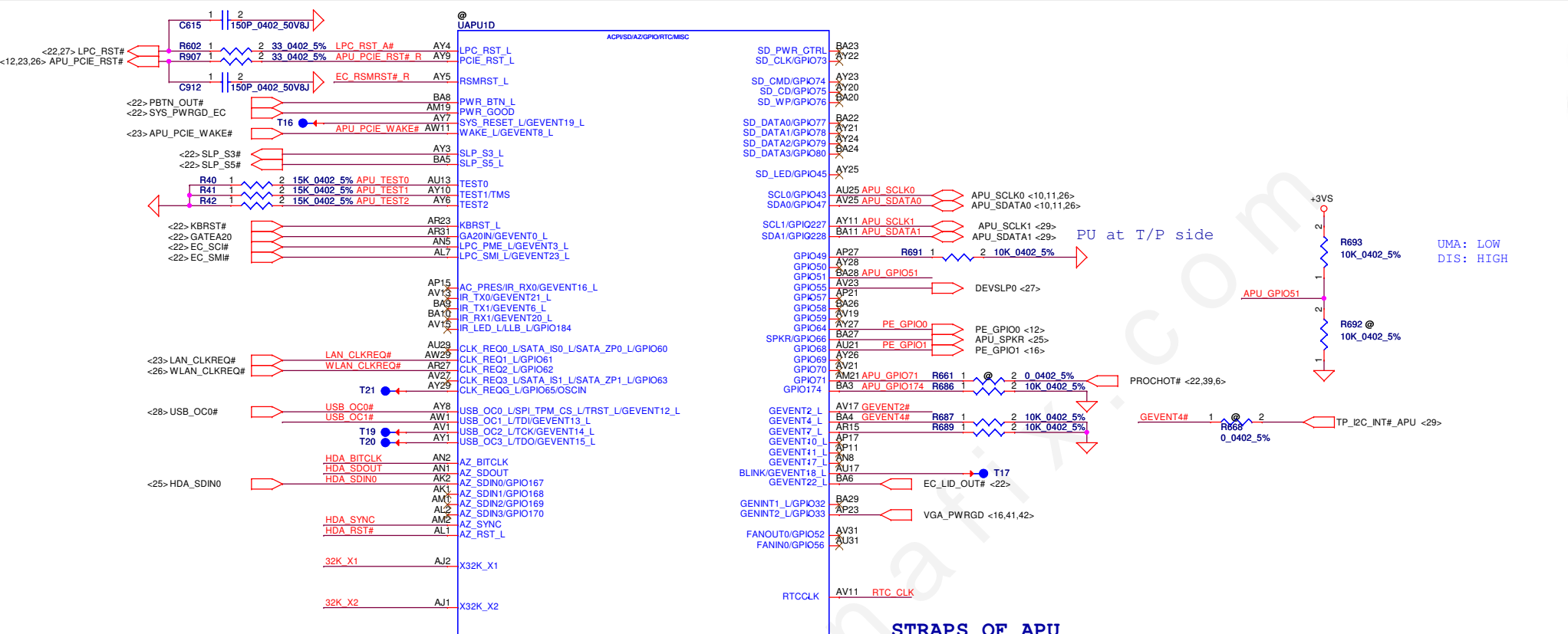


Close To PU801

Close To APU's Pin



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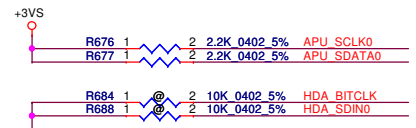
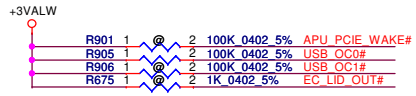
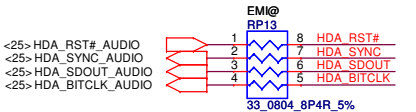
PU at T/P side

PROCHOT# <22.39.6>

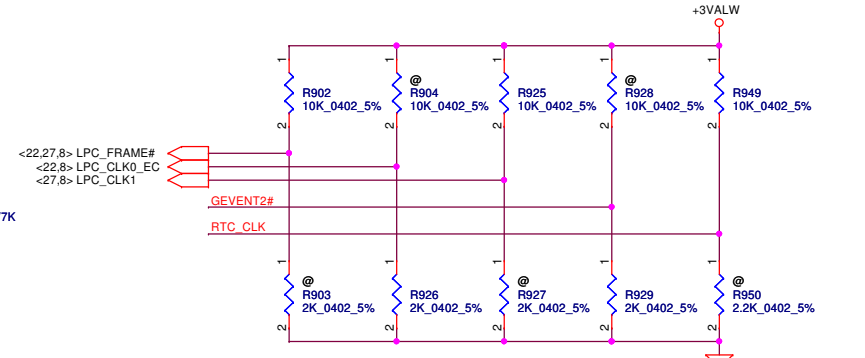
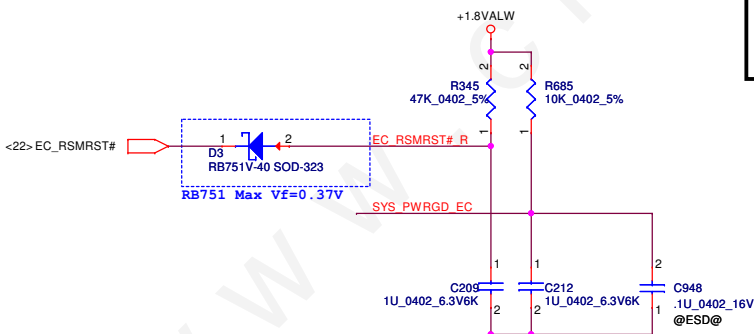
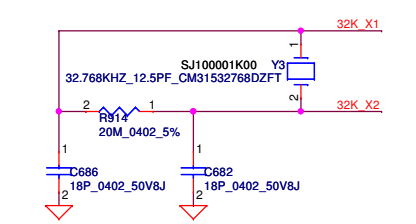
GEVENT4# 1 @ 2 TP_INT#_APU <29> 0.0402_5%

STRAPS OF APU

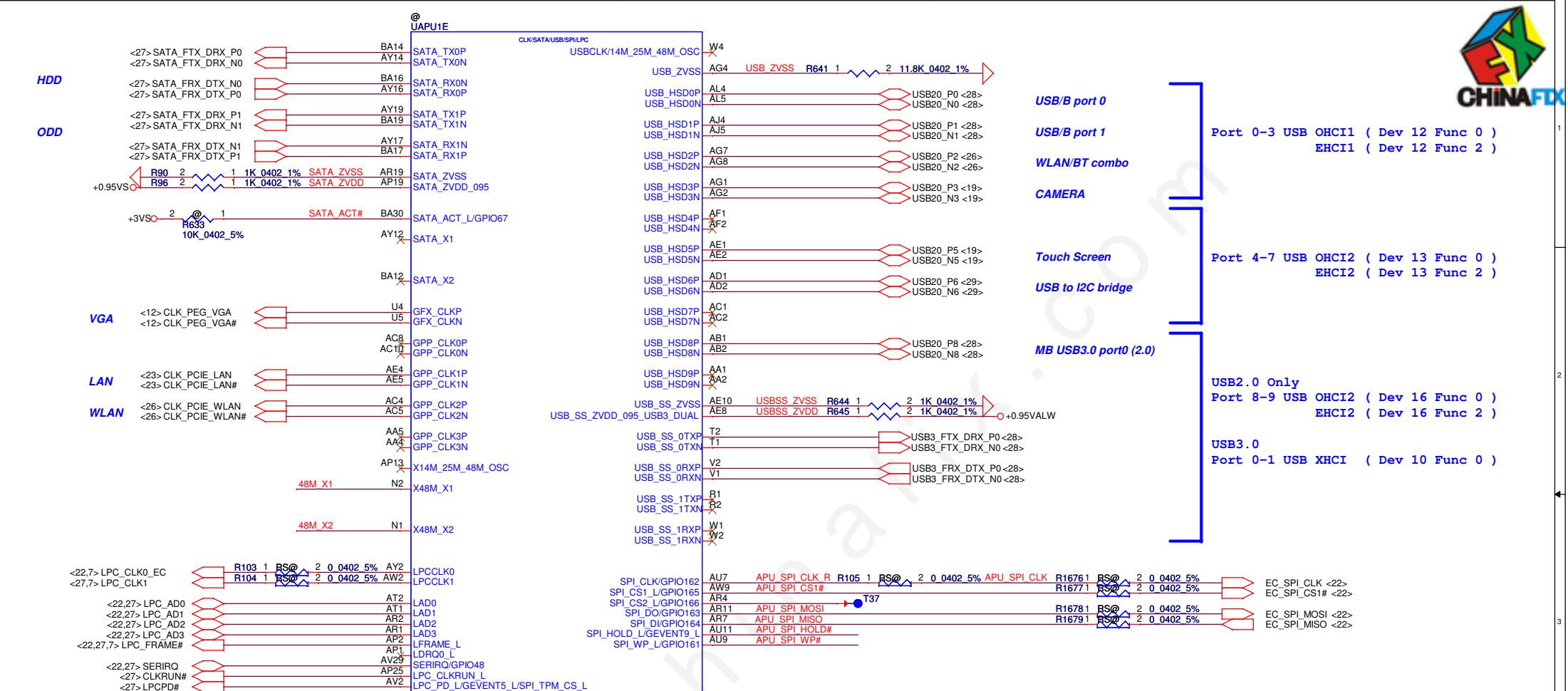
	LPC_FRAME#	LPC_CLK0_EC	LPC_CLK1	GEVENT2_L	RTC_CLK
H	SPI ROM (DEFAULT)	BOOT FAIL TIMER ENABLED	CLKGEN ENABLE (DEFAULT)	1.8V SPI ROM	NORMAL POWER UP/RESET TIMING (DEFAULT)
L	LPC ROM	BOOT FAIL TIMER DISABLED (DEFAULT)	CLKGEN DISABLED	3.3V SPI ROM (DEFAULT)	FAST POWER UP/RESET TIMING FOR SIMULATION



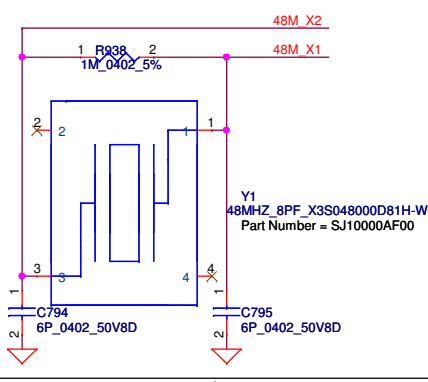
32.768KMHZ CRYSTAL



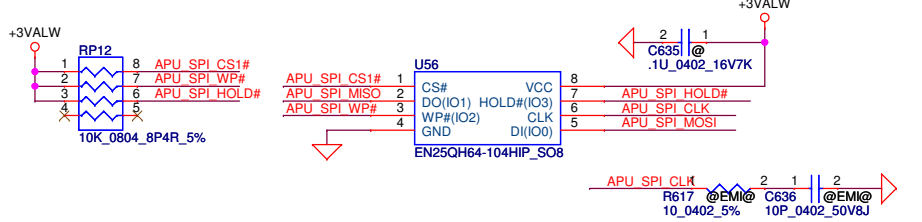
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48MHz CRYSTAL



8MB SPI ROM

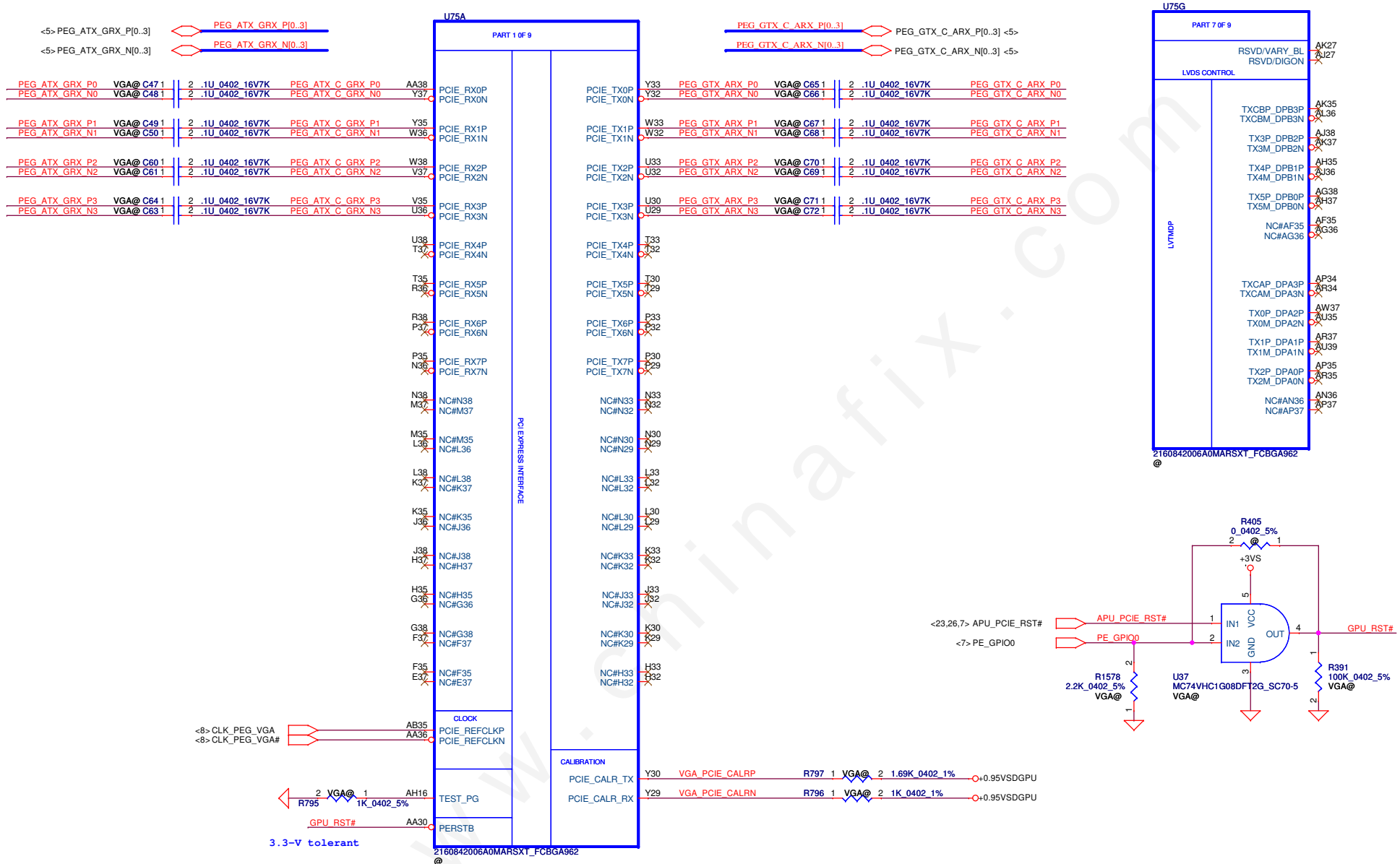


- USB/B port 0
 - USB/B port 1
 - WLAN/BT combo
 - CAMERA
 - Touch Screen
 - USB to I2C bridge
 - MB USB3.0 port0 (2.0)
 - USB2.0 Only
 - USB3.0
- Port 0-3 USB OHCI1 (Dev 12 Func 0)
EHCI1 (Dev 12 Func 2)
- Port 4-7 USB OHCI2 (Dev 13 Func 0)
EHCI2 (Dev 13 Func 2)
- Port 8-9 USB OHCI2 (Dev 16 Func 0)
EHCI2 (Dev 16 Func 2)
- Port 0-1 USB XHCI (Dev 10 Func 0)

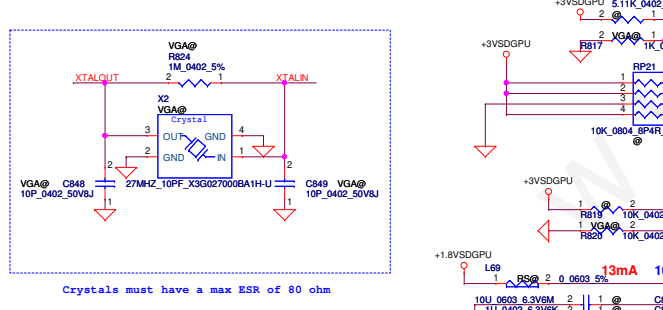
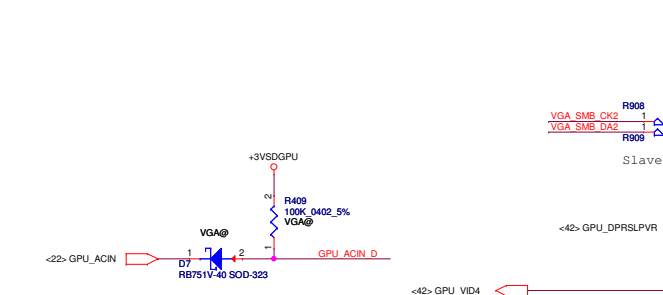
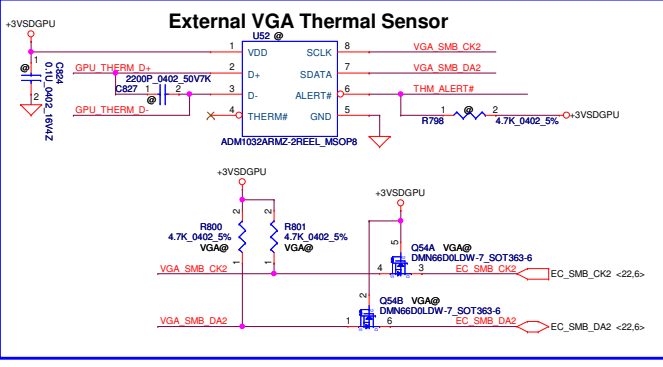
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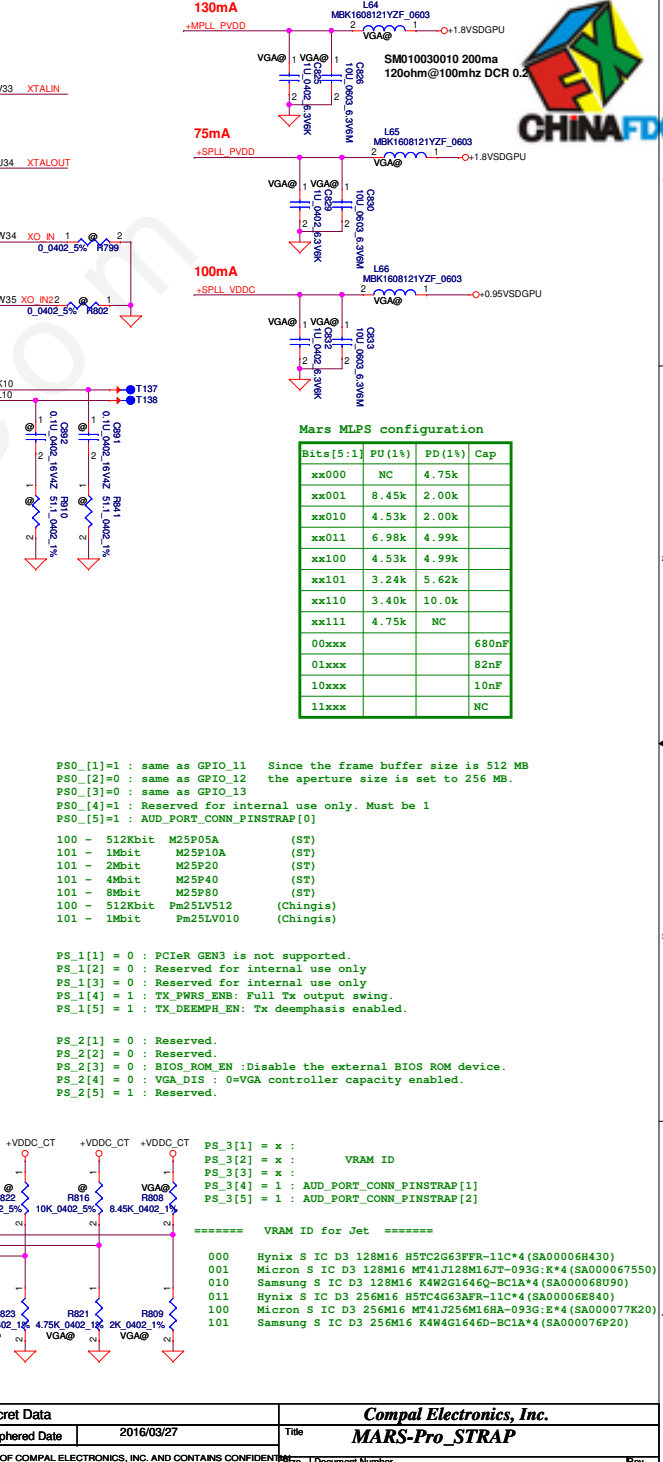
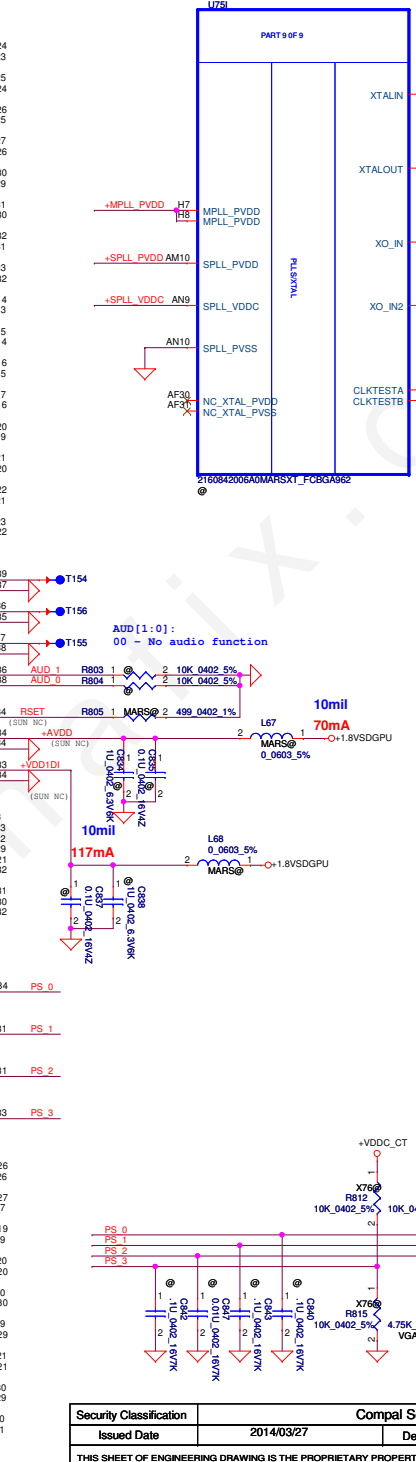
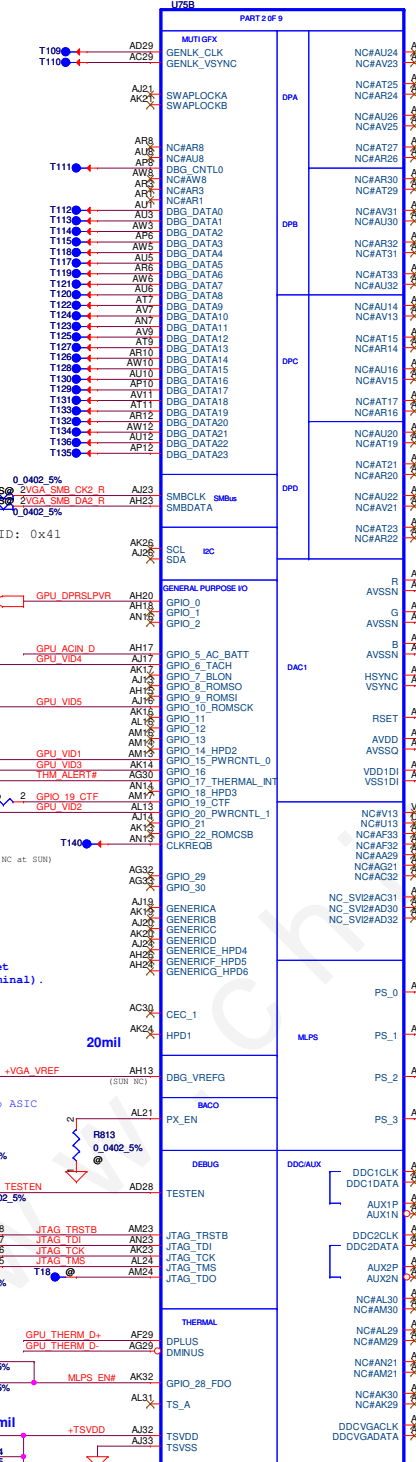
GFX PCIE LANE REVERSAL



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Crystals must have a max ESR of 80 ohm



Mars MLPS configuration

Bits[5:1]	PU(1%)	PD(1%)	Cap
xx000	NC	4.75k	
xx001	8.45k	2.00k	
xx010	4.53k	2.00k	
xx011	6.98k	4.99k	
xx100	4.53k	4.99k	
xx101	3.24k	5.62k	
xx110	3.40k	10.0k	
xx111	4.75k	NC	
00xxx			680nF
01xxx			82nF
10xxx			10nF
11xxx			NC

PS0 [1]=1 : same as GPIO_11 Since the frame buffer size is 512 MB
 PS0 [2]=0 : same as GPIO_12 the aperture size is set to 256 MB.
 PS0 [3]=0 : same as GPIO_13
 PS0 [4]=1 : Reserved for internal use only. Must be 1
 PS0 [5]=1 : AUD_PORT_CONN_PINSTRAP[0]

100 - 512kbit M25P05A (ST)
 101 - 1Mbit M25P10A (ST)
 101 - 2Mbit M25P20 (ST)
 101 - 4Mbit M25P40 (ST)
 101 - 8Mbit M25P80 (ST)
 100 - 512Kbit Pm25LV512 (Chingis)
 101 - 1Mbit Pm25LV010 (Chingis)

PS_1[1] = 0 : PCIeR GEN3 is not supported.
 PS_1[2] = 0 : Reserved for internal use only
 PS_1[3] = 0 : Reserved for internal use only
 PS_1[4] = 1 : TX_PWRS_ENB: Full Tx output swing.
 PS_1[5] = 1 : TX_DEEMPH_EN: Tx deemphasis enabled.

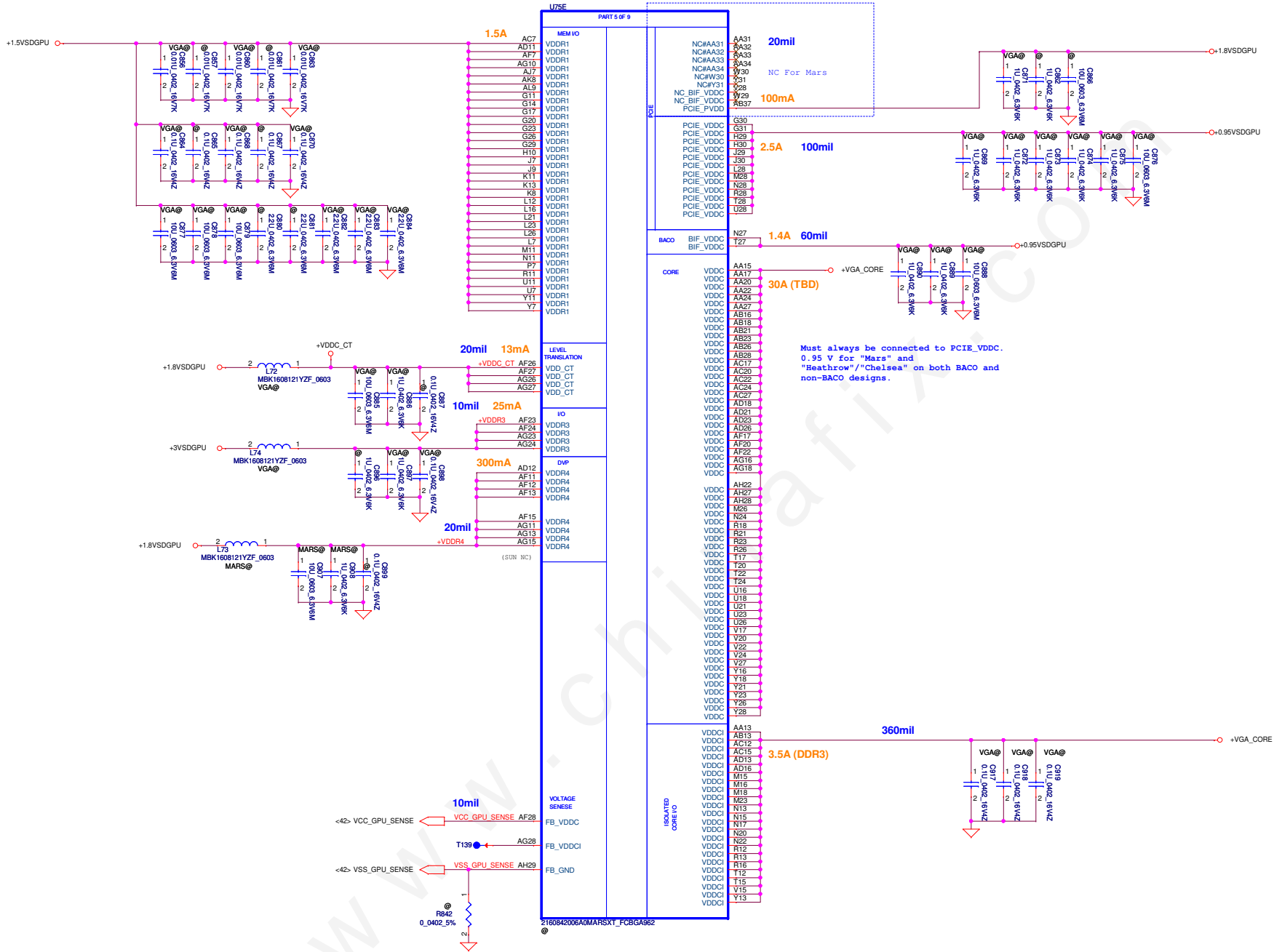
PS_2[1] = 0 : Reserved.
 PS_2[2] = 0 : Reserved.
 PS_2[3] = 0 : BIOS_ROM_EN :Disable the external BIOS ROM device.
 PS_2[4] = 0 : VGA_DIS = 0=VGA controller capacity enabled.
 PS_2[5] = 1 : Reserved.

PS_3[1] = x :
 PS_3[2] = x : VRAM ID
 PS_3[3] = x :
 PS_3[4] = 1 : AUD_PORT_CONN_PINSTRAP[1]
 PS_3[5] = 1 : AUD_PORT_CONN_PINSTRAP[2]

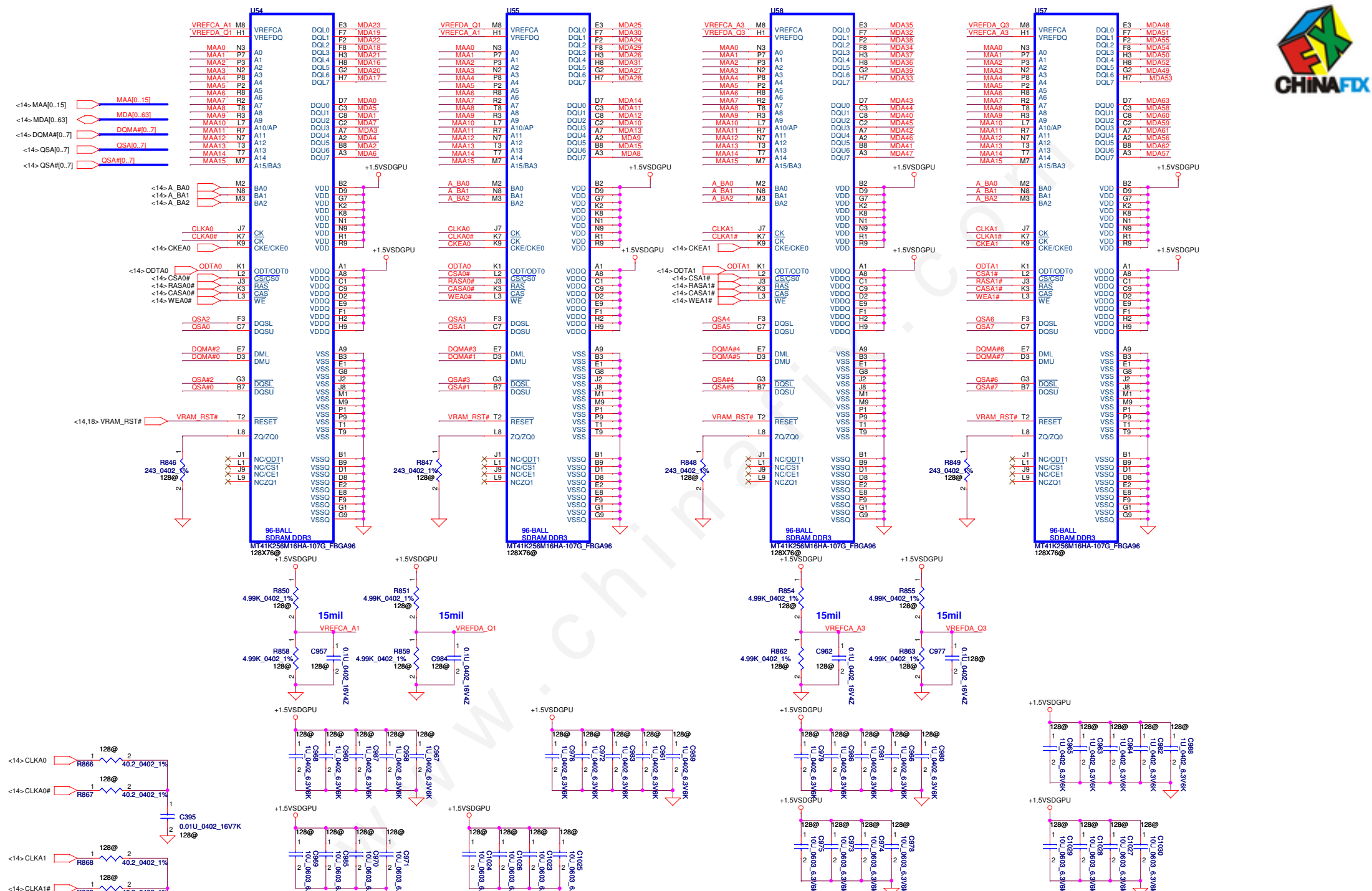
===== VRAM ID for Jet =====

000 Hynix S IC D3 128M16 H5TC2G63FFR-11C*4 (SA00006H430)
 001 Micron S IC D3 128M16 M741J128M16JT-093G:K*4 (SA000067550)
 010 Samsung S IC D3 128M16 K4W2G16460-BC1A*4 (SA000068099)
 011 Hynix S IC D3 256M16 H5PC4G63A8R-11C*4 (SA000068840)
 100 Micron S IC D3 256M16 M741J256M16HA-093G:E*4 (SA000077K20)
 101 Samsung S IC D3 256M16 K4W4G1646D-BC1A*4 (SA000076P20)

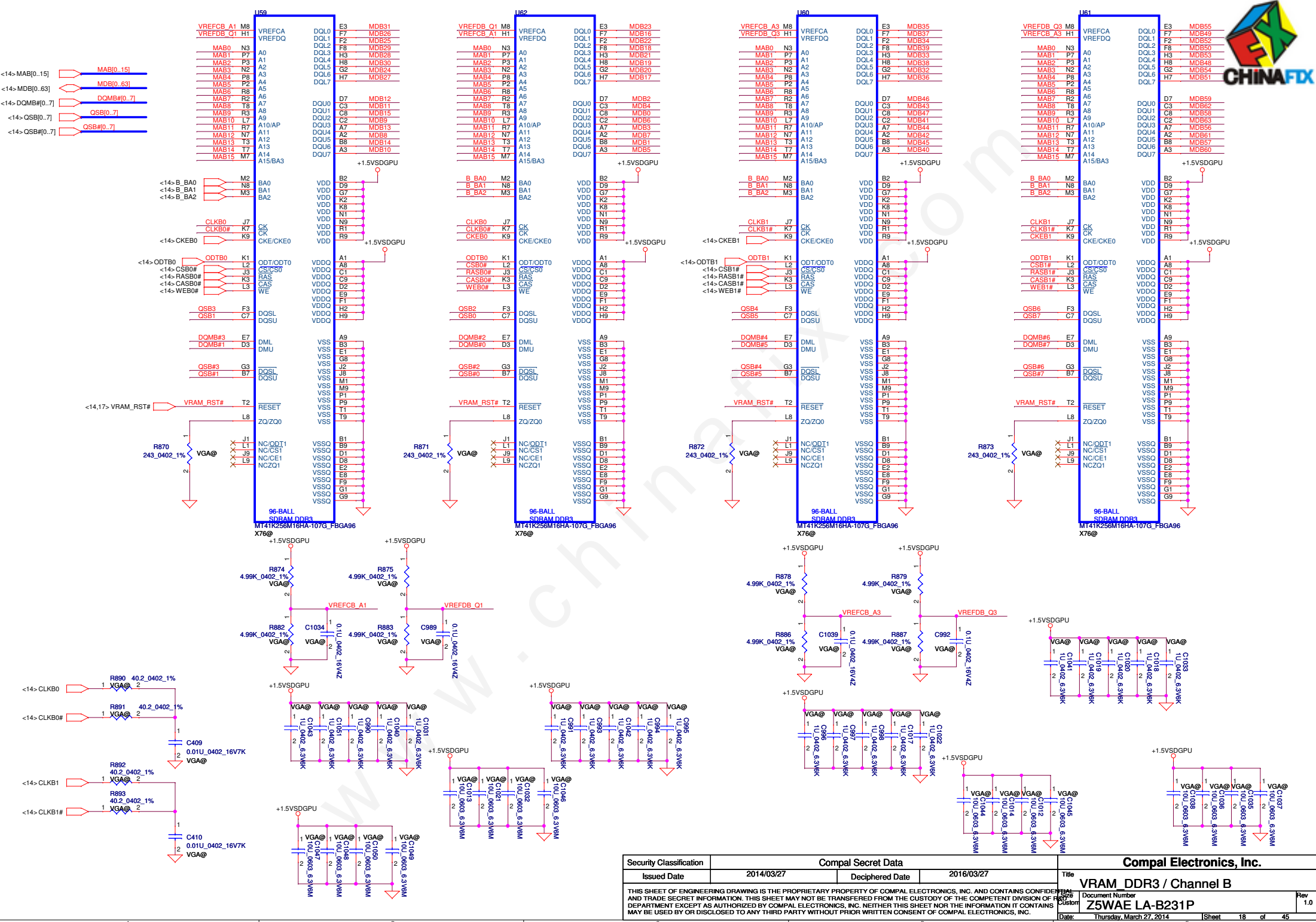
Security Classification	Compal Secret Data		Title	
Issued Date	2014/03/27	Deciphered Date	2016/03/27	MARS-Pro_STRAP
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				Document Number	1.0
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Issued Date	2014/03/27	Deciphered Date	2016/03/27	Title
				VRAM_DDR3 / Channel A
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Date:	Thursday, March 27, 2014	Sheet	17	of 45

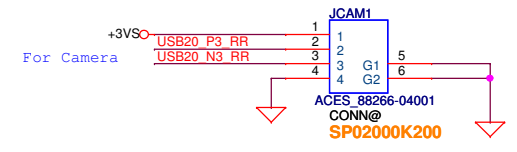
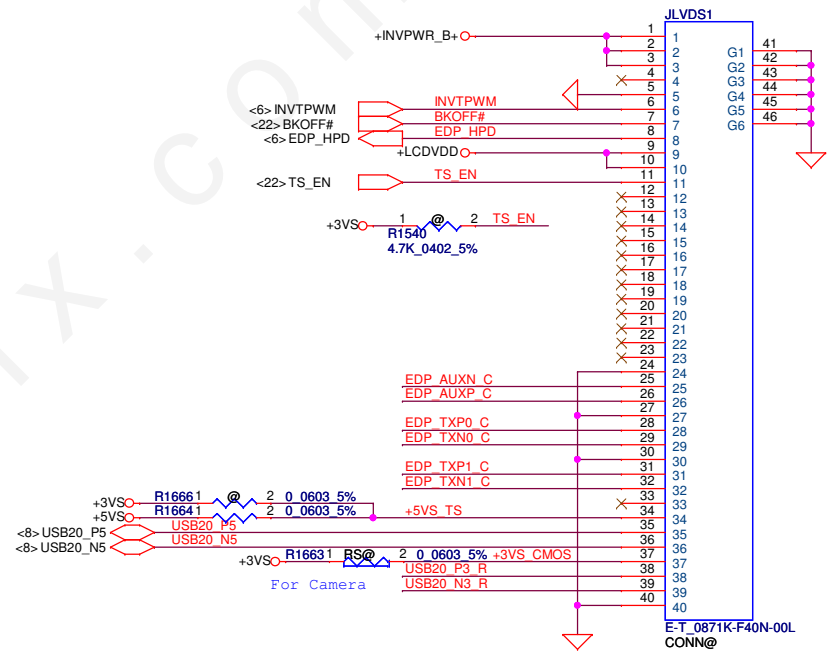
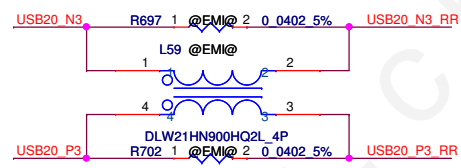
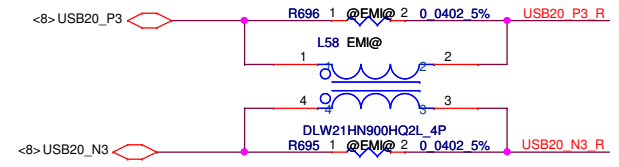
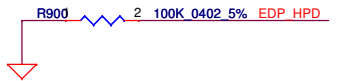
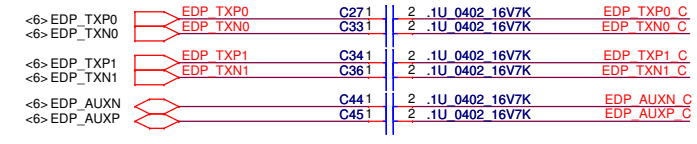
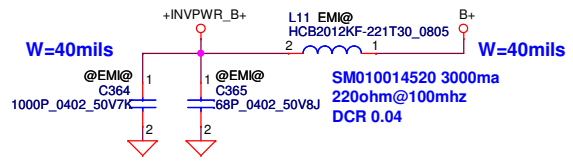
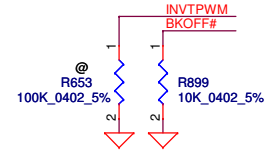
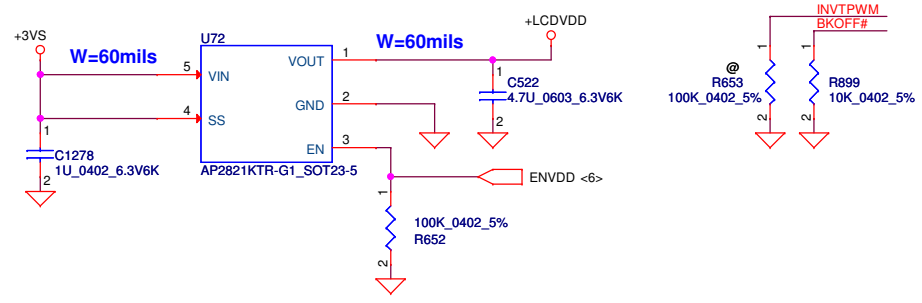


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Date:	Thursday, March 27, 2014	Sheet	18	of 45

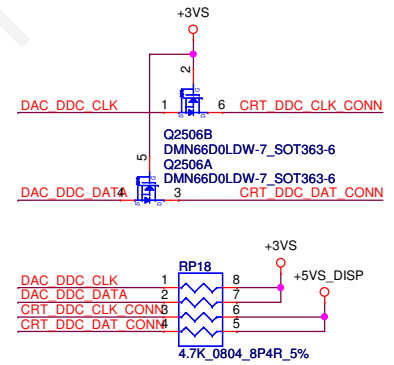
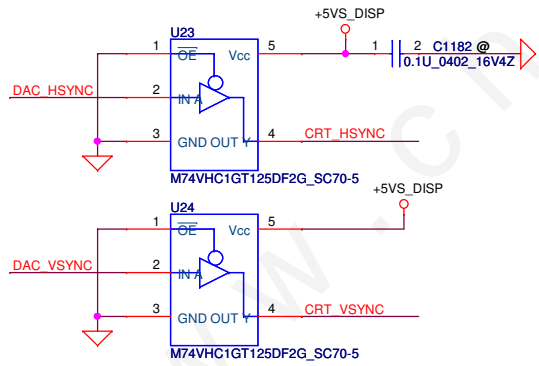
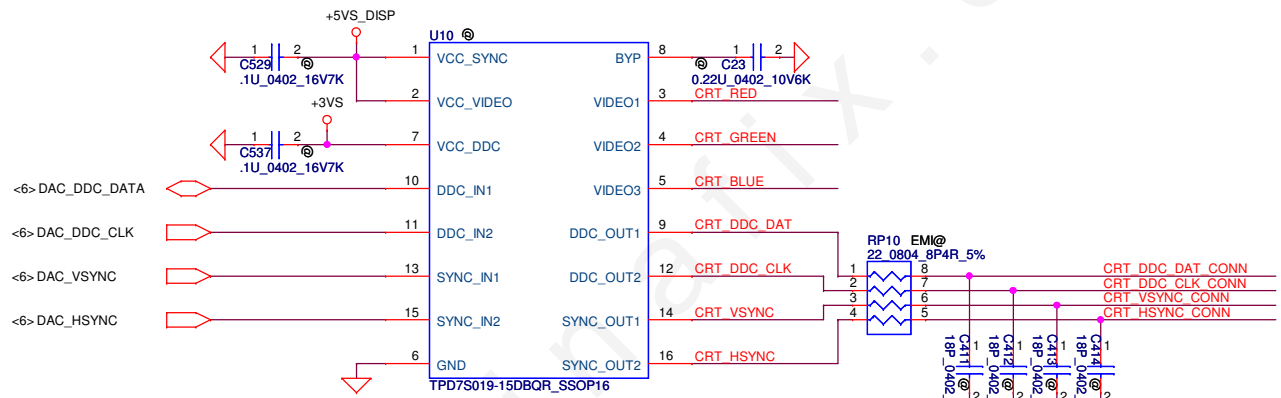
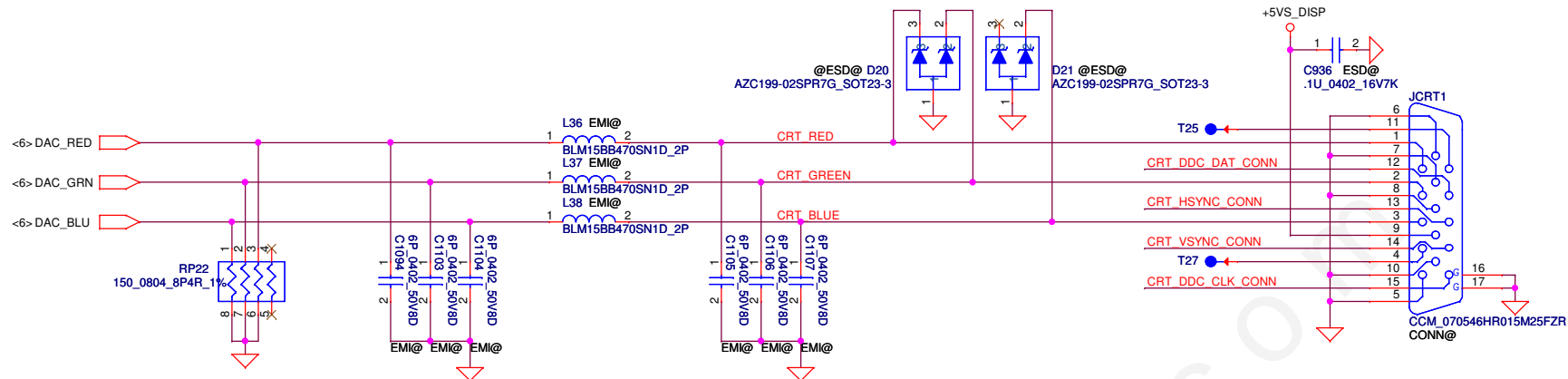
LCD POWER CIRCUIT



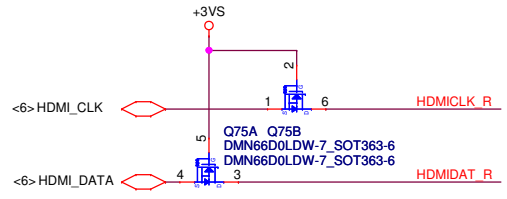
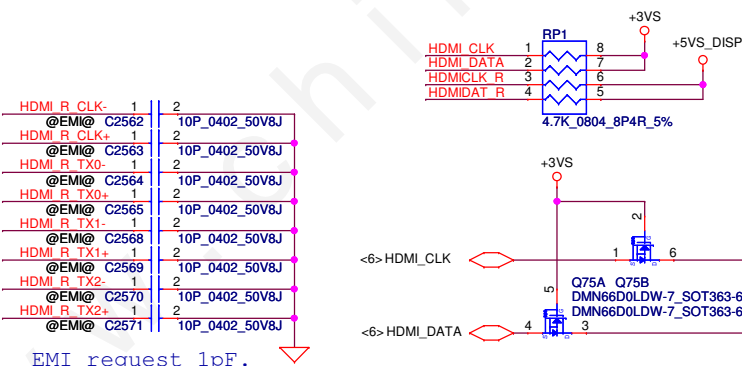
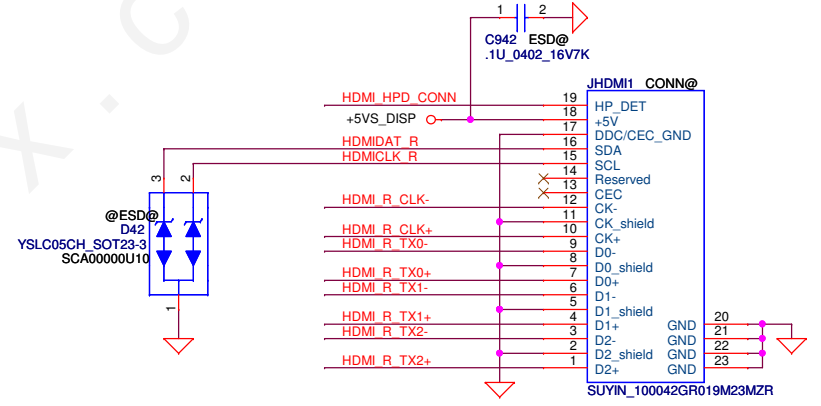
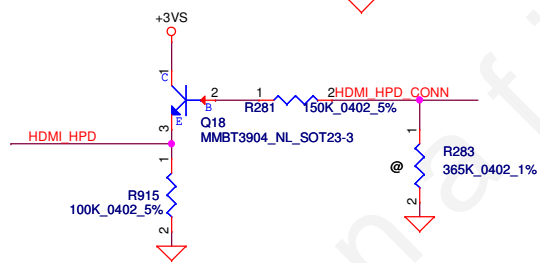
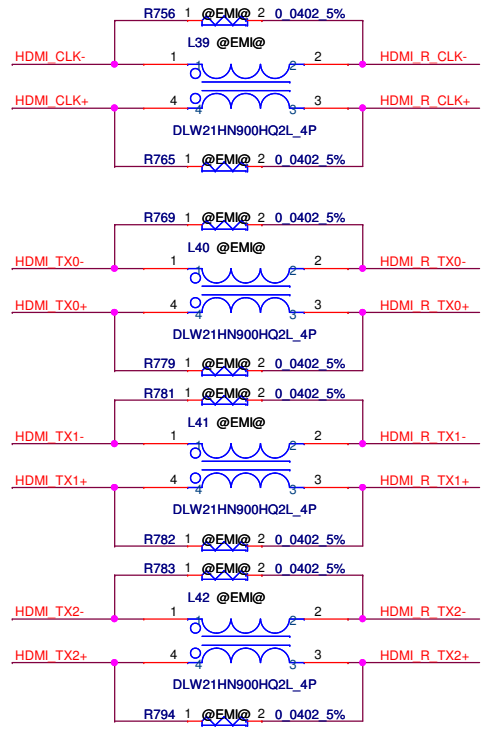
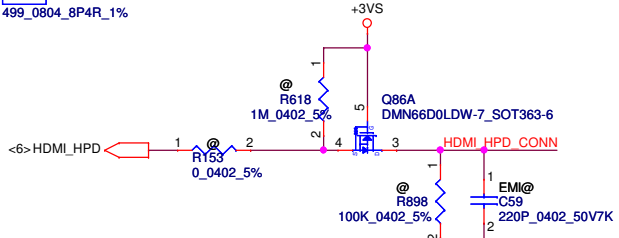
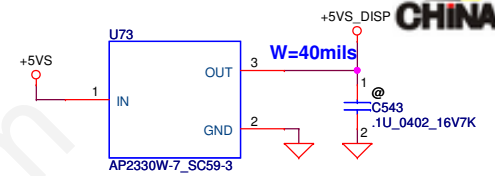
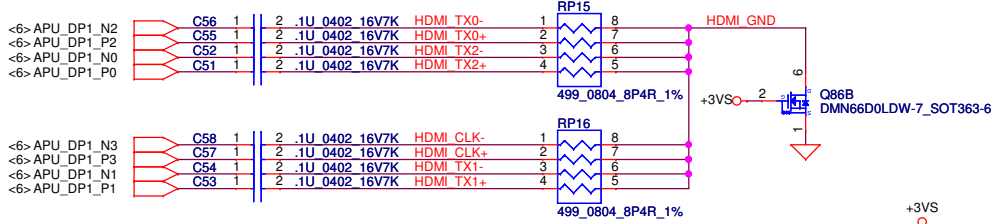
eDP PANEL Conn.



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				Date:	Thursday, March 27, 2014	Sheet 19 of 45



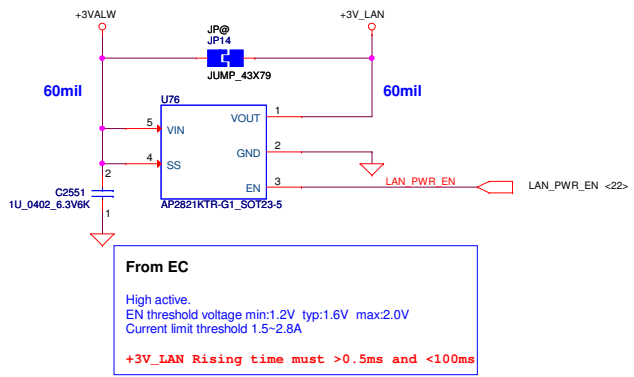
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2014/03/27	Deciphered Date	2016/03/27	Title CRT CONN	
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				Z5WAE LA-B231P	



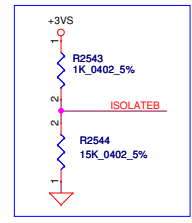
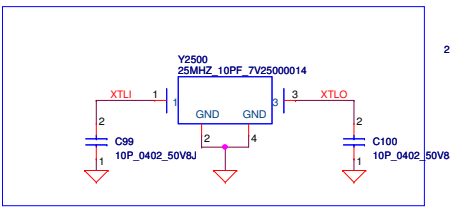
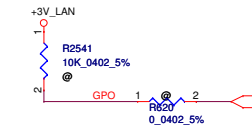
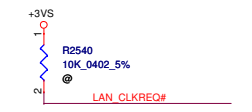
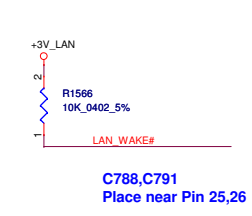
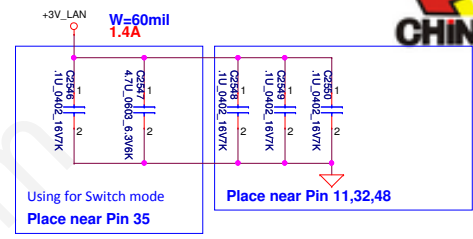
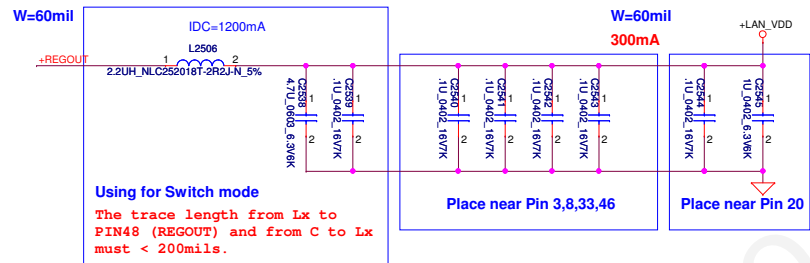
EMI request 1pF.

HDMI R_CLK-	1	2
HDMI R_CLK+	1	2
HDMI R_TX0-	1	2
HDMI R_TX0+	1	2
HDMI R_TX1-	1	2
HDMI R_TX1+	1	2
HDMI R_TX2-	1	2
HDMI R_TX2+	1	2

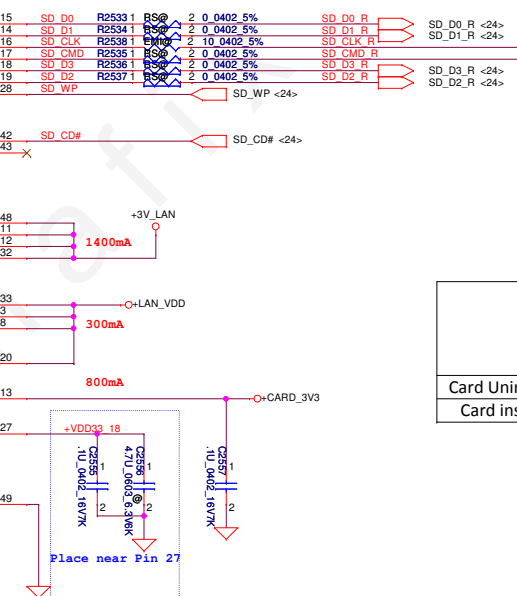
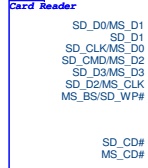
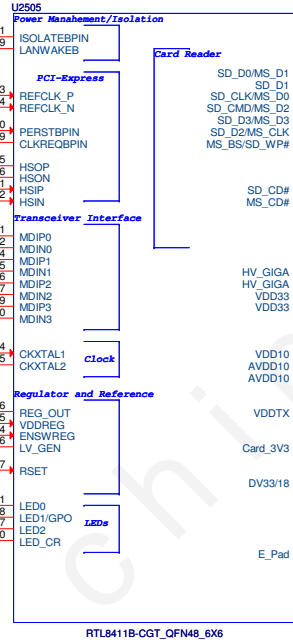
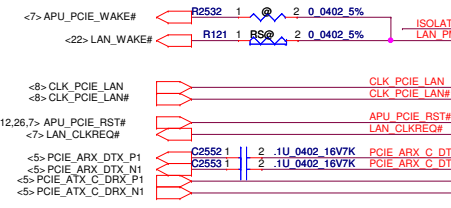
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/03/27	Deciphered Date	2016/03/27	Title
				HDMI CONN
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From EC
 High active.
 EN threshold voltage min:1.2V typ:1.6V max:2.0V
 Current limit threshold 1.5-2.8A
+3V_LAN Rising time must >0.5ms and <100ms

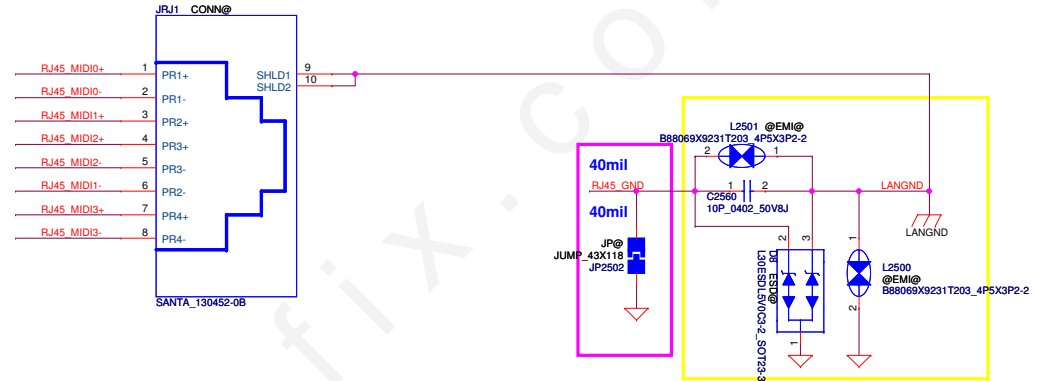
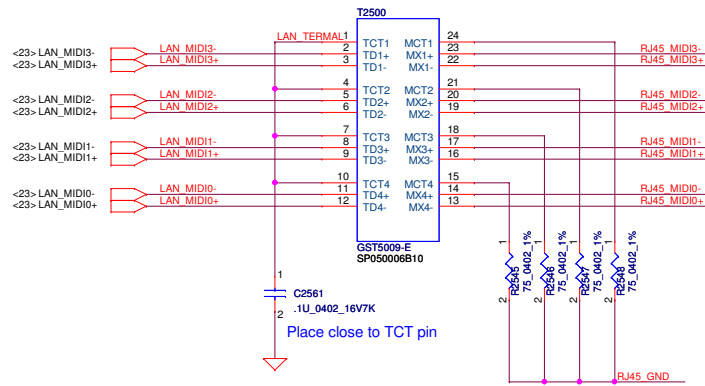


EC_PME# pull high 10K to +3VALW on EC side

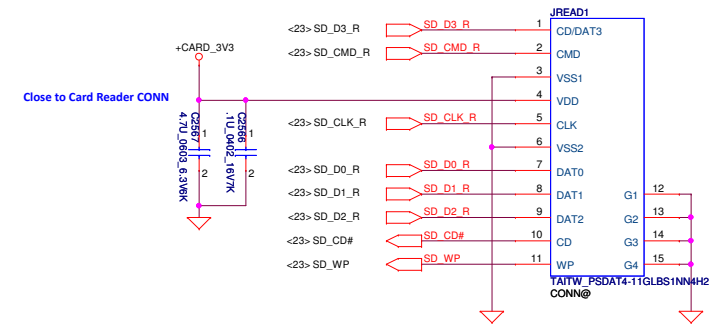


	Protect cotact		Card contact
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Open	Close	Close

LAN Connector

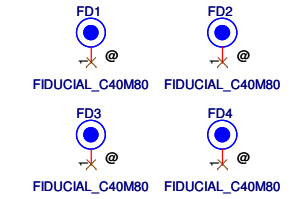
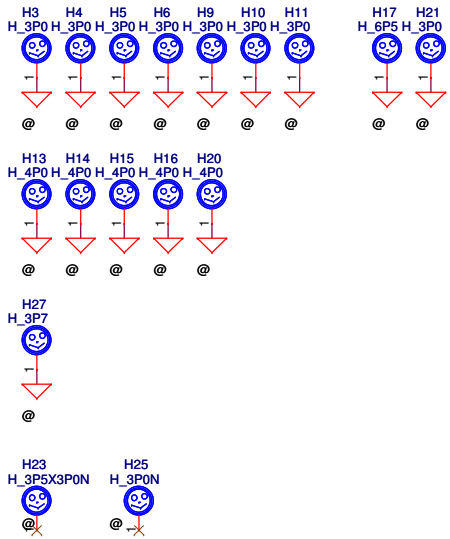
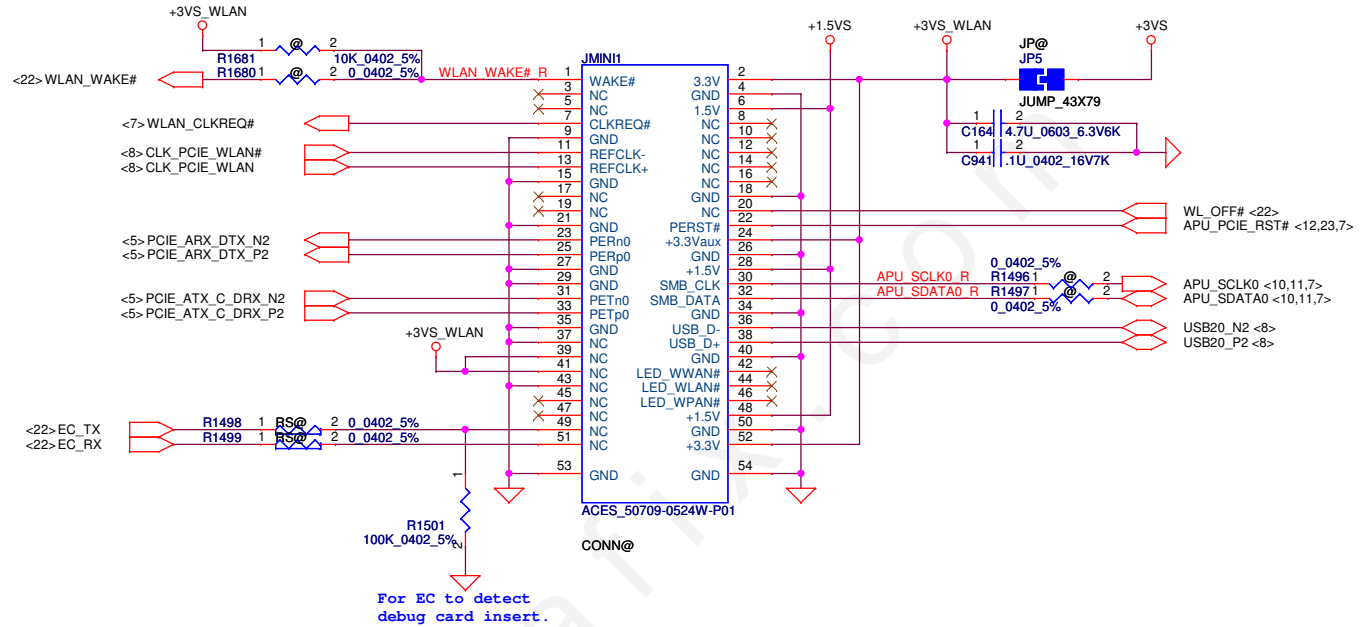
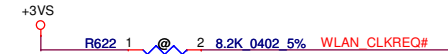
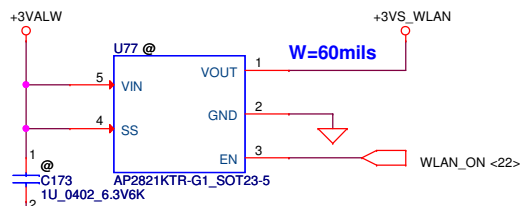


Card Reader Connector



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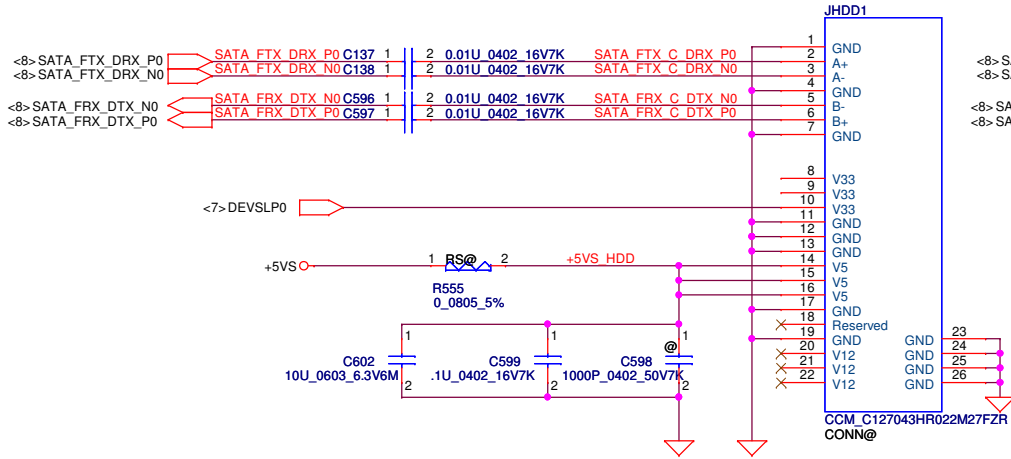
Mini-Express Card(WLAN/WiMAX) H=4mm



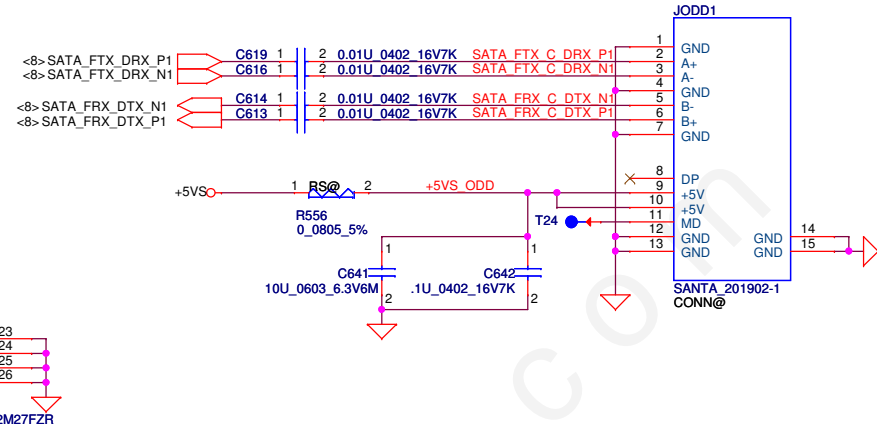
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2014/03/27	Deciphered Date	2016/03/27	Title MINI CARD (WLAN)/Screw	
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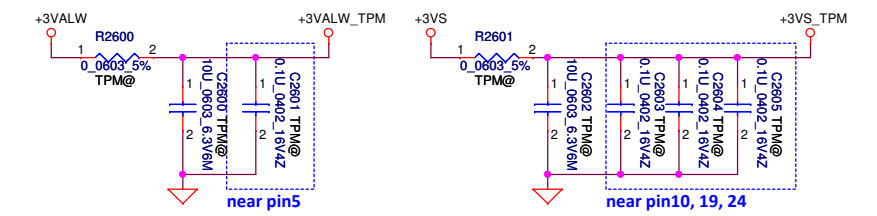
SATA HDD Conn.



SATA ODD Conn.



TPM



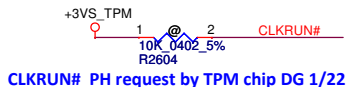
BADD	SELECTION
0	Eh - EfH
* 1	7Eh - 7Fh

GPIO3/BADD with Internal PH (default)

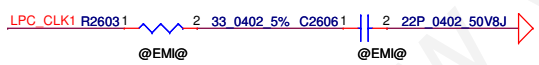
AMD CLKRUN# no need PH (DG1.1)

LPCPD# had internal PH

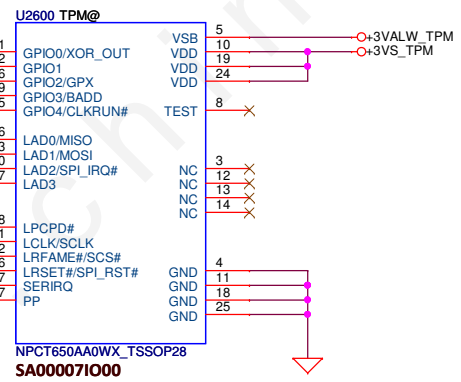
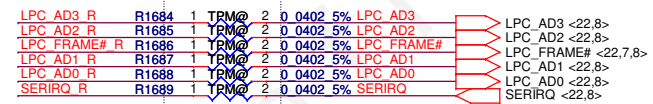
SERIRQ no need PH



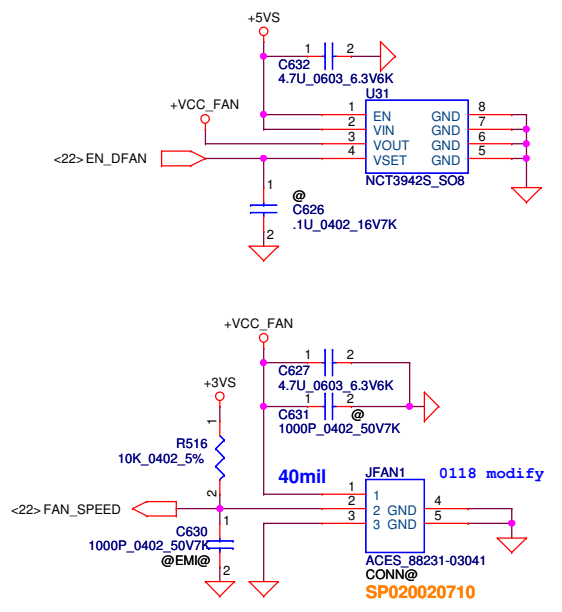
CLKRUN# PH request by TPM chip DG 1/22



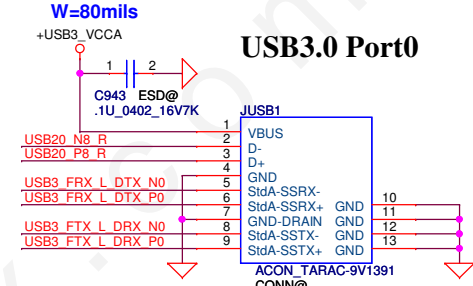
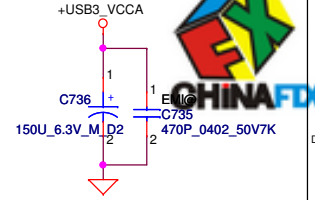
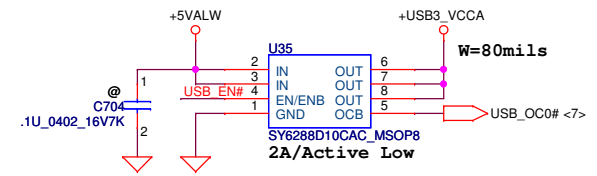
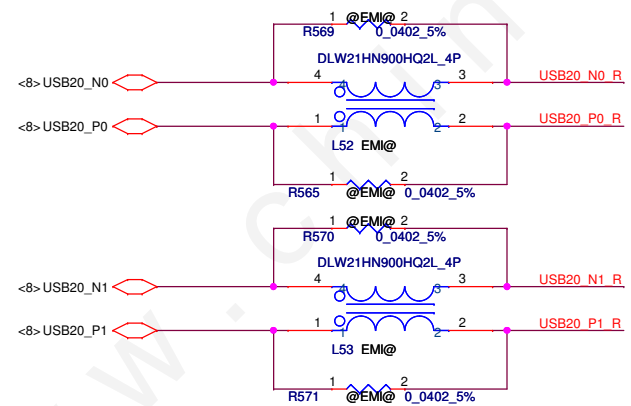
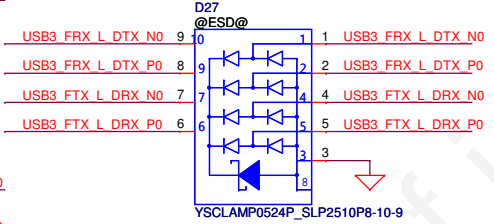
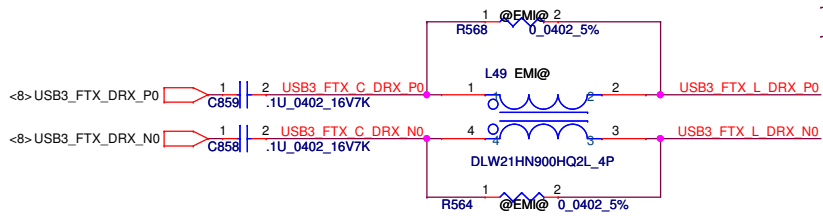
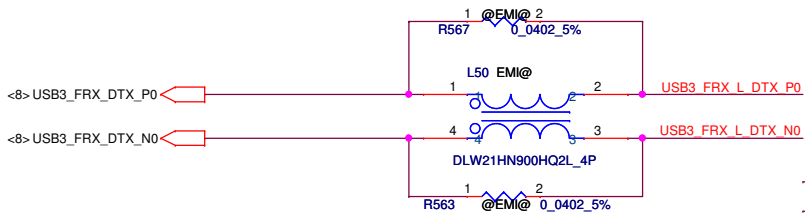
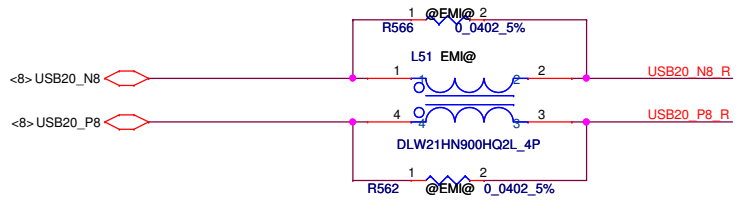
close to EC



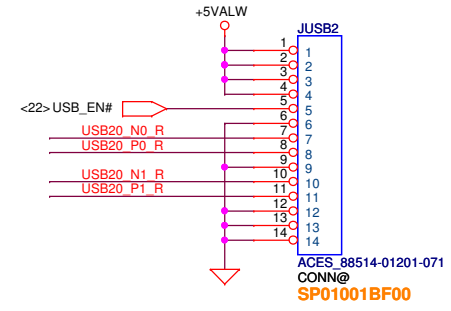
FAN Conn



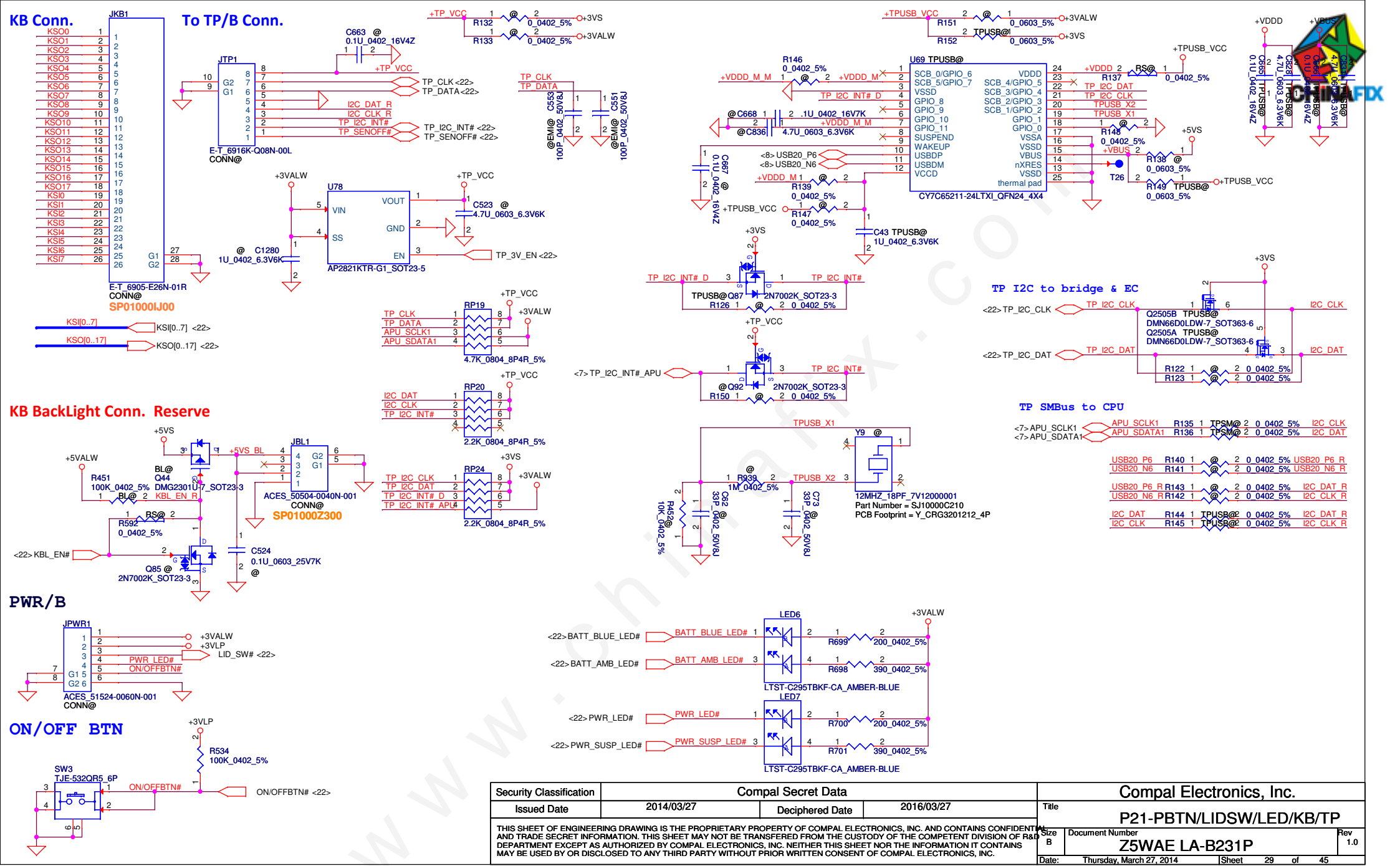
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USB/B(USB Port 0, Port1)



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				Date:	Thursday, March 27, 2014
				Sheet	28 of 45
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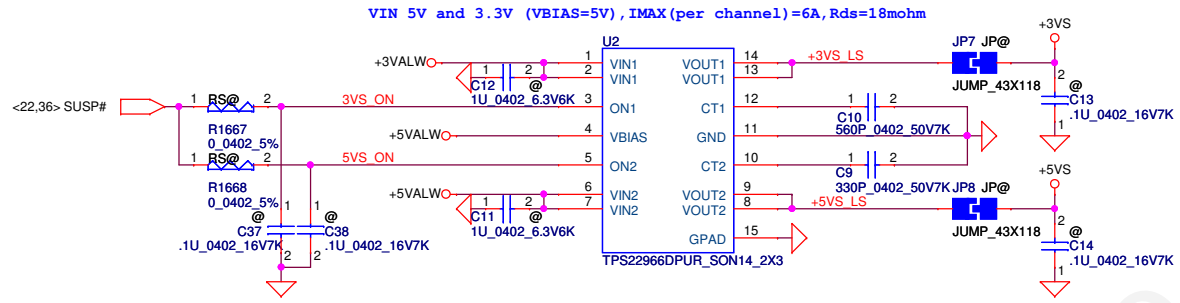


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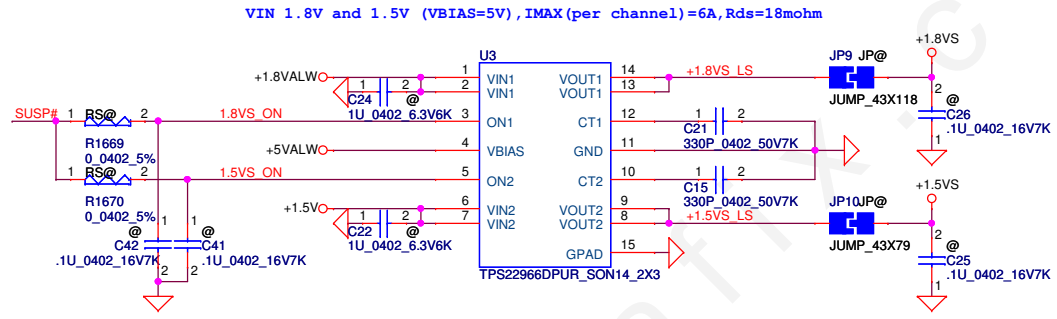
Compal Electronics, Inc.			
Title			
P21-PBTN/LIDSW/LED/KB/TP			
Size	Document Number	Rev	
B	Z5WAE LA-B231P	1.0	
Date:	Thursday, March 27, 2014	Sheet	29 of 45



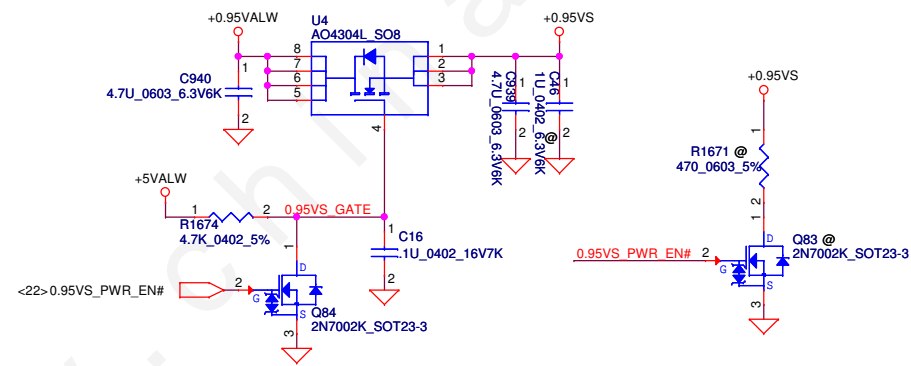
+5VALW TO +5VS
+3VALW TO +3VS
Load switch



+1.8VALW TO +1.8VS
+1.5V TO +1.5VS
Load switch



+0.95VALW to +0.95VS



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0.2

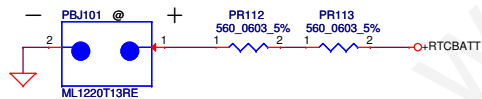
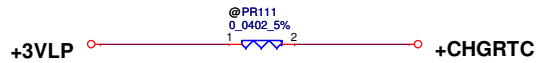
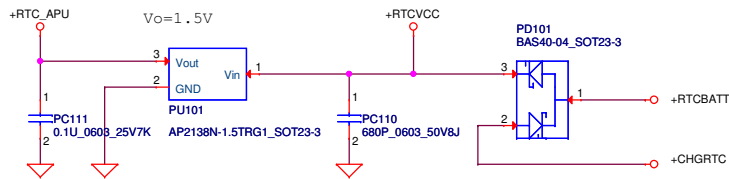
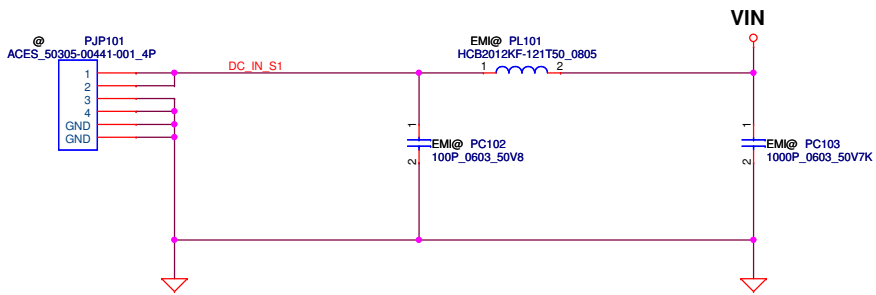
1. Add R693 for UMA/DIS select
2. Change R756,R765,R769,R779,R781,R782,R783 and R794 to Rshort for EMI request
3. Change BID to 1 for DVT
4. Change LAN_WAKE# PU to +3V_LAN
5. Add L76,L77,C2142 and C2140 for ESD request
6. Change R238 and R237 to 59ohm
7. Add L52,L53,R565,R569,R570 and R571 for EMI request.
8. Add R140,R141,R142,R143,R144 and R145 for reserve USB TP
9. Pop Q89, unpop R1690
10. Change D10 to SCA00001B00
11. Change L11 to SM01000EJ00
12. Add U39,R833,C185,R1578 for VGA power sequence issue
13. Remove APU_ALERT#_R
14. Add C668 and C836 for vendor request

0.3

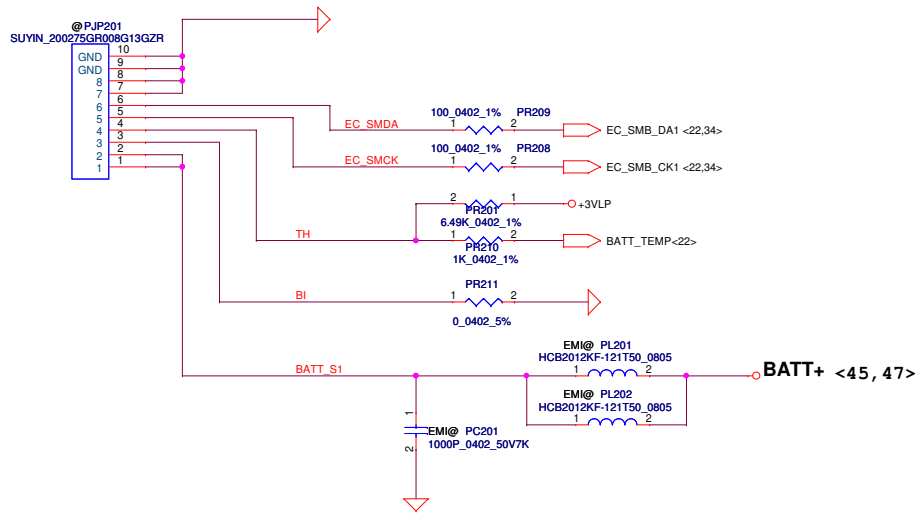
1. Change JTP1
2. Add U78 for TP +3V power plane
3. Change C849, C849 to 10p
4. Change C736 to 150u D2 type.
5. Change R699, R700 to 330ohm; R698, R701 to 560ohm
6. Change U69 +3VALW to +3VS
7. Add C366, C367, C368, C369 for EMI request
8. Add on board TPM
9. Add R619

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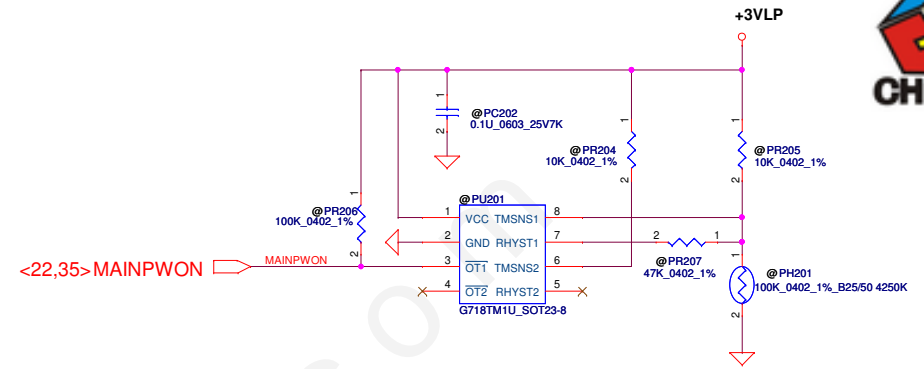
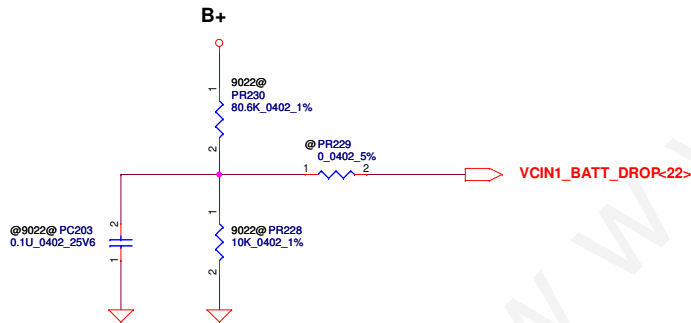
---Battery_pin define---
PIN1 GND
PIN2 GND
PIN3 SMD
PIN4 SMC
PIN5 TS
PIN6 B/I
PIN7 Batt+
PIN8 Batt+

---Battery Con_pin define---
PIN8 GND
PIN7 GND
PIN6 SMD
PIN5 SMC
PIN4 TS
PIN3 B/I
PIN2 Batt+
PIN1 Batt+

```

2013/10/02
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

Battery is 3-cell design.
B+=9V



	For KB9012 OTP	For KB9022 OTP
92°C		1.0V
56°C		2.0V
PR216		16.9K ohm

2014/01/02 update

For KB9022 sense 20mΩ	Active	Recovery
65W	70W, 0.73V	55.9W, 0.59V

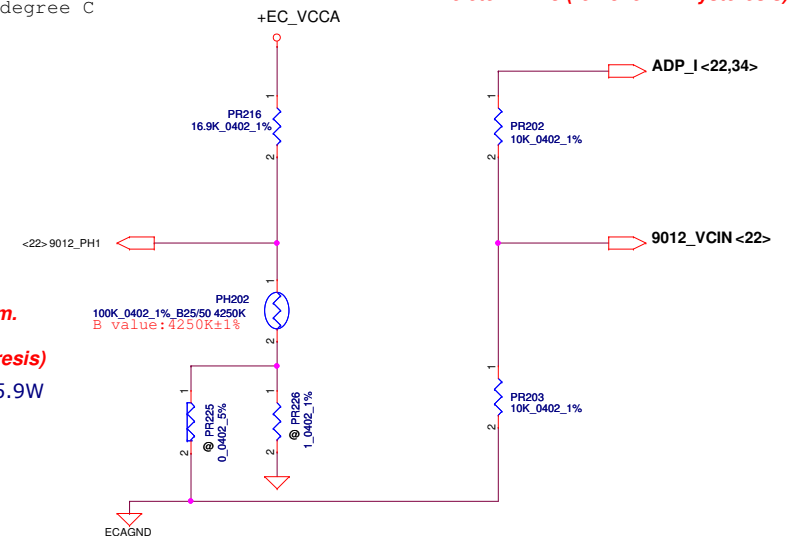
2013/10/22 Modify
PH201,PH202 change to common part.

2013/12/16 Modify
Delete PR223.(remove HW hysteresis)

PH201 under CPU botten side :
 CPU thermal protection at 92 degree C (shutdown)
 Recovery at 56 degree C

2013/10/25 Modify
PR227(9012@) change to 26.1K ohm.
2014/02/07 Modify
Delete @PR227.(remove HW hysteresis)

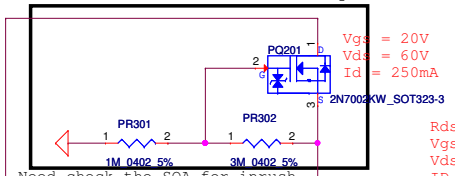
For 65W adapter==>action 70W , Recovery 55.9W



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				BATTERY CONN / OTP	
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Protection for reverse input

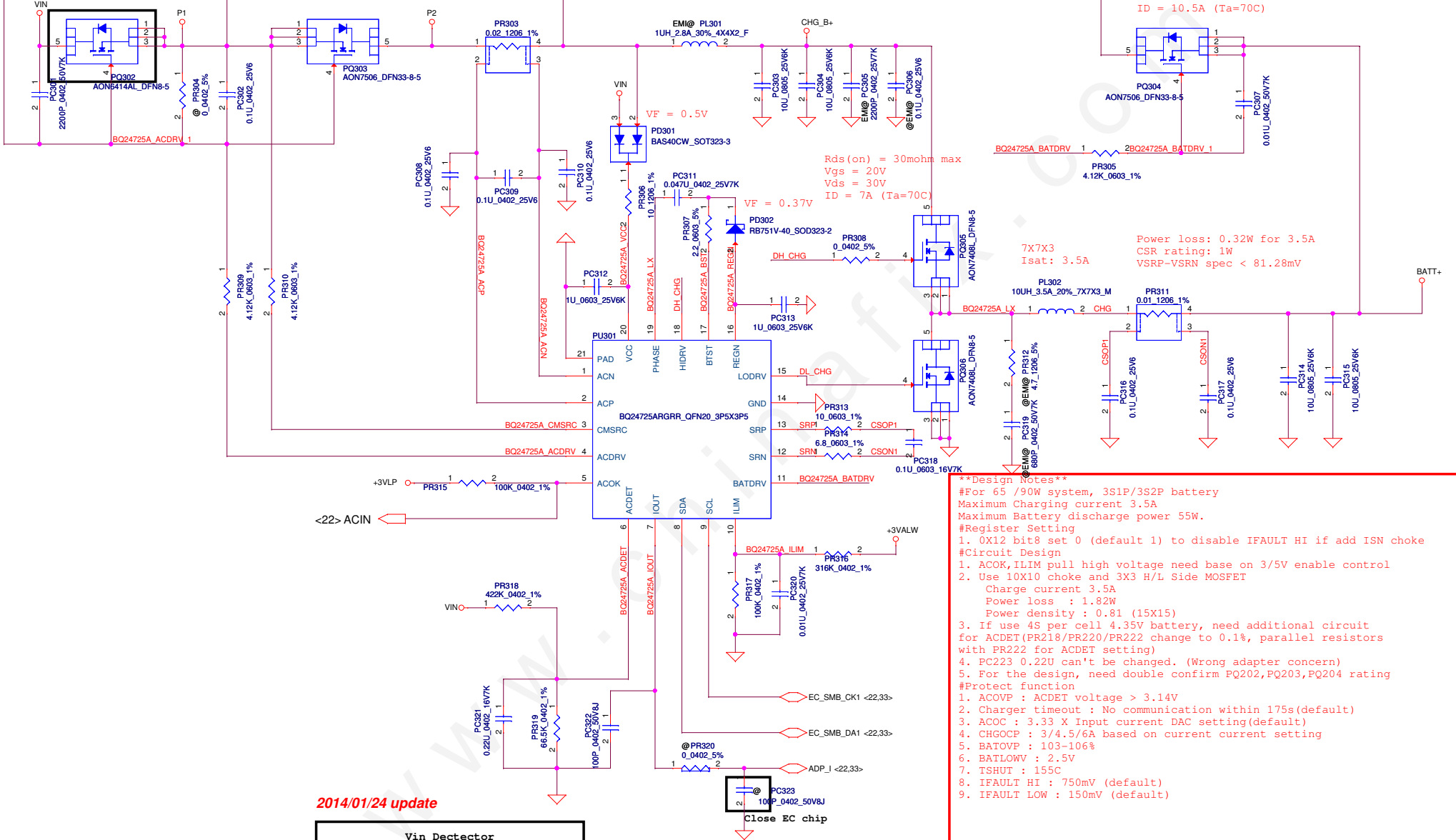


2013/10/14
PR303 10m ohm chang -->20m ohm
SD00000S120

Rds(on) = 15.8mohm max
Vgs = 20V
Vds = 30V
ID = 10.5A (Ta=70C)

2013/10/16 Modify
PQ305,PQ306 change to AON7408L.
2013/10/22 Modify
PL302 change to common part.
2013/11/29 Modify
PL301 change to common part.

Rds(on) = 15.8mohm max
Vgs = 20V
Vds = 30V
ID = 10.5A (Ta=70C)



****Design Notes****

#For 65 /90W system, 3S1P/3S2P battery
Maximum Charging current 3.5A
Maximum Battery discharge power 55W.

#Register Setting
1. 0X12 bit8 set 0 (default 1) to disable IFAULT HI if add ISN choke

#Circuit Design
1. ACOK,ILIM pull high voltage need base on 3/5V enable control
2. Use 10X10 choke and 3X3 H/L Side MOSFET
Charge current 3.5A
Power loss : 1.82W
Power density : 0.81 (15X15)

3. If use 4S per cell 4.35V battery, need additional circuit for ACDET (PR218/PR220/PR222 change to 0.1%, parallel resistors with PR222 for ACDET setting)

4. PC223 0.22U can't be changed. (Wrong adapter concern)

5. For the design, need double confirm PQ202,PQ203,PQ204 rating

#Protect function
1. ACOVP : ACDET voltage > 3.14V
2. Charger timeout : No communication within 175s(default)
3. ACOC : 3.33 X Input current DAC setting(default)
4. CHGOCP : 3/4.5/6A based on current current setting
5. BATOVP : 103-106%
6. BATLOWV : 2.5V
7. TSHUT : 155C
8. IFAULT HI : 750mV (default)
9. IFAULT LOW : 150mV (default)

2014/01/24 update

Vin Detector			
	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

VILIM = 20*ILIM*Rsr
ILIM = 3.3*100/(100+316)/20/0.01
= 3.966 A

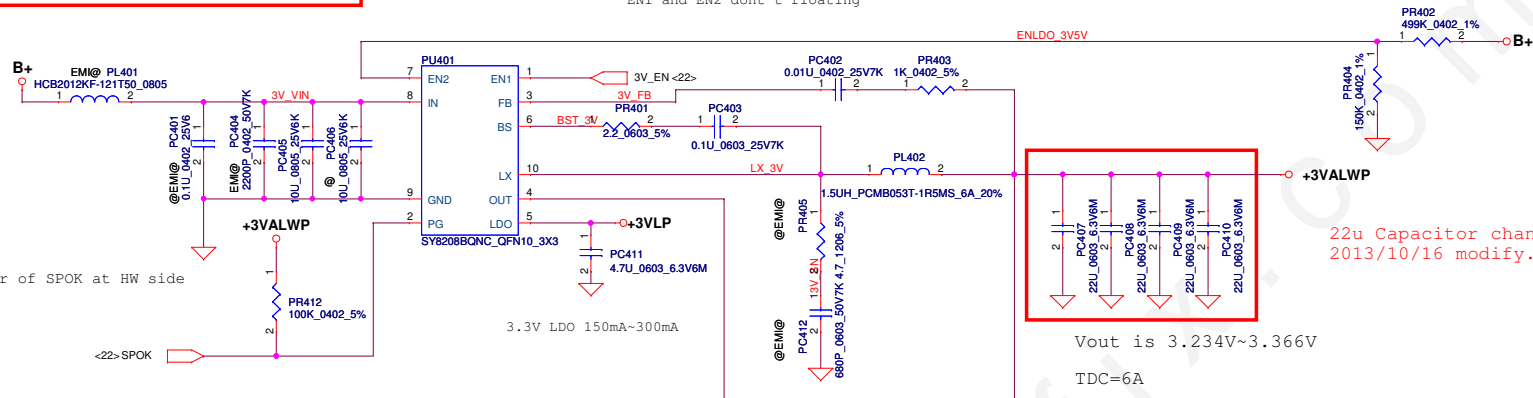
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Compal Electronics, Inc.			
CHARGER			
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Module model information

SY8208B_V2.mdd
SY8208C_V2.mdd

EN1 and EN2 dont't floating

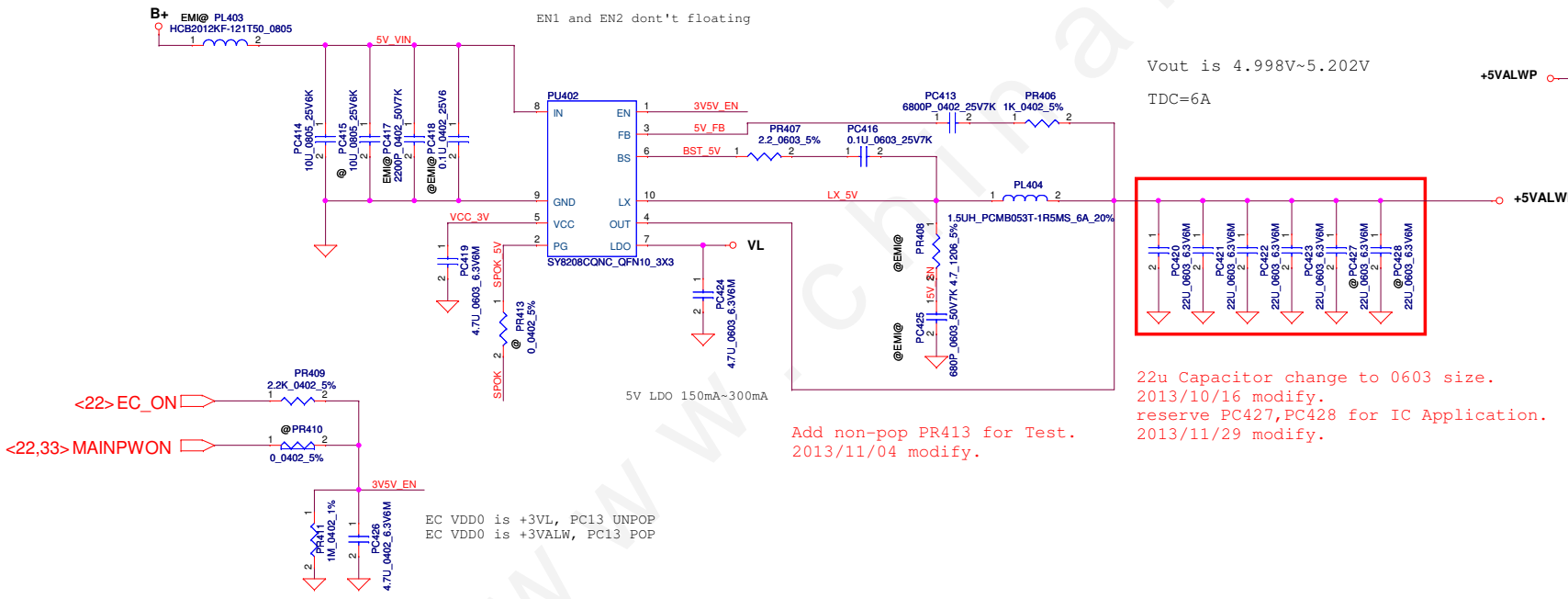


22u Capacitor change to 0603 size.
2013/10/16 modify.

Vout is 3.234V~3.366V
TDC=6A



EN1 and EN2 dont't floating



22u Capacitor change to 0603 size.
2013/10/16 modify.
reserve PC427, PC428 for IC Application.
2013/11/29 modify.

Add non-pop PR413 for Test.
2013/11/04 modify.

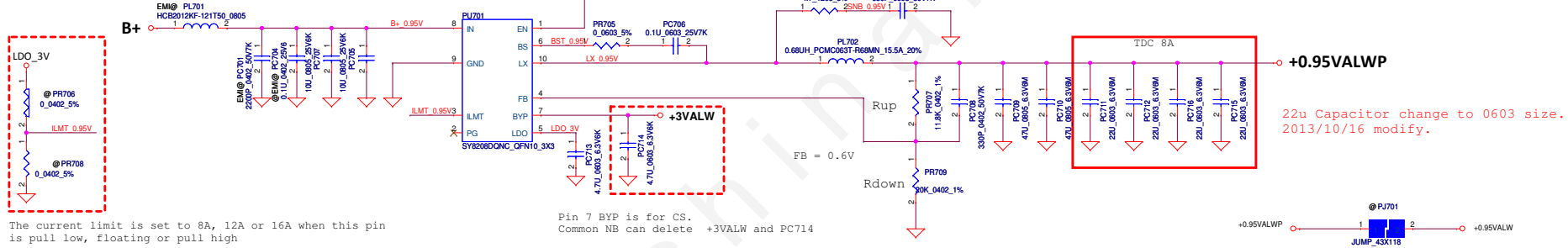
EC VDD0 is +3VL, PC13 UNPOP
EC VDD0 is +3VALW, PC13 POP

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				+3VALW/+5VALW
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Module model information
SY8208D_V1.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2

for this project
Ipeak=8A
Add 22u*2 capacitor,
Chock change to 0.68u.
meet DC-DC design check form.
2013/10/02 Modify.



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC714

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)
Vout=0.954V

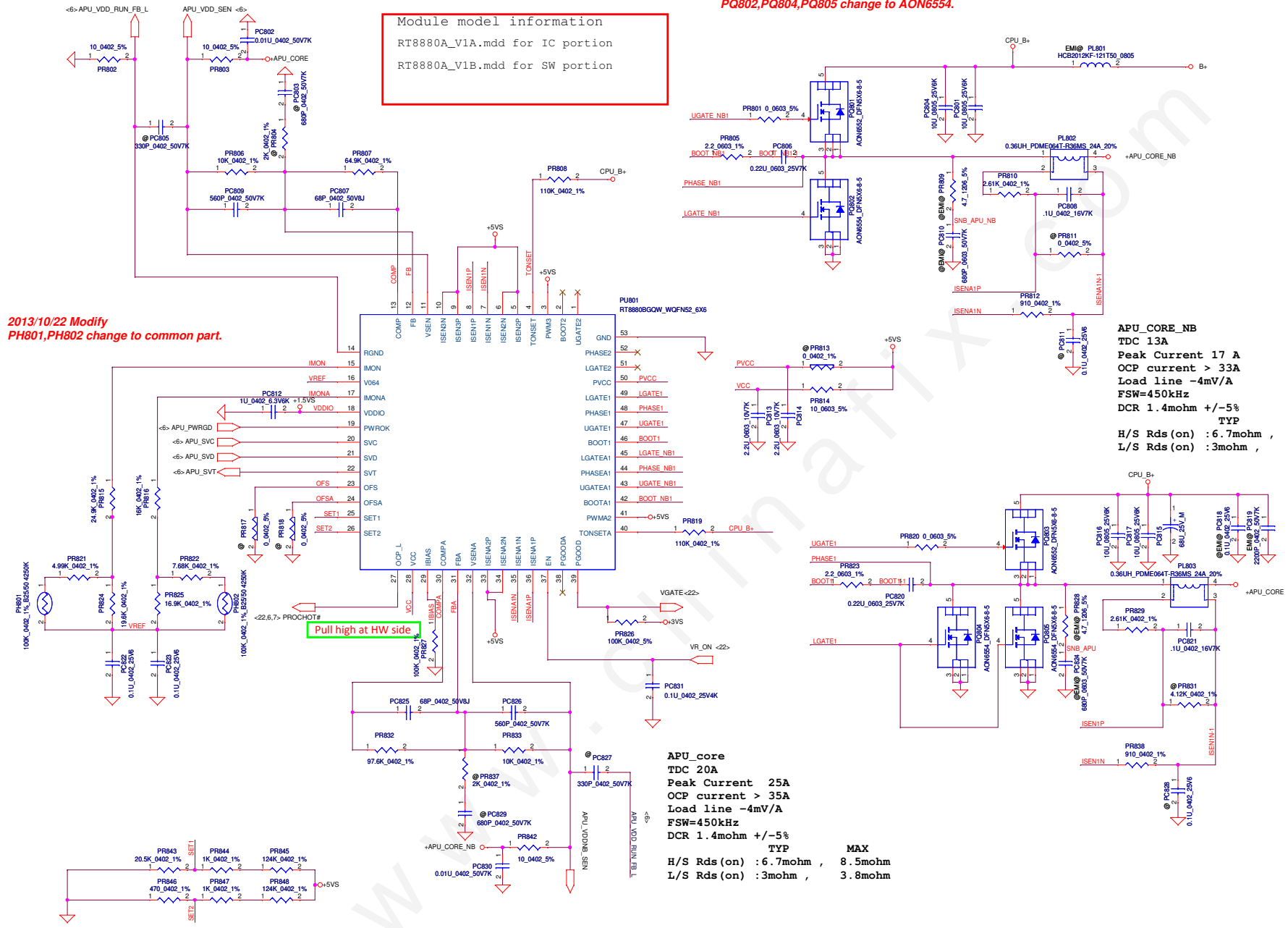
22u Capacitor change to 0603 size.
2013/10/16 modify.

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2013/10/16 Modify
 PQ801,PQ803 change to AON6552.
 PQ802,PQ804,PQ805 change to AON6554.

Module model information
 RT8880A_V1A.mdd for IC portion
 RT8880A_V1B.mdd for SW portion



2013/10/22 Modify
 PH801,PH802 change to common part.

Pull high at HW side

APU_CORE_NB
 TDC 13A
 Peak Current 17 A
 OCP current > 33A
 Load line -4mV/A
 FSW=450kHz
 DCR 1.4mohm +/-5%
 H/S Rds (on) : 6.7mohm , 8.5mohm
 L/S Rds (on) : 3mohm , 3.8mohm

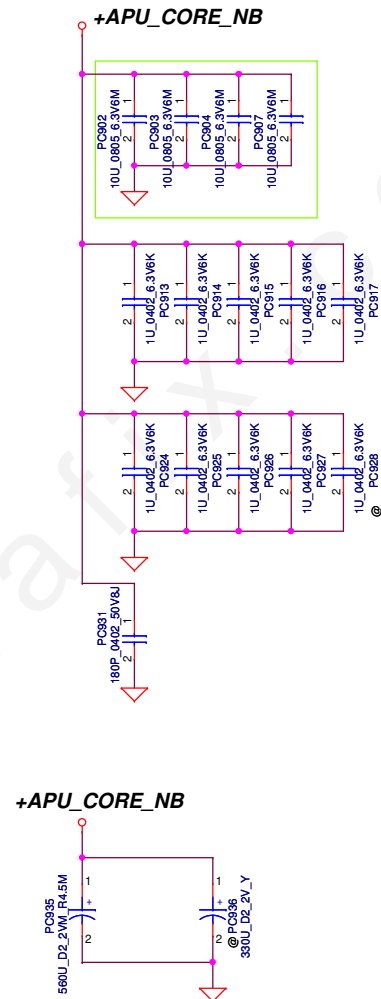
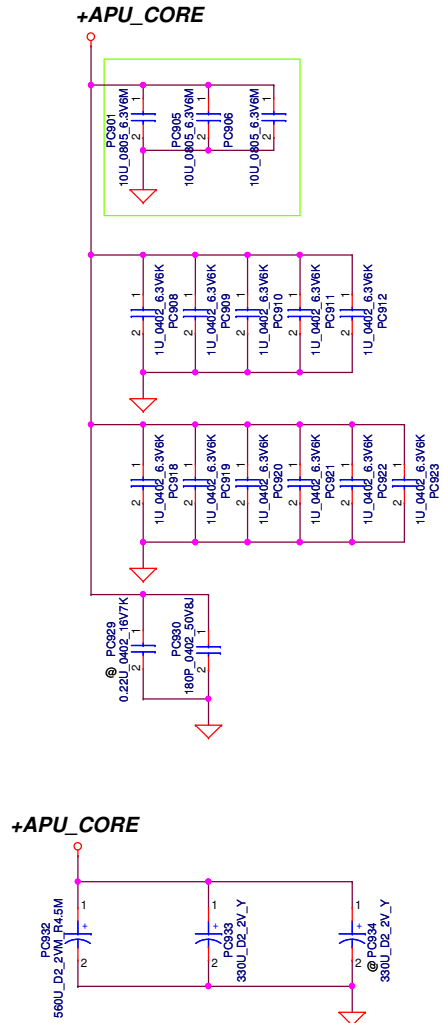
APU_core
 TDC 20A
 Peak Current 25A
 OCP current > 35A
 Load line -4mV/A
 FSW=450kHz
 DCR 1.4mohm +/-5%
 H/S Rds (on) : 6.7mohm , 8.5mohm
 L/S Rds (on) : 3mohm , 3.8mohm

Delete PR834.PR835.PR836.PR839.PR840.PR841,
 follow vender FAE suggest.
 2013/11/29 modify.

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+APU_CORE (36.4)

+APU_CORE_NB (36.5)



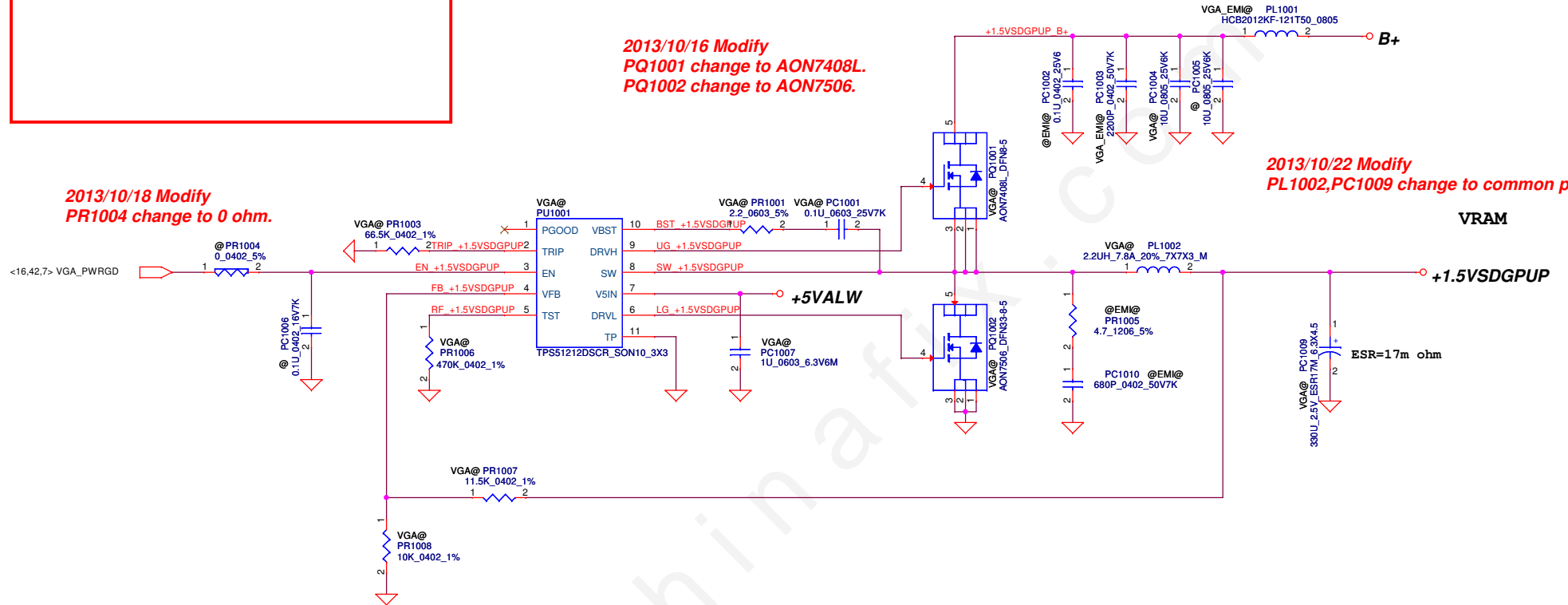
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Module model information
 TPS51212_V1.mdd for Single layer
 TPS51212_V2.mdd for Dual layer

2013/10/16 Modify
 PQ1001 change to AON7408L.
 PQ1002 change to AON7506.

2013/10/22 Modify
 PL1002, PC1009 change to common part.

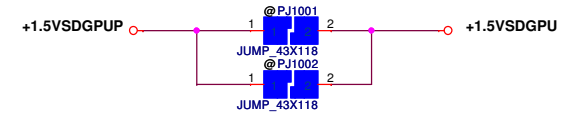
2013/10/18 Modify
 PR1004 change to 0 ohm.



MOSFET: 3x3 DFN
 H/S Rds (on): 27mohm (Typ), 34mohm (Max)
 Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds (on): 13mohm (Typ), 15.8mohm (Max)
 Idsm: 12A@Ta=25C, 10.5A@Ta=70C

Choke: 7x7x3
 Rdc=15.5mohm +/-15%



Vout	PR1007	PR1008	PR1003
+1.2V	7.15K	10k	105K
+1.05V	4.99k	10k	93.1k
+1.5V	11.5K	10k	105K

+1.5V(for this project)

Switching Frequency: 290kHz
 Ipeak=4.7A
 OCP: 6.884A~5.751A
 OVP: 120%~130%
 VFB=0.704V, Vout=1.514V
 PR1003=66.5K Ohm

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2013/10/16 Modify
 PQ1201,PQ1203 change to AON6552.
 PQ1202,PQ1204 change to AON6554.

GPIO21	GPIO29	GPIO30	GPIO20	GPIO15	VDDC
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

GPU	AMD MARS series				AMD SUN series			Description
	MARS XTX	MARS XT	MARS PRO	MARS LP	SUN UL	SUN PRO	SUN XT	
VDDC	0.775-1.175V	0.775-1.125V	0.775-1.050V	0.775-1.000V	0.775-1.125V	0.800-1.075V	0.800-1.150V	NA
TDC	32A (TDC)	25A (TDC)	21A (TDC)	17A (TDC)	16A (TDC)	19A (TDC)	25A (TDC)	NA
EDC	48A	37.5A	31.5A	26A	24A	28.5A	37.5A	NA
OCP	57.6A	45A	37.8A	31.2A	28.8A	34.2A	45A	NA
Vboot	0.85V	0.85V	0.85V	0.85V	0.9V	0.9V	0.9V	NA
Load line	1mohm	1mohm	1mohm	-----	-----	-----	1mohm	NA
RI	1.13K Ohm	887 Ohm	750 Ohm	-----	-----	-----	887 Ohm	for OCP and LoadLine Setting
Rdroop	1.43K Ohm	1.13K Ohm	953 Ohm	-----	-----	-----	1.13K Ohm	for LoadLine Setting
PR1229	187K Ohm	147K Ohm	124K Ohm	-----	-----	-----	147K Ohm	for Compensation
PR1233	51.1K Ohm	51.1K Ohm	51.1K Ohm	-----	-----	-----	51.1K Ohm	for Positive offset

MOS TYP MAX
 H/S Rds(on) :6.7mohm , 8.5mohm
 L/S Rds(on) :3mohm , 3.8mohm
 Choke: 0.22uH (Size:7*7*4)
 Rdc=0.98mohm +5%
 Heat Rating Current=28A
 Saturation Current=28A

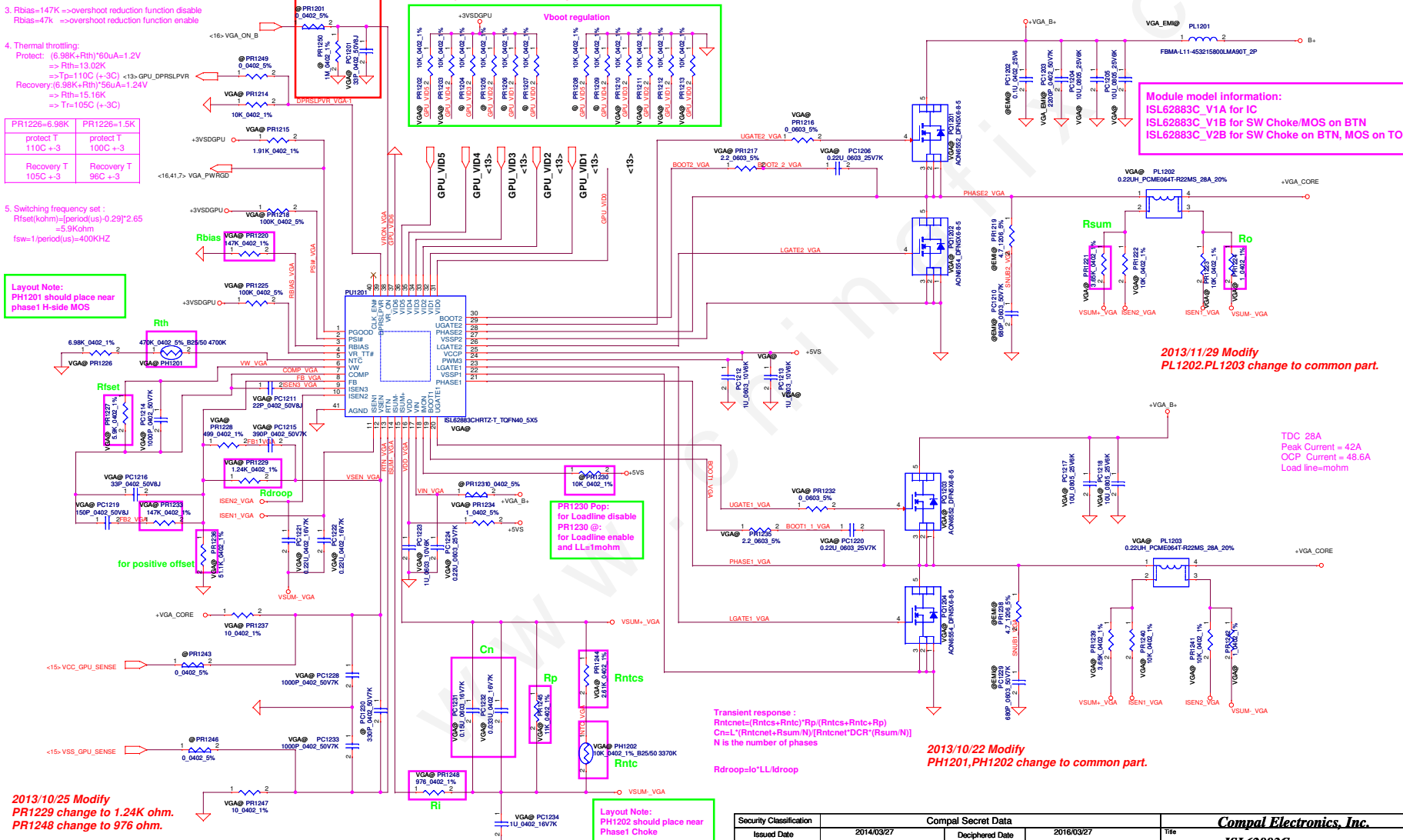
Remark:
 1. PWM3 (Pin24) tie to 5V & CLK# (Pin40) external pull high
 => 2 phase GPU VR config
 PWM3 (Pin24) tie to 5V & CLK# (Pin40) to GND or floating
 => 2 phase GPU VR config

2. When 2 Phase GPU config
 a. DPSPVVR (Pin39)=0 PS# (Pin2)=0
 => 1 phase CCM operation mode
 b. DPSPVVR (Pin39)=0 PS# (Pin2)=1
 => 2 phase CCM operation mode
 c. DPSPVVR (Pin39)=1 PS# (Pin2)=0 or 1
 => 1 phase DE operation mode

2013/10/18 Modify
 EN Signal change to VGA_ON.
 Delay Time follow HW request.

2013/11/29 Modify
 Delay Time follow HW request.
 Add PD Resistor(PR1250)
 2013/12/16 Modify
 Delay Time follow HW request.

Remark: MARS LP/ SUN UL/ SUN PRO
 don't use this 2-phase solution



Module model information:
 ISL62883C_V1A for IC
 ISL62883C_V1B for SW Choke/MOS on BTN
 ISL62883C_V2B for SW Choke on BTN, MOS on TOP

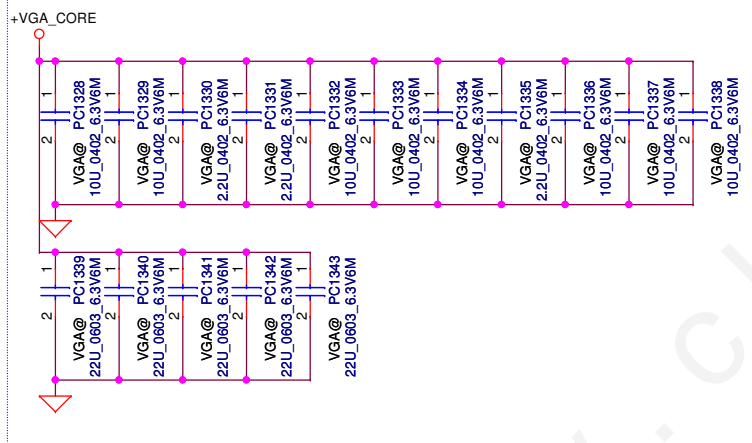
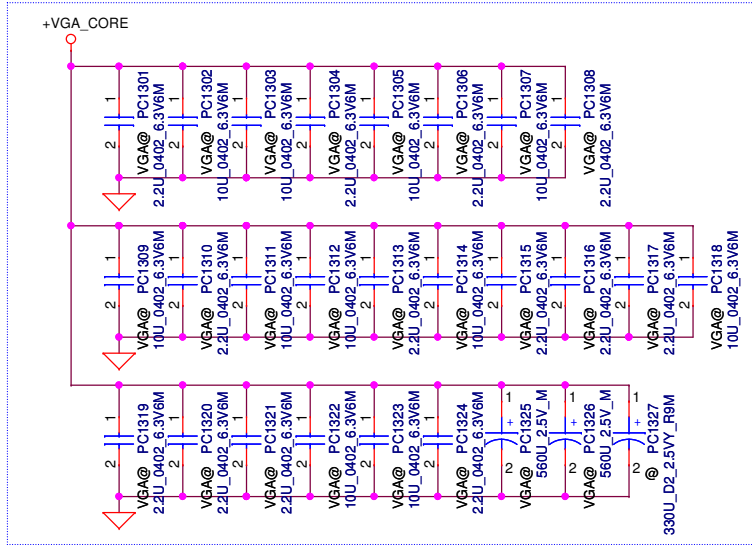
2013/11/29 Modify
 PL1202,PL1203 change to common part.

TDC 28A
 Peak Current = 42A
 OCP Current = 48.6A
 Load Line=1mohm

2013/10/22 Modify
 PH1201,PH1202 change to common part.

2013/10/25 Modify
 PR1229 change to 1.24K ohm.
 PR1248 change to 976 ohm.

Transient response :
 $R_{ntcns} = (R_{ntcs} + R_{ntc}) * R_p / (R_{ntcs} + R_{ntc} + R_p)$
 $C_{ns} = L * (R_{ntcns} + R_{sum} / N) / [R_{ntcns} * DCR * (R_{sum} / N)]$
 N is the number of phases
 $R_{droop} = L * I_{droop}$



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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	
1	Design Change.	Design Change of Diode Application.	0.2	32	Change PD101 to SCS4004010(S SCH DIO BAS40-04 SOT23).	2013/11/29	DVT
2	Design Change.	Design Change of IC Application.	0.2	35	Add non-pop component PC427,PC428.	2013/11/29	DVT
3	Design Change.	reduce part count.	0.2	37	Delete PR605 PD resister.	2013/11/29	DVT
4	Design Change.	reduce part count.	0.2	39	Delete @PR834.@PR835.@PR836.@PR839.@PR840.@PR841.	2013/11/29	DVT
5	Design Change.	Design Change of VGA Type Application.	0.2	42	PR1205 change to non-pop. PR1211 change to pop.	2013/11/29	DVT
6	Design Change.	Design Change of common part.	0.2	34	Change PL301 to SH00000YG00 (S COIL 1UH +-30% 2.8A 4X4X2 FERRITE).	2013/11/29	DVT
7	Design Change.	Design Change of common part.	0.2	42	Change PL1202.PL1203 to SH000011H00 (S COIL .22UH +-20% 24A 7X7X4 MOLDING).	2013/11/29	DVT
8	Design Change.	Design Change of Delay Time.	0.2	42	Change PR1201 to SD028000080(S RES 1/16W 0 +-5% 0402). Change PC1201 to non-pop.	2013/11/29	DVT
9	Design Change.	Design Change of EC Type Application.	0.2	35	Add PD401 SCS00000200(S SCH DIO RB751V-40 SOD-323).	2013/11/29	DVT
10	Design Change.	Design Change of Circuit Application.	0.2	42	Add PR1250 SD034100480(S RES 1/16W 1M +-1% 0402).	2013/11/29	DVT
11	Design Change.	Design Change of Delay Time.	0.2	42	Change PR1201 to SD028000080(S RES 1/16W 0 +-5% 0402). Change PC1201 to SE071330J80(S CER CAP 33P 50V J NPO 0402)	2013/12/16	DVT
12	Design Change.	Design Change of Circuit Application.	0.2	33	Delete PR223.(remove HW hysteresis)	2013/12/16	DVT
13	Design Change.	Design Change of Circuit Application.	0.2	42	Change PR1250 to non-pop.	2013/12/16	DVT
14	Design Change.	Design Change of Circuit Application.	0.2	34	Change PQ303,PQ304 to SB000010A00(S TR AON7506 1N DFN).	2013/12/19	DVT
15	Design Change.	Design Change of Circuit Application.	0.2	33	Add PL202 SM01000C000 (S SUPPRE_ TAI-TECH HCB2012KF-121T50 0805)	2013/12/19	DVT

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Version change list (P.I.R. List)



Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
16	Design Change.	Design Change of Circuit Application.	0.2	33	Change PR211 to SD028000080(S RES 1/16W 0 +-5% 0402).	2013/12/25	DVT
17	Design Change.	Design Change of Circuit Application.	0.2	35	Change PC426 to pop.	2013/12/25	DVT
18	Design Change.	Design Change of Circuit Application.	0.2	33	Change PR216 to SD034162280(S RES 1/16W 16.2K +1% 0402).	2013/12/25	DVT
19	Design Change.	Design Change of Circuit Application.	0.2	33	Change PR216 to SD034169280(S RES 1/16W 16.9K +-1% 0402).	2014/01/02	DVT
20	Design Change.	Design Change of Circuit Application.	0.2	33	Change PR202 to SD034100280(S RES 1/16W 10K +-1% 0402).	2014/01/02	DVT
21	Design Change.	Design Change of Circuit Application.	0.3	37.38. 39.41.	Change PR813,PR601,PR706,PR702,PR1004 to SD028000080(S RES 1/16W 0 +-5% 0402).	2014/02/07	PVT
22	Design Change.	Design Change of Circuit Application.	0.3	35	Remove PD401. Add @PR410 SD028000080(S RES 1/16W 0 +-5% 0402).	2014/02/07	PVT

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