

AMD KABINI EA/EG-40/50  
PX /UMA Schematics Document  
AMD FT3 APU  
AMD GPU SUN XT M2/64bit

EAE50 KB UMA

緯創資通 **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Cover Page**

Size

A4

Document Number

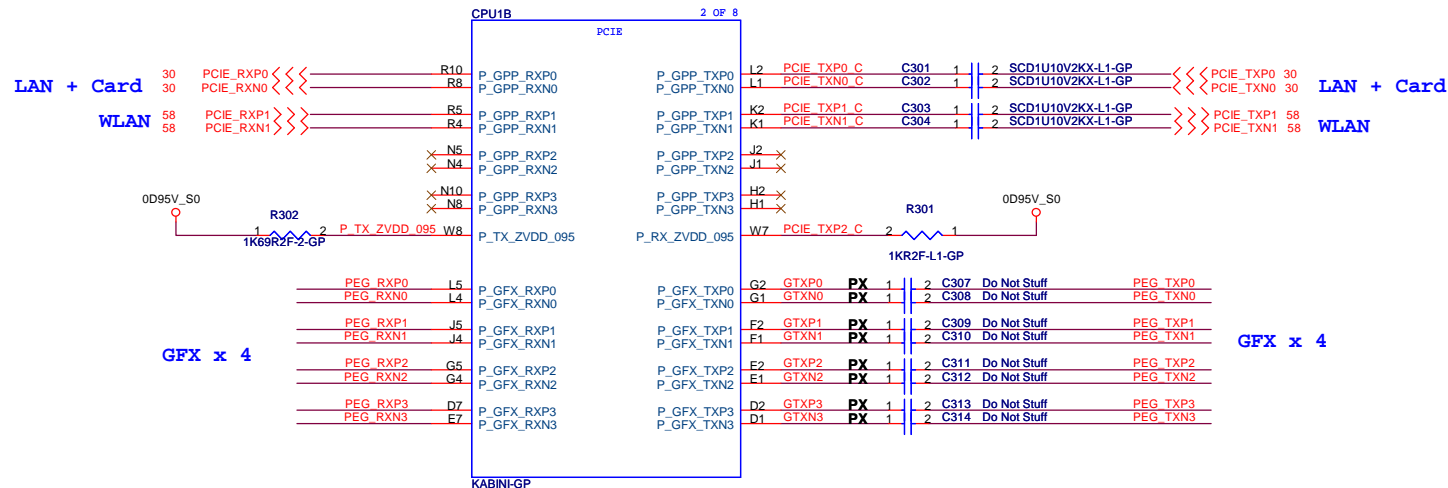
**KABINI**

Rev

Date: Wednesday, October 24, 2012

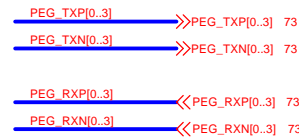
Sheet 1 of 102





### PCIE Table

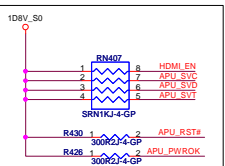
0	LAN + Card
1	WLAN
2	NC
3	NC



71.KABIN.B0U IC CPU Kabini 4110 1.5GHz 15W4C FT3 ES2 BGA  
 71.KABIN.C0U IC CPU Kabini 5110 2.0GHz 25W4C FT3 ES2 BGA

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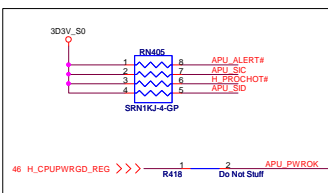
<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>CPU PCIE</b>	
Title <b>CPU PCIE</b>	Rev 1
Size A3	Document Number <b>KABINI</b>
Date: Monday, February 04, 2013	Sheet 3 of 102



20120821 Follow Larne

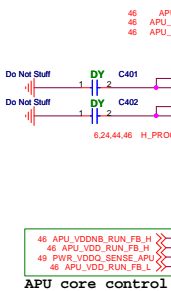
TABLE 6. PRE-PWROK METAL VID CODES

SVC	SVD	OUTPUT VOLTAGE (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

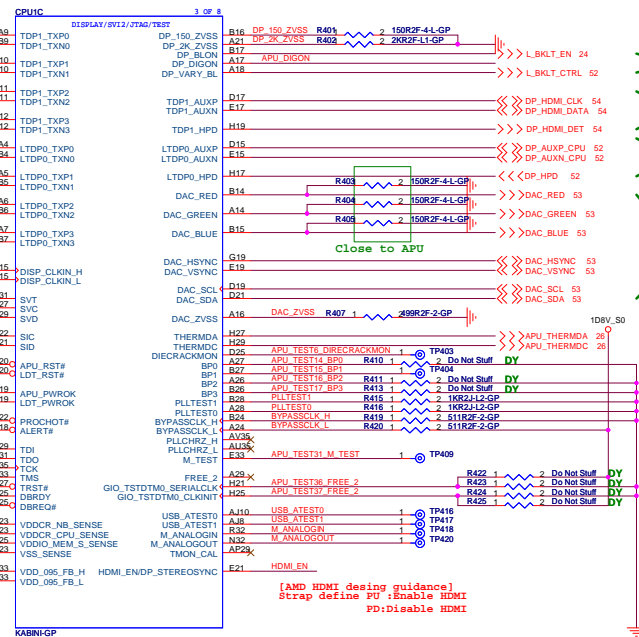
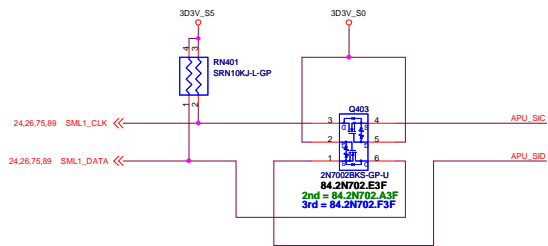


20120820 Follow Larne

APU HDMI  
APU EDP

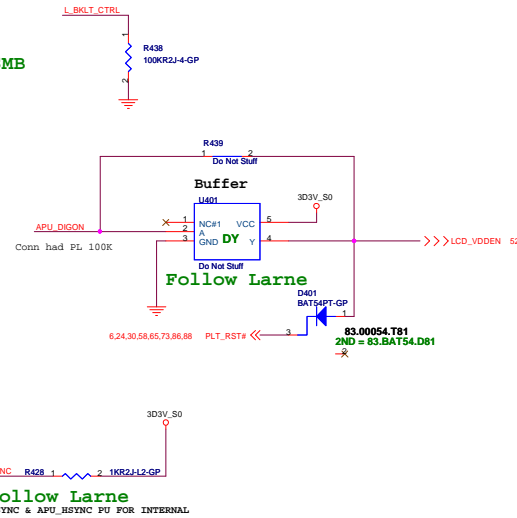


APU core control



[AMD HDMI desing guidance]  
Strap define FU : Enable HDMI  
PD:Disable HDMI

APU EDP  
APU HDMI SMB  
APU EDP  
APU CRT



Follow Larne

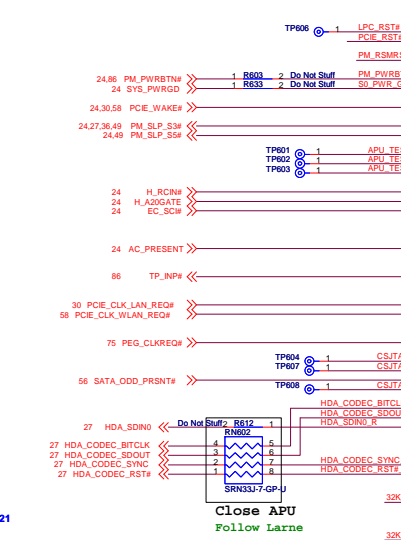
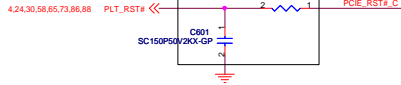
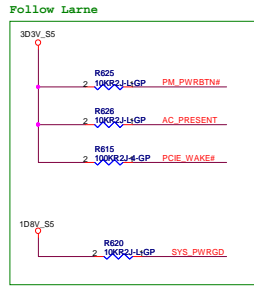
DP\_STEREO SYNC & APU\_HRTWC PU FOR INTERNAL

EAEG50 KB UIMA

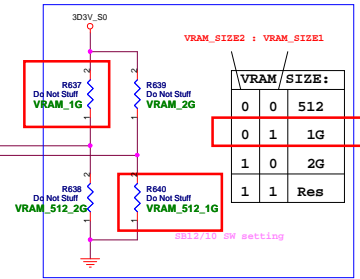


Pass Word Clear

Follow Larne

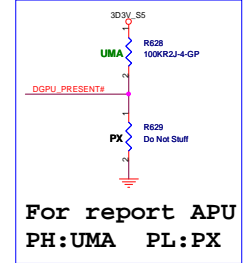
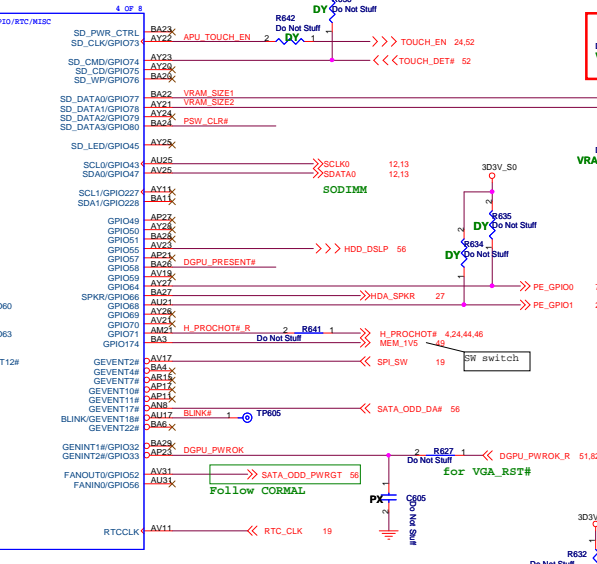
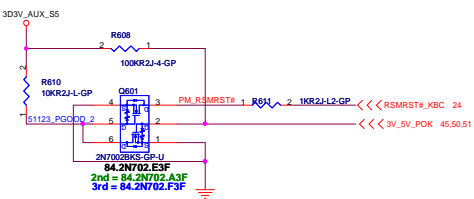
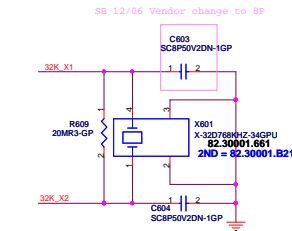


Close APU  
Follow Larne



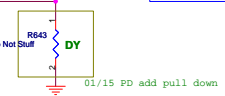
VRAM / SIZE:		
0	0	512
0	1	1G
1	0	2G
1	1	Res

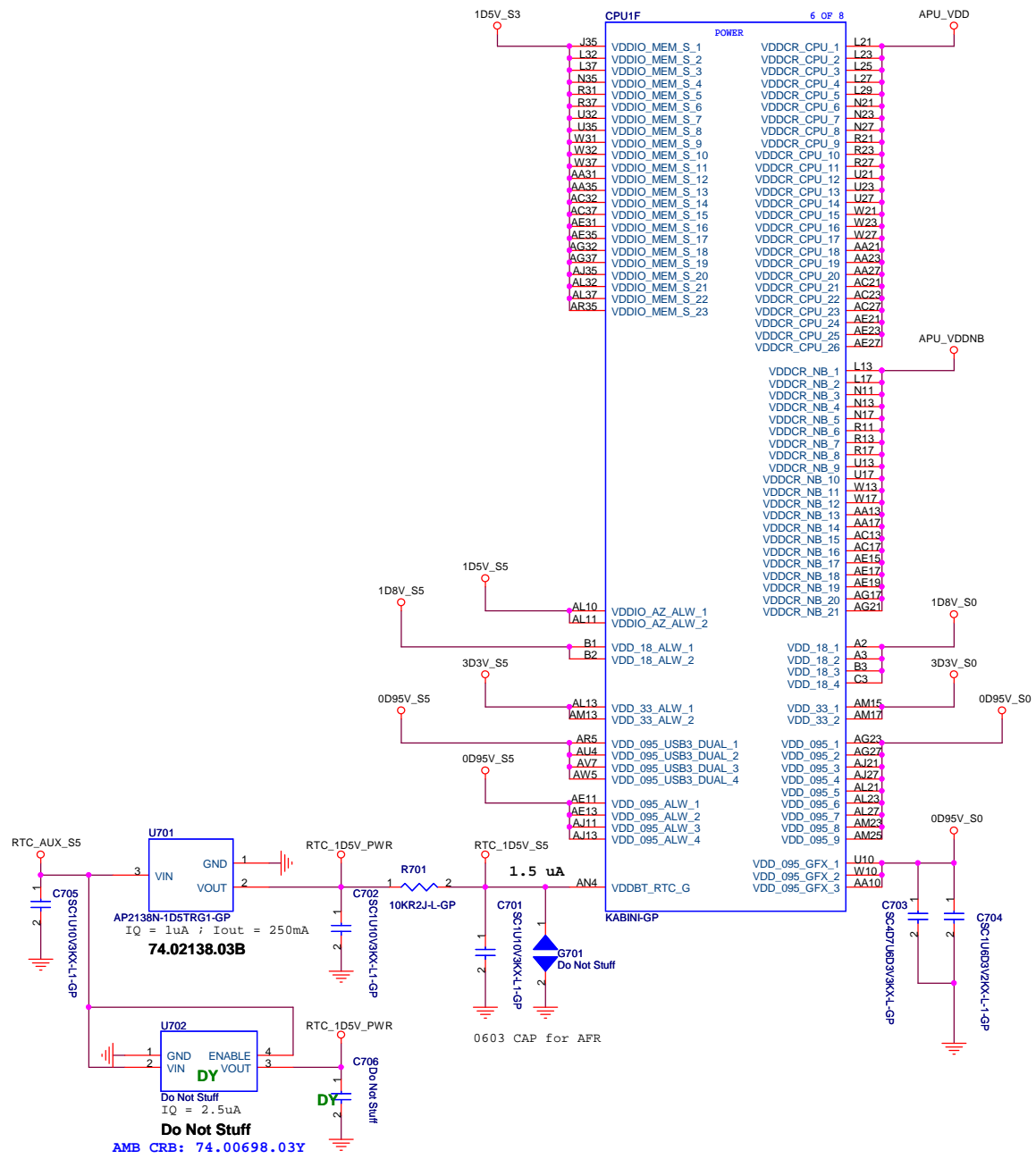
SUN only 4 bank for 1G



For report APU  
PH:UMA PL:PX

HW setting MEM\_IV5 H = 1.5V  
L = 1.35V

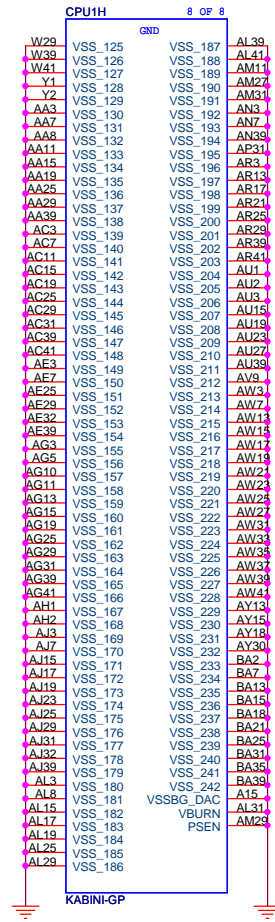
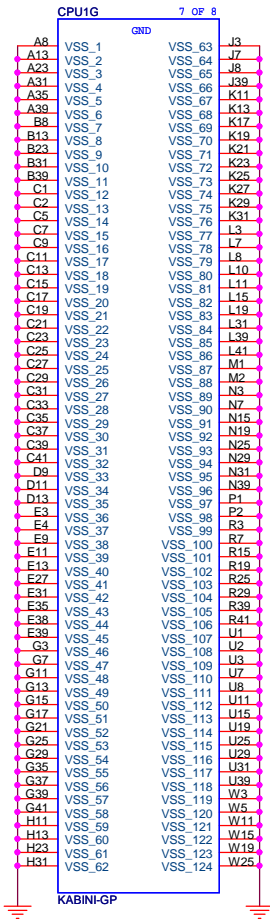




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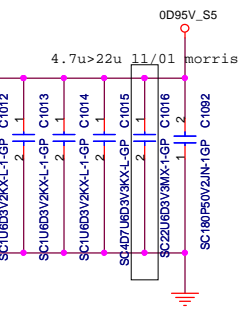
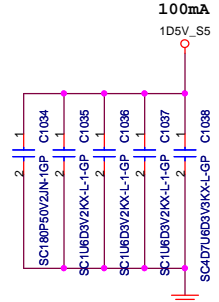
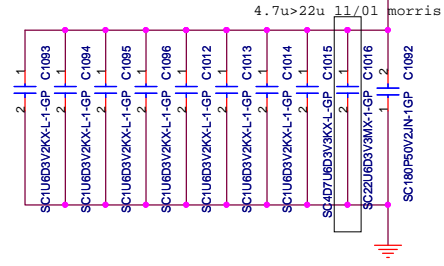
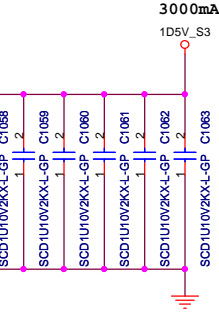
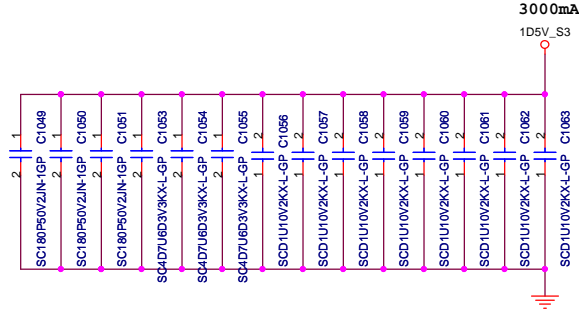
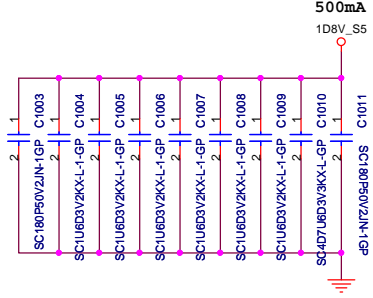
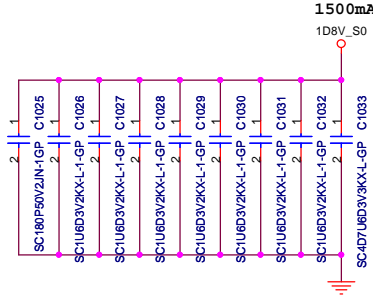
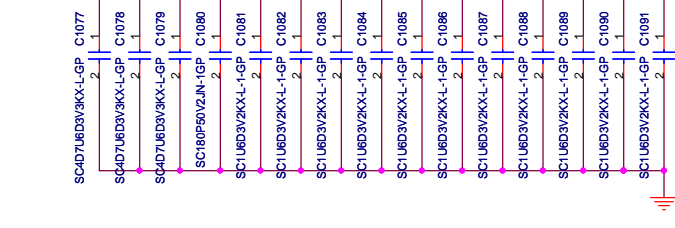
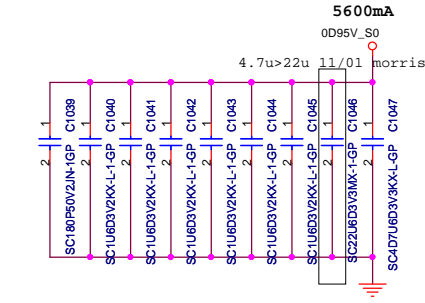
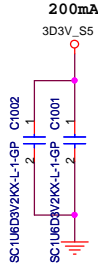
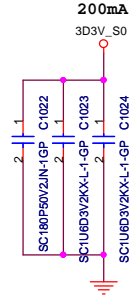
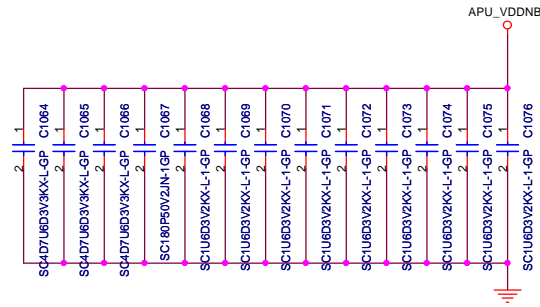
Title <b>CPU VCC CORE</b>		
Size A3	Document Number <b>KABINI</b>	Rev
Date: Tuesday, January 15, 2013	Sheet 7	of 102



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<b>CPU VSS</b>		
Title		
Size	Document Number	Rev
A3	<b>KABINI</b>	
Date:	Wednesday, November 28, 2012	Sheet 9 of 102



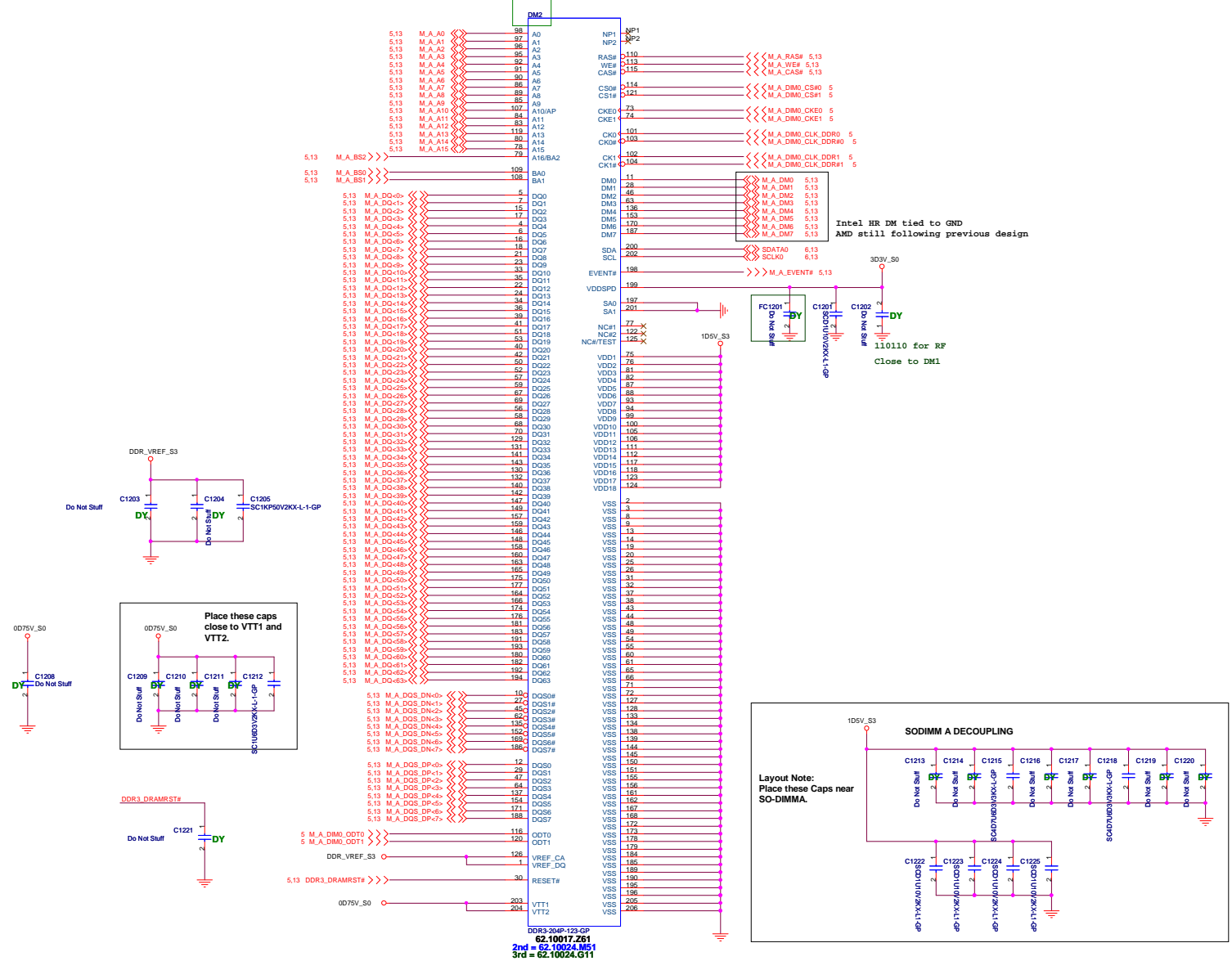


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Title		
CPU POWER CAP1		
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01/14 PD change location name for factory issue



Follow JE50-SB  
H = 4mm

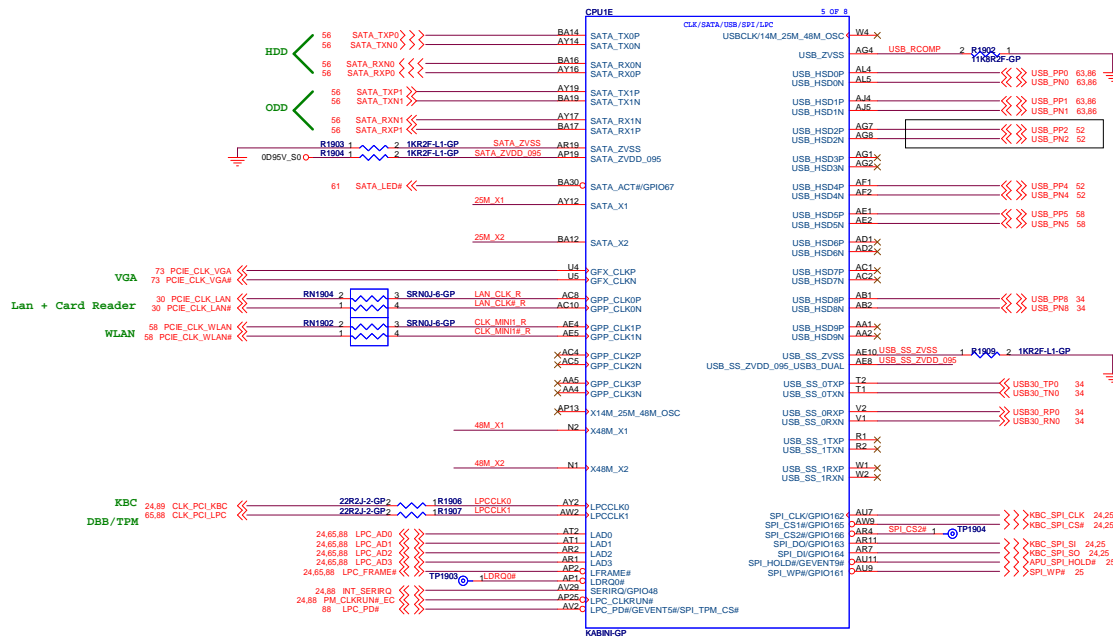
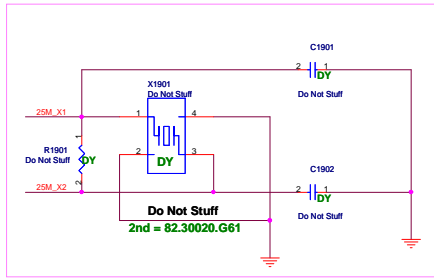
01/15 PD remove 62.10017.X31 for factory issue



### SATA Table

0	HDD
1	ODD

SB 11/27 25M XTAL Reserved for AMD

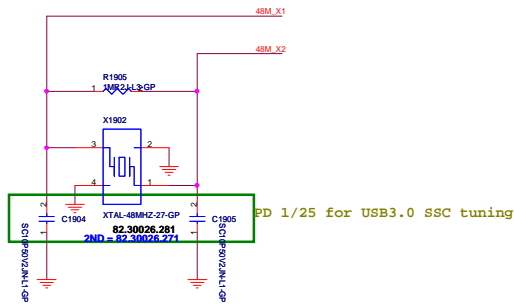
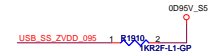


### USB Table

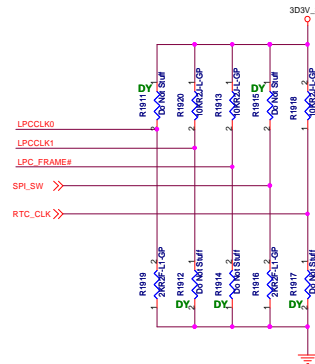
Pair	Device
0	USB2.0 Debug (DB Conn)
1	USB2.0 (DB Conn)
2	Touch Panel
3	
4	CCD (CCD Conn)
5	WLAN + BT (Mini PCI-E)
6	
7	
0/8	USB3.0 & USB 2.0 Charger (MB)
1/9	

### Xtal Table

0	System & USB	CLK
1	RTC	32.768K
2	SATA	25M
3	LAN	25M
4	VGA	27M



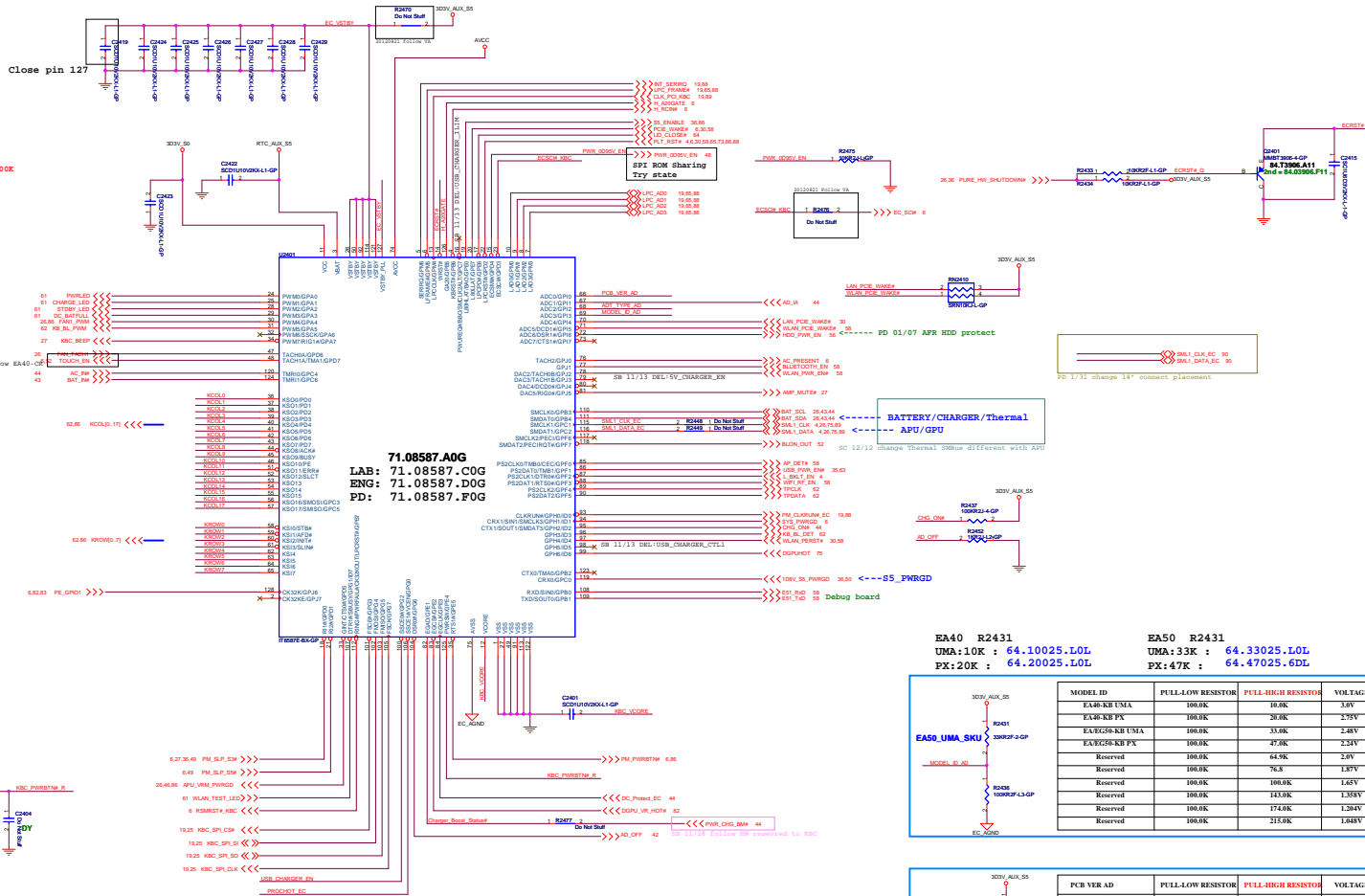
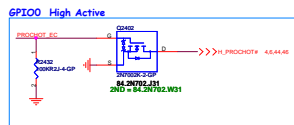
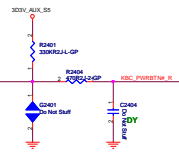
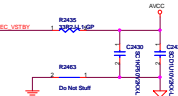
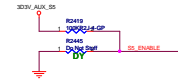
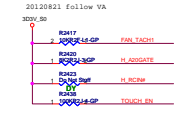
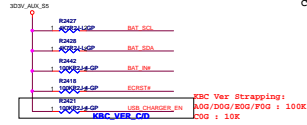
### SYSTEM STRAPPINGS



	LPC_CLK0	LPC_CLK1	LFRAME#	EXPCARD_POE_FWRN#	RTC_CLK
FULL	BOOT FAIL TIMER ENABLED	CLGEN ENABLED	SPI ROM	1.0V SPI ROM (DEFAULT)	NORMAL POWR UP/RESET TIMING (DEFAULT)
HIGH		INACTV#	INACTV#		
FULL	BOOT FAIL TIMER DISABLED	CLGEN DISABLED	LPC ROM	3.3V SPI ROM	FAST POWER UP/RESET TIMING FOR SIMULATION
LOW	(DEFAULT)				

EA650 KB UIM

SSID = KBC



EA40 R2431  
UMA:10K : 64.10025.L0L  
PX:20K : 64.20025.L0L

EA50 R2431  
UMA:33K : 64.33025.L0L  
PX:47K : 64.47025.6DL

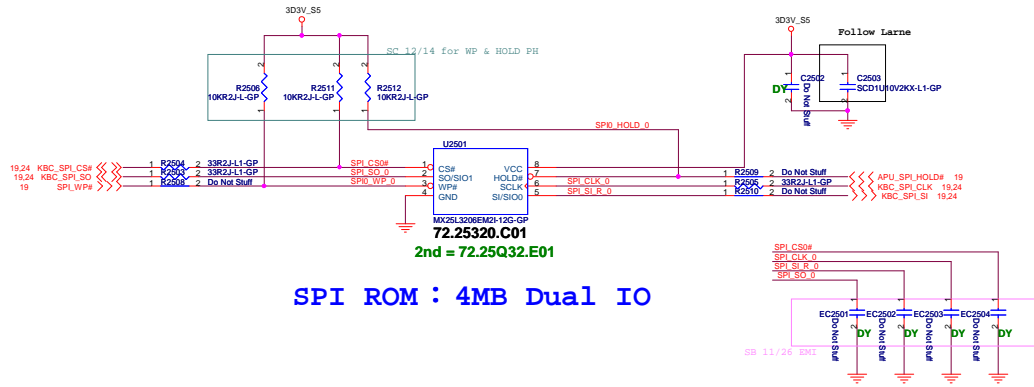
MODEL ID	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
E44E-KB UMA	100.0K	10.0K	2.50V
E44E-KB PX	100.0K	20.0K	2.95V
E44E54-KB UMA	100.0K	33.0K	2.40V
E44E54-KB PX	100.0K	47.0K	2.50V
Reserved	100.0K	64.9K	2.8V
Reserved	100.0K	76.3	1.80V
Reserved	100.0K	100.0K	1.40V
Reserved	100.0K	143.0K	1.55V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

PCB VER AD	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.95V
SC	100.0K	33.0K	2.40V
-1	100.0K	47.0K	2.50V
Reserved	100.0K	64.9K	2.8V
Reserved	100.0K	76.3	1.80V
Reserved	100.0K	100.0K	1.40V
Reserved	100.0K	143.0K	1.55V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

ADT_TYPE_AD	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
65W	N/A	100.0K	3.3V
60W	100.0K	N/A	0V
30W	10.0K	100.0K	0.3V
40W	20.0K	100.0K	0.55V
120W	33.0K	100.0K	0.81V

**SSID = Flash.ROM** SPI FLASH ROM (4M byte) for KBC

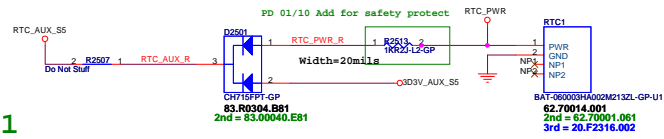
PD 1/28 SPI ROM : 4MB Dual IO  
 1st. MXIC : 72.25320.C01  
 2nd. WINBOND : 72.25Q32.E01  
 (手置件)請PCC移至DIP件



SPI ROM : 4MB Dual IO

**SSID = RBAT**

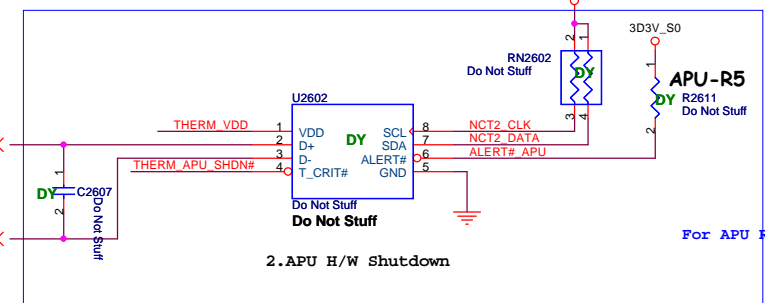
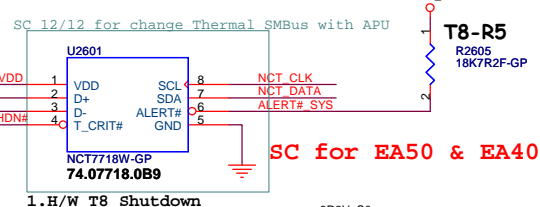
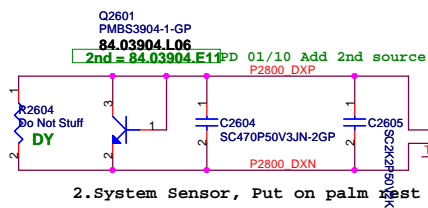
CR2032額外備料:  
 1.KTS: 23.20068.001  
 2.DBV: 23.22065.001



**SSID = Thermal**

# Thermal sensor NCT 7718W

Layout notice :  
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

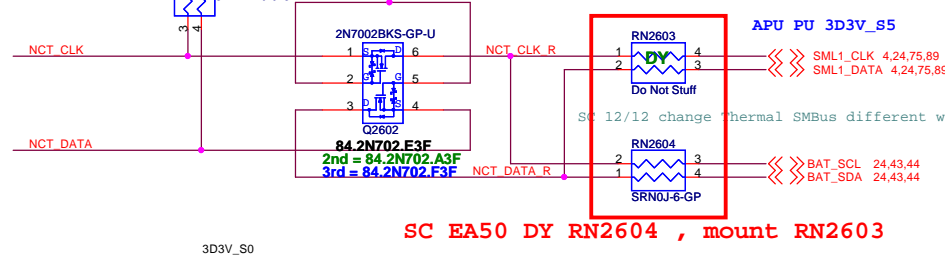


ALERT# /T CRIT#  
Pull-up Resistor

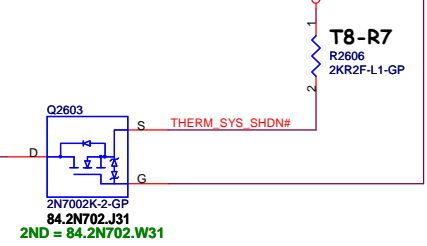
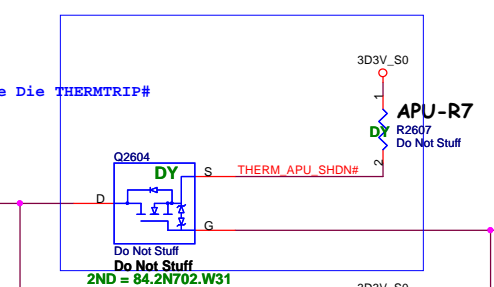
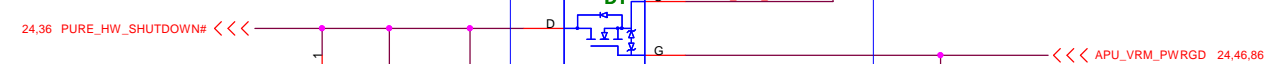
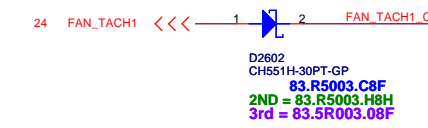
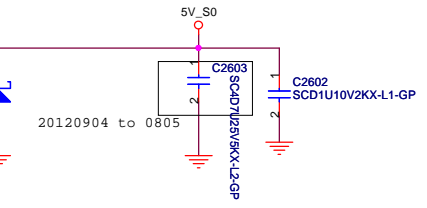
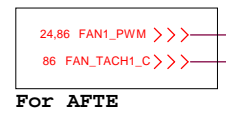
R5	R7				
	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

T\_CRIT temperature strapping point

T8=85 degree  
SYS=85 degree  
APU=125 degree



SC EA50 DY RN2604 , mount RN2603



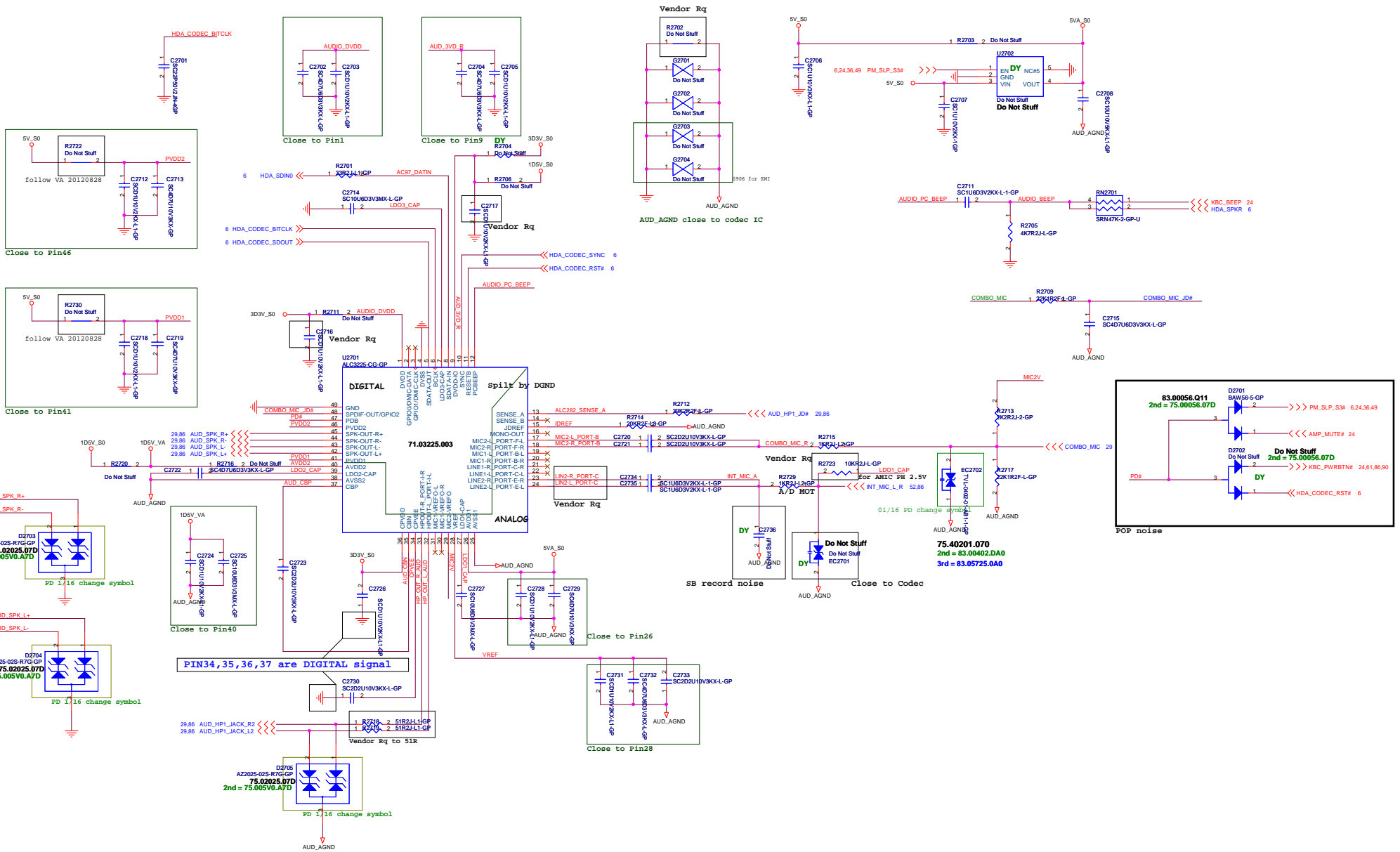
EAEG50 KB UMA

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Title: **Thermal 7718/Fan Controller P2793**

Size: Project Name: **KABINI** Rev: **SA**

Date: Monday, February 04, 2013 Sheet 26 of 102

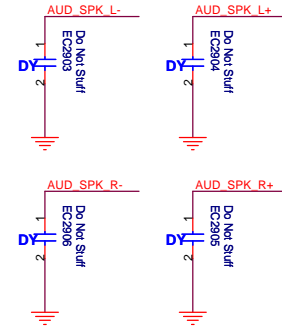
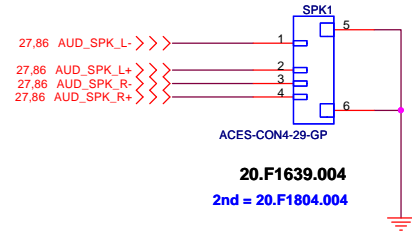




**SSID = AUDIO**

### Speaker

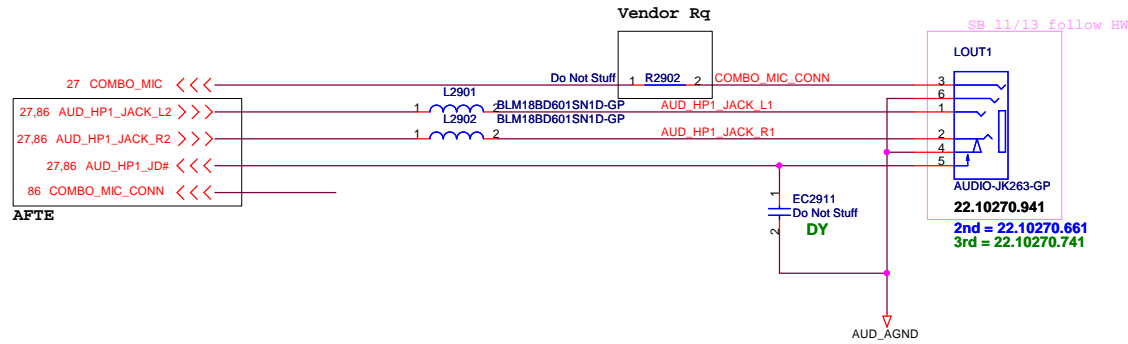
2W 4ohm X 2 speaker



Layout Note:

Trace width=40mil

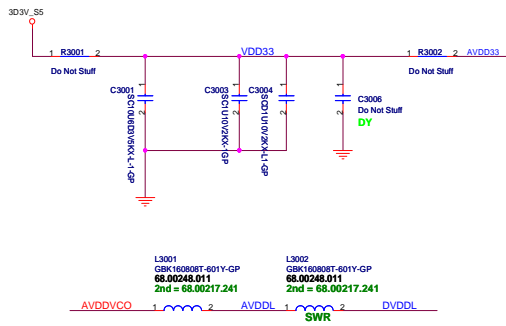
### Combo Jack



EAEG50 KB UMA

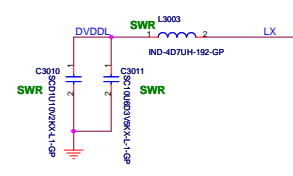
**緯創資通 Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title		Audio Jack	
Size	Project Name	KABINI	Rev SA
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L3001 GRK18008T-601Y-GP  
68.00248.011  
2nd = 68.00217.241

L3002 GRK18008T-601Y-GP  
68.00248.011  
2nd = 68.00217.241



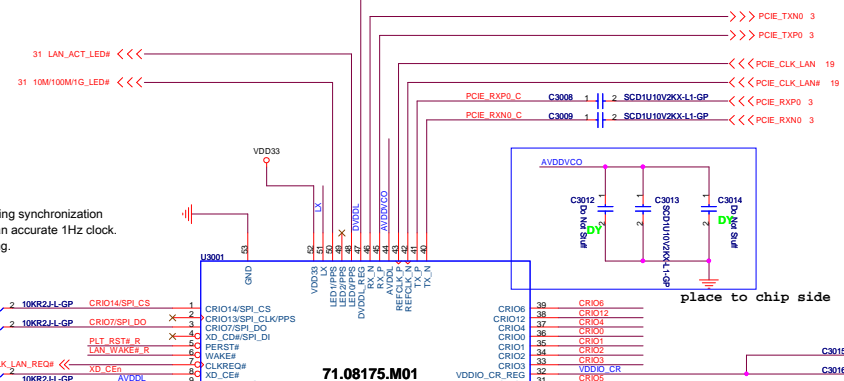
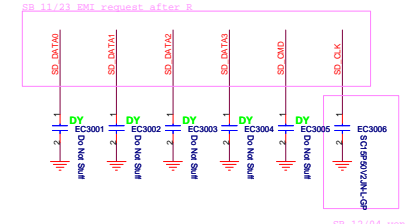
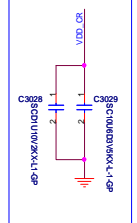
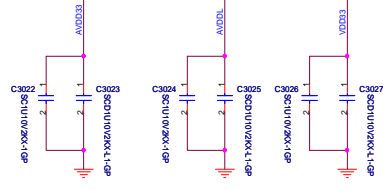
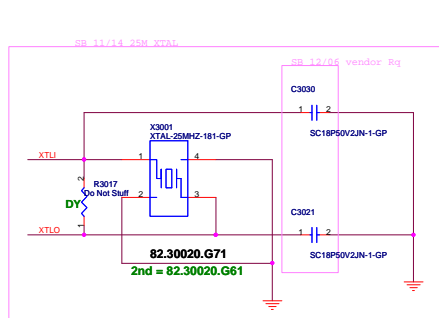
PPS is used for IEEE 1588 timing synchronization and is an output pin to output an accurate 1Hz clock. Currently this pin can be floating.

### Power-On-Strapping Table

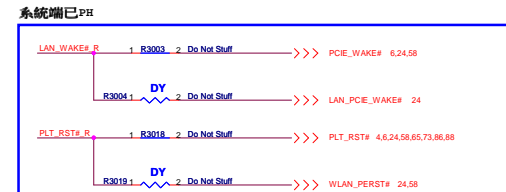
Pin	Description
LED[1]	1 Switch mode regulator (SWR) select
	0 Linear regulator (LDO) select
LED[3]	1 25MHz clock input
	0 48MHz clock input
[CRIO14, CRIO17]	10 1. Support xD, not support SPI. 2. Can support PPS, PPS at LED[0] or LED[1] or LED[2] which is selected by eFuse.
	01 1. Support SPI, not Support xD. 2. Can support PPS, PPS at LED[0] or LED[1] or LED[2] which is selected by eFuse.
	11 1. Not support xD, not support SPI. 2. Only Support PPS, PPS always at CRIO13.

Check!!  
ISOLATn is active low to isolate the whole chip to place in lowest power consumption mode.

place at chip side FAE suggest

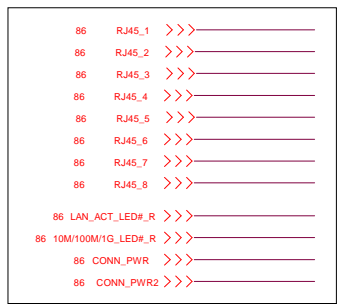
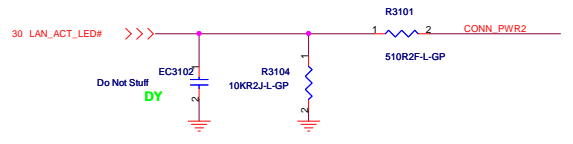
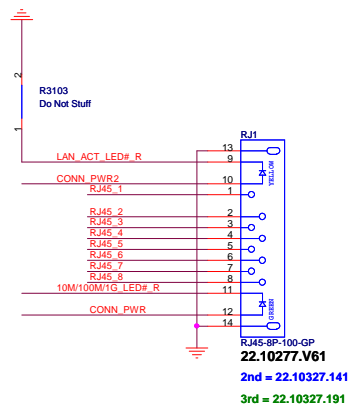
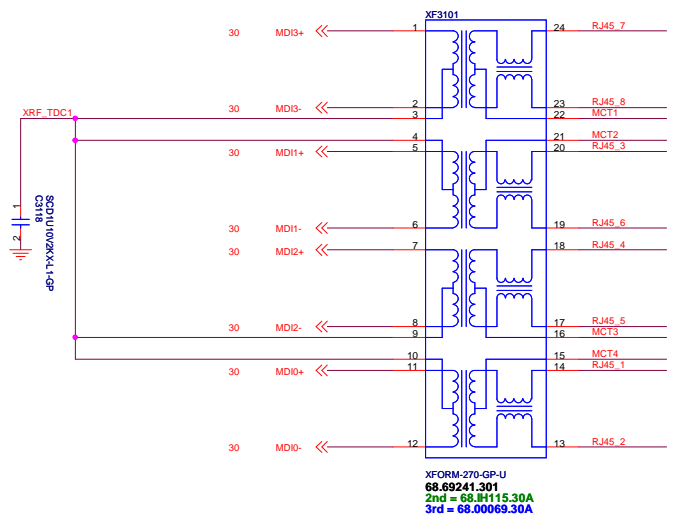


CRIO[0:14]	CRIO[0:14]	xD_CEn	xD_CEn
CRIO14	SDMMC eDn	xD_ALE	xD_CEn
CRIO13	SDMMC eDn	xD_RbDYn	xD_CEn
CRIO12	SDMMC CLK	xD_BiSh	xD_CEn
CRIO11	MMC DAT7	MS DAT7	xDDATA7
CRIO10	MMC DAT6	MS DAT6	xDDATA6
CRIO9	MMC DAT5	MS DAT5	xDDATA5
CRIO8	MMC DAT4	MS CLK	xDDATA4
CRIO7		xD_CLE	xD_CEn
CRIO6	SD_WP	MS_Bs	xD_WPh
CRIO5	SDMMC CMD	MS DAT11	xD_CEn
CRIO4	SDMMC CMD	MS CDn	xD_WEn
CRIO3	SDMMC DAT9	MS DAT9	xDDATA9
CRIO2	SDMMC DAT2	MS DAT2	xDDATA2
CRIO1	SDMMC DAT1	MS DAT14	xDDATA1
CRIO0	SDMMC DAT0	MS DAT0	xDDATA0

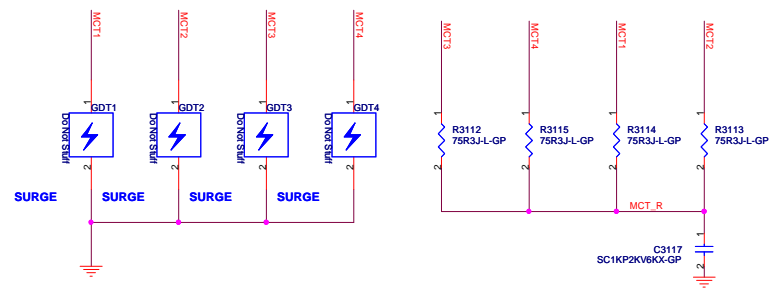
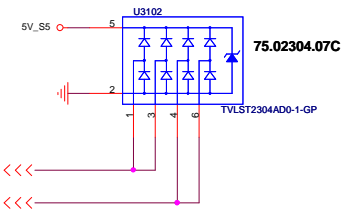
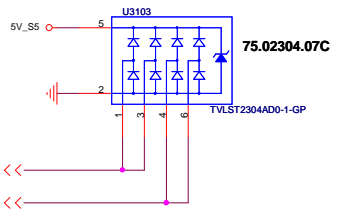
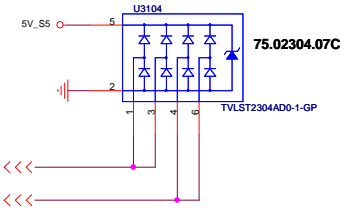
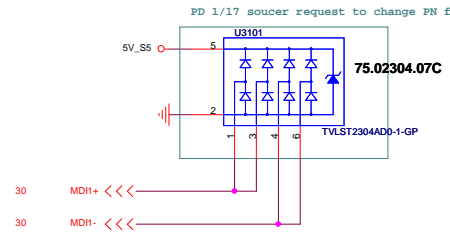
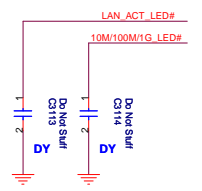
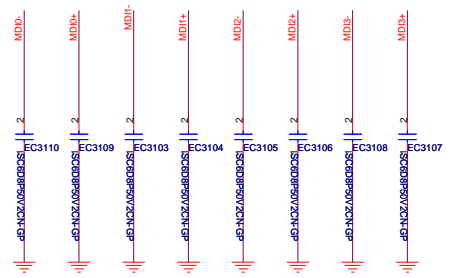
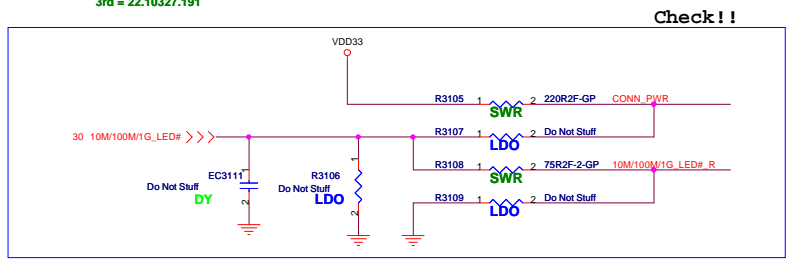


CRIO0	R3007	2	<<>>	SD_DATA0	33.86
CRIO1	R3008	2	<<>>	SD_DATA1	33.86
CRIO2	R3009	2	<<>>	SD_DATA2	33.86
CRIO3	R3010	2	<<>>	SD_DATA3	33.86
CRIO4	R3011	2	<<>>	SD_CMD	33.86
CRIO5	R3012	2	<<>>	SD_CLK	33.86
CRIO6	R3013	2	<<>>	SD_WP	33
CRIO12	R3014	2	<<>>	SD_CD#	33

**SSID = LAN**



For AFTE



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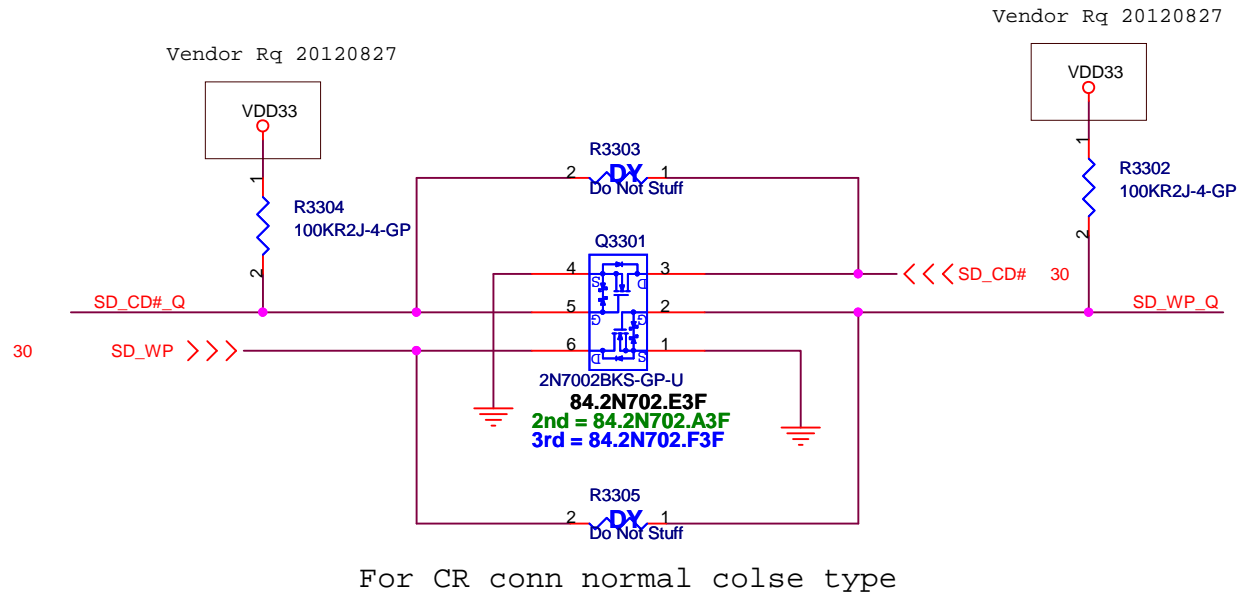
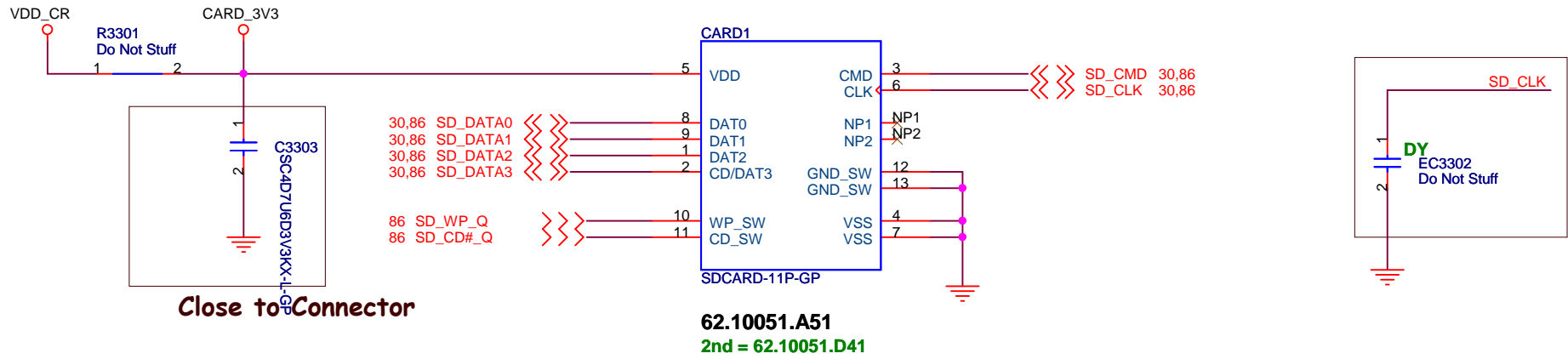
緯創資通 **Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONNECTOR**  
 Project Name: **KABINI**

Date: Monday, February 04, 2013 Sheet 31 of 102

**SSID = SDIO**

# SD//MS Card Reader



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緯創資通

**Wistron Corporation**

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**CARD Reader CONN**

Size

Project Name

**KABINI**

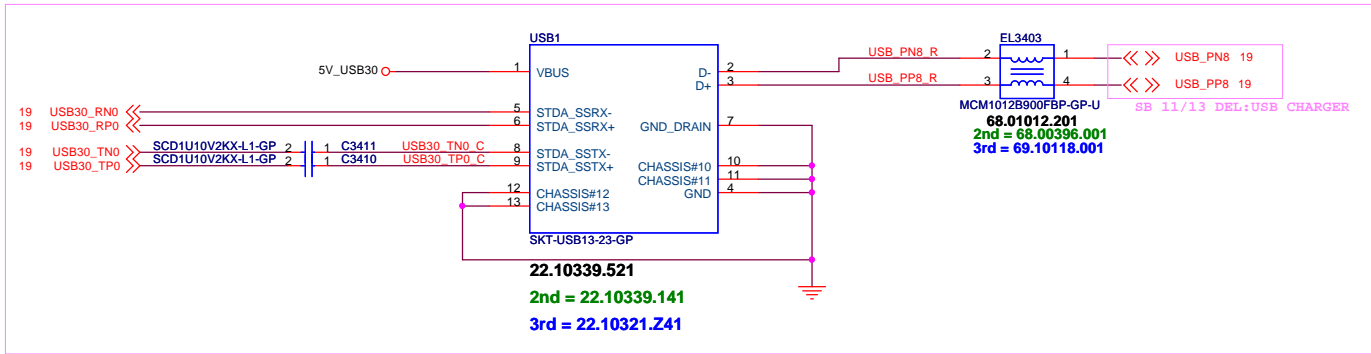
Rev

**SA**

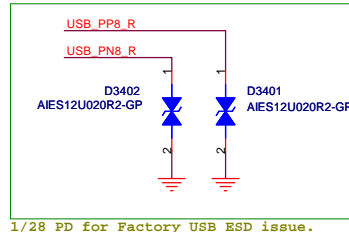
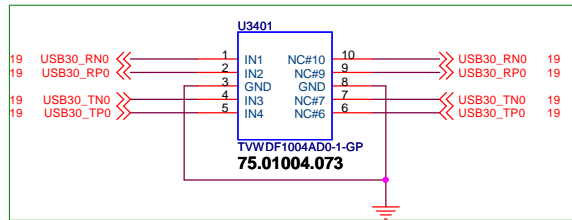
Date: Monday, February 04, 2013

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USB 2.0 CONTACT PIN		USB 3.0 CONTACT PIN	
PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME
1	VBUS	5	StdA_SSRX-
2	D-	6	StdA_SSRX+
3	D+	7	GND_DRAIN
4	GND	8	StdA_SSTX-
		9	StdA_SSTX+

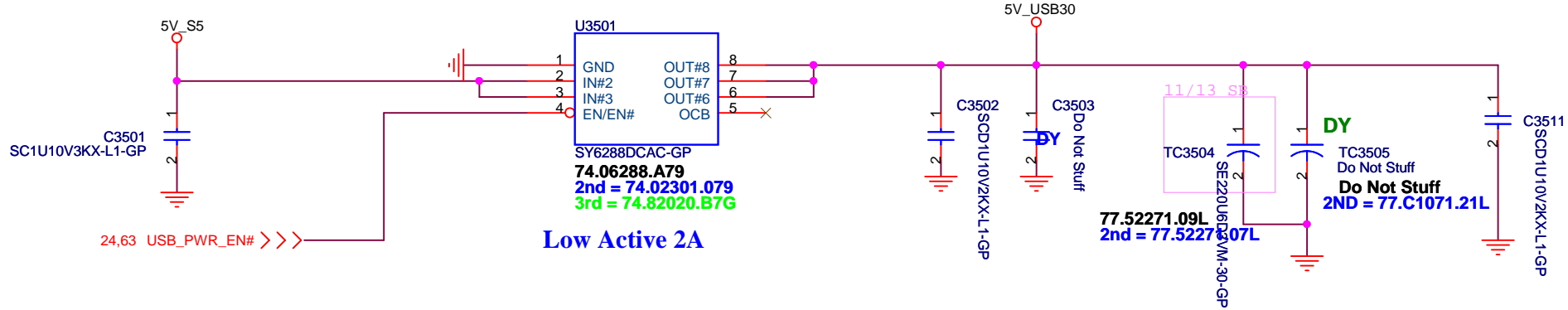


SB 11/13 Change USB30 P/N



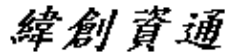
EAEG50 KB UMA

<b>緯創資通</b>		<b>Wistron Corporation</b>	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title		<b>USB 3.0 Port</b>	
Size	Project Name	<b>KABINI</b>	Rev
			<b>5A</b>
Date: Monday, February 04, 2013		Sheet 34 of 102	

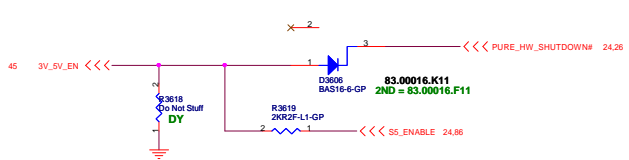
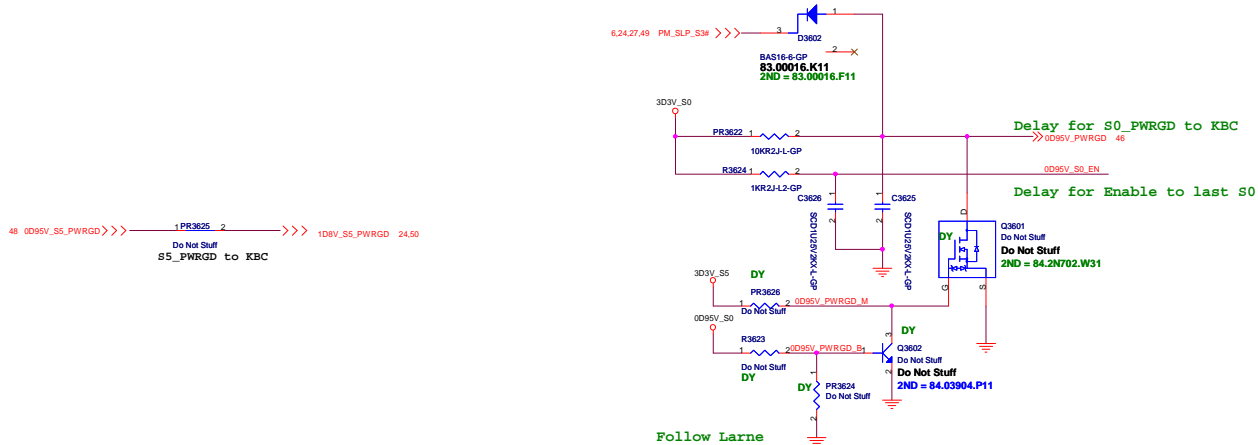
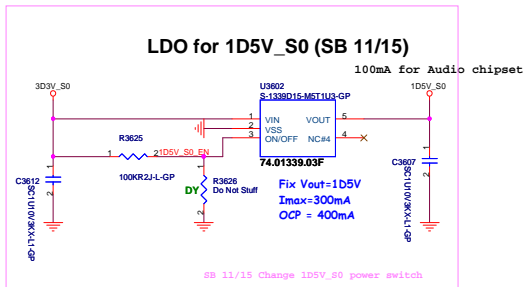
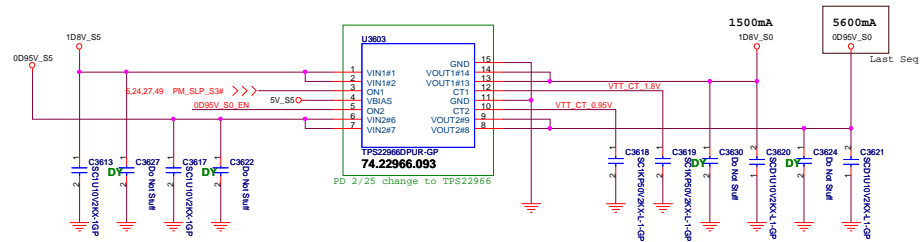
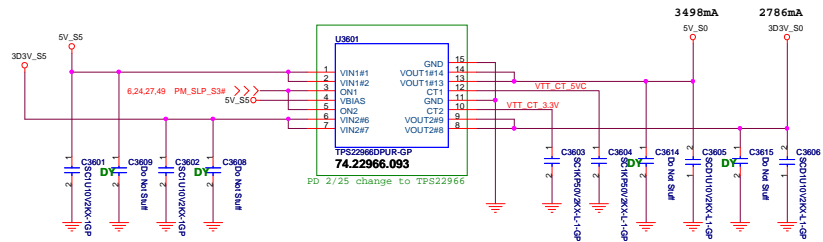


SC 12/20 EA50: Mount TC3504 , DY TC3505

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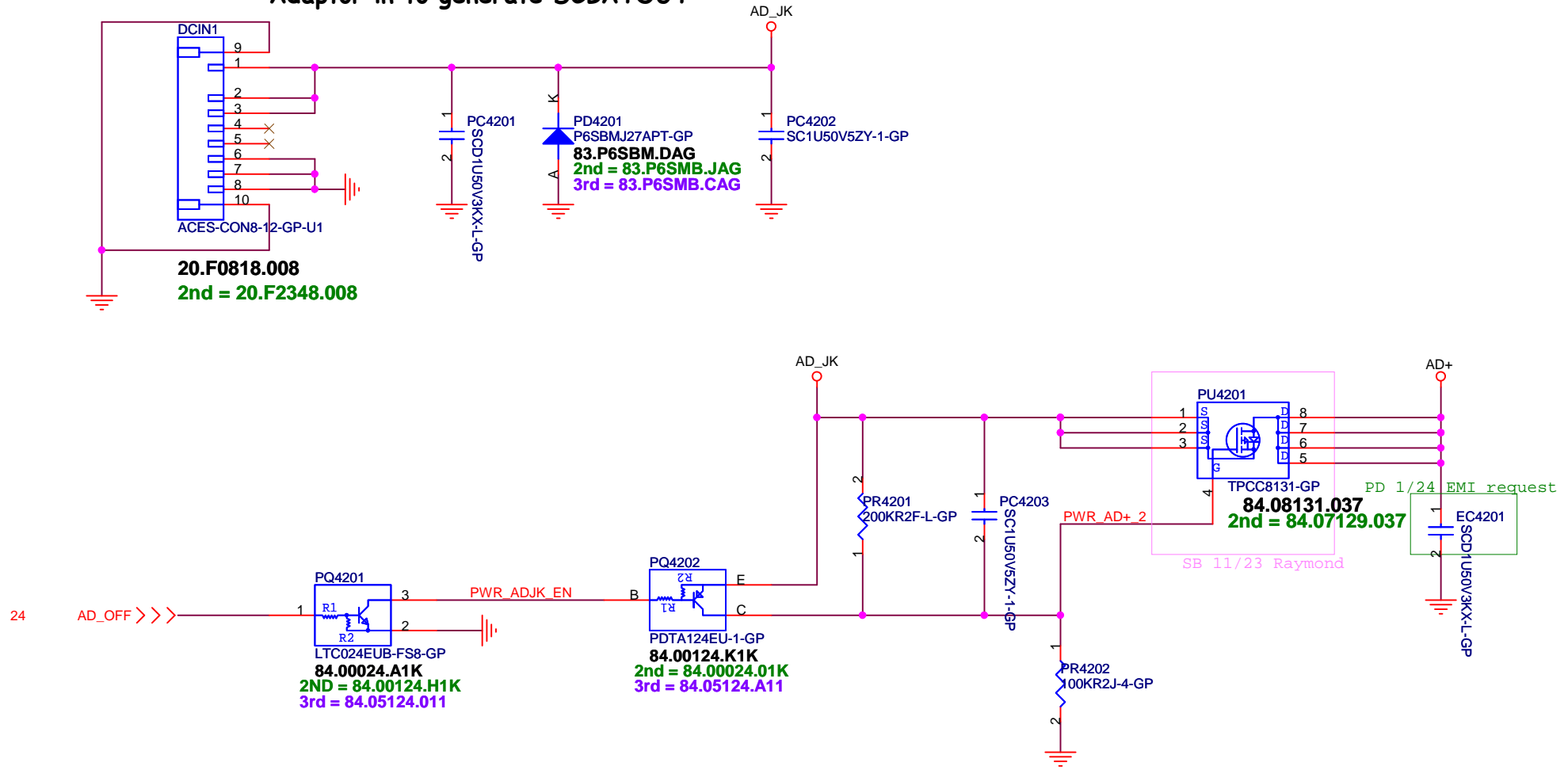
 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b> USB_Charger	
<b>Size</b>	<b>Project Name</b> KABINI
<b>Date</b> Monday, February 04, 2013	<b>Rev</b> SA
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# Power Sequence



# ANNIE solution

## Adaptor in to generate DCBATOUT



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Taipei Hsien 221, Taiwan, R.O.C.

Title

**DCIN JACK**

Size

Project Name

**KABINI**

Rev

**SA**

Date: Tuesday, February 19, 2013

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**SSID = PWR.Plane.Regulator\_3p3v5v**

Cut off itself

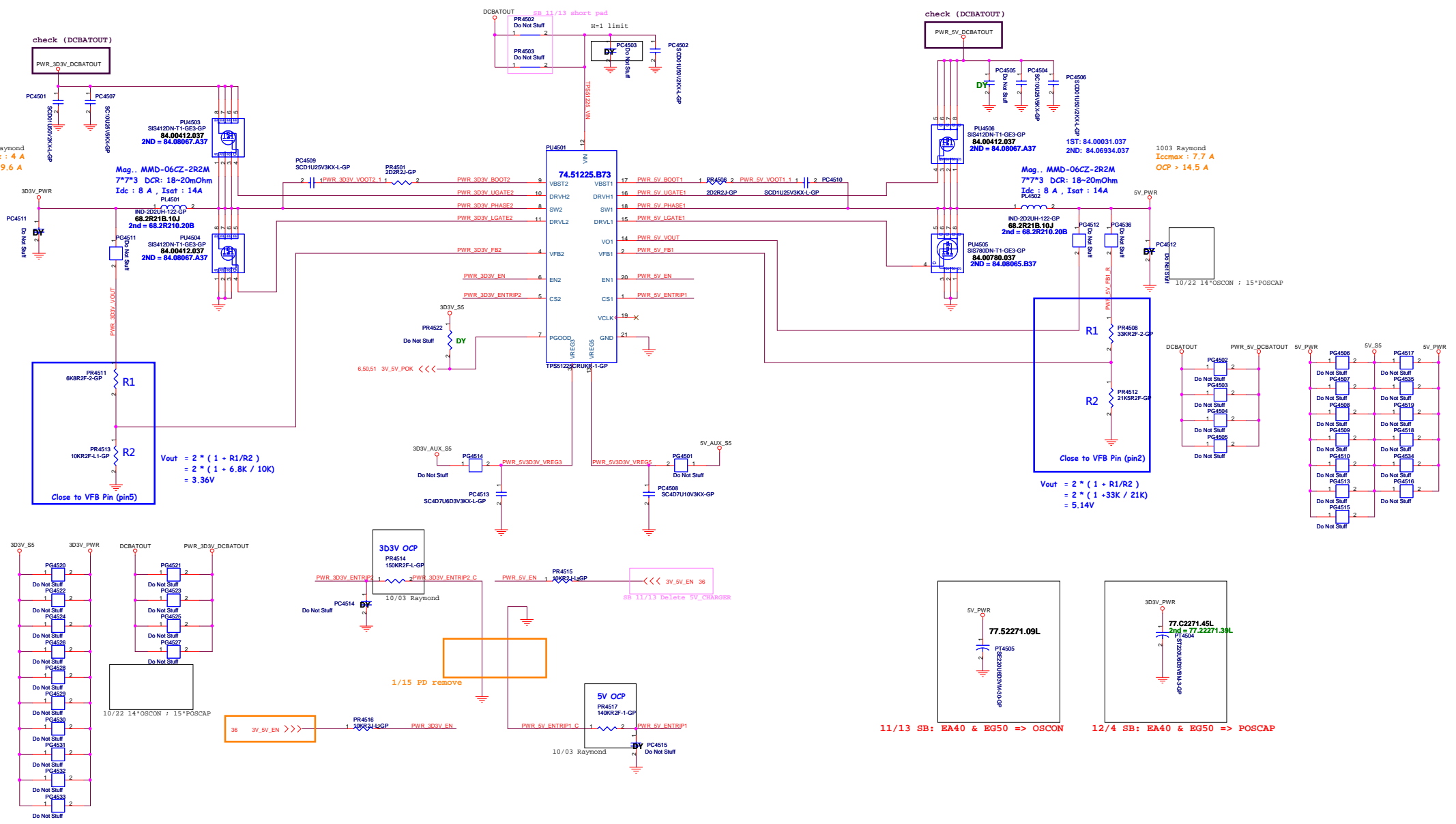
check (UVP)

check (DCBATOUT)

check (DCBATOUT)

1003 Raymond  
Iccmax : 4 A  
OCP > 9.6 A

1003 Raymond  
Iccmax : 7.7 A  
OCP > 14.5 A

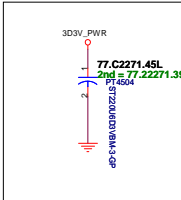
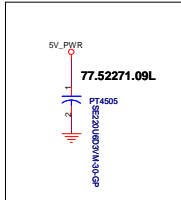
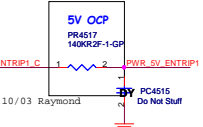
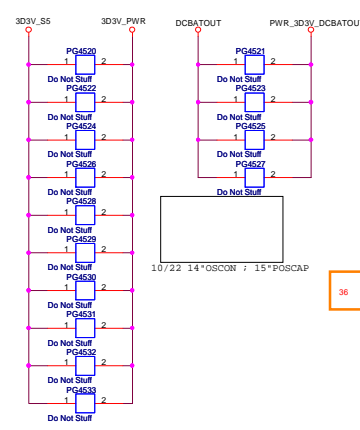


Close to VFB Pin (pin5)

$V_{out} = 2 * (1 + R1/R2)$   
 $= 2 * (1 + 6.8K / 10K)$   
 $= 3.36V$

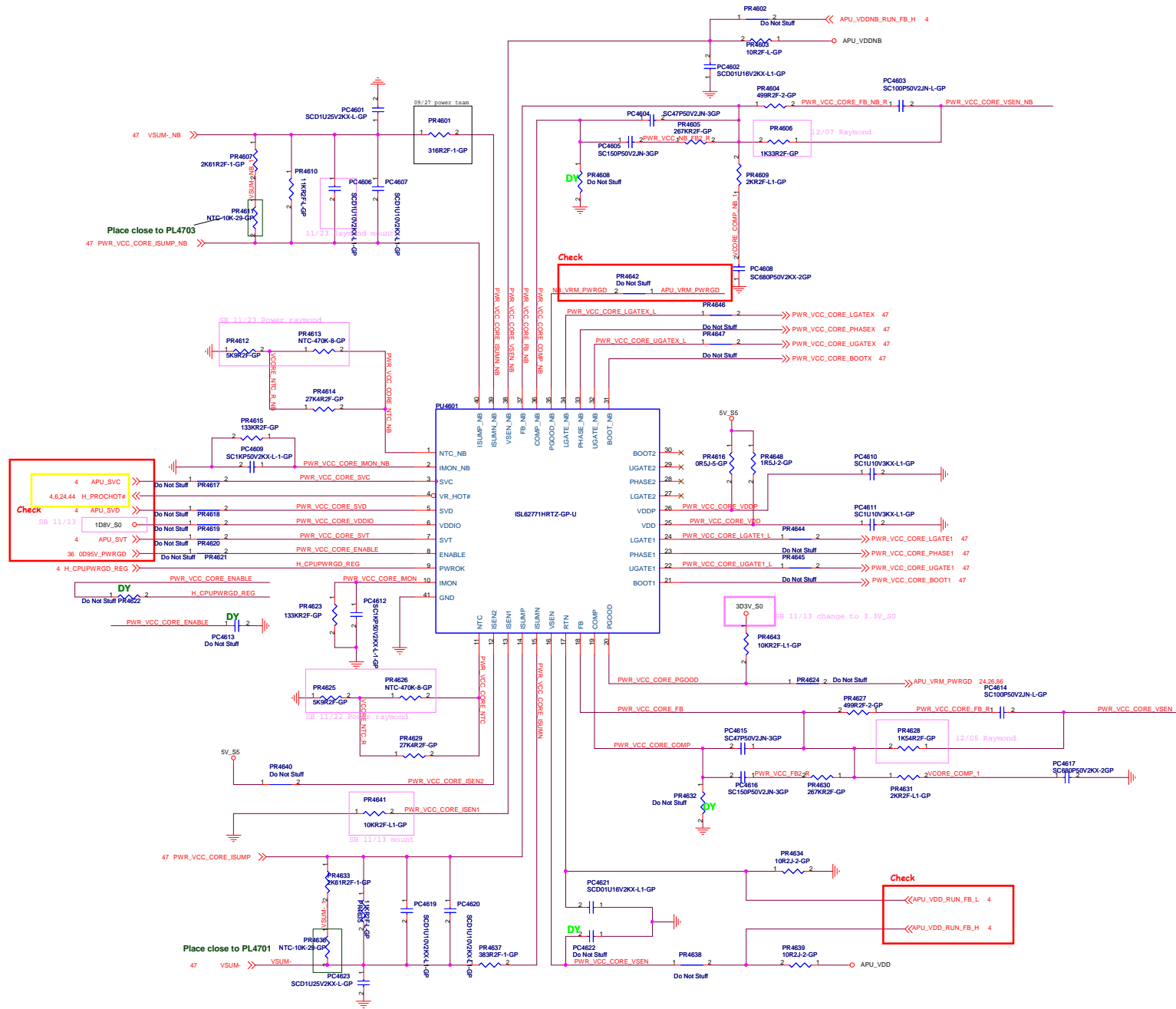
Close to VFB Pin (pin2)

$V_{out} = 2 * (1 + R1/R2)$   
 $= 2 * (1 + 33K / 21K)$   
 $= 5.14V$



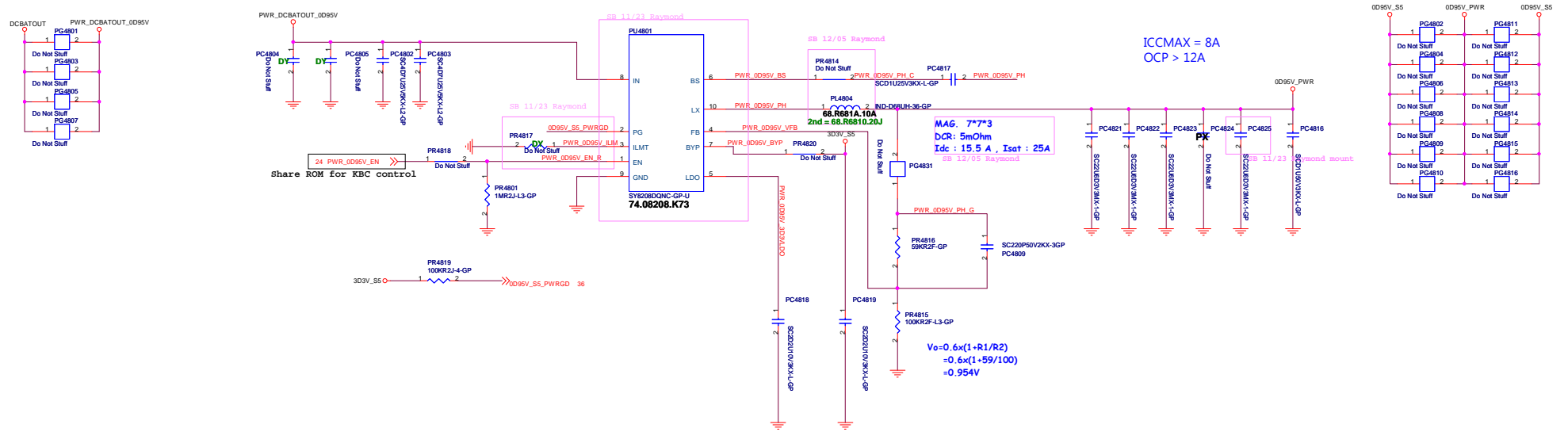
11/13 SB: EA40 & EG50 => OSCON

12/4 SB: EA40 & EG50 => POSCAP





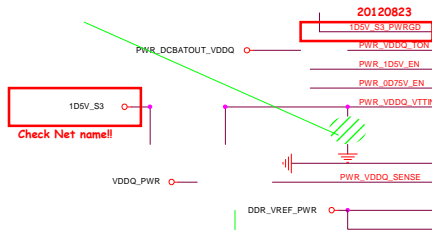
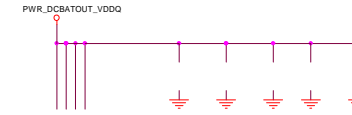
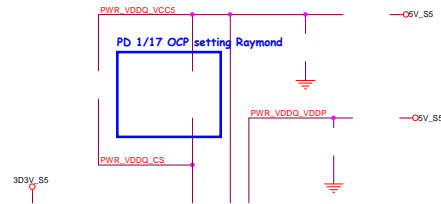
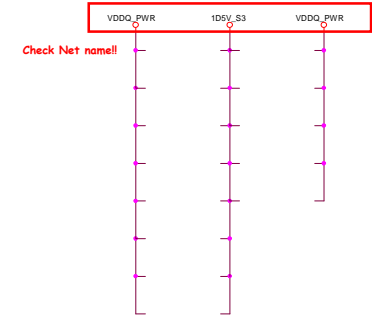
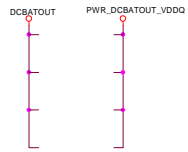
# SY8208D for OD95V



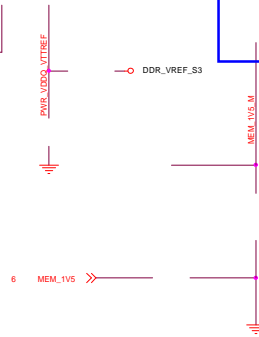
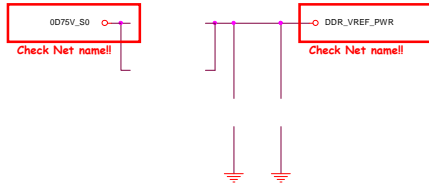
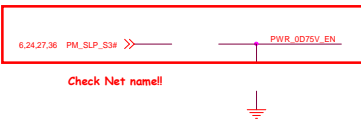
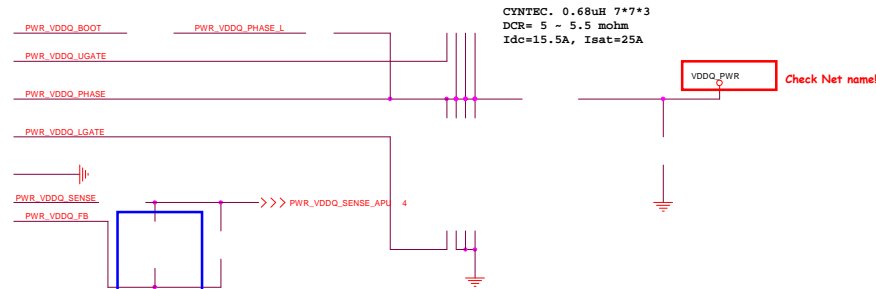
EAE650 KB UIM

緯創資通 Wistron Corporation  
21F, 8F, Sec.1, Hsin Tai Wu Rd., Hsichia, Taipei Hsien 221, Taiwan, R.O.C.

Title			
DC to DC OD95V(RT8237C)			
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**I<sub>o</sub>max=1A  
OCP>1.5A**  
Close to output cap pin1, not inside of the output cap

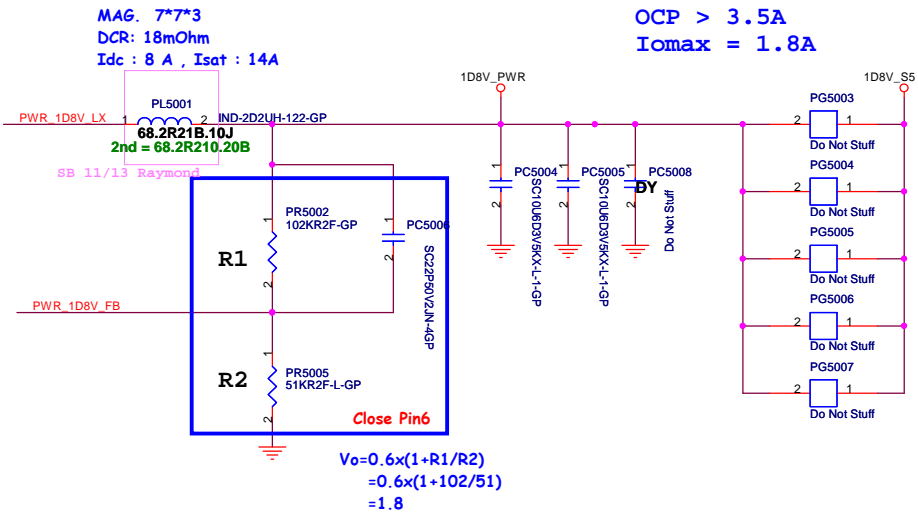
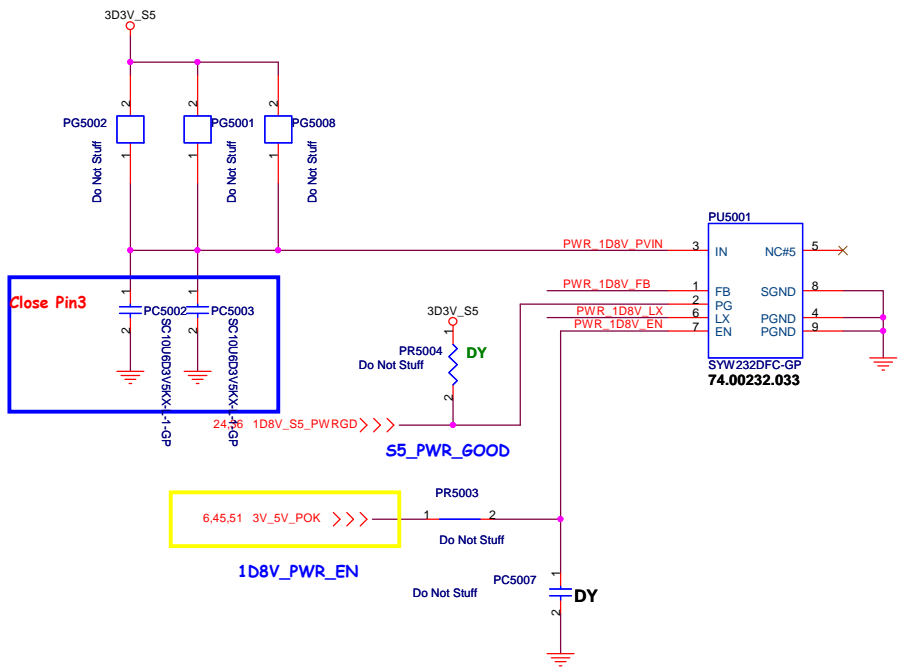


EAEG50 KB UIM

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Title			RT8207		
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A2	KABINI				
Date	Monday, February 04, 2013	Sheet	49	of	102

# SSID = PWR.Plane.Regulator\_1p8v



EAEG50 KB UMA

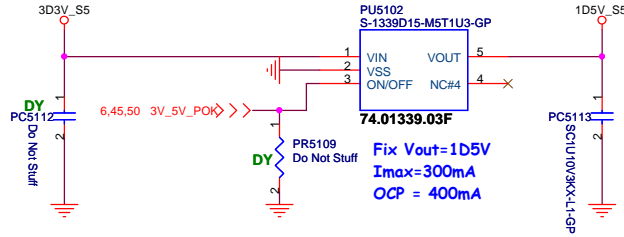
緯創資通 **Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

<b>Title</b>		
<b>1D8V_S0 SYW232</b>		
<b>Size</b>	<b>Document Number</b>	<b>Rev</b>
A3	<b>KABINI</b>	
<b>Date:</b> Monday, February 04, 2013		<b>Sheet</b> 50 <b>of</b> 102

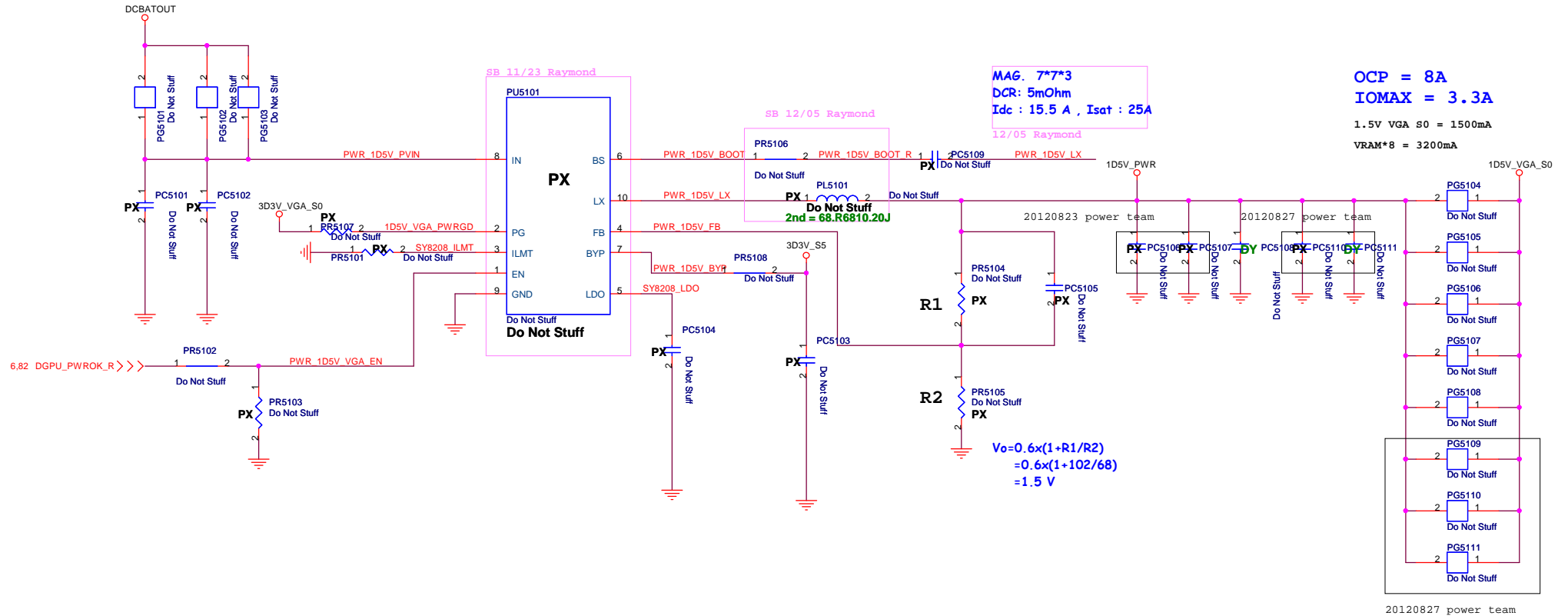


### LDO for 1D5V\_S5 (SB 11/13)

$$1.5V\ S0 = 100mA(VDDIO\_AZ) + 100mA(Audio) + 600mA(Minicard\ DY) = 200mA$$



### SY8208D for 1D5V\_VGA\_S0 (SB 11/13)



EAEG50 KB UMA

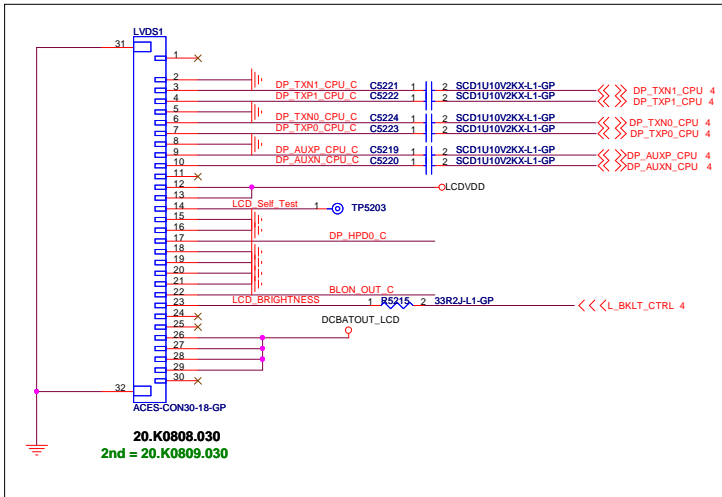
**緯創資通 Wistron Corporation**  
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title **1D5V\_S5 SY8208D**

Size A3 Document Number **KABINI** Rev

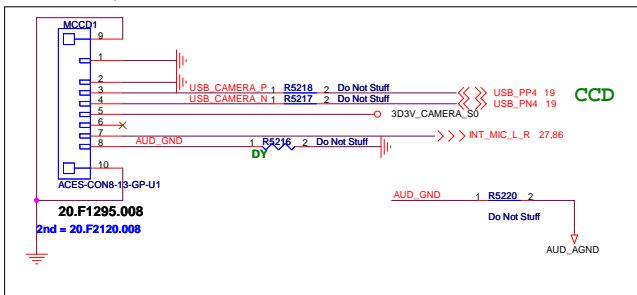
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eDP Conn.



10/04 change to 20.K0808.030 for ME request

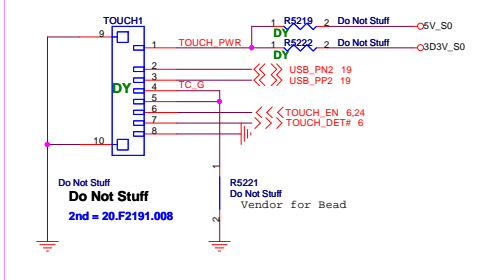
Camera+MIC Conn.



10/03 change to 8pin for del DMIC

10/15 change to 20.F1295.008 follow HW

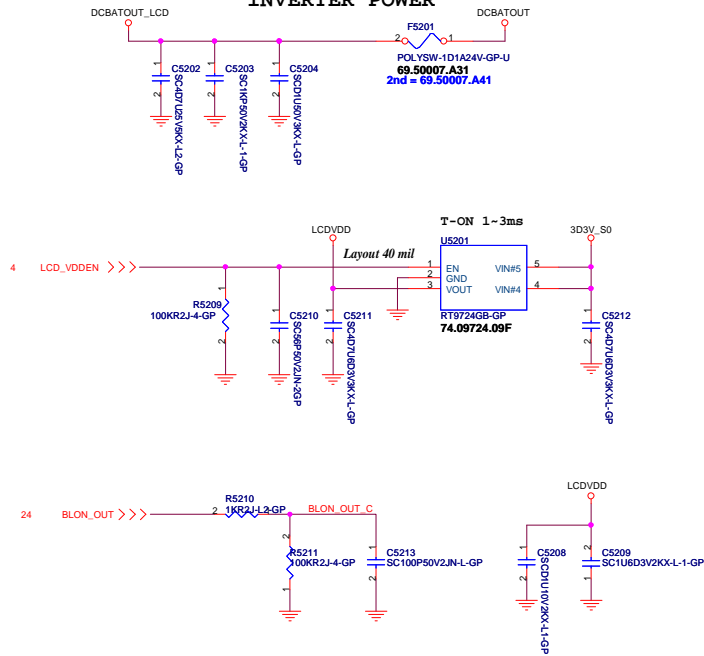
Touch Conn.



SB 12/12 DUMMY for ME issue

SC NO support

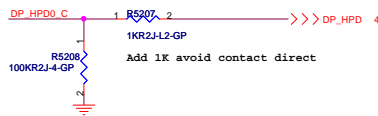
INVERTER POWER



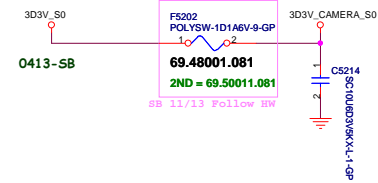
- 86 AUD\_GND <<<
- 86 DP\_HP00\_C >>>
- 86 BLON\_OUT\_C >>>
- 86 LCD\_BRIGHTNESS >>>
- 86 DP\_TXN1\_CPU\_C >>>
- 86 DP\_TXP1\_CPU\_C >>>
- 86 DP\_TXN0\_CPU\_C >>>
- 86 DP\_TXP0\_CPU\_C >>>
- 86 DP\_AUXP\_CPU\_C <<<
- 86 DP\_AUXN\_CPU\_C <<<

For AFTE

EDP HPD High active



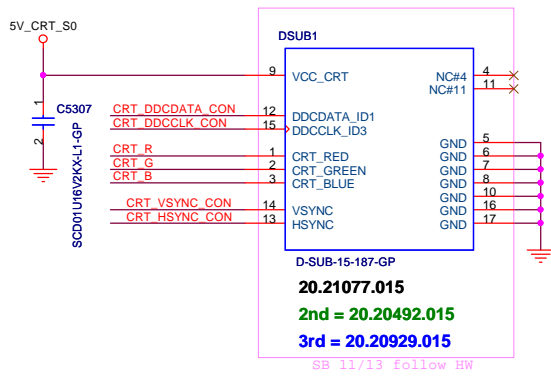
Camera Power



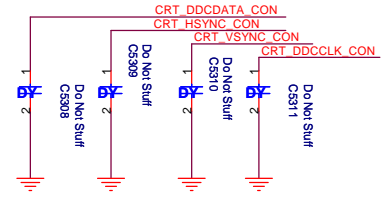
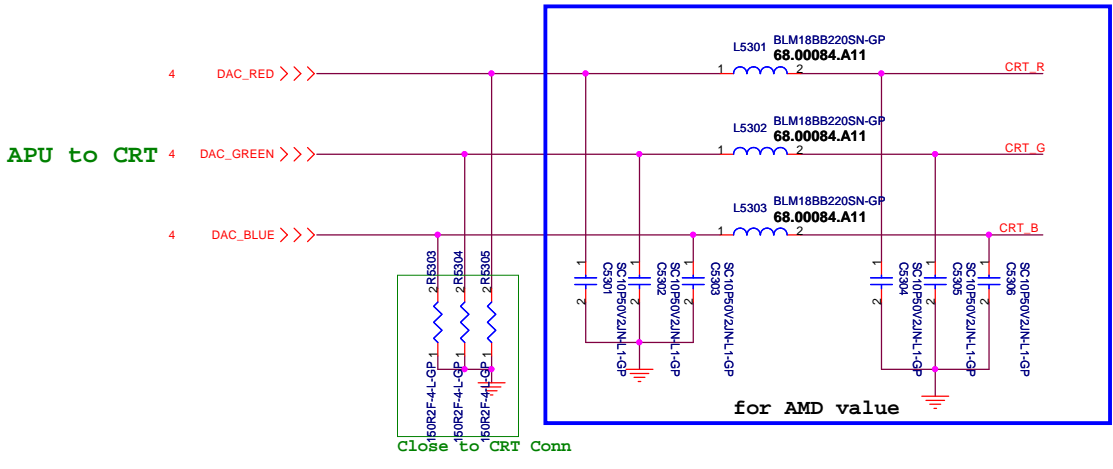
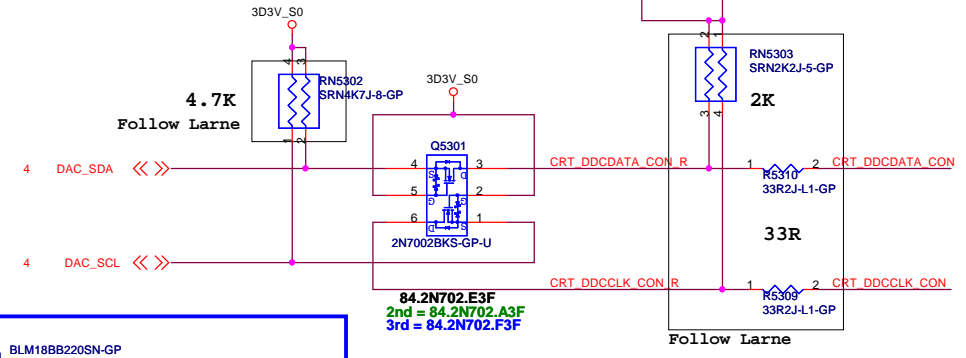
EAEG50 KB UMA

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		LCD Connector	
Size	Project Name	KABINI	Rev SA
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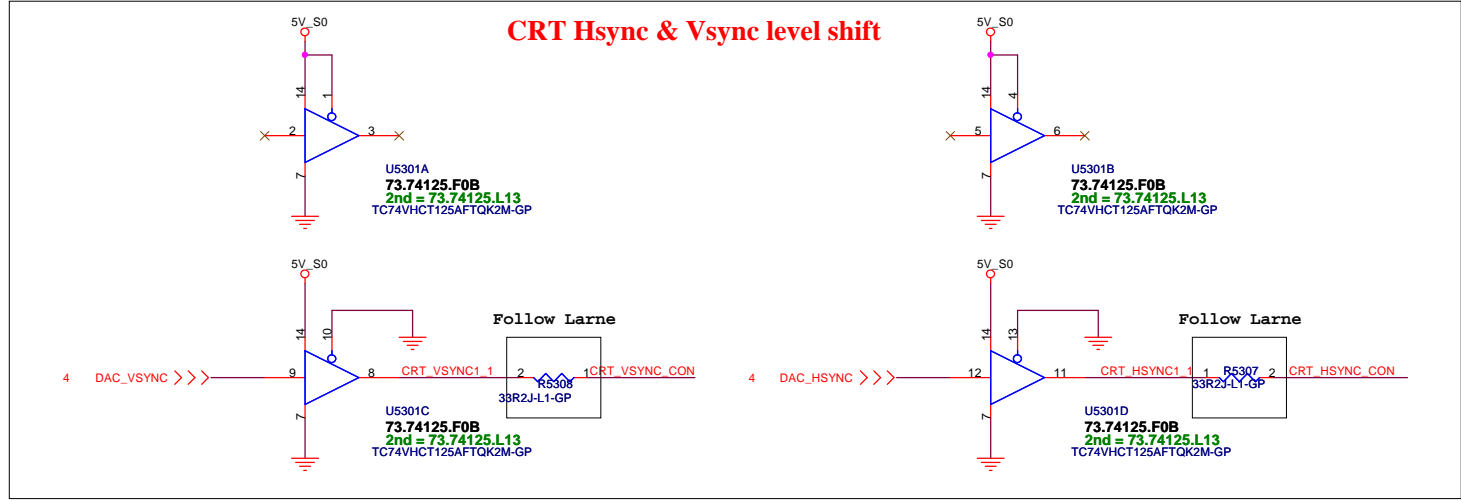


### CRT DDCDATA & DDCCLK level shift



10/16 follow COMAL

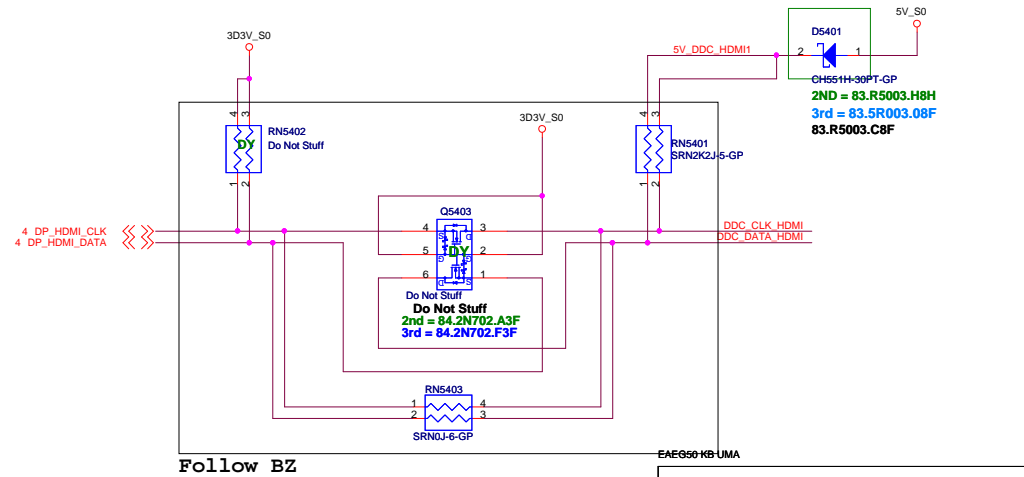
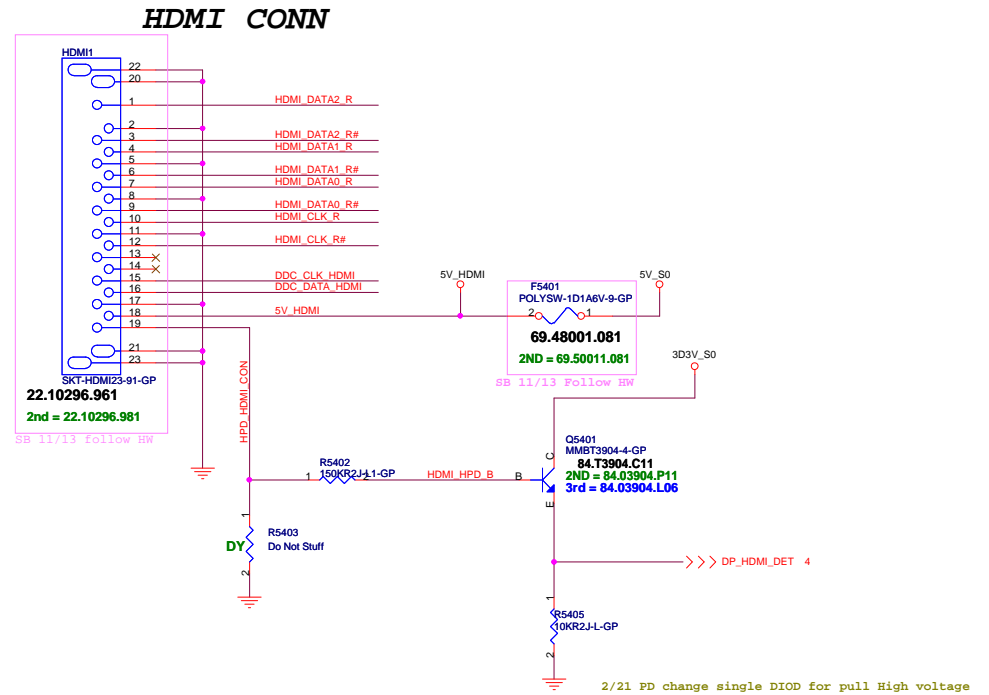
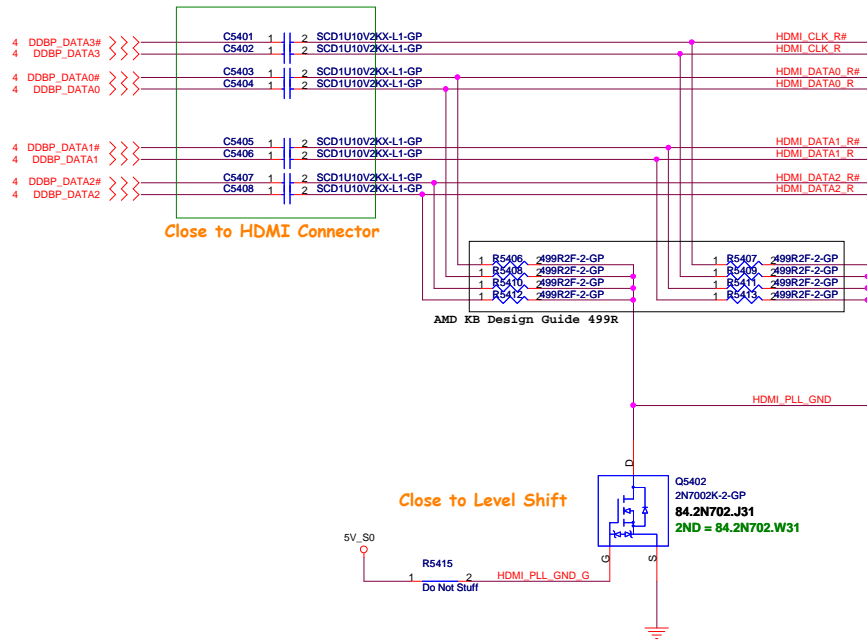
### CRT Hsync & Vsync level shift



EAEG50 KB UMA

<b>緯創資通 Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>CRT Board Connector</b>	
Title	Rev <b>SA</b>
Size	Project Name
<b>KABINI</b>	
Date: Monday, February 04, 2013	Sheet 53 of 102

# SSID = VIDEO HDMI Level Shifter & CONNECTOR

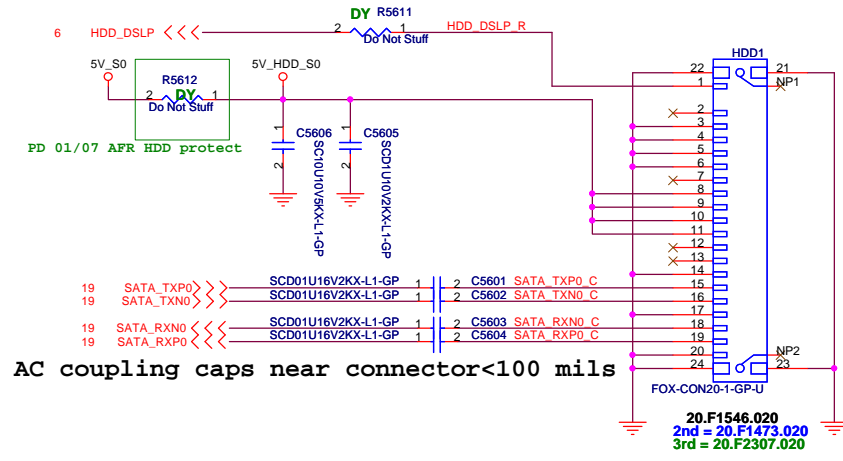
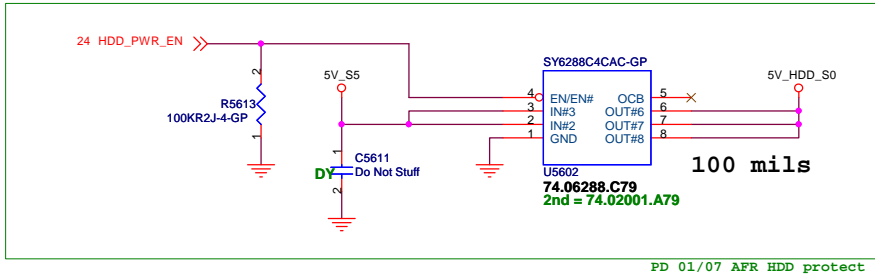


緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title			HDMI Level Shifter/Connector		
Size	Project Name				Rev
	KABINI				SA
Date:	Thursday, February 21, 2013	Sheet	54	of	102

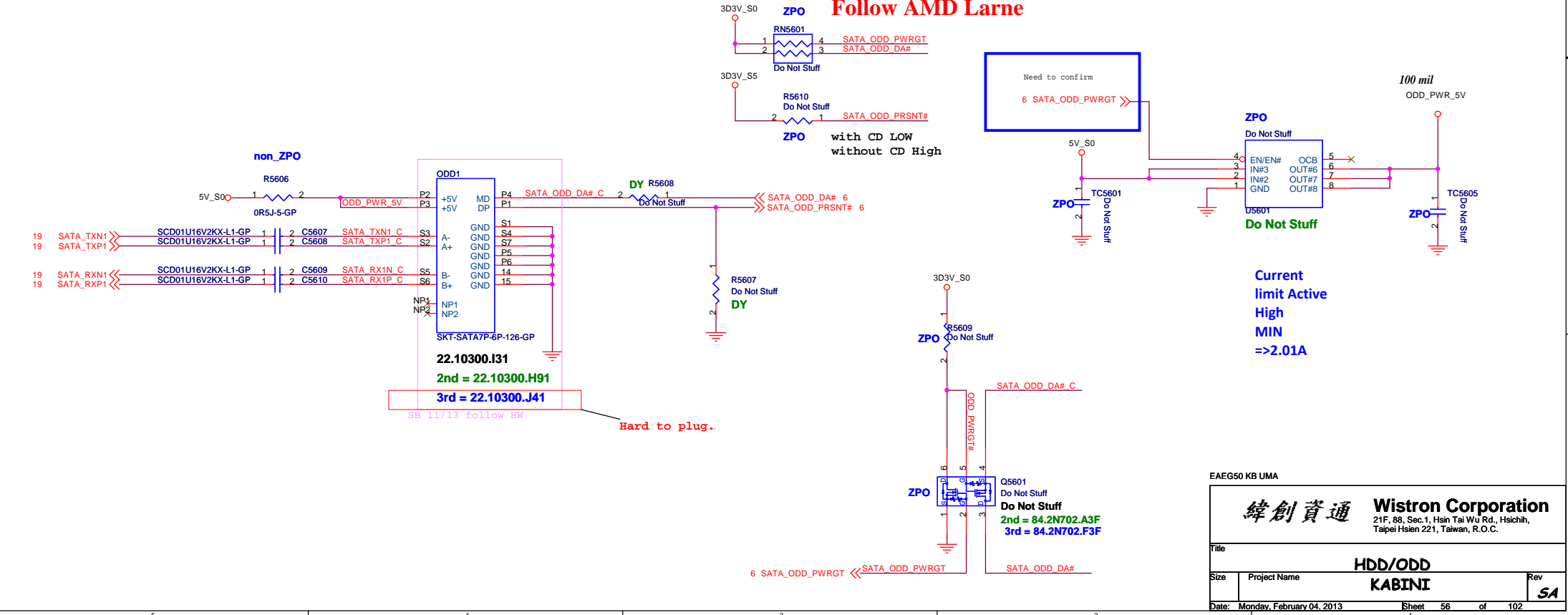
SSID = SATA

# SATA HDD Connector



# ODD Connector

## SATA Zero Power ODD Follow AMD Larne



EAEG50 KB UMA

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size: Project Name: KABINI Rev: SA

Date: Monday, February 04, 2013 Sheet 56 of 102



**SSID = Wireless**

# *Mini Card Connector(WWAN)*

EAEG50 KB UMA

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**WWAN CONN**

Size

Project Name

**KABINI**

Rev

**SA**

Date: Friday, September 07, 2012

Sheet 59 of 102

SSID = mSATA

# Mini Card Connector(mSATA)

EAEG50 KB UMA

緯創資通

**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**mSATA Connector**

Size

Project Name

**KABINI**

Rev

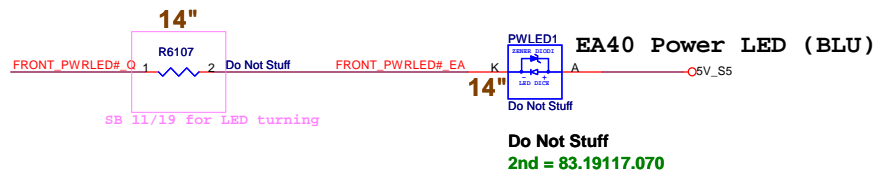
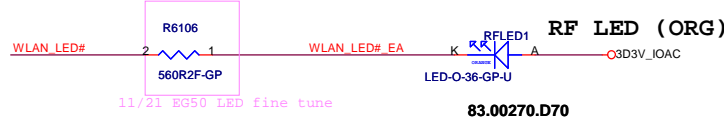
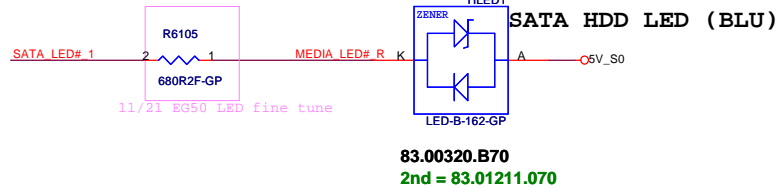
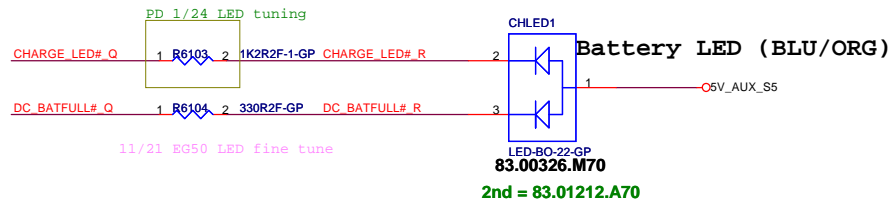
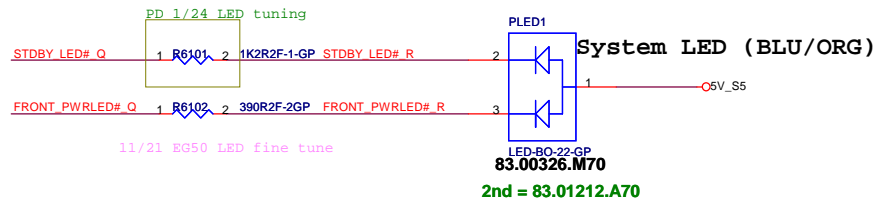
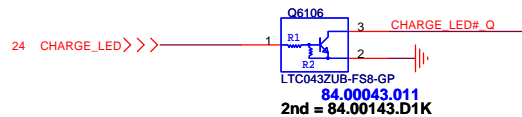
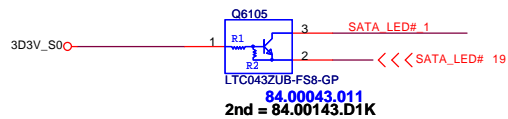
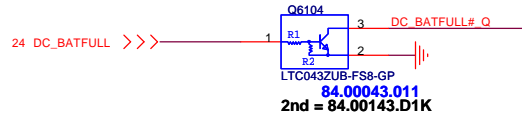
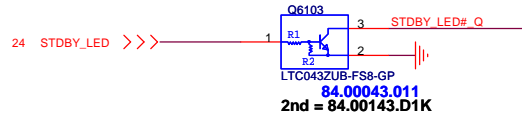
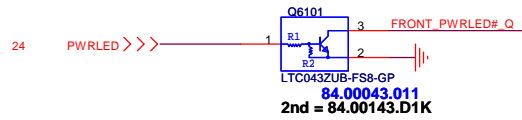
**SA**

Date: Friday, September 07, 2012

Sheet 60 of 102

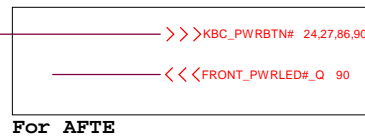
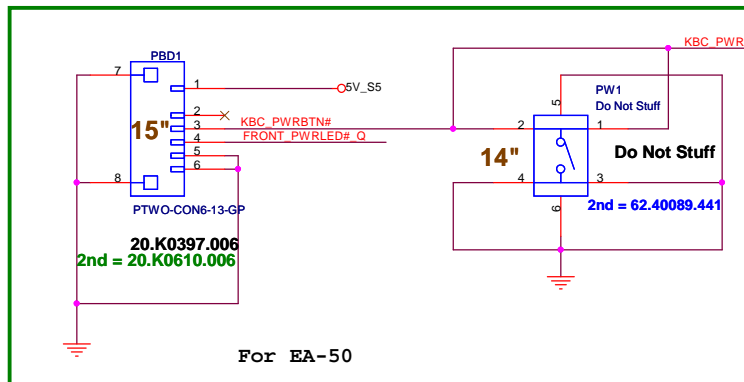
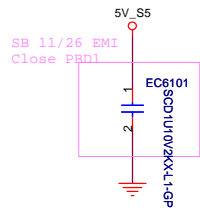
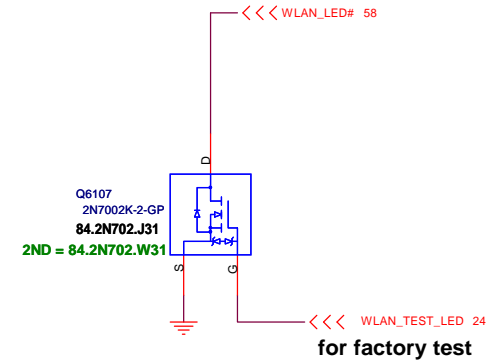


# SSID = User.Interface



## WLAN\_LED

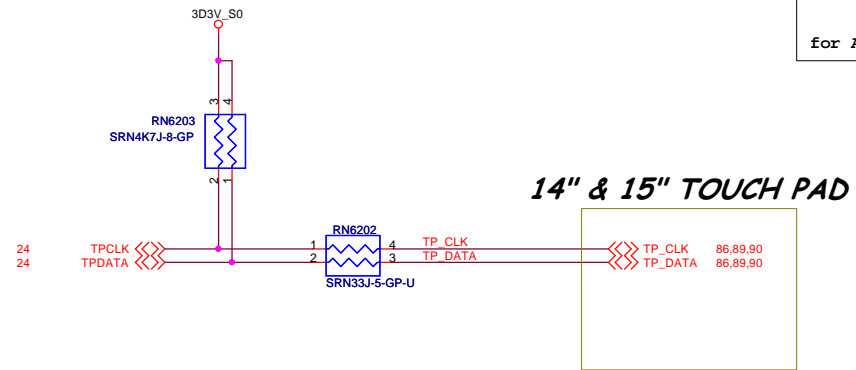
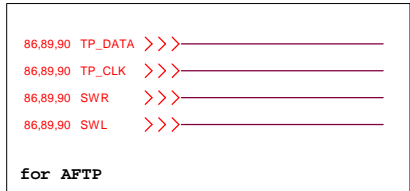
From module



EAEG50 KB UMA

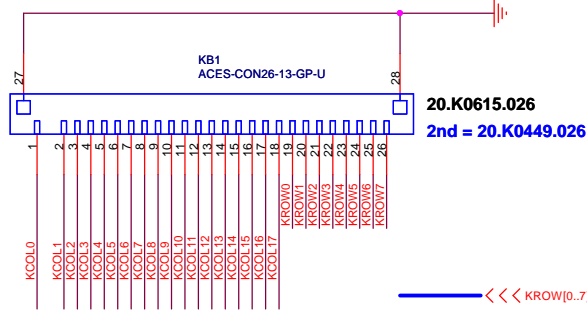
**SSID = KBC**

**Internal Keyboard  
Connector**



PD 1/14 Different 14" & 15" TOUCH PAD reversion

14"& 15" use the same KB



<<< KROW[0..7] 24,86

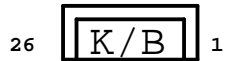
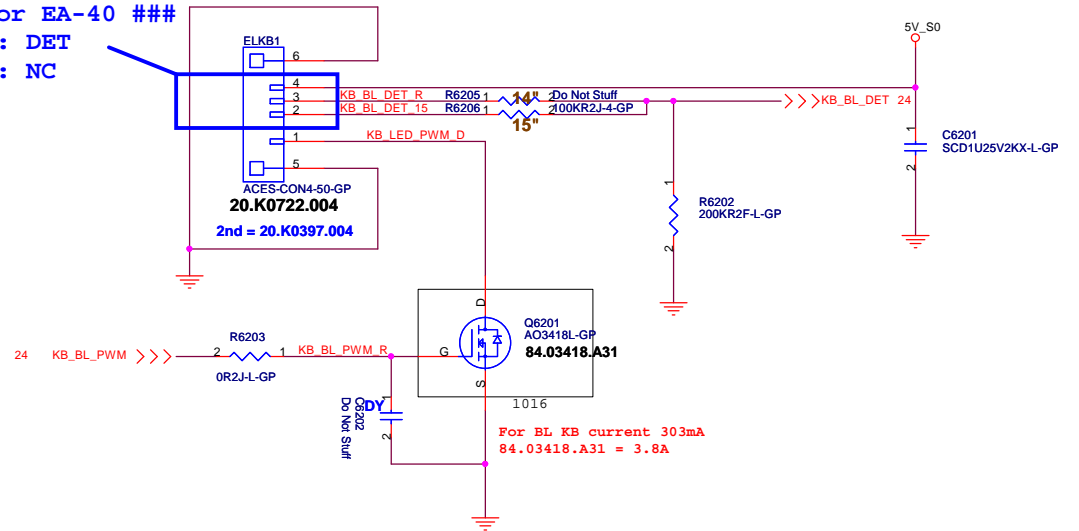
>>> KCOL[0..17] 24,86

### for EA/EG-50 ###

Pin3 : NC  
 Pin2 : DET

### for EA-40 ###

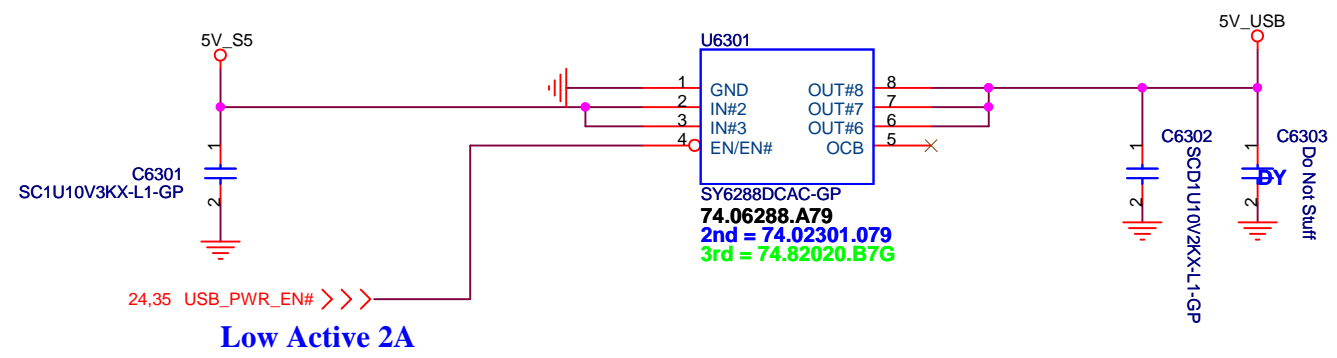
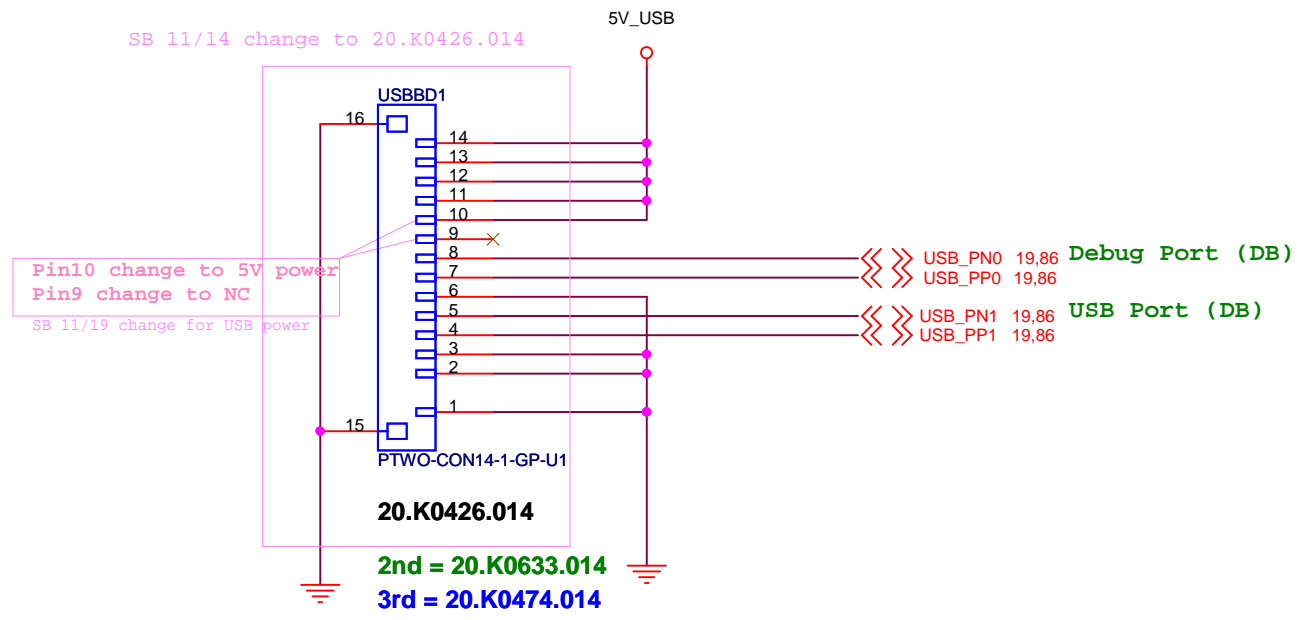
Pin3 : DET  
 Pin2 : NC



MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1  
 KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26

EAEG50 KB UMA

<b>緯創資通 Wistron Corporation</b>	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Key Board/Touch Pad</b>	
Title	Rev SA
Size	Project Name
<b>KABINI</b>	
Date: Tuesday, February 19, 2013	Sheet 62 of 102

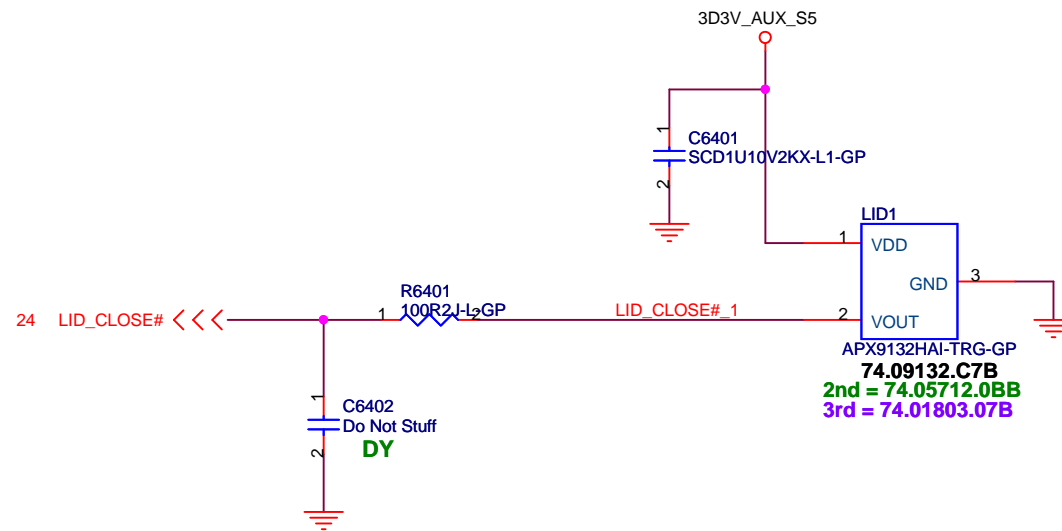


EAE50 KB UMA

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	

**IO Board Connector**

Size	Project Name	<b>KABINI</b>	Rev
			<b>SA</b>



EAEG50 KB UMA

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Hall Sensor**

Size

Project Name

**KABINI**

Rev

**SA**

Date: Monday, February 04, 2013

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(Blanking)

EAEG50 KB UMA

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

Size

Project Name

**KABINI**

Rev

**SA**

Date: Friday, September 07, 2012

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**SSID = User.Interface**

EAEG50 KB UMA

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**G Sensor**

Size

Project Name

**KABINI**

Rev

**SA**

Date: Friday, September 07, 2012

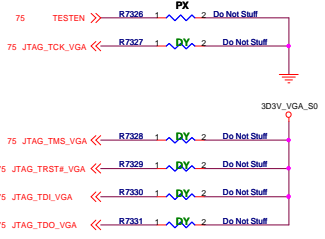
Sheet 67 of 102



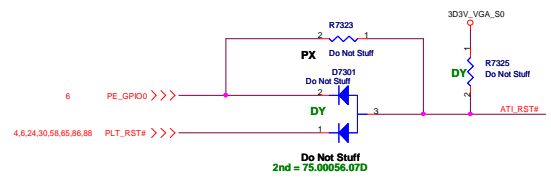
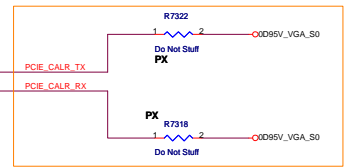
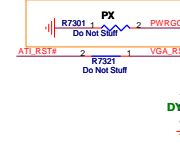
KABINI only 4 lane PEG

JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"0" (PD)	"1" (PU)	"0" (PD)
JTAG_TRST#	"1" (PU)	"1" (PU)	NC
JTAG_TCK	"0" (PD)	"1" (PU)	NC
JTAG_TMS	"1" (PU)	"1" (PU)	NC



100MHz  
check register value



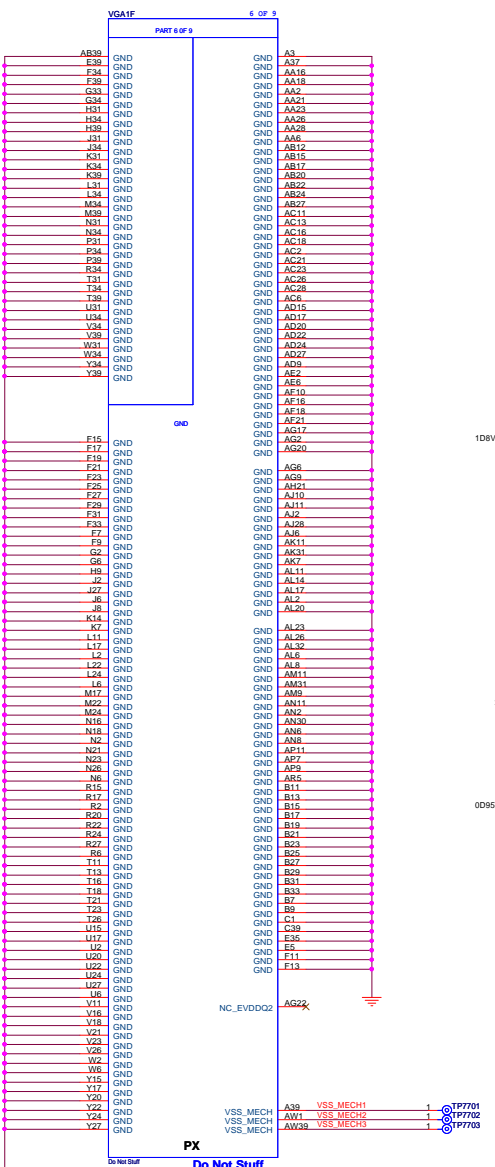
	PE_GPI00
dGPU mode	H
IGPU	L
IGPU with BACO	H







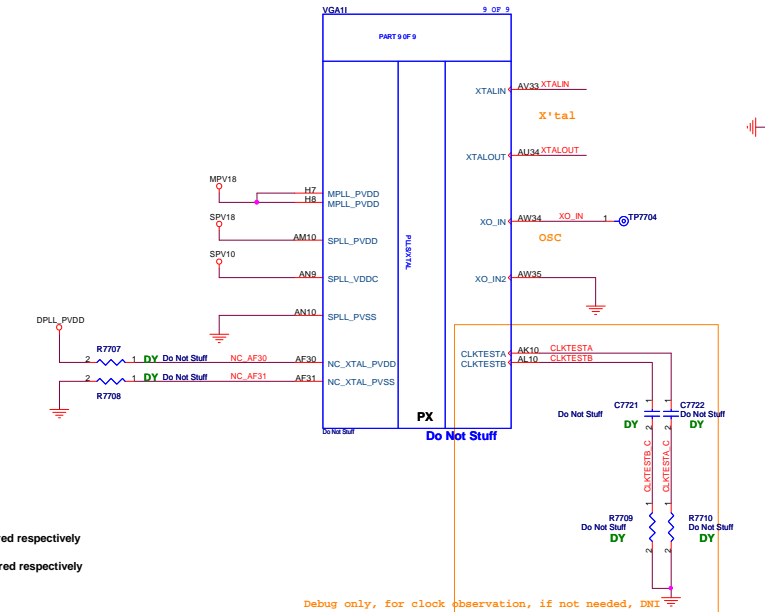
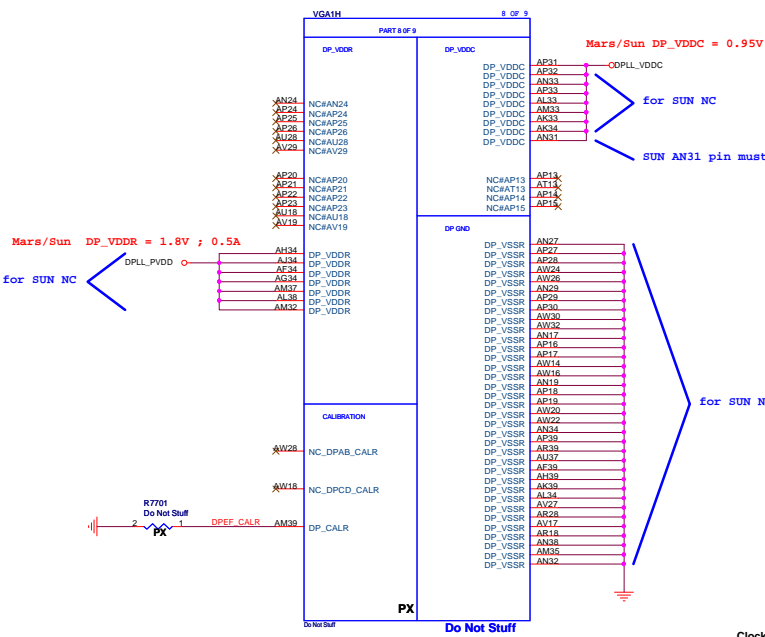




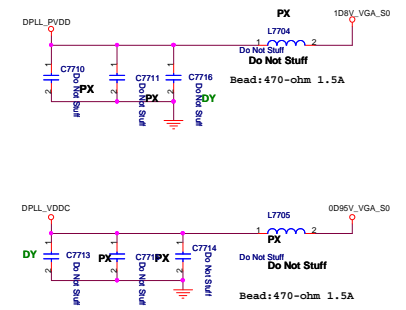
For dual link DVI using DPA AND DPB, DPA\_VDDxx and DPB\_VDDxx can be shared respectively

For dual link DVI using DPC AND DPD, DPC\_VDDxx and DPD\_VDDxx can be shared respectively

For dual link LVDS, DPE\_VDDxx and DPF\_VDDxx can be shared respectively

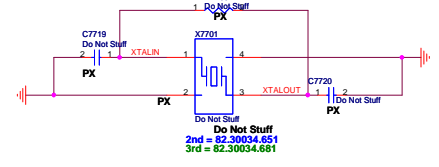


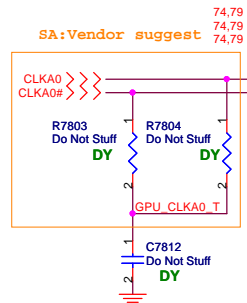
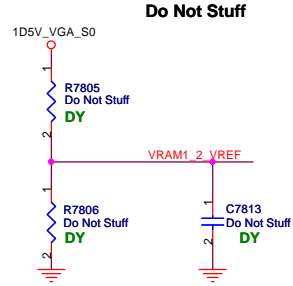
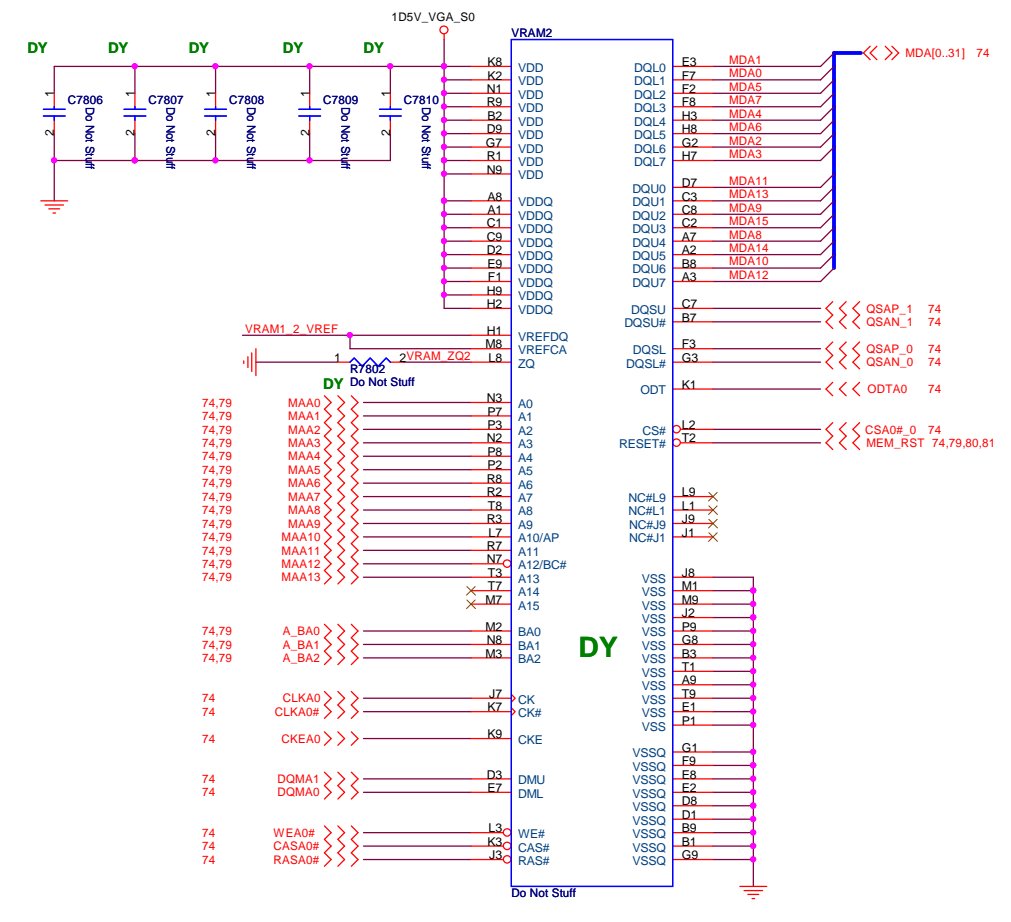
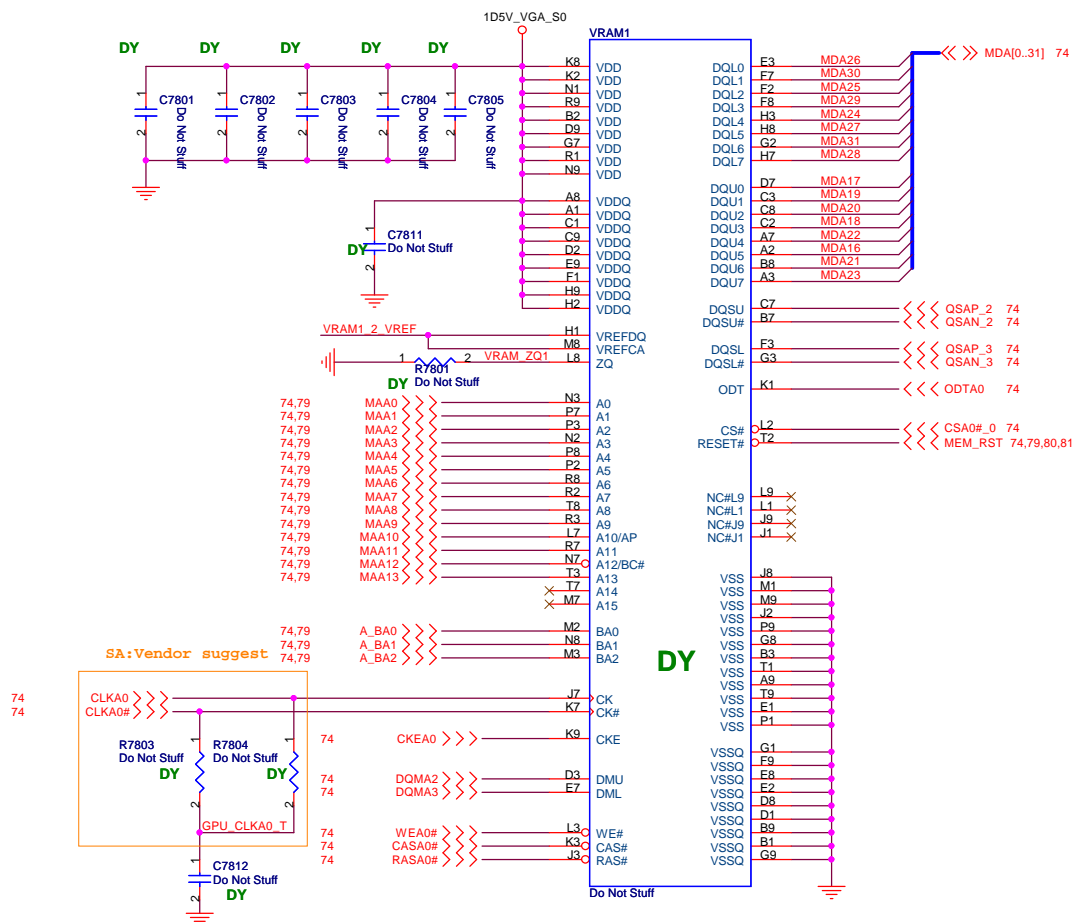
Debug only, for clock observation, if not needed, DNI



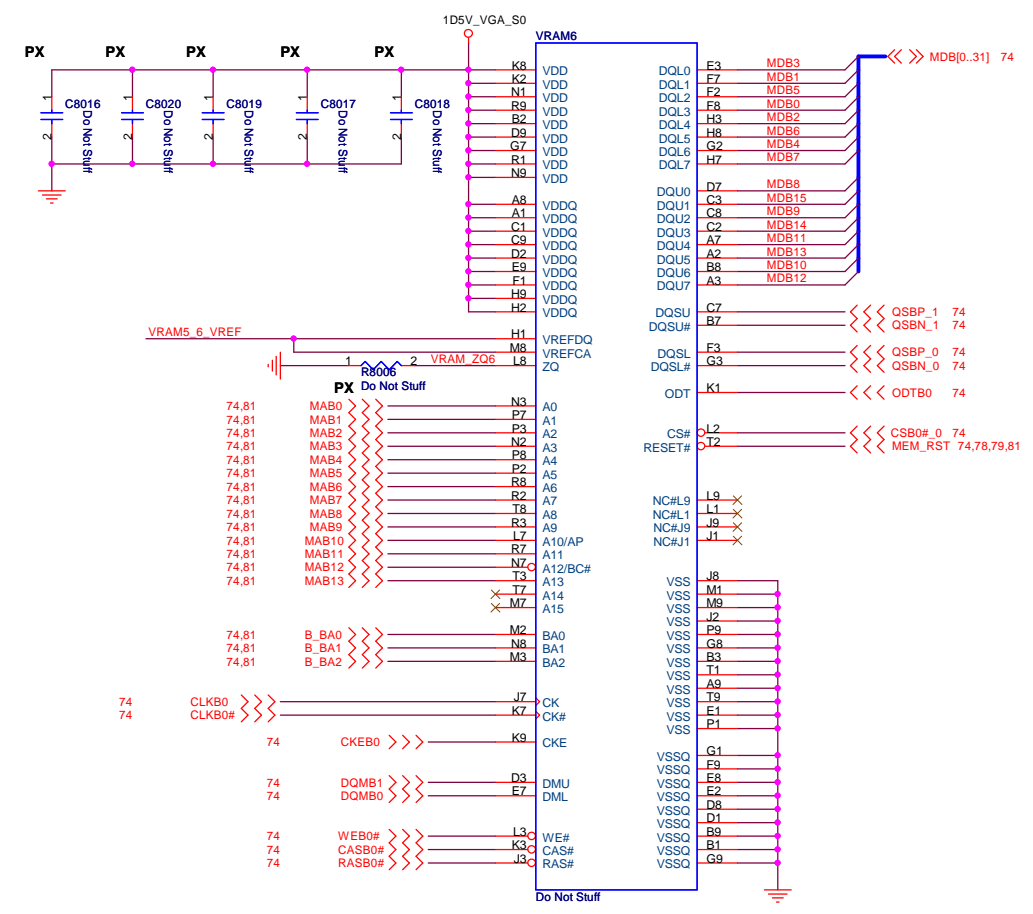
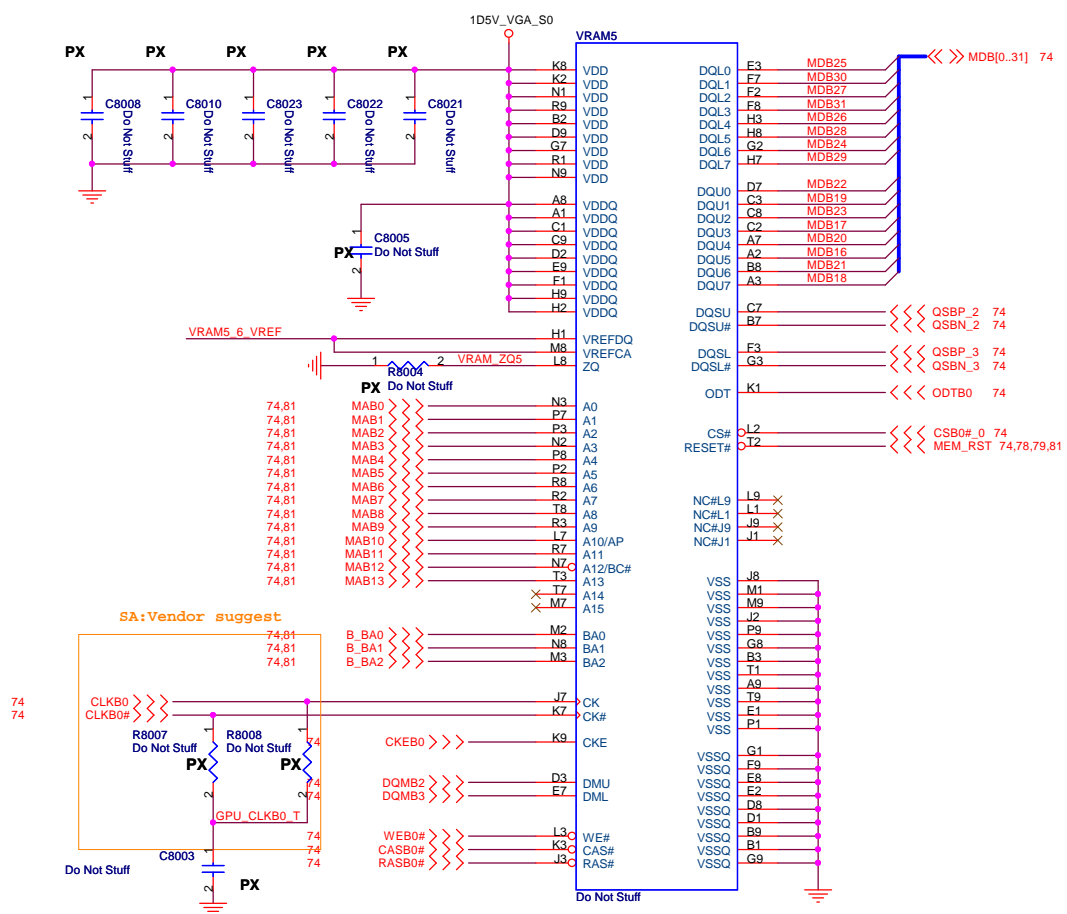
Clock Input Configuration - GDDR3/DDR3

- 27MHz crystal connected to XTALIN or XTALOUT or
- 27MHz (1.8V) oscillator connected to XTALIN or
- 27MHz (3.3V) oscillator connected to XO\_IN (Park, Madison, and Broadway only)





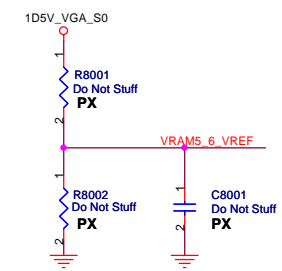




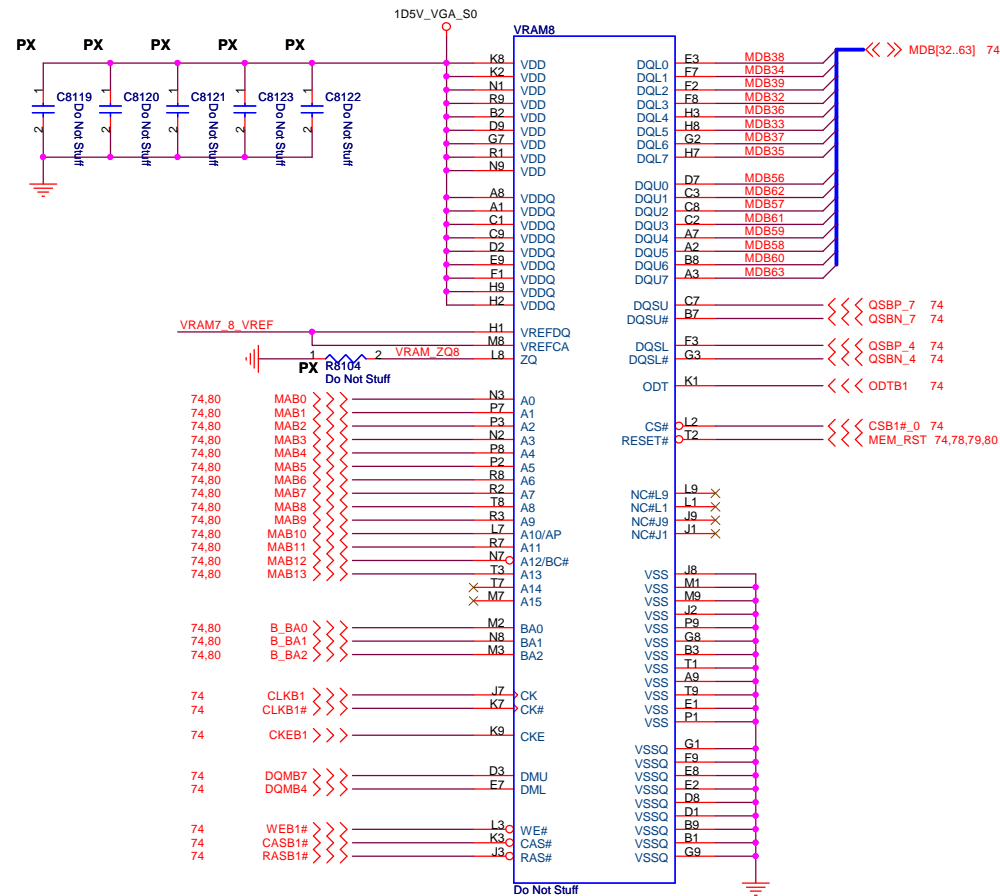
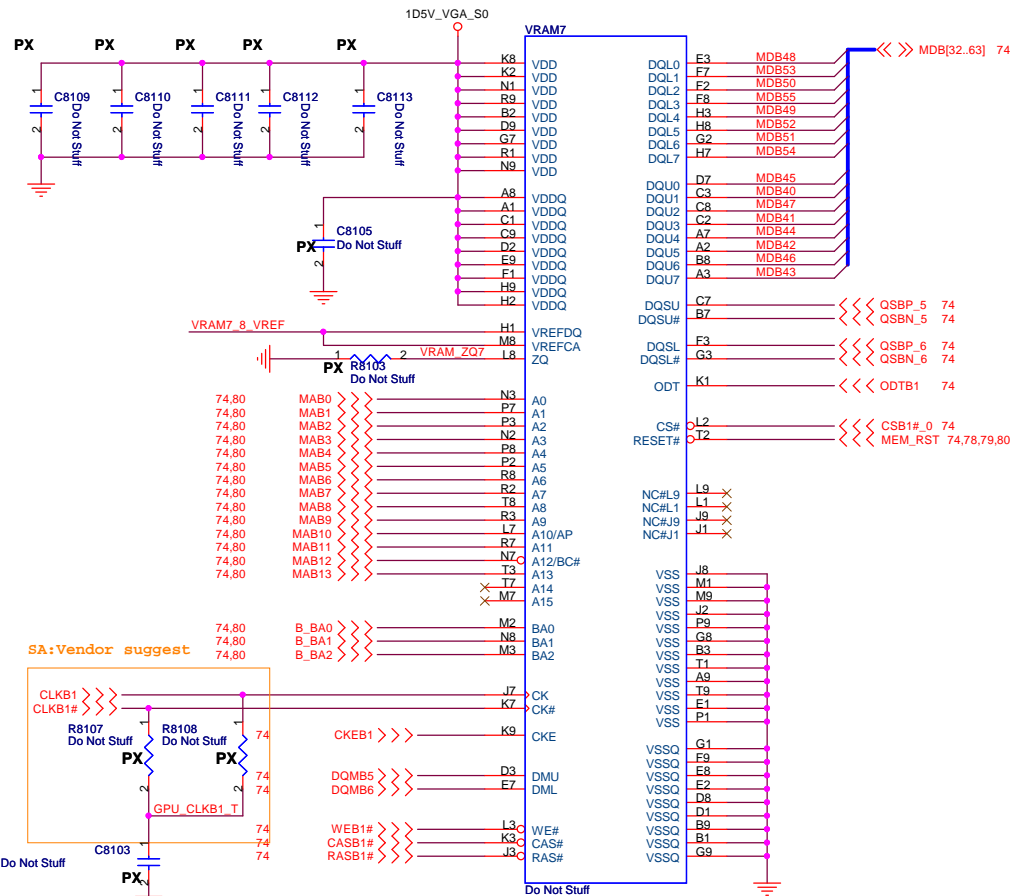
PX  
Do Not Stuff

PX  
Do Not Stuff

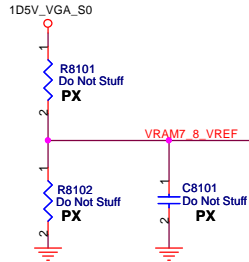
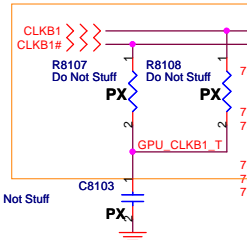
**EG50 VRAM: 72.52G63.C0U (VR.2GB0G.005)**  
**IC VRAM H5TQ2G63DFR-11C FBGA 96P 128M\*16 x4**







SA: Vendor suggest



EG50 VRAM: 72.52G63.C0U (VR.2GB0G.005)  
 IC VRAM H5TQ2G63DFR-11C FBGA 96P 128M\*16 x4

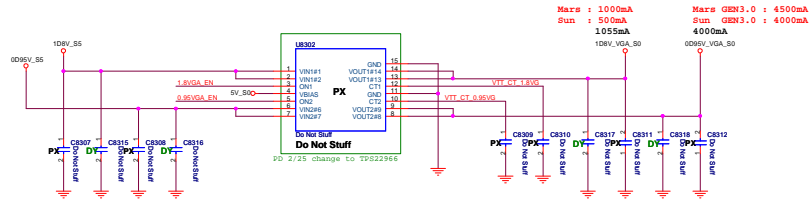
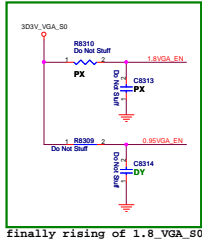
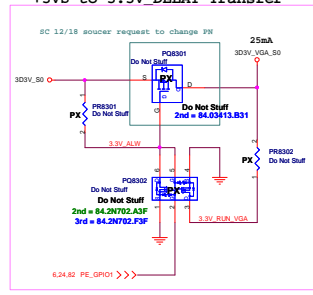




# APL3523 for VGA\_Power

	FE_GPI00	FE_GPI01
dGPU mode	H	H
IGPU	L	L
IGPU with BACO	H	H

## +3VS to 3.3V DELAY Transfer

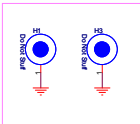


EAE050 KB LMA

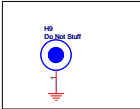
<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai W. Rd., Hsinshih, Taipei Power 231, Taiwan, R.O.C.	
<b>DISCRETE VGA POWER</b>	
<b>KABINI</b>	
Doc. Name	SA
Date	Monday, February 25, 2013
Page	83 of 102

**ZZ.00PAD.2N1**

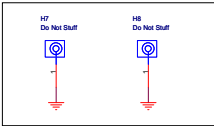
SB 11/14 follow HW for factory issue



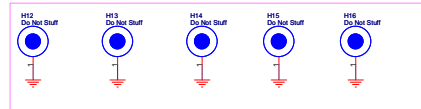
**ZZ.00PAD.D01**



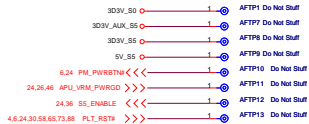
**ZZ.00PAD.E01**



SB 11/20 ZZ.00pad.2T1 for change BKT size



**Check test point**

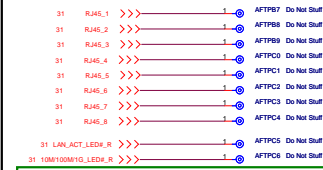


Test Point放在Dimm Door打開可量測處

10/15 follow HW 24.27.61.90\_KBC\_PWRBSTM >>> 1 AFTP91 Do Not Stuff



**EDP + MIC connector**



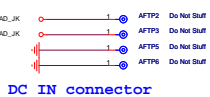
**LAN\_RJ45 connector**



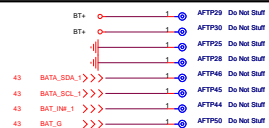
**Card reader connector**



**USBDD connector**



**DC IN connector**



**Battery connector**



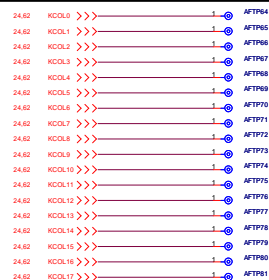
**Speaker connector**



**HP connector**



**FAN connector**



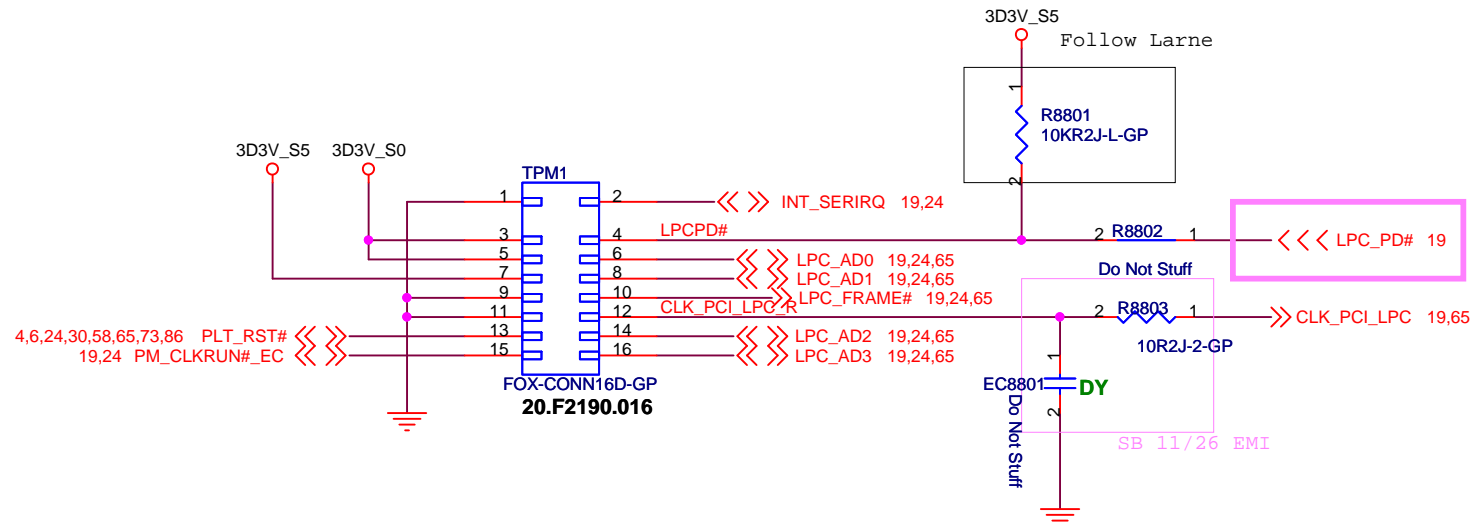
**Normal KB connector**



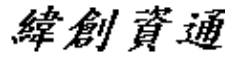
**Touch Pad connector**

EAE050 KB UMA

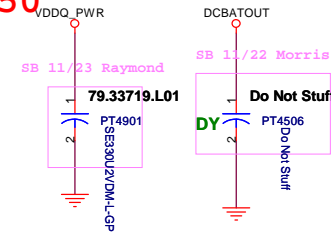
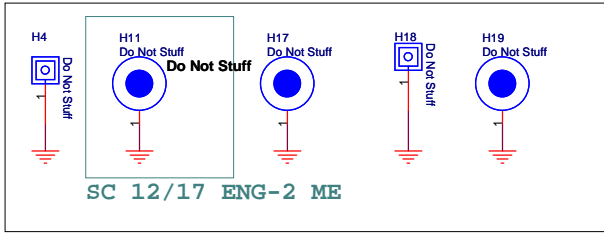
緯創資通 Wistron Corporation  
21F, 8F, 5th, 11th, 12th, 14th, 15th, 16th, 17th, 18th, 19th, 20th, 21st, 22nd, 23rd, 24th, 25th, 26th, 27th, 28th, 29th, 30th, 31st, 32nd, 33rd, 34th, 35th, 36th, 37th, 38th, 39th, 40th, 41st, 42nd, 43rd, 44th, 45th, 46th, 47th, 48th, 49th, 50th, 51st, 52nd, 53rd, 54th, 55th, 56th, 57th, 58th, 59th, 60th, 61st, 62nd, 63rd, 64th, 65th, 66th, 67th, 68th, 69th, 70th, 71st, 72nd, 73rd, 74th, 75th, 76th, 77th, 78th, 79th, 80th, 81st, 82nd, 83rd, 84th, 85th, 86th, 87th, 88th, 89th, 90th, 91st, 92nd, 93rd, 94th, 95th, 96th, 97th, 98th, 99th, 100th



EAE50 KB UMA

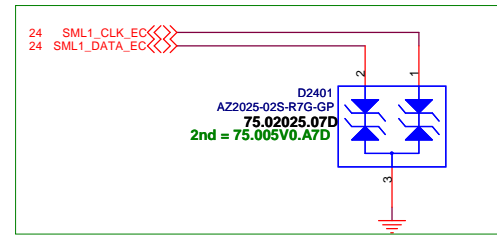
 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b> TPM	
<b>Size</b>	<b>Project Name</b> KABINI
<b>Date</b> Monday, February 04, 2013	<b>Rev</b> SA
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# H4 & H11 & H17 & H18 & H19 for EG50



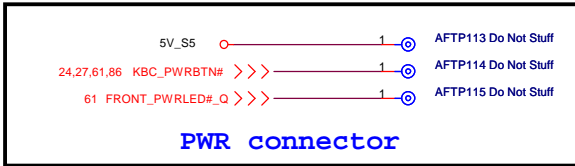
SB 11/23 3mm high limit in EG50

PD 01/31 Different Net name in 14" & 15" for placement

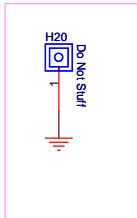


24,62,86	KCOL0	>>>
24,62,86	KCOL1	>>>
24,62,86	KCOL2	>>>
24,62,86	KCOL3	>>>
24,62,86	KCOL4	>>>
24,62,86	KCOL5	>>>
24,62,86	KCOL6	>>>
24,62,86	KCOL7	>>>
24,62,86	KCOL8	>>>
24,62,86	KCOL9	>>>
24,62,86	KCOL10	>>>
24,62,86	KCOL11	>>>
24,62,86	KCOL12	>>>
24,62,86	KCOL13	>>>
24,62,86	KCOL14	>>>
24,62,86	KCOL15	>>>
24,62,86	KCOL16	>>>
24,62,86	KCOL17	>>>
24,62,86	KROW0	>>>
24,62,86	KROW1	>>>
24,62,86	KROW2	>>>
24,62,86	KROW3	>>>
24,62,86	KROW4	>>>
24,62,86	KROW5	>>>
24,62,86	KROW6	>>>
24,62,86	KROW7	>>>

# PWRBD AFTP for EG50

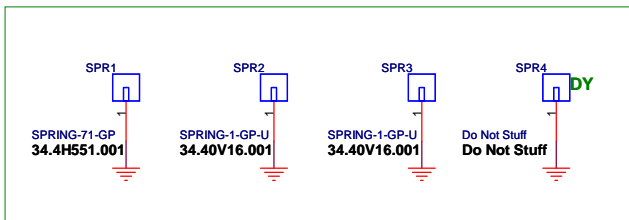


# ZZ.00PAD.571

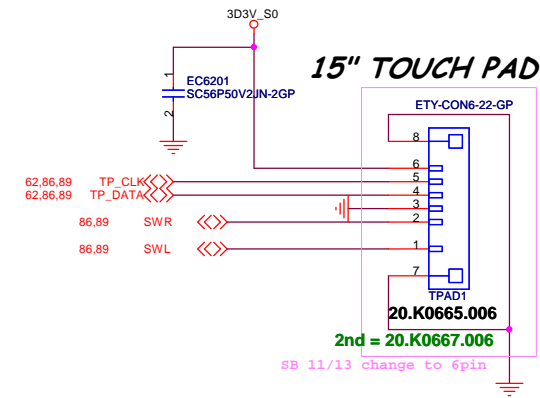


SB 11/20 location same with 14" H2

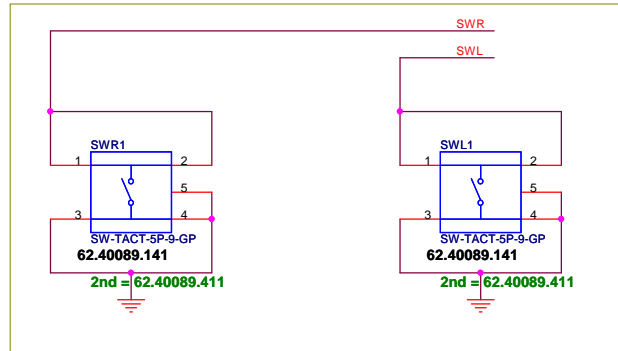
# PD 1/23 EMI Jen



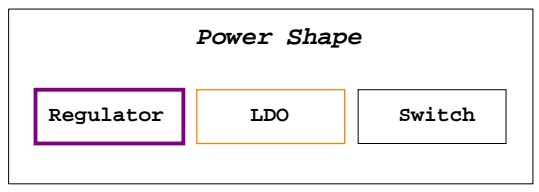
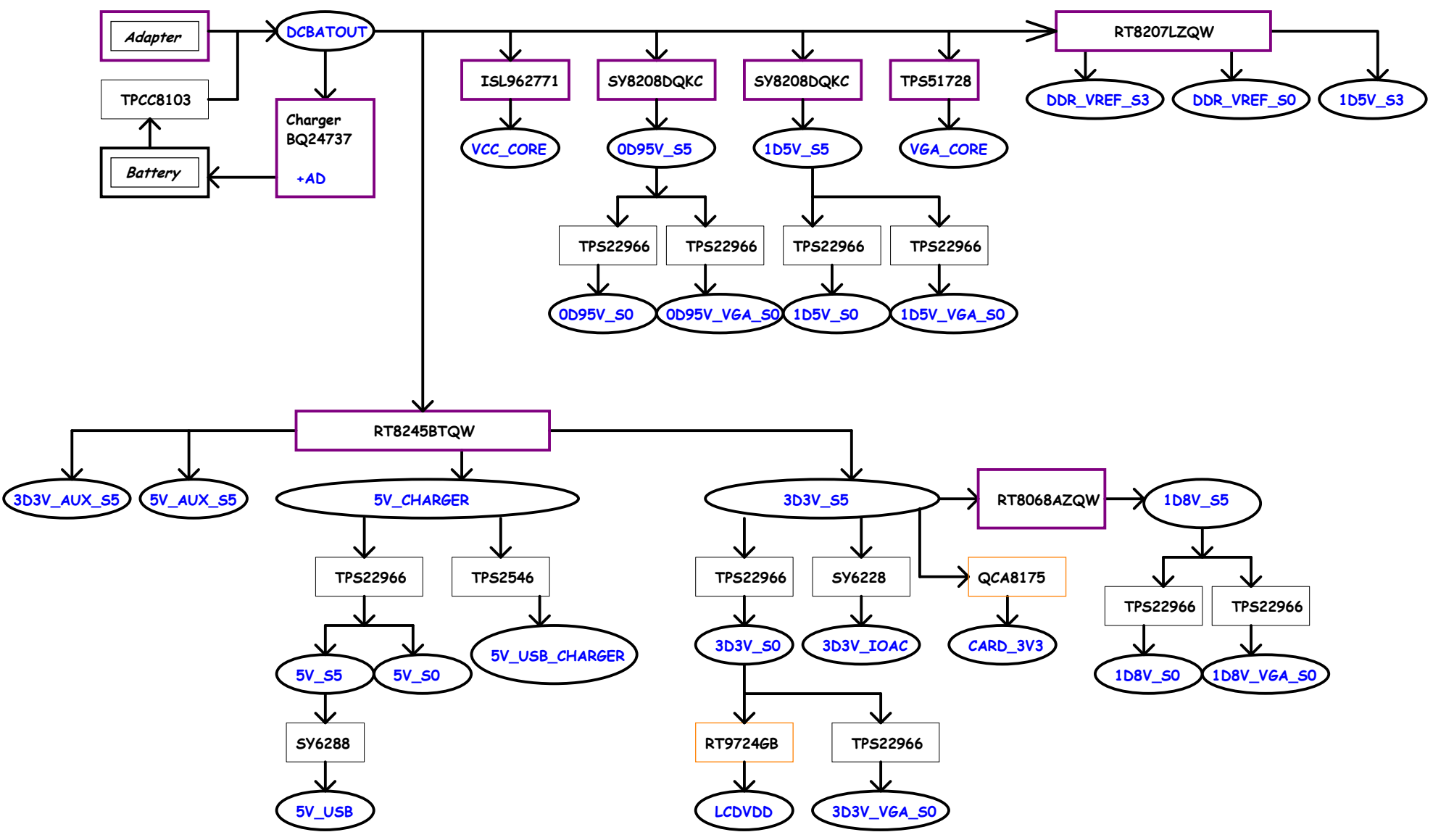
# 15" TOUCH PAD



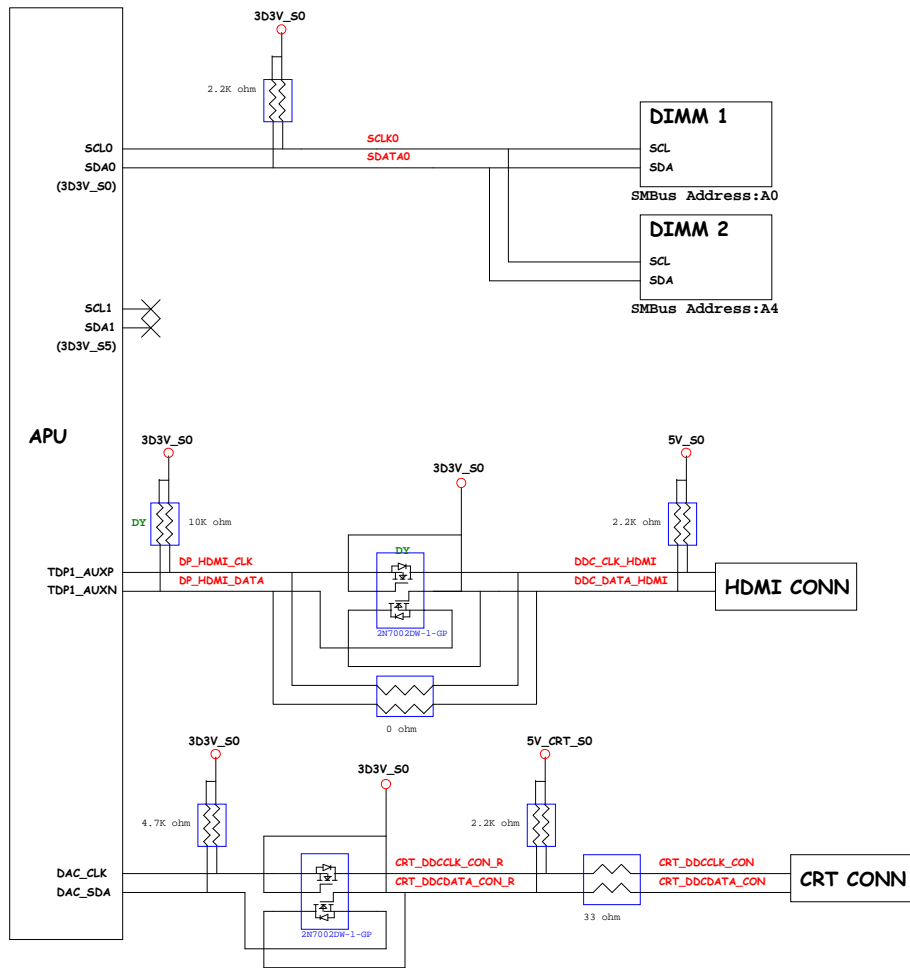
For AFTE



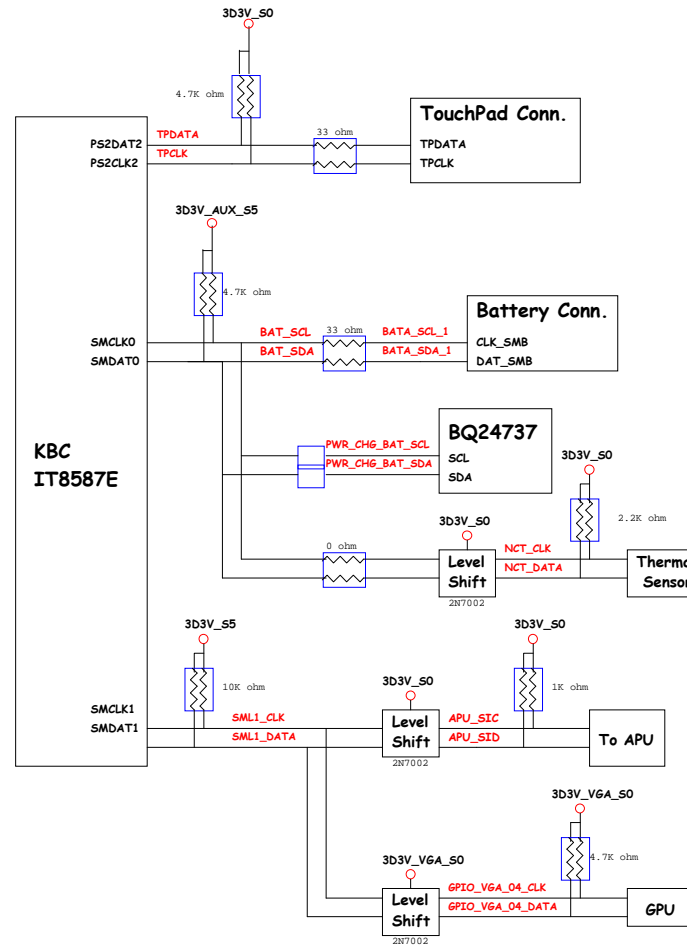
PD 1/21  
SWL1 / SWR1 1st change to 62.40089.141, 2nd change to 62.40089.411 ,  
because 160kg change to 100kg.



# SMBus Block Diagram

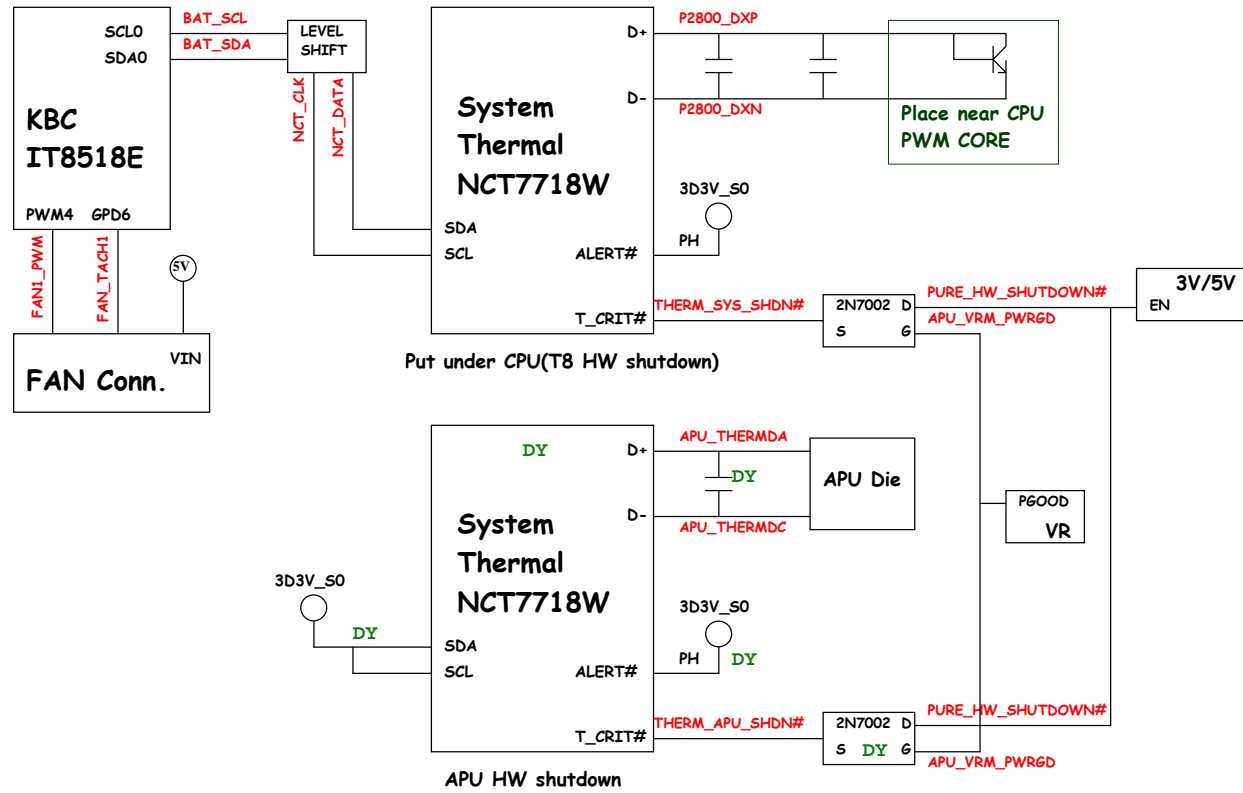


# KBC SMBus Block Diagram

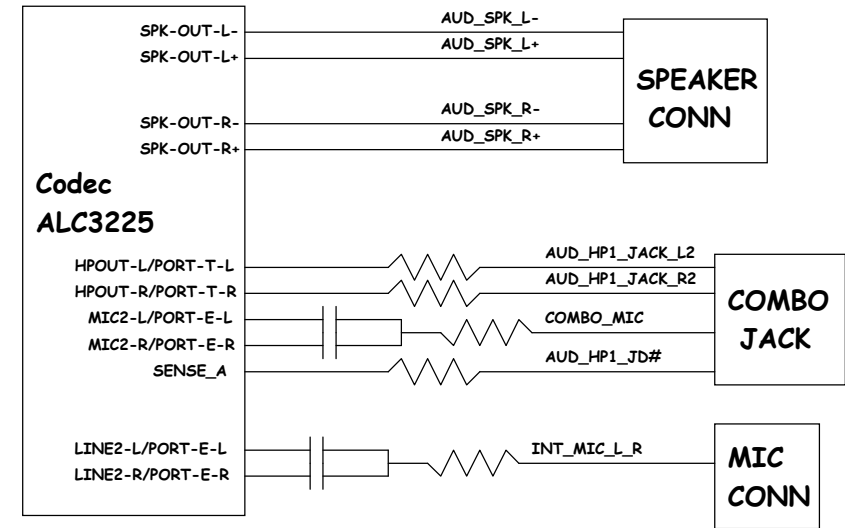


EAE650 KB UIM

# Thermal Block Diagram



# Audio Block Diagram



EAEG50 KB UMA