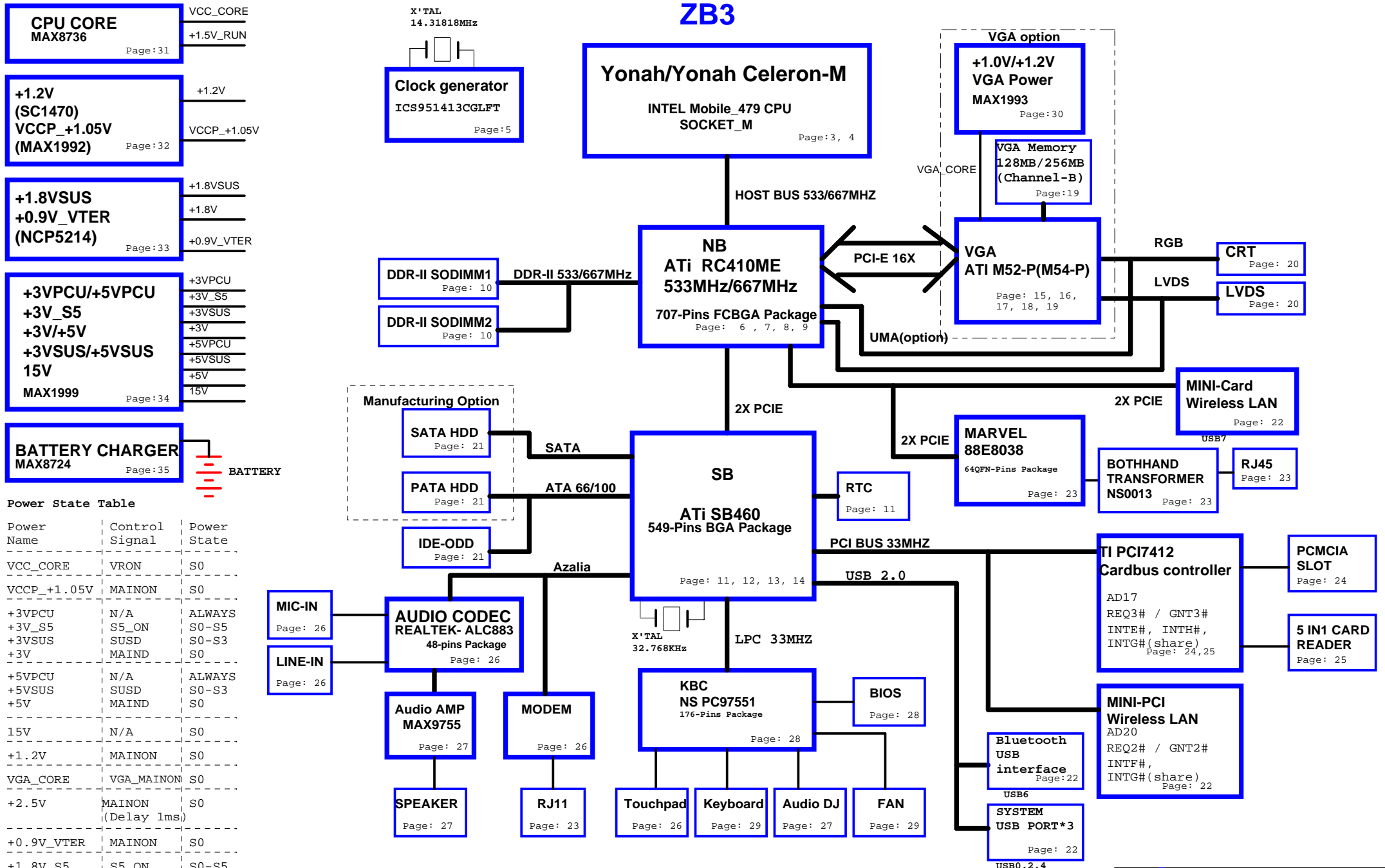


# ZB3



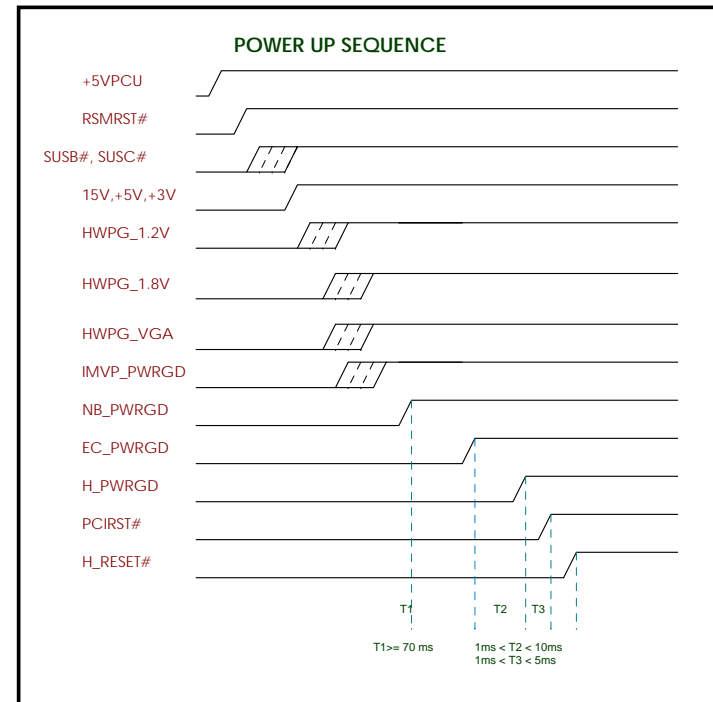
**Power State Table**

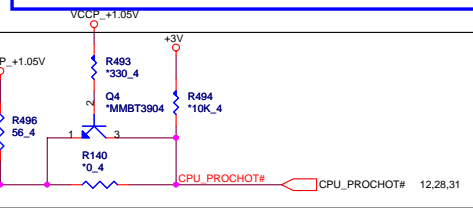
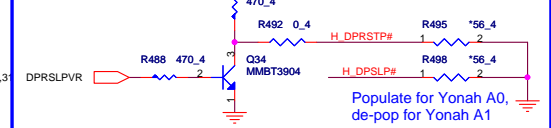
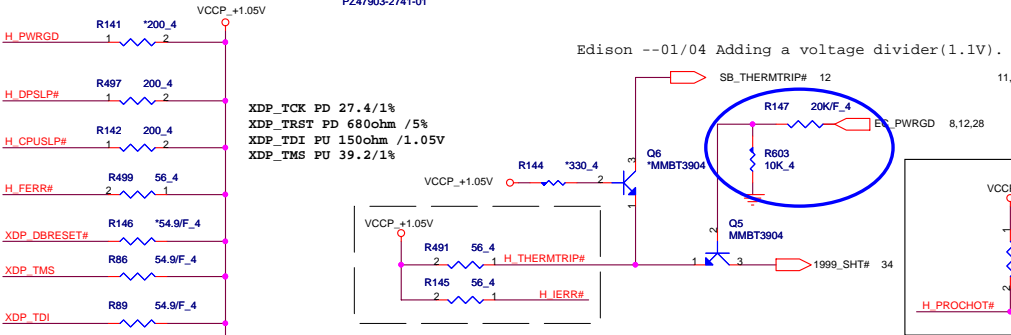
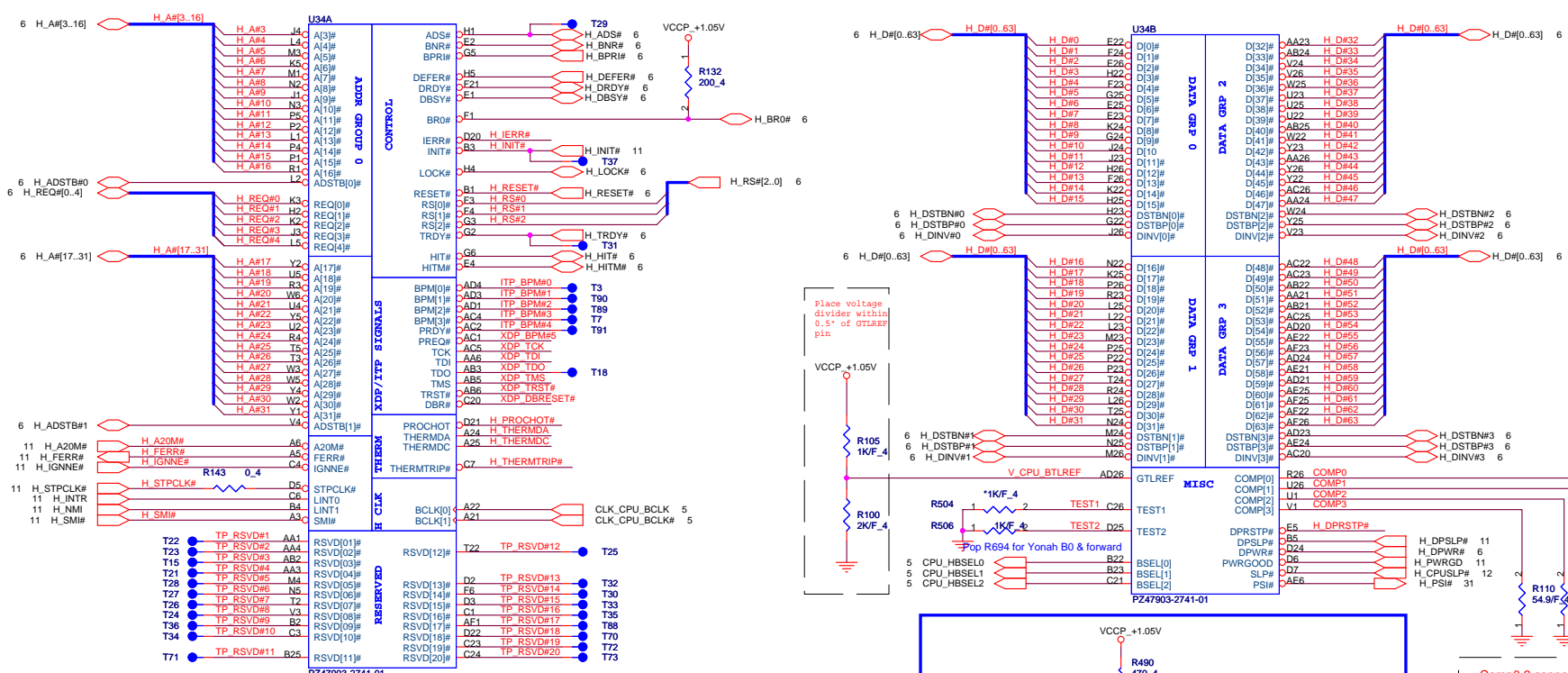
Power Name	Control Signal	Power State
VCC_CORE	VRON	S0
VCCP_+1.05V	MAINON	S0
+3VPCU	N/A	ALWAYS
+3V_S5	S5_ON	S0-S5
+3VSUS	SUSD	S0-S3
+3V	MAIND	S0
+5VPCU	N/A	ALWAYS
+5VSUS	SUSD	S0-S3
+5V	MAIND	S0
15V	N/A	S0
+1.2V	MAINON	S0
VGA_CORE	VGA_MAINON	S0
+2.5V	MAINON (Delay 1ms)	S0
+0.9V_VTER	MAINON	S0
+1.8V_S5	S5_ON	S0-S5
+1.8VSUS	SUSON	S0-S3
+1.8V	MAIND	S0
+1.5V_RUN	MAINON	S0

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 Page 20 : CRT & LVDS  
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 Page 23 : LAN PCI-E EE88038  
 Page 24 : PCI7412-PCMCIA CONTROLLE  
 Page 25 : PCI7412-CARD READER  
 Page 26 : CODEC T/P MIC/LINE-IN/OUT-ALC883  
 Page 27 : AUDIO AMP&LINE OUT  
 Page 28 : PC97551 & FLASH  
 Page 29 : FAN,SWITCH,LED,KB  
 Page 30 : VGA CORE 1.0V/1.2V  
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 Page 32 : +VCCP(1.05V)& 1.2V(NB PWR  
 Page 33 : DDRII PWR\_1.8VSUS-VTERM  
 Page 34 : SYSTEM +5V& +3V MAX1999A  
 Page 35 : BATTERY CHARGER

	POWER	VOLTAGE	ACTIVE SCOPE	PAGE
SYSTEM	15V	15V	S0	33
	+5V	+5V	S0	33
	+3V	+3.3V	S0	33
	+5VPCU	+5V	ALWAYS	33
	+3VPCU	+3.3V	ALWAYS	33
	+5VSUS	+5V	S0-S3	33
	+3VSUS	+3.3V	S0-S3	33
	+3V_S5	+3.3V	S0-S5	33
CPU	VCC_CORE	VID[0..6]	S0	31
	VCCP_+1.05V	+1.05V	S0	31
	+1.5V_RUN	+1.5V	S0	31
RC410ME NB	VCCP_+1.05V	+1.05V	S0	31
	+1.8V	+1.8V	S0	33
	+1.8VSUS	+1.8V	S0-S3	33
	+1.2V	+1.2V	S0	32
	+3V	+3.3V	S0	33
	+1.2V_PCIE	+1.2V	S0	9
	+1.2V_CORE	+1.2V	S0	9
	VDD18	+1.8V	S0	9
	VDDA18	+1.8V	S0	9
	NB_VDDR	+3.3V	S0	8
	AVDD_NB	+3.3V	S0	8
	AVDDQ	+1.8V	S0	8
	PLVDD	+1.8V	S0	8
	NB_LPVDD	+1.8V	S0	8
	NB_LVDDR18A	+1.8V	S0	8
	SB460 SB	+3V	+3.3V	S0
+1.8V		+1.8V	S0	33
+3V_S5		+3.3V	S0-S5	33
+1.8V_S5		+1.8V	S0-S5	30
VCCP_+1.05V		+1.05V	S0	31
+1.8VUSB_PHY		+1.8V	S0-S5	13
V5_REF		+5V	S0	13
+1.8V_ATA		+1.8V	Reserve	13
PLLVDV_ATA		+1.8V	Reserve	13
XTLVDD_ATA		+1.8V	Reserve	13
PCIE_PVDD		+1.8V	S0	11
PCIE_VDDR		+1.8V	S0	11
AVDD_USB		+3VSUS	S0-S3	12
+3.3V_AVDDC		+3.3V	S0-S3	12
VCCRTC		+3.0V	--	11
VDDQ_3V		+3.3V	S0	13
VDD_1.8V		+1.8V	S0	13
SB_S5_3V		+3.3V	S0-S5	13
SB_S5_1.8V	+1.8V	S0-S5	13	
AVDD_CK_1.8V	+1.8V	S0	13	
DDR2	+1.8V	+1.8V	S0	33
	+1.8VSUS	+1.8V	S0-S3	10
	+0.9V_VTER	+0.9V	S0	10

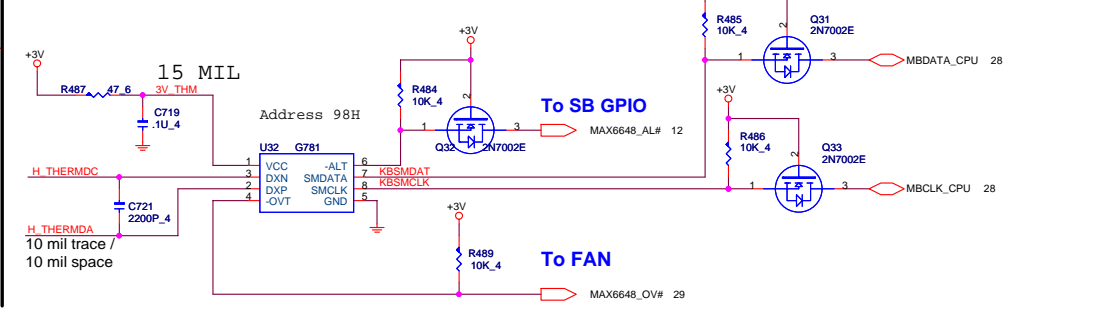




Comp0,2 connect with Zo=27.4ohm.  
Comp1,3 connect with Zo=55ohm,  
make these trace length shorter than 0.5".



### CPU H/W MONITOR

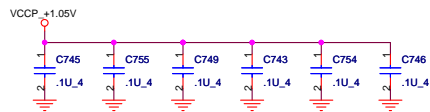
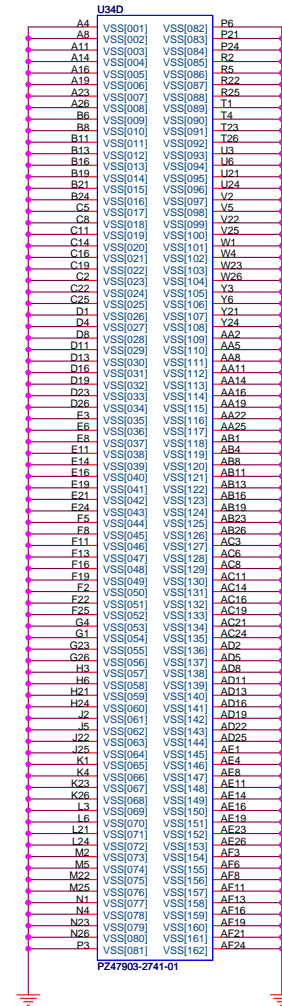
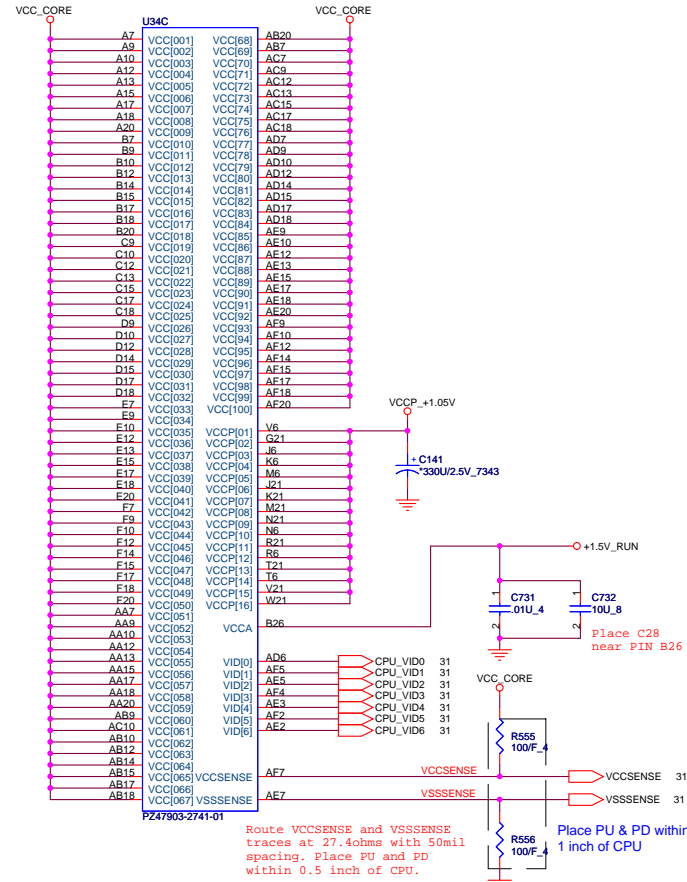
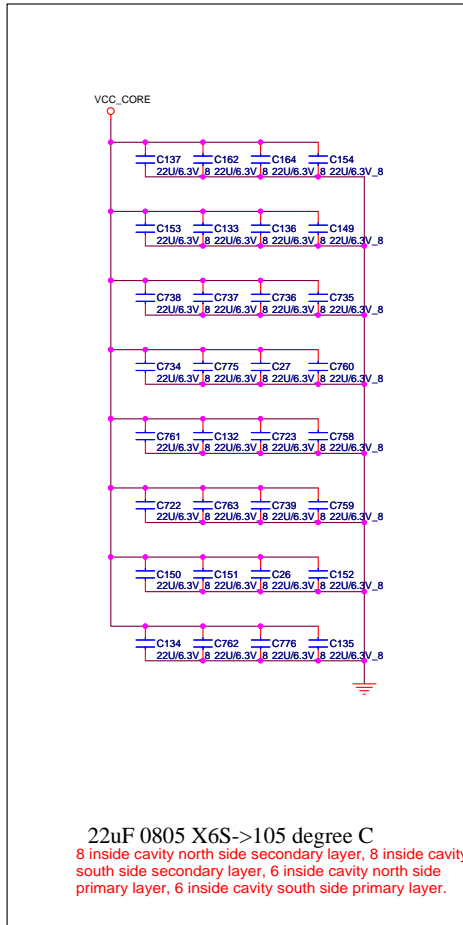


Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the CPU
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the CPU
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the CPU
TCK	27 ohm +/- 5%	GND	Within 2.0" of the CPU
TDO	Open	VTT	Within 2.0" of the CPU
ITP_EN	R366 Depop	+3VTRUN	Close to CK410M Pin8

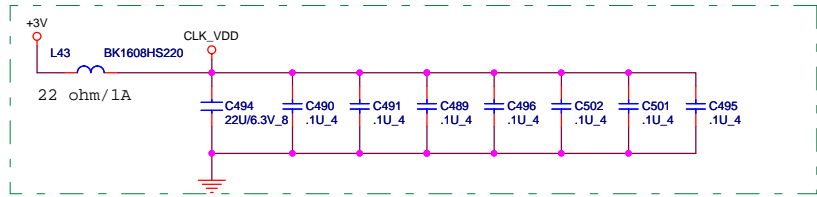
**PROJECT : ZB3**  
**Quanta Computer Inc.**

Size: \_\_\_\_\_ Document Number: **Yonah CPU(HOST Bus)-1** Rev: 1A  
Date: Monday, April 03, 2006 Sheet: 3 of 37

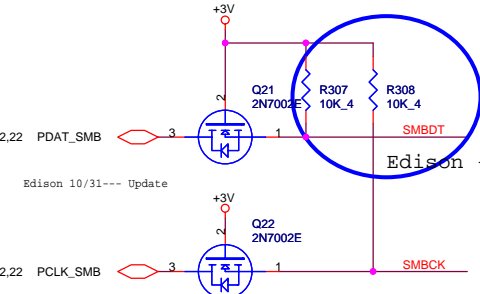
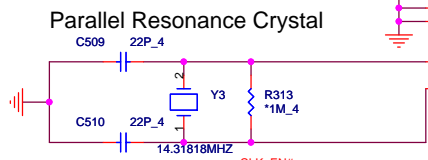
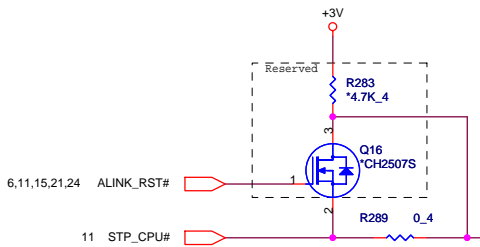
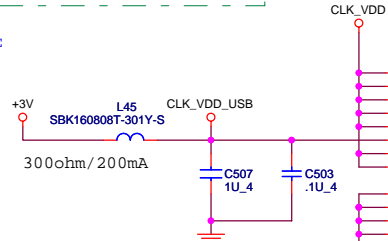




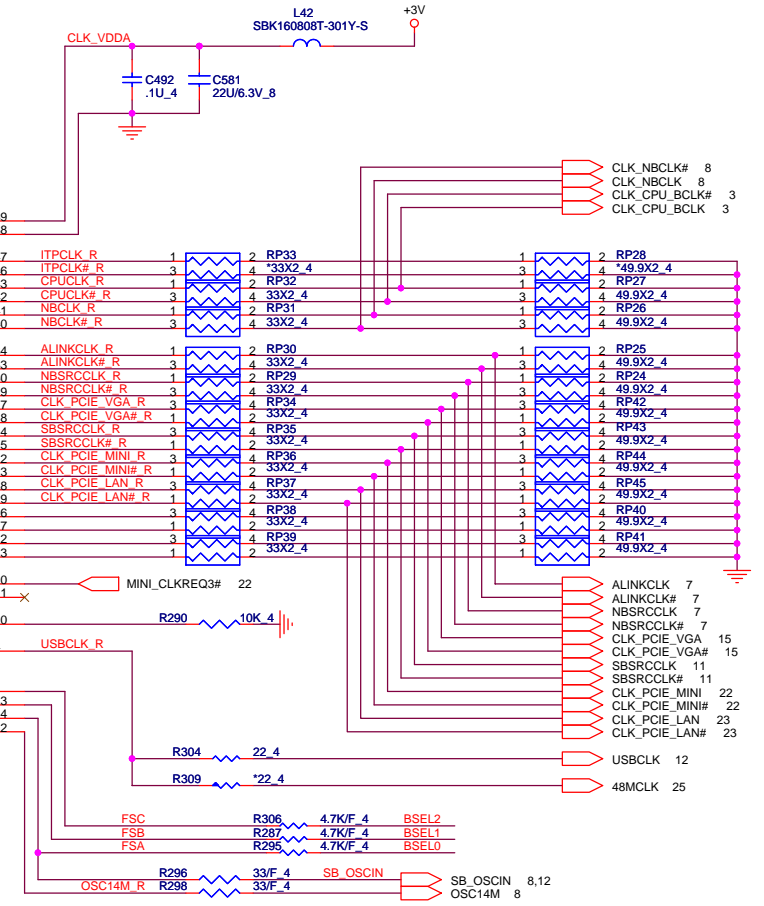
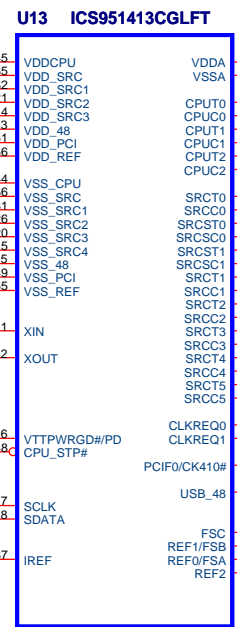
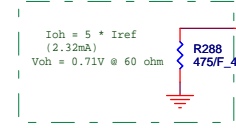
CPU



- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE AS U16 AS POSSIBLE
- 2- ROUTE ALL CPUCLK/#, NBCLK/# AND ITPCLK/# AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U16 POWER PIN



Edison -- 01/03 Modify



### CK410 FREQUENCY SELECT TABLE(MHZ)

FSC	FSB	FSA	CPU	SRC	PCI	REF
BSEL2	BSEL1	BSEL0				
1	0	1	100	100	33	14.31
0	0	1	133	100	33	14.31
0	1	1	166	100	33	14.31
0	0	0	200	100	33	14.31
0	0	0	266	100	33	14.31
1	0	0	333	100	33	14.31
1	1	0	400	100	33	14.31
1	1	1	Resv	100	33	14.31

CY28RS400 and ICS951413 are fully pin compatible and can be interchanged without any hardware modification.

# CLK

**PROJECT : ZB3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
<b>CLOCK GENERATOR</b>		1A
Date:	Monday, April 03, 2006	Sheet 5 of 37





# NB-2

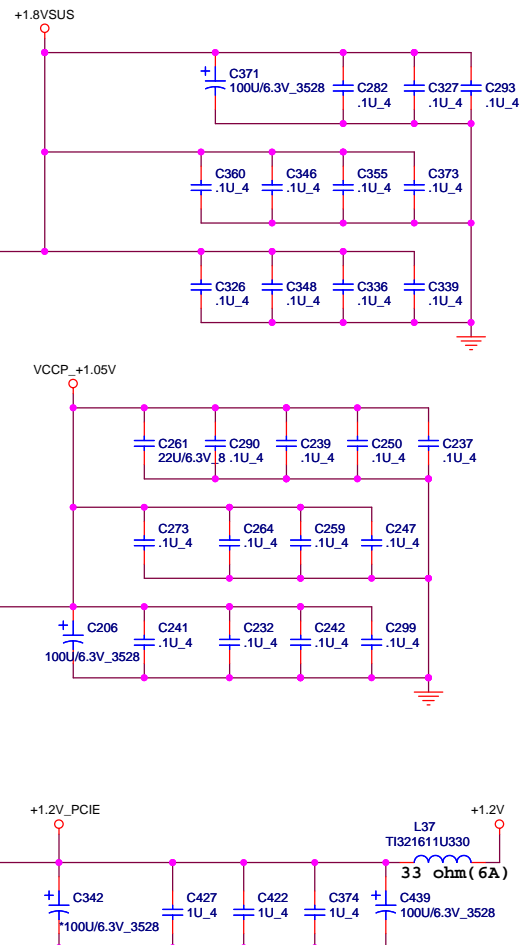
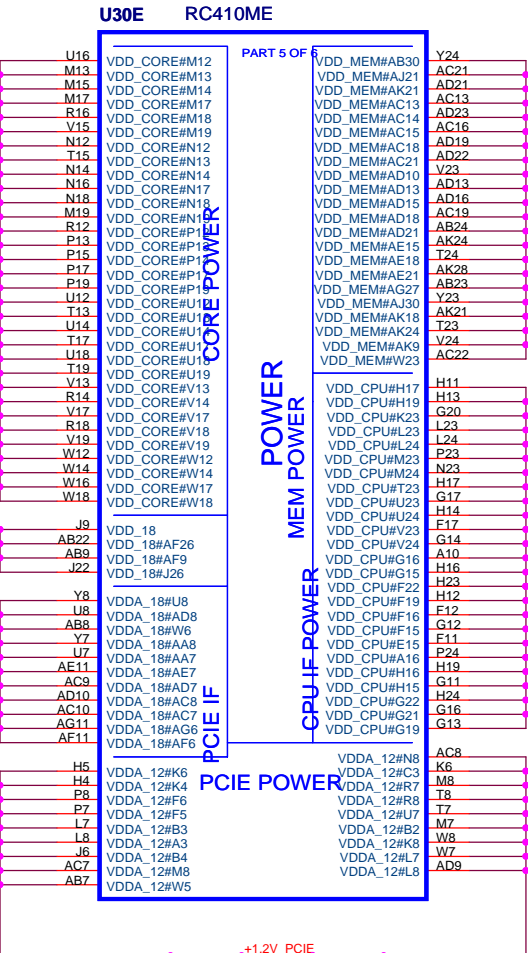
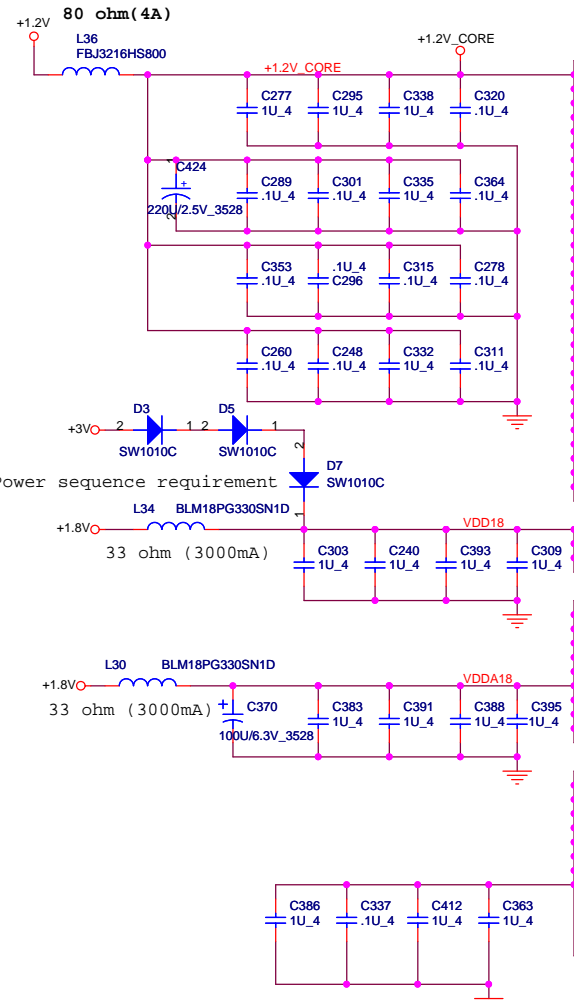
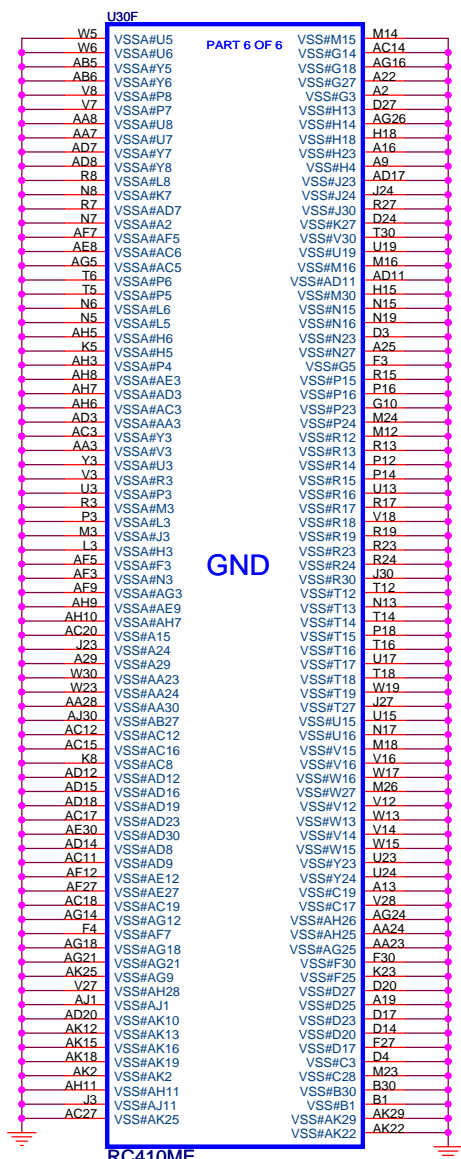


**PROJECT : ZB3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>RC410MB-PCIE LINK I/F</b>	1A
Date:	Monday, April 03, 2006	Sheet 7 of 37





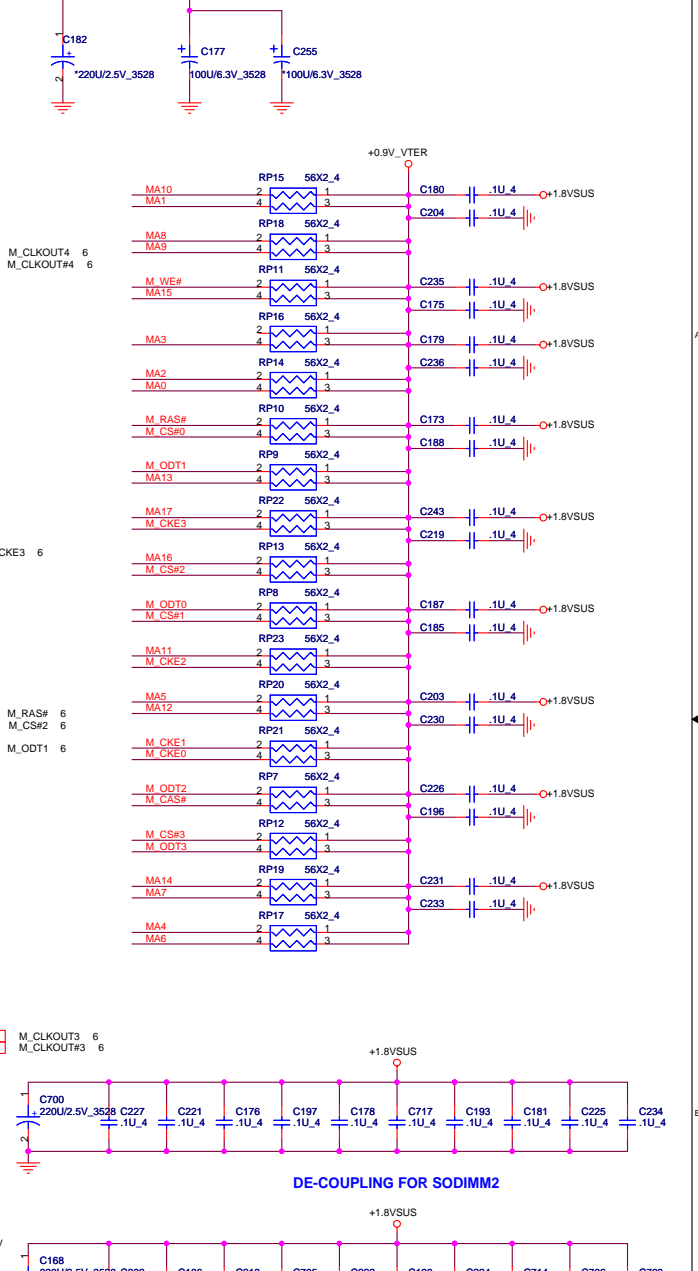
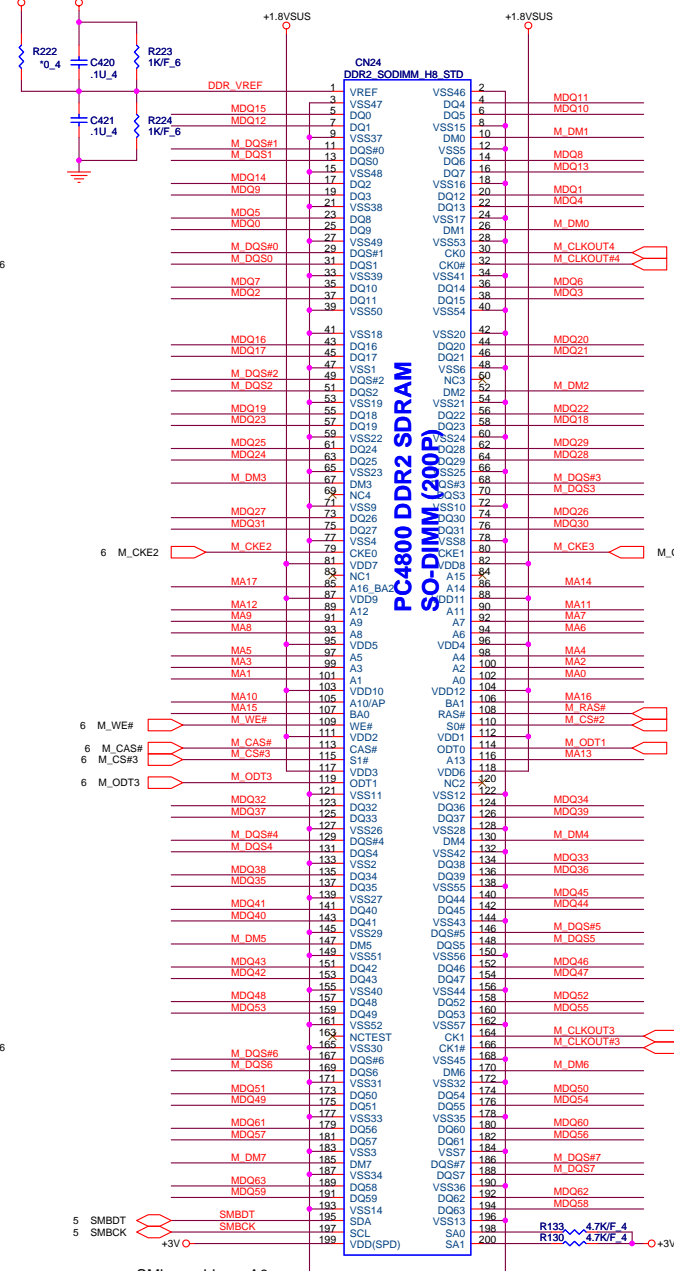
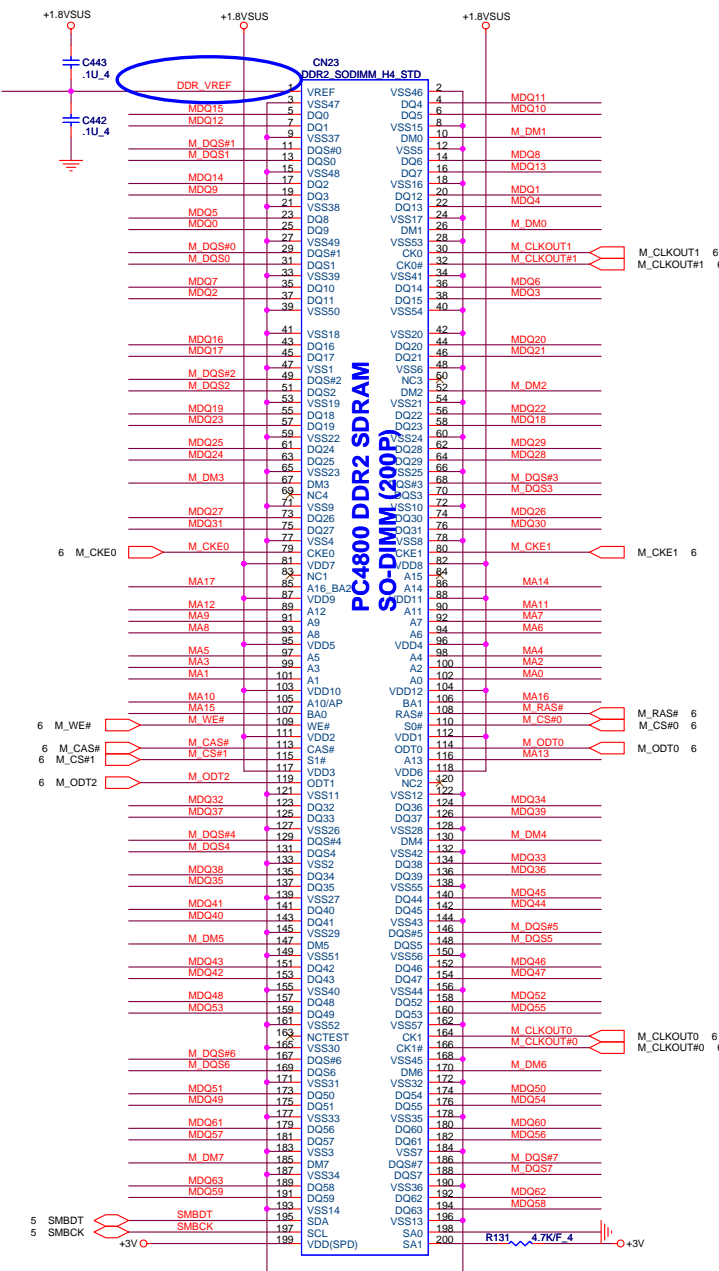


**NB-4**

**PROJECT : ZB3**

**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>RC410MB-POWER</b>	<b>1A</b>
Date:	Monday, April 03, 2006	Sheet 9 of 37

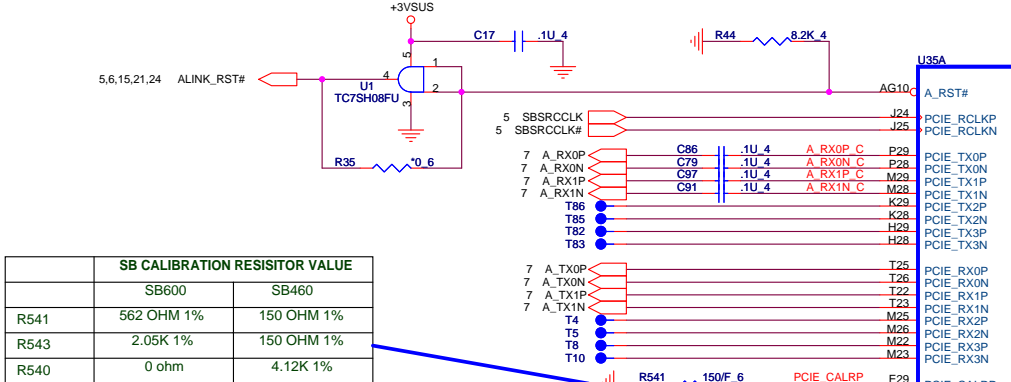


# DDR II

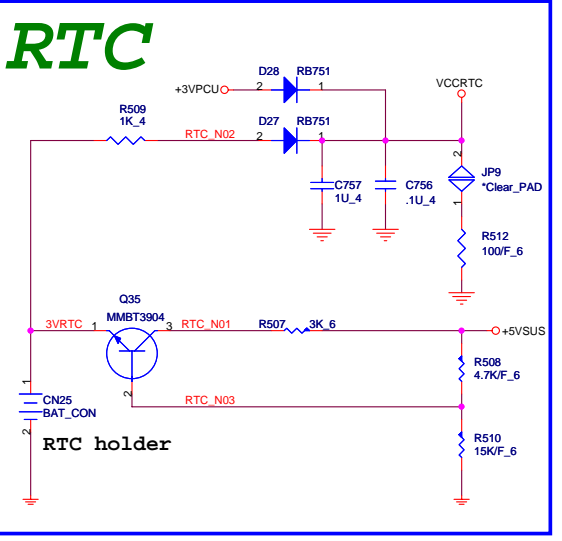
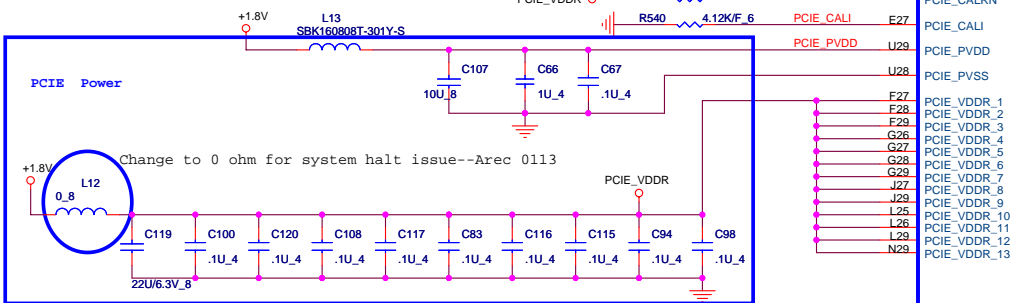
- MDO[63..0] MDO[63..0] 6
- MA[17..0] MA[17..0] 6
- M\_DM[7..0] M\_DM[7..0] 6
- M\_DQS[7..0] M\_DQS[7..0] 6
- M\_DQS#[7..0] M\_DQS#[7..0] 6

**PROJECT : ZB3**  
**Quanta Computer Inc.**

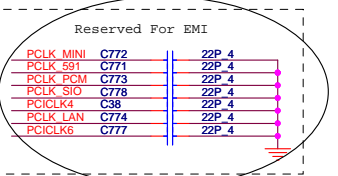
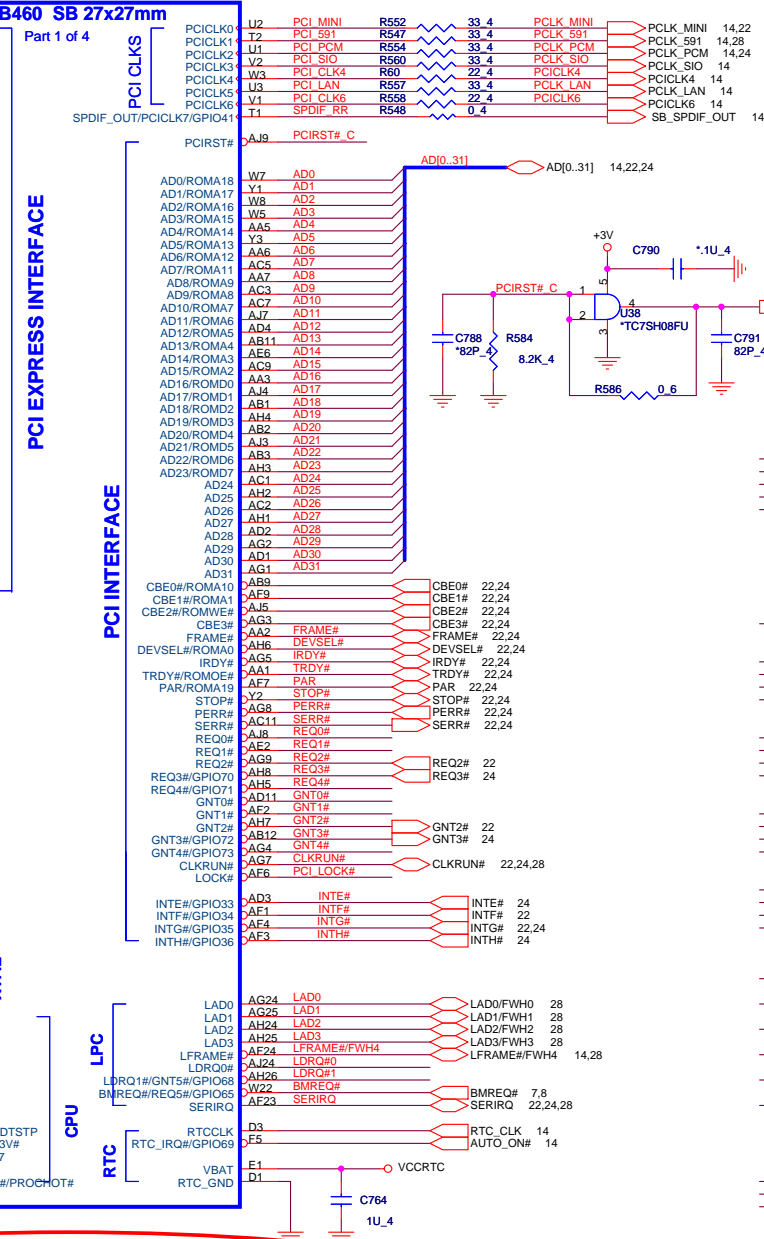
Size: Document Number: **DDR2 SO-DIMM** Rev: 1A  
 Date: Monday, April 03, 2006 Sheet: 10 of 37



SB CALIBRATION RESISTOR VALUE		
	SB600	SB460
R541	562 OHM 1%	150 OHM 1%
R543	2.05K 1%	150 OHM 1%
R540	0 ohm	4.12K 1%

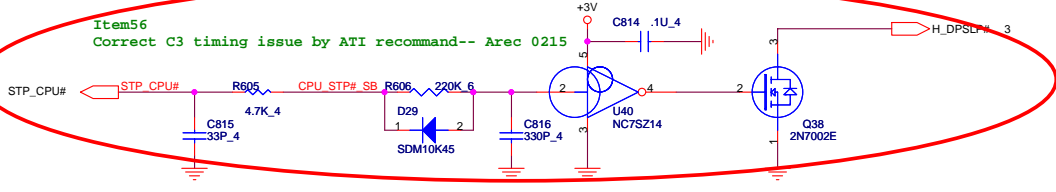
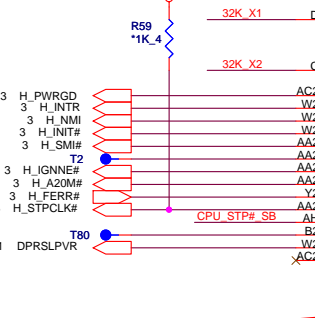
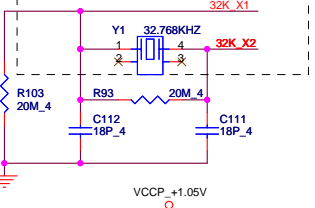


**SB-1**



Edison -- Feb/27 -- The EMI recommend to install decoupling capas for the PCI Clock.  
Richard 3/8 -- From 33P\_4 Change to 22P\_4

ATI Recommend  
Vendor: NSK  
Part Number: NXG 32.768KAE12FUD 16 PPM!



**PROJECT : ZB3**  
**Quanta Computer Inc.**

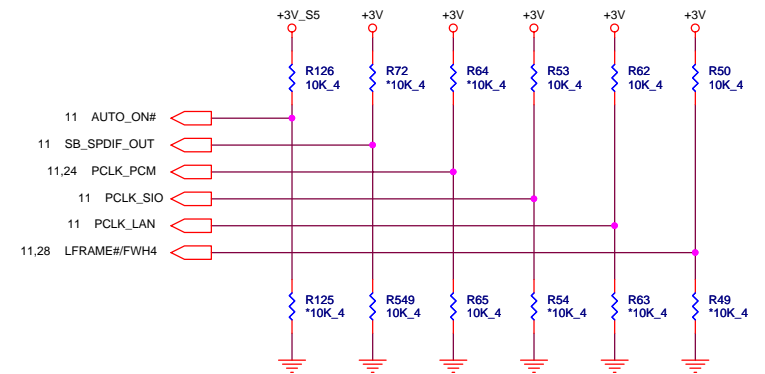
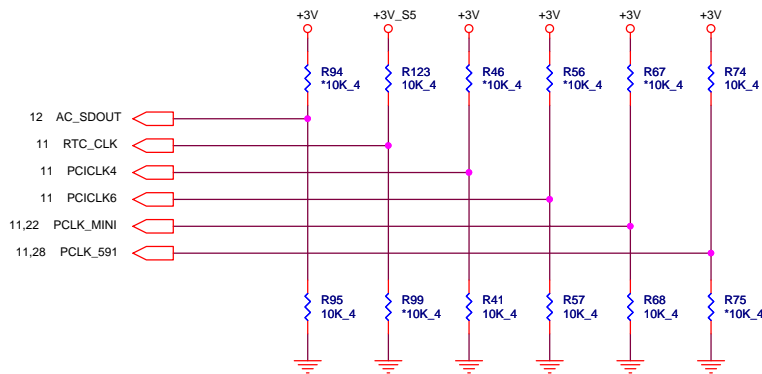
Size: \_\_\_\_\_ Document Number: **SB450M PCIE/PCI/CPU/LPC I/F** Rev: 1A  
 Custort: \_\_\_\_\_  
 Date: Monday, April 03, 2006 Sheet 11 of 37







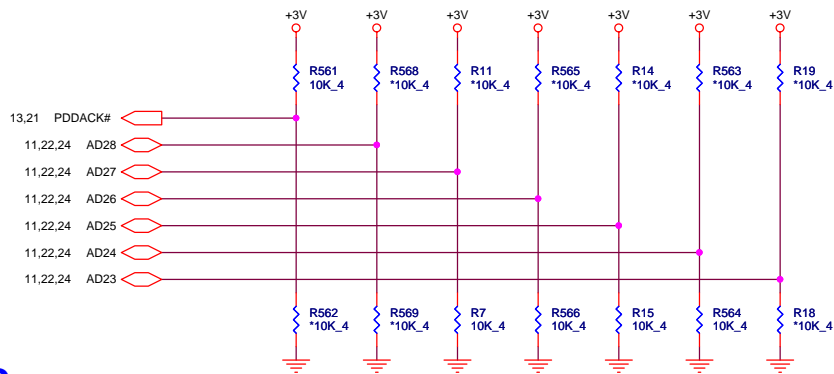
# REQUIRED STRAPS



	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCLK_MINI	PCLK_591
<b>PULL HIGH</b>	USE DEBUG STRAPS <i>DEFAULT</i>	INTERNAL RTC <i>DEFAULT</i>	USE INT. PLL48	CPU IF=K8	PCI_CLK0	PCI_CLK1
<b>PULL LOW</b>	IGNORE DEBUG STRAPS <i>DEFAULT</i>	EXTERNAL RTC	USE EXT. 48MHZ <i>DEFAULT</i>	CPU IF=P4 <i>DEFAULT</i>	ROM TYPE: H, H = PCI ROM H, L = LPC TYPE I ROM L, H = LPC TYPE II ROM <i>DEFAULT</i> L, L = FWH ROM NOTE: FOR SB460, PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]	

	AUTO_ON#	SB_SPDIF_OUT	PCLK_PCM	PCLK_SIO	PCLK_LAN	LFRAME#
<b>PULL HIGH</b>	ACPWON <i>DEFAULT</i>	SPDIF_OUT	PCI_CLK2 <i>NOT SUPPORTED</i>	PCI_CLK3 <i>DEFAULT</i>	PCI_CLK5 <i>DEFAULT</i>	LFRAME# <i>DEFAULT</i>
<b>PULL LOW</b>	AUTO PWR ON	SIO 24MHz <i>DEFAULT</i>	48MHZ OSC MODE <i>DEFAULT</i>	USB PHY POWERDOWN DISABLE <i>DEFAULT</i>	PCIE_CM_SET LOW <i>DEFAULT</i>	ENABLE THERMTRIP# <i>DEFAULT</i>

Edison-11/07-- Modify



# DEBUG STRAPS

	PDAK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE LONG RESET <i>DEFAULT</i>	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
<b>PULL LOW</b>	USE SHORT RESET		USE PCI PLL <i>DEFAULT</i>	USE ACPI BCLK <i>DEFAULT</i>	USE IDE PLL <i>DEFAULT</i>	USE DEFAULT PCIE STRAPS <i>DEFAULT</i>	

# SB-4



**PROJECT : ZB3**  
**Quanta Computer Inc.**

Size Custom	Document Number	Rev 1A
SB450M STRAPS		
Date: Monday, April 03, 2006		Sheet 14 of 37

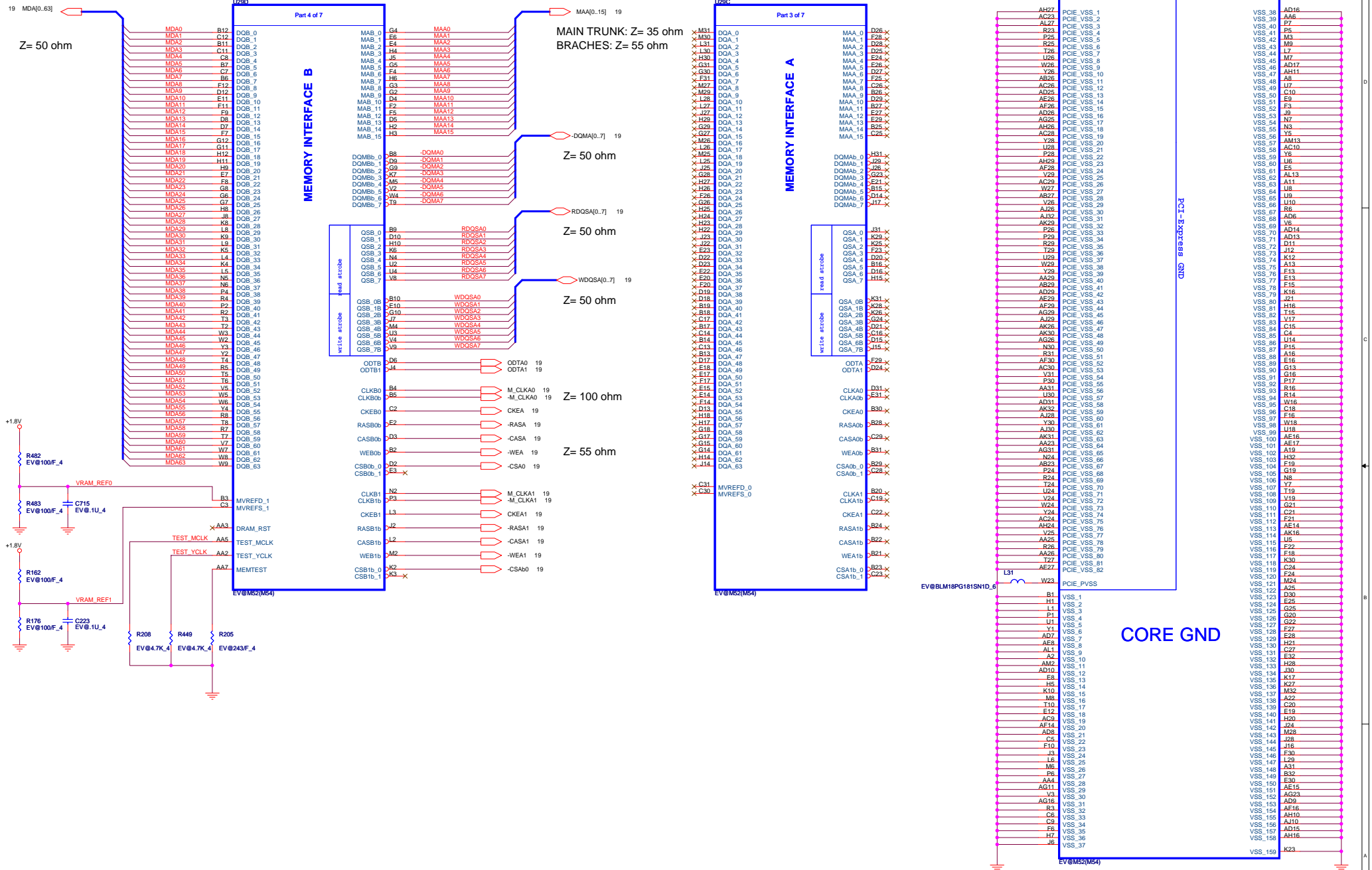




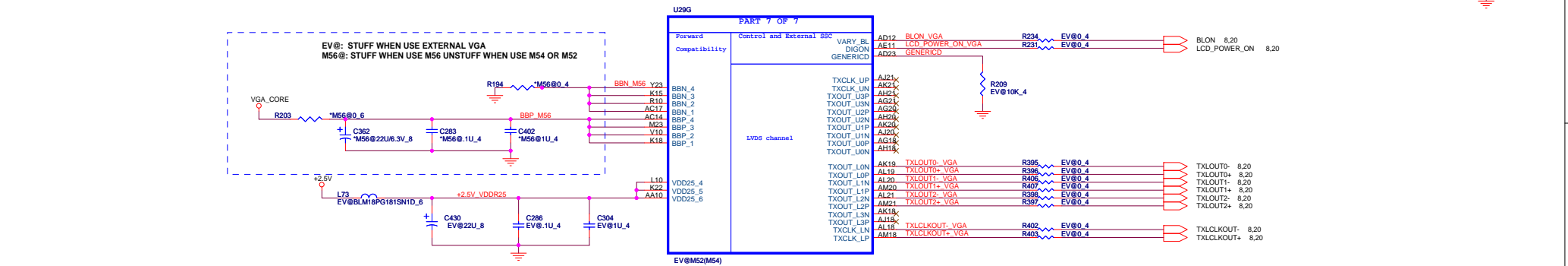
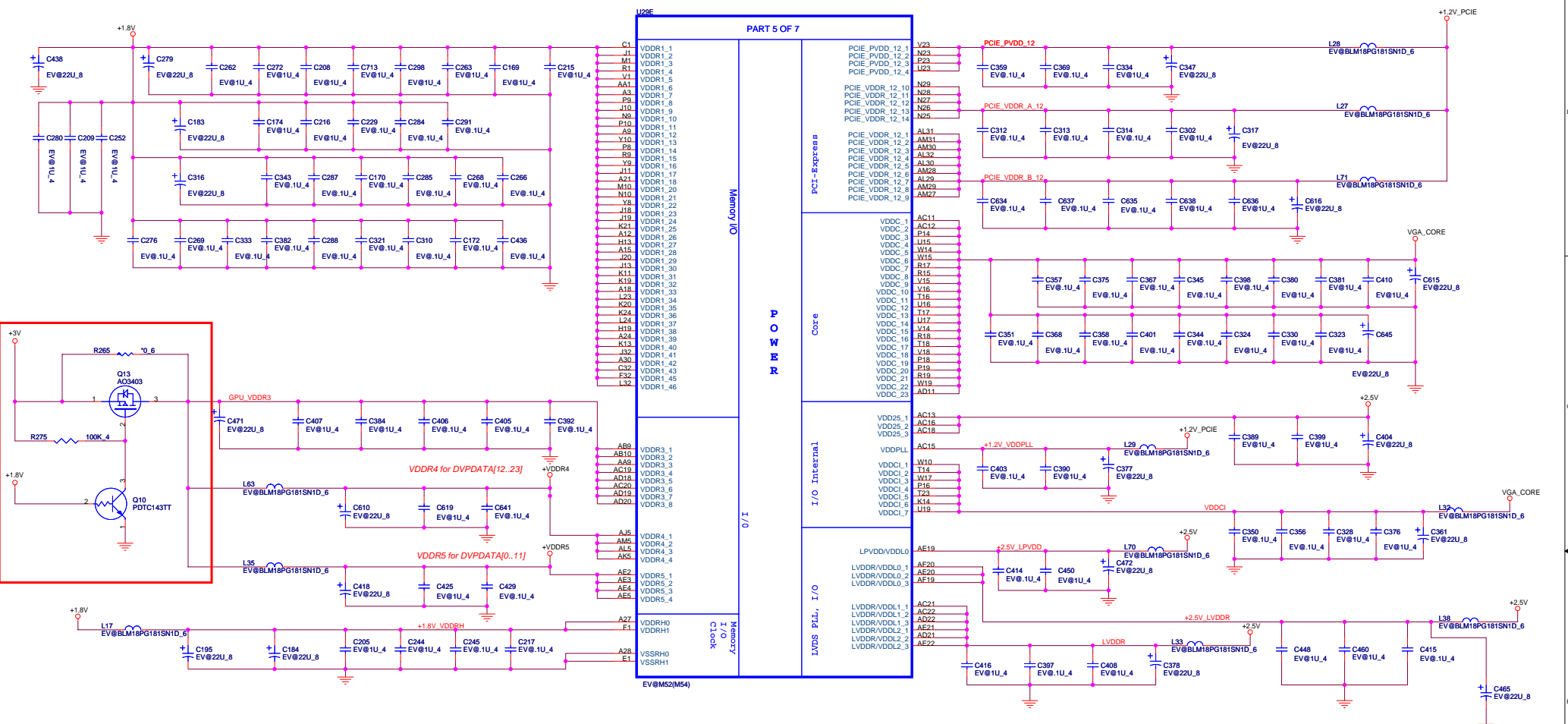
RV410 MEMORY CHANNELS A and B

Channel B

Channel A



CORE GND



### OPTION STRAPS

Overlap pads to save space and to prevent assembly of both resistors.

Layout



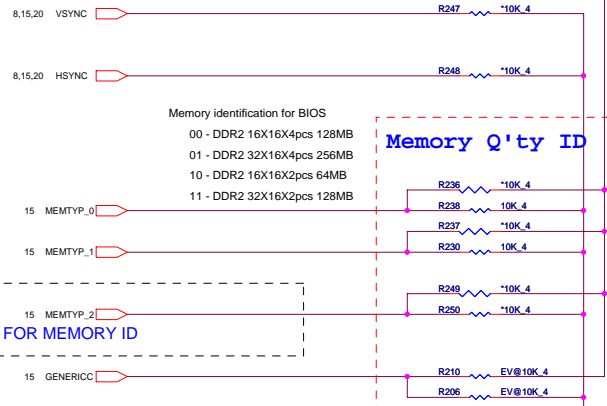
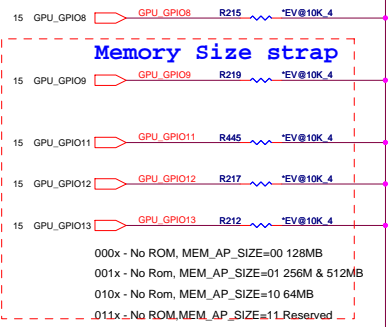
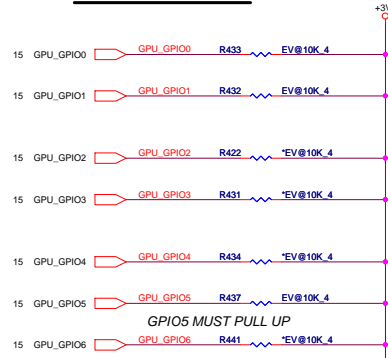
Ground  
High logic voltage  
Signal

Add Text "Populate to Enable Debug" Beside JU23 on Silkscreen.

Vendor P/N	QCI P/N	Size	GPU_GPIO1	GPU_GPIO12	MEMTYP_1	MEMTYP_0
HYB18T256161AFL2	AKD5JG-T*08	16M*16 *4pcs (128MB)	0	0	0	0
HY5PS561621AFP-25	AKD5JG-TW12	32M*16 *2pcs (128MB)	0	0	1	1
K4N56163QG-ZC25	AKD5JG-T514					
HYB18T512161BF-25	AKD5FG-T*00	32M*16 *4pcs (256MB)	0	1	0	1
HY5PS121621BFP-25	AKD5FG-TW14	32M*16 *4pcs (256MB)	0	1	0	1
K4N51163QC-ZC25	AKD5FGT501					

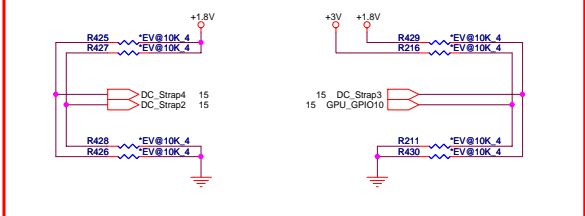
Memory Aperture Size Select  
When no ROM is attached, GPIO\_9 is set to 0  
GPIO\_13:12] is used to select the memory aperture size.  
GPIO\_13:12] = 00: 128M memory aperture, same as ROM strap 00  
GPIO\_13:12] = 01: 256M memory aperture, same as ROM strap 01  
GPIO\_13:12] = 10: 64M memory aperture, same as ROM strap 10  
GPIO\_13:12] = 11: reserved, same as ROM strap 11

Default: 128M memory aperture.  
GPIO\_13:12] = 01 (256M memory aperture) recommended for designs with 256MB or 512MB of physical memory.



RESERVE FOR MEMORY ID

ATI FAE: ALL N/A



### M56-P Strap

STRAPS	PIN	DESCRIPTION	Board DEFAULT
TX_PWRS_ENB	GPIO0 (Internal pull-down)	Transmitter Power Saving Enable 0: 50% Tx output swing 1.Full Tx output swing	1
TX_DEEMPH_EN	GPIO1 (Internal pull-down)	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1.Tx de-emphasis enabled	1
	GPIO (3:2)	RSVD	
DEBUG_ACCESS	GPIO4 (Internal pull-down)	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible	0
	GPIO5 (Internal pull-down)	RSVD	
	GPIO6 (Internal pull-down)	RSVD	
Force_Combpliance	GPIO8 (Internal pull-down)	Force chip to get to compliance state quickly for Tester purposes	0
ROMIDCFG(3:0)	GPIO(9,13,12,11) (Internal pull-down)	If no ROM attached, controls chip IDis. If rom attached identifies ROM type 000x - No ROM, MEM_AP_SIZE=00 128M 001x - No Rom, MEM_AP_SIZE=01 256M 010x - No Rom, MEM_AP_SIZE=10 64M 011x - No ROM, MEM_AP_SIZE=11 Reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM 1100 - Serial M25P05 ROM (ST), chip IDis from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	000
VIP_SERVICE	VSYN	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port deiced present. 1-No slave VIP port devices reporting presence during reset	No default
	H2SYN, V2SYN, GENERICC	RSVD	
	VSYN	RSVD	
	HSYN	RSVD	
	PCIE_TEST	RSVD	

### Board Straps

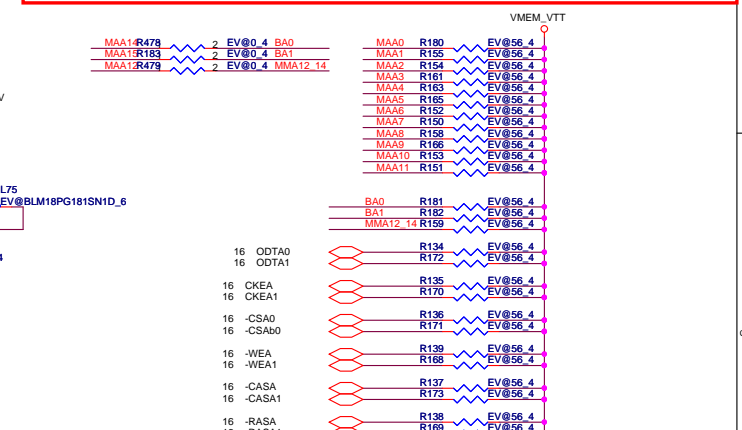
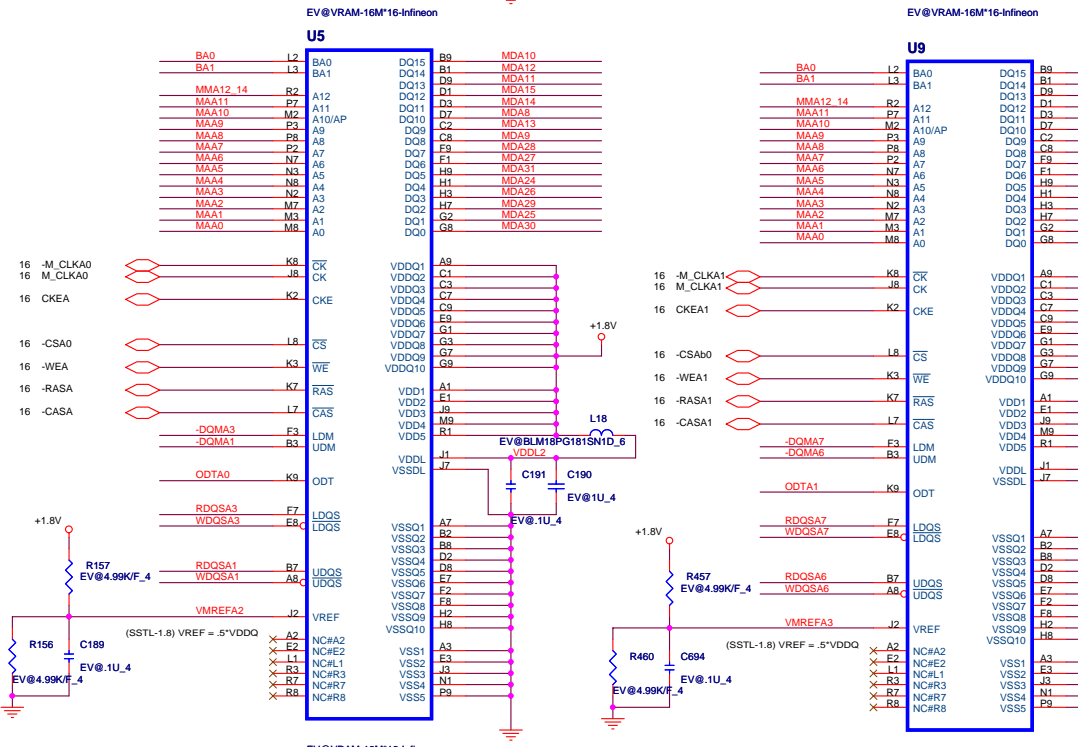
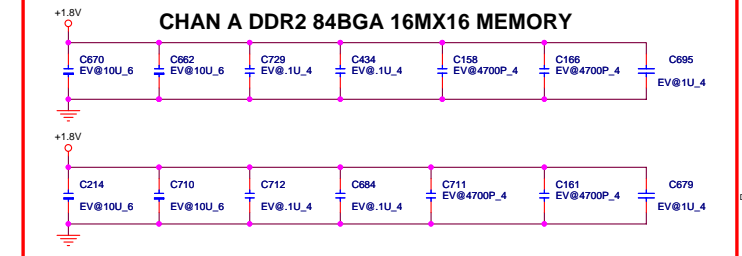
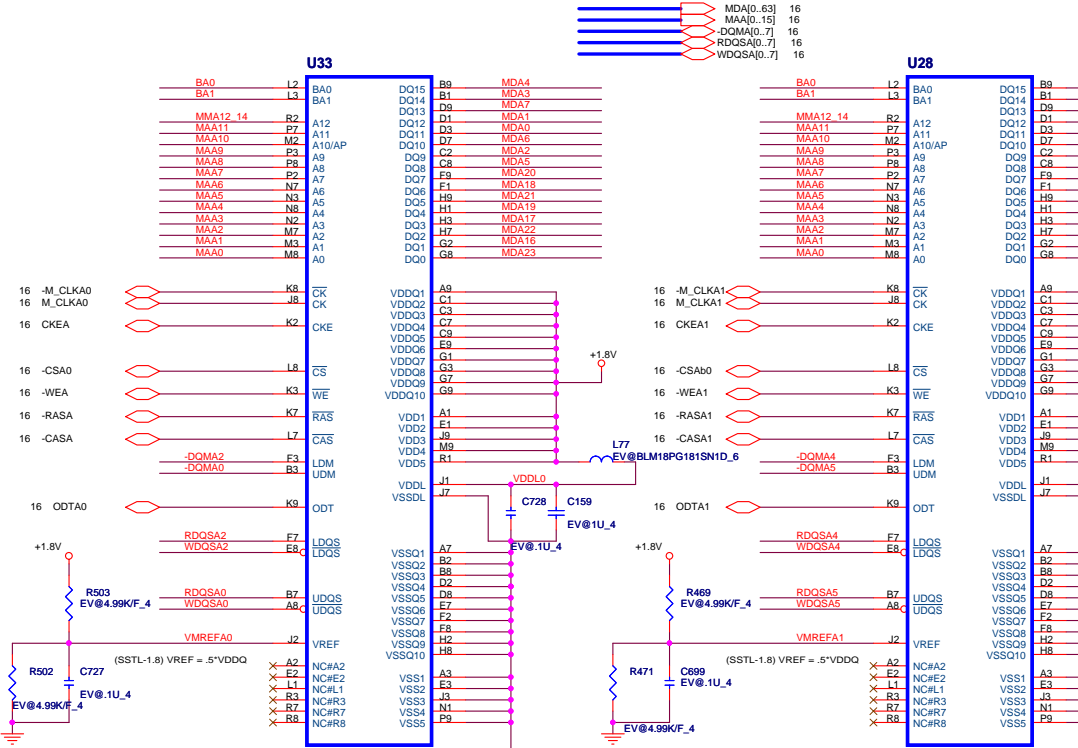
REV. 0.3

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYP(1:0)	DVPDATA(1:0)	Memory identification for BIOS 00 - DDR2 16X16X4pcs 128MB 01 - DDR2 32X16X4pcs 256MB 10 - DDR2 16X16X2pcs 64MB 11 - DDR2 32X16X2pcs 128MB	
DC_Strap1	GPIO(10)	Internal TMDs Enabled 0 - Disabled 1 - Enabled	1
DC_Strap2	DVPDATA13	Video Capture Enabled 0 - Disabled 1 - Not detected	0
DC_Strap3	DVPDATA14	HDTV out detect 0 - Detected 1 - Enabled	1
DC_Strap4, DEMUX_SEL	DVPDATA15	Video capture enable 00 - DAC2 Off 01 - DAC2 On as CRT 10 - DAC2 On as TVOUT 11 - DAC2 On as TVOUT and CRT	01
PALNTSC	LCDDATA(18)	TVO Standard Default (Resistor pull-up and switch short to GND) 0 - PAL (on board resistor pull-down and switch closed) 1 - NTSC (on board resistor pull-up)	1

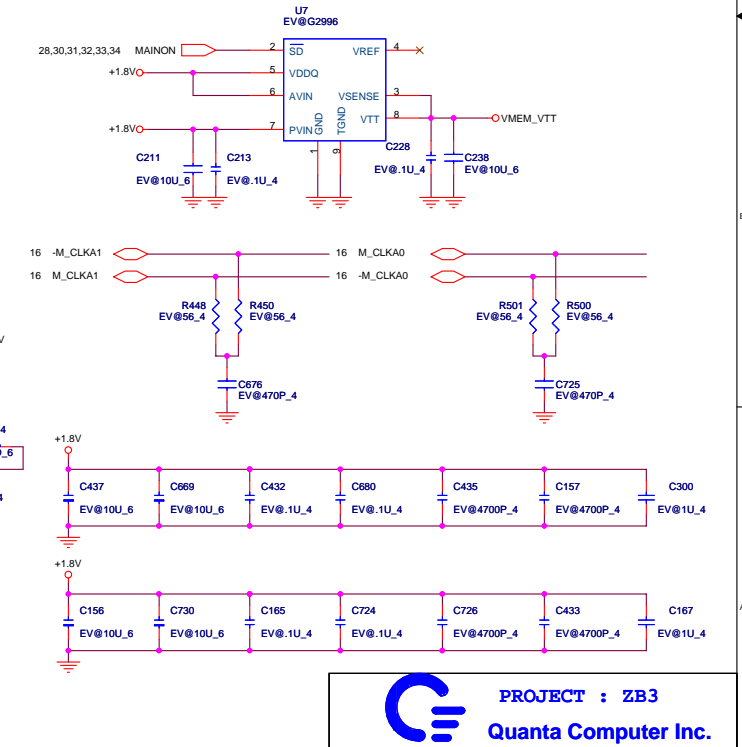
**PROJECT : ZB3**  
**Quanta Computer Inc.**

Size Document Number  
**M52-P\_Straps (4 of 4)** Rev 00

Date: Monday, April 03, 2006 Sheet 18 of 37



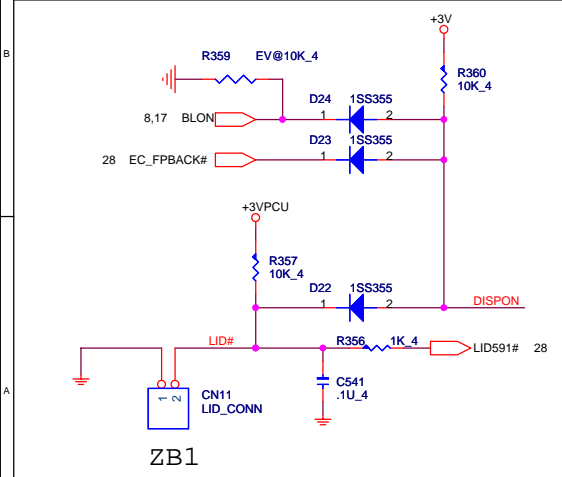
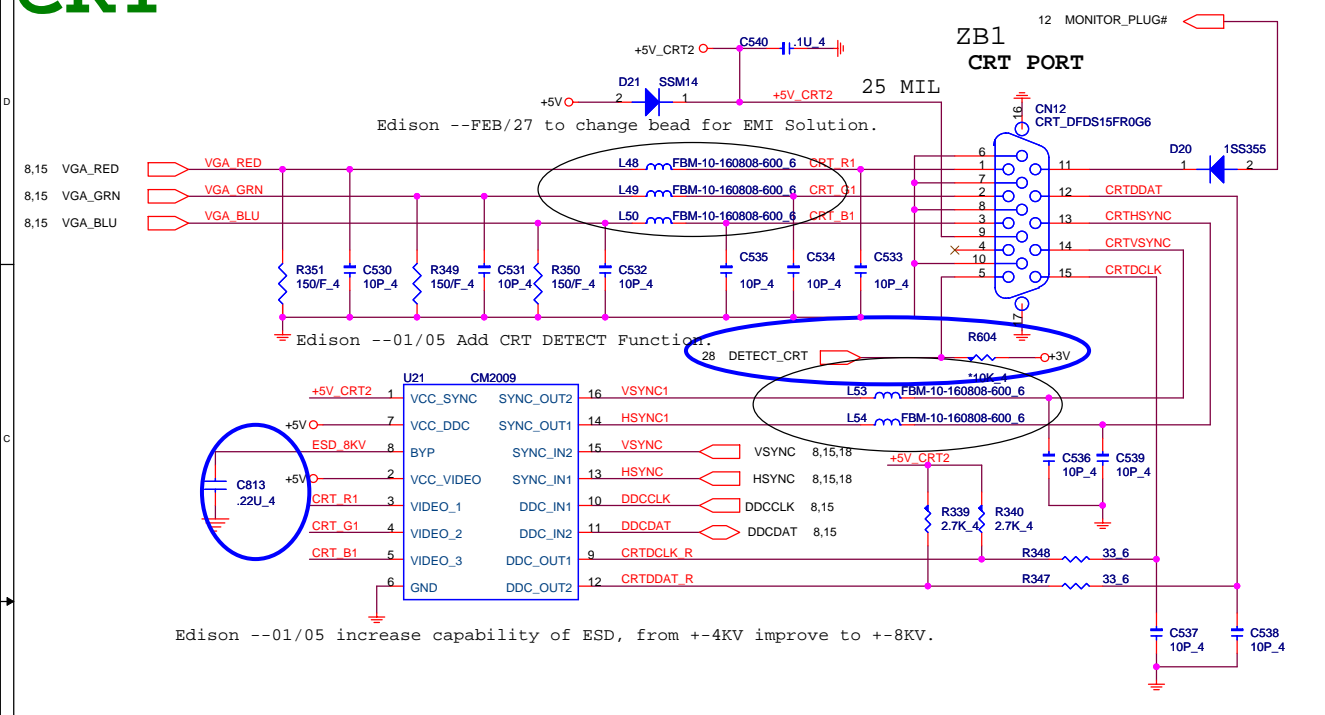
FOR M56P AT DDR2 MEMORY SPEEDS ABOVE 350MHZ MEMORY CONTROL SIGNALS WE,CAS,RAS,CS,CKE,ODT AND MEMORY ADDRESS SIGNALS REQUIRE 55 OHM PULLUP TO A VTT RAIL (50% OF VDDQ)



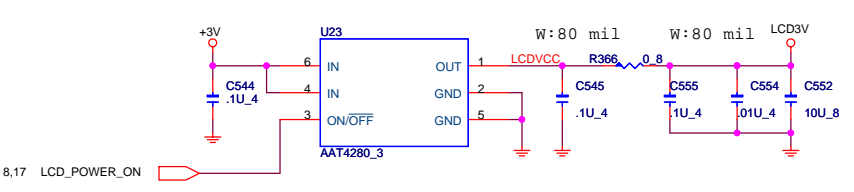
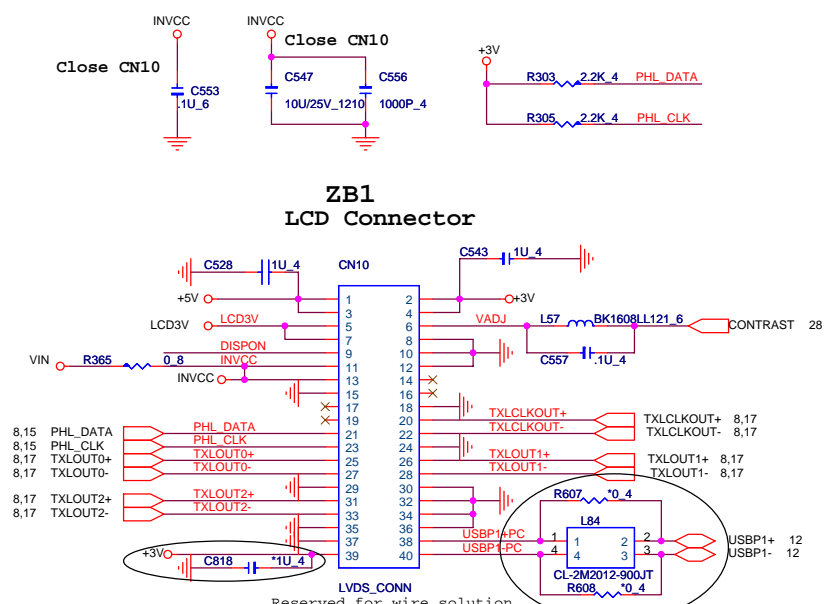
**PROJECT : ZB3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>VRAM DDR2</b>	1A
Date:	Monday, April 03, 2006	Sheet 19 of 37

# CRT



# LVDS



DSC Pinout : pin1 -- VCC(+3V)  
 pin2 -- USB-  
 pin3 -- USB+  
 pin4 -- GND  
 pin5 -- Shielding  
 the connector is JST SM05B-SSR-H-TB

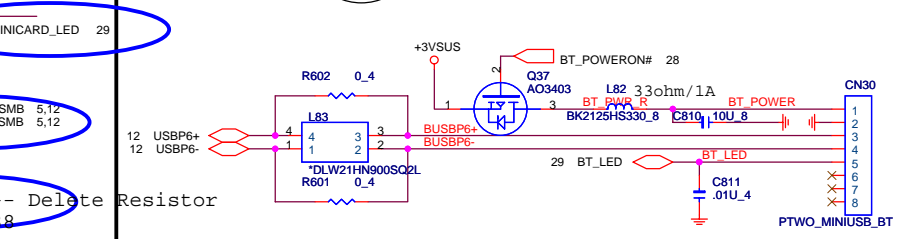
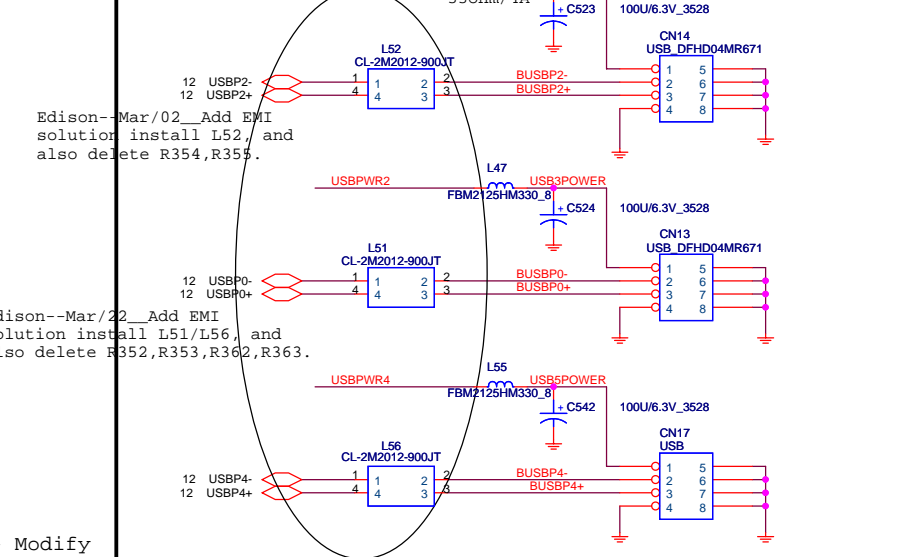
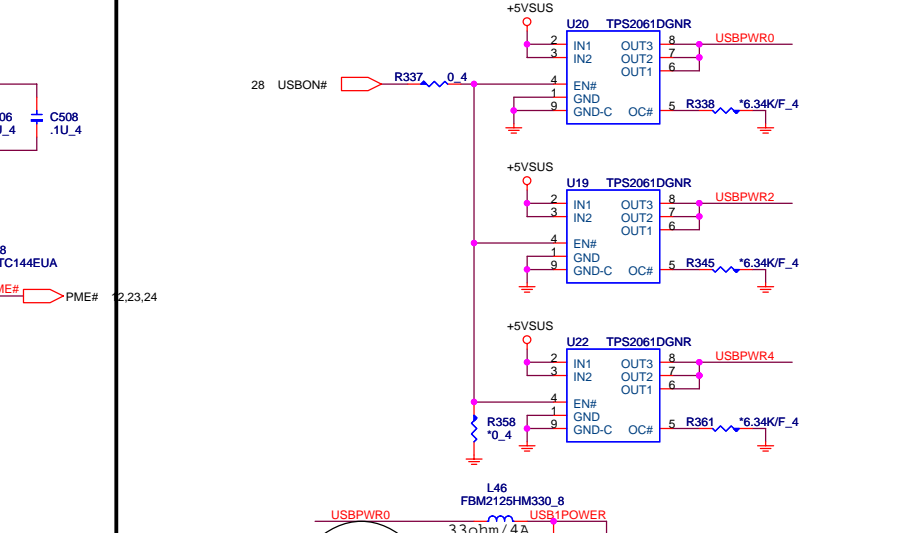
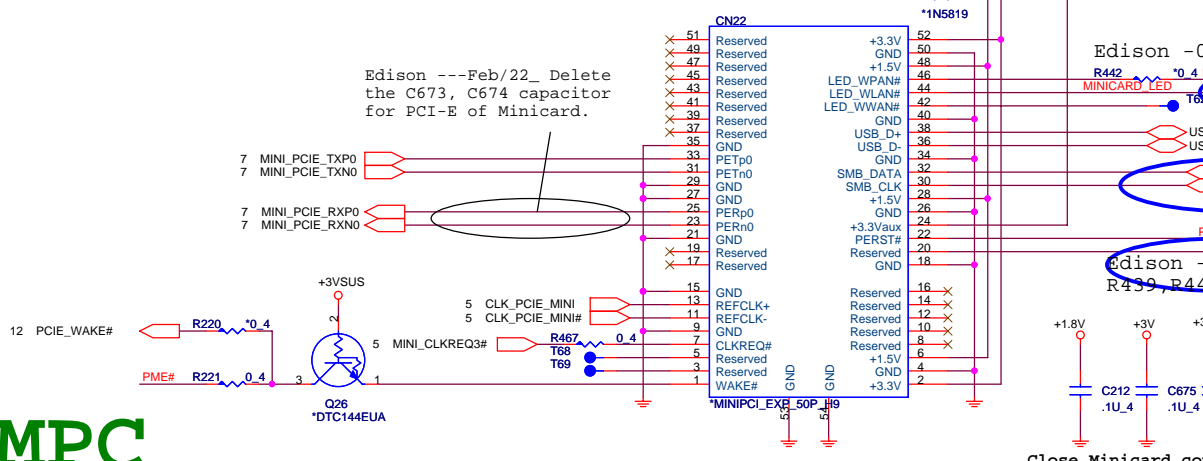
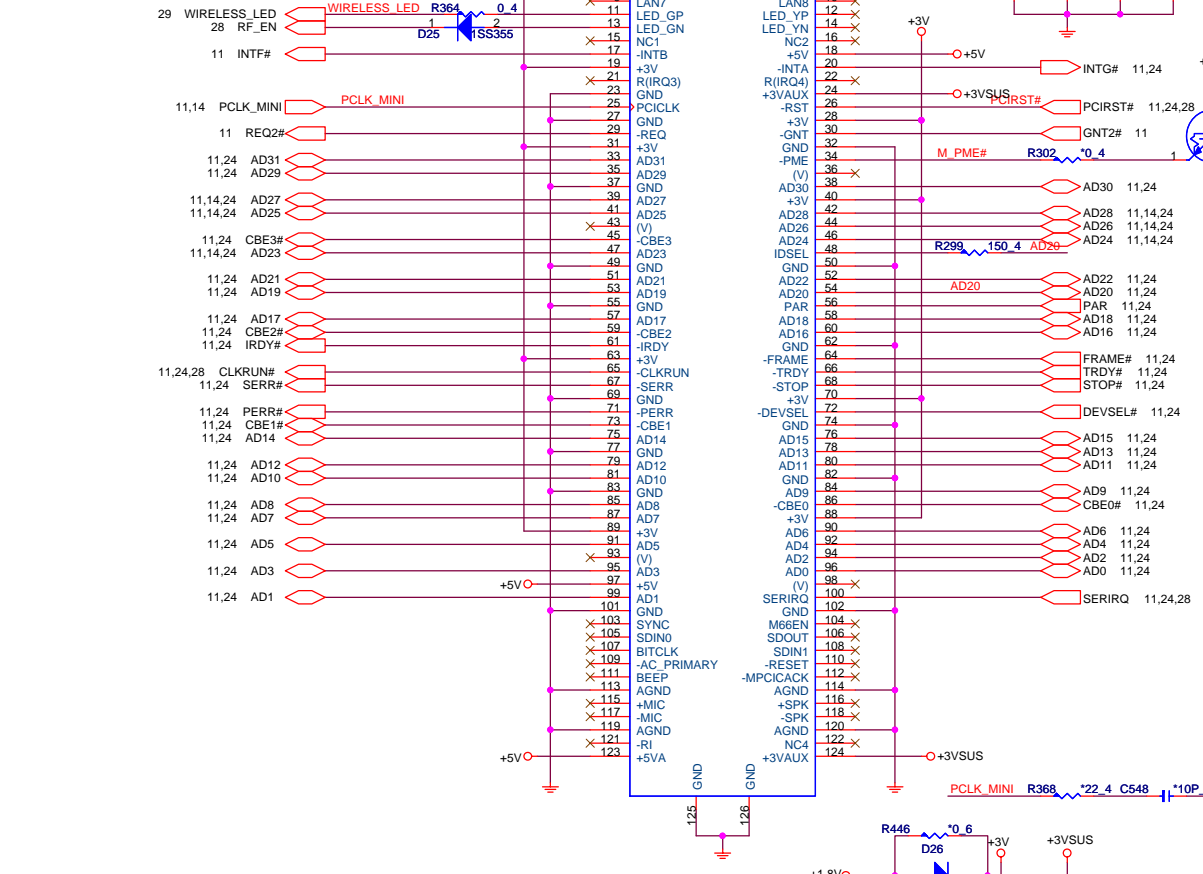
**PROJECT : ZB3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
<b>VGA Ports, LID, &amp; HOLES</b>		<b>1A</b>
Date:	Monday, April 03, 2006	Sheet 20 of 37





ID Select : AD20  
 Interrupt Pin : INTF#, INTG#  
 Request Indicate : REQ2#  
 Grant Indicate : GNT2#



Edison ---Feb/22\_ Delete the C673, C674 capacitor for PCI-E of Minicard.

Edison -0104-- Modify

Edison -0111-- Delete Resistor

Edison--Mar/02\_Add EMI solution install L52, and also delete R354,R355.

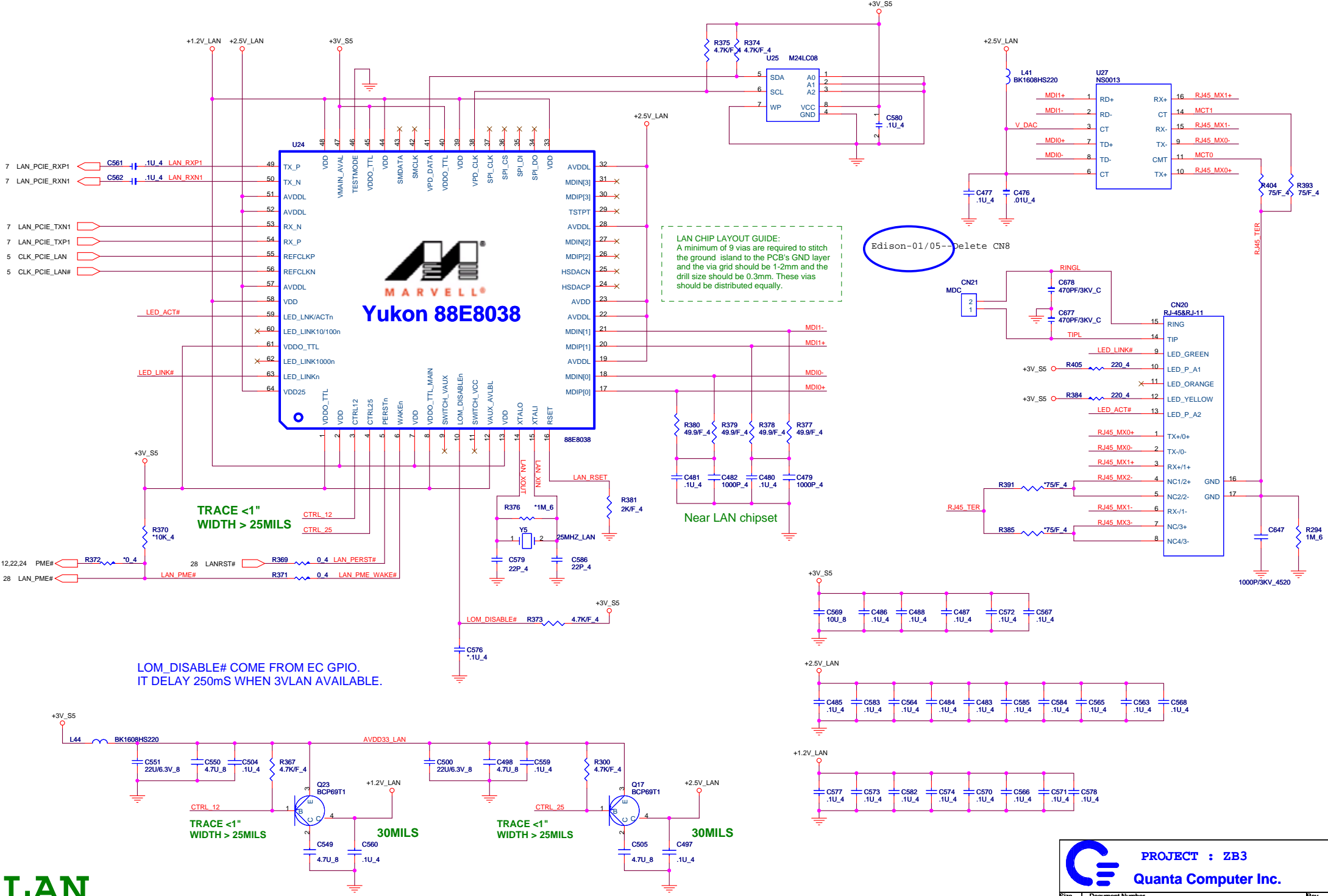
Edison--Mar/22\_Add EMI solution install L51/L56, and also delete R352,R353,R362,R363.

**MPC**

**USB**

**PROJECT : ZB3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>MINI PCI&amp;PCI-E,USB PORT</b>	1A
Date:	Monday, April 03, 2006	Sheet 22 of 37



**LAN CHIP LAYOUT GUIDE:**  
 A minimum of 9 vias are required to stitch the ground island to the PCB's GND layer and the via grid should be 1-2mm and the drill size should be 0.3mm. These vias should be distributed equally.

Edison-01/05--Delete CN8

TRACE <1" WIDTH > 25MILS

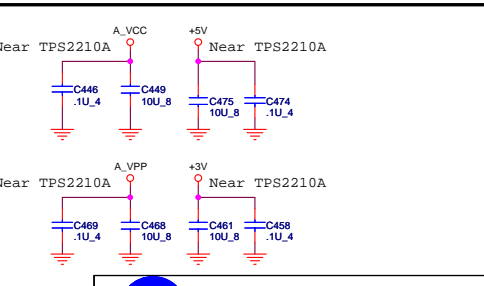
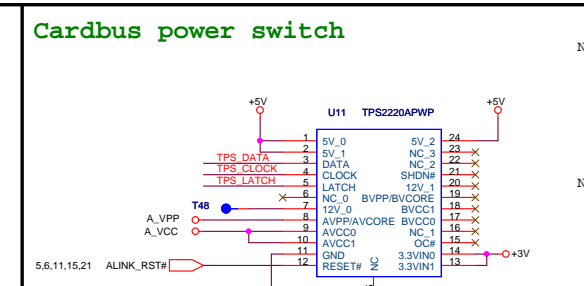
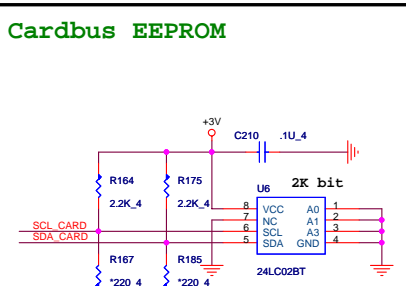
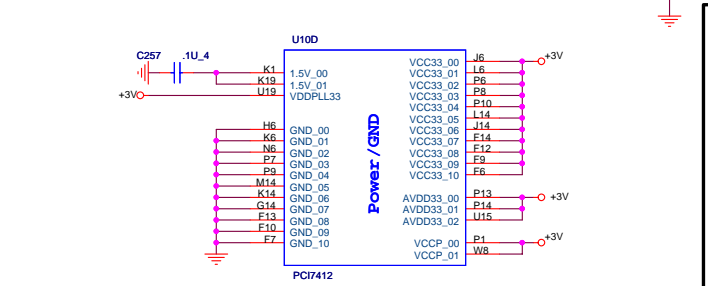
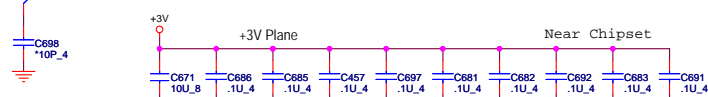
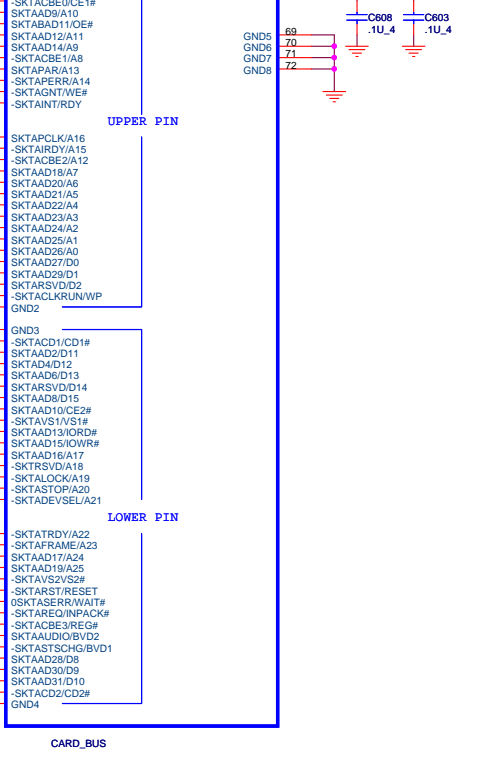
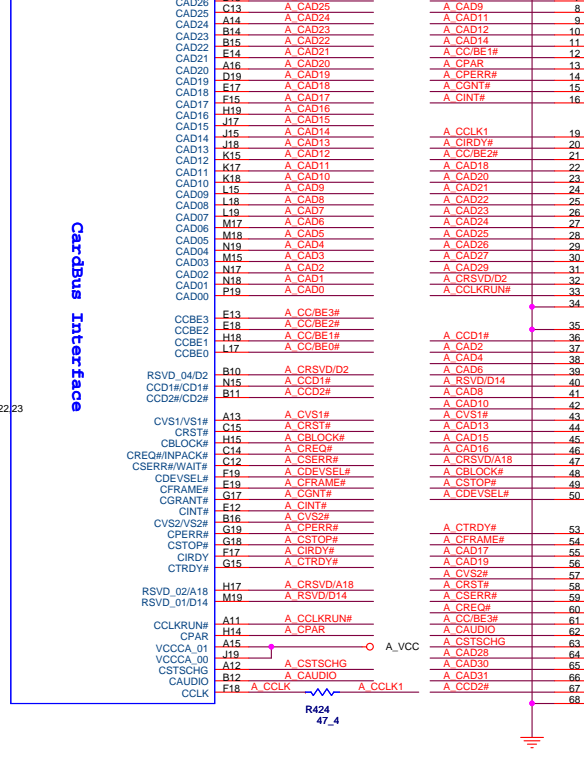
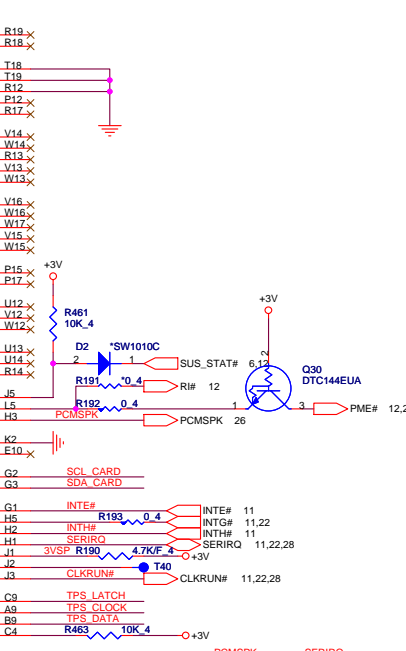
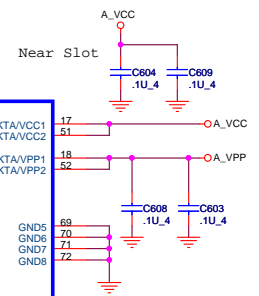
LOM\_DISABLE# COME FROM EC GPIO. IT DELAY 250ms WHEN 3VLN AVAILABLE.

**LAN**


ID Select : AD17  
 Interrupt Pin : INTE#/INTG#/INTH#  
 Request Indicate : REQ3#  
 Grant Indicate : GNT3#

### CARDBUS SLOT

ZB1



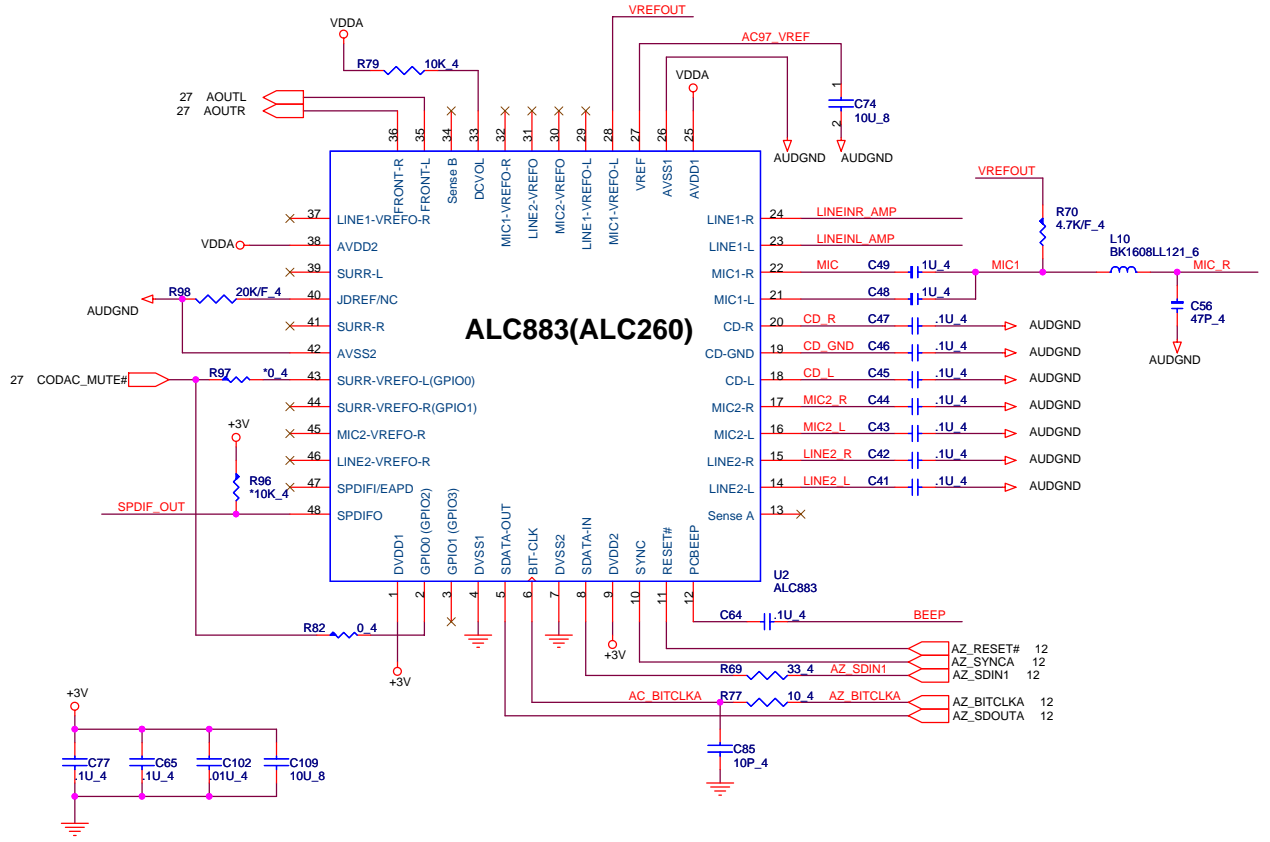
# CARD Bus


**PROJECT : ZB3**  
**Quanta Computer Inc.**

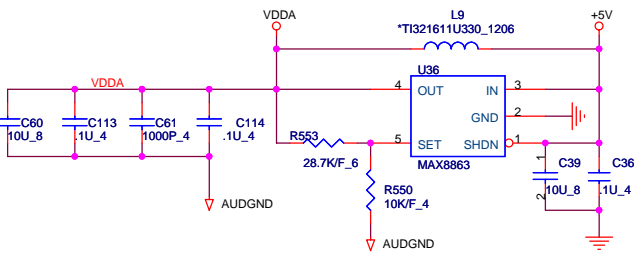
Size	Document Number	Rev
	<b>PCI7412-PCMCIA CONTROLLE</b>	1A
Date:	Monday, April 03, 2006	Sheet 24 of 37



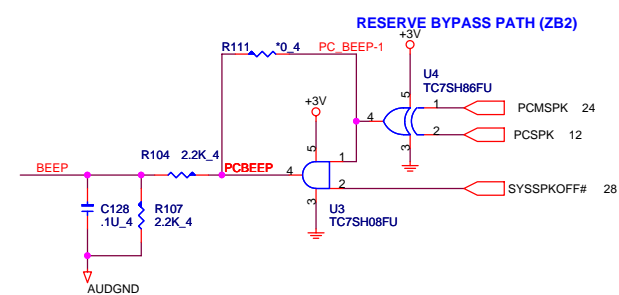
# ADO



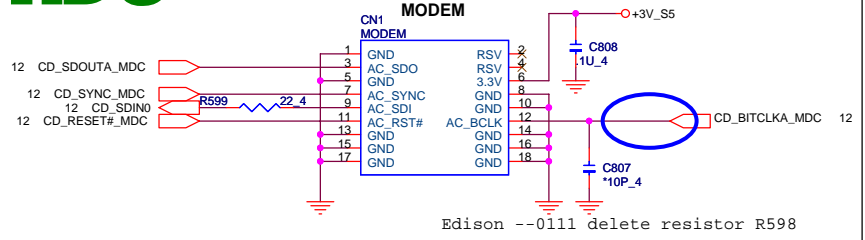
# Audio Power



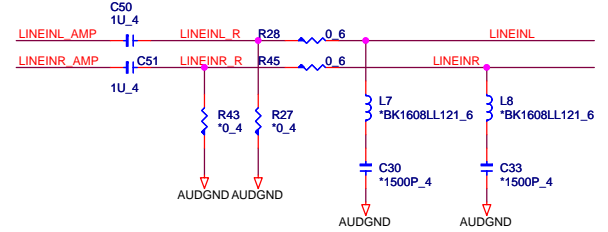
# BEEP



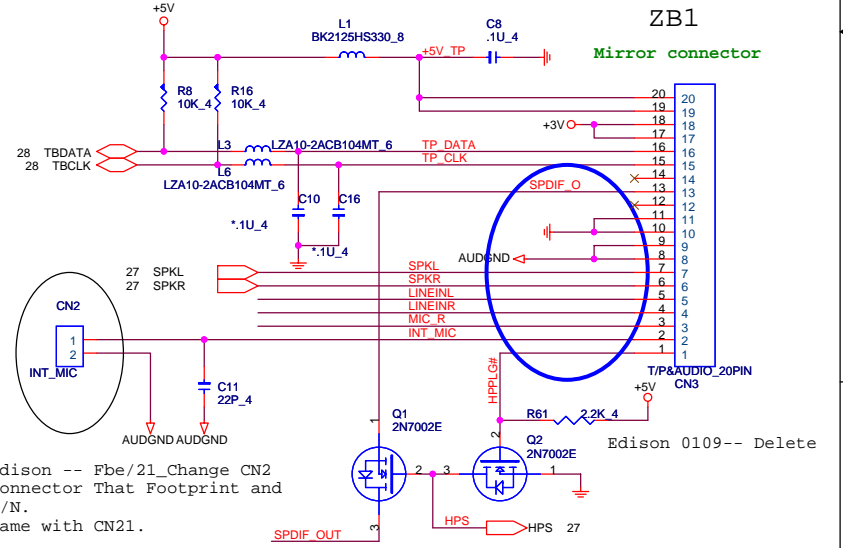
# MDC



# LINE IN



# ZB1

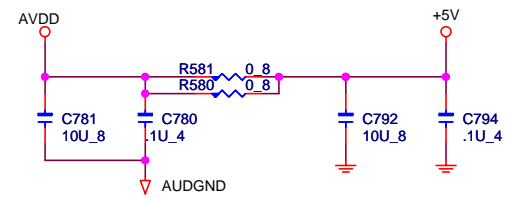
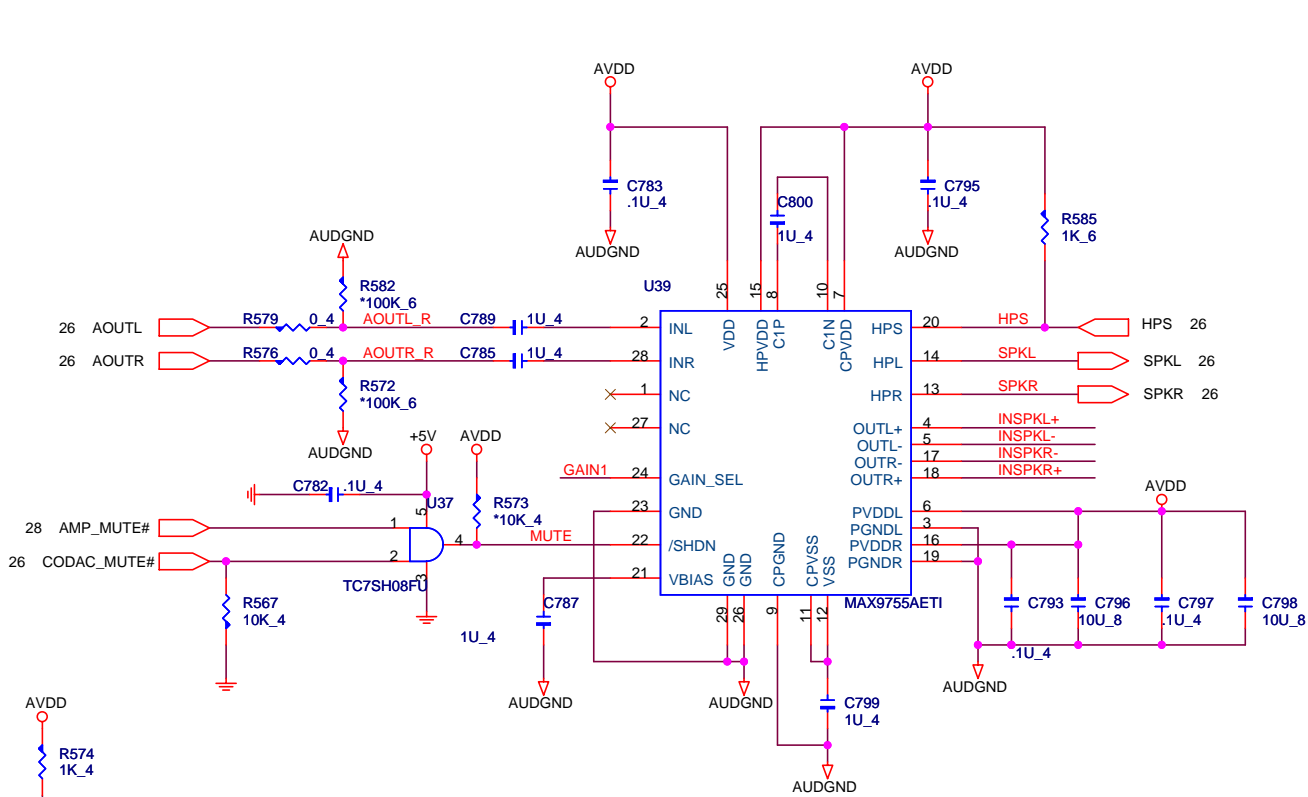


Edison -- Fbe/21\_change CN2 connector That footprint and P/N. same with CN21.

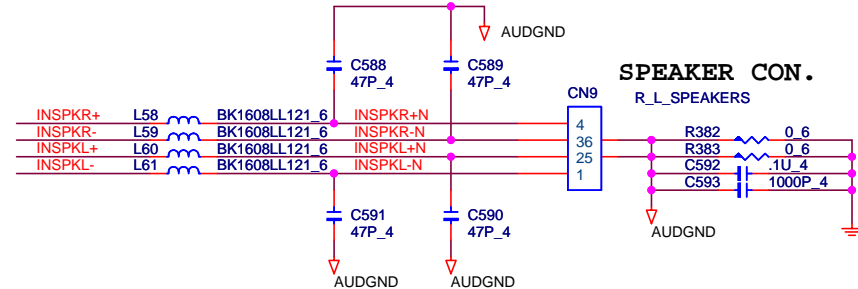
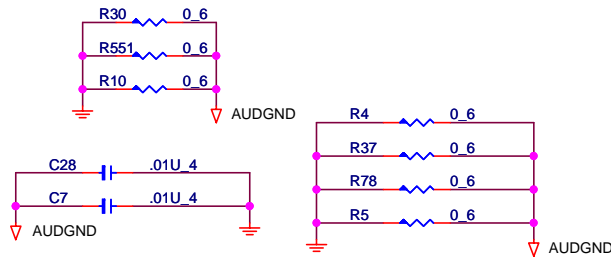
**PROJECT : ZB3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>CODEC &amp; LINE IN &amp; MIC</b>	1A
Date:	Monday, April 03, 2006	Sheet 26 of 37





GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0



**AMP**



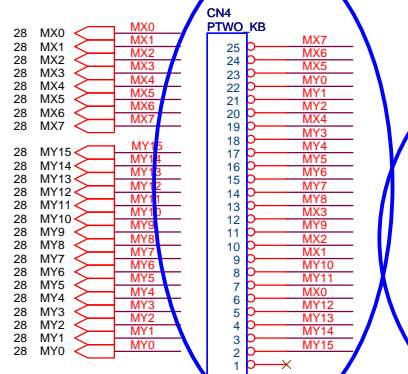
**PROJECT : ZB3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>AUDIO AMP</b>	1A

Date: Monday, April 03, 2006 Sheet 27 of 37

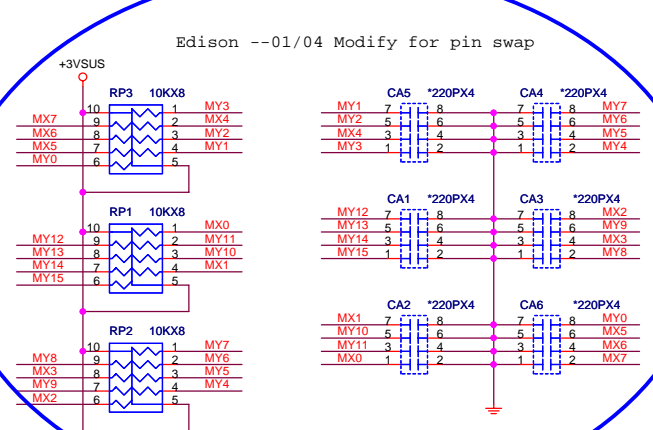


**INT K/B** Edison --01/03 Modify

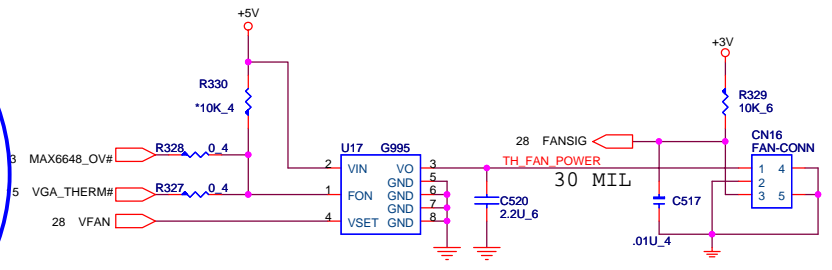


**KBC**

**ZB1** Edison --01/04 Modify for pin swap

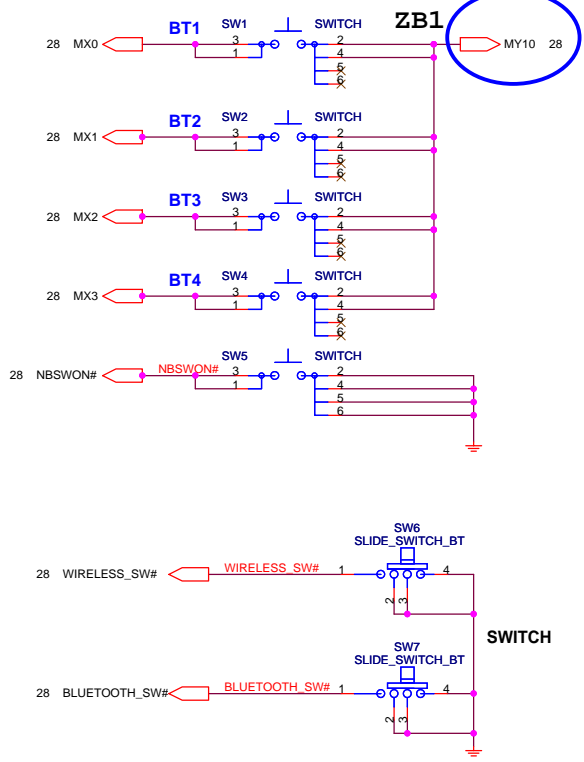


**FAN CONTROL**



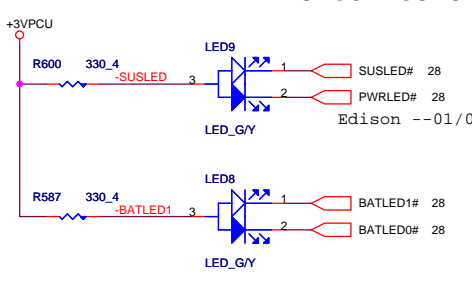
**THM**

Edison --01/04 Modify

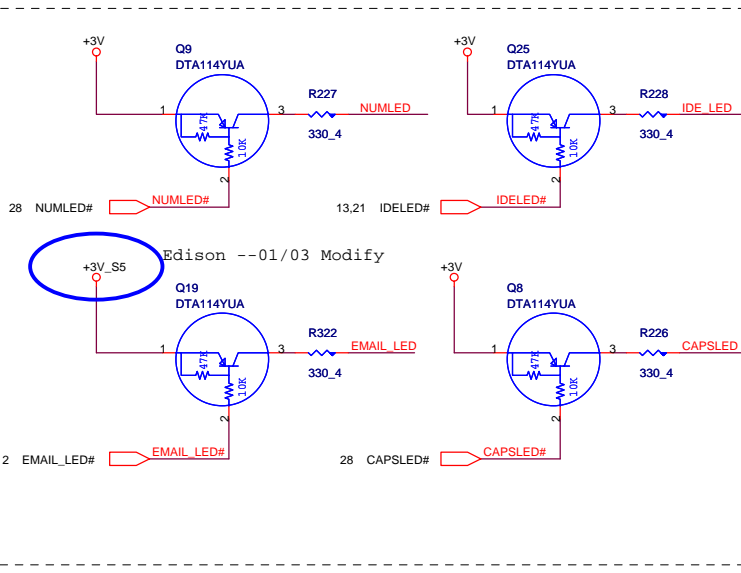
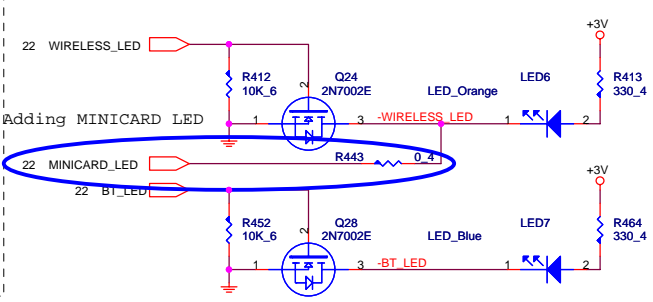


**Switch**

Check color

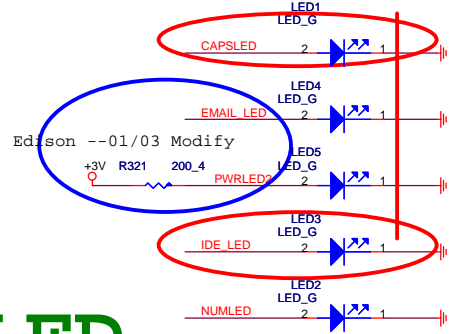


Edison --01/04 Adding MINICARD LED



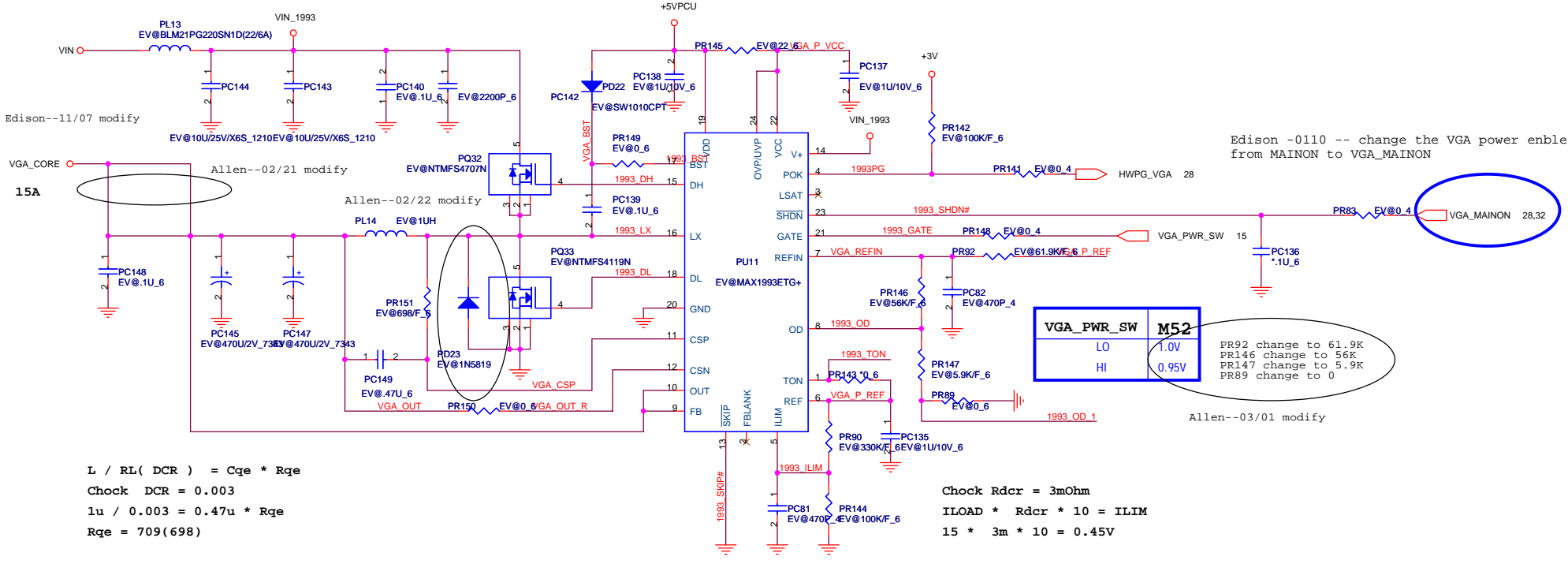
**LED**

Exchange Layout position



**PROJECT : ZB3**  
**Quanta Computer Inc.**

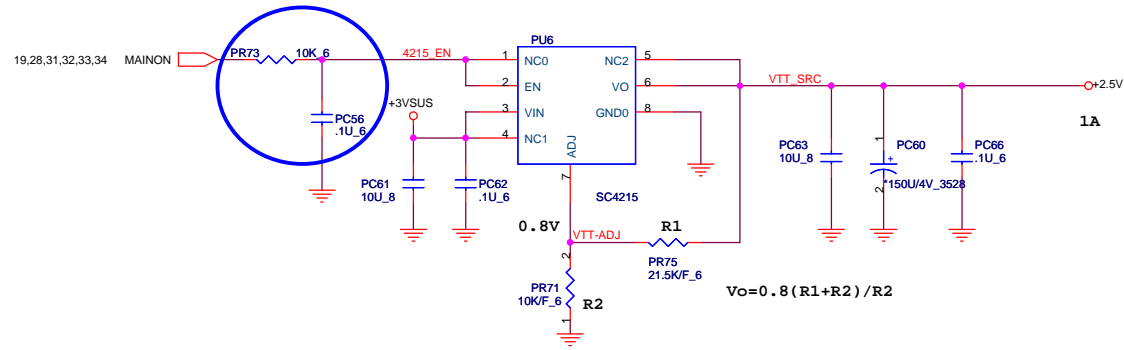
Size	Document Number	Rev
	<b>T/P,FAN,SWITCH,LED,K/B</b>	1A
Date:	Monday, April 03, 2006	Sheet 29 of 37



$L / R_L( DCR ) = C_{qe} * R_{qe}$   
 Chock DCR = 0.003  
 $1u / 0.003 = 0.47u * R_{qe}$   
 $R_{qe} = 709(698)$

Chock Rdcr = 3mOhm  
 $I_{LOAD} * R_{dcr} * 10 = I_{LIM}$   
 $15 * 3m * 10 = 0.45V$

+2.5v delay lms for VGA power-up sequence --Arec 0113



# VGA CORE

**PROJECT : ZB3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>VGA CORE</b>	1A
Date:	Monday, April 03, 2006	Sheet 30 of 37

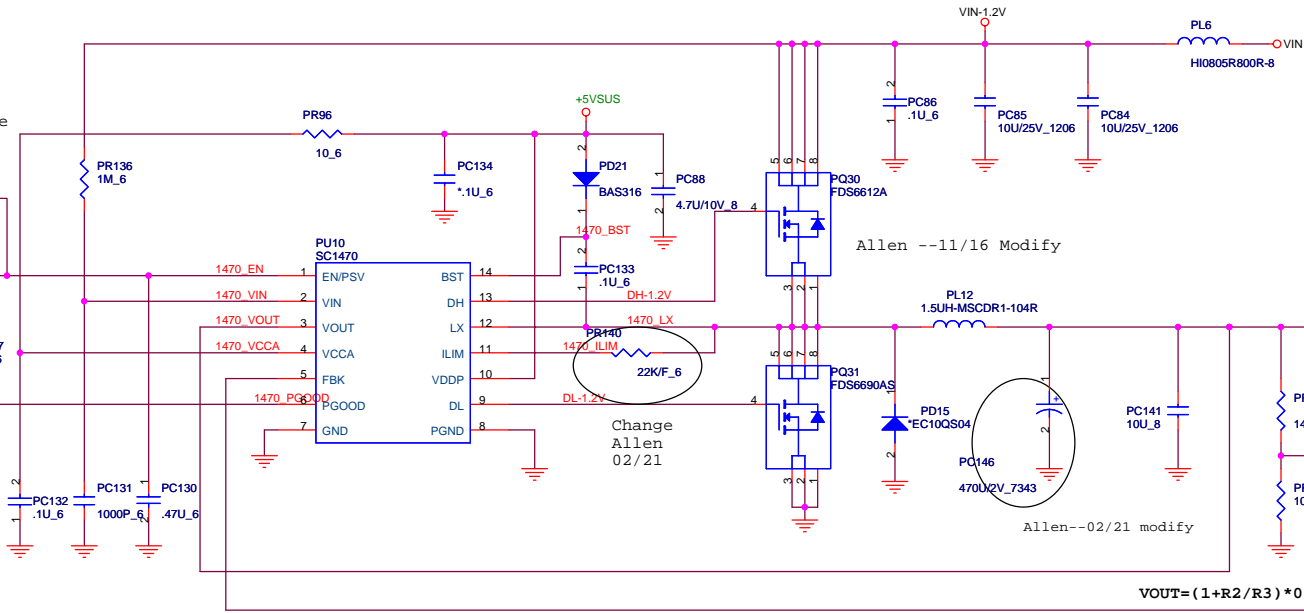


Alan --11/17 Modify  
Reserve for VGA sequence

28,30 VGA\_MAINON PR135 0.6

19,28,30,31,33,34 MAINON PR139 0.6

28 HWPG\_1.2V PR138 0.6



Allen --11/16 Modify

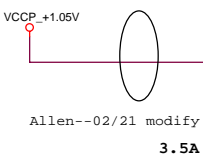
Change Allen  
02/21

Allen--02/21 modify

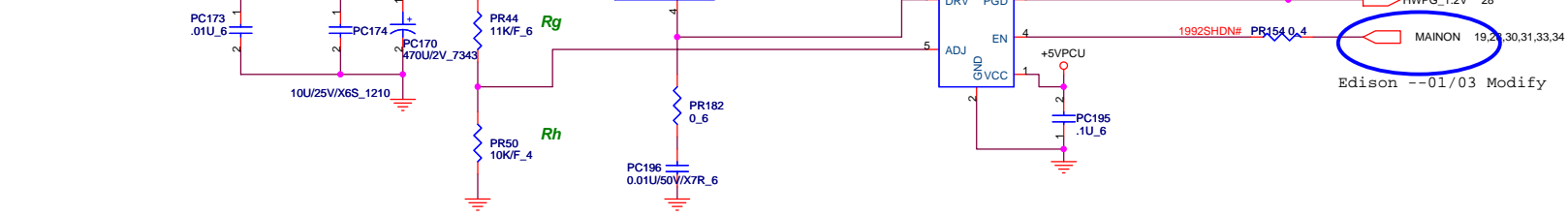
7.5A+3.5A for  
VCCP\_+1.05V

Allen--02/21 modify

$$V_{OUT} = (1 + R2/R3) * 0.5$$




Allen--02/21 modify  
3.5A



$$V_{out1} = (1 + Rg/Rh) * 0.5$$

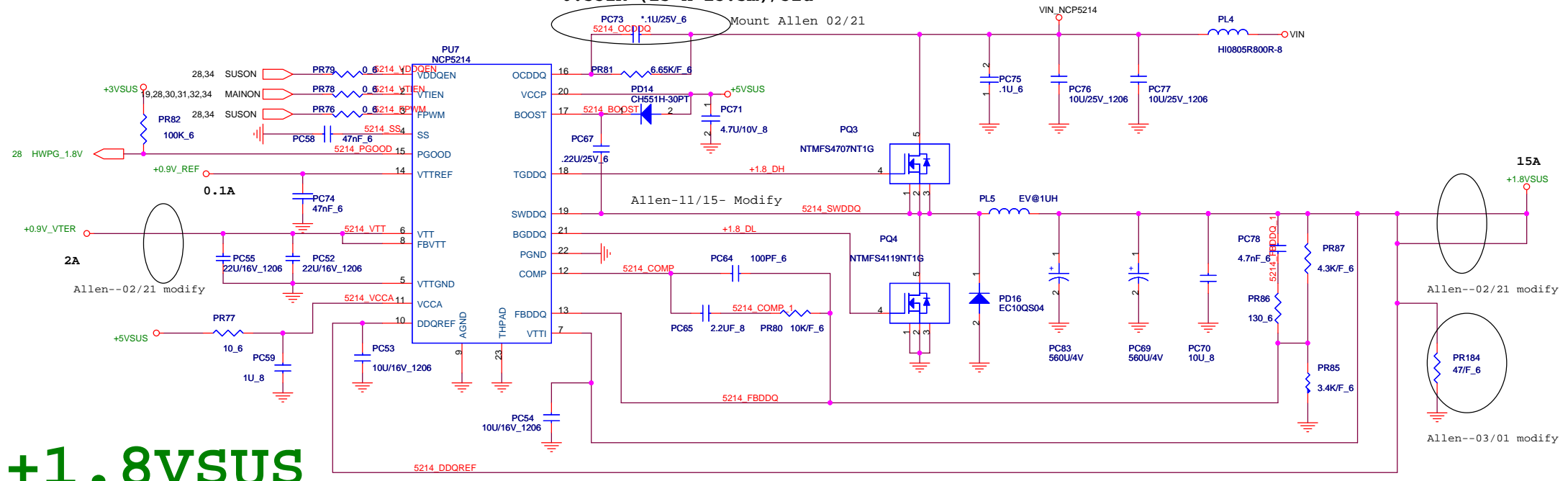
Edison --01/03 Modify

		PROJECT : ZB3	
		Quanta Computer Inc.	
Size	Document Number	DISCHAGE&+1.8V	
Date: Monday, April 03, 2006	Sheet	32	of 37
			Rev 1A



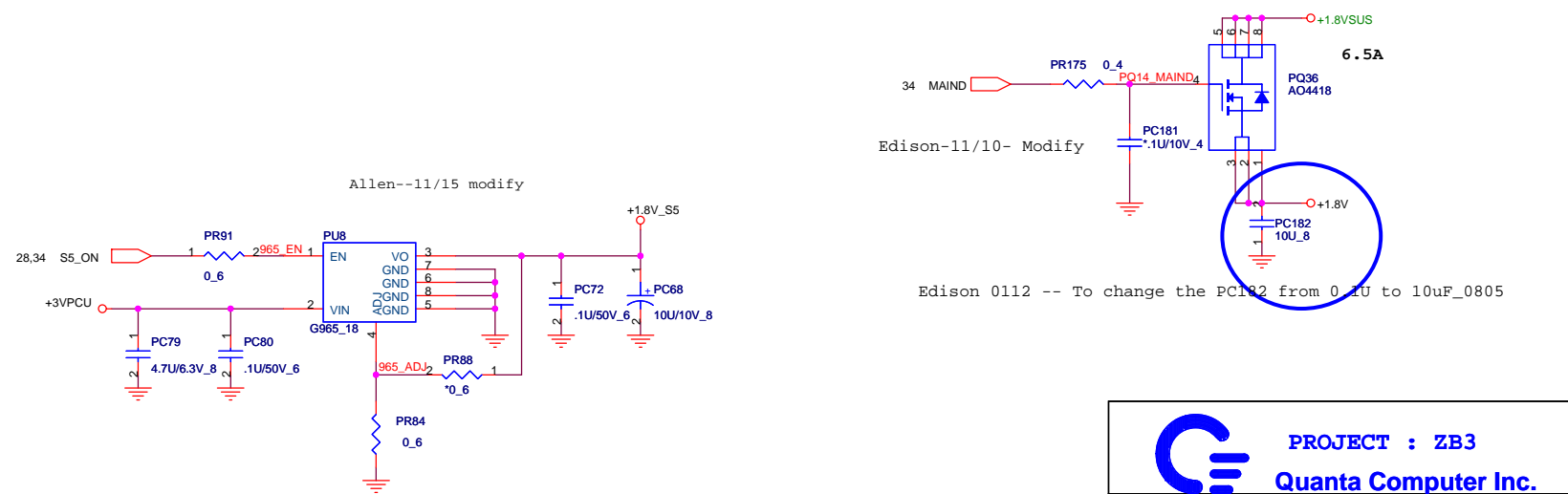
$$RL1 = (I_{lim} \times R_{dson-h}) / I_{OC}(31\mu A)$$

$$6.532K = (15 \times 13.5m) / 31\mu$$

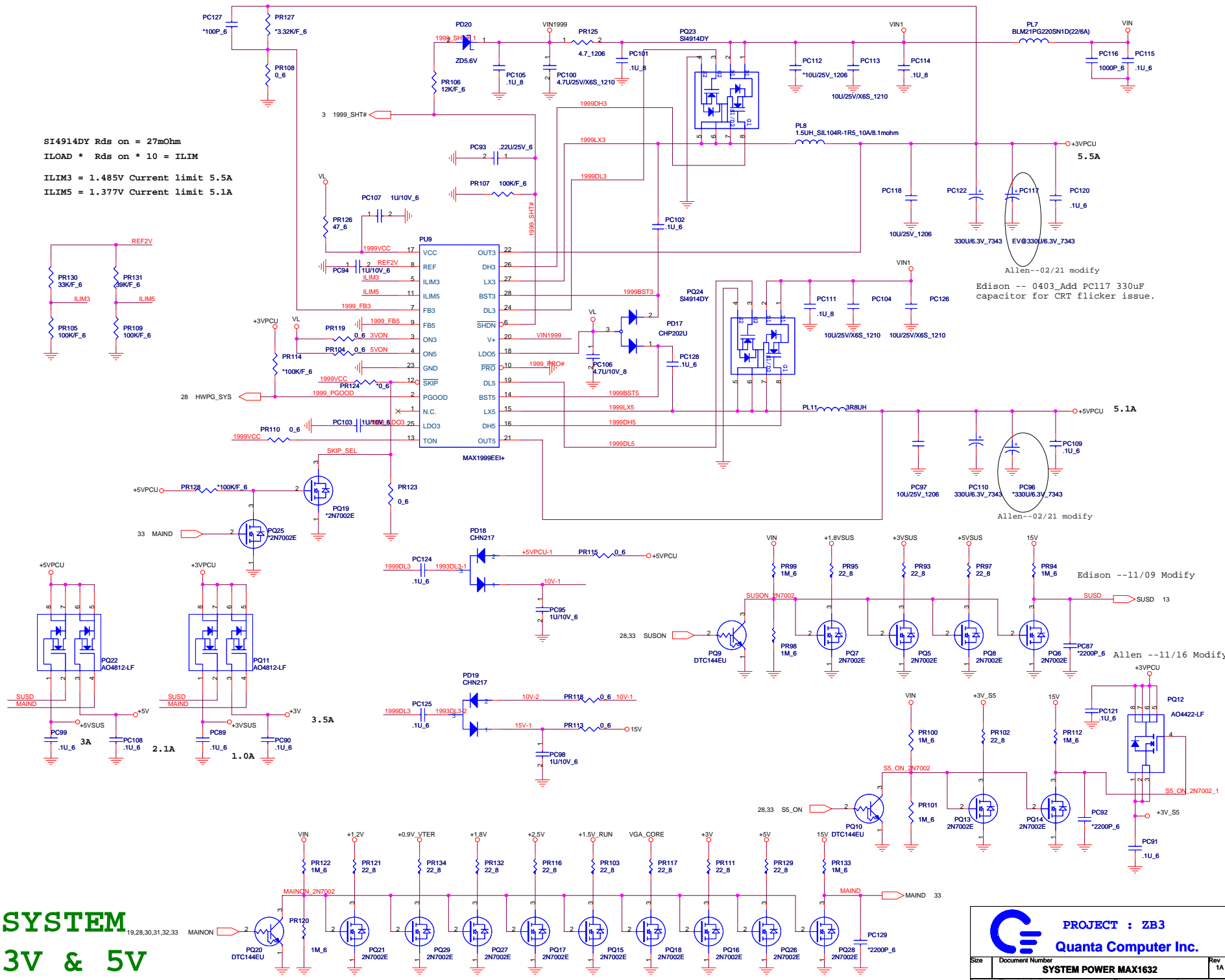


**+1.8VSUS**

## DDR Power & NB Power



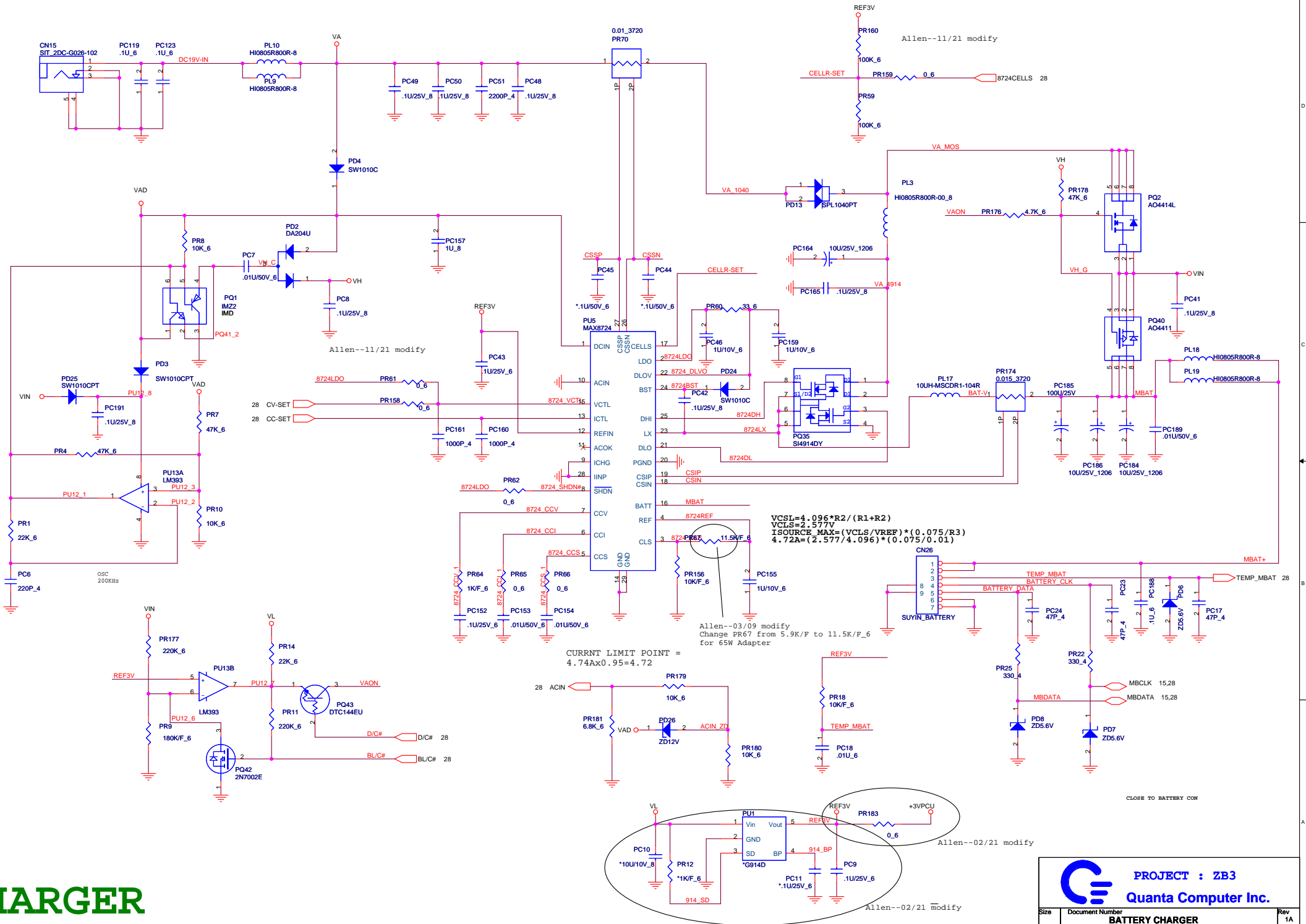
SI4914DY Rds on = 27mOhm  
 $I_{LOAD} * R_{ds\ on} * 10 = I_{LIM}$   
 $I_{LIM3} = 1.485V$  Current limit 5.5A  
 $I_{LIM5} = 1.377V$  Current limit 5.1A



# SYSTEM 3V & 5V

		PROJECT : ZB3	
		Quanta Computer Inc.	
Size	Document Number	SYSTEM POWER MAX1632	
Date	Thursday, April 06, 2006	Sheet	34 of 37

# CHARGER



$$VCSL = 4.096 * R2 / (R1 + R2)$$

$$VCLS = 2.577V$$

$$ISOURCE\_MAX = (VCLS / VREF) * (0.075 / R3)$$

$$4.72A = (2.577 / 4.096) * (0.075 / 0.01)$$

CURRENT LIMIT POINT = 4.74Ax0.95=4.72

Allen--03/09 modify  
Change PR67 from 5.9K/F to 11.5K/F for 65W Adapter

Allen--02/21 modify

Allen--02/21 modify

