

# Compal Confidential

## Qiao Hong Schematics Document

Intel Diamondville Processor with Calistoga(945GSE) + DDRII + ICH7M

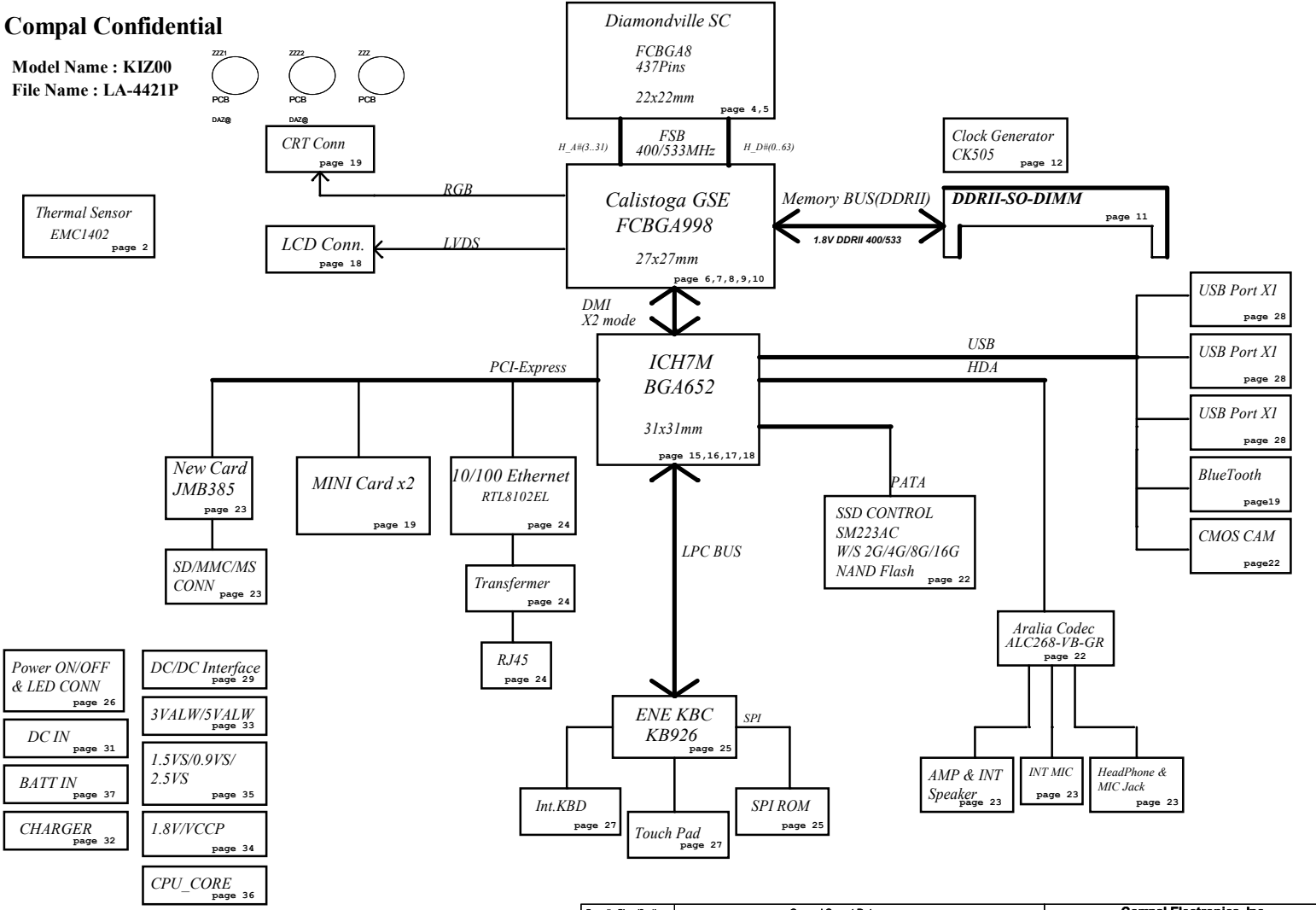
2008-07-07

REV: 1.0

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Issued Date	2006/08/18	Deciphered Date	2007/6/18	Title	Cover Page
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				Document Number	LA-4421P
				Date	Friday, August 10th, 2008
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Model Name : KIZ00  
File Name : LA-4421P



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### Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	VCCP switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL	SLP			+VALW	+V	+VS	Clock
		SLP_S3#	SLP_S4#	SLP_S5#				
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

### BOARD ID Table(Page 25)

ID	BRD ID	Ra	Rb	Vab
0	R01 (EVT)	NC	0	0V
1	R02 (DVT)	100K	8.2K	0.25V
2	R03 (PVT)	100K	18K	0.50V
3	R10A (MP)	100K	NC	3.3V

### External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
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No PCI Device

### EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16)(02)	1010 000X b

### EC SM Bus2 address

Device	Address
EMC1402	1001 100X b

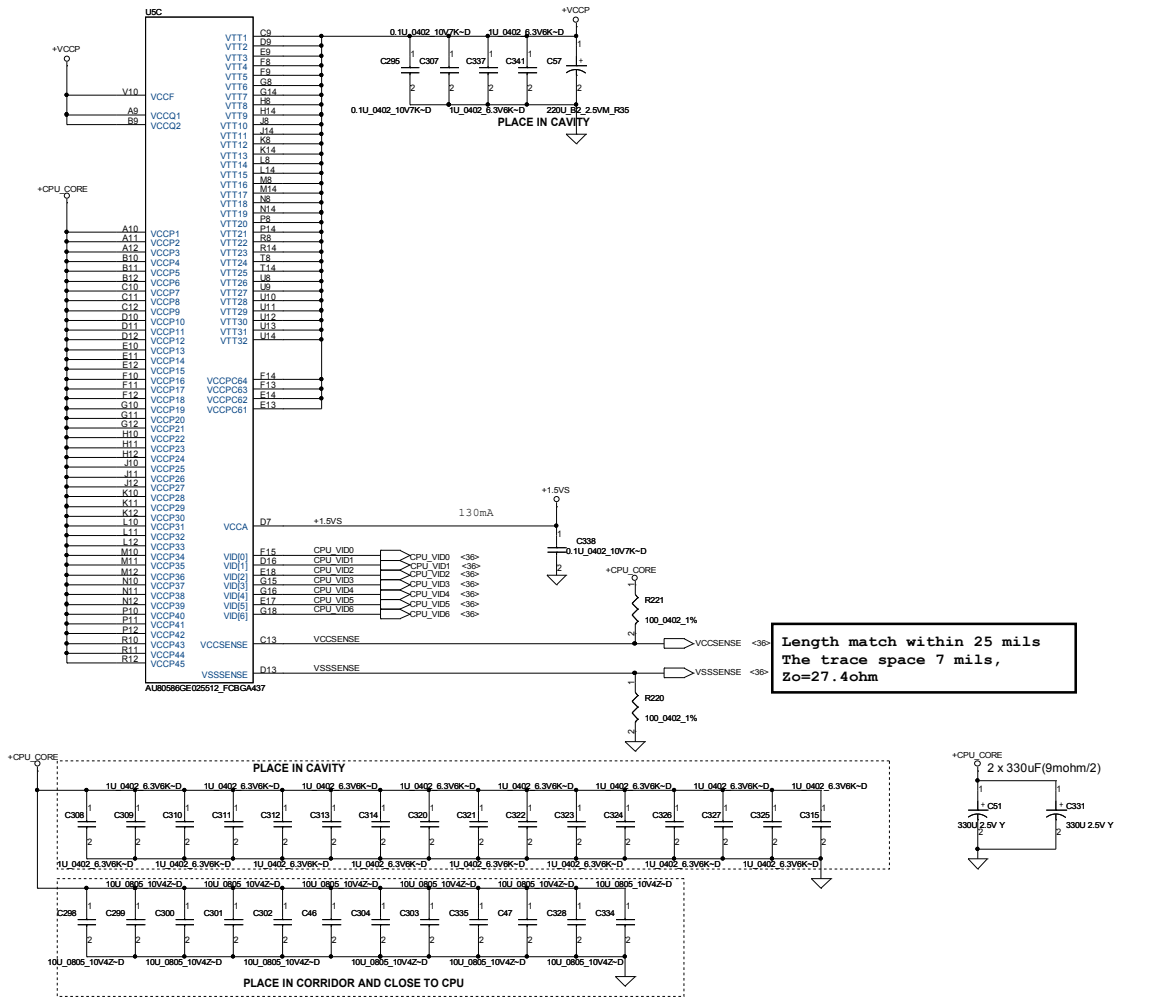
### ICH7M SM Bus address

Device	Address
Clock Generator (SL58P55SVTR)	1101 001Xb
DDR DIMMA	1010 000Xb

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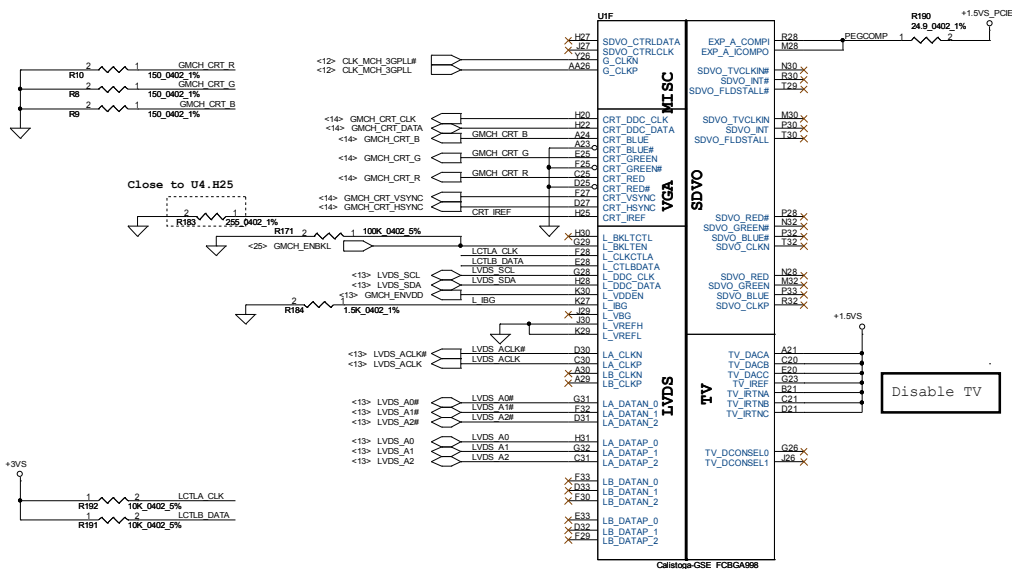


USD	NS
A2	VSS1
A4	VSS2
A6	VSS4
A8	VSS6
A10	VSS8
A12	VSS10
A14	VSS12
A16	VSS14
A18	VSS16
A20	VSS18
B1	VSS20
B3	VSS22
B5	VSS24
B7	VSS26
B9	VSS28
B11	VSS30
B13	VSS32
B15	VSS34
B17	VSS36
B19	VSS38
B21	VSS40
B23	VSS42
B25	VSS44
B27	VSS46
B29	VSS48
B31	VSS50
B33	VSS52
B35	VSS54
B37	VSS56
B39	VSS58
B41	VSS60
B43	VSS62
B45	VSS64
B47	VSS66
B49	VSS68
B51	VSS70
B53	VSS72
B55	VSS74
B57	VSS76
B59	VSS78
B61	VSS80
B63	VSS82
B65	VSS84
B67	VSS86
B69	VSS88
B71	VSS90
B73	VSS92
B75	VSS94
B77	VSS96
B79	VSS98
B81	VSS100
B83	VSS102
B85	VSS104
B87	VSS106
B89	VSS108
B91	VSS110
B93	VSS112
B95	VSS114
B97	VSS116
B99	VSS118
B101	VSS120
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B111	VSS130
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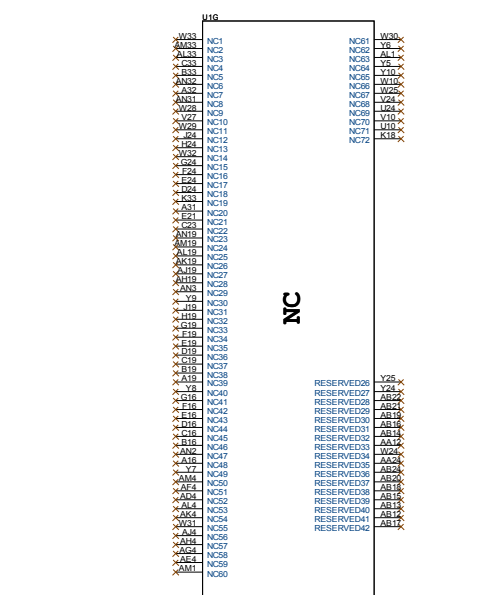
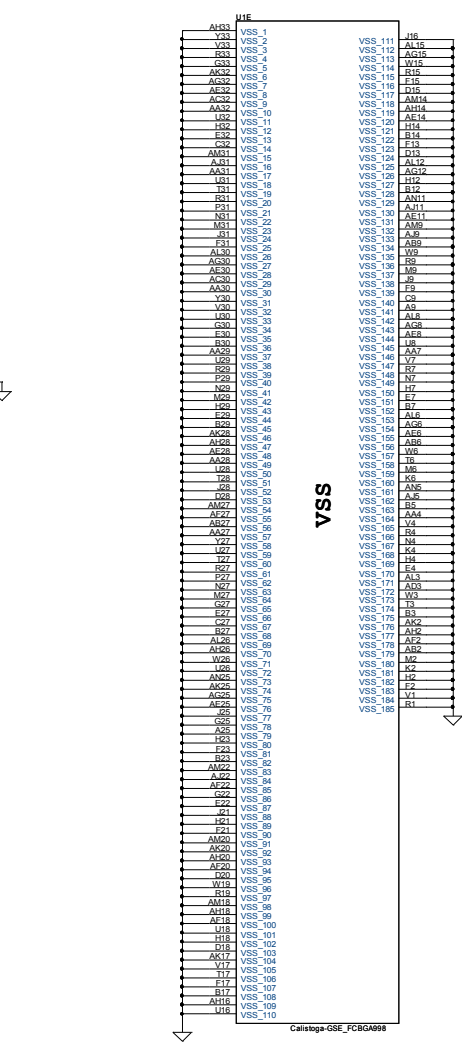
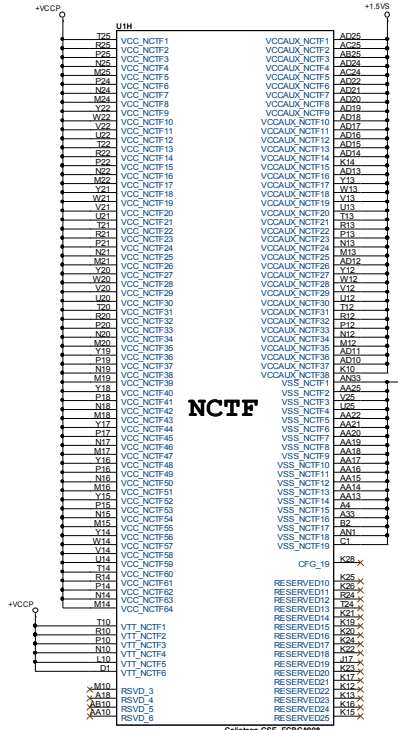




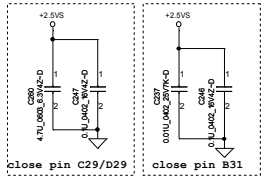
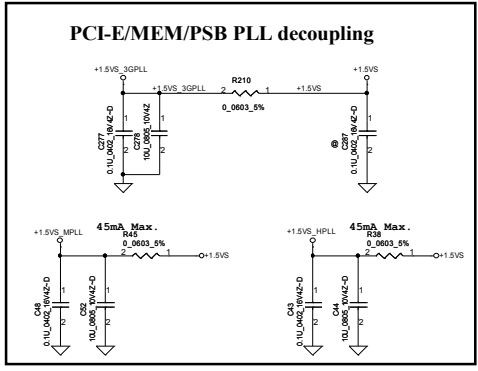
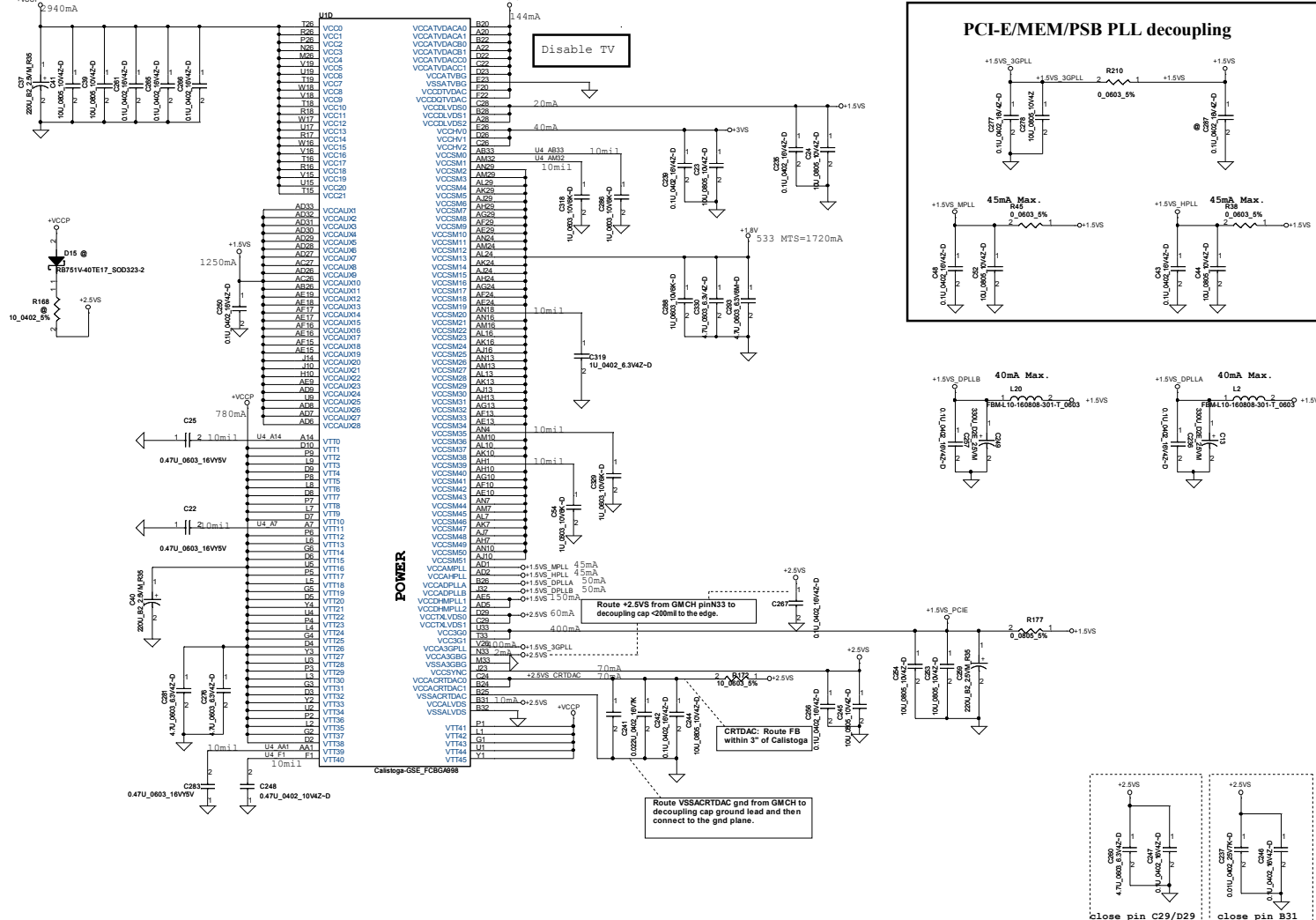


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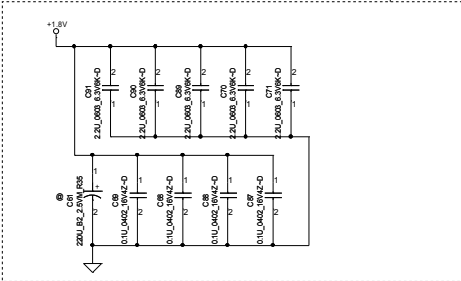
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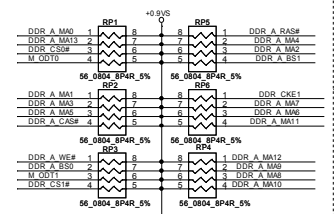
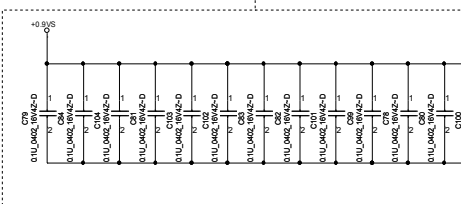
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- <-> DDR\_A\_DQS#(0..7)
- <-> DDR\_A\_DQ(0..63)
- <-> DDR\_A\_DM(0..7)
- <-> DDR\_A\_DQS(0..7)
- <-> DDR\_A\_MA(0..13)

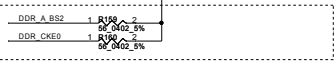
Layout Note:  
Place near JDIM1



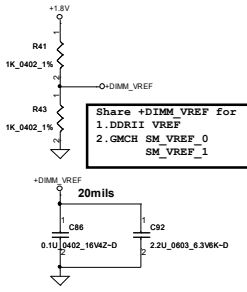
Layout Note:  
Place one cap close to every 2 pullup resistors terminated to +0.9VS



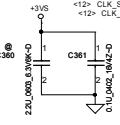
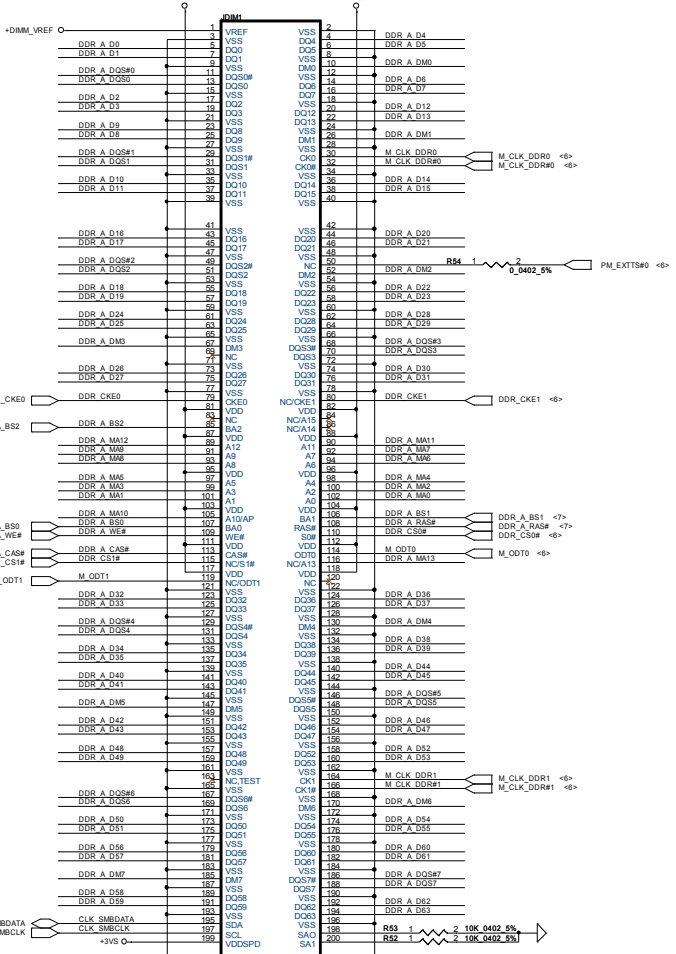
Layout Note:  
Place these resistor closely DIMMA, all trace length < 750 mil



Layout Note:  
Place these resistor closely DIMMA, all trace length Max=1.3"



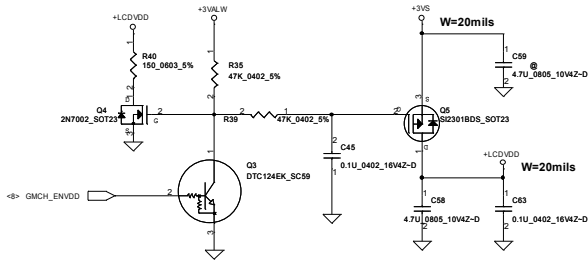
Shaze +DIMM VREF for  
1. DDRII VREF\_0  
2. GMCR SM\_VREF\_0  
SM\_VREF\_1



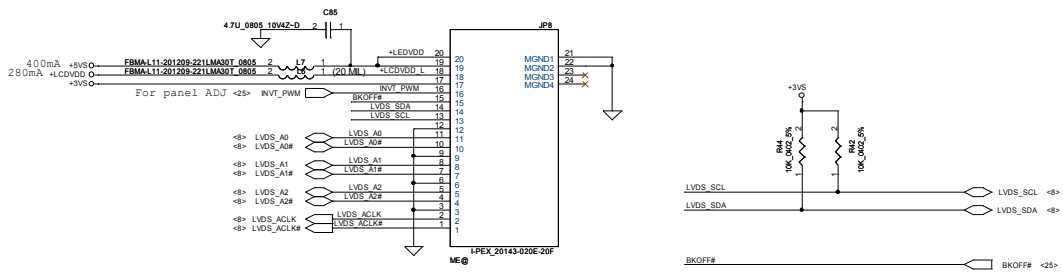
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### LCD POWER CIRCUIT

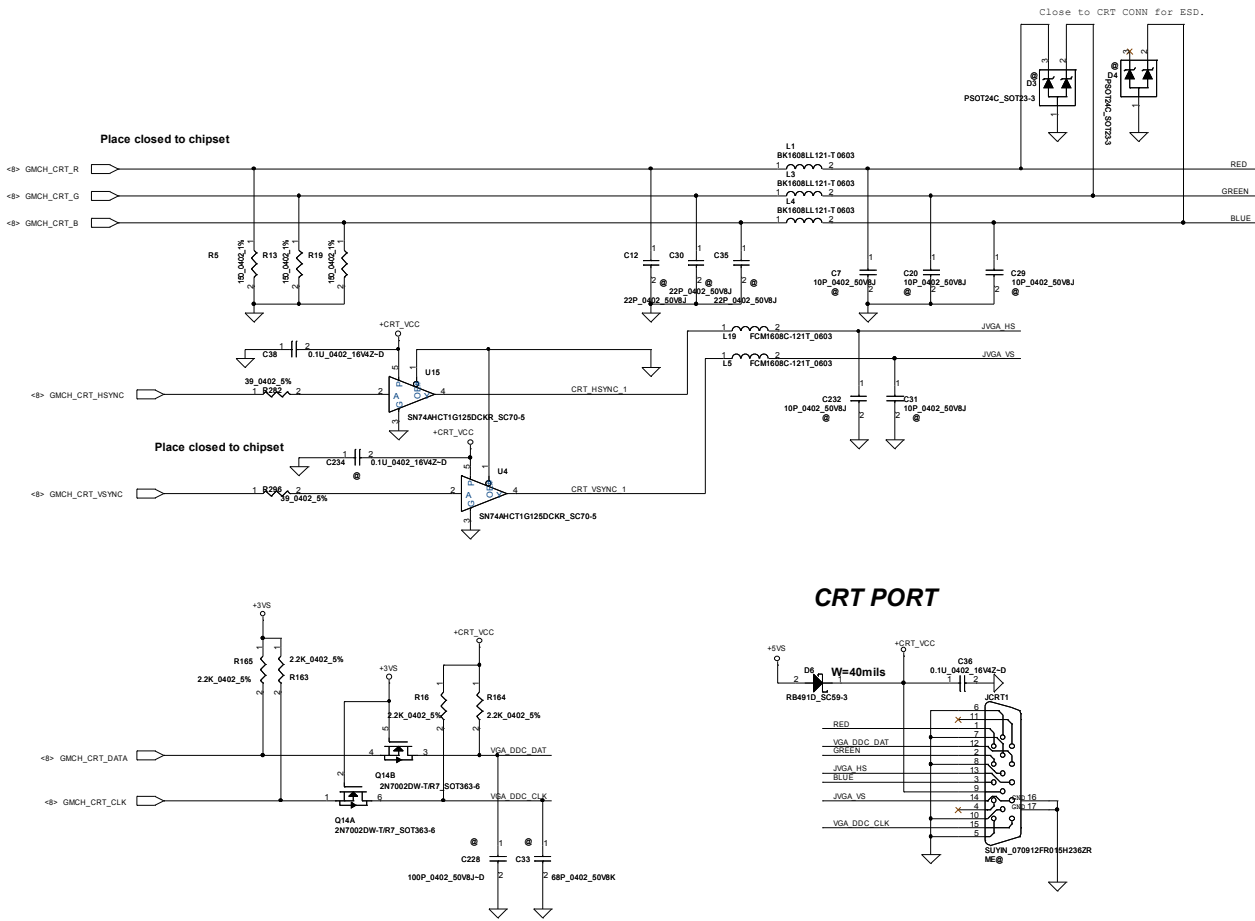


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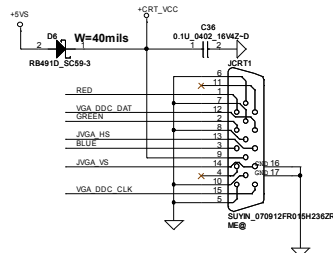


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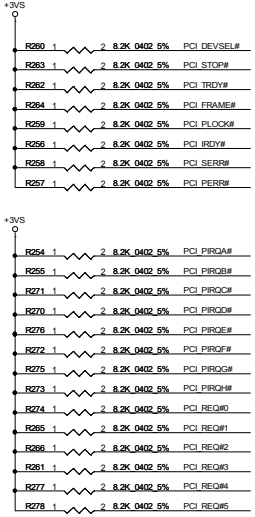
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**CRT PORT**



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Size	B	Document Number	LA-4421P	Rev	0.2
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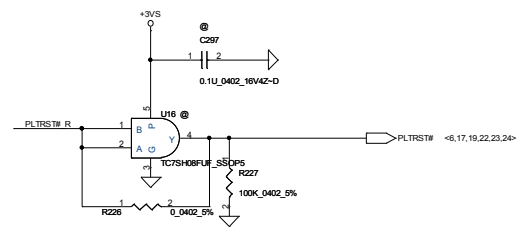
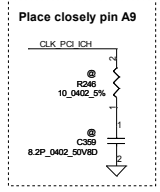
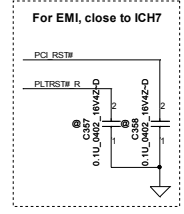
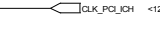
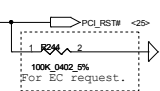
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✗E18	AD2	REQ1#
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✗E17	AD4	REQ2#
✗A18	AD5	GNT2#
✗A17	AD6	REQ3#
✗A15	AD7	GNT3#
✗E14	AD8	REQ4# / GPIO22
✗E14	AD9	GNT4# / GPIO4
✗E14	AD10	GPIO1 / REQ5#
✗E12	AD11	GPIO17 / GNT5#
✗E13	AD12	
✗E16	AD13	C/BE0#
✗E12	AD14	C/BE1#
✗E13	AD15	C/BE2#
✗E11	AD16	C/BE3#
✗D11	AD17	
✗D11	AD18	IRDY#
✗A11	AD19	PAR
✗A10	AD20	PCIRST#
✗E11	AD21	DEVSEL#
✗E10	AD22	PCIRST#
✗D9	AD23	PERRW
✗D9	AD24	PLOCK#
✗B9	AD25	SERRW
✗A6	AD26	STOP#
✗A6	AD27	TRDY#
✗C7	AD28	FRAME#
✗B6	AD29	
✗E6	AD30	PLTRST# R
✗D6	AD31	PCICLK
		PME#

Interrupt I/F		
PCI PIRQA#	A3	GPIO2 / PIRQE#
PCI PIRQB#	B4	GPIO3 / PIRQF#
PCI PIRQC#	C5	GPIO4 / PIRQG#
PCI PIRQD#	B5	GPIO5 / PIRQH#

MISC		
✗AES	RSVD[1]	AES
✗A02	RSVD[2]	AGC0
✗A04	RSVD[3]	AH0
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✗A02	RSVD[5]	F12
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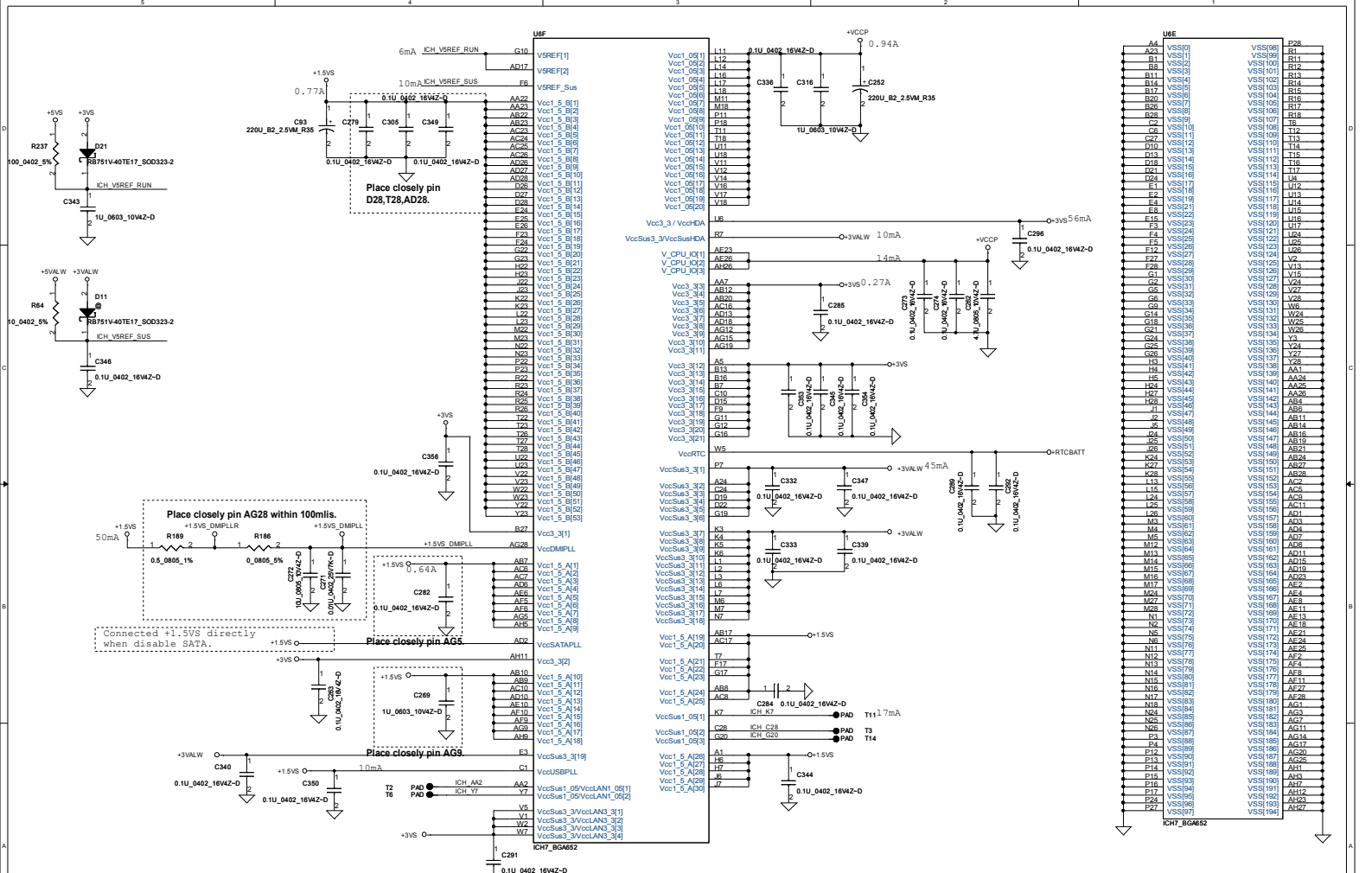


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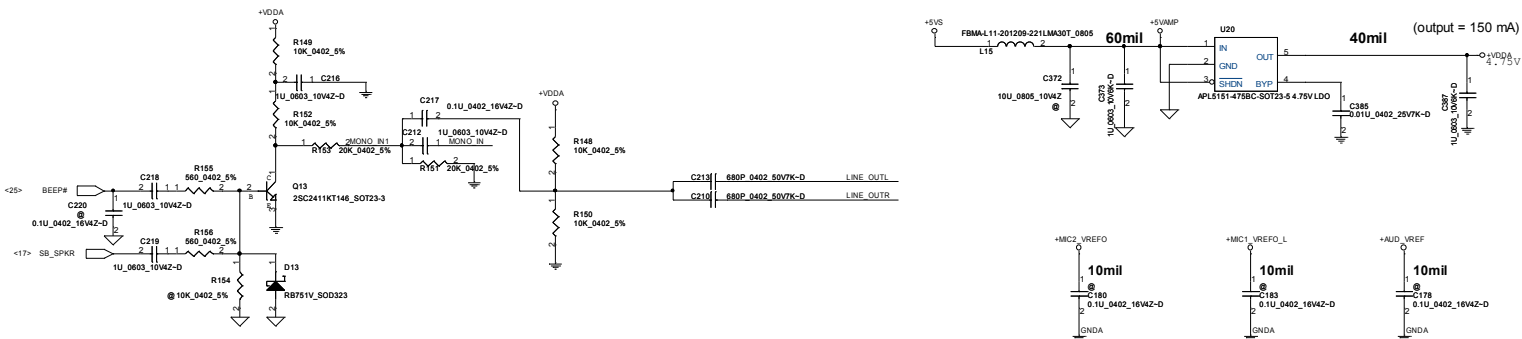




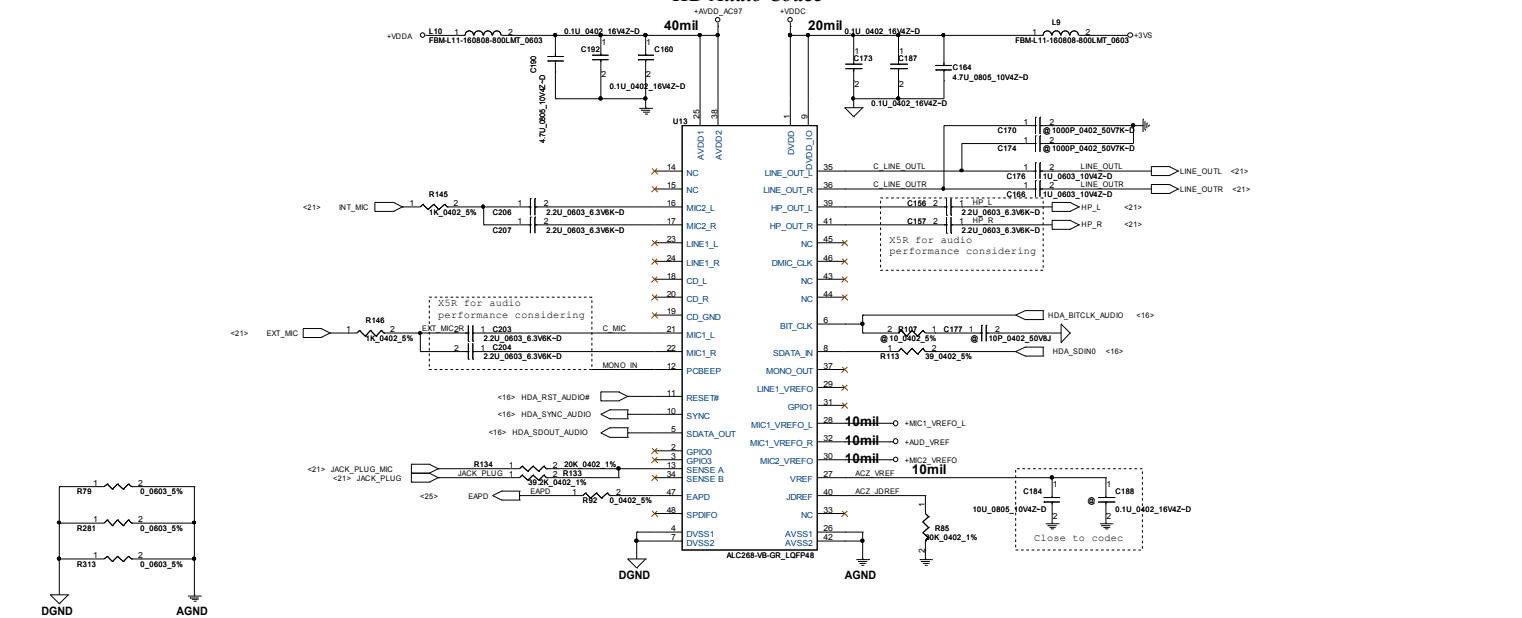


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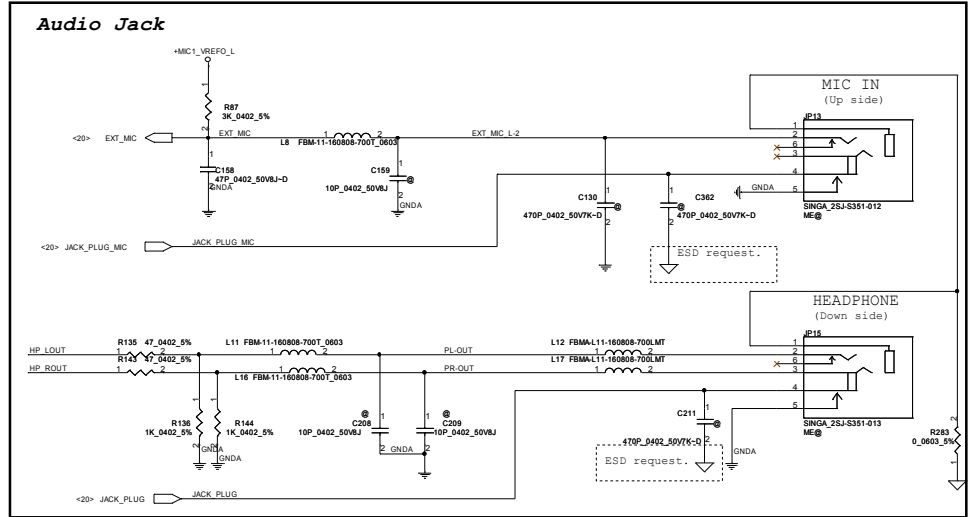
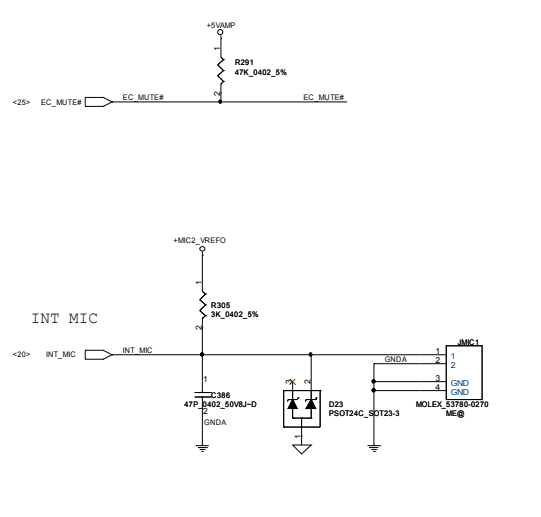
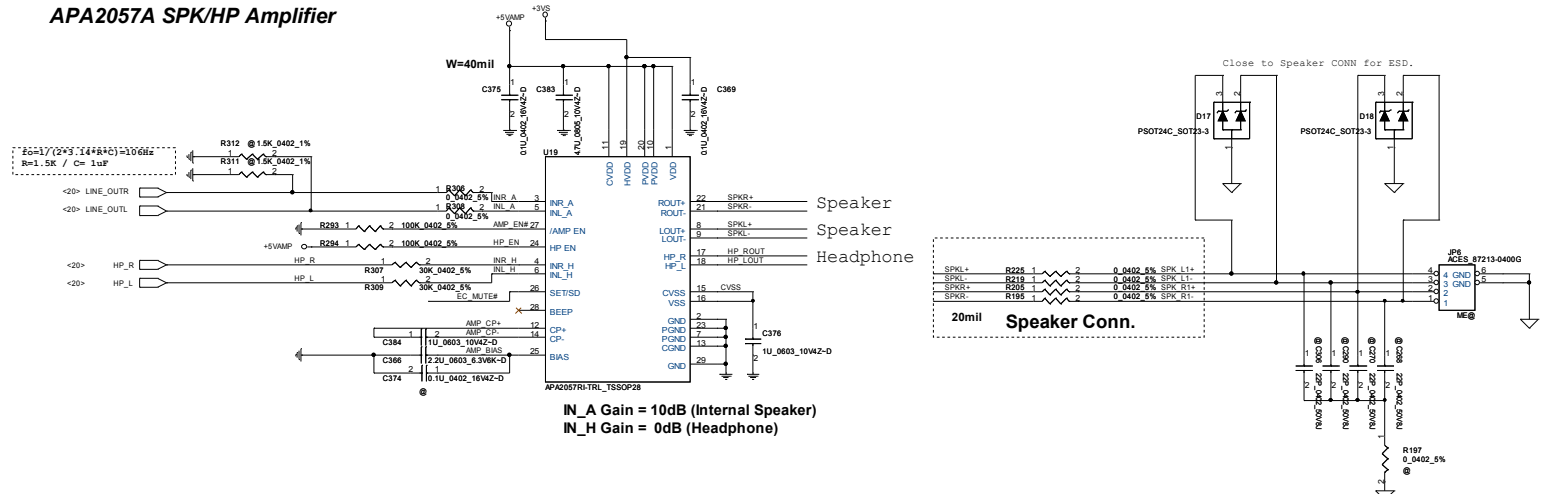


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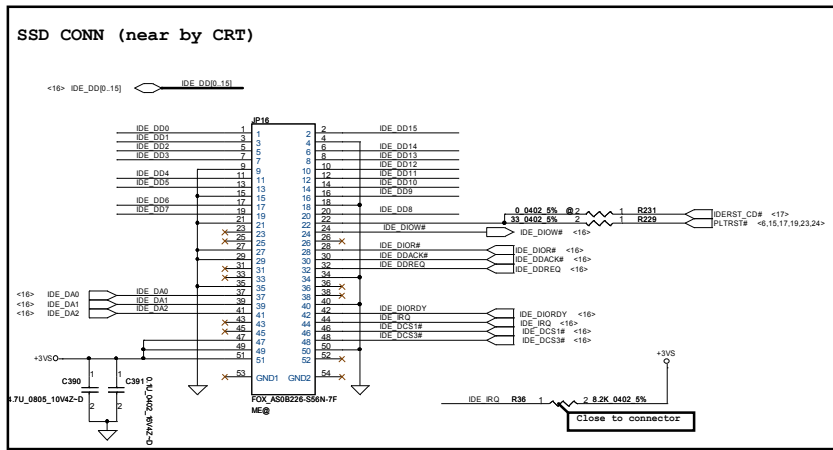
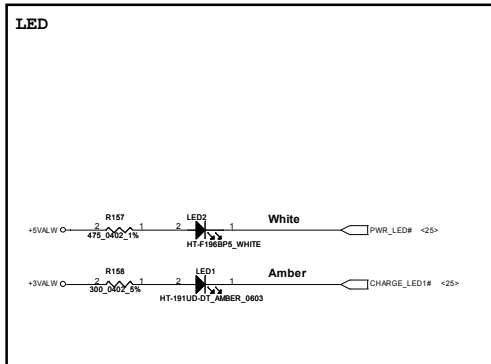
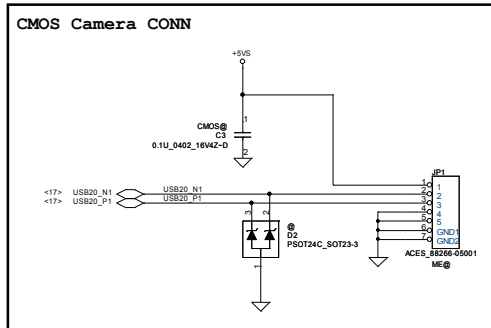


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Date	Friday, August 04, 2006	Sheet	26	of 40

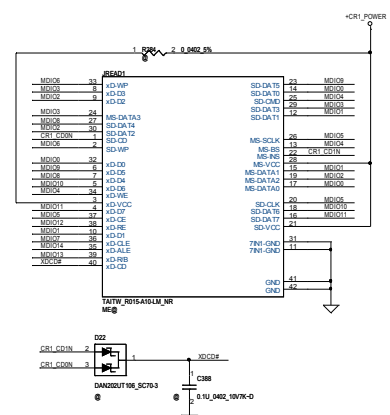
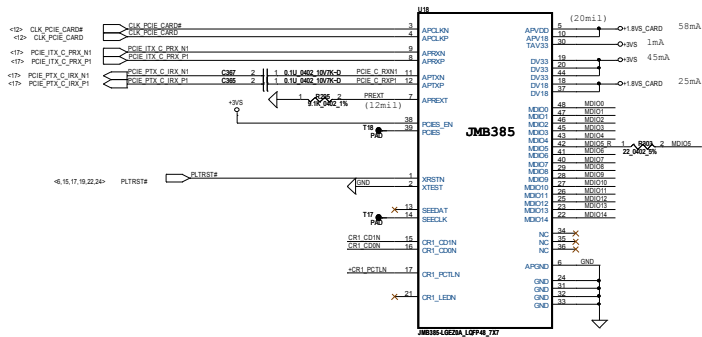
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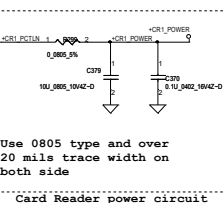
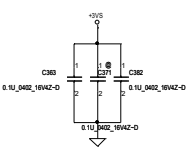
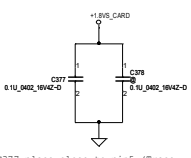
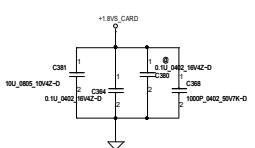
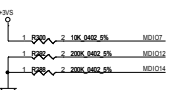
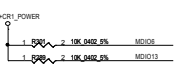


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**JMB385 Operation Modes**

Mode	Notes
XTEST	0
CRI_CDDN	X
CRI_CDLN	X



**SD,MMC,MS,XD multi-function pin define**

MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name	XD Card PIN Name
MDIO00	SD_DAT0	MMC_DAT0	MS_DAT0	XD_DAT0
MDIO01	SD_DAT1	MMC_DAT1	MS_DAT1	XD_DAT1
MDIO02	SD_DAT2	MMC_DAT2	MS_DAT2	XD_DAT2
MDIO03	SD_DAT3	MMC_DAT3	MS_DAT3	XD_DAT3
MDIO04	SD_CMD	MMC_CMD	MS_CS	XD_WE#
MDIO05	SDCLK1	MMCCLK	MSCLKR	XD_CE#
MDIO06	SD_WP#	MMC_WP#		XD_WP#
MDIO07				XD_CLE
MDIO08		MMC_DAT4	MS_DAT4	XD_DAT4
MDIO09		MMC_DAT5	MS_DAT5	XD_DAT5
MDIO10		MMC_DAT6	MS_DAT6	XD_DAT6
MDIO11		MMC_DAT7	MS_DAT7	XD_DAT7
MDIO12				XD_RS#
MDIO13				XD_R/B#
MDIO14				XD_ALE

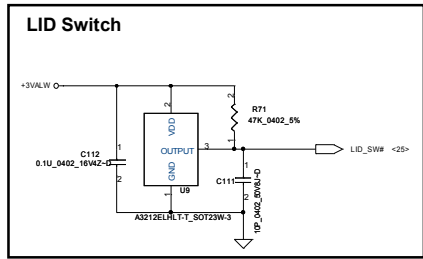
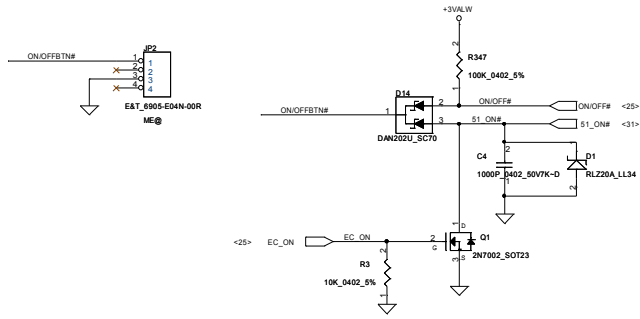
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Size	Custom	Document Number	Date: Friday, August 08, 2009	

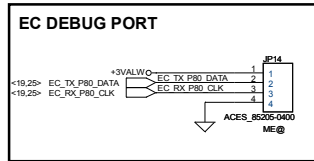
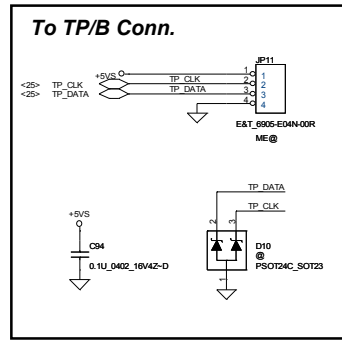
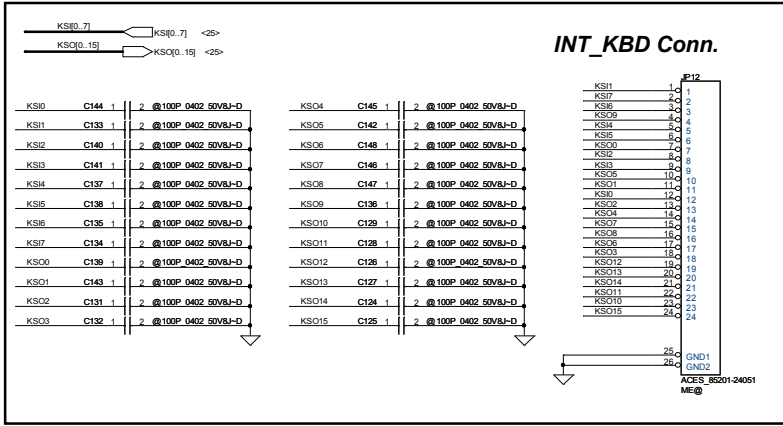




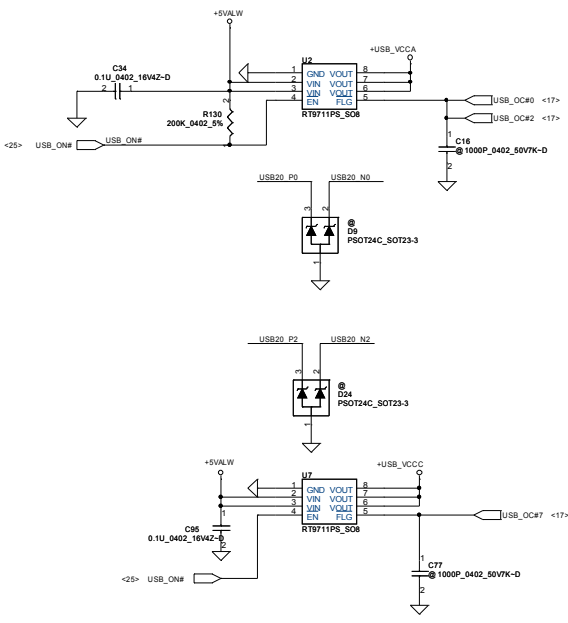




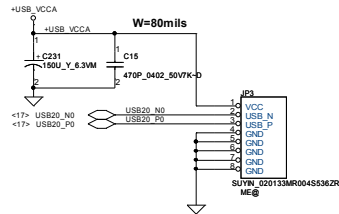
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Size B	Rev 0.2	Sheet 26	of 40	



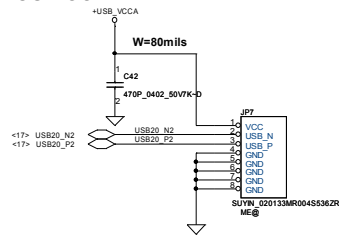
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				Date	Friday, August 08, 2008



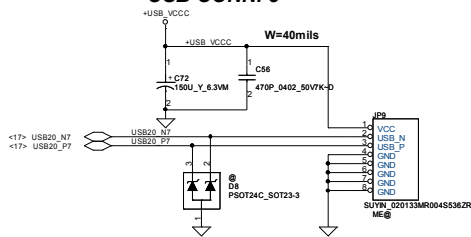
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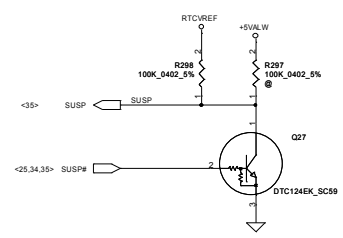
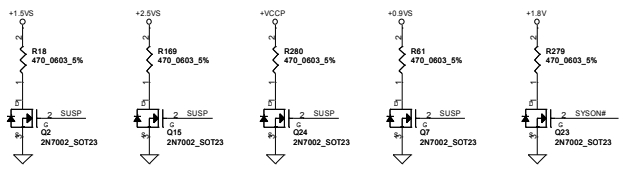
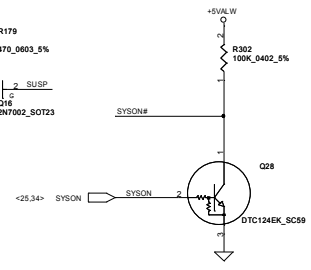
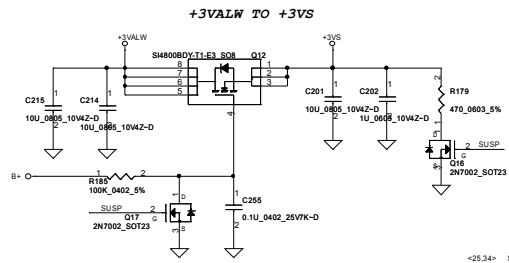
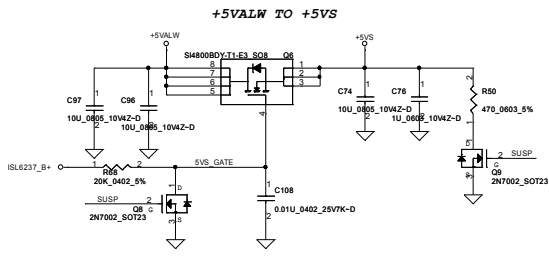
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**USB CONN. 3**



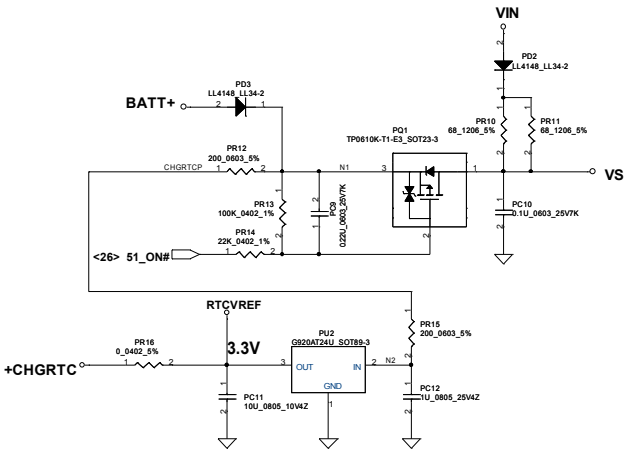
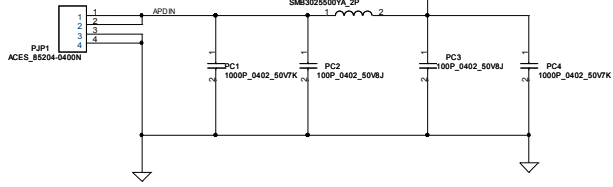
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Size	B	Document Number	LA-4421P	Rev	0.2
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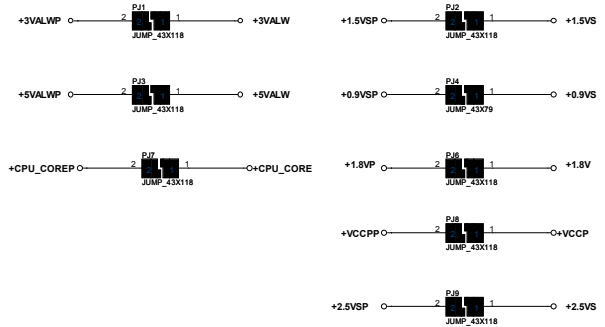
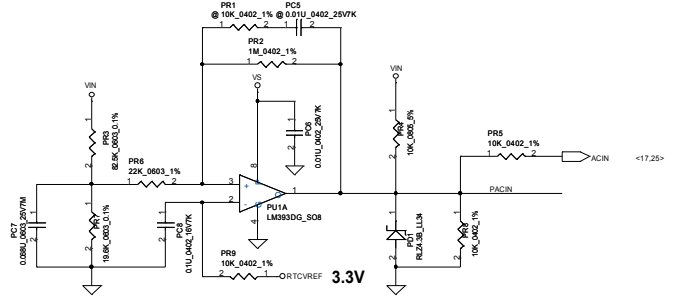


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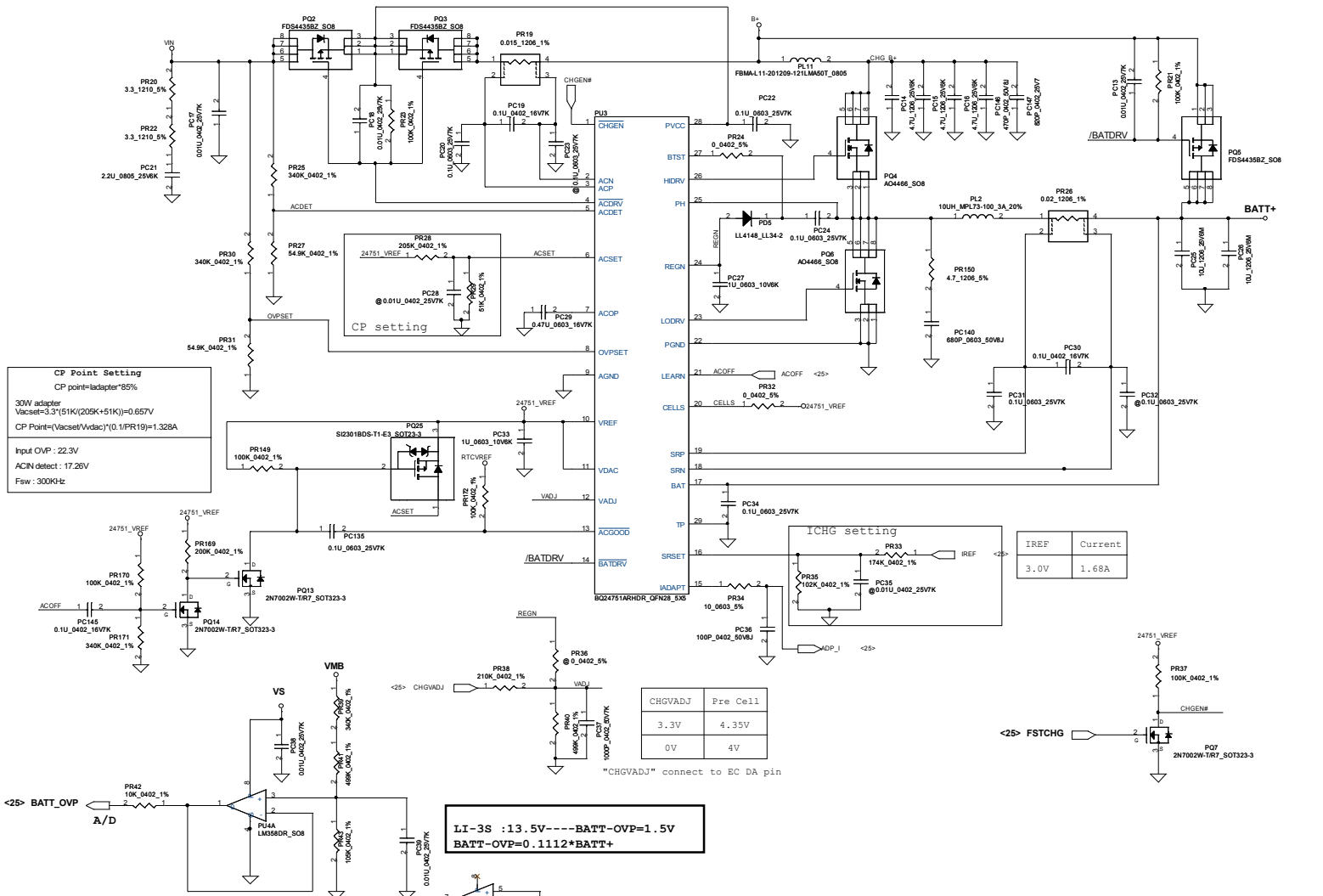


SP02000D000

Vin Detector		
High	18.059	17.841
Low	17.418	16.998



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				DCIN & DETECTOR
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**CP Point Setting**  
 CP point=ladder\*85%  
 30W adapter  
 $V_{acset}=3.3 \cdot (51K / (205K + 51K)) = 0.65V$   
 $CP \text{ Point} = (V_{acset} / V_{vdac}) \cdot (0.1 / PR19) = 1.328A$

Input OVP : 22.3V  
 ACIN detect : 17.26V  
 Fsw : 300KHz

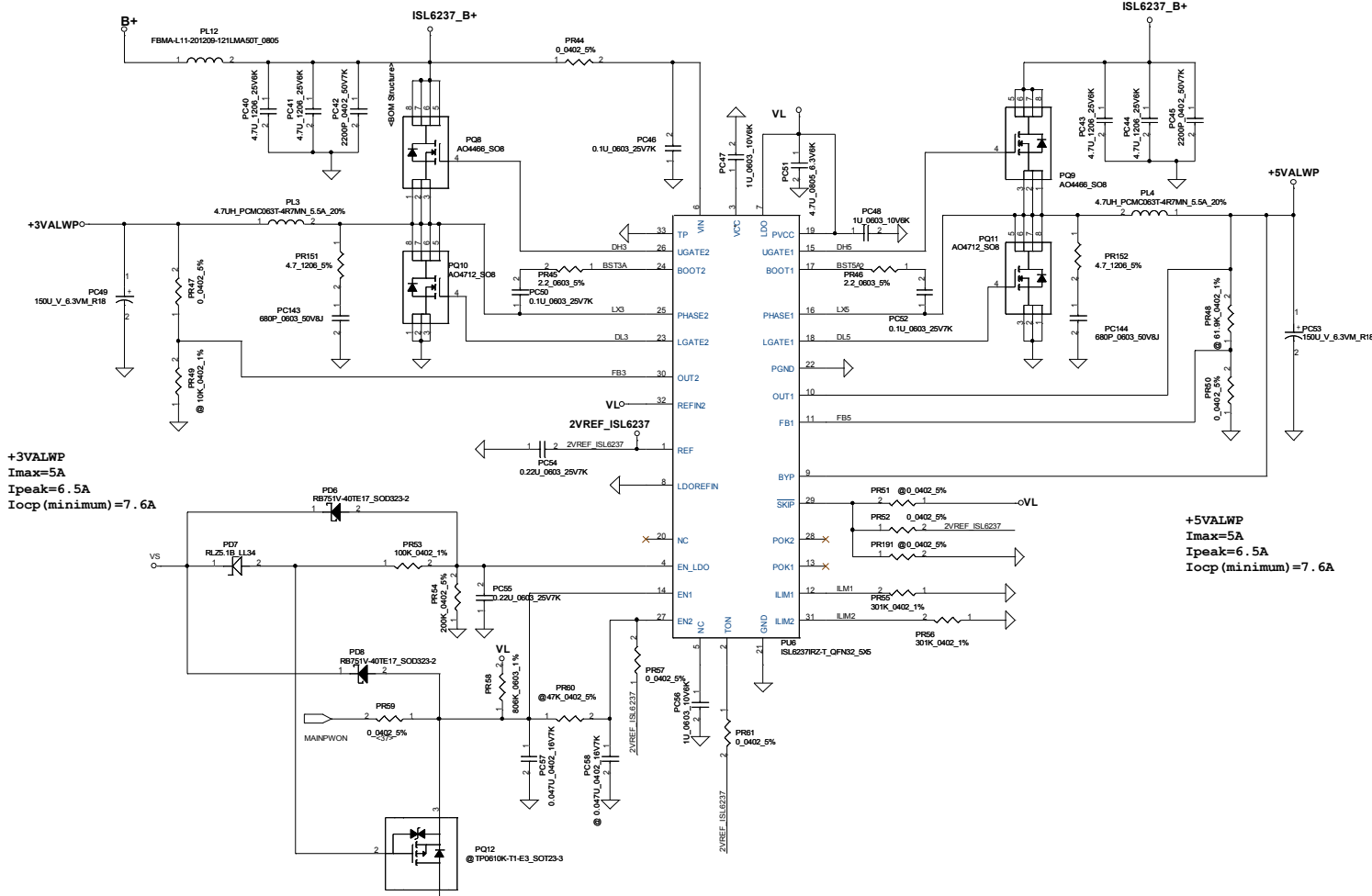
**LI-3S : 13.5V --- BATT-OVP=1.5V**  
**BATT-OVP=0.1112 \* BATT+**

CHGVADJ	Pre Cell
3.3V	4.35V
0V	4V

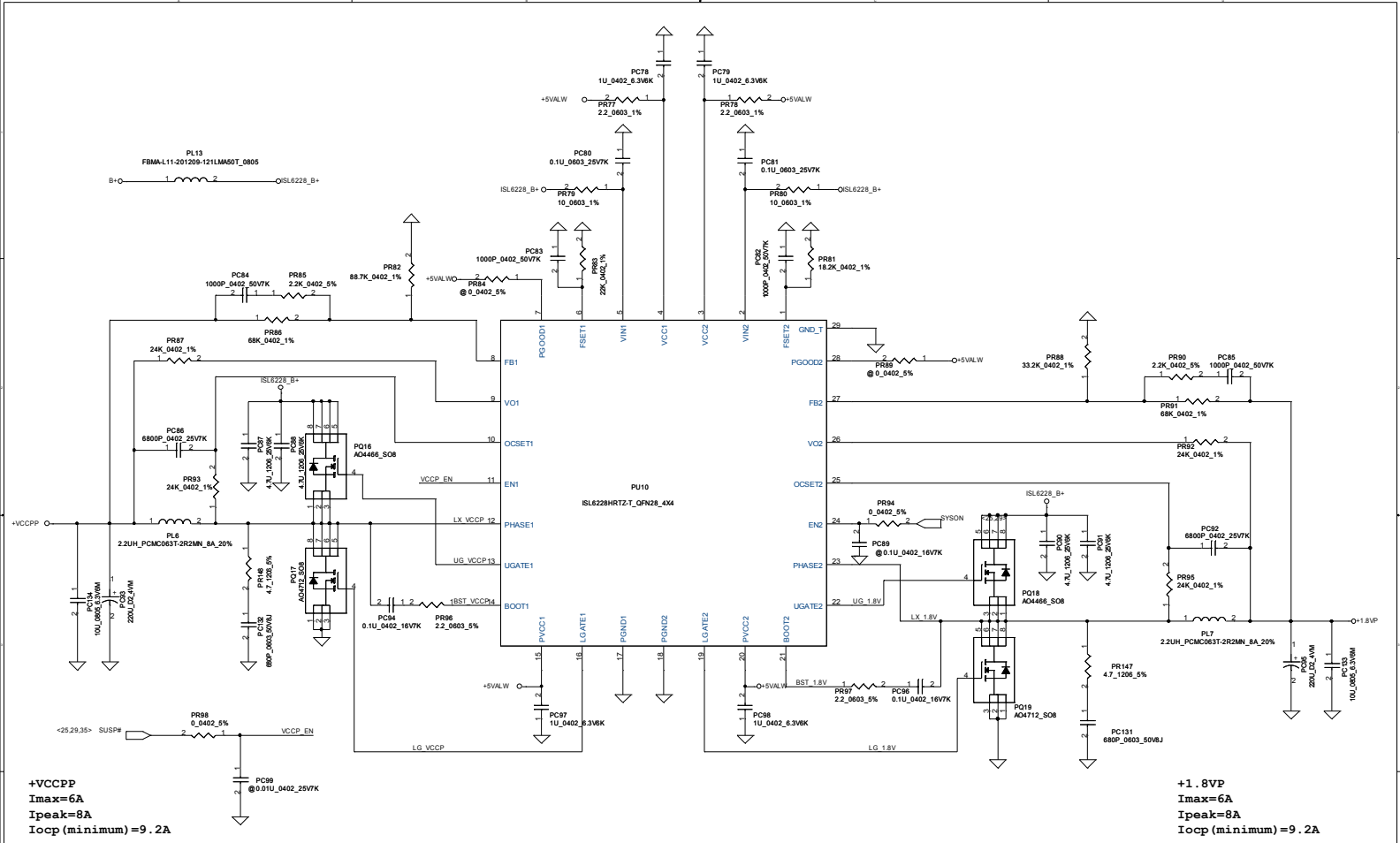
IREF	Current
3.0V	1.68A

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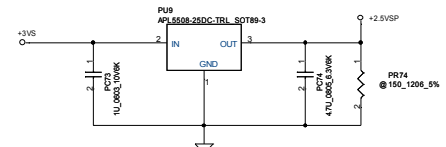
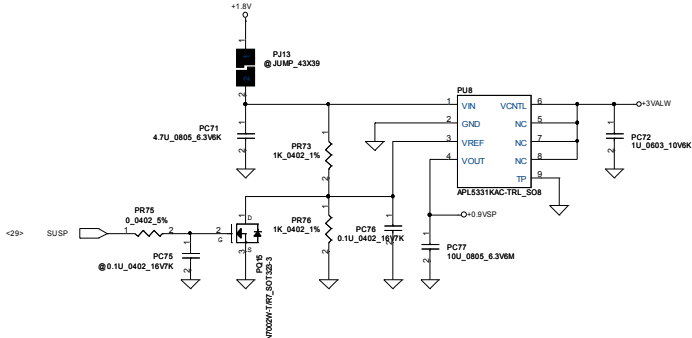
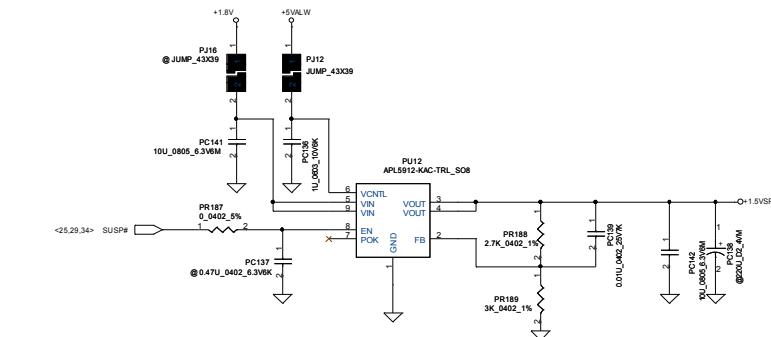
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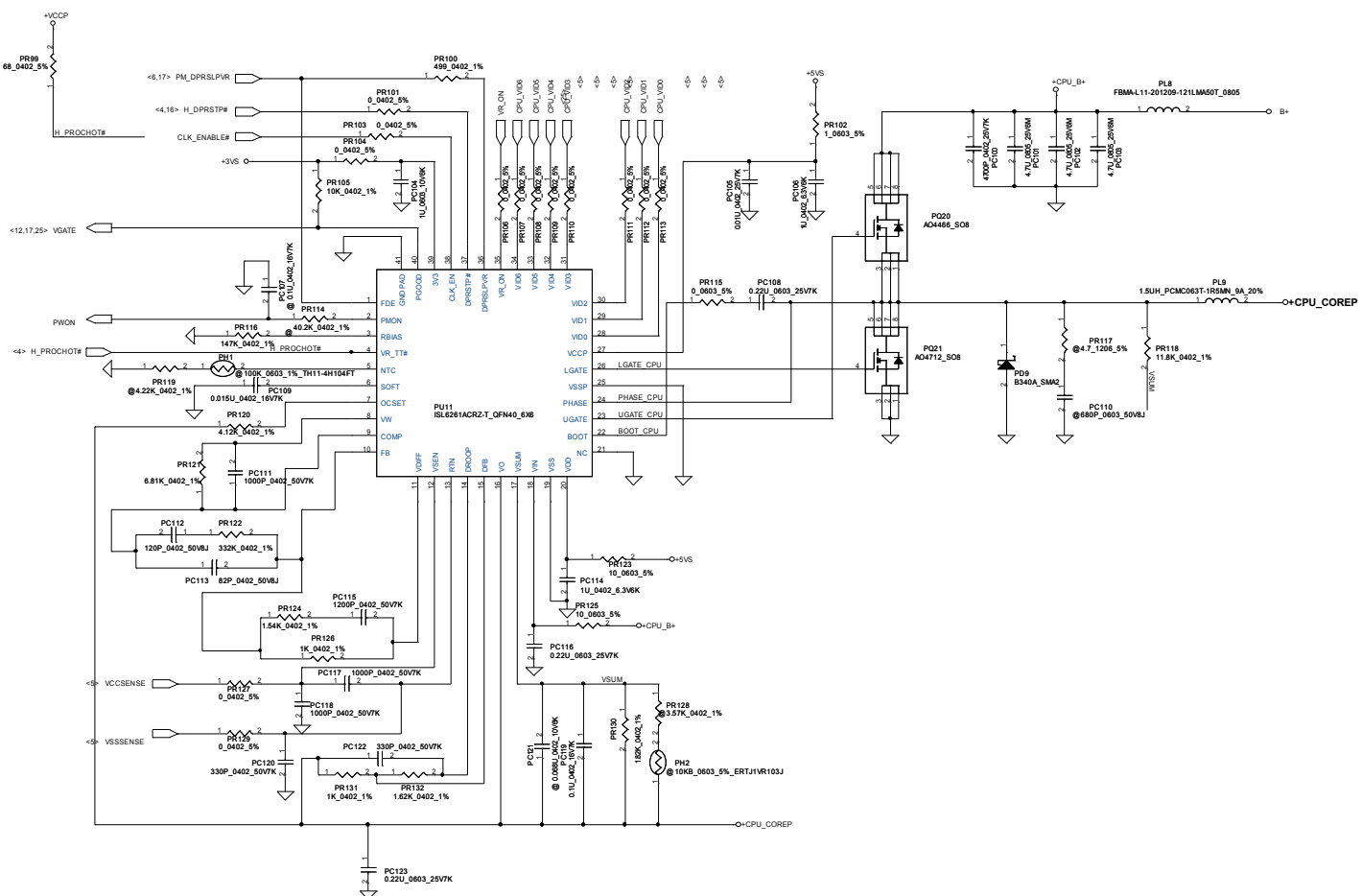
+VCCPP  
 Imax=6A  
 Ipeak=8A  
 Iocp (minimum)=9.2A

+1.8V  
 Imax=6A  
 Ipeak=8A  
 Iocp (minimum)=9.2A

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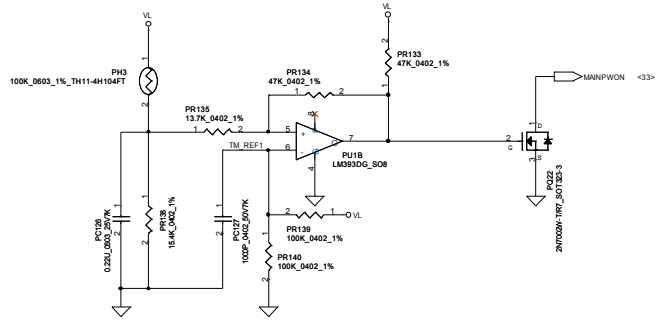
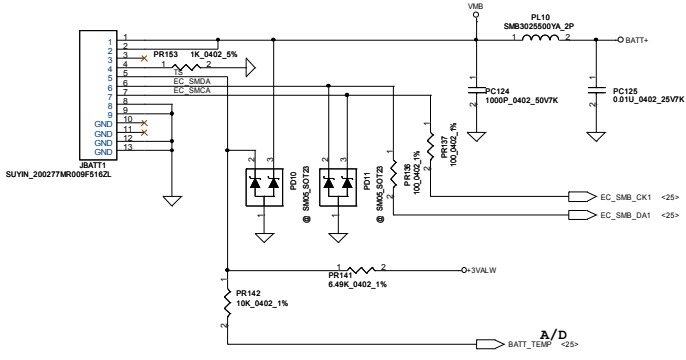


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PH3 under CPU bottom side :  
 CPU thermal protection at 92 degree C  
 Recovery at 56 degree C



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				BATTERY CONN / OTP
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Item	Fixed Issue	Rev.	PG#	Modify List
1	Deleted Kill switch circuit.	0.2	P26	1.Deleted R60,C85,SW2
2	Changed to Dell PN.	0.2	---	1.Change C308,309,310,311,312,313,314,315,320,321,322,323,324,325,326,327,337,341 from SE00000K80 (0402) to SE00000K8L (0402) 2.Change C46,47,298,299,300,301,302,303,304,328,334,335 from SE000005TM8 (0603) to SE00000480L (0805) 3.Change C22,25,248,283 from SE1244748K0 (0402) to SE02747428L (0603) 4.Change C108,255,238 from SE042104R80 (0603) to SE068103K8L (0402) 5.Change C11,369,376,384 from SE100105Z80 (0402) to SE052105Z8L (0603) 6.Change C44,52 from SE077106M80 (1206) to SE053106Z8L (0805) 7.Change C373 from SE054106Z80 (1206) to SE053106Z8L (0805) 8.Change C260,276,281,293,330 from SE107475K80 (0603) to SE053475Z8L (0805) 9.Change C92 from SE064225K80 (0805) to SE107225K8L (0603) 9.Change C54,286,288,318,319,329 from SE100105Z80 (0402) to SE080105K8L (0603)
3	Use LAN internal EEPROM and CLKREQ	0.2	P24	Unstuff U3 C32, R173 stuff R170 R111
4	LCD sequence	0.2	P13	Change R35,39 to 47K ohm and C45 to 0.1u
5	Changed to Dell PN.	0.2	P28	U2,7 change from SA00001H600 (Dell not approve) to SA000017B00 part
6	Add C390 and 391 for SSD	0.2	P22	Add C390 and 391 and unstuff C59 for SSD
7	Follow LAN report	0.2	P24	Short C22,226, C229,230 change from 2p to 30p
8	Follow checklist	0.2	P10	Delete C280
9	Changed to Dell PN.	0.2	P6	Change R167,180 to SD00000680L
10	Follow power sequence	0.2	---	Unstuff D11 D15 R168 SW1
11	Change symbol	0.2	P11	Update DIMM termination to 8P4R
12	Remove LED function	0.2	---	Delete Q25,26,11,22,LED3,R159,JP4 Change LED2 to white
13	EC code for B phase	0.2	P25	R126 change 0ohm to 8.2K ohm and stuff R120
14	For derating report	0.2	P20	Change R148,149,150,152 to 10k ohm
15	EA test	0.2	P25	C123,150 change from 15p to 22p
16	EA test	0.2	P23	Change R295 to 9.1K ohm
17	EA test	0.2	P14	GMCH_CR1_VSYNC and GMCH_CR1_HSYNC add R282,296 390ohm
18	single part	0.2	P24	R193 change to 47k ohm
19	SPEC change	0.2	P19	Change BT pin define
20	improve power consumption	0.2	P29	Change R298 to 100K
21		0.2	P25	Unstuff C194
22	ME change	0.2	P13	Change LVDS connect to 20pin
23	Dell request	0.2	---	Change M/B to OSP
24		0.2	P22	Delete LPC debug connect (JP20,R102,296)
25		0.2	P13	Add C95 for +1.8VDD, Delete R46,C55
26		0.2	P21	Delete L21,C383 change to 4.7u,unstuff C374,R291 change to 47k ohm
27		0.2	P20	Change U20 to Anpec and Delete R304,310 change C373,387 to 1u Delete L18,unstuff C372,Change C369 to 0.1u
28	Change EC susp# to 116 pin PBTN_out# to 117 pin LID_SW# to 109 pin EC_PME# to 118 pin	0.2	---	Change EC_Therm# 25 to 115 pin BT_OFF# 98 to 106 pin WL_OFF# 106 to 98 pin Delete R290,285
29		0.2	---	Delete R290,285
30	DFX request	0.3	P21	Change JP13,15 PCB footprint from SINGA 28J-8351-012 EP to FOX JW63331-B350-7F EP
31	EC code for C phase	0.3	P25	R126 change 18Kohm
32	ENE request	0.3	P25	C116 change to 1u
33		0.3	---	Delete R215, Change netname +RTCVCC to +RTCBATT ,Add J6 D19, C191 with C185 switch,
34	EMI request	0.3	---	Add C389
35	LAN LED	0.3	---	Add R46 and C55 LAN LED add orange
36	ENE request	1.0	P25	C116 change to 4.7u
37		1.0	---	Delete J1,JP,SW1,JP18
38		1.0	---	C127 change to 1000p

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<b>Compal Electronics, Inc.</b>	
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Change RTC battery to CR2032.	To meet customer specification (3 years).	R.02	31	Add PD12 (RB751) and PR190 (1K).	20080428	DVT
2	Adjust Vin detector setting.	Change Vin "High==>Low" voltage from 14.355V to 17.210V.	R.02	31	Change PR6 to 22K and PR7 to 19.6K.	20080428	DVT
3	Adjust VCCP OCP setting.	Change VCCP OCP to 9A.	R.02	34	Change PR87 and PR93 to 24K and PC86 to 6800P.	20080428	DVT
4	Adjust 1.8V output voltage.	Change 1.8V power rail voltage from 1.8V to 1.828V.	R.02	34	Change PR88 from 34K to 33.2K.	20080428	DVT
5	Change Vin and battery discharge MOSFET.	Due to SI4835BDY will EOL, so, we change to Compal standard 2nd source, FDS4435BZ.	R.02	32	Change PQ2, PQ3 and PQ5 from SI4835BDY to FDS4435BZ.	20080428	DVT
6	Change battery connector.	The new battery connector has screw hole.	R.02	32	Change battery connector.	20080430	DVT
7	Power board-band.	EMI requests to add solution to reduce power board-band.	R.02	32 33 34	Change PJ10, PJ11 and PJ14 from Jump to bead. Change PR45, PR46, PR96 and PR97 from 0 ohm to 2.2 ohm. Add PR151, PR152, PC143, PC144, PR147, PR148, PC131, PC132, PC146, PC147, PR150 AND PC140.	20080506	DVT
8	Modify CPU CORE OCP.	Change CPU CORE OCP from 10A to 7A.	R.02	36	Change PR120 from 5.9K to 4.12K.	20080514	DVT
9	Remove PR16 and PR17.	Change RTC battery, so, remove PR17 and PR16.	R.03	31	Delete PR17 and change PR16 to 0 Ohm.	20080605	FVT
10							
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Issued Date		Deciphered Date		PIR (PWR)	
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				Customer	<DOC>
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Item	Fixed Issue	Rev.	PG#	Modify List
1	Deleted Kill switch circuit.	0.2	P26	1.Deleted R60,C85,SW2
2	Changed to Dell PN.	0.2	--	1.Change C309,309,310,311,312,313,314,315,320,321,322,323,324,325,326,327,329,341 from SE000000K80(0402) to SE000000K8L(0402) 2.Change C46,47,298,299,300,301,302,303,304,328,334,335 from SE000005TM8(0603) to SE00000480L(0805) 3.Change C22,25,248,283 from SE1244748K0(0402) to SE02747428L(0603) 4.Change C108,255,238 from SE042104K80(0603) to SE068103K8L(0402) 5.Change C11,369,376,384 from SE100105Z80(0402) to SE052105Z8L(0603) 6.Change C44,52 from SE077106M80(1206) to SE053106Z8L(0805) 7.Change C373 from SE054106Z80(1206) to SE053106Z8L(0805) 8.Change C260,276,281,293,330 from SE107475R80(0603) to SE053475Z8L(0805) 9.Change C92 from SE064225K80(0805) to SE107225K8L(0603) 9.Change C54,286,288,318,319,329 from SE100105Z80(0402) to SE080105K8L(0603)
3	Use LAN internal EEPROM and CLKREQ	0.2	P24	Unstuff U3 C32 R173 stuff R170 R111
4	LCD squence	0.2	P13	Change R35,39 to 47K ohm and C45 to 0.1u
5	LVDS connect	0.2	P13	LVDS connector change to 20 pins
6	Changed to Dell PN.	0.2	P28	U2,7 change from SA00001H600(Dell not approve) to SA000017B00 part
7	EA test	0.2	P23	Change R295 to 9.1k ohm
8	Follow LAN report	0.2	P24	Short C222,226, C229,230 change from 27p to 30p
9	Delete A -phase reserve	0.2	P20	Delete L18,
10	Changed to Dell PN.	0.2	P6	Change R167,180 to SD00000680L
11		0.2		Change M/B to OSP
12		0.2		
13	Remove LED function	0.2	--	Delete Q25,26,11,22,LED3,R159 Change LED2 to white
14	EC code for B phase	0.2	P25	R126 change 0ohm to 8.2k ohm and stuff R120
15	For derating report	0.2	P20	Change R148,149,150,152 to 10k ohm
16	EA test	0.2	P25	C123,150 change from 15p to 22p
17		0.2	P13	Add C85 for +LEDVDD
18		0.2	P22	Delete LPC debug connect (JP20,R102,296)
19	ENE	0.2	P25	change SUSP# to U8.116 due to KB926 C0 bug
20	SSD	0.2	P22	add C390&C391 for Dell consign SSD
21	LED	0.2	P22	add white LED
22		0.2		
23		0.2		
24				

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Title	HW PIR	
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