

COMPAL CONFIDENTIAL

MODEL NAME : 888L2(SOLANO2-M)

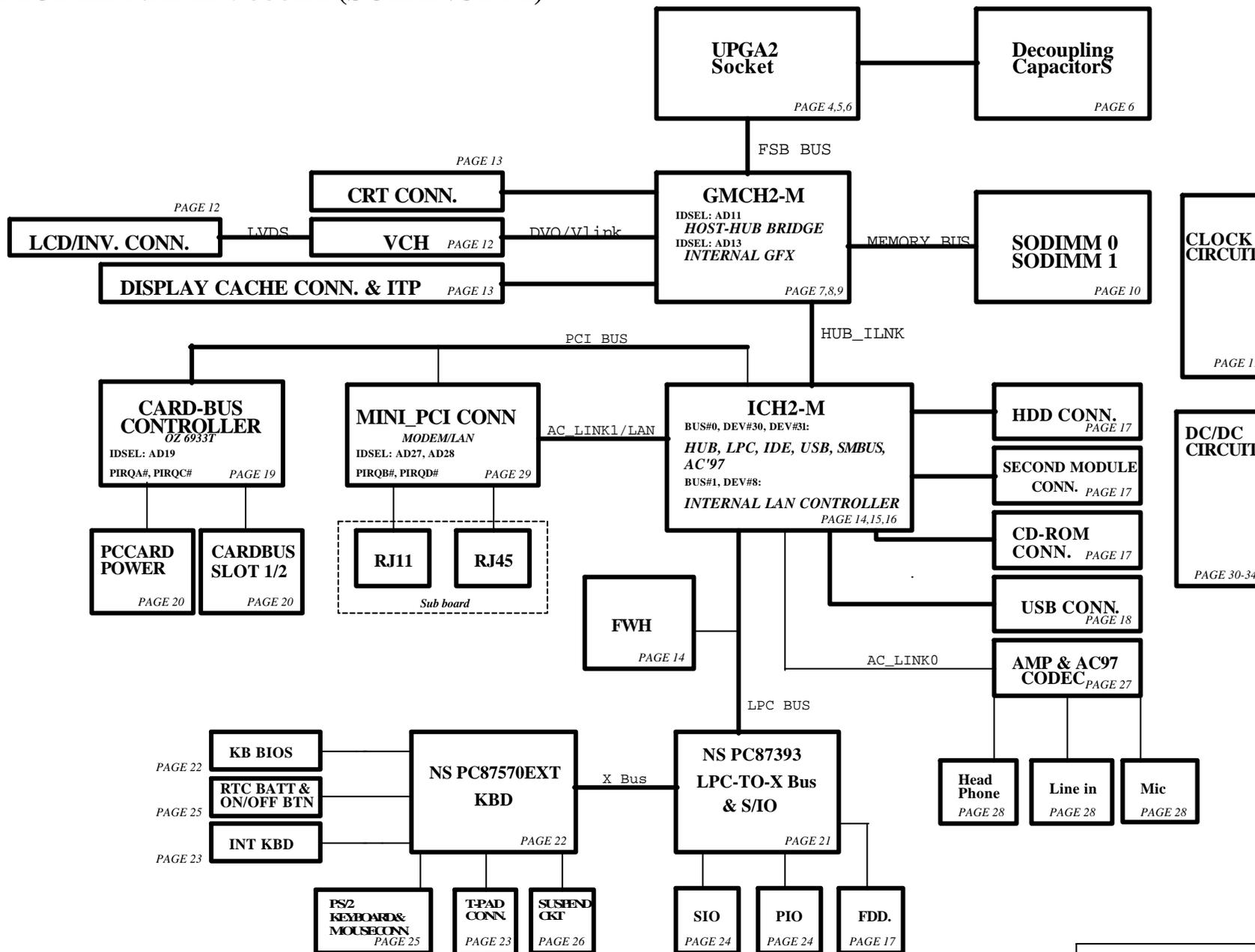
Date: 01/11/01

Version: 2.0

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CLOCK
CIRCUIT
PAGE 11

DC/DC
CIRCUIT
PAGE 30-34

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Revision History			
#	Date	Description	Version
1	2000/7/21	First Release (<i>EVT-SST</i>)	0.1
2	2000/9/20	Second Release (<i>DVT1-PT1</i>)	0.2A
3	2000/11/3	Third Release (<i>DVT2-PT2</i>)	0.2C1
4	2000/12/27	Fouth Release (<i>ST</i>)	1B
5	2001/01/11	fifth release (<i>QT</i>)	2.0

Chip information

GMCH2-M FW82815EM

Version	S-spec.	Q-spec.
A0		QA38
A1	SL4MP	QA75

ICH2-M FW82801BAM

Version	S-spec.	Q-spec.
A0		Q908, Q909, Q910, Q911, Q912
B0	SL45HQ	Q967, Q968
B1	SL4HN	QA36, QA37
B2		QA56, QA57

VCH FW82807AA

Version	S-spec.	Q-spec.
A0		Q989
A1		QA76
A2		QB41ES

EVT (SST)

GMCH2-M	QA38ES (A0)
ICH2-M	Q967ES (B0)
VCH	Q989ES (A0)

DVT1 (PT1)	DVT2 (PT2)
GMCH2-M	QA75ES (A1)
ICH2-M	QA57ES (B2)
VCH	Q076ES (A1)

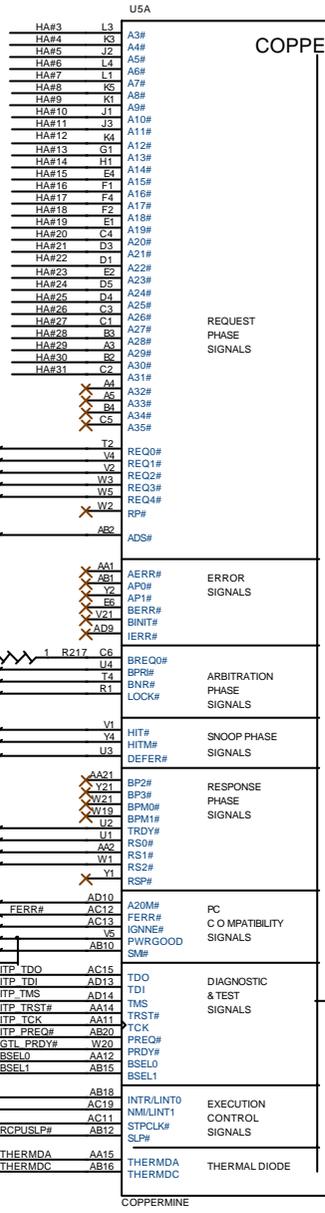
ST

GMCH2-M	A1
ICH2-M	B2
VCH	A2

QT same as ST

Compal Electronics, Inc.			
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COPPERMINE



REQUEST PHASE SIGNALS

DATA PHASE SIGNALS

ERROR SIGNALS

ARBITRATION PHASE SIGNALS

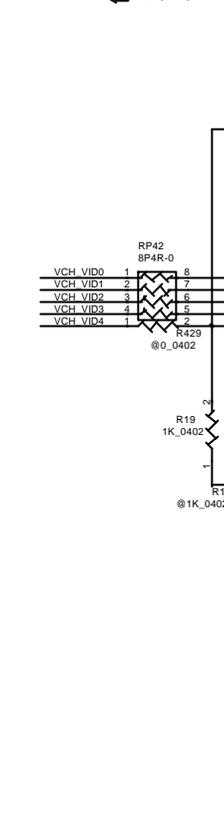
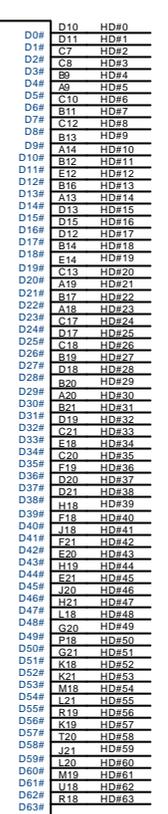
RESPONSE PHASE SIGNALS

PC COMPATIBILITY SIGNALS

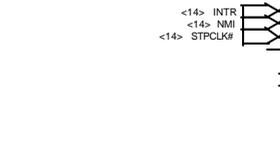
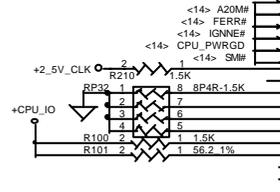
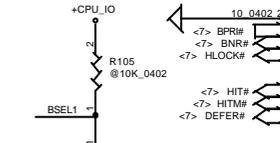
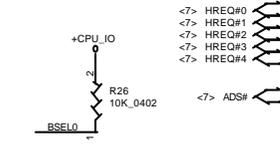
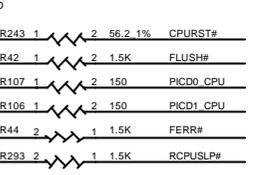
DIAGNOSTIC & TEST SIGNALS

EXECUTION CONTROL SIGNALS

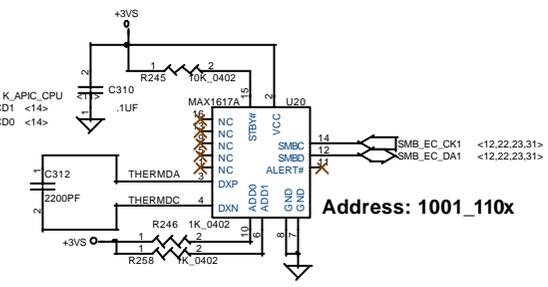
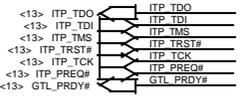
THERMAL DIODE



VI D[4:0]	CPU VCC	VI D[4:0]	CPU VCC
00000	2.00	10000	1.275
00001	1.95	10001	1.250
00010	1.90	10010	1.225
00011	1.85	10011	1.200
00100	1.80	10100	1.175
00101	1.75	10101	1.150
00110	1.70	10110	1.125
00111	1.65	10111	1.100
01000	1.60	11000	1.075
01001	1.55	11001	1.050
01010	1.50	11010	1.025
01011	1.45	11011	1.000
01100	1.40	11100	0.975
01101	1.35	11101	0.950
01110	1.30	11110	0.925
01111	NO CPU	11111	NO CPU



BSEL[1:0]	STSEM BUS FREQUENCY
00	66MHZ
01	100MHZ
10	RESERVED
11	133MHZ



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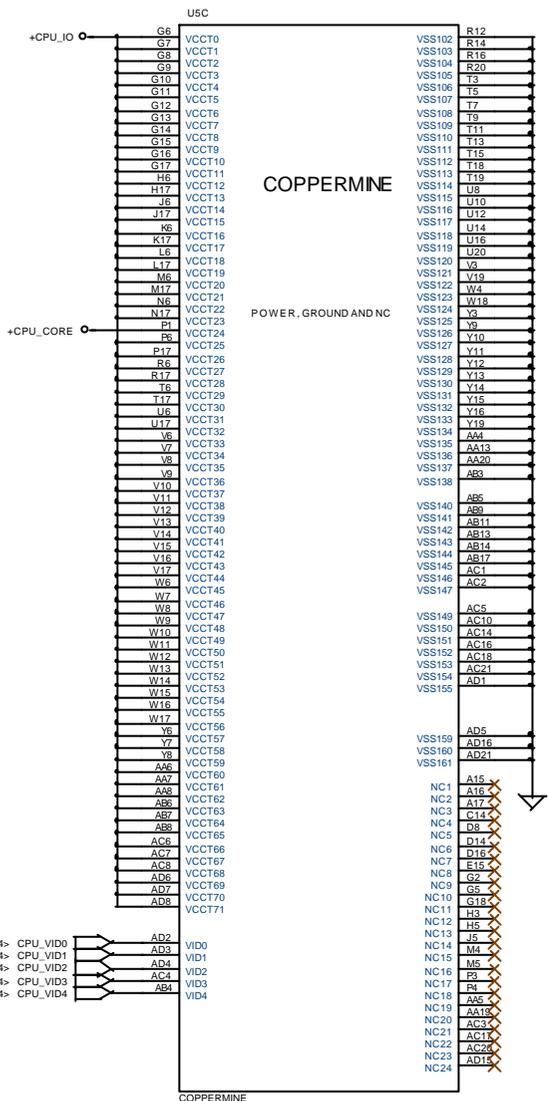
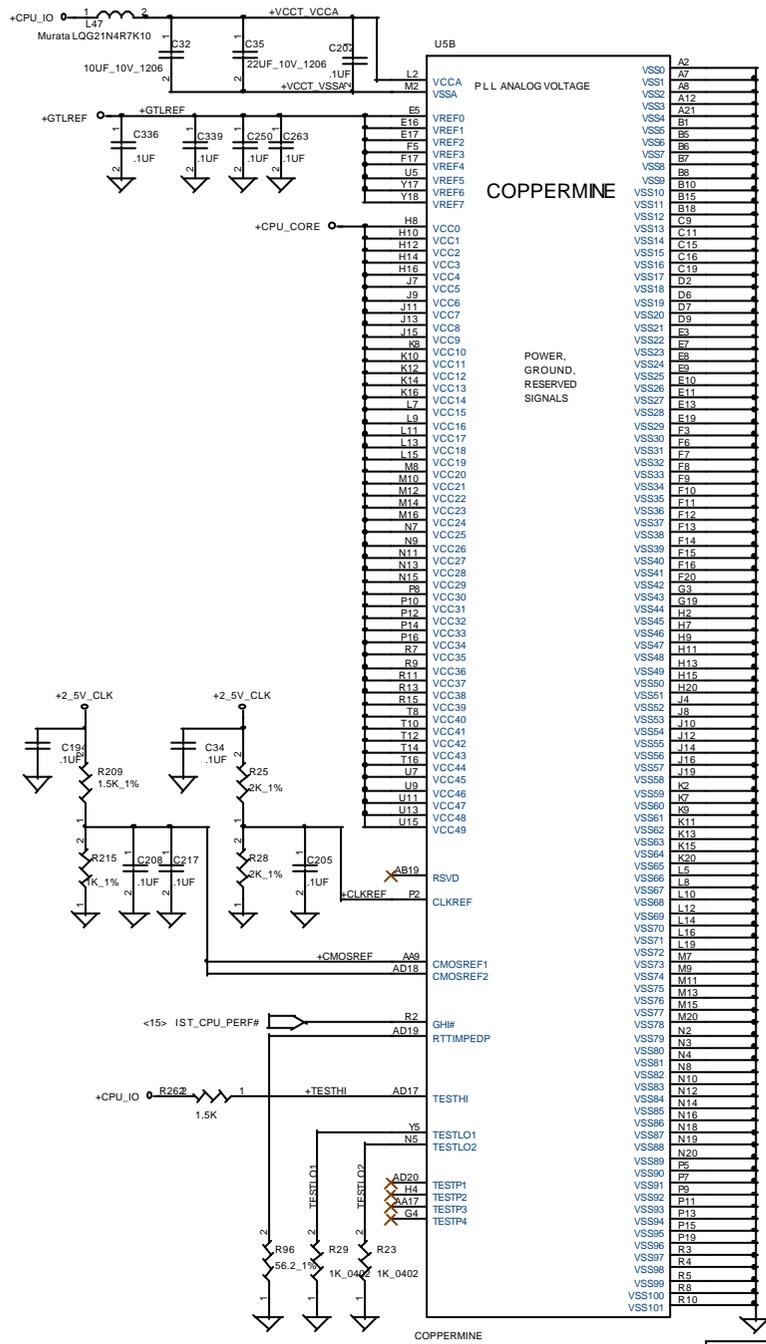
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Size: Document Number 888L2 Main Board

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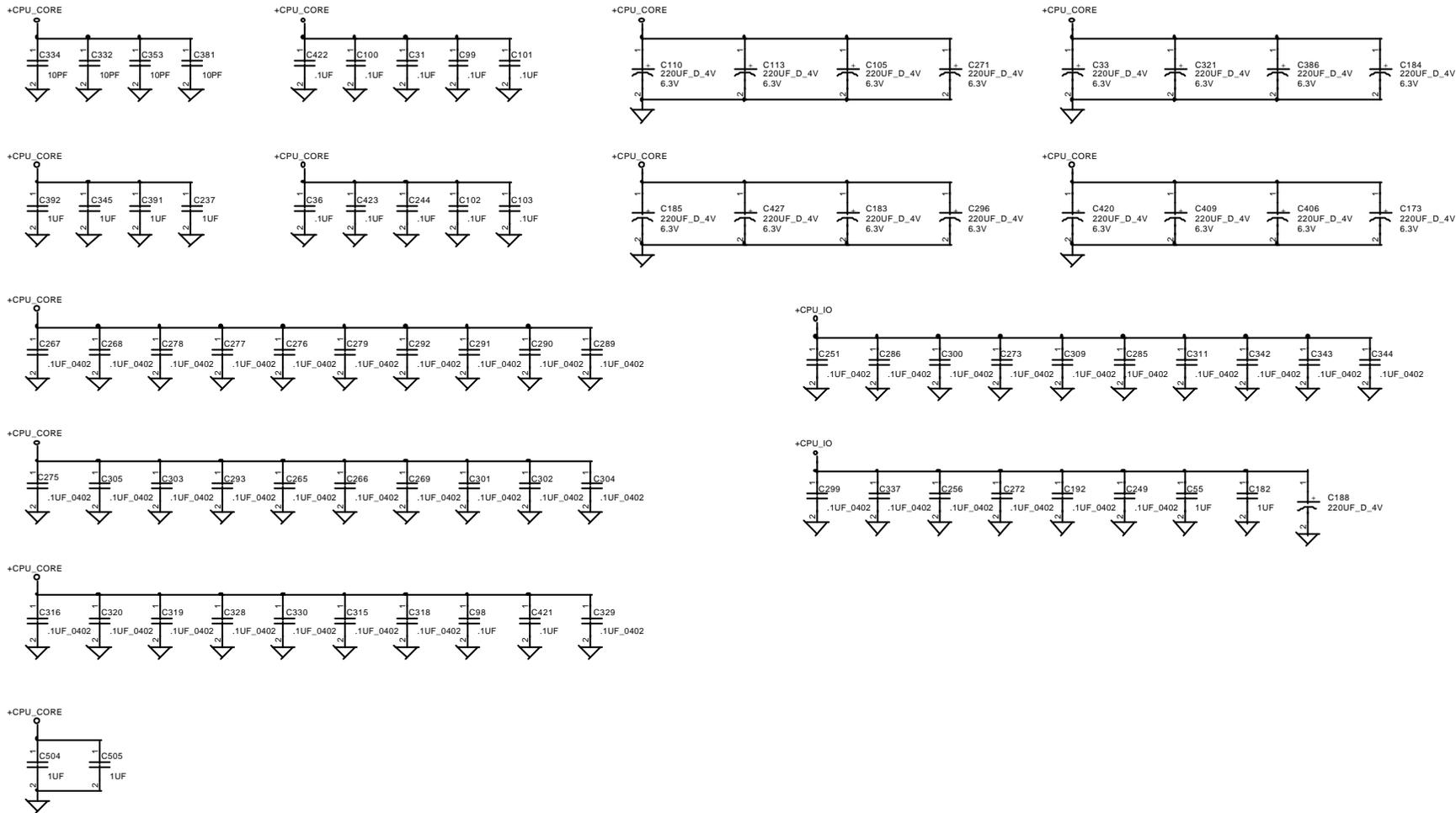


uPGA2 and uBGA2 PI N P1:
 for low voltage Cumine CPU: connect to +CPU_CORE, only uBGA2 package.
 for normal Cumine CPU: connect to +CPU_IO.

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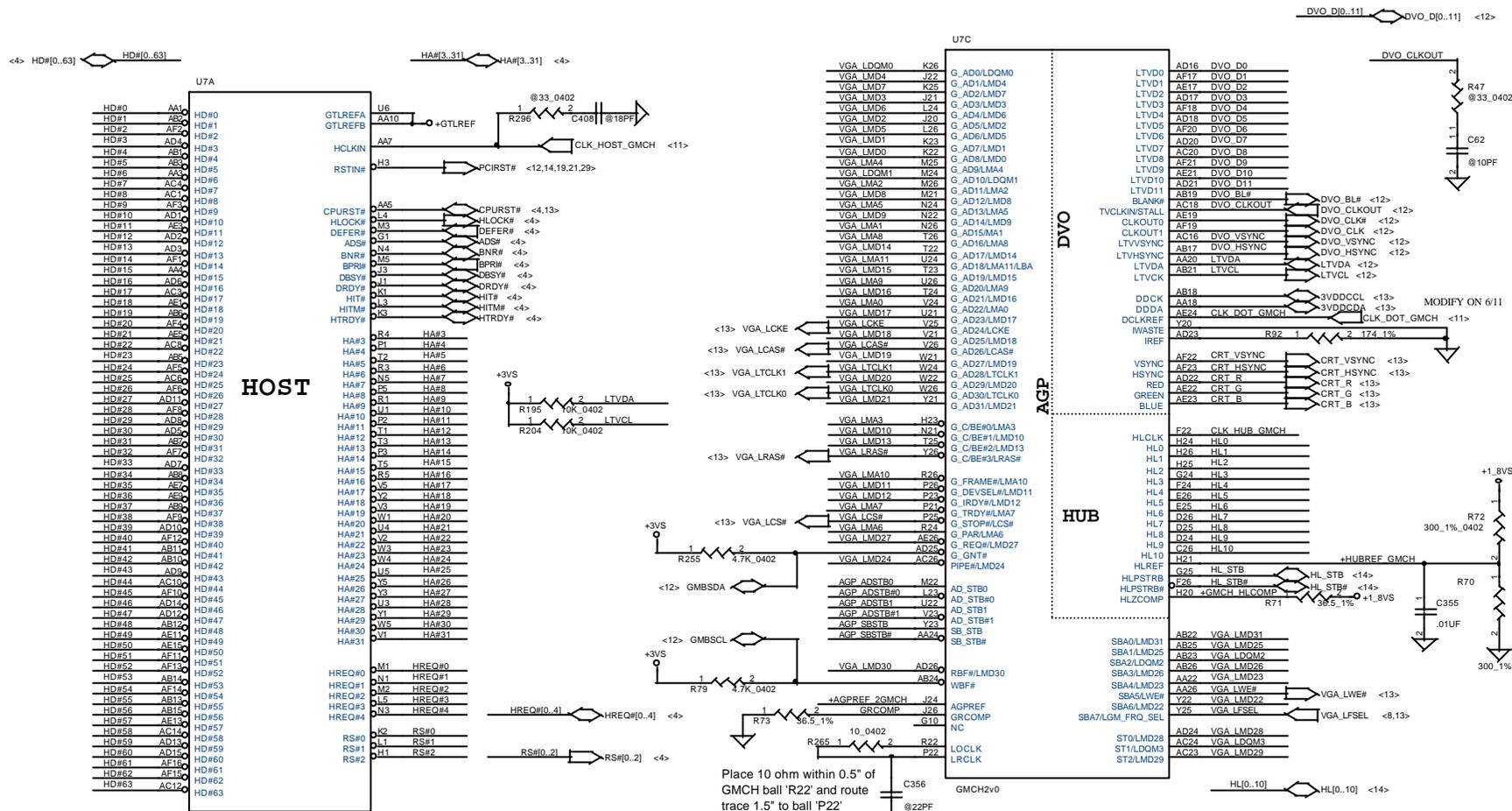
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Compal Electronics, Inc.		
File		
CPU BYPASS		
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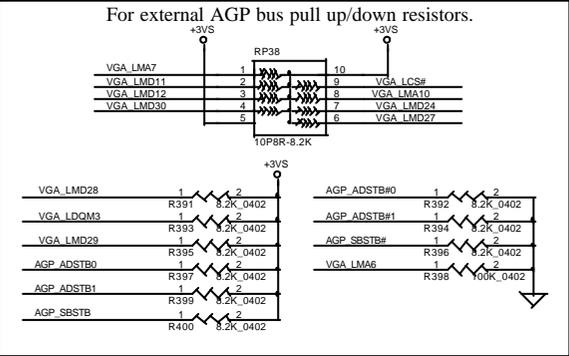


HOST

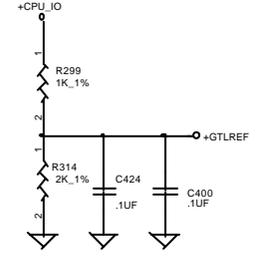
DVO

AGP

HUB



TYPEDET#	+VDDQ	AGP-REF
0	1.5V	0.5VDDQ
1	3.3V	0.4VDDQ



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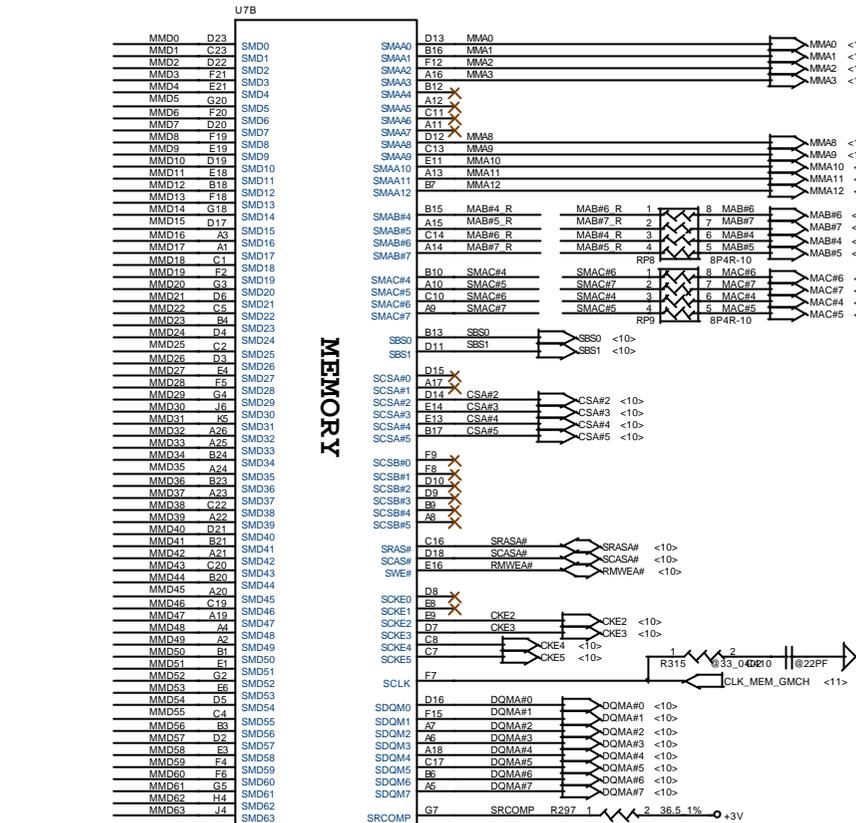
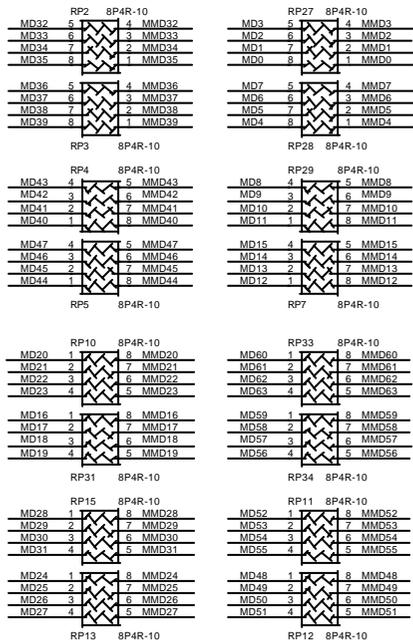
Compal Electronics, Inc.

Title: **GMCH2-M -1/3**

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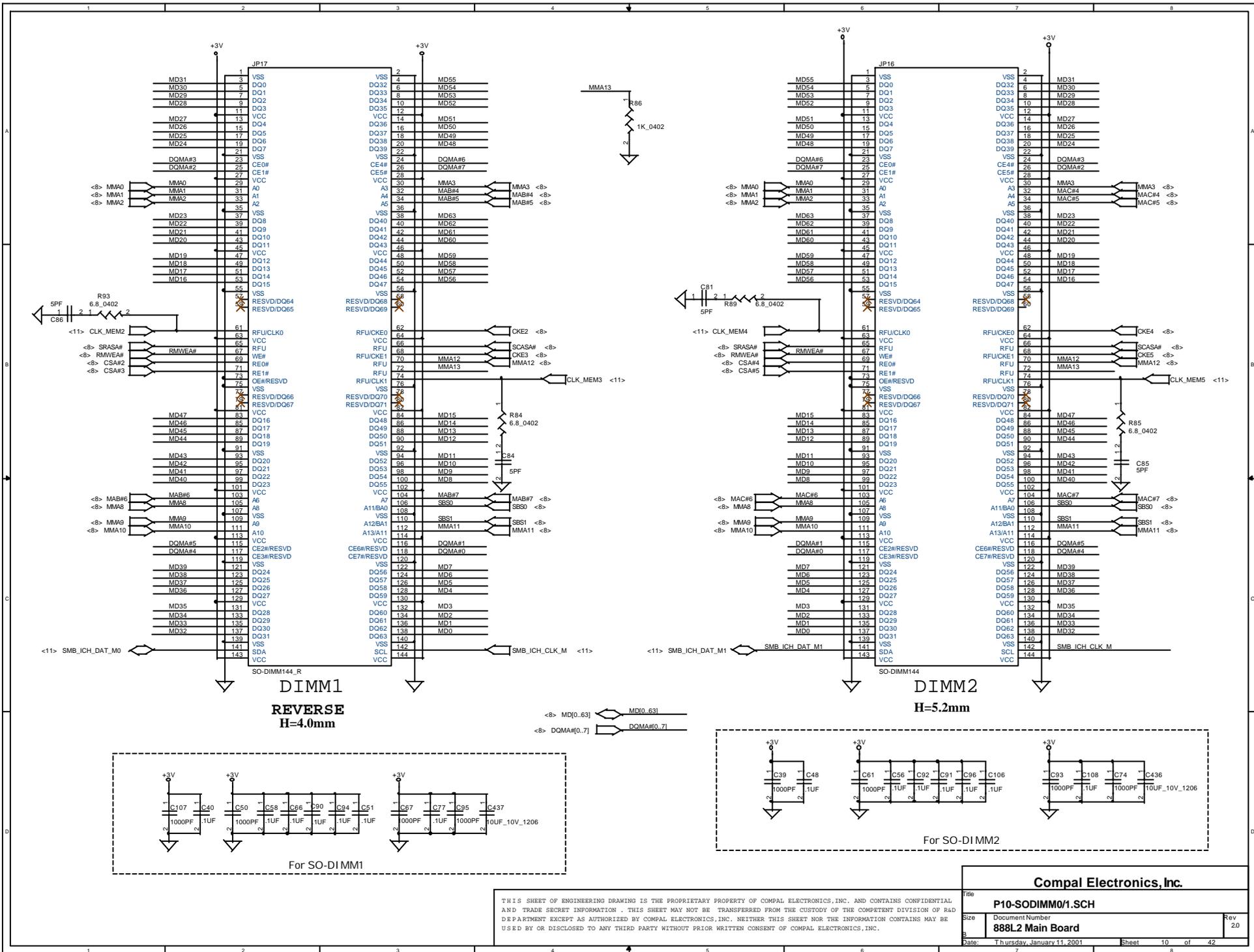
Power-Up Strap Options				
Pin Name	Strap Description	Configuration	Interface	Internal
SCAS#	Host Freq.	"H" : 133MHz (Default) "L" : 100MHz	System Memory	PULL_UP
SWE#	Host Freq.	"H" : 100MHz (Default) "L" : 66MHz	System Memory	PULL_UP
SMAA11	IOQ Depth	"H" : 4 (Default) "L" : 1	System Memory	PULL_UP
SMAA10	ALL Z	"H" : Normal "L" : All Z	System Memory	PULL_UP
SMAA9	FSB P-MOS Kicker Enable	"H" : Enabled (Default) "L" : Disabled (Cumine)	System Memory	PULL_UP
SMAC6#	Enable VCH Serial Programming Mode	"H" : Enabled (Default) "L" : Disabled	System Memory	PULL_UP
SMAC5#	Enable Quick Start Support	"H" : Enabled (Default) (Quick Start Mode) "L" : Disabled (Stop Grant Mode)	System Memory	PULL_UP
VGA_LFSEL#	Local Memory Freq. Select	"H" : 133MHz (Default) "L" : 100MHz	AGP/LM	i815/i815-m



<10> MD[0..63] MD[0..63]

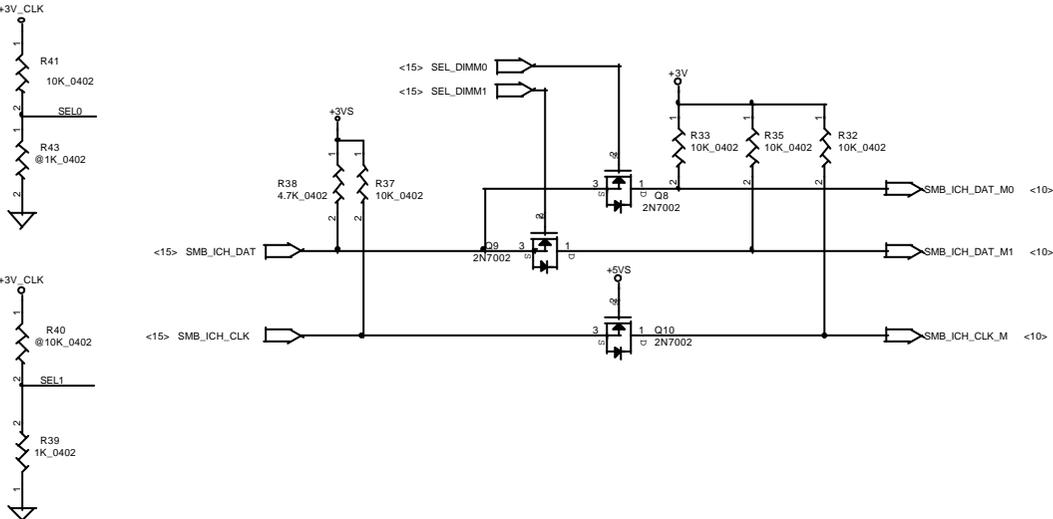
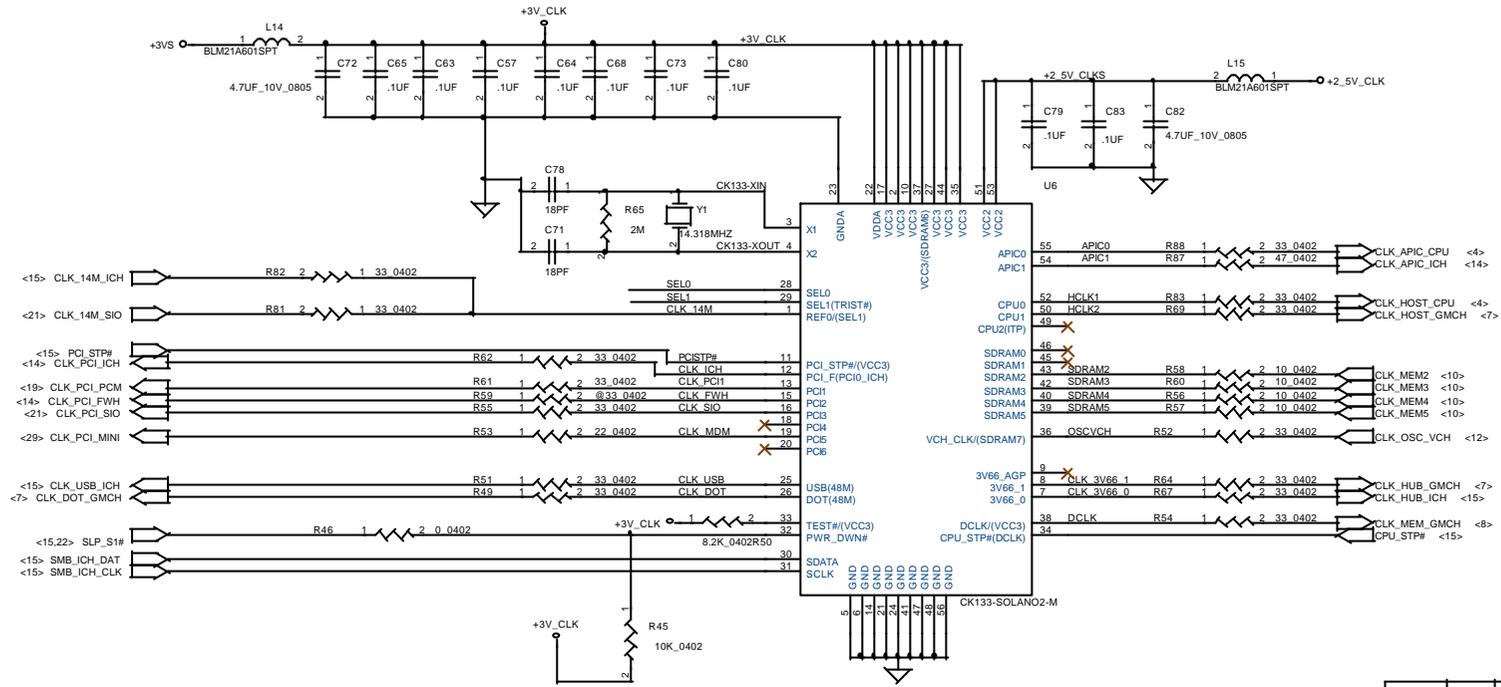
Compal Electronics, Inc.		
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Compal Electronics, Inc.		
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SEL1	SEL0	PSB	SDRAM
0	0	66	100
0	1	100	100
1	0	133	133
1	1	133	100

Pin #	CK-Solano		CK-Solano2-m	
	W218	C9815	W224	C9835
1	REF0/SEL1	REF/SEL1	REF	REF
11	VCC3	VCC3	PCI_STP#	PCI_STP#
29	Tristate#	Tristate#	SEL1	SEL1
33	VCC3	VCC3	TEST#	TEST#
34	DCLK	DCLK	CPU_STP#	CPU_STP#
36	SDRAM7	SDRAM7	VCH_CLK	VCH_CLK
37	SDRAM6	SDRAM6	VCC3	VCC3
38	VCC3	VCC3	DCLK	DCLK

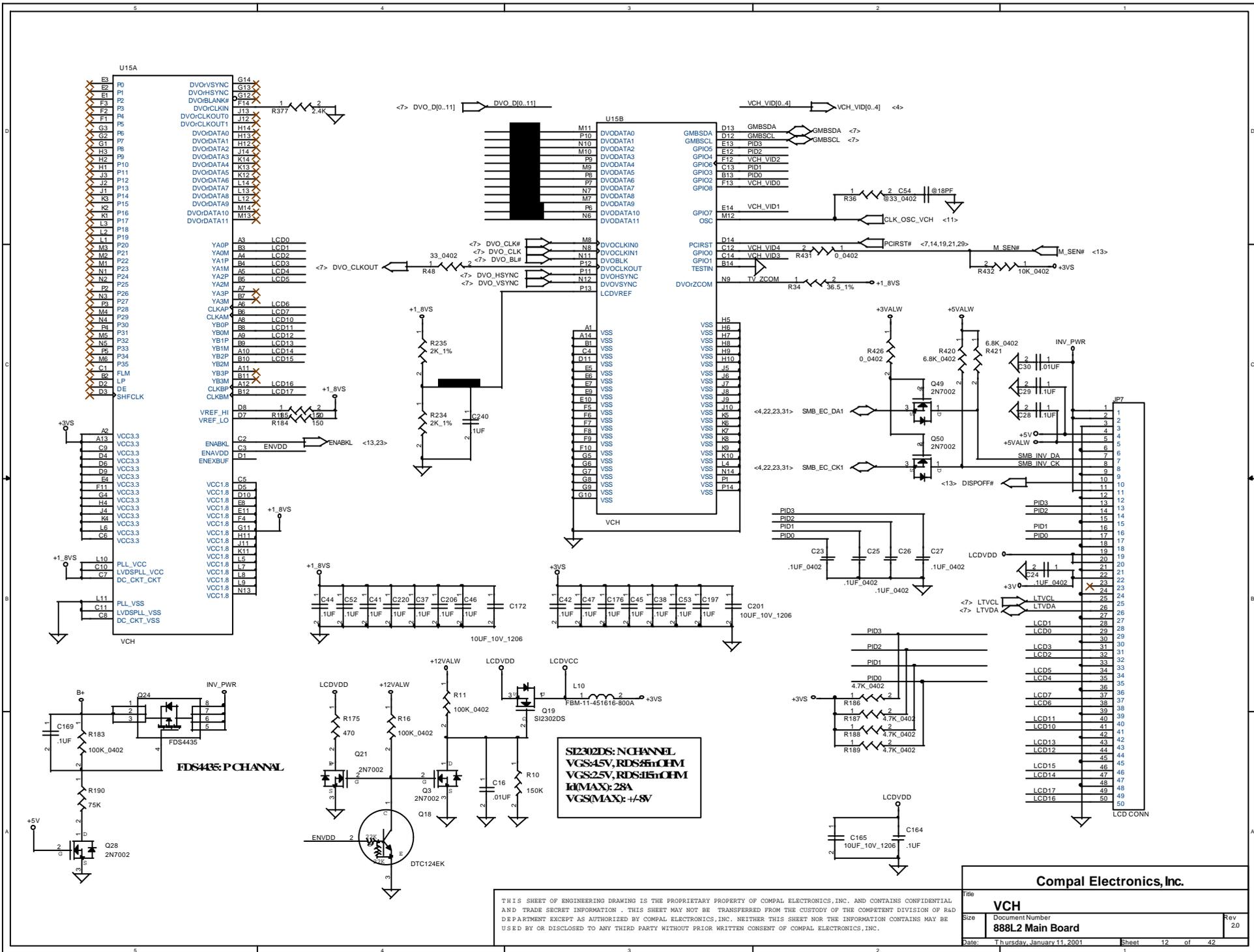
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File: **Clock Synthesizer**

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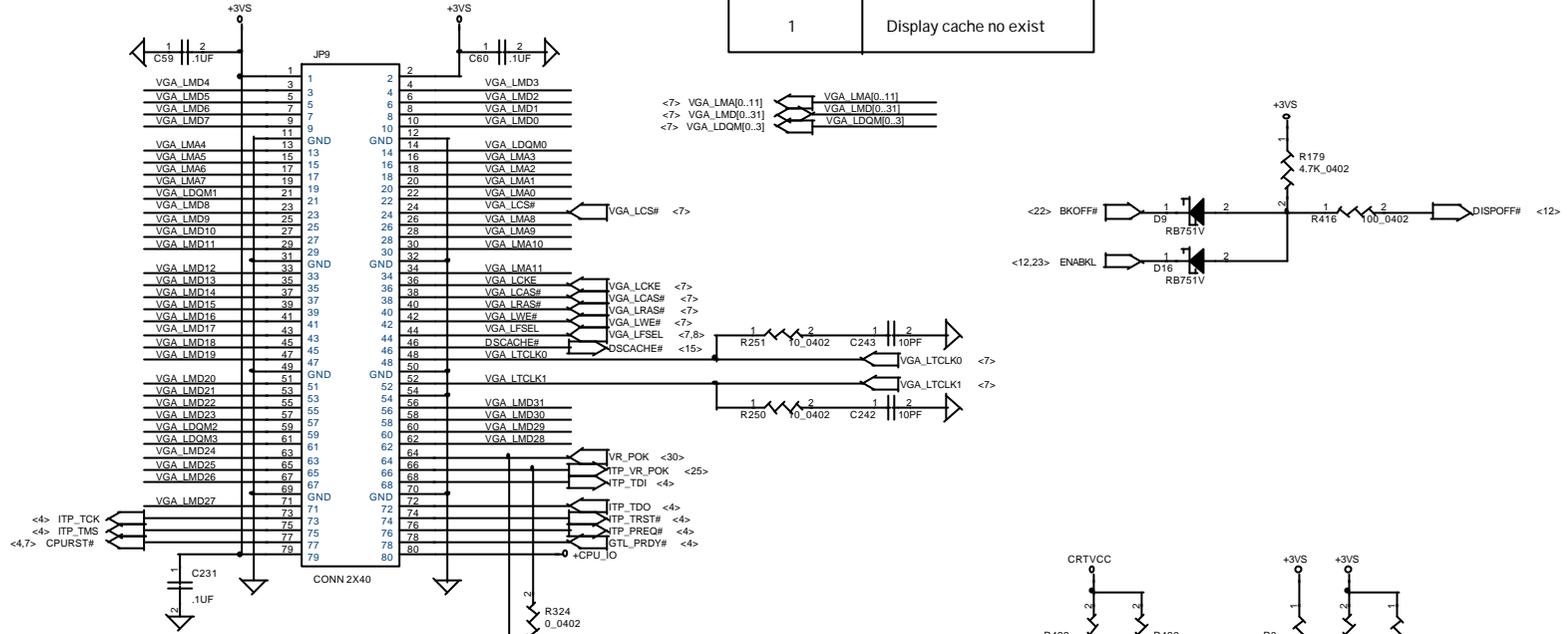


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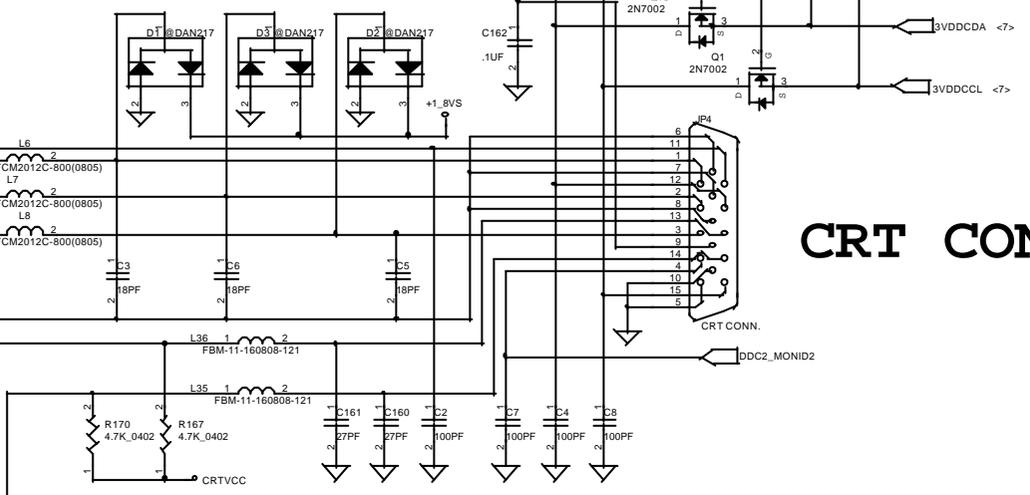
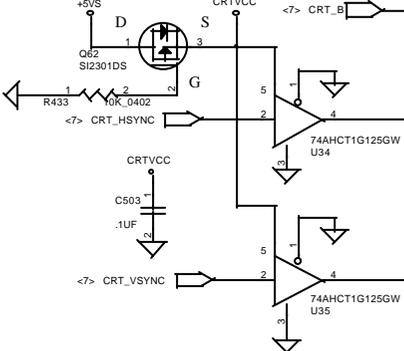
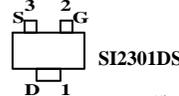
Compal Electronics, Inc.		
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DISPLAY CACHE INTERFACE

DSCACHE#	Status
0	Display cache exist
1	Display cache no exist



SI2301DS: P CHANNEL
 VGS: -4.5V, RDS: 130mOHM
 VGS: -2.5V, RDS: 190mOHM
 Id(MAX): 23A
 VGS(MAX): +8V

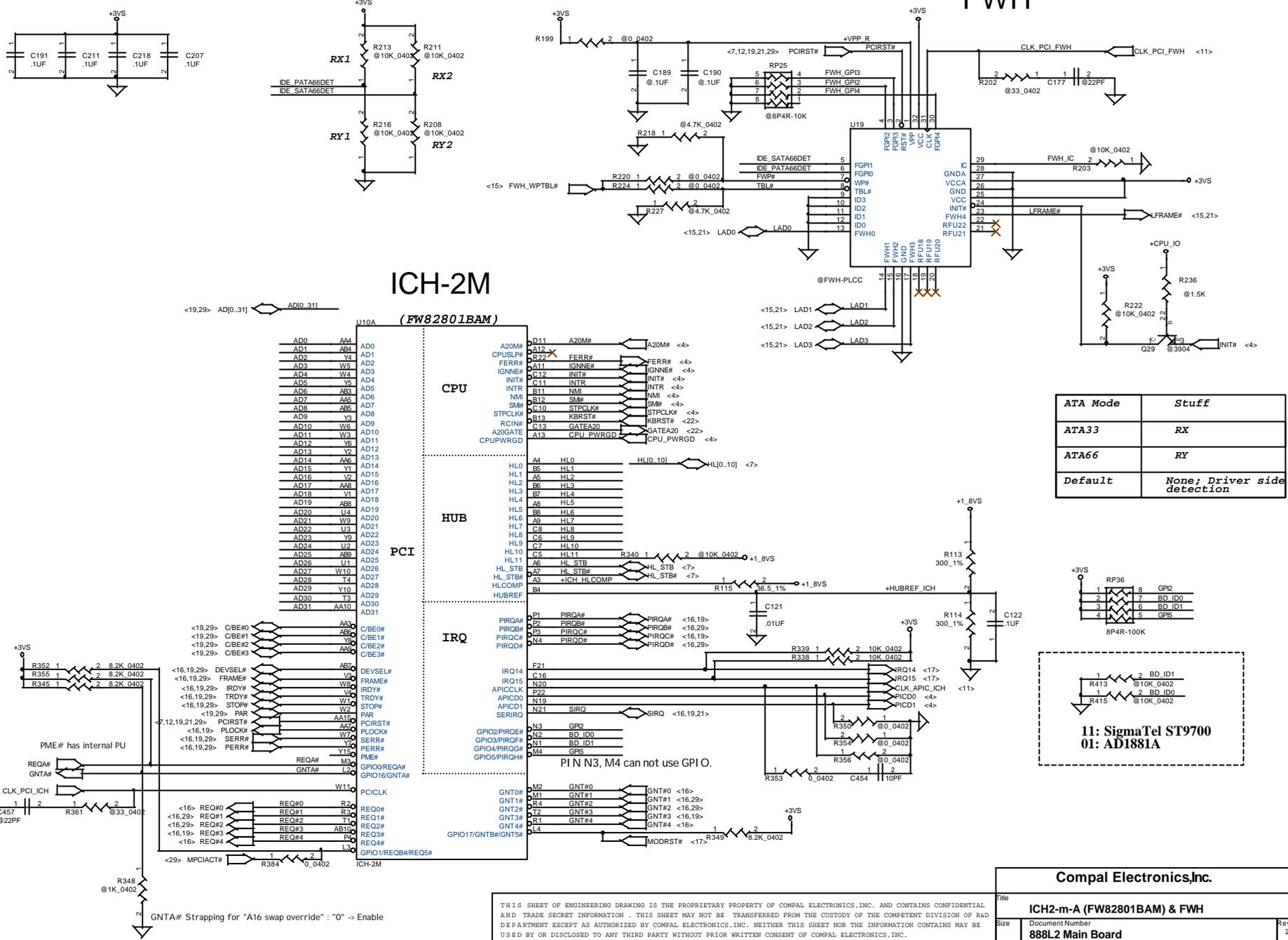


CRT CONN.

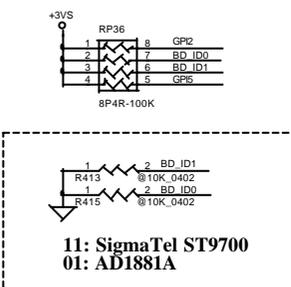
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FWH



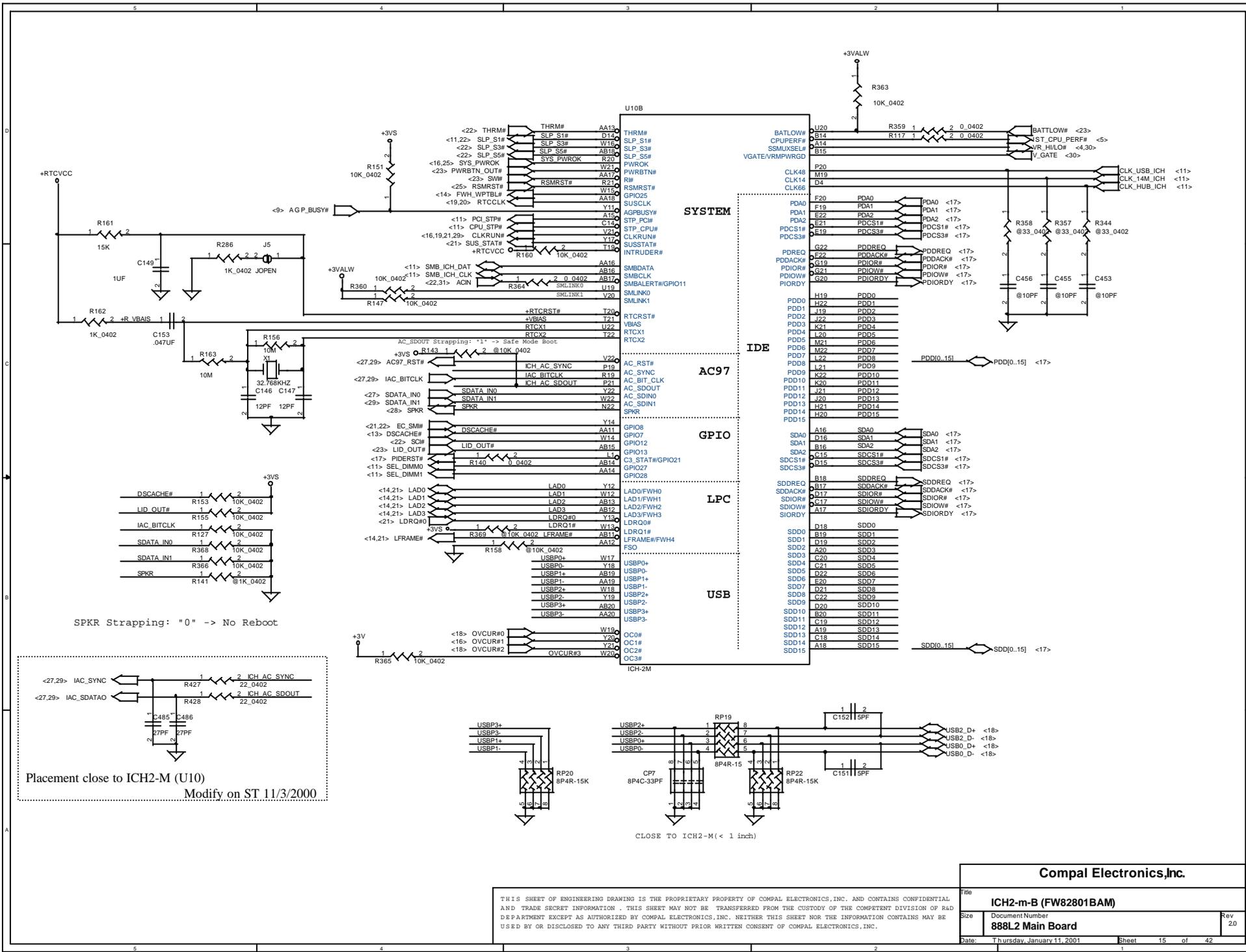
ATA Mode	Stuff
ATA33	RX
ATA66	RY
Default	None; Driver side detection



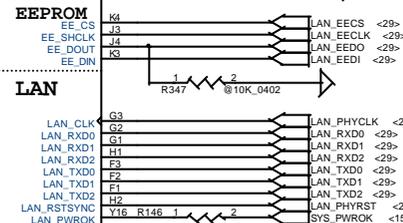
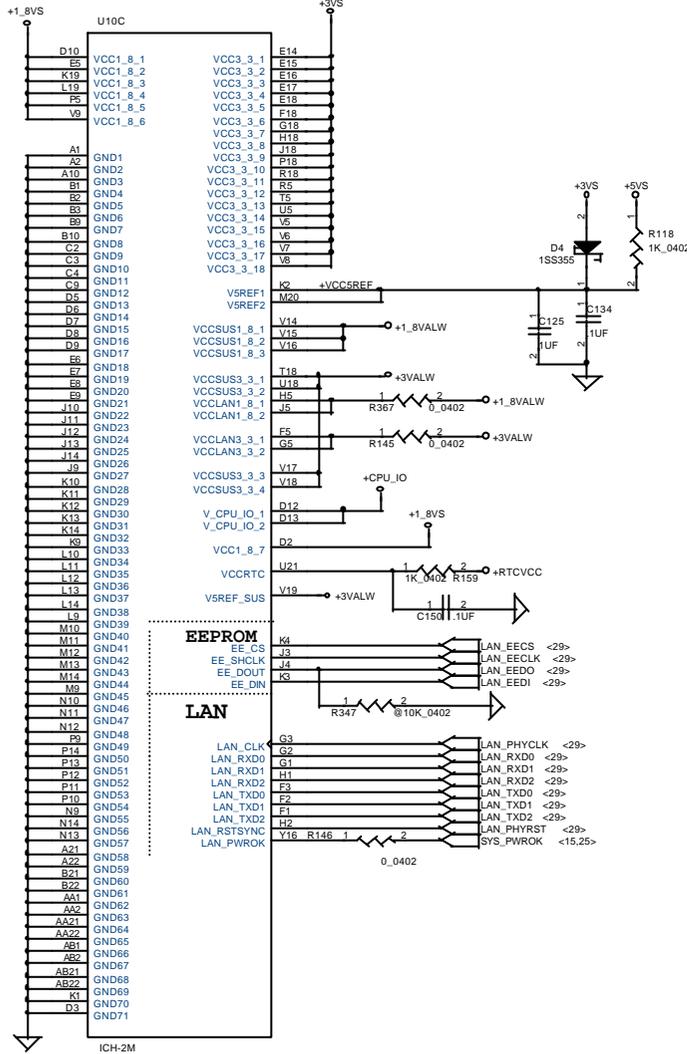
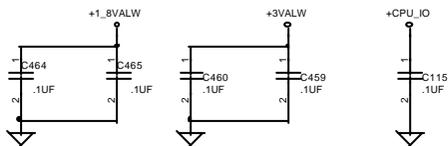
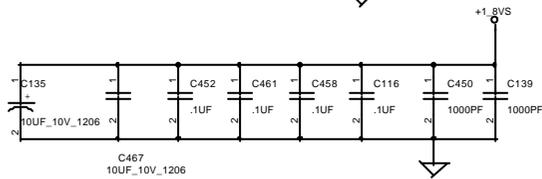
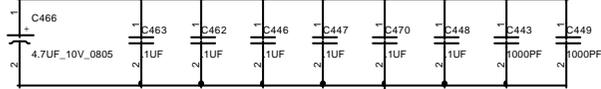
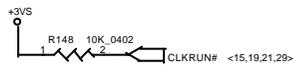
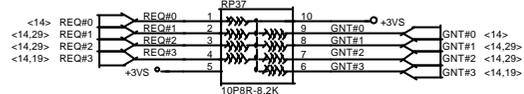
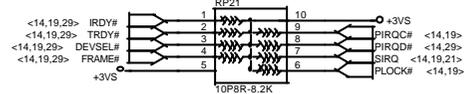
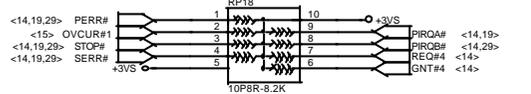
**11: SigmaTel ST9700
01: AD1881A**

Compal Electronics, Inc.		
File: ICH2-m-A (FW82801BAM) & FWH		
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PCI

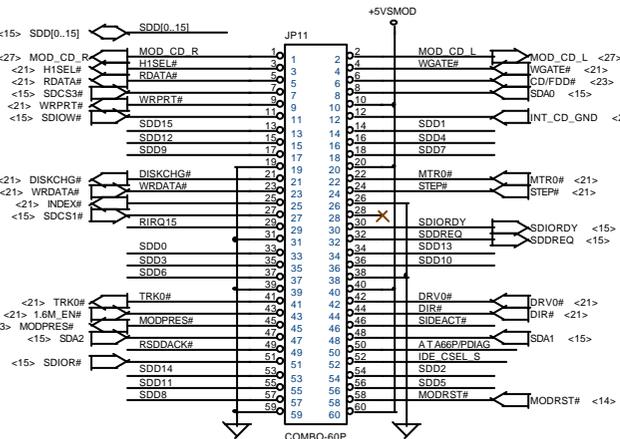
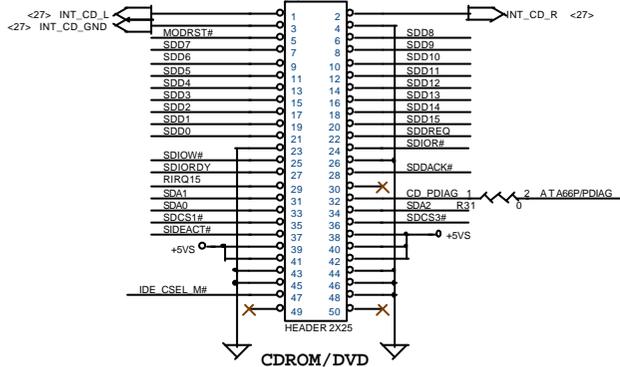
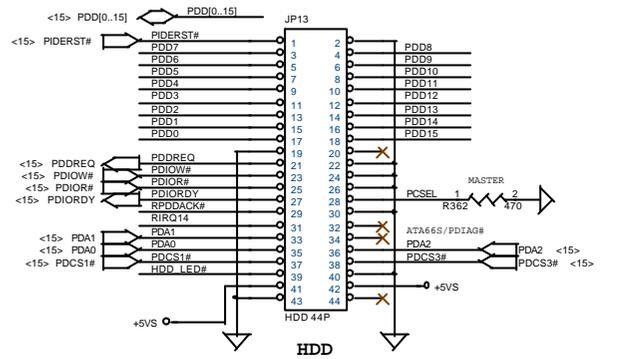


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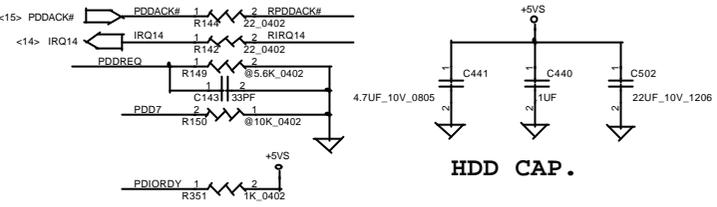
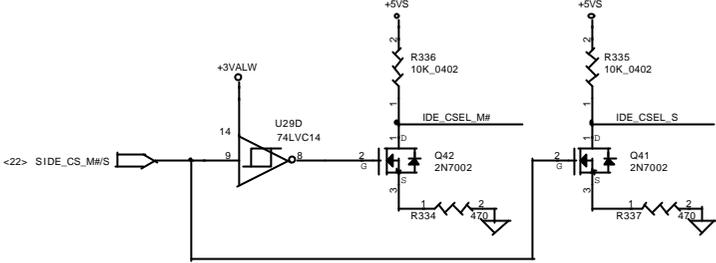
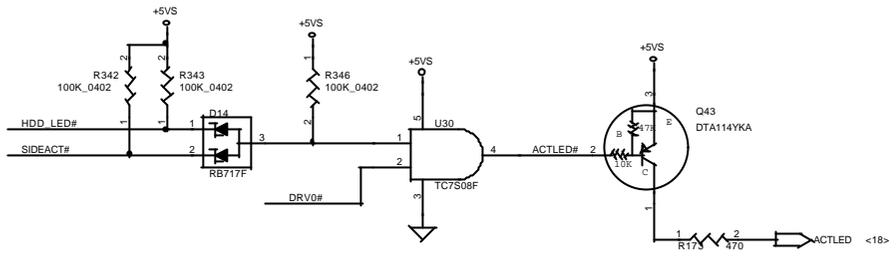
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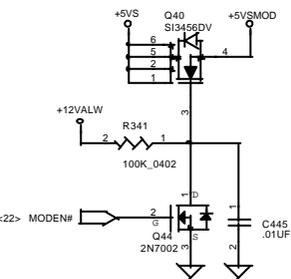
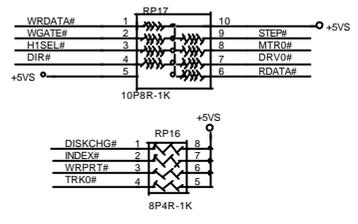
IDE,CD-ROM & FDD Module CONN.



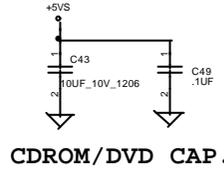
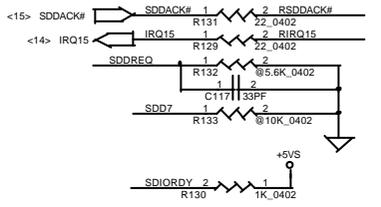
MODULE
FDD/CDROM/DVD



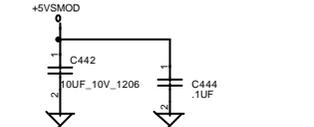
HDD CAP.



SI3456DV: NCHANNEL
VGS: 4.5V, RDS: 65mOhm
Id(MAX): 5.1A



CDROM/DVD CAP.

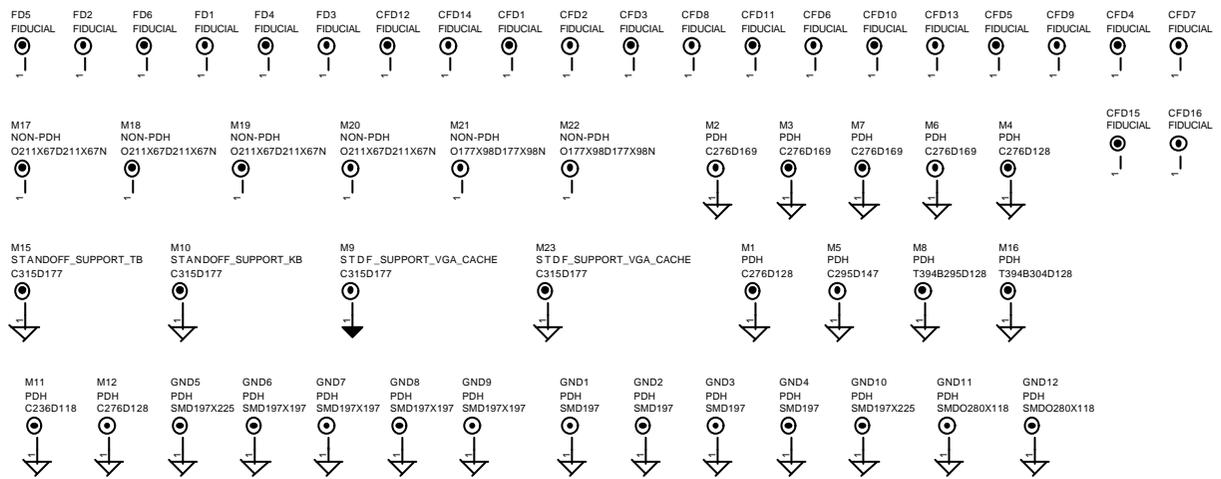
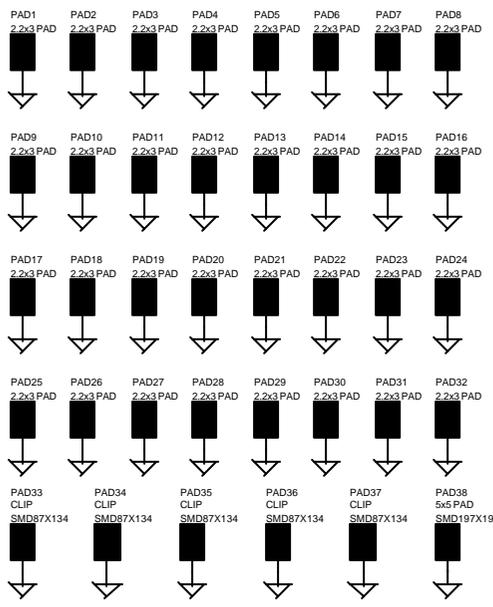
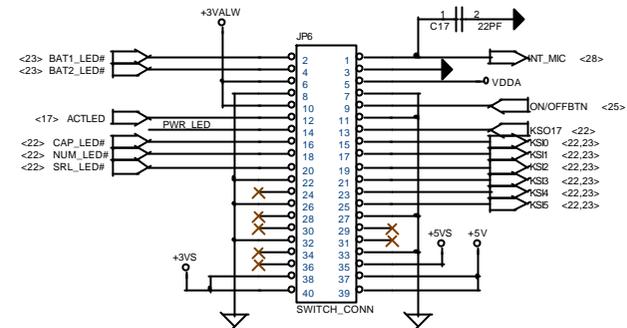
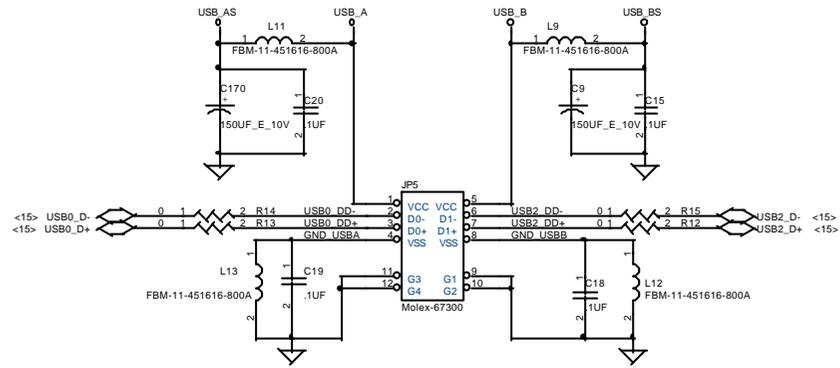
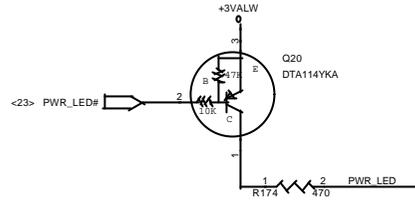
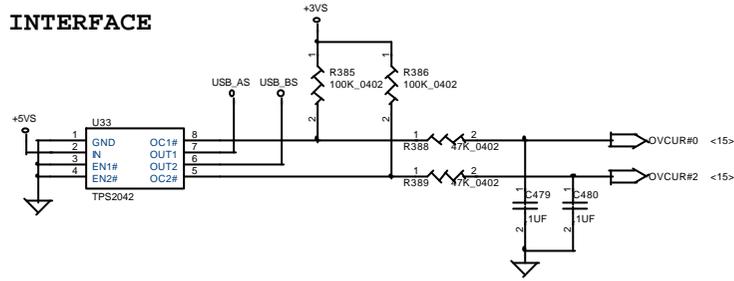


SECOND MODULE CAP.

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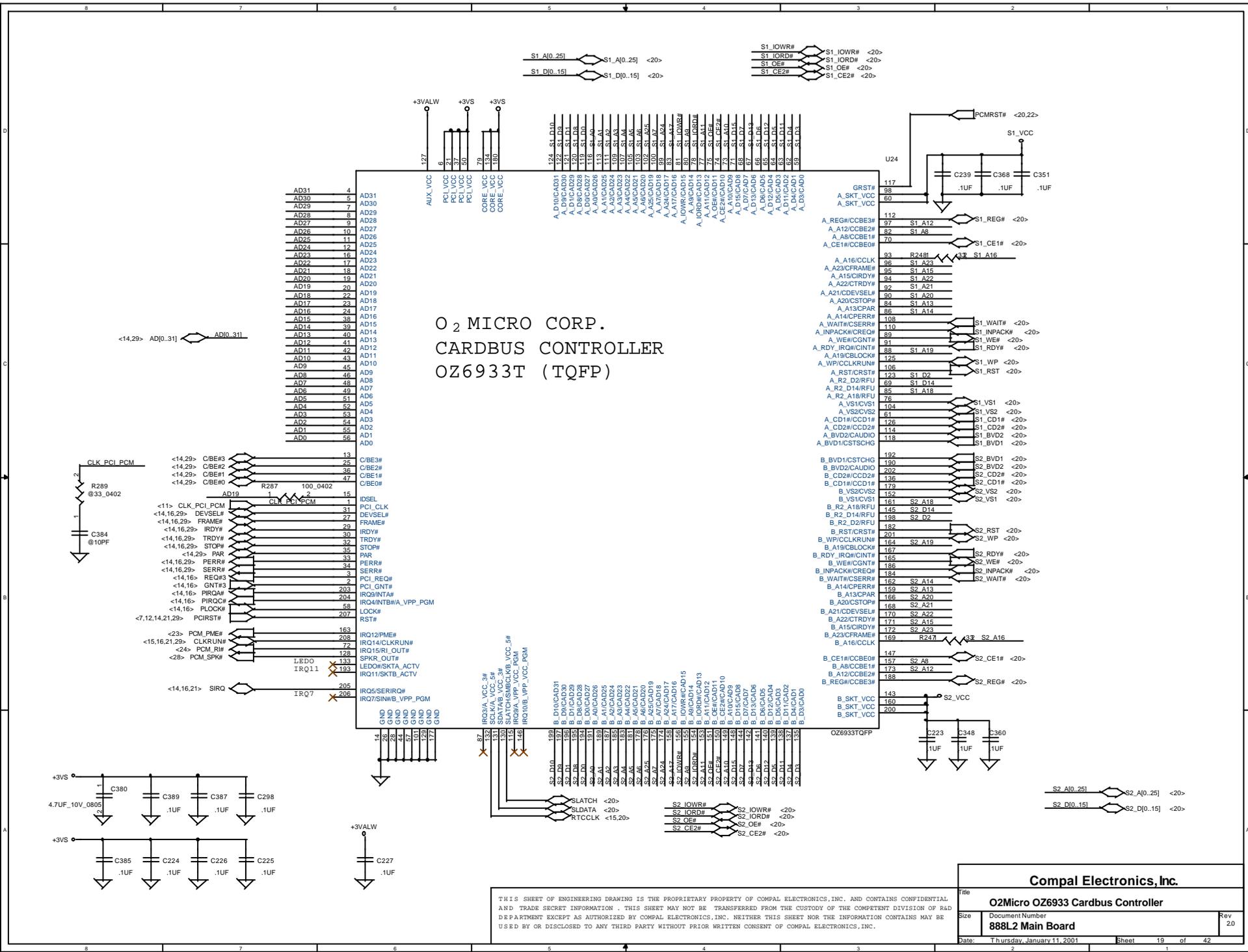
Compal Electronics, Inc.		
File	IDE/FDD MODULE	
Size	Document Number	Rev
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USB&LED INTERFACE



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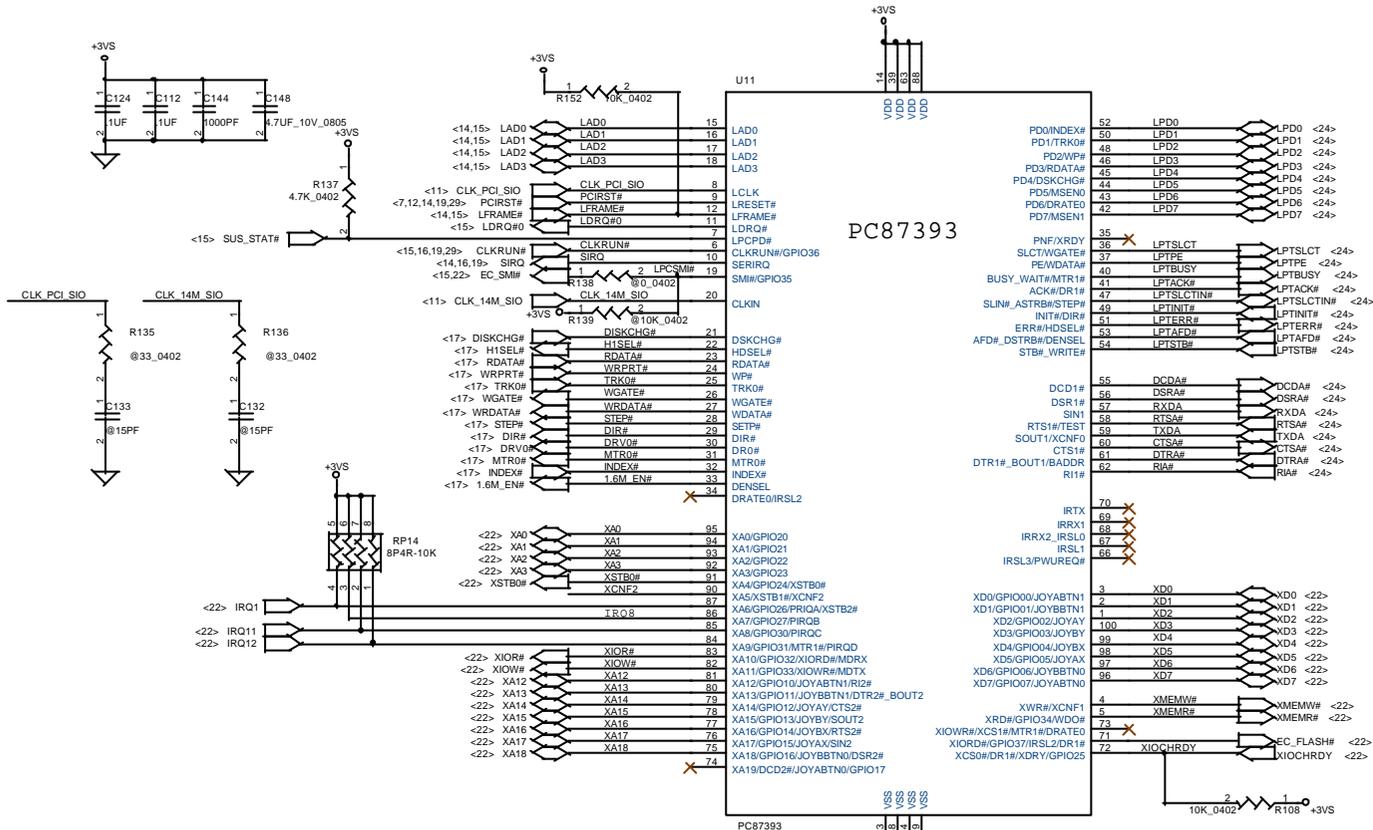
Compal Electronics, Inc.		
File: USB & FRONT PANEL I/F		
Size: 888L2 Main Board	Document Number: 888L2 Main Board	Rev: 20
Date: Thursday, January 11, 2001	Sheet: 18	of 42



O₂ MICRO CORP.
 CARDBUS CONTROLLER
 OZ6933T (TQFP)

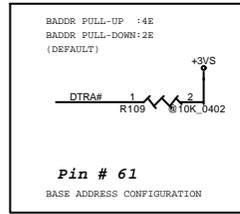
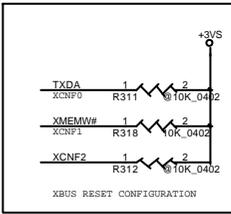
Compal Electronics, Inc.		
File	O2Micro OZ6933 Cardbus Controller	
Size	Document Number	Rev
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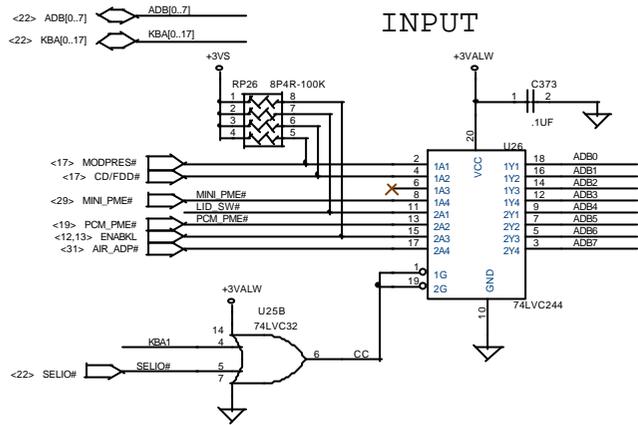
Signal	Pin #	Description
BADDR	61	BASE Address Selection "0": 2E-2F (Default) "1": 4E-4F
TEST	58	"0": Normal (Default) "1": Test Mode
XCNF[2:0]	90, 4, 59	2 1 0 Function
		x 0 0 No BIOS
		x 0 1 Normal Mode. XRDY disabled
		(default) 0 1 0 Latch Mode. XA12-19, XRDY enabled
		1 1 0 Latch Mode. GPIO10-17, XRDY enabled
	0 1 1 Latch Mode. XA12-19, XRDY disabled	
	1 1 1 Latch Mode. GPIO10-17, XRDY disabled	

* 1 ROM SOLUTION

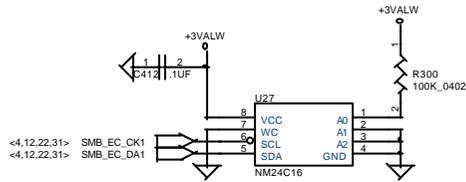


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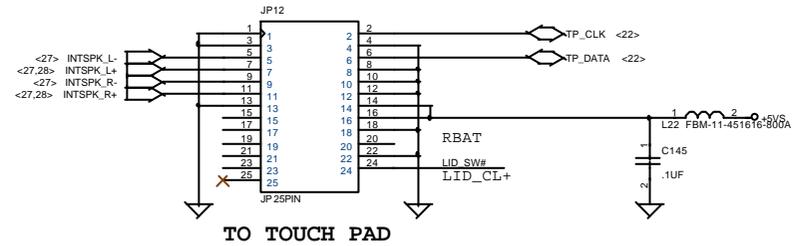
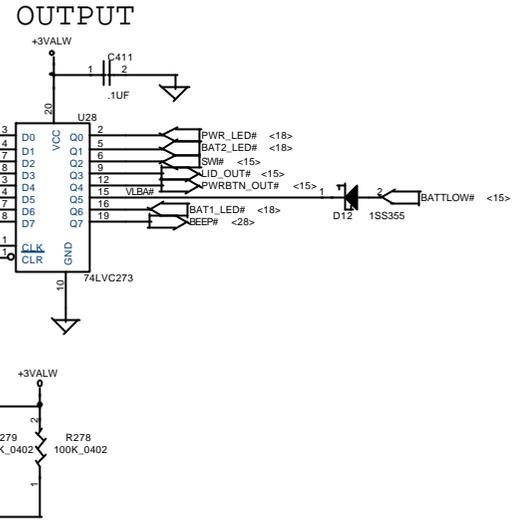
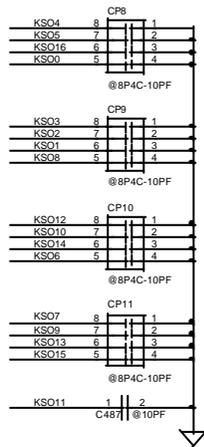
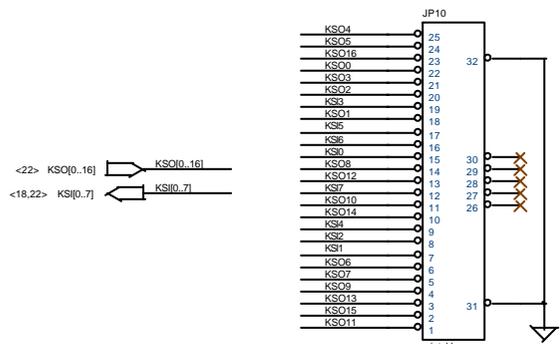
Compal Electronics, Inc.		
File	SUPER I/O PC87393 CHIP	
Size	Document Number	Rev
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NM24C164 Address definition: 1 A2 A1# A0 B2 B1 B0 R/W#



EC I2C Bus Address:
 24C164: 1011xxxx R/W#
 24C16: 1010xxxx R/W#



Compal Electronics, Inc.

File: **EC Extended I/O Port**

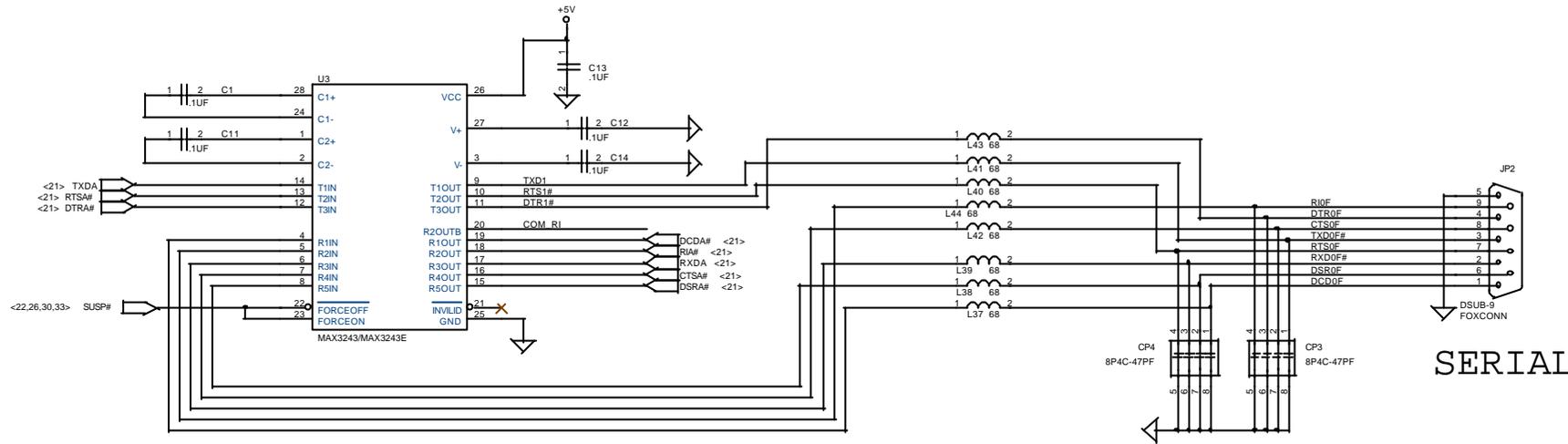
Size: **Document Number 888L2 Main Board**

Rev: **2.0**

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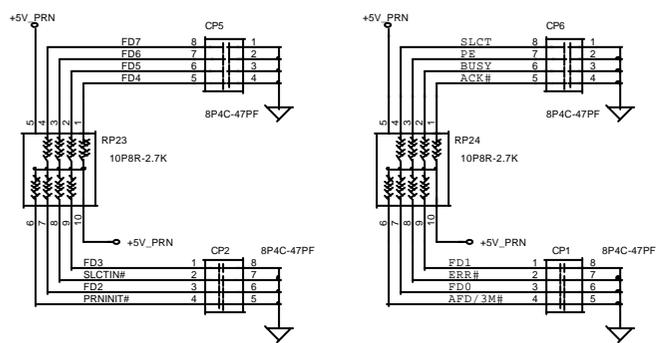
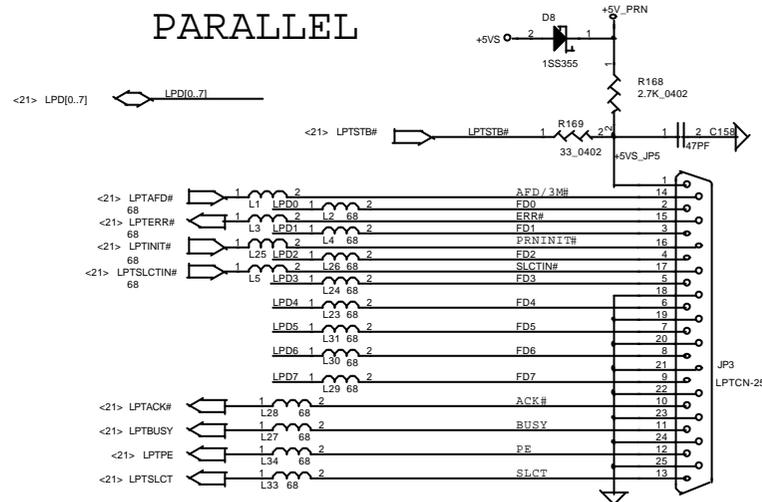
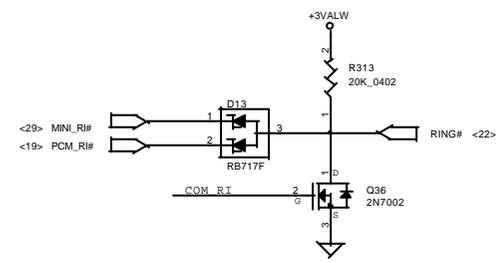
SERIAL / PARALLEL PORT

SERIAL & PARALLEL



SERIAL

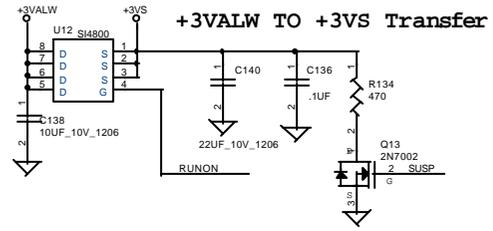
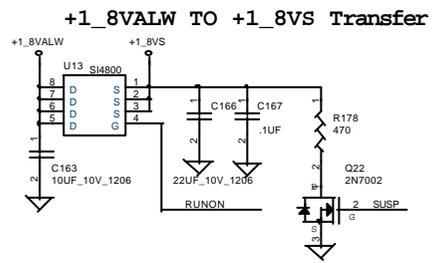
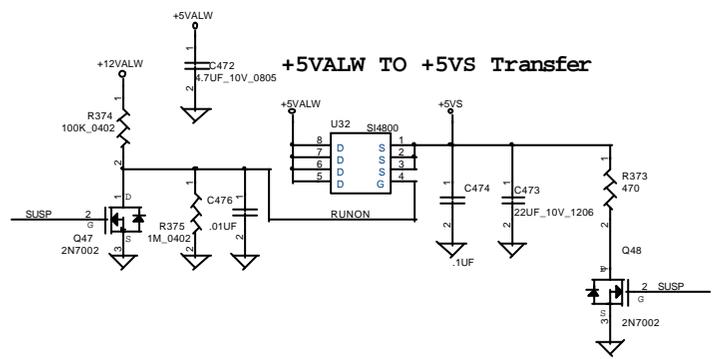
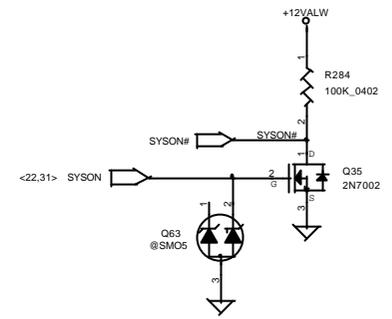
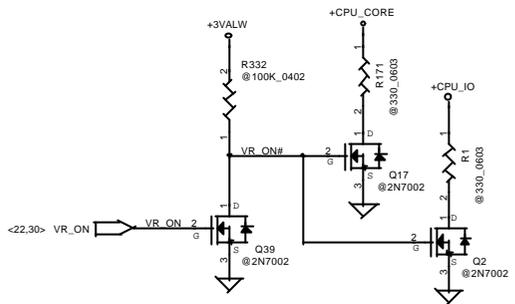
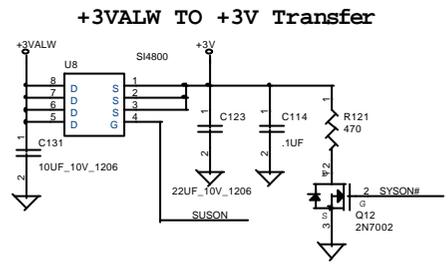
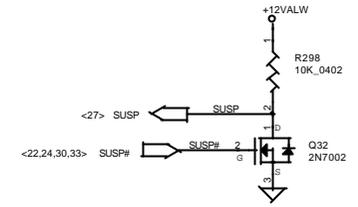
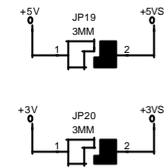
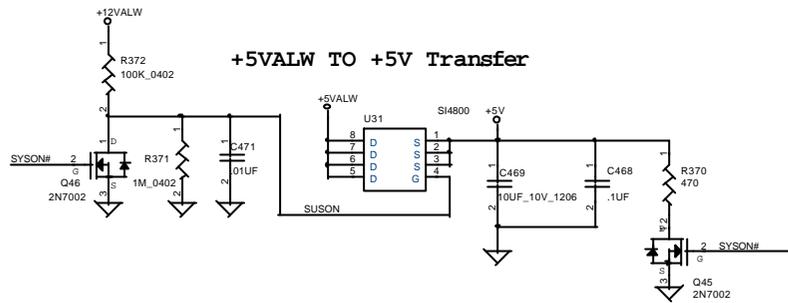
PARALLEL



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Compal Electronics, Inc.		
File	Serial/parallel ports	
Size	Document Number	Rev
	888L2 Main Board	20
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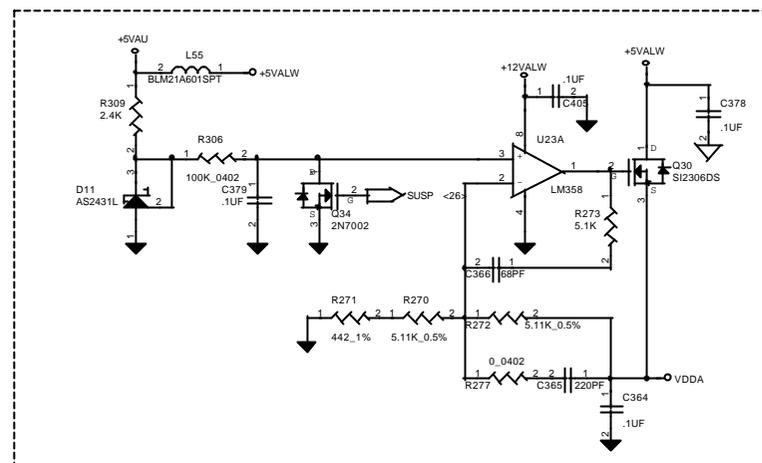
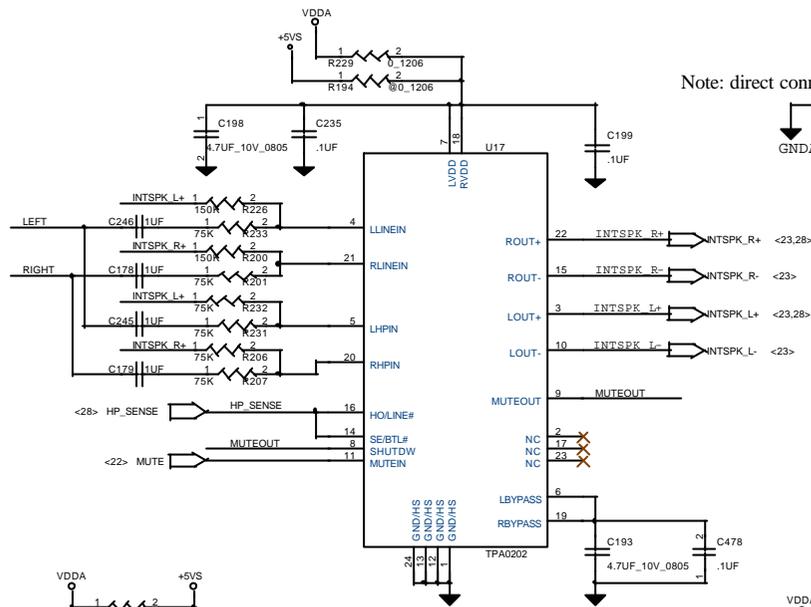
RESET & SUSPEND CKT



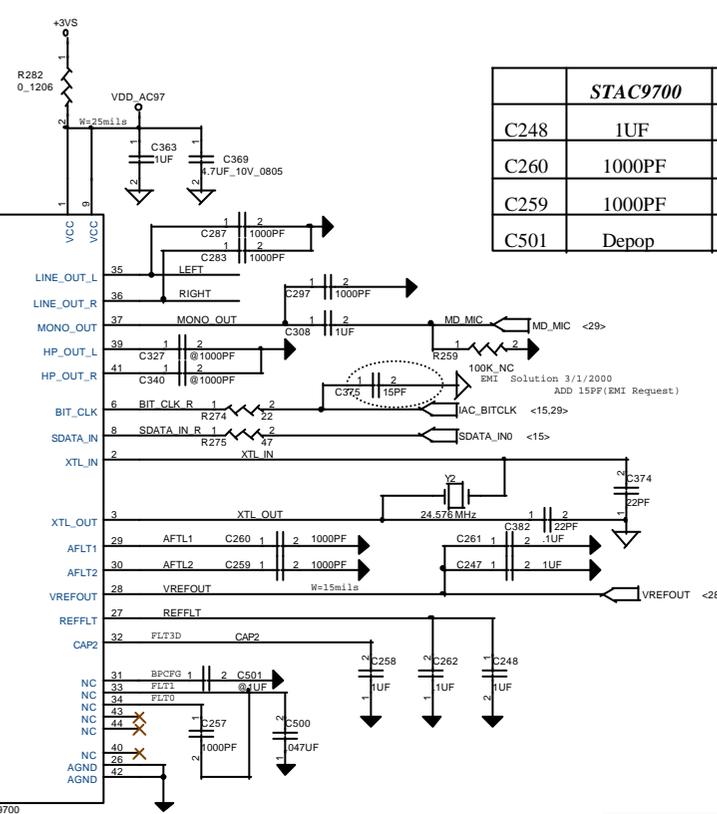
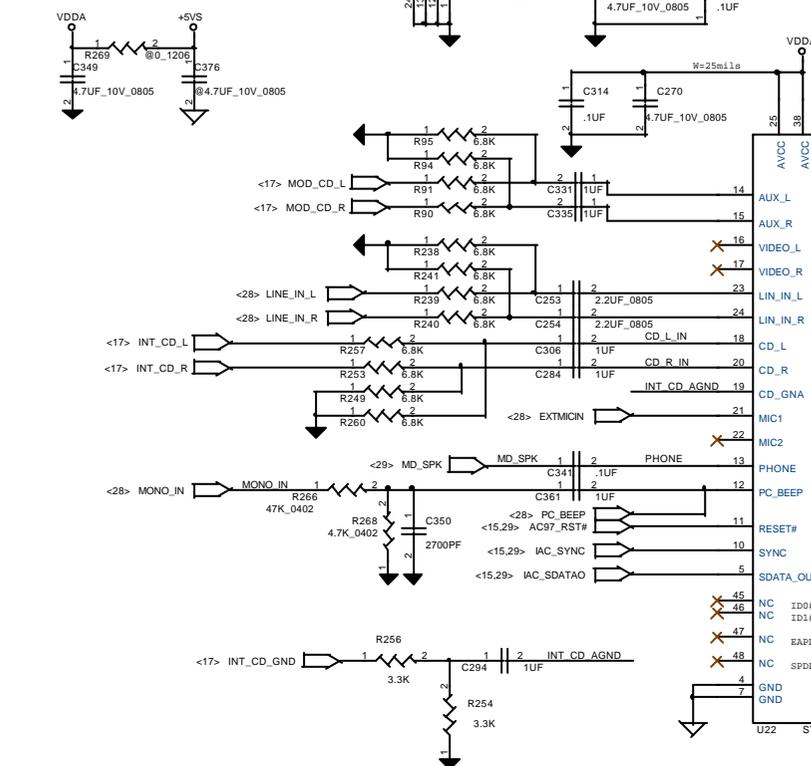
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Compal Electronics, Inc.		
File	DC/DC INTERFACE	
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Note: direct connect GNDA to GND.



	STAC9700	AD1881A
C248	1UF	4.7UF 10V 0805
C260	1000PF	270PF
C259	1000PF	270PF
C501	Depop	1UF



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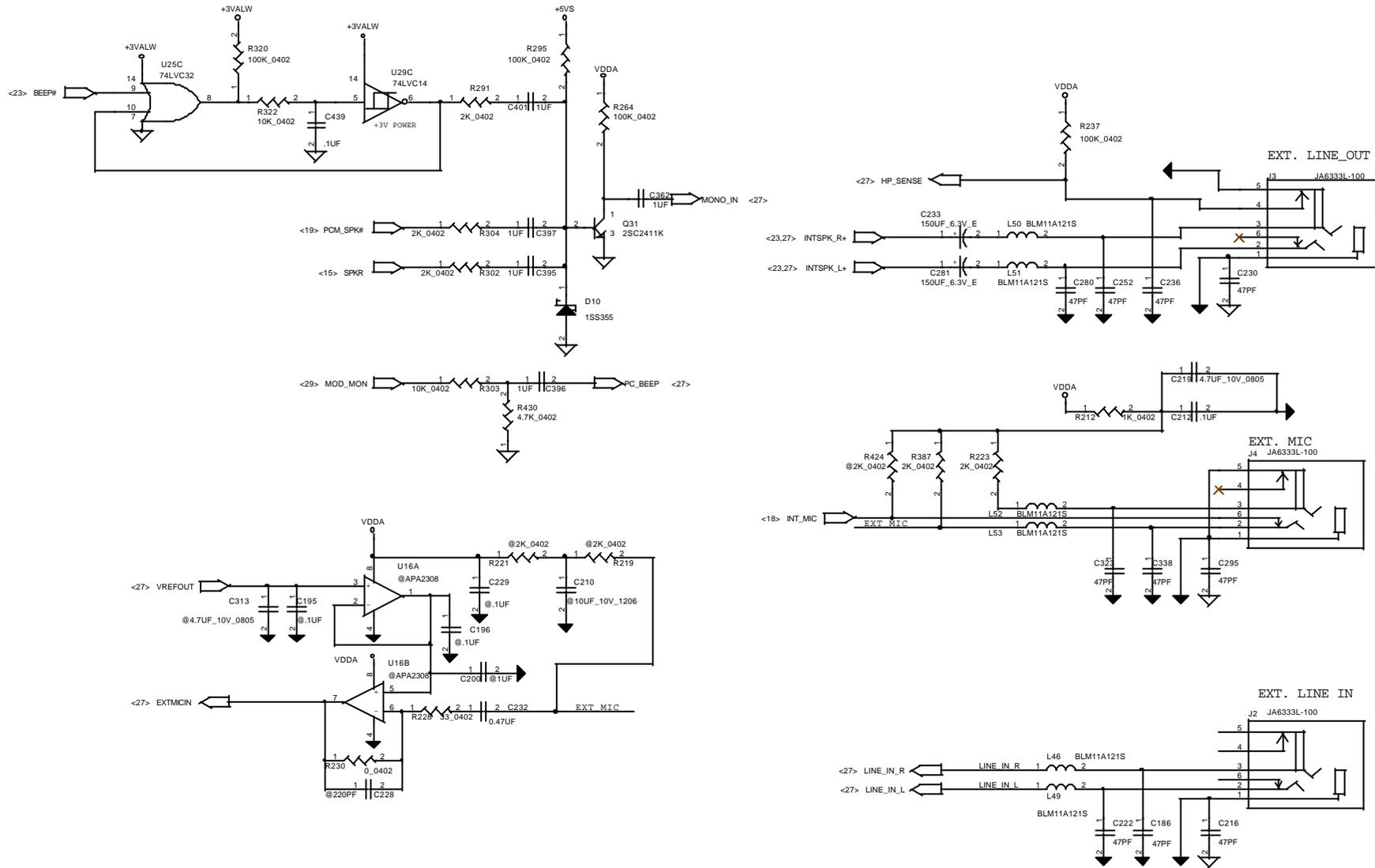
Compal Electronics, Inc.

File: **AUDIO CODEC & AMP**

Size: Document Number **888L2 Main Board** Rev **20**

Date: Thursday, January 11, 2001 Sheet 27 of 42

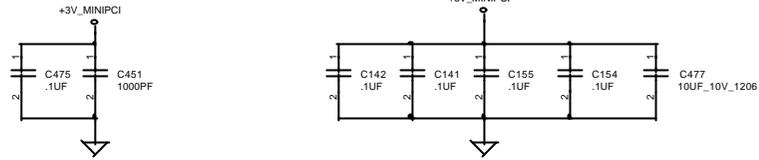
AUDIO JACK



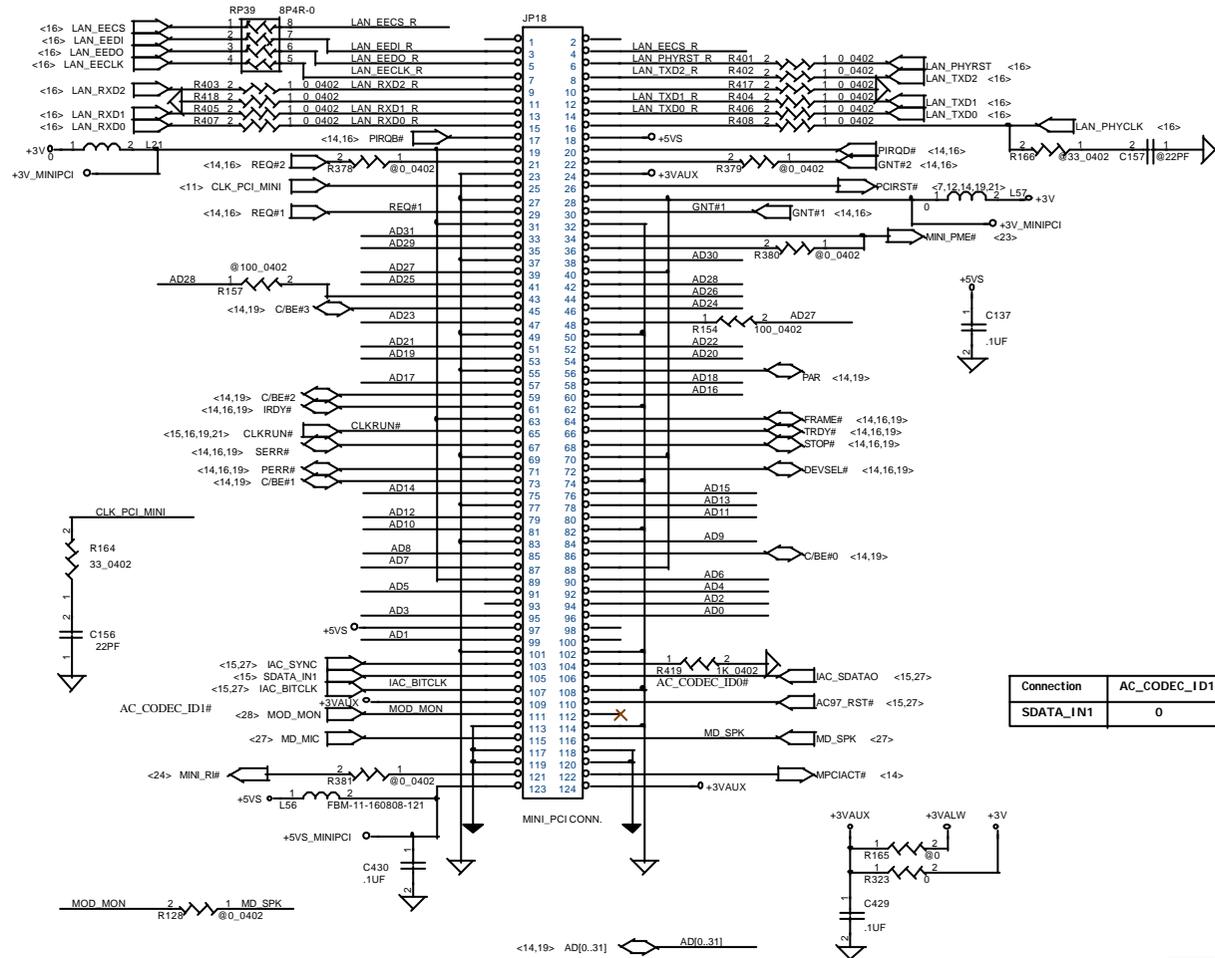
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Compal Electronics, Inc.		
File	MONO_IN	
Size	Document Number	Rev
	888L2 Main Board	20
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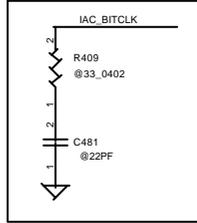
For Compal private Mini-PCI combo card - Mini-PCI type III c
 pin 21. LAN REQ#
 pin 22. LAN GNT#
 pin 36. LAN PME#
 pin 43. LAN IDSEL



MINI_PCI CONNECTOR



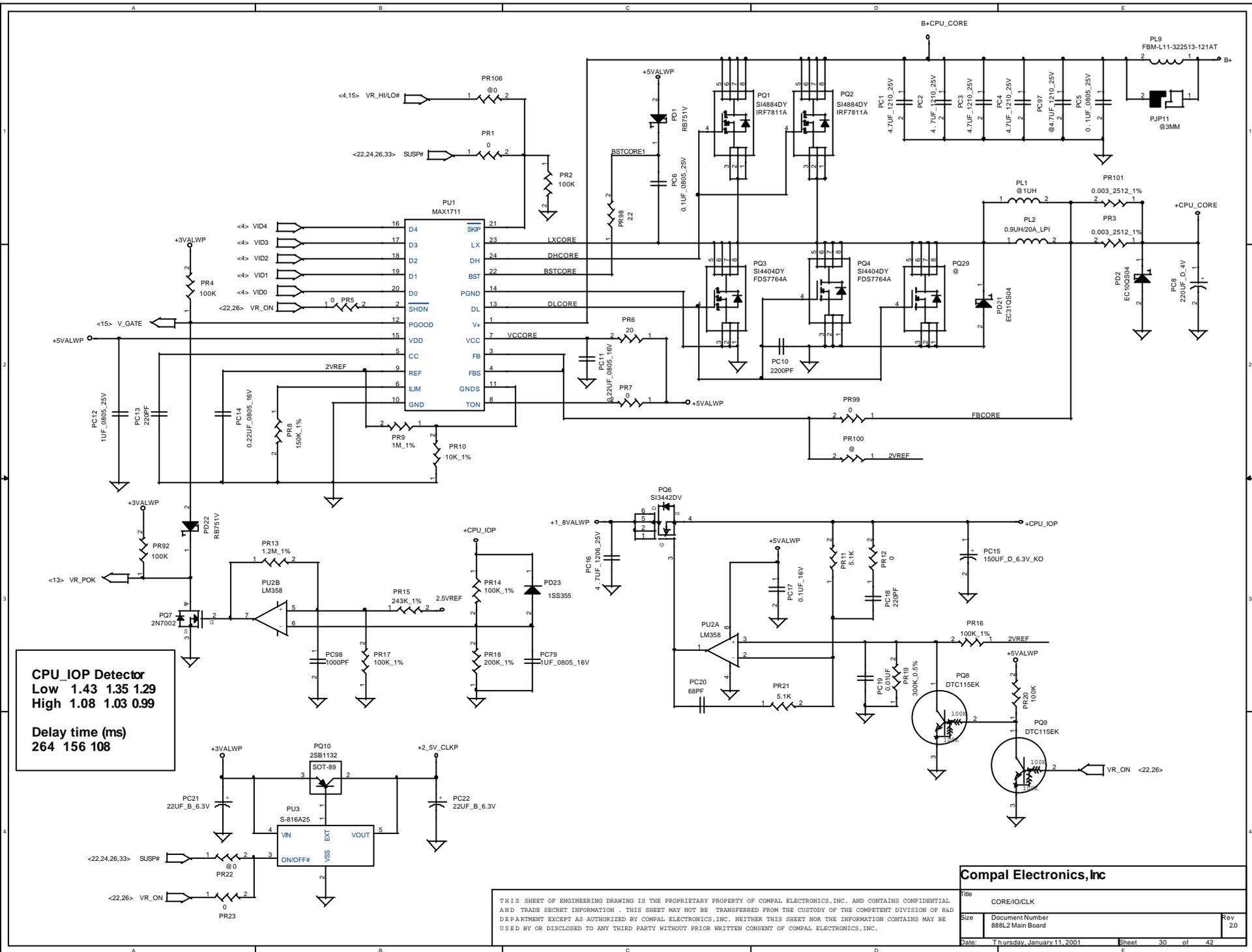
Connection	AC_CODECID1#	AC_CODECID0#
SDATA_IN1	0	1



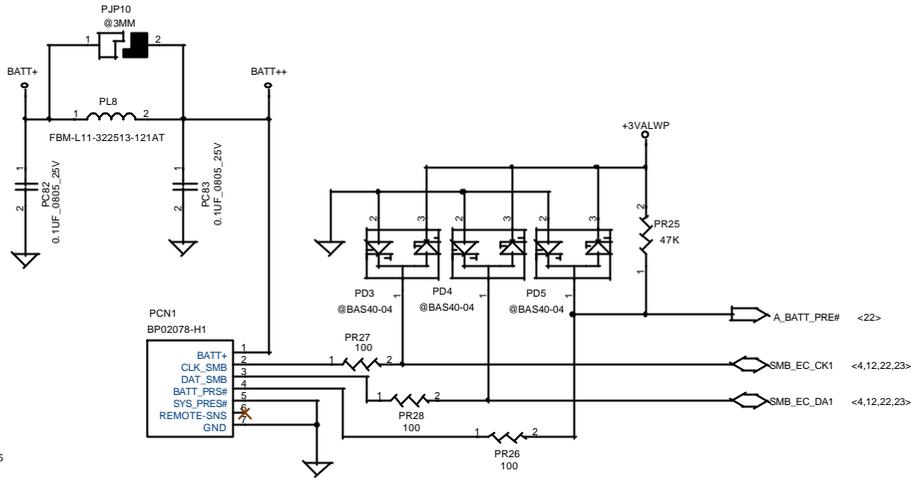
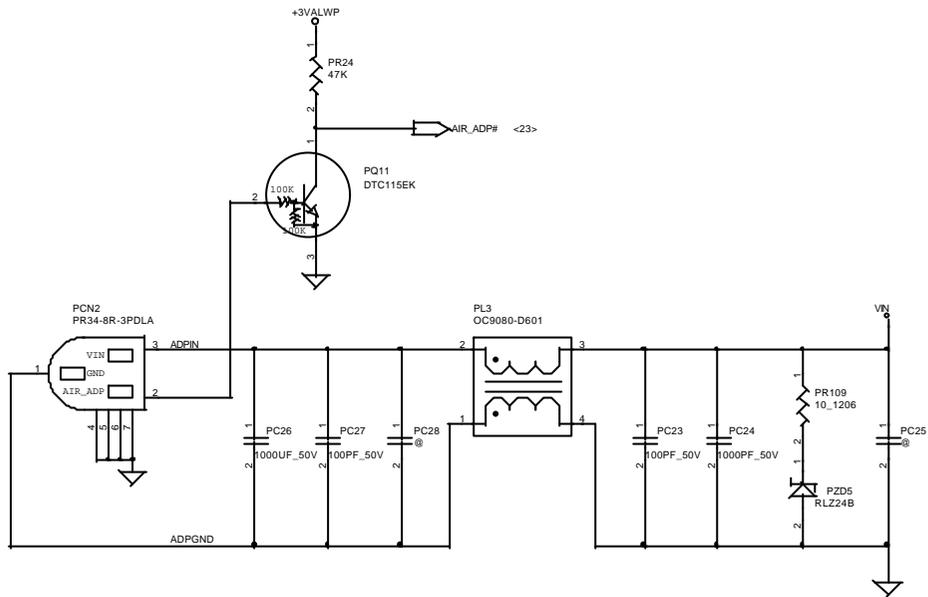
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Compal Electronics, Inc.

File		Mini-PCI Connector	
Size	Document Number	888L2 Main Board	
Date:	Thursday, January 11, 2001	Sheet	29 of 42
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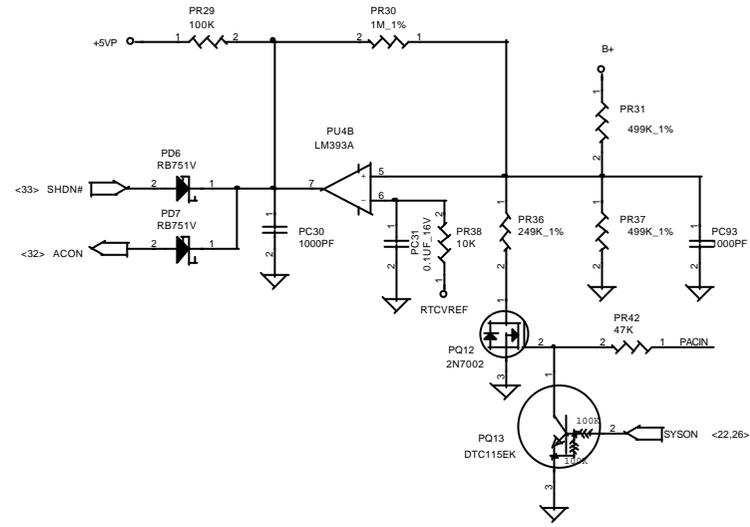
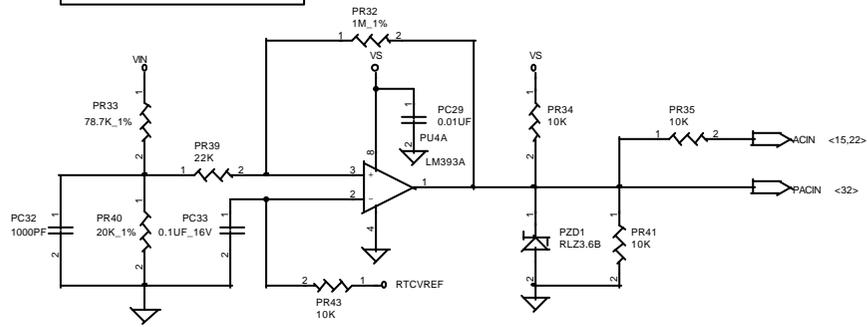


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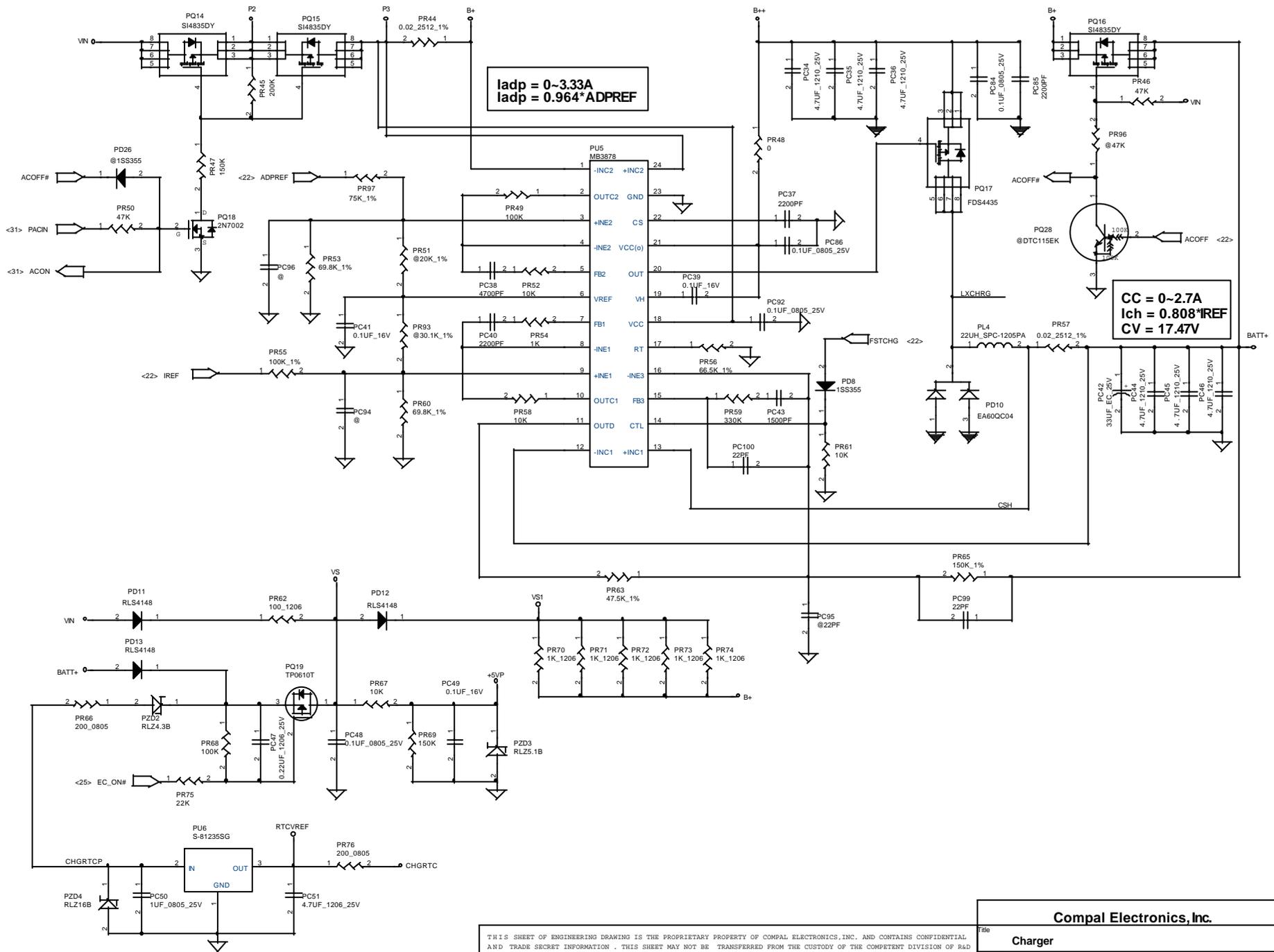
Precharge detector while AC adaptor
 High 16.5 15.8 15.1
 Low 13.9 13.2 12.5

Vin Detector
 High 18.7 17.9 17.1
 Low 18.0 17.3 16.5



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Compal Electronics, Inc.			
Detector			
File	Document Number	Rev	
	888L2 Main Board	20	
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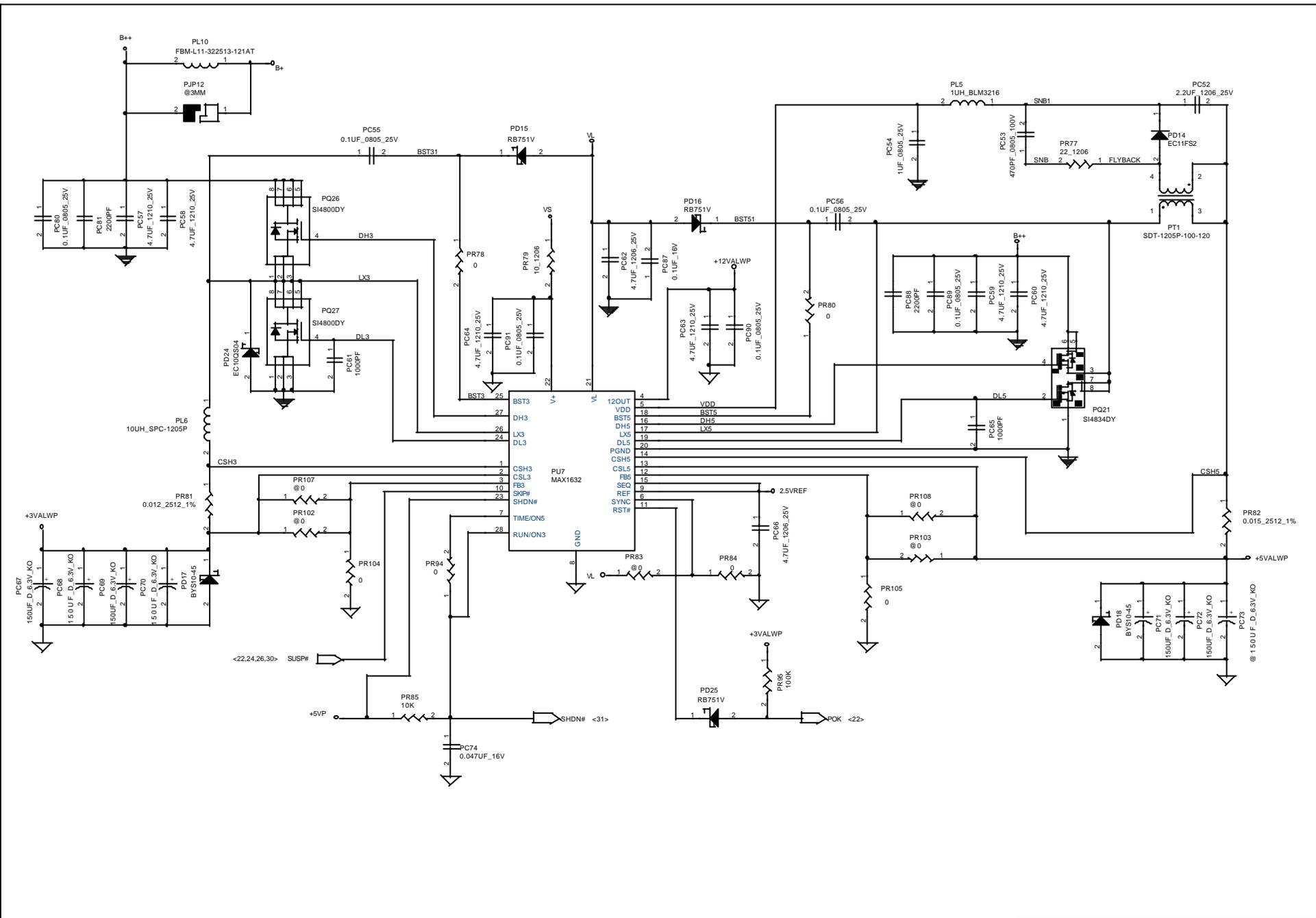


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ladp = 0.964*ADPREF

CC = 0~2.7A
Ich = 0.808*IREF
CV = 17.47V

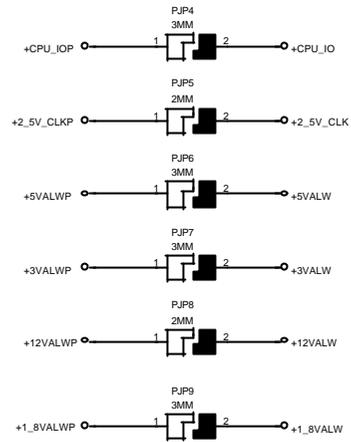
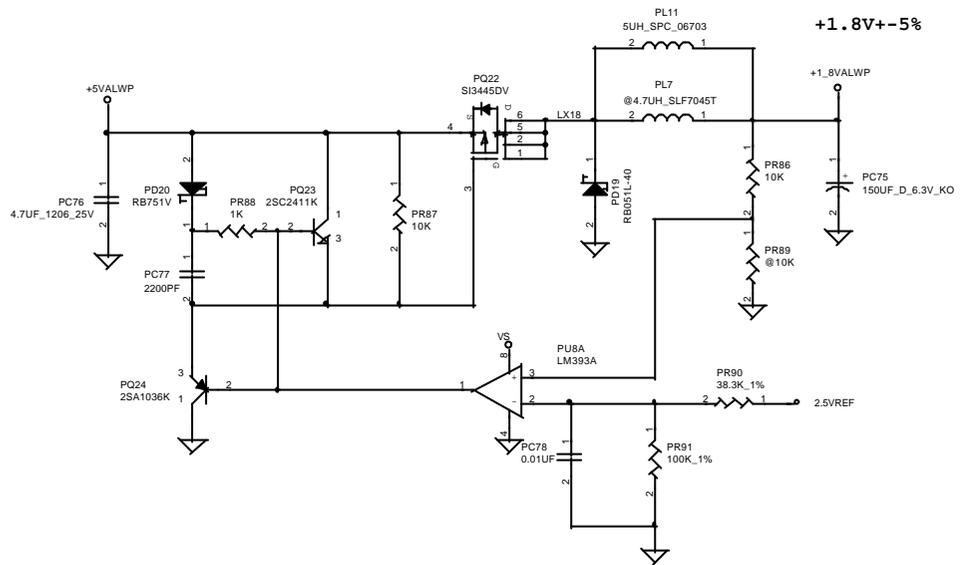
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Compal Electronics, Inc.			
Charger			
File	Document Number	Rev	
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Compal Electronics, Inc.		
Title	3.3V/5V/12V	
Size	Document Number	Rev
	888L2 Main Board	20
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Compal Electronics, Inc.		
File	+1.8VS	
Size	Document Number	Rev
	888L2 Main Board	20
Date:	Thursday, January 11, 2001	Sheet 34 of 42