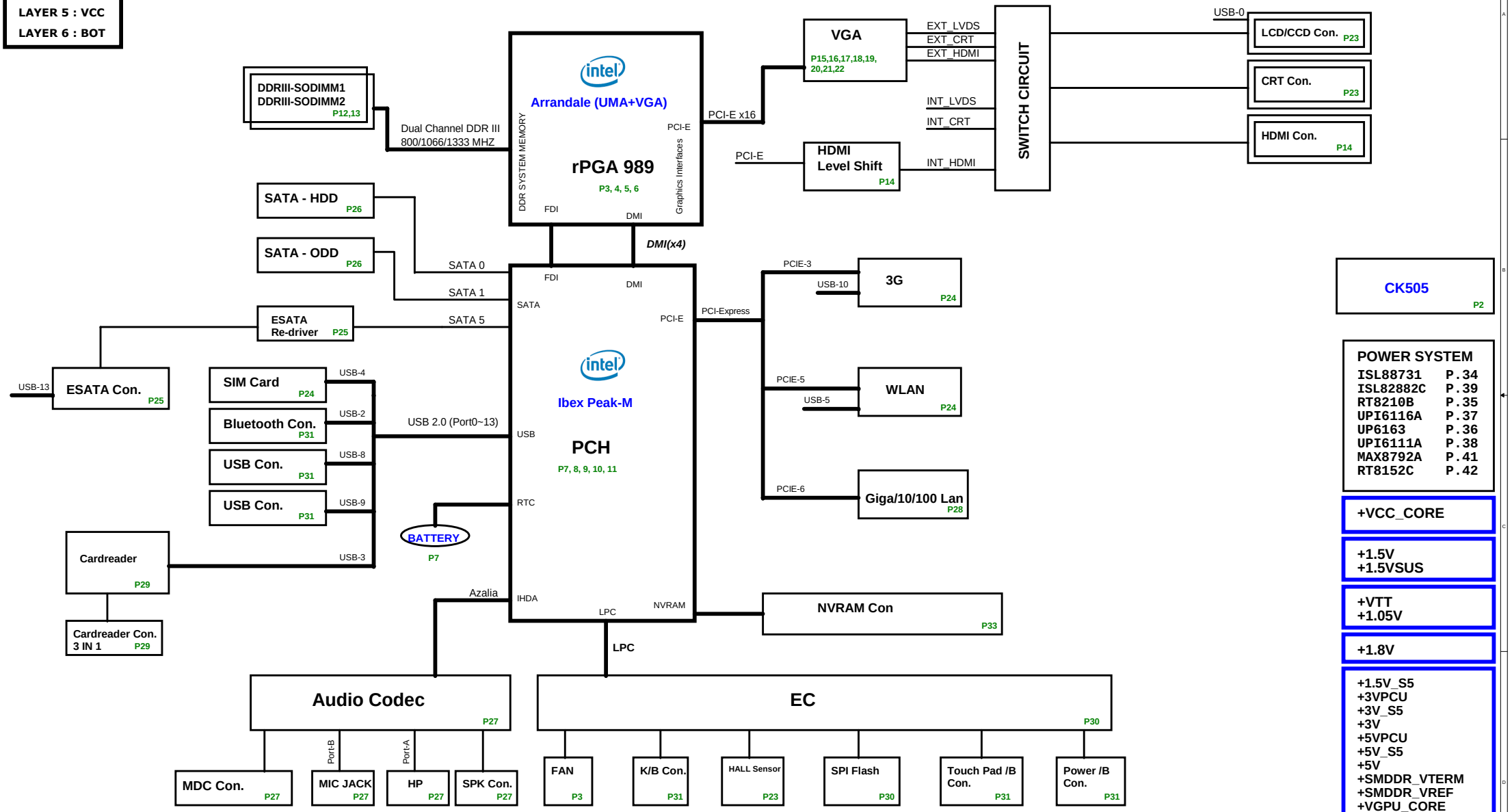
BL6 Block Diagram

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT



POWER SYSTEM

ISL88731	P.34
ISL82882C	P.39
RT8210B	P.35
UPI6116A	P.37
UP6163	P.36
UPI6111A	P.38
MAX8792A	P.41
RT8152C	P.42

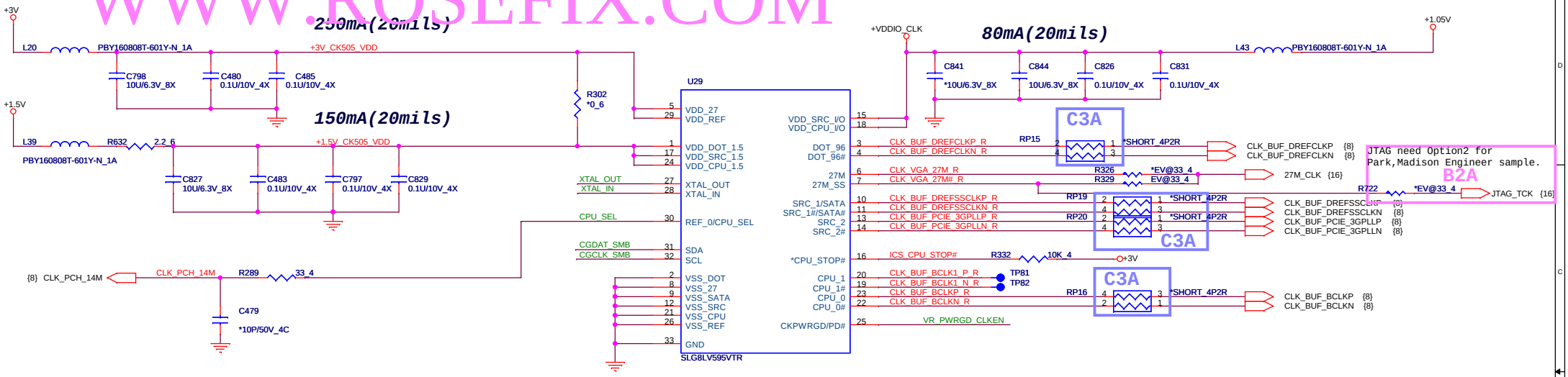
- +VCC_CORE
- +1.5V
  +1.5VSUS
- +VTT
  +1.05V
- +1.8V
- +1.5V_S5
  +3VPCU
  +3V_S5
  +3V
  +5VPCU
  +5V_S5
  +5V
  +SMDDR_VTERM
  +SMDDR_VREF
  +VGPU_CORE
  +VAXG

Quanta Computer Inc.
PROJECT : BL6

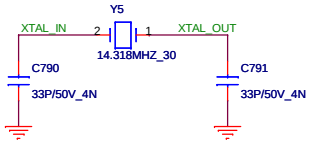
Size	Document Number	Rev
	Block Diagram	A1A

Date: Wednesday, April 07, 2010 Sheet 1 of 45

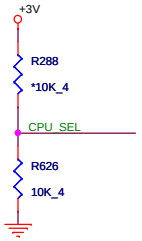
CLOCK Gen



CLK CRYSTAL

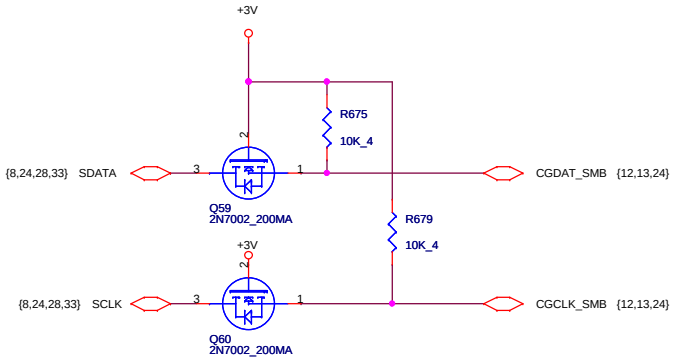


CLK CPU_SEL



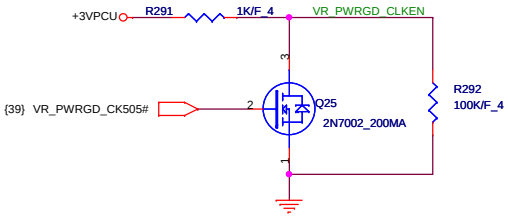
	0	1
CPU_SEL	CPU =133MHz (default)	CPU=100MHz

CLK I2C



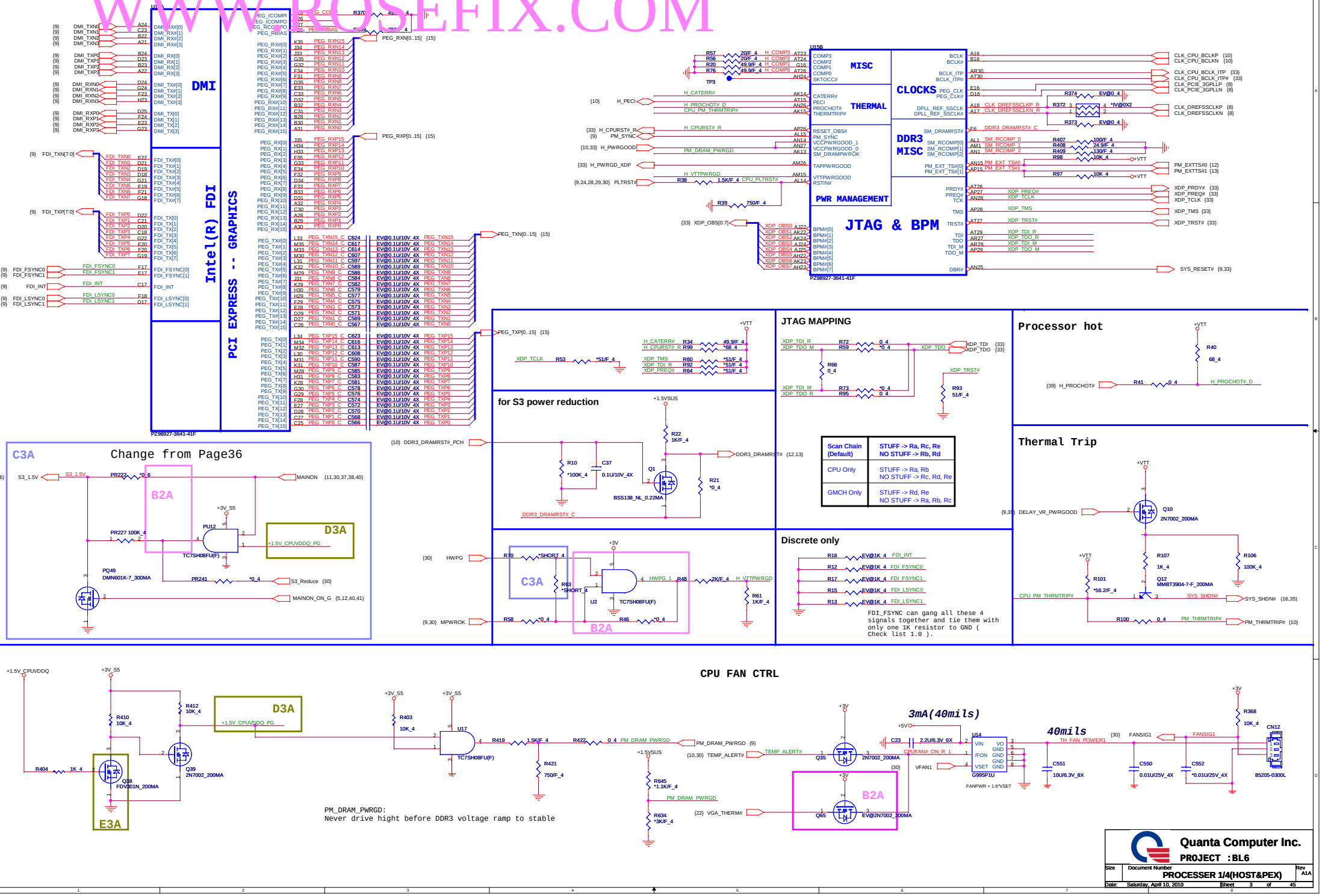
CLK POWERGOOD

Change to +3VPCU
(follow CRB)



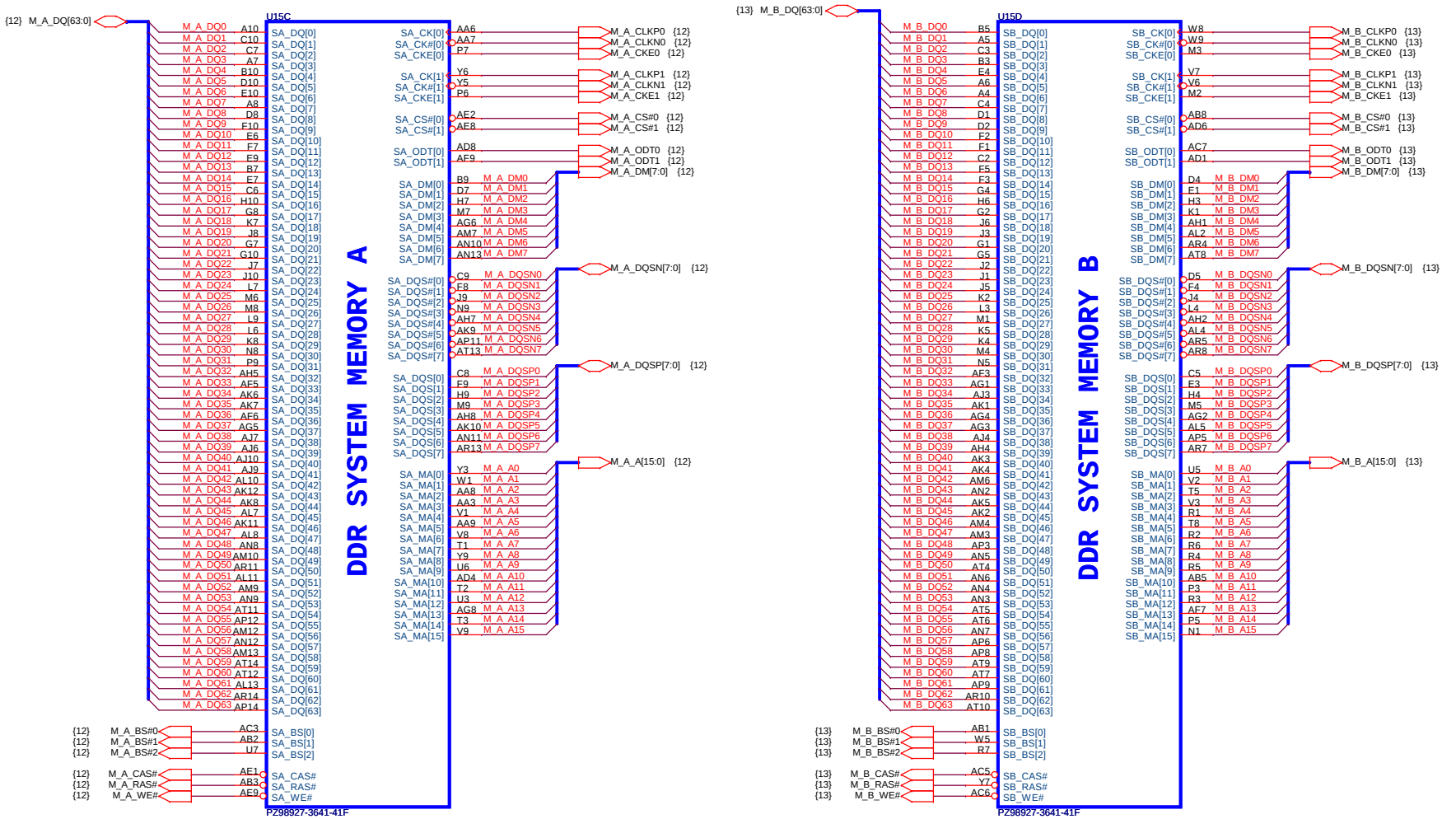
Quanta Computer Inc.
PROJECT : BL6

Size	Document Number	Rev
	CLOCK GENERATOR	A1A
Date: Thursday, April 08, 2010	Sheet 2 of 45	



Quanta Computer Inc.		
PROJECT : BL6		
Size	Document Number	Rev
	PROCESSER 1/4(HOST&PEX)	A1A
Date: Saturday, April 10, 2010	Sheet 3 of 45	

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

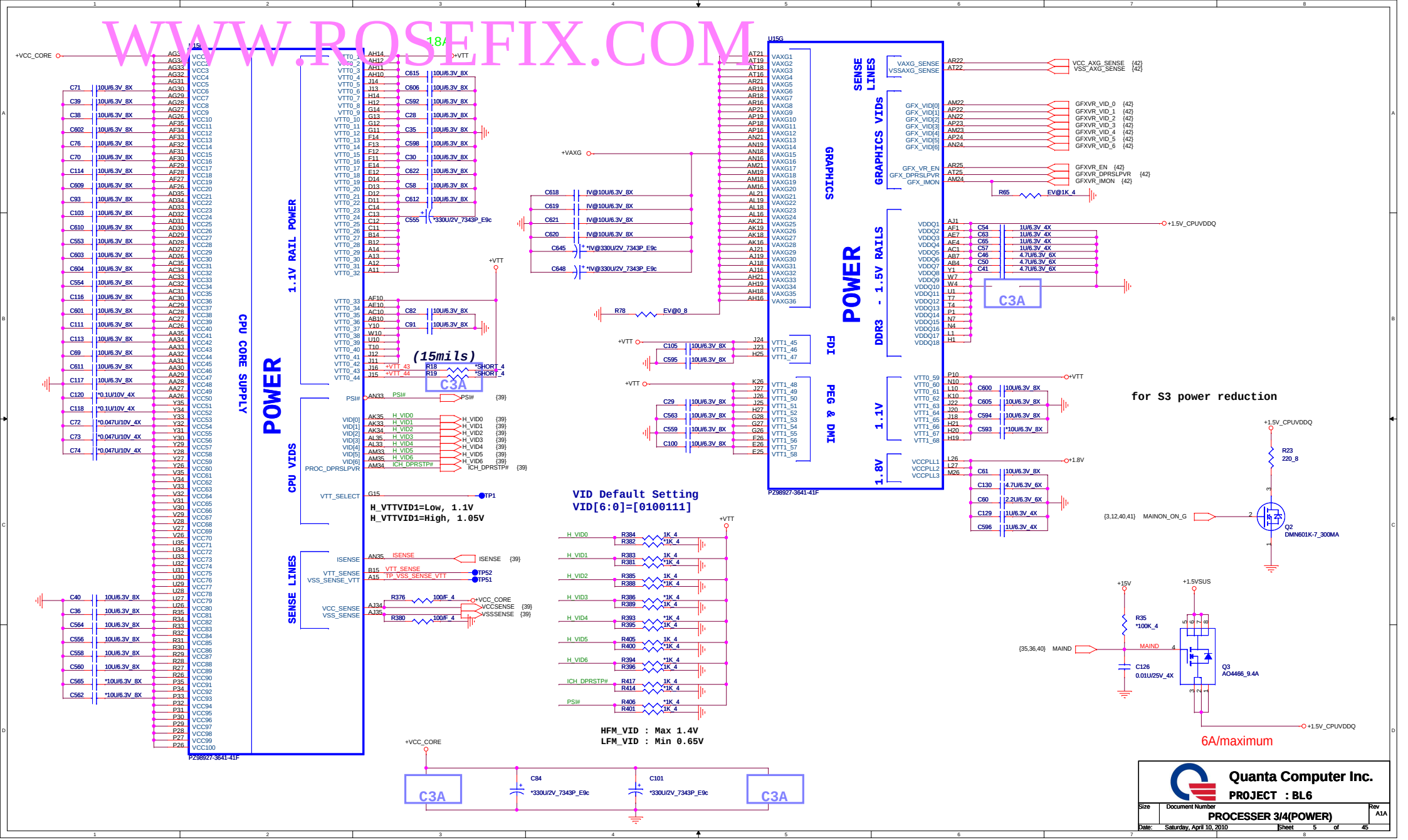


Quanta Computer Inc.

PROJECT : BL6

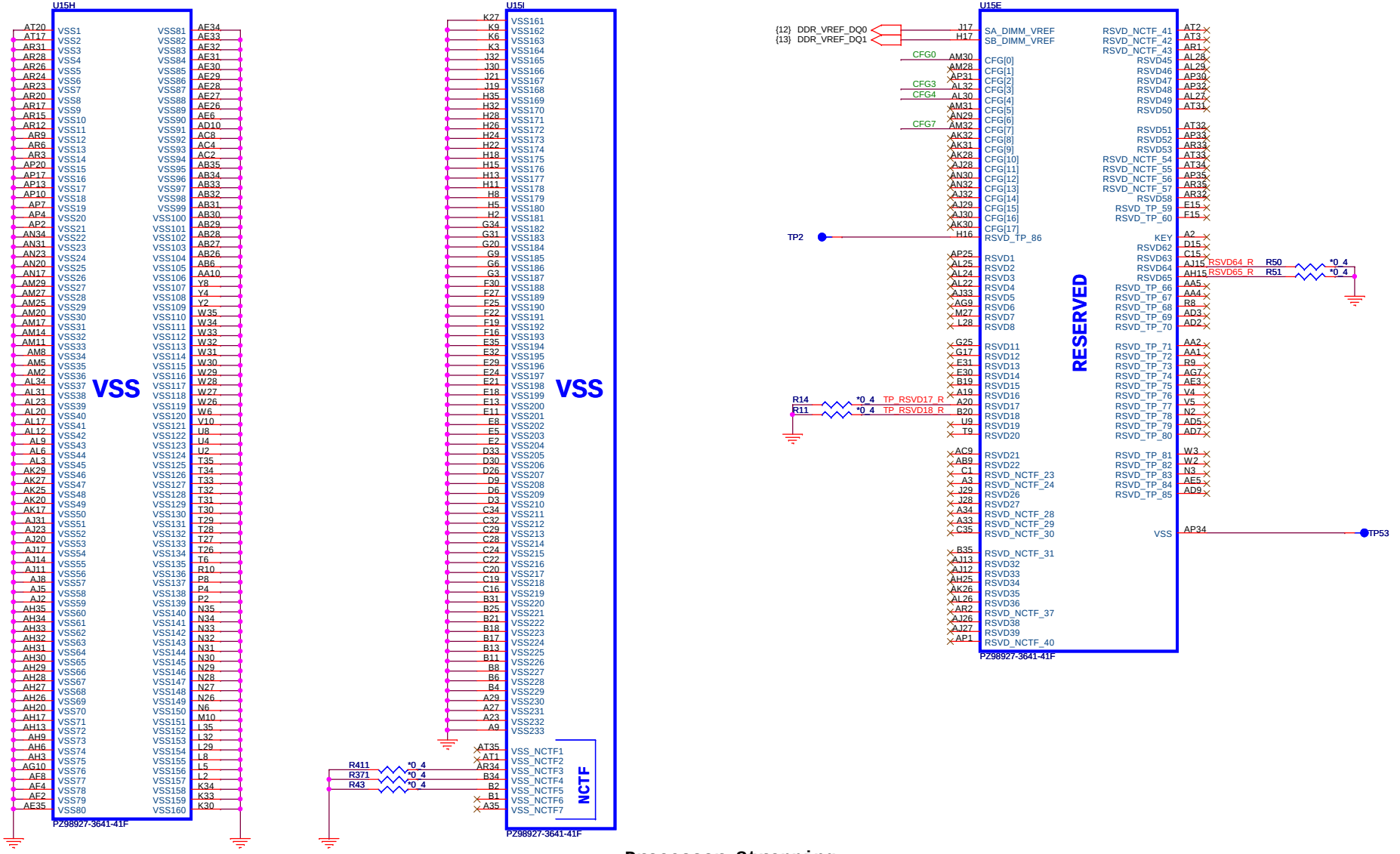
Size	Document Number	Rev
	PROCESSER 2/4(DDR)	A1A

Date: Saturday, April 10, 2010 Sheet 4 of 45



AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Processor Strapping

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	**Lane Numbers Reversed 15 -> 0 , 14 -> 1**

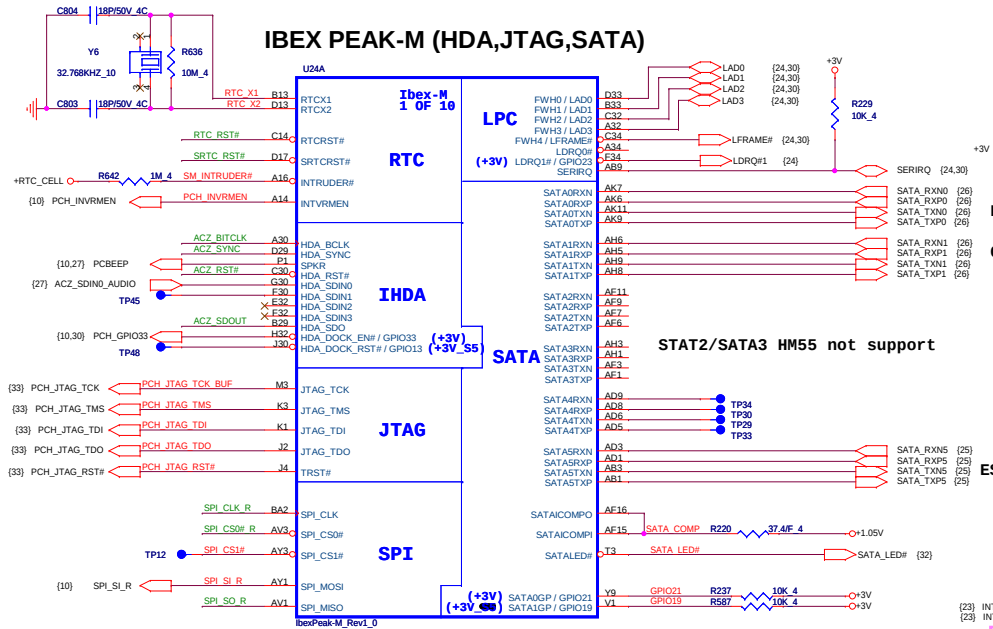
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

Quanta Computer Inc.
PROJECT : BL6

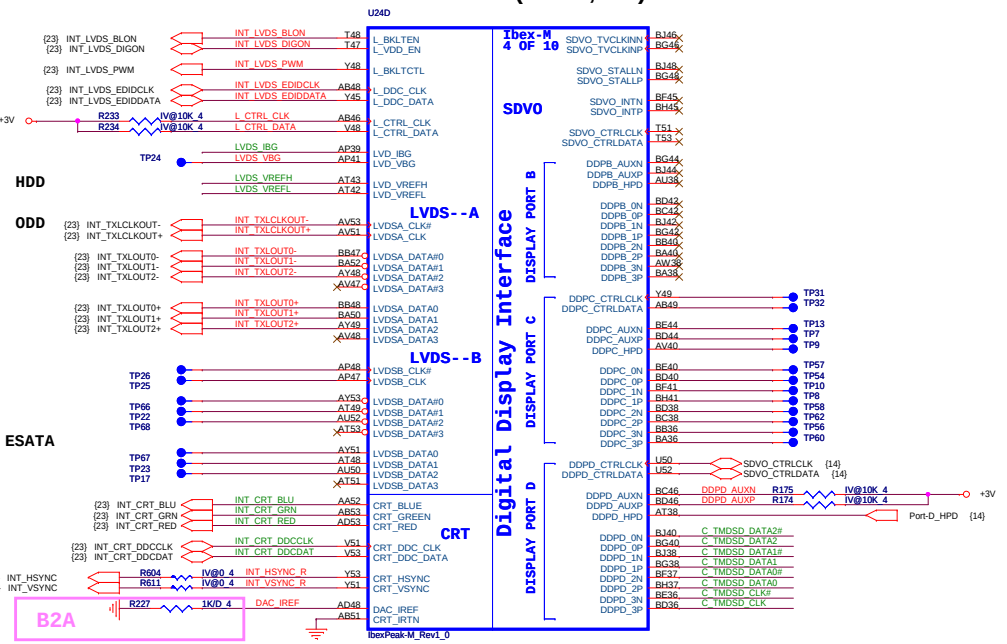
Size	Document Number	Rev
	PROCESSER 4/4 (GND)	1A

Date: Saturday, April 10, 2010 Sheet 6 of 45

IBEX PEAK-M (HDA,JTAG,SATA)

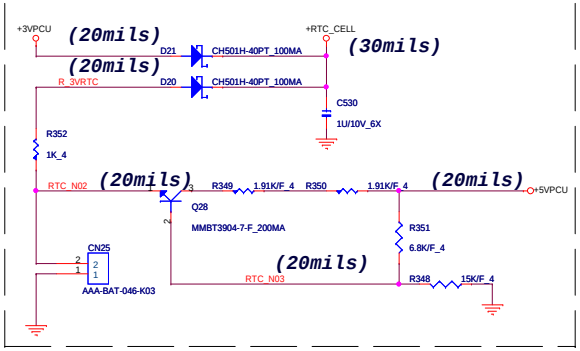


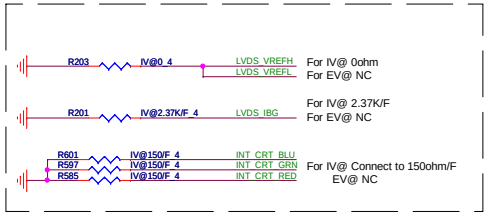
IBEX PEAK-M (LVDS,DDI)

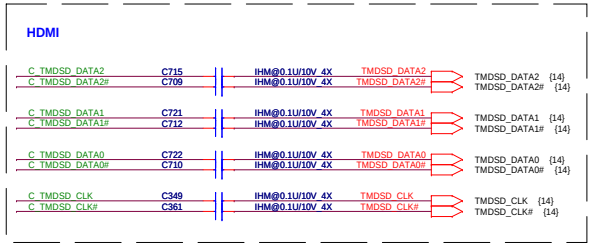


Port	Strap	How to enable Port?	How to disable Port?
LVDS	L_DDC_DATA	PU to 3.3V with 2.2k+/- 5%	NC
Port B	SDVO_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port C	DDPC_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port D	DDPD_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
eDP	CFG[4]	PD to GND directly	NC

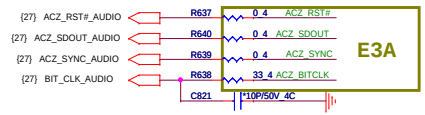
RTC BATTERY

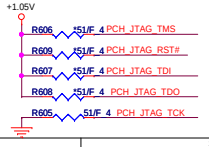






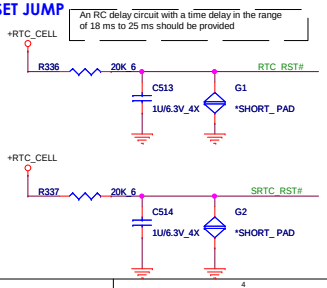
For AUDIO



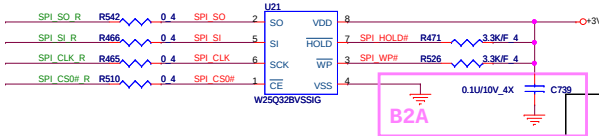


RESET JUMP

An RC delay circuit with a time delay in the range of 18 ms to 25 ms should be provided



4M byte SPI ROM



PCH	2MB	4MB	8MB
PM55	●		
HM55		●	
HM57/PM57		●	●
QM57/QS57			●

Quanta Computer Inc.
PROJECT : BL6

Size	Document Number	Rev
	PCH 1/5 (SATA,HDA,LPC)	A1A
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IBEX PEAK-M (GND)

U24I

AY7	VSS[159]	VSS[259]	H49
B11	VSS[160]	VSS[260]	H5
B15	VSS[161]	VSS[261]	J24
B19	VSS[162]	VSS[262]	K11
B23	VSS[163]	VSS[263]	K43
B31	VSS[164]	VSS[264]	K47
B35	VSS[165]	VSS[265]	K7
B39	VSS[166]	VSS[266]	L14
B43	VSS[167]	VSS[267]	L18
B47	VSS[168]	VSS[268]	L2
B7	VSS[169]	VSS[269]	L22
BG12	VSS[170]	VSS[270]	L32
BB12	VSS[171]	VSS[271]	L36
BB16	VSS[172]	VSS[272]	L40
BB20	VSS[173]	VSS[273]	L52
BB24	VSS[174]	VSS[274]	M12
BB30	VSS[175]	VSS[275]	M16
BB34	VSS[176]	VSS[276]	M20
BB38	VSS[177]	VSS[277]	M34
BB42	VSS[178]	VSS[278]	M38
BB49	VSS[179]	VSS[279]	M42
BB5	VSS[180]	VSS[280]	M46
BC10	VSS[181]	VSS[281]	M49
BC14	VSS[182]	VSS[282]	M5
BC18	VSS[183]	VSS[283]	M8
BC2	VSS[184]	VSS[284]	N24
BC22	VSS[185]	VSS[285]	P11
BC32	VSS[186]	VSS[286]	AD15
BC36	VSS[187]	VSS[287]	P22
BC40	VSS[188]	VSS[288]	P30
BC44	VSS[189]	VSS[289]	P32
BC52	VSS[190]	VSS[290]	P34
BH9	VSS[191]	VSS[291]	P42
BD48	VSS[192]	VSS[292]	P45
BD49	VSS[193]	VSS[293]	P47
BD5	VSS[194]	VSS[294]	R2
BE12	VSS[195]	VSS[295]	R52
BE16	VSS[196]	VSS[296]	T12
BE20	VSS[197]	VSS[297]	T41
BE24	VSS[198]	VSS[298]	T46
BE30	VSS[199]	VSS[299]	T49
BE34	VSS[200]	VSS[300]	T5
BE38	VSS[201]	VSS[301]	T8
BE42	VSS[202]	VSS[302]	U30
BE46	VSS[203]	VSS[303]	U31
BE48	VSS[204]	VSS[304]	U32
BE50	VSS[205]	VSS[305]	U34
BF6	VSS[206]	VSS[306]	P38
BF8	VSS[207]	VSS[307]	V11
BF3	VSS[208]	VSS[308]	P16
BF49	VSS[209]	VSS[309]	V19
BF51	VSS[210]	VSS[310]	V20
BG18	VSS[211]	VSS[311]	V22
BG24	VSS[212]	VSS[312]	V30
BG4	VSS[213]	VSS[313]	V31
BG50	VSS[214]	VSS[314]	V32
BH11	VSS[215]	VSS[315]	V34
BH15	VSS[216]	VSS[316]	V35
BH19	VSS[217]	VSS[317]	V38
BH23	VSS[218]	VSS[318]	V43
BH31	VSS[219]	VSS[319]	V45
BH35	VSS[220]	VSS[320]	V46
BH39	VSS[221]	VSS[321]	V47
BH43	VSS[222]	VSS[322]	V49
BH47	VSS[223]	VSS[323]	V5
BH7	VSS[224]	VSS[324]	V7
C12	VSS[225]	VSS[325]	V8
C50	VSS[226]	VSS[326]	W2
D51	VSS[227]	VSS[327]	W52
E12	VSS[228]	VSS[328]	Y11
E16	VSS[229]	VSS[329]	Y12
E20	VSS[230]	VSS[330]	Y15
E24	VSS[231]	VSS[331]	Y19
E30	VSS[232]	VSS[332]	Y23
E34	VSS[233]	VSS[333]	Y28
E38	VSS[234]	VSS[334]	Y30
E42	VSS[235]	VSS[335]	Y31
E46	VSS[236]	VSS[336]	Y32
E48	VSS[237]	VSS[337]	Y38
E6	VSS[238]	VSS[338]	Y43
E8	VSS[239]	VSS[339]	Y46
F49	VSS[240]	VSS[340]	P49
F5	VSS[241]	VSS[341]	Y5
G10	VSS[242]	VSS[342]	Y6
G14	VSS[243]	VSS[343]	Y8
G18	VSS[244]	VSS[344]	P24
G2	VSS[245]	VSS[345]	T43
G22	VSS[246]	VSS[346]	AD51
G32	VSS[247]	VSS[347]	AT8
G36	VSS[248]	VSS[348]	AD47
G40	VSS[249]	VSS[349]	Y47
G44	VSS[250]	VSS[350]	AT12
G52	VSS[251]	VSS[351]	AM6
AF39	VSS[252]	VSS[352]	AT13
H16	VSS[253]	VSS[353]	AM5
H20	VSS[254]	VSS[354]	AK45
H30	VSS[255]	VSS[355]	AK39
H34	VSS[256]	VSS[356]	AV14
H38	VSS[257]	VSS[366]	
H42	VSS[258]		

IbexPeak-M_Rev1_0

IBEX PEAK-M (PCI-E,SMBUS,CLK)

U24B

Ibex-M 2 OF 10

PCI-E*

SMBus

(+3V_S5) SMBALERT# / GPIO11 — B9 SMBALERT# — SCLK {2,24,28,33}
SMBCLK — H14 SCLK — SDATA {2,24,28,33}
SMBDATA — C8 SDATA
(+3V_S5) SML0ALERT# / GPIO60 — J14 SMBL0ALERT#
SML0CLK — C6 SMB_CLK_ME0
SML0DATA — G8 SMB_DATA_ME0
(+3V_S5) SML1ALERT# / GPIO74 — M14 SML1ALERT#
(+3V_S5) SML1CLK / GPIO58 — E10 MBCLK2
(+3V_S5) SML1DATA / GPIO75 — G12 MBDATA2

Controller Link

CL_CLK1 — T13 CL_CLK1 — CL_CLK1 {24}
CL_DATA1 — T11 CL_DATA1 — CL_DATA1 {24}
CL_RST1# — T9 CL_RST#1 — CL_RST#1 {24}

PEG

(+3V_S5) PEG_A_CLKRQ# / GPIO47 — H1 PEG_CLKREQ#
CLKOUT_PEG_A_N — AD43 — CLK_PCIE_VGA# {15}
CLKOUT_PEG_A_P — AD45 — CLK_PCIE_VGA {15}
CLKOUT_DMI_N — AN4 — CLK_PCIE_3GPLLN {3}
CLKOUT_DMI_P — AN2 — CLK_PCIE_3GPLLP {3}

From CLK BUFFER

CLKOUT_DP_N / CLKOUT_BCLK1_N — AT1 — CLK_DREFSSCLKN {3}
CLKOUT_DP_P / CLKOUT_BCLK1_P — AT3 — CLK_DREFSSCLKP {3}
CLKIN_DMI_N — AW24 — CLK_BUF_PCIE_3GPLLN {2}
CLKIN_DMI_P — BA24 — CLK_BUF_PCIE_3GPLLP {2}
CLKIN_BCLK_N — AP3 — CLK_BUF_BCLKN {2}
CLKIN_BCLK_P — AP1 — CLK_BUF_BCLKP {2}
CLKIN_DOT_96N — F18 — CLK_BUF_DREFCLKN {2}
CLKIN_DOT_96P — E18 — CLK_BUF_DREFCLKP {2}
CLKIN_SATA_N / CKSSCD_N — AH13 — CLK_BUF_DREFSSCLKN {2}
CLKIN_SATA_P / CKSSCD_P — AH12 — CLK_BUF_DREFSSCLKP {2}
REFCLK14IN — P41 — CLK_PCH_14M {2}
CLKIN_PCILOOPBACK — J42 — CLK_PCI_FB — CLK_PCI_FB {9}
XTAL25_IN — AH51 XTAL25_IN
XTAL25_OUT — AH53 XTAL25_OUT
XCLK_RCOMP — AF38 XCLK_RCOMP — R226 90.9/F_4 — +1.05V

Clock Flex

(+3V) CLKOUTFLEX0 / GPIO64 — T45 CLK_FLEX0 — R235 10K_4 — +3V
(+3V) CLKOUTFLEX1 / GPIO65 — P43 CLK_FLEX1 — T34
(+3V) CLKOUTFLEX2 / GPIO66 — T42 CLK_FLEX2 — T33
(+3V) CLKOUTFLEX3 / GPIO67 — N50 CLK_FLEX3 — R257 22_4 — 48M_CARD {29}

48M_Card Reserve for cardreader 48MHZ

IbexPeak-M_Rev1_0

3G

{24} PCIE_RXN3 — PCIE_RXN3 AU30
{24} PCIE_RXP3 — PCIE_RXP3 AT30
{24} PCIE_TXN3 — C364 *3G@0.1U/10V_4X — PCIE_TXN3_C AU32
{24} PCIE_TXP3 — C365 *3G@0.1U/10V_4X — PCIE_TXP3_C AV32

B2A

WLAN

{24} PCIE_RXN5 — PCIE_RXN5 BF33
{24} PCIE_RXP5 — PCIE_RXP5 BH33
{24} PCIE_TXN5 — C343 0.1U/10V_4X — PCIE_TXN5_C BG32
{24} PCIE_TXP5 — C342 0.1U/10V_4X — PCIE_TXP5_C BJ32

LAN

{28} PCIE_RXN6 — PCIE_RXN6 BA34
{28} PCIE_RXP6 — PCIE_RXP6 AW34
{28} PCIE_TXN6 — C379 0.1U/10V_4X — PCIE_TXN6_C BC34
{28} PCIE_TXP6 — C378 0.1U/10V_4X — PCIE_TXP6_C BD34

PCIE7/PCIE8 HM55 not support

B2A

TP74 — CLKOUT_PCIE0N AK48
TP87 — CLKOUT_PCIE0P AK47

PCIE_CLK_REQ0# — P9 — PCIECLKRQ0# / GPIO73 (+3V_S5)
TP21 — CLKOUT_PCIE1N AM43
TP27 — CLKOUT_PCIE1P AM45

PCIE_CLK_REQ1# — U4 — PCIECLKRQ1# / GPIO18 (+3V)

TP28 — CLKOUT_PCIE2N AM47
TP20 — CLKOUT_PCIE2P AM48

PCIE_CLK_REQ2# — N4 — PCIECLKRQ2# / GPIO20 (+3V)

LAN

{28} CLK_PCIE_LAN# — CLKOUT_PCIE3N AH42
{28} CLK_PCIE_LAN — CLKOUT_PCIE3P AH41

{28} PCIE_CLK_REQ3# — PCIE_CLK_REQ3# A8 — PCIECLKRQ3# / GPIO25 (+3V_S5)

3G

{24} CLK_PCIE_3G# — CLKOUT_PCIE4N AM51
{24} CLK_PCIE_3G — CLKOUT_PCIE4P AM53

{24} PCIE_CLK_REQ4# — PCIE_CLK_REQ4# M9 — PCIECLKRQ4# / GPIO26 (+3V_S5)

WLAN

{24} CLK_PCIE_MINI# — CLKOUT_PCIE5N AJ50
{24} CLK_PCIE_MINI — CLKOUT_PCIE5P AJ52

{24} PCIE_CLK_RQ5# — PCIE_CLK_RQ5# H6 — PCIECLKRQ5# / GPIO44 (+3V_S5)

TP70 — CLKOUT_PEG_B_N AK53
TP71 — CLKOUT_PEG_B_P AK51

PCIE_CLK_REQB# — P13 — PEG_B_CLKRQ# / GPIO56 (+3V_S5)

C3A

+3V_S5 — Q15 2N7002_200MA
MBDATA2 — 2ND_MBDATA {30}
+3V_S5 — Q13 2N7002_200MA
MBCLK2 — 2ND_MBCLK {30}

+3V

PCIE_CLK_REQ1# — R588 — 10K_4
PCIE_CLK_REQ2# — R600 — 10K_4

+3V_S5

SMBALERT# — R650 — 10K_4
SCLK — R311 — 2.2K_4
SDATA — R654 — 2.2K_4
SMBL0ALERT# — R300 — 10K_4
SMB_CLK_ME0 — R631 — 2.2K_4
SMB_DATA_ME0 — R623 — 2.2K_4
SML1ALERT# — R310 — 10K_4
MBCLK2 — R299 — 2.2K_4
MBDATA2 — R313 — 2.2K_4

+3V_S5

PCIE_CLK_REQ0# — R309 — 10K_4

B2A

PCIE_CLK_REQ3# — R653 — *10K_4
PCIE_CLK_REQ4# — R276 — 10K_4
PCIE_CLK_REQB# — R301 — 10K_4
PCIE_CLK_RQ5# — R619 — 10K_4
PEG_CLKREQ# — R615 — IV@10K_4
PEG_CLKREQ# — R610 — EV@10K_4

Placement close

R560 EV@0_4

XTAL25_IN — C749 IV@27P/50V_4N
R552 IV@1M/F_4
Y4 IV@25MHZ_30
XTAL25_OUT — C747 IV@27P/50V_4N

B2A

Quanta Computer Inc.	PROJECT : BL6		
Size	Document Number	PCH 2/5 (PCIE, SMBUS, CK)	Rev A1A
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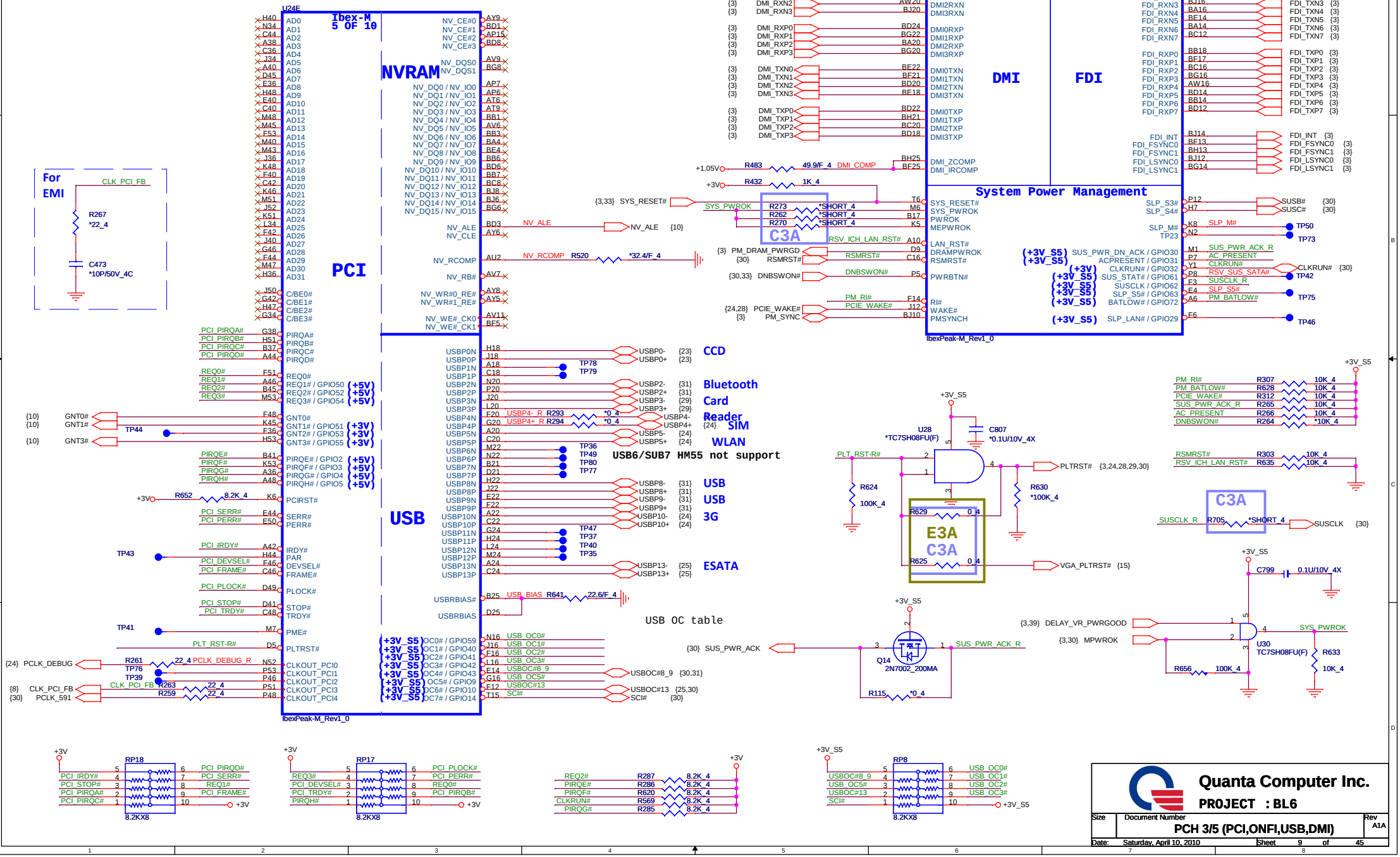
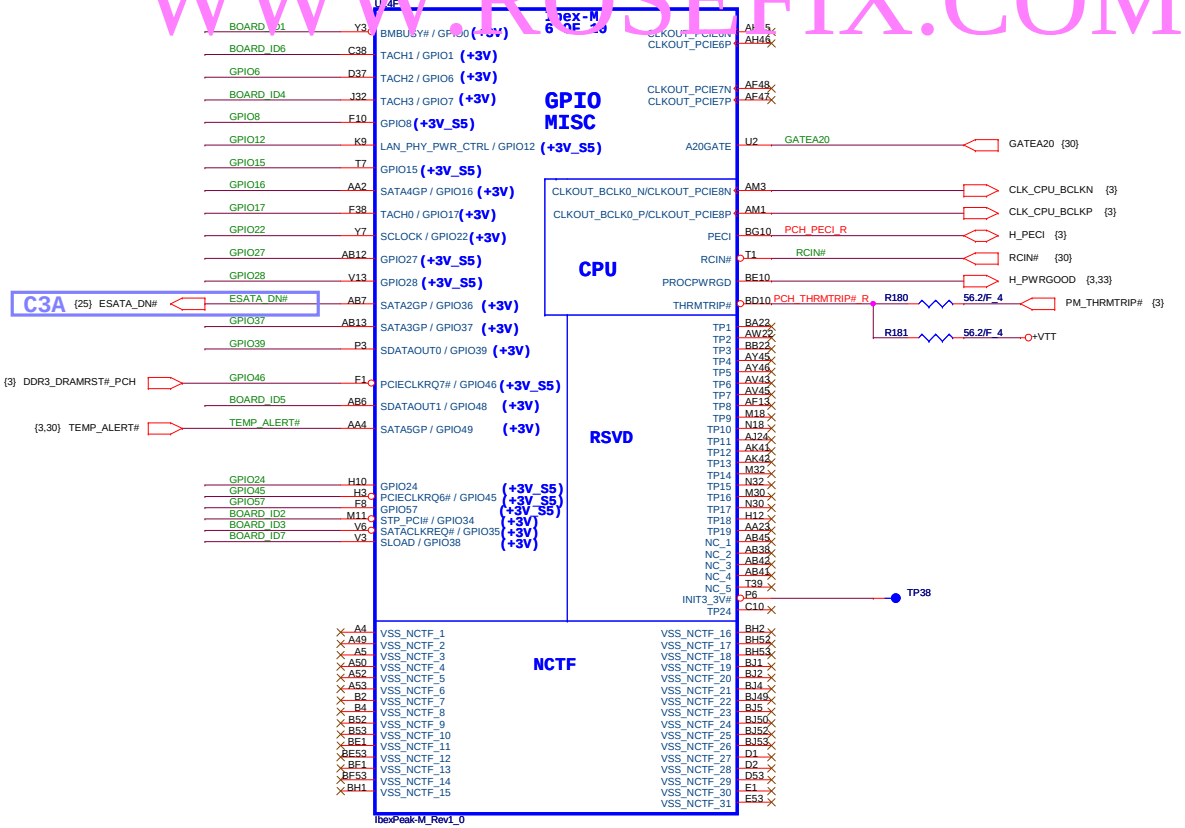
IBEX PEAK-M (DMI,FDI,GPIO)

IBEX PEAK-M (PCI,USB,NVRAM)

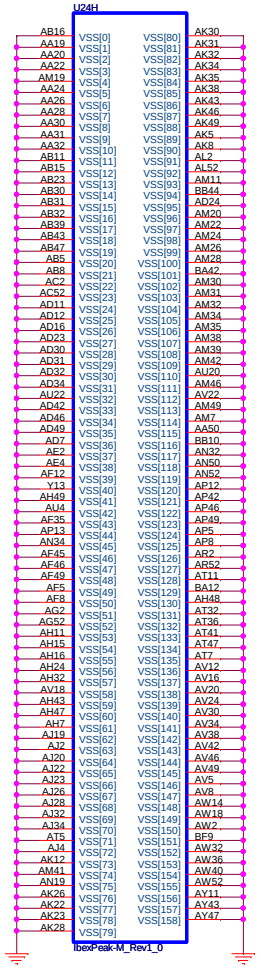


Quanta Computer Inc.			
PROJECT : BL6			
Size	Document Number		Rev
	PCH 3/5 (PCI,ONFI,USB,DMI)		A1A
Date: Saturday, April 10, 2010		Sheet 9 of 45	

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



IBEX PEAK-M (GND)



PCH Strap Pin Configuration Table

SPKR

{7,27} PCBEEP — R592 *1K_4 — +3V

Reboot option at power-up

0 = Default Mode (Internal weak Pull-down)
1 = No Reboot Mode with TCO Disabled

GNT3# / GPIO55

{9} GNT3# — R622 *10K_4

Top-Block Swap Override

0 = Top Block Swap Mode
1 = Default Mode (Internal pull-up)

HDA_DOCK_EN #/GPIO33

{7,30} PCH_GPIO33 — R282 1K_4 — E3A — JP1 2 — *SHORT PAD 1

Flash Descriptor Security Override

0 = Flash Descriptor Security will be overridden
1 = Security measure defined in the Flash Descriptor will be enabled.

GNT0#, GNT1#

{9} GNT0# — R272 *1K_4
{9} GNT1# — R621 *1K_4

Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved (NAND)
1	1	SPI

SPI_MOSI

{7} SPI_SI_R — R504 *1K_4 — +3V

TPM Functionality Disable

1 = Enabled
0 = Disable

NV_ALE

{9} NV_ALE — R496 *10K_4 — +1.8V

IntelR Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable

1 = Enabled
0 = Disabled (Default)

GPIO8

GPIO8 — R298 10K_4 — +3V_S5

Reserved

This signal has a weak internal pull up.
NOTE: This signal should not be pulled low

GPIO15

GPIO15 — R248 1K_4 — +3V_S5

Reserved

0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

GPIO27

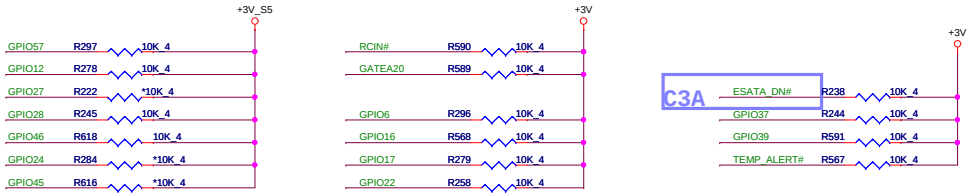
GPIO27 — R232 *10K_4

On-Die PLL Voltage Regulator

0 = Disables the VccVRM. Need to use on-board filter circuits for analog rails.
1 = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit.
This signal has a weak internal pull-up.

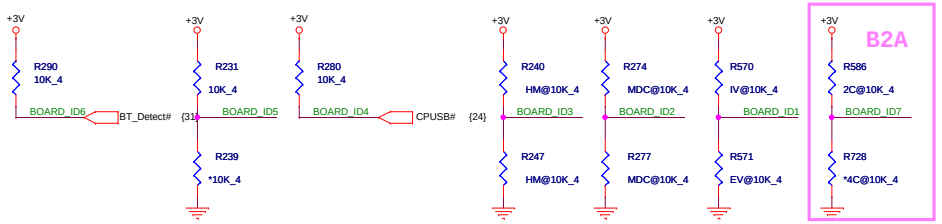
+RTC_CELL — R644 330K_6 — PCH_INVRMEN — PCH_INVRMEN {7}

```
INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs
```



BOARD ID SETTING

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7
UMA SKU VGA SKU	H L						
W/ MDC W/O MDC		H L					
W/ HDMI W/O HDMI			H L				
W/O 3G W/ 3G				H L			
15" 14"					H L		
W/O BT W/ BT						H L	
2 Core 4 Core							H L



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VCCCORE = 1.432A(80mils)

POWER

U24G Ibex-M 7 OF 10

VCC CORE

PCI E*

FDI

CRT

LVDS

HVCMOS

DMI

NAND / SPI

IbexPeak-M_Rev1_0

40mA(15mils)

VCCIO = 3.062A(150mils)

37mA(15mils)

68mA(15mils)

Reserve for clear CRT Power

Plcaement close to U52

+VCCA_DAC_1_2=69mA(15mils)

VCCALVDS= 59mA(15mils)

VCCTX_LVDS= 59mA(15mils)

VCCLAN = 0.32A(30mils)

VCCME = 1.849A(100mils)

VCCDMI= 61mA(15mils)

VCC3_3 = 0.357A(30mils)

VCCVRM= 196mA(15mils)

VCCPNAND= 156mA(15mils)

VCCME3_3= 85mA(15mils)

VCCIO = 3.062A(150mils)

Isolate the power supply for pins AF32,AF34,AH34
Reduce the jitter on HDMI interface for
1080P 60Hz Deep color mode.

VCCSUS3_3 = 0.163A(20mils)

VCC3_3 = 0.357A(30mils)

V_CPU >1mA(15mils)

VCCRTC= 2mA(15mils)

VCCSUSHDA= 6mA(15mils)

POWER

U24J Ibex-M 10 OF 10

Clock and Miscellaneous

USB

PCI/GPIO/LPC

SATA

CPU

RTC

HDA

IbexPeak-M_Rev1_0

VCCIO = 3.062A(150mils)

VCCSUS3_3 = 0.163A(20mils)

V5REF_SUS< 1mA

V5REF< 1mA

VCC3_3 = 0.357A(30mils)

VCCIO = 3.062A(150mils)

VCCME = 1.849A(100mils)

Quanta Computer Inc.		
PROJECT : BL6		
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H=4

JDIM1A

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDRRK-20401-TP4B

{4} M_A_A[15:0]

M_A_A0 98 A0
M_A_A1 97 A1
M_A_A2 96 A2
M_A_A3 95 A3
M_A_A4 92 A4
M_A_A5 91 A5
M_A_A6 90 A6
M_A_A7 86 A7
M_A_A8 89 A8
M_A_A9 85 A9
M_A_A10 107 A10/AP
M_A_A11 84 A11
M_A_A12 83 A12/BC#
M_A_A13 119 A13
M_A_A14 80 A14
M_A_A15 78 A15

M_A_DQ[63:0] {4}

M_A_DQ0 5 DQ0
M_A_DQ1 7 DQ1
M_A_DQ2 15 DQ2
M_A_DQ3 17 DQ3
M_A_DQ4 4 DQ4
M_A_DQ5 6 DQ5
M_A_DQ6 16 DQ6
M_A_DQ7 18 DQ7
M_A_DQ8 21 DQ8
M_A_DQ9 23 DQ9
M_A_DQ10 33 DQ10
M_A_DQ11 35 DQ11
M_A_DQ12 22 DQ12
M_A_DQ13 24 DQ13
M_A_DQ14 34 DQ14
M_A_DQ15 36 DQ15
M_A_DQ16 39 DQ16
M_A_DQ17 41 DQ17
M_A_DQ18 51 DQ18
M_A_DQ19 53 DQ19
M_A_DQ20 40 DQ20
M_A_DQ21 42 DQ21
M_A_DQ22 50 DQ22
M_A_DQ23 52 DQ23
M_A_DQ24 57 DQ24
M_A_DQ25 59 DQ25
M_A_DQ26 67 DQ26
M_A_DQ27 69 DQ27
M_A_DQ28 56 DQ28
M_A_DQ29 58 DQ29
M_A_DQ30 68 DQ30
M_A_DQ31 70 DQ31
M_A_DQ32 129 DQ32
M_A_DQ33 131 DQ33
M_A_DQ34 141 DQ34
M_A_DQ35 143 DQ35
M_A_DQ36 130 DQ36
M_A_DQ37 132 DQ37
M_A_DQ38 140 DQ38
M_A_DQ39 142 DQ39
M_A_DQ40 147 DQ40
M_A_DQ41 149 DQ41
M_A_DQ42 157 DQ42
M_A_DQ43 159 DQ43
M_A_DQ44 146 DQ44
M_A_DQ45 148 DQ45
M_A_DQ46 158 DQ46
M_A_DQ47 160 DQ47
M_A_DQ48 163 DQ48
M_A_DQ49 165 DQ49
M_A_DQ50 175 DQ50
M_A_DQ51 177 DQ51
M_A_DQ52 164 DQ52
M_A_DQ53 166 DQ53
M_A_DQ54 174 DQ54
M_A_DQ55 176 DQ55
M_A_DQ56 181 DQ56
M_A_DQ57 183 DQ57
M_A_DQ58 191 DQ58
M_A_DQ59 193 DQ59
M_A_DQ60 180 DQ60
M_A_DQ61 182 DQ61
M_A_DQ62 192 DQ62
M_A_DQ63 194 DQ63

{4} M_A_BS#0 109 BA0
{4} M_A_BS#1 108 BA1
{4} M_A_BS#2 79 BA2
{4} M_A_CS#0 114 S0#
{4} M_A_CS#1 121 S1#
{4} M_A_CLKP0 101 CK0
{4} M_A_CLKN0 103 CK0#
{4} M_A_CLKP1 102 CK1
{4} M_A_CLKN1 104 CK1#
{4} M_A_CKE0 73 CKE0
{4} M_A_CKE1 74 CKE1
{4} M_A_CAS# 115 CAS#
{4} M_A_RAS# 110 RAS#
{4} M_A_WE# 113 WE#

R44 10K/F_4 DIMM0_SA0 197 SA0
R42 10K/F_4 DIMM0_SA1 201 SA1

{2,13,24} CGCLK_SMB 202 SCL
{2,13,24} CGDAT_SMB 200 SDA

{4} M_A_ODT0 116 ODT0
{4} M_A_ODT1 120 ODT1

{4} M_A_DM[7:0]

M_A_DM0 11 DM0
M_A_DM1 28 DM1
M_A_DM2 46 DM2
M_A_DM3 63 DM3
M_A_DM4 136 DM4
M_A_DM5 153 DM5
M_A_DM6 170 DM6
M_A_DM7 187 DM7

{4} M_A_DQSP[7:0]

M_A_DQSP0 12 DQS0
M_A_DQSP1 29 DQS1
M_A_DQSP2 47 DQS2
M_A_DQSP3 64 DQS3
M_A_DQSP4 137 DQS4
M_A_DQSP5 154 DQS5
M_A_DQSP6 171 DQS6
M_A_DQSP7 188 DQS7

{4} M_A_DQSN[7:0]

M_A_DQSN0 10 DQS#0
M_A_DQSN1 27 DQS#1
M_A_DQSN2 45 DQS#2
M_A_DQSN3 62 DQS#3
M_A_DQSN4 135 DQS#4
M_A_DQSN5 152 DQS#5
M_A_DQSN6 169 DQS#6
M_A_DQSN7 186 DQS#7

+1.5VSUS

JDIM1B

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDRRK-20401-TP4B

VDD1 75
VDD2 76
VDD3 81
VDD4 82
VDD5 87
VDD6 88
VDD7 93
VDD8 94
VDD9 99
VDD10 100
VDD11 105
VDD12 106
VDD13 111
VDD14 112
VDD15 117
VDD16 118
VDD17 123
VDD18 124

+3V

VDDSPD 199

for S3 power reduction

NC1 77
NC2 122
NCTEST 125

{3} PM_EXTTS#0
PM_EXTTS#0 198 EVENT#
{3,13} DDR3_DRAMRST# 30 RESET#

{6} DDR_VREF_DQ0

R8 *0_6 SMDDR_VREF_DQ0
SMDDR_VREF_DIMM 1 VREF_DQ
126 VREF_CA

R7 100K_4

VSS1 2
VSS2 3
VSS3 8
VSS4 9
VSS5 13
VSS6 14
VSS7 19
VSS8 20
VSS9 25
VSS10 26
VSS11 31
VSS12 32
VSS13 37
VSS14 38
VSS15 43

VSS16 44
VSS17 48
VSS18 49
VSS19 54
VSS20 55
VSS21 60
VSS22 61
VSS23 65
VSS24 66
VSS25 71
VSS26 72
VSS27 127
VSS28 128
VSS29 133
VSS30 134
VSS31 138
VSS32 139
VSS33 144
VSS34 145
VSS35 150
VSS36 151
VSS37 155
VSS38 156
VSS39 161
VSS40 162
VSS41 167
VSS42 168
VSS43 172
VSS44 173
VSS45 178
VSS46 179
VSS47 184
VSS48 185
VSS49 189
VSS50 190
VSS51 195
VSS52 196

VTT1 203 +SMDDR_VTERM
VTT2 204

GND 205
GND 206

+SMDDR_VTERM

R69 22_4

Q4 2N7002_200MA

{3,5,40,41} MAINON_ON_G

C107 470P/50V_4X
R32 *10K/F_4
R30 0_4
R29 *10K/F_4

SMDDR_VREF_DIMM {13}
+SMDDR_VREF
+1.5VSUS

Place these Caps near So-Dimm0.

+1.5VSUS

C62 4.7U/6.3V_6X
C51 4.7U/6.3V_6X
C42 4.7U/6.3V_6X
C80 4.7U/6.3V_6X
C85 4.7U/6.3V_6X
C99 4.7U/6.3V_6X
C43 0.1U/10V_4X
C79 0.1U/10V_4X
C53 0.1U/10V_4X
C67 0.1U/10V_4X
C95 0.1U/10V_4X
C47 *0.047U/10V_4X
C89 *0.047U/10V_4X

SMDDR_VREF_DQ0

C26 0.1U/10V_4X
C34 2.2U/6.3V_6X

SMDDR_VREF_DIMM

C108 0.1U/10V_4X
C124 2.2U/6.3V_6X
C125 *0.047U/10V_4X

+3V

C167 2.2U/6.3V_6X
C162 *0.1U/10V_4X
C156 *0.047U/10V_4X

+SMDDR_VTERM

C170 1U/6.3V_4X
C182 1U/6.3V_4X
C168 1U/6.3V_4X
C171 1U/6.3V_4X
C166 *10U/6.3V_8X
C174 *10U/6.3V_8X
C179 4.7U/6.3V_6X
C181 *0.047U/10V_4X
C165 *0.047U/10V_4X

+1.5VSUS

R9 1K/F_4

SMDDR_VREF_DQ0

R6 1K/F_4
C25 0.1U/10V_4X
C32 *0.047U/10V_4X

+1.5VSUS

C599 *330U/2.5V_7343P_E9a

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	DDR3 DIMM-0	A1A

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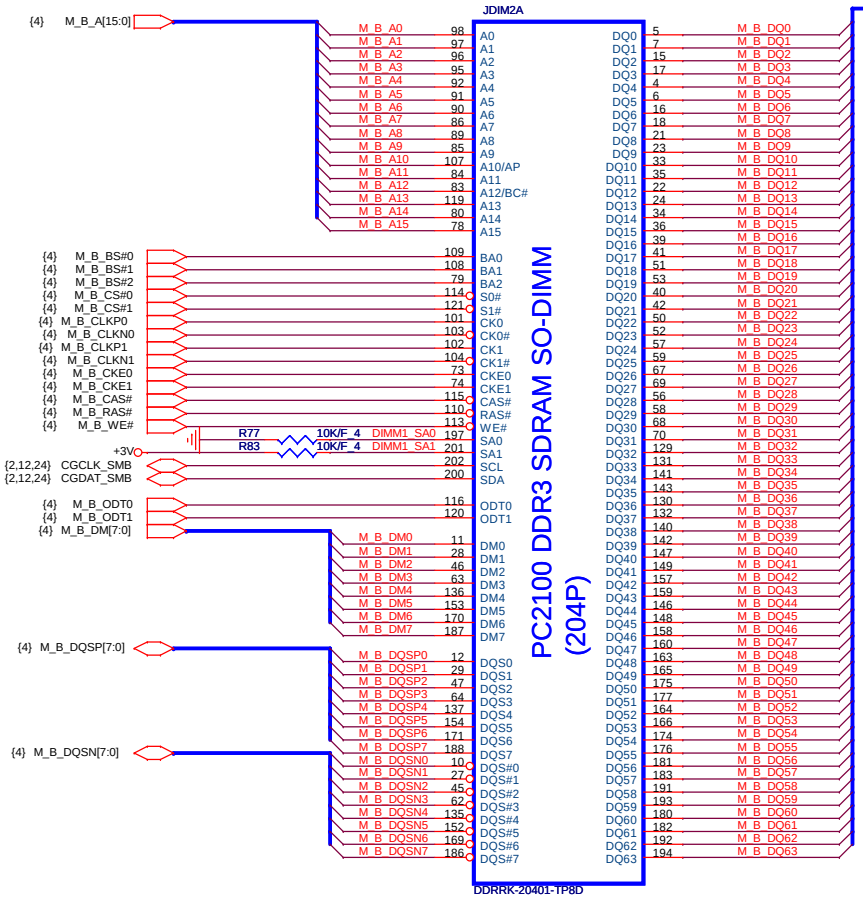
H=8



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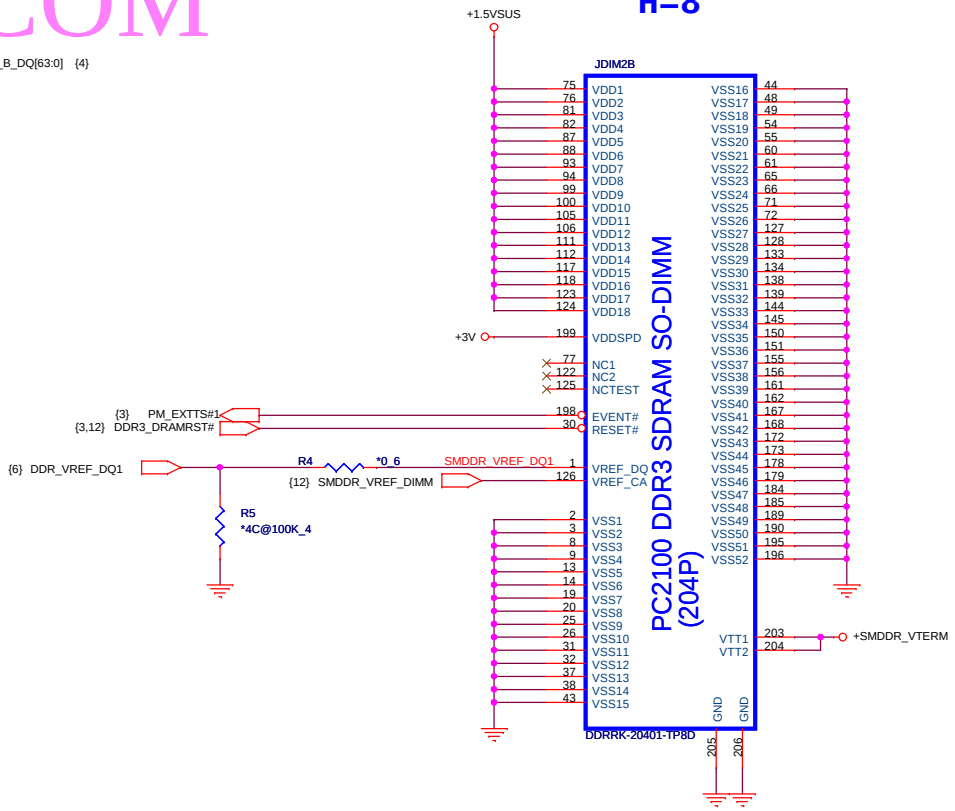
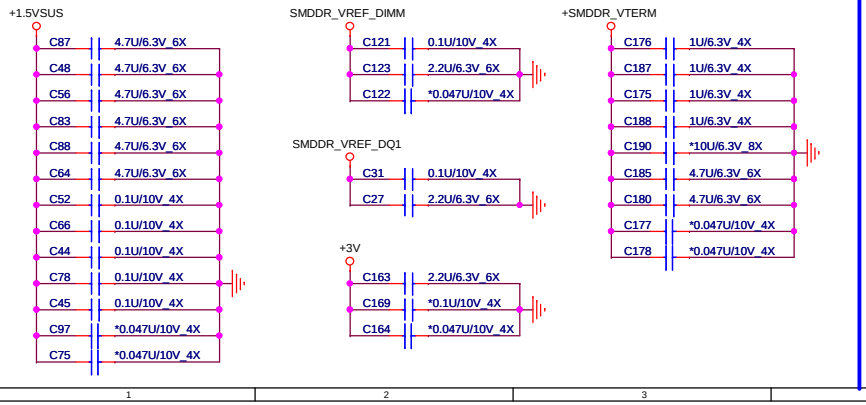
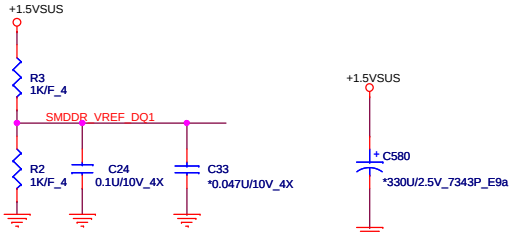


Place these Caps near So-Dimm1.





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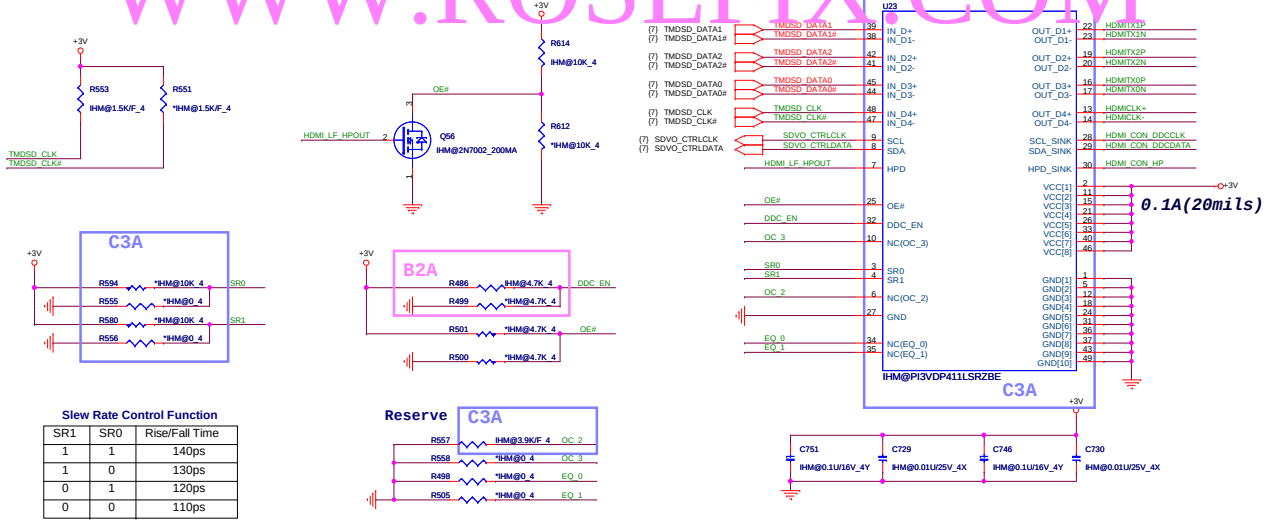
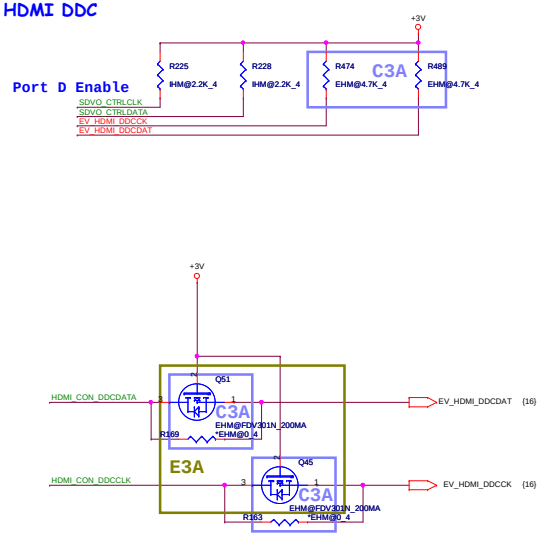
HDMI Level Shift



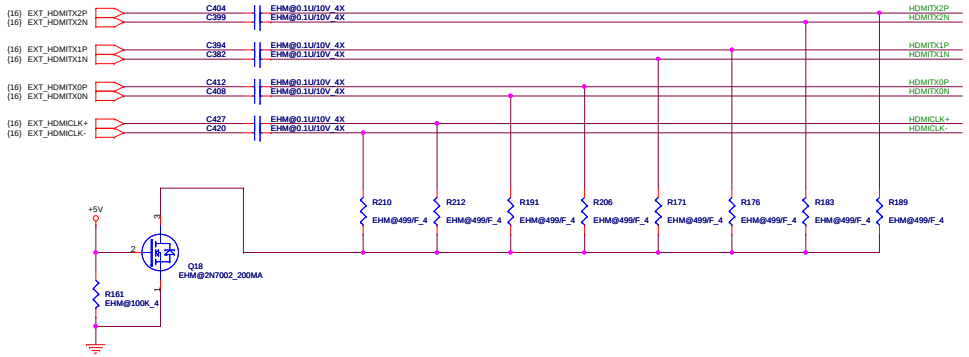
Slew Rate Control Function

SR1	SR0	Rise/Fall Time
1	1	140ps
1	0	130ps
0	1	120ps
0	0	110ps

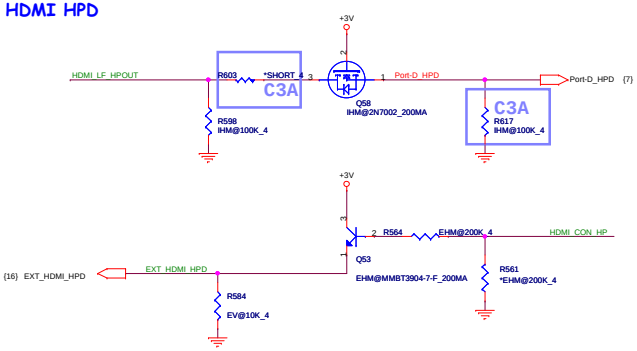
HDMI DDC



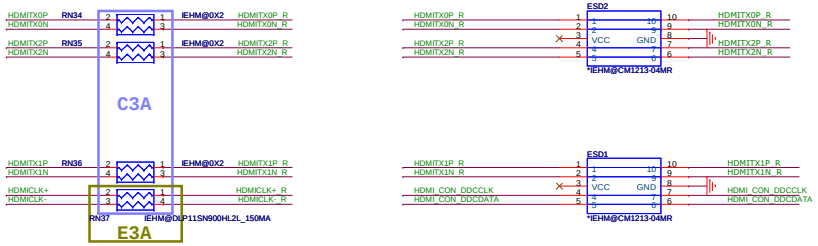
Discrete HDMI

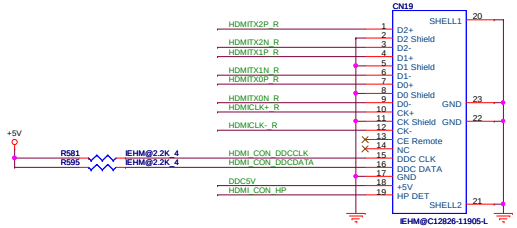


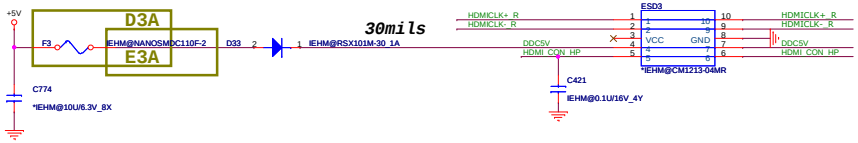
HDMI HPD



Close to HDMI CONN







Quanta Computer Inc.			
PROJECT : BL6			
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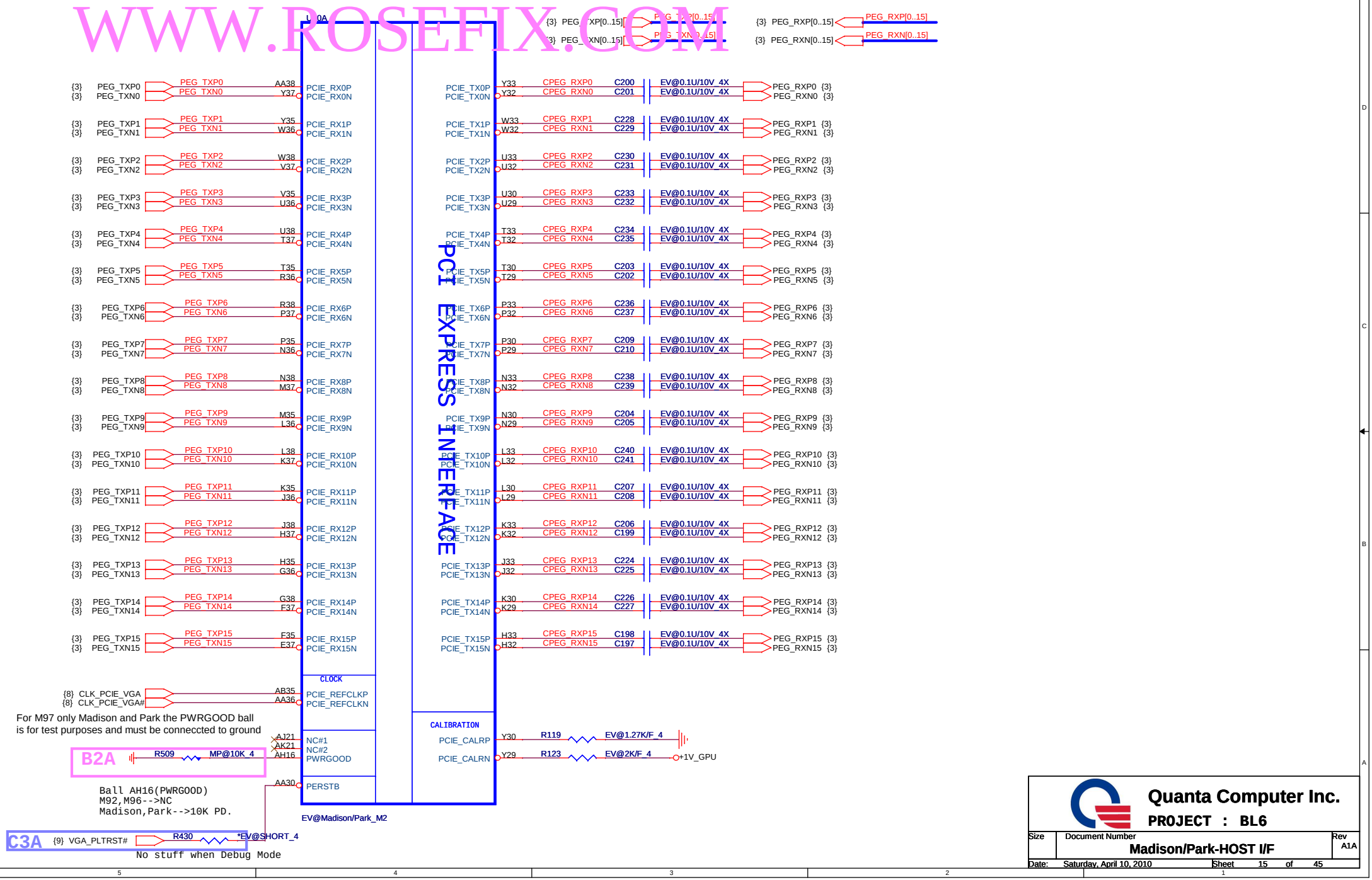

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	Madison/Park-HOST I/F	A1A
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B2A

JTAG SIGNAL STUFF OPTION FOR OPTION2

SIGNALS	NORMAL MODE	JTAG MODE (DEBU
TESTEN	"1" (PU)	"1" (PU)
GPIO24_TRSTB	"0" (PD)	"1" (PU)
GPIO26_TCK	CLK	"1" (PU)
GPIO27_TMS	"1" (PU)	"1" (PU)

1.8V GPIO

B2A
NC on Park
M92,M96,Madison support

B2A
NC on Park
M92,M96,Madison support

SCL must be tied high if not used

B2A
Park Channel D-->No support
M92 Channel C&D-->No support

HDMI

LVDS

EV@Madison/Park_M2

TjMax = 110
change by VBIOS

B2A
M92,M96 GPIO_21 pin control BB function.Park,Madison no suport.

B2A
M96,Madison-->support
Ball AH26-->HPD5
Ball AH24-->HPD6
M92,Park-->No support

JTAG need Option2 for Park,Madison Engineer sample

Place close to Chip

+1.8V(20mA)

5mA (5mils)

B2A
Madison,Park-->125mA (10mils)
M92,M96-->300mA(20mils)

(3.3V@130mA A2VDD)

(1.8V@70mA AVDD)

(1.8V@45mA VDD1DI/ 50mA VFF2D)

(1.8V@1.5mA A2VDDQ)

B2A
Port 3
M96,Madison,Park-->support
M92-->No support
Port 4
M96,Madison-->support
M92,Park-->No support

B2A
Port7
Madison-->support
M92,M96,Park-->No support

Quanta Computer Inc.
PROJECT : BL6

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	Madison/Park-HOST I/F	A1A

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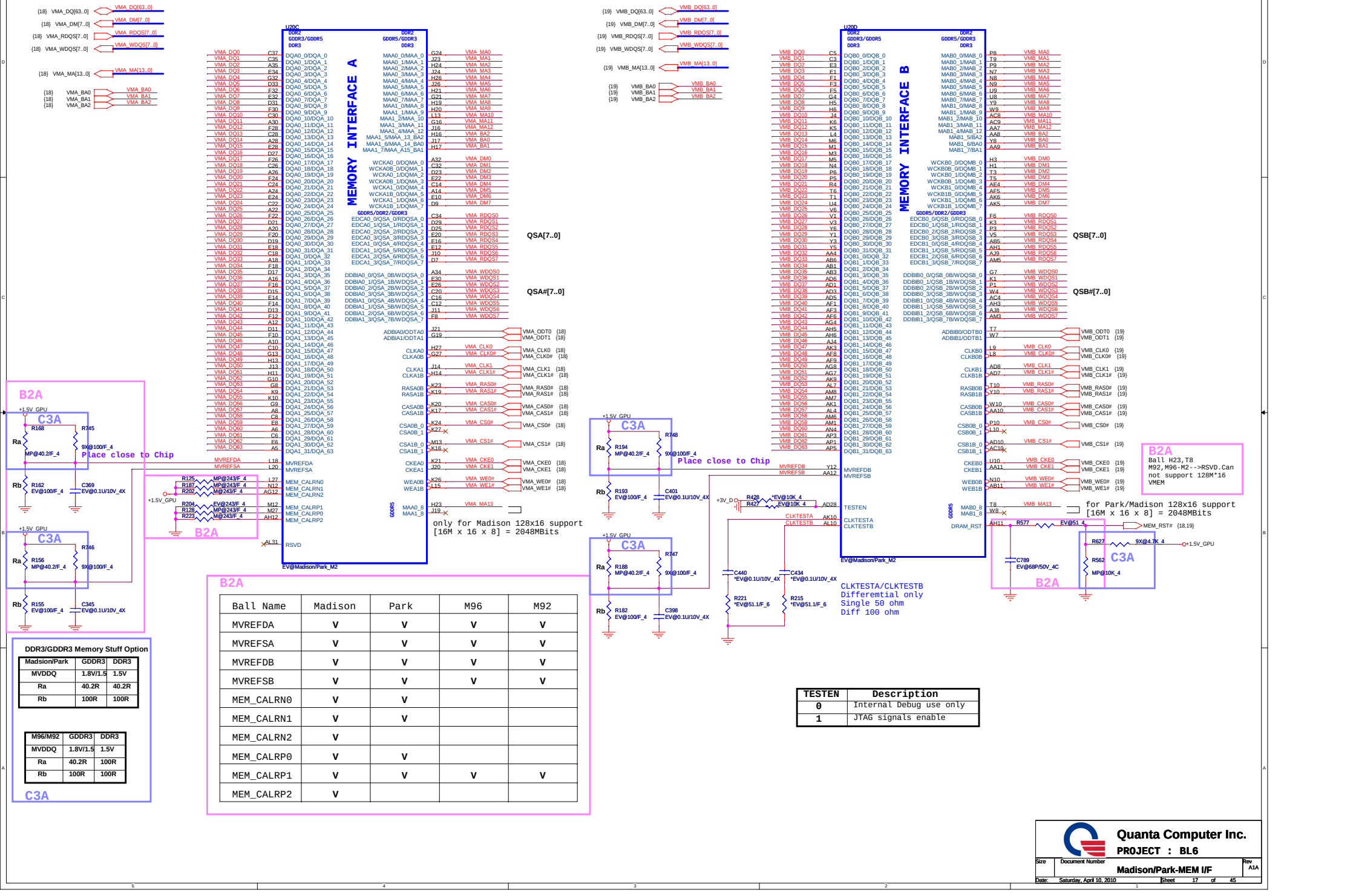


DDR3/GDDR3 Memory Stuff Option

Madsion/Park	GDDR3	DDR3
MVDDQ	1.8V/1.5	1.5V
Ra	40.2R	40.2R
Rb	100R	100R

M96/M92	GDDR3	DDR3
MVDDQ	1.8V/1.5	1.5V
Ra	40.2R	100R
Rb	100R	100R

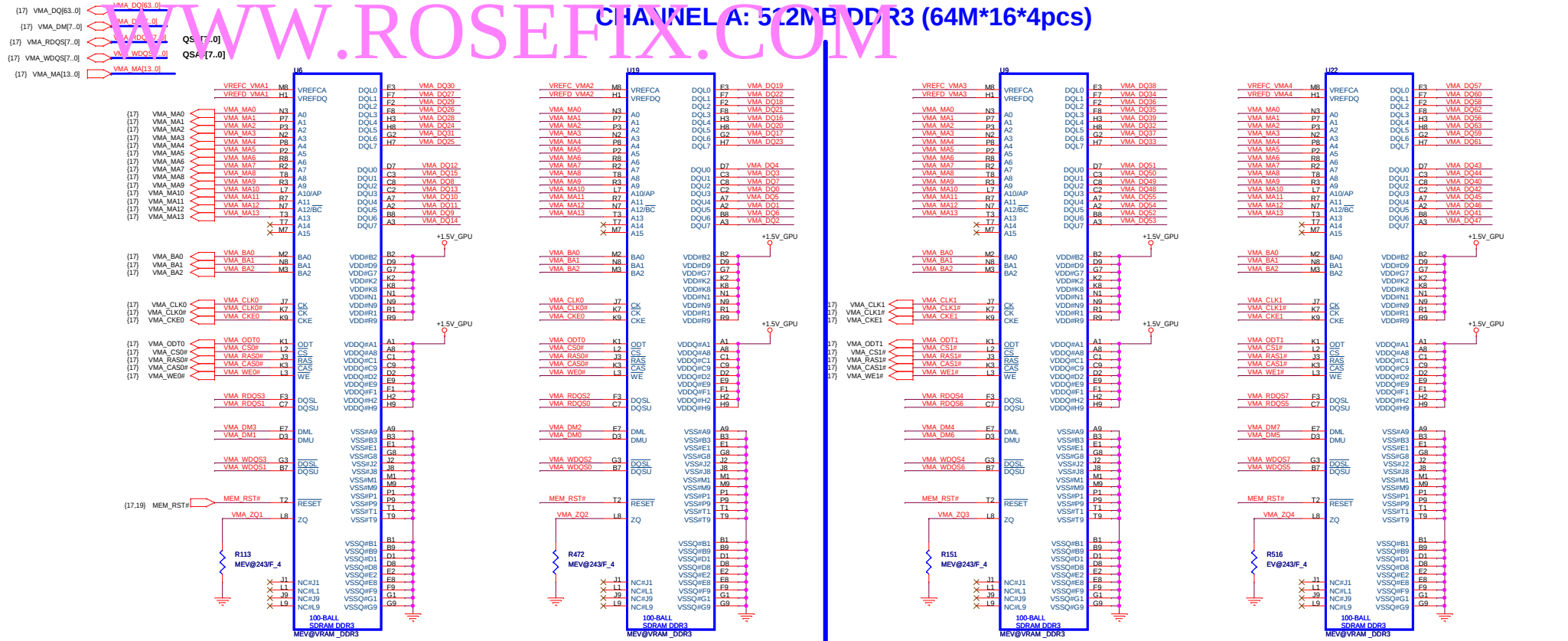
C3A

Ball Name	Madison	Park	M96	M92
MVREFDA	V	V	V	V
MVREFSA	V	V	V	V
MVREFDB	V	V	V	V
MVREFSB	V	V	V	V
MEM_CALRN0	V	V		
MEM_CALRN1	V	V		
MEM_CALRN2	V			
MEM_CALRP0	V	V		
MEM_CALRP1	V	V	V	V
MEM_CALRP2	V			

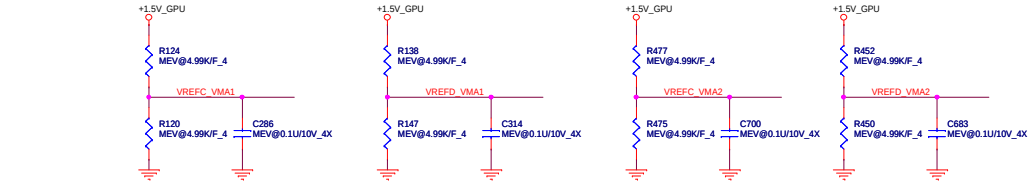
TESTEN	Description
0	Internal Debug use only
1	JTAG signals enable

Quanta Computer Inc.				
PROJECT : BL6				
Size	Document Number	Madison/Park-MEM I/F		Rev A1A
Date: Saturday, April 10, 2010		Sheet 17 of 45		

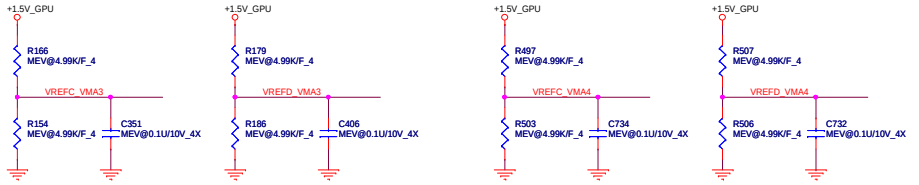
CHANNEL A: 512MB DDR3 (64M*16*4pcs)



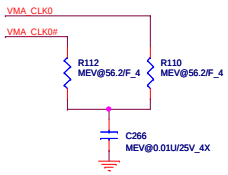
Group-A0 VREF



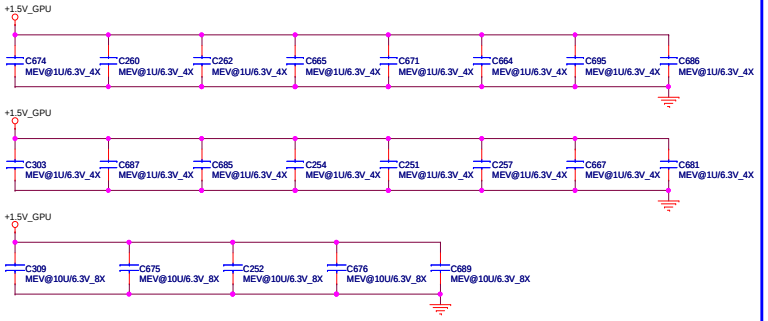
Group-A1 VREF



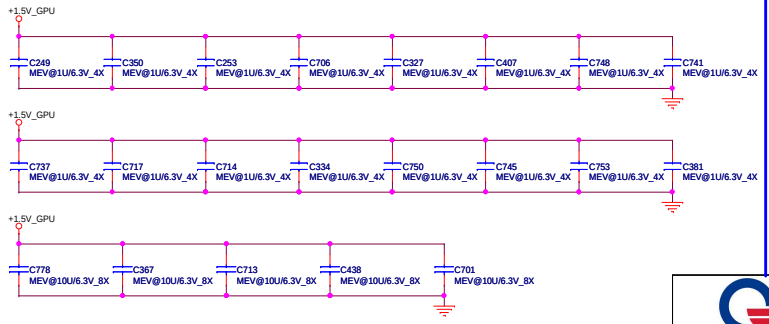
MEM_A0 CLK



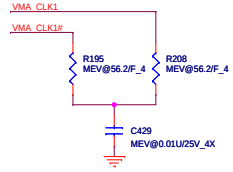
Group-A0 decoupling CAP



Group-A1 decoupling CAP



MEM_A1 CLK



Quanta Computer Inc.
PROJECT : BL6

Size	Document Number	Rev
	VRAM_A: DDR3-64M*16*4PCS	A1A
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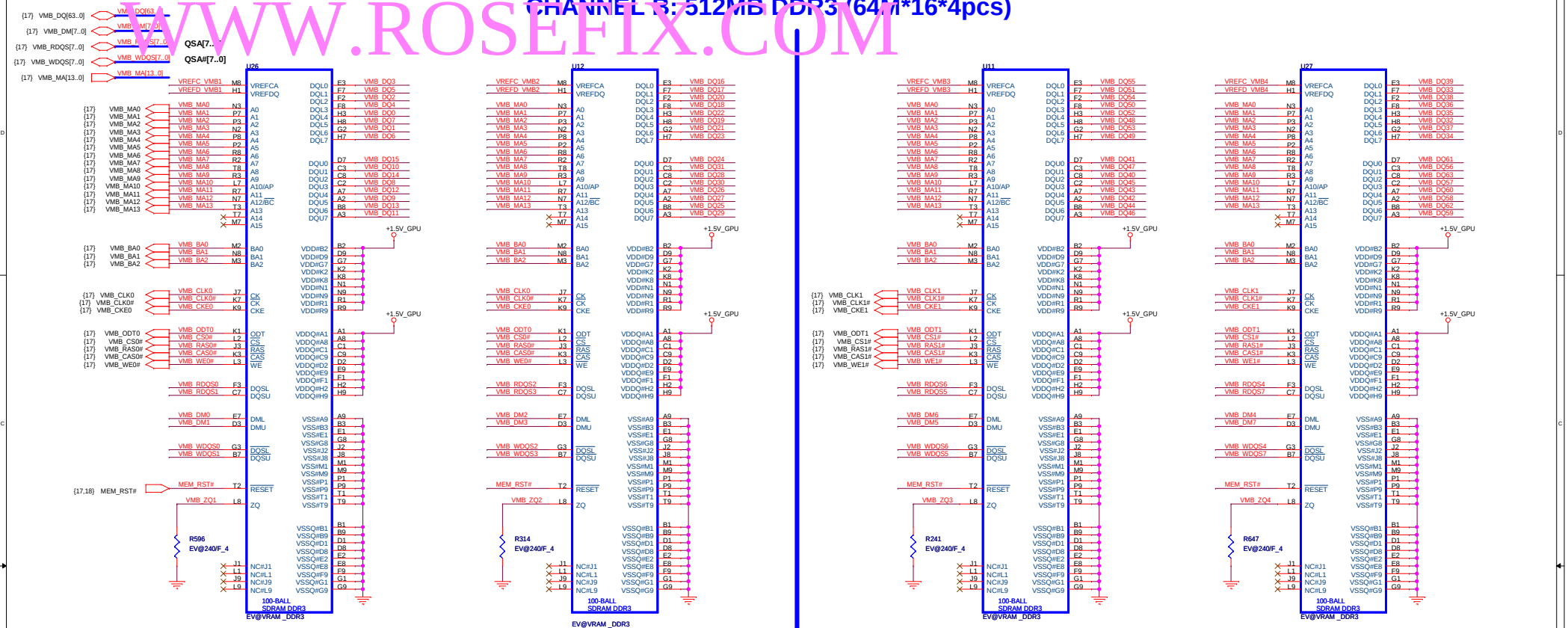
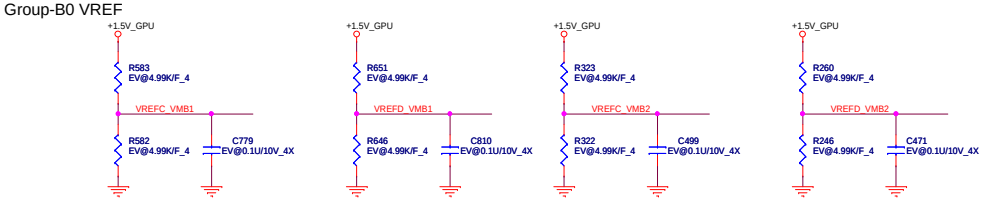
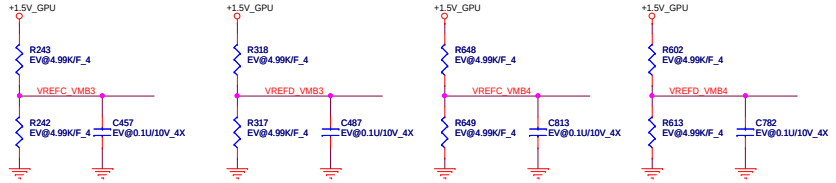
CHANNEL B: 512MB DDR3 (64M*16*4pcs)



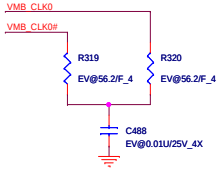
Group-B0 VREF



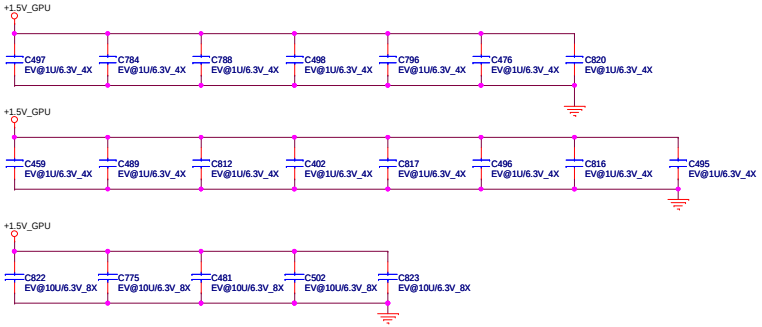
Group-B1 VREF



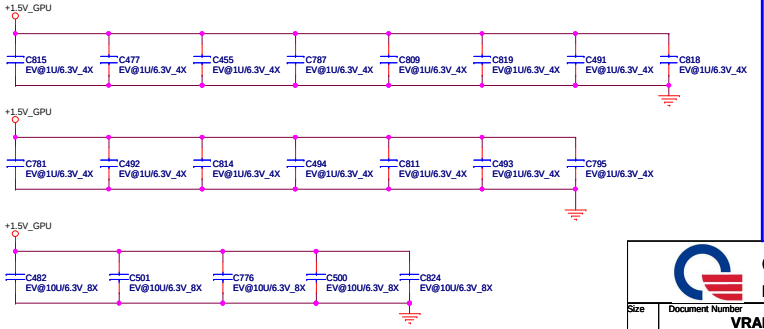
MEM_B0 CLK



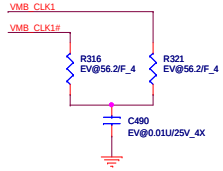
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK



Quanta Computer Inc.
PROJECT : BL6

Size	Document Number	Rev
	VRAM_B: DDR3-64M*16*4PCS	A1A
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For Madison and Park VDDCI and VDDC can share one common regulator

VDD/VDDQ =1.5V at 1333
VDD/VDDQ =1.8V at 1600 and 1800

(1.5V@3.4A_VDDR1)

(1.8V@17mA VDD_CT)

(3.3V@60mA)

(1.8V@170mA)

(1.8V@40mA PCIE_PVDD)

(1.8V@150mA MPV18)

(1.8V@50mA SPV18)

(1.0V@100mA SPV10)

(1.8V@40mA PCIE_VDDR)

(1.0V@2A PCIE_VDDC)

(30A or more)

(DDR3 1.12V@4A VDDCI) or more

VDDCI:33.6A

GPU +3V power
0.5A

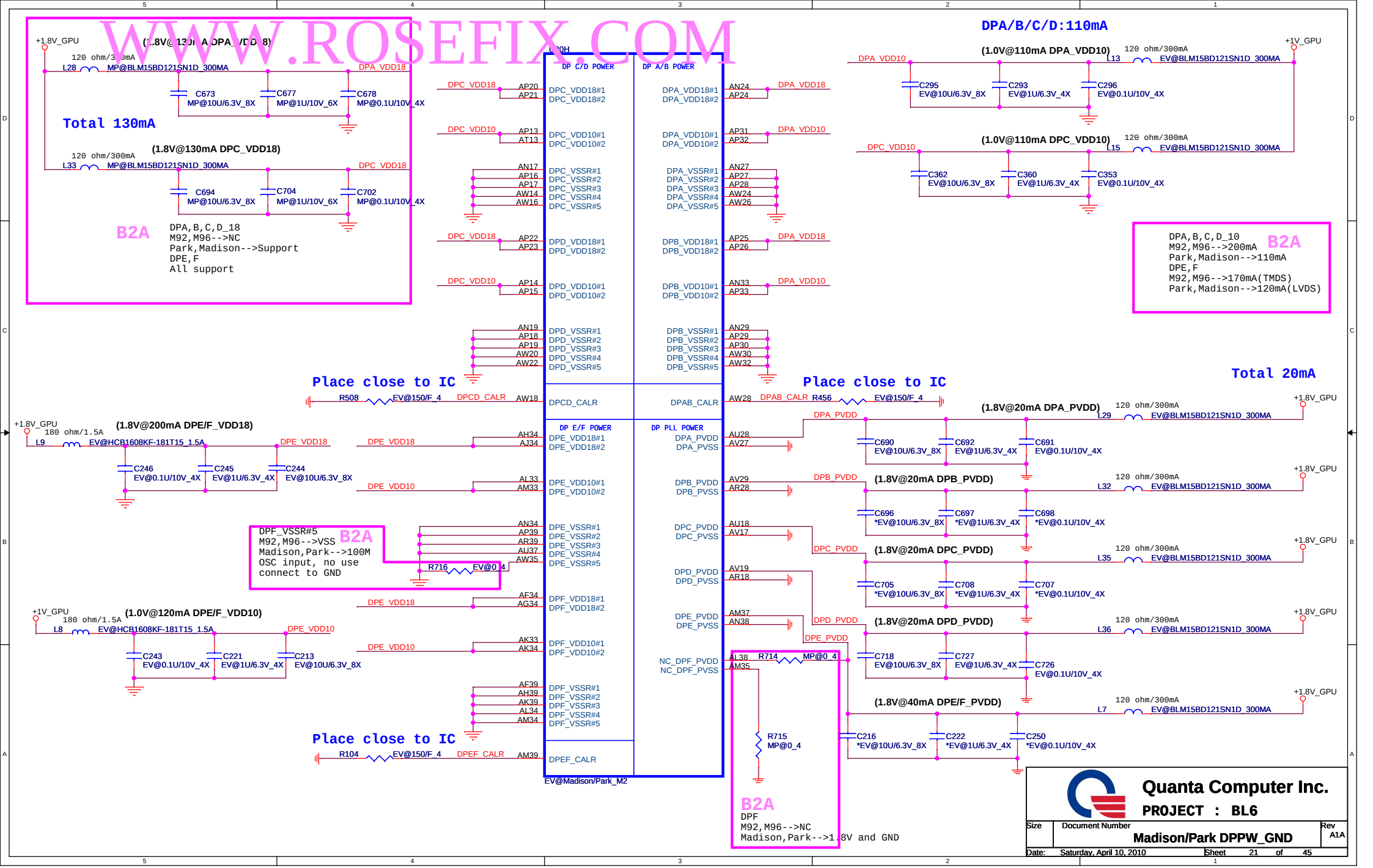
GND

POWER

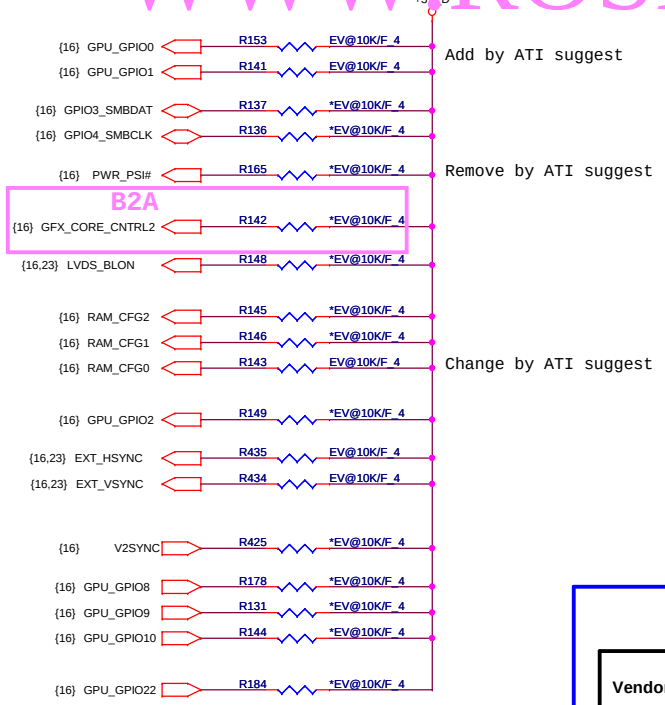
Route as differential Pair

	M92	M96	Park	Madison
VDDRHA	NC	VDDR1	NC	NC
VDDRHB	VDDR1	VDDR1	NC	NC
VSSRHA	NC	VSS	NC	NC
VSSRHB	VSS	VSS	NC	NC

Quanta Computer Inc.
PROJECT : BL6
Madison/Park PWR_GND
Size: Document Number: Rev: A1A
Date: Saturday, April 10, 2010 Sheet 20 of 45



PIN STRAPS



Memory Aperture size	
RAM_CFG[2:0]	Size
000	128MB
001	256MB
010	64MB
011	32MB

ROM Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

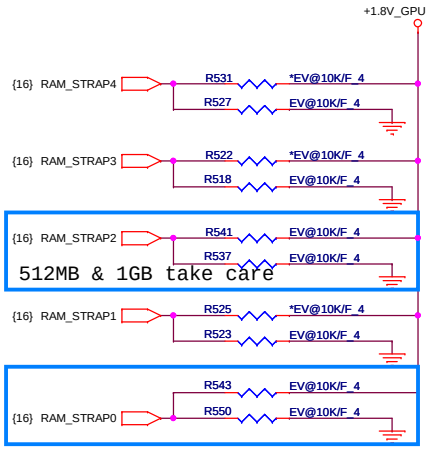
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

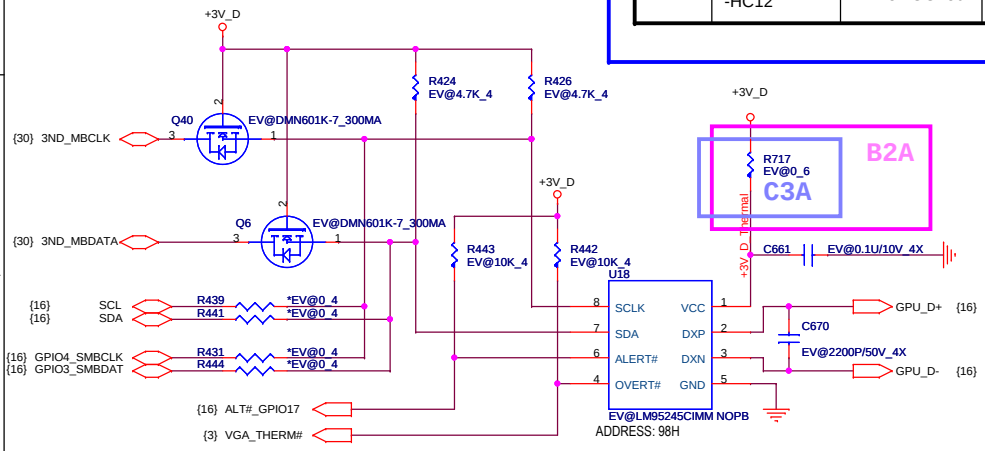
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM (Only for GDDR5) 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA VIP: Video Capture Port Interface	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

DDR3 Memory TYPE

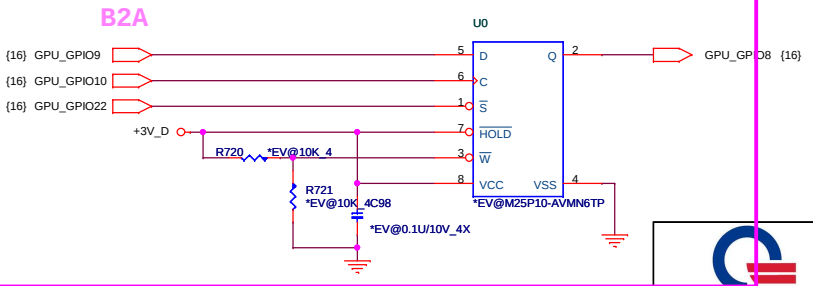
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3 DVPDATA_3	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0	RAM_STRAP4 15"	RAM_STRAP4 14"
Hynix	H5TQ1G63BFR -12C	AKD5LZGTW00 (64M*16)	512MB	0	1	0	0	0	1
			1GB	0	0	0	0	0	1
			2GB	0	0	1	0	0	1
Samsung	K4W1G1646E -HC12	AKD5LGGT502 (64M*16)	512MB	0	1	0	1	0	1
			1GB	0	0	0	1	0	1
	K4W2G1646B -HC12	AKD5MGGT501	2GB	0	0	1	1	0	1



Thermal Sensor



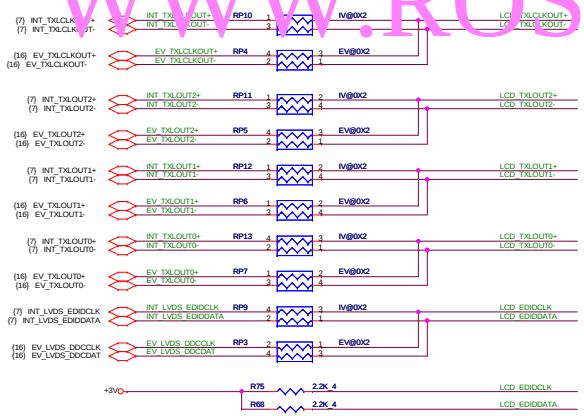
EEPROM



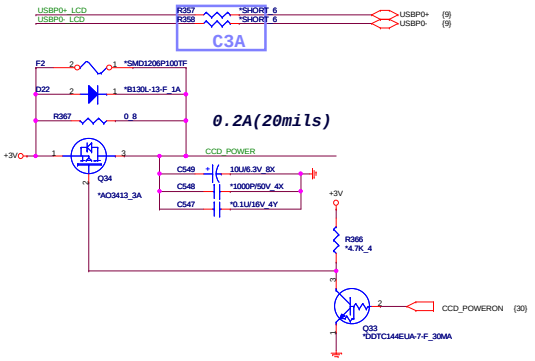
Quanta Computer Inc.
PROJECT : BL6

Size	Document Number	Rev
	Memory strip/Thermal/HDCP	A1A
Date: Saturday, April 10, 2010	Sheet 22 of 45	

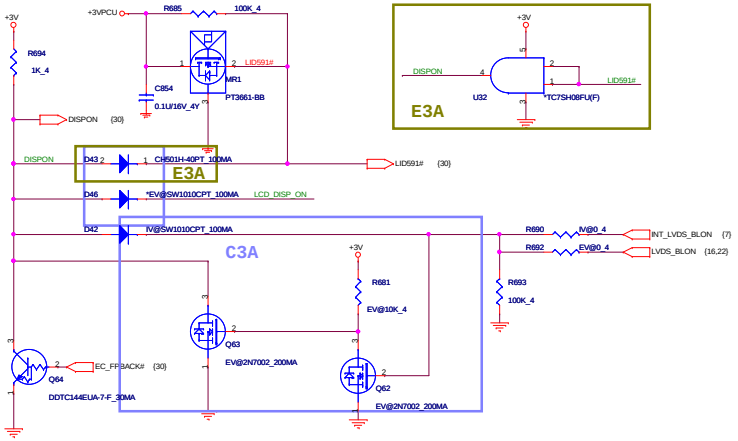
LVDS Signals



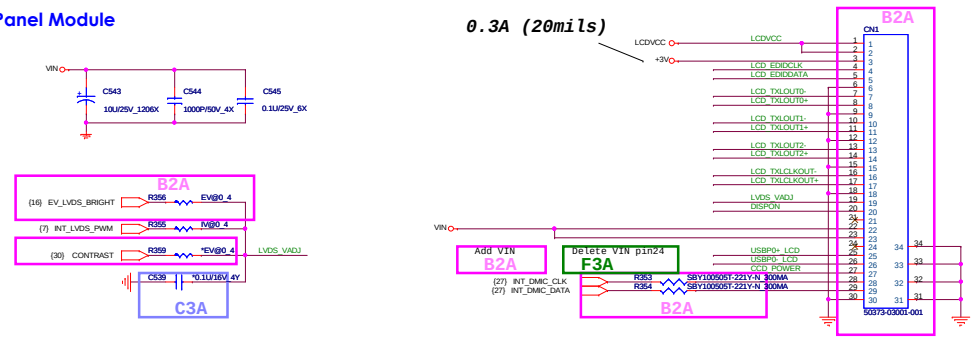
CCD



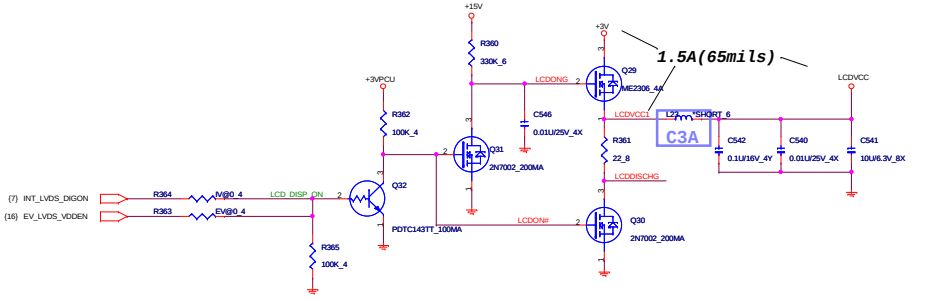
HALL SENSOR&BACK LIGHT SWITCH



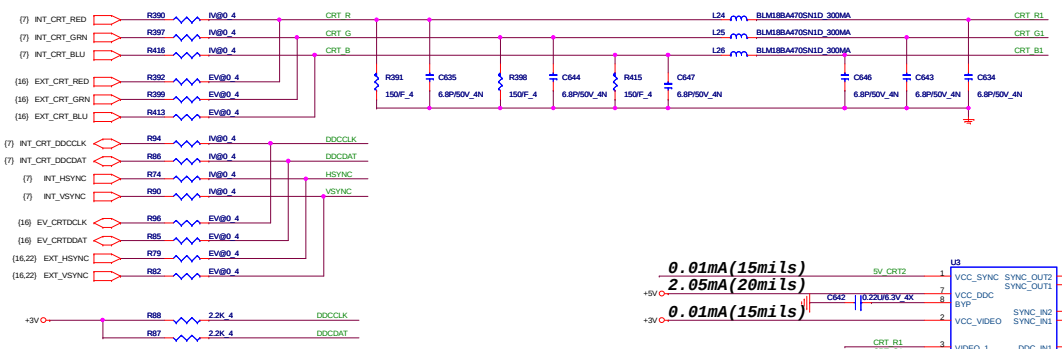
LCD Panel Module

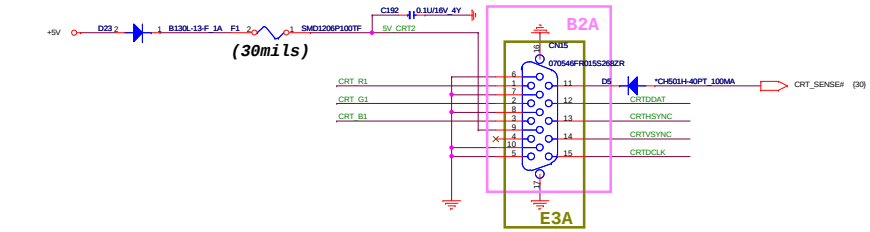


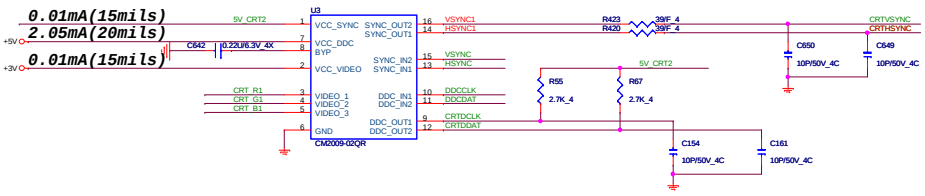
LCD POWER SWITCH



CRT







Quanta Computer Inc.		
PROJECT : BL6		
Size	Document Number: LCD/LED Panel/CCD	Rev: XLA
Date: Saturday, April 10, 2010	Sheet 23 of 45	

MINI Card Slot#1 (WiFi)

Before RAMP must to remove debug card component

2.75A(120mils)

0.33A(30mils)

Intel module use S5 power for +3.3V
Other module keep +3V for +3.3V

MINI Card Slot#2 3G

2.75A(120mils)

0.5A(30mils)

SIM CARD board to board

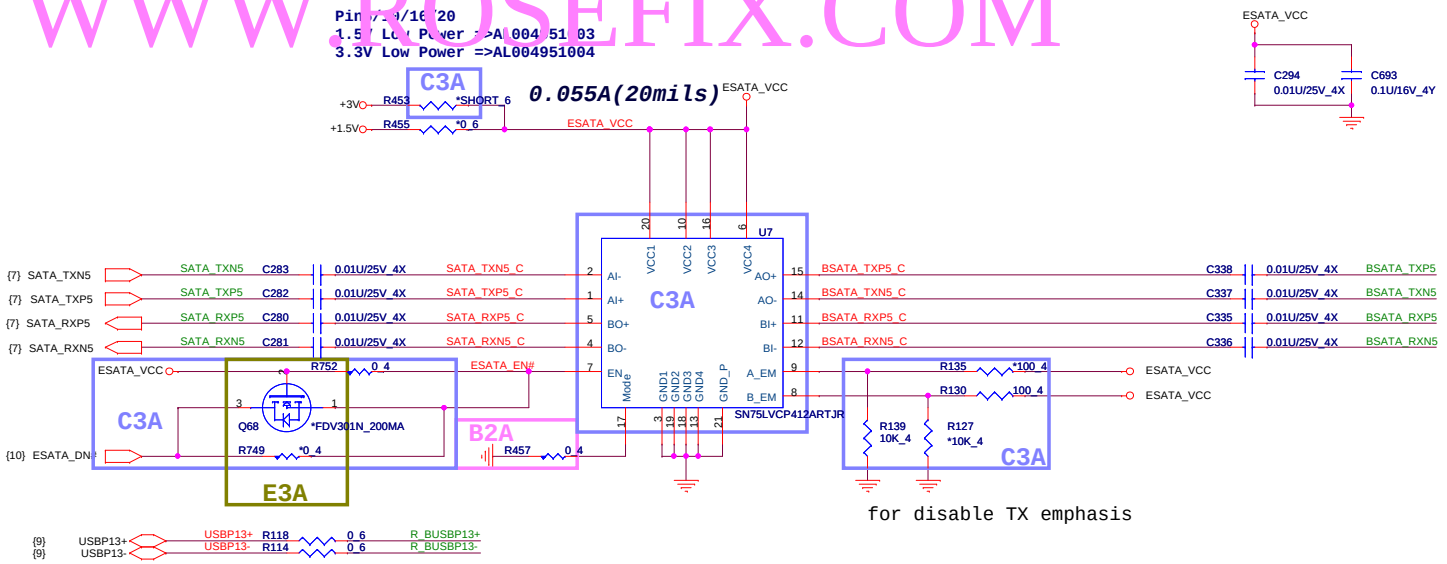
3G CONN

Close to 3G MINI Card

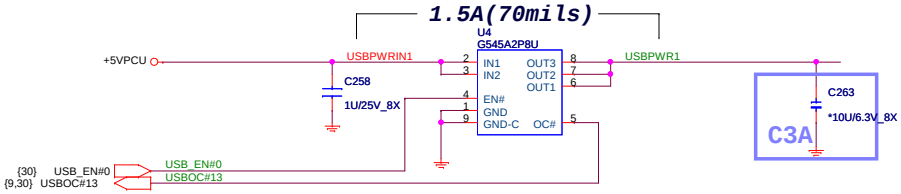
Quanta Computer Inc.	
PROJECT : BL6	
Size	Document Number: MINI CARD(WLAN/3G/SIM Card) — Rev A1A
Date: Saturday, April 10, 2010	Sheet 24 of 45

ESATA Re-driver IC

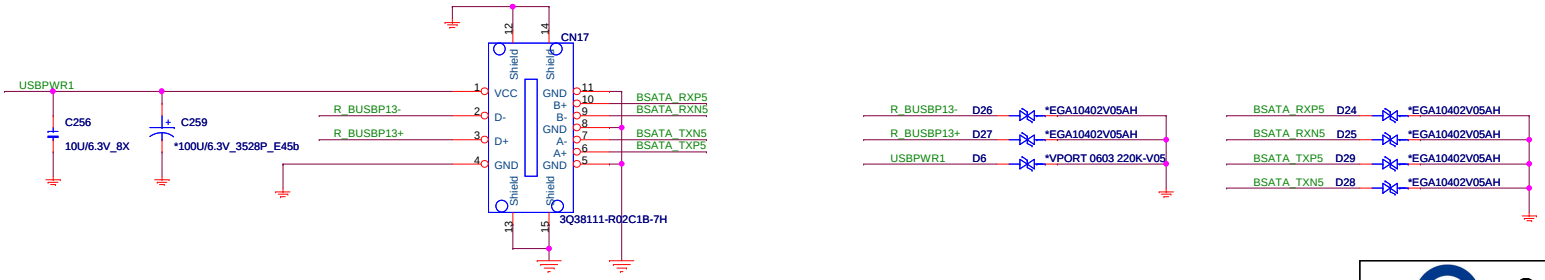
Pin 7/9/16/20
1.5V Low Power =>AL004951003
3.3V Low Power =>AL004951004



for disable TX emphasis



ESATA CONN



Quanta Computer Inc.
PROJECT : BL6

Size	Document Number	Rev
	TP/SW/ESATA/USB+Audio/LED	A1A
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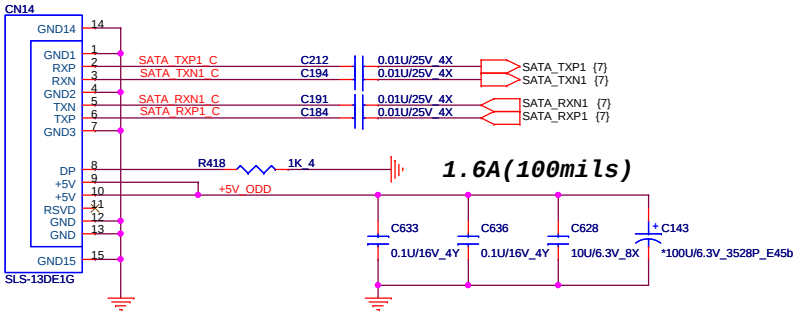
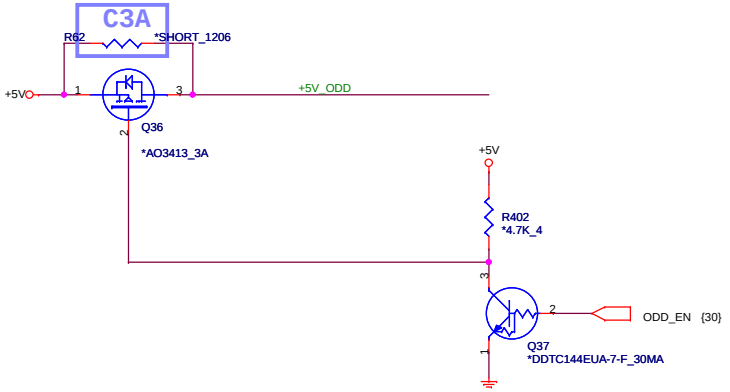
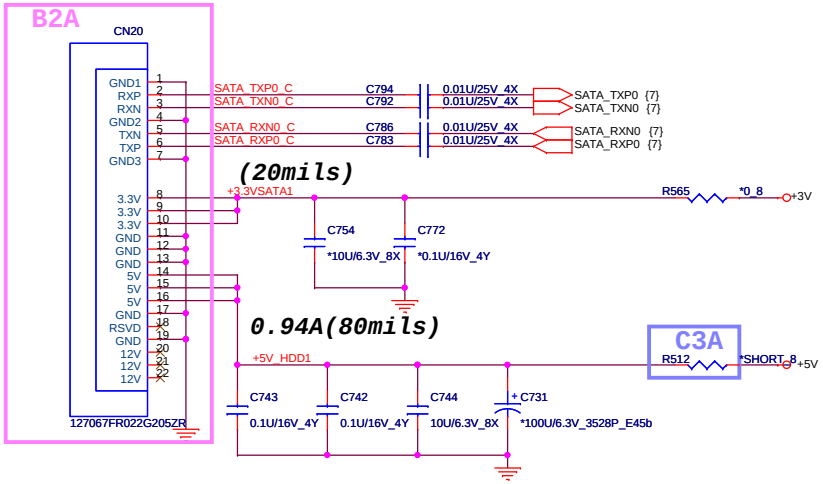
SATA ODD

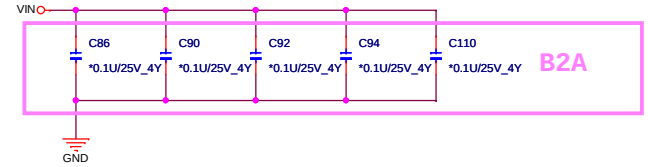


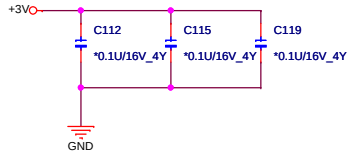


SATA HDD



EMI

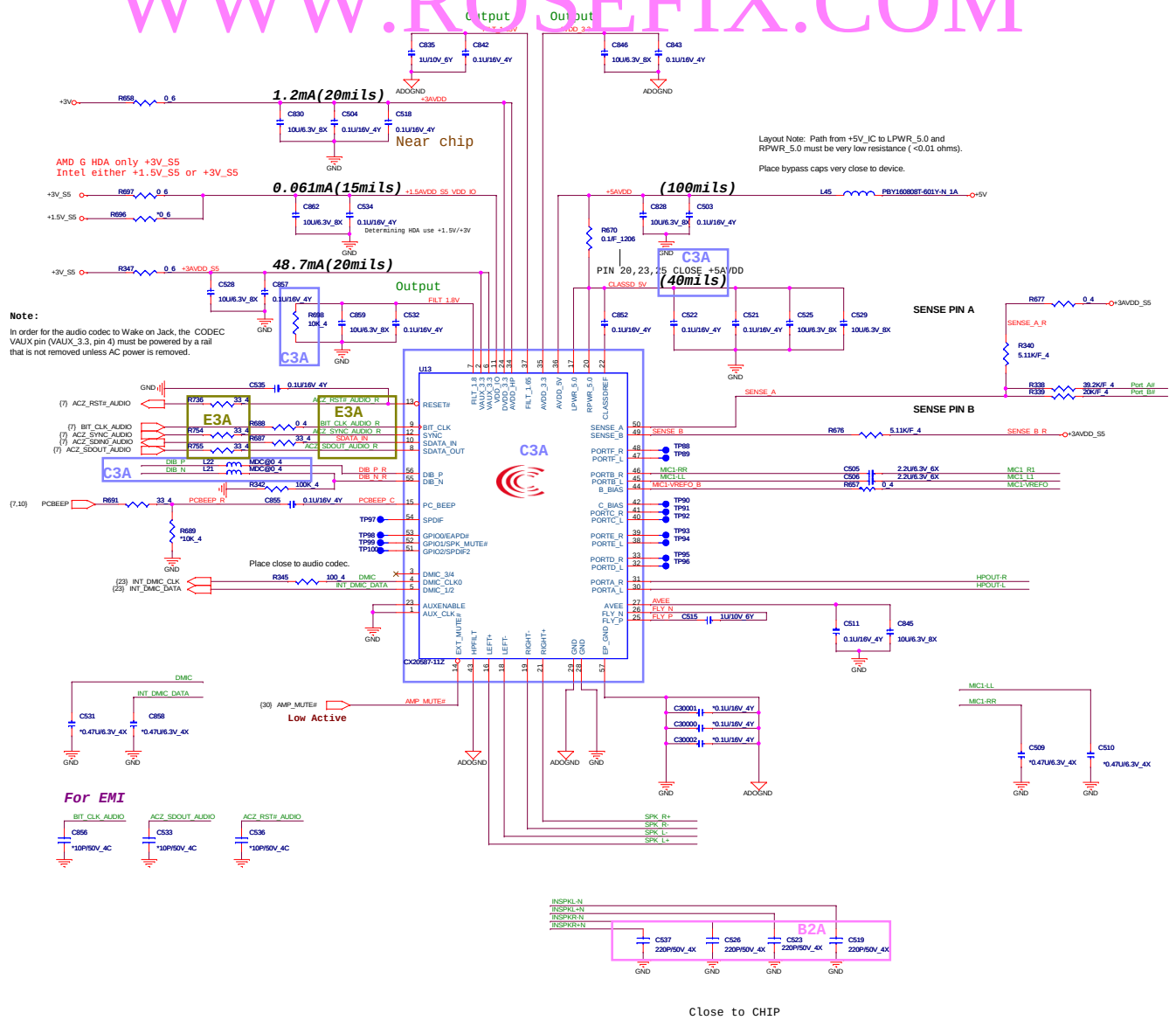




Quanta Computer Inc.
PROJECT : BL6

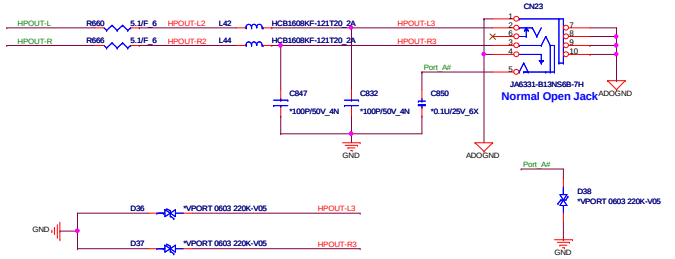
Size	Document Number	Rev
	HDD/ODD/EMI	A1A
Date: Saturday, April 10, 2010	Sheet 26 of 45	

Codec (CX20583)

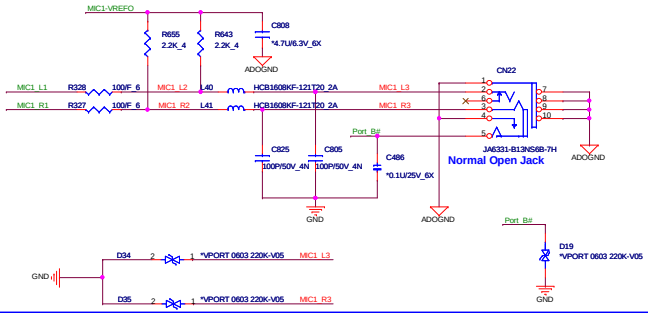


AUDIO JACKS

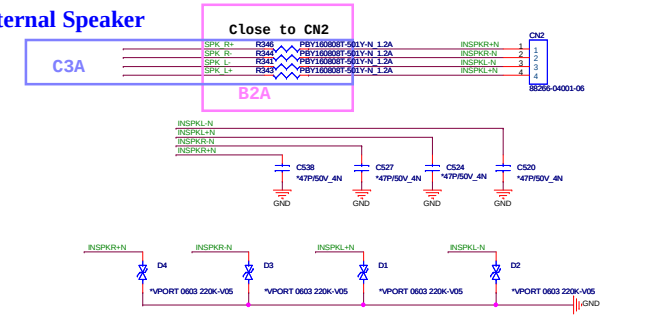
Earphone



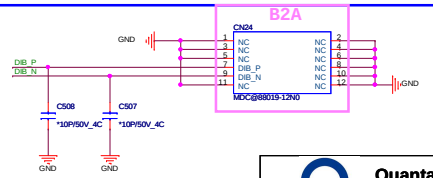
External MIC



Internal Speaker

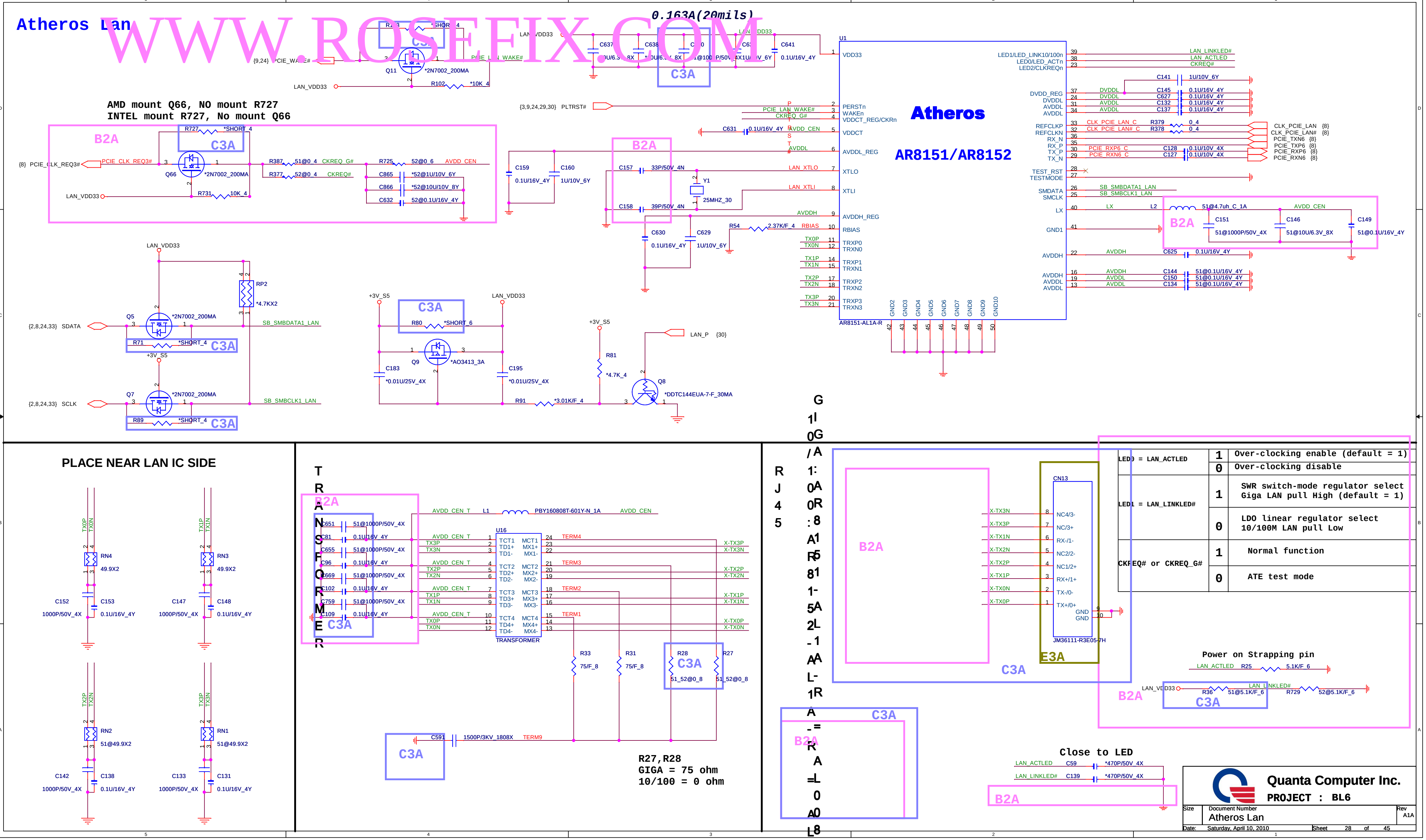


MDC



Quanta Computer Inc.			
PROJECT : BL6			
Size	Document Number		Rev
	Audio Codec (CX20583)		A1A
Date: Saturday, April 10, 2010		Sheet 27 of 45	

Atheros Lan



LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G#	1	Normal function
	0	ATE test mode

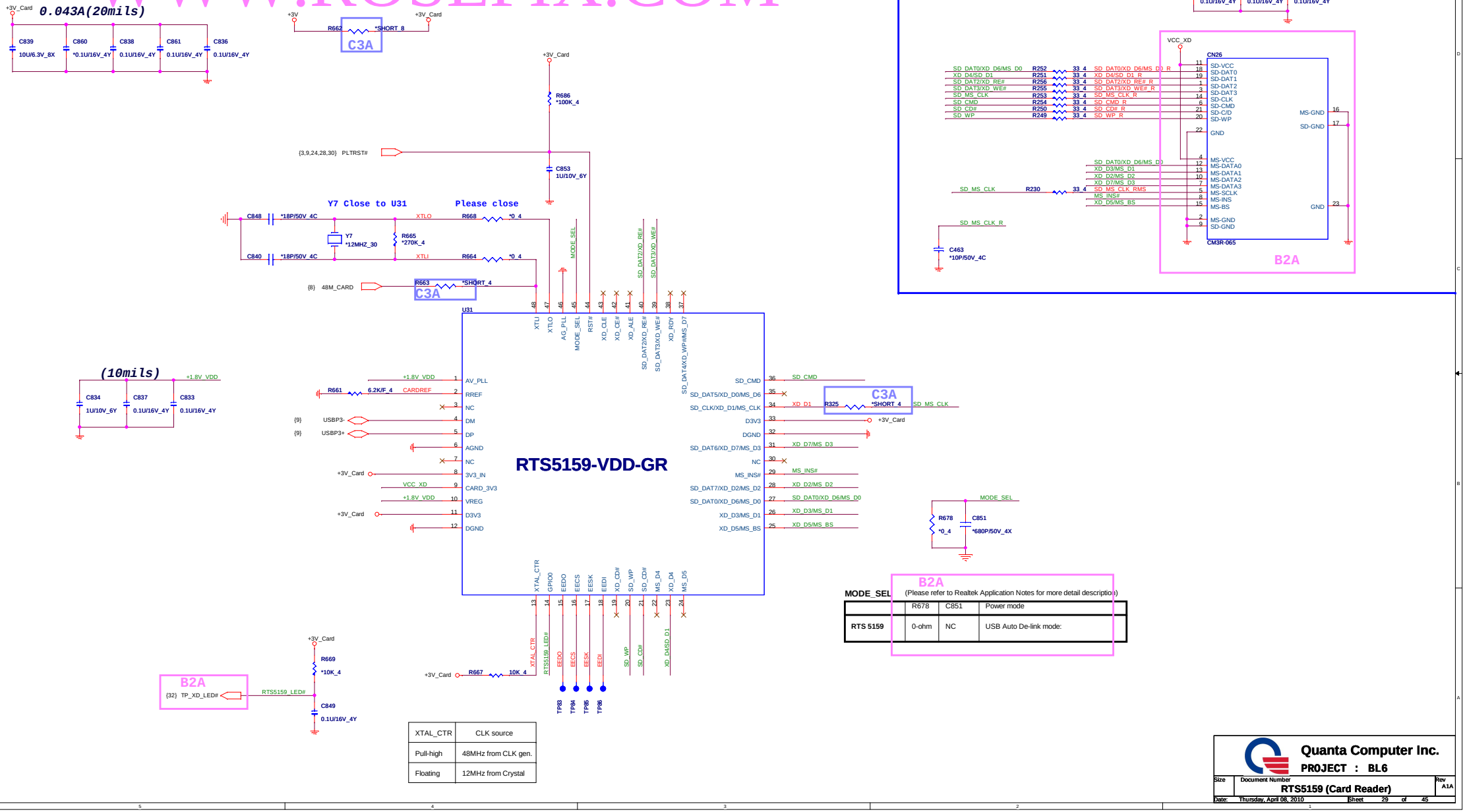
Quanta Computer Inc.

PROJECT : BL6

Size | Document Number: Atheros Lan | Rev: A1A

Date: Saturday, April 10, 2010 | Sheet 28 of 45

5 IN 1 CARD READER

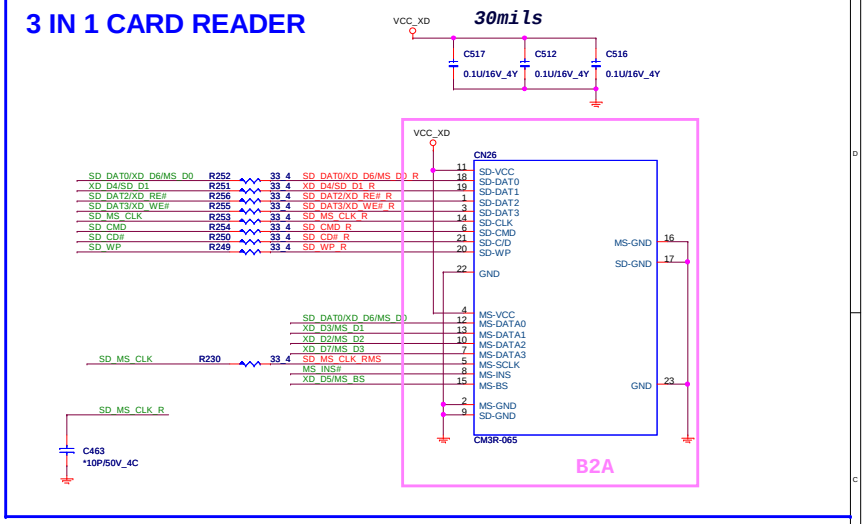


MODE_SEL (Please refer to Realtek Application Notes for more detail description)

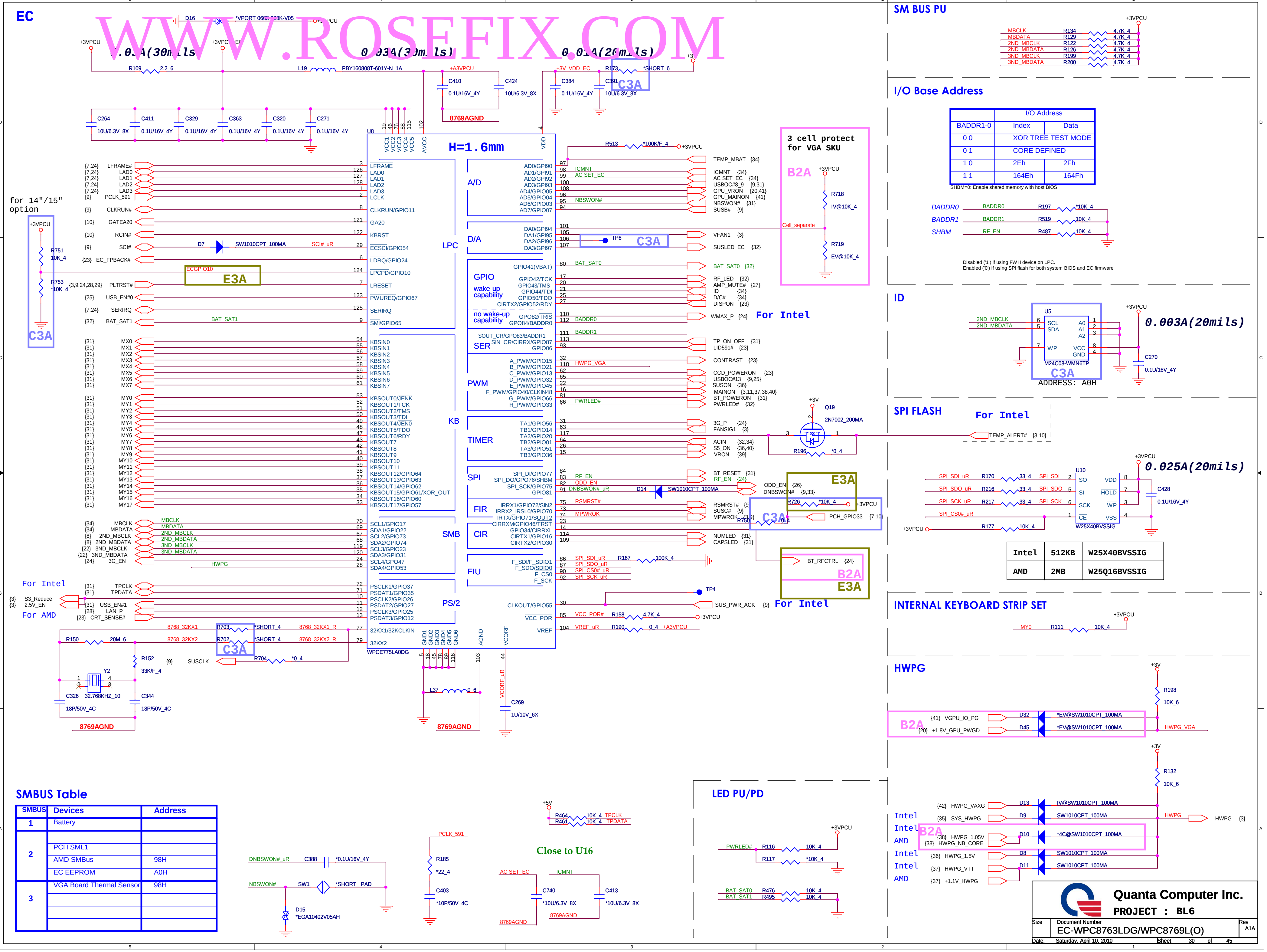
	R678	C851	Power mode
RTS 5159	0-ohm	NC	USB Auto De-link mode:

XTAL_CTR	CLK source
Pull-high	48MHz from CLK gen.
Floating	12MHz from Crystal

3 IN 1 CARD READER



Quanta Computer Inc.
PROJECT : BL6
Size | Document Number: RTS5159 (Card Reader) | Rev A1A
Date: Thursday, April 08, 2010 | Sheet 29 of 45



I/O Base Address

BADDR1-0	I/O Address Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SPI FLASH

Intel	512KB	W25X40BVSSIG
AMD	2MB	W25Q16BVSSIG

SMBUS Table

SMBUS	Devices	Address
1	Battery	
2	PCH SML1	
	AMD SMBus	98H
	EC EEPROM	A0H
3	VGA Board Thermal Sensor	98H

Quanta Computer Inc.
PROJECT : BL6

Document Number: EC-WPC8763LDG/WPC8769L(O)
Rev: A1A
Date: Saturday, April 10, 2010
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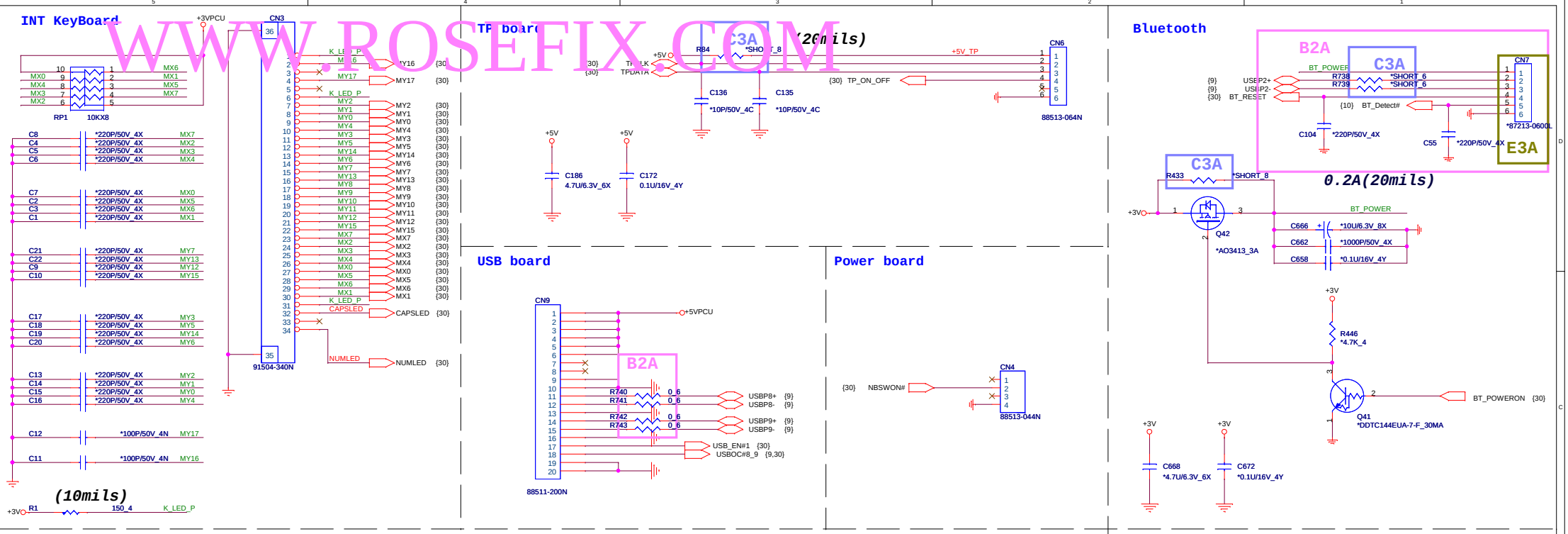
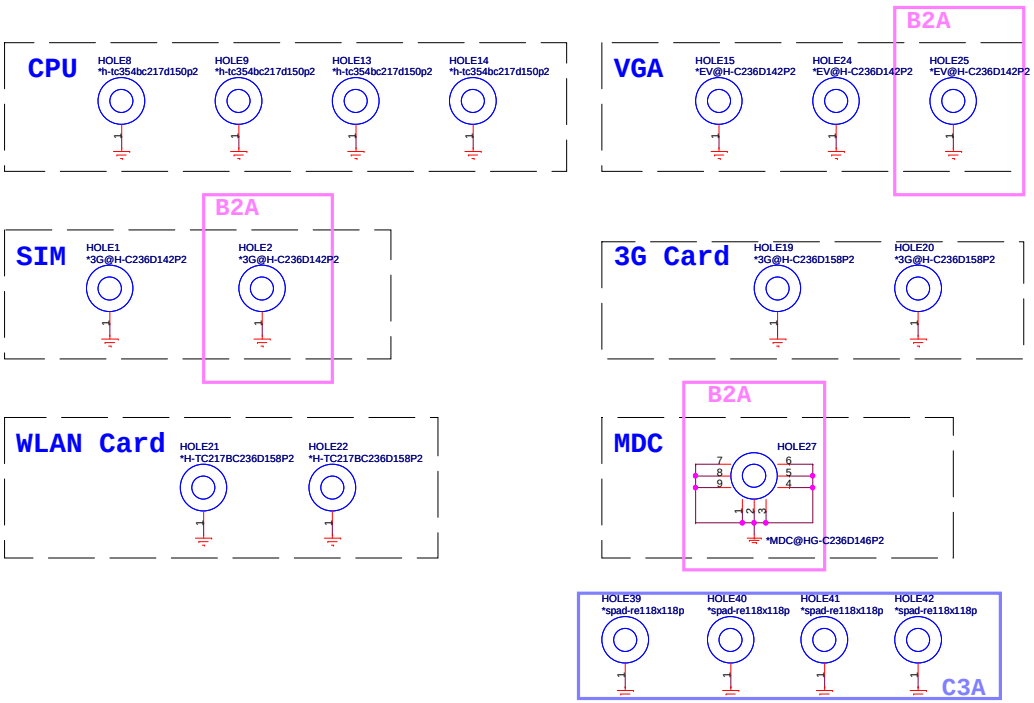
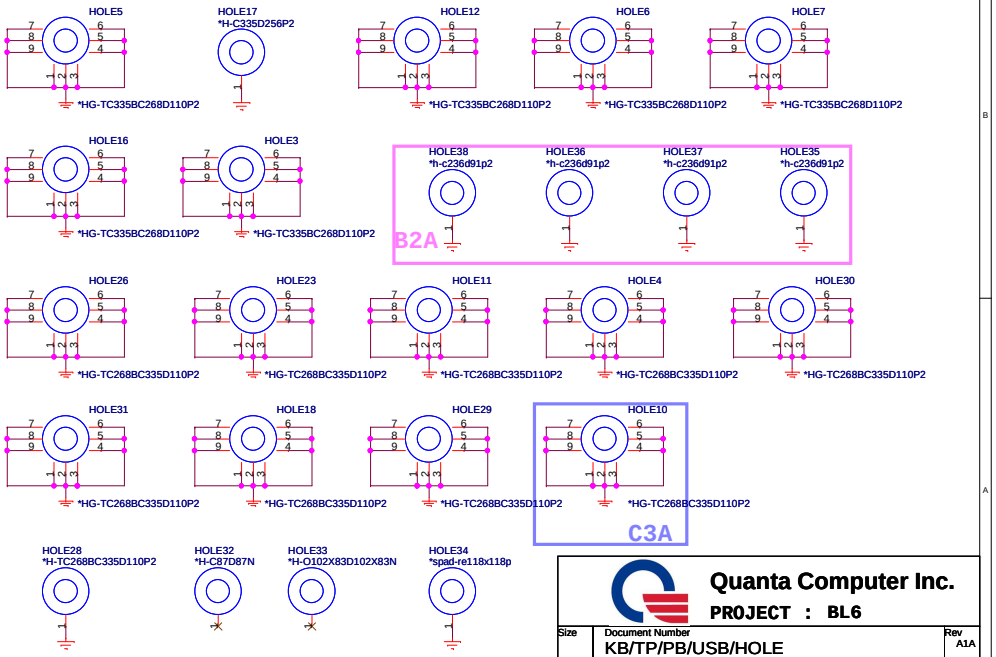


NUT



HOLE



Quanta Computer Inc.
PROJECT : BL6

Size	Document Number	Rev
	KB/TP/PB/USB/HOLE	A1A
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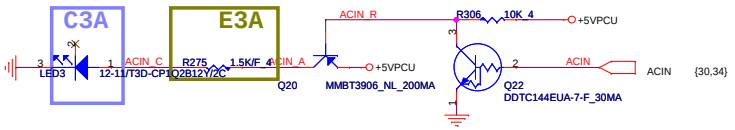
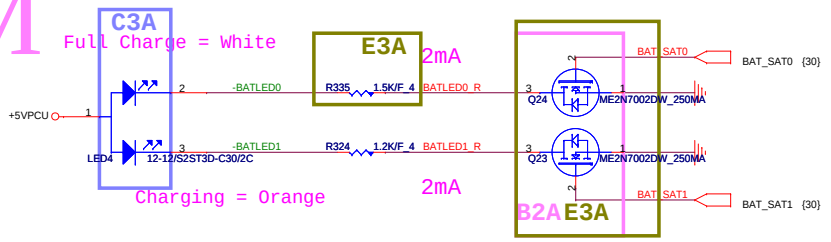
LED

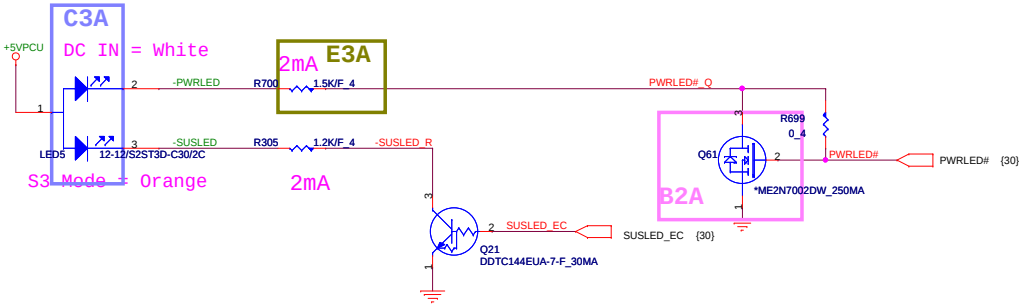
AC-IN



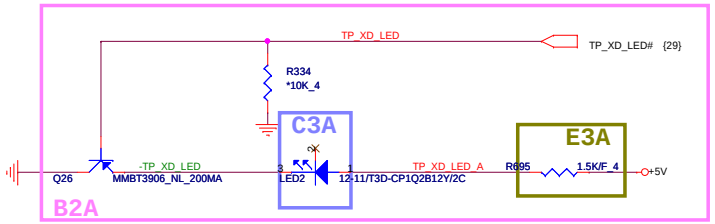
BATTERY



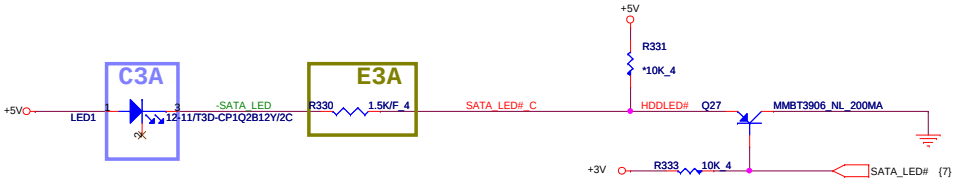
POWER



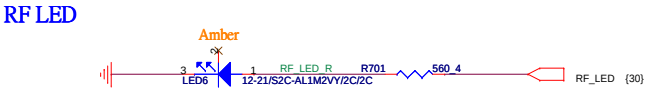
CARDREADER



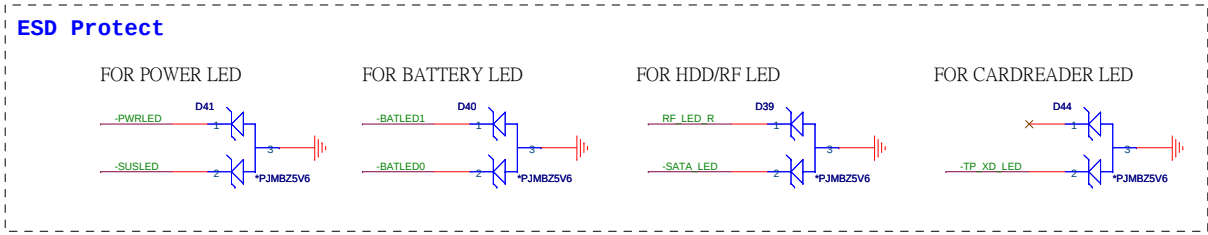
HDD/ODD



RF LED



ESD Protect



Quanta Computer Inc.		
PROJECT : BL6		
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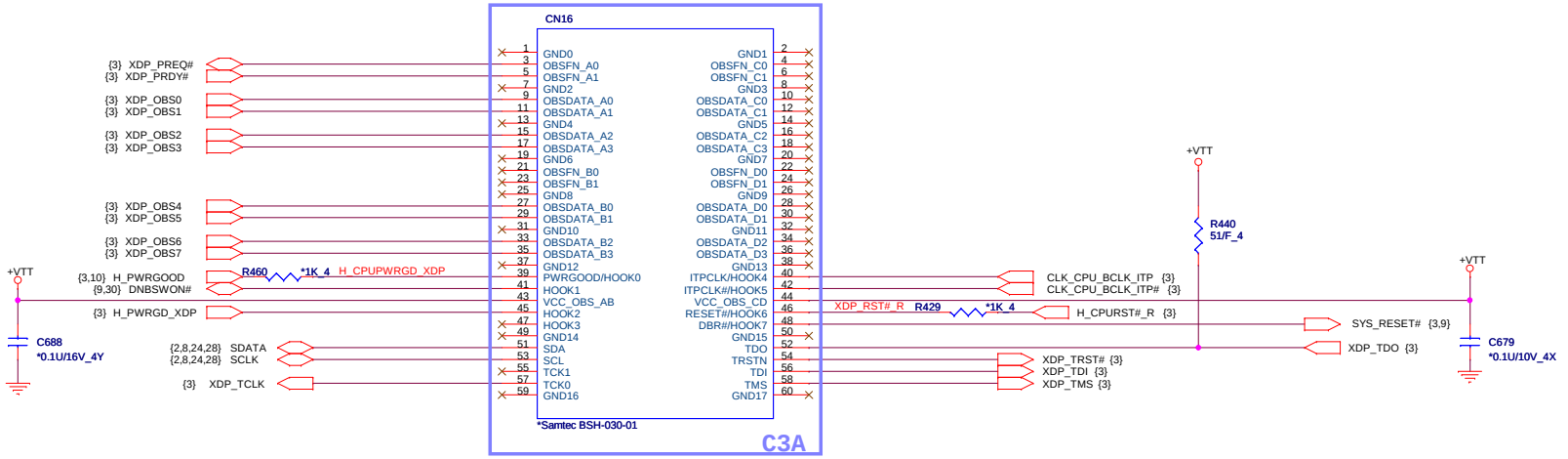
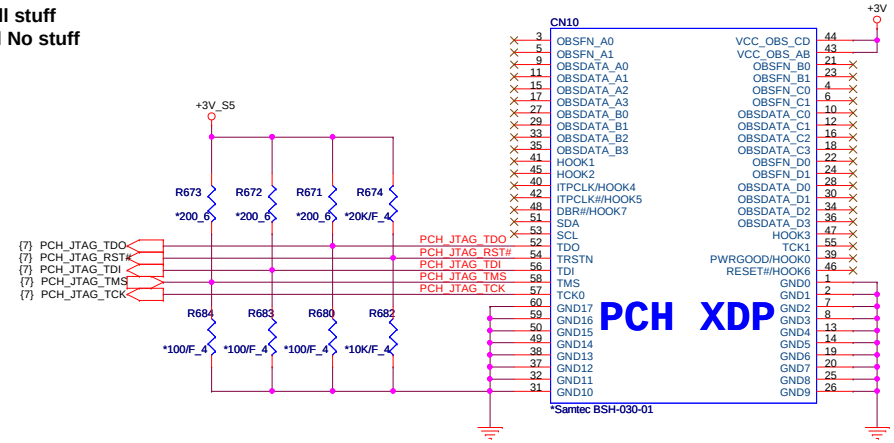
CPU XDP



Feature Set	SKU Name (S)				
	Q57	H57	H55	P55	P57
BraidWood	Y	Y	N	N	Y

PCH XDP

Note: For ES1/ES2 version all stuff
Production version all No stuff



Quanta Computer Inc.
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Size	Document Number	Rev
	NVRAM Connector	A1A

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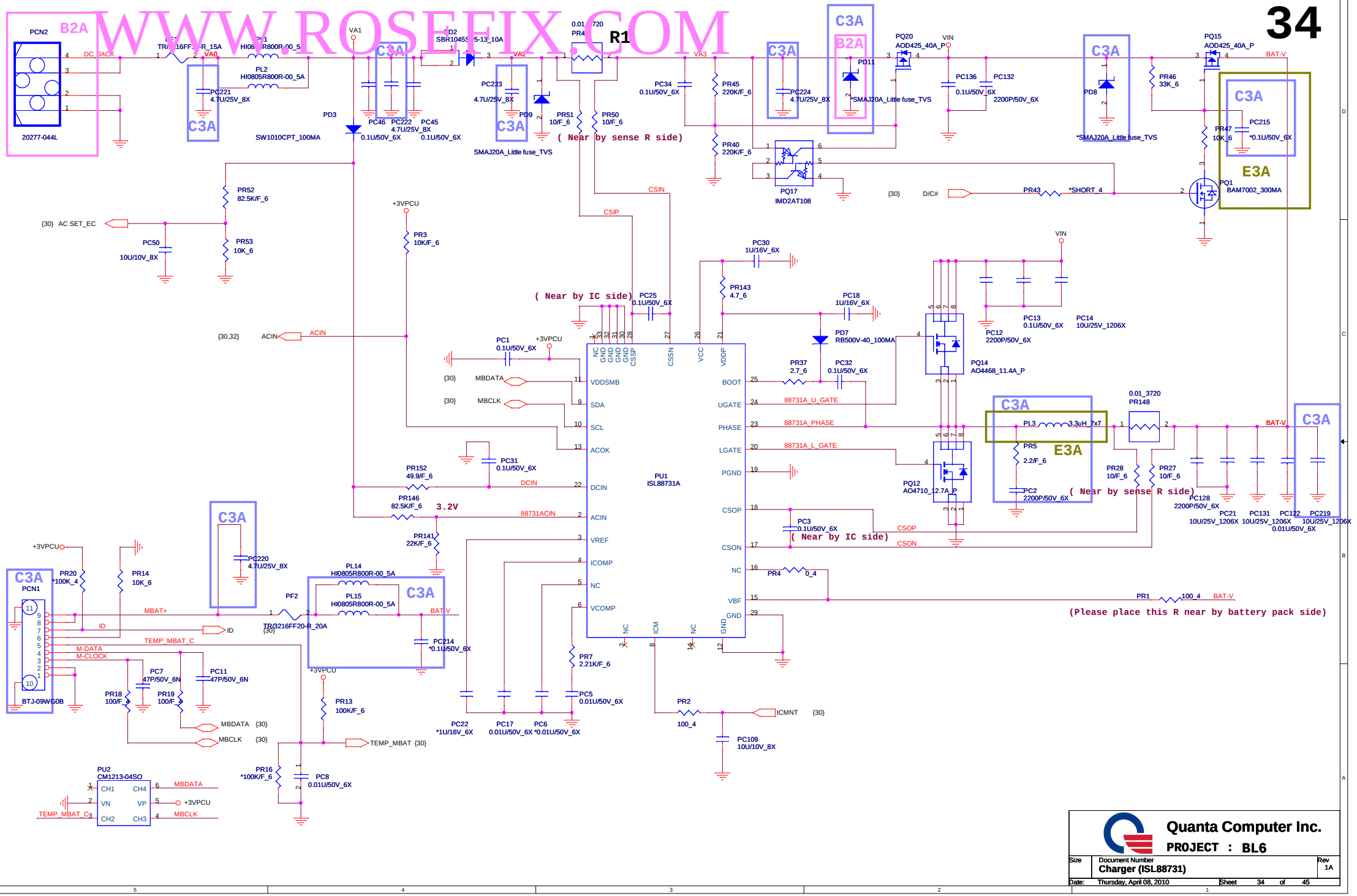


Quanta Computer Inc.		
PROJECT : BL6		
Size	Document Number: Charger (ISL88731)	Rev: 1A
Date: Thursday, April 08, 2010	Sheet 34 of 45	

For RT8210B 0_4 & 10K_4
For ISL6237 ZD5.6V , 100K/F_4 & 200K/F_4

(Peak 10.2 ,AVG 8.135A)
f : 400k Hz
OCP:11A

f : 500k Hz
(Peak 9A, AVG 7.623A)
OCP:11A

6A
7A

PU5 RT8210B

PQ29 AO4468_11.4A_P
PQ30 AO4710_12.7A_P
PQ33 AO4468_11.4A_P
PQ32 AO4710_12.7A_P
PQ4 AO4496_10A
PQ59 AO6402A_7A
PQ3 AO4496_10A
PQ2 AO6402A_7A

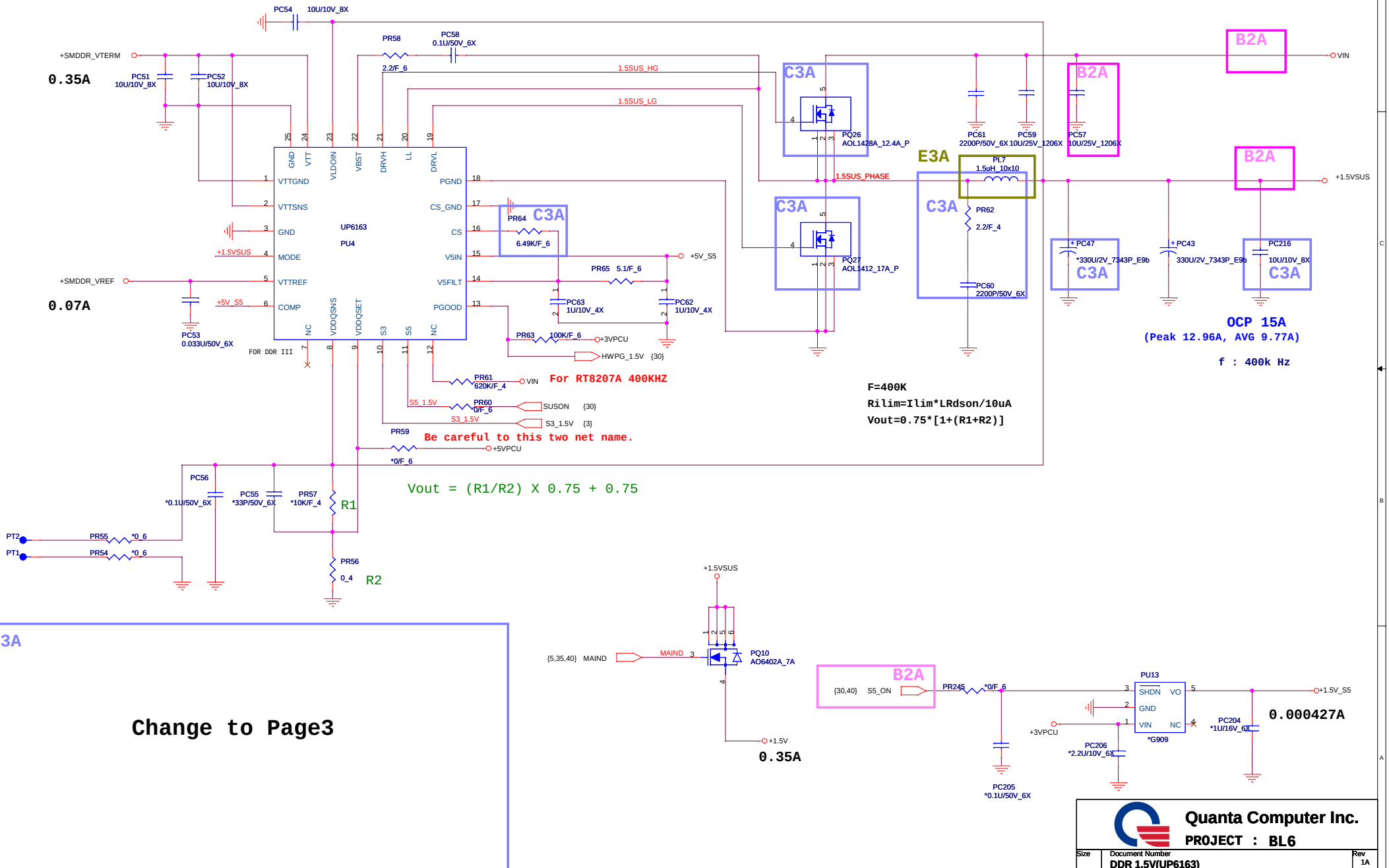
PD5 CHN21UPT_100MA
PD4 CHN21UPT_100MA
PD6 *ZD5.6V

PL10 2.2uH_10x10
PL8 2.2uH_10x10

2.744A~4.984A
0.001A
1.984A
4.253A

Quanta Computer Inc.
PROJECT : BL6

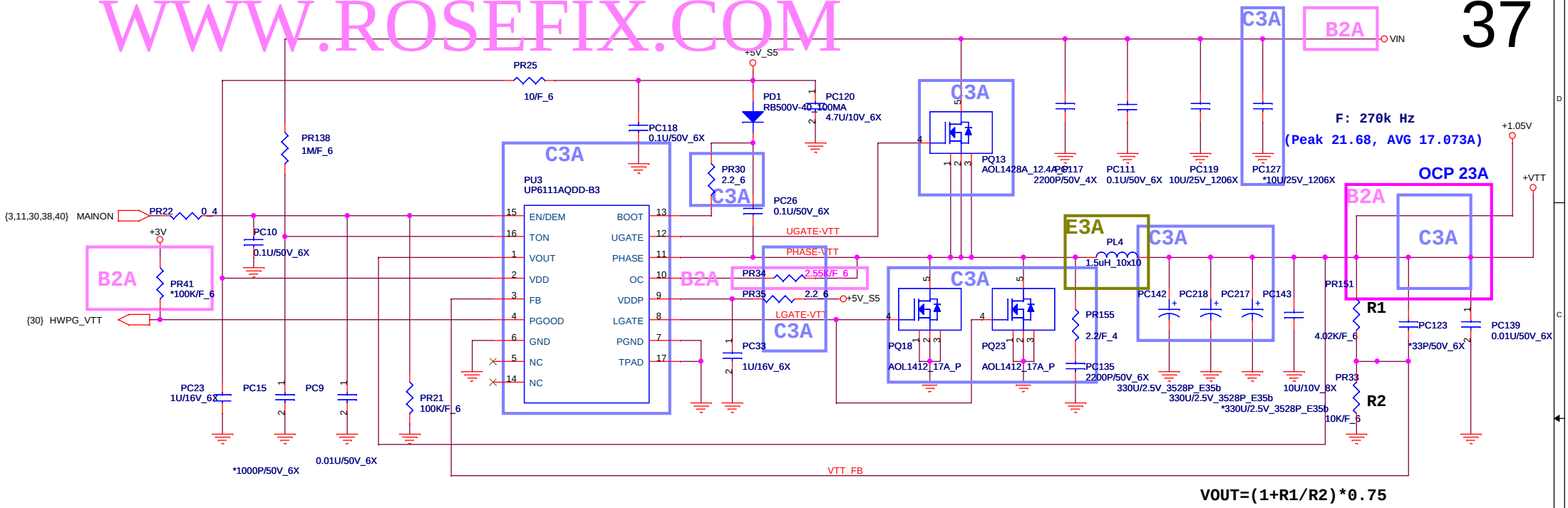
Size	Document Number	Rev
	System 5V/3V (ISL6237)	1A
Date: Wednesday, April 07, 2010	Sheet 35 of 45	



Quanta Computer Inc.

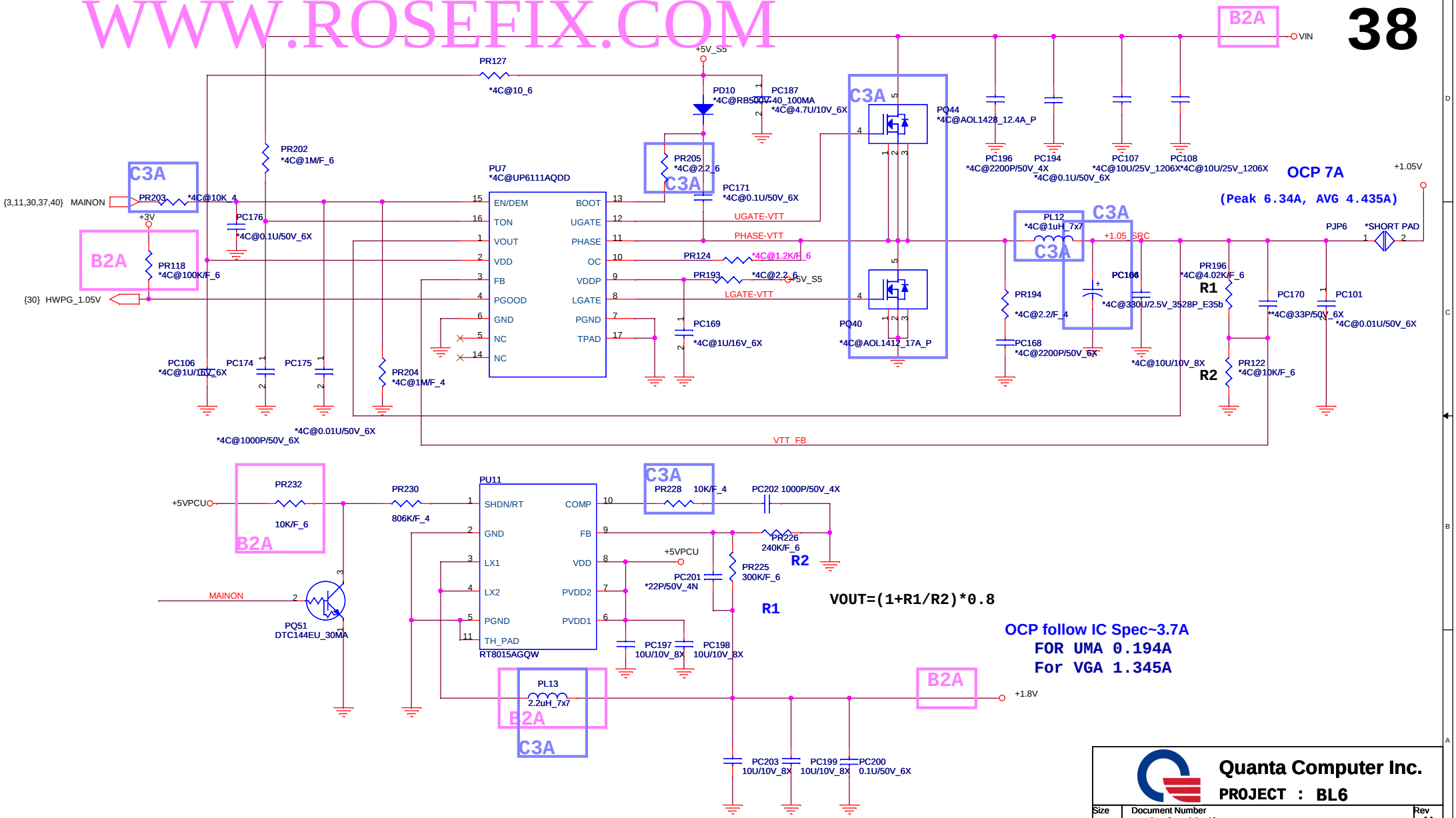
PROJECT : BL6

Size	Document Number	Rev
	DDR 1.5V(UP6163)	1A
Date: Wednesday, April 07, 2010	Sheet 36 of 45	

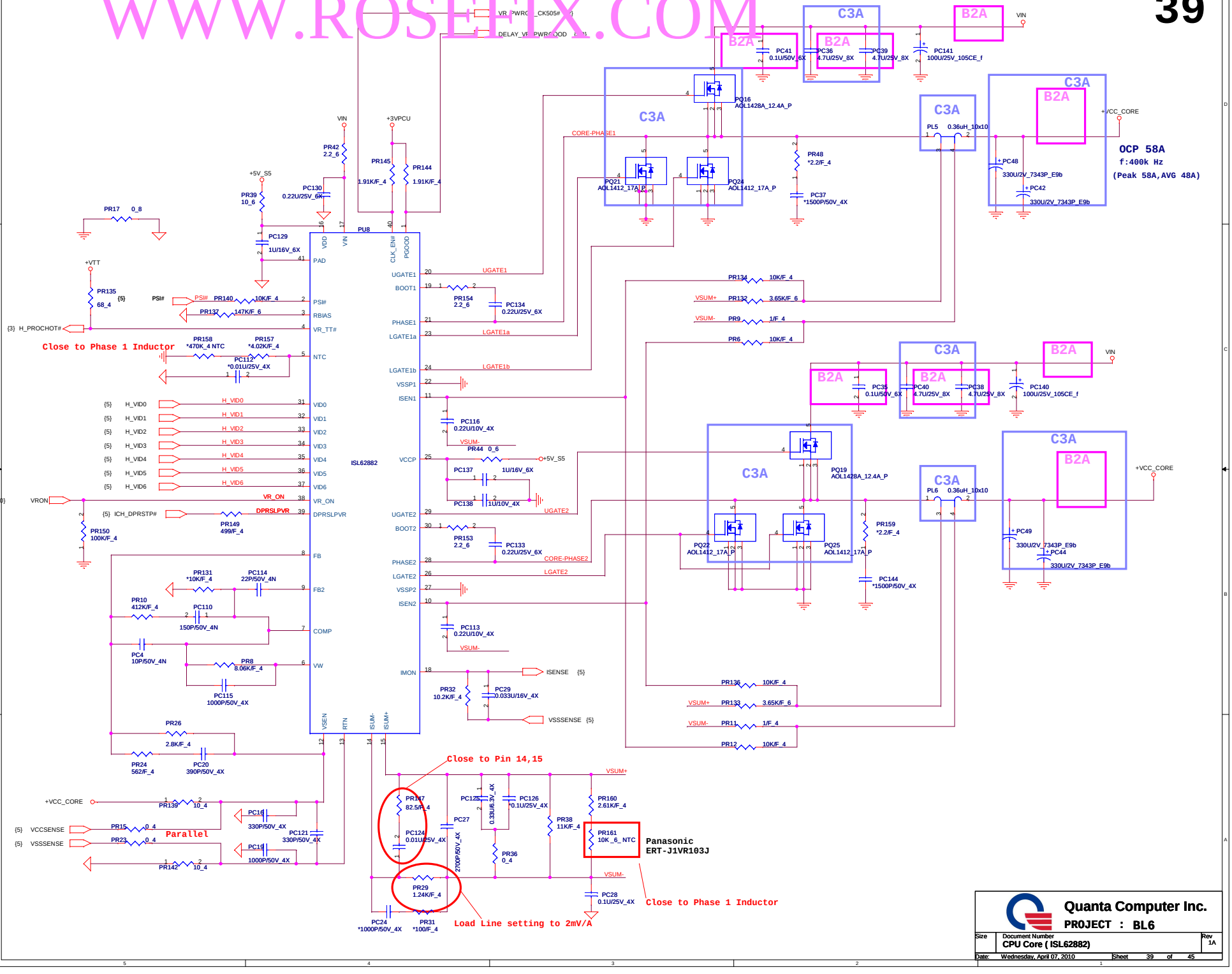


$$VOUT=(1+R1/R2)*0.75$$

Quanta Computer Inc.		
PROJECT : BL6		
Size	Document Number: +VTT (UP6111A)	Rev: 1A
Date: Wednesday, April 07, 2010	Sheet 37 of 45	



Quanta Computer Inc.		
PROJECT : BL6		
Size	Document Number: +1.8V (RT8253)	Rev: 1A
Date: Wednesday, April 07, 2010	Sheet 38 of 45	



Quanta Computer Inc.
PROJECT : BL6
Size
Document Number
CPU Core (ISL62882)
Rev 1A
Date: Wednesday, April 07, 2010
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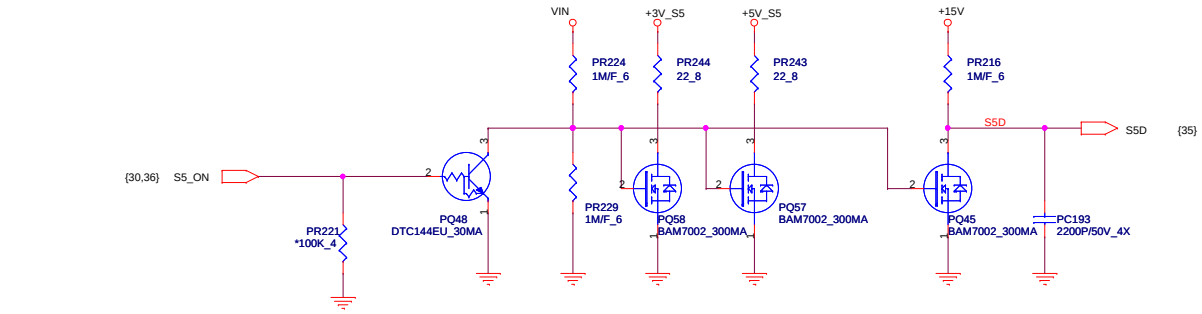

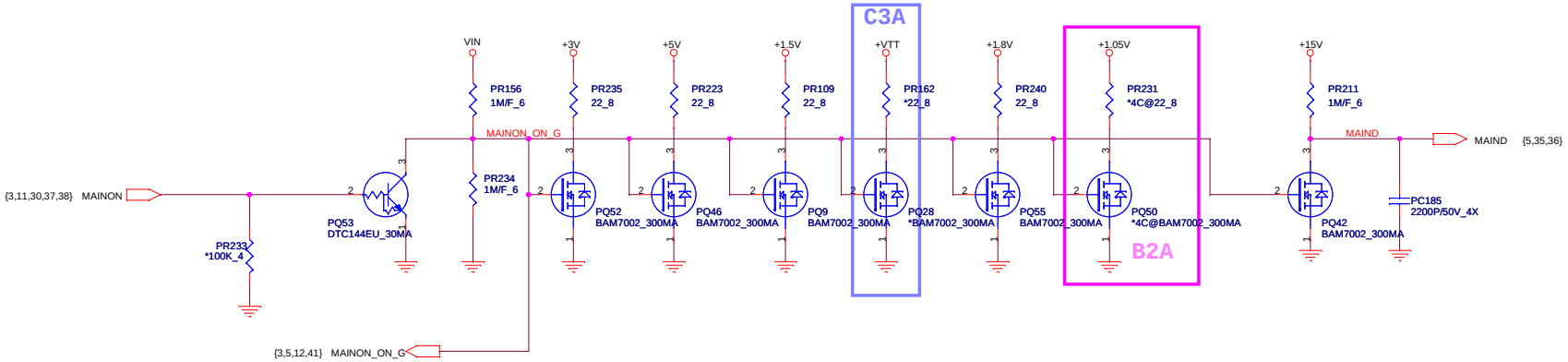

Quanta Computer Inc.		
PROJECT : BL6		
Size	Document Number: Discharge (1.5V_S5/1.8V)	Rev: 1A
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OCP:30A
(Peak 28A, AVG 23.1A)
F: 297k Hz

B2A

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	Madison/Park	Madison/Park Resistor	M92	M92 Resistor	M96	M96 Resistor
LOW	LOW	0.9V	R1=39.2K CS33922FB15	0.9V	R1=39.2K CS33922FB15	0.9V	R1=39.2K CS33922FB15
LOW	HIGH	0.95V	R2=60.4K CS36042FB10	0.95V	R2=60.4K CS36042FB10	0.95V	R2=49.9K CS34992FB10
HIGH	LOW	1.12V	R3=309K CS43092FB16	1.1V	R3=270K CS42702FB10	1V	R3=249K CS42492FB18
HIGH	HIGH	NA	R4=88.7K CS38872FB18	1.2V	R4=93.1K CS39312FB15	1.1V	R4=140K CS41402FB14

0.996A

1.791A

VO=(0.8(R1+R2)/R2)
R2<120Kohm

B2A
PCIE_VDDC
M92,M96-->1.1V
Madison,Park-->1.0V

	Madison,Park	M92,M96
PR163 = R1	25.5K/F_4 CS32552FB11	38.3K/F_4 CS33832FB08
PR166 = R2	100K/F_4 CS41002FB28	100K/F_4 CS41002FB28

5.74A

Quanta Computer Inc.
PROJECT : BL6

Size	Document Number	Rev
	+VGPU_CORE (MAX8792)	1A

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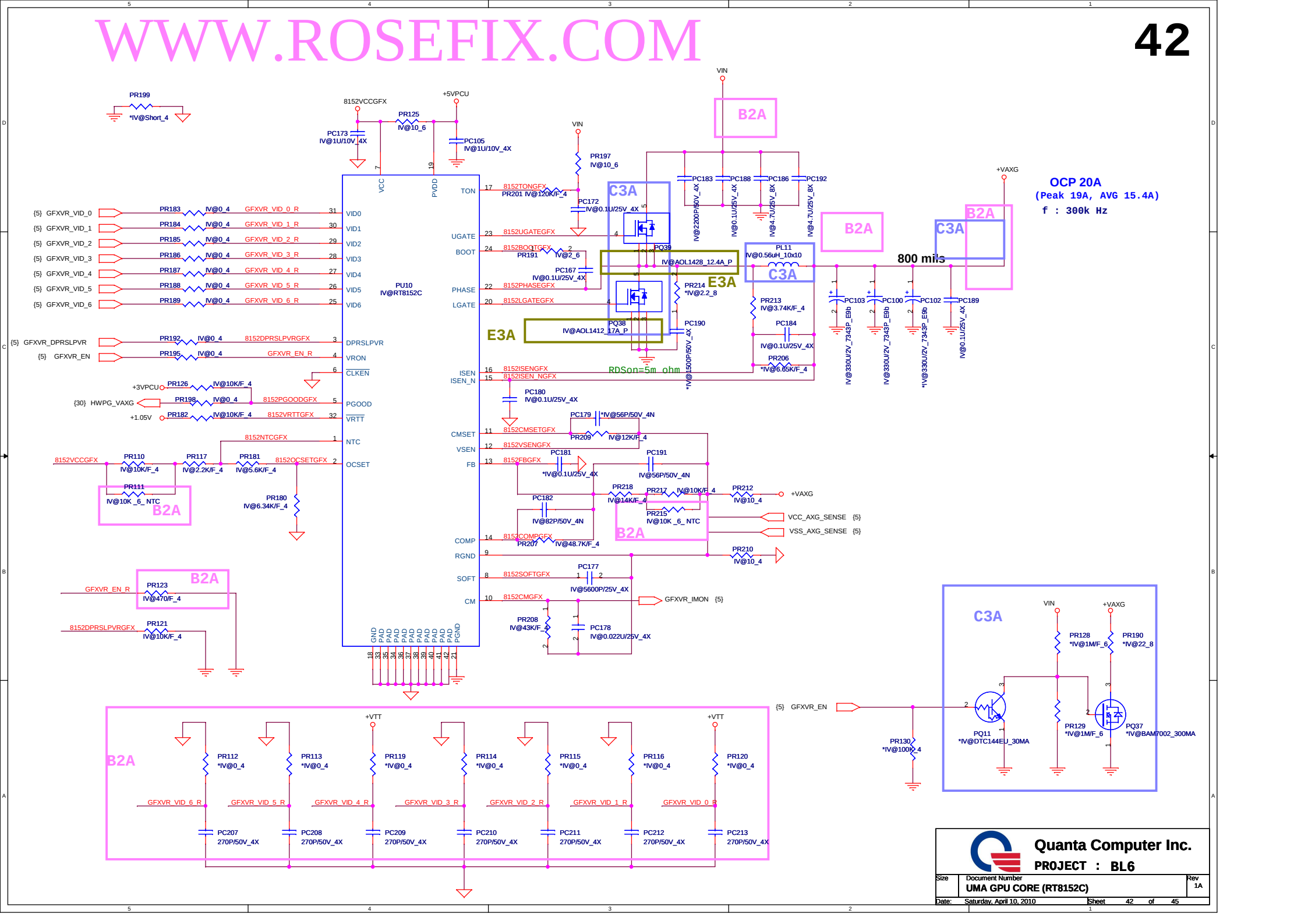

Quanta Computer Inc.

PROJECT : BL6

Size	Document Number	Rev
	UMA GPU CORE (RT8152C)	1A
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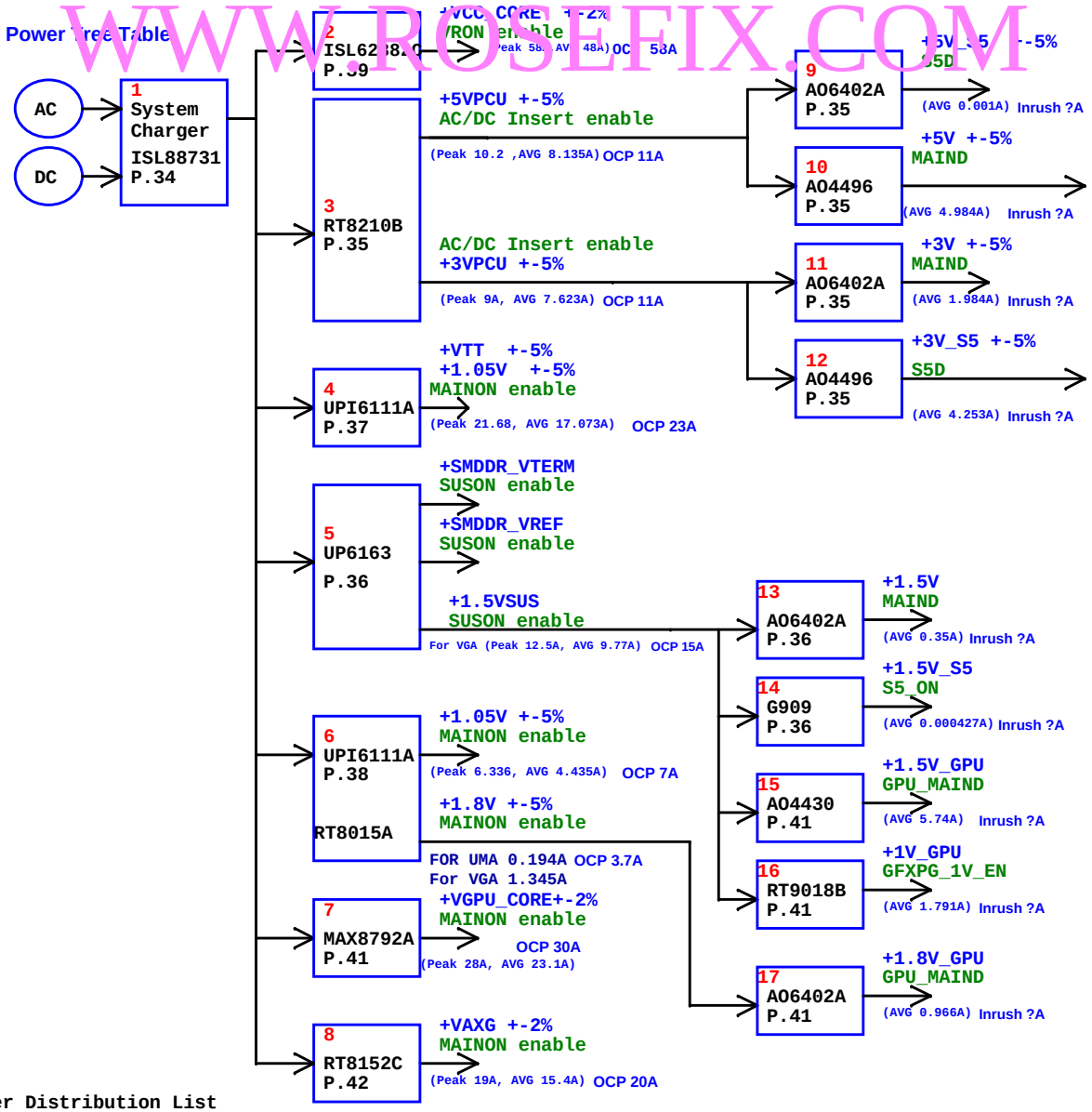
Power Tree Table



Power Distribution List

Power	Distribution

Quanta Computer Inc.
PROJECT : BL6

Size	Document Number	Rev
	Power Tree Table	1A

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