

# ***NBQAA***

## ***Bordeaux 10G***

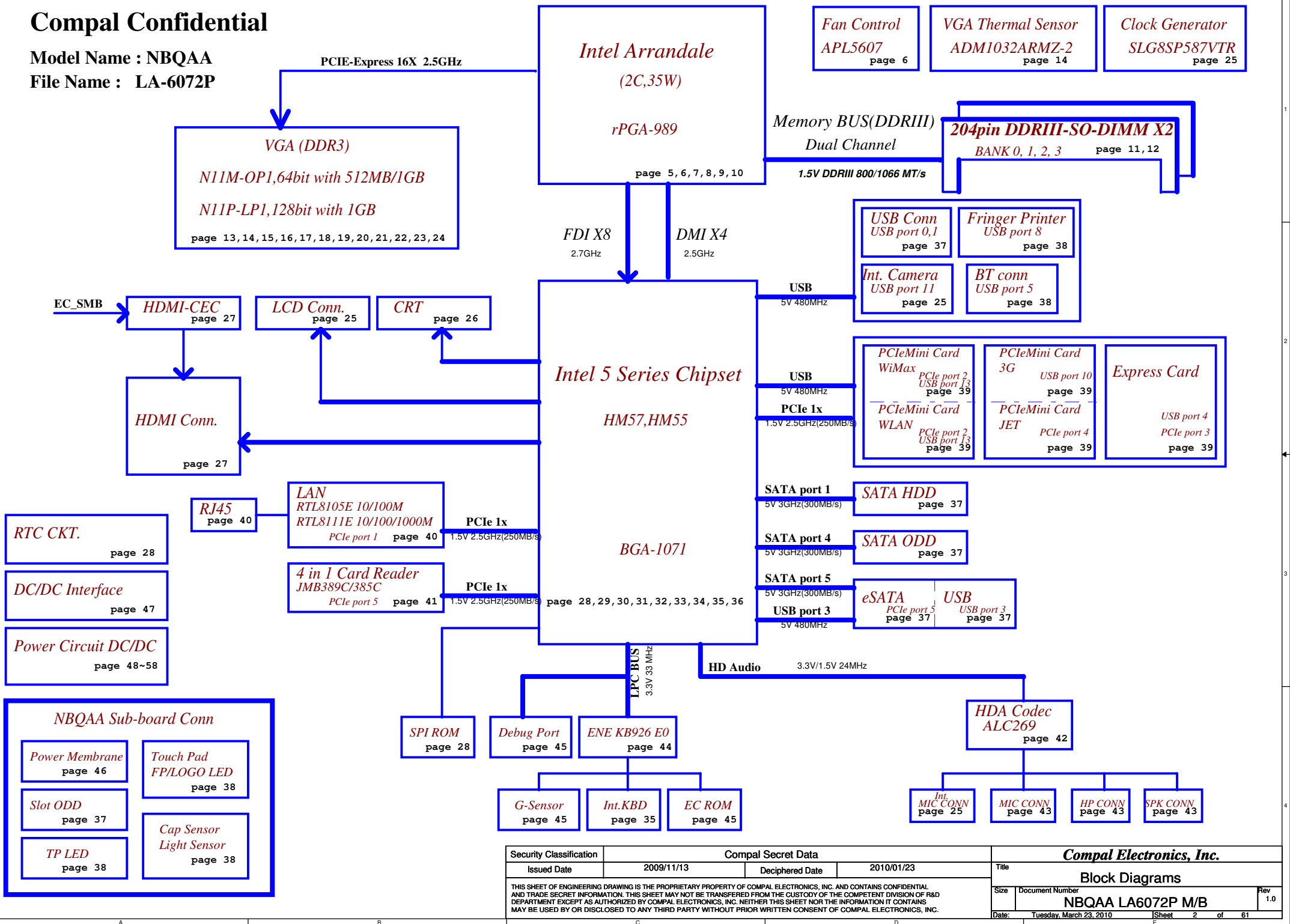
### ***LA-6072P REV 1.0 Schematic***

Intel Arrandale CPU / Intel 5 Series Chipset  
2010-03-22 Rev 1.0

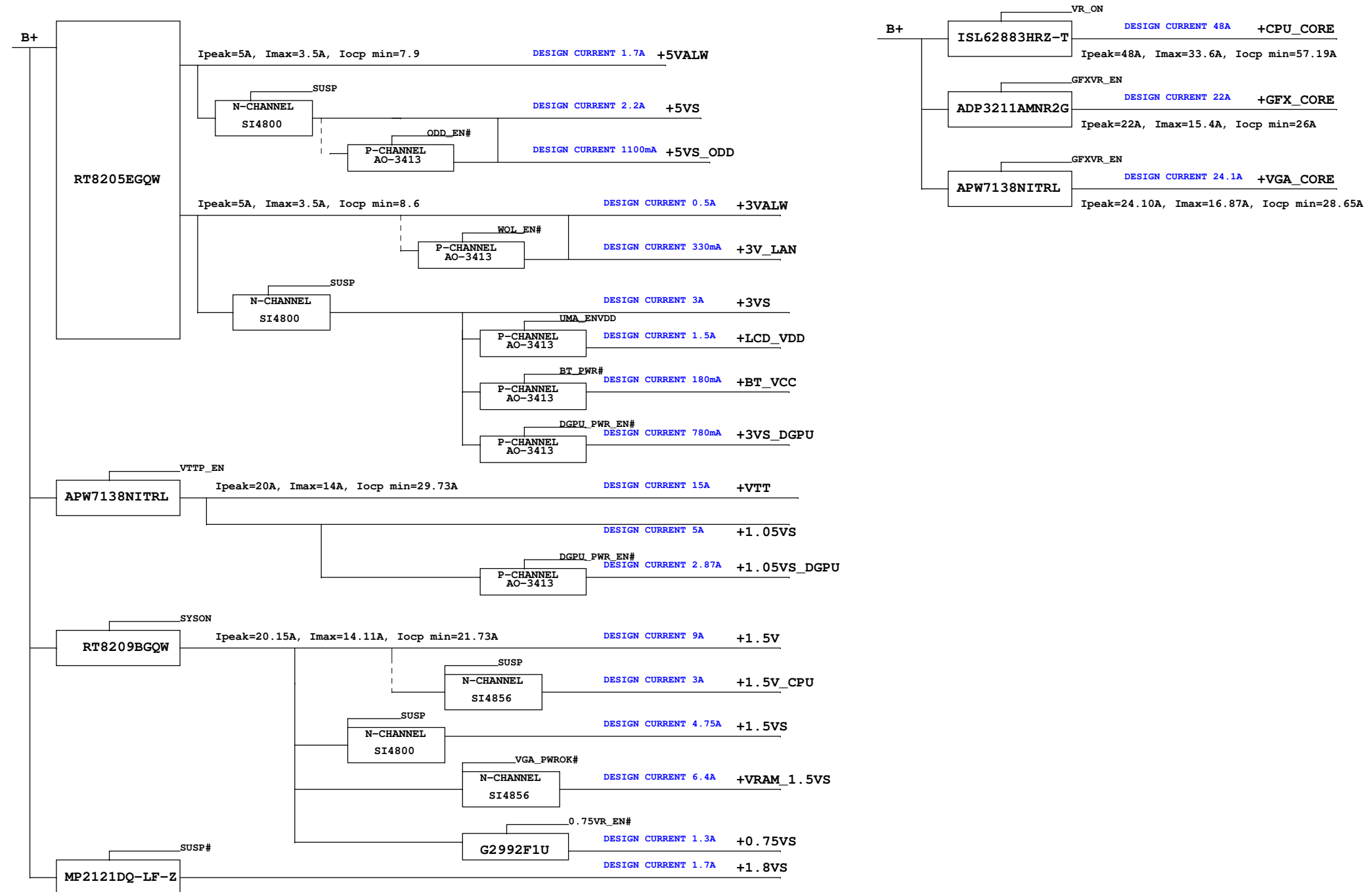
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Issued Date	2009/11/13	Deciphered Date	2010/01/23	Title <b>Cover Page</b>		
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# Compal Confidential

Model Name : NBQAA  
File Name : LA-6072P



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### Voltage Rails

( O MEANS ON X MEANS OFF )

power plane / State	+RTCVCC	+B	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.5VS +VGA_CORE +CPU_CORE +VTT +1.05VS +1.8VS +1.1VS +0.75VS
S0	O	O	O	O	O
S1	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	O	X	X
S5 S4/ Battery only	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X

### BTO Option Table

Function	Bluetooth	Card Reader		HDMI-CEC		LAN		CAM+MIC
description	B				Y	U	V	X
explain	Bluetooth	JMB389	JMB385	HDMI	HDMI+CEC	10/100	10/100/1000	CAM
BTO	BT@	JMB389@	JMB385@	IHDMI@	IHDMI@+CEC@	8105E@	8111E@	CAM@

Function	ODD		KB LED	Mini Card			GPU	
description		T	K	G	J	W	P	M
explain	Normal	Slot	KB LED	3G	JET	WiMAX	N11P-LP1	N11M-OP1
BTO	ODD0@	ODD1@	KBL@	3G@	JET@	WiMAX@	N11P@	N11P@

Function	PCH		VRAM	
description	H5	H7	512	1G
explain	HM55	HM57	512M	1G
BTO	HM55@	HM57@	4pcs@	4pcs@+8pcs@

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1 (Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

### EC SM Bus1 address

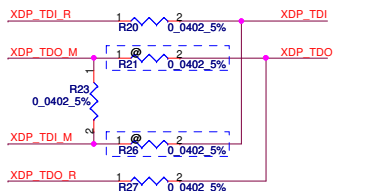
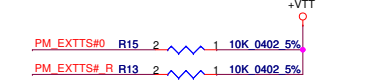
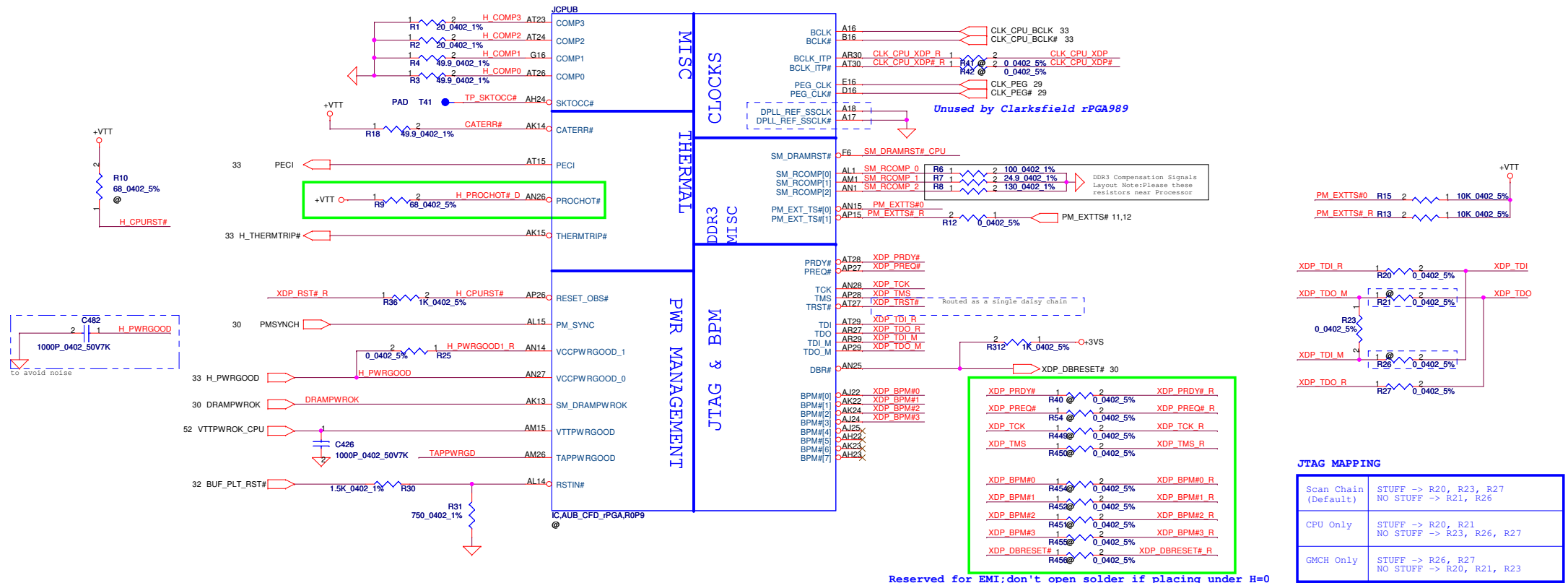
### EC SM Bus2 address

Power	Device	Address	Power	Device	Address
+3VL	EC KB926 D3		+3VS	EC KB926 D3	
+3VL	HDMI-CEC		+3VS	AMD GPU Thermal Sensor	
+3VL	Smart Battery	0001 011x b	+3VS	Ambient Ligh Sensor	
			+3VALW	PCH	
			+3VS	G-Sensor	

### PCH SM Bus address

Power	Device	Address
+3VALW	PCH	
+3VS	Clock Generator	1101 001x b
+3VS	DDR DIMMA	1001 000x b
+3VS	DDR DIMMB	1001 010x b
+3VS	Express	
+3VS	Slot#1--WLAN/Wimax	
+3VS	Slot#2--JET/3G	

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				Size Custom
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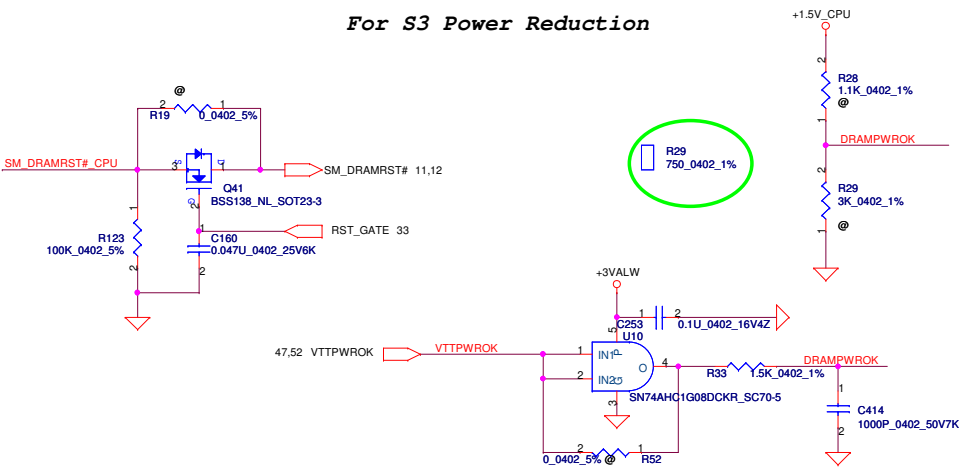


**JTAG MAPPING**

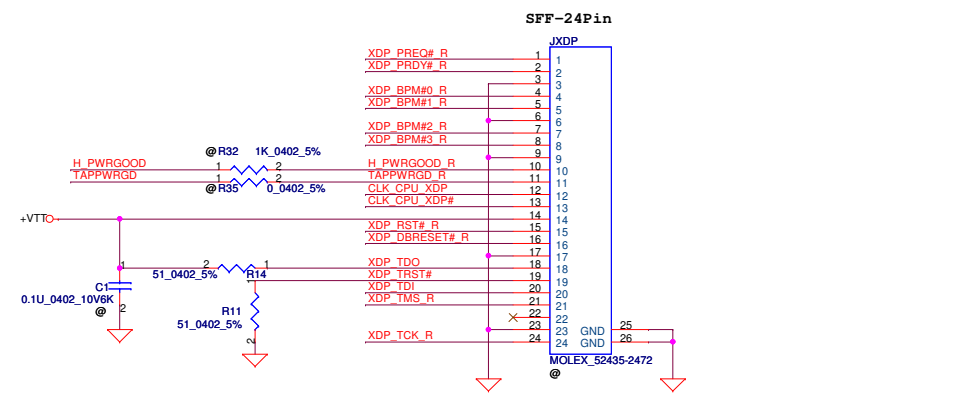
Scan Chain (Default)	STUFF -> R20, R23, R27 NO STUFF -> R21, R26
CPU Only	STUFF -> R20, R21 NO STUFF -> R23, R26, R27
GMCH Only	STUFF -> R26, R27 NO STUFF -> R20, R21, R23

Reserved for EMI; don't open solder if placing under H=0

**For S3 Power Reduction**

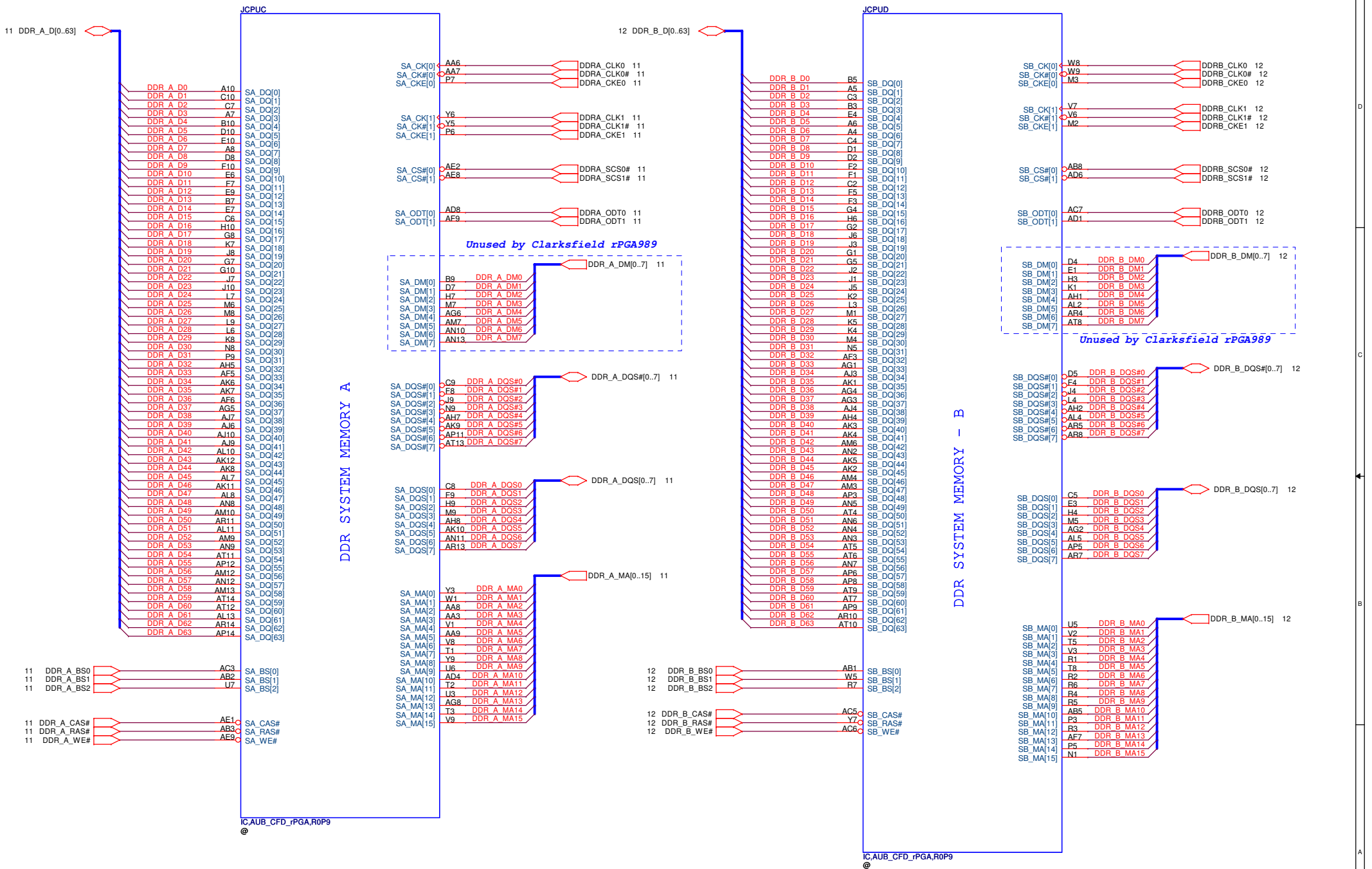


**XDP Connector**

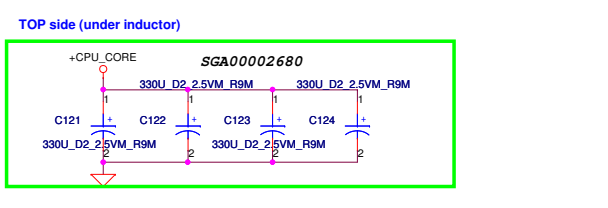
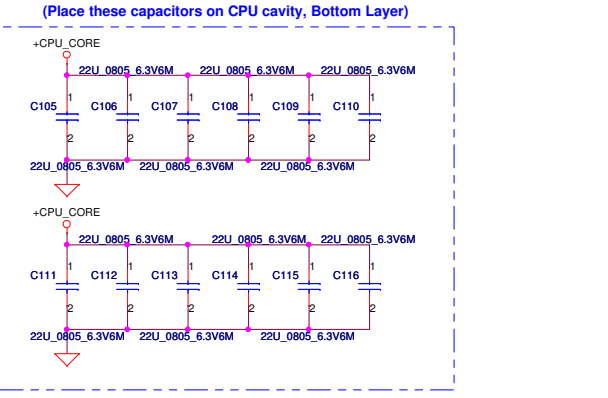
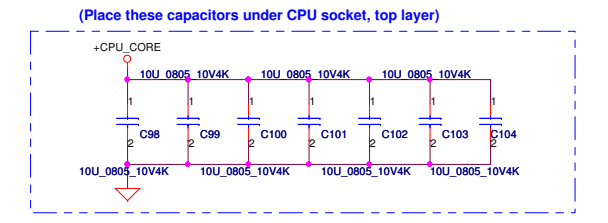
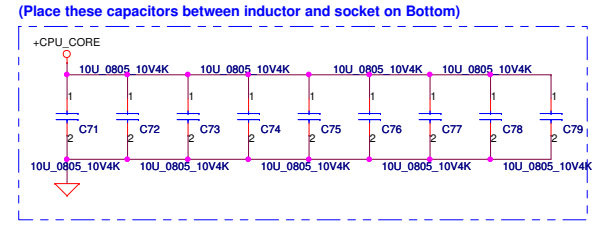
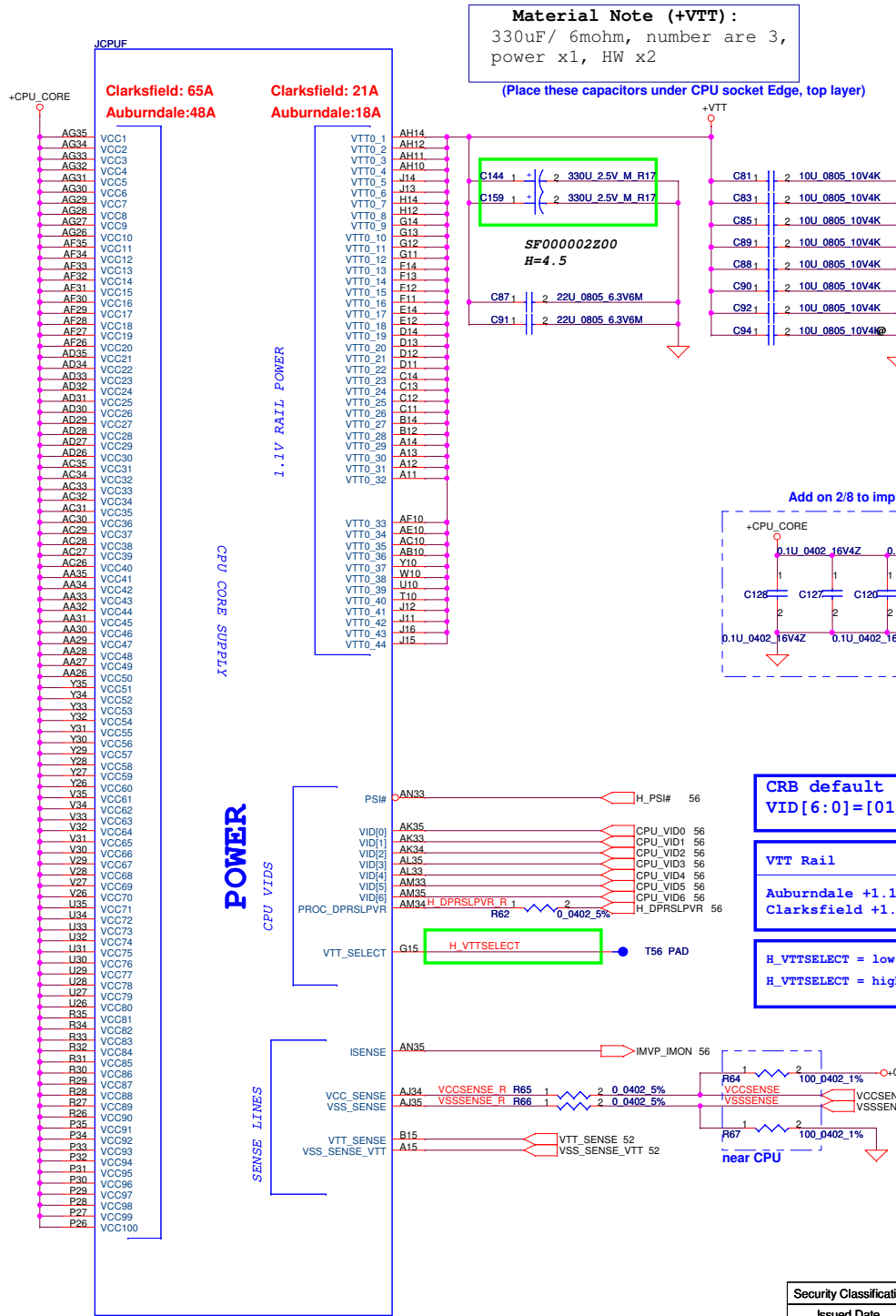


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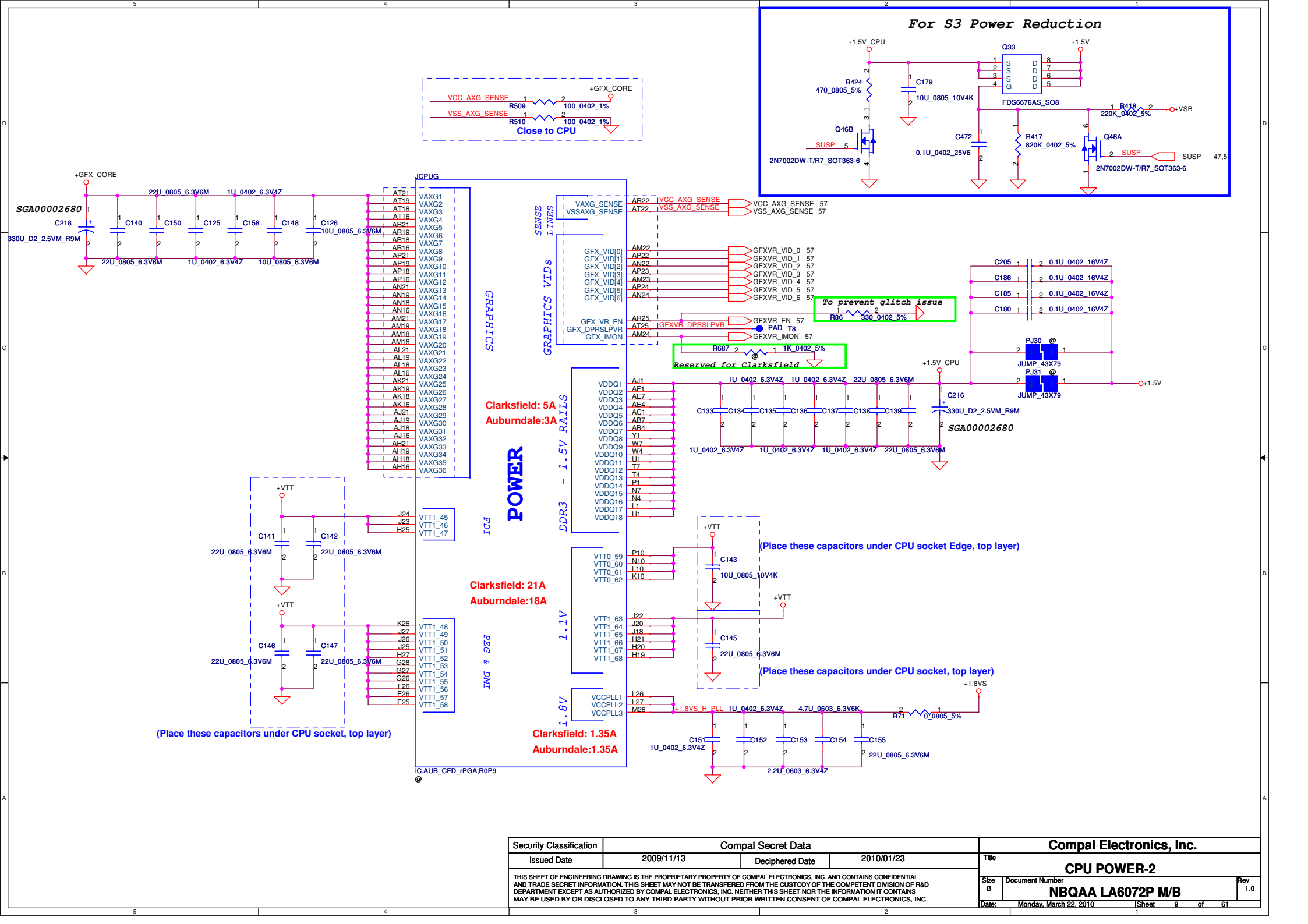
**Check list:**

+CPU\_CORE: 6x 470uF, 12x 22uF, 17x 10uF

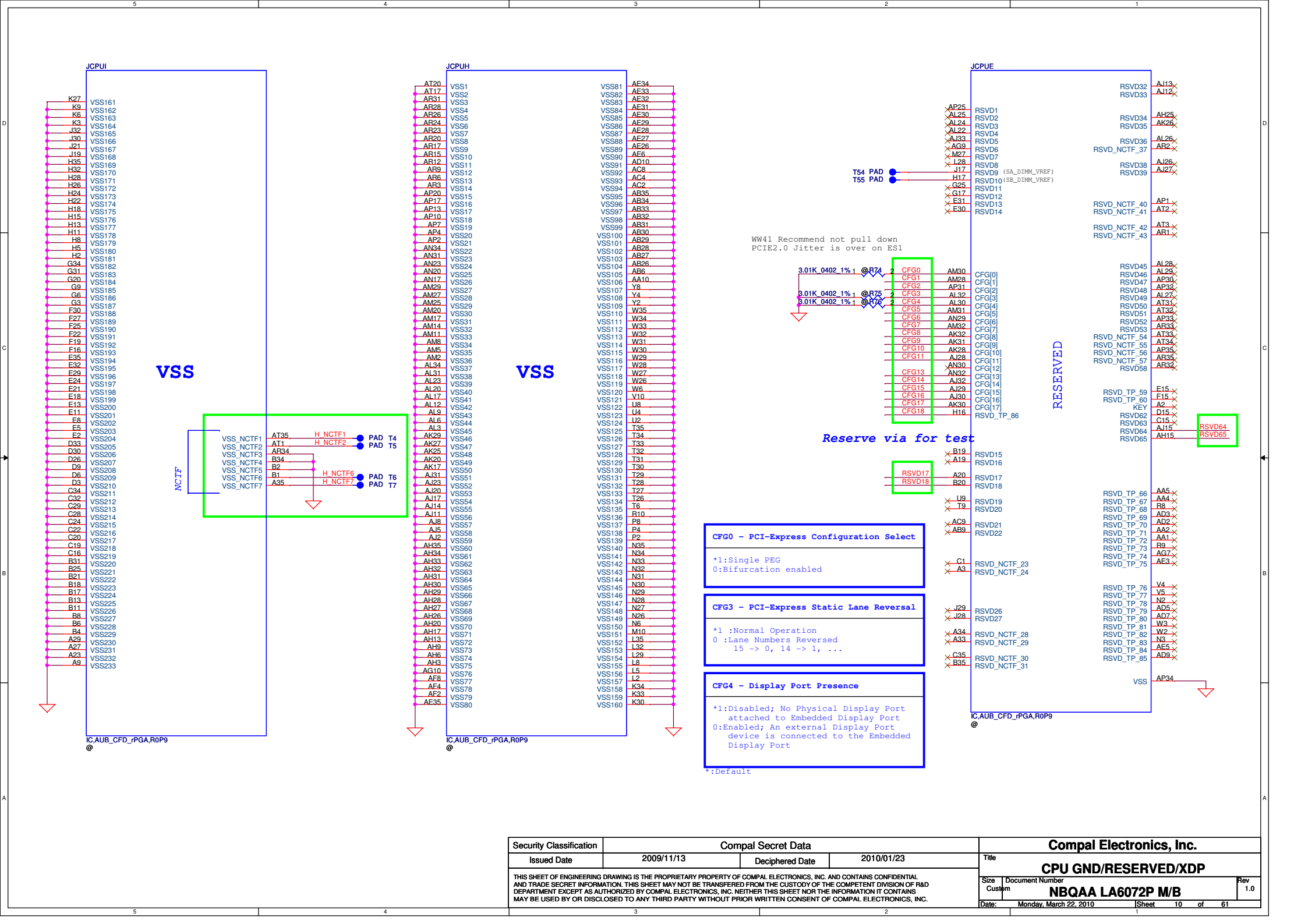
+VTT: 4x 330uF, 7x 22uF, 8x 10uF

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				<b>CPU POWER-1</b>	
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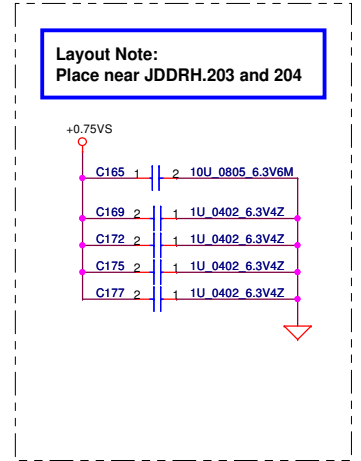
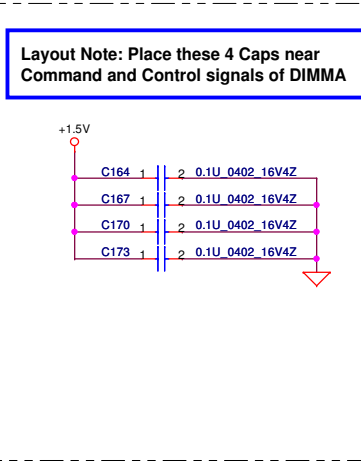
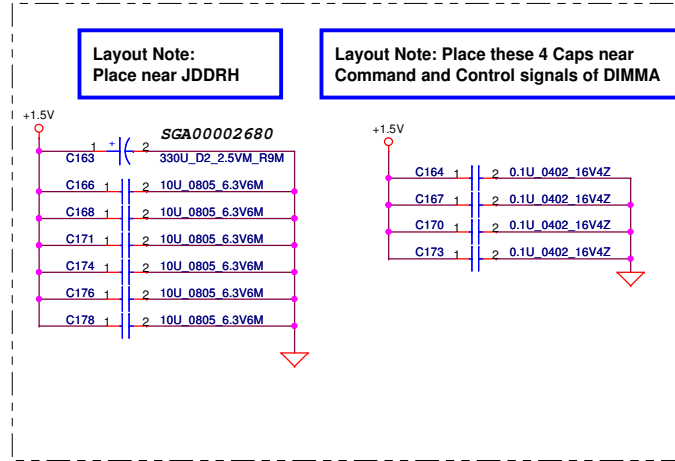
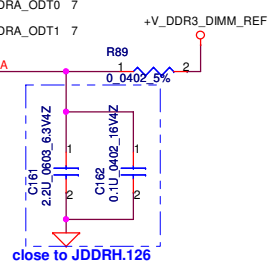
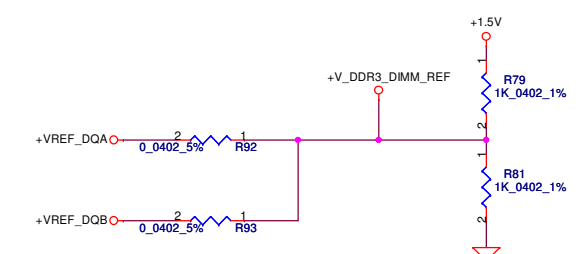
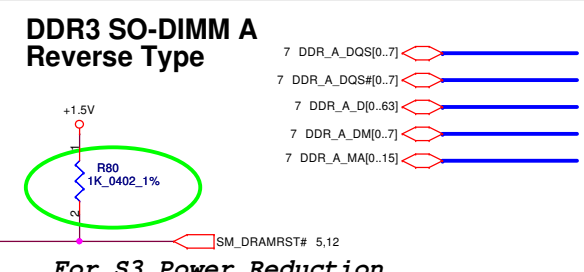
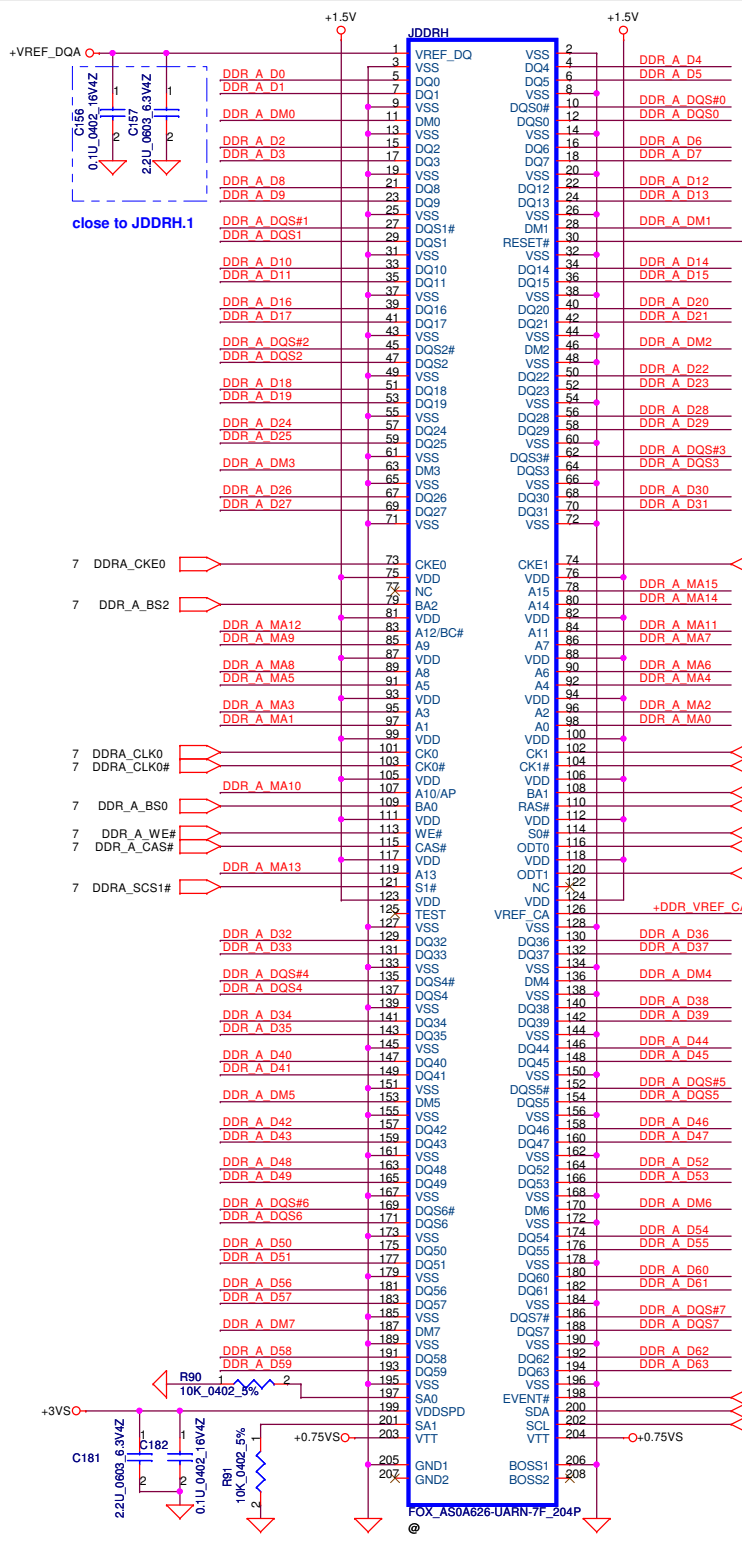




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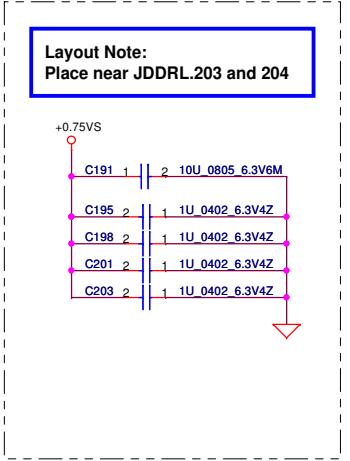
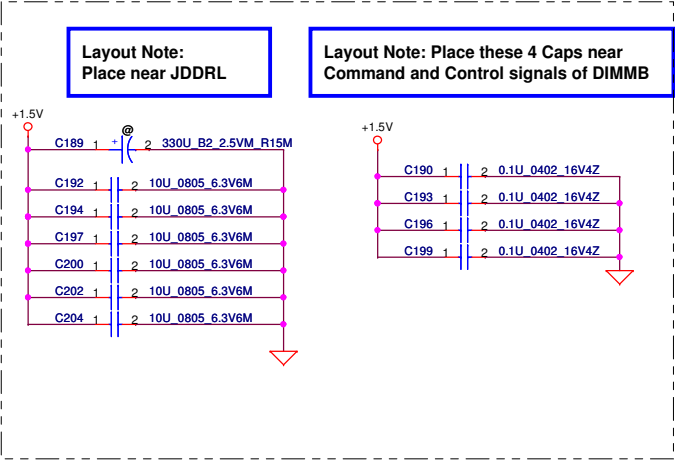
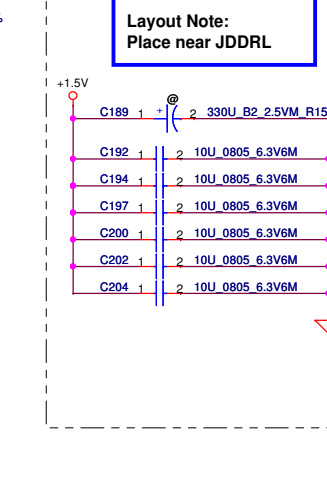
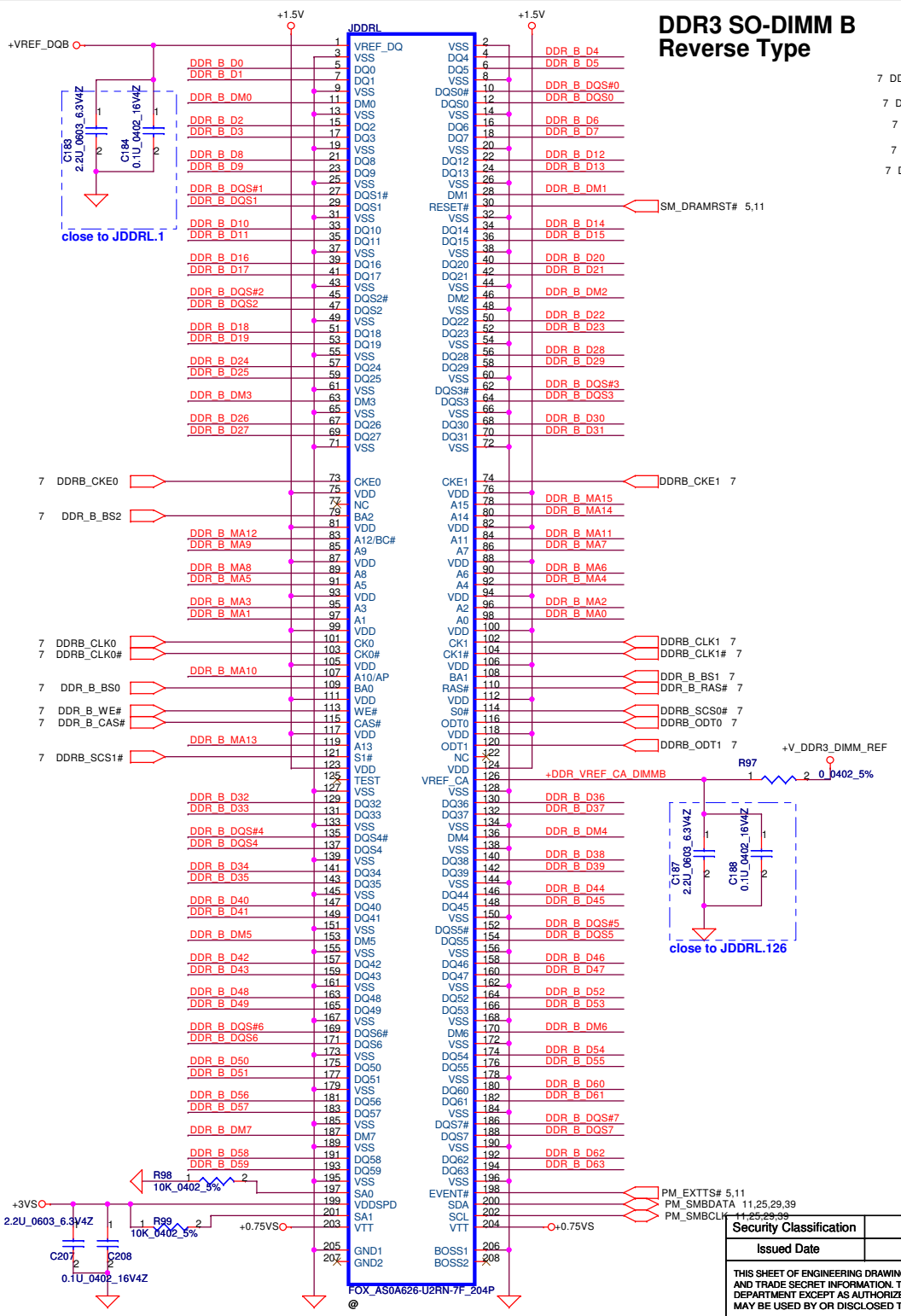
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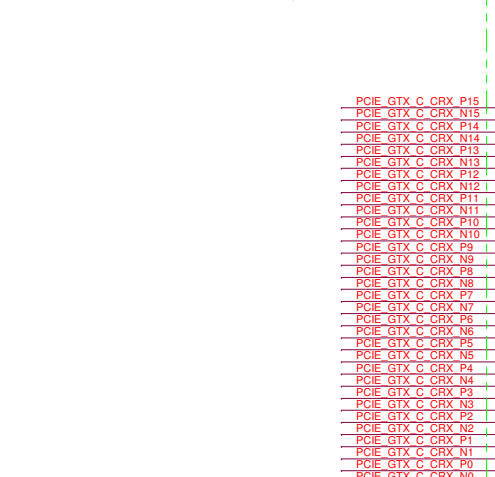
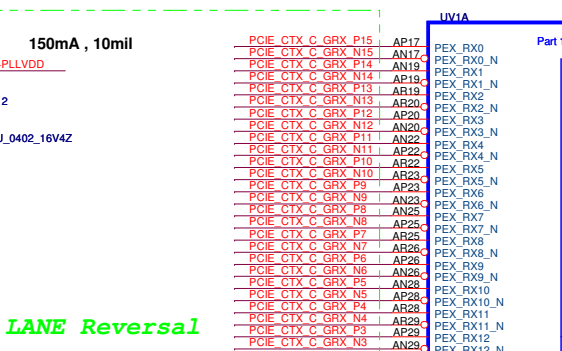
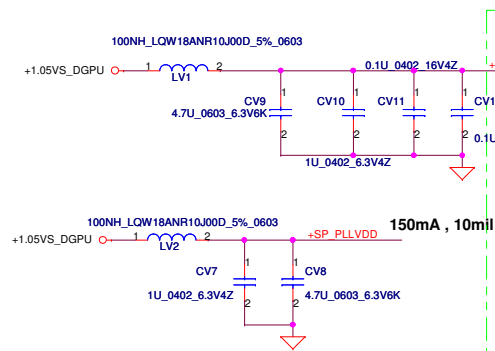
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DDRIII-SODIMMO			
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# DDR3 SO-DIMM B Reverse Type

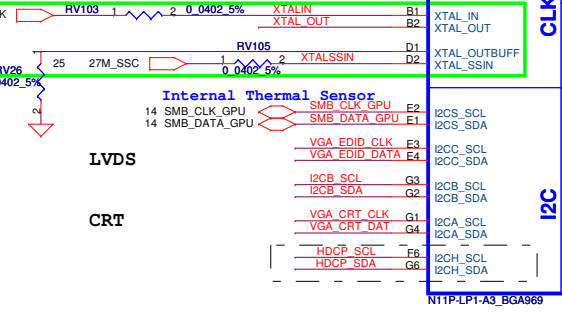
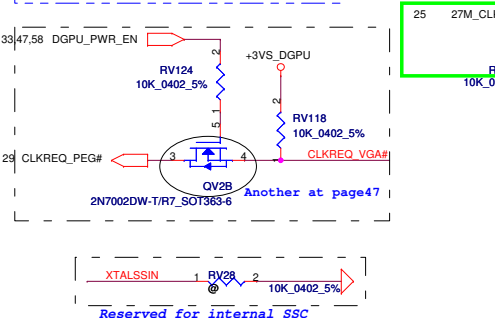
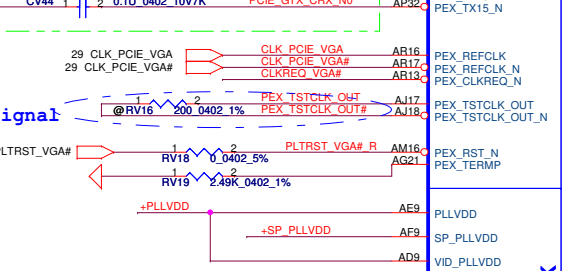
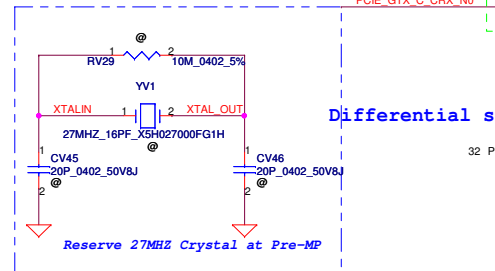


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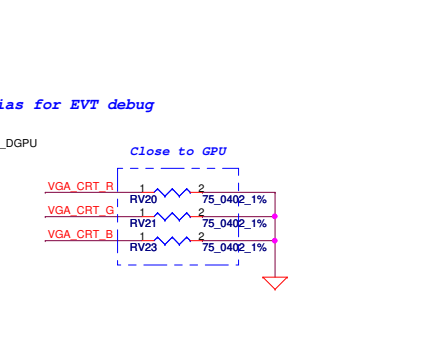
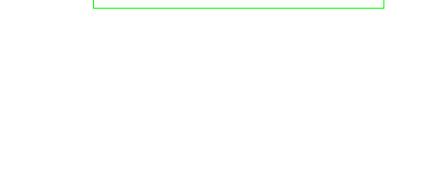
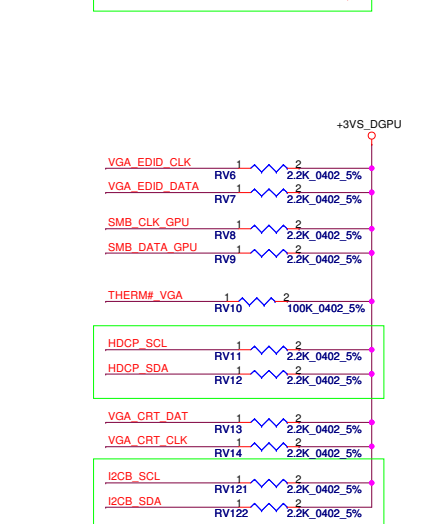
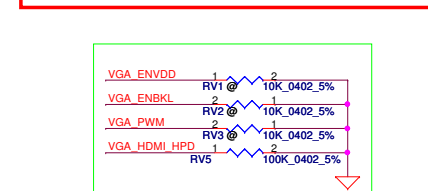
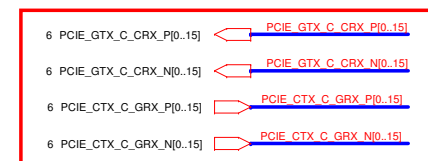
**LANE Reversal**

PCIE GTX C CRX P15	CV13	1	2	0.1U_0402_10V7K	PCIE GTX CRX P15	AL17
PCIE GTX C CRX N15	CV14	1	2	0.1U_0402_10V7K	PCIE GTX CRX N15	AN17
PCIE GTX C CRX P14	CV15	1	2	0.1U_0402_10V7K	PCIE GTX CRX P14	AL18
PCIE GTX C CRX N14	CV16	1	2	0.1U_0402_10V7K	PCIE GTX CRX N14	AN18
PCIE GTX C CRX P13	CV17	1	2	0.1U_0402_10V7K	PCIE GTX CRX P13	AL19
PCIE GTX C CRX N13	CV18	1	2	0.1U_0402_10V7K	PCIE GTX CRX N13	AN19
PCIE GTX C CRX P12	CV19	1	2	0.1U_0402_10V7K	PCIE GTX CRX P12	AL20
PCIE GTX C CRX N12	CV20	1	2	0.1U_0402_10V7K	PCIE GTX CRX N12	AN20
PCIE GTX C CRX P11	CV21	1	2	0.1U_0402_10V7K	PCIE GTX CRX P11	AL21
PCIE GTX C CRX N11	CV22	1	2	0.1U_0402_10V7K	PCIE GTX CRX N11	AN21
PCIE GTX C CRX P10	CV23	1	2	0.1U_0402_10V7K	PCIE GTX CRX P10	AL22
PCIE GTX C CRX N10	CV24	1	2	0.1U_0402_10V7K	PCIE GTX CRX N10	AN22
PCIE GTX C CRX P9	CV25	1	2	0.1U_0402_10V7K	PCIE GTX CRX P9	AL23
PCIE GTX C CRX N9	CV26	1	2	0.1U_0402_10V7K	PCIE GTX CRX N9	AN23
PCIE GTX C CRX P8	CV27	1	2	0.1U_0402_10V7K	PCIE GTX CRX P8	AL24
PCIE GTX C CRX N8	CV28	1	2	0.1U_0402_10V7K	PCIE GTX CRX N8	AN24
PCIE GTX C CRX P7	CV29	1	2	0.1U_0402_10V7K	PCIE GTX CRX P7	AL25
PCIE GTX C CRX N7	CV30	1	2	0.1U_0402_10V7K	PCIE GTX CRX N7	AN25
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PCIE GTX C CRX N5	CV34	1	2	0.1U_0402_10V7K	PCIE GTX CRX N5	AN27
PCIE GTX C CRX P4	CV35	1	2	0.1U_0402_10V7K	PCIE GTX CRX P4	AL28
PCIE GTX C CRX N4	CV36	1	2	0.1U_0402_10V7K	PCIE GTX CRX N4	AN28
PCIE GTX C CRX P3	CV37	1	2	0.1U_0402_10V7K	PCIE GTX CRX P3	AL29
PCIE GTX C CRX N3	CV38	1	2	0.1U_0402_10V7K	PCIE GTX CRX N3	AN29
PCIE GTX C CRX P2	CV39	1	2	0.1U_0402_10V7K	PCIE GTX CRX P2	AL30
PCIE GTX C CRX N2	CV40	1	2	0.1U_0402_10V7K	PCIE GTX CRX N2	AN30
PCIE GTX C CRX P1	CV41	1	2	0.1U_0402_10V7K	PCIE GTX CRX P1	AL31
PCIE GTX C CRX N1	CV42	1	2	0.1U_0402_10V7K	PCIE GTX CRX N1	AN31
PCIE GTX C CRX P0	CV43	1	2	0.1U_0402_10V7K	PCIE GTX CRX P0	AL32
PCIE GTX C CRX N0	CV44	1	2	0.1U_0402_10V7K	PCIE GTX CRX N0	AN32

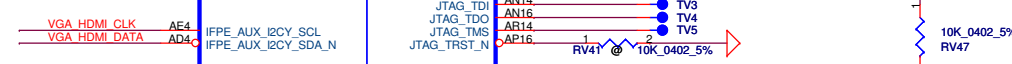
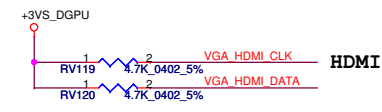
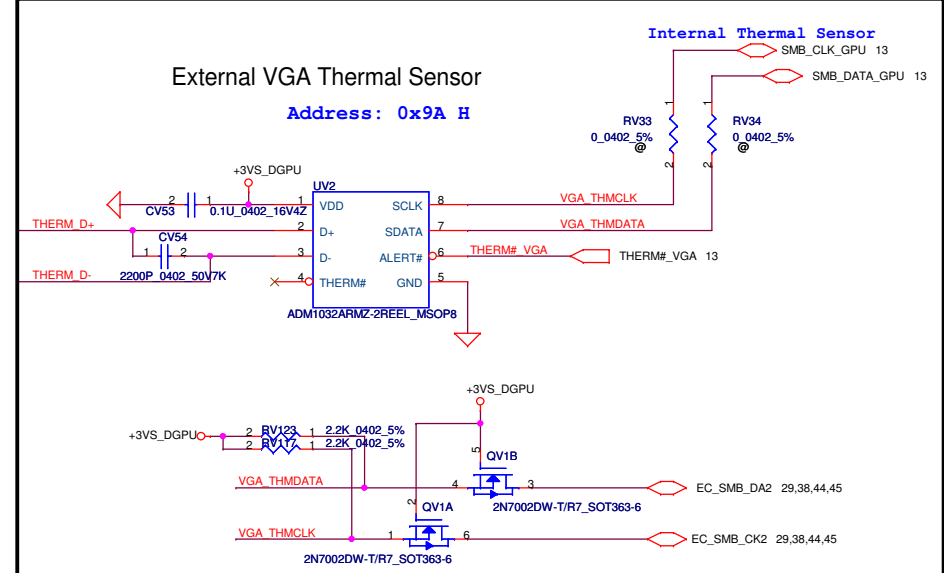
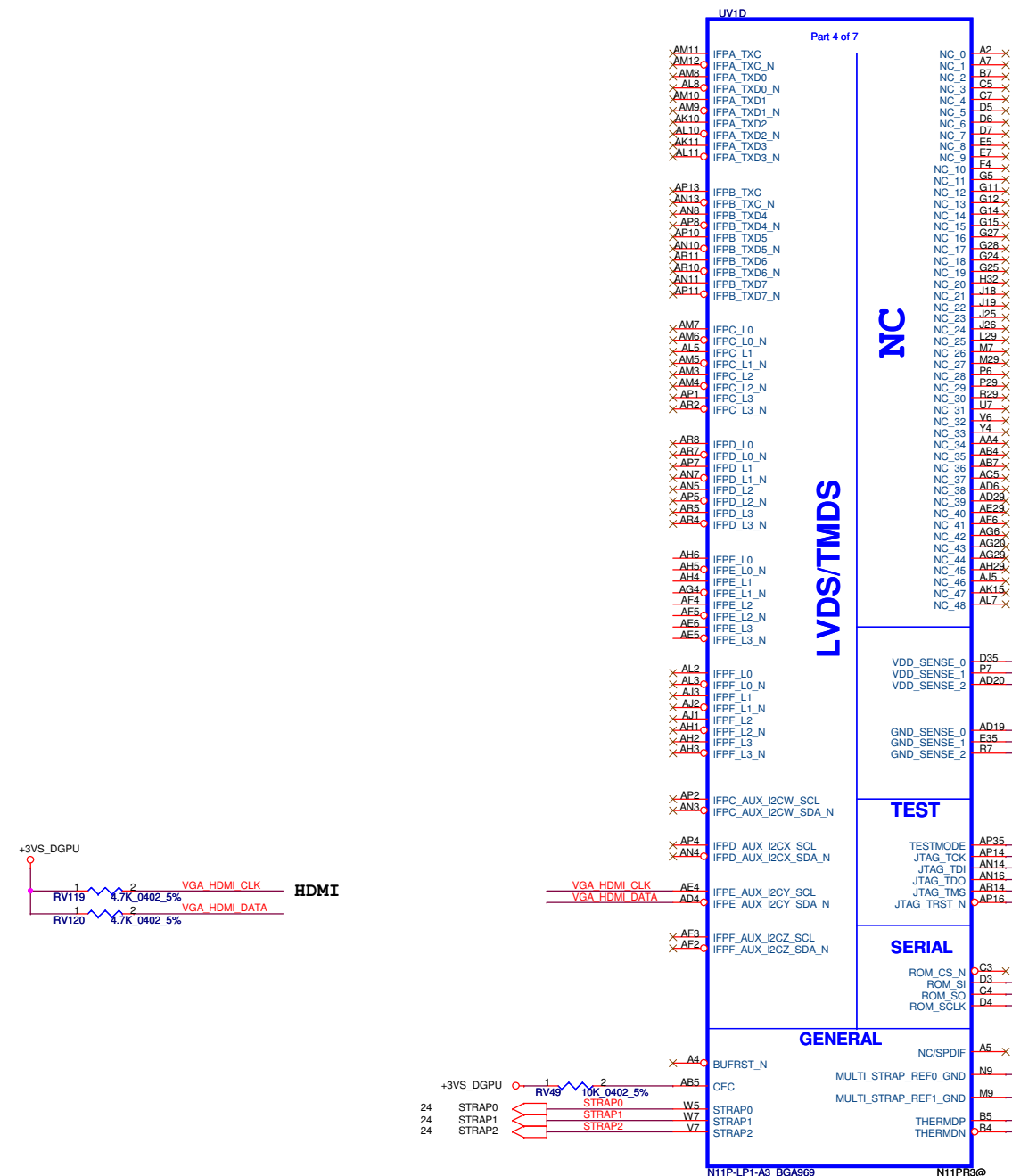


Part 1 of 7

GPIO	K1	X	GPIO0	N1	X
	K2	X	GPIO1	P4	X
	K5	X	GPIO2	P1	X
	K3	X	GPIO3	M2	X
	H2	X	GPIO4	P3	X
	H1	X	GPIO5	T2	X
	H4	X	GPIO6	M10	X
	H5	X	GPIO7	T1	X
	H6	X	GPIO8	M10A	X
	J7	X	GPIO9	M10B	X
	K5	X	GPIO10	M10C	X
	H7	X	GPIO11	M10D	X
	J4	X	GPIO12	M10E	X
	J6	X	GPIO13	M10F	X
	L2	X	GPIO14	M10G	X
	M4	X	GPIO15	M10H	X
	L4	X	GPIO16	M10I	X
	M4	X	GPIO17	M10J	X
	L5	X	GPIO18	M10K	X
	K6	X	GPIO19	M10L	X
	L6	X	GPIO20	M10M	X
	M6	X	GPIO21	M10N	X
	L6	X	GPIO22	M10O	X
	M6	X	GPIO23	M10P	X
			MIOA_D0	N1	X
			MIOA_D1	P4	X
			MIOA_D2	P1	X
			MIOA_D3	M2	X
			MIOA_D4	P3	X
			MIOA_D5	T2	X
			MIOA_D6	M10	X
			MIOA_D7	T1	X
			MIOA_D8	M10A	X
			MIOA_D9	M10B	X
			MIOA_D10	M10C	X
			MIOA_D11	M10D	X
			MIOA_D12	M10E	X
			MIOA_D13	M10F	X
			MIOA_D14	M10G	X
			MIOB_D0	Y1	X
			MIOB_D1	Y2	X
			MIOB_D2	AB3	X
			MIOB_D3	AB2	X
			MIOB_D4	AB1	X
			MIOB_D5	AC4	X
			MIOB_D6	AC1	X
			MIOB_D7	AC2	X
			MIOB_D8	AC3	X
			MIOB_D9	AE3	X
			MIOB_D10	AE2	X
			MIOB_D11	U6	X
			MIOB_D12	W6	X
			MIOB_D13	W6	X
			MIOB_D14	Y6	X
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			MIOA_VSYNCN	L3	X
			MIOB_HSVCN	W1	X
			MIOB_VSYNCN	W2	X
			MIOA_DE	N2	X
			MIOA_VREF	P5	X
			MIOB_DE	W3	X
			MIOB_VREF	AE1	X
			MIOA_CLKIN	N4	X
			MIOA_CLKOUT	R4	X
			MIOB_CLKIN	AE1	X
			MIOB_CLKOUT	V4	X
			MIOA_CLKOUT_N	T4	X
			MIOB_CLKOUT_N	W4	X
			MIOACAL_PD_VDDO	U5	X
			MIOACAL_PU_GND	T5	X
			MIOBCAL_PD_VDDO	AA7	X
			MIOBCAL_PU_GND	AA6	X
			DACA_RED	AM15	X
			DACA_GREEN	AM14	X
			DACA_BLUE	AL14	X
			DACA_HSVCN	AM13	X
			DACA_VSYNC	AL13	X
			DACA_VDD	AK12	X
			DACA_VREF	AK12	X
			DACA_RSET	AK13	X
			DACA_VDD	AK12	X
			DACA_VREF	AK12	X
			DACA_RSET	AK13	X
			DACB_RED	AK4	X
			DACB_GREEN	AL4	X
			DACB_BLUE	AL4	X
			DACB_HSVCN	AM1	X
			DACB_VSYNC	AM2	X
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			DACB_RSET	AH2	X

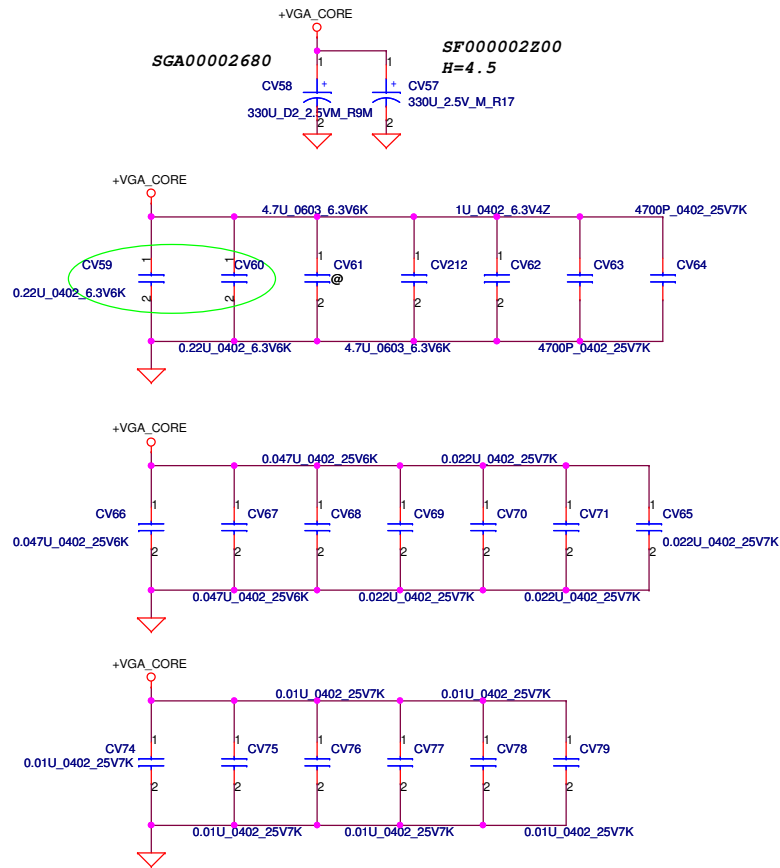
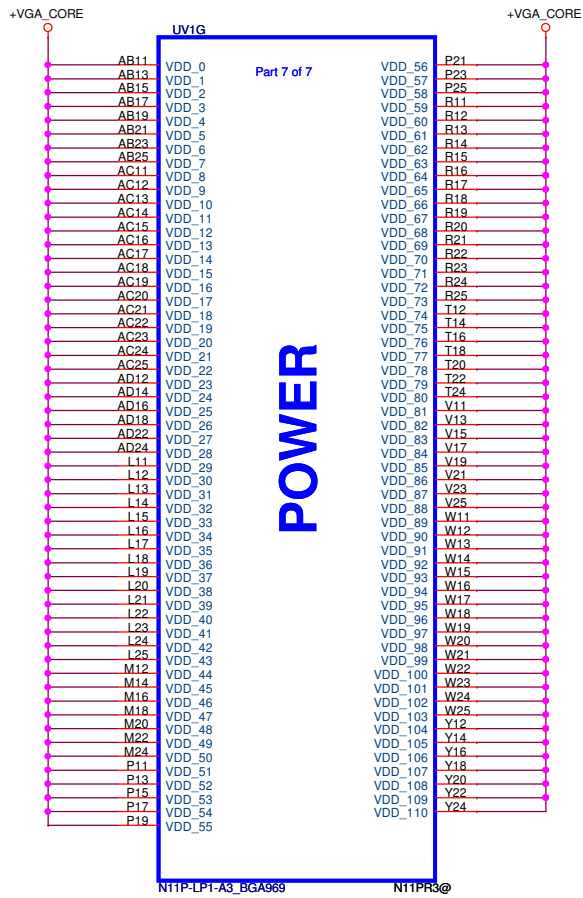


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Date	Monday, March 22, 2010	Sheet	13	of	61	



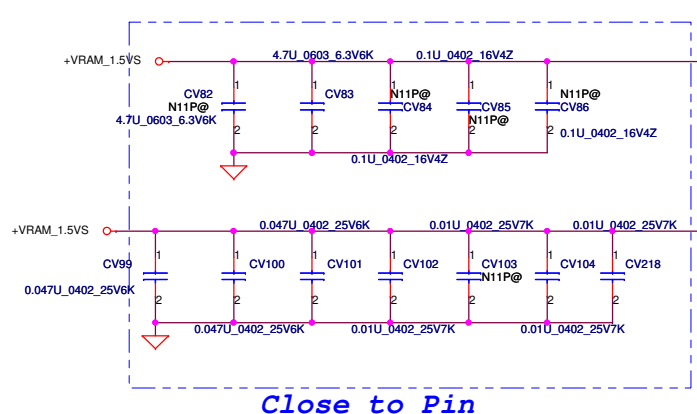
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Compal Electronics, Inc.			
LVDS/HDMI/DP/THM			
Size	Document Number	Rev	
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Date:	Monday, March 22, 2010	Sheet	14 of 61

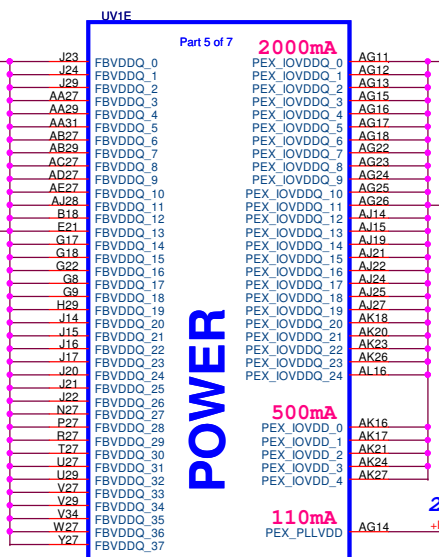


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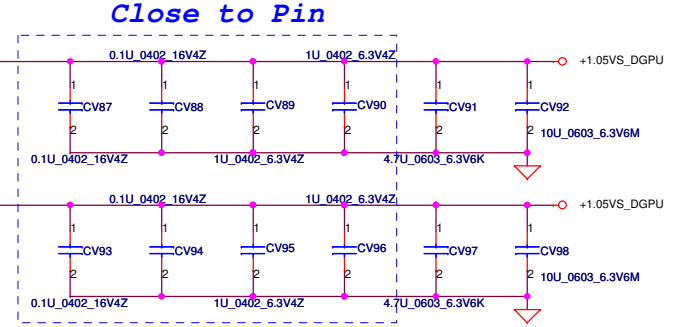
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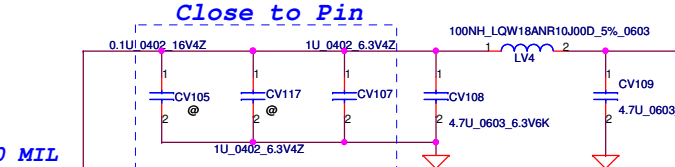
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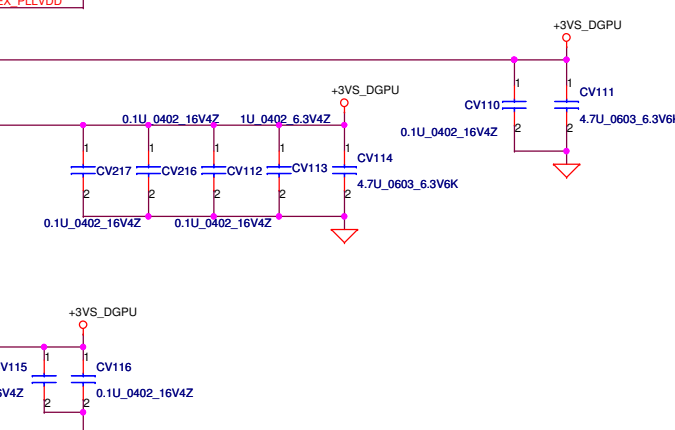
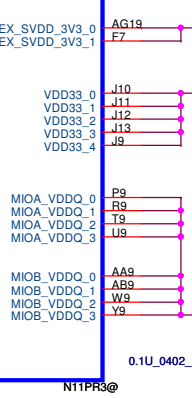
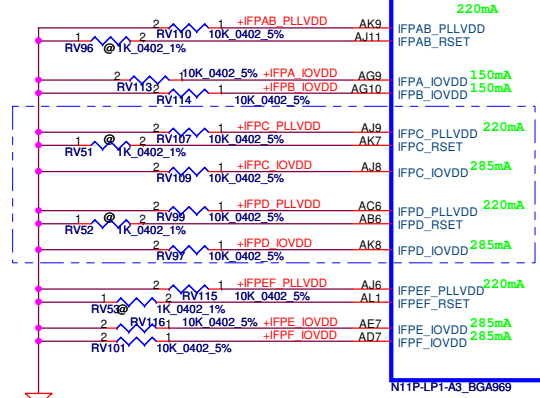
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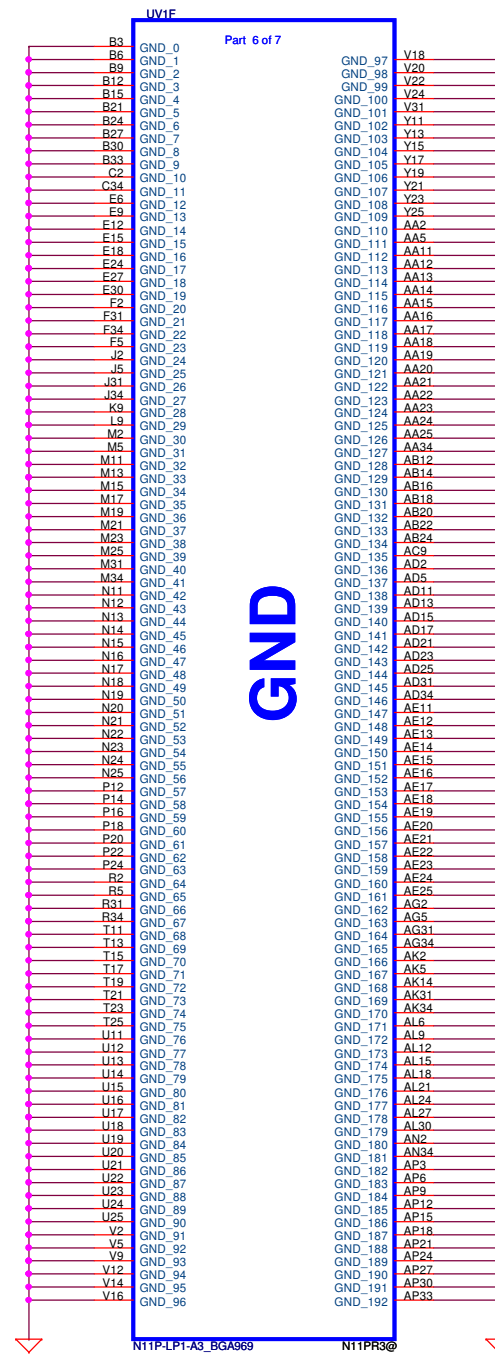
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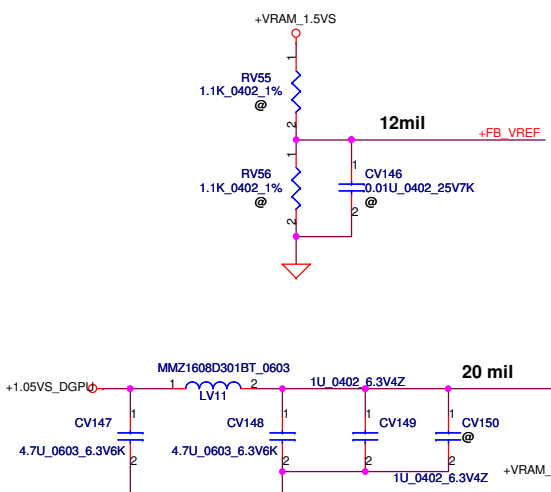
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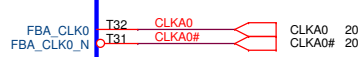
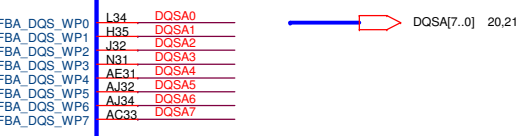
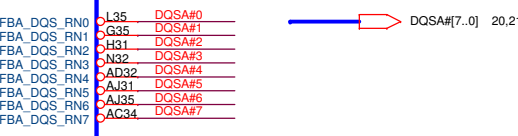
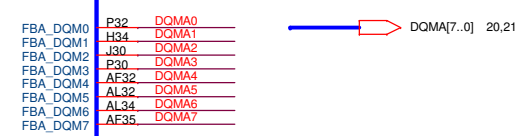
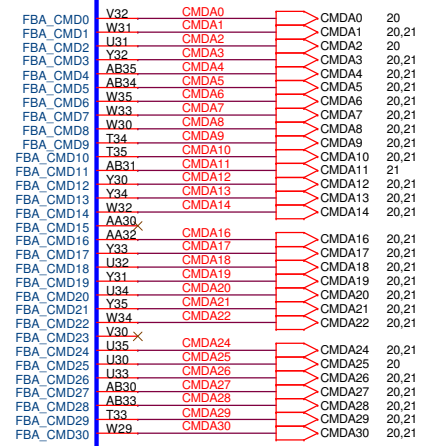
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20,21 MDA[0..63] ← MDA[0..63]



- Part 2 of 7
- MDA0 L32 FBA\_D0
  - MDA1 N33 FBA\_D1
  - MDA2 L33 FBA\_D2
  - MDA3 N34 FBA\_D3
  - MDA4 N35 FBA\_D4
  - MDA5 P35 FBA\_D5
  - MDA6 P33 FBA\_D6
  - MDA7 P34 FBA\_D7
  - MDA8 K35 FBA\_D8
  - MDA9 K33 FBA\_D9
  - MDA10 K34 FBA\_D10
  - MDA11 H33 FBA\_D11
  - MDA12 G34 FBA\_D12
  - MDA13 G33 FBA\_D13
  - MDA14 E34 FBA\_D14
  - MDA15 E33 FBA\_D15
  - MDA16 G31 FBA\_D16
  - MDA17 F30 FBA\_D17
  - MDA18 G30 FBA\_D18
  - MDA19 G32 FBA\_D19
  - MDA20 K30 FBA\_D20
  - MDA21 K32 FBA\_D21
  - MDA22 H30 FBA\_D22
  - MDA23 K31 FBA\_D23
  - MDA24 L31 FBA\_D24
  - MDA25 L30 FBA\_D25
  - MDA26 M32 FBA\_D26
  - MDA27 N30 FBA\_D27
  - MDA28 N30 FBA\_D28
  - MDA29 P31 FBA\_D29
  - MDA30 R32 FBA\_D30
  - MDA31 R30 FBA\_D31
  - MDA32 AG30 FBA\_D32
  - MDA33 AG32 FBA\_D33
  - MDA34 AH31 FBA\_D34
  - MDA35 AF31 FBA\_D35
  - MDA36 AF30 FBA\_D36
  - MDA37 AE30 FBA\_D37
  - MDA38 AC32 FBA\_D38
  - MDA39 AD30 FBA\_D39
  - MDA40 AN33 FBA\_D40
  - MDA41 AL31 FBA\_D41
  - MDA42 AL33 FBA\_D42
  - MDA43 AK30 FBA\_D43
  - MDA44 AK30 FBA\_D44
  - MDA45 AK32 FBA\_D45
  - MDA46 AJ30 FBA\_D46
  - MDA47 AH30 FBA\_D47
  - MDA48 AH33 FBA\_D48
  - MDA49 AH35 FBA\_D49
  - MDA50 AH34 FBA\_D50
  - MDA51 AH32 FBA\_D51
  - MDA52 AJ33 FBA\_D52
  - MDA53 AL35 FBA\_D53
  - MDA54 AM34 FBA\_D54
  - MDA55 AM35 FBA\_D55
  - MDA56 AF33 FBA\_D56
  - MDA57 AE32 FBA\_D57
  - MDA58 AF34 FBA\_D58
  - MDA59 AE35 FBA\_D59
  - MDA60 AE34 FBA\_D60
  - MDA61 AE33 FBA\_D61
  - MDA62 AB32 FBA\_D62
  - MDA63 AC35 FBA\_D63

MEMORY INTERFACE A



Mode C - Mirror Mode Mapping

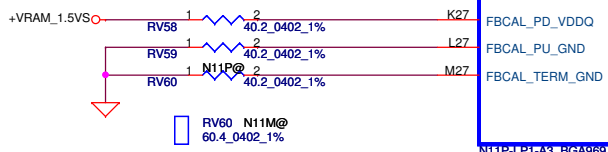
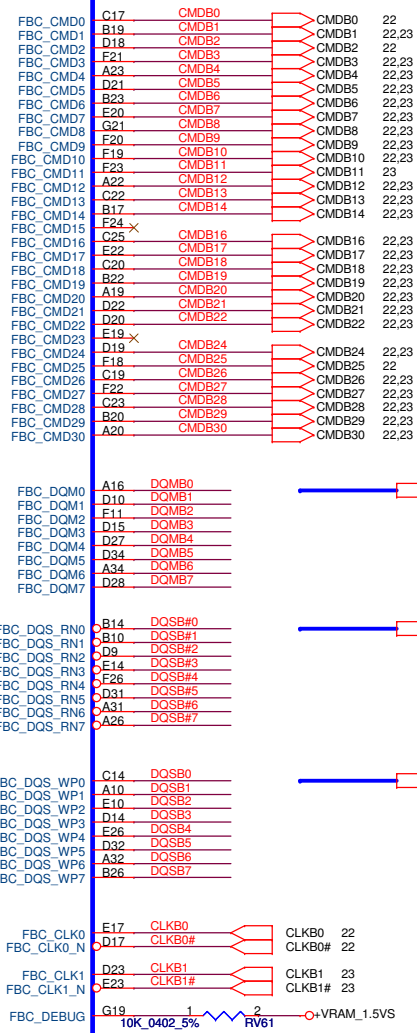
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CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

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				Date:	Monday, March 22, 2010
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22.23 MDB[0..63] ← MDB[0..63]

- UVIC
- Part 3 of 7
- MDB0 B13 FBC\_D0
  - MDB1 D13 FBC\_D1
  - MDB2 A13 FBC\_D2
  - MDB3 C16 FBC\_D3
  - MDB4 C16 FBC\_D4
  - MDB5 B16 FBC\_D5
  - MDB6 A17 FBC\_D6
  - MDB7 D16 FBC\_D7
  - MDB8 C13 FBC\_D8
  - MDB9 B11 FBC\_D9
  - MDB10 C11 FBC\_D10
  - MDB11 A11 FBC\_D11
  - MDB12 C10 FBC\_D12
  - MDB13 C8 FBC\_D13
  - MDB14 B8 FBC\_D14
  - MDB15 A8 FBC\_D15
  - MDB16 E8 FBC\_D16
  - MDB17 F8 FBC\_D17
  - MDB18 F10 FBC\_D18
  - MDB19 F12 FBC\_D19
  - MDB21 D8 FBC\_D20
  - MDB22 D11 FBC\_D21
  - MDB23 E11 FBC\_D22
  - MDB24 D12 FBC\_D23
  - MDB25 E13 FBC\_D24
  - MDB26 F13 FBC\_D25
  - MDB27 F14 FBC\_D26
  - MDB28 F15 FBC\_D27
  - MDB29 E16 FBC\_D28
  - MDB30 F16 FBC\_D29
  - MDB31 F17 FBC\_D30
  - MDB32 D29 FBC\_D31
  - MDB33 F27 FBC\_D32
  - MDB34 F28 FBC\_D33
  - MDB35 E28 FBC\_D34
  - MDB36 D26 FBC\_D35
  - MDB37 F25 FBC\_D36
  - MDB38 D24 FBC\_D37
  - MDB39 E25 FBC\_D38
  - MDB40 E32 FBC\_D39
  - MDB41 F32 FBC\_D40
  - MDB42 D33 FBC\_D41
  - MDB43 E31 FBC\_D42
  - MDB44 C33 FBC\_D43
  - MDB45 F29 FBC\_D44
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  - MDB50 C29 FBC\_D49
  - MDB51 B31 FBC\_D50
  - MDB52 C32 FBC\_D51
  - MDB53 B32 FBC\_D52
  - MDB54 B35 FBC\_D53
  - MDB55 B34 FBC\_D54
  - MDB56 A29 FBC\_D55
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  - MDB58 A28 FBC\_D57
  - MDB59 C28 FBC\_D58
  - MDB60 C26 FBC\_D59
  - MDB61 D25 FBC\_D60
  - MDB62 B25 FBC\_D61
  - MDB63 A25 FBC\_D62

MEMORY INTERFACE C



### Mode C - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

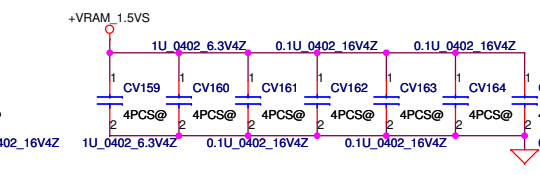
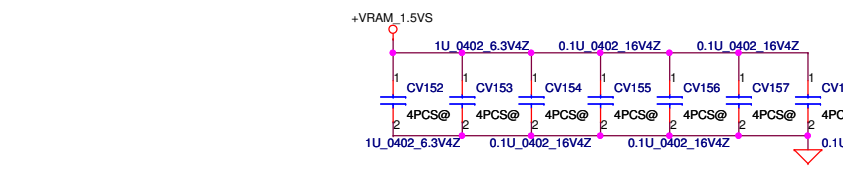
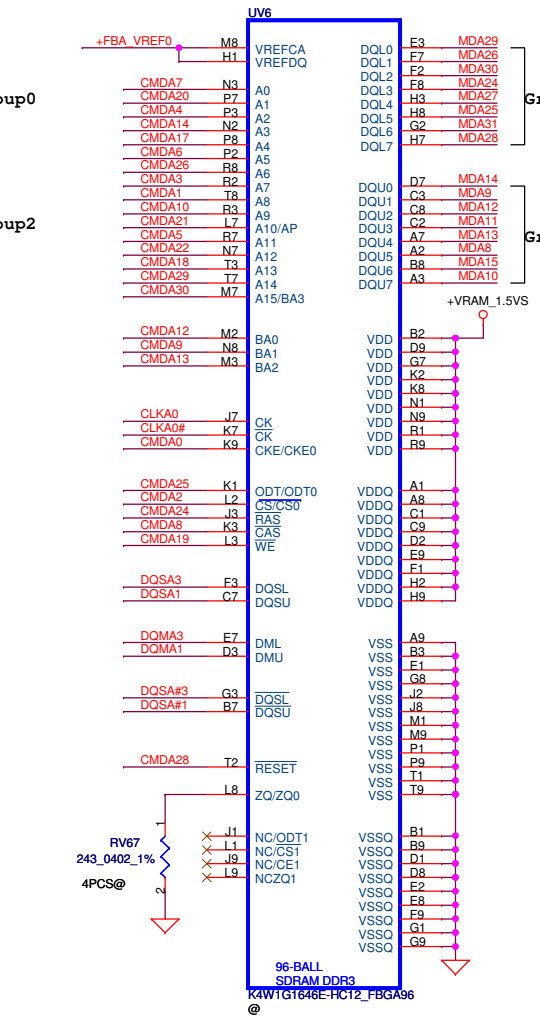
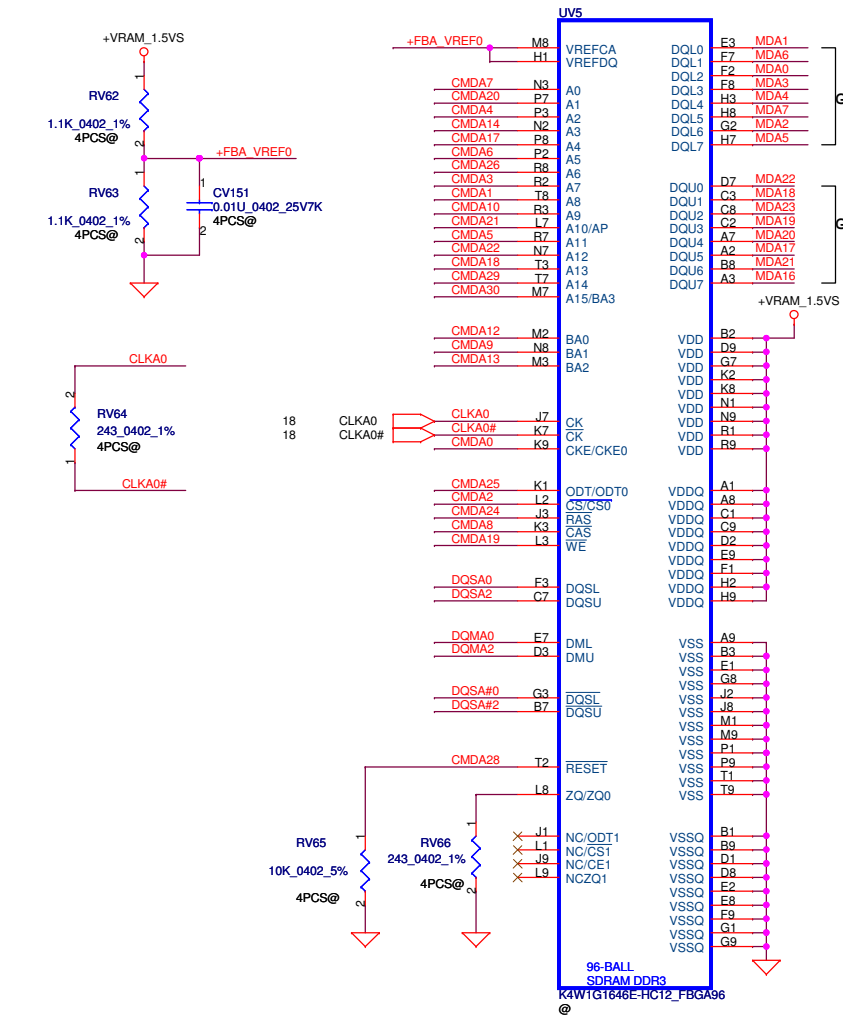
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# Memory Partition A - Lower 32 bits



## Mode C - Mirror Mode Mapping

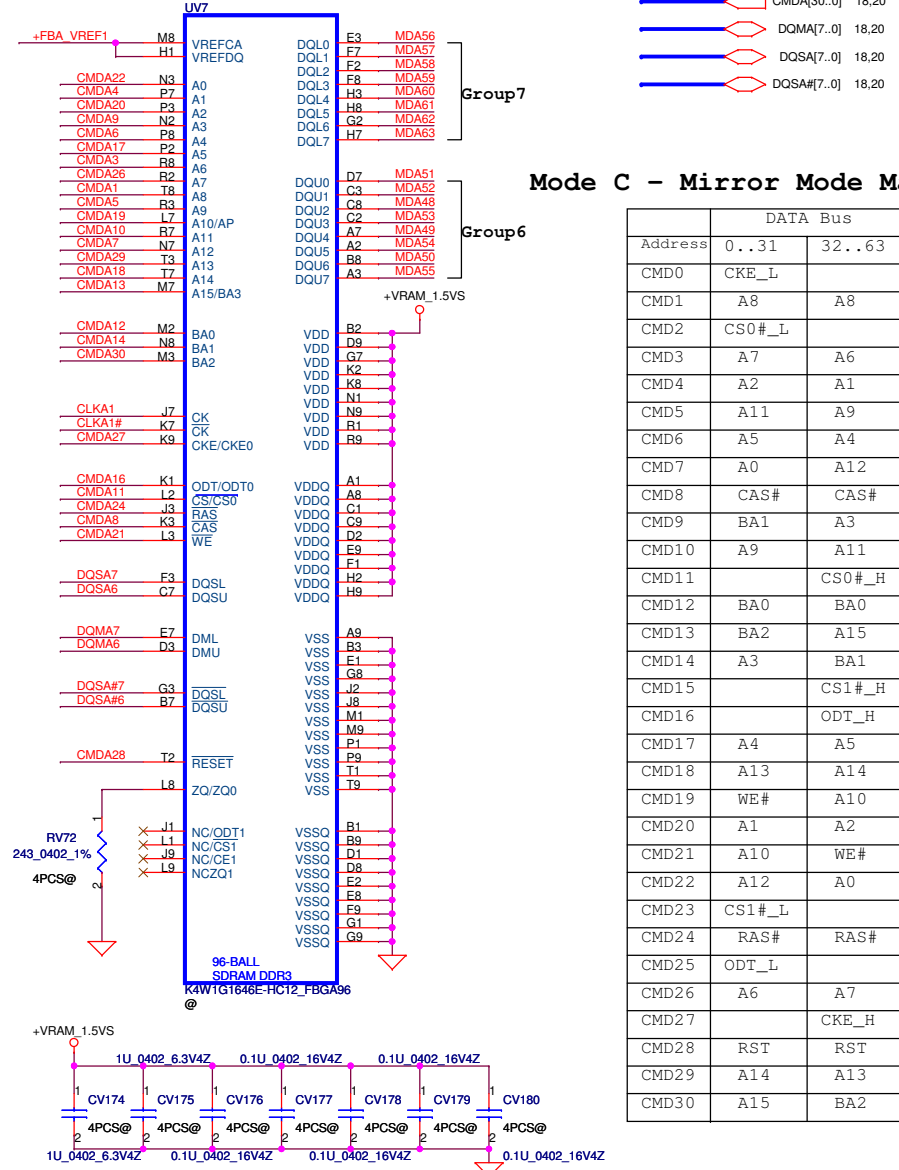
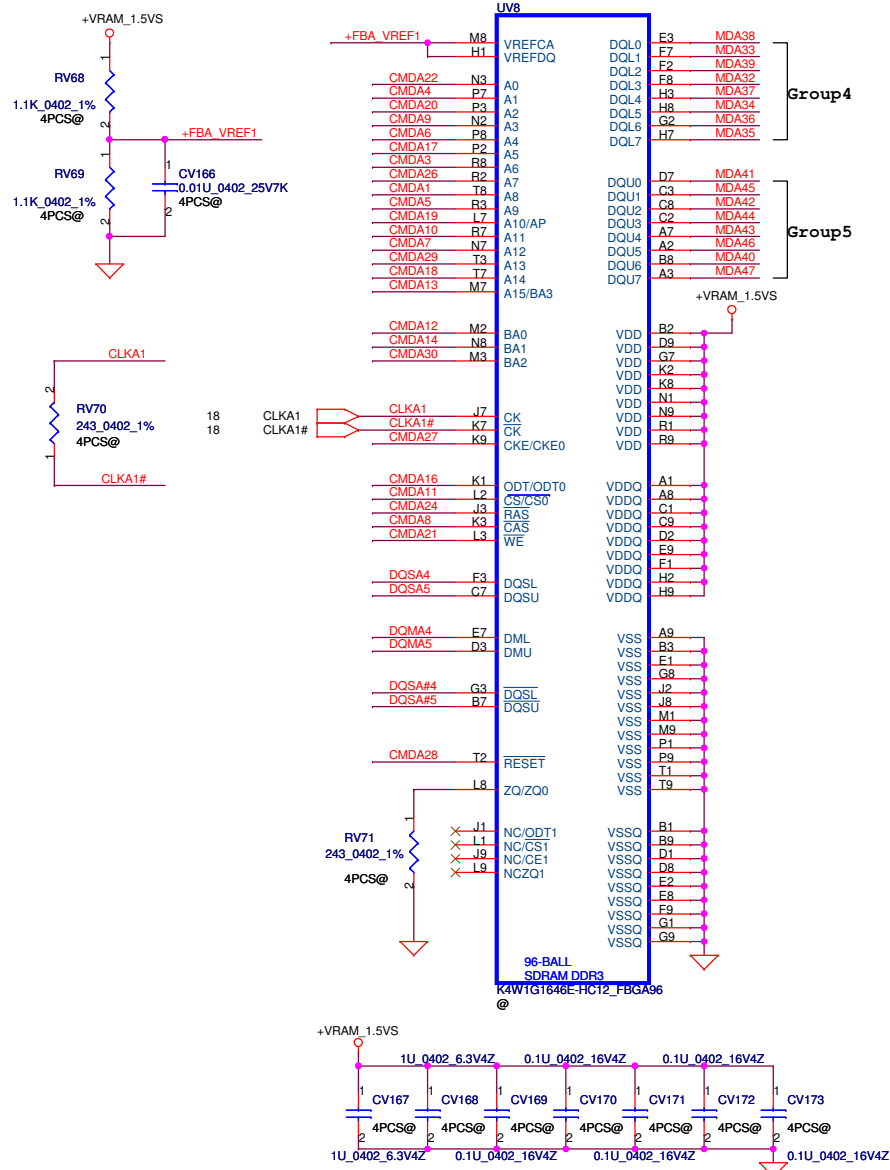
Address	DATA Bus	
	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2



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<b>Compal Electronics, Inc.</b>			
<b>VRAM A Lower</b>			
Size	Document Number	Rev 1.0	
	<b>NBQA LA6072P M/B</b>		
Date:	Monday, March 22, 2010	Sheet	20 of 61

# Memory Partition A - Upper 32 bits



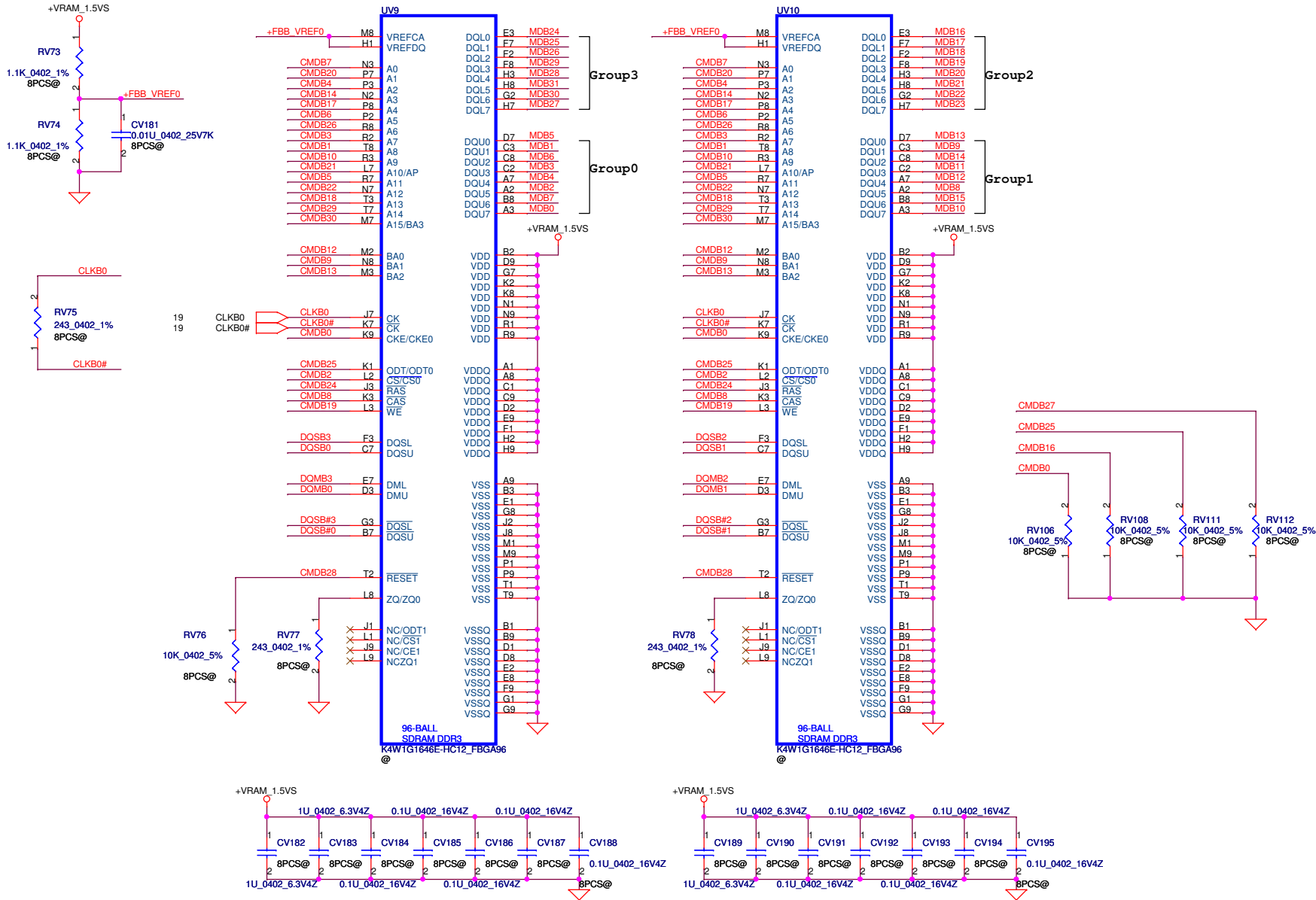
- MDA[0..63] 18,20
- CMDA[30..0] 18,20
- DQMA[7..0] 18,20
- DQSA[7..0] 18,20
- DQSA# [7..0] 18,20

## Mode C - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD0	CKE_L	A8
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

Security Classification		Compal Secret Data		Title	
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				NBQAA LA6072P M/B	
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# Memory Partition C - Lower 32 bits

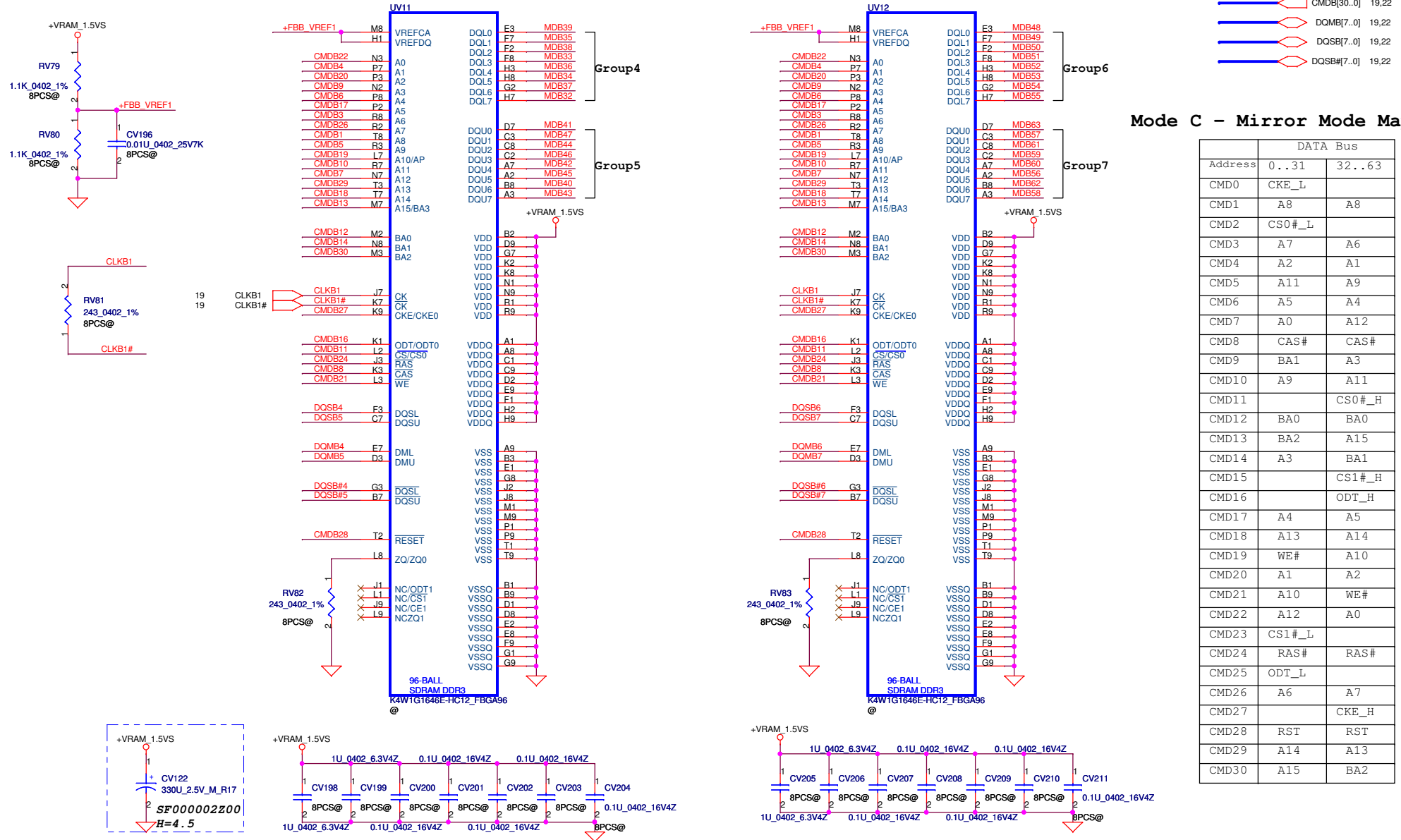


## Mode C - Mirror Mode Mapping

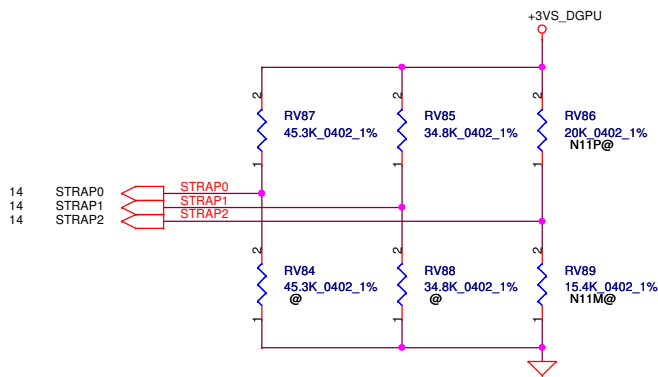
Address	DATA Bus	
	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>VRAM C Lower</b>	
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# Memory Partition C - Upper 32 bits

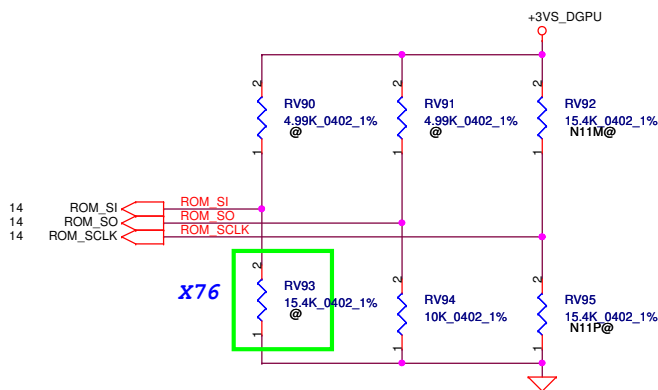


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### Device ID straps

	DeviceID	PCI_DEVID[4..0]	ROM_SCLK	STRAP2
N11P-LP1	0xA2B	[01011]	Pull down 15K	Pull up 20K
N11M-GE1	0xA75	[10101]	Pull up 15K	Pull down 30K
N11M-OP1	0xA72	[10010]	Pull up 15K	Pull down 15K



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	VDD33	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	VDD33	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLEN_TERM
ROM_SI	VDD33	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	VDD33	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	VDD33	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	VDD33	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

	VRAM	RAMCFG[3..0]	RV93
DDR3	Hynix H5TQ1G63BFR-12C SA000032400	512MB	0010 PD 15K SD034154280
		1GB	0010 PD 15K SD034154280
64M16	Samsung K4W1G1646E-HC12 SA000035700	512MB	0011 PD 20K SD034200280
		1GB	0011 PD 20K SD034200280
DDR3			
128M16			

Reserved for 128M16

SUB_VENDOR	
0	No VBIOS ROM (Default)
1	BIOS ROM is present

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User [3:0]	1110=EDID
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
1110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

SLOT_CLOCK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

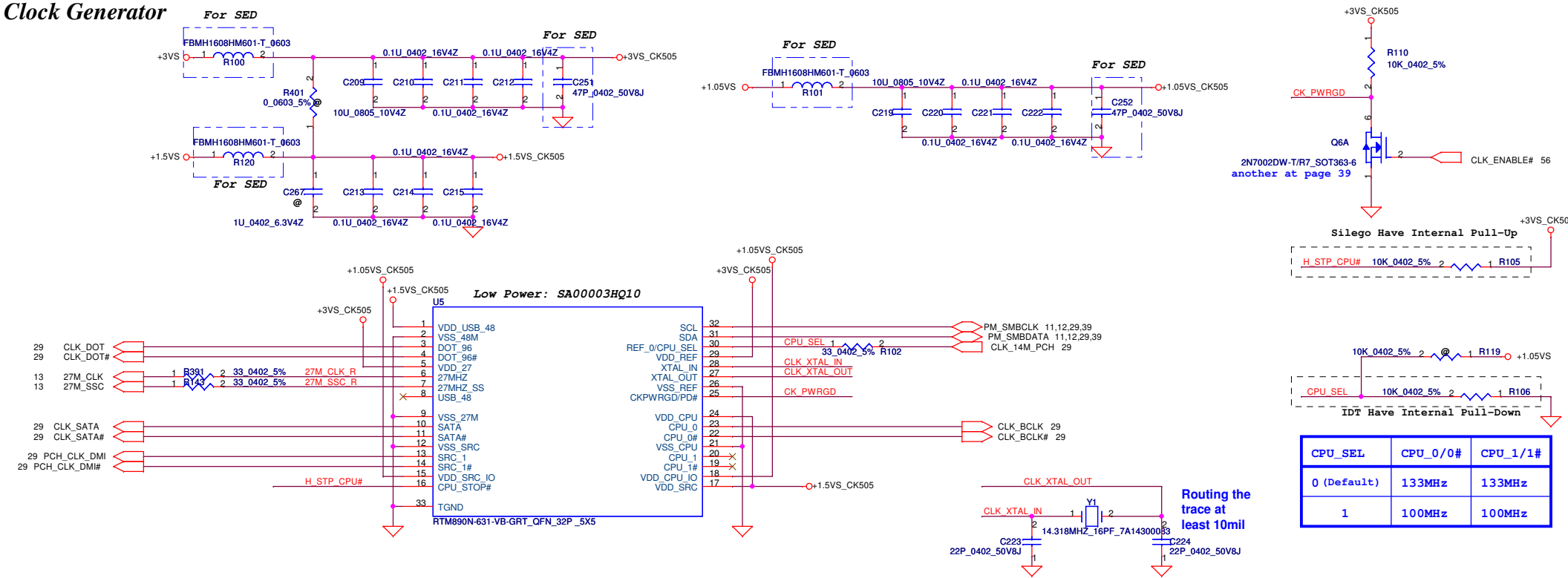
SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

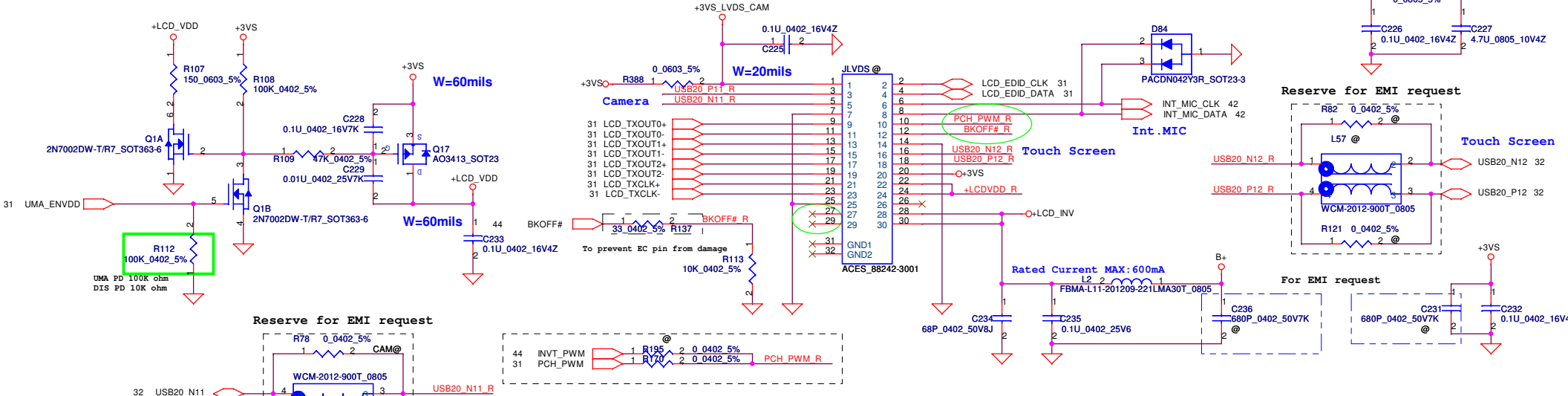
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# Clock Generator

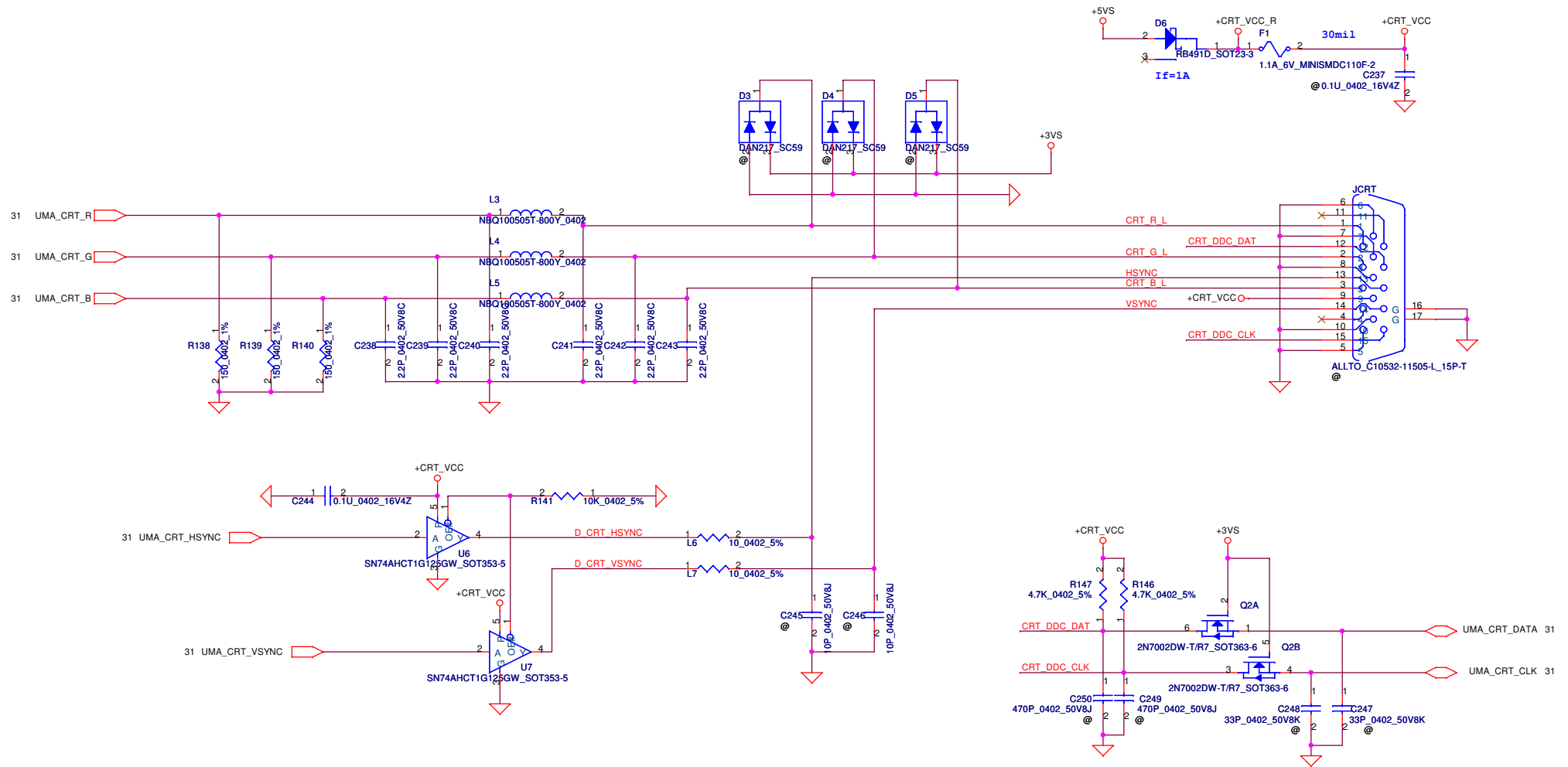


# LVDS / Int.Camera / TouchScreen / Int.MIC Conn



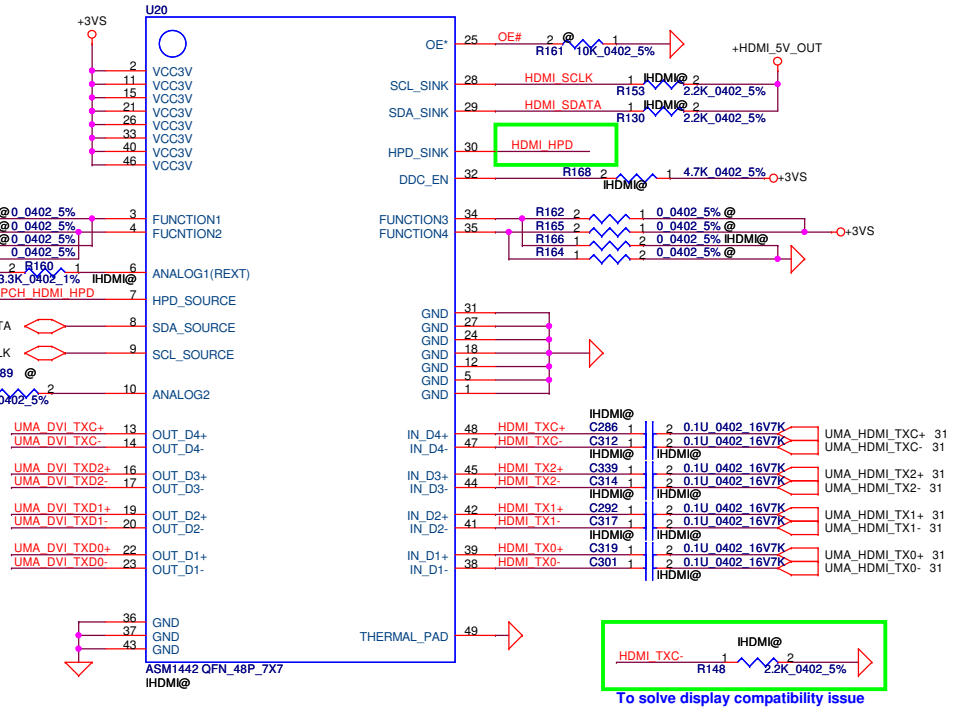
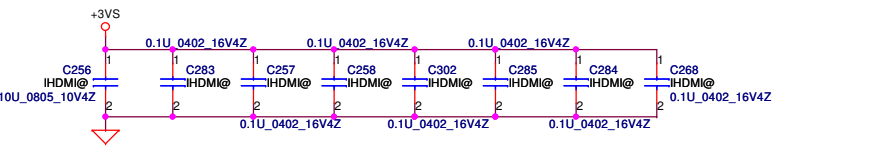
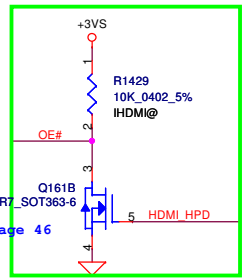
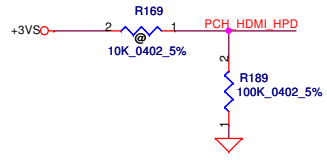
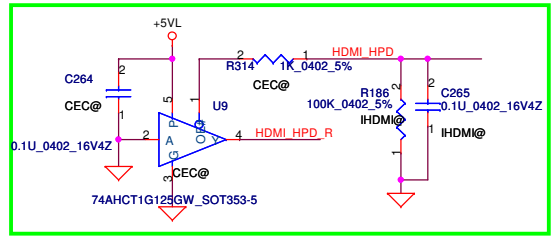
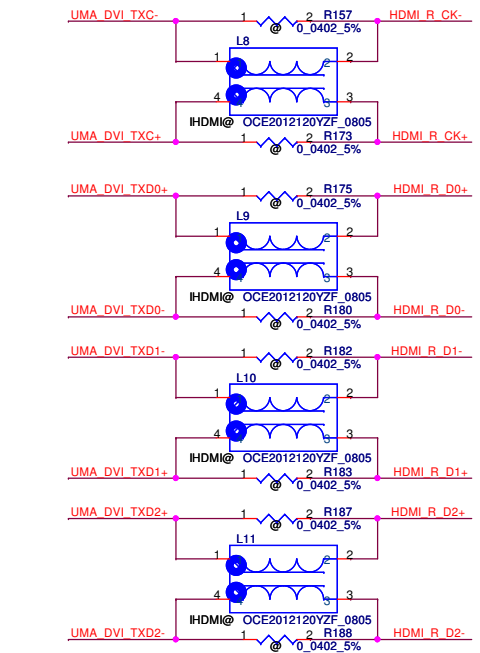
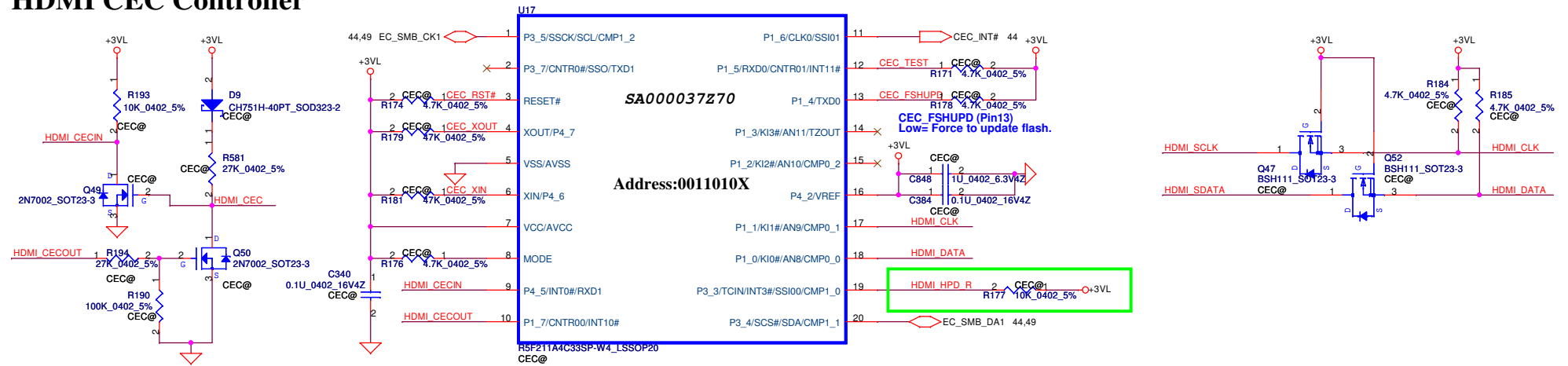
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Size	Document Number	Customer		Rev	
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# CRT CONNECTOR

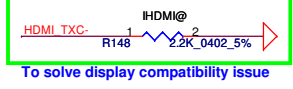
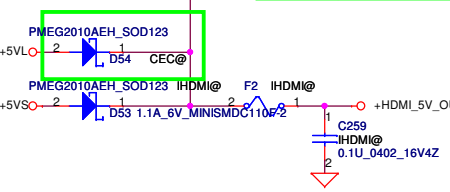
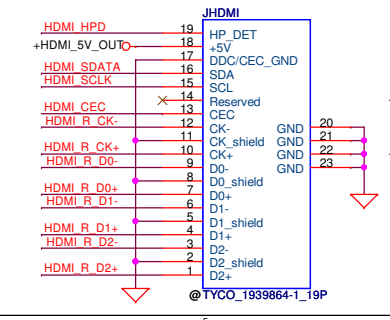


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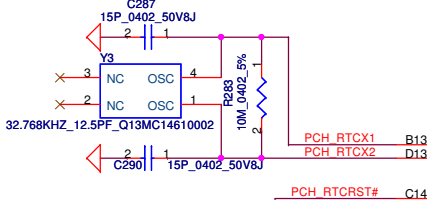
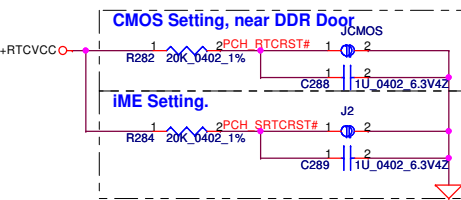
# HDMI CEC Controller



# HDMI Connector



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**Integrated SUS 1.05V VRM Enable**

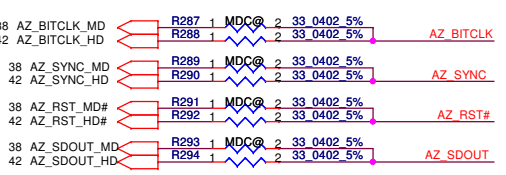
PCH_INTVRMEN	High - Enable Internal VRs (must be always pulled high)
--------------	---

**HDA\_SYNC**  
 This signal has a weak internal pull down.  
 H=>On Die PLL is supplied by 1.5V  
 L=>On Die PLL is supplied by 1.8V

**HDA\_SDO**  
 This signal has a weak internal pull down.  
 This signal can't PU

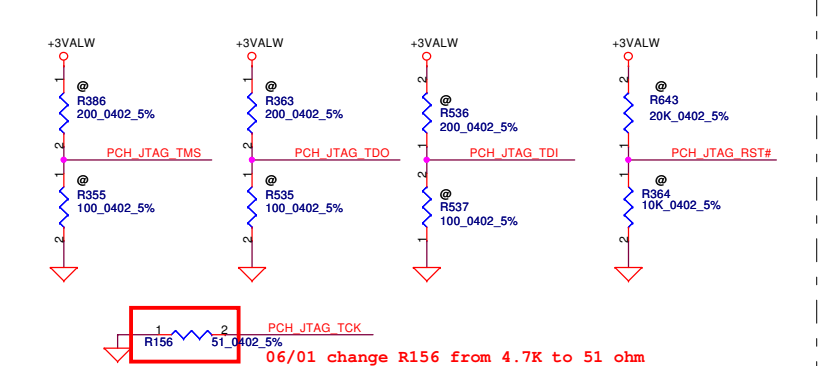
**Flash Descriptor Security Override**

HDA_DOCK_EN#	Low = Enabled High = Disabled *
--------------	------------------------------------

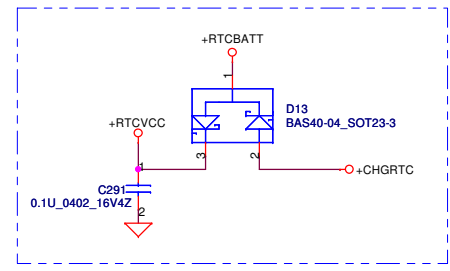
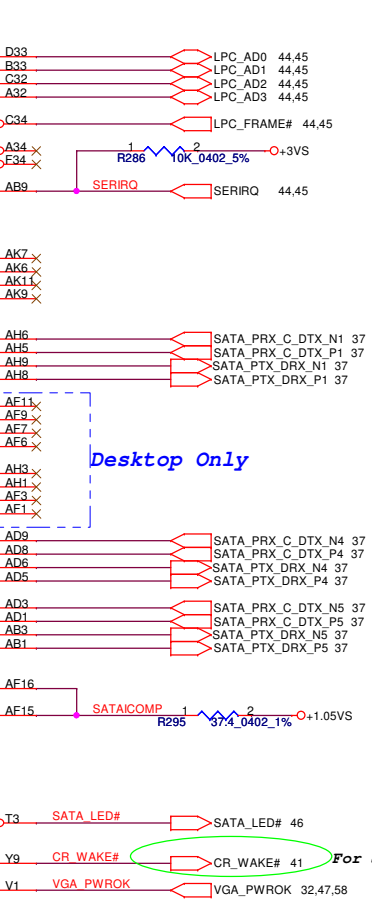
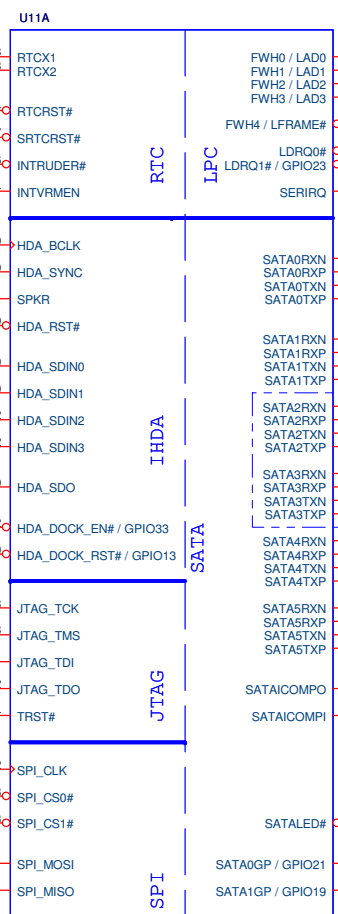
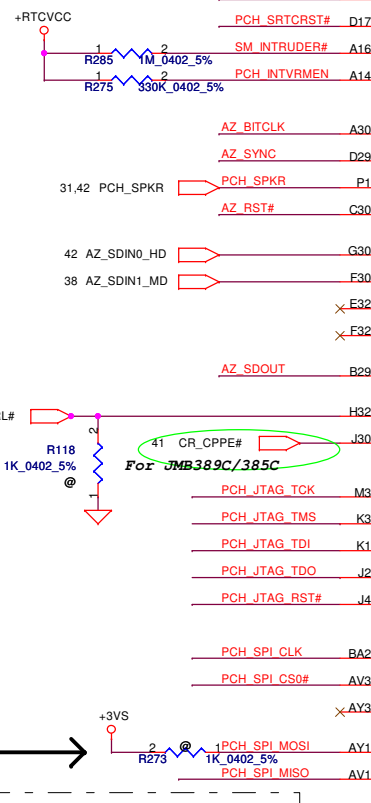


**ITPM Enabled Internal: Pull down 20k**

SPI_MOSI	High = Enabled Low = Disabled (Default)
----------	--



PCH Pin	RefDes	PCH JTAG Enable		PCH JTAG Disable (Default)	
		ES1	ES2	ES1	ES2
PCH_JTAG_TDO	R358	No Install	200ohm	No Install	No Install
PCH_JTAG_TMS	R355	No Install	100ohm	No Install	No Install
PCH_JTAG_TDI	R354	100ohm	100ohm	No Install	No Install
PCH_JTAG_RST#	R536	200ohm	200ohm	20kohm	No Install
PCH_JTAG_TCK	R156	51ohm	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R643	20kohm	20kohm	No Install	No Install
	R353	10kohm	10kohm	No Install	No Install



1ST HDD

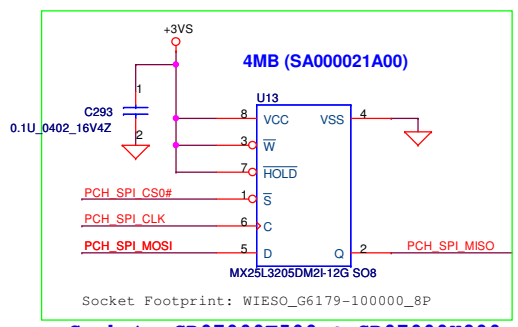
SATA ODD

eSATA

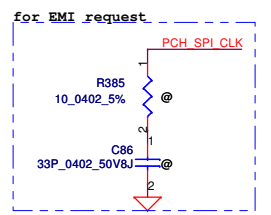
SATA LED#

CR\_WAKE#

VGA\_PWROK



Socket: SP07000F500 & SP07000H900



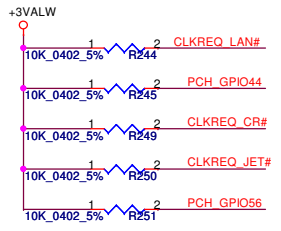
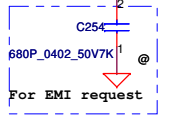
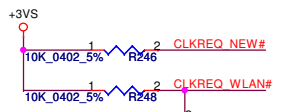
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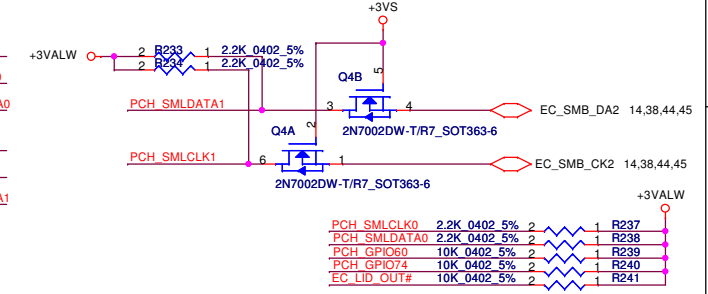
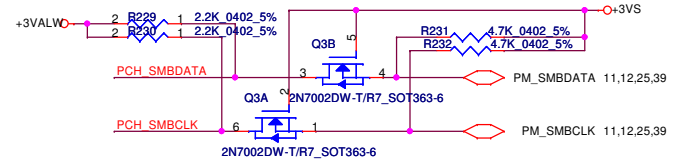
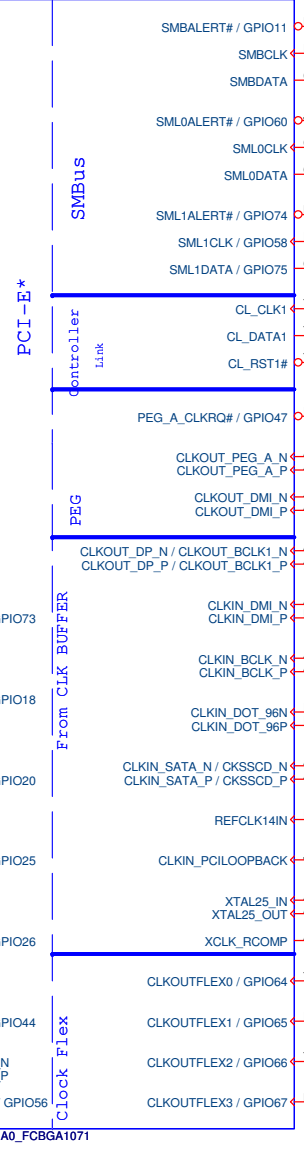
Compal Electronics, Inc.			
<b>PCH-SPI/SATA/LPC/RTC/HDA</b>			
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- LAN**
  - 40 PCIE\_PRX\_C\_LANTX\_N1
  - 40 PCIE\_PRX\_C\_LANTX\_P1
  - 40 PCIE\_PTX\_C\_LANRX\_N1
  - 40 PCIE\_PTX\_C\_LANRX\_P1
- WLAN**
  - 39 PCIE\_PRX\_WLANTX\_N2
  - 39 PCIE\_PRX\_WLANTX\_P2
  - 39 PCIE\_PTX\_C\_WLANRX\_N2
  - 39 PCIE\_PTX\_C\_WLANRX\_P2
- New Card**
  - 39 PCIE\_PRX\_NEWTX\_N3
  - 39 PCIE\_PRX\_NEWTX\_P3
  - 39 PCIE\_PTX\_C\_NEWRX\_N3
  - 39 PCIE\_PTX\_C\_NEWRX\_P3
- JET**
  - 39 PCIE\_PRX\_JETTX\_N4
  - 39 PCIE\_PRX\_JETTX\_P4
  - 39 PCIE\_PTX\_C\_JETRX\_N4
  - 39 PCIE\_PTX\_C\_JETRX\_P4
- Card Reader**
  - 41 PCIE\_PRX\_C\_CRTX\_N5
  - 41 PCIE\_PRX\_C\_CRTX\_P5
  - 41 PCIE\_PTX\_C\_CRRX\_N5
  - 41 PCIE\_PTX\_C\_CRRX\_P5

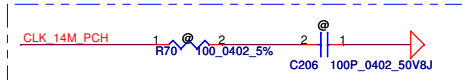
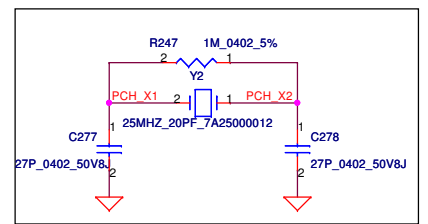
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  - 40 CLK\_LAN#
  - 40 CLK\_LAN
  - 40 CLKREQ\_LAN#
- WLAN**
  - 39 CLK\_WLAN#
  - 39 CLK\_WLAN
  - 39 CLKREQ\_WLAN#
- New Card**
  - 39 CLK\_NEW#
  - 39 CLK\_NEW
  - 39 CLKREQ\_NEW#
- JET**
  - 39 CLK\_JET#
  - 39 CLK\_JET
  - 39 CLKREQ\_JET#
- Card Reader**
  - 41 CLK\_CR#
  - 41 CLK\_CR
  - 41 CLKREQ\_CR#



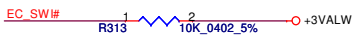
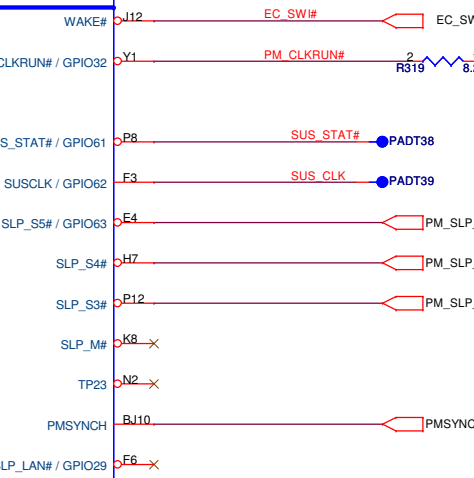
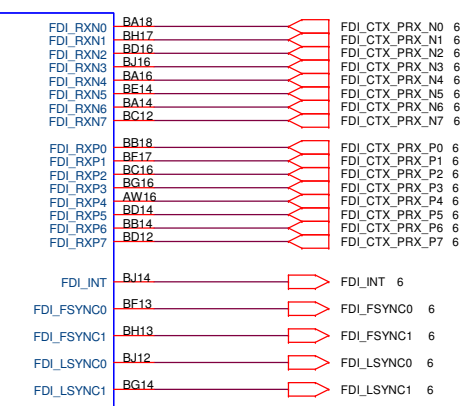
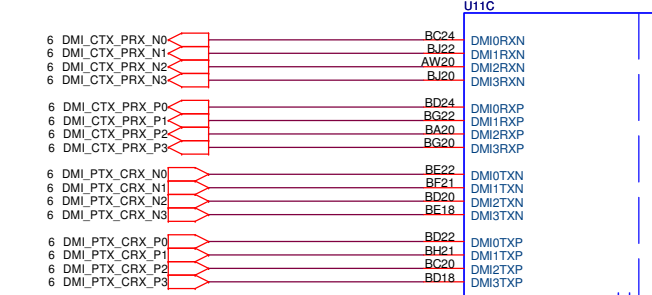
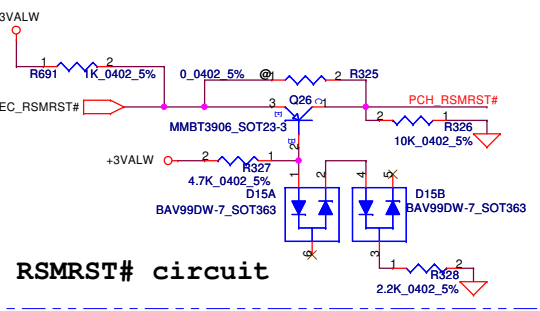
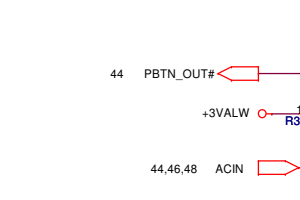
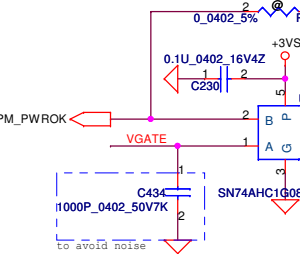
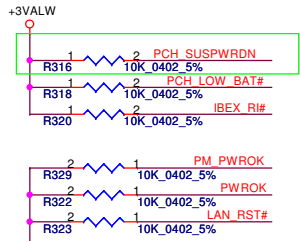
U11B



FROM CLK GEN FOR: 133/100/96/14.318 MHZ

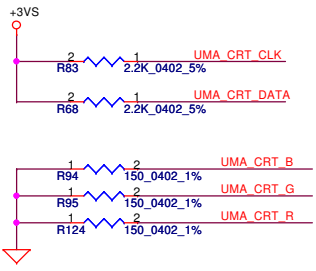
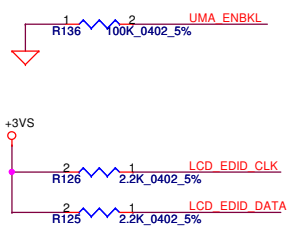


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Size B	Document Number	Rev		1.0	
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Date:	Monday, March 22, 2010	Sheet	29	of	61

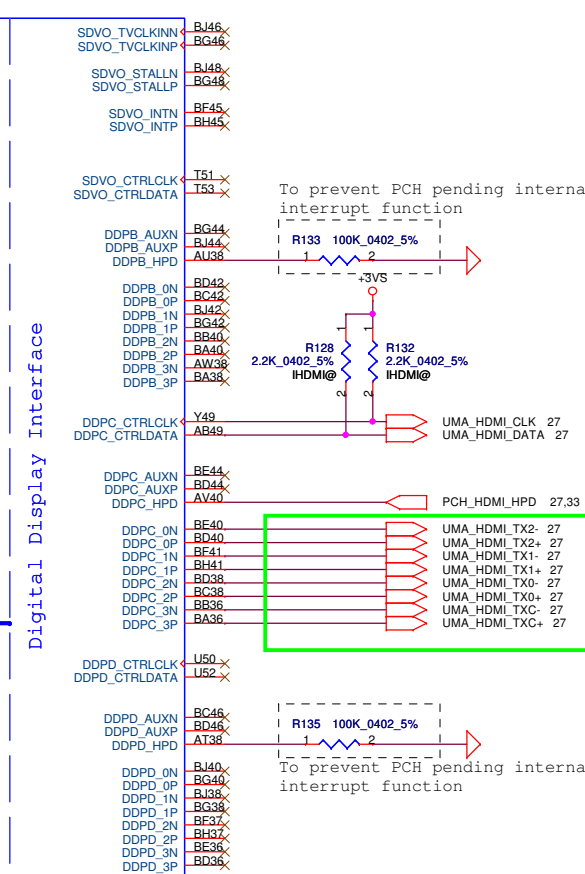
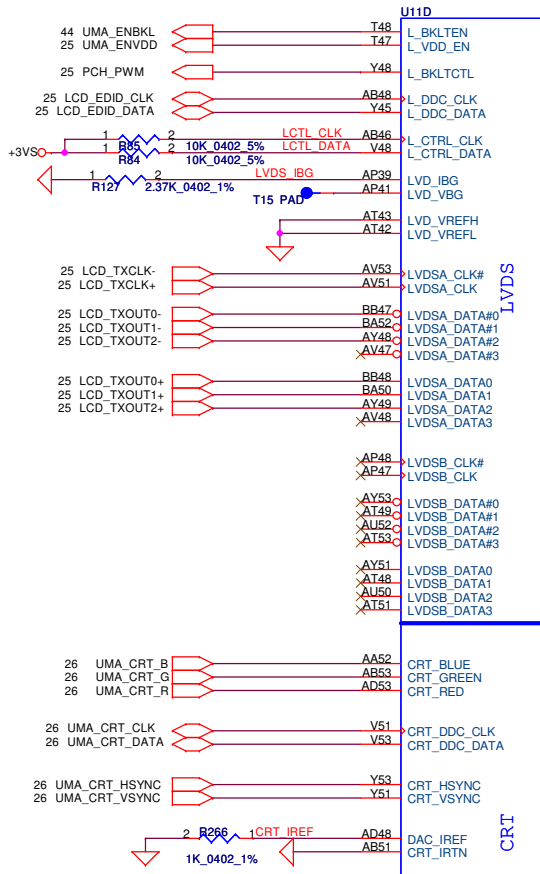
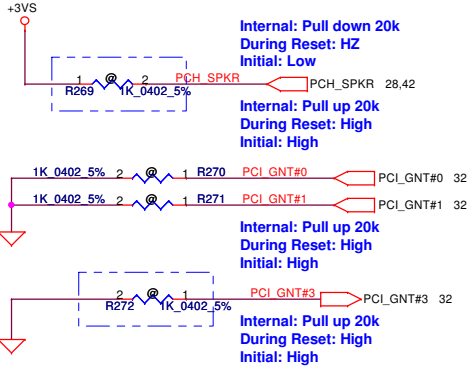


System Power Management

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				PCH-DMI/FDI/PWM	
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				NBQAA LA6072P M/B	
				Date:	Rev
				Tuesday, March 23, 2010	1.0
				Sheet	30 of 61

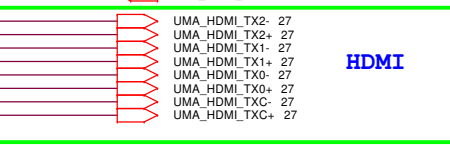


**PCH Strap Pin**



To prevent PCH pending internal HPD interrupt function

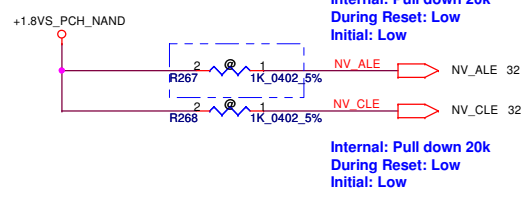
To prevent PCH pending internal HPD interrupt function



NO REBOOT Strap		
PCH_SPKR	Low= Disable	High= Enable

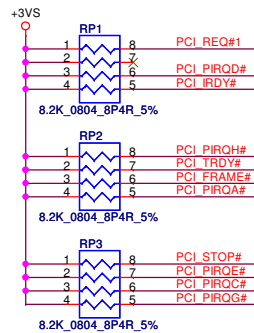
Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC (Default)
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= A16 swap override Disable

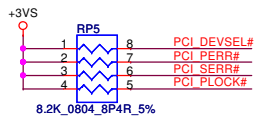
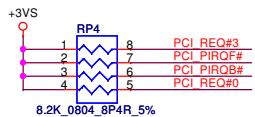


Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled (Default)

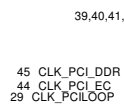
DMI Termination Voltage	
NV_CLE	Low= Set to Vss (Default) High= Set to Vcc



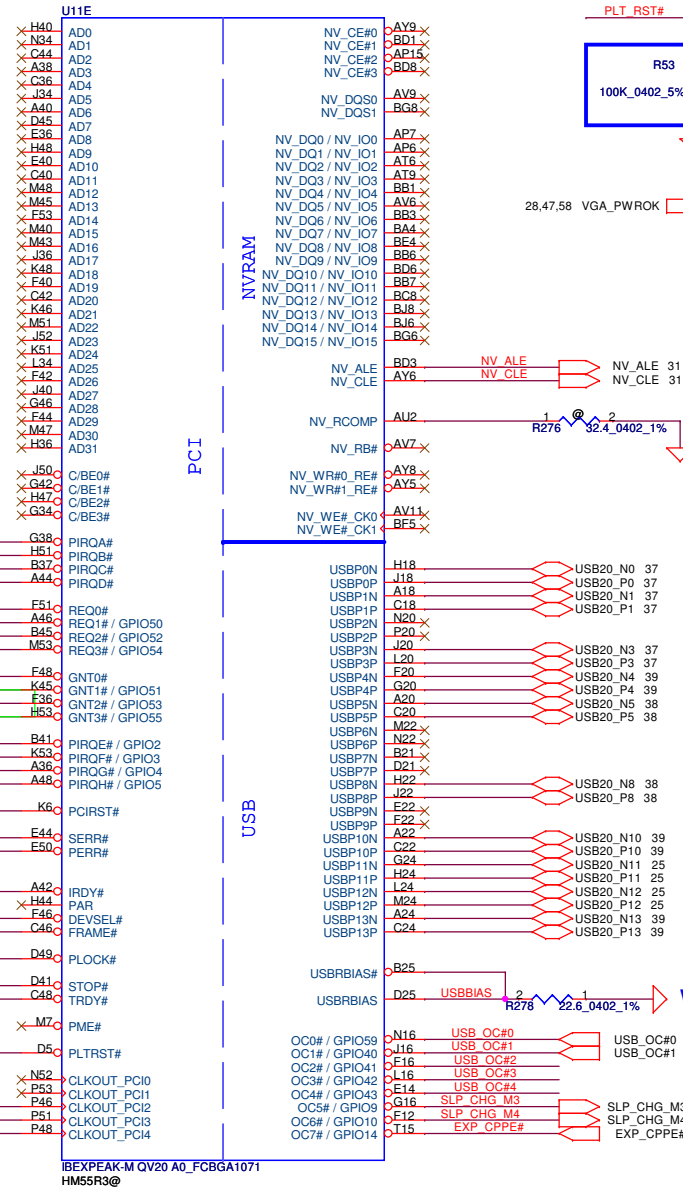
GNT2#/GPIO53: Not pull low, internal pull up 20K



T37 PAD



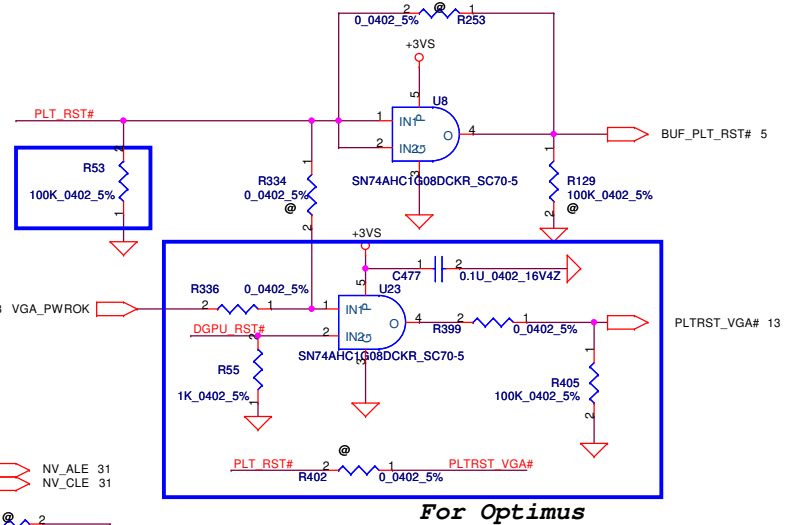
Change to 47 ohm?



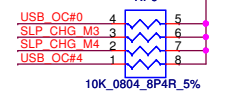
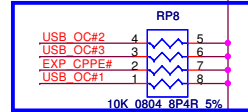
USB-LEFT1  
USB-LEFT2  
eSATA-USB  
NewCard  
BT

Finger Printer  
3G  
Int. Camera  
Touch Screen  
WiMax/WLAN

Within 500 mils



For Optimus



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				Date	Monday, March 22, 2010
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				Rev	1.0

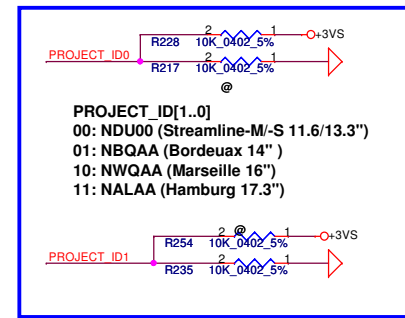
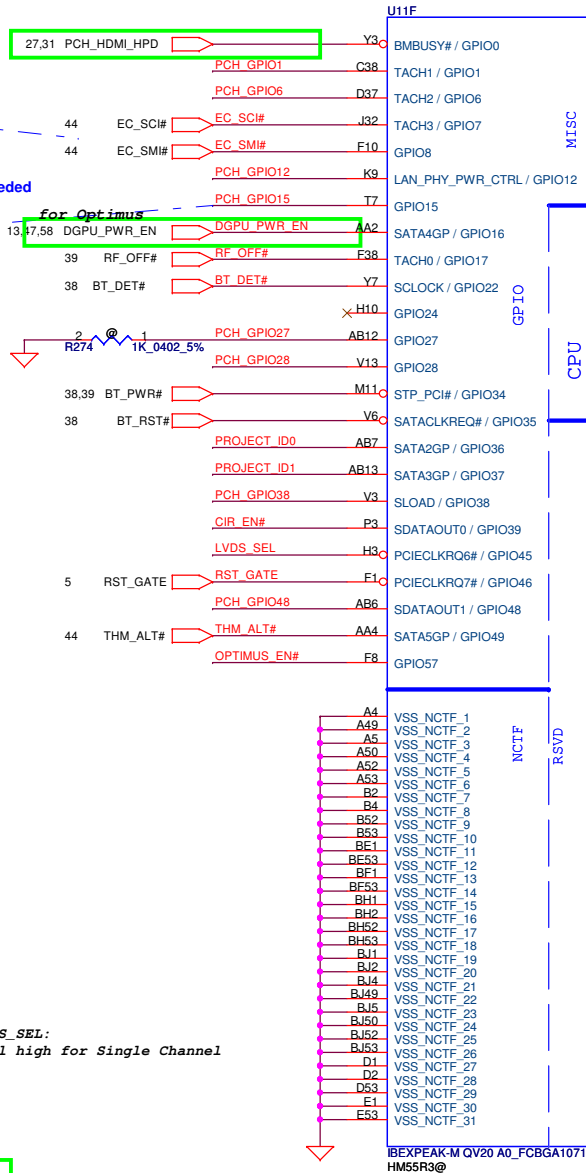
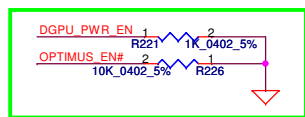
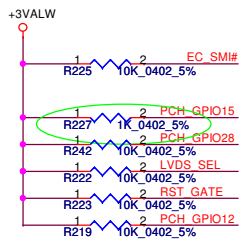
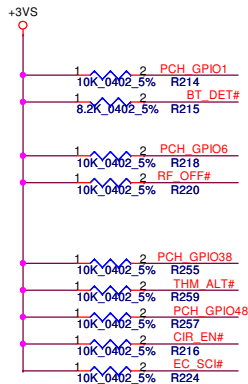


**GPIO8**  
Not pull down  
Internal: Pull up 20k  
During Reset: High  
Initial: High

**GPIO15**  
a Strong pull up may be needed  
for GPIO Functionality  
Internal: Pull down 20k  
During Reset: Low  
Initial: Low

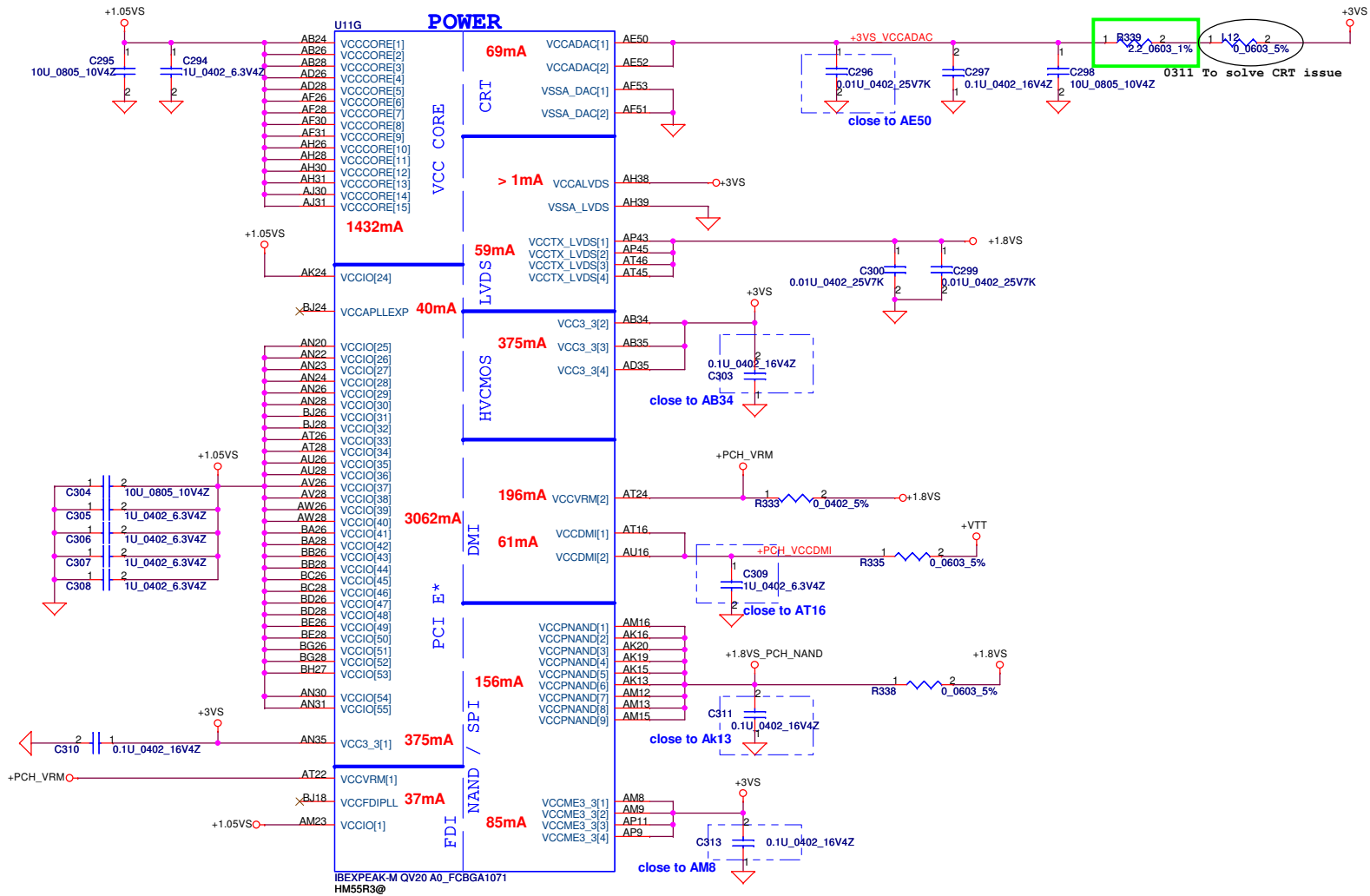
**On-Die PLL VR**

**PCH\_GPIO27** High = Enabled (Default)  
Low = Disabled



Not pull low  
internal pull up  
Internal: Pull up 20k  
During Reset: High  
Initial: High

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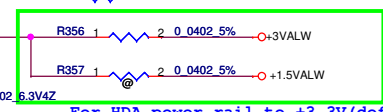
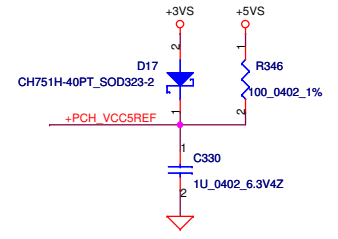
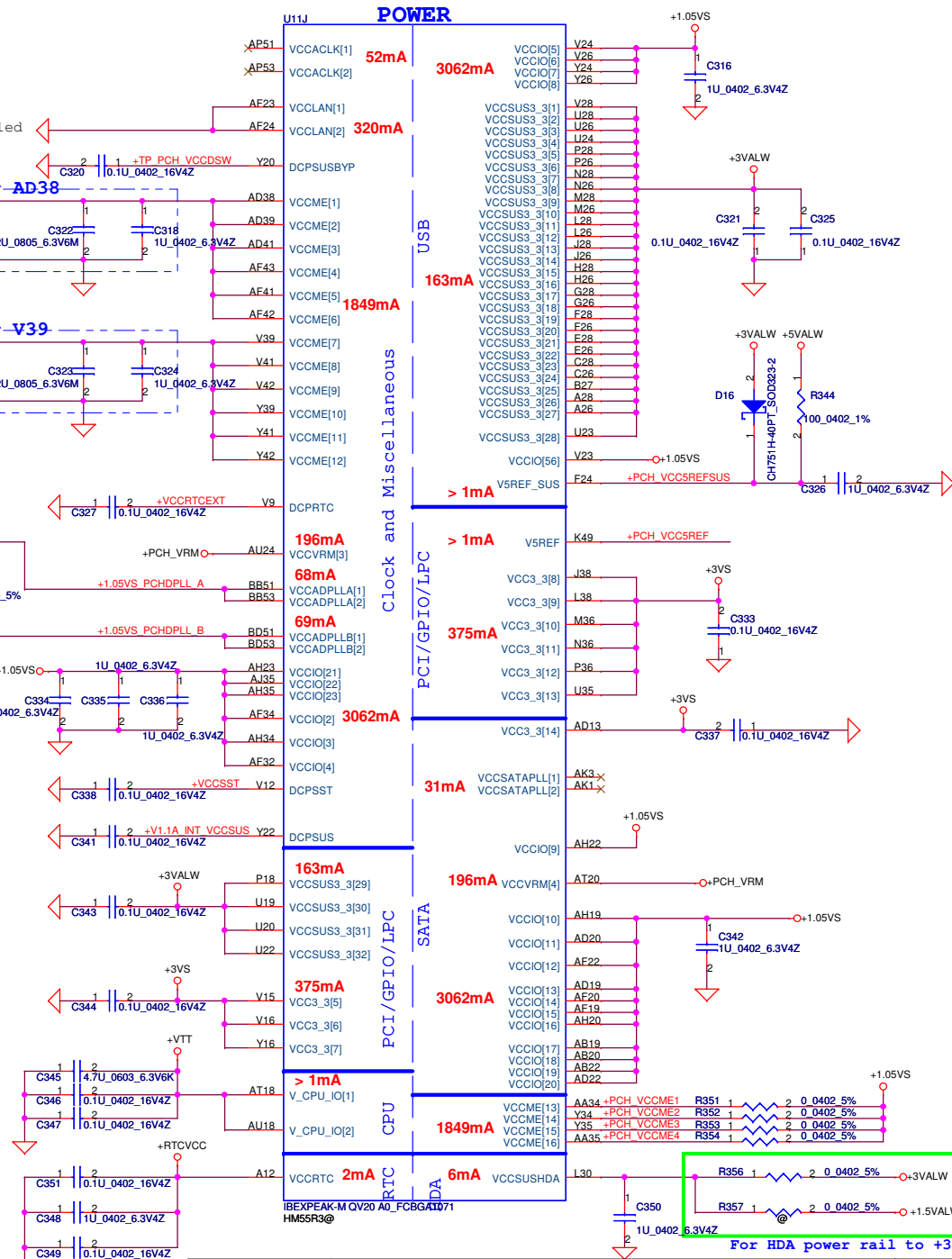
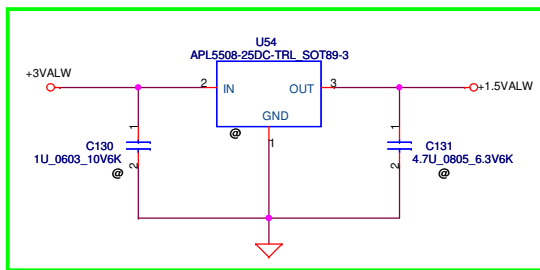


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VccLAN may be grounded if Intel LAN is disabled

If two VccME rails can be combined, only total 2 x 22  $\mu$ F and 2 x 1  $\mu$ F caps are necessary

For HDA power rail



VCCSUSHDA can be either 1.5V or 3.3V

For HDA power rail to +3.3V(default) /+1.5V

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Size	Document Number	Customer	Rev	Rev	
	NBQAA LA6072P M/B		1.0		
Date:	Monday, March 22, 2010	Sheet	35	of 61	

U11		H49	
AY7	VSS[159]	VSS[259]	H5
B11	VSS[160]	VSS[260]	J24
B15	VSS[161]	VSS[261]	K11
B19	VSS[162]	VSS[262]	K43
B23	VSS[163]	VSS[263]	K47
B31	VSS[164]	VSS[264]	L14
B35	VSS[165]	VSS[265]	L18
B39	VSS[166]	VSS[266]	L2
B43	VSS[167]	VSS[267]	L22
B47	VSS[168]	VSS[268]	L32
B7	VSS[169]	VSS[269]	L36
BC12	VSS[170]	VSS[270]	L40
BB16	VSS[171]	VSS[271]	L52
BB20	VSS[172]	VSS[272]	M12
BB24	VSS[173]	VSS[273]	M16
BB30	VSS[174]	VSS[274]	M20
BB34	VSS[175]	VSS[275]	N39
BB38	VSS[176]	VSS[276]	M34
BB42	VSS[177]	VSS[277]	M38
BB49	VSS[178]	VSS[278]	M42
BB5	VSS[179]	VSS[279]	M46
BC10	VSS[180]	VSS[280]	M49
BC14	VSS[181]	VSS[281]	M5
BC18	VSS[182]	VSS[282]	M8
BC2	VSS[183]	VSS[283]	N24
BC22	VSS[184]	VSS[284]	P11
BC32	VSS[185]	VSS[285]	AD15
BC36	VSS[186]	VSS[286]	P22
BC40	VSS[187]	VSS[287]	P30
BC44	VSS[188]	VSS[288]	P32
BC52	VSS[189]	VSS[289]	P34
BH0	VSS[190]	VSS[290]	P42
BD48	VSS[191]	VSS[291]	P45
BD49	VSS[192]	VSS[292]	P47
BD5	VSS[193]	VSS[293]	R2
BE12	VSS[194]	VSS[294]	R52
BE16	VSS[195]	VSS[295]	T12
BE20	VSS[196]	VSS[296]	T41
BE24	VSS[197]	VSS[297]	T46
BE30	VSS[198]	VSS[298]	T49
BE34	VSS[199]	VSS[299]	T5
BE38	VSS[200]	VSS[300]	T8
BE42	VSS[201]	VSS[301]	U0
BE46	VSS[202]	VSS[302]	U31
BE48	VSS[203]	VSS[303]	U32
BE50	VSS[204]	VSS[304]	U34
BE6	VSS[205]	VSS[305]	P38
BE8	VSS[206]	VSS[306]	V11
BF3	VSS[207]	VSS[307]	P16
BF49	VSS[208]	VSS[308]	V19
BF51	VSS[209]	VSS[309]	V20
BG18	VSS[210]	VSS[310]	V22
BG24	VSS[211]	VSS[311]	V30
BG4	VSS[212]	VSS[312]	V31
BG50	VSS[213]	VSS[313]	V32
BH11	VSS[214]	VSS[314]	V34
BH15	VSS[215]	VSS[315]	V35
BH19	VSS[216]	VSS[316]	V38
BH23	VSS[217]	VSS[317]	V43
BH31	VSS[218]	VSS[318]	V45
BH35	VSS[219]	VSS[319]	V46
BH39	VSS[220]	VSS[320]	V47
BH43	VSS[221]	VSS[321]	V49
BH47	VSS[222]	VSS[322]	V5
BH7	VSS[223]	VSS[323]	V7
C12	VSS[224]	VSS[324]	V8
C50	VSS[225]	VSS[325]	W2
D51	VSS[226]	VSS[326]	W52
E12	VSS[227]	VSS[327]	Y11
E16	VSS[228]	VSS[328]	Y12
E20	VSS[229]	VSS[329]	Y15
E24	VSS[230]	VSS[330]	Y19
E30	VSS[231]	VSS[331]	Y23
E34	VSS[232]	VSS[332]	Y28
E38	VSS[233]	VSS[333]	Y30
E42	VSS[234]	VSS[334]	Y31
E46	VSS[235]	VSS[335]	Y32
E48	VSS[236]	VSS[336]	Y38
E6	VSS[237]	VSS[337]	Y43
E8	VSS[238]	VSS[338]	Y46
F49	VSS[239]	VSS[339]	P49
F5	VSS[240]	VSS[340]	Y5
F5	VSS[241]	VSS[341]	Y6
G10	VSS[242]	VSS[342]	Y8
G14	VSS[243]	VSS[343]	P24
G18	VSS[244]	VSS[344]	T43
G2	VSS[245]	VSS[345]	AD51
G22	VSS[246]	VSS[346]	AT8
G32	VSS[247]	VSS[347]	AD47
G36	VSS[248]	VSS[348]	Y47
G40	VSS[249]	VSS[349]	AT12
G44	VSS[250]	VSS[350]	AM6
G52	VSS[251]	VSS[351]	AT13
AF39	VSS[252]	VSS[352]	AM5
H16	VSS[253]	VSS[353]	AK45
H20	VSS[254]	VSS[354]	AK38
H30	VSS[255]	VSS[355]	AV14
H34	VSS[256]	VSS[356]	
H38	VSS[257]	VSS[357]	
H42	VSS[258]	VSS[358]	

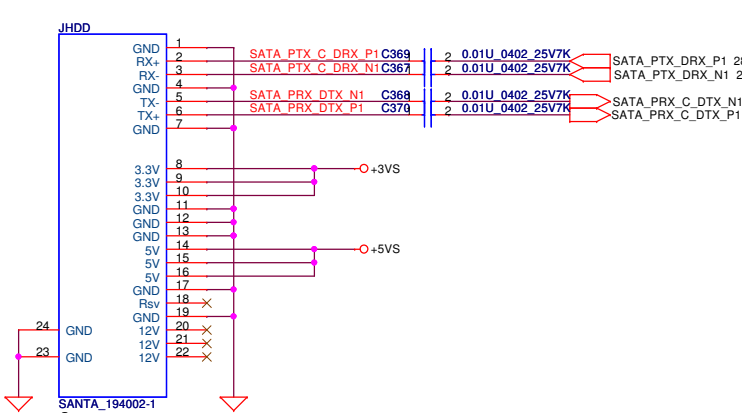
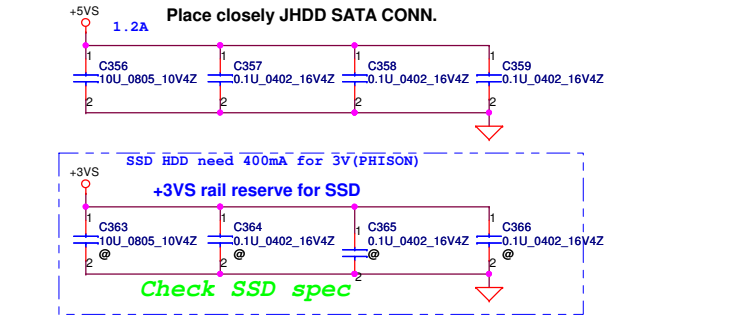
IBEXPEAK-M QV20 A0\_FCBGA1071  
HM55R3@

U11H		AK30	
AA19	VSS[1]	VSS[80]	AK31
AA20	VSS[2]	VSS[81]	AK32
AA22	VSS[3]	VSS[82]	AK34
AM19	VSS[4]	VSS[83]	AK35
AA24	VSS[5]	VSS[84]	AK38
AA26	VSS[6]	VSS[85]	AK43
AA28	VSS[7]	VSS[86]	AK44
AA30	VSS[8]	VSS[87]	AK45
AA31	VSS[9]	VSS[88]	AK49
AA32	VSS[10]	VSS[89]	AK5
AB11	VSS[11]	VSS[90]	AK8
AB15	VSS[12]	VSS[91]	AL2
AB23	VSS[13]	VSS[92]	AL52
AB30	VSS[14]	VSS[93]	AM11
AB31	VSS[15]	VSS[94]	B44
AB39	VSS[16]	VSS[95]	AD24
AB43	VSS[17]	VSS[96]	AM20
AB47	VSS[18]	VSS[97]	AM22
AB5	VSS[19]	VSS[98]	AM24
AB5	VSS[20]	VSS[99]	AM26
AB5	VSS[21]	VSS[100]	AM28
AC2	VSS[22]	VSS[101]	B42
AC52	VSS[23]	VSS[102]	AM30
AD11	VSS[24]	VSS[103]	AM31
AD12	VSS[25]	VSS[104]	AM32
AD16	VSS[26]	VSS[105]	AM34
AD23	VSS[27]	VSS[106]	AM35
AD30	VSS[28]	VSS[107]	AM38
AD31	VSS[29]	VSS[108]	AM39
AD32	VSS[30]	VSS[109]	AM42
AD34	VSS[31]	VSS[110]	AM44
AU22	VSS[32]	VSS[111]	AM46
AD42	VSS[33]	VSS[112]	AV22
AD46	VSS[34]	VSS[113]	AM49
T12	VSS[35]	VSS[114]	AM7
AD7	VSS[36]	VSS[115]	AM7
AE2	VSS[37]	VSS[116]	AA50
AE4	VSS[38]	VSS[117]	BB10
AE12	VSS[39]	VSS[118]	AN32
Y13	VSS[40]	VSS[119]	AN50
AAH9	VSS[41]	VSS[120]	AN52
AU4	VSS[42]	VSS[121]	AP12
AF35	VSS[43]	VSS[122]	AP24
AP13	VSS[44]	VSS[123]	AP46
AN34	VSS[45]	VSS[124]	AP49
AF45	VSS[46]	VSS[125]	AP5
AF46	VSS[47]	VSS[126]	AP8
AF49	VSS[48]	VSS[127]	AP52
AE5	VSS[49]	VSS[128]	AT11
AF8	VSS[50]	VSS[129]	AT128
AG2	VSS[51]	VSS[130]	AH48
AG52	VSS[52]	VSS[131]	AT32
AH11	VSS[53]	VSS[132]	AT36
AH15	VSS[54]	VSS[133]	AT41
AH18	VSS[55]	VSS[134]	AT47
AH22	VSS[56]	VSS[135]	AT7
AV18	VSS[57]	VSS[136]	AV12
AH43	VSS[58]	VSS[137]	AV16
AH47	VSS[59]	VSS[138]	AV20
AH7	VSS[60]	VSS[139]	AV24
AU19	VSS[61]	VSS[140]	AV30
AJ2	VSS[62]	VSS[141]	AV34
AJ20	VSS[63]	VSS[142]	AV38
AJ22	VSS[64]	VSS[143]	AV42
AJ23	VSS[65]	VSS[144]	AV46
AJ25	VSS[66]	VSS[145]	AV49
AJ26	VSS[67]	VSS[146]	AV5
AJ28	VSS[68]	VSS[147]	AV8
AJ32	VSS[69]	VSS[148]	AW14
AJ34	VSS[70]	VSS[149]	AW18
AT5	VSS[71]	VSS[150]	AW2
AJ4	VSS[72]	VSS[151]	AW2
AK12	VSS[73]	VSS[152]	BF9
AN41	VSS[74]	VSS[153]	AW32
AN19	VSS[75]	VSS[154]	AW36
AK26	VSS[76]	VSS[155]	AW40
AK22	VSS[77]	VSS[156]	AW52
AK23	VSS[78]	VSS[157]	AY11
AK28	VSS[79]	VSS[158]	AY43
			AY47

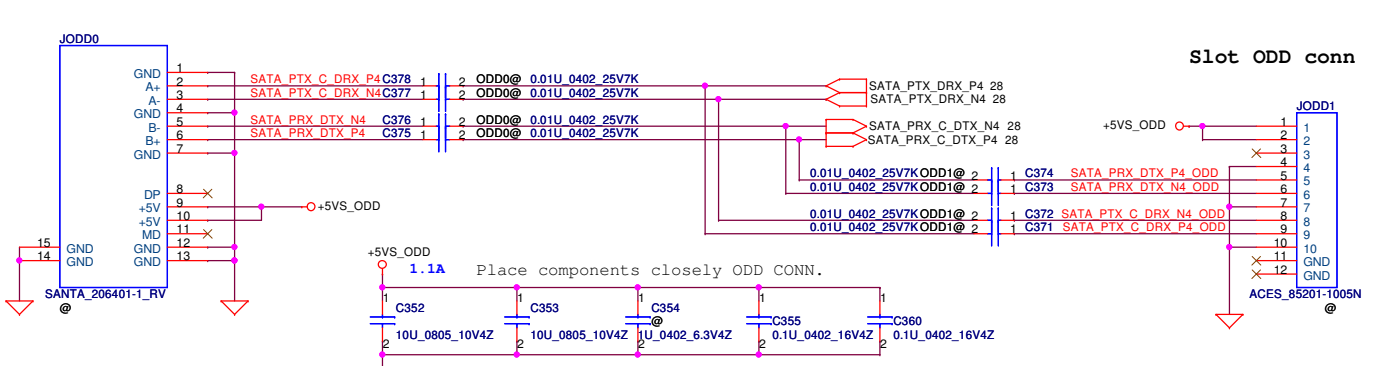
IBEXPEAK-M QV20 A0\_FCBGA1071  
HM55R3@

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Size	Document Number	Date		Rev	1.0
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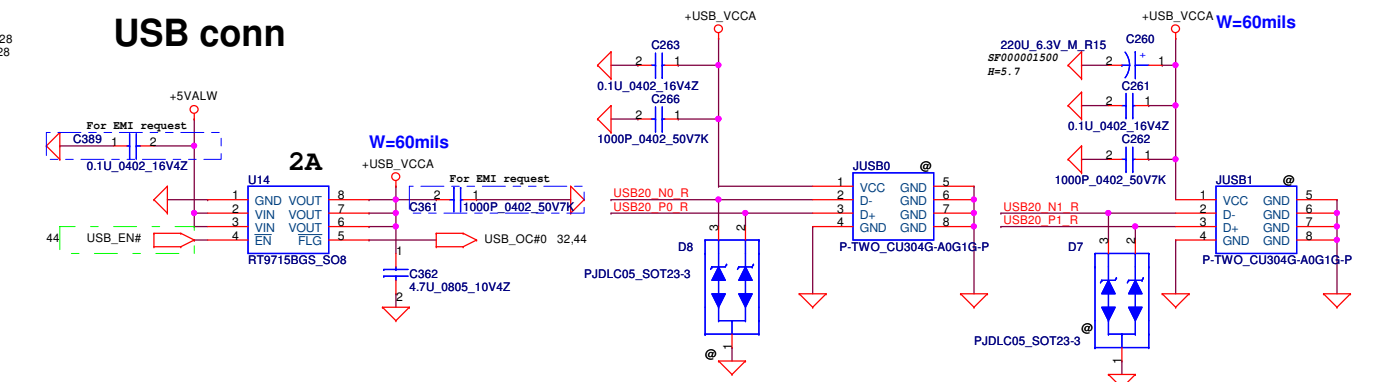
# SATA HDD Conn.



# SATA ODD Conn



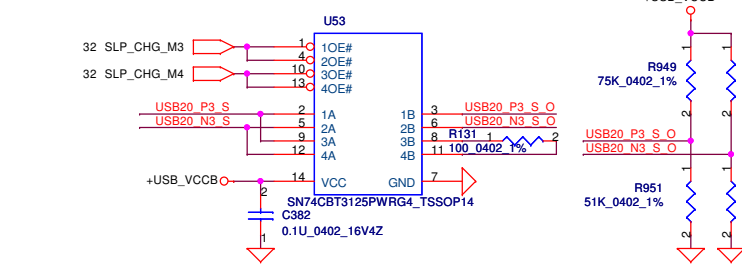
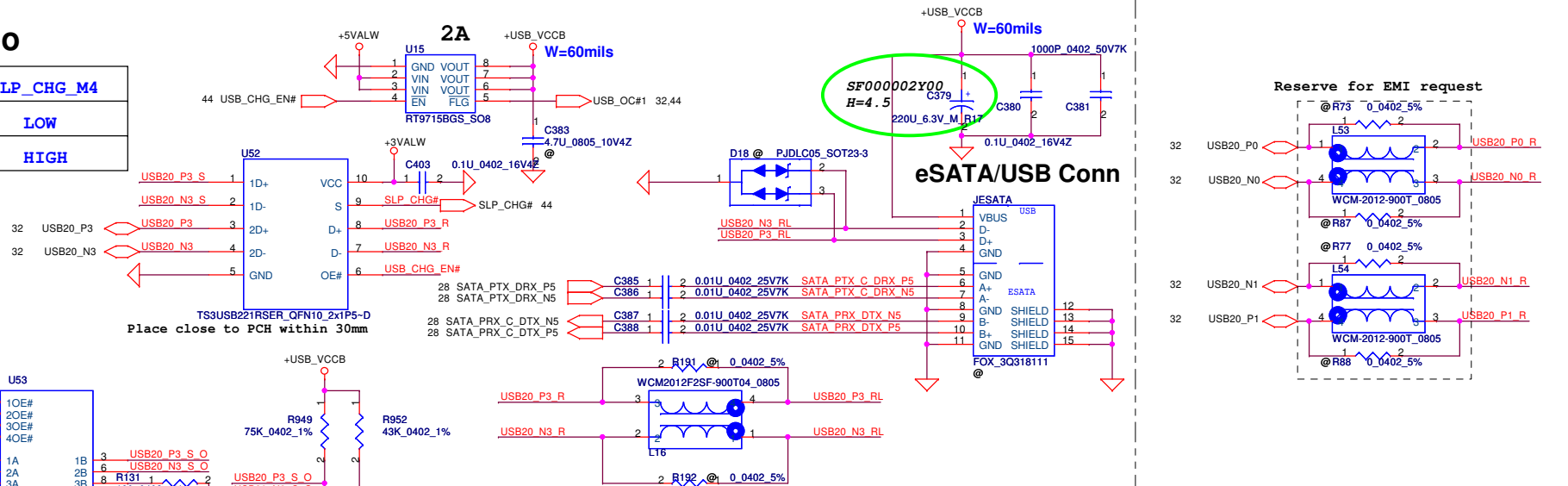
# USB conn



# eSATA/USB combo

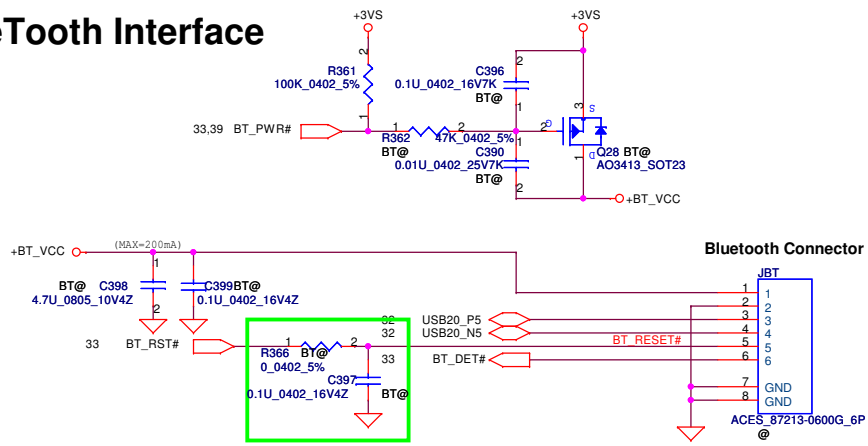
	SLP_CHG_M3	SLP_CHG_M4
Mode 3	HIGH	LOW
Mode 4	LOW	HIGH

SLP_CHG	FUNCTION
LOW	D=1D
HIGH	D=2D

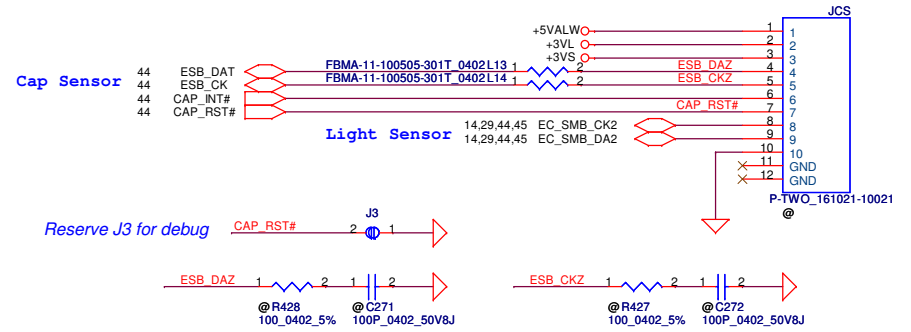


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Size	Document Number	NBQAA LA6072P M/B		Rev	1.0
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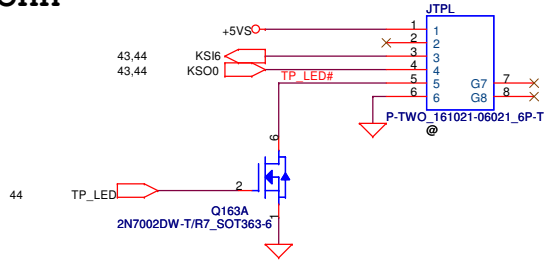
# BlueTooth Interface



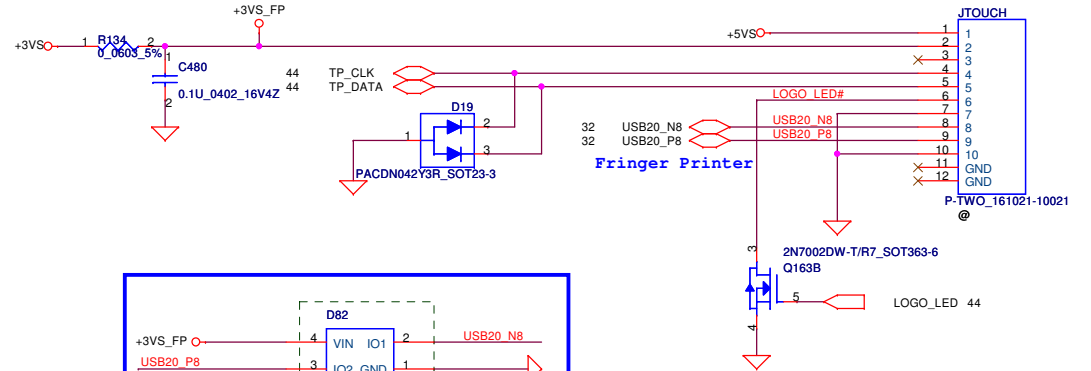
# Cap Sensor / Light Sensor Conn



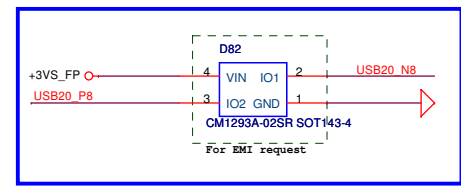
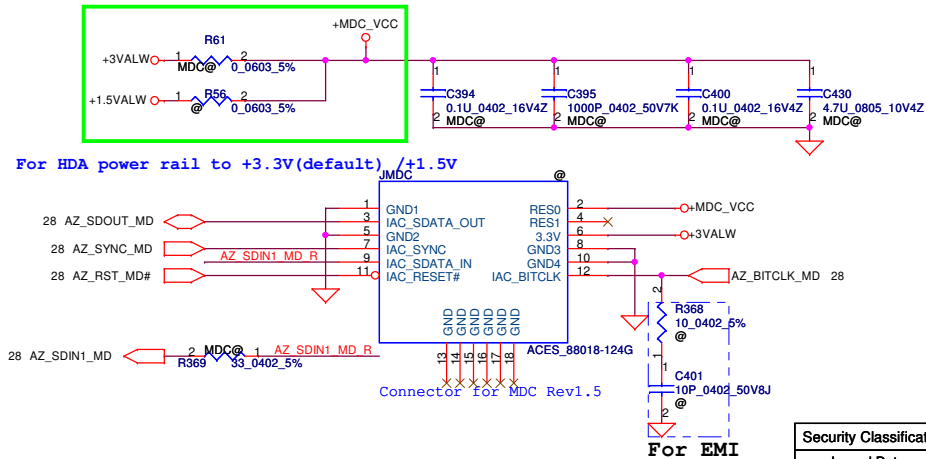
# TP LED Conn



# TP/B LED/B FP/B Conn

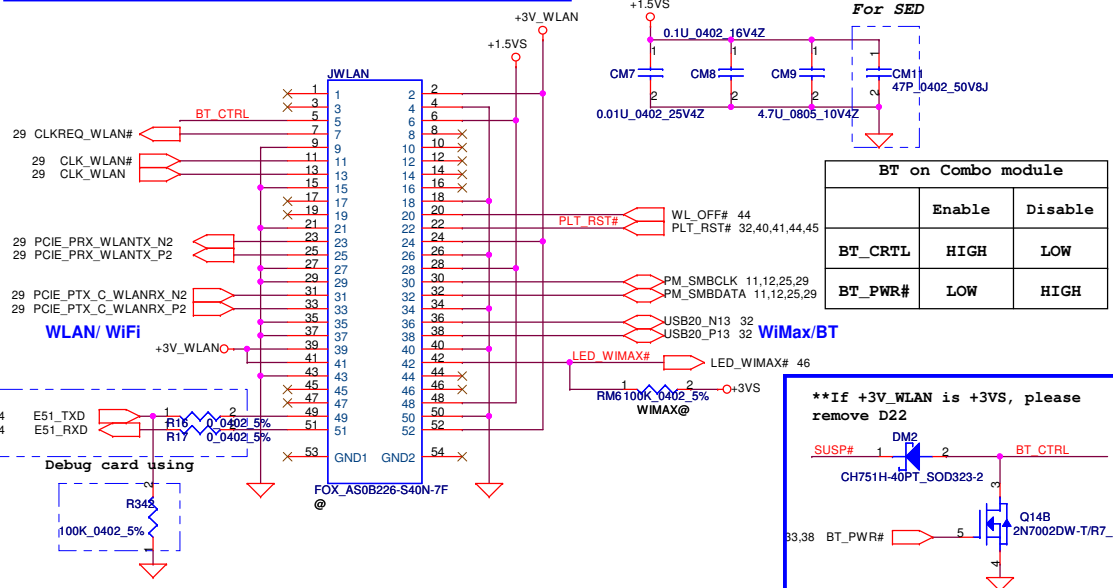
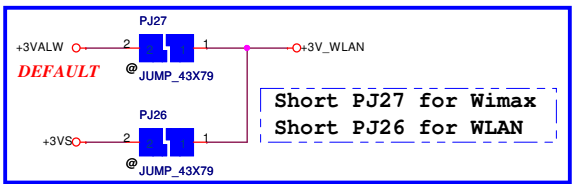


# MDC 1.5 Conn

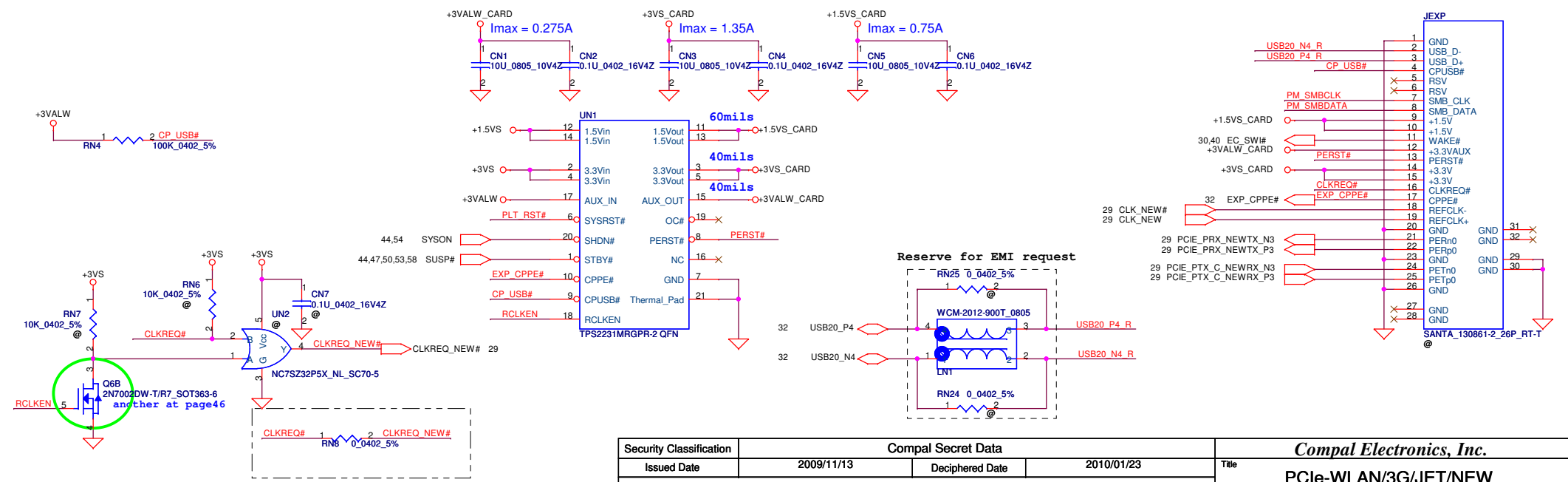
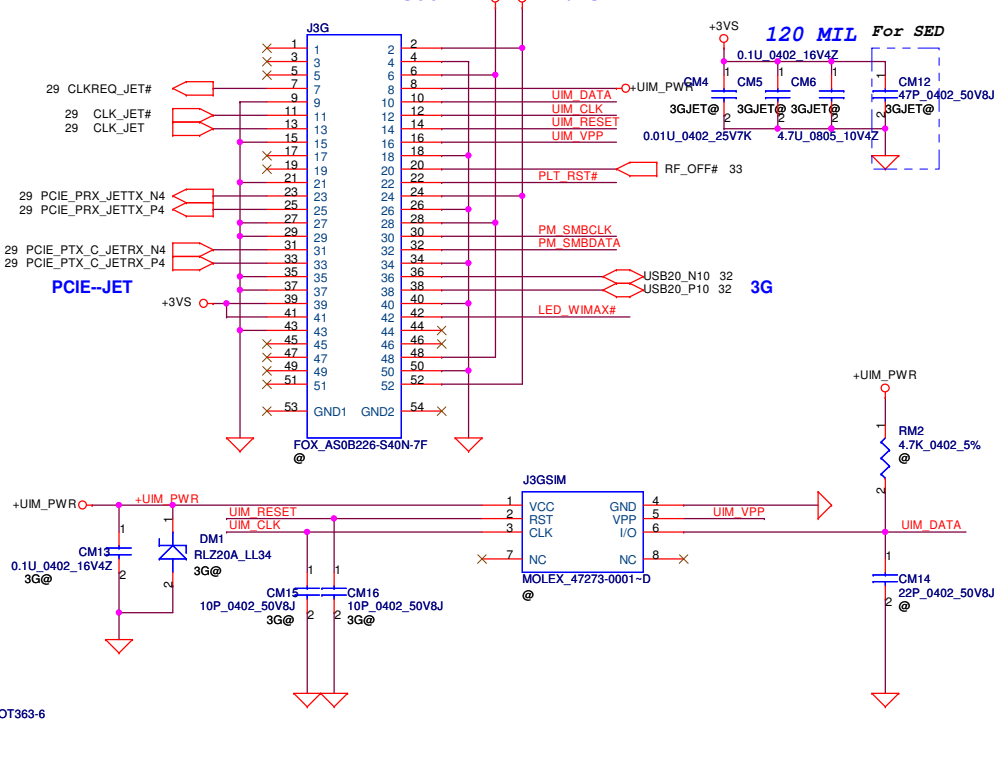


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Size	Document Number	Rev		1.0	
Date: Monday, March 22, 2010		Sheet 38 of 61		NBQAA LA6072P M/B	

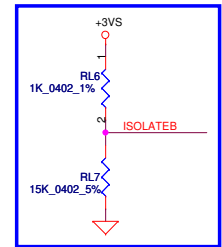
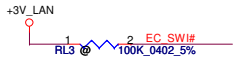
# PCIe Mini Card-WLAN/WiMax



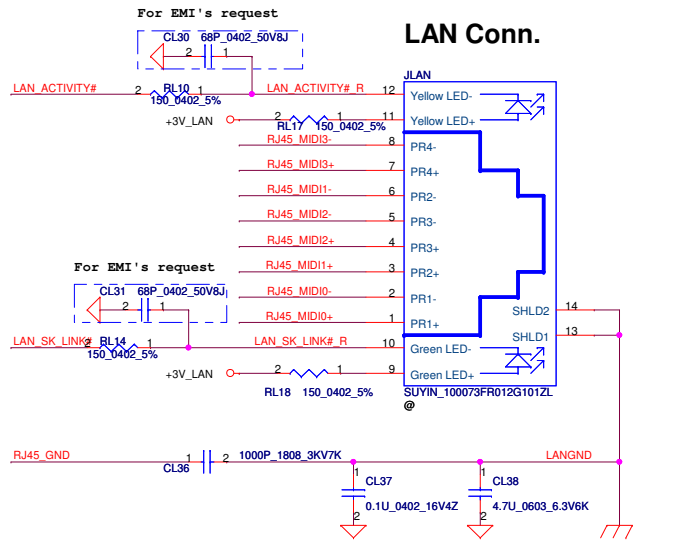
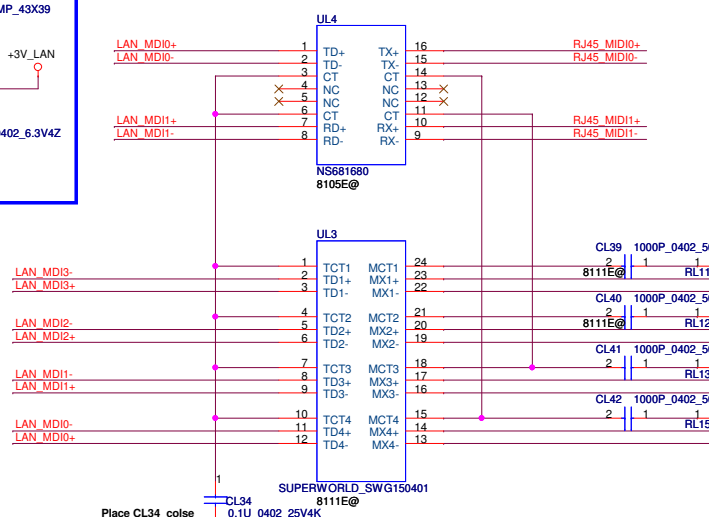
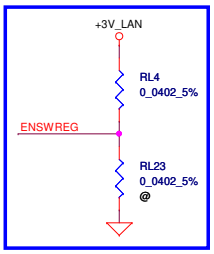
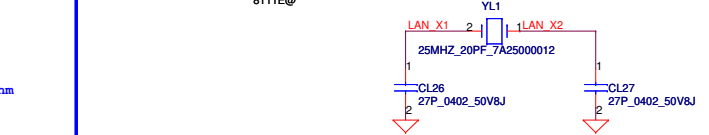
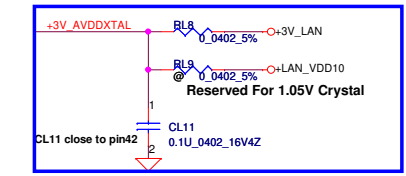
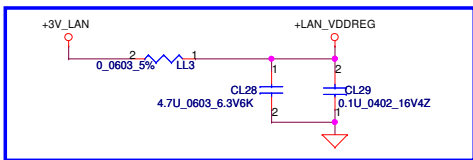
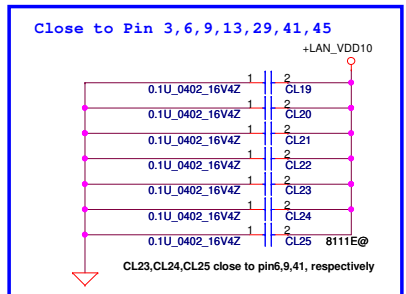
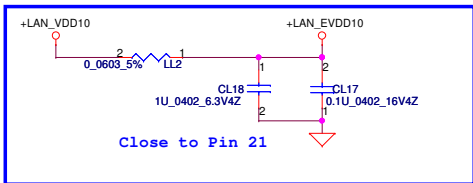
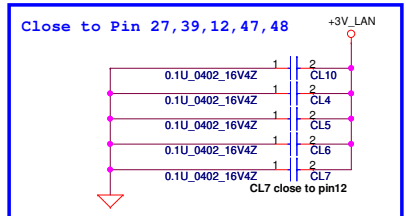
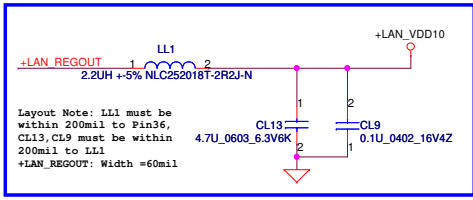
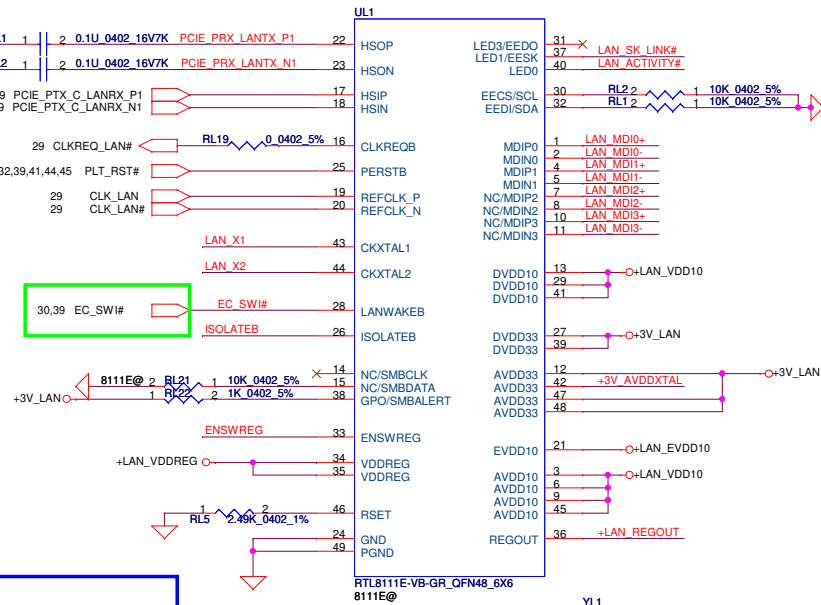
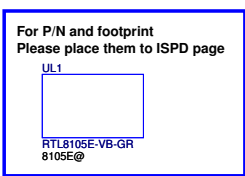
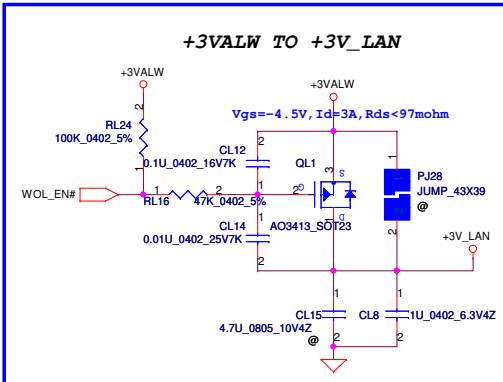
# PCIe Mini Card-3G/JET



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PCIe-WLAN/3G/JET/NEW			NBOAA LA6072P M/B	



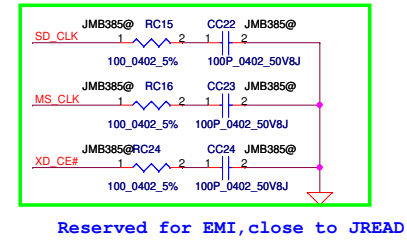
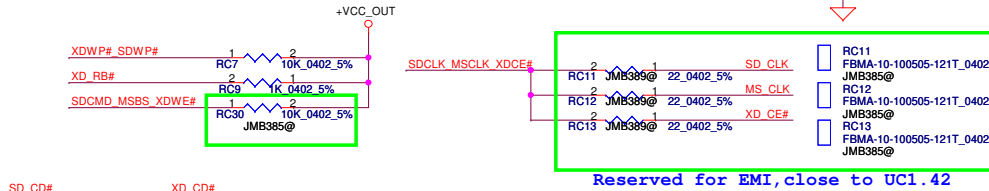
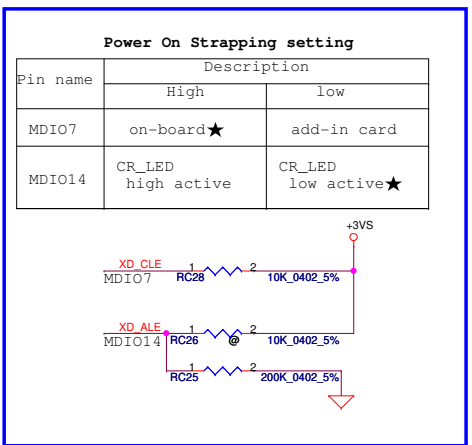
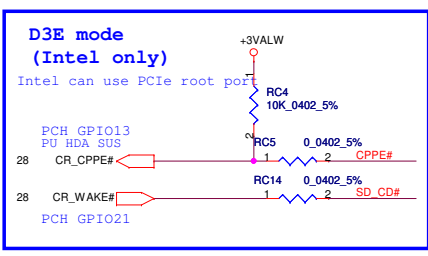
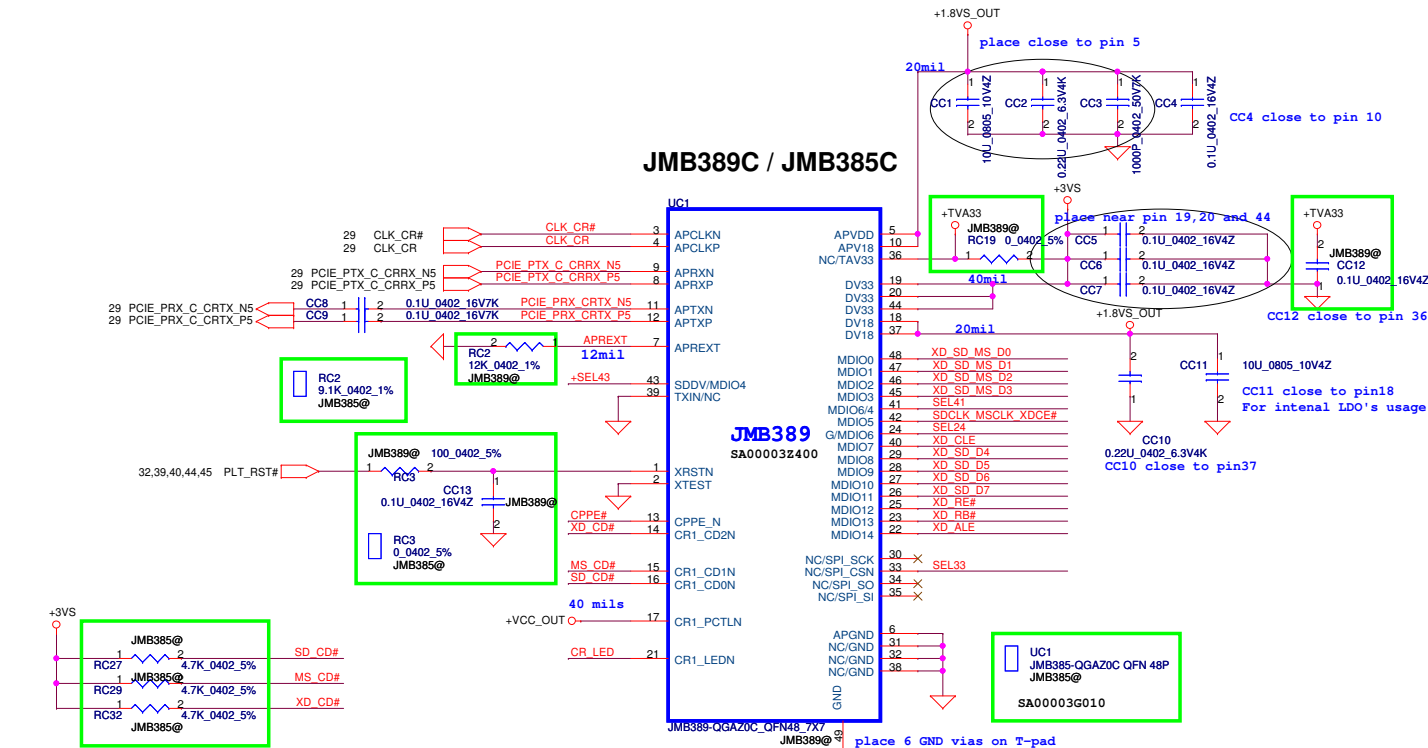
	RTL8105E	RTL8111E
Pin14	NC	NC
Pin15	NC	10K ohm PD
Pin38	1K ohm Pull-high	



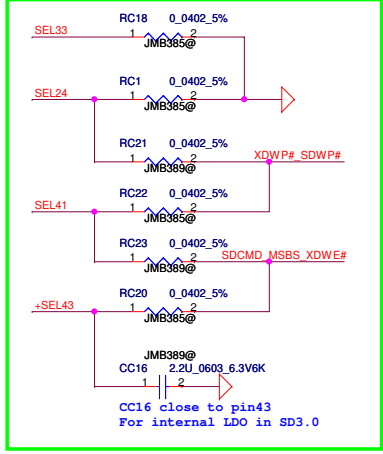
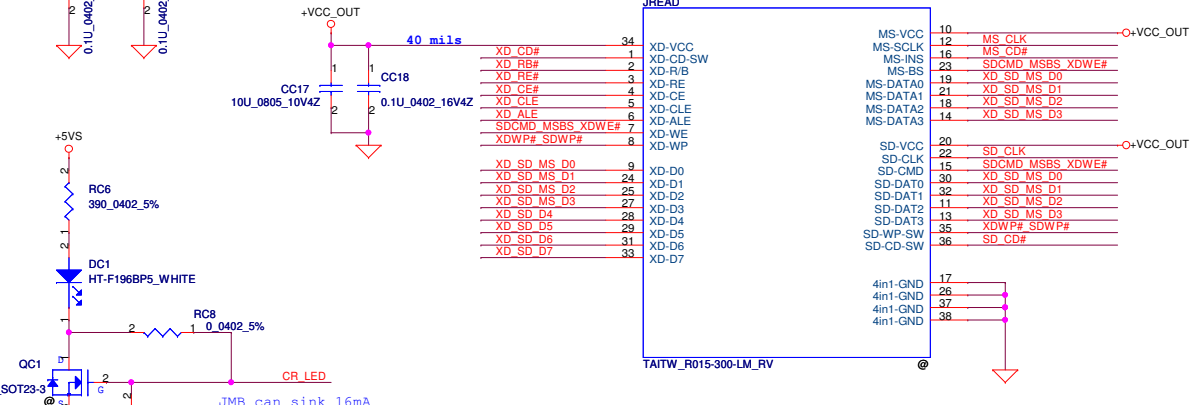
Security Classification		Compal Secret Data		Title	
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### JMB389C / JMB385C



### NBQAA 4 in 1 Card Reader

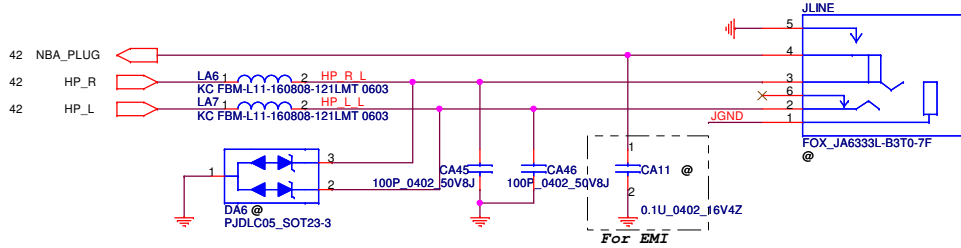


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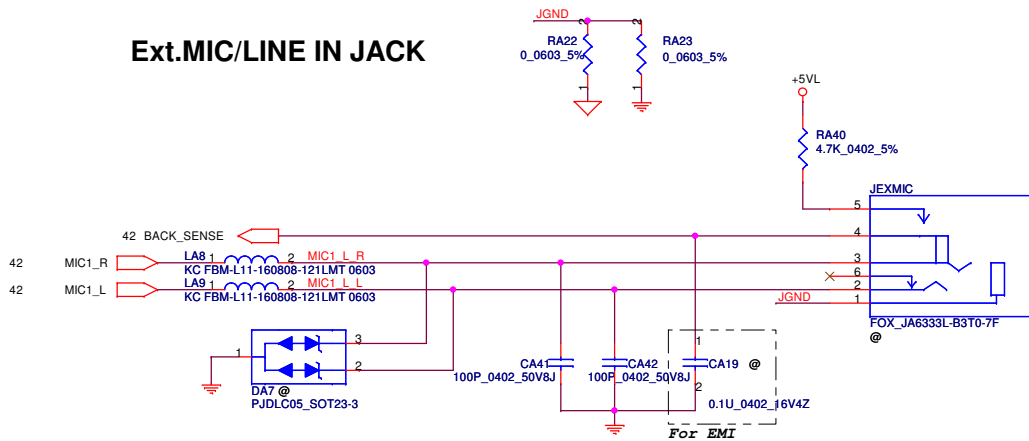
Compal Electronics, Inc.			
Title <b>Card Reader-JMB389C/385C</b>			
Size	Document Number	Rev	
Custom	NBQAA LA6071P M/B	2.0	
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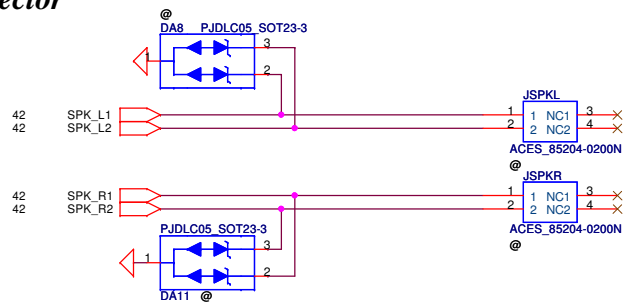
## HeadPhone/LINE Out JACK



## Ext.MIC/LINE IN JACK

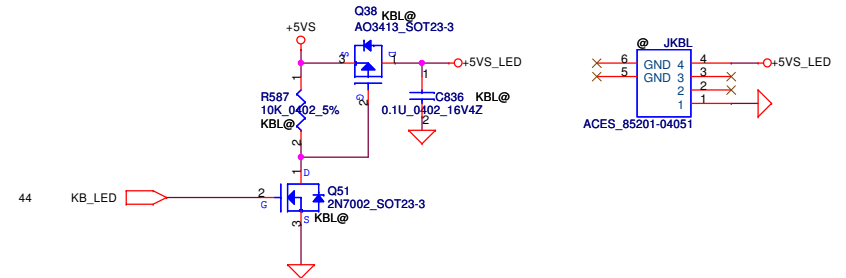


## Speaker Connector

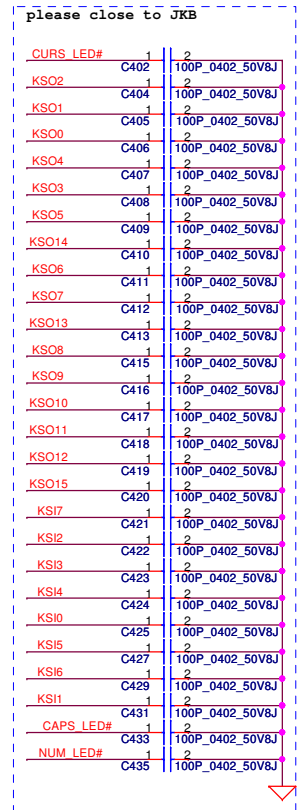
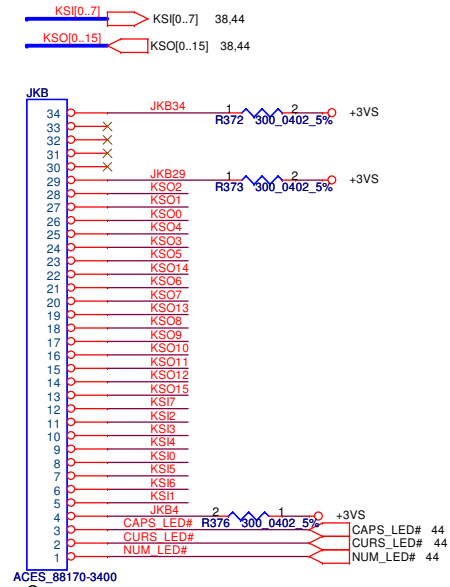


Need to update symbol

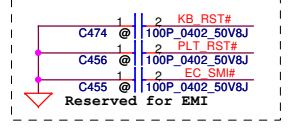
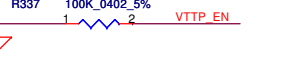
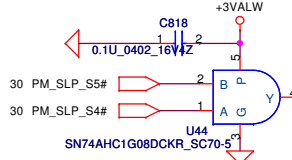
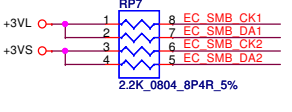
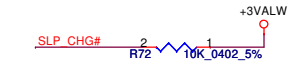
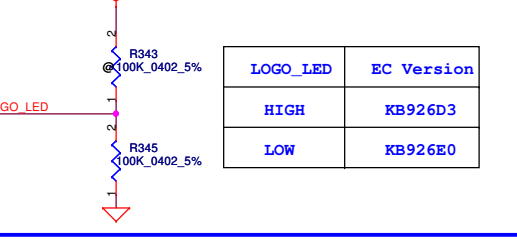
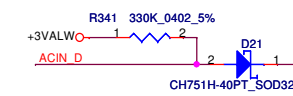
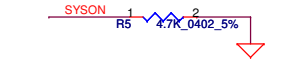
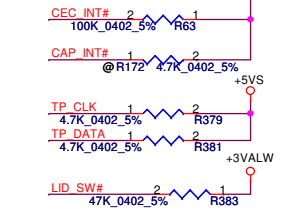
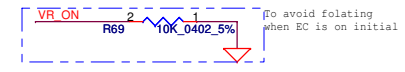
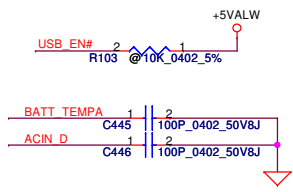
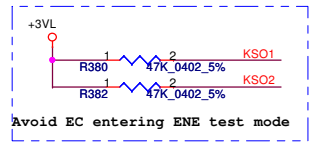
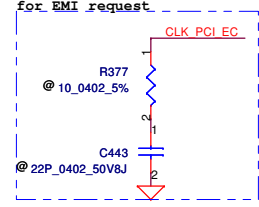
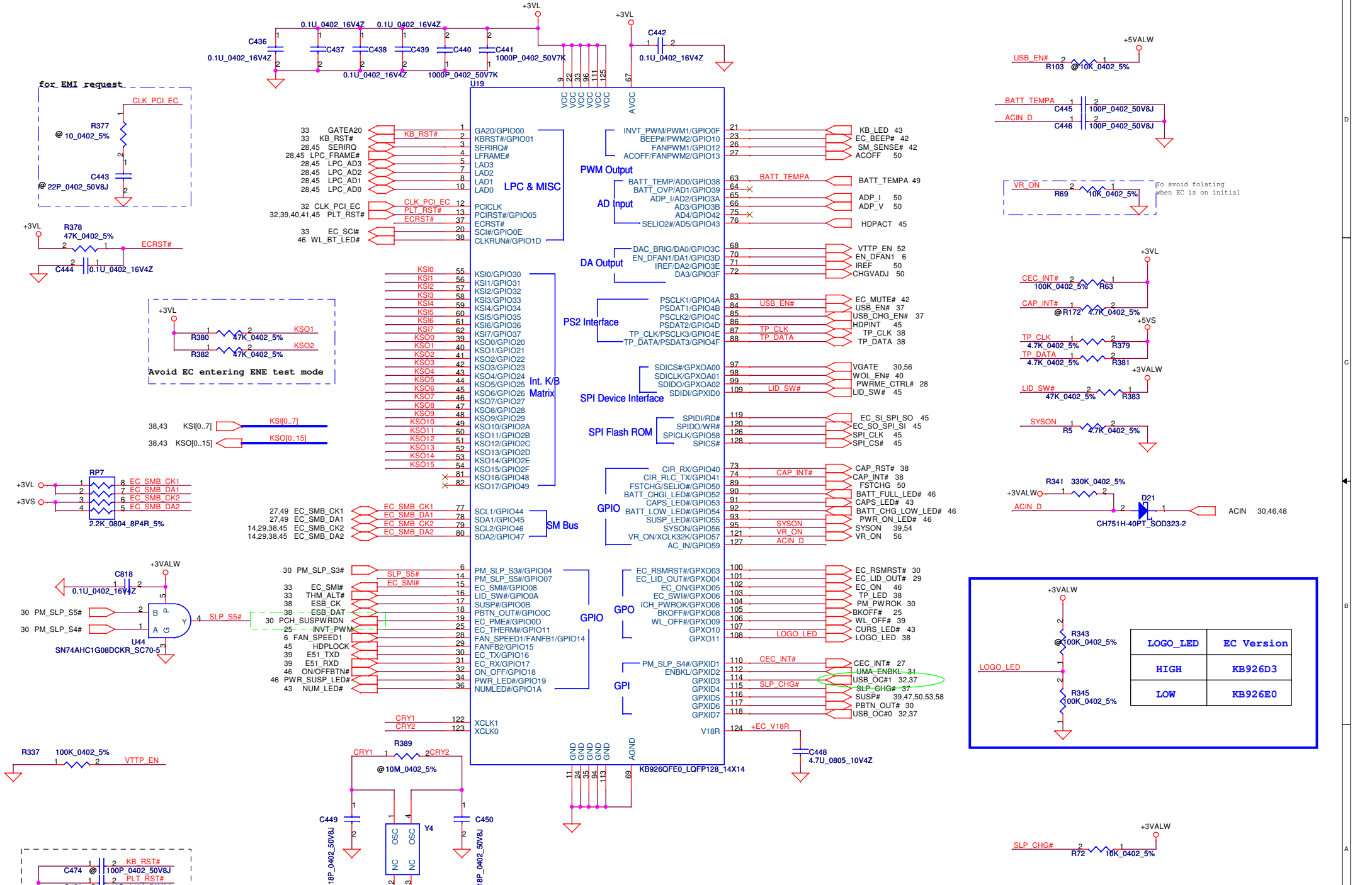
## Keyboard LED



## KEYBOARD CONN.



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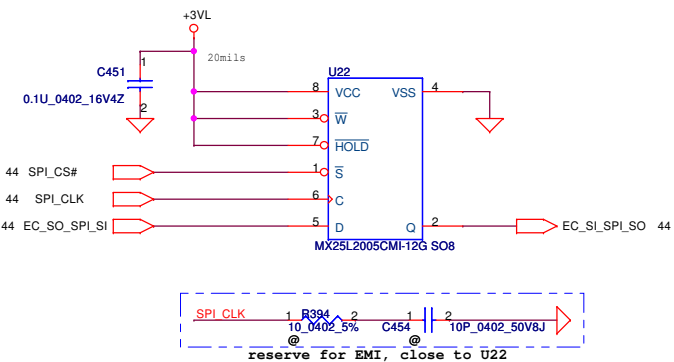


Reserved for EMI

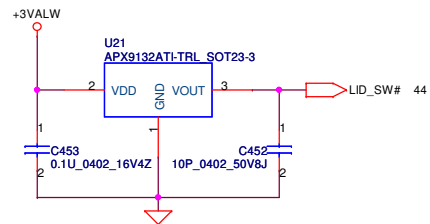
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Issued Date	2009/11/13	Deciphered Date	2010/01/23	ENE-KB926 RevD3/E0	
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	NBQAA LA6072P M/B	Monday, March 22, 2010		1.0	
				Sheet	44 of 61

# SPI Flash (256KB)

Socket: SP07000F500 & SP07000H900

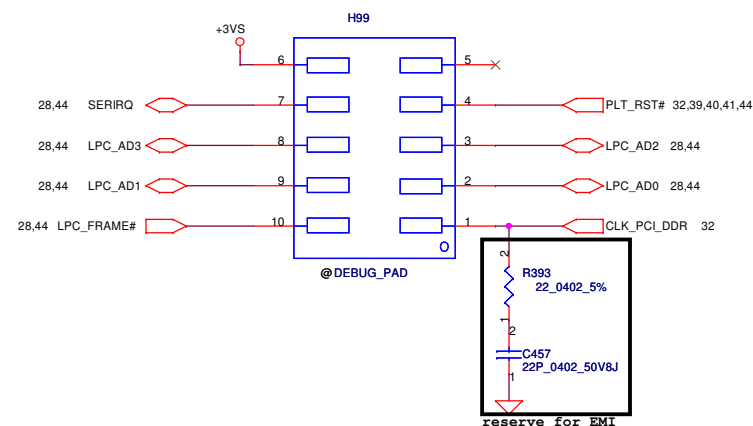


# Lid SW

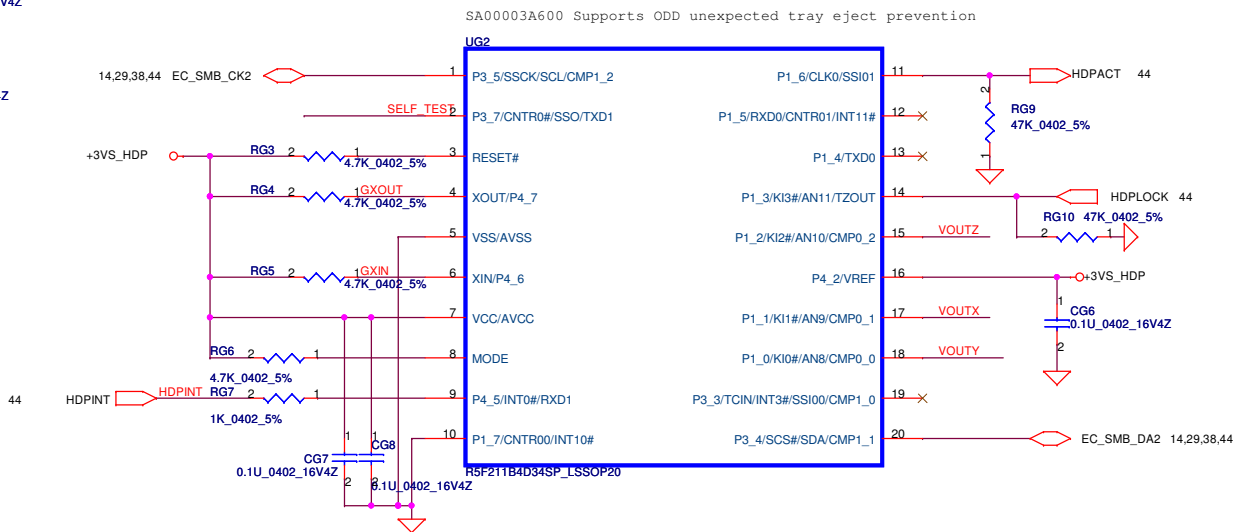
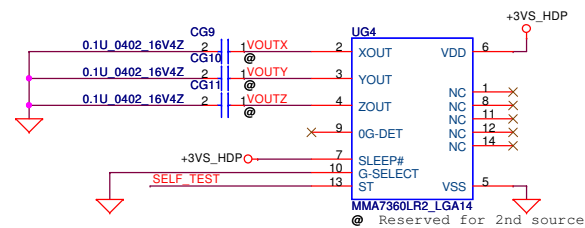
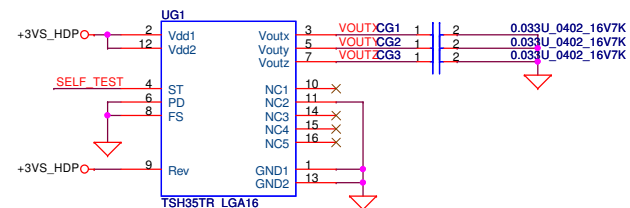
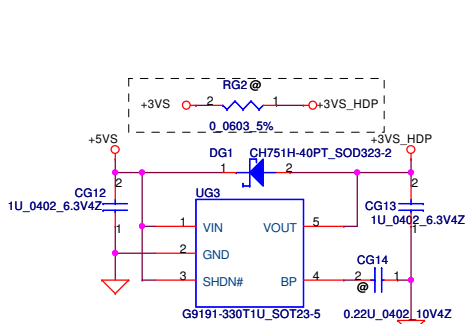


# LPC Debug Port

Please place the PAD under DDR DIMM.

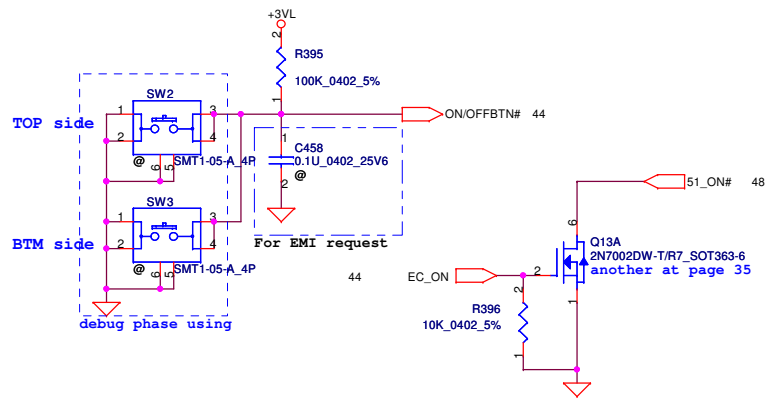


# G-Sensor

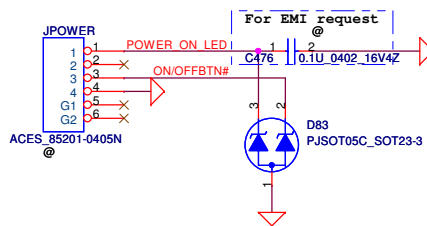


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Size	Document Number	NBQAA LA6072P M/B		Rev 1.0
Date:	Monday, March 22, 2010	Sheet	45 of 61	

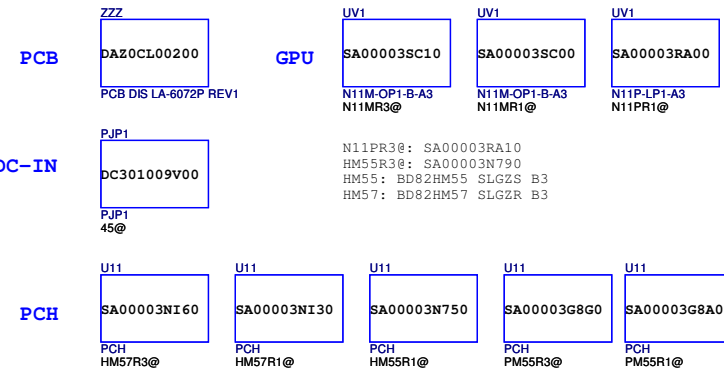
# Power Button



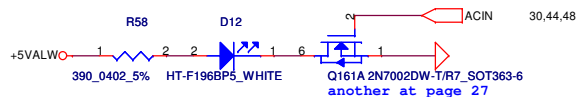
# PWR/B Conn



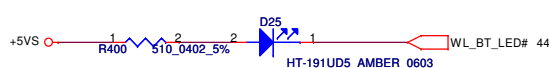
# ISPD



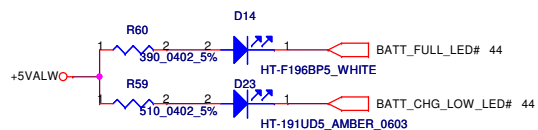
# DC-IN LED



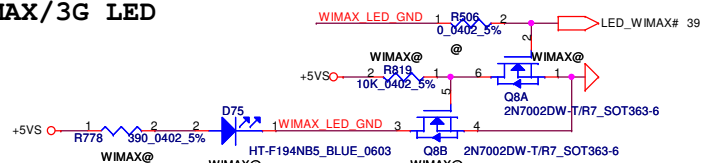
# WL/BT LED



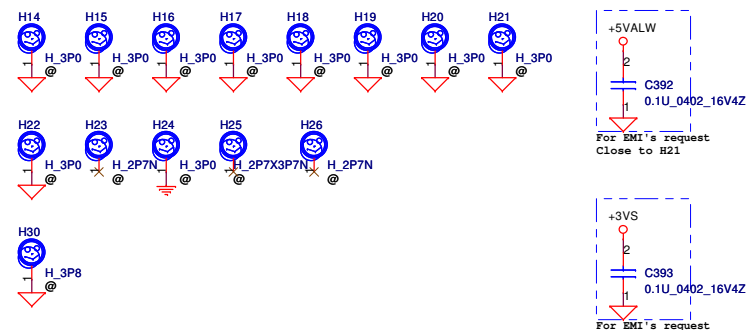
# BATT CHARGE/FULL LED



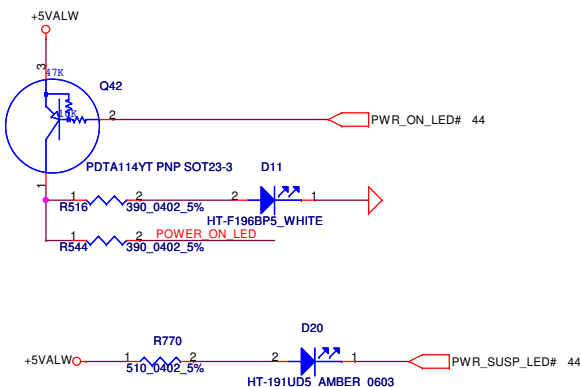
# WiMAX/3G LED



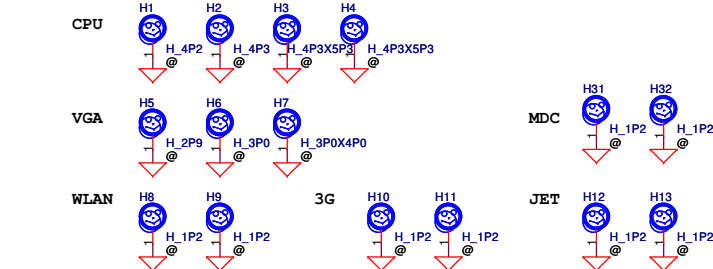
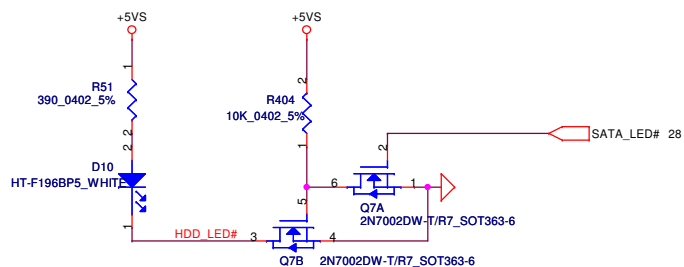
# Screw Hole



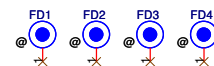
# POWER/SUSPEND LED



# HDD LED

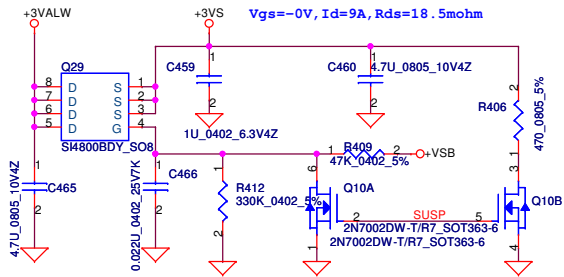


# PCB Fedcal Mark PAD

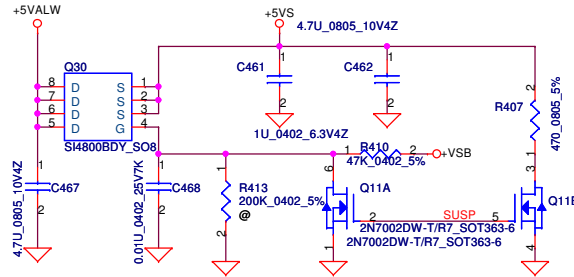


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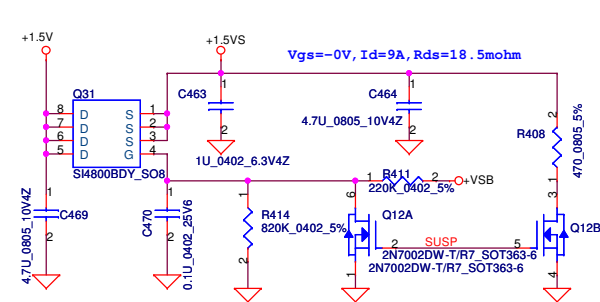
**+3VALW TO +3VS**



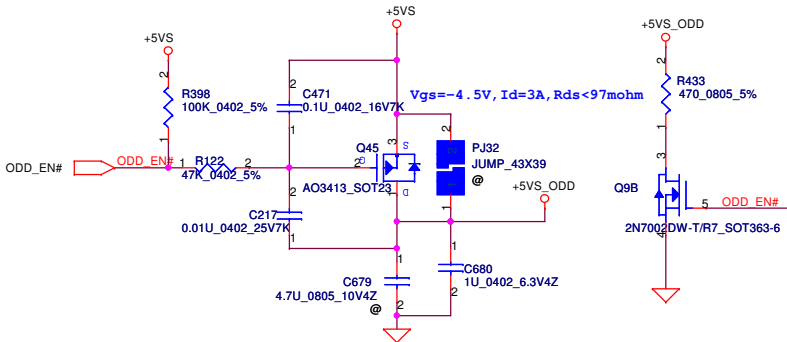
**+5VALW TO +5VS**



**+1.5V to +1.5VS**

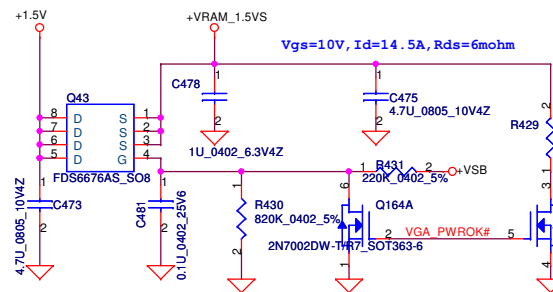


**+5VS TO +5VS\_ODD**



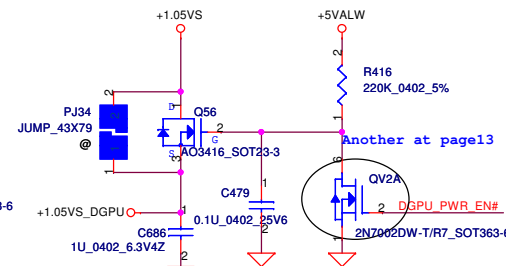
**+1.5V to +VRAM\_1.5VS**

(11A, 440mils, Via NO. = 22)



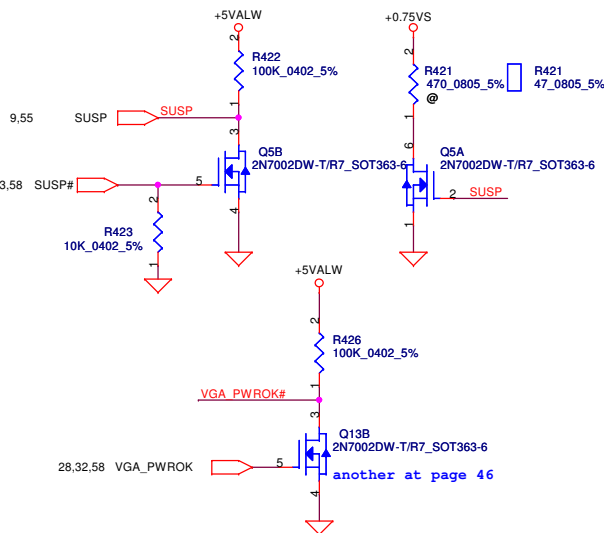
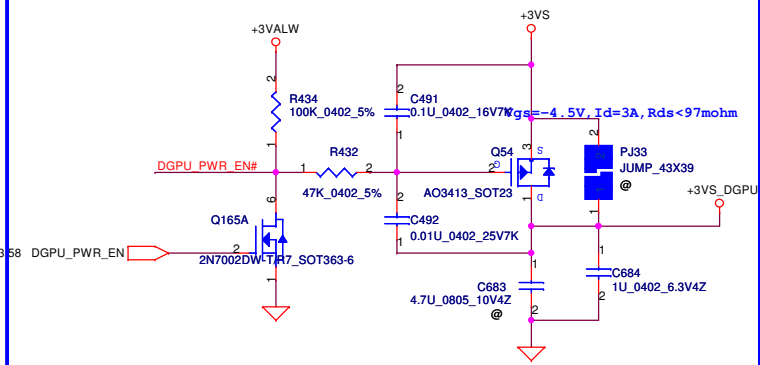
**+1.05VS to +1.05VS\_DGPU**

(2.87A, 120mils, Via NO. = 6)

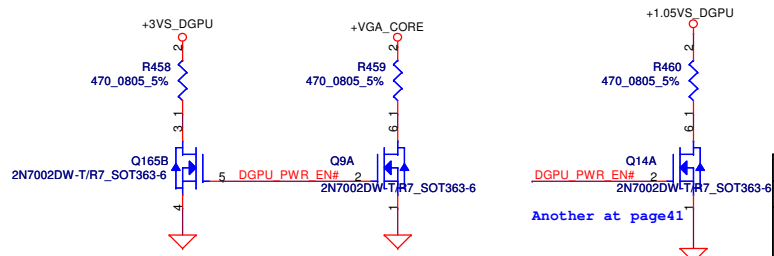
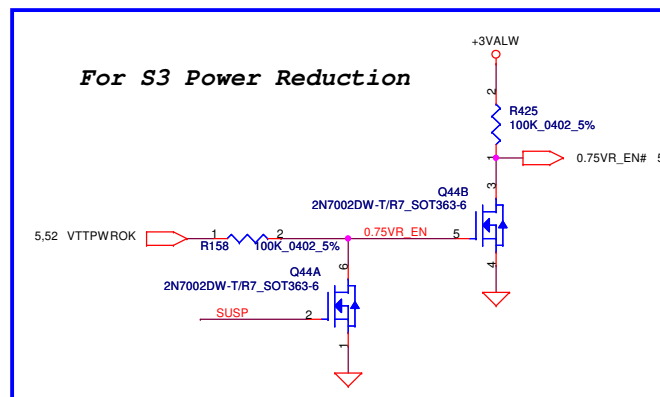


**+3VS to +3VS\_DGPU**

(780mA, 40mils, Via NO. = 2)

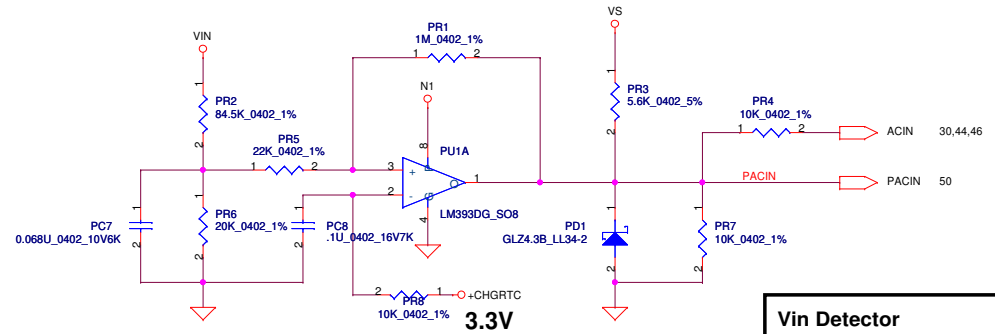
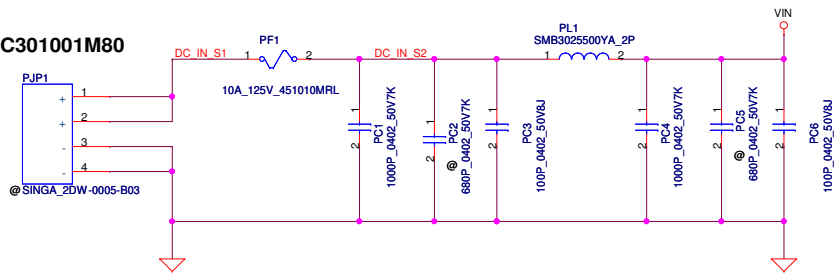


**For S3 Power Reduction**

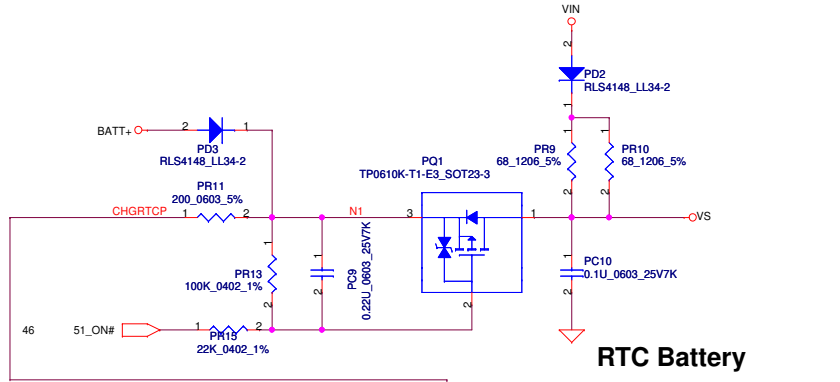


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	NBQAA LA6072P M/B	Monday, March 22, 2010		47 of 61	1.0

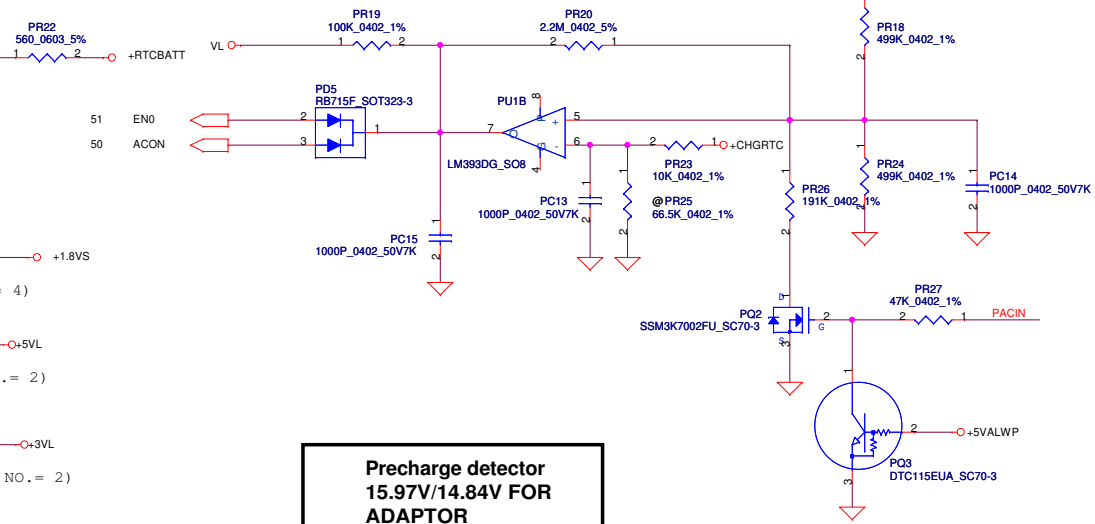
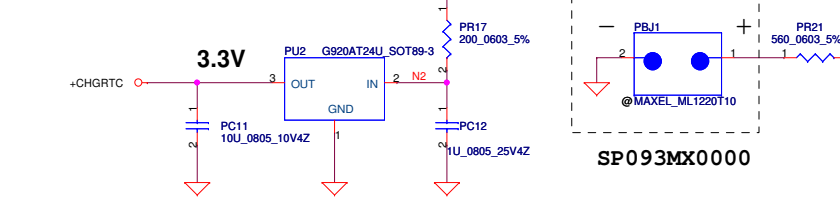
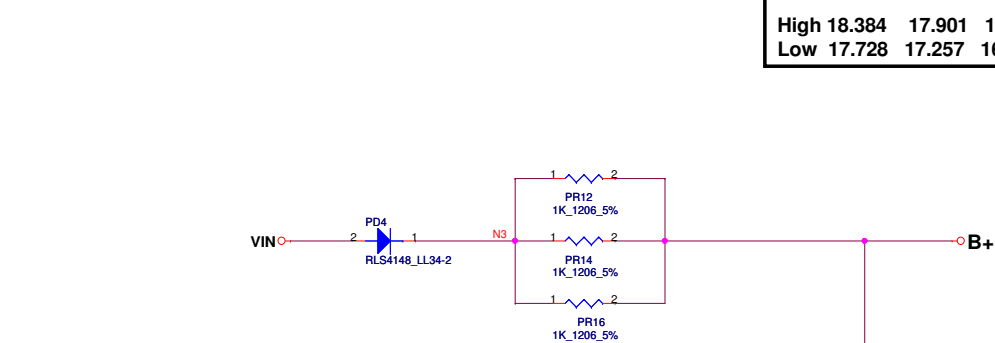
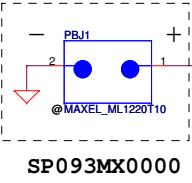
**DC301001M80**



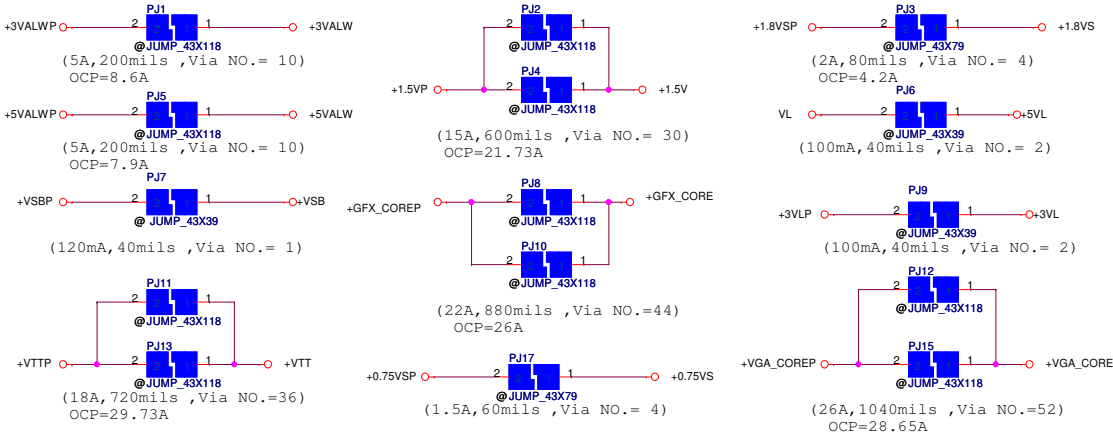
**Vin Detector**  
 High 18.384 17.901 17.430  
 Low 17.728 17.257 16.976



**RTC Battery**

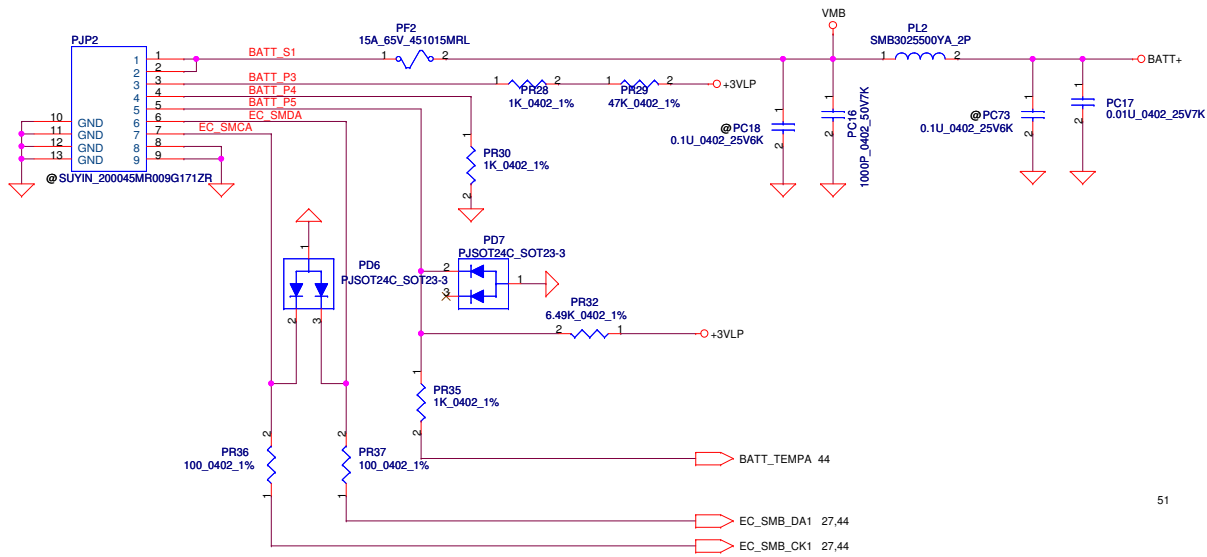


**Precharge detector**  
 15.97V/14.84V FOR ADAPTOR



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				<b>DCIN / DETECTOR</b>	
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<b>Size</b>	Document Number	NBQAA DIS		<b>Rev</b>	1.0
<b>Date:</b> Monday, March 22, 2010		<b>Sheet</b> 48		<b>of</b> 61	



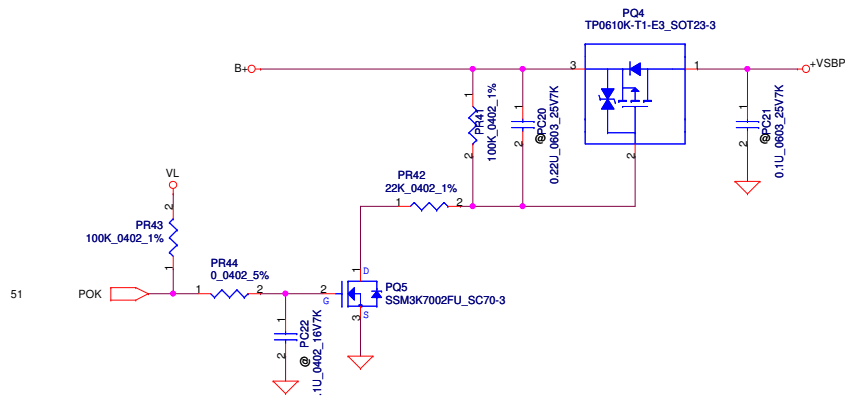
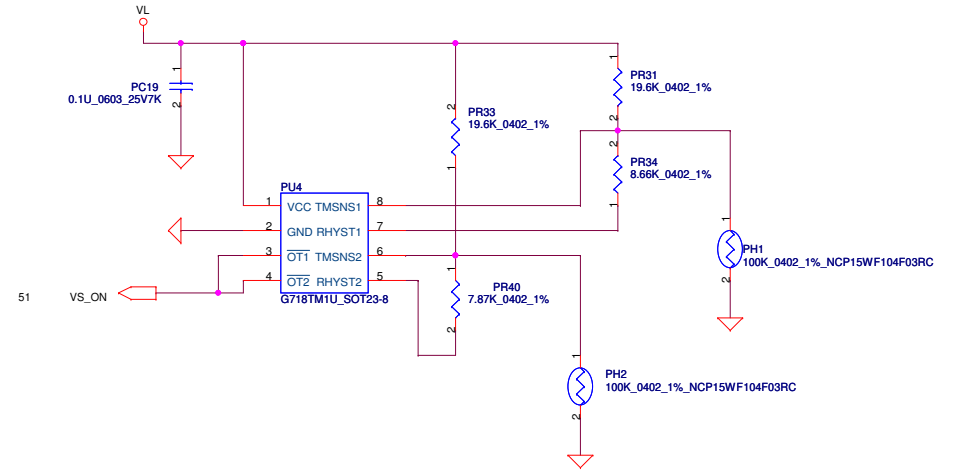


**PH1 under CPU botten side :**

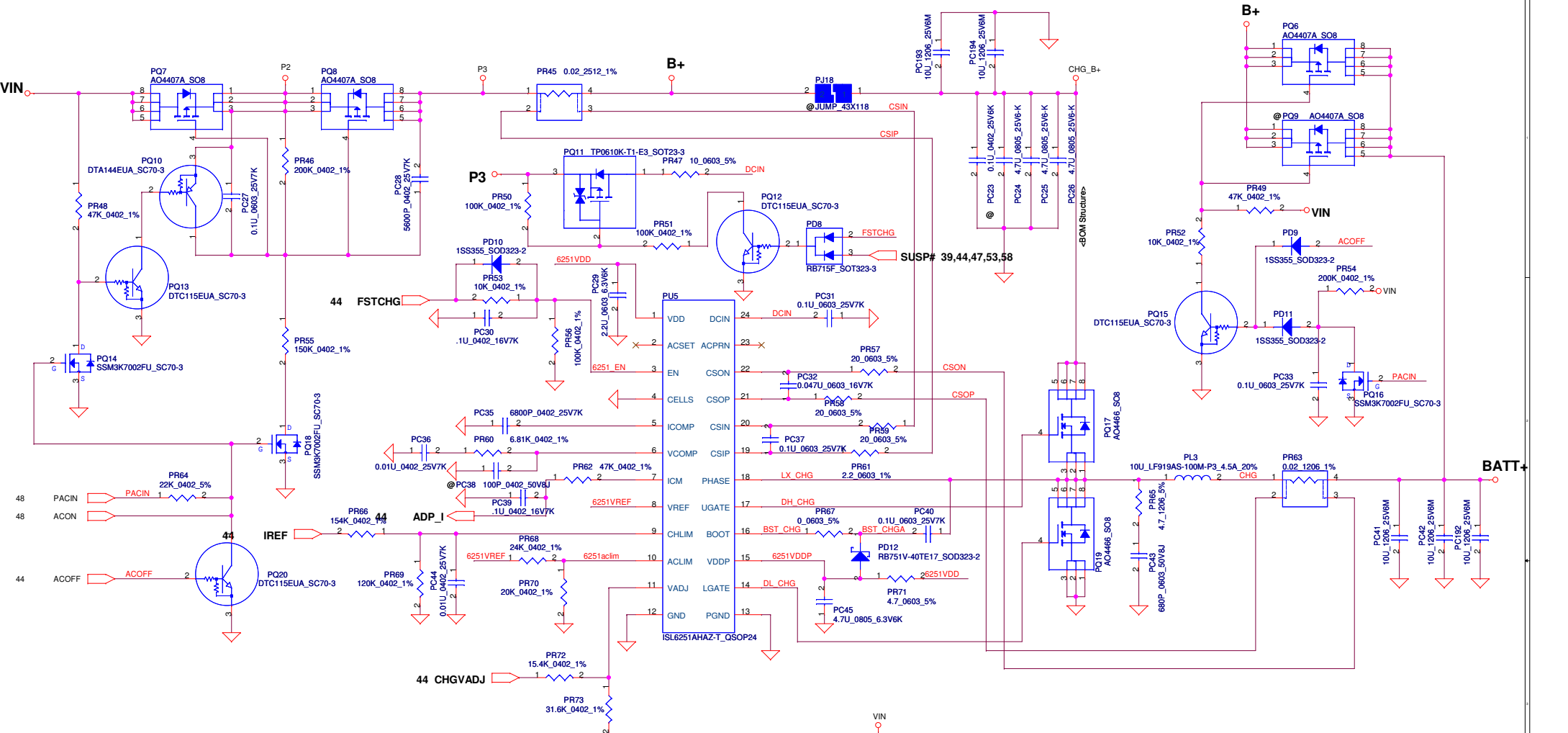
CPU thermal protection at 95 degree C  
Recovery at 56 degree C

**PH2 near main Battery CONN :**

BAT. thermal protection at 95 degree C  
Recovery at 48 degree C



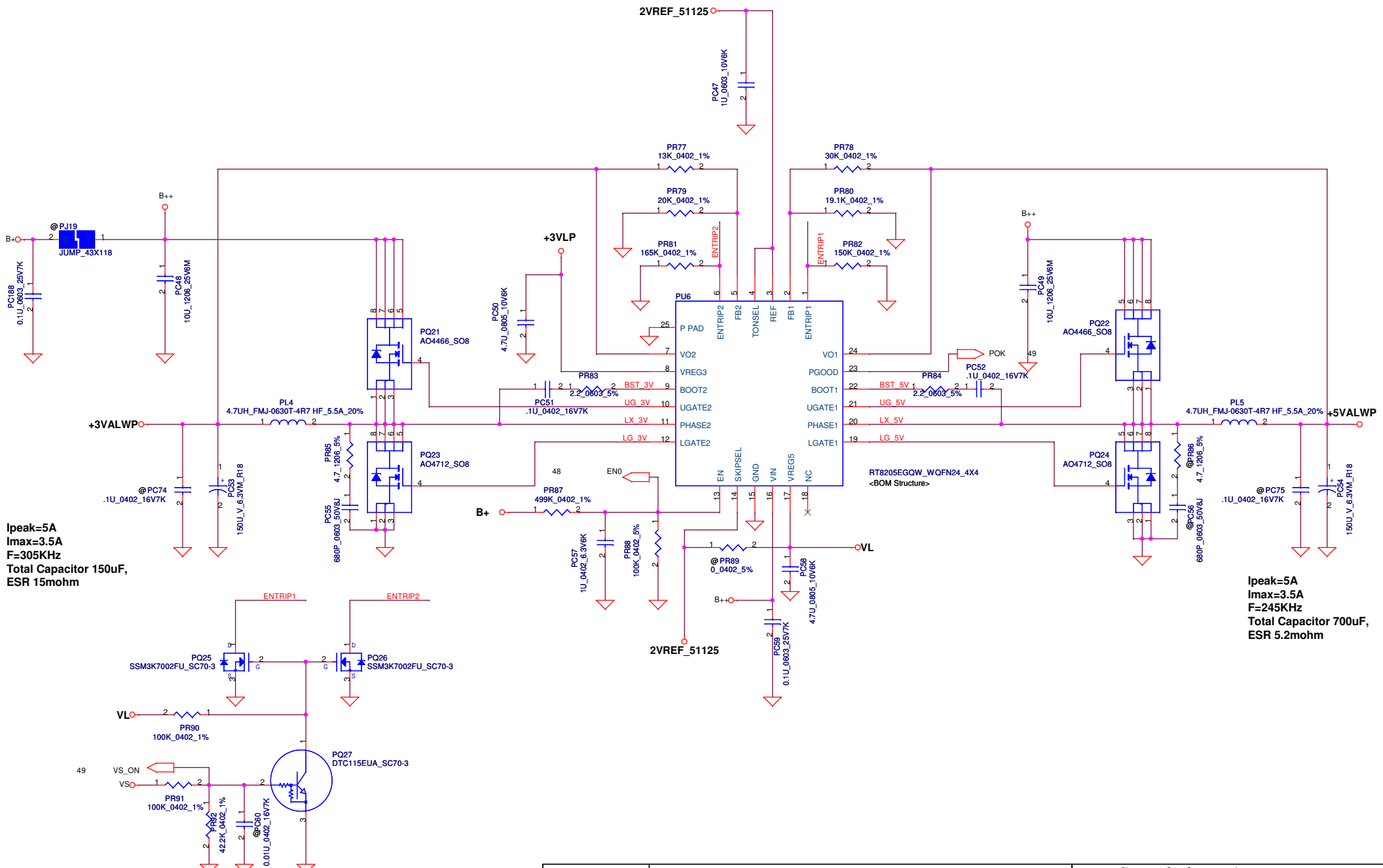
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CP mode  
 $I_{ada} = 0 \sim 4.737A$  (90W) CP =  $92\% \cdot I_{ada}$ ; CP = 4.36A  
 $V_{clim} = 0.736V$  (90W) PR70 = 53.6k PR49 = 0.015

CC = 0.25A - 3A  
 $I_{REF} = 1.016 \cdot I_{charge}$   
 $I_{REF} = 0.254V \sim 3.048V$   
 VCHLIM need over 95mV

CHGVADJ = (Vcell - 4) / 0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V



**i<sub>peak</sub>=5A**  
**Im<sub>ax</sub>=3.5A**  
**F=305KHz**  
**Total Capacitor 150uF,**  
**ESR 15mohm**

**i<sub>peak</sub>=5A**  
**Im<sub>ax</sub>=3.5A**  
**F=245KHz**  
**Total Capacitor 700uF,**  
**ESR 5.2mohm**

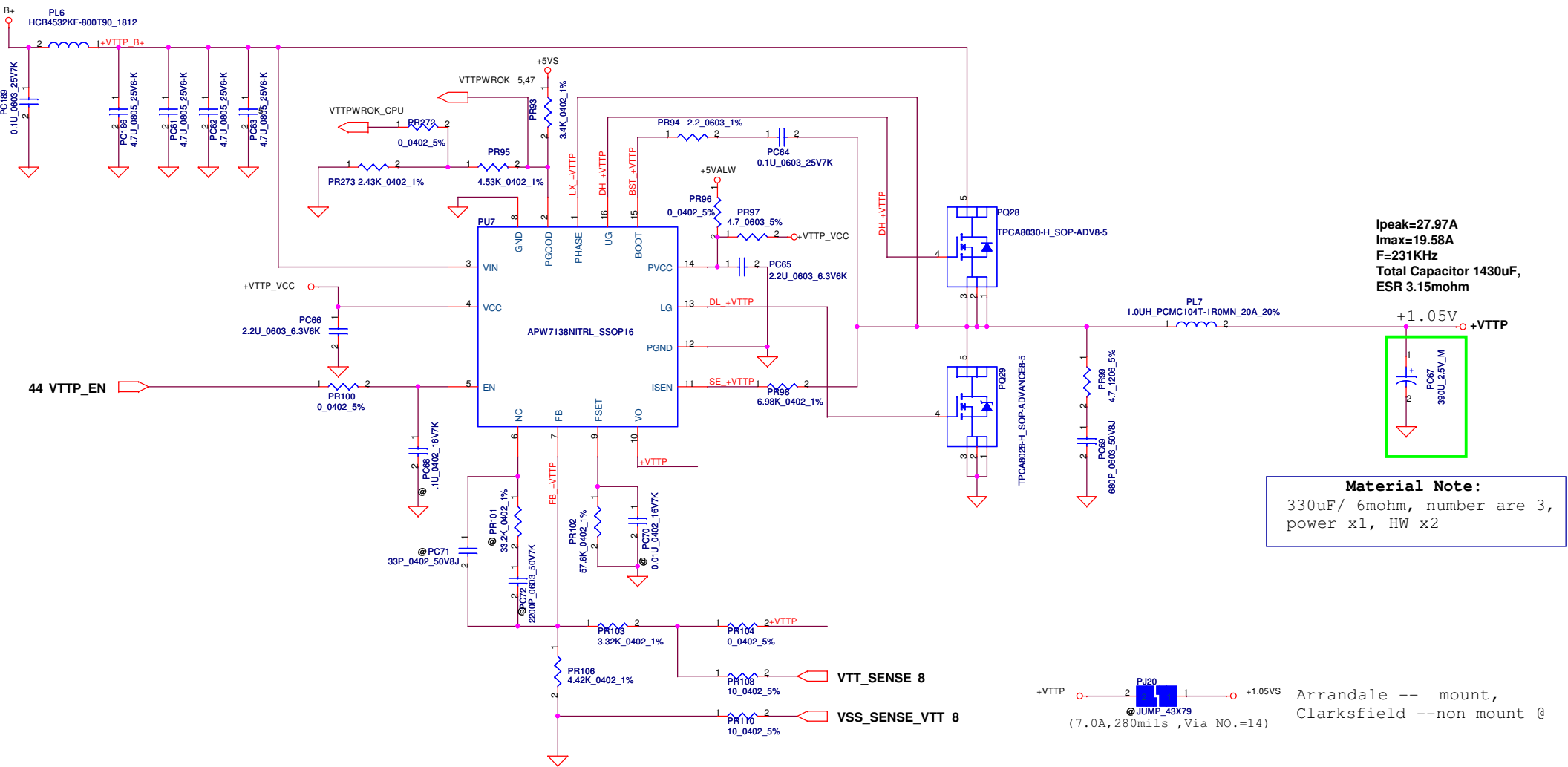
Security Classification		Compal Secret Data		Title	
Issued Date	2009/11/13	Deciphered Date	2010/10/21	3VALWP/5VALWP	
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**Compal Electronics, Inc.**

**3VALWP/5VALWP**

NBQAA 1.0

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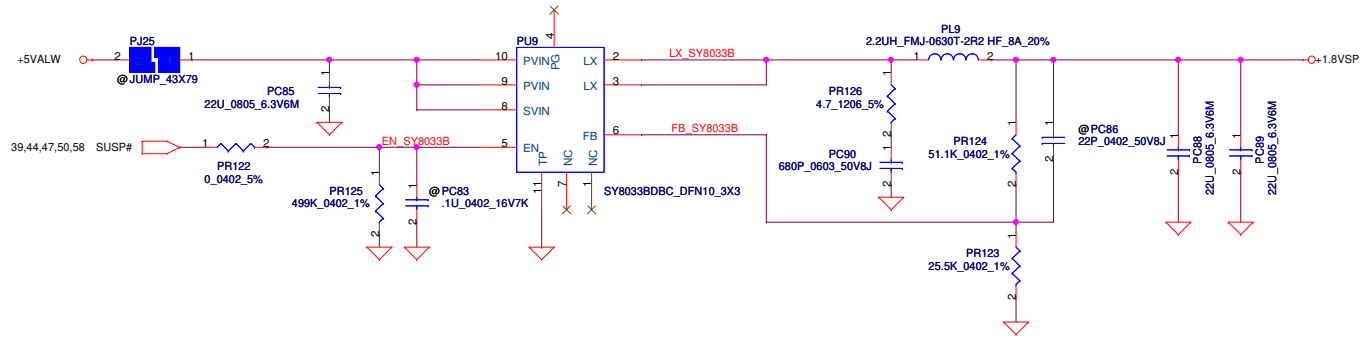
Ipeak=27.97A  
 Imax=19.58A  
 F=231KHz  
 Total Capacitor 1430uF,  
 ESR 3.15mohm

**Material Note:**  
 330uF/ 6mohm, number are 3,  
 power x1, HW x2

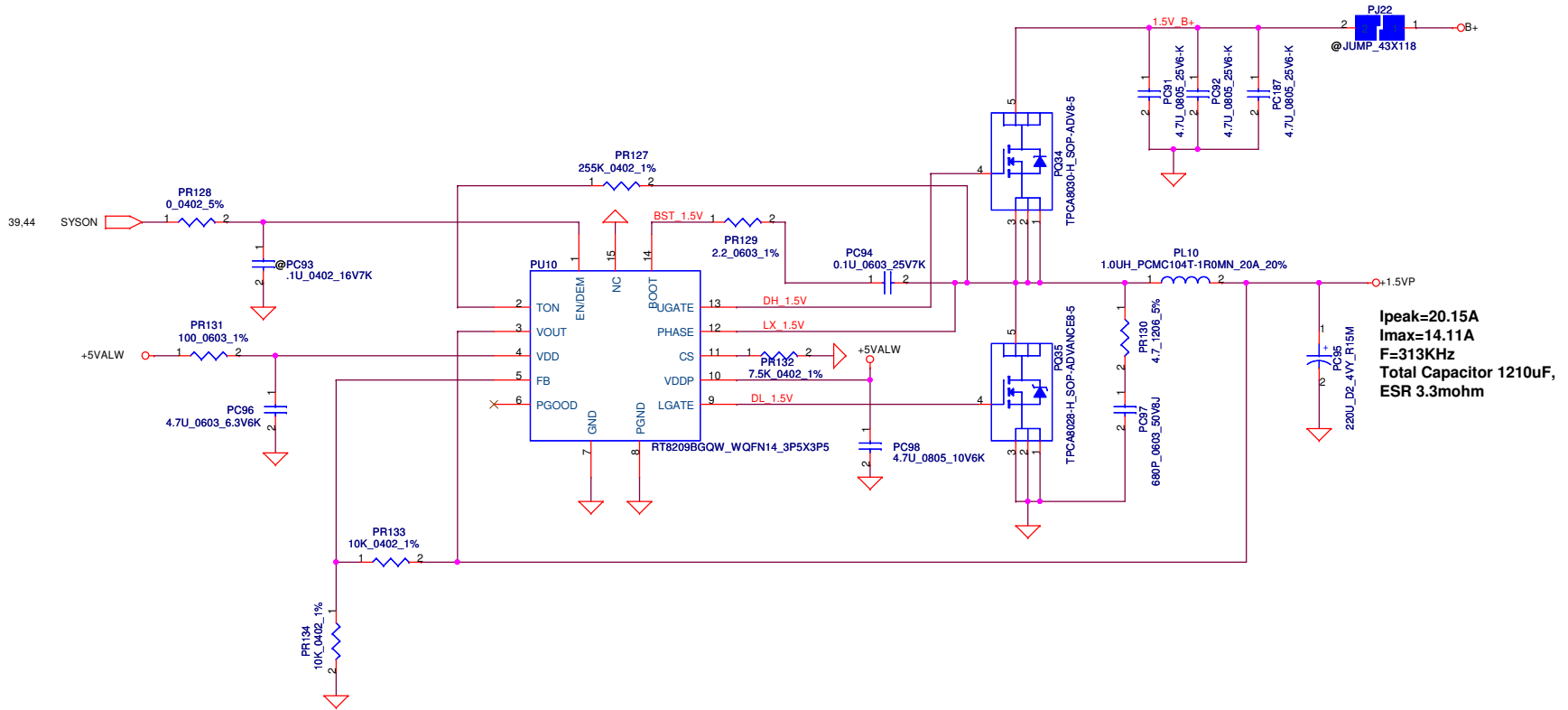
Arrandale -- mount,  
 Clarksfield --non mount @

PJ20  
 @ JUMP\_43X79  
 (7.0A, 280mils ,Via NO.=14)

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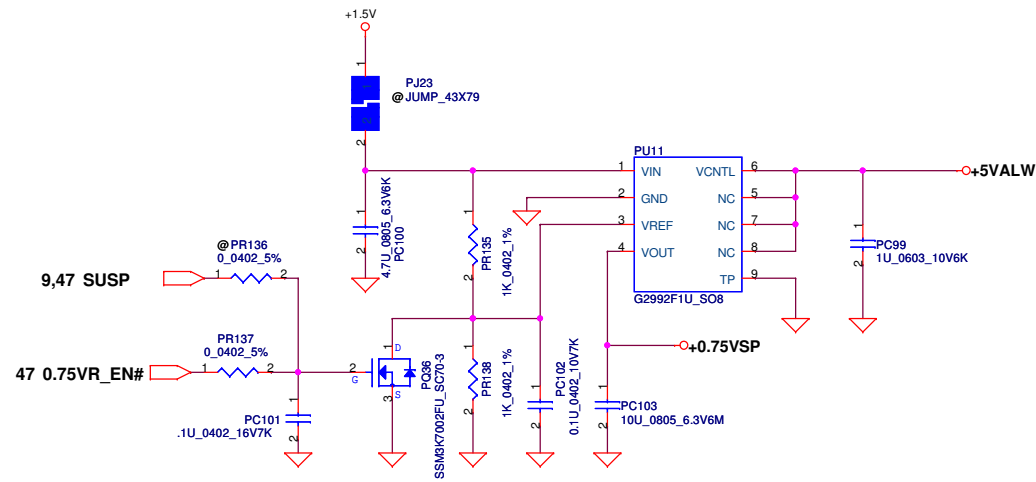


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Title				+1.8VSP	
Size	Document Number			Rev	
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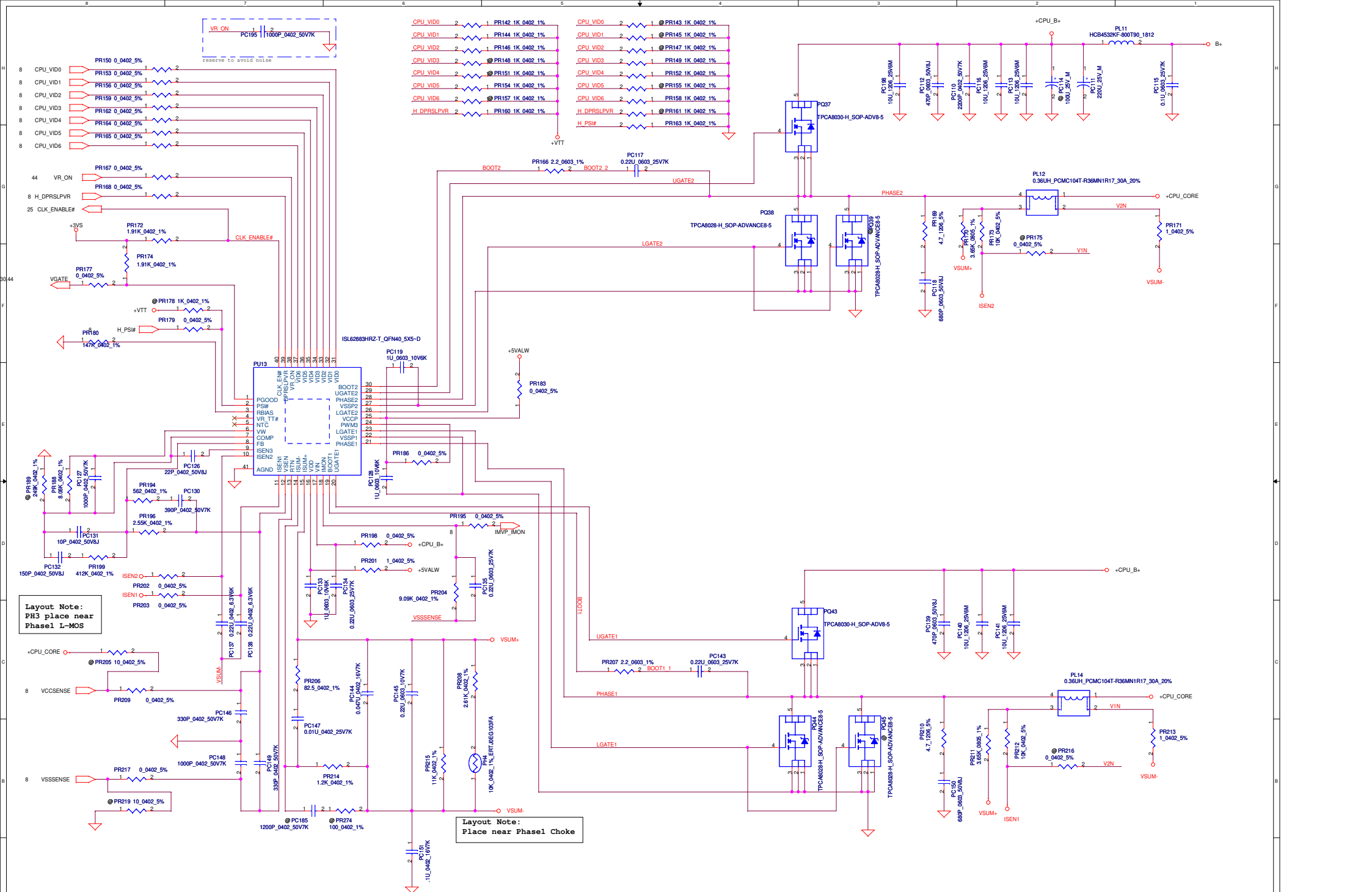


**I<sub>peak</sub>=20.15A**  
**I<sub>max</sub>=14.11A**  
**F=313KHz**  
**Total Capacitor 1210uF,**  
**ESR 3.3mohm**

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Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b>	
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Date: Monday, March 22, 2010				Sheet	55 of 61

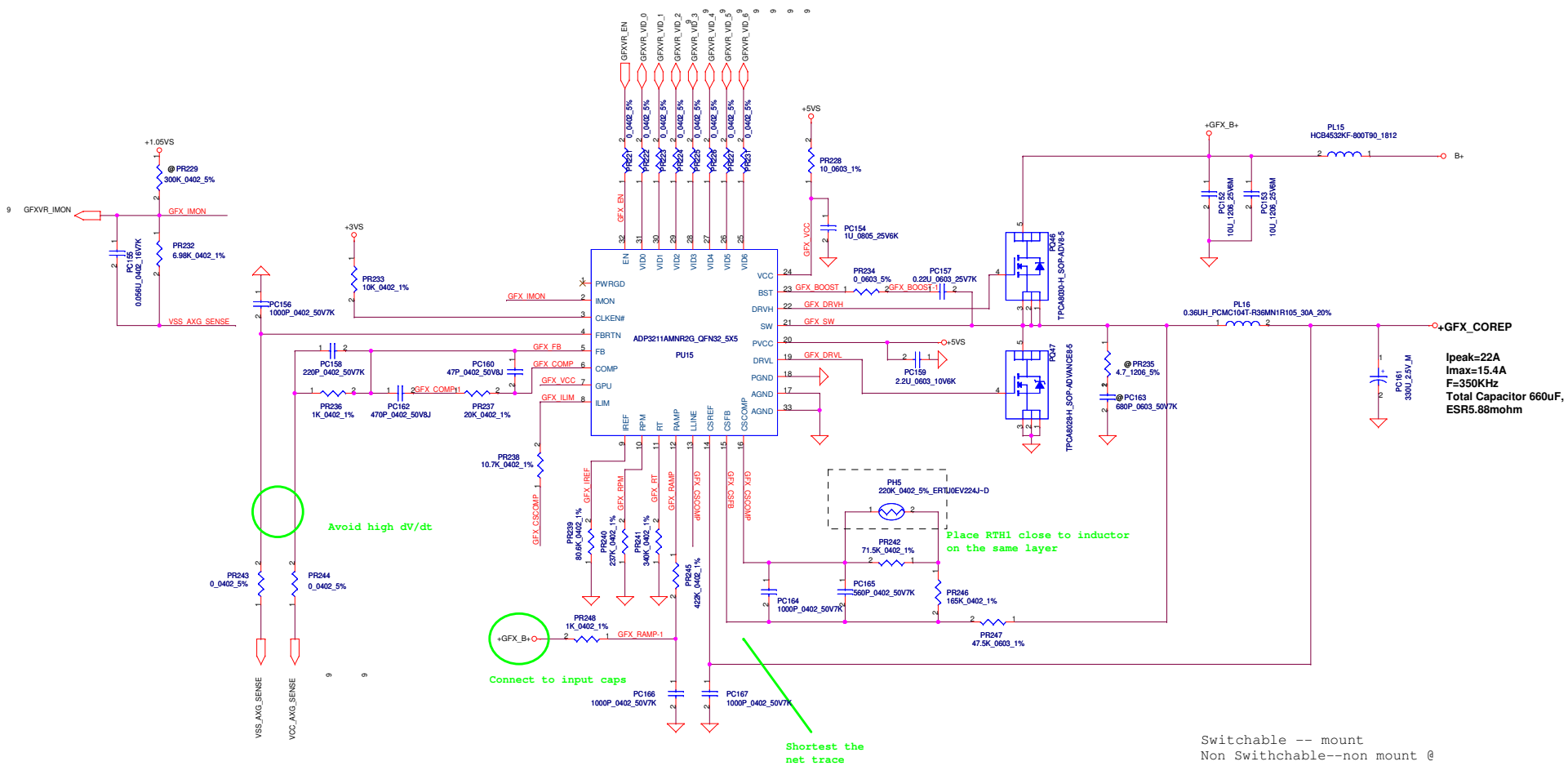


Layout Note:  
PH3 place near  
Phasel L-MOS

Layout Note:  
Place near Phasel Choke

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Avoid high dV/dt

Connect to input caps

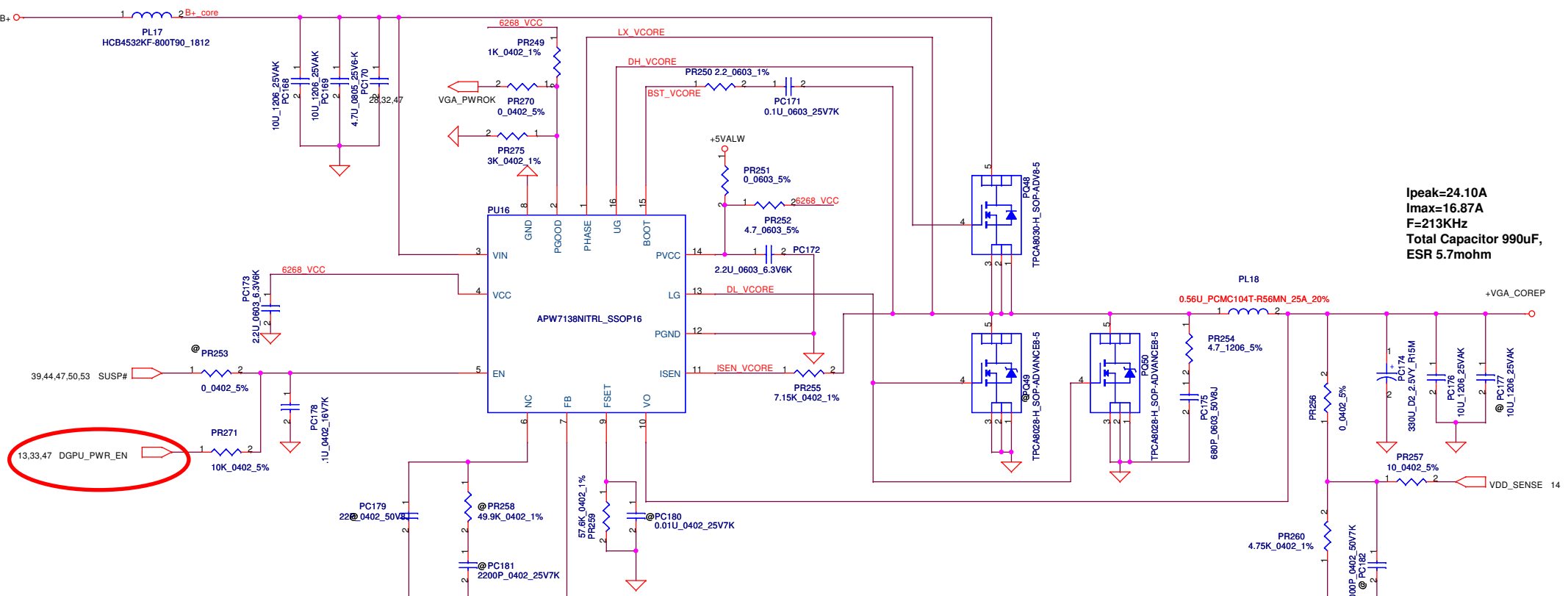
Shortest the net trace

Place RTH1 close to inductor on the same layer

Switchable -- mount  
Non Switchable--non mount @

Ipeak=22A  
Imax=15.4A  
F=350KHz  
Total Capacitor 660uF,  
ESR5.68mohm

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Ipeak=24.10A  
 Imax=16.87A  
 F=213KHz  
 Total Capacitor 990uF,  
 ESR 5.7mohm

13.33,47 DGPU\_PWR\_EN

FSW=1/(75E-12\*57.6K)=231.48KHz

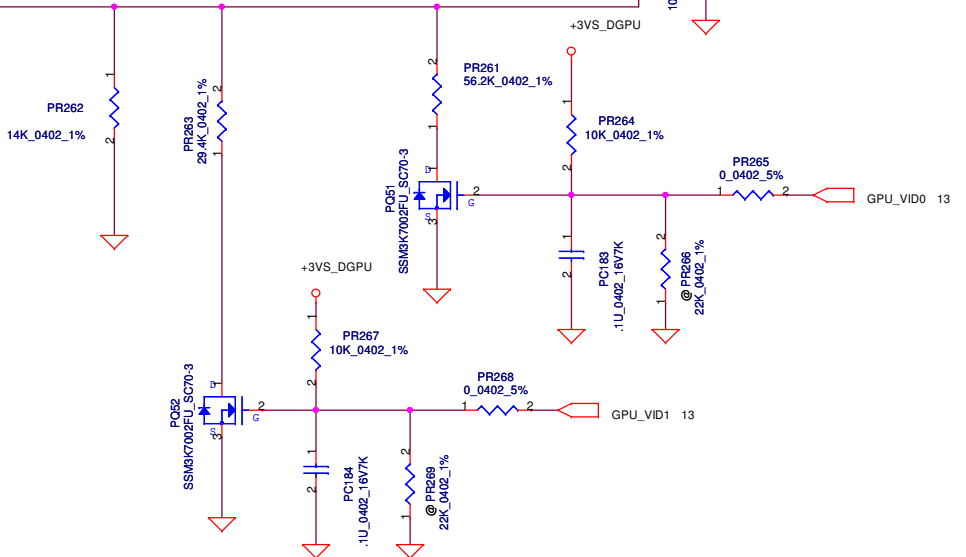
N11P	N11M
Imax=16.87A Ipeak=24.10A Iocp=28.65A	Imax=12.73A Ipeak=18.19A Iocp=20.48A
PR255=7.15K PQ49=unpop	PR255=5.36K PQ49=unpop

VFB(0.6)=Vout\*Rbottom/(Rtop+Rbottom)

GPU_VID0	GPU_VID1	N11M-OP1	N11P
0	0		0.80V
1	0	0.85V	0.85V
0	1		1.03V
1	1	1.03V	

PR260= 4.75K	PR260= 4.75K
PR262 =14K	PR262 =14K
PR261 =56.2K	PR261 =56.2K
PR263=16.2K	PR263=29.4K



NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
2009/12/06		P48-59	Release	
2009/12/18		P49	PR31,PR33,PR34,PR40	PH1,PH2 setting point change
2009/12/18		P52	PR98	VTT adjust OCP
2009/12/18		P55	Remove PR136,Add PR137,PC101	0.75VSP Enable signal (EVT added by memo)
2009/12/18		P58	Add PR254,PC175	VGA add snubber (EVT added by memo)
2009/12/18		P58	PC174	VGA output cap change to lower
2009/12/28		P51,P52	Add PC188,PC189,PC115	Add EMC,EMI solution.
2009/12/28		P51	change PR83,PR84,Add PR85,PC55	For EMI,EMC solution
2010/01/06		P51	PR81,PR132,PR255	OCP setting.
2010/01/06		P58	change PR249,PR271,PC178	HW request
2010/02/05		P53	change PU9 solution	change 1.8V Solution
2010/02/05		P51	change PL4,PL5	Change to lower height to solve ME request
2010/01/28		P43	PC197	Reserve 10uF at B+ shape for ripple improvement.
2010/02/08		P50	Add PD6,PD7	ESD solution.
2010/02/08		P57	Change PR247	GFX load-line
2010/02/08		P50	Add PC192,PC193,PC194	ISN issue
2010/03/16		P50	Change PR45,PR68	CP setting
2010/03/16		P50	Change PL3	ME issue
2010/03/16		P51	Change PC53,PC54	ME issue
2010/03/16		P53	PR122,PC83 unmount	1.8V enable signal adjust
2010/03/16		P56	Add PC195	VR_ON prevent noise,same as UMA
2010/03/16		P58	Change PC174	ME issue
2010/03/16		P58	Change PR264,PR265,PR267,PR268,PR263,PC184,PQ52	GPU voltage adjust
2010/03/18		P57	Add PC198	High frequency noise
2010/03/22		P58	Add PR275	Adjust VGA POK voltage level for HW request

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**PIR (Product Improve Record)**  
**NBQAA LA-6072P SCHEMATIC CHANGE LIST**

REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	12/22	25	Change JLVDS routing	To prevent workmanship and burn issue
2.	12/22	09	Change Q33 routing	For common design
3.	12/22	47	Change Q43 routing	For common design
4.	12/22	39	Change JEXP footprint to SANTA_130861-2_26P_RT-T	Modify footprint
5.	12/22	38	Change JTPL footprint to P-TWO_161021-06021_6P-T	For ME's request
6.	12/22	43	Change JKBL footprint to ACES_85201-04051_4P-T	For ME's request
7.	12/22	13	Delete DV2, Add RV124, QV2 for CLKREQ_VGA#	CLKREQ_VGA# circuit for NV's Optimus
8.	12/23	38	Change JCS footprint to P-TWO_161021-10021_10P-T	For ME's request
9.	12/23	38	Change JTOUCH footprint to P-TWO_161021-10021_10P-T	For ME's request
10.	12/23	33	Change PCH's GPIO57 netname to OPTIMUS_EN# and pull down to GND	For BIOS recognizing Optimus
11.	12/23	33	Change PCH's GPIO45 netname to LVDS_SEL	For Common design
12.	12/23	33	Change PCH's GPIO39 netname to CIR_EN#	For Common design
13.	12/24	39	Add DM2, QM1, BT_CTRL on JWLAN.5	For WLAN/BT combo module
14.	12/24	42	Add RA43 on EC_MUTE#	For Audio issue
15.	12/24	43	Detetele JEXMIC.5 from GND	For Audio issue
16.	12/24	44	Change PWRME_CTRL to PWRME_CTRL#	Active low signal
17.	12/24	33	Delete GND guide pins of JTOUCH, JCS, JTPL, JODD1	For common design
18.	12/29	29	Add C254 on CLKREQ_WLAN#	For EMI's Request
19.	12/29	43	Exchange JKBL pin1 and pin4	To meet correct footprint
20.	12/29	37	Add C389 on U14	For EMI's Request
21.	12/29	46	Add C392 on H21 for +5VALW	For EMI's Request
22.	12/29	40	Stuff CL7, CL23, CL24	For EMI's Request
23.	12/29	46	Add C393, close to C7 for +3VS	For EMI's Request
24.	12/29	32	Add R55 on DGPU_RST#	For common design
25.	12/29	27	Add R314 on HDMI_HPD and U9	To prevent ESD damage to U9
26.	01/03	47	change +1.05VS_DGPU routing	To turn on/off normally

REVISION CHANGE: 0.2 TO 0.3

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	02/01	31	Change RA40 to pull up +5VL	Support S/M function in battery mode
2.	02/01	30	Change RA34 to pull up +3VL	Support S/M function in battery mode
3.	02/01	44	Add R103 to USB_EN# and pull up +5VALW	For common code with NBQAA
4.	02/01	44	Add R69 to VR_ON and pull low to GND	To avoid folating when EC is on initial
5.	02/01	30	Add C434 to VGATE	Reserve to avoid noise
6.	02/01	05	Add C482 to H_PWRGOOD	Reserve to avoid noise
7.	02/01	40	Add UL4	for 10/100/1000 transformer co-layout
8.	02/01	38	Add MDC circuits	For A51's request, Add MDC in DIS SKU
9.	02/01	35	Reserve U54 for +1.5VALW LDO and change VCCSUSHDA power rail	For MDC design change
10.	02/01	28	Add R287, R289, R291, R293 for Azalia bus to MDC	For MDC design change
11.	02/02	46	Add H31, H32	For MDC design change
12.	02/02	44	Add CAP_RST# on EC pin73 and link to JCS	For Cap sensor design change
13.	02/04	31	Stuff R133, R135 to 100Kohm PD GND	To prevent PCH pending internal HPD
14.	02/04	14	Reserve UV4, RV54, CV56, RV44	Reserved for VBIOS
15.	02/04	42	Add RA45, un-stuff RA43	To solve audio issue
16.	02/06	32	Exchange USB port 4&8	Design change, for A51's request
17.	02/08	08	Change C117, C118, C119, C120, C127, C128, C129	To improve ESD
18.	02/08	40	Change LL1, CL13	For design change
19.	02/09	41	Change RC7, RC8, RC9, RC12, RC13, RC14 from 0 ohm to 22 ohm	For EMI's request

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# PIR (Product Improve Record)

## NBQAA LA-6072P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.3 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	03/11	27	Add R148	To solve display compatibility issue
3.	03/11	15	Change CV58 from OSCON to POLY type	Due to the keyboard stress test is fail
4.	03/11	09	Change C216 from OSCON to POLY type	Due to the keyboard stress test is fail
5.	03/11	11	Change C163 from OSCON to POLY type	Due to the keyboard stress test is fail
6.	03/11	14	Delete UV4, RV54, CV56, RV44	Design change, no need extra BIOS ROM
7.	03/11	25	Stuff D84, D82, D19, D83	For ESD's request
8.	03/11	34	Change L12 from bead to R389 2.2 ohm+- 1%	For CRT issue
9.	03/14	13	Reserve YV1, RV29, CV45, CV46	Reserved for design change
10.	03/14	33	Change R221 to 1K ohm	For NV's Optimus sequence
11.	03/14	32	Change R55 to 1K ohm	For NV's Optimus sequence
12.	03/14	32	Reserve R334, add R336	For NV's Optimus sequence
13.	03/14	39	Change QM1 to Q14B	For cost down
14.	03/15	42	Un-mount CA16	For audio noise issue
15.	03/15	46	Un-mound SW2, SW3	Power button is no need after pre-MP
16.	03/16	42	Change CA12.1, RA12.2, CA18.2 from GND to AGND	For audio noise issue
17.	03/16	42	Change CA9 and CA10 to from 4700pF tp 1uF	For audio noise issue
18.	03/16	42	Add CA34-CA40 and CA51	For audio noise issue
19.	03/18	41	Change Card reader solution from O2 to JMB389C/385C	For design change
20.	03/19	27	Add D54	For HDMI CEC
21.	03/19	34	Add L12 that reserved 0 ohm for EMI	For CRT issue
22.	03/19	46	H22 from 6.0 to 3.0	For ME's request
23.	03/20	20	Change BIOS ROM footprint to M25P80-VMW6TP_S08	No need the debug connector in MP phase
24.	03/22	13	Stuff RV28, un-stuff RV105	Reserved for 27M_SSC from clock gen
25.	03/22	43	Add RA22, RA23	Reserved to solve GPRS noise
26.	03/22	05	Stuff C482	To avoid noise
27.	03/22	30	Stuff C434	To avoid noise

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