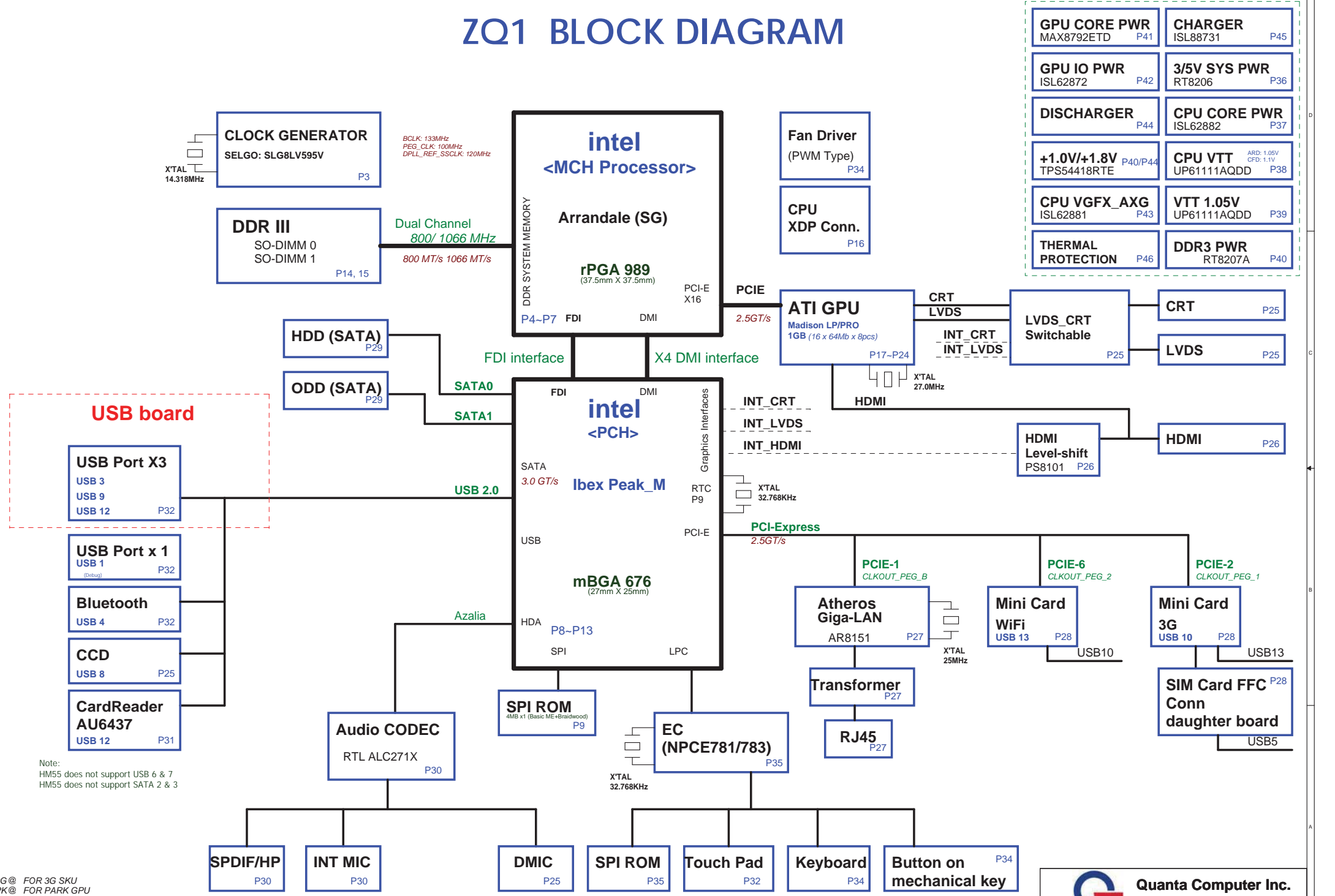



ZQ1 BLOCK DIAGRAM



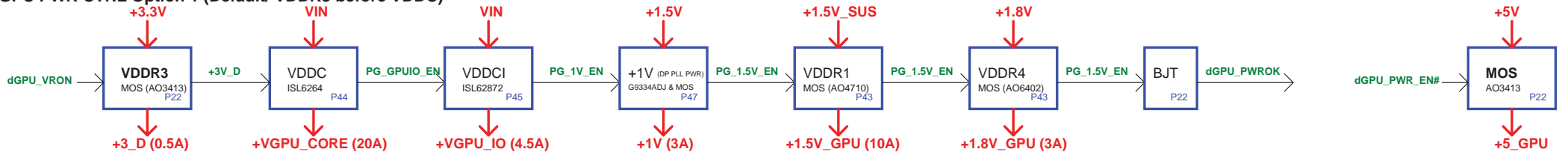
Note:
 HM55 does not support USB 6 & 7
 HM55 does not support SATA 2 & 3

3G@ FOR 3G SKU
 PK@ FOR PARK GPU
 MD@ FOR MADSION GPU
 IV@ FOR UMA
 SW@ FOR SWITCHABLE GRAPHIC

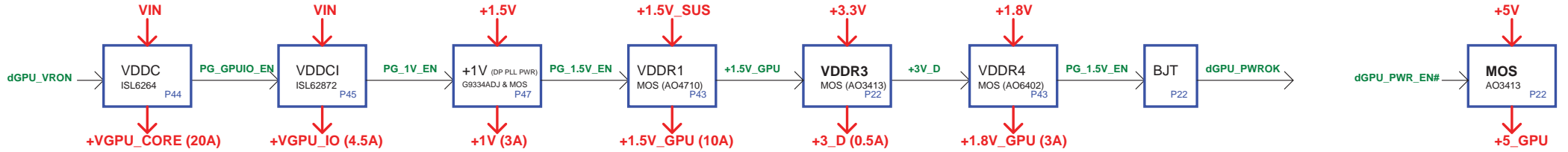
<http://laptop-motherboard-schematic.blogspot.com/>

| | | | | |
|--|------------------------------|-------|-----------------|-------|
|  Quanta Computer Inc. PROJECT : ZQ1 | | Size | Document Number | Rev |
| | | | | 1A |
| Block Diagram | | | | |
| Date: | Wednesday, December 16, 2009 | Sheet | 1 | of 48 |

GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDR1)



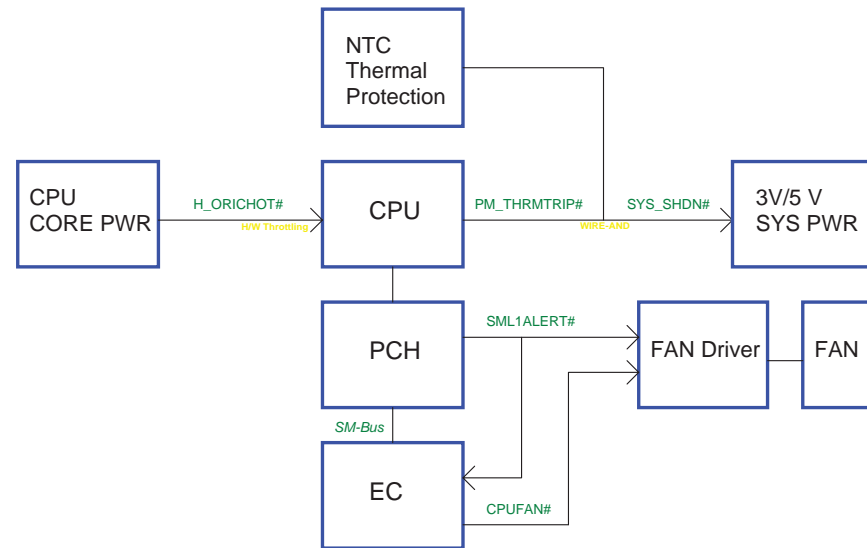
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



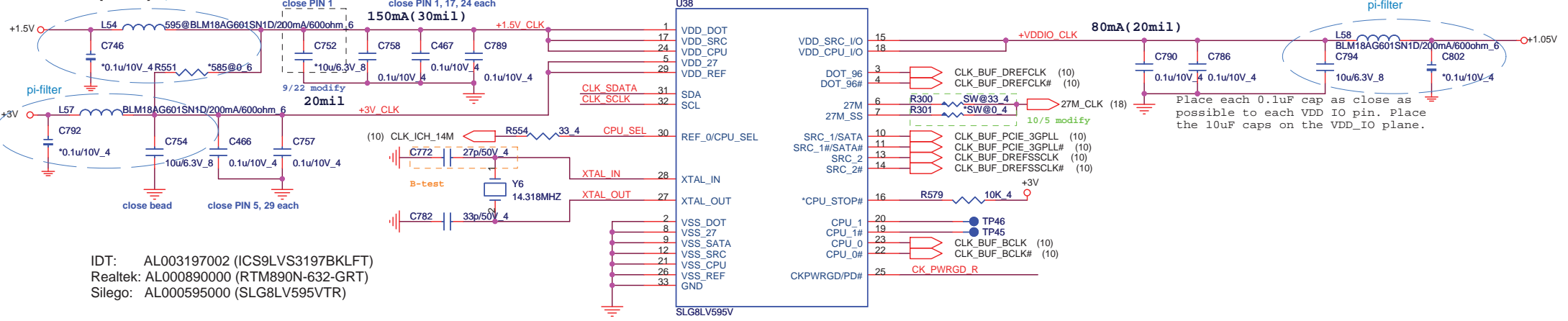
Power States

| POWER PLANE | VOLTAGE | DESCRIPTION | CONTROL SIGNAL | ACTIVE IN |
|----------------|--------------|----------------|----------------|-----------|
| VIN | +10V~+19V | MAIN POWER | | S0-S5 |
| +RTC_CELL | +3V~+3.3V | RTC | | S0-S5 |
| +3VPCU | +3.3V | 8051 POWER | ALWON | S0-S5 |
| +5VPCU | +5V | CHARGE POWER | ALWON | S0-S5 |
| +15V | +15V | LARGE POWER | +15V_ALWP | S0-S5 |
| 3V_LAN_S5 | +3.3V | LAN POWER | AUX_ON | |
| +5VSUS | +5V | | SUSD | |
| +3VSUS | +3.3V | | SUSD | |
| +1.5V_SUS | +1.5V | SODIMM POWER | SUSON | |
| +0.75V_DDR_VTT | +0.9V | SODIMM POWER | MAINON | |
| +5V | +5V | | MAIND | |
| +3V | +3.3V | | MAIND | |
| +1.8V | +1.8V | | MAINON | |
| +1.5V | +1.5V | PCH POWER | MAIND | |
| +1.1V_VTT | +1.05V~+1.1V | CPU POWER | MAINON | |
| +1.05V | +1.05V | PCH POWER | MAINON | |
| +VCC_CORE | 0V~+1.5V | CPU CORE POWER | VRON | |
| LCDVCC | +3.3V | LCD Power | LVDS_VDDEN | |
| MBAT+ | +10V~+17V | MAIN BATTERY | | |
| +5V_S5 | +5V | | S5_ON | |
| +3V_S5 | +3.3V | | S5D | |

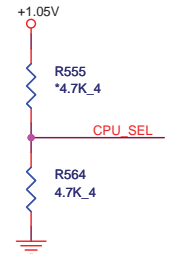
Thermal Follow Chart



CLK Gen(CLK)

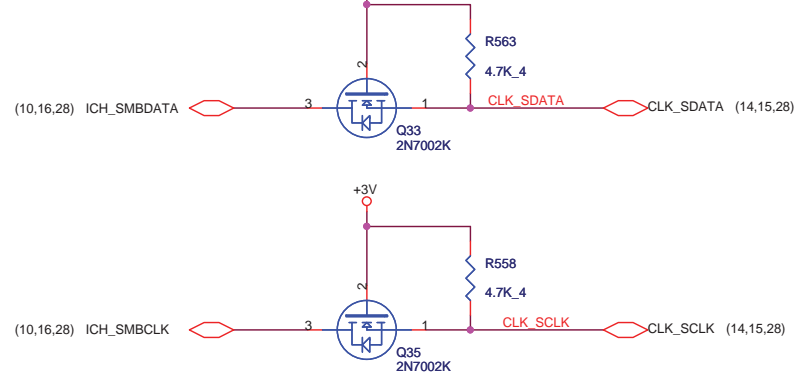


CPU_CLK select(CLK)

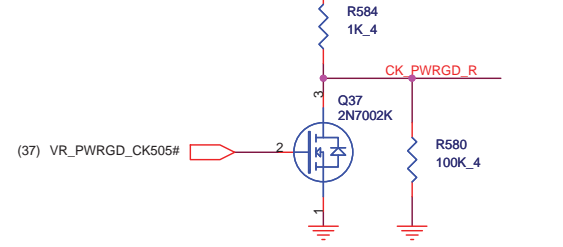



| | | |
|---------|-------------------------|---------------|
| | 0 | 1 |
| CPU_SEL | CPU0/1=133MHz (default) | CPU0/1=100MHz |

SMBus(CLK)



CLK Enable(CLK)

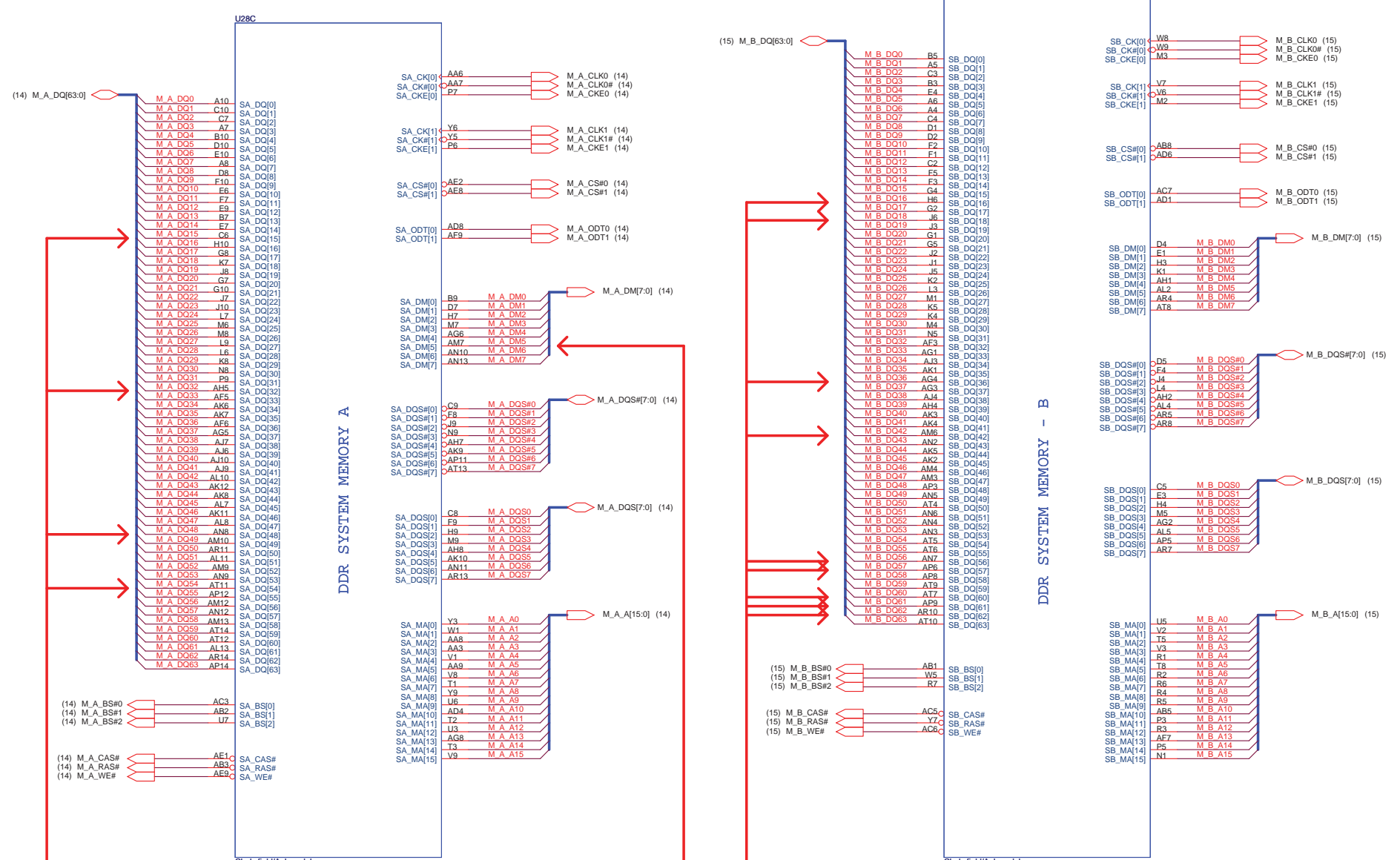




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| | | |
|-------|--------------------------|---------------|
| Size | Document Number | Rev |
| | Clock Generator | 1A |
| Date: | Friday, January 22, 2010 | Sheet 3 of 48 |



Channel A DQ[15,32,48,54], DM[5]
 Requires minimum 12mils spacing
 with all other signals, including data signals.

Channel B DQ[16,18,36,42,56,57,60,61,62]
 Requires minimum 12mils spacing
 with all other signals, including data signals.

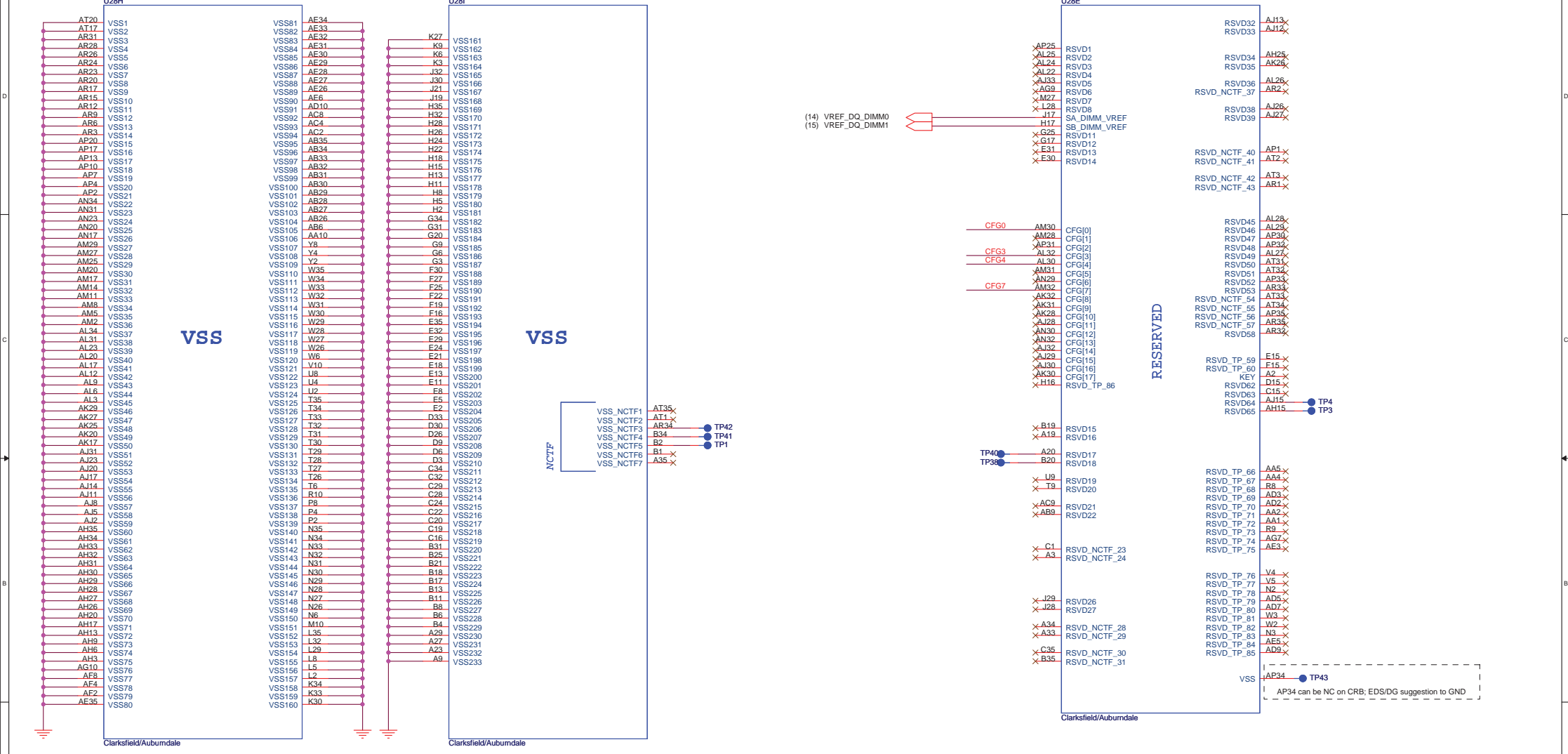
Quanta Computer Inc.
 PROJECT : ZQ1

| | | |
|-------|--------------------------|---------------|
| Size | Document Number | Rev |
| | AUBURNDA 2/4 | 1A |
| Date: | Friday, January 22, 2010 | Sheet 5 of 48 |

Arrandale_4(CPU)

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

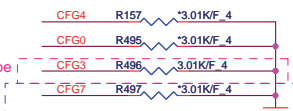
AUBURNDALE/CLARKSFIELD PROCESSOR (RESERVED, CFG)



Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

| | 1 | 0 |
|--|--|--|
| CFG4 (Display Port Presence) | Disabled; No Physical Display Port attached to Embedded Display Port | Enabled; An external Display port device is connected to the Embedded Display port |
| CFG0 (PCI-Epress Configuration Select) | Single PEG | Bifurcation enabled |
| CFG3 (PCI-Epress Static Lane Reversal) | Normal Operation | Lane Numbers Reversed |

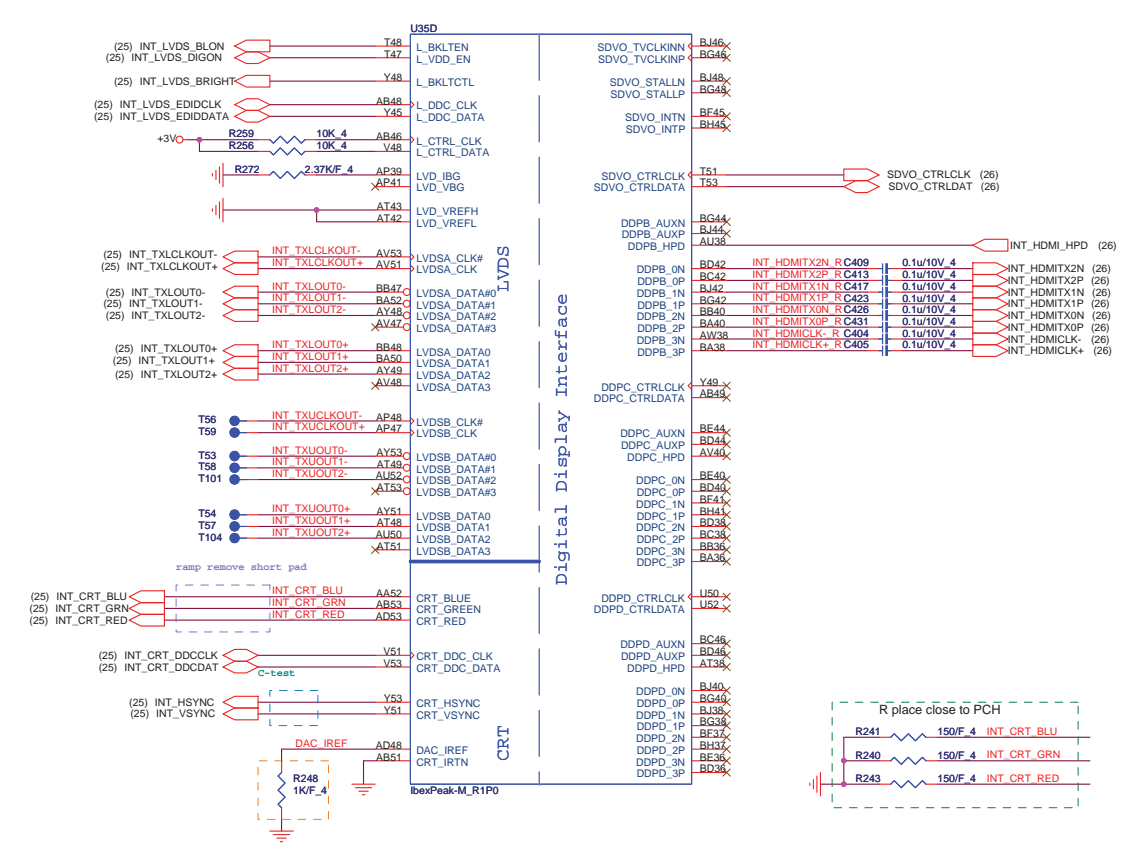
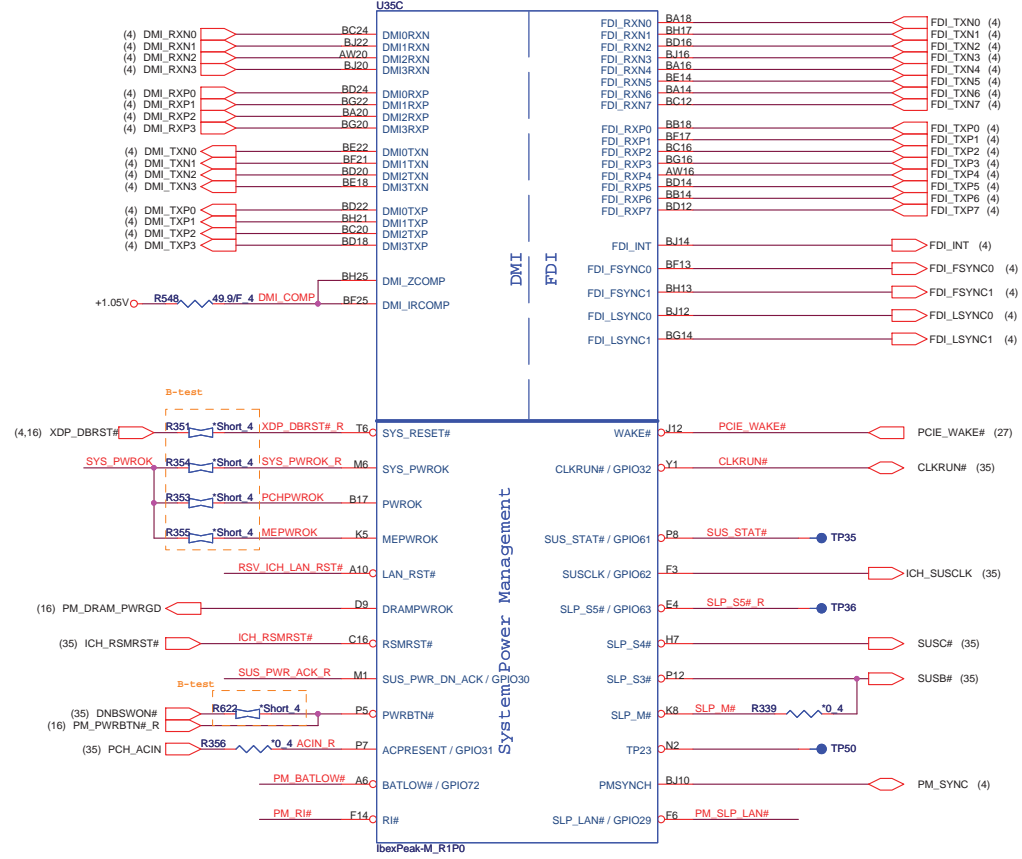
CFG[1:0] - PCI_Epress Configuration Select
 * 11= 1 x 16 PEG
 * 10= 2 x 8 PEG



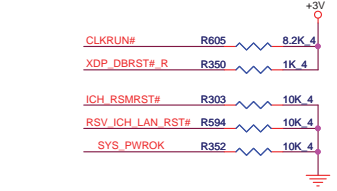
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01k +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed. (ES1 only)

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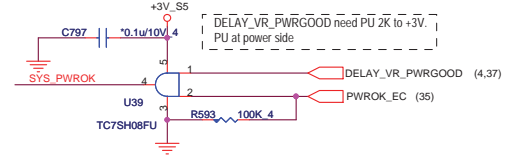
| | | |
|-------|--------------------------|---------------|
| Size | Document Number | Rev |
| | AUBURND4/4 | 1A |
| Date: | Friday, January 22, 2010 | Sheet 7 of 48 |



PCH Pull-high/low(CLG)



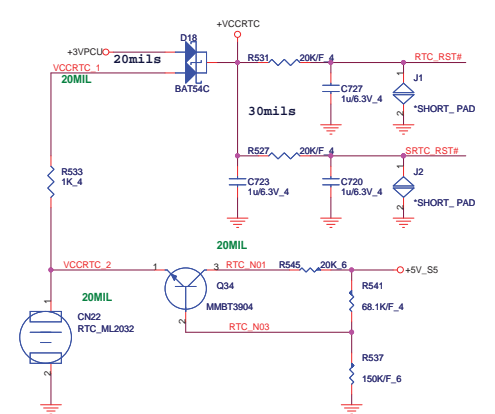
System PWR_OK(CLG)



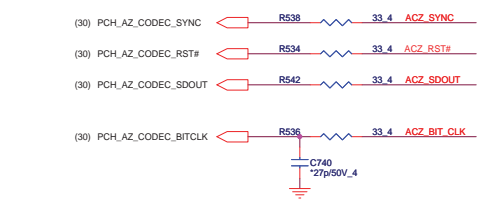
Quanta Computer Inc.
PROJECT : ZQ1

| | | |
|-------|--------------------------|---------------|
| Size | Document Number | Rev |
| | IBEX PEAK-M /16 | 1A |
| Date: | Friday, January 22, 2010 | Sheet 8 of 48 |

RTC Circuitry(RTC)

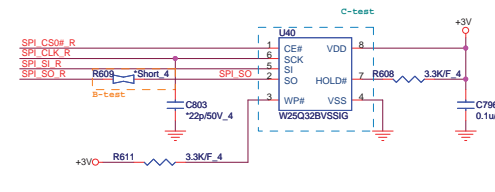


HDA Bus(CLG)

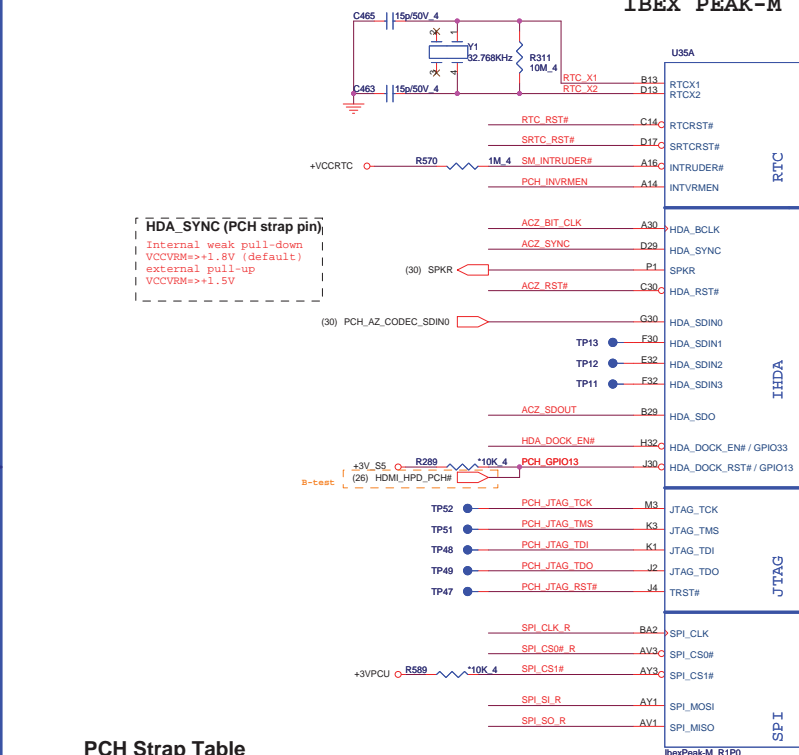


Place all series terms close to PCH except for SDIN input lines, which should be close to source. Placement of R should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

PCH SPI(CLG)



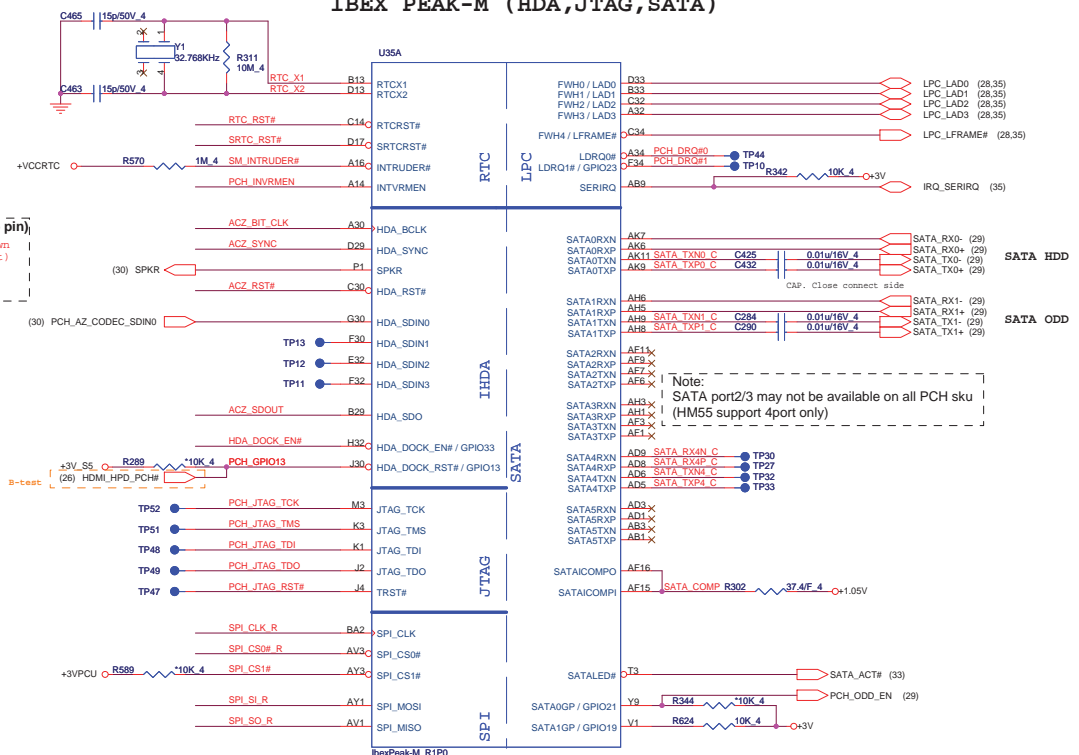
PCH2(CLG)



PCH Strap Table

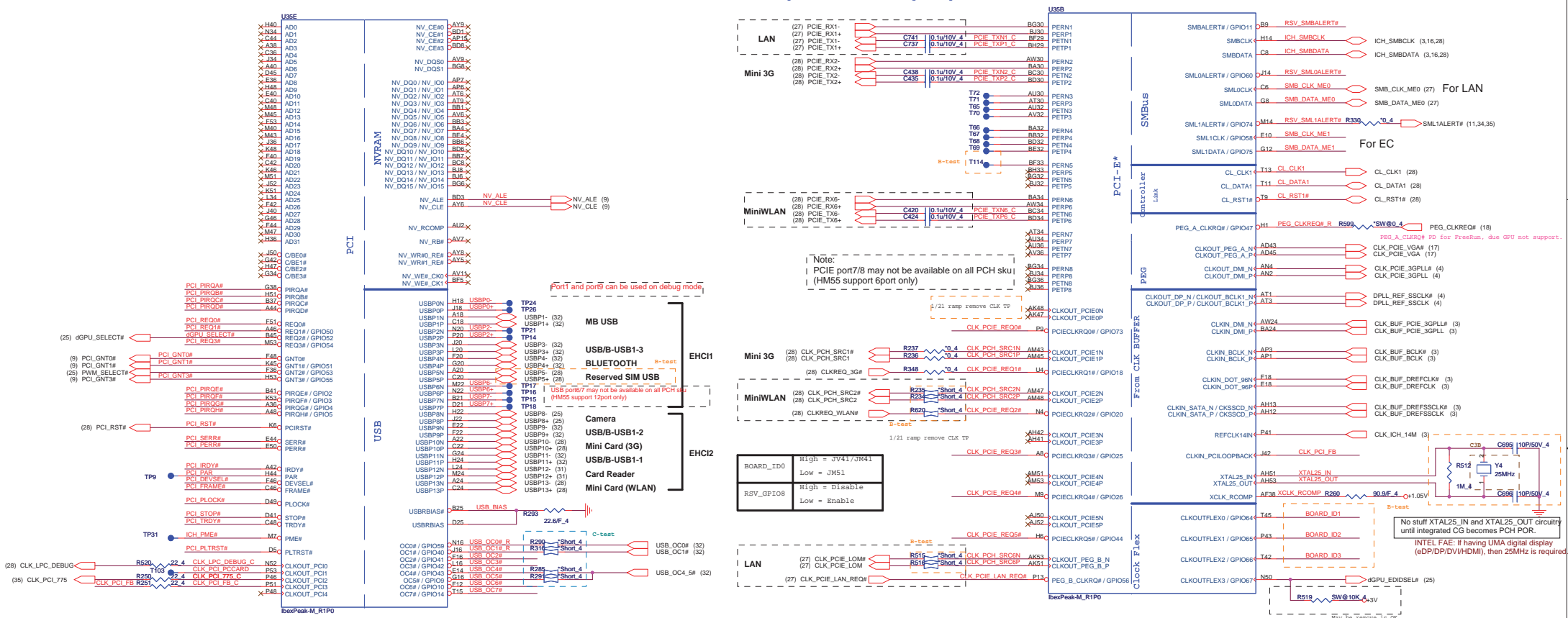
| Pin Name | Strap description | Sampled | Configuration | ZQ1 note | | | | | | | | | | | | |
|---------------------|---------------------------------|---------------|---|--|-------|---------------|---|---|-----|---|---|-----|---|---|-----|---|
| SPKR | No reboot mode setting | PWROK | 0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode | +3V0 - R601 - 10K_4 - SPCR | | | | | | | | | | | | |
| INIT3_3V | Reserved | PWROK | 1 = Default (weak pull-up 20K) Should not be pull-down | | | | | | | | | | | | | |
| GNT3# / GPIO55 | Top-Block Swap Override | PWROK | 0 = "top-block swap" mode 1 = Default (weak pull-up 20K) | R517 - 10K_4 - PCL_GNT3# (10) | | | | | | | | | | | | |
| INTVRMEN | Integrated 1.05V VRM enable | ALWAYS | Should be always pull-up | +VCCRTC - R567 - 330K_4 - PCH_INVRMEN | | | | | | | | | | | | |
| GNT1# / GPIO51 | Boot BIOS Selection 1 [bit-1] | PWROK | <table border="1"> <tr> <th>GNT1#</th> <th>GNT0#</th> <th>Boot Location</th> </tr> <tr> <td>1</td> <td>1</td> <td>SPI</td> </tr> <tr> <td>1</td> <td>0</td> <td>PCI</td> </tr> <tr> <td>0</td> <td>0</td> <td>LPC</td> </tr> </table> | GNT1# | GNT0# | Boot Location | 1 | 1 | SPI | 1 | 0 | PCI | 0 | 0 | LPC | Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS] |
| GNT1# | GNT0# | Boot Location | | | | | | | | | | | | | | |
| 1 | 1 | SPI | | | | | | | | | | | | | | |
| 1 | 0 | PCI | | | | | | | | | | | | | | |
| 0 | 0 | LPC | | | | | | | | | | | | | | |
| GNT0# | Boot BIOS Selection 0 [bit-0] | PWROK | | | | | | | | | | | | | | |
| GNT2# / GPIO53 | ESI strap (Server only) | PWROK | Should not be pull-down (weak pull-up 20K) | USE GPIO PIN | | | | | | | | | | | | |
| NV_ALE | Intel Anti-Theft HDD protection | PWROK | 0 = Disable (Internal pull-down 32ohm) | +1.8V - R590 - 1K_4 - NV_ALE - NV_ALE (10) | | | | | | | | | | | | |
| NV_CLE | DMI Termination voltage | PWROK | weak pull-down 32ohm | +1.8V - R591 - 1K_4 - NV_CLE - NV_CLE (10) | | | | | | | | | | | | |
| HDA_DOCK_EN#/GPIO33 | Flash Descriptor Security | PWROK | 0 = Override 1 = Default (weak pull-up 20K) | +3V0 - R277, R273 - 1K_4, 10K_4 - HDA_DOCK_EN# | | | | | | | | | | | | |
| SPI_MOSI | iTPM function Disable | MEPWROK | 0 = Default (weak pull-down 20K) 1 = Enable | +3V0 - R627 - 1K_4 - SPI_SI_R | | | | | | | | | | | | |
| HDA_SDO | Reserved | RSMRST# | Should not be pull-up (weak pull-down 20K) | | | | | | | | | | | | | |
| GPIO8 | Reserved | RSMRST# | Should not be pull-down (weak pull-up 20K) | | | | | | | | | | | | | |
| GPIO27 | On-die PLL Voltage Regulator | RSMRST# | 0 = Disable 1 = Enable (weak pull-up 20K) | +3V_SS - R340 - 10K_4 - RSV_GPIO8 (11) | | | | | | | | | | | | |
| HDA_SYNC | On-die PLL PWR supply select | RSMRST# | 0 = 1.8V supply (weak pull-down 20K) 1 = 1.5V supply | use default (0 = 1.8V supply) | | | | | | | | | | | | |
| GPIO15 | Reserved | RSMRST# | 0 = TLS no Confidentiality (weak pull-down 20K) 1 = TLS Confidentiality | +3V_SS - R349 - 1K_4 - CR_WAKE# (11) | | | | | | | | | | | | |

IBEX PEAK-M (HDA, JTAG, SATA)

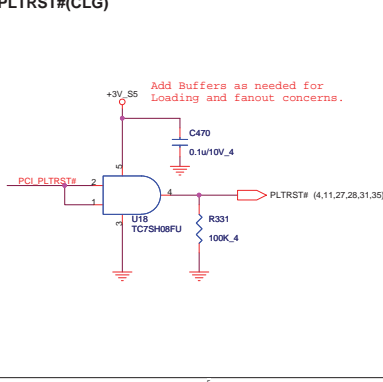


Note:
SATA port2/3 may not be available on all PCH sku
(HM55 support 4port only)

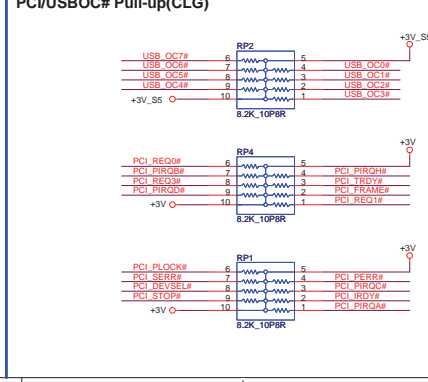
8/13 Swap Lan and WLAN/ Lan chagne to port 1



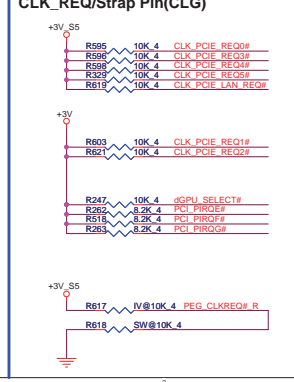
PLTRST#(CLG)



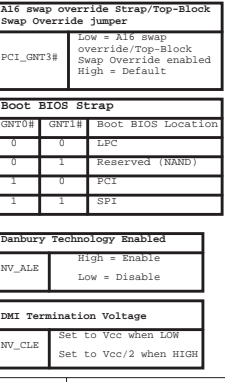
PCI/USBOC# Pull-up(CLG)



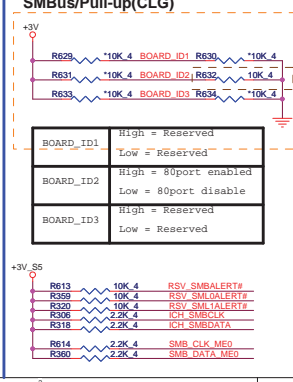
CLK_REQ/Strap Pin(CLG)



AI16 swap override Strap/Top-Block Swap Override jumper



SMBus/Pull-up(CLG)



Boot BIOS Strap

| GNT# | GNT# | Boot BIOS Location |
|------|------|--------------------|
| 0 | 0 | LRC |
| 0 | 1 | Reserved (NAND) |
| 1 | 0 | PCI |
| 1 | 1 | SPI |

Danbury Technology Enabled

| | |
|--------|---------------|
| NV_ALE | High = Enable |
| NV_CLE | Low = Disable |

DMI Termination Voltage

| | |
|--------|------------------------|
| NV_CLE | Set to Vcc when LOW |
| NV_CLE | Set to Vcc/2 when HIGH |

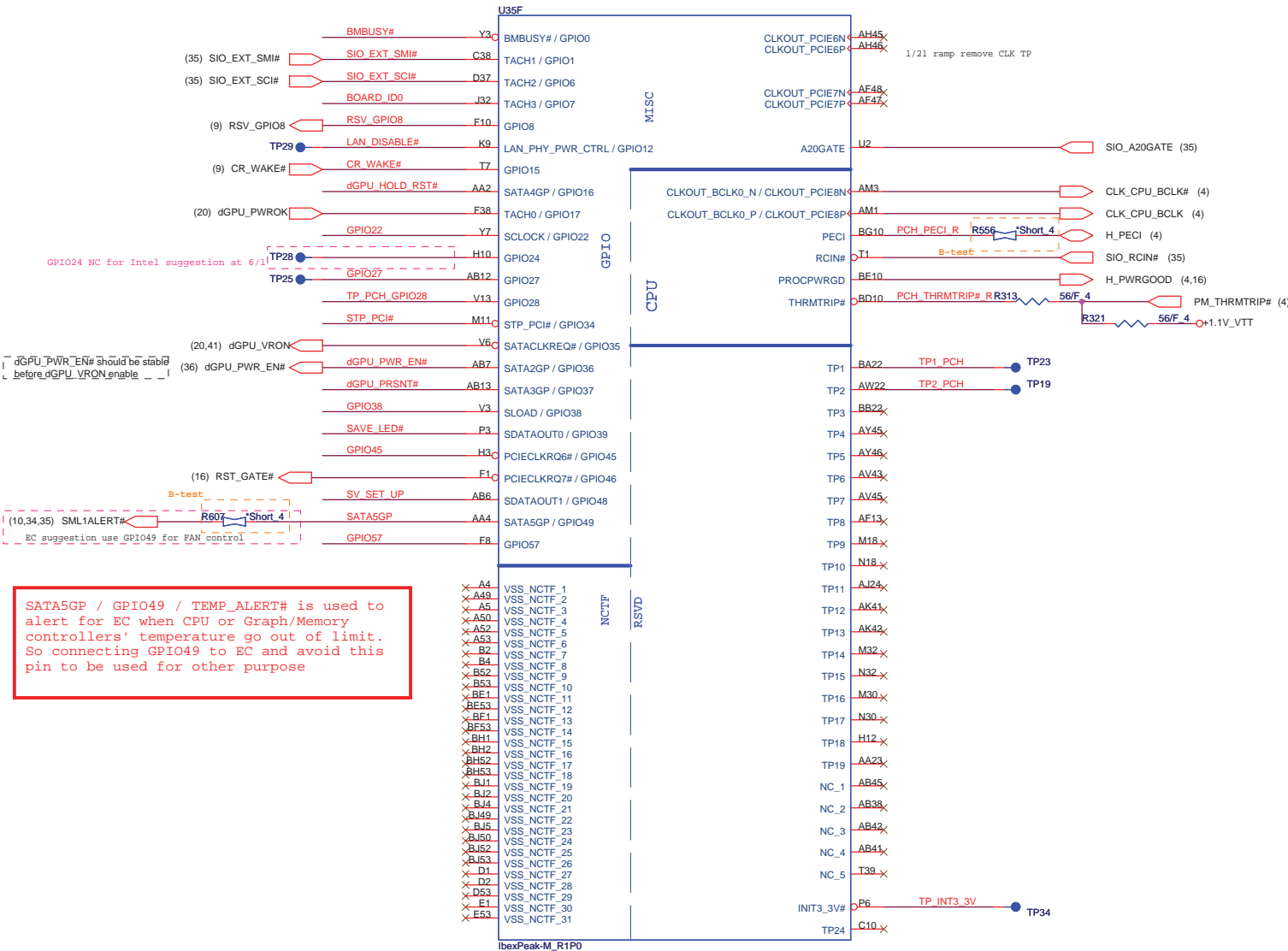
PROJECT : ZQ1

Size: Document Number: IBEX PEAK-M 3/6 Rev 1A
Date: Friday, January 22, 2010 Sheet 10 of 48

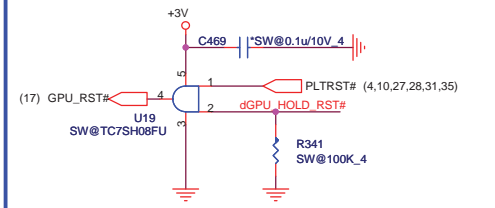
PCH4 (CLG)

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

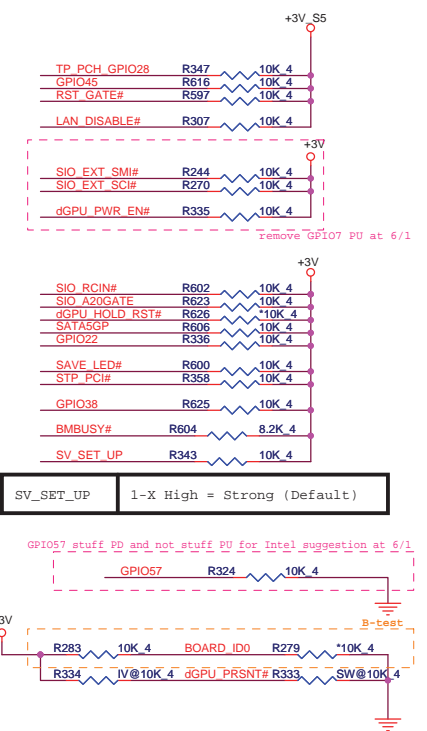
GPU RST#(CLG)



SATA5GP / GPIO49 / TEMP_ALERT# is used to alert for EC when CPU or Graph/Memory controllers' temperature go out of limit. So connecting GPIO49 to EC and avoid this pin to be used for other purpose



GPIO Pull-up/Pull-down(CLG)



SV_SET_UP | 1-X High = Strong (Default)

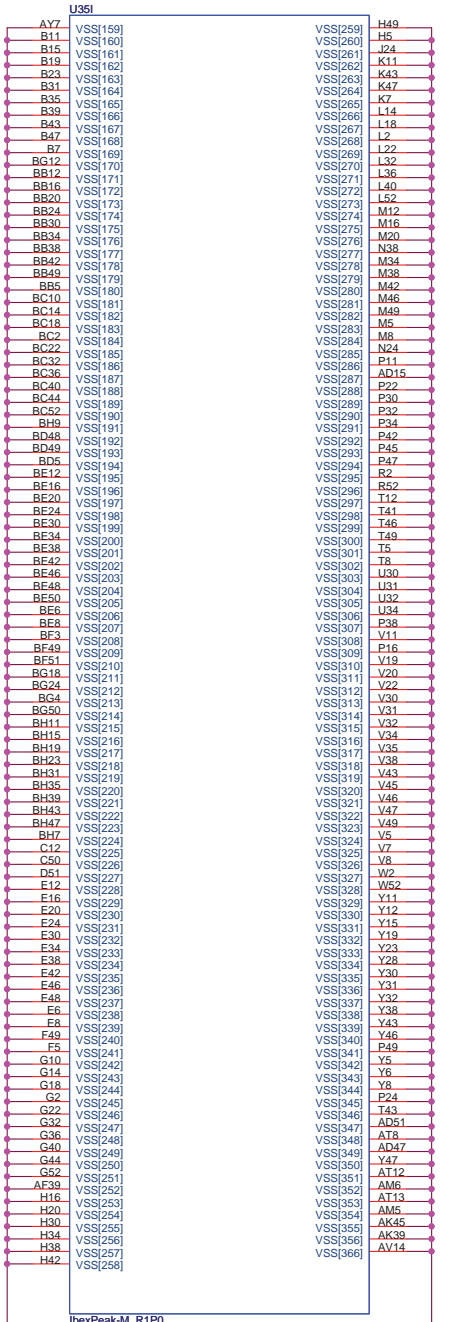
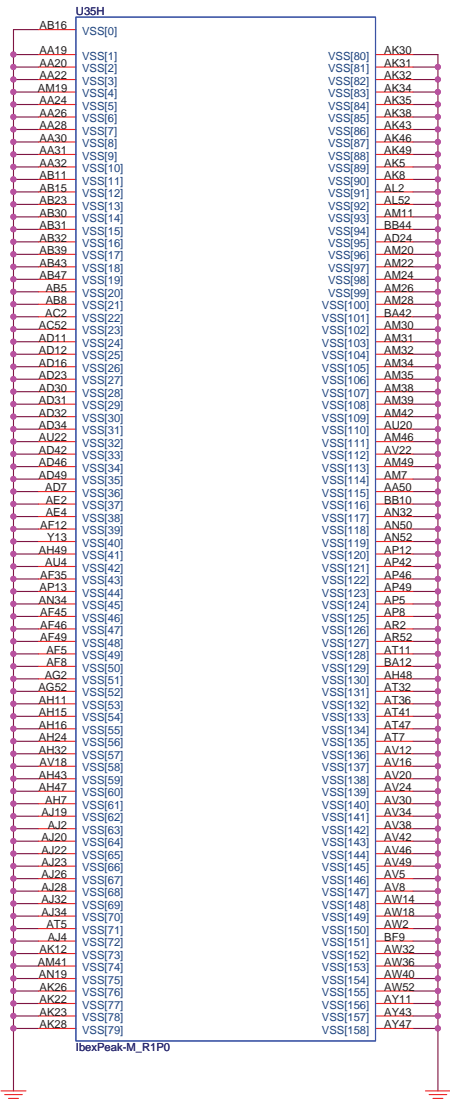
GPIO57_stuff PD and not_stuff PU for Intel suggestion at 6/1


| | |
|-----------|--------------------------------|
| BOARD_ID0 | High = JV41/JM41 Low = JM51 |
| RSV_GPIO8 | High = Disable Low = Enable |

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| | | |
|-------|--------------------------|----------------|
| Size | Document Number | Rev |
| | IBEX PEAK-M 4/6 | 1A |
| Date: | Friday, January 22, 2010 | Sheet 11 of 48 |

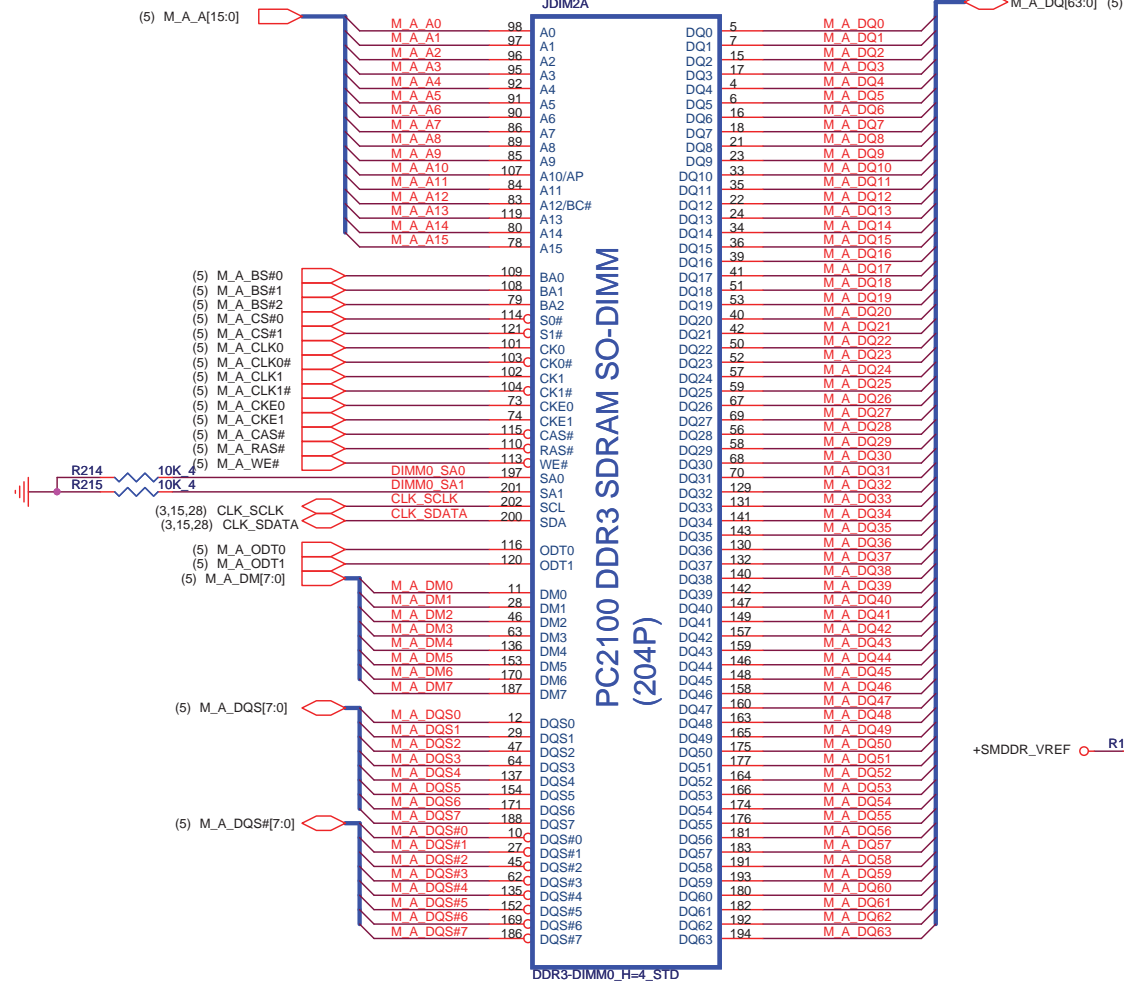
IBEX PEAK-M (GND)



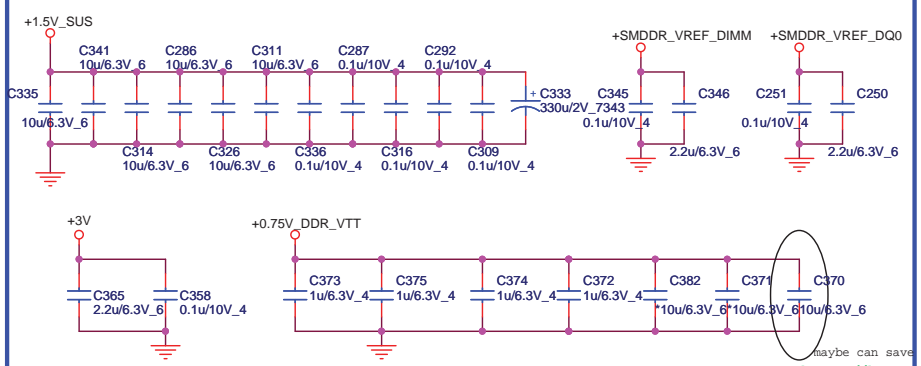
 **Quanta Computer Inc.**
PROJECT : ZQ1

| | | |
|-------|------------------------------|----------------|
| Size | Document Number | Rev |
| | IBEX PEAK-M 6/6 | 1A |
| Date: | Wednesday, December 16, 2009 | Sheet 13 of 48 |

DDR_STD (DDR)



Place these Caps near So-Dimm0.



| | STD 4H | STD 8H |
|-----|-------------|-------------|
| FOX | | |
| LTK | DGMK4000004 | DGMK4000097 |
| SUY | | |
| MLX | DGMK4000011 | DGMK4000080 |

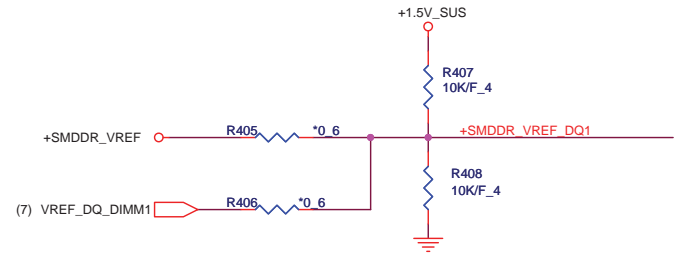
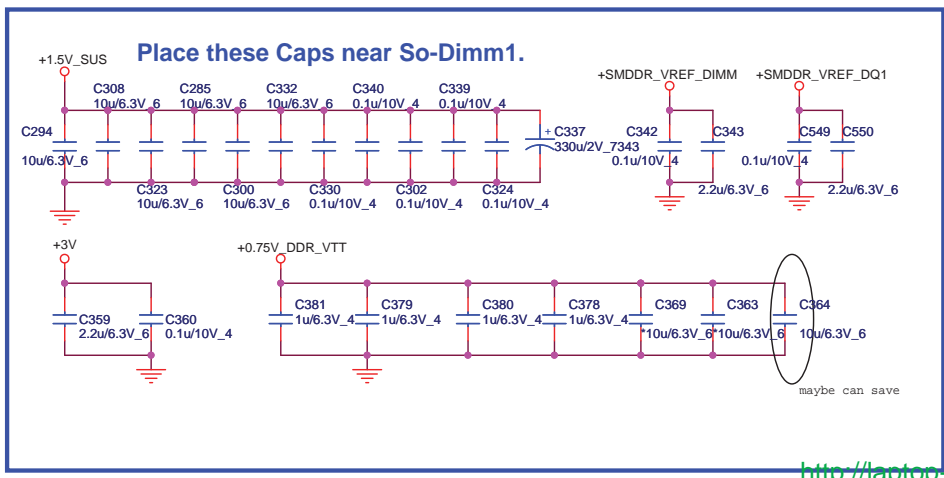
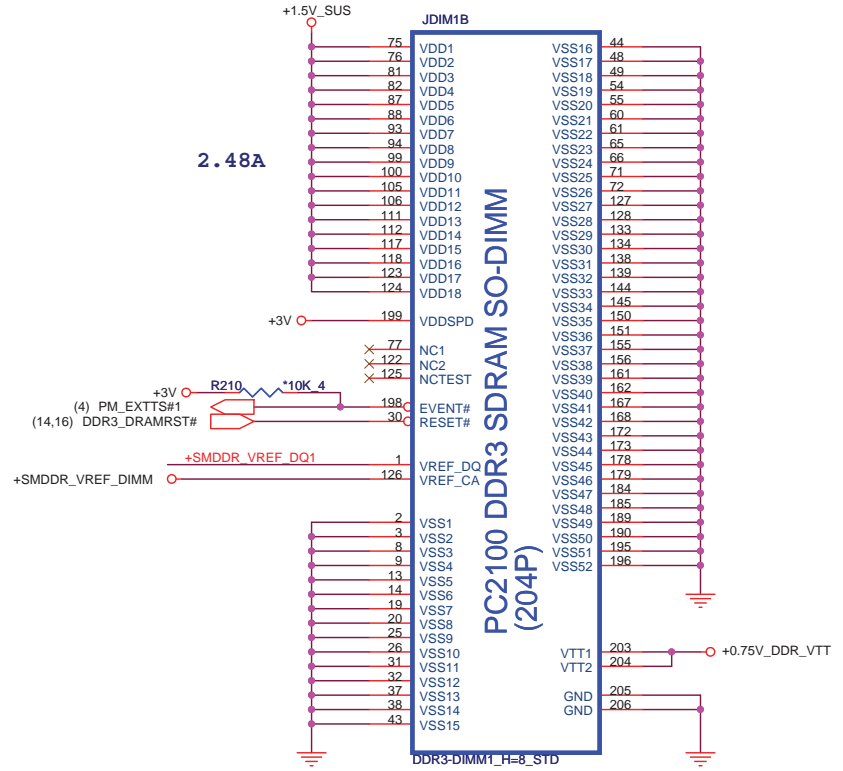
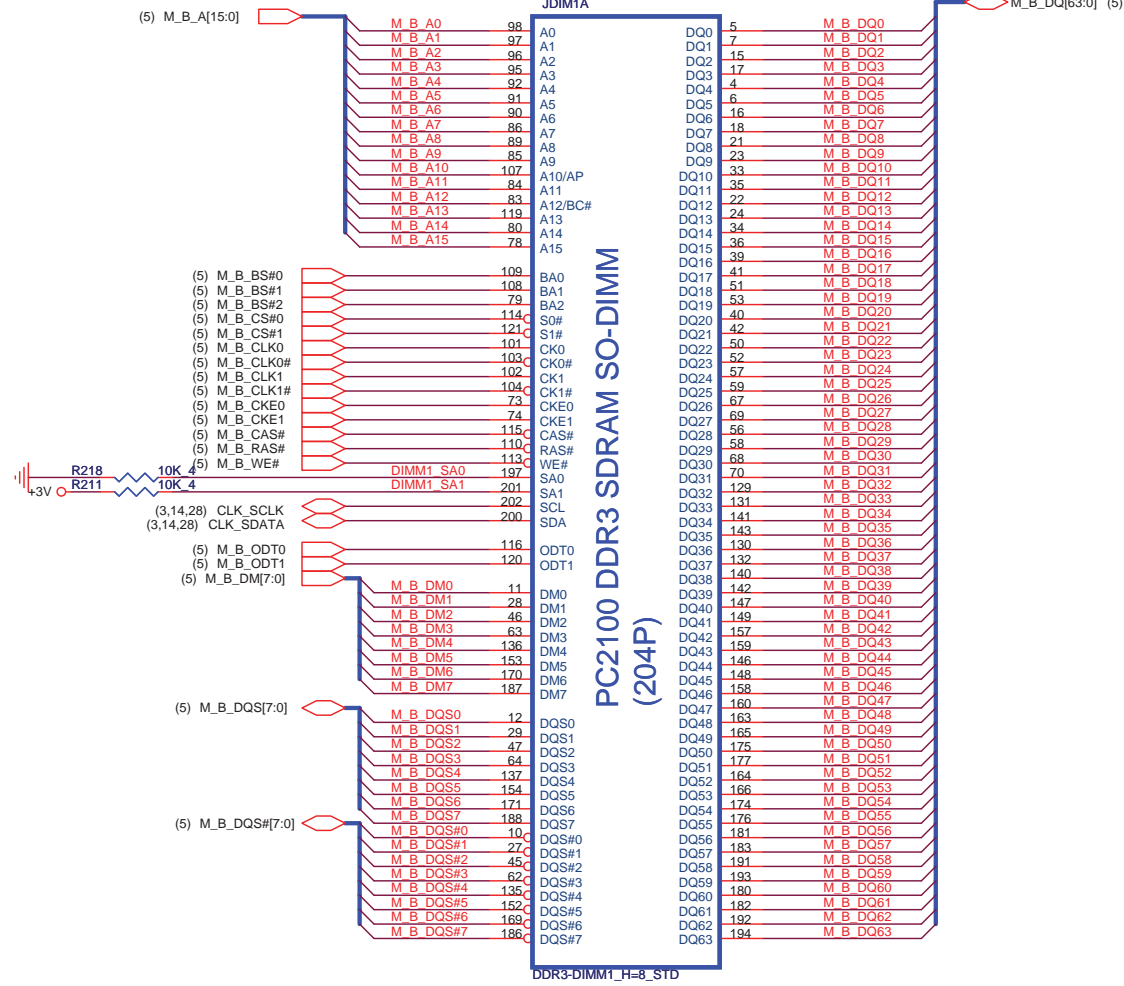
Standard 4H type:DDR-C-2013289-204p
<http://laptop-motherboard-schematic.blogspot.com/>

- M1:PWR SMDRR_VREF
- M1+:voltage divider(Default)
- M3:CPU VREF_DQ_DIMM0

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| | | |
|-------|--------------------------|----------------|
| Size | Document Number | Rev |
| | DDR3 SO-DIMM-0 | 1A |
| Date: | Friday, January 22, 2010 | Sheet 14 of 48 |

DDR_STD (DDR)



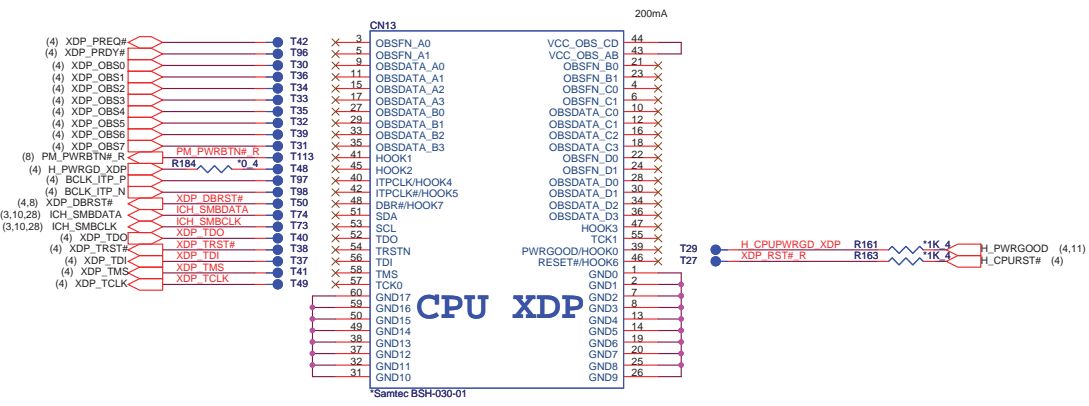
| | STD 4H | STD 8H |
|-----|-------------|-------------|
| FOX | | |
| LTK | DGMK4000004 | DGMK4000097 |
| SUY | | |
| MLX | DGMK4000011 | DGMK4000080 |

- M1:PWR SMDDR_VREF
- M1+:voltage divider(Default)
- M3:CPU VREF_DQ_DIMM0

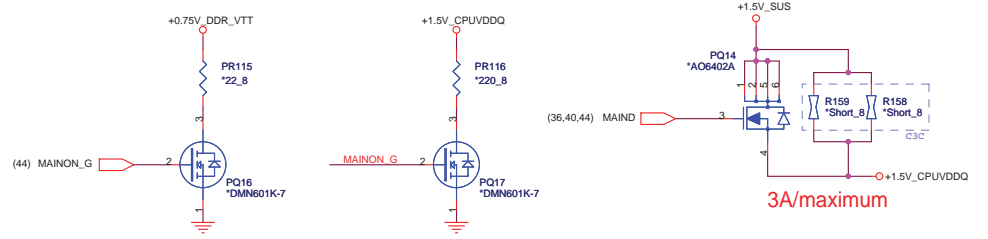
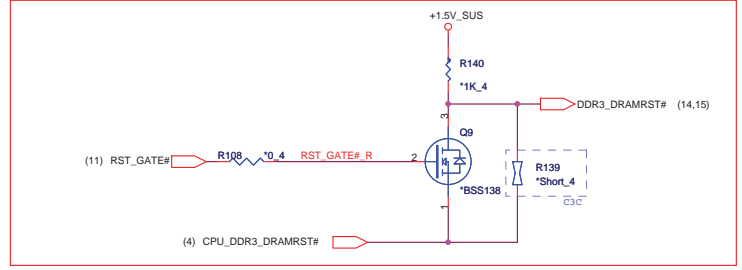
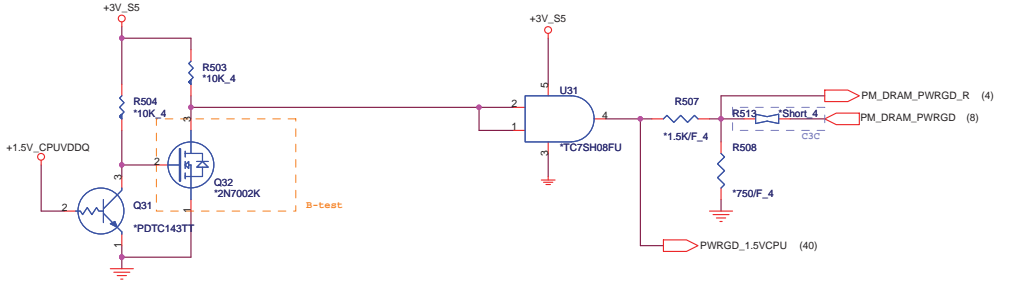
Quanta Computer Inc.
PROJECT : ZQ1

| | | |
|-------|--------------------------|----------------|
| Size | Document Number | Rev |
| | DDR3 SO-DIMM-1 | 1A |
| Date: | Friday, January 22, 2010 | Sheet 15 of 48 |

CPU XDP Connector(CPU)



S3 leakage solution(CLG)



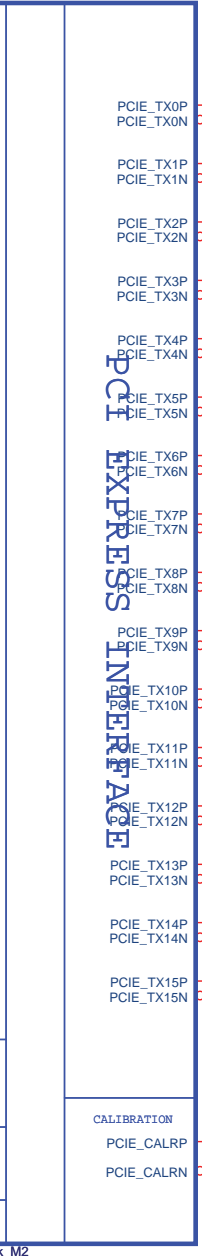
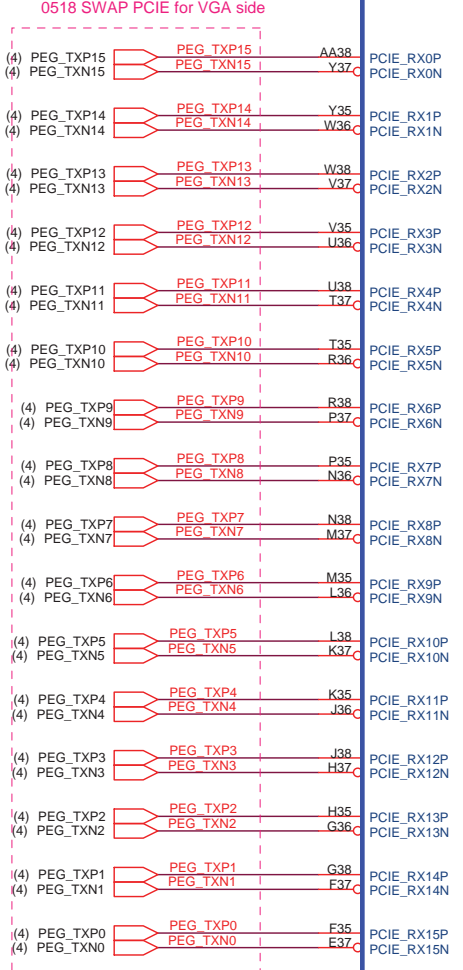
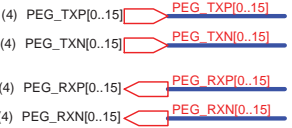
Quanta Computer Inc.
PROJECT : ZQ1

| | | |
|-------|--------------------------|----------------|
| Size | Document Number | Rev |
| | XDP | 1A |
| Date: | Friday, January 22, 2010 | Sheet 16 of 48 |

GPU_1(VGA)

U23A

0518 SWAP PCIE for VGA side



For Broadway, Madison and Park the PWRGOOD ball must be connected to ground

R61 SW@10K_4



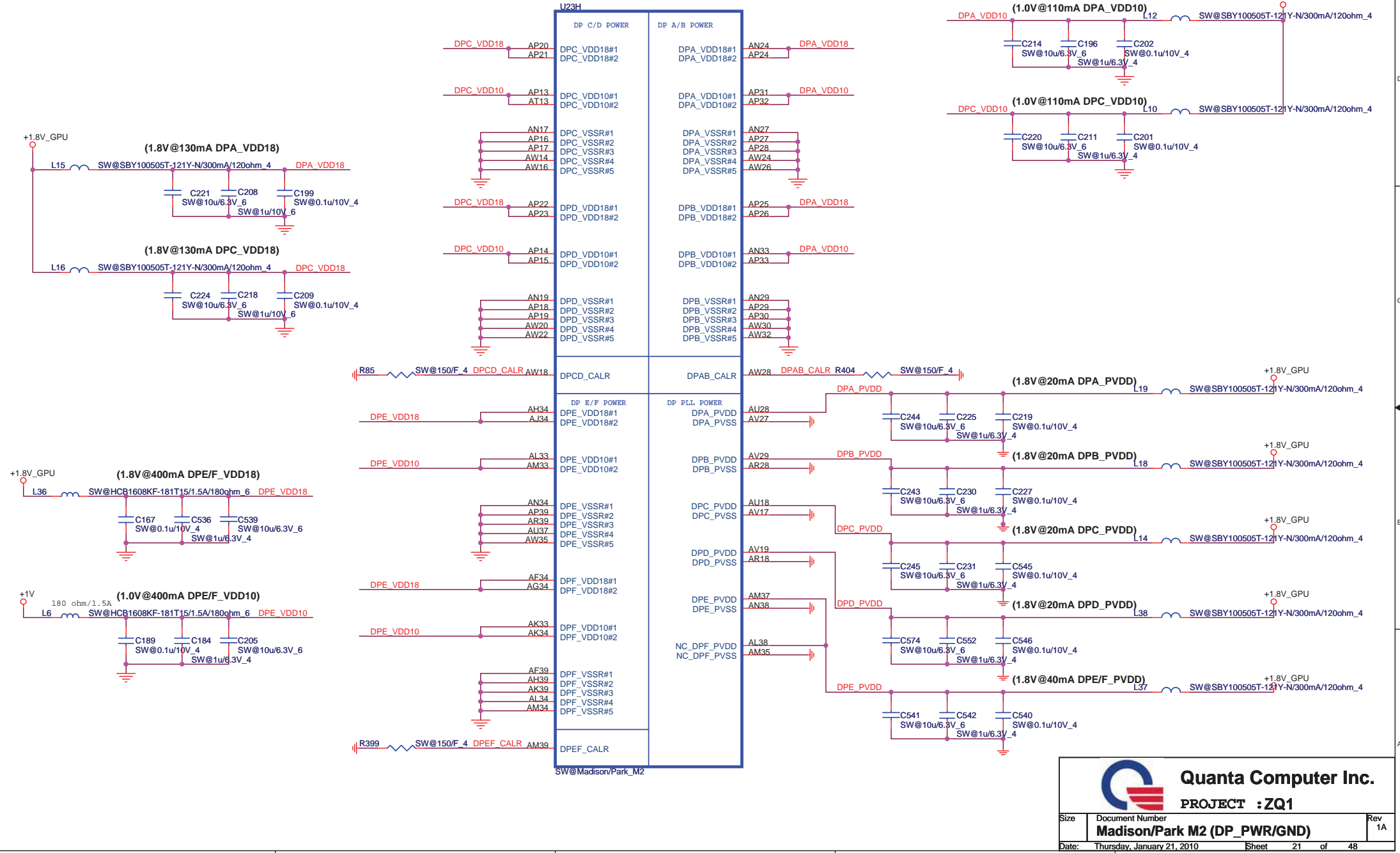
For M97, Broadway, Madison and Park PCIE_VDDC is 1.0V

| | |
|---------|-------------|
| Madison | AJ007720T02 |
| Park | AJ077400T08 |

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| | | |
|-------|---------------------------------|----------------|
| Size | Document Number | Rev |
| | Madison/Park M2-PCIE I/F | 1A |
| Date: | Friday, January 22, 2010 | Sheet 17 of 48 |

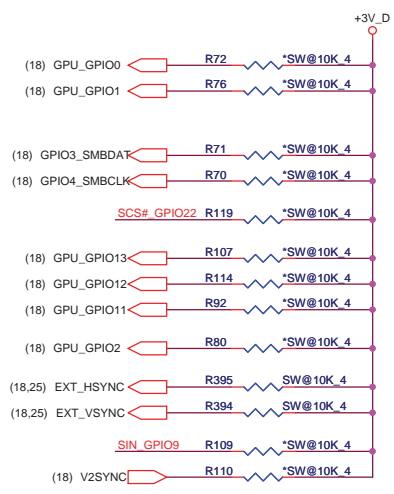
GPU_5(VGA)



Quanta Computer Inc.
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| | | |
|-------|-------------------------------------|----------------|
| Size | Document Number | Rev |
| | Madison/Park M2 (DP_PWR/GND) | 1A |
| Date: | Thursday, January 21, 2010 | Sheet 21 of 48 |

PIN STRAPS(VGA)

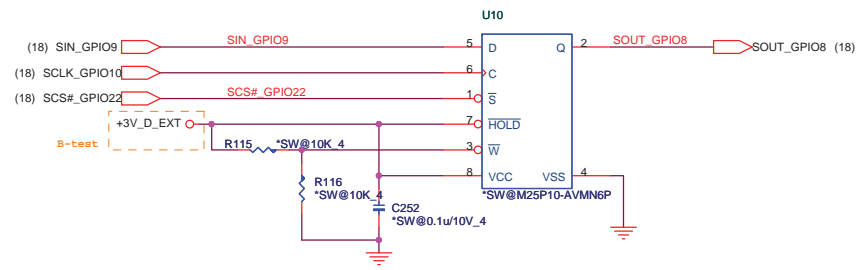


| ROM Table | | |
|-----------------------------------|-------------|------|
| Manufacturer | Part Number | Code |
| Numonyx ST Microelectronics | M25P05A | 100 |
| | M25P10A | 101 |
| | M25P20 | 101 |
| | M25P40 | 101 |
| | M25P80 | 101 |
| Chingis PMC | Pm25LV512A | 100 |
| | Pm25LV010A | 101 |

| ROM Table | | |
|-----------|-----------|--------------------|
| EXT_HSYNC | EXT_VSYNC | Discription |
| 0 | 0 | No Audio |
| 0 | 1 | Any one by detectc |
| 1 | 0 | DP only |
| 1 | 1 | Both DP & HDMI |

| CONFIGURATION STRAPS | | | | |
|---|---------------------------|---|---------|-----------------|
| ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET | | | | |
| STRAPS | PIN | DESCRIPTION OF DEFAULT SETTINGS | DEFAULT | REMARK |
| TX_PWRS_ENB | GPIO0 | 0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING | 0 | |
| TX_DEEMPH_EN | GPIO1 | PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED | 0 | |
| BIOS_ROM_EN | GPIO_22_ROMCSB | ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE | 1 | |
| ROMIDCFG(2:0) | GPIOQ[13:11] | SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101 | 101 | See ROM table |
| BIF_GEN2_EN_A | GPIO2 | 0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE | 0 | |
| GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN | GPIO8 H2SYNC GPIO21 | Reserved Only | 0 | |
| AUD[1] AUD[0] | HSYNC VSYNC | AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI. | 11 | See Audio table |
| GPIO_9_ROMSI | GPIO9 | 0 = VGA controller capacity enable | 0 | |
| VIP_DEVICE_STRAP_ENA | V2SYNC | 0 = DRIVER would ignore the value sample on VHAD_0 during RESET. | 0 | |

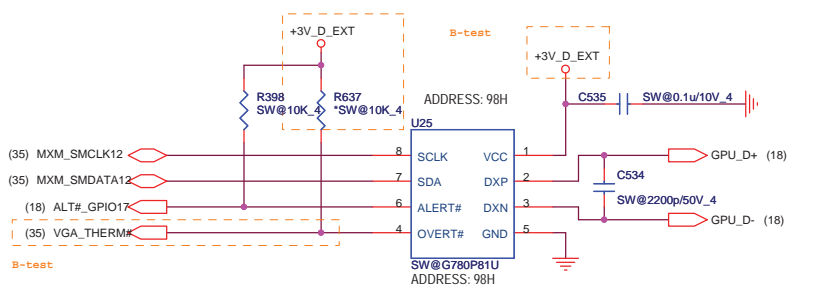
EEPROM(VGA)



Thermal Sensor(VGA)

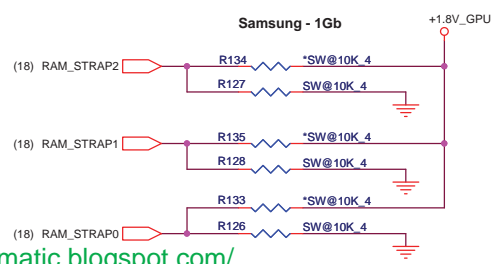
| Vendor | P/N |
|----------|-------------|
| WINDBOND | AL83L771K01 |
| GMT | AL000780000 |

USD0.16



DDR3 Memory Aperture size(GPU)

| DDR3 Memory Aperture size | | | | | | |
|---------------------------|-----------------|-------------------------|-------|-------------------------|-------------------------|-------------------------|
| Vendor | Vendor P/N | STN B/S P/N | Size | RAM_STRAP2 DVPDATA_2 | RAM_STRAP1 DVPDATA_1 | RAM_STRAP0 DVPDATA_0 |
| Hynix | | | 512Mb | 1 | 1 | 0 |
| | H5TQ1G63BFR-12C | AKD5LZGTW04 (64M*16) | 1Gb | 1 | 0 | 0 |
| | | | 2Gb | 1 | 0 | 1 |
| Samsung | | | 512Mb | | | |
| | K4W1G1646E-HC12 | AKD5LGGT506 (64M*16) | 1Gb | 0 | 0 | 0 |
| | K4W2G1646B-HC12 | AKD5MGGT500 | 2Gb | 0 | 0 | 1 |
| AMD | 23EY2387MA12-SZ | AKD5LGGT700 | 1Gb | 0 | 1 | 0 |



RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

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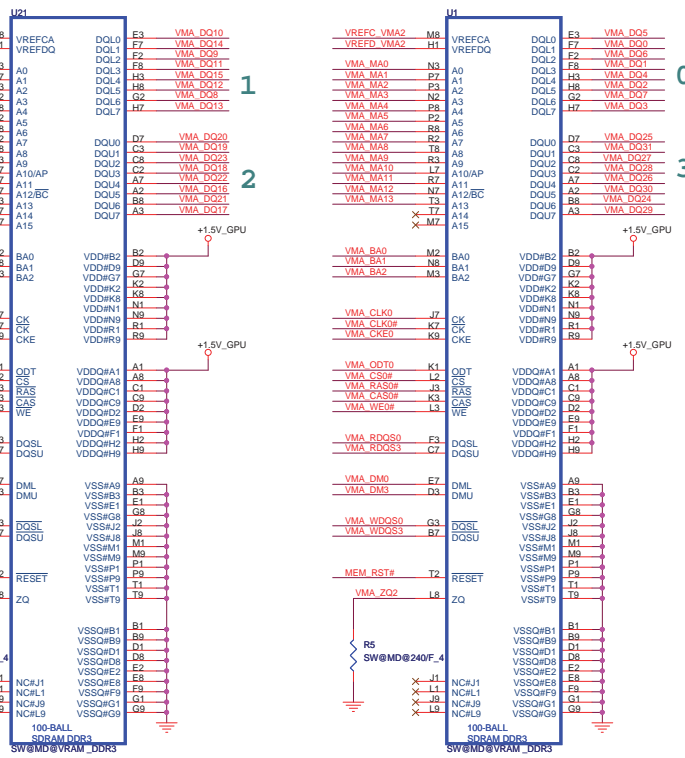
Size Document Number Strip/Thermal Rev 1A
Date: Friday, January 22, 2010 Sheet 22 of 48

- (19) VMA_DQ[63..0] VMA_DQ[63..0]
- (19) VMA_DM[7..0] VMA_DM[7..0]
- (19) VMA_RDQS[7..0] VMA_RDQS[7..0]
- (19) VMA_WDQS[7..0] VMA_WDQS[7..0]

CHANNEL A: 512MB DDR3 (16*64M*4pcs)

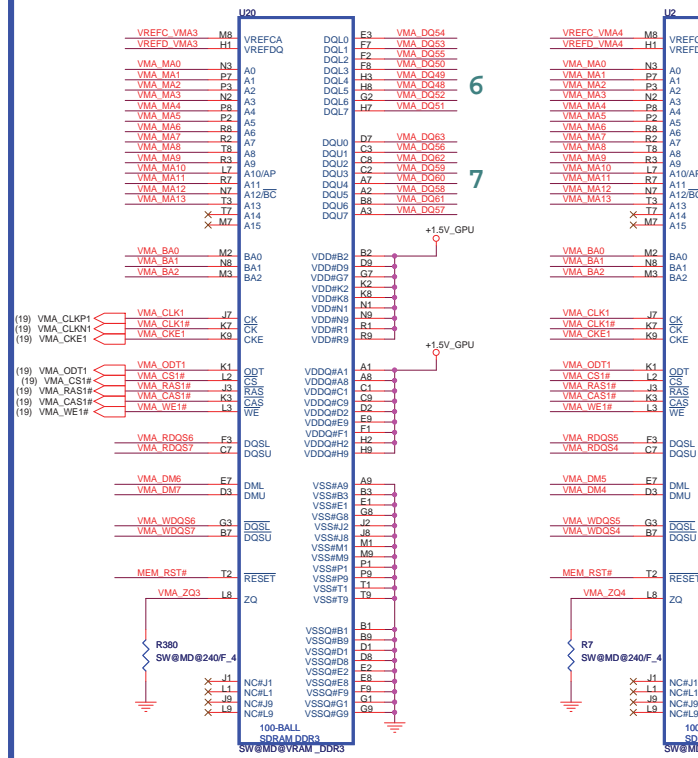
Park, M92M Use Channel B Memory Interface Only

QSA[7..0] QSA#[7..0]



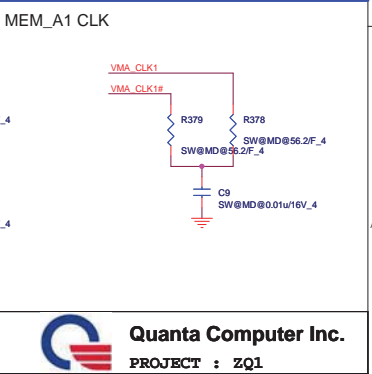
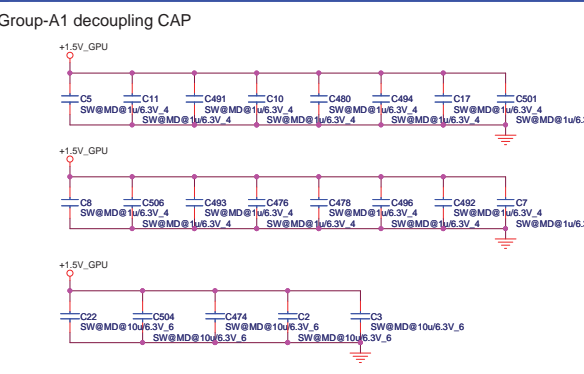
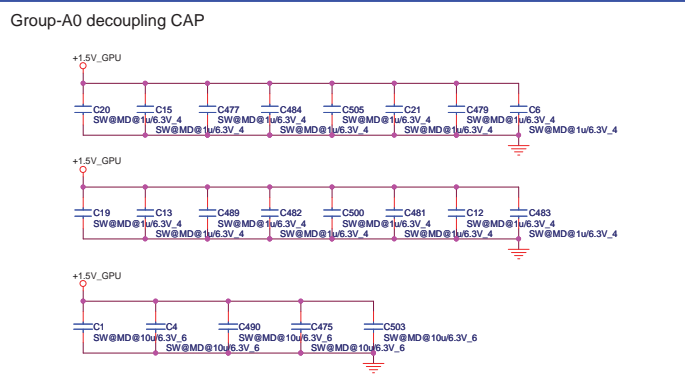
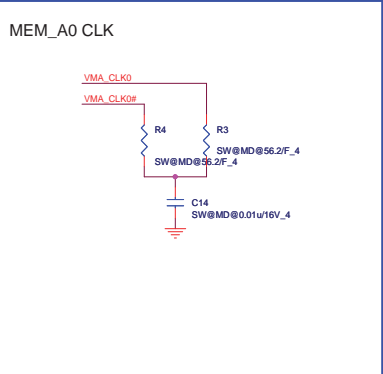
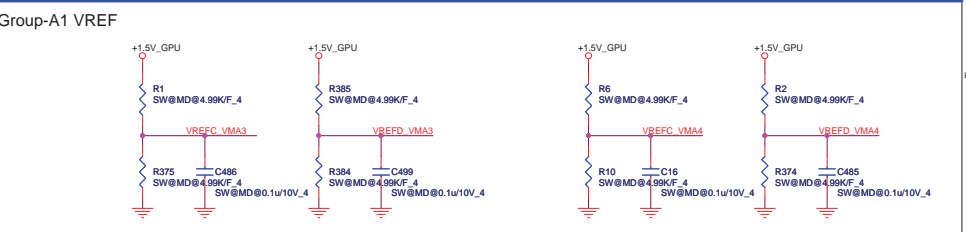
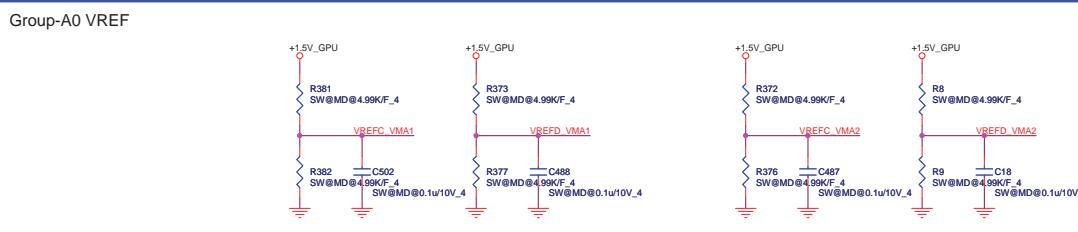
TOP Left

BOT Left



BOT Right

TOP Right



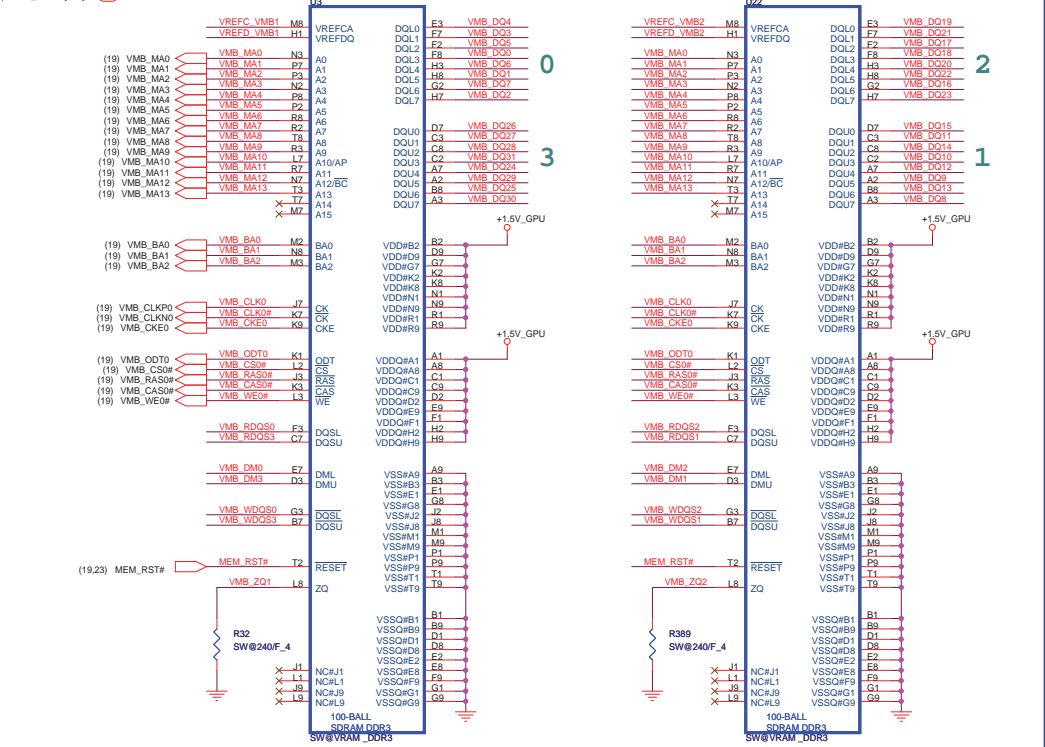
<http://laptop-motherboard-schematic.blogspot.com/>

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Size Document Number
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CHANNEL B: 512MB DDR3 (16*64M*4pcs)

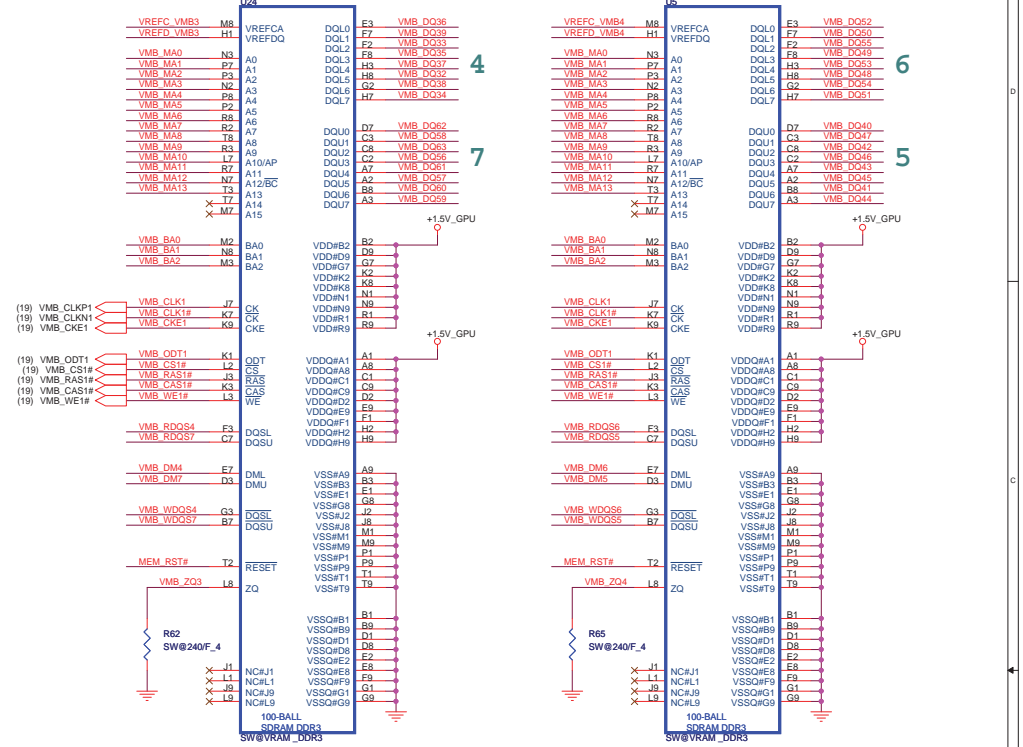
- (19) VMB_DM[63..0] VMB_DM63_0I
- (19) VMB_DM[7..0] VMB_DM7_0I
- (19) VMB_RDQS[7..0] VMB_RDQS7_0I
- (19) VMB_WDQS[7..0] VMB_WDQS7_0I

QSA[7..0]
QSA#[7..0]



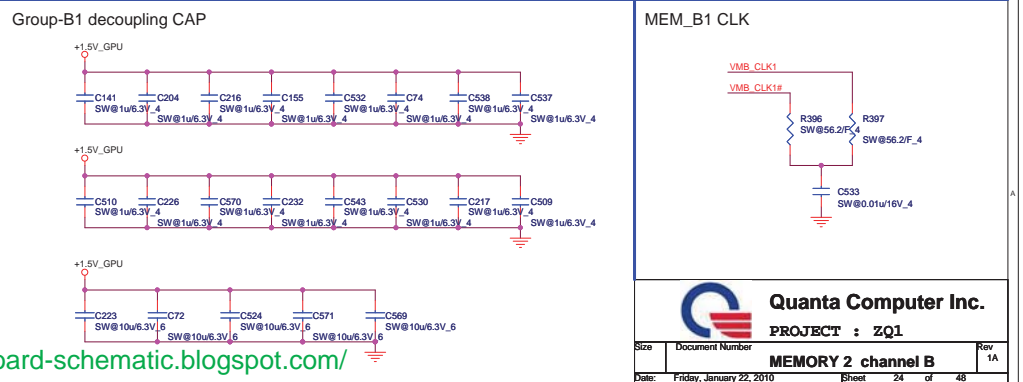
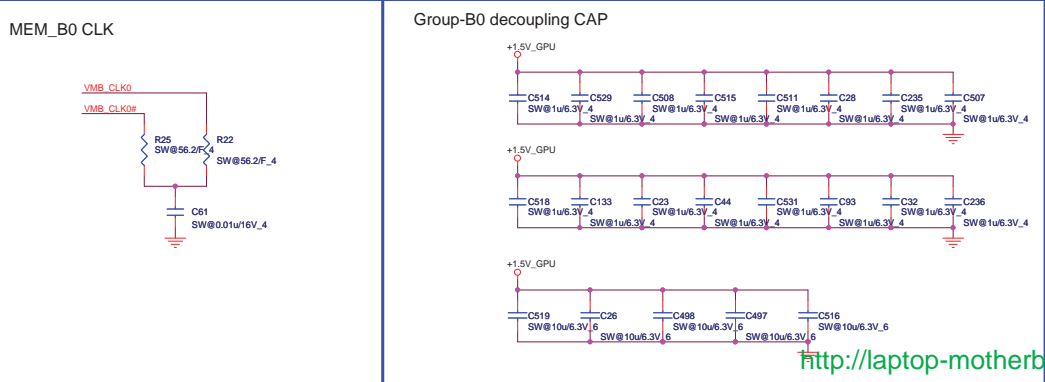
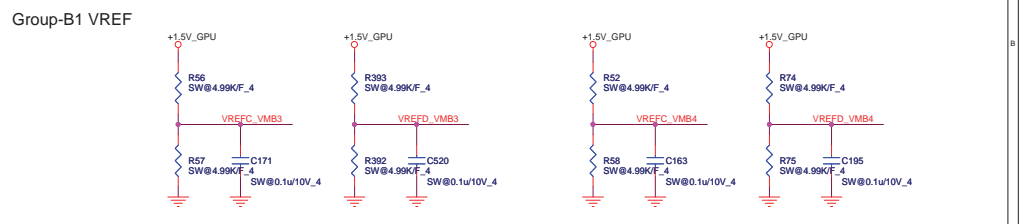
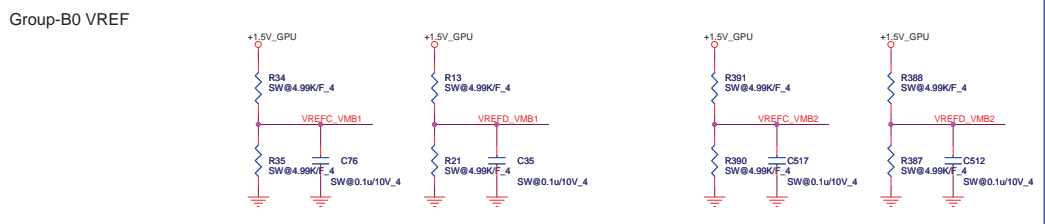
BOT Down

TOP Down



TOP Up

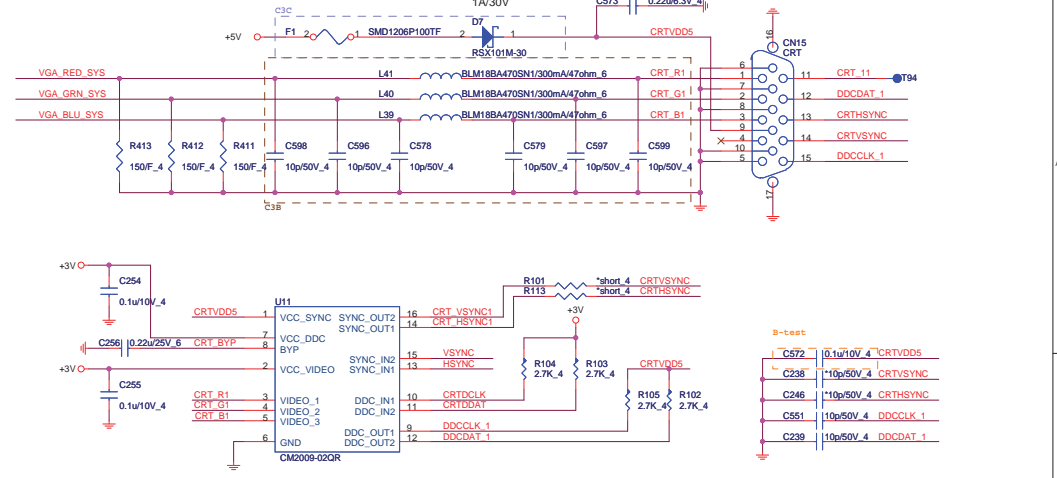
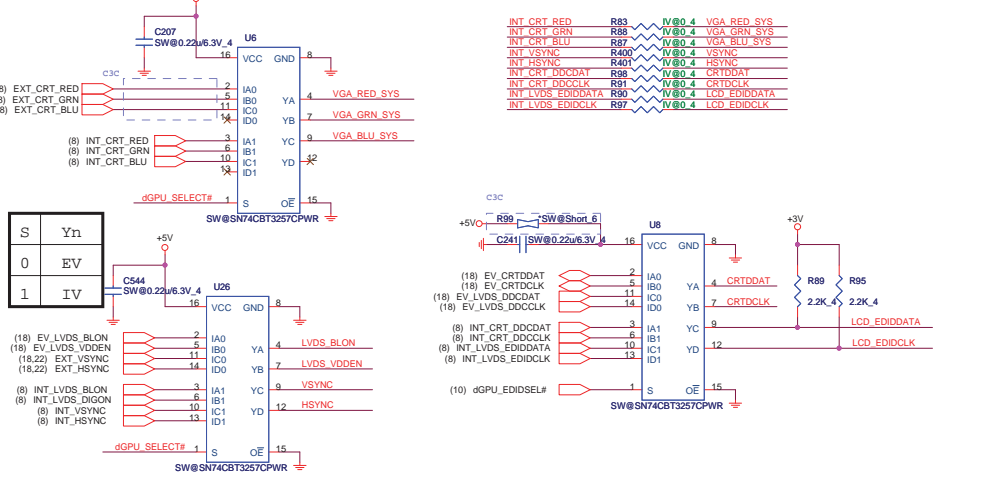
BOT Up



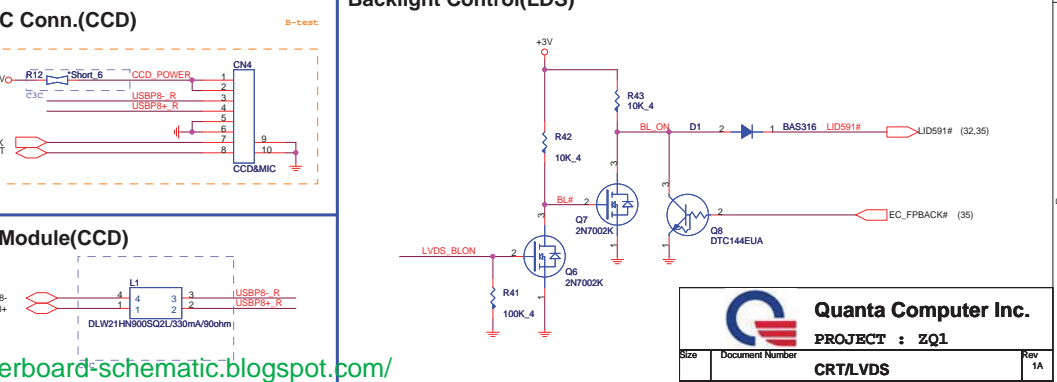
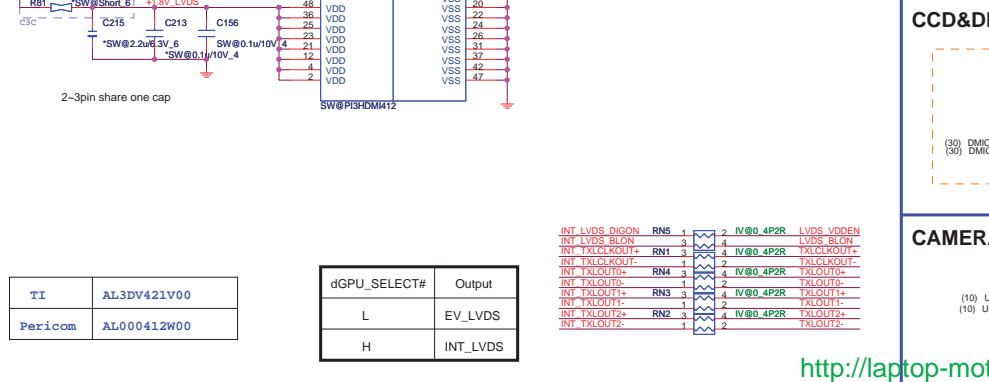
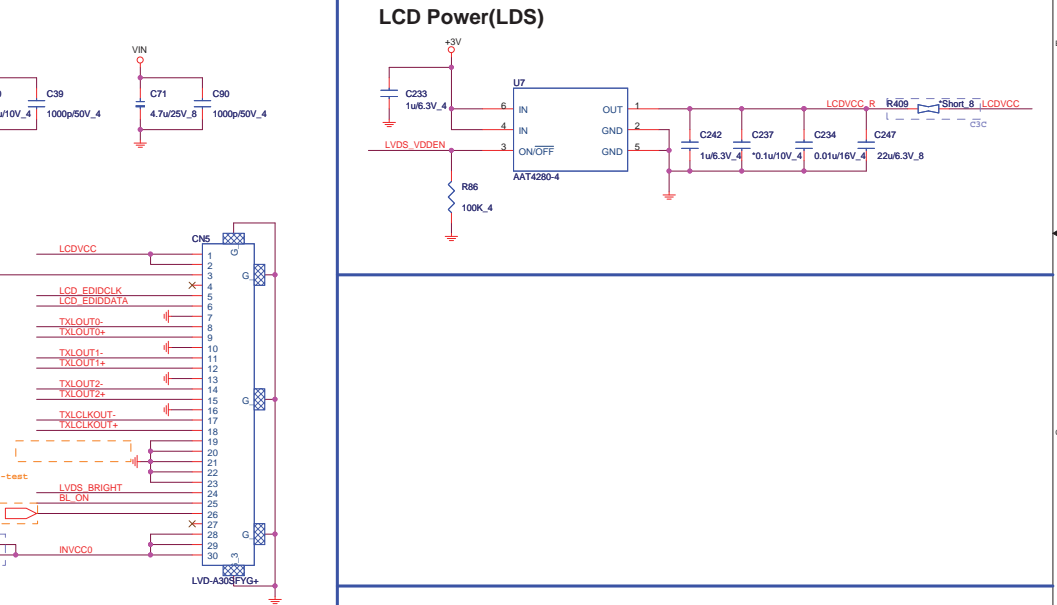
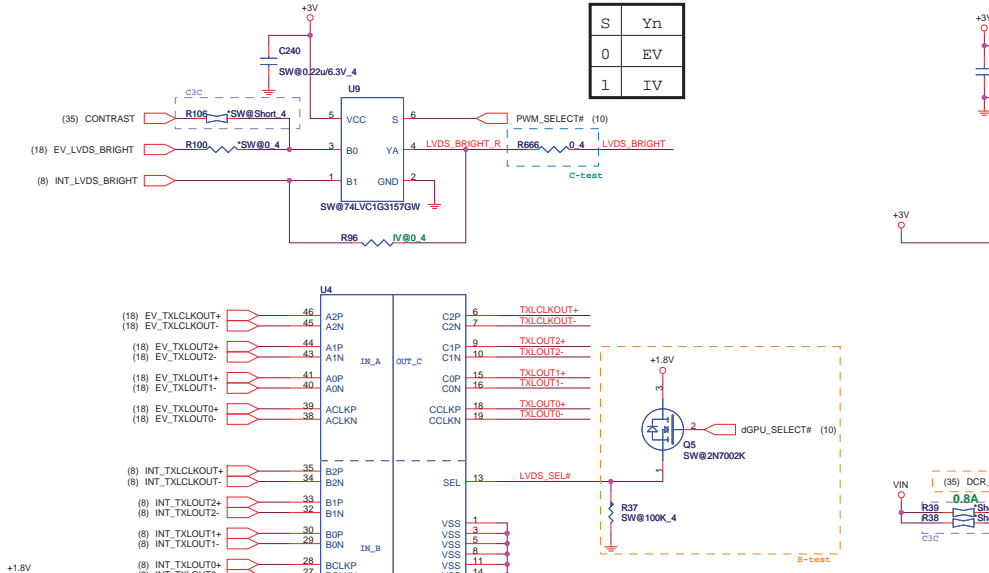
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| | | | |
|-------|--------------------------|--------------------|--------|
| Size | Document Number | MEMORY 2 channel B | Rev 1A |
| Date: | Friday, January 22, 2010 | Sheet 24 of 48 | |

CRT(CRT)



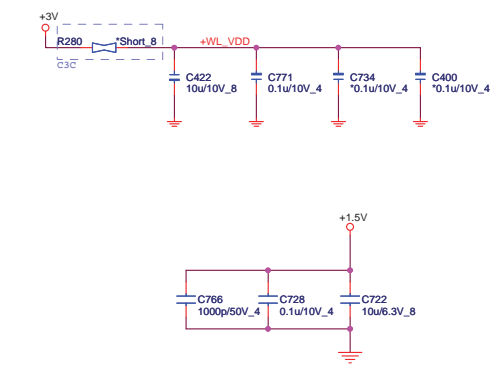
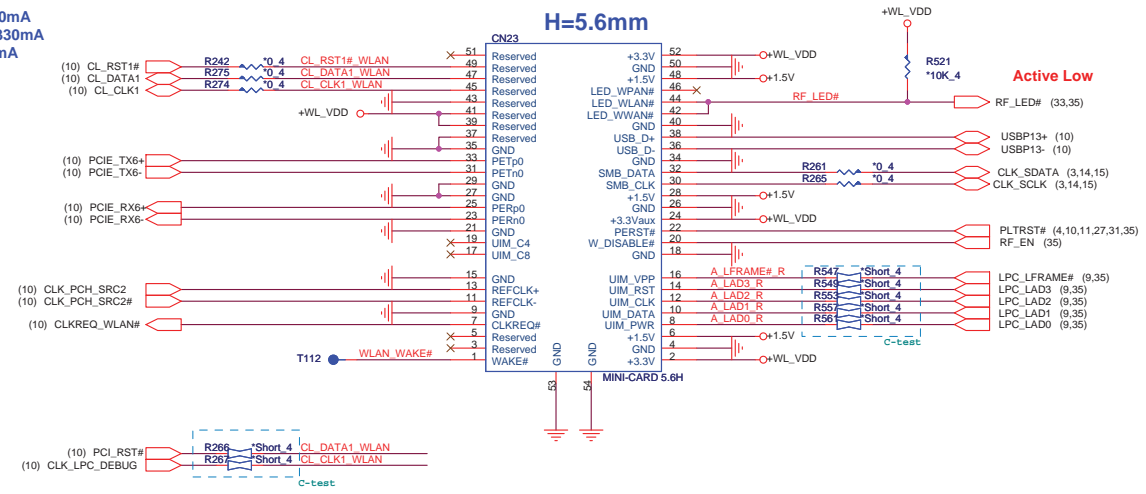
LVDS(LDS)



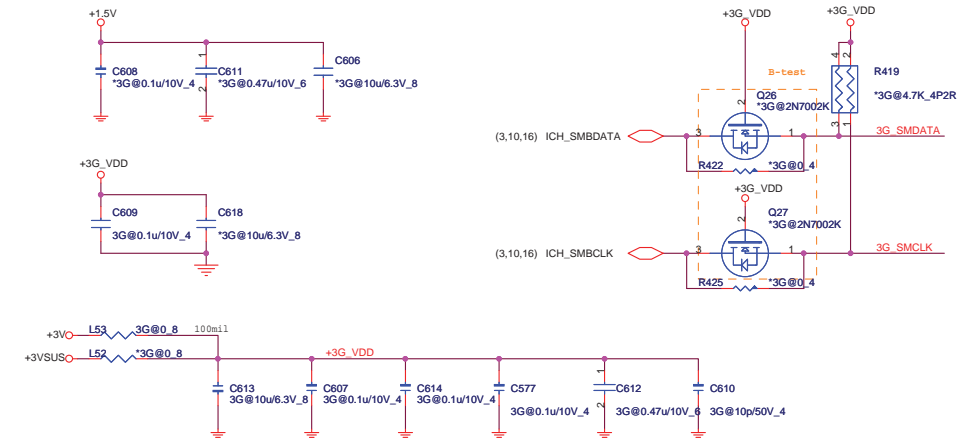
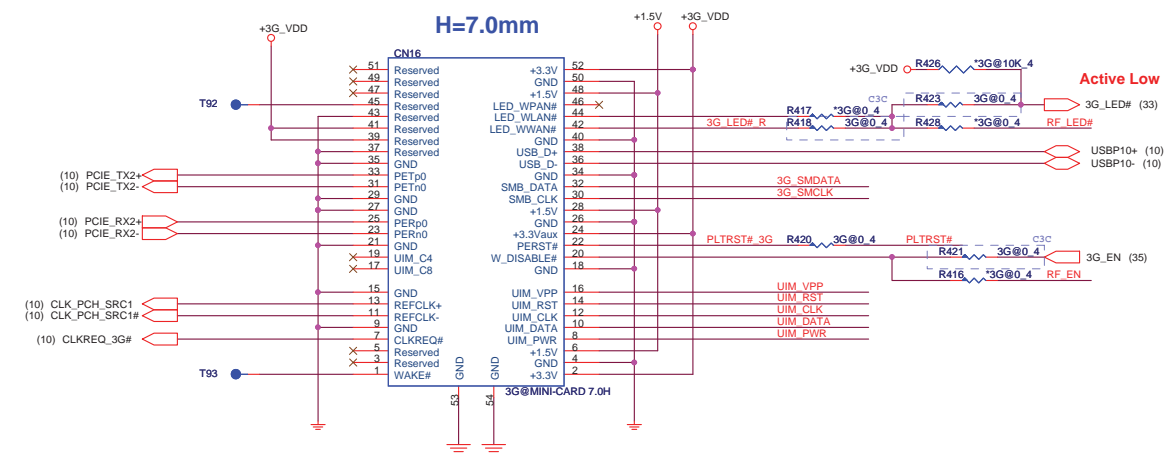
| | | | |
|---------|-------------|--------------|----------|
| TI | AL3DV421V00 | dGPU_SELECT# | Output |
| Pericom | AL000412W00 | L | EV_LVDS |
| | | H | INT_LVDS |

MINI-CARD WLAN(MPC)

+3.3V: 1000mA
 +3.3Vaux: 330mA
 +1.5V: 500mA

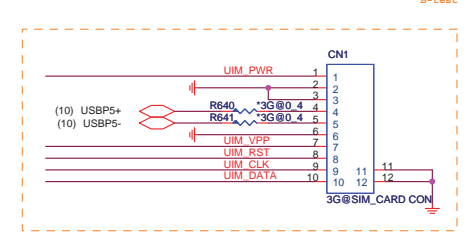


MINI-CARD 3G(MNC) Reserve for JV41-CP



A: (10/17)FAE confirm:
 3G module need +3VSUS and no need +1.5V and no need SMBUS

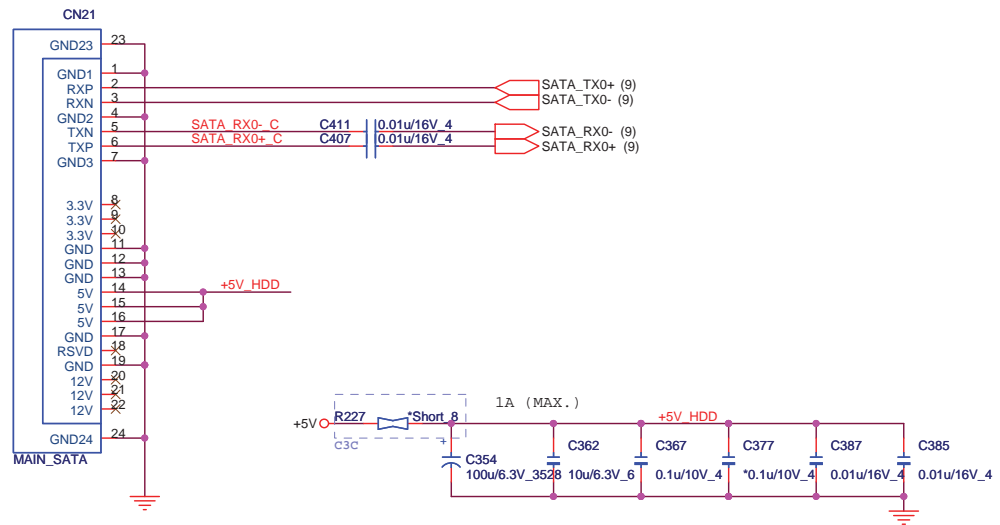
SIM CARD FFC connector(RFM)



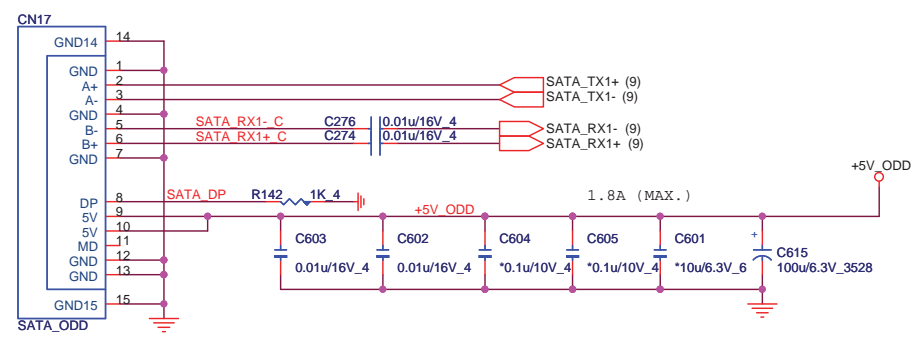
Quanta Computer Inc.
PROJECT : ZQ1

| | | |
|-------|--------------------------|----------------|
| Size | Document Number | Rev |
| | Mini-Card/WL/3G/SIM | 1A |
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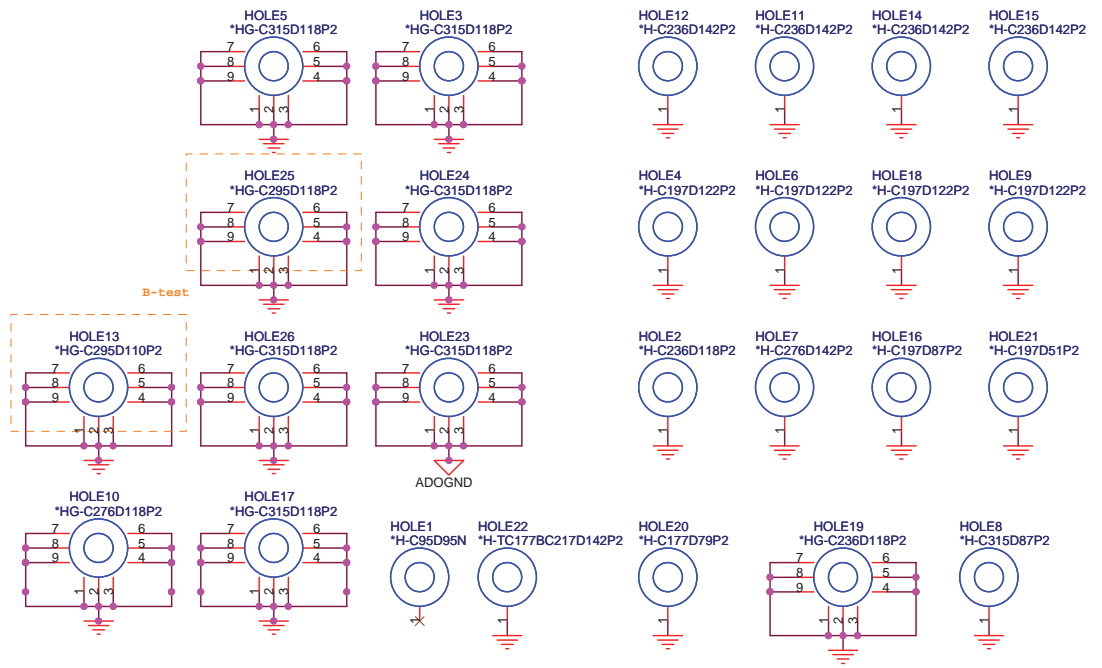
SATA HDD(HDD)



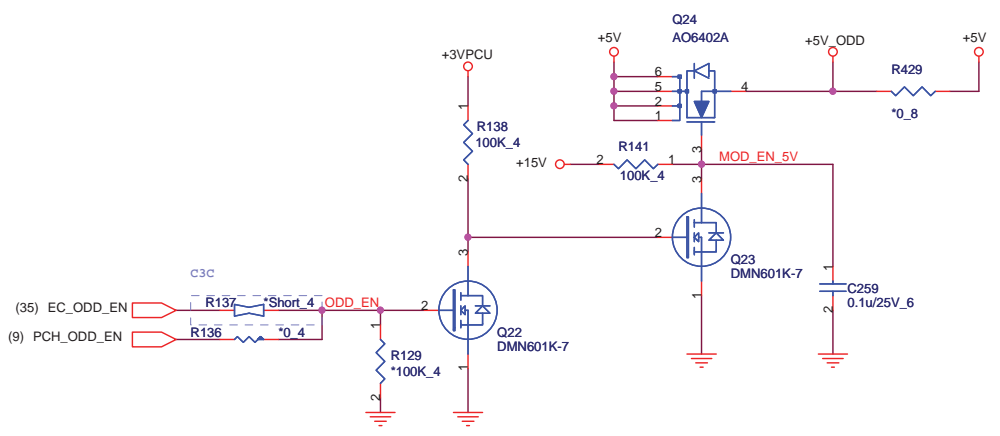
SATA ODD (ODD)



HOLE(OTH)



ODD POWER(ODD)

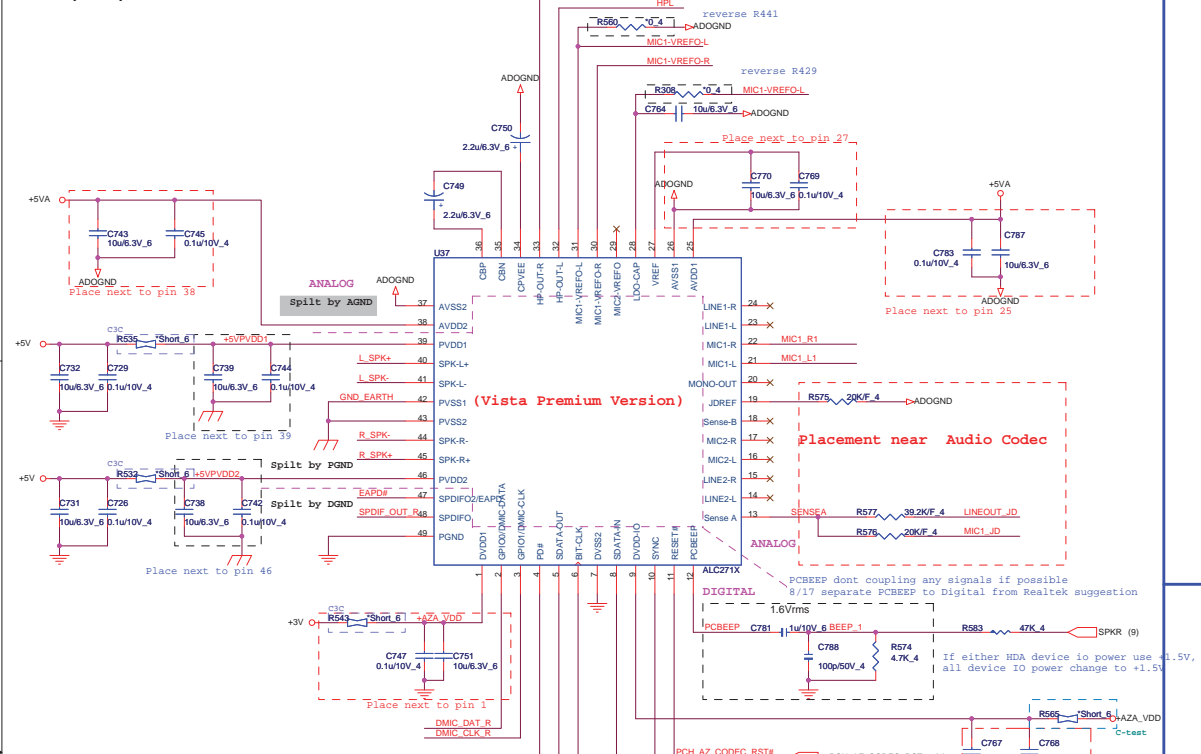


Connect to PCH(GPIO21) pin Y9 and EC pin28(GPIO53)

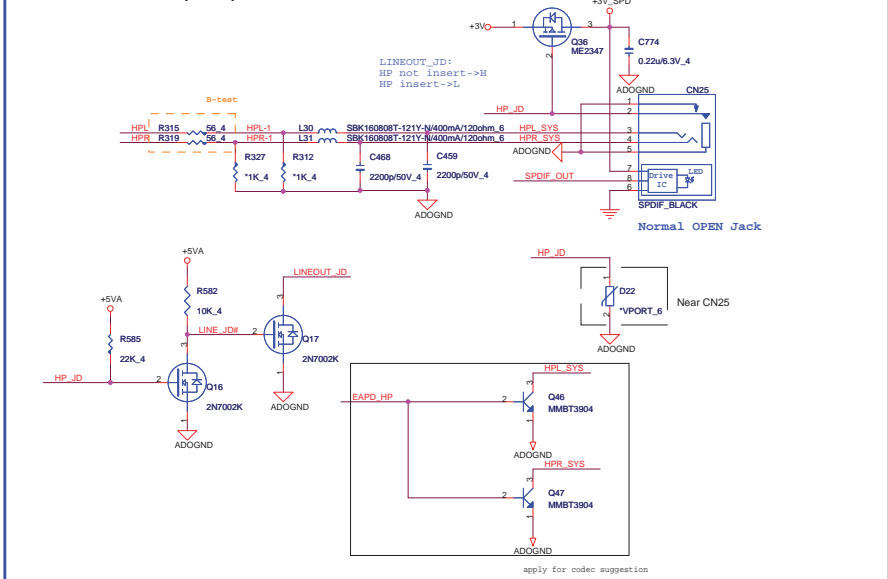
Quanta Computer Inc.
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| | | |
|--------------------------------|--------------------------|-----|
| Size | Document Number | Rev |
| | SATA-HDD/ODD/HOLE | 1A |
| Date: Friday, January 22, 2010 | | |
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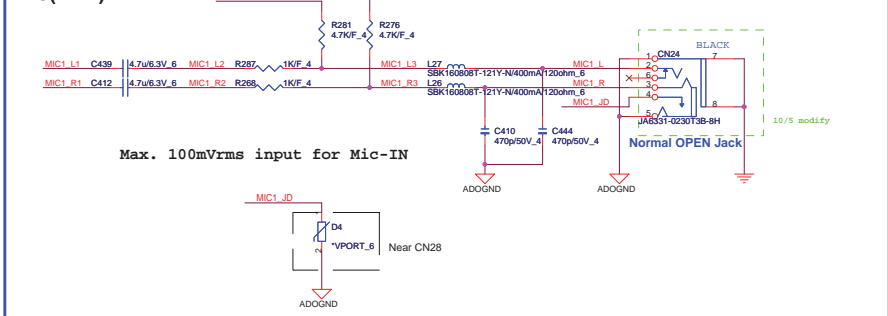
Codec(ADO)



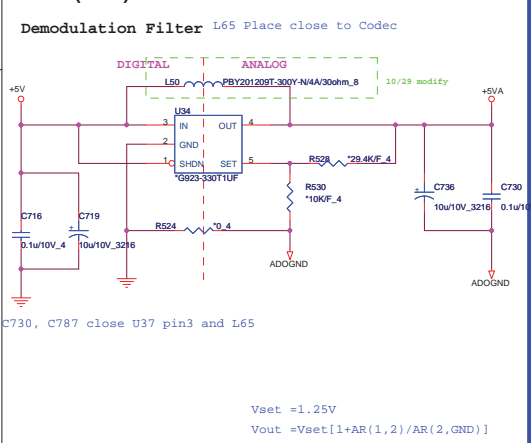
LINE-OUT/SPDIFO(AMP)



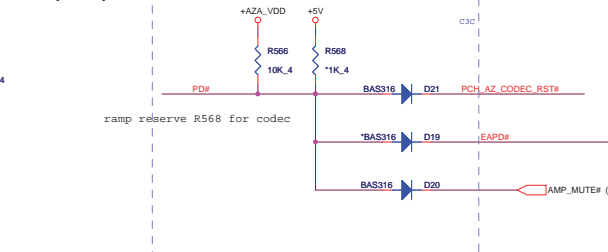
MIC(AMP)



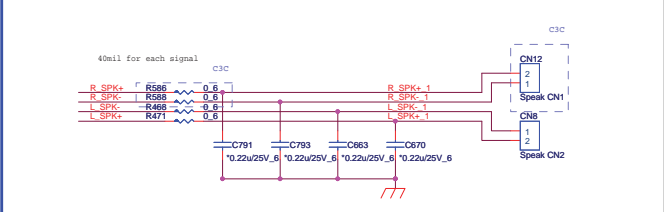
Power (ADO)



Mute(ADO)

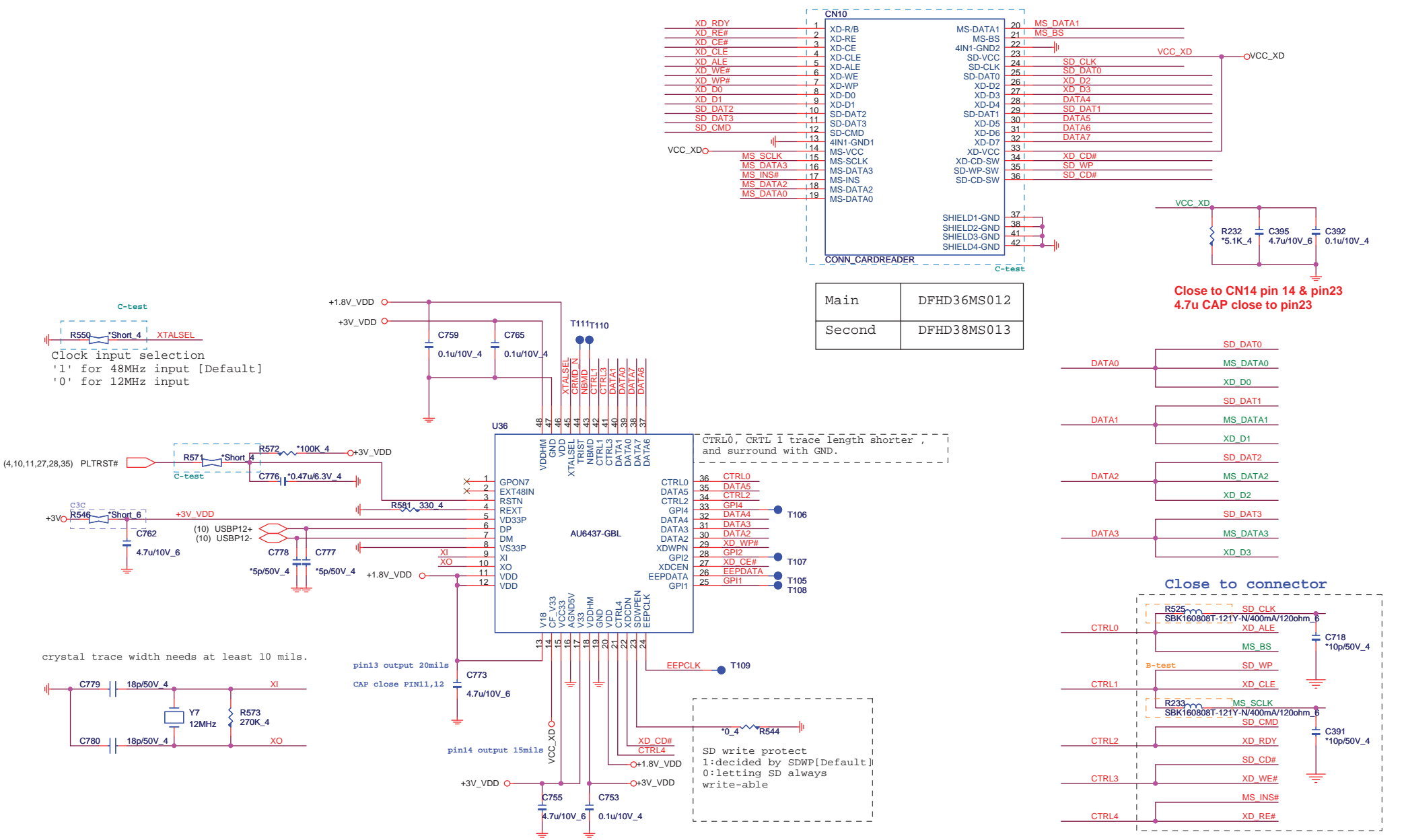


Internal Speaker(AMP)

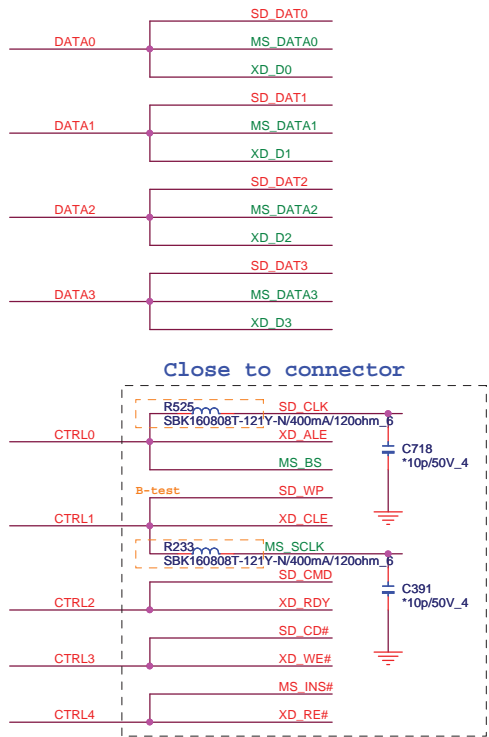


Cardreader(MMC)

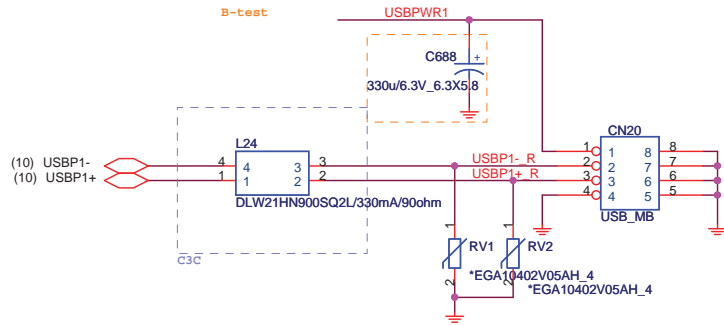
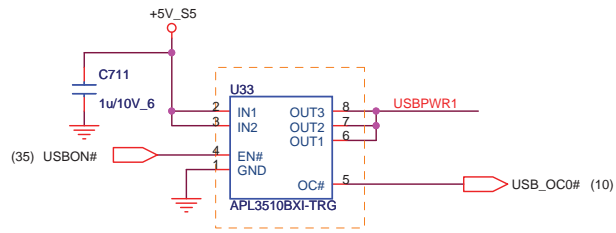
4 IN 1 CARD READER (MMC)



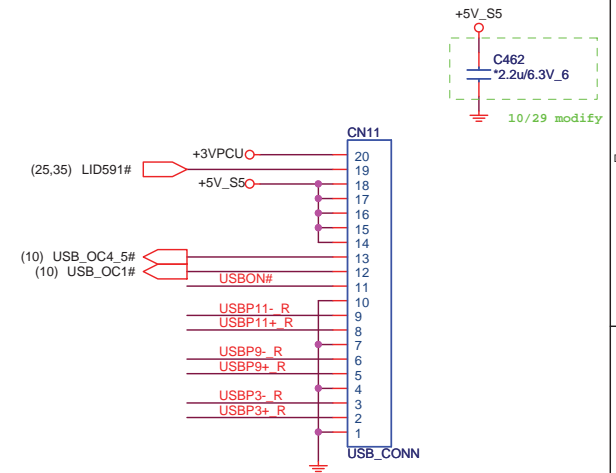
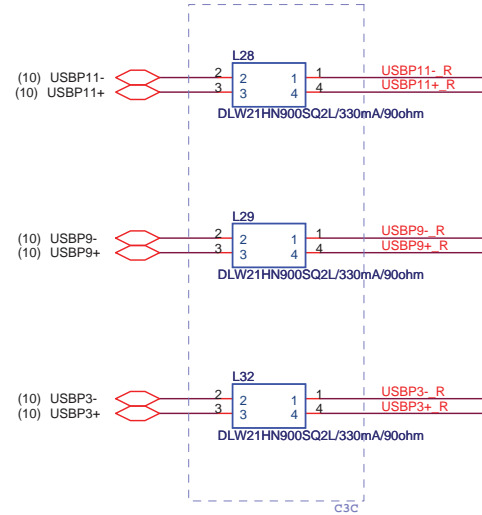
| | |
|--------|-------------|
| Main | DFHD36MS012 |
| Second | DFHD38MS013 |



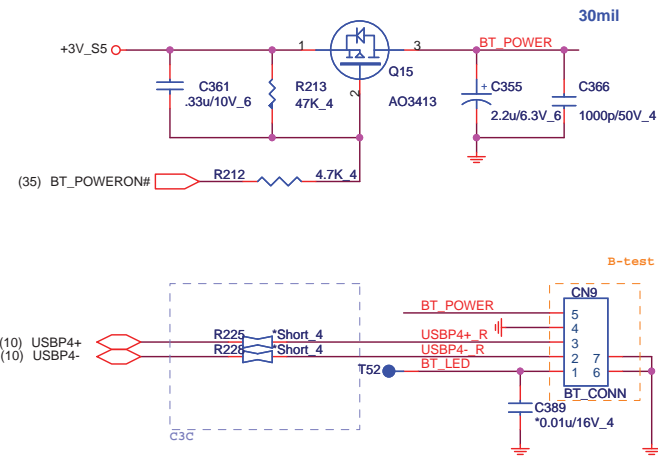
USB PORT(USB)



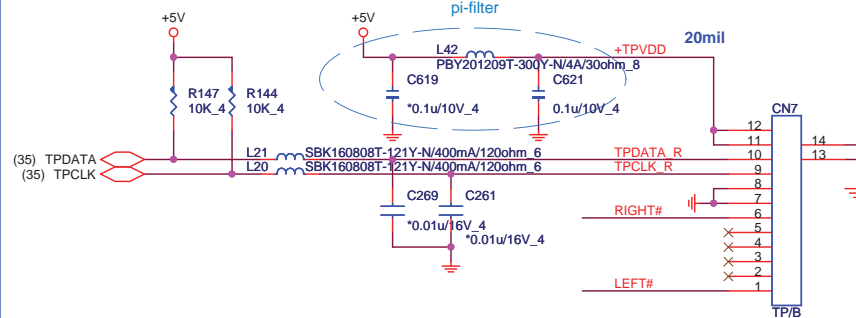
USB BOARD CONN(USB)



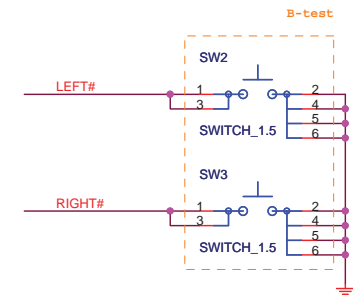
BLUETOOTH CONN(BTM)



TOUCHPAD BOARD CONN(TPD)



TP SWITCH(UIF)



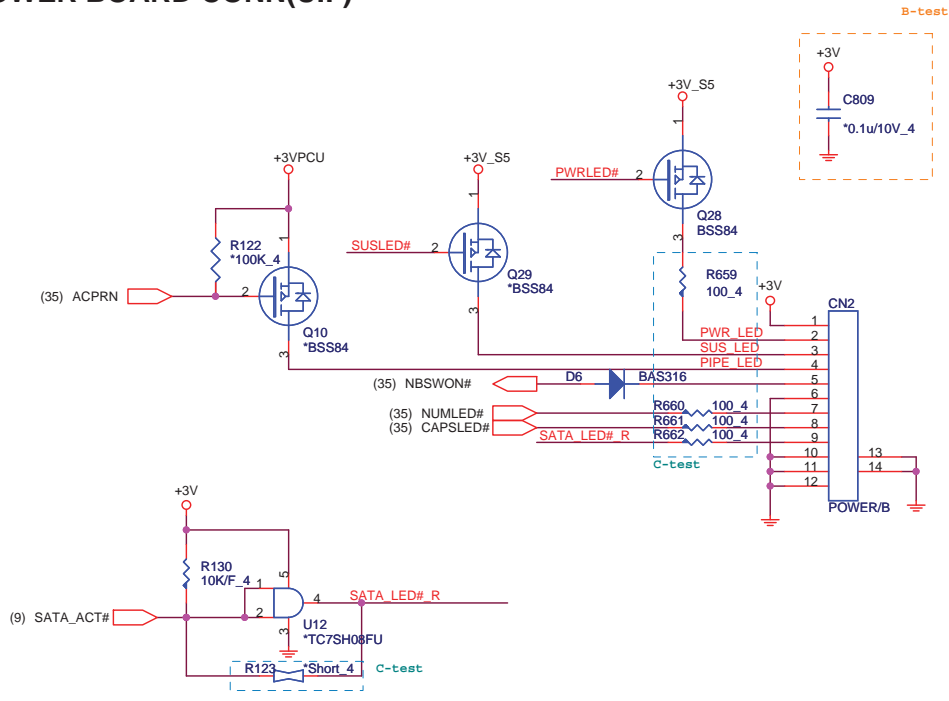
Quanta Computer Inc.

PROJECT : ZQ1

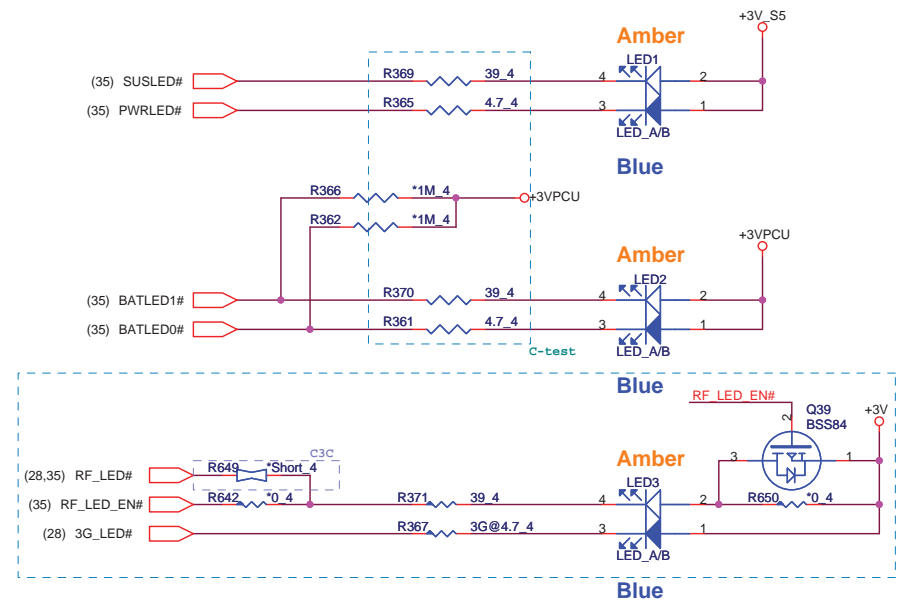
| | | |
|------|-----------------|-----|
| Size | Document Number | Rev |
| | eSATA/USB | 1A |

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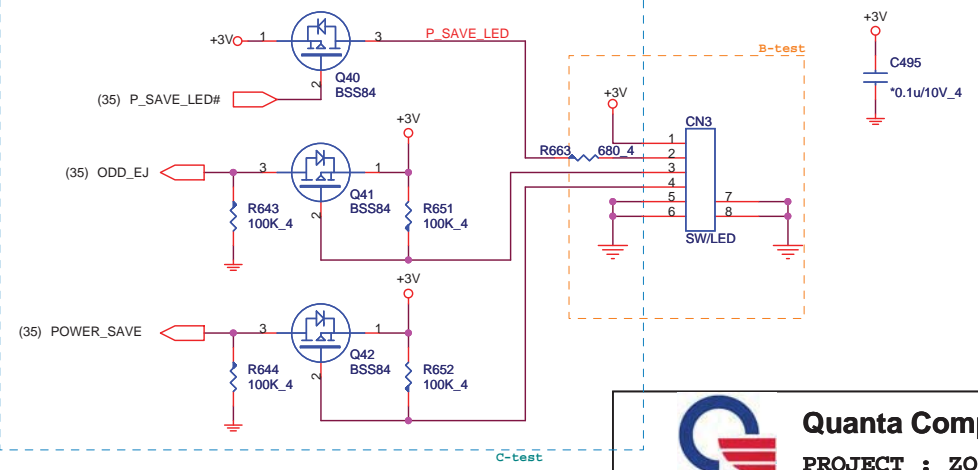
POWER BOARD CONN(UIF)



LED(UIF)



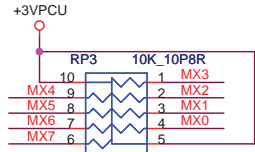
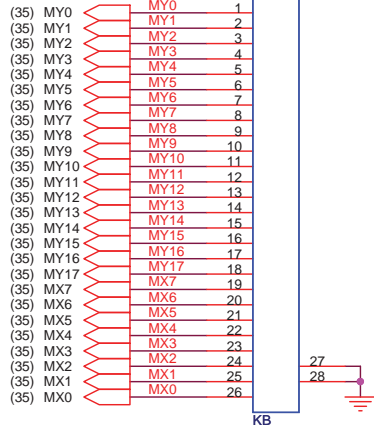
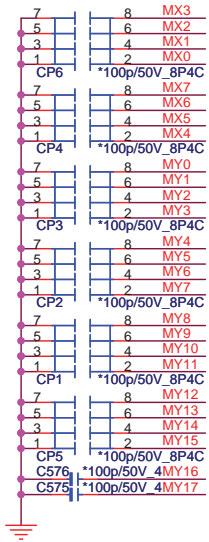
SW BOARD CONNECTOR(UIF)



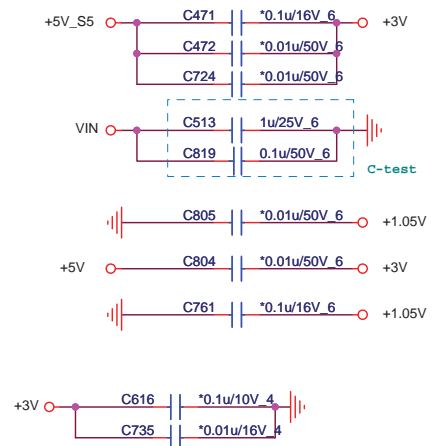
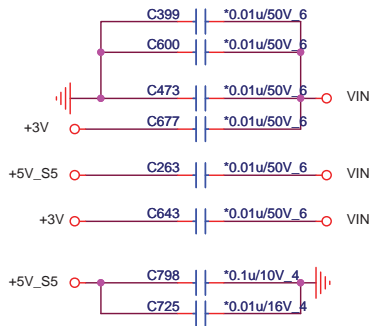
Quanta Computer Inc.
 PROJECT : ZQ1

| | | |
|-------|------------------------------|----------------|
| Size | Document Number | Rev |
| | POWER BOARD/LED/SW DB | 1A |
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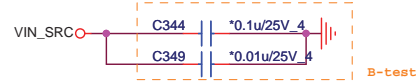
14" K/B(KBC)



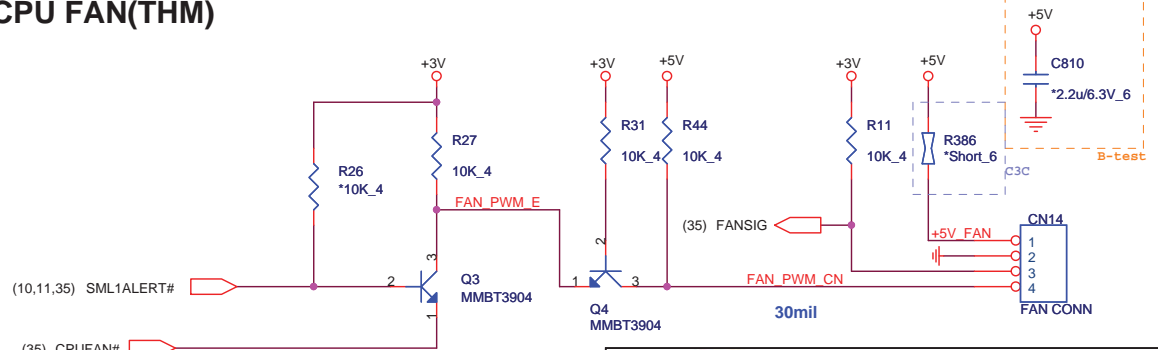
EE RETURN-PATH CAPACITORS(EMC)



STITCHING for LPC



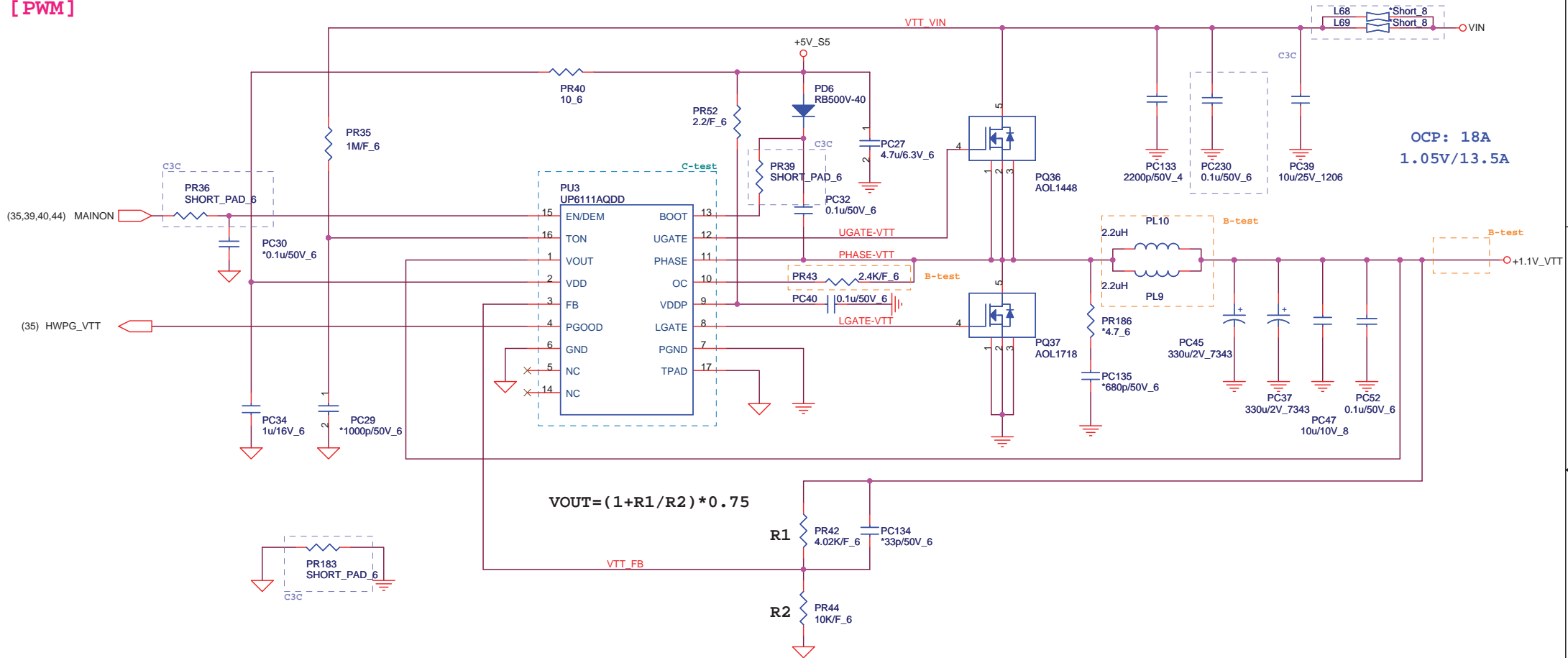
CPU FAN(THM)



Quanta Computer Inc.
PROJECT : ZQ1

| | | |
|-------|-----------------------------|----------------|
| Size | Document Number | Rev |
| | KB/FAN/EE RETURN CAP | 1A |
| Date: | Friday, January 22, 2010 | Sheet 34 of 48 |


[PWM]

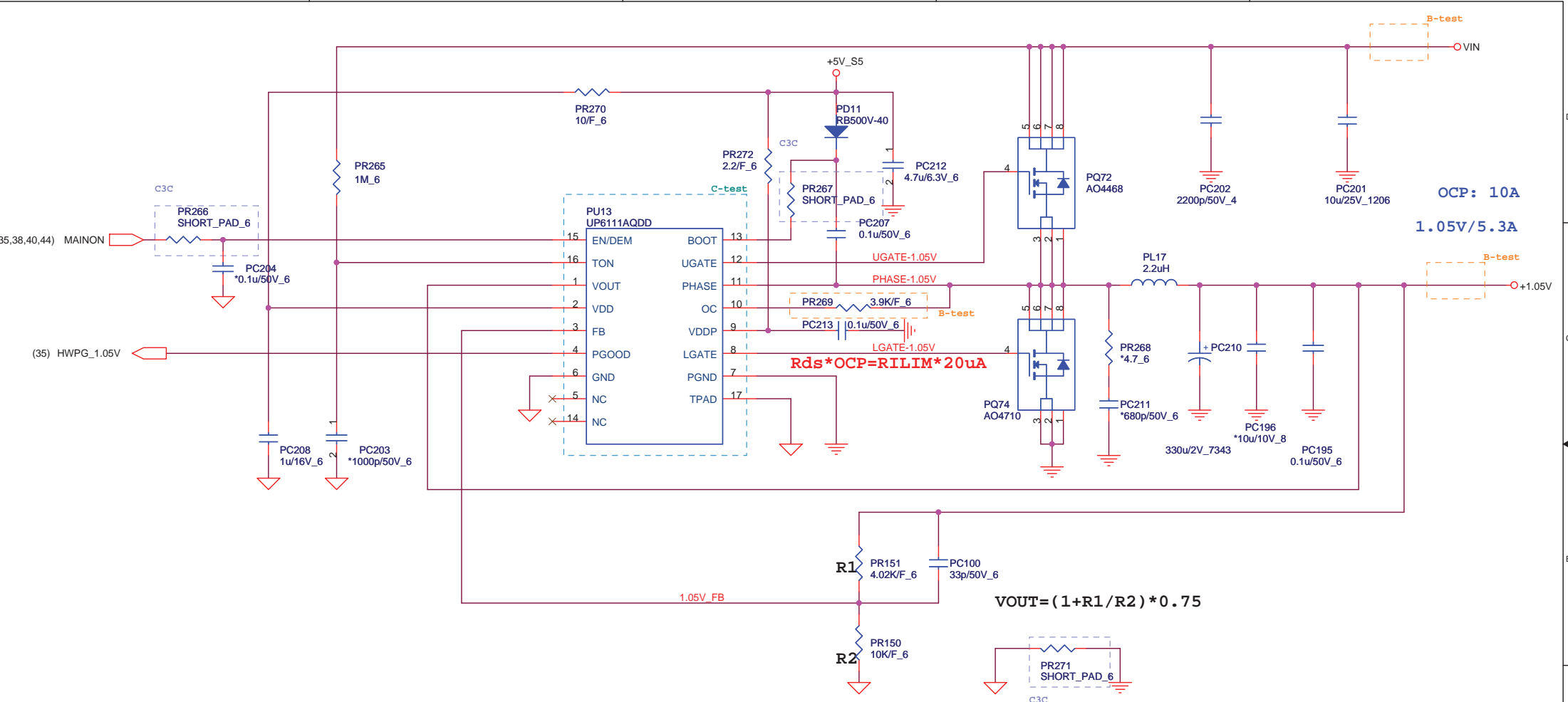


$$V_{OUT} = (1 + R1/R2) * 0.75$$

$TON = 3.85p * RTON * Vout / (Vin - 0.5)$
 $Frequency = Vout / (Vin * TON)$
 $TON = 3.85p * 1M * 1 / (Vin - 0.5)$
 $Frequency = 1 / (0.0036767) = 272K$

AO1718 $R_{dson} = 3 \sim 4.3m\Omega$
 $L(\text{ripple current}) = (19 - 1.05) * 1.05 / (1\mu * 272k * 19) \sim 3.64\mu H$
 $4.3m * 18 = RILIM * 20\mu A$
 $RILIM = 3.87K \text{ --- } 3.92K$

| | | |
|--|--|-----------------|
|  Quanta Computer Inc. PROJECT : ZQ1 | | Size |
| | | Document Number |
| +VTT (UP611A) | | Rev |
| Date: Friday, January 22, 2010 | | 1A |
| Sheet 38 of 48 | | |



OCP: 10A
1.05V/5.3A

$$R_{ds} * OCP = R_{ILIM} * 20\mu A$$

$$V_{OUT} = (1 + R1/R2) * 0.75$$

$$T_{ON} = 3.85p * R_{TON} * V_{out} / (V_{in} - 0.5)$$

$$Frequency = V_{out} / (V_{in} * T_{ON})$$

$$T_{ON} = 3.85p * 1M * 1 / (V_{in} - 0.5)$$


$$Frequency = 1 / (0.0036767) = 272K$$

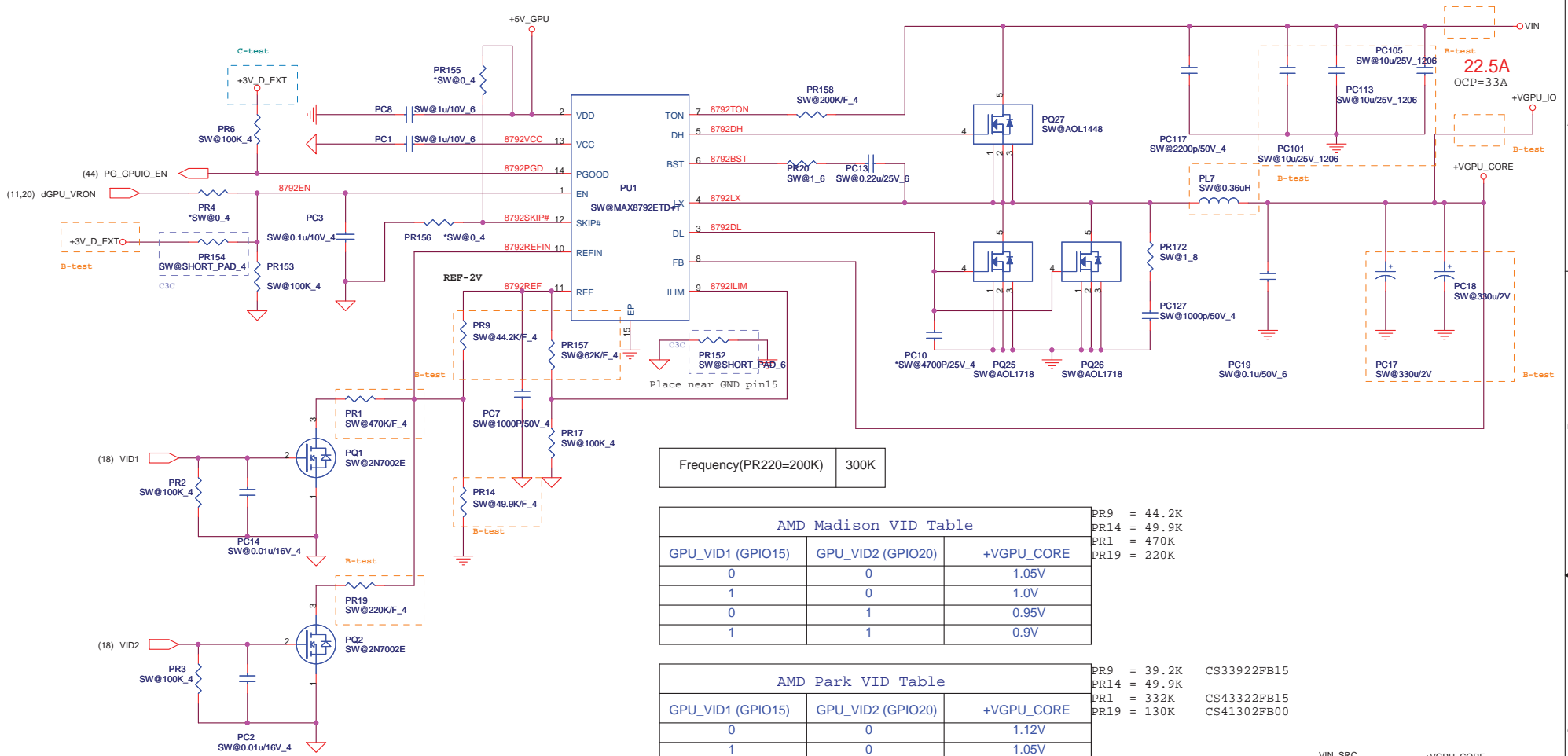
AO4710 $R_{dson} = 11.7 \sim 14.2m\Omega$

L(ripple current)
 $= (19 - 1.05) * 1.05 / (1\mu * 272k * 19)$
 $\sim 3.646A$

$14.2m * 10 = R_{ILIM} * 20\mu A$

$R_{ILIM} = 7.1K \text{ --- } 7.15K$

| | | | | |
|---|--------------------------|-------|----------------------------|-------|
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| | | | VCCP 1.05V(UP6111A) | 1A |
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AMD Madison VID Table

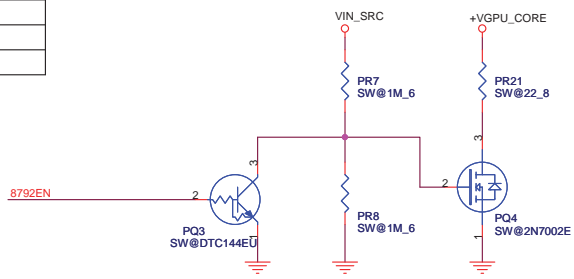
| GPU_VID1 (GPIO15) | GPU_VID2 (GPIO20) | +VGPU_CORE |
|-------------------|-------------------|------------|
| 0 | 0 | 1.05V |
| 1 | 0 | 1.0V |
| 0 | 1 | 0.95V |
| 1 | 1 | 0.9V |

PR9 = 44.2K
 PR14 = 49.9K
 PR1 = 470K
 PR19 = 220K

AMD Park VID Table

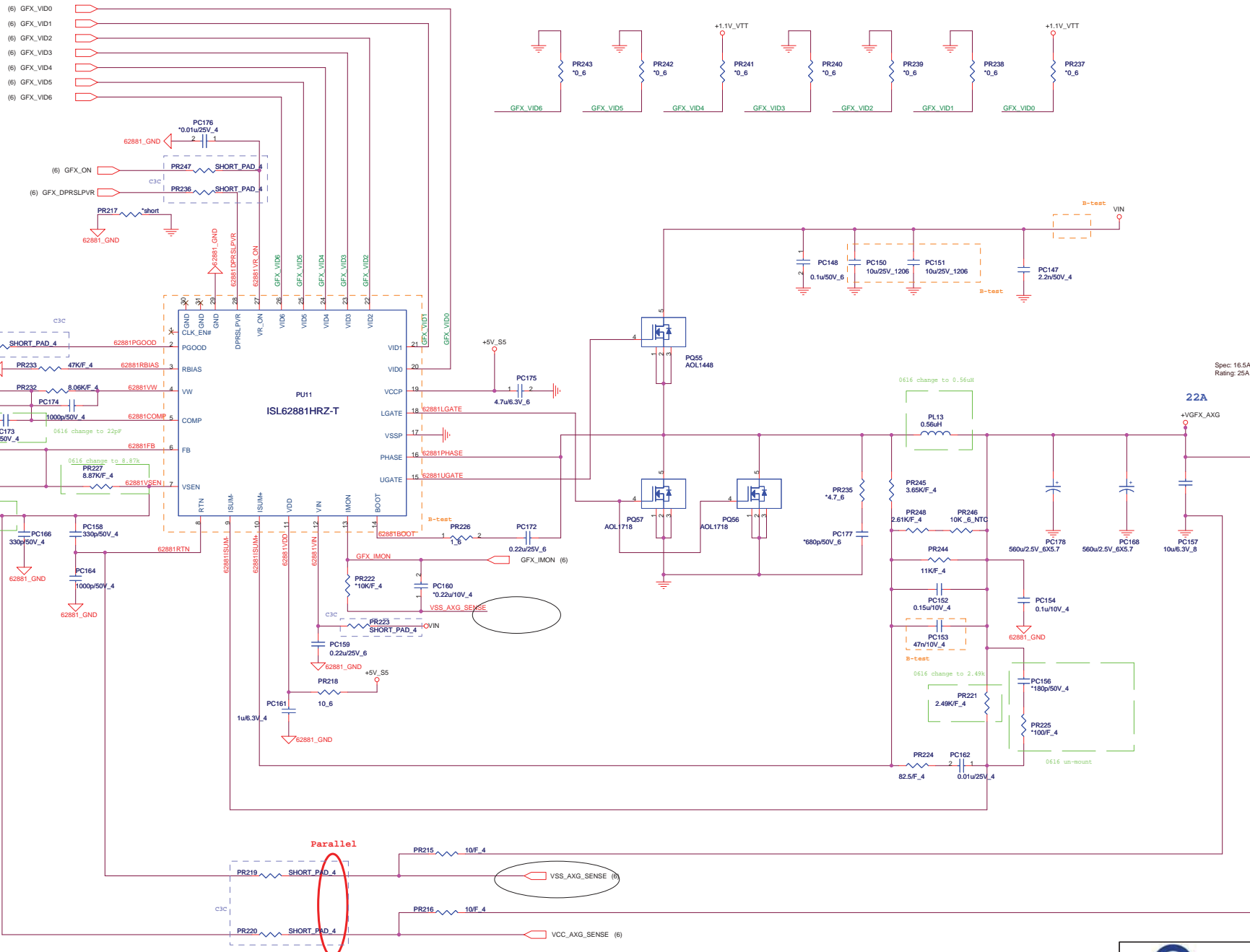
| GPU_VID1 (GPIO15) | GPU_VID2 (GPIO20) | +VGPU_CORE |
|-------------------|-------------------|------------|
| 0 | 0 | 1.12V |
| 1 | 0 | 1.05V |
| 0 | 1 | 0.95V |
| 1 | 1 | 0.9V |

PR9 = 39.2K CS33922FB15
 PR14 = 49.9K
 PR1 = 332K CS43322FB15
 PR19 = 130K CS41302FB00



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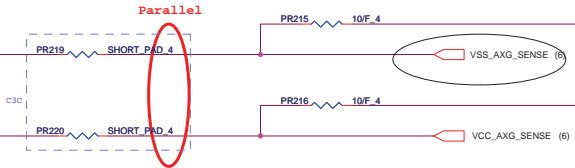
| | | |
|-------|--------------------------|----------------|
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| | GPU CORE(MAX8792) | 1A |
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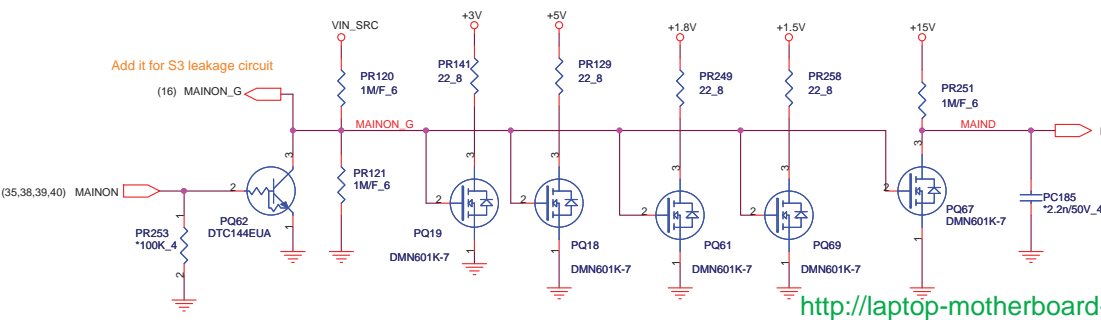
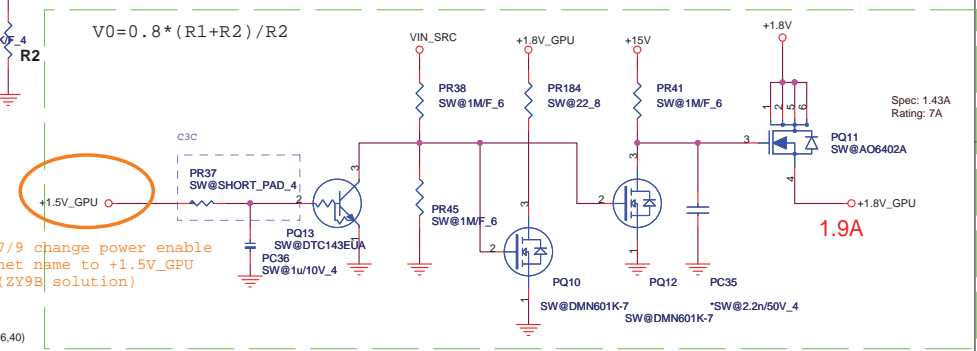
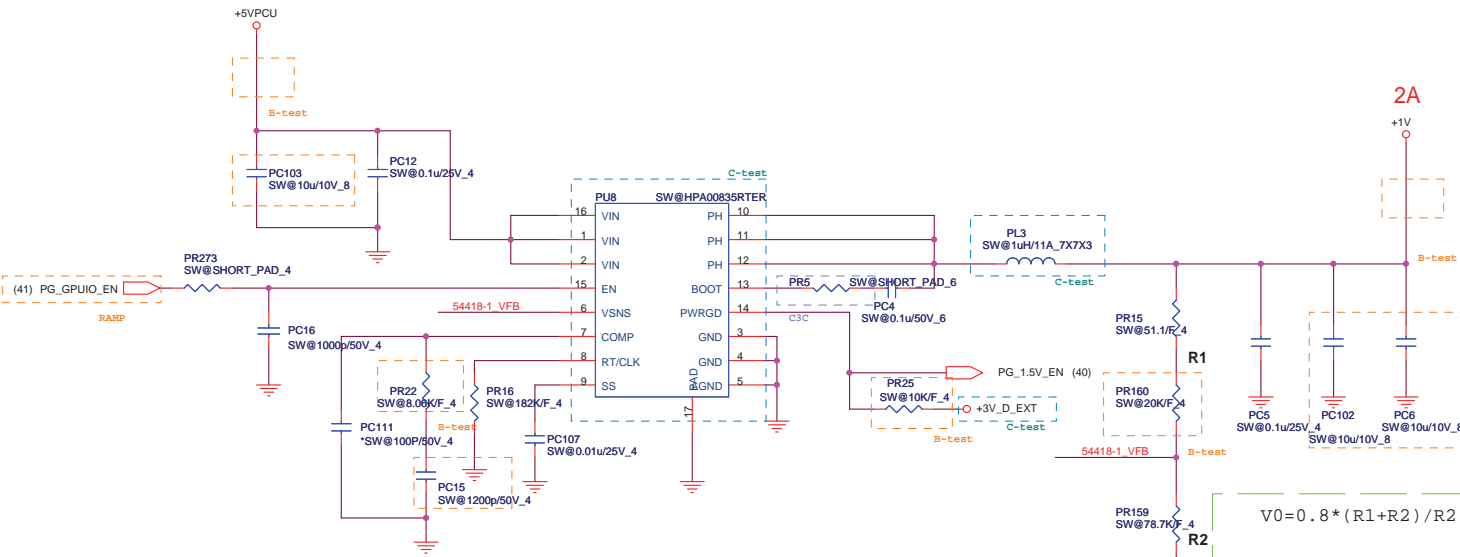
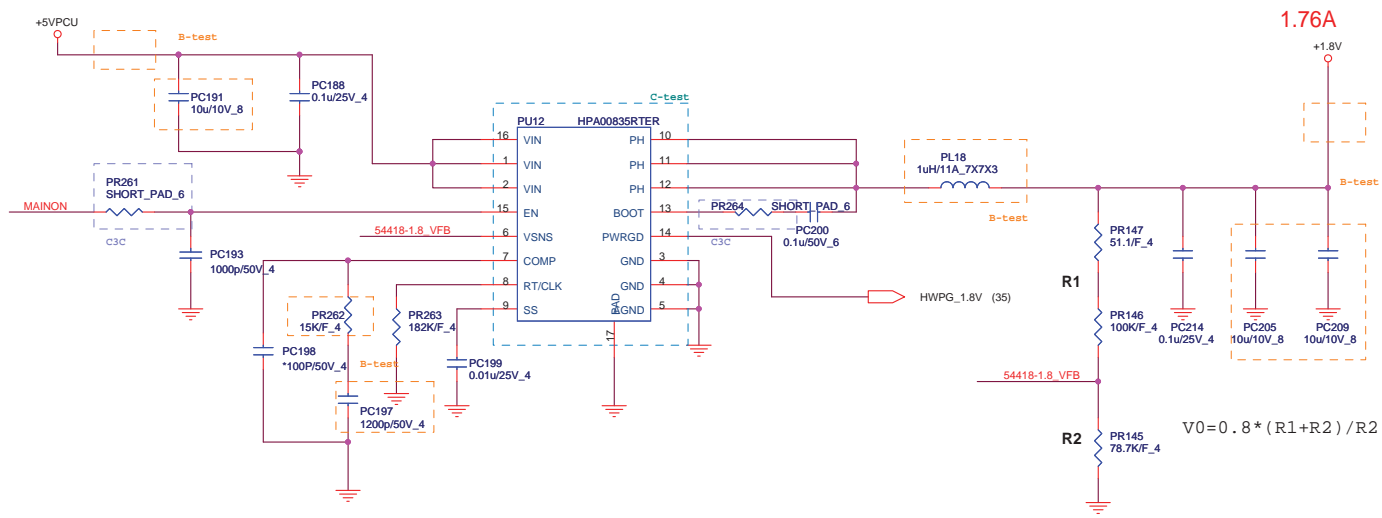
DRC=2.7~3mOhm/2

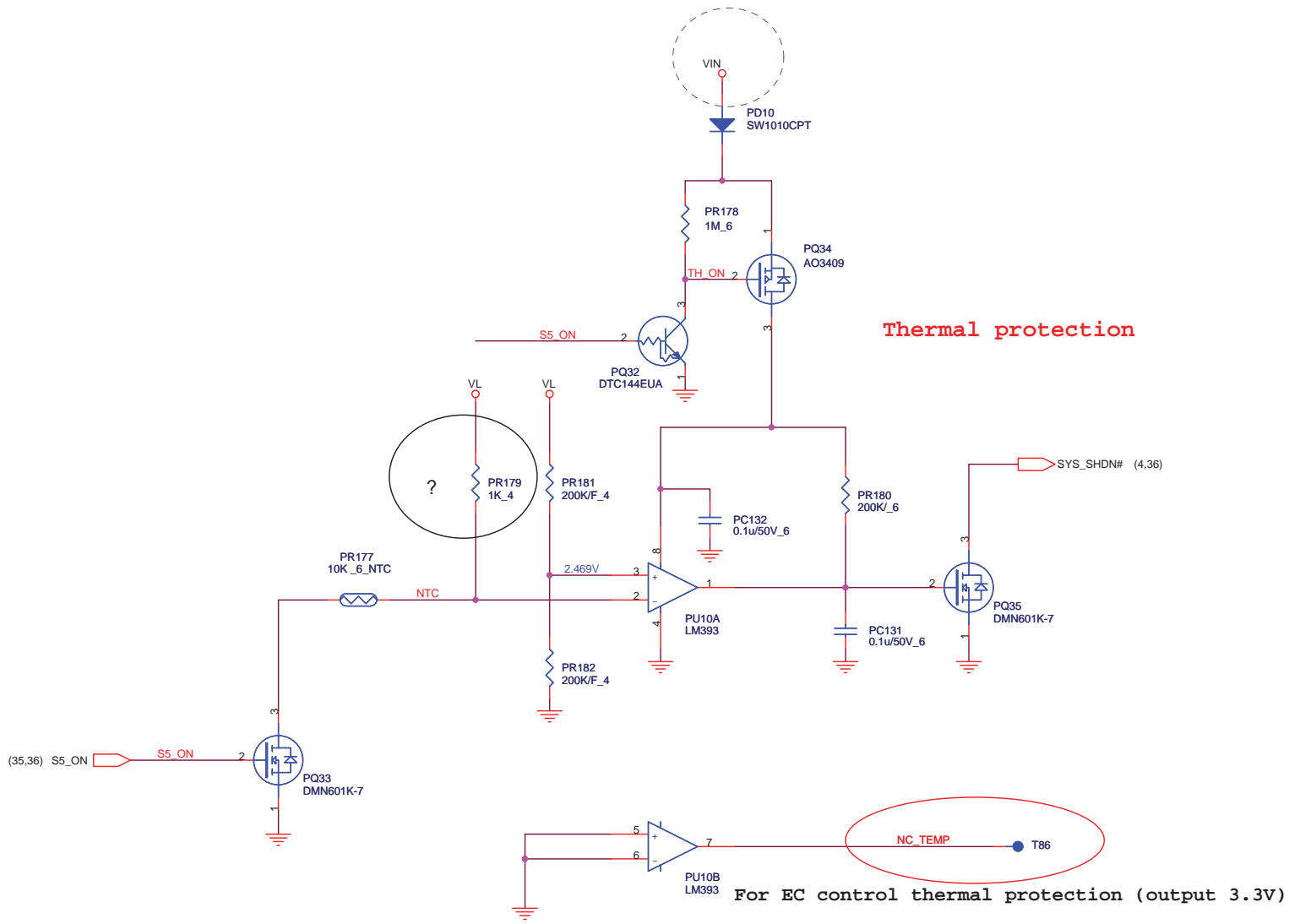
Load Line=7mV/A
 3m*6.168=0.925m
 0.925m/2.49K=371p
 371p*2*6.87K=6.58m
 OCP
 20u/2*2.42K=24.2m
 24.2m/0.6168=36.64m
 36.64m/3m=12.21A


Spec: 16.5A
 Rating: 25A



1.Level 1 Environment-related Substances should NEVER be Used.
 2.Purchase Ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.





| | | |
|--|--------------------------|----------------|
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| | | 1A |
| Size | Document Number | |
| Thermal Protection | | |
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