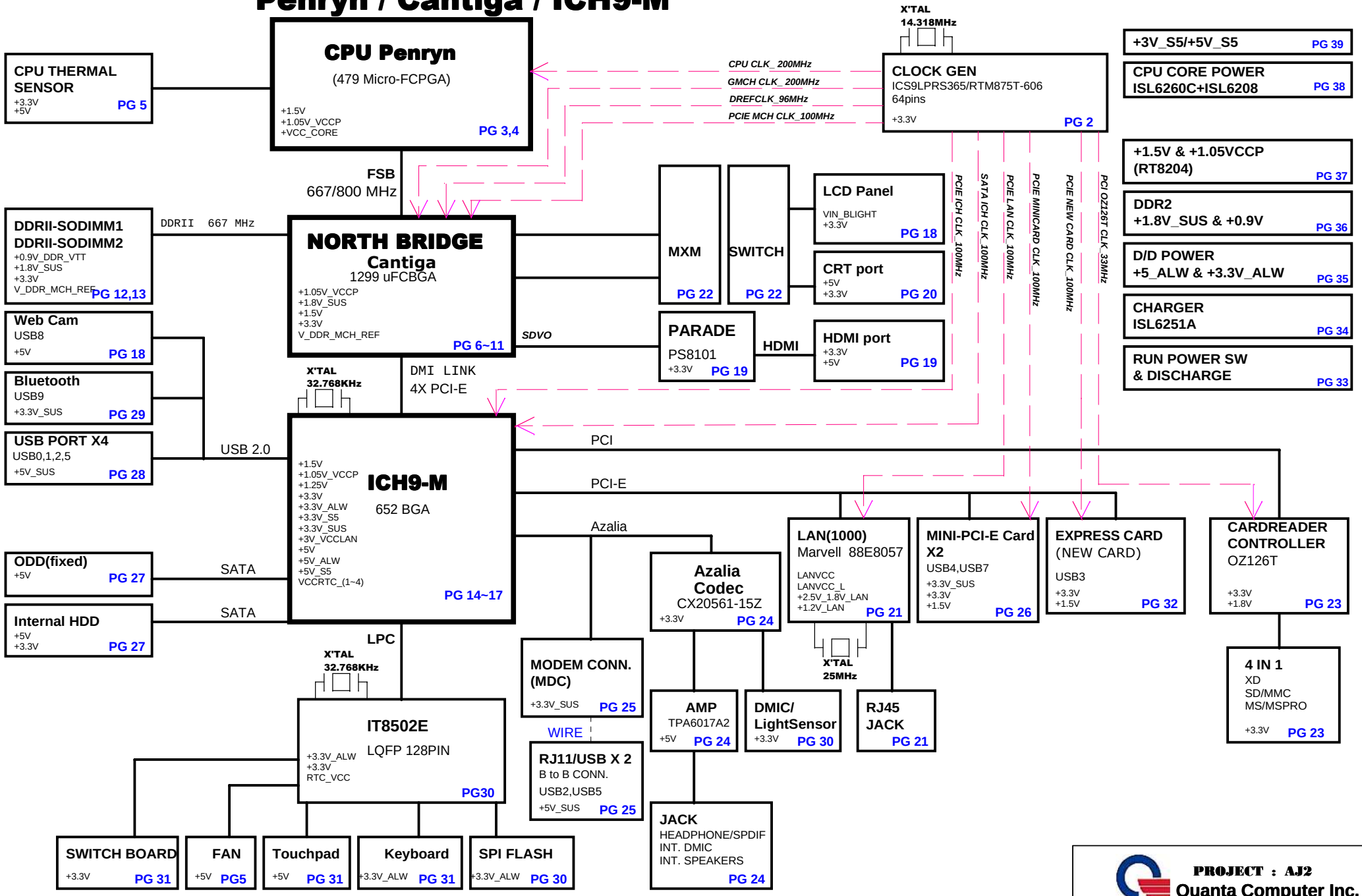
AJ2 BLOCK DIAGRAM

Penryn / Cantiga / ICH9-M

(Montevina Platform)



PROJECT : AJ2

Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

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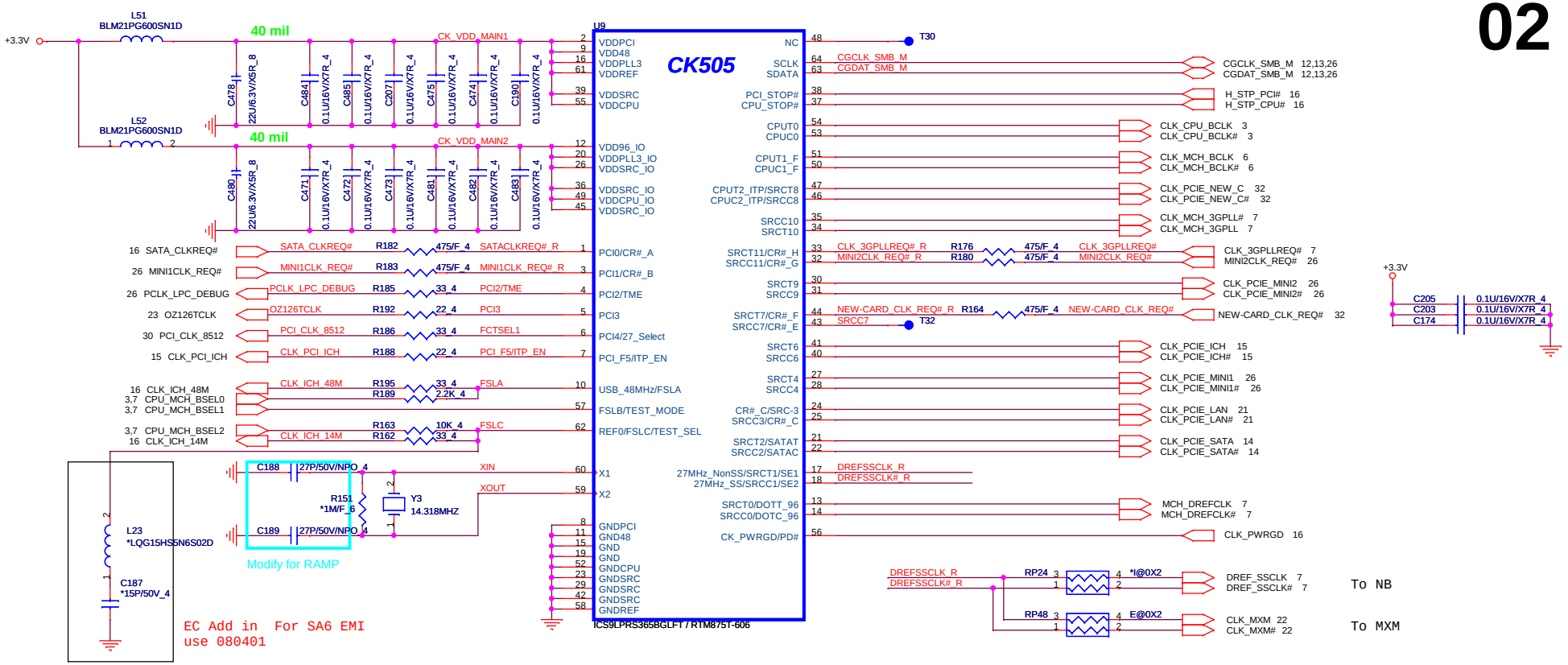
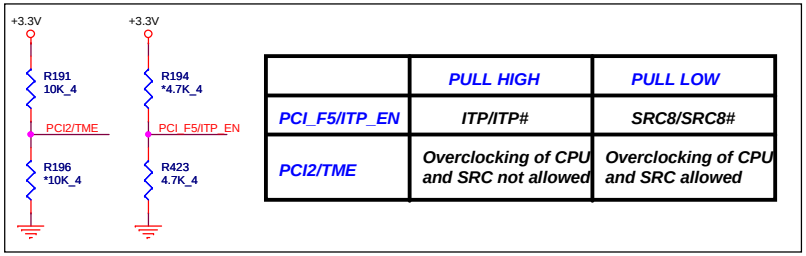
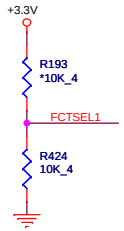


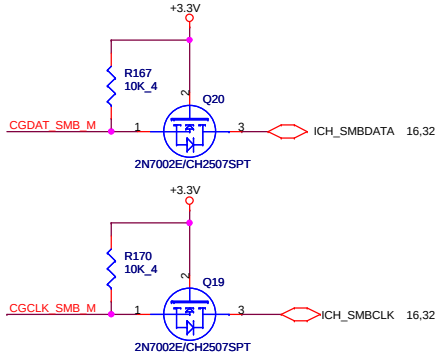


	PULL HIGH	PULL LOW
PCI_F5/ITP_EN	ITP/ITP#	SRC8/SRC8#
PCI2/TME	Overclocking of CPU and SRC not allowed	Overclocking of CPU and SRC allowed

GCLK_SEL = FCTSEL1

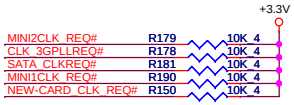
FCTSEL1 (PIN6)	PIN13	PIN14	PIN17	PIN18
0=UMA	DOT96	DOT96#	SRC-1/LCDT_100	SRC-1#/LCDT_100
1 = External VGA	SRC-0	SRC-0#	27Mout-NSS	27Mout-SS

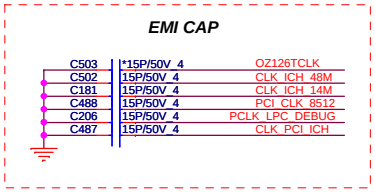


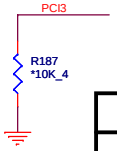


CPU Clock select

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100.00	100	33
0	0	1	133.33	100	33
0	1	1	166.66	100	33
0	1	0	200.00	100	33
0	0	0	266.66	100	33
1	0	0	333.33	100	33
1	1	0	400.00	100	33
1	1	1	200.00	100	33







	PULL HIGH	PULL LOW
PCI3	PIN37/38 is CPU_STOP/PCI_STOP PIN37/38 IS SRC5.	**SRC5_EN/PCI-3 (Internal Pull Low)

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Quanta Computer Inc.

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Custom	CLOCK GENERATOR	1A
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03

U18A — Penryn Ball-out Rev 1a

U18B — Penryn Ball-out Rev 1a

Layout Note: Place R288 close to CPU.

Layout Note: Place voltage divider within 0.5" of GTLREF pin

Note: H_DPRTSTP need to daisy chain from ICH9 to IMVP6 to CPU.

Voltage Level shift

For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

Place C close to the CPU_TEST4 pin. Make sure CPU_TEST4 routing is reference to GND and away from other noisy signal.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

Comp0,2 connect with Zo=27.4ohm,Comp1,3 connect with Zo=55ohm, make those traces length shorter than 0.5".Trace should be at least 25 mils away from any other toggling signal.

Populate ITP700Flex for bringup

04/17 jack hsu

ITP700 layout guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm ± 5%	VCCP	Place the pull-up near CPU
TMS	39 ohm ± 1%	VCCP	Within 200ps of ITP connector
TRST#	500 to 680 ohm ± 5%	GND	Place the pull-down near CPU
TCK	27 ohm ± 1%	GND	Connect to TCK pin of CPU and then connect it to FBO pin of ITP connector in daisy chain. Place the pull-down near TCK0 pin of ITP connector
TDO	51 ohm ± 5%	VCCP	Place the pull-up near ITP
RESET#	22.6 ohm ± 1% series resistor and pullup 51 ohm ± 1%.	VCCP	Connect to CPURST# pin of GMCH through the series resistor placed within 200ps of ITP connector. Place the pull-up after the series resistor from ITP connector.

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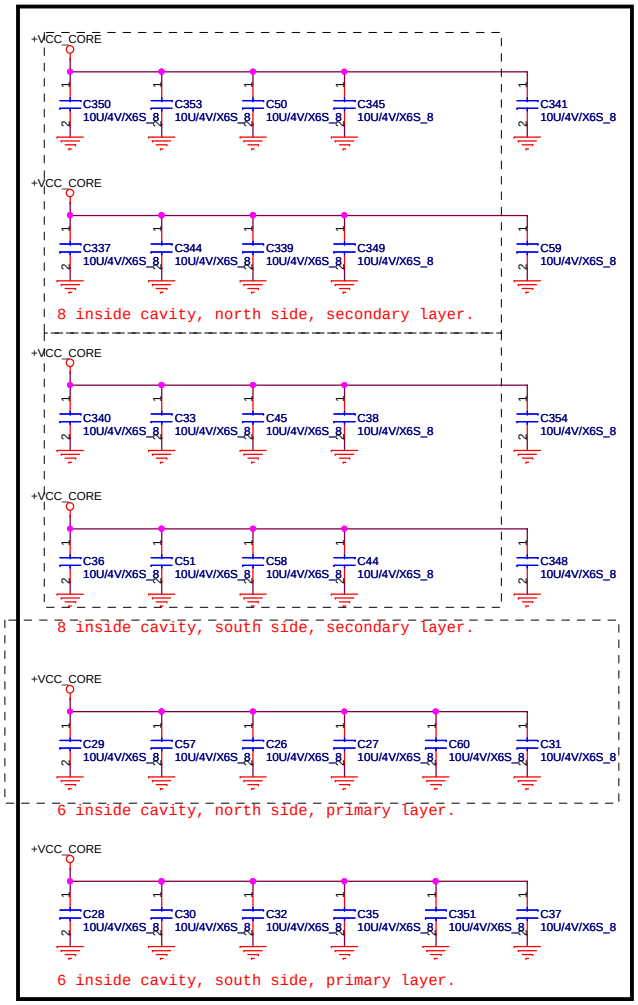
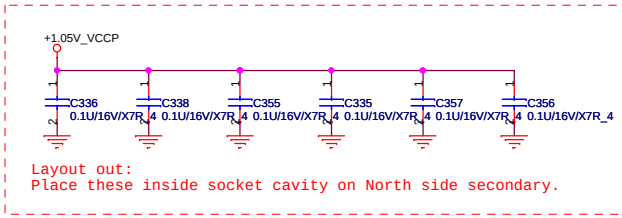
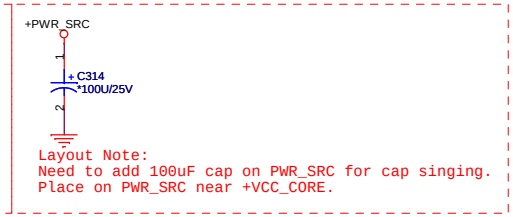
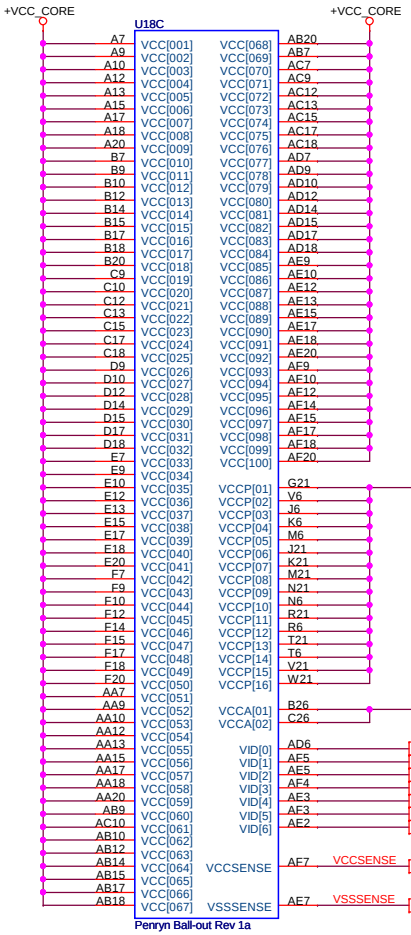
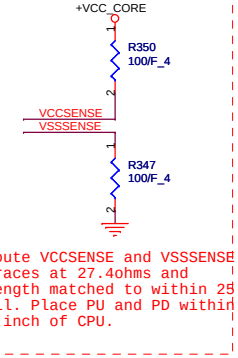
All use 22U 10V(+-20%,X5R,1210)Pb-Free.

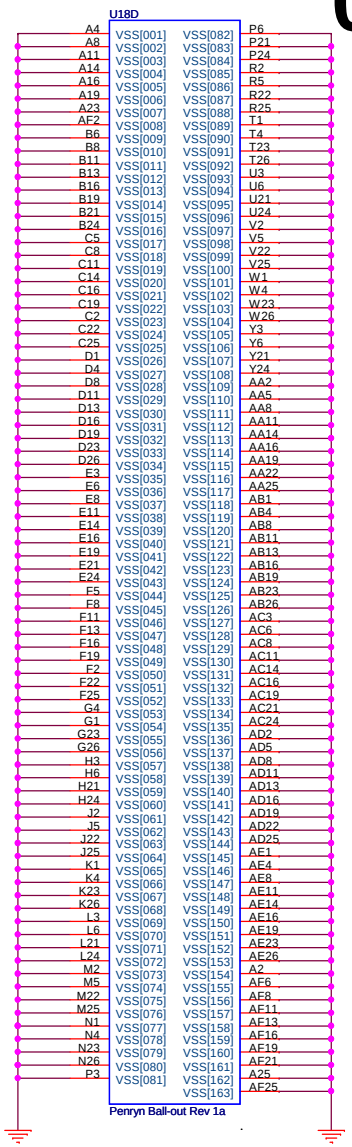












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Quanta Computer Inc.

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Custom	Penryn Processor (POWER)	1A
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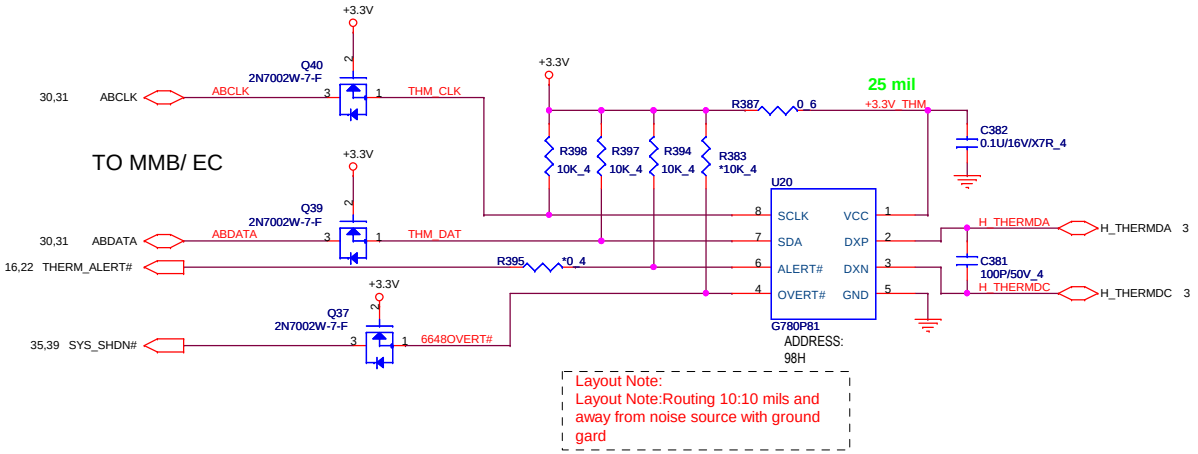
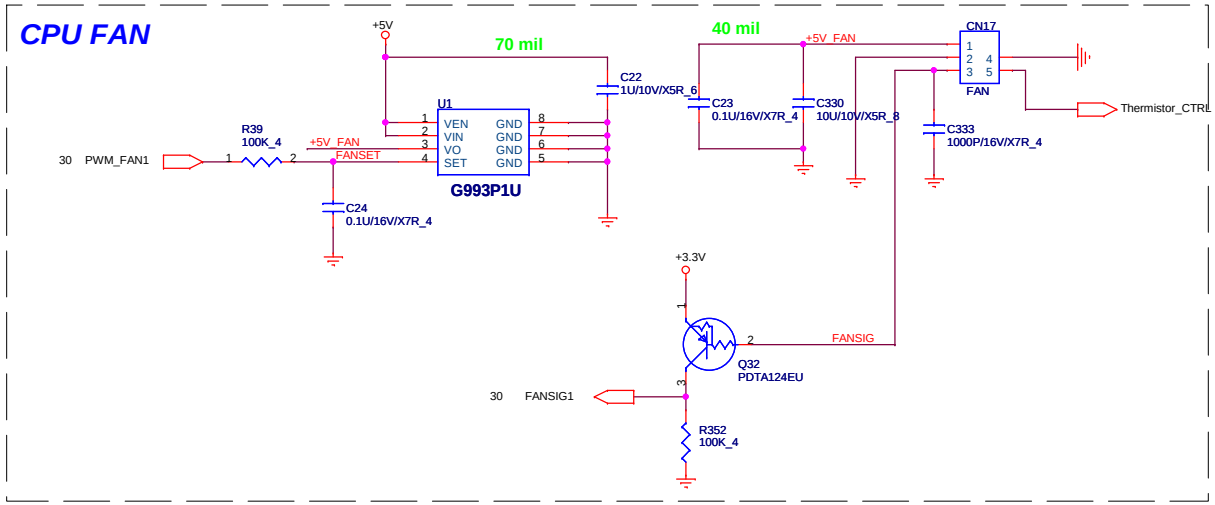
CPU Thermal monitor





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Quanta Computer Inc.			
Size: Custom	Document Number: Thermal IC		Rev: 1A
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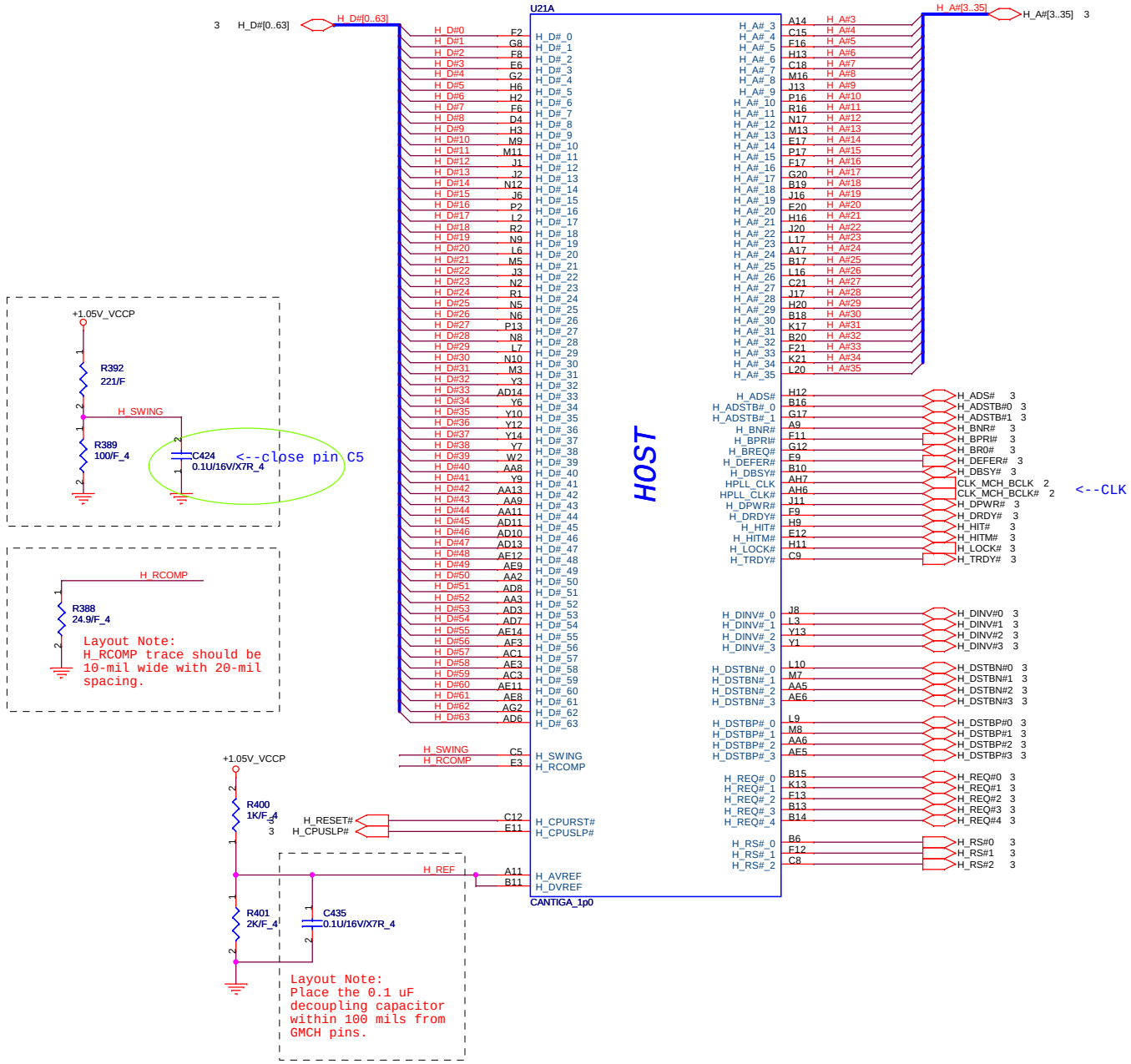

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Custom	Cantiga (HOST)	1A

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U21B

RSVD

DDR CONTROL/COMPENSATION

CLK

DMI

GRAPHICS VID

PWR

NC

MISC

HDA

U21C

LVDS

PCI-EXPRESS GRAPHICS

TV

VGA

pull up/down impedance compensation For Memory

Layout Note: Locoation of all MCH_CFG strap resistors needs to be close to minmize stub.

IV&EV Dis/Enable setting

If LVDS no use,all signal can NC

Layout Note: Place 150 ohm termination resistors close to GMCH.

INTEL FAE Suggest PD for Ext graphics

Layout Note: HSYNC/VSYNC serial R place close to NB

Modify for C-TEST

EMC reserved (Near to pin B28)

Non-iAMT

For ME Management Engine

For Memory

49.9 ohm for cantiga

Can support reversal routing.If CFG9=1, PCI Express is normal operation. If CFG9=0, then PEG_TXP0 becomes PEG_TXP15, PEG_TXP1 becomes PEG_TXP14, PEG_TXP2 becomes PEG_TXP13, etc. similarly for PEG_RXP[15:0] and PEG_RXN[15:0]

CANTIGA_1p0

Modify for C-TEST

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Quanta Computer Inc.

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Custom	Cantiga (VGA,DMI)	1A
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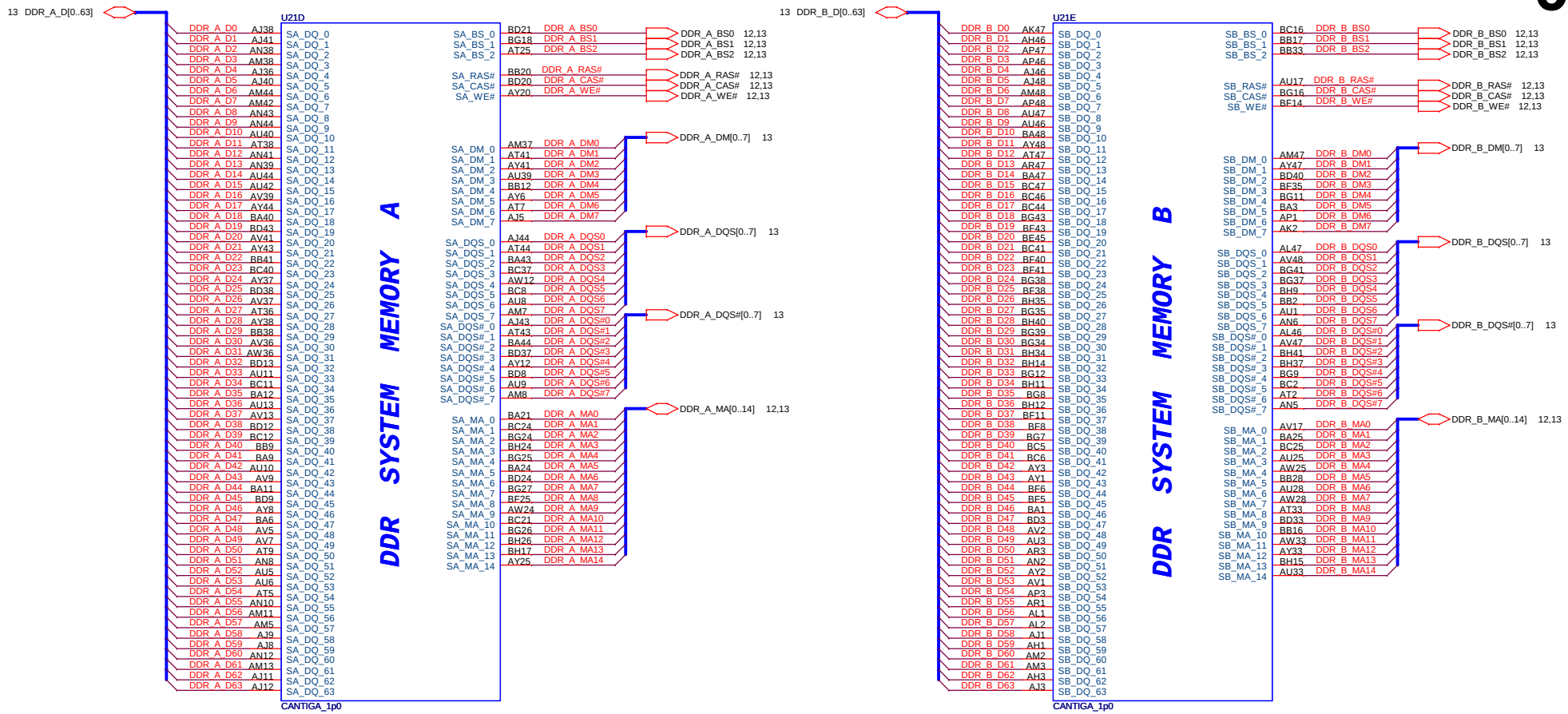
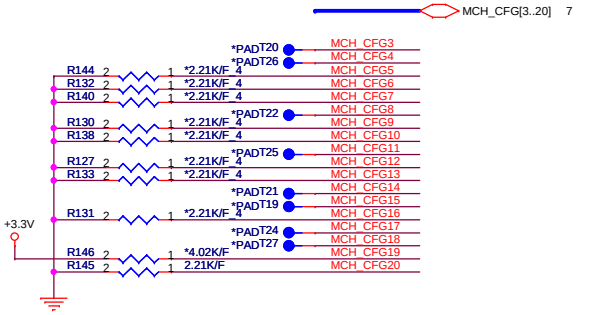
DDR2



STRAPPING

CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4(Default)
CFG6	iTPM Host Interface	Low= Enable High=Disable(Default)
CFG7	Intel Management Engine Crypto Strap	Low= Intel Management Engine Crypto TLS cipher suite with no Confidentiality High=Intel Management Engine Crypto TLS cipher suite with Confidentiality(Default)
CFG9	PCI Express Graphic Lane	Low= Reveise Lane High=Normal operation
CFG10	PCIe Loopback Enable	Low= Enable High=Disable(Default)
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(default). High=Lane Reversed
CFG20	Digital Display Port(SDVO/DP/iHDMI) and PCIe Concurrent Operation.	Low=Only DP or inly PCIe is operational (defaults) High=DP and PCIe x1 are operating simultaneously.
CFG13 / CFG12	XOR / ALLZ / Clock Un-gating	00=Reserved. 10=XOR Mode Enabled. 01=All-Z Mode Enabled. 11=Normal Operation (Default).



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Quanta Computer Inc.

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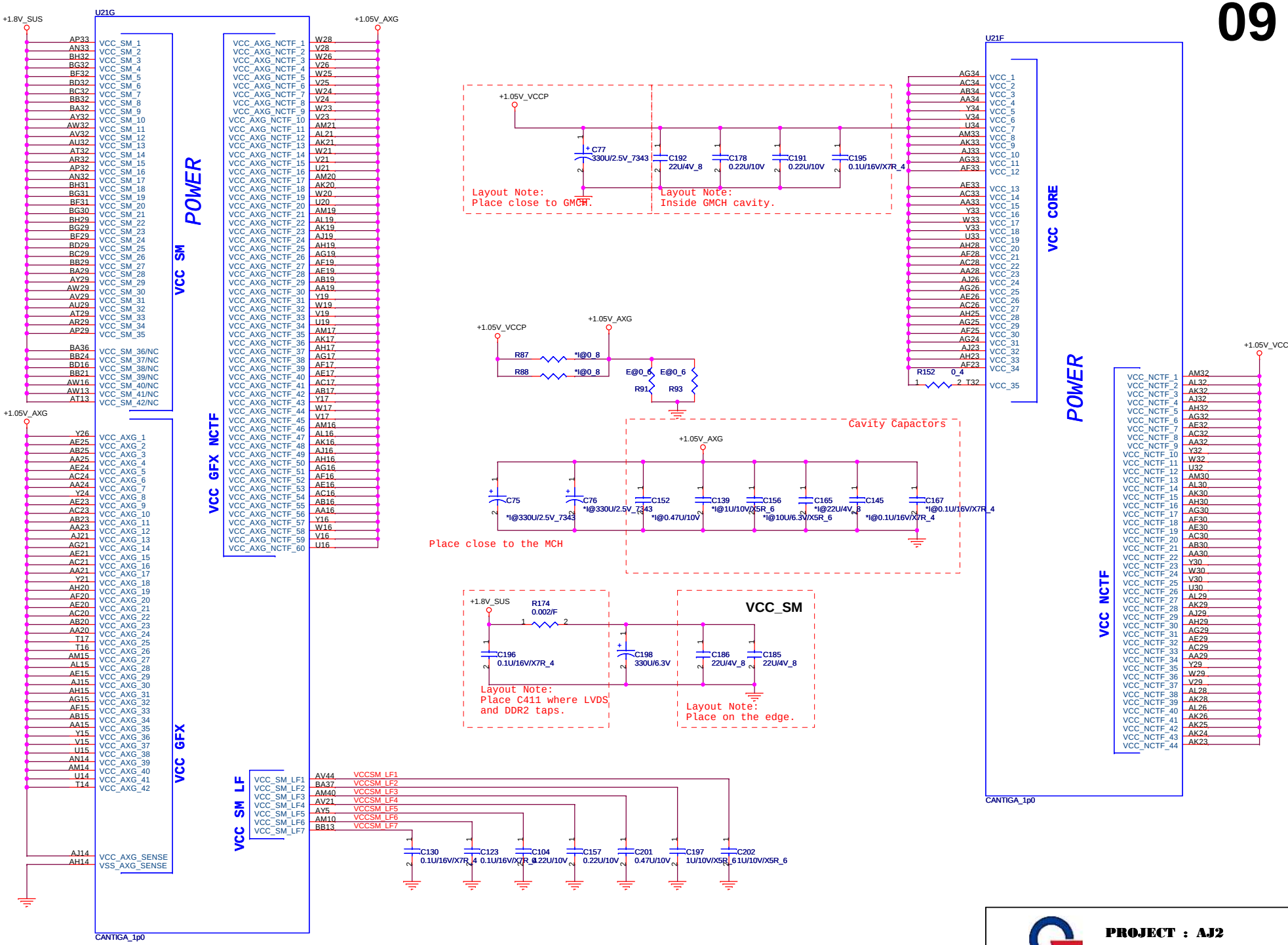

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Quanta Computer Inc.

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Custom	Cantiga (VCC,NCTF)	1A
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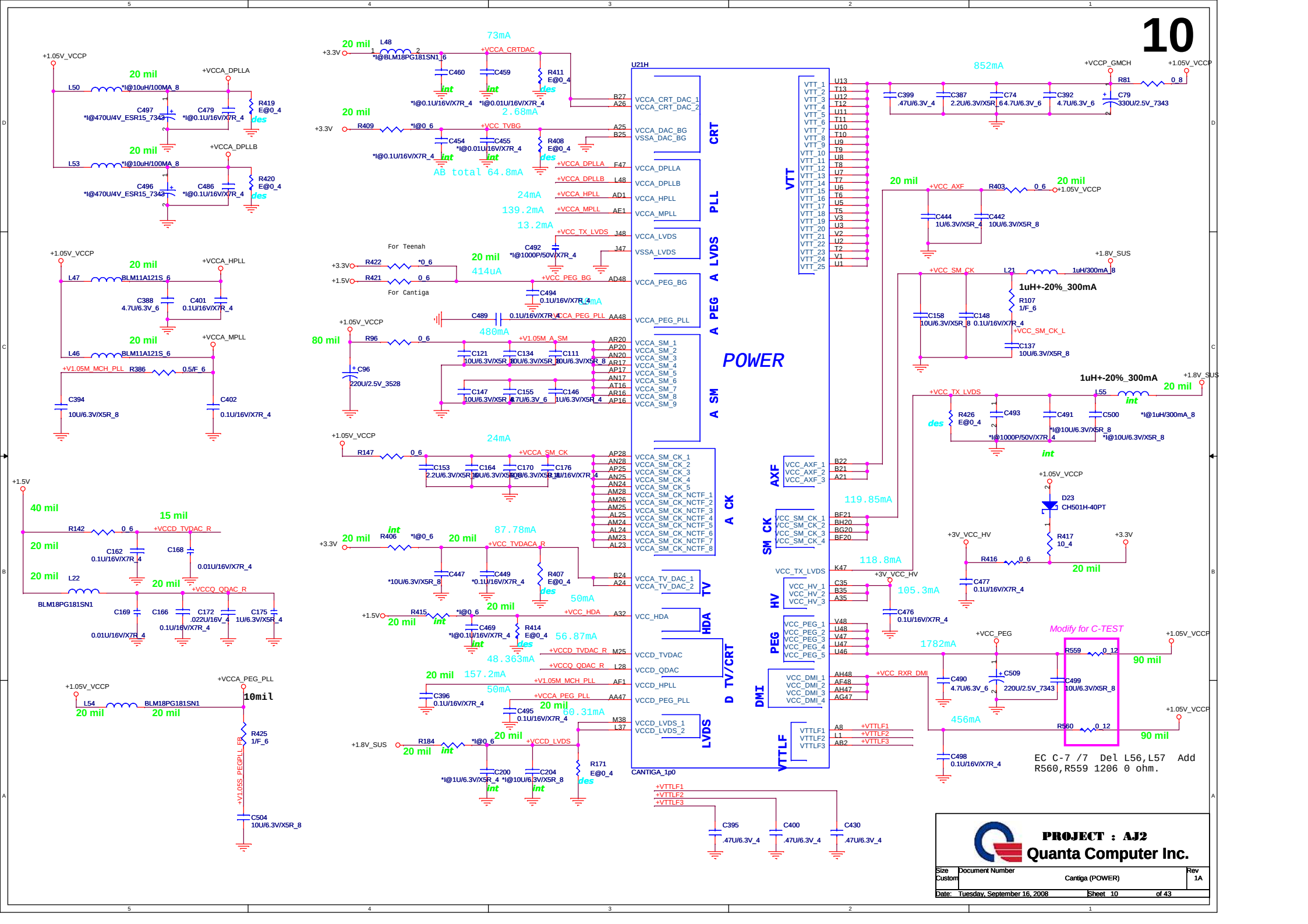
+1.05V_VCCP
+VCCA_DPLLA
L50
*I@10uH/100MA_8
C497
*I@470U/4V_ESR15_7343
C479
*I@0.1U/16V/X7R_4
R419
E@0_4
des
+VCCA_DPLLB
L53
C496
C486
R420
+VCCA_HPLL
L47
BLM11A121S_6
C388
4.7U/6.3V_6
C401
0.1U/16V/X7R_4
+VCCA_MPLL
L46
+V1.05M_MCH_PLL
R386
0.5/F_6
C394
10U/6.3V/X5R_8
C402
+1.5V
R142
0_6
+VCCD_TVDAC_R
C162
C168
0.01U/16V/X7R_4
L22
BLM18PG181SN1
+VCCQ_QDAC_R
C169
C166
C172
.022U/16V_4
C175
1U/6.3V/X5R_4
+VCCA_PEG_PLL
10mil
L54
R425
1/F_6
+V1.05S_PEGPLL_FB
C504
10U/6.3V/X5R_8
+3.3V
L48
*I@BLM18PG181SN1_6
+VCCA_CRTDAC
C460
C459
R411
R409
+VCC_TVBG
C454
C455
R408
+VCCA_DPLLA
+VCCA_DPLLB
+VCCA_HPLL
+VCCA_MPLL
+VCC_TX_LVDS
For Teenah
For Cantiga
R422
R421
+VCC_PEG_BG
C492
*I@1000P/50V/X7R_4
C494
0.1U/16V/X7R_4
C489
+VCCA_PEG_PLL
+V1.05M_A_SM
R96
C121
C134
C111
C96
220U/2.5V_3528
C147
C155
C146
R147
+VCCA_SM_CK
C153
C164
C170
C176
R406
+VCC_TVDACA_R
C447
C449
R407
R415
+VCC_HDA
C469
R414
+VCCD_TVDAC_R
+VCCD_QDAC_R
+V1.05M_MCH_PLL
C396
+VCCA_PEG_PLL
C495
R184
+VCCD_LVDS
C200
C204
R171
U21H
VCCA_CRT_DAC_1
VCCA_CRT_DAC_2
VCCA_DAC_BG
VSSA_DAC_BG
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_MPLL
VCCA_LVDS
VSSA_LVDS
VCCA_PEG_BG
VCCA_PEG_PLL
VCCA_SM_1
VCCA_SM_2
VCCA_SM_3
VCCA_SM_4
VCCA_SM_5
VCCA_SM_6
VCCA_SM_7
VCCA_SM_8
VCCA_SM_9
VCCA_SM_CK_1
VCCA_SM_CK_2
VCCA_SM_CK_3
VCCA_SM_CK_4
VCCA_SM_CK_5
VCCA_SM_CK_NCTF_1
VCCA_SM_CK_NCTF_2
VCCA_SM_CK_NCTF_3
VCCA_SM_CK_NCTF_4
VCCA_SM_CK_NCTF_5
VCCA_SM_CK_NCTF_6
VCCA_SM_CK_NCTF_7
VCCA_SM_CK_NCTF_8
VCCA_TV_DAC_1
VCCA_TV_DAC_2
VCC_HDA
VCCD_TVDAC
VCCD_QDAC
VCCD_HPLL
VCCD_PEG_PLL
VCCD_LVDS_1
VCCD_LVDS_2
CRT
PLL
LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
POWER
CANTIGA_1p0
VTT
AXF
SM CK
HV
PEG
DMI
VTTLF
VTT_1
VTT_2
VTT_3
VTT_4
VTT_5
VTT_6
VTT_7
VTT_8
VTT_9
VTT_10
VTT_11
VTT_12
VTT_13
VTT_14
VTT_15
VTT_16
VTT_17
VTT_18
VTT_19
VTT_20
VTT_21
VTT_22
VTT_23
VTT_24
VTT_25
VCC_AXF_1
VCC_AXF_2
VCC_AXF_3
VCC_SM_CK_1
VCC_SM_CK_2
VCC_SM_CK_3
VCC_SM_CK_4
VCC_HV_1
VCC_HV_2
VCC_HV_3
VCC_PEG_1
VCC_PEG_2
VCC_PEG_3
VCC_PEG_4
VCC_PEG_5
VCC_DMI_1
VCC_DMI_2
VCC_DMI_3
VCC_DMI_4
VTTLF1
VTTLF2
VTTLF3
+VTTLF1
+VTTLF2
+VTTLF3
C395
.47U/6.3V_4
C400
.47U/6.3V_4
C430
.47U/6.3V_4
852mA
+VCCP_GMCH
R81
C399
C387
2.2U/6.3V/X5R_6
C74
4.7U/6.3V_6
C392
4.7U/6.3V_6
C79
330U/2.5V_7343
+VCC_AXF
R403
C444
1U/6.3V/X5R_4
C442
10U/6.3V/X5R_8
+1.8V_SUS
+VCC_SM_CK
L21
1uH/300mA_8
1uH+-20%_300mA
R107
1/F_6
C158
10U/6.3V/X5R_8
C148
0.1U/16V/X7R_4
+VCC_SM_CK_L
C137
10U/6.3V/X5R_8
+VCC_TX_LVDS
L55
R426
E@0_4
C493
C491
C500
*I@1uH/300mA_8
*I@10U/6.3V/X5R_8
*I@1000P/50V/X7R_4
119.85mA
118.8mA
105.3mA
+3V_VCC_HV
C476
0.1U/16V/X7R_4
D23
CH501H-40PT
R417
10_4
R416
C477
0.1U/16V/X7R_4
1782mA
+VCC_PEG
Modify for C-TEST
R559
0_12
R560
456mA
C490
4.7U/6.3V_6
C509
220U/2.5V_7343
C499
10U/6.3V/X5R_8
C498
0.1U/16V/X7R_4
+VCC_RXR_DMI
EC C-7 /7 Del L56,L57 Add
R560,R559 1206 0 ohm.
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Quanta Computer Inc.
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Cantiga (POWER)
Rev 1A
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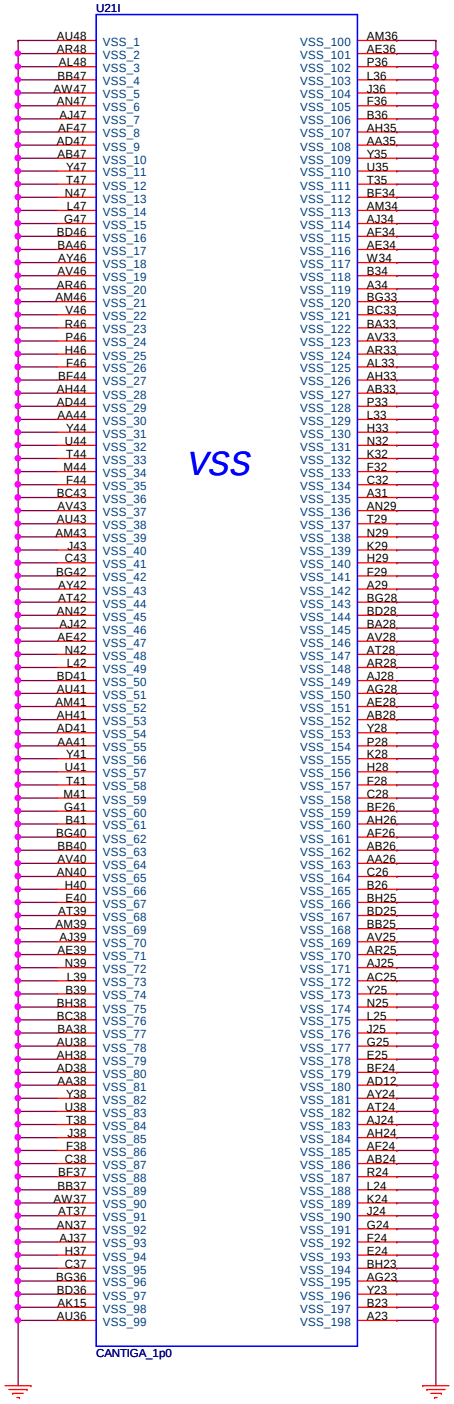

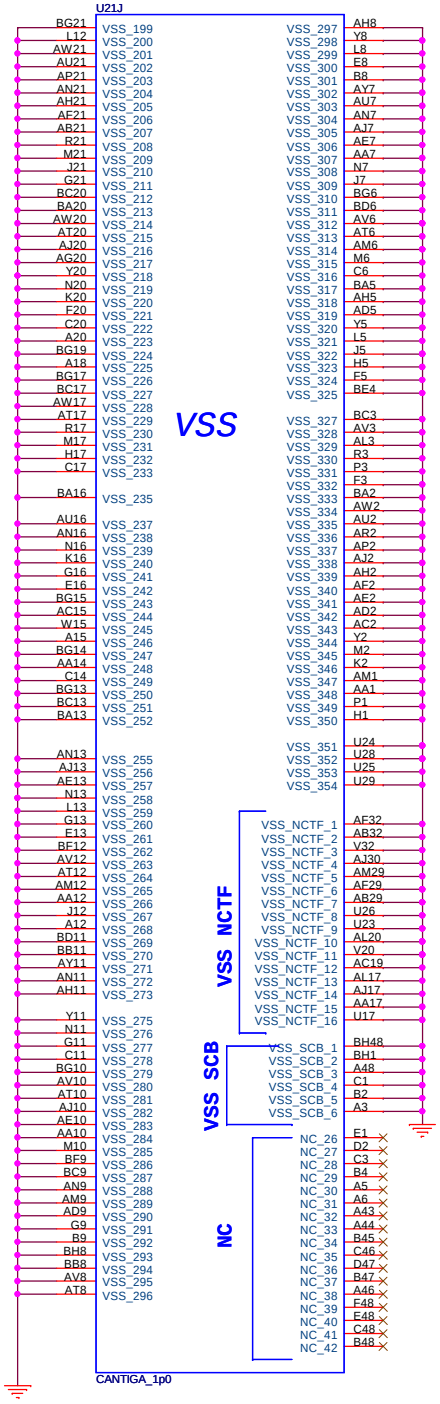

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DDR2 Dual channel A/B PU

12

DDRII A CHANNEL

+0.9V_DDR_VTT

Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.

C141 C136 C405 C408 C161 C448 C416 C87 C160 C109 C100 C112 C94

0.1U/16V/X7R_4

DDRII B CHANNEL

+0.9V_DDR_VTT

C90 C106 C131 C118 C154 C97 C83 C124 C89 C451 C86 C150 C133

0.1U/16V/X7R_4

+0.9V_DDR_VTT

+0.9V_DDR_VTT 33,36

8,13 DDR_A_MA[0..13]

DDR_B_MA[0..13] 8,13

DDR_A_MA11 / DDR_A_MA7	RP47	56X2	RP16	56X2	DDR_B_MA11 / DDR_B_MA7
DDR_A_MA6 / DDR_A_MA4	RP46	56X2	RP11	56X2	DDR_B_MA6 / DDR_B_MA2 (SWAP)
8,13 DDR_A_BS1 / 8,13 DDR_A_RAS#	RP44	56X2	RP5	56X2	DDR_B_BS1 8,13 / DDR_B_RAS# 8,13
7,13 M_ODT0 / DDR_A_MA13	RP43	56X2	RP2	56X2	DDR_B_MA13 / M_ODT2 7,13
8,13 DDR_A_BS2 / DDR_A_MA12	RP17	56X2	RP13	56X2	DDR_B_MA5 / DDR_B_MA8
DDR_A_MA9 / DDR_A_MA8	RP15	56X2	RP14	56X2	DDR_B_MA9 / DDR_B_MA12
DDR_A_MA5 / DDR_A_MA3	RP12	56X2	RP9	56X2	DDR_B_MA1 / DDR_B_MA3
8,13 DDR_A_BS0 / DDR_A_MA10	RP6	56X2	RP7	56X2	DDR_B_MA10 / DDR_B_BS0 8,13
8,13 DDR_A_WE# / 8,13 DDR_A_CAS#	RP4	56X2	RP3	56X2	DDR_B_WE# 8,13 / DDR_B_CAS# 8,13
DDR_A_MA2 / DDR_A_MA0	RP45	56X2	RP8	56X2	DDR_B_MA4 / DDR_B_MA0 (SWAP)

7,13 M_ODT1 / DDR_A_MA1	R97 / R102	56_4	R95 / R105 56_4 — M_ODT3 7,13 / DDR_B_BS2 8,13
7,13 DDR_CS0_DIMMA#	R396	56_4	R101 56_4 — DDR_CS2_DIMMB# 7,13
7,13 DDR_CS1_DIMMA#	R100	56_4	R98 56_4 — DDR_CS3_DIMMB# 7,13
7,13 DDR_CKE0_DIMMA	R123	56_4	R109 56_4 — DDR_CKE3_DIMMB 7,13
7,13 DDR_CKE1_DIMMA	R405	56_4	R126 56_4 — DDR_CKE4_DIMMB 7,13
8,13 DDR_A_MA14	R404	56_4	R125 56_4 — DDR_B_MA14 8,13

Please these resistor closely DIMMA,all trace length<750 mil.

Please these resistor closely DIMMB,all trace length<750 mil.

DDR2 Thermal Sensor SO-DIMM 0 & 1

Uninstall

+3.3V — 30 mil — +3.3V 2,5,7,8,10,13,14,15,16,17,18,19,20,21,22,23,24,26,27,30,31,32,33

R48 *220_6 — C42 *0.1U/16V/X7R_4

20 mil

U4 *LM86CIMM

2,13,26 CGCLK_SMB_M	8	SCLK	VCC 1 — LM86_3V
2,13,26 CGDAT_SMB_M	7	SDA	DXP 2 — DDR_THERMDA
7,13 PM_EXTTS#0	6	ALERT#	DXN 3 — DDR_THERMDC
7 PM_EXTTS#1 — R62 *0_4	4	OVERT#	GND 5

*MMBT3904 Q14

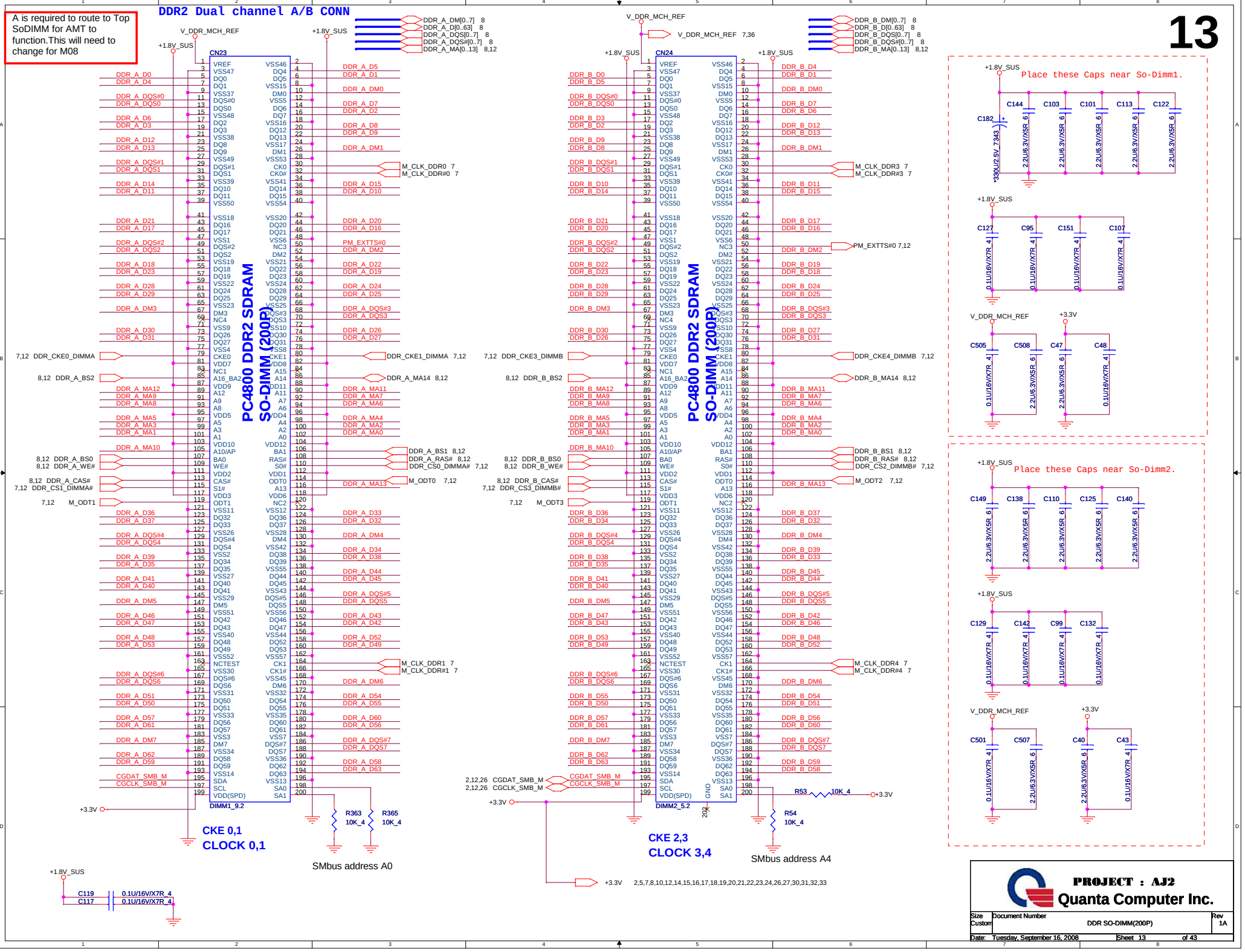
PROJECT : AJ2

Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR RES. ARRAY	1A
Date: Tuesday, September 16, 2008	Sheet 12	of 43

A is required to route to Top SoDIMM for AMT to function.This will need to change for M08

DDR2 Dual channel A/B CONN



RTC

AZ Interface(MDC, CODEC, HDMI)

AC-TX for SATA

SB Strap

ICH8-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

ICH8M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

XOR Chain Entrance Strap		
ICH TP3	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

Reserved for Intel Nineveh design.

Place all series terms close to ICH9 except for SDIN input lines,which should be close to source.Placement of R603, R600, R607 & R612 should equal distance to the T split trace point as R604, R599, R606 & R608 respective. Basically,keep the same distance from T for all series termination resistors.

Distance between the ICH-9 M and cap on the "P" signal should be identical distance between the ICH-9 M and cap on the "N" signal for same pair.

EMC reserved

Place within 500mils of ICH9 ball

ICH9M REV 1.0

PROJECT : AJ2

Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M (CPU,IDE,SATA,LPC,AC97,LAN)	1A
Date: Tuesday, September 16, 2008	Sheet 14	of 43

Place TX DC blocking caps close ICH8.

OC# pull up

RP49 10P8R-10K

USB_OC2#	6	5	USB_OC3#
OC9#	7	4	WLAN_RF_OFF#
USB_OC5#	8	3	USB_OC0#
USB_OC4#	9	2	OC#_NWC
+3.3V_SUS	10	1	

R234	2	1	10K_4 OC10#
R231	2	1	10K_4 OC11#
R238	2	1	10K_4 USB_OC7#
R237	2	1	10K_4 USB_OC1#

MiniCard-1 (WLAN) / MiniCard-2 / Express Card (NEWCARD)

26	PCIE_RX1-			N29 PERN1
26	PCIE_RX1+			N28 PERP1
26	PCIE_TX1-	C230	0.1U/16V/X7R_4 PCIE_TXN1_C	P27 PETN1
26	PCIE_TX1+	C233	0.1U/16V/X7R_4 PCIE_TXP1_C	P26 PETP1
26	PCIE_RX2-			L29 PERN2
26	PCIE_RX2+			L28 PERP2
26	PCIE_TX2-	C237	0.1U/16V/X7R_4 PCIE_TXN2_C	M27 PETN2
26	PCIE_TX2+	C242	0.1U/16V/X7R_4 PCIE_TXP2_C	M26 PETP2
32	PCIE_RXN3			J29 PERN3
32	PCIE_RXP3			J28 PERP3
32	PCIE_TXN3	C247	0.1U/16V/X7R_4 PCIE_TXN3_C	K27 PETN3
32	PCIE_TXP3	C262	0.1U/16V/X7R_4 PCIE_TXP3_C	K26 PETP3
		T12		G29 PERN4
		T12		G28 PERP4
		T12		H27 PETN4
		T56		H26 PETP4
		T13		E29 PERN5
		T13		E28 PERP5
		T12		F27 PETN5
		T62		F26 PETP5
21	PCIE_RX6-/GLAN_RX-			C29 PERN6/GLAN_RXN
21	PCIE_RX6+/GLAN_RX+	C268	0.1U/16V/X7R_4 GLAN_TXN_C	C28 PERP6/GLAN_RXP
21	PCIE_TX6-/GLAN_TX-	C267	0.1U/16V/X7R_4 GLAN_TXP_C	D27 PETN6/GLAN_TXN
21	PCIE_TX6+/GLAN_TX+			D26 PETP6/GLAN_TXP

U25D — PCI-Express / Direct Media Interface

DMI0RXN	V27	DMI_MTX_IRX_N0	7
DMI0RXP	V26	DMI_MTX_IRX_P0	7
DMI0TXN	U29	DMI_MRX_ITX_N0	7
DMI0TXP	U28	DMI_MRX_ITX_P0	7
DMI1RXN	Y27	DMI_MTX_IRX_N1	7
DMI1RXP	Y26	DMI_MTX_IRX_P1	7
DMI1TXN	W29	DMI_MRX_ITX_N1	7
DMI1TXP	W28	DMI_MRX_ITX_P1	7
DMI2RXN	AB27	DMI_MTX_IRX_N2	7
DMI2RXP	AB26	DMI_MTX_IRX_P2	7
DMI2TXN	AA29	DMI_MRX_ITX_N2	7
DMI2TXP	AA28	DMI_MRX_ITX_P2	7
DMI3RXN	AD27	DMI_MTX_IRX_N3	7
DMI3RXP	AD26	DMI_MTX_IRX_P3	7
DMI3TXN	AC29	DMI_MRX_ITX_N3	7
DMI3TXP	AC28	DMI_MRX_ITX_P3	7
DMI_CLKN	T26	CLK_PCIE_ICH#	2
DMI_CLKP	T25	CLK_PCIE_ICH	2
DMI_ZCOMP	AF29	R219 24.9/F_4	
DMI_IRCOMP	AF28	DMI_IRCOMP_R	2

Place within 500mils of ICH9

R219 24.9/F_4 — 1 — +1.5V_PCIE_ICH

SPI

20 mil

C256 *0.1U/16V/X7R_4 FAI Remove

C257 *0.1U/16V/X7R_4

U10 *MX25L512MC-12G

SPI_CLK_R			D23 SPI_CLK
SPI_CS#0_R			D24 SPI_CS0#
SPI_CS1#_R			F23 SPI_CS1#/GPIO58/CLGPIO6
SPI_MOSI_R			D25 SPI_MOSI
SPI_MISO_R			E23 SPI_MISO

U10 pin 1 SPI_CS#0 — R293 *22_4 — SPI_CS#0_R
U10 pin 6 SPI_CLK — R252 *22_4 — SPI_CLK_R
U10 pin 5 SPI_MOSI — R253 *22_4 — SPI_MOSI_R
U10 pin 2 SPI_MISO — R294 *22_4 — SPI_MISO_R
U10 pin 3 SPI_WP#
U10 pin 7 SPI_HOLD#
R251 *10K/F_4
R295 *10K/F_4

EC B-12 /15 Add U31 for HDCP support.

512K byte SPI ROM

USB

USB_OC0#	N4	OC0#/GPIO59	
USB_OC1#	N5	OC1#/GPIO40	
USB_OC2#	N6	OC2#/GPIO41	
USB_OC3#	P6	OC3#/GPIO42	
USB_OC4#	M1	OC4#/GPIO43	
USB_OC5#	N2	OC5#/GPIO29	
WLAN_RF_OFF#	M4	OC6#/GPIO30	
USB_OC7#	M3	OC7#/GPIO31	
OC#_NWC	N3	OC8#/GPIO44	
OC9#	N1	OC9#/GPIO45	
OC10#	P5	OC10#/GPIO46	
OC11#	P3	OC11#/GPIO47	
R464 22.6/F			AG2 USBRBIAS
USB_RBIAS_PN	1		AG1 USBRBIAS#

28 USB_OC1#
28 USB_OC2#
26,31 WLAN_RF_OFF#
32 OC#_NWC

placed within 500-mils of the ICH9M

ICH9M REV 1.0

USBP0N	AC5	USBP0-	28
USBP0P	AC4	USBP0+	28
USBP1N	AD3	USBP1-	28
USBP1P	AD2	USBP1+	28
USBP2N	AC1	USBP2-	28
USBP2P	AC2	USBP2+	28
USBP3N	AA5	USBP3-	32
USBP3P	AA4	USBP3+	32
USBP4N	AB2	USBP4-	26
USBP4P	AB3	USBP4+	26
USBP5N	AA1	USBP5-	28
USBP5P	AA2	USBP5+	28
USBP6N	W5	USBP6-	T49
USBP6P	W4	USBP6+	T51
USBP7N	Y3	USBP7-	26
USBP7P	Y2	USBP7+	26
USBP8N	W1	USBP8-	18
USBP8P	W2	USBP8+	18
USBP9N	V2	USBP9-	29
USBP9P	V3	USBP9+	29
USBP10N	U5	ICH_USBP10-	T54
USBP10P	U4	ICH_USBP10+	T53
USBP11N	U1	ICH_USBP11-	T122
USBP11P	U2	ICH_USBP11+	T123

- USB-0
- USB-1
- TO Board USB-0
- NEWCARD
- MiniCard-1 (WLAN)
- TO Board USB-1
- MiniCard-2(reserved)
- WEB CAM
- BLUETOOTH

PCI Pullups

+3.3V_S5	R492 2	1	10K_4 PCI_PME#
+3.3V	R269		8.2K_4 PCI_FRAME#

RP34 10P8R-8.2K

PCI_IRDY#	6	5	PCI_PERR#
PCI_PLOCK#	7	4	PCI_PIRQD#
PCI_TRDY#	8	3	PCI_STOP#
PCI_PIRQC#	9	2	PCI_DEVSEL#
+3.3V	10	1	

RP50 10P8R-8.2K

ICH_GPIO3_PIRQF#	6	5	PCI_PIRQB#
ICH_GPIO2_PIRQE#	7	4	ICH_GPIO4_PIRQG#
PCI_PIRQA#	8	3	PCI_REQ0#
PCI_SERR#	9	2	ICH_GPIO5_PIRQH#
+3.3V	10	1	

PCI

U25B

AD0	D11	REQ0#	F1 PCI_REQ0#
AD1	C8	GNT0#	G4 PCI_GNT0#
AD2	D9	REQ1#/GPIO50	B6 BOARD_ID1
AD3	E12	GNT1#/GPIO51	A7 PCI_GNT1#
AD4	E9	REQ2#/GPIO52	F13 BOARD_ID2
AD5	C9	GNT2#/GPIO53	E12 PCI_GNT2#
AD6	E10	REQ3#/GPIO54	E6 BOARD_ID3
AD7	B7	GNT3#/GPIO55	F6 PCI_GNT3#
AD8	C7		
AD9	C5	C/BE0#	D8 C/BE0#
AD10	G11	C/BE1#	B4 C/BE1#
AD11	F8	C/BE2#	D6 C/BE2#
AD12	F11	C/BE3#	A5 C/BE3#
AD13	E7		
AD14	A3	IRDY#	D3 PCI_IRDY#
AD15	D2	PAR	E3 PCI_PAR
AD16	F10	PCIRST#	R1
AD17	D5	DEVSEL#	C6 PCI_DEVSEL#
AD18	D10	PERR#	E4 PCI_PERR#
AD19	B3	PLOCK#	C2 PCI_PLOCK#
AD20	F7	SERR#	J4 PCI_SERR#
AD21	C3	STOP#	A4 PCI_STOP#
AD22	E3	TRDY#	F5 PCI_TRDY#
AD23	E4	FRAME#	D7 PCI_FRAME#
AD24	C1		
AD25	G7	PLTRST#	C14 PLTRST#_NB
AD26	H7	PCICLK	D4 CLK_PCI_ICH
AD27	D1	PME#	R2 PCI_PME#
AD28	G5		
AD29	H6		
AD30	G1		
AD31	H3		

PCI_REQ0# 23 — PCI_GNT0# 23 — BOARD_ID1 16 — T139 — BOARD_ID2 16 — T61 — BOARD_ID3 16

C/BE0# 23 — C/BE1# 23 — C/BE2# 23 — C/BE3# 23

PCI_IRDY# 23 — PCI_PAR 23 — PCIRST# 20,23 — PCI_DEVSEL# 23

PCI_STOP# 23 — PCI_TRDY# 23 — PCI_FRAME# 23

CLK_PCI_ICH 2 — PCI_PME# 23

23 AD[0..31]

Interrupt I/F

PIRQA#	J5	PIRQE#/GPIO2	H4 ICH_GPIO2_PIRQE#
PIRQB#	E1	PIRQF#/GPIO3	K6 ICH_GPIO3_PIRQF#
PIRQC#	J6	PIRQG#/GPIO4	F2 ICH_GPIO4_PIRQG#
PIRQD#	C4	PIRQH#/GPIO5	G2 ICH_GPIO5_PIRQH#

23 PCI_PIRQA#
T131
T57
T79

T77
T71
T129
T125

ICH9M REV 1.0

Reserved for EMI. Place resister and cap close to ICH.

CLK_PCI_ICH — R273 *10_4 — C275 *10P/50V/COG_4

PLTRST#_NB 7

+3.3V_SUS — C288 0.1U/16V/X7R_4 — U11 TC7SH08FU(F) — PLTRST# 7,21,22,26,32 — R299 100K_4

Boot BIOS Strap

SPI_CS1#_R — R259 *1K_4
PCI_GNT0# — R260 *1K_4

		GNT0#	SPI_CS1#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

PCI_GNT3# — R258 *1K_4

A16 away override strap.

Low = A16 swap override enabled.
High = Default.

PROJECT : AJ2

Quanta Computer Inc.

Size	Document Number	Rev
A3	ICH9-M (USB,DMI,PCIE,PCI)	1A
Date: Tuesday, September 16, 2008	Sheet 15	of 43

Non-iAMT ASF 2.0

Option to " Disable " clkrun. Pulling it down will keep the clks running.

Place these close to ICH8.

LCD_ID

Board ID	ID3	ID2	ID1	ID0
INTEL SENTAROSA	1	1	1	1
INTEL MENTAVIRA	1	1	0	0
AMD	1	0	1	1
NVIDIA	1	0	0	1

Modify for FAI

GPIO[20]--Integrated Pull-Down 20K.

Modify for FAI

No Reboot strap.	
ACZ_SPKR	Low = Default. High = No Reboot.

Non-iAMT
For ME

PROJECT : AJ2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M (PM,GPIO,SMB,CL)	1A
Date: Tuesday, September 16, 2008	Sheet 16	of 43

EC A-04/01 chamge C479,C493 to 10, R448,R417 to 100 ohm for USB 1.0 can't work and meet Intel Spec.

FB_330ohm+-25%_100mHz_ 1.5A_0.09 ohm DC

1uH+-20%_800mA

10uH+-20%_100mA

Modify for C-TEST

EC C-7 /8 only UMA Stuff.

Vout=1.25(1+R1/R2)

Impact ICH9M VCCHDA and VCCSUSHDA supply 1.5V/3.3V

Support INT HDMI HDA interface. These power only support 1.5V.Device must to meet.

NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

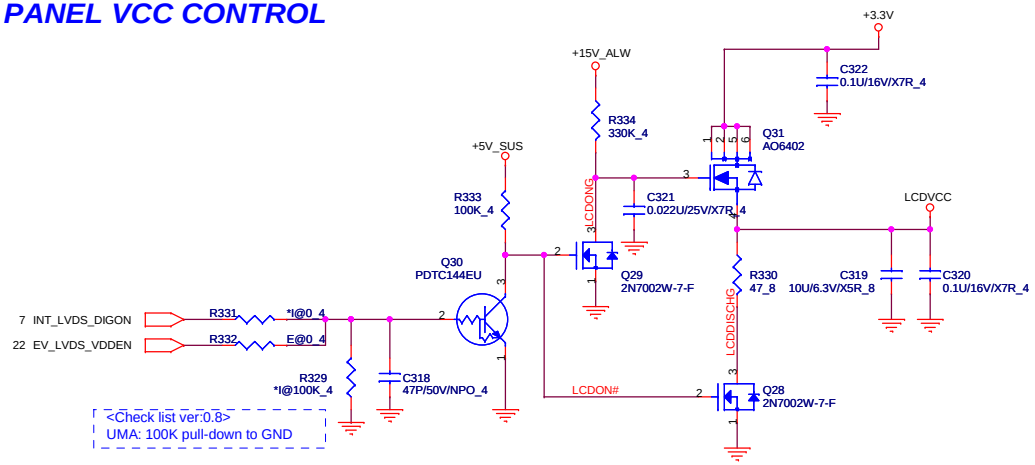
WWAN Noise - ICH improvements

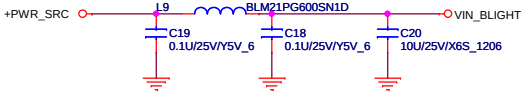
PROJECT : AJ2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M (POWER,GND)	1A
Date: Tuesday, September 16, 2008	Sheet 17	of 43

WEB CAM(Include BACKLIGHT function)

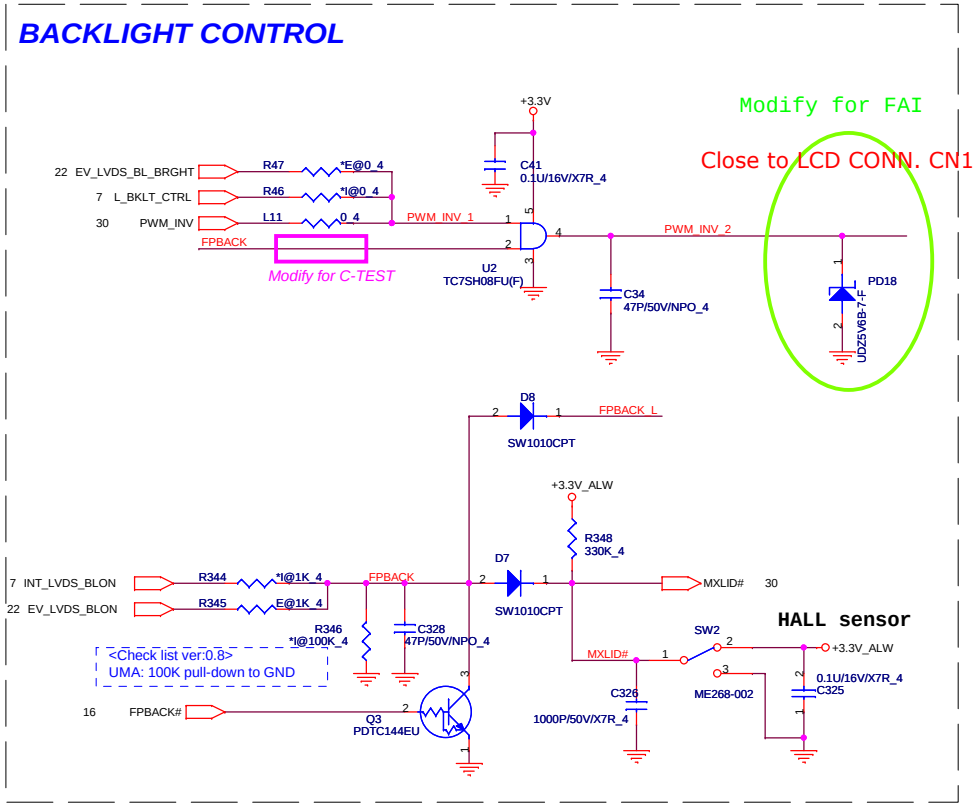
PANEL VCC CONTROL



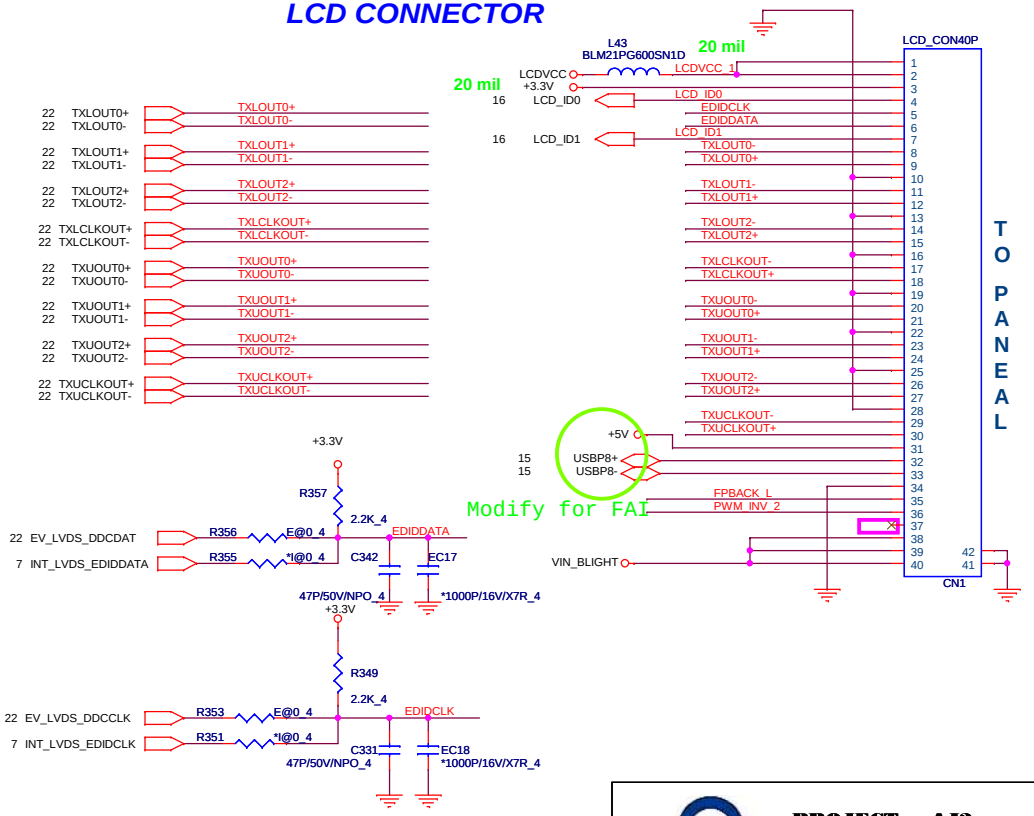


	Single LVDS 1366*768	Dial LVDS 1920*1080
LCD_ID0	TBD	TBD
LCD_ID1	HIGH	LOW

BACKLIGHT CONTROL



LCD CONNECTOR



Quanta Computer Inc.

PROJECT : AJ2

Size	Document Number	Rev
Custom	LVDS/LCD CONN/LID/WEB CAM	1A
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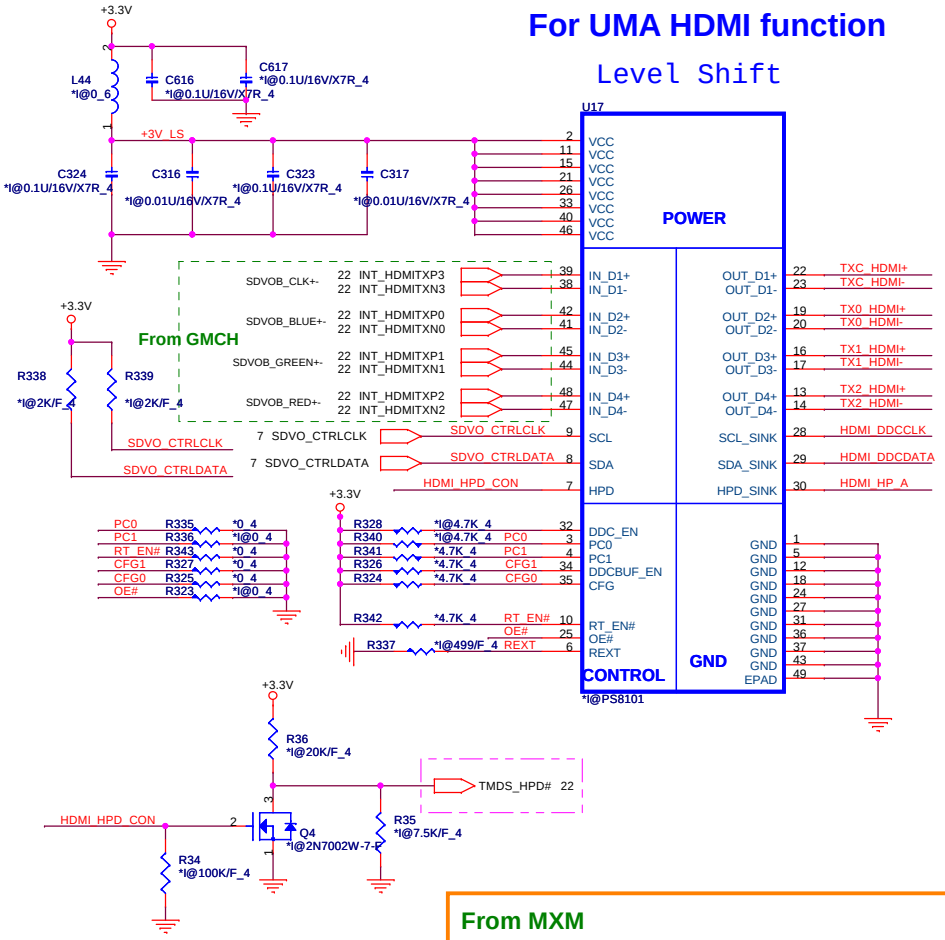
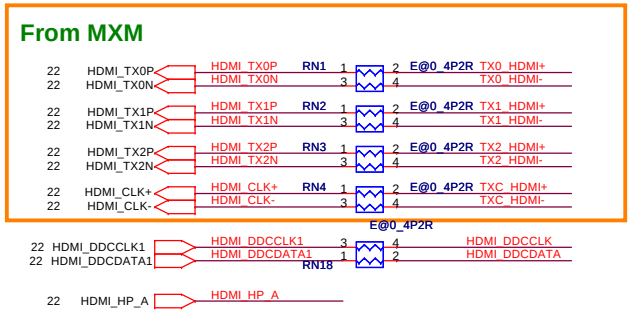
For UMA HDMI function

Level Shift



From MXM

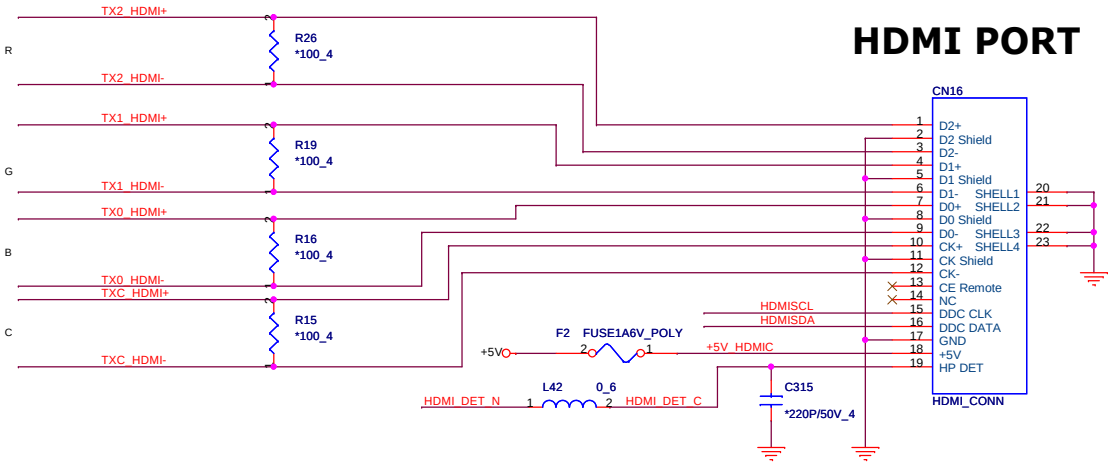


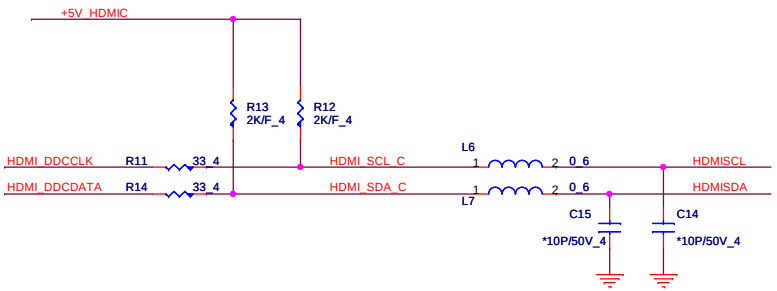
MXM DOES NOT NEED LEVEL SHIFT.
BYPASS PATH RESISTERS.

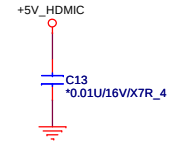
EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

SCLZ/SDAZ Low-level input/output Voltage
CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF1:CGF0=0:1 VIL:<0.36V VOL:0.55V
CGF1:CGF0=1:0 VIL:<0.44V VOL:0.65V
CGF1:CGF0=1:1 VIL:<0.36V VOL:0.6V

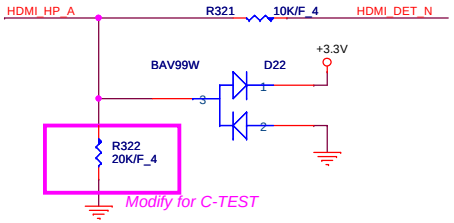
HDMI PORT







for EMI request



Modify for C-TEST

PROJECT : AJ2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDMI	1A
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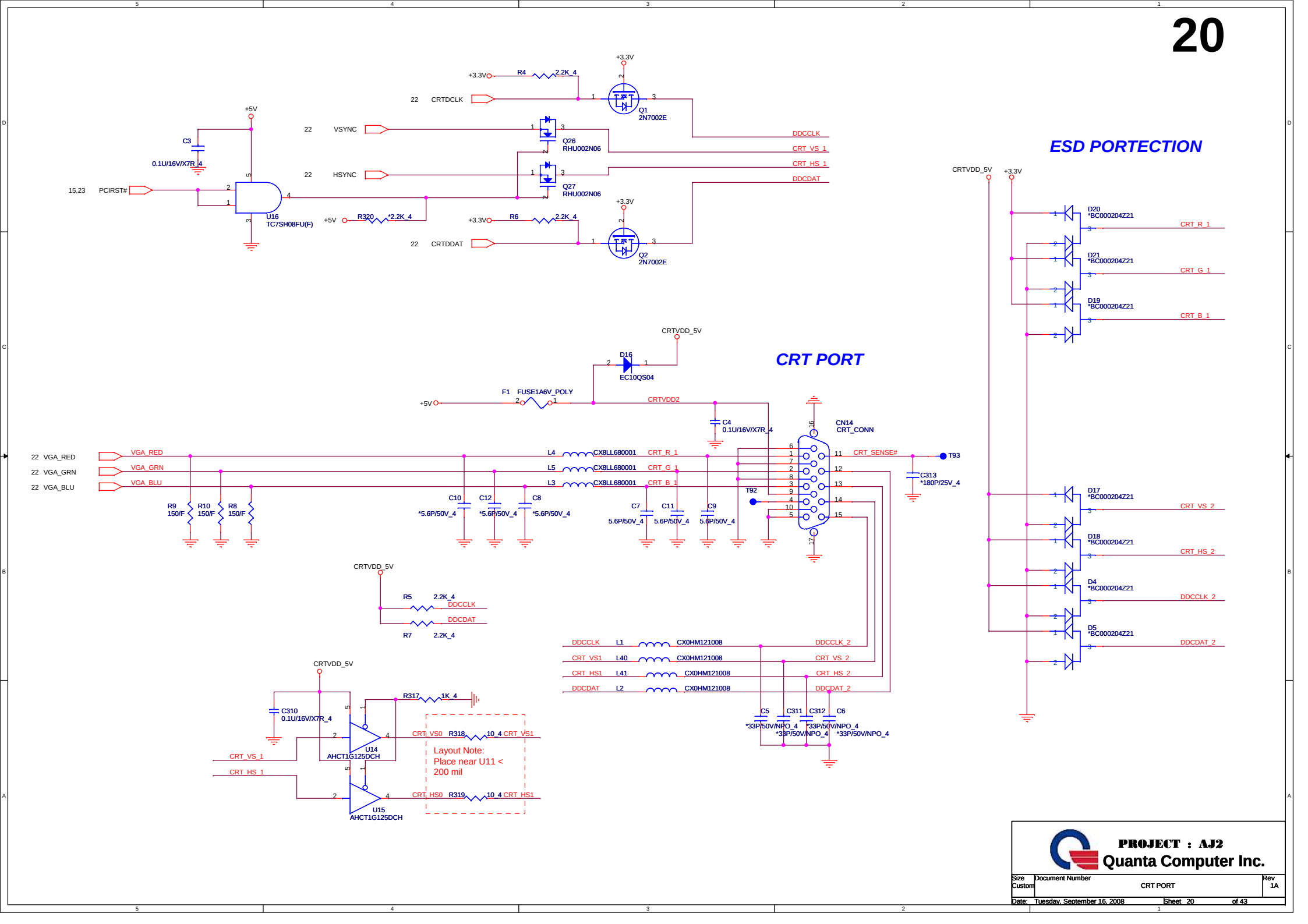

PROJECT : AJ2			
Quanta Computer Inc.			
Size: Custom	Document Number: CRT PORT		Rev: 1A
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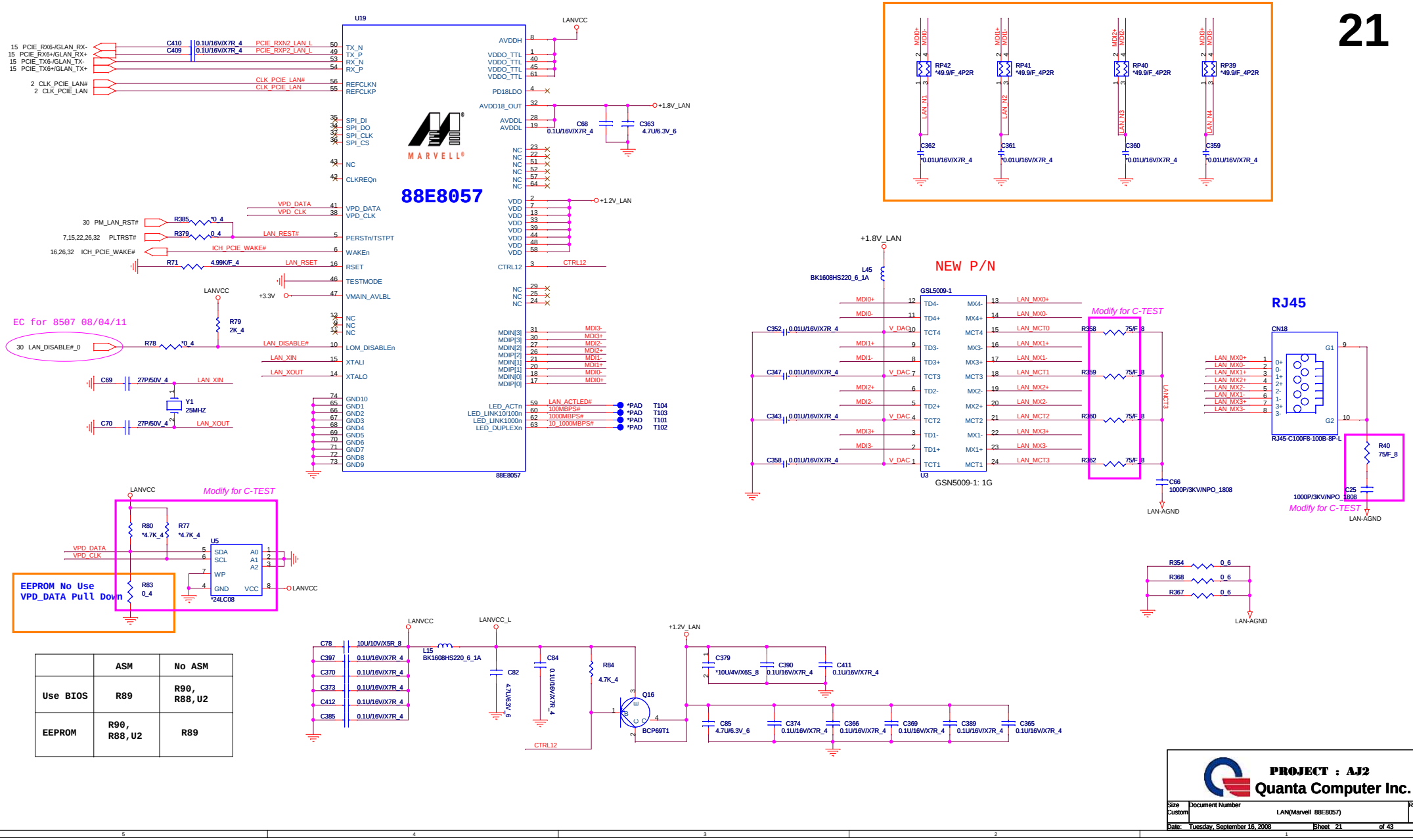

	ASM	No ASM
Use BIOS	R89	R90, R88,U2
EEPROM	R90, R88,U2	R89

PROJECT : AJ2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN(Marvell 88E8057)	1A
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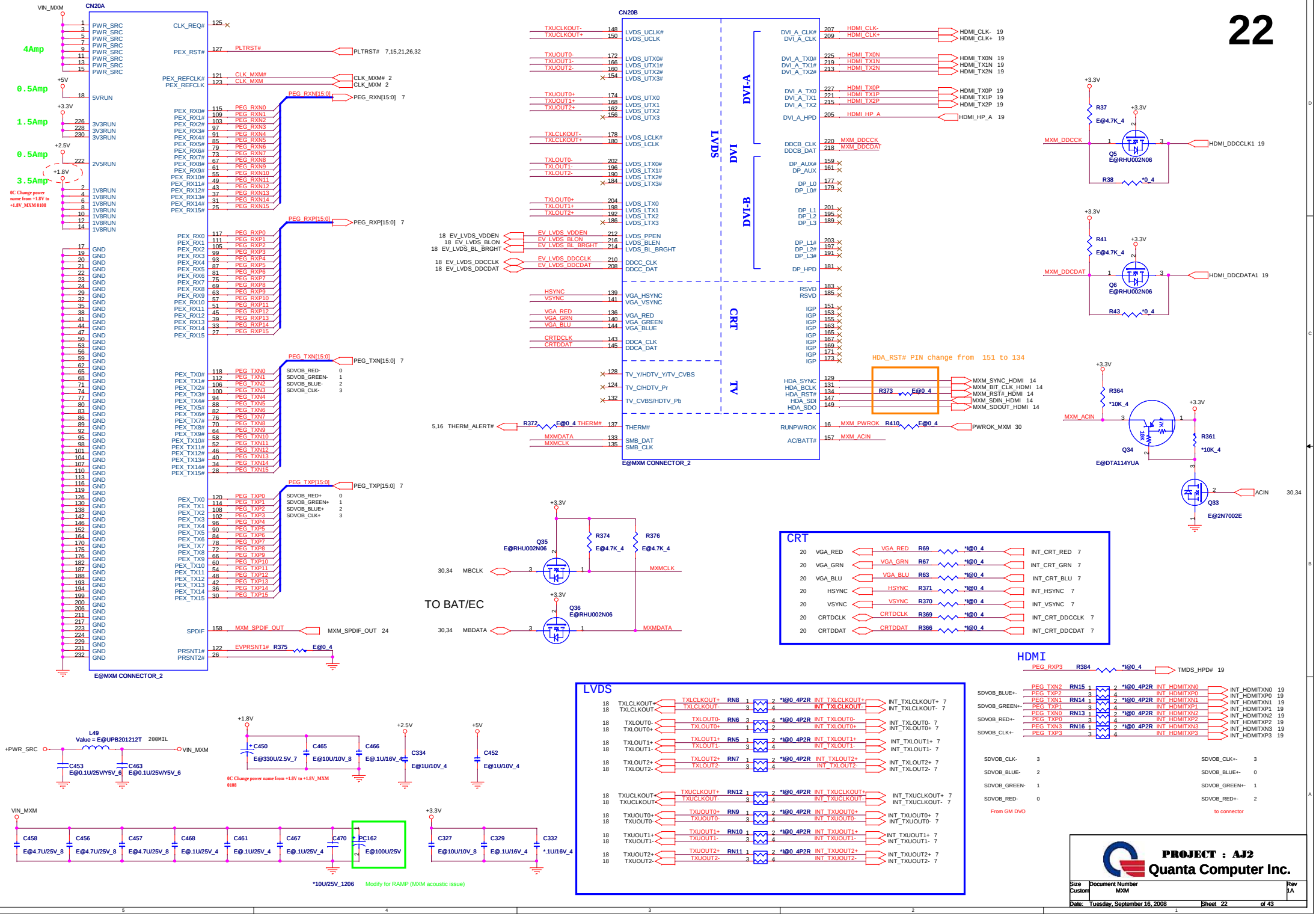
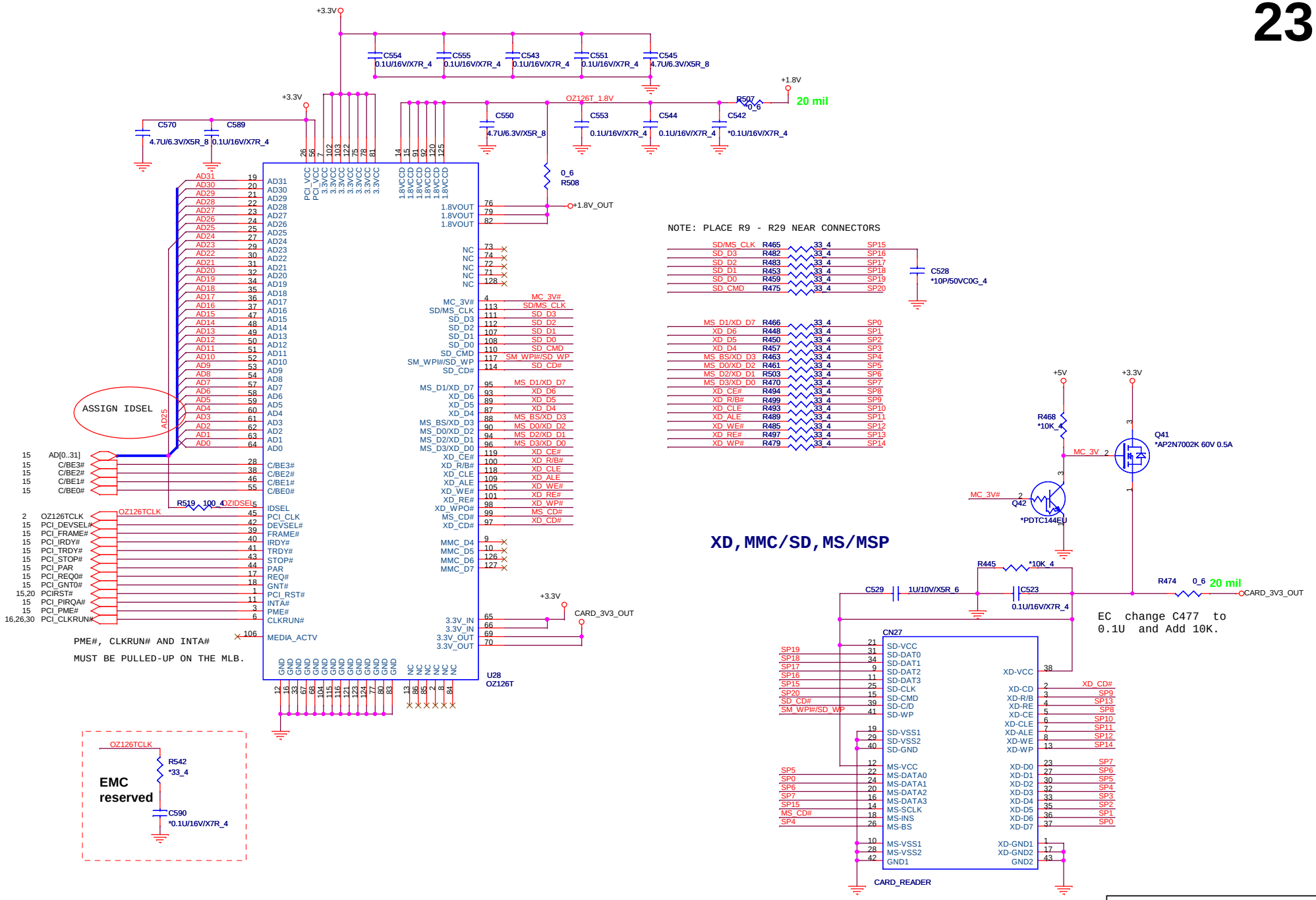
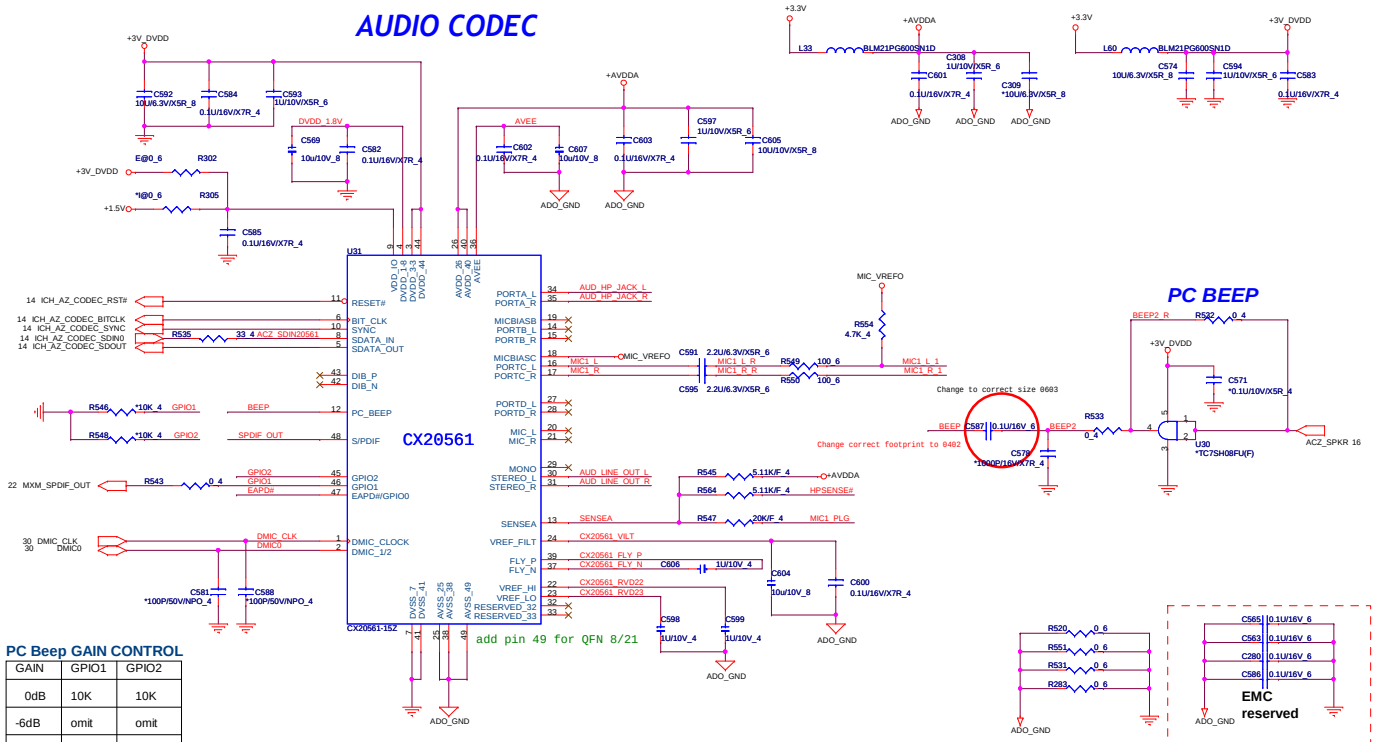

CN20A
VIN_MXM
4Amp
0.5Amp
1.5Amp
0.5Amp
3.5Amp
+5V
+3.3V
+2.5V
+1.8V
5VRUN
3V3RUN
2V5RUN
1V8RUN
GND
PWR_SRC
CLK_REQ#
PEX_RST#
PLTRST#
PEX_REFCLK#
PEX_REFCLK
CLK_MXM#
CLK_MXM
PEG_RXN[15:0]
PEG_RXP[15:0]
PEG_TXN[15:0]
PEG_TXP[15:0]
SDVOB_RED-
SDVOB_GREEN-
SDVOB_BLUE-
SDVOB_CLK-
SDVOB_RED+
SDVOB_GREEN+
SDVOB_BLUE+
SDVOB_CLK+
SPDIF
MXM_SPDIF_OUT
EVPRSNT1#
R375
E@0_4
PRSNT1#
PRSNT2#
0C Change power name from +1.8V to +1.8V_MXM 0108
E@MXM CONNECTOR_2
CN20B
LVDS_UCLK#
LVDS_UCLK
LVDS_UTX0#
LVDS_UTX1#
LVDS_UTX2#
LVDS_UTX3#
LVDS_UTX0
LVDS_UTX1
LVDS_UTX2
LVDS_UTX3
LVDS_LCLK#
LVDS_LCLK
LVDS_LTX0#
LVDS_LTX1#
LVDS_LTX2#
LVDS_LTX3#
LVDS_LTX0
LVDS_LTX1
LVDS_LTX2
LVDS_LTX3
LVDS_PPEN
LVDS_BLEN
LVDS_BL_BRGHT
DDCC_CLK
DDCC_DAT
VGA_HSYNC
VGA_VSYNC
VGA_RED
VGA_GREEN
VGA_BLUE
DDCA_CLK
DDCA_DAT
TV_Y/HDTV_Y/TV_CVBS
TV_C/HDTV_Pr
TV_CVBS/HDTV_Pb
THERM#
SMB_DAT
SMB_CLK
LVDS
DVI
DVI-A
DVI-B
CRT
TV
DVI_A_CLK#
DVI_A_CLK
DVI_A_TX0#
DVI_A_TX1#
DVI_A_TX2#
DVI_A_TX0
DVI_A_TX1
DVI_A_TX2
DVI_A_HPD
DDCB_CLK
DDCB_DAT
DP_AUX#
DP_AUX
DP_L0
DP_L0#
DP_L1
DP_L2
DP_L3
DP_L1#
DP_L2#
DP_L3#
DP_HPD
RSVD
IGP
HDA_SYNC
HDA_BCLK
HDA_RST#
HDA_SDI
HDA_SDO
RUNPWROK
AC/BATT#
HDMI_CLK-
HDMI_CLK+
HDMI_TX0N
HDMI_TX1N
HDMI_TX2N
HDMI_TX0P
HDMI_TX1P
HDMI_TX2P
HDMI_HP_A
MXM_DDCCK
MXM_DDCDAT
HDA_RST# PIN change from 151 to 134
R373
MXM_SYNC_HDMI
MXM_BIT_CLK_HDMI
MXM_RST#_HDMI
MXM_SDIN_HDMI
MXM_SDOUT_HDMI
MXM_PWROK
R410
PWROK_MXM
MXM_ACIN
E@MXM CONNECTOR_2
TO BAT/EC
Q35
Q36
E@RHU002N06
R374
R376
E@4.7K_4
MBCLK
MBDATA
MXMCLK
MXMDATA
R37
R38
R41
R43
Q5
Q6
E@RHU002N06
*0_4
HDMI_DDCCLK1
HDMI_DDCDATA1
R364
R361
*10K_4
Q34
E@DTA114YUA
Q33
E@2N7002E
ACIN
CRT
VGA_RED
VGA_GRN
VGA_BLU
HSYNC
VSYNC
CRTDCLK
CRTDDAT
R69
R67
R63
R371
R370
R369
R366
*I@0_4
INT_CRT_RED
INT_CRT_GRN
INT_CRT_BLU
INT_HSYNC
INT_VSYNC
INT_CRT_DDCCLK
INT_CRT_DDCDAT
HDMI
R384
TMDS_HPD#
LVDS
RN8
RN6
RN5
RN7
RN12
RN9
RN10
RN11
*I@0_4P2R
INT_TXLCLKOUT+
INT_TXLCLKOUT-
INT_TXLOUT0+
INT_TXLOUT0-
INT_TXLOUT1+
INT_TXLOUT1-
INT_TXLOUT2+
INT_TXLOUT2-
INT_TXUCLKOUT+
INT_TXUCLKOUT-
INT_TXUOUT0+
INT_TXUOUT0-
INT_TXUOUT1+
INT_TXUOUT1-
INT_TXUOUT2+
INT_TXUOUT2-
RN15
RN14
RN13
RN16
INT_HDMITXN0
INT_HDMITXP0
INT_HDMITXN1
INT_HDMITXP1
INT_HDMITXN2
INT_HDMITXP2
INT_HDMITXN3
INT_HDMITXP3
From GM DVO
to connector
L49
Value = E@UPB201212T
200MIL
+PWR_SRC
VIN_MXM
C453
C463
E@0.1U/25V/Y5V_6
C450
C465
C466
C334
C452
E@330U/2.5V_7
E@10U/10V_8
E@.1U/16V_4
E@1U/10V_4
0C Change power name from +1.8V to +1.8V_MXM 0108
C458
C456
C457
C468
C461
C467
C470
C462
C327
C329
C332
E@4.7U/25V_8
E@.1U/25V_4
E@100U/25V
*.1U/16V_4
*10U/25V_1206
Modify for RAMP (MXM acoustic issue)
PROJECT : AJ2
Quanta Computer Inc.
Size
Custom
Document Number
MXM
Rev
1A
Date: Tuesday, September 16, 2008
Sheet 22
of 43



PROJECT : AJ2		
Quanta Computer Inc.		
Size: Custom	Document Number: OZ126T(CARD READER)	Rev: 1A
Date: Tuesday, September 16, 2008	Sheet 23 of 43	

AUDIO CODEC

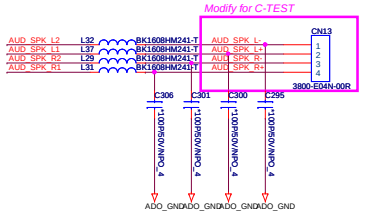


PC Beep GAIN CONTROL

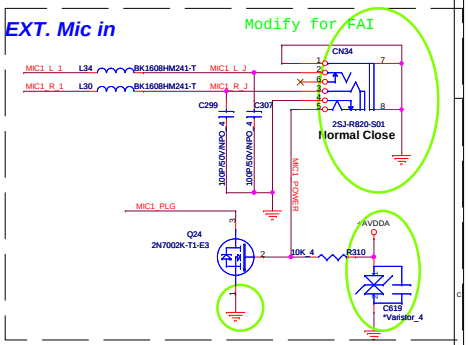
GAIN	GPIO1	GPIO2
0dB	10K	10K
-6dB	omit	omit
-12dB	10K	omit
-18dB	omit	10K

PC BEEP

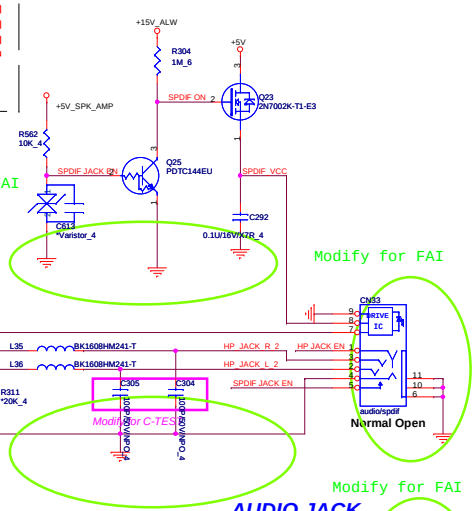
Int. Stereo Speakers



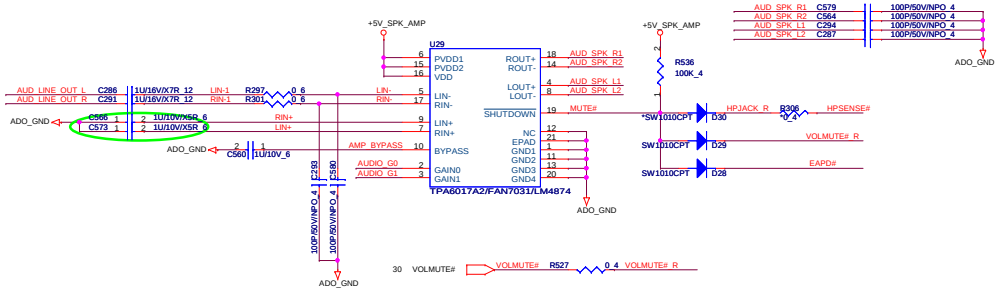
EXT. Mic in



Headphone out + Spdif Out

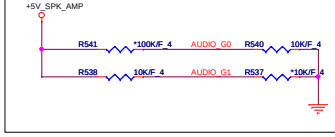


AUDIO AMPLIFIER

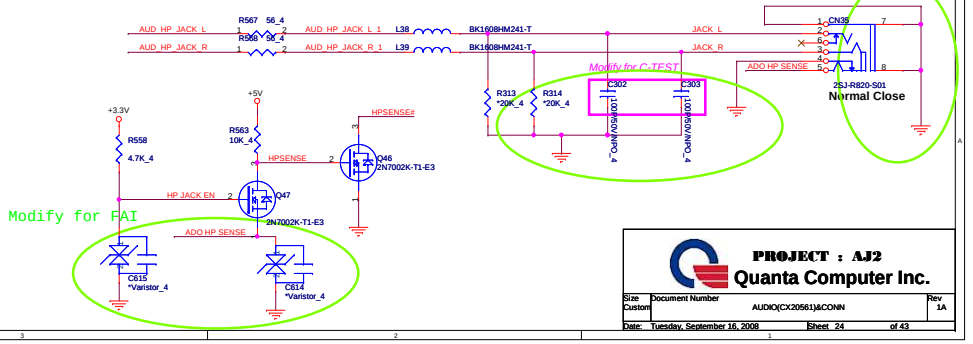


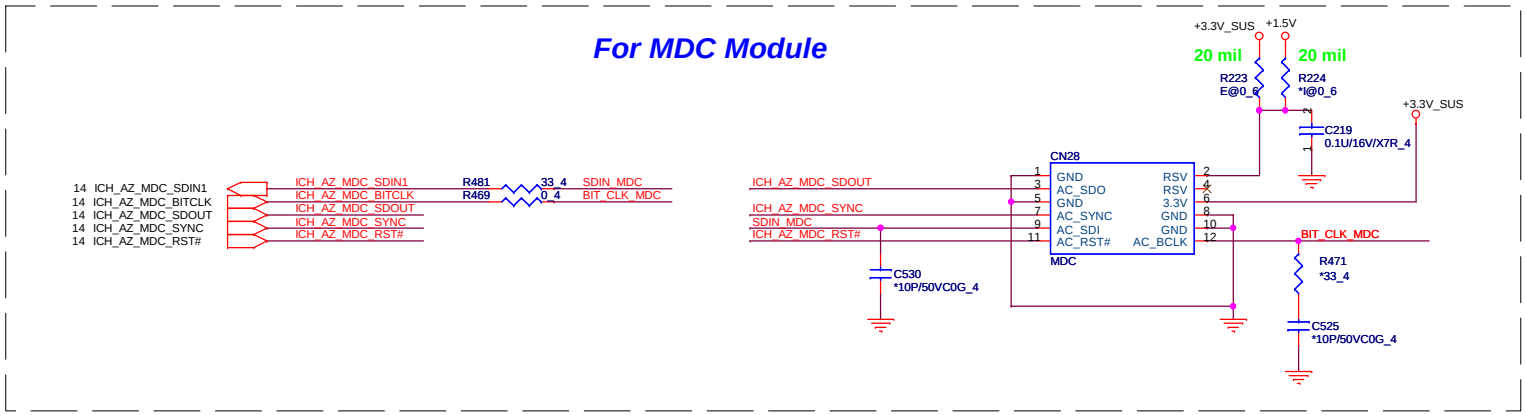
6017A2 Gain Table

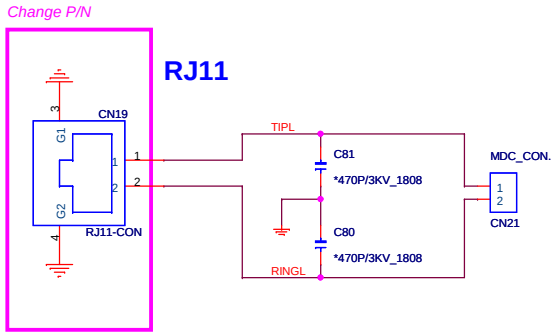
GAIN0	GAIN1	AV(INV)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



AUDIO JACK



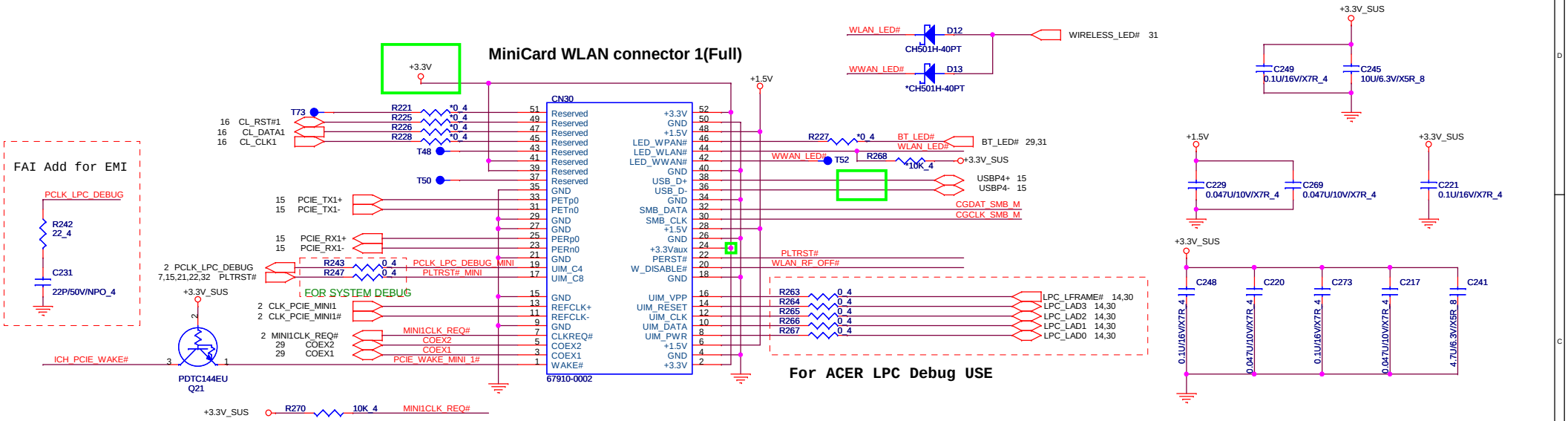




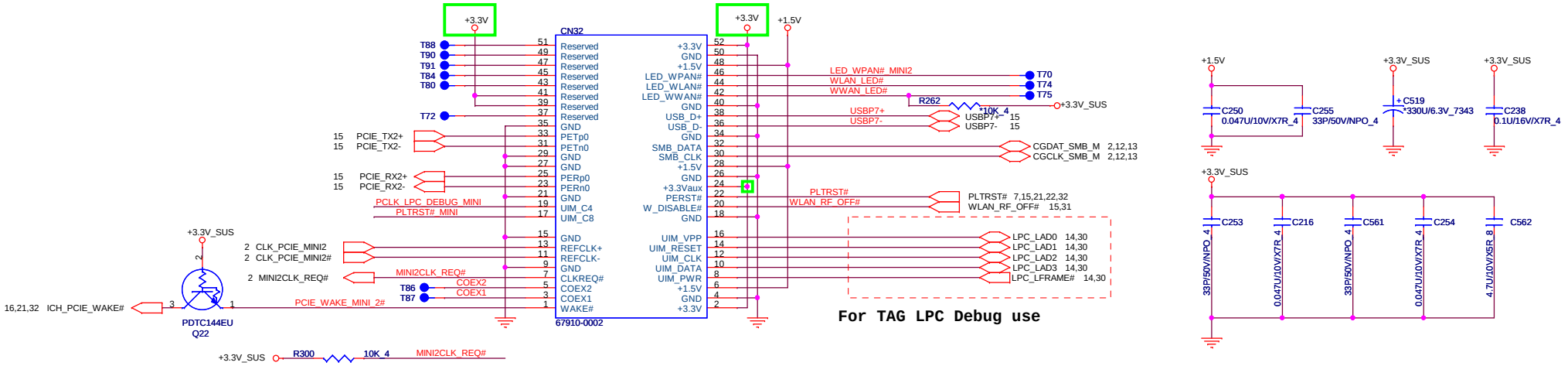
PROJECT : AJ2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MODEM(MDC)/RJ11 BOARD	1A
Date: Tuesday, September 16, 2008	Sheet 25 of 43	

MiniCard WLAN connector 1(Full)

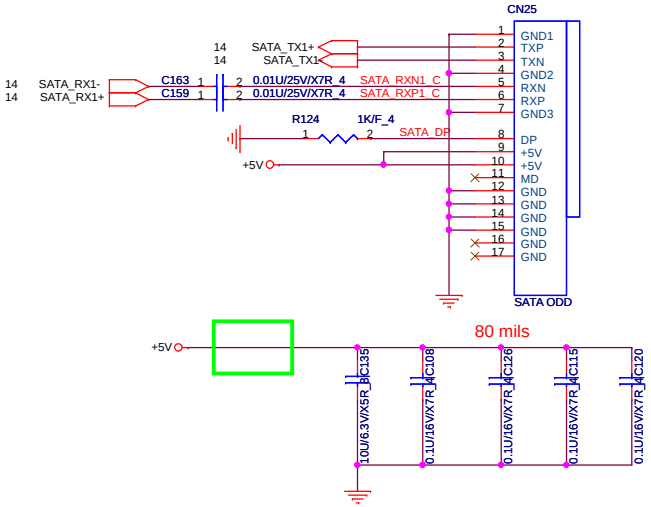


MiniCard connector 2 (half)

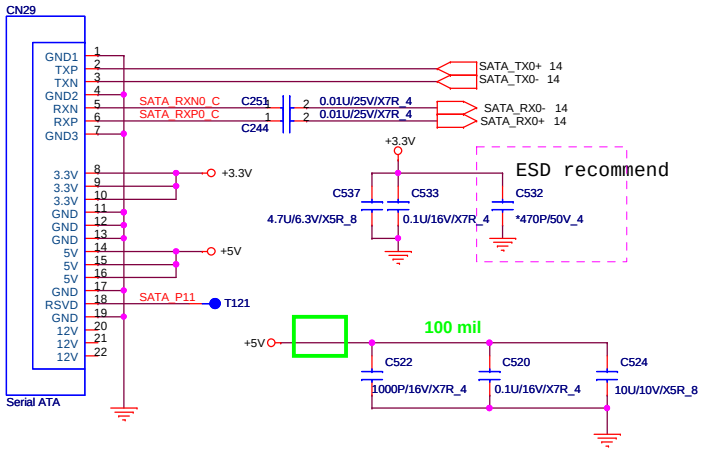


PROJECT : AJ2			
Quanta Computer Inc.			
Size: Custom	Document Number: MINI PCI-E Card		Rev: 1A
Date: Tuesday, September 16, 2008		Sheet 26	of 43

SATA CD-ROM



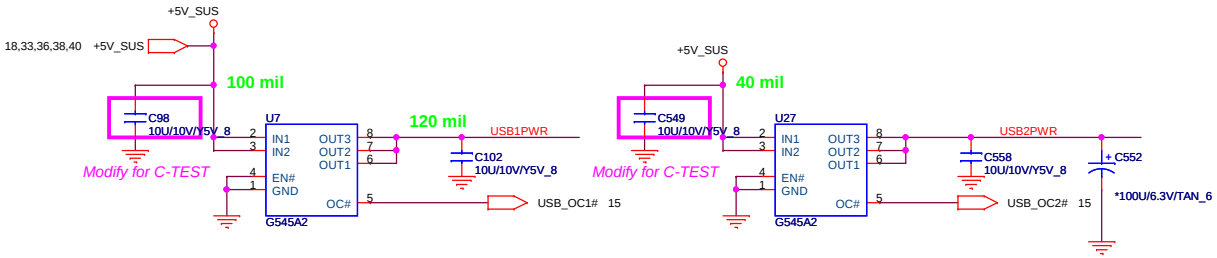
SATA CONNECTOR

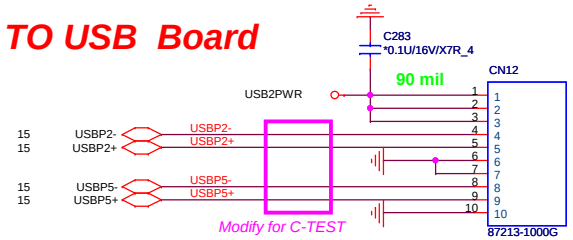


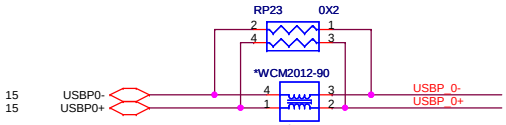
PROJECT : AJ2

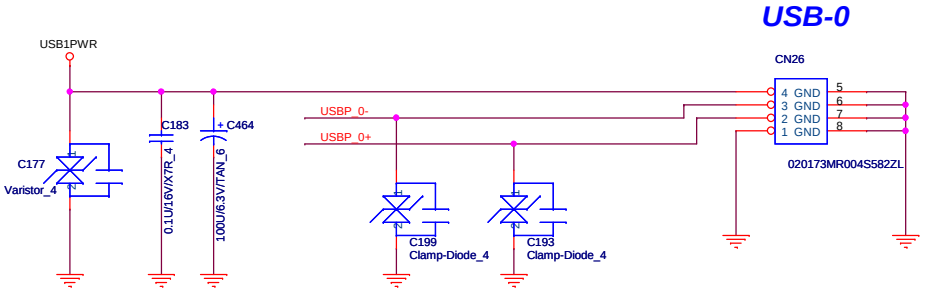
Quanta Computer Inc.

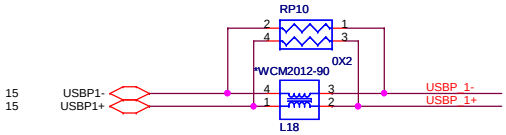
Size	Document Number	Rev
Custom	SATA HDD ODD	1A
Date: Tuesday, September 16, 2008	Sheet 27	of 43

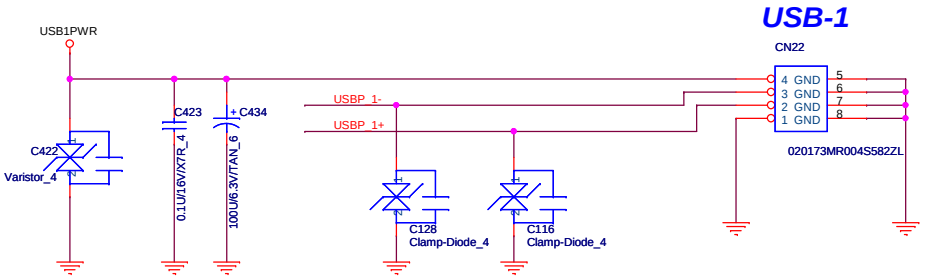












PROJECT : AJ2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB CONN	1A

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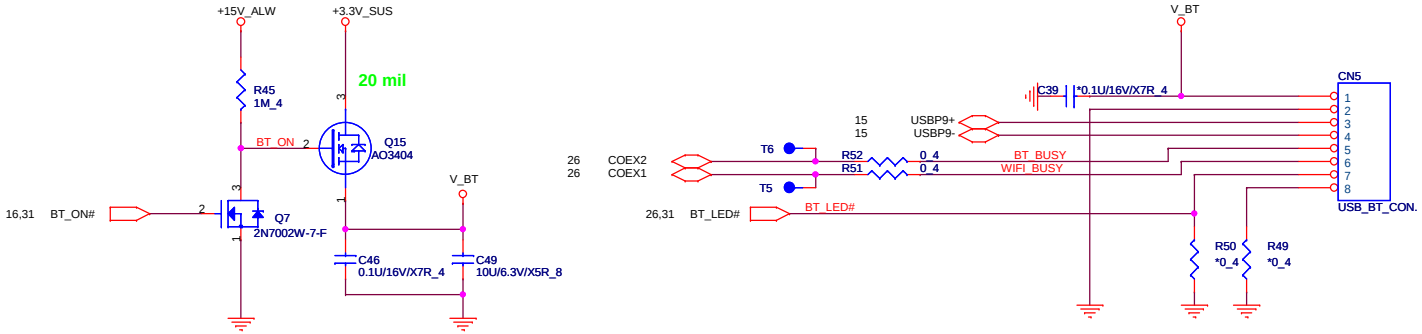
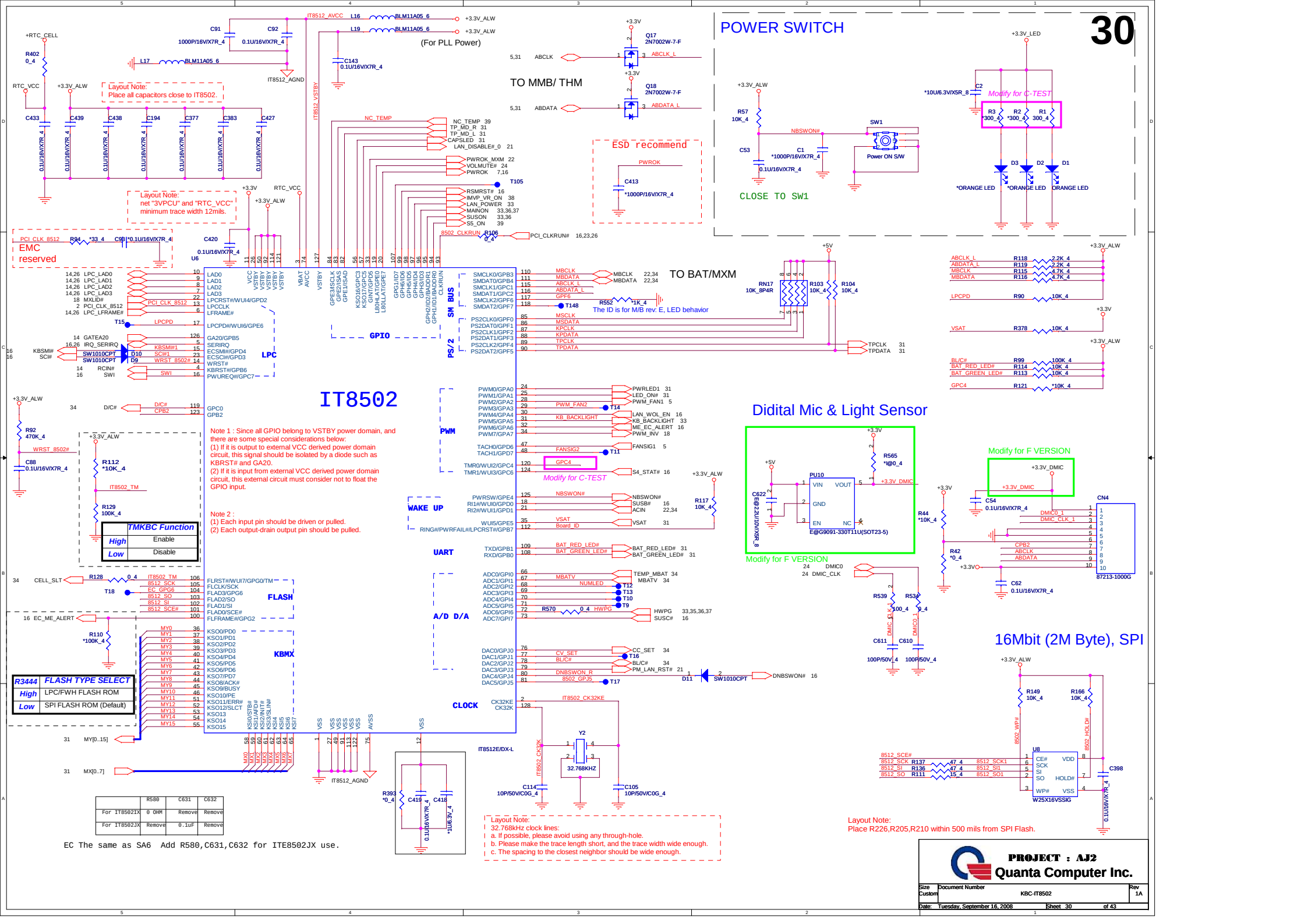
BLUETOOTH CONNECTOR



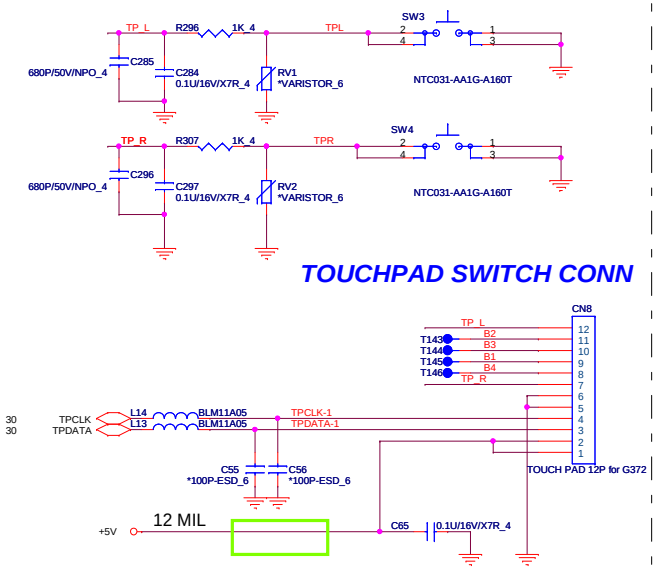
PROJECT : AJ2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BT	1A

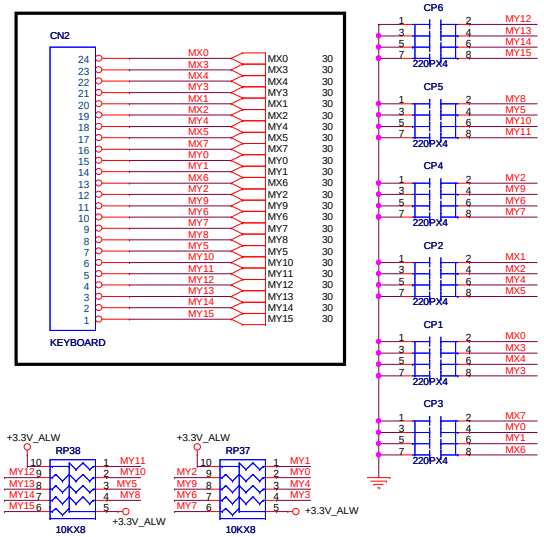
Date: Tuesday, September 16, 2008 Sheet 29 of 43


30
POWER SWITCH
IT8502
TO MMB/ THM
TO BAT/MXM
ESD recommend
EMC reserved
Layout Note: Place all capacitors close to IT8502.
Layout Note: net "3VPCU" and "RTC_VCC" minimum trace width 12mils.
(For PLL Power)
CLOSE TO SW1
Power ON S/W
Modify for C-TEST
*ORANGE LED
ORANGE LED
The ID is for M/B rev: E, LED behavior
Didital Mic & Light Sensor
Modify for F VERSION
16Mbit (2M Byte), SPI
Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.
Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.
TMKBC Function
High Enable
Low Disable
R3444 FLASH TYPE SELECT
High LPC/FWH FLASH ROM
Low SPI FLASH ROM (Default)
EC The same as SA6 Add R580,C631,C632 for ITE8502JX use.
Layout Note: 32.768kHz clock lines: a. If possible, please avoid using any through-hole. b. Please make the trace length short, and the trace width wide enough. c. The spacing to the closest neighbor should be wide enough.
Layout Note: Place R226,R205,R210 within 500 mils from SPI Flash.
PROJECT : AJ2
Quanta Computer Inc.
KBC-IT8502
Tuesday, September 16, 2008
Sheet 30 of 43

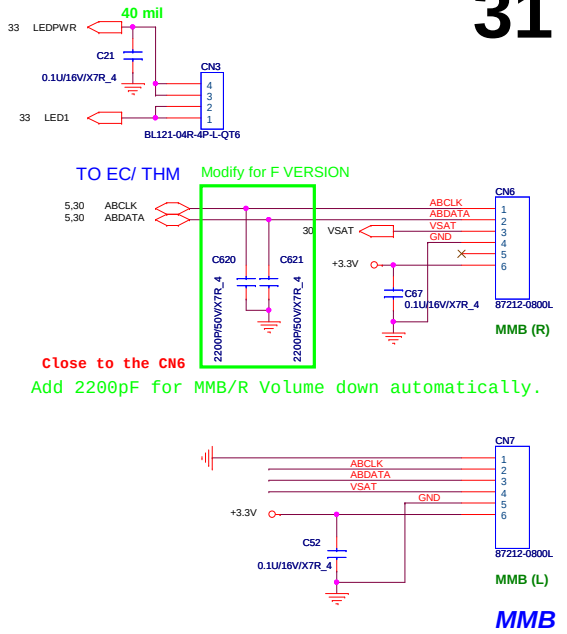
TOUCHPAD SWITCH CONN



KEYBOARD
For New Keyboard use.

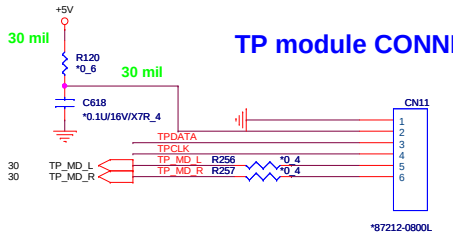


LED Power

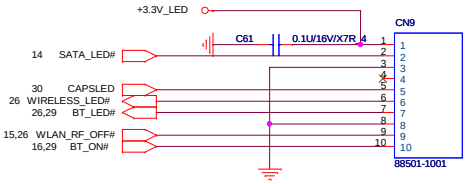


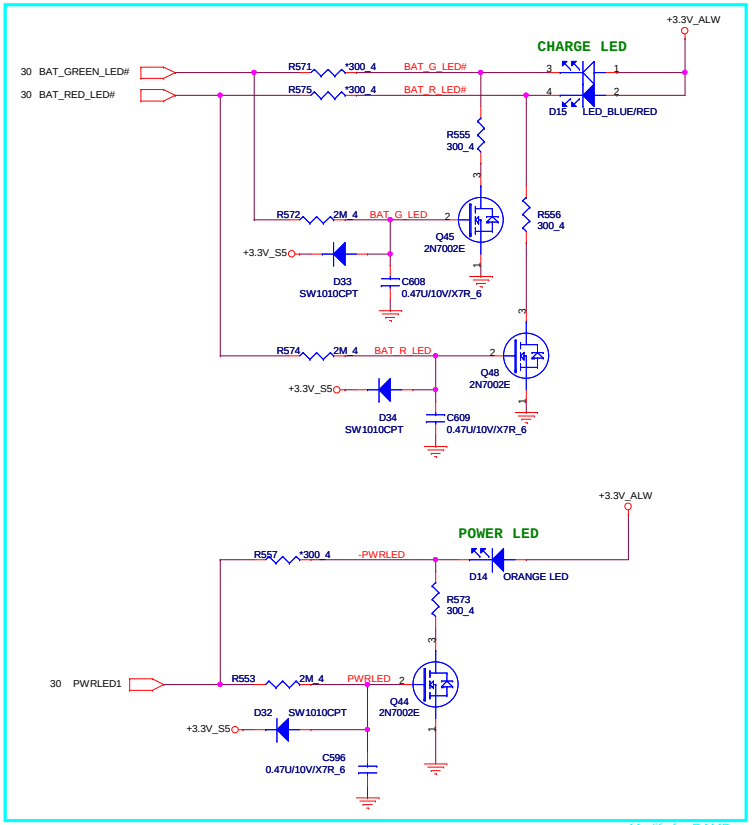
MMB

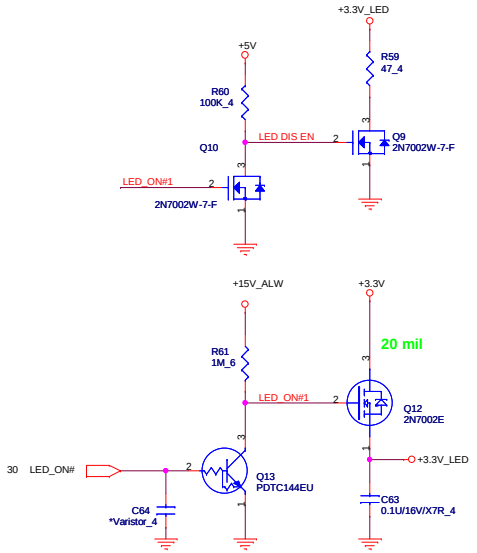
TP module CONNECTOR



To LED board







PROJECT : AJ2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	TP/KB/LED/MMB	1A
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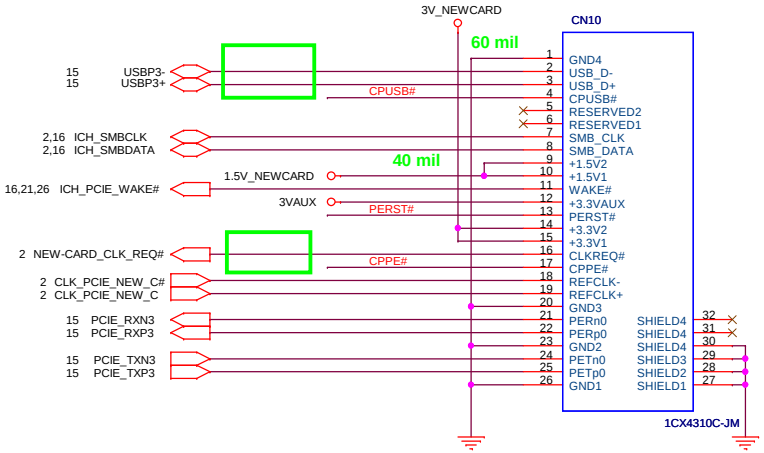
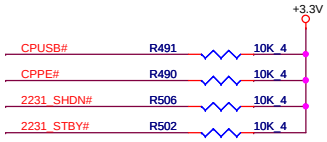
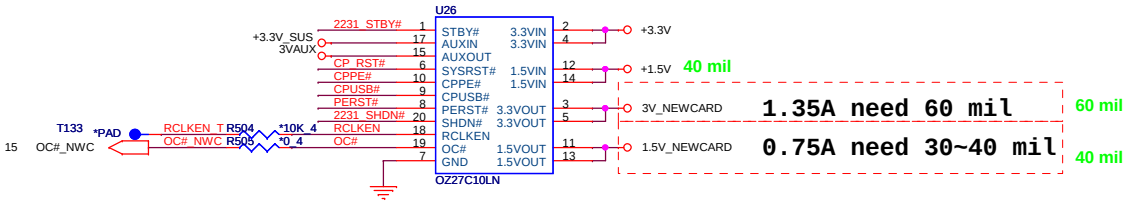
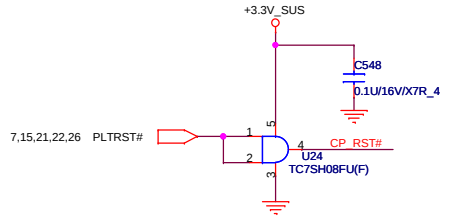
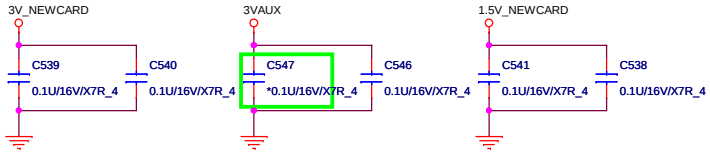
NEWCARD











PROJECT : AJ2

Quanta Computer Inc.

Size	Document Number	Rev
Custom	NEW CARD	1A

Date: Tuesday, September 16, 2008 Sheet 32 of 43

+5V
4.06A

+3.3V
3.93A

+3.3V_SUS
1.02A

+5V_SUS
5.0A

0.8A

Modify for C-TEST

For LED Keyboard Function

50mA

Discharge

Vout =0.8(1+R1/R2)
=2.5V

PROJECT : AJ2
Quanta Computer Inc.

Size	Document Number	Rev
A3	RUN POWER SW & DISCHARGER	1A

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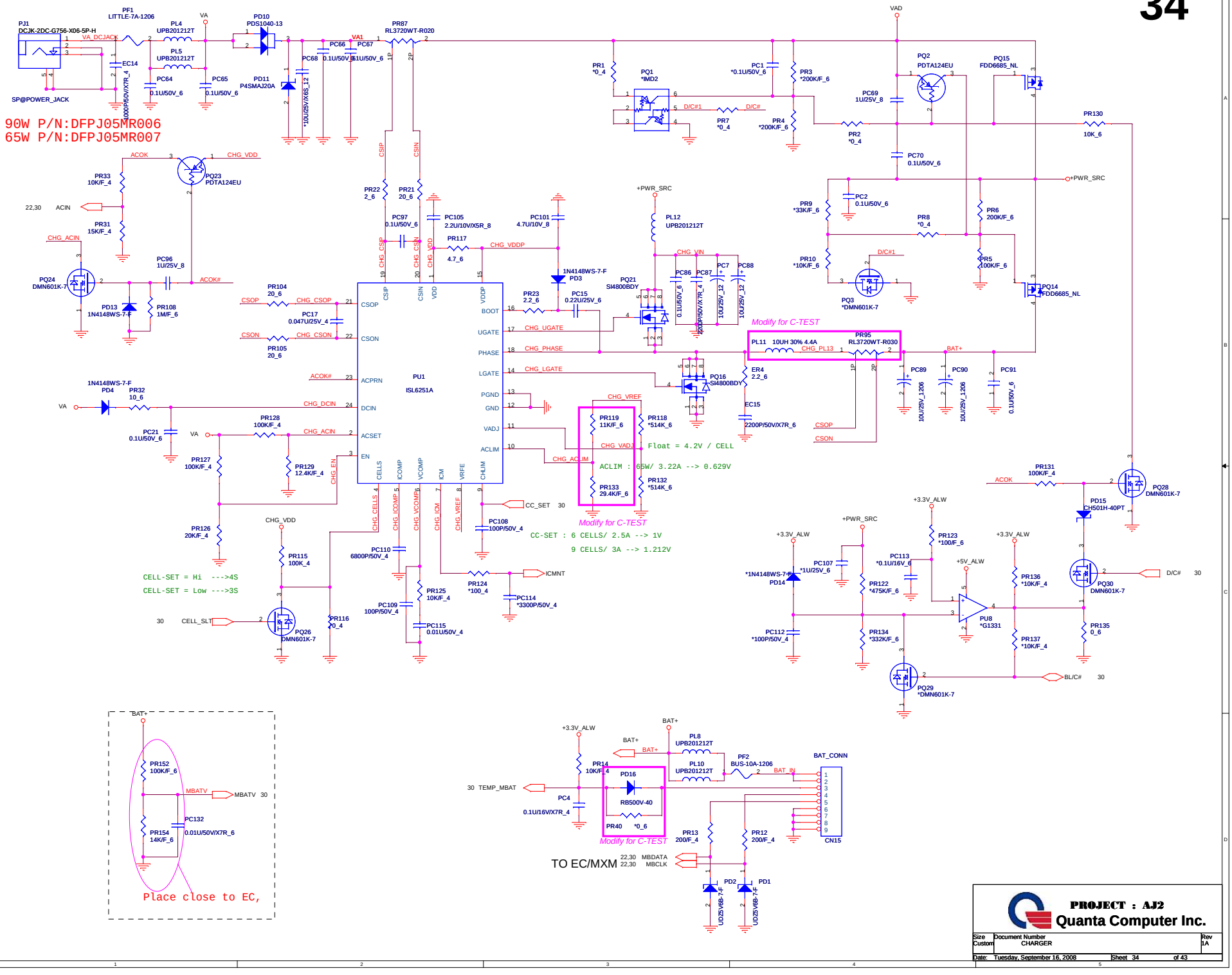
90W P/N:DFPJ05MR006
65W P/N:DFPJ05MR007
PU1 ISL6251A
PQ1 *IMD2
PQ2 PDTA124EU
PQ3 *DMN601K-7
PQ14 FDD6685_NL
PQ15 FDD6685_NL
PQ16 SI4800BDY
PQ21 SI4800BDY
PQ23 PDTA124EU
PQ24 DMN601K-7
PQ26 DMN601K-7
PQ28 DMN601K-7
PQ29 *DMN601K-7
PQ30 DMN601K-7
PU8 *G1331
PD1 UDZSV6B-7-F
PD2 UDZSV6B-7-F
PD3 1N4148WS-7-F
PD4 1N4148WS-7-F
PD10 PDS1040-13
PD11 P4SMAJ20A
PD13 1N4148WS-7-F
PD14 *1N4148WS-7-F
PD15 CH501H-40PT
PD16 RB500V-40
PF1 LITTLE-7A-1206
PF2 BUS-10A-1206
PJ1 DCJK-2DC-G756-X06-5P-H
SP@POWER_JACK
Modify for C-TEST
Float = 4.2V / CELL
ACLIM : 65W/ 3.22A --> 0.629V
CC-SET : 6 CELLS/ 2.5A --> 1V
9 CELLS/ 3A --> 1.212V
CELL-SET = Hi ---->4S
CELL-SET = Low ---->3S
Place close to EC,
TO EC/MXM
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Quanta Computer Inc.
Size Custom
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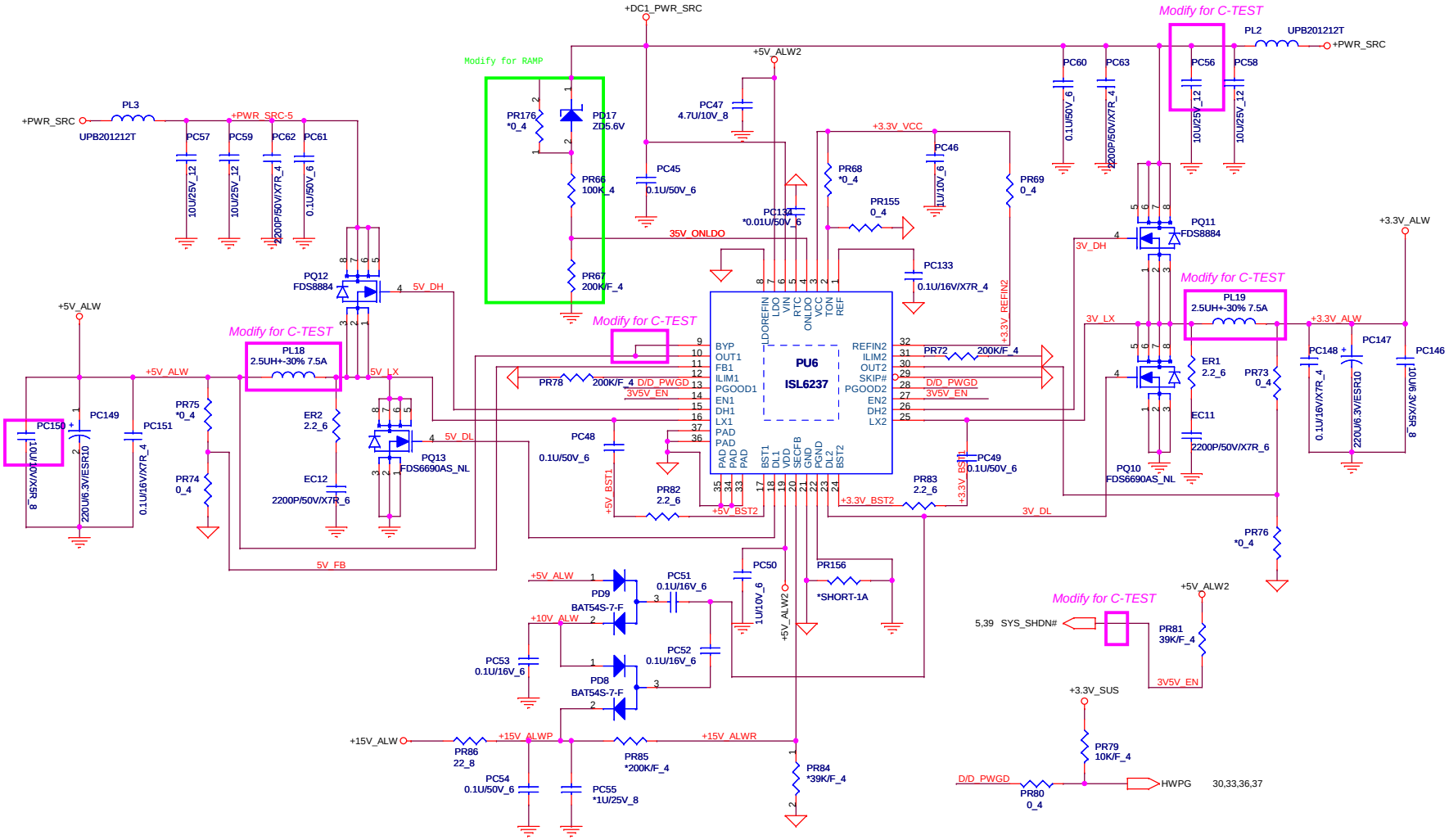
EC C-7 /8 Stuff PC56.



Size: Custom	Document Number: D/D POWER		Rev: 1A
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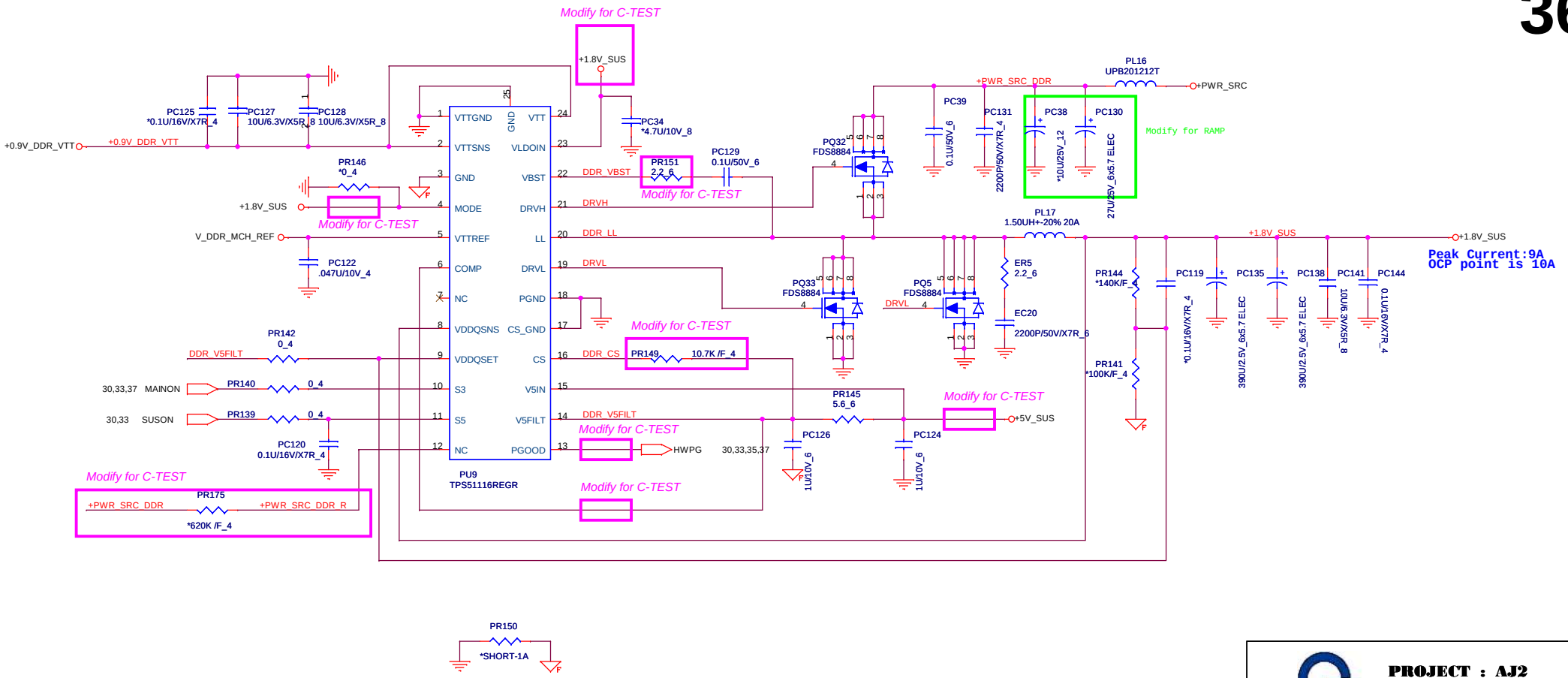

PROJECT : AJ2

Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR2_1.8VSUS,0.9V	1A

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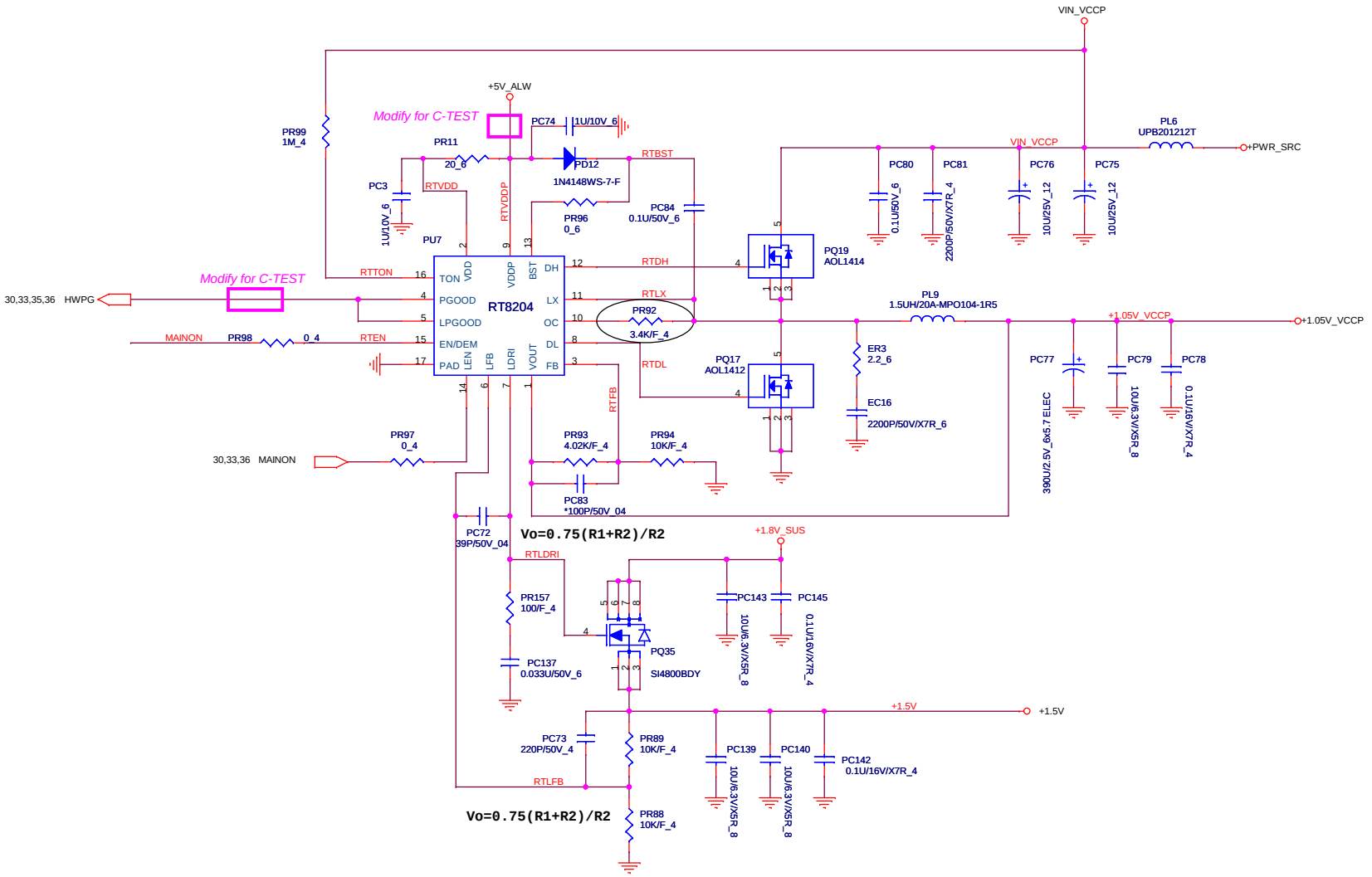

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Size	Document Number	Rev
Custom	+1.5v&1.05V	1A
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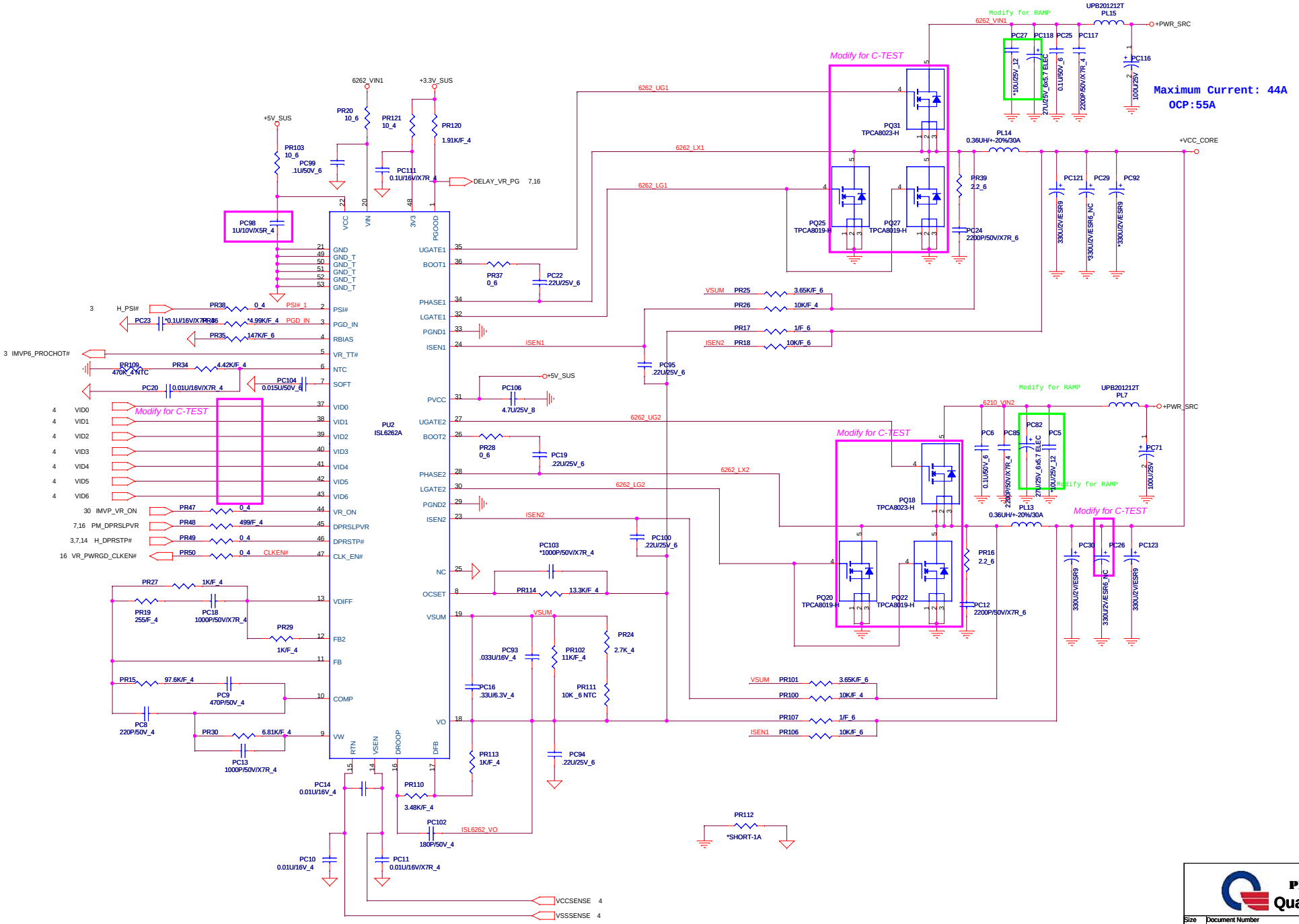
Maximum Current: 44A
OCP:55A
Modify for C-TEST
Modify for RAMP
PU2
ISL6262A
UPB201212T
PL15
PL14
0.36UH/+-20%/30A
PL7
PL13
PQ31
TPCA8023-H
PQ25
TPCA8019-H
PQ27
TPCA8019-H
PQ18
TPCA8023-H
PQ20
TPCA8019-H
PQ22
TPCA8019-H
+PWR_SRC
+VCC_CORE
+5V_SUS
+3.3V_SUS
6262_VIN1
6210_VIN2
6262_UG1
6262_LG1
6262_LX1
6262_UG2
6262_LG2
6262_LX2
ISEN1
ISEN2
VSUM
ISL6262_VO
DELAY_VR_PG 7,16
VCCSENSE 4
VSSSENSE 4
*SHORT-1A
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CPU_CORE POWER
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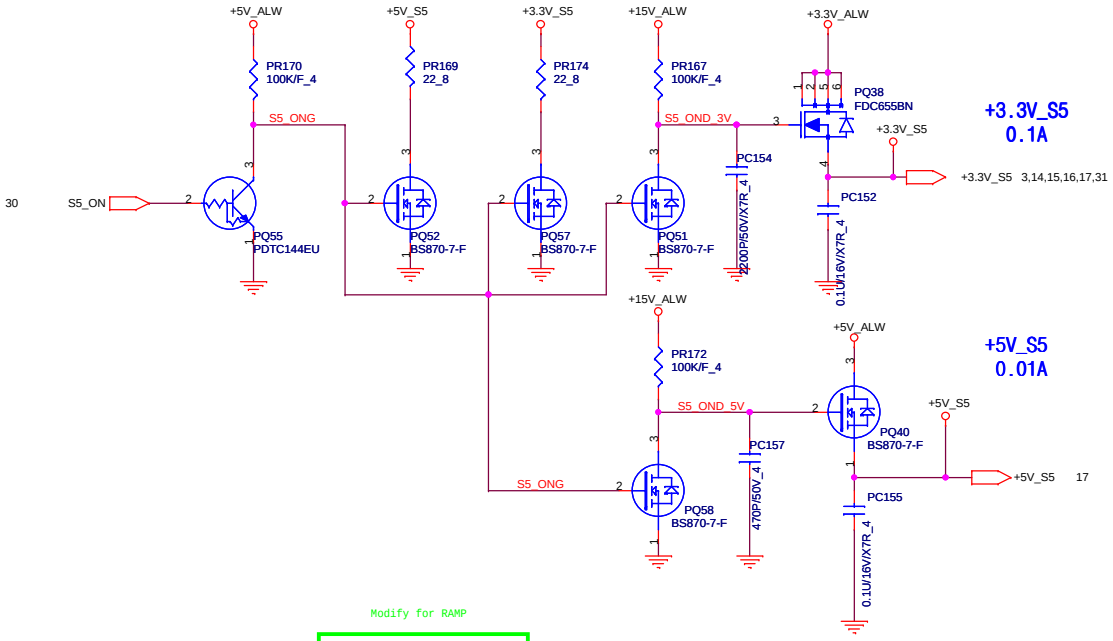

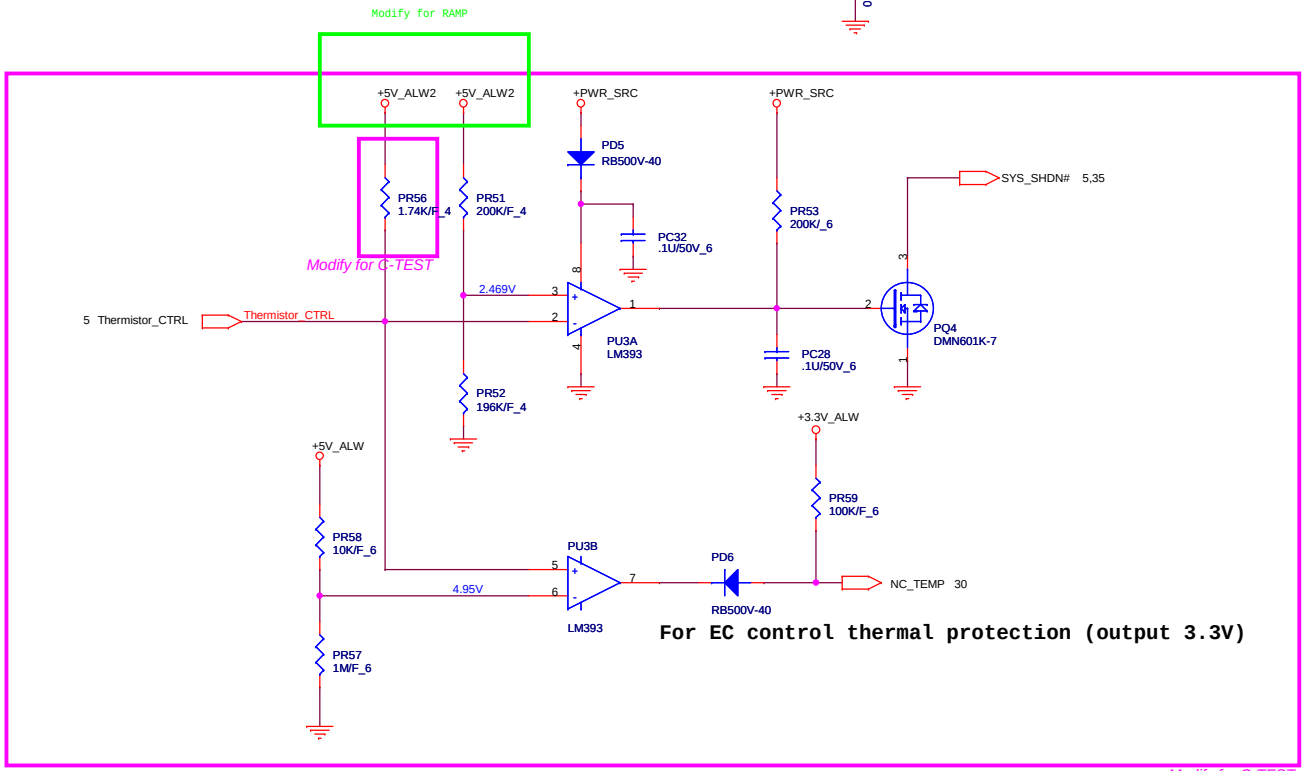

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A-Type H-C315D102P2

HOLE2 *H-C315D110P2

HOLE30 *H-C315D110P2

B-Type H-C315D118P2 *12 PCS.

HOLE20 *H-C315D118P2
HOLE3 *H-C315D118P2
HOLE19 *H-C315D118P2
HOLE33 *H-C315D118P2
HOLE34 *H-C315D118P2
HOLE15 *H-C315D118P2
HOLE4 *H-C315D118P2
HOLE9 *H-C315D118P2
HOLE22 *H-C315D118P2
HOLE32 *H-C315D118P2

C-Type H-TC315D169P1

CPU SCREW HOLE

HOLE8 *h-c236d169i209p2
HOLE13 *h-c236d169i209p2
HOLE14 *h-c236d169i209p2
HOLE7 *h-c236d169i209p2

for wirless wire

HOLE5 *H-C295D295N

for MXM NUT*4

HOLE11 E@H-C236D142P2
HOLE12 E@H-C236D142P2
HOLE16 E@H-C236D142P2
HOLE17 E@H-C236D142P2

for MDC NUT*2

HOLE28 H-C236D142P2
HOLE24 H-C236D142P2

for NB UNT

HOLE23 H-TC169BC236D142P2

Modify for C-TEST

HOLE1 H-TC169BC236D142P2
HOLE6 H-TC169BC236D142P2

Add new hole boss

HOLE21 h-c276d118p2

for Mini PCIE NUT*4

HOLE29 H-TC160BC236D142P2
HOLE27 H-TC160BC236D142P2
HOLE25 H-TC160BC236D142P2
HOLE26 H-TC160BC236D142P2

HOLE10 E@H-C236D142P2
HOLE18 E@H-C236D142P2

Full **Half**

EMI Use

+5V_SUS
EC7 0.1U/16V/X7R_4
EC19 0.1U/16V/X7R_4
EC22 0.1U/16V/X7R_4
EC24 0.1U/16V/X7R_4

+3.3V_ALW
EC8 0.1U/16V/X7R_4
EC23 0.1U/16V/X7R_4
EC21 0.1U/16V/X7R_4

+1.05V_VCCP
EC10 0.1U/16V/X7R_4
EC6 0.1U/16V/X7R_4

+15V_ALW
EC5 0.1U/25V_4
EC13 0.1U/25V_4
EC9 0.1U/25V_4

+PWR_SRC
+1.05V_VCCP
EC1 1000P/50V/X7R_4
EC4 1000P/50V/X7R_4
EC2 1000P/50V/X7R_4
EC3 1000P/50V/X7R_4

MODEM

PAD1 FDBF1006

Modify for C-TEST

Power JACK ESD PAD

PAD2 CON1_10

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EC A06 page7 R154,R157 Change HSYNC,VSYNC value form 30.1 to 24.9/F
EC A08 page7 R418 Change LVDS_IBG value form 24K/F to 2.4K/F
EC A07 page7 R159 Change CRTIREF value form 75/F to 1K/F
EC A03 page9 Modify to*E@0_6 R91,R93 for UMA BOM .
EC A04 page16 Add R544,R561 for LCD GPIO fucction use!.
EC A19.page18 Change R344,345 value from 0 ohm to 1K ohm for lid S/W function .
EC A19.page18 ADD L11 Del R46,R47 for EC Backlight control function .
EC A04 page19 Del R341,D6 for HDMI LEVEL SHIFT use!.
EC A17.page19 Modify to correct net,ADD RN18 for MXM HDMI SCH.
EC A17.page21 Change Value to 75_6 (R40,358,359,360,362) ;C379 change to 10uf/4v.
EC A10 page22 C457,C468 Modify to *E@XX for UMA BOM.
EC A16.page22 Modify to correct net for UMA HDMI SCH.
EC A14.page25 Del C80,C81 CAP. for MDC RJ11 BOM.
EC A01 page28 USB CONN CN22,CN26 PIN define USB +-data swape it.
EC A05 page28 Change C102,C558 value&footprint 10U/10V_0805 (CH6102M9A01)
EC A12 page30 Del R120,R121 FOR Change the SMBus from 117 & 118 to 115 & 116 .
EC A02 page30 Modify LAN_DISABLE#_0 form pin68 to pin56.
EC A11 page31 Modify CN8 SCH. for TUCHPAD G372 PIN Define.
EC A15.page31 Modify MMB(L) CN7.Pin6 net TO GND .
EC A18.page31 Del. T/P module CONNECTOR SCH .
EC A20 page31 Modify LED POWER CONN. CN3 PIN define .
EC A09 page37 PR93 Change value from 4.7K/F to 4.02K/F for +1.05V use.
EC A13.page40 Del Hole11,12,16,17 MXM NUT for UMA BOM.

B-test to C-test EC list

1.EC page2 _Remove 0 ohm resistance array(RP18,RP19,RP20,RP21,RP29,RP22,RP28,RP27,RP26,RP25).
2.EC page7 _Remove R89,R86 and NET(PLTRST#_R).
3.EC page10 _Change L56,L57 to R560,R559.
4.EC page15 _Not stuff U10,C257,R251,R293,R252,R253,R294,R295.
5.EC page17 _Not stuff U22,C510,R446,R431,C514 for MXM.
6.EC page18 _Remove 0 ohm resistance L10.
7.EC page18 _Modify LCD Connector's pin definition(PIN37 from GND to NC).
8.EC page19 _Change R322 value form 100K/F to 20K/F.
9.EC page21 _Not stuff U5,R77,R80 ; stuff R83.
10.EC page21 _Change R358,R359,R360,R362,R40 footprint from 0603 to 0805.
11.EC page21 _Change C25 value from 1500pF to 1000pF(same as C66).
12.EC page24 _Modify SPEAKER Connector's pin definition(mirror).
13.EC page24 _Change C298,C305,C304,C302,C303 footprint from 0603 to 0402.
14.EC page28 _Remove 0 ohm resistance array RP32,RP33.
15.EC page28 _Change C98,C549 value from 22uF to 10uF.
16.EC page30 _Add R552(1k) and R121(*10k) to pull low and pull high.
17.EC page30 _Remove R122(10k) and net EC_GPB7.
18.EC page30 _Change R1,R2(*),R3(*) value from 150 ohm to 300 ohm.
19.EC page31 _Modify MMB Connector's pin definition(mirror:CN6,CN7).
20.EC page31 _Modify LED Display circuit.
21.EC page33 _Change PL1 value from 22UH to 10UH.
22.EC page33 _Remove 0 ohm resistance PR65,PR60.
23.EC page34 _Change PL11's part number to CV01044TZ01.
24.EC page34 _Add PD16 and PR40(*) on BAT CON's pin3 to avoid leakage current.
25.EC page34 _Change PR95 part number to CS+0308FL00.
26.EC page34 _Change PR133 value from 11k/F ohm to 29.4k/F ohm .
27.EC page34 _Change PR119 value from 16k/F(MXM) or 75K/F(UMA) ohm to 11k/F(MXM) or 178K/F(UMA) ohm .
28.EC page35 _Change PL19 and PL18 part number to CV-2575TZ04.
29.EC page35 _Short PU6 pin9 and pin10.
30.EC page35 _Remove 0 ohm resistance PR77.
31.EC page35 _Stuff PC56.
32.EC page36 _Remove 0 ohm resistance PR147,PR148,PR138,PR143.
33.EC page36 _Modify PU9 pin23's net from +1.8V_SUSP to +1.8V_SUS.
34.EC page36 _Add PR175(*) connect to PU9 pin12 and pull high to +PWR_SRC_DDR(buffer).
35.EC page36 _Change PR149 value from 14k/F ohm to 10.7k/F ohm.
36.EC page36 _Change PR151 value from 0 ohm to 2.2 ohm.
37.EC page37 _Remove 0 ohm resistance PR90,PR91.
38.EC page38 _Remove 0 ohm resistance PR40,PR41,PR42,PR43,PR44,PR45,PR46.
39.EC page38 _Change PQ31 and PQ18 part number to BAM80230000.
40.EC page38 _Change PQ25,PQ27,PQ20,PQ22 part number to BAM80190000.
41.EC page38 _Change PC26 part number to CH733RM8874.
42.EC page39 _Stuff PR51,PR52,PR53,PR56,PR57,PR58,PR59,PC28, PC32,PD5, PD6,PQ4,PU3 for EC control thermal protection.
43.EC page40 _Change HOLE23's NUT to FBAJ2003010.
44.EC page40 _Add SPRING PAD1 to fix MODEM's cable.

C-test to FAI list

1.EC page2 _Change C188,C189 value form 30P to 27P for RCT timing.
2.EC page2 _Change UAM BOM add original RP24 for LVDS spread spectrum clock issue.
3.EC page16 _Change BOARD_ID0 resister to pull low. (remove R201 and add R202).
4.EC page16 _Add C612 0.1uF/16v_4 near R27810/F_4 fix RTC CMOS checksum error.
5.EC page18 _Add PD18 Close to LCD CONN. CN1 fix U2 break down .
6.EC page18 _Del. USB8+- data remove the RP1&L8;Del. R32 0 ohm.
7.EC page18 _Change value C325 from 0.1U/16V/Y5V to 0.1U/16V/X7R .
8.EC page24_ Change GND CN33,34,35 from ADO_GND to Digtal_GND for ESD solution.
9.EC page24_Add *C619 Varistor_0402 near R310 for ESD use.
10.EC page26_Change net CN30,32 name from +3.3v_sus to +3.3v .
11.EC page30_Del. R552 for EC change to"slowly pulse" detect pin use .
12.EC page30_Add +3.3V C54,C62 0.1UF/16V;C610,C611 100P/50V near CN4.
13.EC page30_Move the R539,R534 from 24 page to 30 page.
14.EC page31_Modify BOM to POWER,Charge LED bevhavior "solwly pulse" .
15.EC page26,27,31,32_Del. 0 ohm RP30,RP31,R230,R233,R254,R255,R229,L20,L59,L12,R569,R248 cost doown .
16.EC page22_ ADD PC162 100U/25V.
17.EC page35_ ADD PD17 ;Change value PR67 to 200K/F_4 PR66 to 100K/F_4.
18.EC page36_Change value PC130 to 27U/25V .
19.EC page38_Change value PC118 to 27U/25V .

20.EC page30_ ADD LDO(PU10) circuit to reduce DMIC noise.
21.EC page31_Add 2200pF(C620,C621) for MMB/R Volume down automatically issue.
22.EC page21_Change transformer's PCB footprint.