VFKTA

Rosetta 10FT/10FTG

LA-9862P REV 1.0 Schematic

Intel Processor (Ivy Bridge/Sandy Bridge)+
PCH(Panther Point)

2013-02-06 Rev 1.0

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Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	Cover Page
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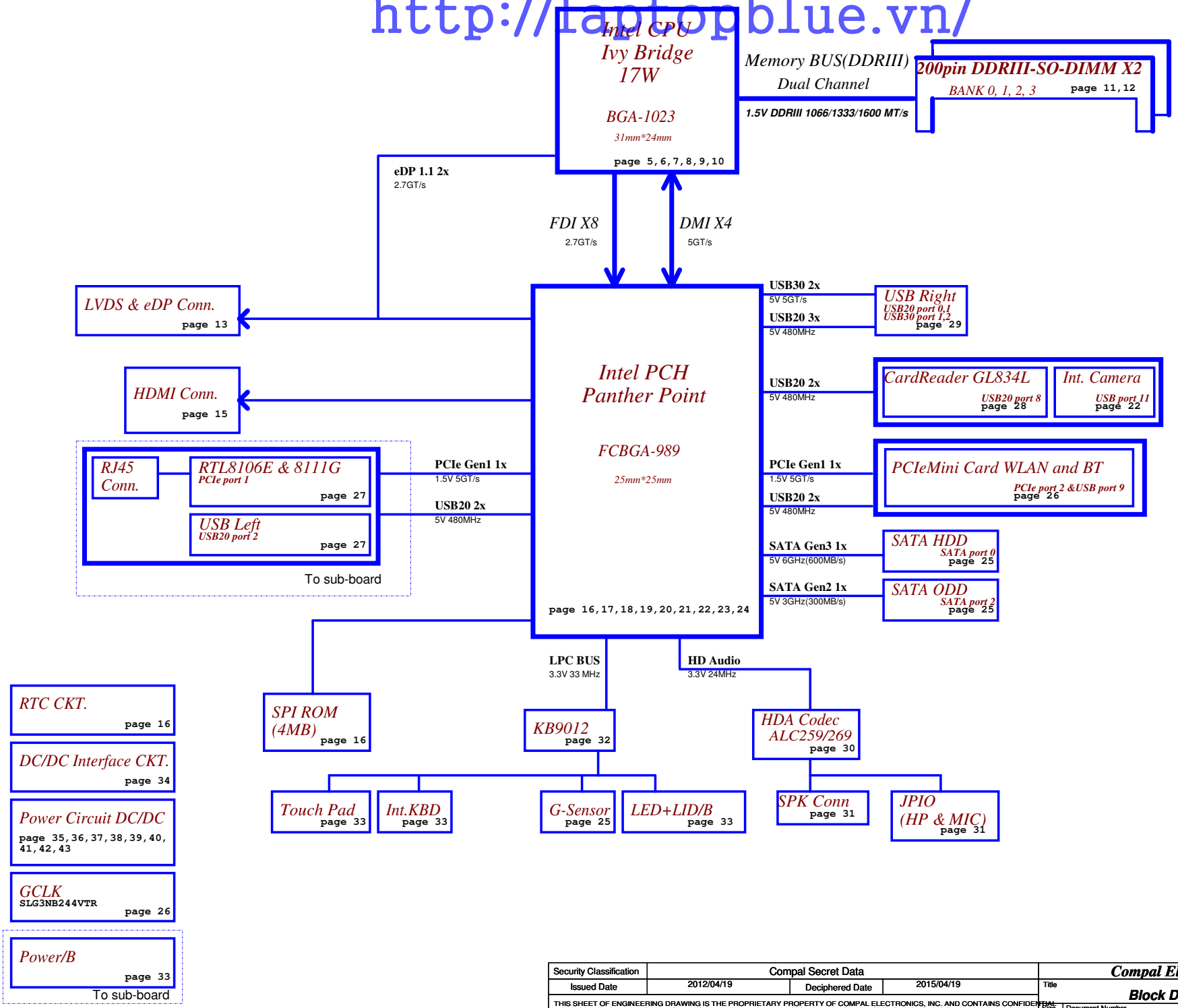

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Compal Electronics, Inc.			
Title: Block Diagram			
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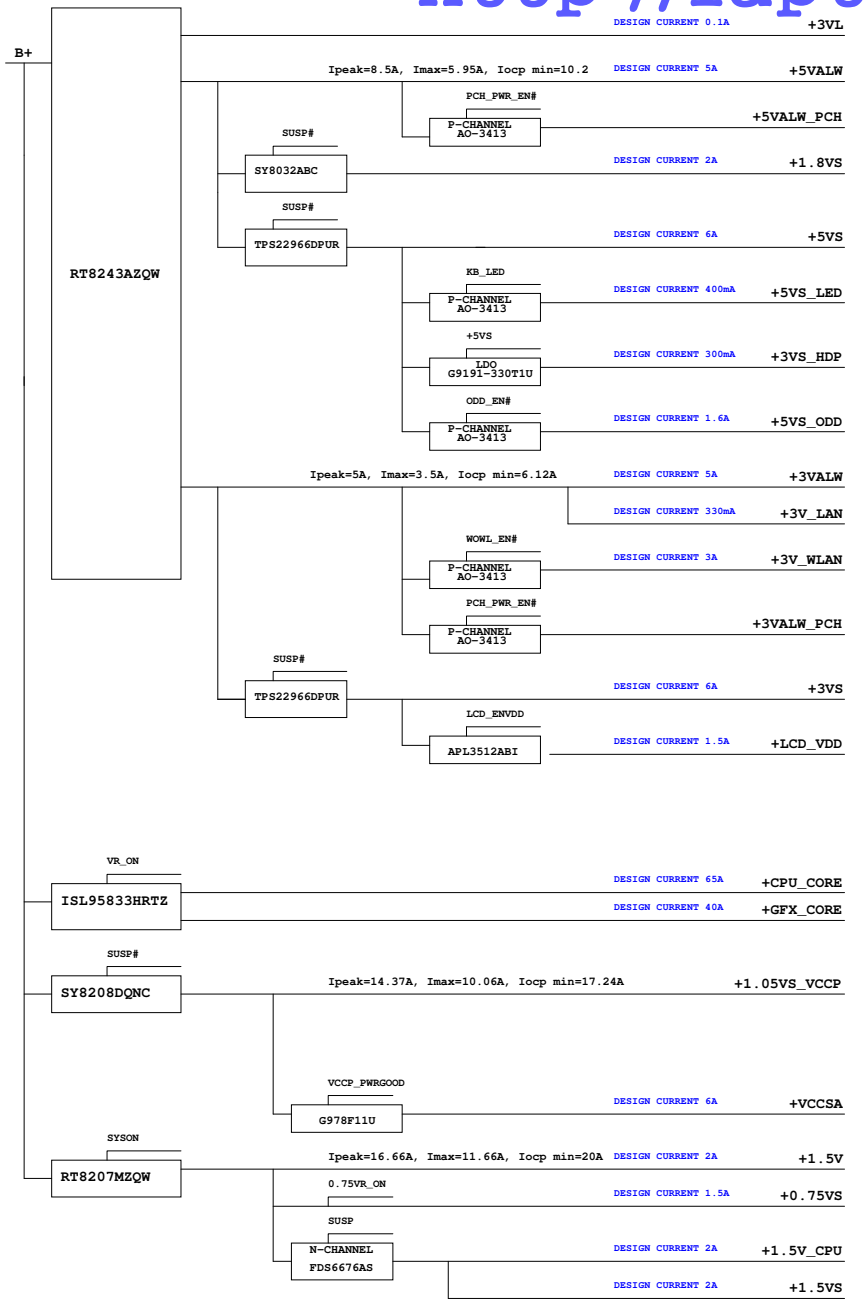

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Compal Electronics, Inc.			
Title	Power Tree		
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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.5V_CPU +0.75VS +CPU_CORE +GFX_CORE +VCCSA +1.05VS_VCCP +3V_WLAN +3V_LAN +LCD_VDD
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

BTO Option Table

Function	CPU					PCH	
description	IVB i5 3337U	IVB i3 3227U	IVB i3 2375M	IVB P 2117U	IVB C 847	Panther Point	
explain	IVB i5 3337U	IVB i3 3227U	IVB i3 2375M	IVB P 2117U	IVB C 847	HM76	HM70
BTO	CPUI53337UR1@	CPUI33227UR1@	CPUI32375MR1@	CPUP2117UR1@	CPUC847R1@	HM76R1@	HM70R1@
	CPUI53337UR3@	CPUI33227UR3@	CPUI32375MR3@	CPUP2117UR3@	CPUC847R3@	HM76R3@	HM70R3@

Function	LVDS-eDP		Camera & Mic	USB S&C		CRT			EC	
description	LVDS-eDP		Camera & Mic	14640	14641	CRT			EC	
explain	LVDS	eDP	Camera & Mic	14640	14641	w/ CRT		w/o CRT	KB9012	NPCE885N
BTO	LVDS@	IEDP@	CAM_EMI@	14640@	14641@	CRT@	CRT_EMI@	NOCRT@	9012@	885@

Function	WOWL		G-SENSOR	ZPODD		GCLK		Touch Screen	
description	WOWL		G-SENSOR	ZPODD		GCLK	non-GCLK	Touch Screen	
explain	w/	w/o	G-SENSOR	w/	w/o	GCLK	non-GCLK	Touch Screen	
BTO	WOWL@	NOWOWL@	GSENSOR@	ZPODD@	NONZP@	GCLK@	NOGCLK@	TOUCH_EMI@	

Function	Sleep & Music		KB Light	EMI/ESD/RF part					ISPD	
description	Sleep & Music		KB Light	EMI/ESD/RF part					HDMI Logo	
explain	w/ S&M	w/o S&M	KB Light	EMI/ESD/RF part					HDMI Logo	
BTO	269@	259@	KBL@	EMI@	@EMI@	ESD@	@ESD@	@RF@	HDMI45@	

Red Word: always un-mount

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Touch Pad	2C H	0010 1100 b

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	Smart Charger	12 H	0001 0010 b
+3VL	USB S&C 14640	35 H	0011 0101 b

Power	Device	HEX	Address

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	G-Sensor	40 H	0100 0000 b

10/22A Add G-sensor reference Hemen

10/22A Add Smart Charger SMBus address: 0x12 Hemen
we Add already

STATE / SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

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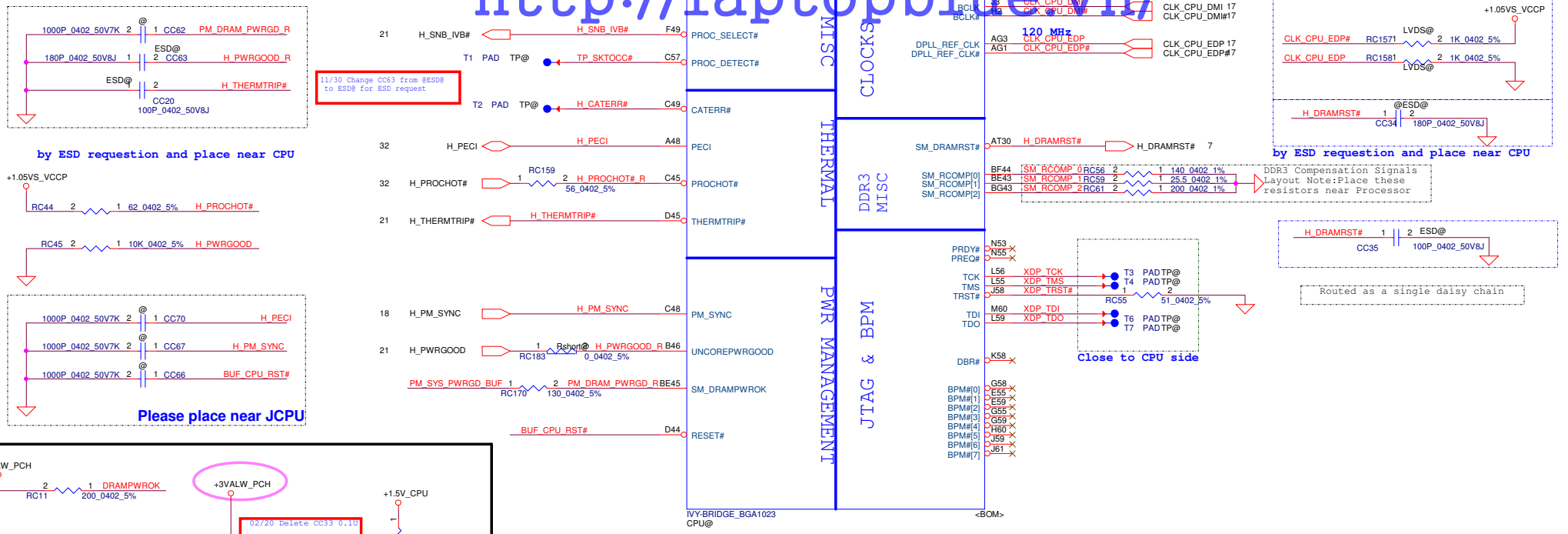
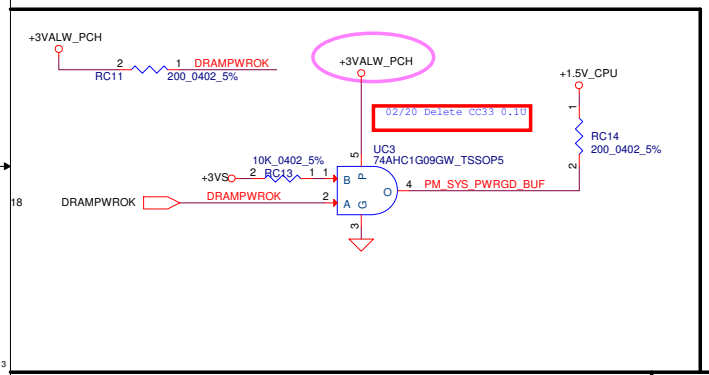
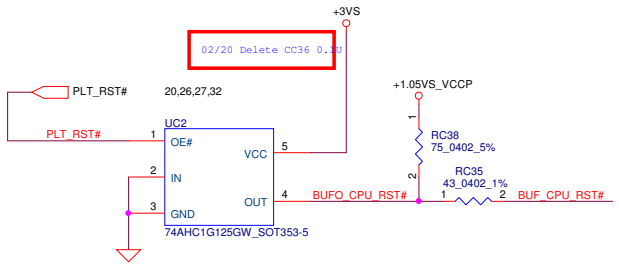


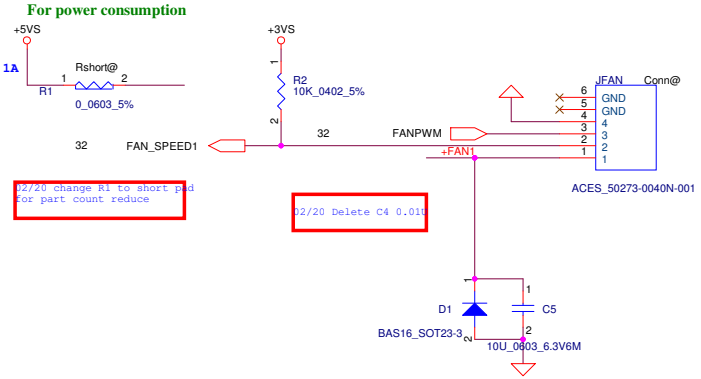


Buffered Rest to CPU



XDP Connector

FAN Control Circuit



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Title	Ivy Bridge_JTAG/XDP/FAN		
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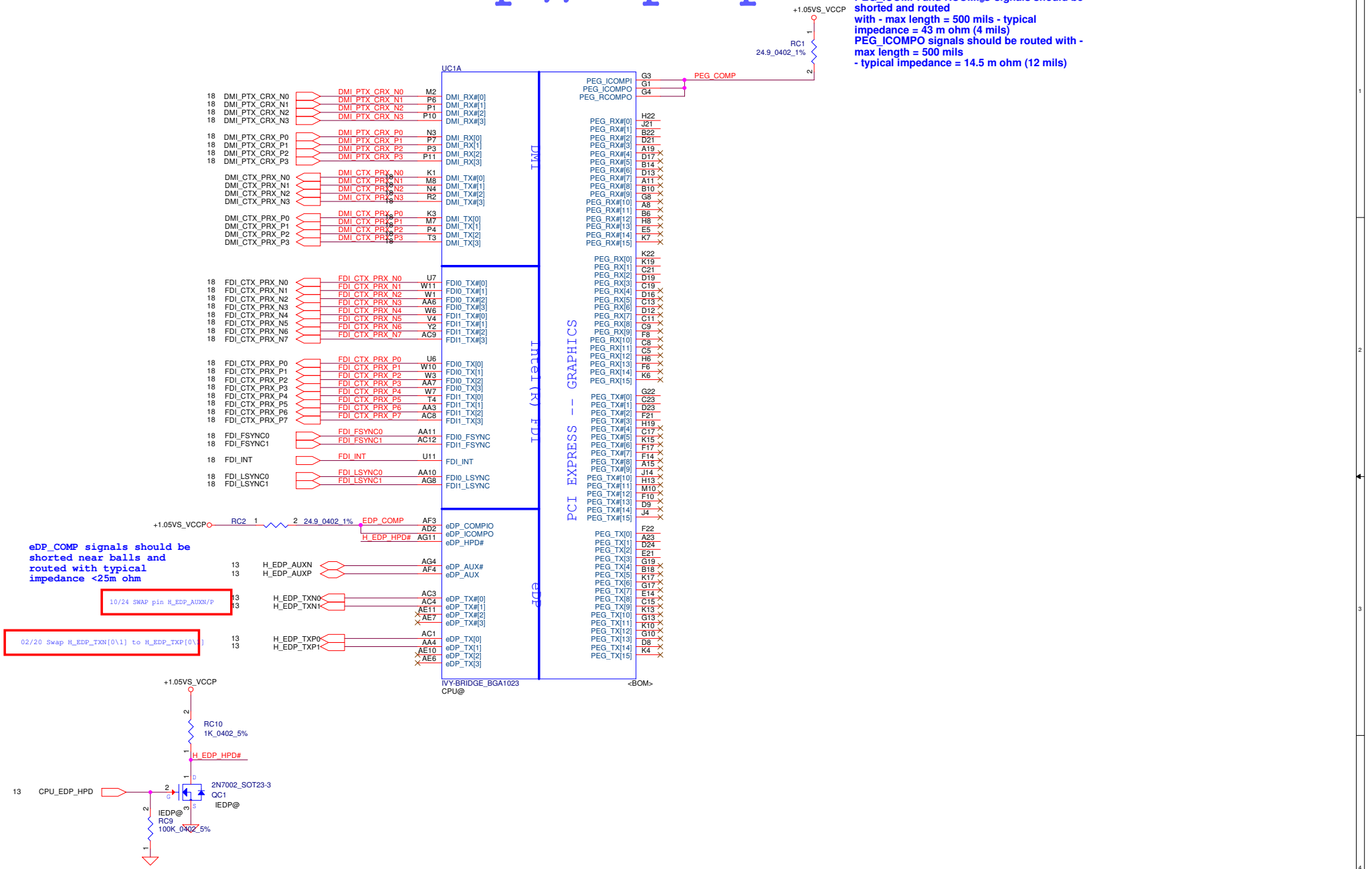

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Title	Ivy Bridge_DMI/PEG/FDI		
Size: Custom	Document Number: VFKTA		Rev: 1.0
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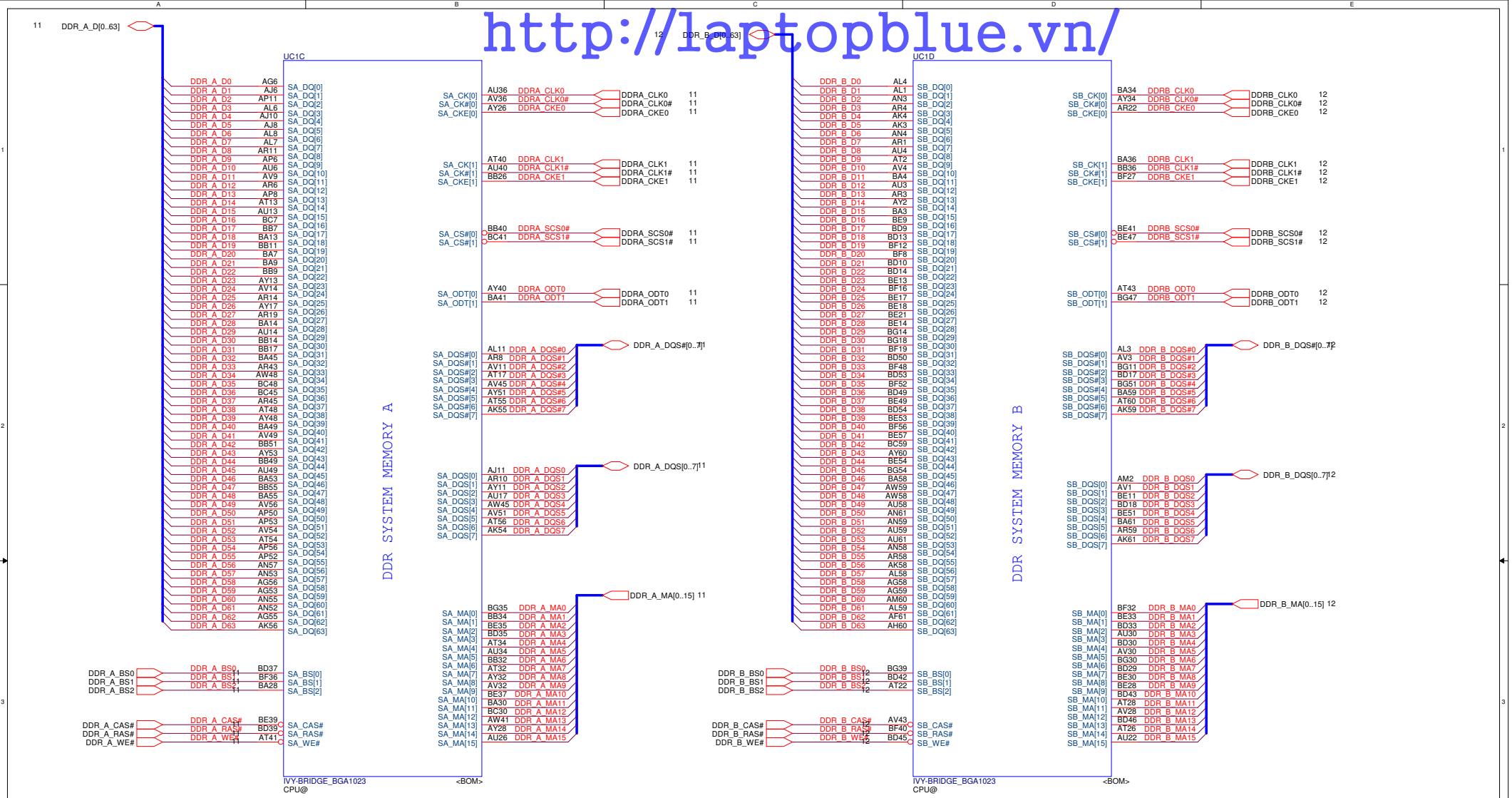

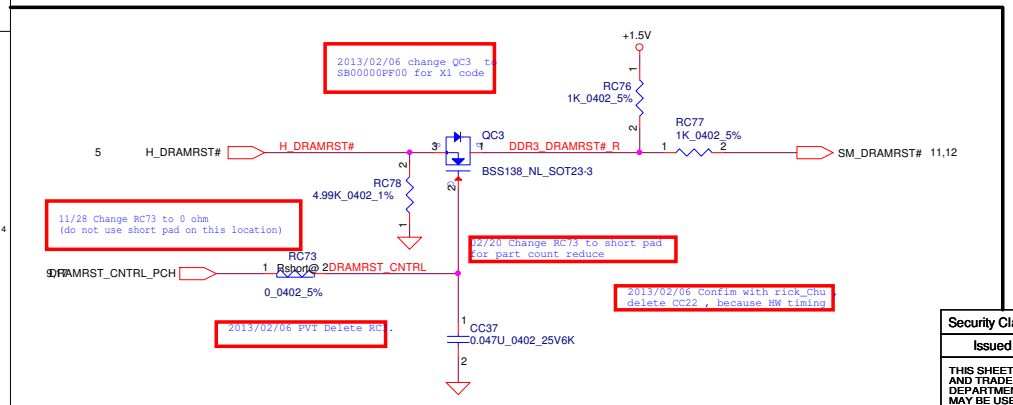

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Title	Ivy Bridge_DDR3		
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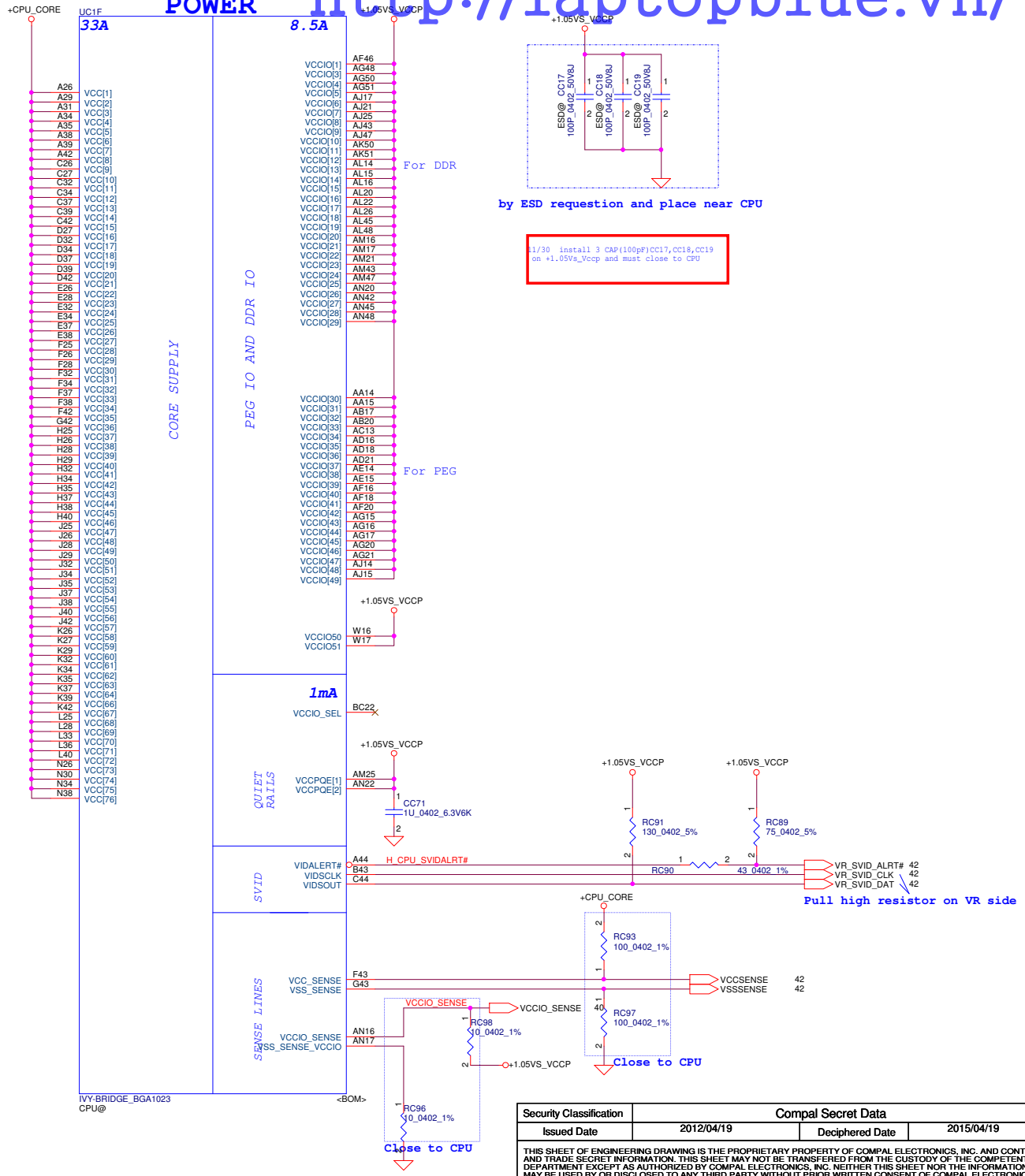
POWER



by ESD requestion and place near CPU

11/30 install 3 CAP(100pF)CC17,CC18,CC19 on +1.05Vs_Vccp and must close to CPU

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Title	Ivy Bridge_POWER-1		
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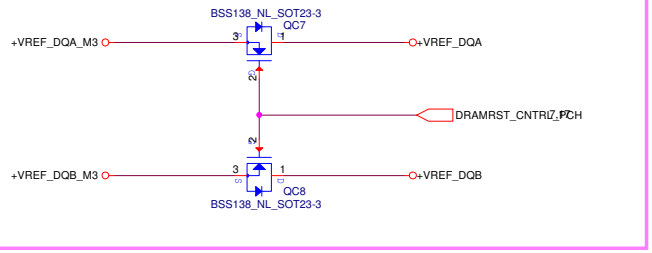
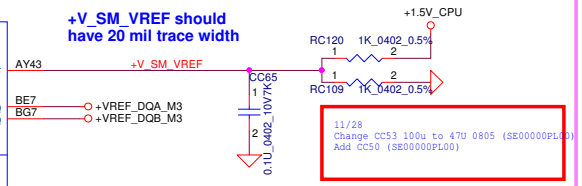
POWER

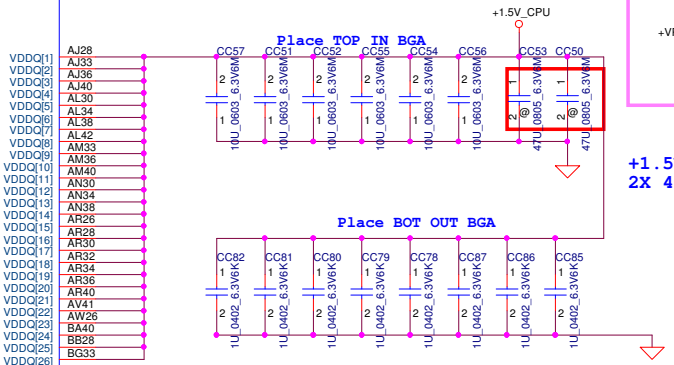
Intel DDR Vref M3



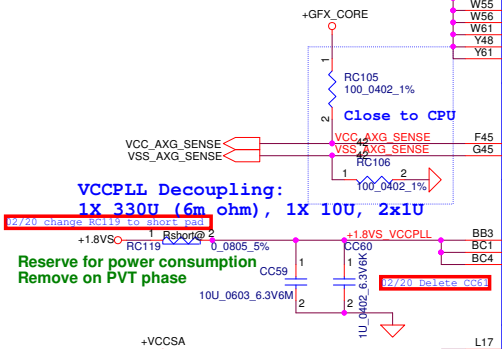
+V_SM_VREF should have 20 mil trace width



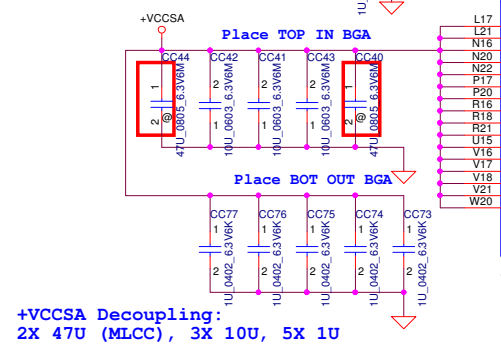
+1.5V_CPU Decoupling: 2X 47U(MLCC), 6X 10U, 8X 1U



VCCPLL Decoupling: 1X 330U (6m ohm), 1X 10U, 2x1U

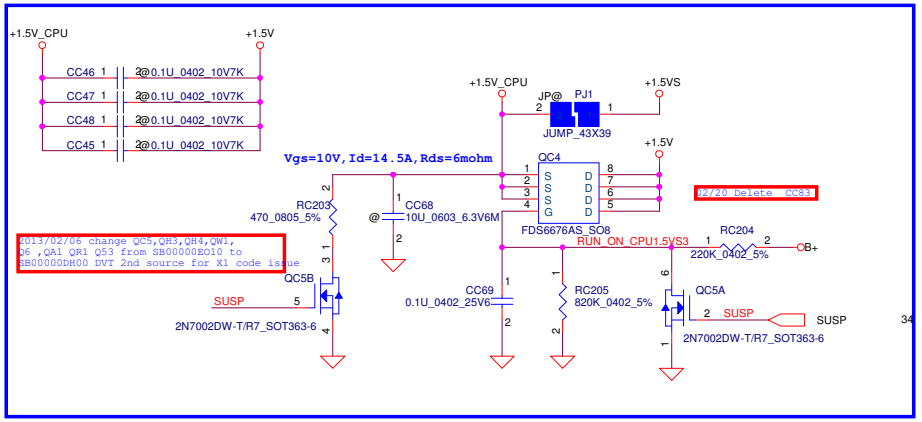


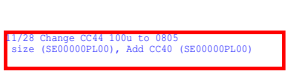
+VCCSA Decoupling: 2X 47U (MLCC), 3X 10U, 5X 1U



VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.90 V
0	1	0.80 V
1	0	0.725 V
1	1	0.675 V

For Sandy Bridge





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Title	Ivy Bridge_POWER-2		
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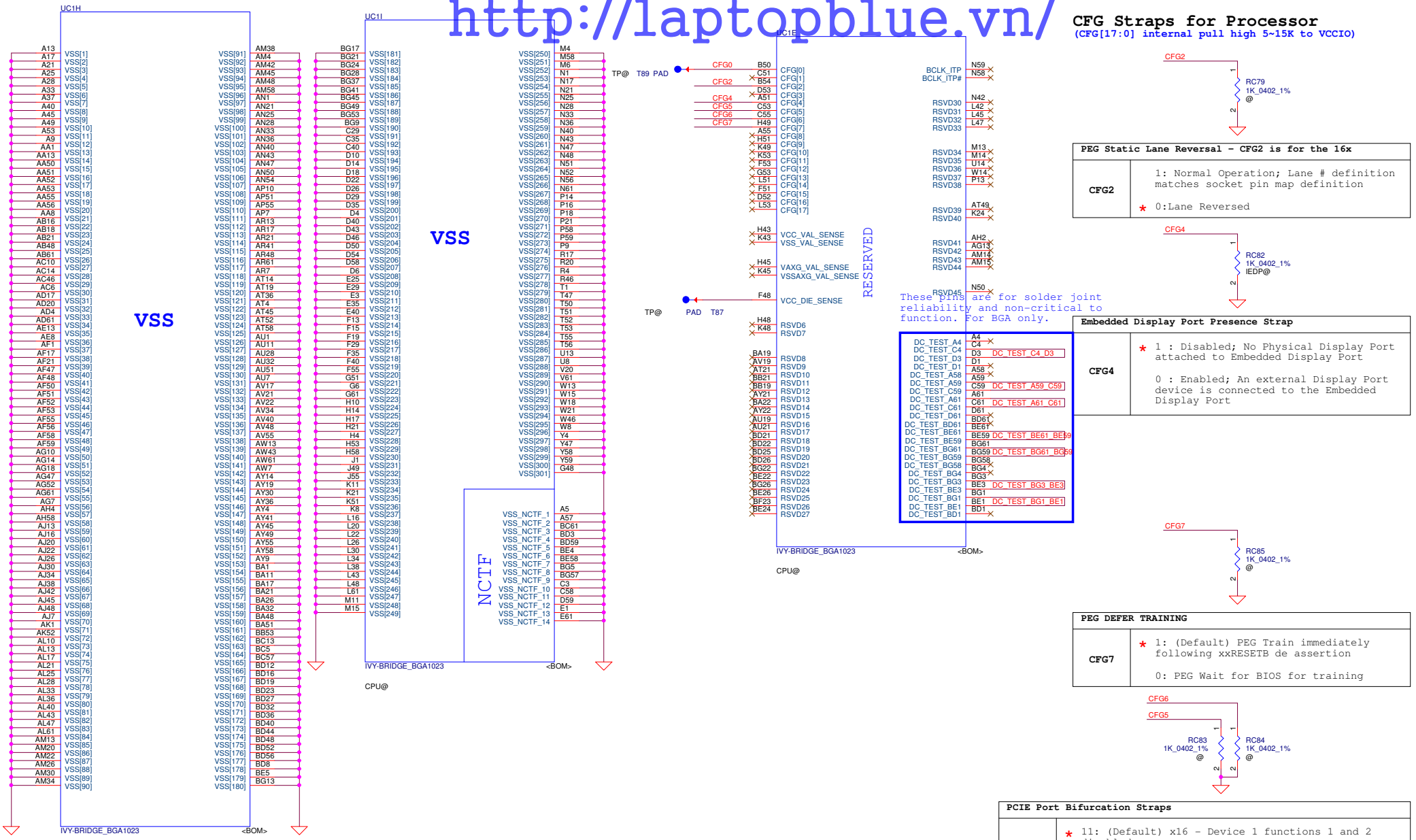

CFG Straps for Processor

(CFG[17:0] internal pull high 5~15K to VCCIO)

PEG Static Lane Reversal – CFG2 is for the 16x

CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

Embedded Display Port Presence Strap

CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PEG DEFER TRAINING

CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

PCIE Port Bifurcation Straps

CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled 01: Reserved - (Device 1 function 1 disabled; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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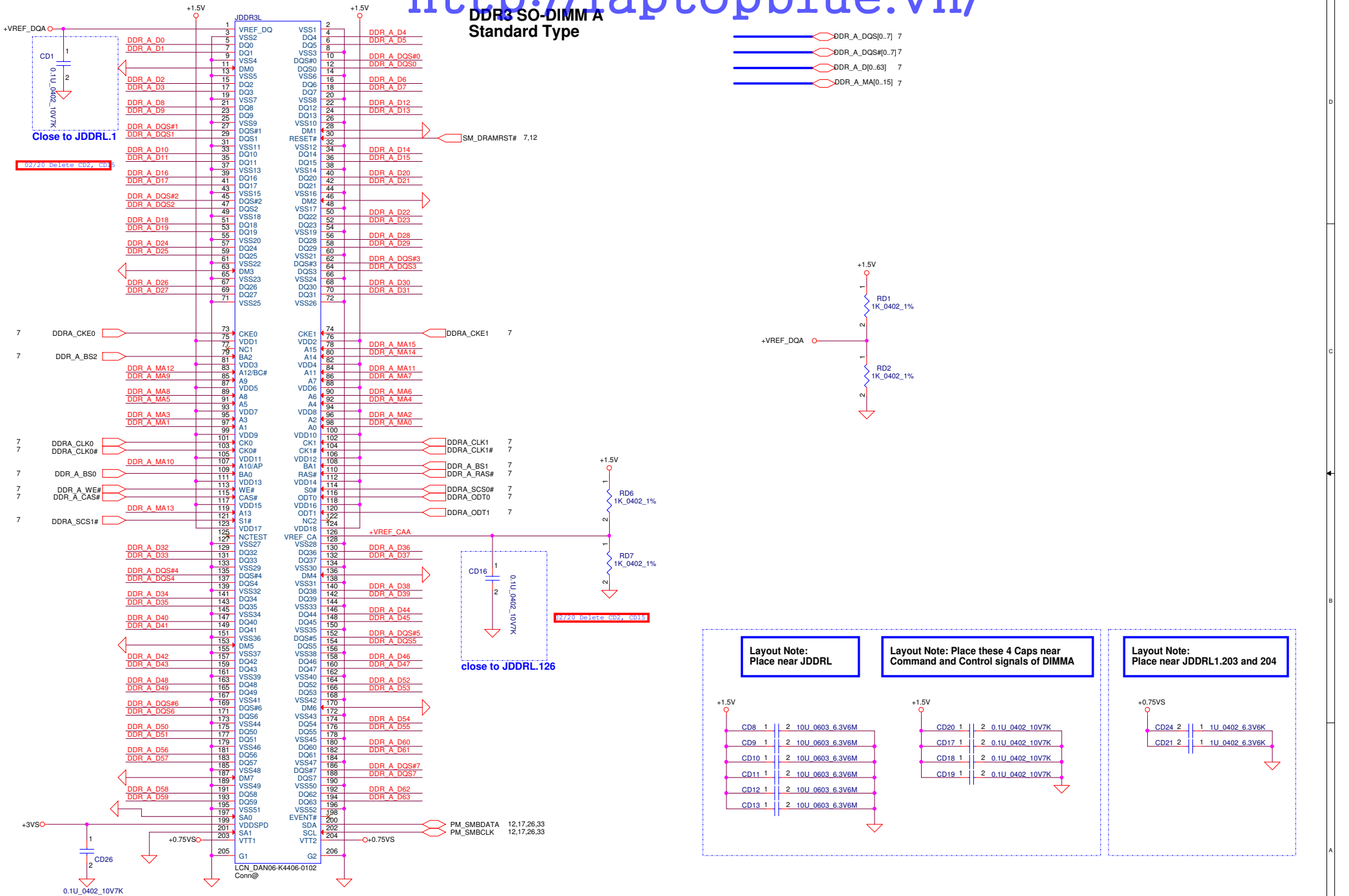
DDR3 SO-DIMM A
Standard Type



SPD setting (SA0, SA1)
PU/PD by Channel A/B
->Channel A 00
->Channel B 01

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Title	DDRIII-SODIMM0		
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DDR3 SO-DIMM B
Standard Type

JDDR3H

+VREF_DQB
+1.5V
+3VS
+0.75VS

CD27 0.1U_0402_10V7K — D2/20 Delete CD28, CD46 — Close to JDDRH.1

CD47 0.1U_0402_10V7K — D2/20 Delete CD28, CD46 — Close to JDDRH.126

CD49 0.1U_0402_10V7K

RD15 10K_0402_5%

RD10 1K_0402_1%

RD11 1K_0402_1%

RD12 1K_0402_1%

RD13 1K_0402_1%

11/28 Move RD10, RD11 to page 12

DDR_B_DQS#[0..7]
DDR_B_DQS[0..7]
DDR_B_D[0..63]
DDR_B_MA[0..15]

SM_DRAMRST# 7,11

PM_SMBDATA 11,17,26,33
PM_SMBCLK 11,17,26,33

DDRB_CKE0 7
DDRB_CKE1 7
DDR_B_BS2 7
DDR_B_BS0 7
DDR_B_WE# 7
DDR_B_CAS# 7
DDRB_SCS1# 7
DDRB_CLK0 7
DDRB_CLK0# 7
DDRB_CLK1 7
DDRB_CLK1# 7
DDR_B_BS1 7
DDR_B_RAS# 7
DDRB_SCS0# 7
DDRB_ODT0 7
DDRB_ODT1 7

+VREF_CAB

LCN_DAN06-K4806-0102
Conn@

SPD setting (SA0, SA1)
PU/PD by Channel A/B
->Channel A 00
->Channel B 01

Layout Note:
Place near JDDRH

Layout Note: Place these 4 Caps near Command and Control signals of DIMMB

CD31 2_47U_0805_6.3V6M
CD41 2_10U_0603_6.3V6M
CD36 2_10U_0603_6.3V6M
CD37 2_10U_0603_6.3V6M
CD38 2_10U_0603_6.3V6M
CD39 2_10U_0603_6.3V6M
CD40 2_10U_0603_6.3V6M

11/28 Change CD31 47U 1206 to 0805 size (SE000009PL00)

CD33 2_0.1U_0402_10V7K
CD29 2_0.1U_0402_10V7K
CD30 2_0.1U_0402_10V7K
CD32 2_0.1U_0402_10V7K

Layout Note:
Place near JDDRH.203 and 204

CD45 2_1U_0402_6.3V6K
CD42 2_1U_0402_6.3V6K

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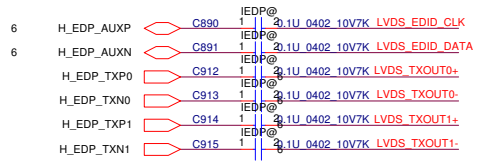
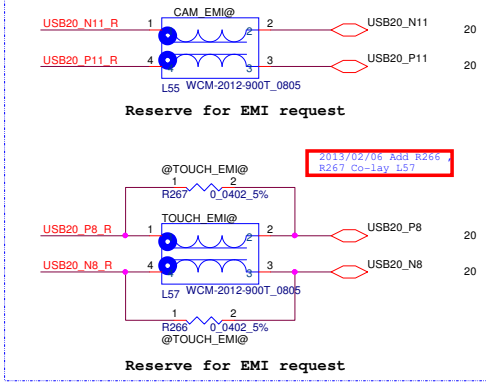
For eDP Panel

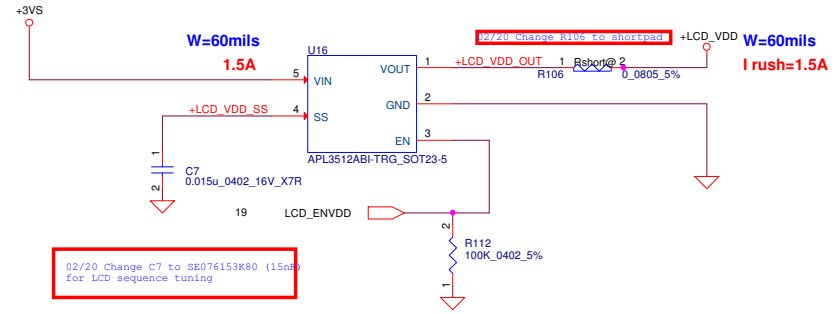




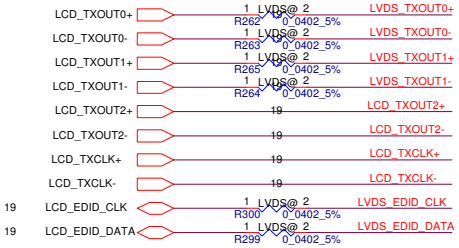
LCD POWER CIRCUIT

Need check eDP&LVDS both 3V power rail.

Reserve for power consumption
Remove on PVT phase



For LVDS 1ch Panel



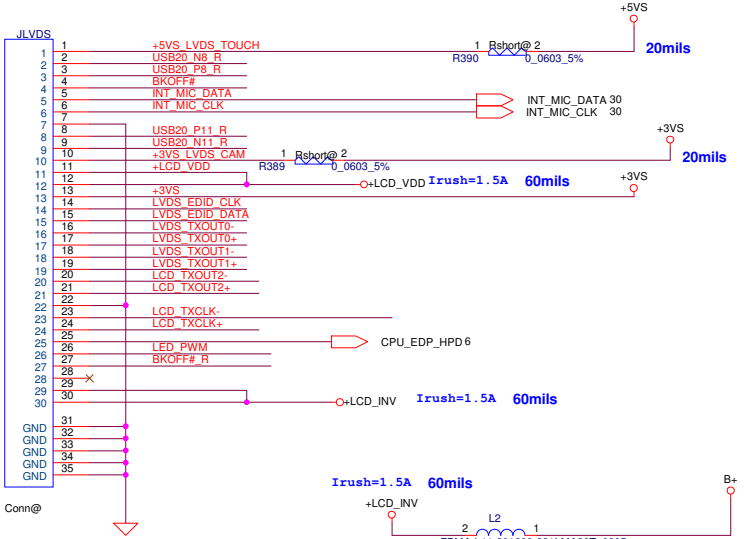
LVDS colay eDP cable

Pin define will be change after ME ready

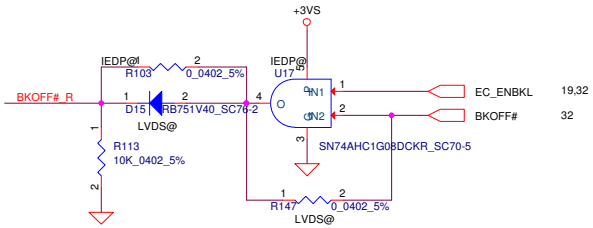
pin1-4 Touch function for panel

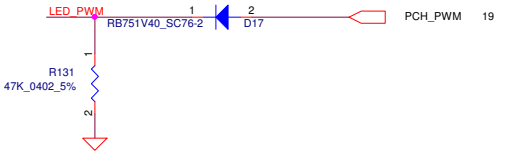
pin5-10 For Webcam with single or dual MIC

pin11-30 For LVDS or EDP panel



Reserve for eDP panel potential issue





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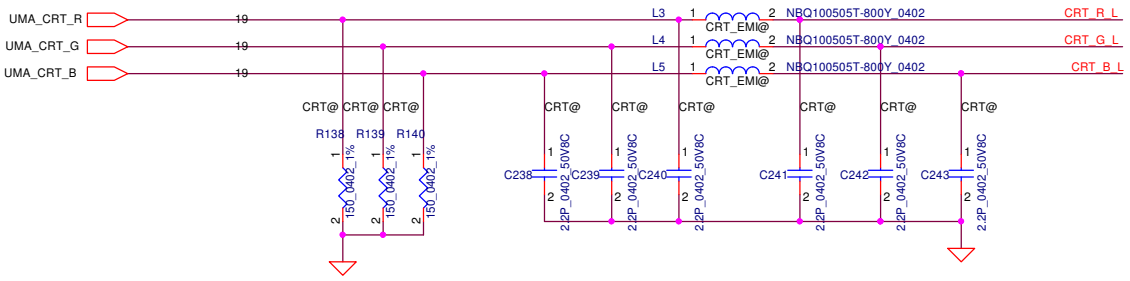
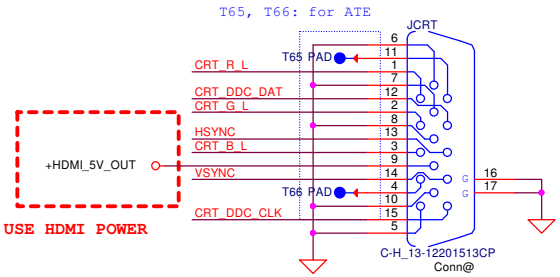
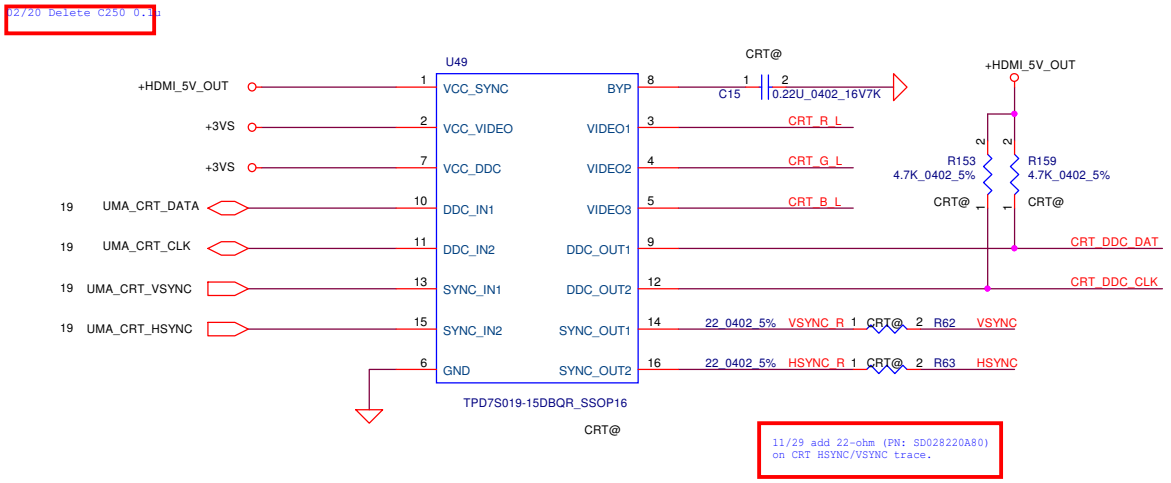
CRT CONNECTOR







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Compal Electronics, Inc.

Title: **CRT**

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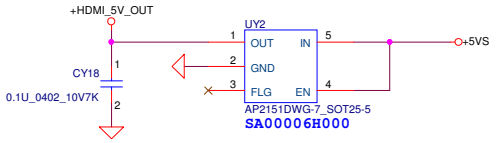
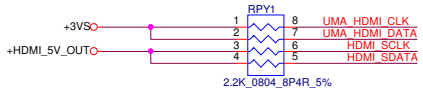
OE#	A	Y
L	L	L
L	H	H
H	X	Z

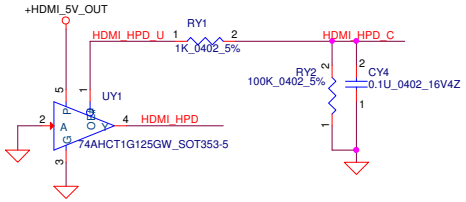
HDMI POWER CIRCUIT

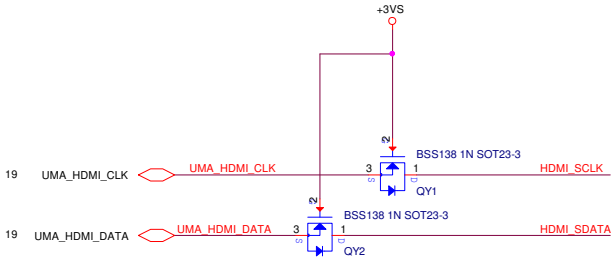
VIN = 5V, IOUT = 0.5A , RDS(ON) TYP=95m ; MAX=115m
Current Limit: TYP=0.8A ; MAX=1A



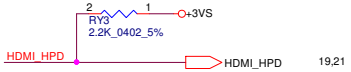
11/28 Update HDMI current limited IC from AP230W-7 to AP2151DDWG-7.



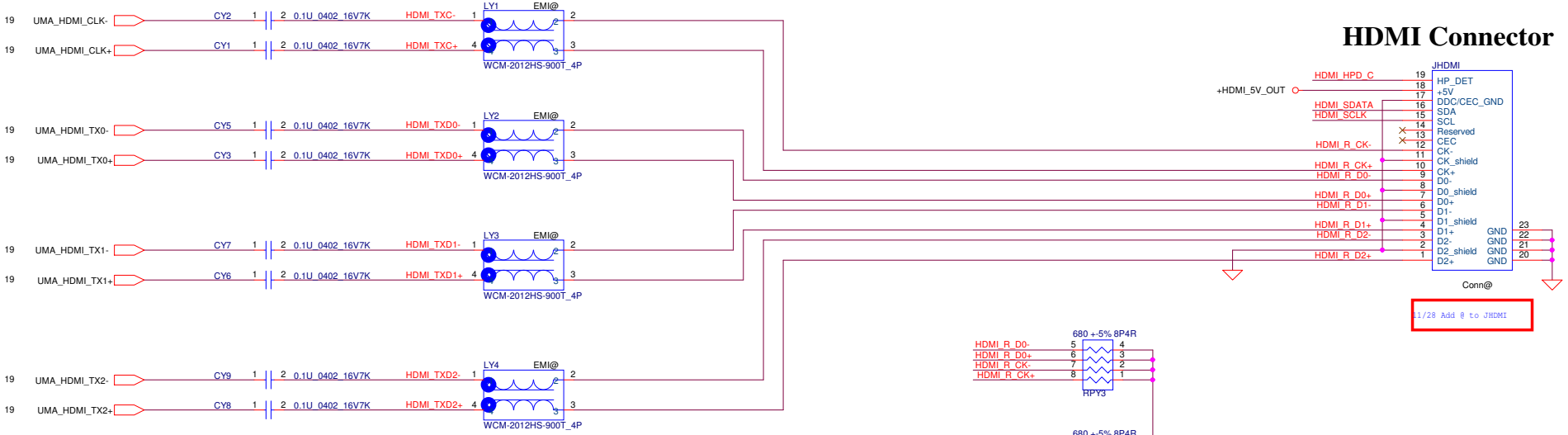




2013/02/06 change QY1 QY2 to SB00000PF00 for X1 code

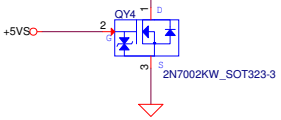


HDMI Connector

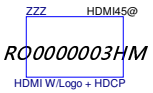


11/28 Add @ to JHDMI

12/04 SWAP RPY4 netname



HDMI Royalty



10/18 Modify the BOM structure @ to HDMI45@ , change Location HDMI to ZZZ.

HDMI W/O Logo: RO0000001HM
HDMI W/Logo: RO0000002HM
HDMI W/Logo + HDCP: RO0000003HM

please manually load
this virtual material to 45@ BOM

Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.	
Title	HDMI Conn.
Document Number	VFKTA
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Date:	Monday, March 11, 2013
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CMOS Setting, near DDR Door

iME Setting.

Integrated SUS 1.05V VRM Enable

PCH_INTVRMEN	High - Enable Internal VRs (must be always pulled high)

PCH_SPKR
High = Enabled "No Reboot Mode"
*Low = Disabled (Default)

HDA_SDO
ME debug mode,
this signal has a weak internal pull down
*Low = Disable (default)
High = Enable (flash descriptor security overide)

HDA_SYNC
*This signal has a weak internal pull down
H=>On Die PLL is supplied by 1.5V
L=>On Die PLL is supplied by 1.8V
Need to pull high for Chief River Mobile platform

Placement near to YH1

Change Net name due to this function is high active

HDD

ODD

BOOT BIOS Strap Bit 0

SPI ROM for BIOS & ME (4MByte)

SPI ROM for Win8 (2MByte)

4MB ROM P/N:
SA00003K800
SA00004LI00

2MB ROM P/N:
SA000041N00
SA00003FO10

Socket: SP07000F500/SP07000H900
Please place UH3 & UH4 close to UH1 PCH,
please place RH66, RH67, RH68 near UH3
Please place RH267 near RH66, Please place RH271 near RH67,
Please place RH269 near RH68.

Reserve for NPCE885N EC

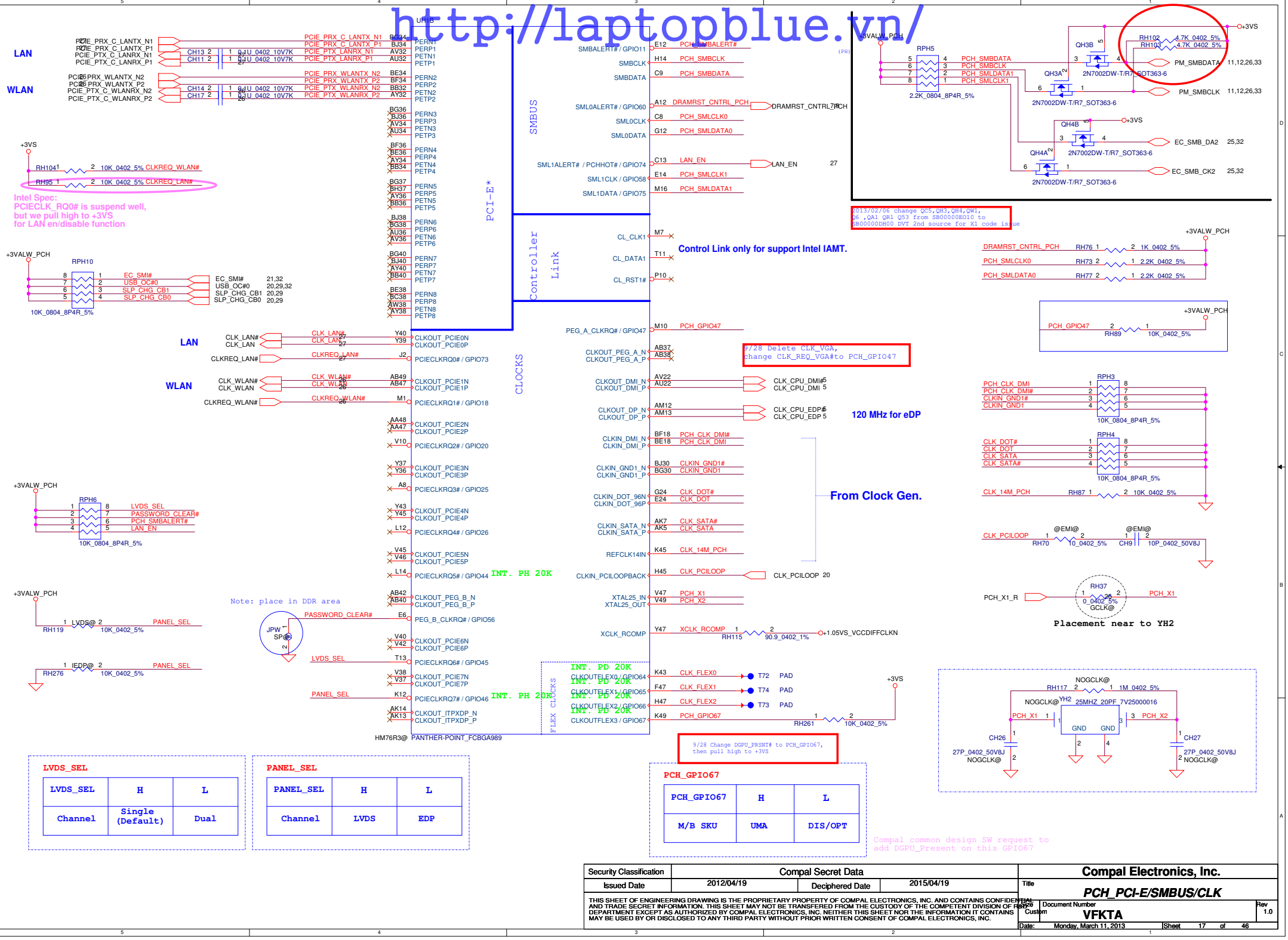
Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

Title: PCH_HDA/JTAG/SATA/SPI/LPC

Size: Custom | Document Number: VFKTA | Rev: 1.0

Date: Monday, March 11, 2013 | Sheet 16 of 46



LVDS_SEL

LVDS_SEL	H	L
Channel	Single (Default)	Dual

PANEL_SEL

PANEL_SEL	H	L
Channel	LVDS	EDP

PCH_GPIO67

PCH_GPIO67	H	L
M/B SKU	UMA	DIS/OPT

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/19	Deciphered Date 2015/04/19	Title: PCH_PCI-E/SMBUS/CLK
			Size: Custom; Document Number: VFKTA; Rev: 1.0
			Date: Monday, March 11, 2013; Sheet 17 of 46

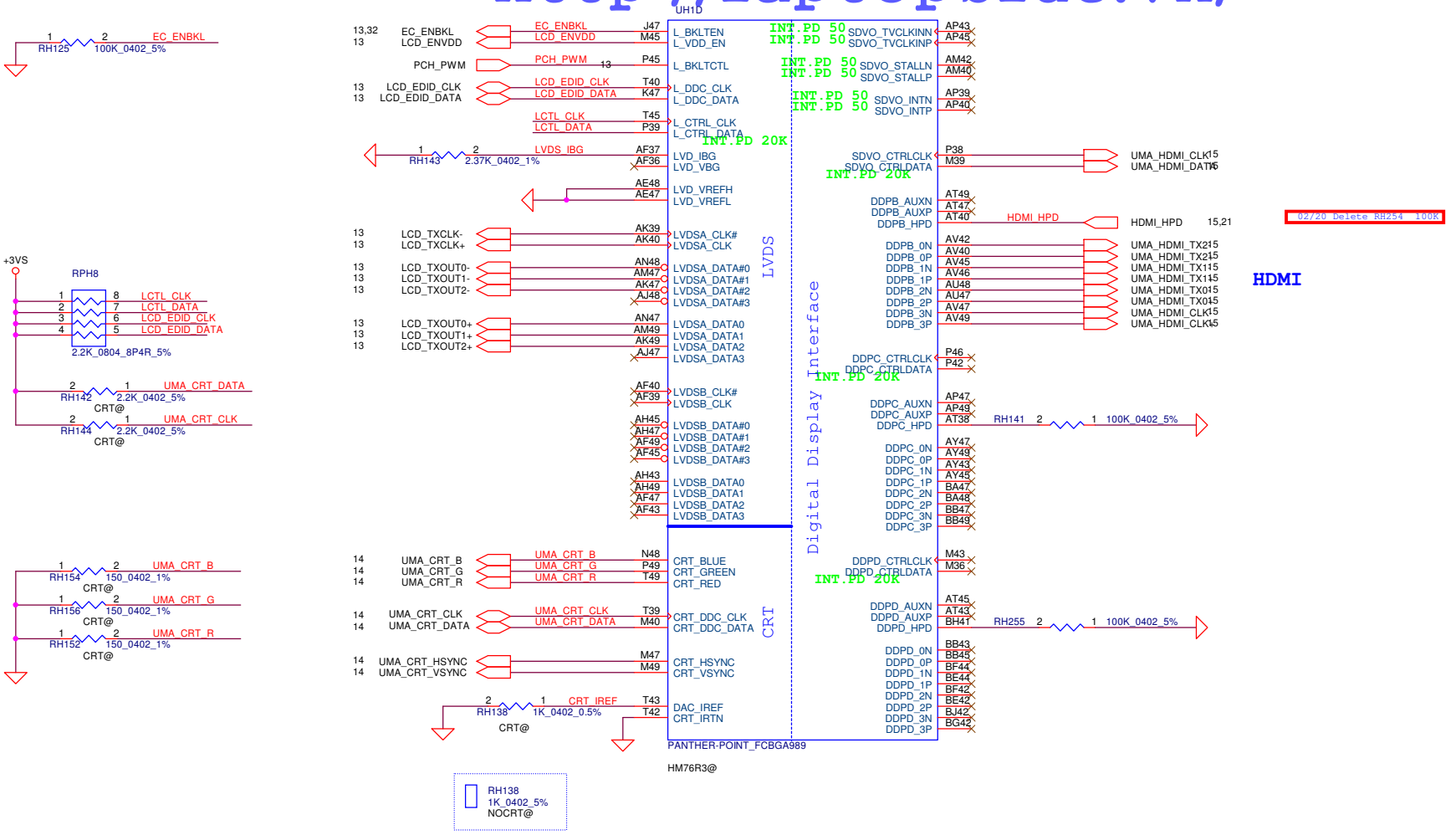
Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

Title: *PCH_DMI/FDI/PM*

Size	Document Number	Rev
Custom	VFKTA	1.0

Date: Monday, March 11, 2013 Sheet 18 of 46



Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

Title: ***PCH_CRT/LVDS/HDMI***

Size	Document Number	Rev
Custom	VFKTA	1.0

Date: Monday, March 11, 2013 Sheet 19 of 46

UH1E

RSVD

PCI

USB

EHCI 1

EHCI 2

PANTHER-POINT_FCBGA989
HM76R3@

Note: HM70 only enable
USB port 0, 1, 2, 3, 8, 9, 10, 11

USB-Right1
USB-Right2
USB-Left
CardReader
Touch Screen
BT
NFC
Int. Camera
USB-Right Rear
USB-Right Front
USB-Left

Within 500 mils

10/24B PLT_RST# Add RH173 100K Pull Down to GND

9/28 Delete PLTRST_VGA# Circuit

Intel Anti-Theft Techonlogy

NV_ALE	High=Endabled
	Low=Disable(floating) *

10/18B Add USB port 10 for NFC

11/28 Delete NFC Function

9/28 change DGPU_RST#/ DGPU_PWR_EN to PCH_GPIO50/54, then PCH_GPIO50 8.2k pull high to +3vs

2013/02/28change RH167 pin2 netname from CLK_EC_R to CLK_PCI_EC_R
2013 back to CLK_EC_R as the same for DIS

2012/10/19A Change RH166 to short pad
2013/02/06 PVT change back to 0 ohm again

11/30 Move PLT_RST# ESD capacitor (CH104) to EC side (CB13) and mount 0.1u for ESD request

10/18 Need confirm PCH_GPIO55, 10/19A remove RH295

OC#1 PH @ page 26
CB0 PH @ page 27

Boot BIOS Strap

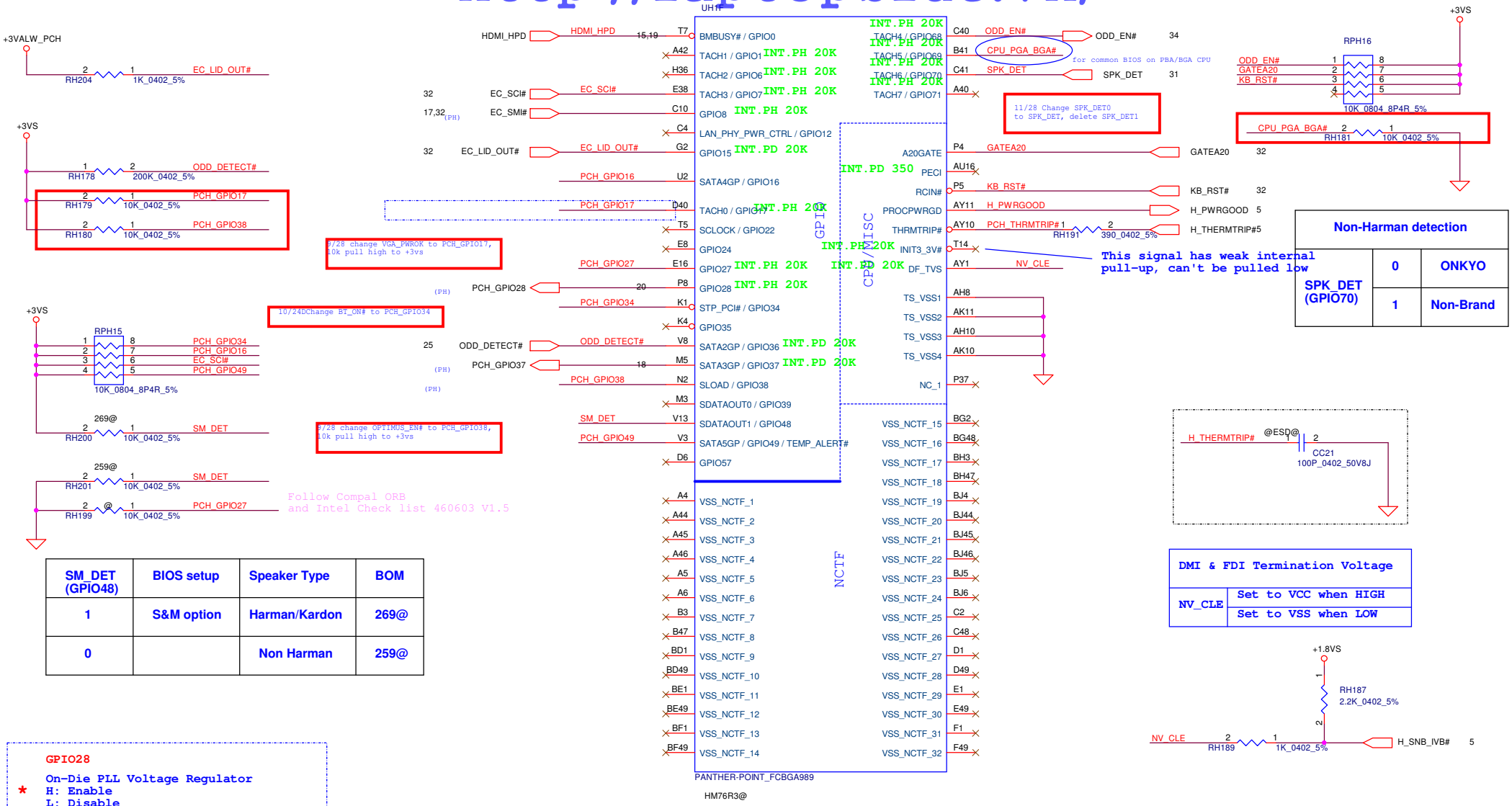
PCH_GPIO51	PCH_GPIO19	Boot BIOS Loaction
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI *

A16 Swap Override Strap

WL_OFF#	*	Low= A16 swap override Enable High= A16 swap override Disable

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/19	Deciphered Date 2015/04/19	Title: PCH_PCI/USB/NAND

Size: Custom	Document Number: VFKTA		Rev: 1.0
Date: Monday, March 11, 2013	Sheet 20 of 46		



SM_DET (GPIO48)	BIOS setup	Speaker Type	BOM
1	S&M option	Harman/Kardon	269@
0		Non Harman	259@

Non-Harman detection		
SPK_DET (GPIO70)	0	ONKYO
	1	Non-Brand

DMI & FDI Termination Voltage	
NV_CLE	Set to VCC when HIGH
	Set to VSS when LOW

GPIO28

On-Die PLL Voltage Regulator
* H: Enable
L: Disable

GPIO8

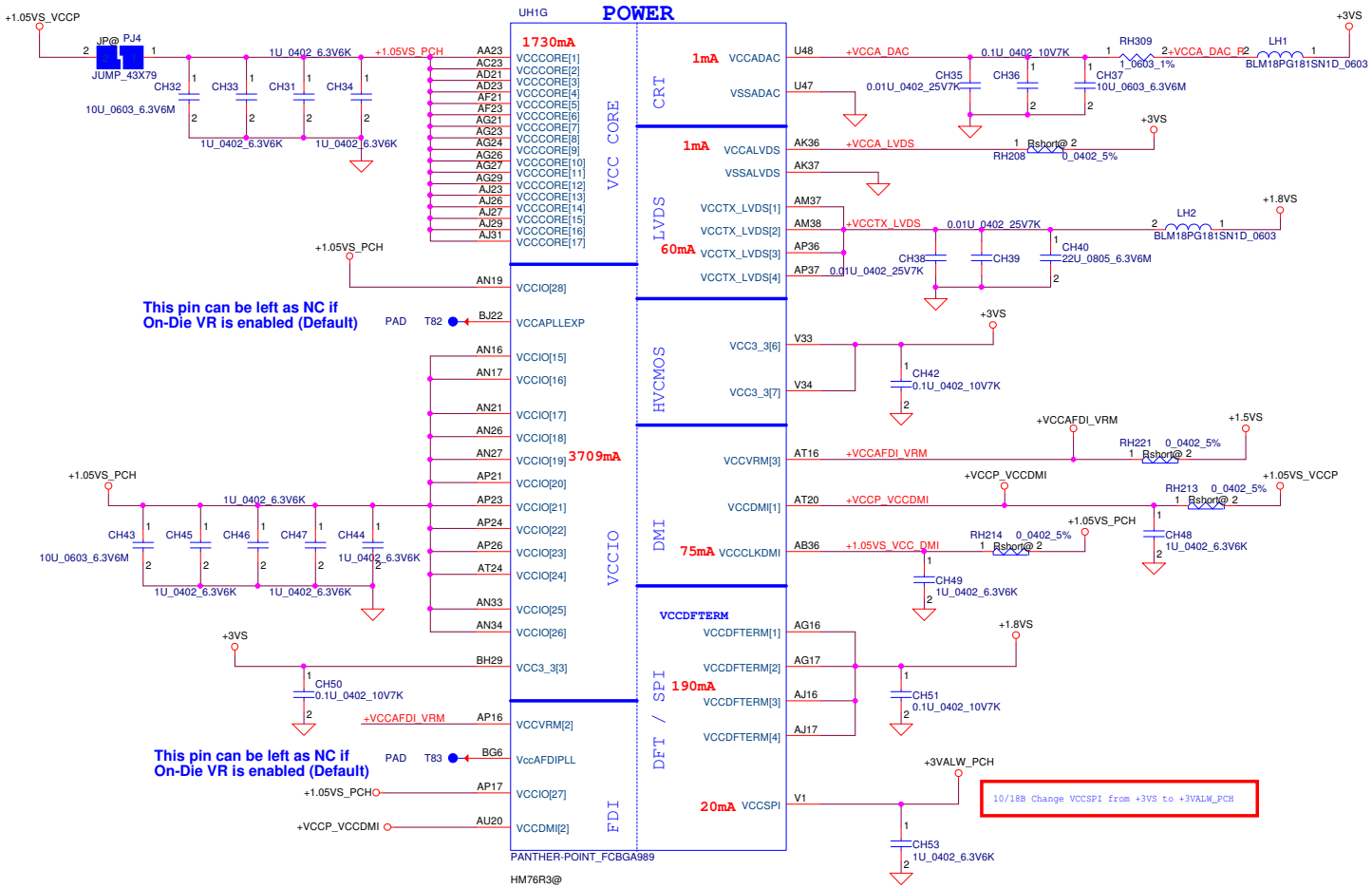
Integrated Clock Chip Enable (Removed)
H: Disable
* L: Enable

Integrated clock enable functionality is achieved by soft-strap
The current default is clock enable

OPTIMUS_EN#

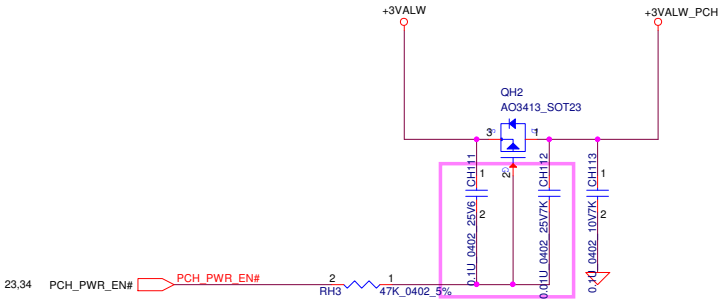
OPTIMUS_EN#	H	L
SKU	NonOPT	Optimus

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/19	Deciphered Date 2015/04/19	Title: PCH_CPU/GPIO
			Size: B; Document Number: VFKTA; Rev: 1.0
			Date: Monday, March 11, 2013; Sheet 21 of 46



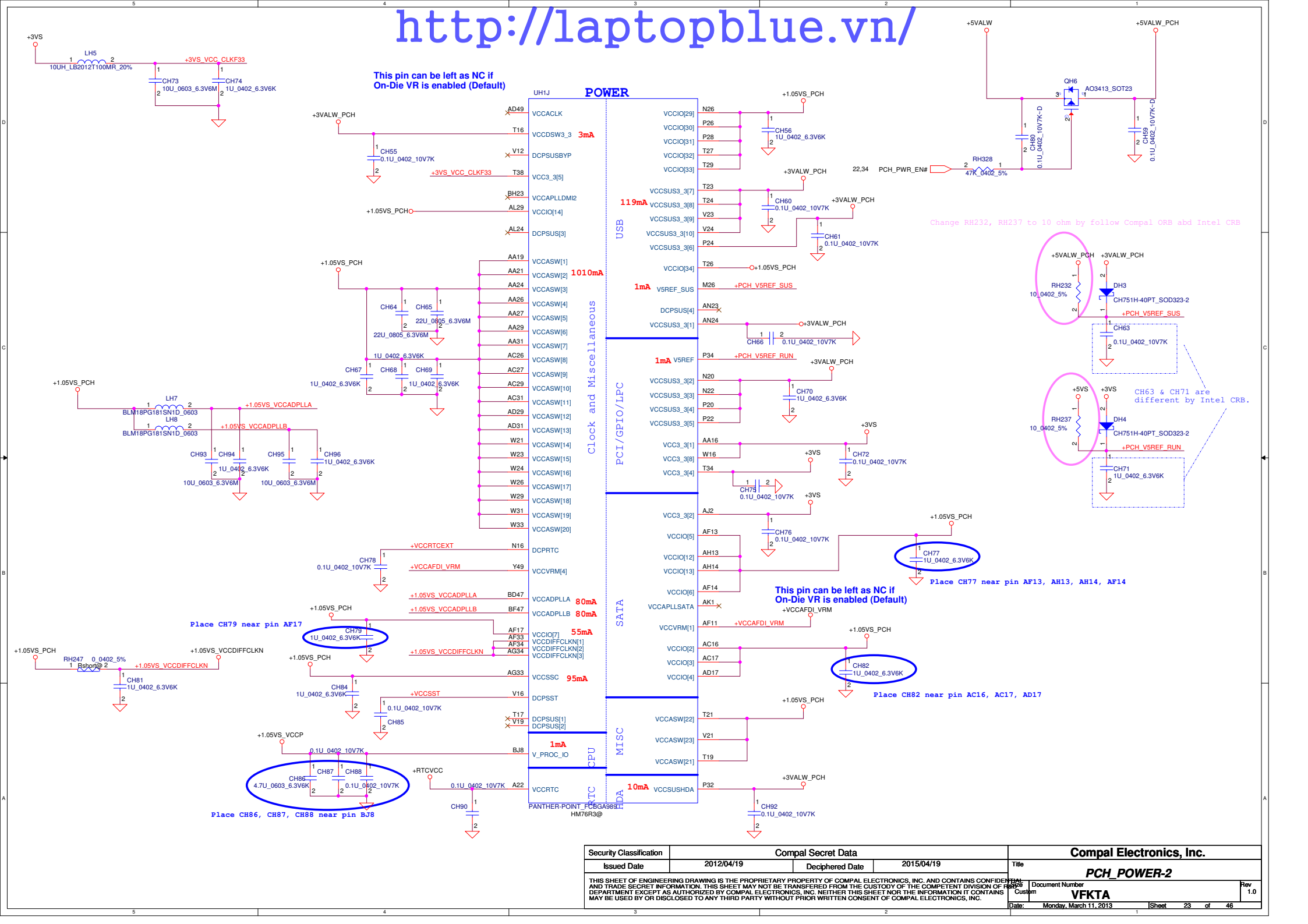
PCH Power Rail Table Refer to PCH EDS R1.0		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.1	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	N/A
VccSus3_3	3.3	0.095
VccSusHDA	3.3	0.01
VccVRM	1.5	0.167
VccCLKDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

+3VALW to +3VALW_PCH



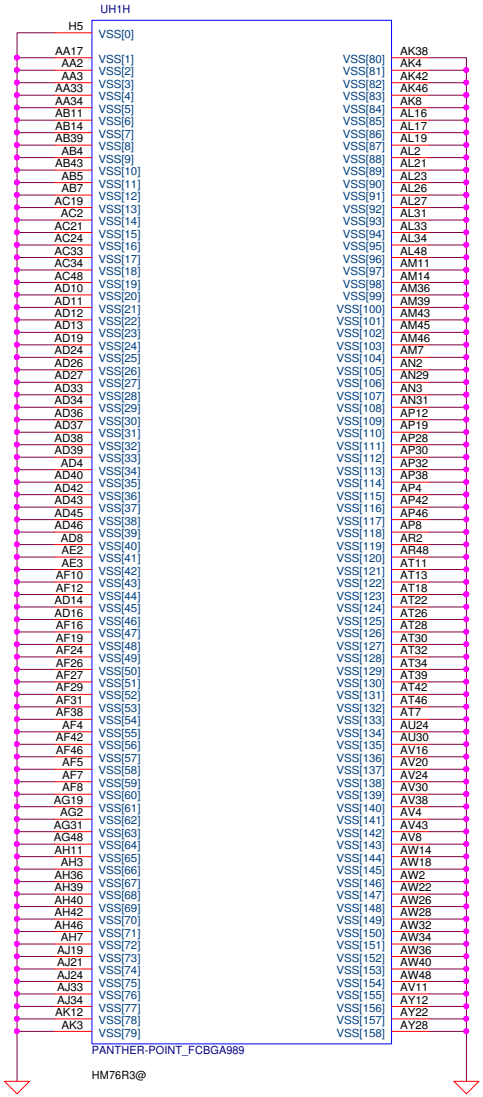
Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

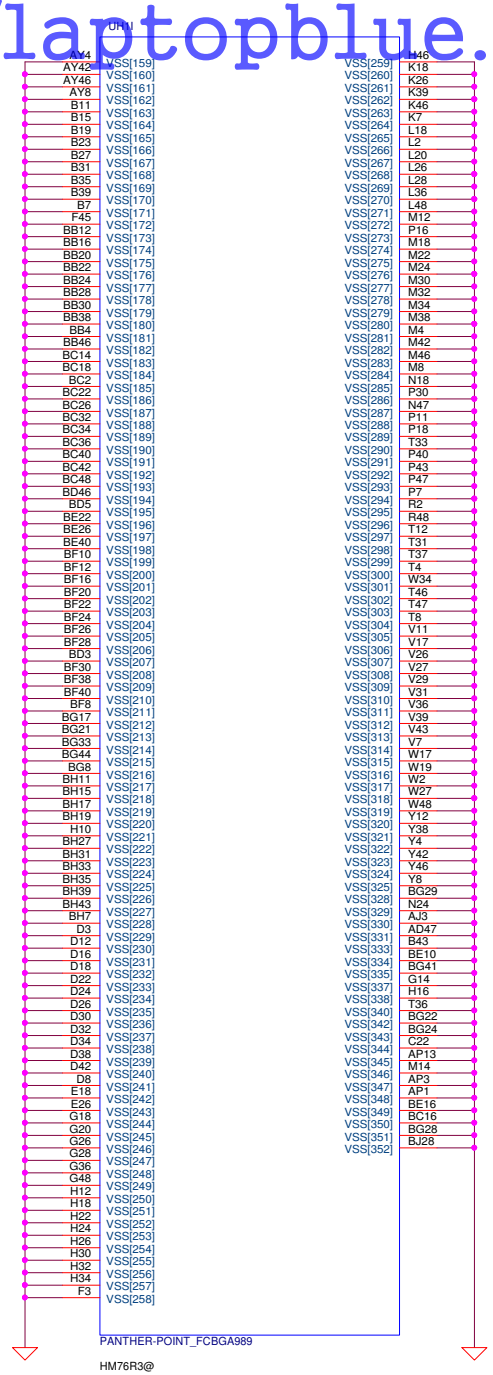
Compal Electronics, Inc.			
Title	PCH_POWER-1		
Size	Document Number		Rev
Custom	VFKTA		1.0
Date:	Monday, March 11, 2013	Sheet	22 of 46



Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.			
Title	PCH_POWER-2		
Size	Custom	Document Number	VFKTA
Rev	1.0		
Date:	Monday, March 11, 2013	Sheet	23 of 46





Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

Title: ***PCH_GND***

Size	Document Number	Rev
Custom	VFKTA	1.0

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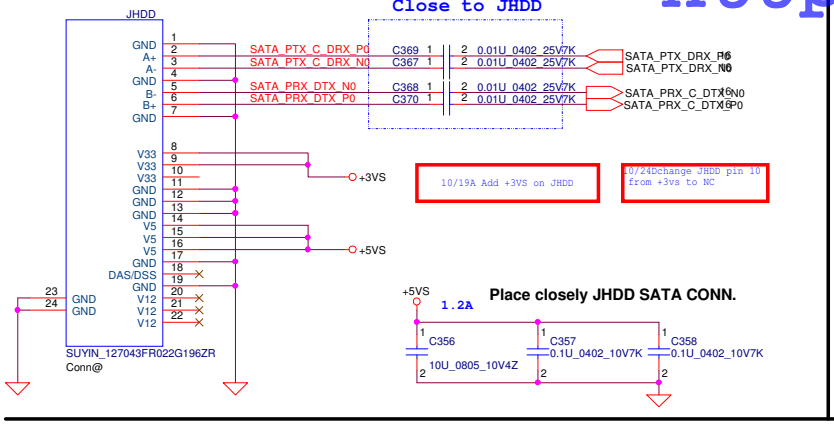
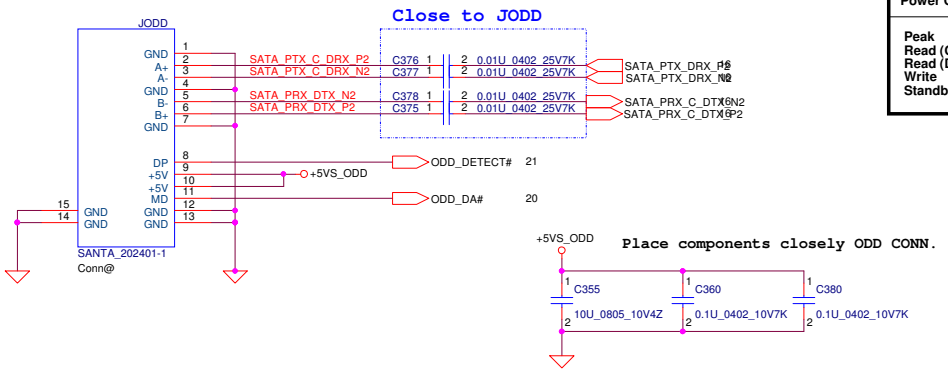
SATA HDD Conn.



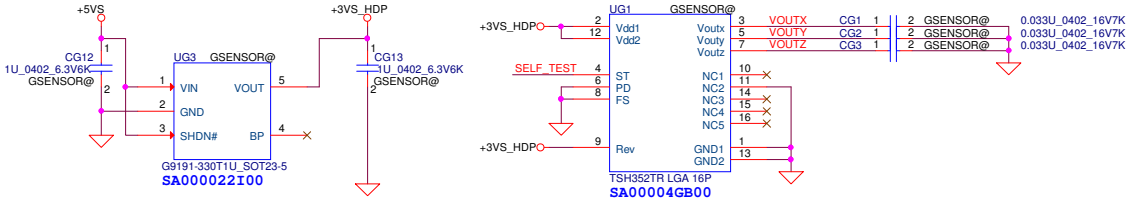
SATA ODD Conn

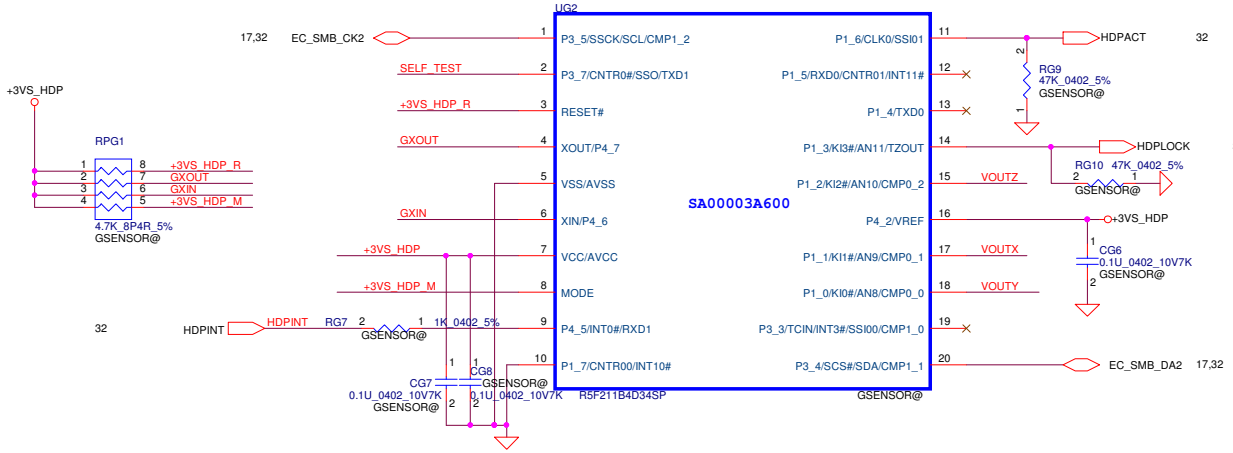


Power Consumption

Peak	1800 mA
Read (CD)	1100 mA
Read (DVD)	950 mA
Write	1300 mA
Standby	20mA

G-Sensor





Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

Title: **HDD/ODD/G-Sensor**

Size: C | Document Number: VFKTA | Rev: 1.0

Date: Monday, March 11, 2013 | Sheet 25 of 46

Slot 1 Half PCIe Mini Card-WLAN

+3V_WLAN 40 mils

0.1U_0402_10V7K

CM1 CM2 CM3

0.1U_0402_10V7K 4.7U_0603_6.3V6K

10/24 Remove +1.5VS on WLAN pin6/28/48, delete CM7, CM8 Delete RM22 (EC will programming H/L)

Reserve +1.5 power rail & cap. to supoort unknown keypart.

WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_ON	H	L

10/24D Delete QM1, change BT_ON design

From 32 BT_ON — BT_ON 1 RM27 2 E51_RXD 1K_0402_5%

For isolate BT_ON and Compal Debug Card.

10/24Dchange RM24 pin1 netname from BT_CTRL to BT_ON

To EC (Need pull-up +3VL) 32

WLAN_WAKE#

BT_ON 1 RM24 2 BT_CTRL_R @0_0402_5%

17 CLKREQ_WLAN#

To PCH 17 CLK_WLAN#

17 CLK_WLAN

To PCH PCIE_PRX_WLANTX_N2

PCIE_PRX_WLANTX_P2

WLAN/ WiFi

To PCH PCIE_PTX_C_WLANRX_N2

PCIE_PTX_C_WLANRX_P2

+3V_WLAN

32 E51_TXD

32 E51_RXD

Debug card using

JWLAN

LOTES_AAA-PCI-049-P06-A

Conn@

WL_OFF# PLT_RST#

To EC WL_OFF# 32

PLT_RST# 5,20,27,32

To PCH

PM_SMBCLK 11,12,17,33

PM_SMBDATA 11,12,17,33

USB20_N9 20

USB20_P9

WiMax/ BT

LED_WIMAX# LED_WIMAX# 33

RM6 100K_0402_5%

+3VS

+3VALW TO +3V_WLAN for WOWL

10/24Dchange RM31 to 10K, Add RM2

+3VALW

RM31 10K_0402_5%

WOWL@

To EC WOWL_EN#

47K_0402_5% RM30

RM2 100K_0402_5%

WOWL@ CM9 0.1U_0402_10V7K

WOWL@ CM10 0.01U_0402_25V7K

AO3413_SOT23 QM2

Vgs=-4.5V,Id=3A,Rds<97mohm

Need short PJ3 if system don't support WOWL

+3V_WLAN

RM1 0_0402_5% NOWOWL@

+3VS

10/24 Change PJ3 to RM1 and add BOM structure *NOWOWL@*

+3VL +1.05VS_VCCP +3VALW

0.1U_0402_10V7K

02/20 Delete CCL2, RCL5

CCL1 GCLK@ CCL3 GCLK@ CCL8 GCLK@

10/24 10/24 Change CCL2 to @

UCL1 GCLK@

+3VALW +3VL

+1.05VS_VCCP

VDD +V3.3A

VDDIO_25M_A VDDIO_25M_B

XTAL_IN XTAL_OUT

VBAT NC

32K NC

25M_B 25M_A

VSS VSS VSS Thermal Pad

VDD_RTC_OUT

SLG3NB244VTR_TQFN16_2X3

CCL14 22U_0805_6.3V6M GCLK@

for safety request

RCL4 120_0603_5% GCLK@ +RTC

PCH_RTCX1_R 16

CLK_X1 CLK_X2

PCH_X1_R_R

CCL13 2.2U_0402_6.3V6M GCLK@

PN: SA000057I00

GCLK@ YCL1 25MHZ 12PF X3G025000DK1H-X

CLK_X1 GND GND CLK_X2

CCL9 18P_0402_50V8J GCLK@

CCL12 18P_0402_50V8J GCLK@

10/19A Change RCL2 to short pad

02/20 Delete RCL2 LAN_X1_R_R, LAN_X1_R

PCH_X1_R_R 1 RCL1 Reboot@ 2 0_0402_5% PCH_X1_R 17

Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

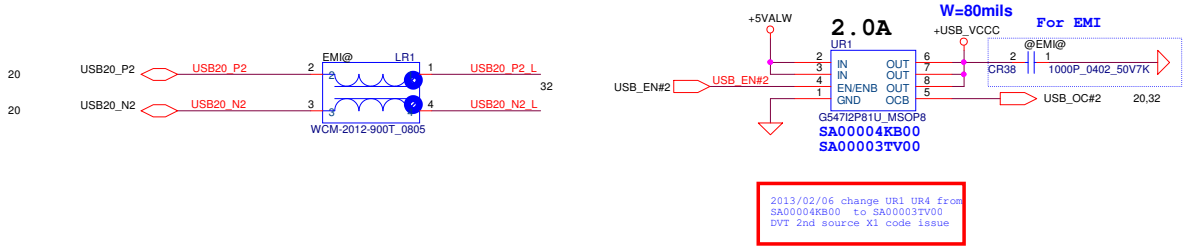
Compal Electronics, Inc.

Title: WLAN/GCLK

Size | Document Number: VFKTA | Rev: 1.0

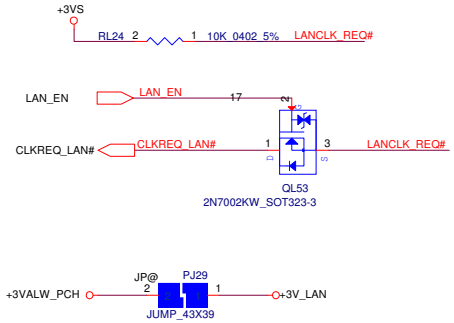
Date: Monday, March 11, 2013 | Sheet 26 of 46

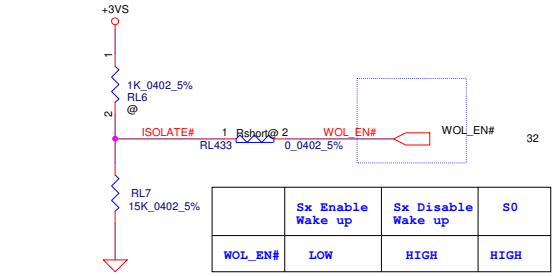
Left USB 2.0 x 1



2013/02/06 change UR1 UR4 from SA00004KB00 to SA00003TV00 DVT 2nd source X1 code issue

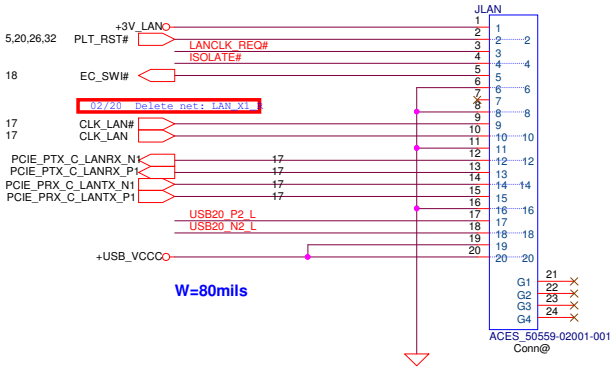
For LAN function





	Sx Enable Wake up	Sx Disable Wake up	S0
WOL_EN#	LOW	HIGH	HIGH

10/24 Add note for WOL_EN# S0 status



10/16 Swap JLAN pin define due to FFC fold

+3V_LAN rising time (10%~90%) need > 1ms and <100ms.

LAN	WOL	LAN_EN S0	LAN_EN Sx	ISOLATEB S0	ISOLATEB Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

*
S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms

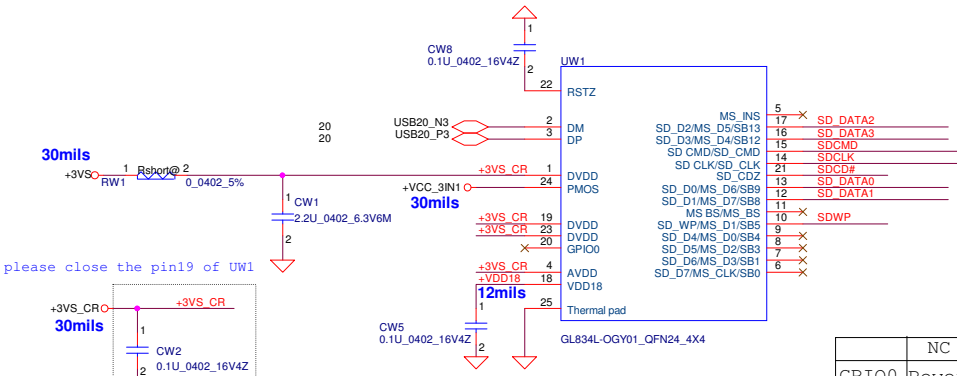
Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

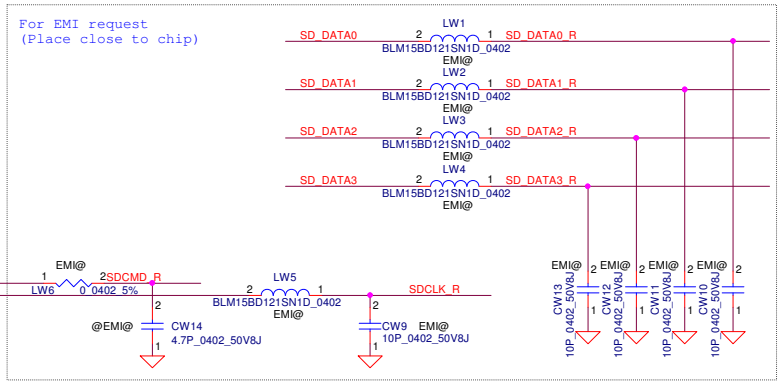
Compal Electronics, Inc.

Title: LUSB20/LAN conn.

Size: Custom | Document Number: VFKTA | Rev: 1.0

Date: Monday, March 11, 2013 | Sheet 27 of 46

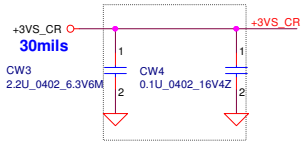




please close the pin19 of UW1

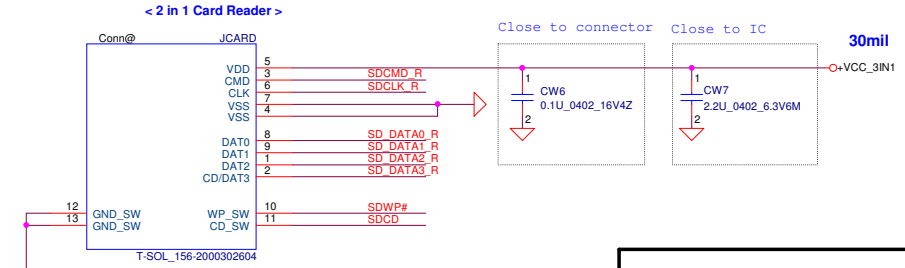
	NC (default)	10K pull down
GPIO0	Power saving mode	Normal mode

please close the pin4 of UW1



De-coupling and Bulk capacitor should place near to Cardreader chip and Combo Socket

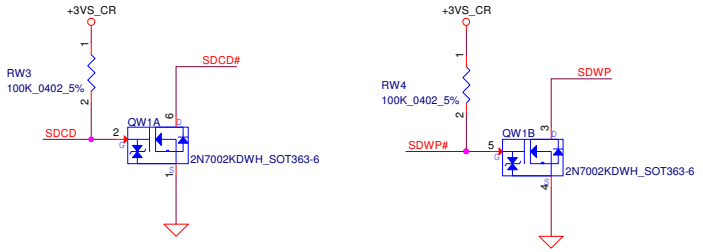
< 2 in 1 Card Reader >



"Normal Close" type connector

	CD_SW	WP_SW	
		Protect disable	Protect Enable
Card Uninsertion	Close	Close	Close
Card Insertion	Open	Open	Close

For normal close type connector invert circuit



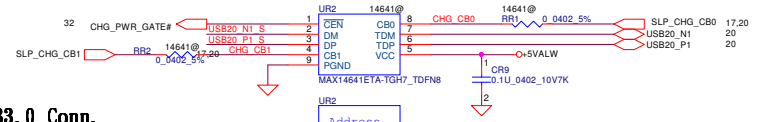
Security Classification	Compal Secret Data		
Issued Date	2012/10/26	Deciphered Date	2013/10/26

Compal Electronics, Inc.			
Title	USB-CardReader GL834L		
Size: Custom	Document Number: VFKTA		Rev: 1.0
Date: Monday, March 11, 2013	Sheet 28 of 46		

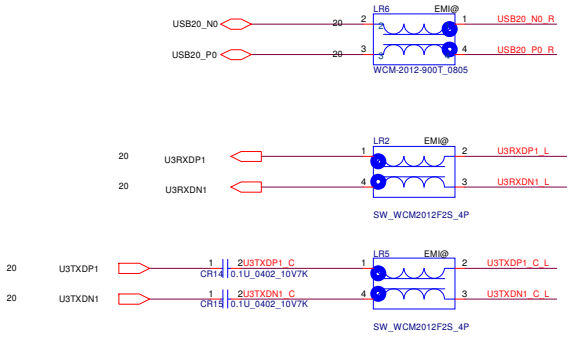
USB Sleep & Charge

State table for MAX14641			
CB0	CB1	Mode	STATUS
0	0	AM2	2A auto-detection charger mode for Apple device. Resistor dividers are connected to DP/DM. Including DCP
0	1	AP1	Forced 1A charger mode for Apple devices. Resistor dividers are connected to DP/DM.
1	0	PM	USB pass-through mode.DP/DM are connected to TDP/TDM
1	1	CM	USB pass-through mode with CDP emulation. Auto connects DP/DM to TDP/TDM depending on CDP detection status.

12/05 S&C IC Pin1 was connected to the EC(GPIO49) Pin82.



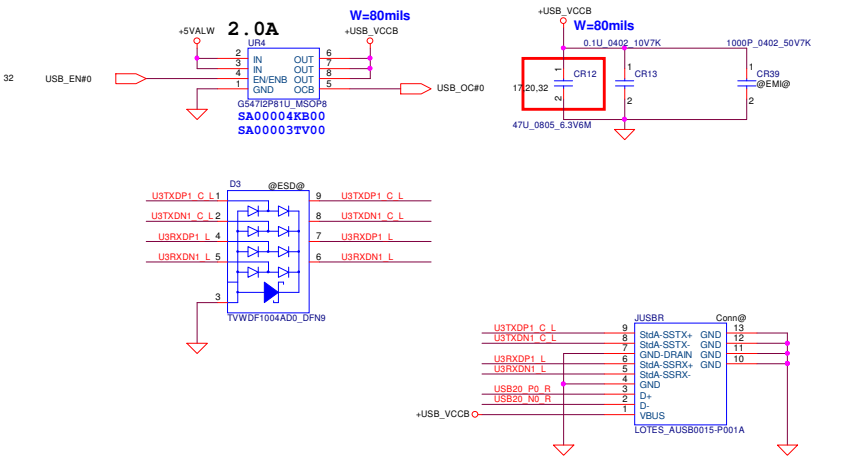
Right rear USB3.0 Conn.



2013/02/06 change LR2,LR3,LR4,LR5 from SM070001U00 to SM070001R00 DVT 2nd source for X1 code issue

02/22 SWAP CR16 pin1 U3TXDN2 to CR17 pin1 U3TXDP2

2013/02/06 change UR1 UR4 from SA00004KB00 to SA00003TV00 DVT 2nd source X1 code issue



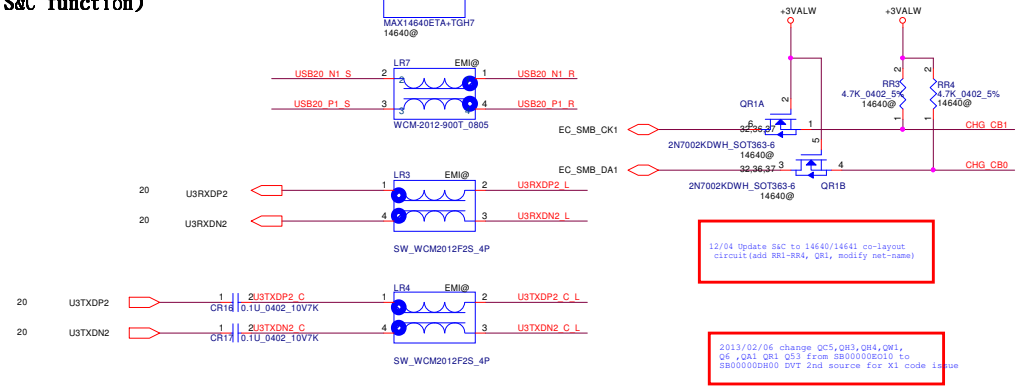
10/22A ESD request Delete DR1, DR2

11/28 Change CR10, CR12 from 47u 1206 to 0805 size (SE00000PL00)

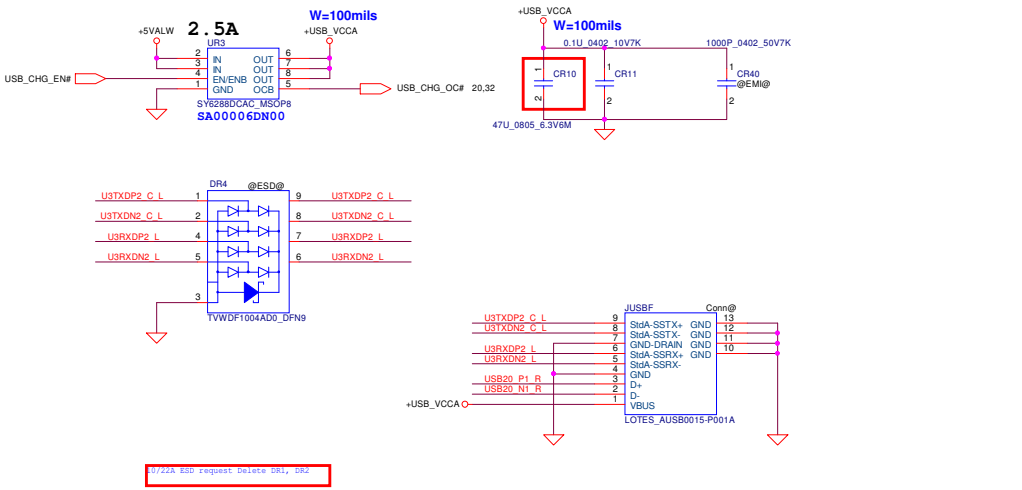
02/20 Delete CR7, CR8

Right front USB3.0 Conn. (Support S&C function)

12/04 Update S&C to 14640/14641 co-layout circuit(add RR1-RR4, QR1, modify net-name)



2013/02/06 change QC5,QH3,QR4,QW1, Q6 ,QA1 QR1 Q53 from SB00000EO10 to SB00000DH00 DVT 2nd source for X1 code issue



10/22A ESD request Delete DR1, DR2

Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

Title: RUSB30/S&C

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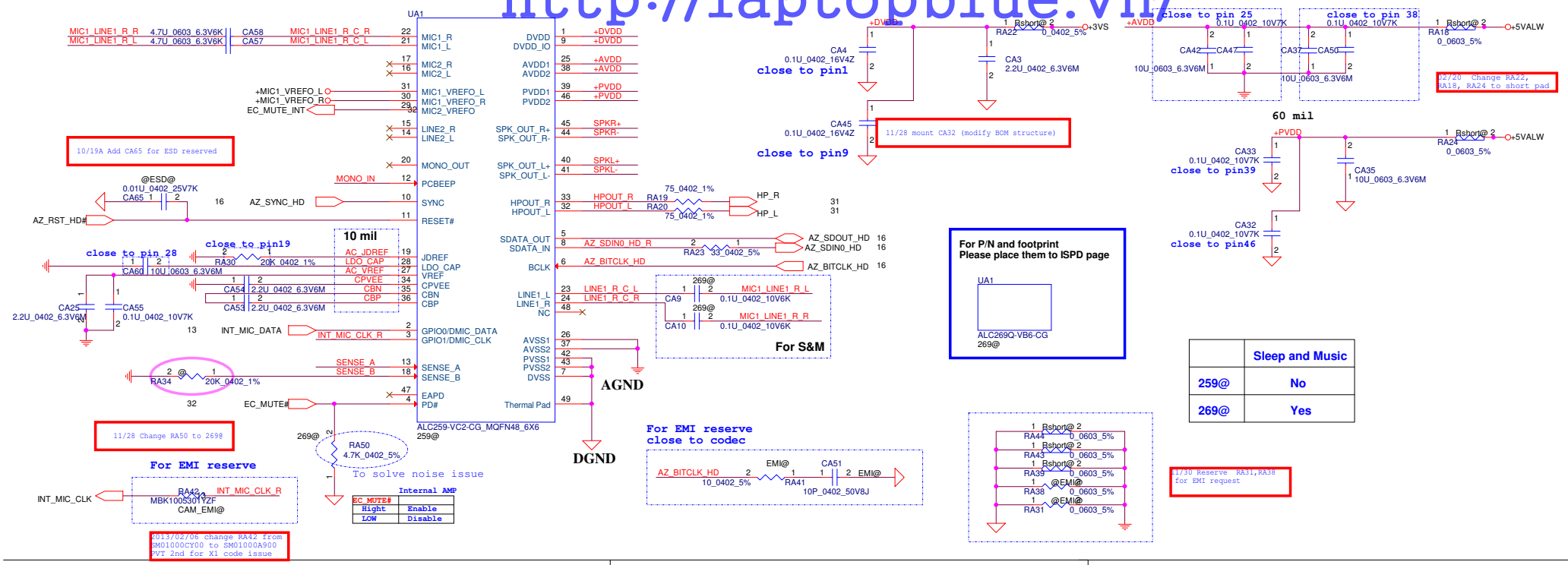
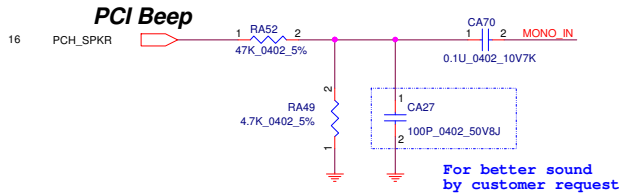


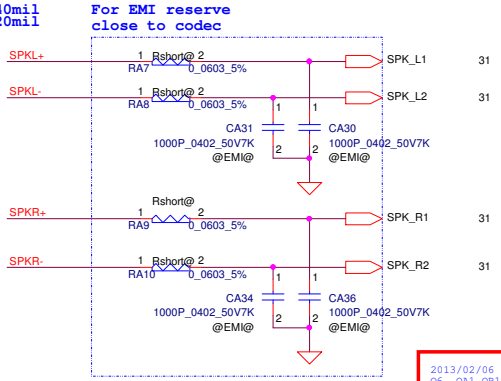
	Sleep and Music
259@	No
269@	Yes

Beep sound

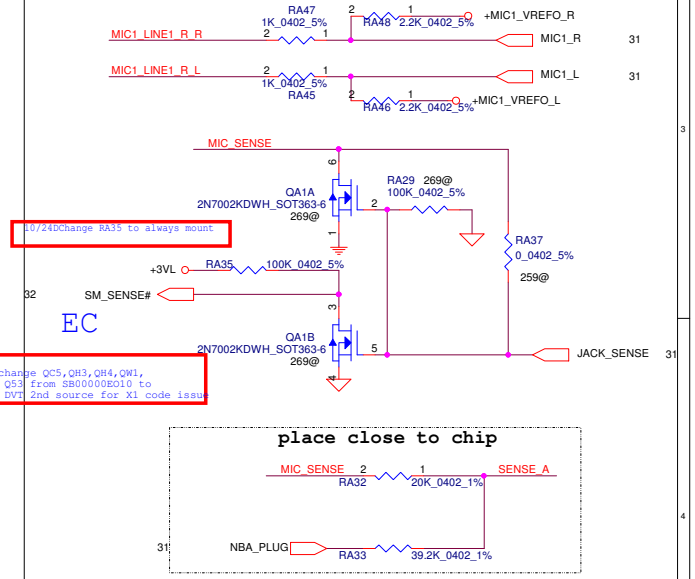


SPK

2W 4ohm =40mil
1W 8ohm =20mil



MIC/LINE IN



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

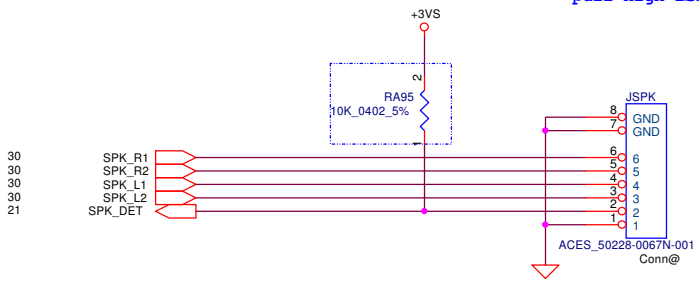
Title: HDA-ALC259-VC/269-VB

Size: Custom | Document Number | Rev

Date: Monday, March 11, 2013 | Sheet 30 of 46

SPK Conn.

For common design,
pull-high resistor should be placed at connector side.



10/19A Follow the latest connector list to change SPK footprint, The ME drawing with new JSPK will be updated 10/20

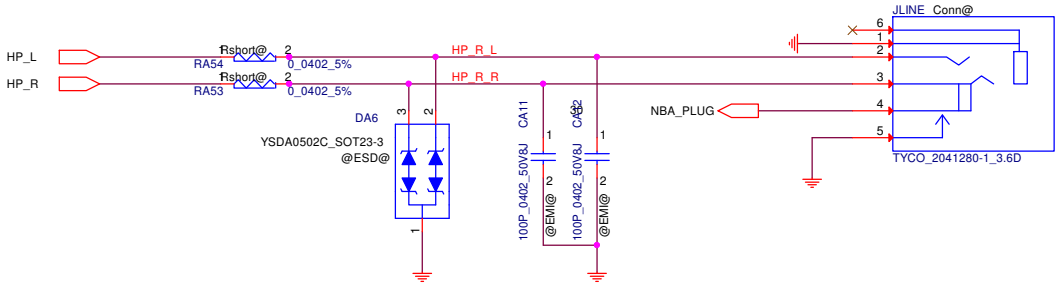
SM_DET (GPIO48)	BIOS setup	Speaker Type	BOM
1	S&M option	Harman/Kardon	269@
0		Non Harman	259@

Non-Harman detection		
SPK_DET (GPIO70)	0	ONKYO
	1	Non-Brand

10/22A ESD request Delete DA5, DA8 covered by ME design

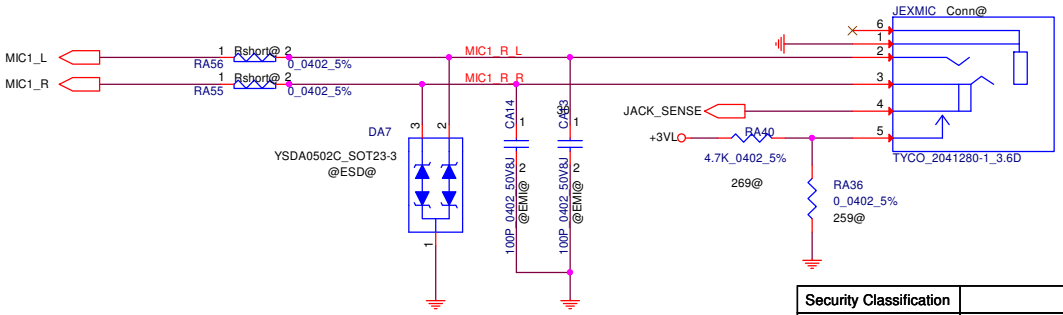
11/28 Change SPK connector to 6 pin, change SPK_DET0 to SPK_DET, delete SPK_DET1 and RA96

HeadPhone/LINE Out JACK



10/24 Change RA53~56 to short pad.....again.....~

MIC/LINE IN JACK



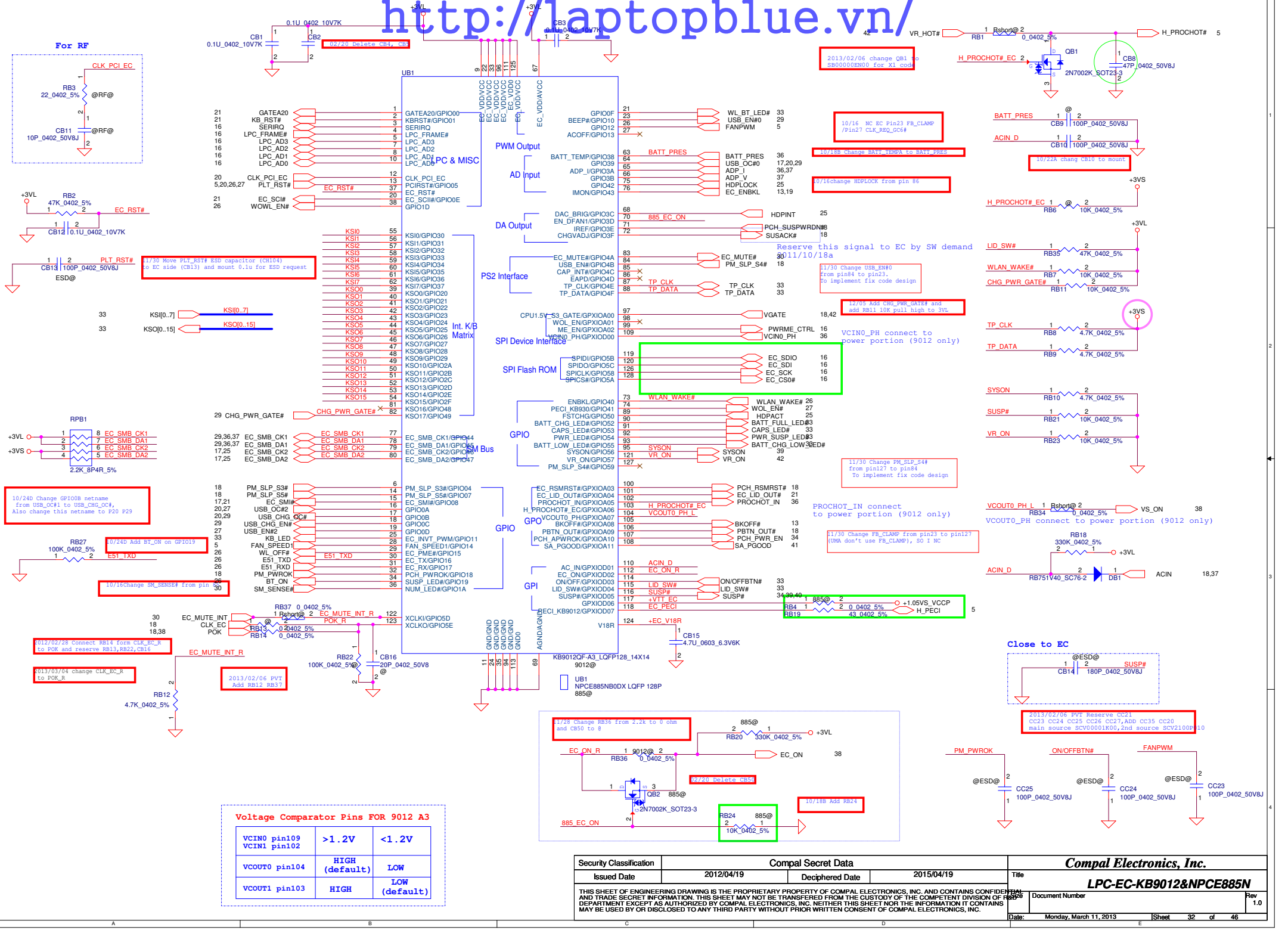
Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

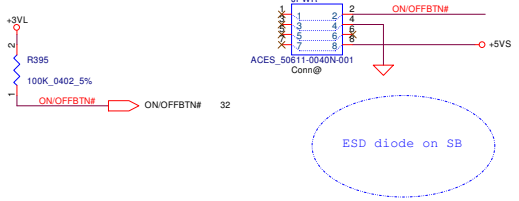
Title: AUDIO CONN

Size | Document Number | Rev 1.0

Date: Monday, March 11, 2013 | Sheet 31 of 46

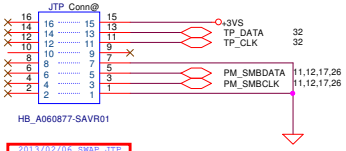


Power Button

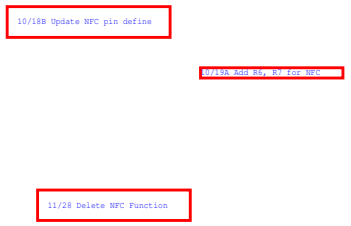


Conn.

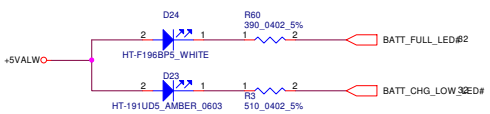
Touchpad Connector



NFC

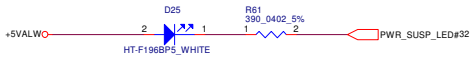


BATT CHARGE /FULL LED



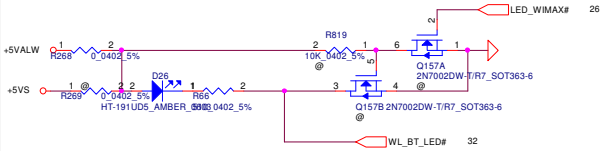
White LED bright when both AC-adaptor is plugged in and Battery is full charged
Amber LED bright while charging battery from AC-adaptor.
Amber LED blink during Critical Low Battery

POWER LED



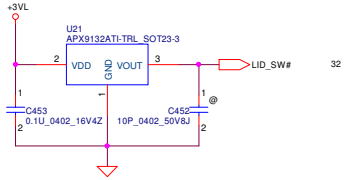
White LED bright when system is power on.
White LED blink when system is sleep mode.

WLAN/WiMAX LED

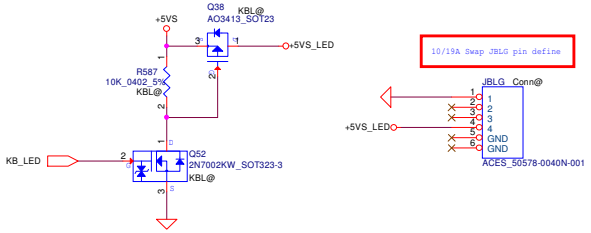


Amber LED bright while Wireless and/or WiMAX turns on.

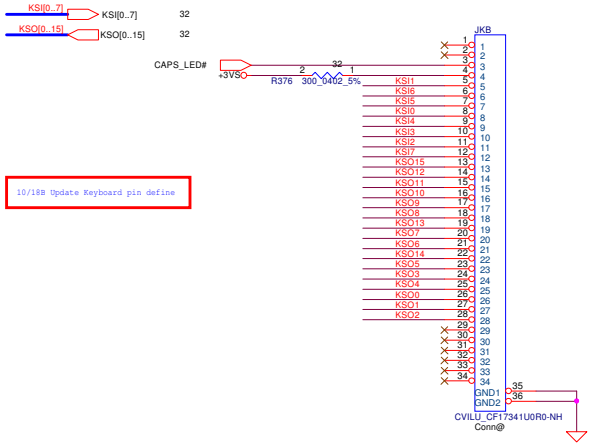
Lid SW



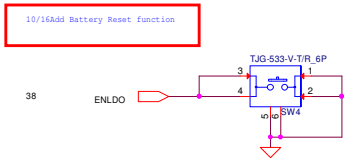
Keyboard LED



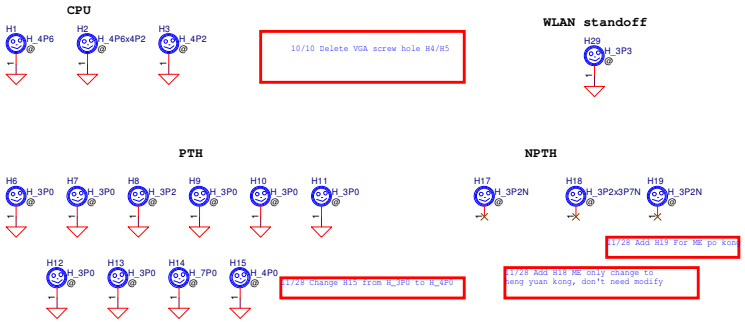
KEYBOARD CONN.



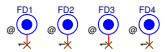
Battery Reset



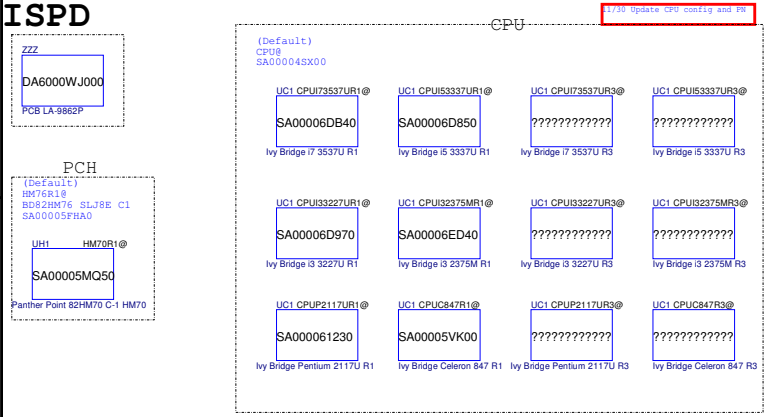
Screw Hole



PCB Fedical Mark PAD

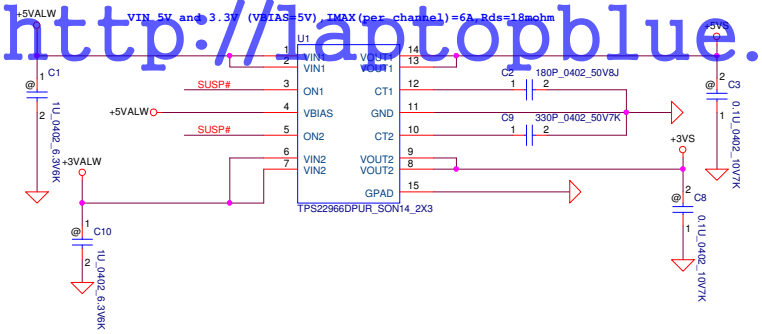


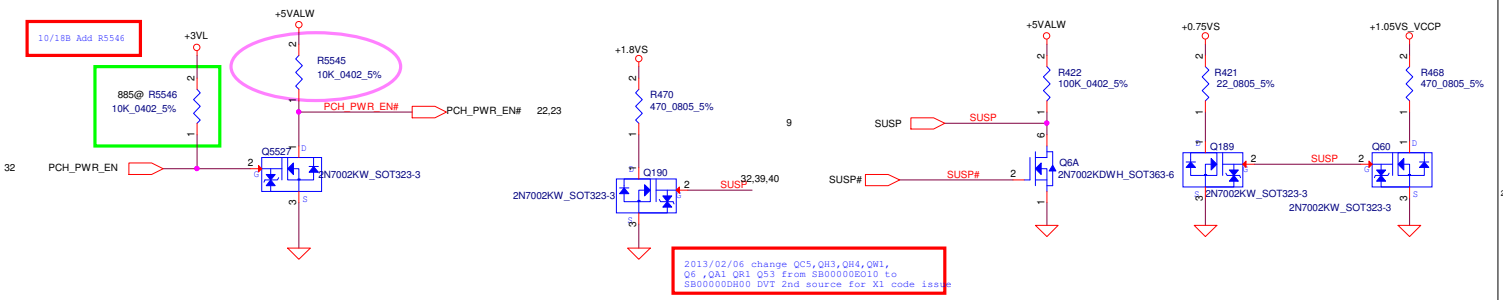
ISPD



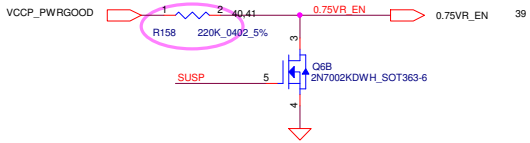
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/19	Deciphered Date 2015/04/19	Title: TP/ISPD/KB/LED/Screw
Size	Document Number: VFKTA		Rev: 1.0
Date: Monday, March 11, 2013	Sheet 33 of 46		

+5VALW TO +5VS
+3VALW TO +3VS
Load switch

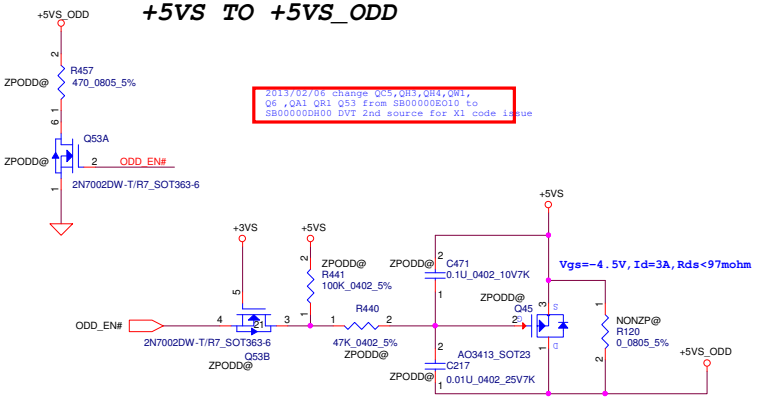




For S3 CPU Power Saving



+5VS TO +5VS_ODD



Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

Title: DC-DC INTERFACE

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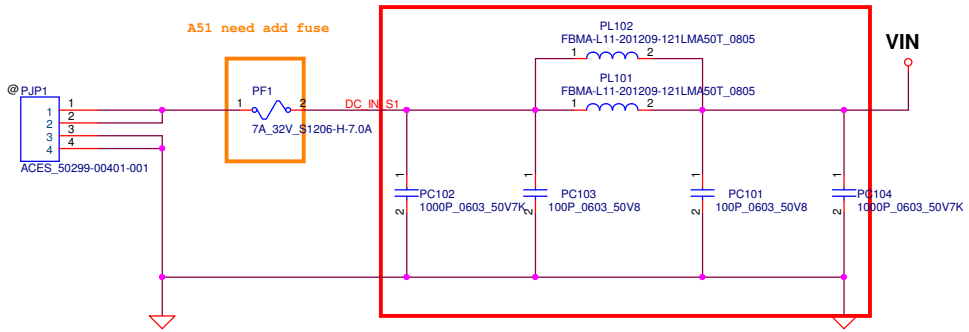
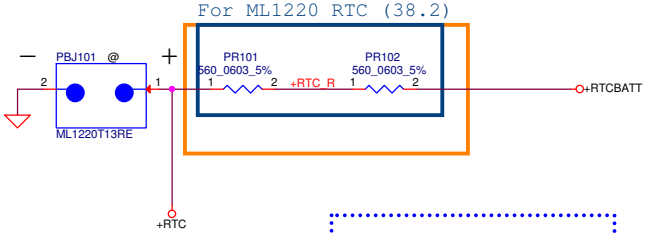
Date: Monday, March 11, 2013 | Sheet 34 of 46

EMI Part (47.1)



For ML1220 RTC (38.2)



01/17: Change PBJ101 footprint to BJ_ML1220T10_2P

Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

Title: *DCIN/PRECHARGE*

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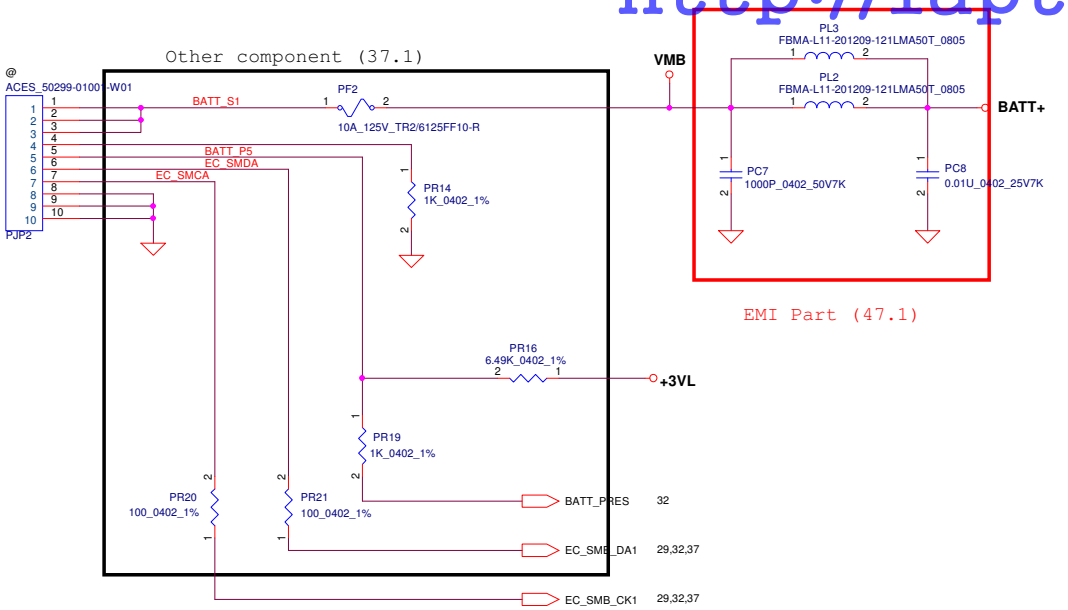
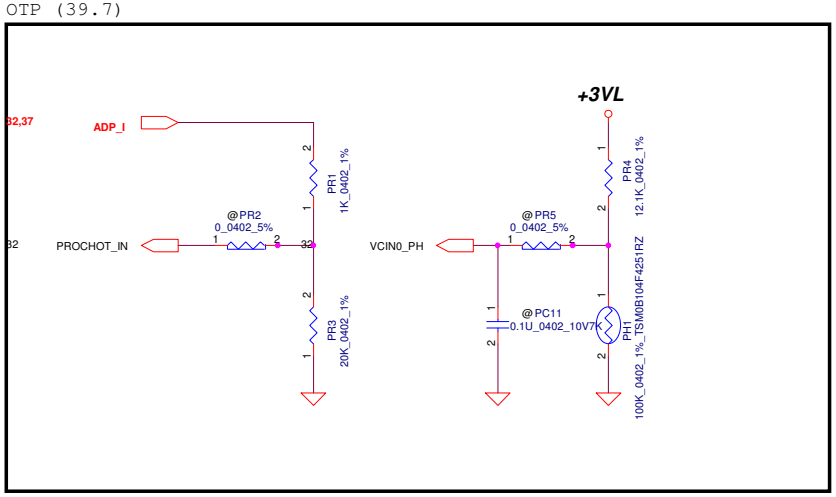




Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

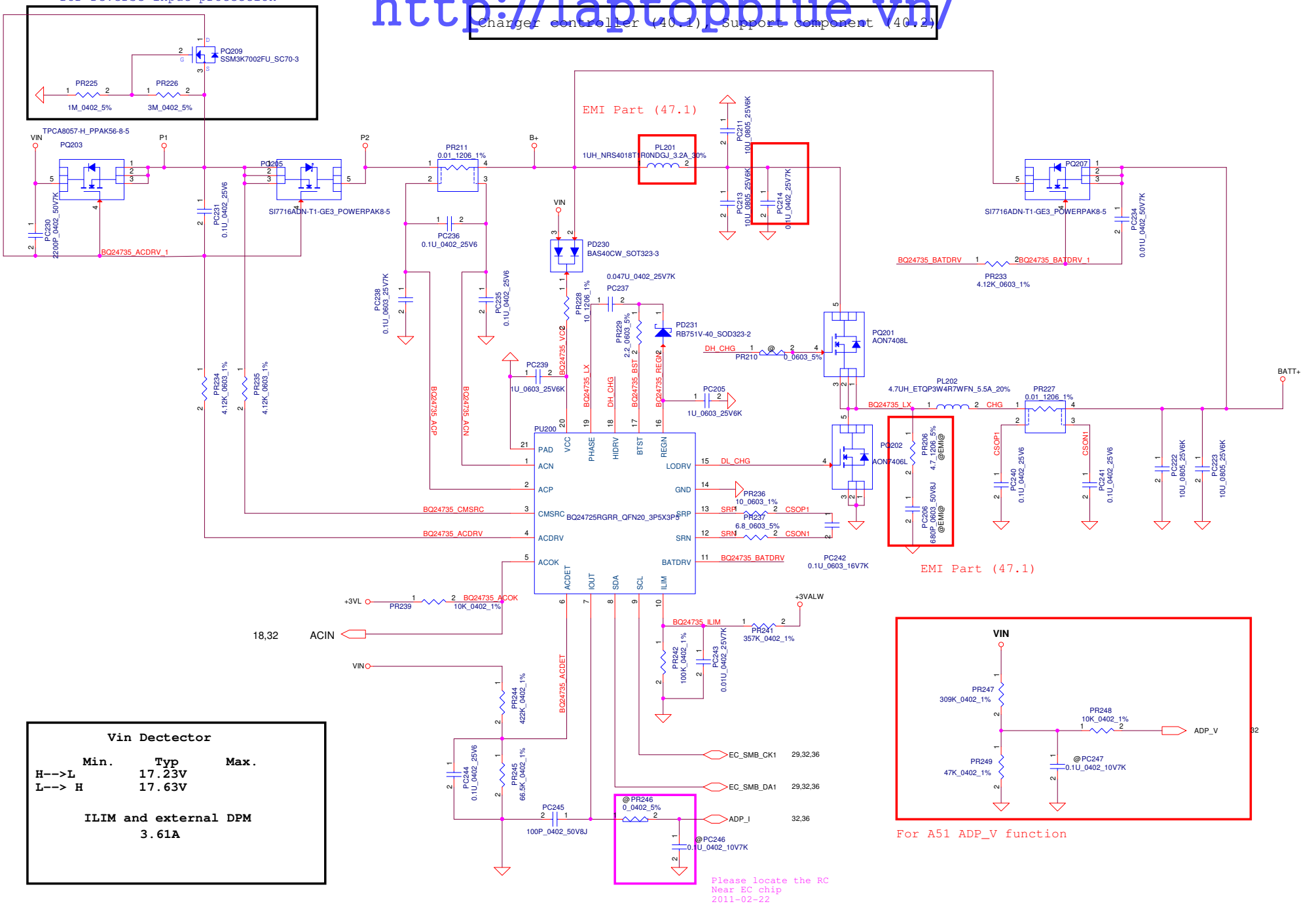
Title: ***BATTERY CONN / OTP***

Size: Custom | Document Number: *VFKTA* | Rev: 1.0

Date: | Sheet 36 of 46

for reverse input protection

Charger controller (40.1) Support component (40.2)



Vin Dectector

	Min.	Typ	Max.
H-->L		17.23V	
L--> H		17.63V	

ILIM and external DPM
3.61A

Please locate the RC
Near EC chip
2011-02-22

Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

Title: **CHARGER**

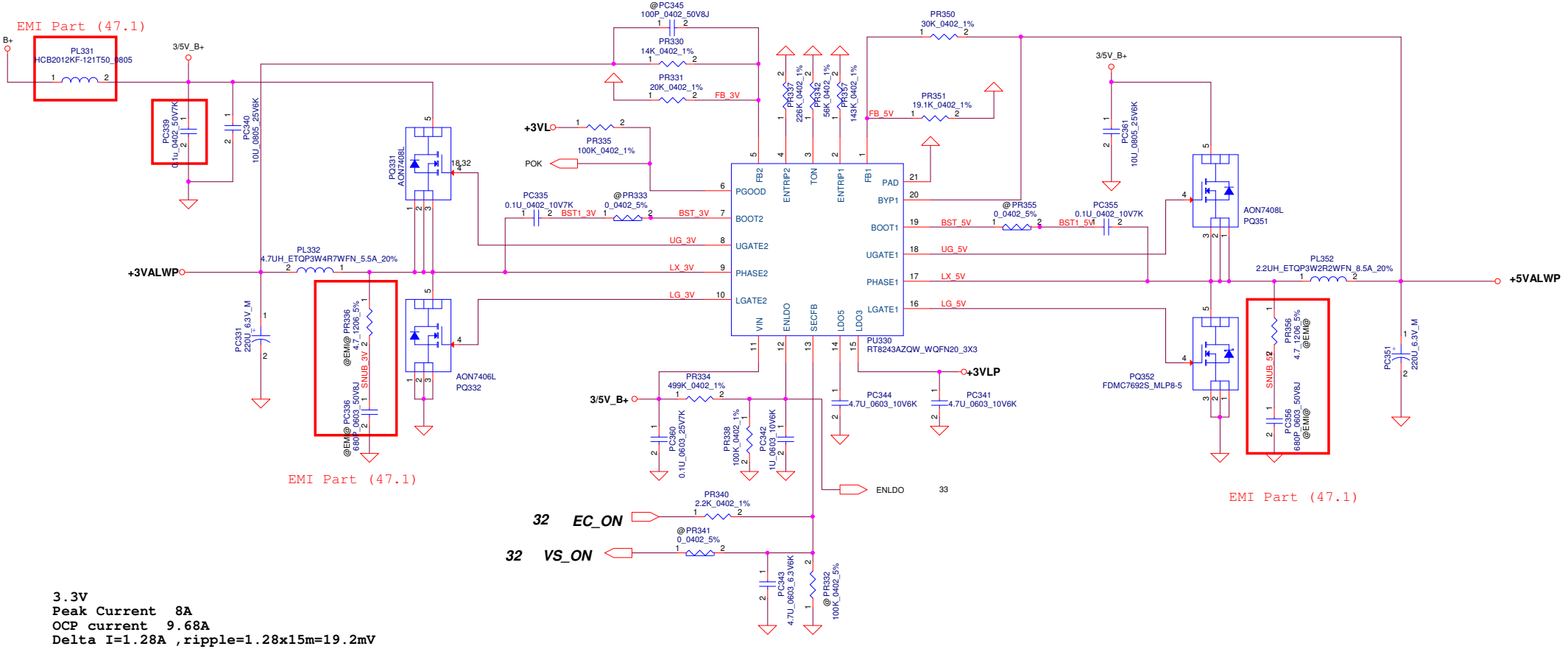
Size: Custom | Document Number: VFKTA | Rev: 1.0

Date: | Sheet 37 of 46

3/5VALW controller (35.1), Support component (35.2)

5V
Peak Current 10A
OCP current 12.03A
FSW=390kHz
Delta I=4.29A,ripple=4.29*17m=72.93mV
DCR 15.5mohm+/-15%
ESR 17mohm

	TYP	MAX
H/S Rds(on)	:27mohm ,	34mohm
L/S Rds(on)	:10.8mohm ,	13.6mohm



3.3V
Peak Current 8A
OCP current 9.68A
Delta I=1.28A ,ripple=1.28x15m=19.2mV
FSW=455kHz
DCR 35mohm +/-15%
ESR 15mohm

	TYP	MAX
H/S Rds(on)	:27mohm ,	34mohm
L/S Rds(on)	:19mohm ,	23.5mohm

Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

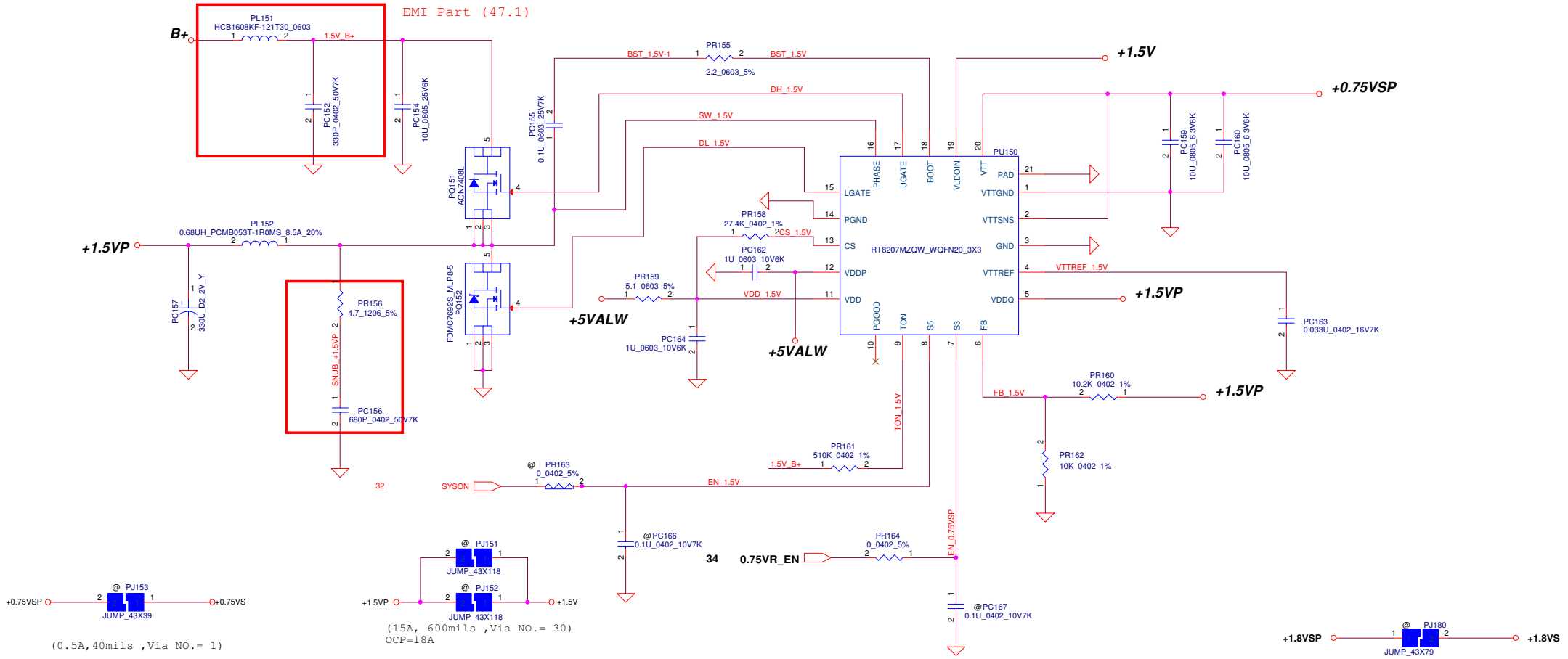
Compal Electronics, Inc.

Title: *3VALW/5VALW*

Size: Custom | Document Number: VFKTA | Rev: 1.0

Date: | Sheet 38 of 46

DDR controller (35.3), Support component (35.4)



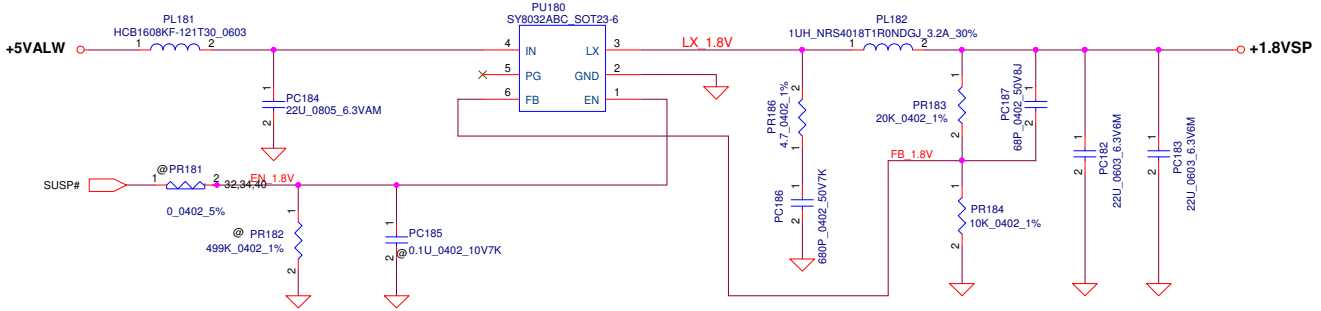
(0.5A,40mils ,Via NO.= 1)

(15A, 600mils ,Via NO.= 30)
OCP=18A

1.5V
Peak Current 16.8A
OCP current 20 A
FSW=495kHz
DCR 13mohm
ESR 9mohm

	TYP	MAX
H/S Rds(on)	:27mohm ,	34mohm
L/S Rds(on)	:10.8mohm ,	13.6mohm

1.8VS controller (35.15), Support component (35.16)



STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off

Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

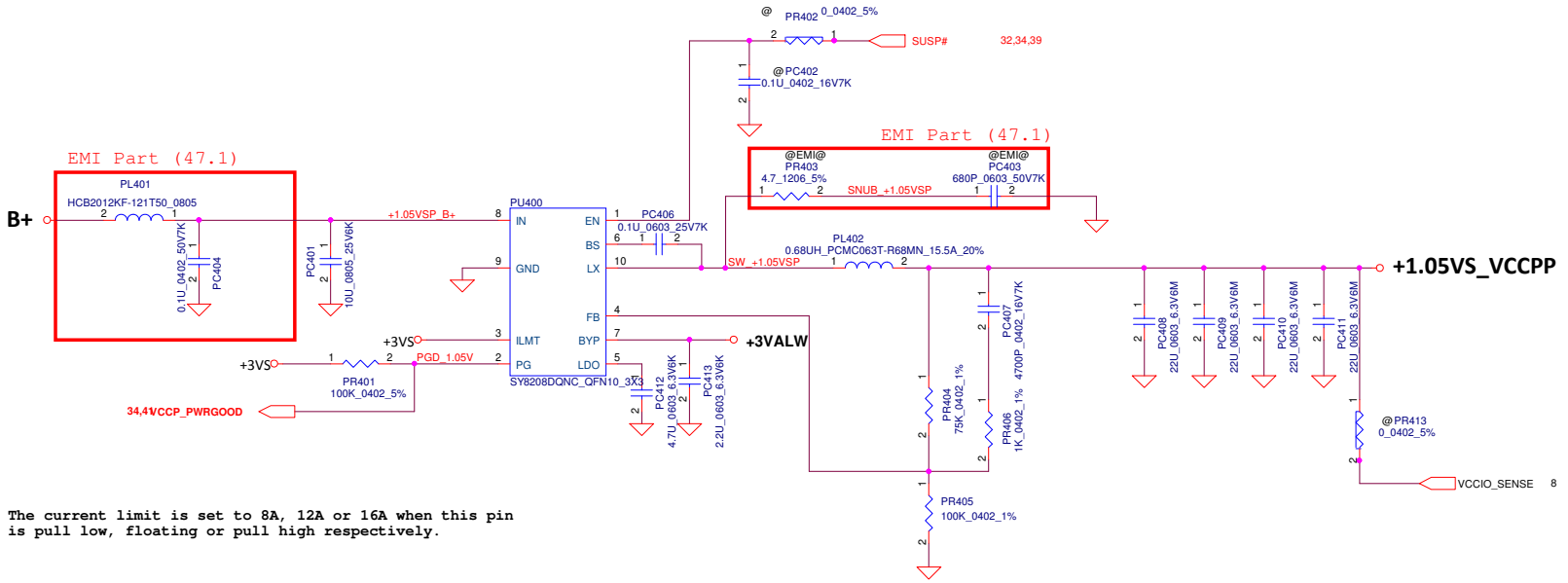
Compal Electronics, Inc.

Title: *1.5VP/0.75VSP/1.8VSP*

Size: Custom | Document Number: VFKTA | Rev: 1.0

Date: | Sheet 39 of 46

1.05VCCP controller (35.5), Support component (35.6)



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high respectively.

(17A,680mils ,Via NO.=34)
OCP=23.91A

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: ***+1.05VS_VCCP***

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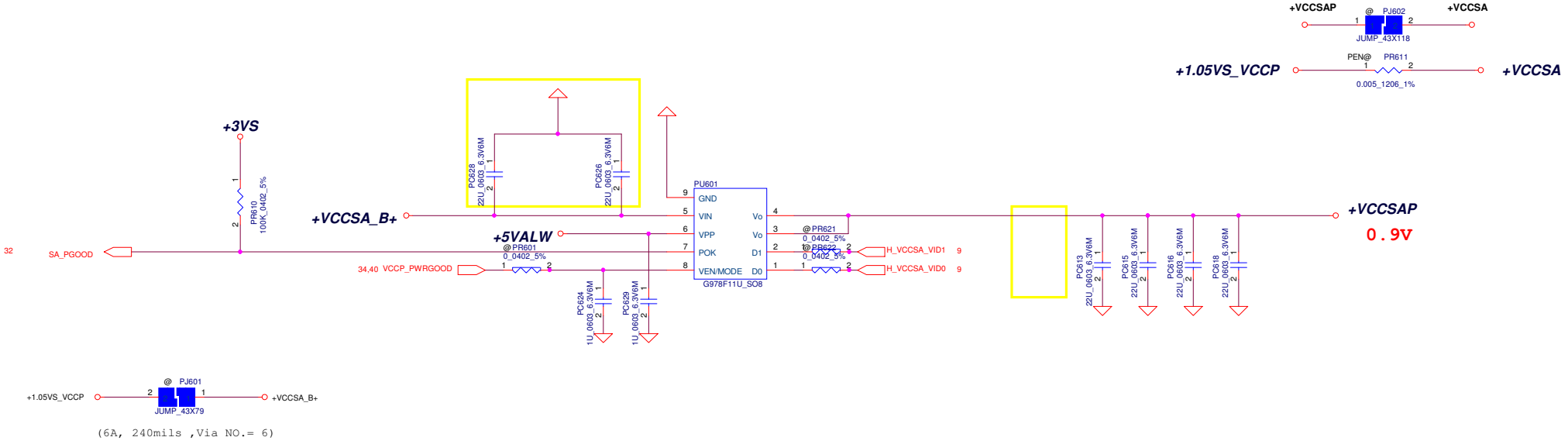
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

VCCSA controller (35.17), Support component (35.18)



(6A, 240mils ,Via NO.= 6)

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Compal Electronics, Inc.

Title	VCC_SAP	
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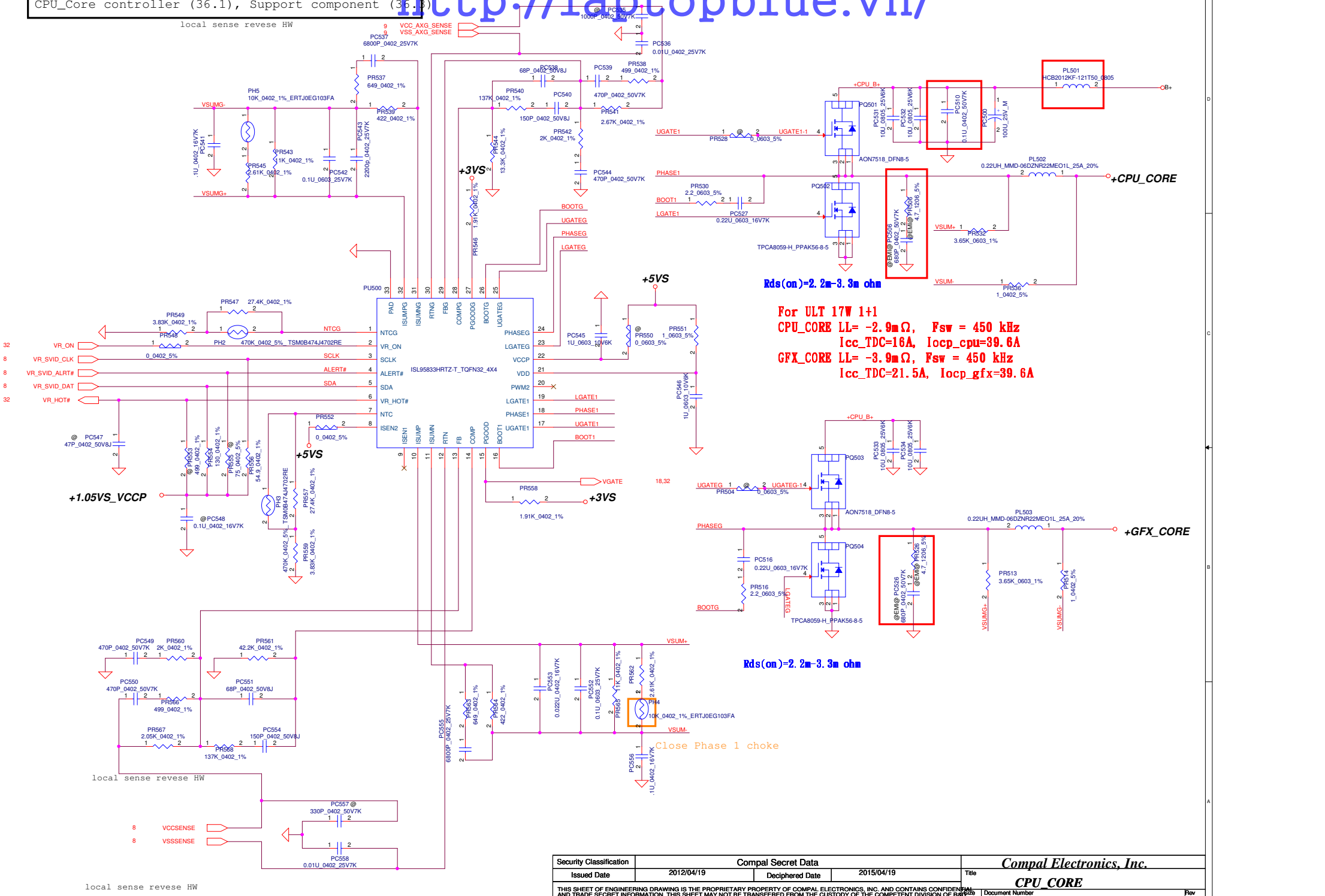
CPU_Core controller (36.1), Support component (36.2)



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: CPU_CORE

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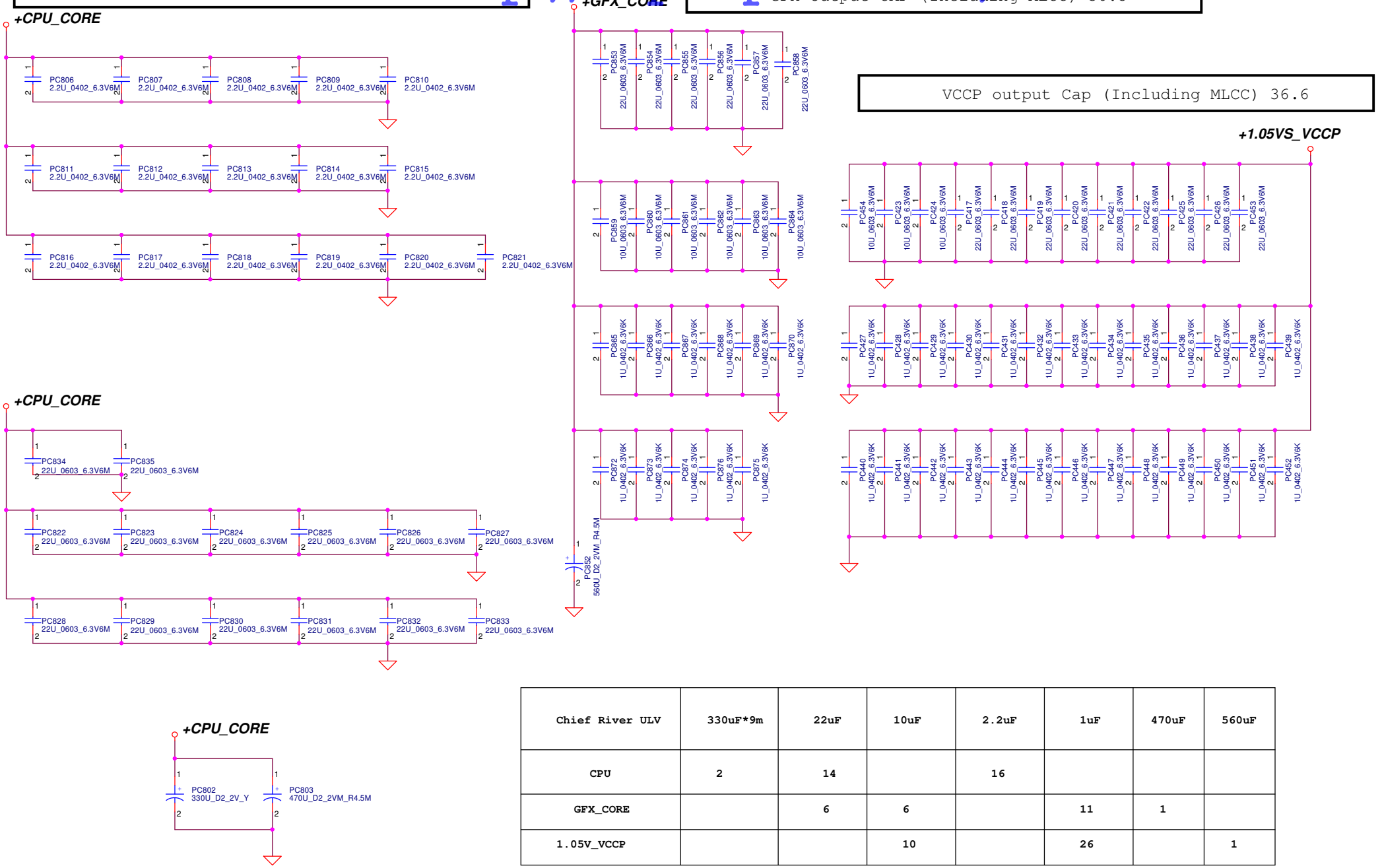
CPU_Core output CAP (Including MLCC) 36.4

GFX output CAP (Including MLCC) 36.5

VCCP output Cap (Including MLCC) 36.6



Chief River ULV	330uF*9m	22uF	10uF	2.2uF	1uF	470uF	560uF
CPU	2	14		16			
GFX_CORE		6	6		11	1	
1.05V_VCCP			10		26		1

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Compal Electronics, Inc.

Title: PWR - PROCESSOR DECOUPLING

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Version change list (P.I.R. List)

for PWR

Item	Time (When)	Page (Where)	Location / Discription (How / What)	Request (Who)	Reson (Why)
1	EVT--2012/10/24	P36-PWR-BATTERY CONN / OTP	@PD5 / Remove ESD diode	company	For part count reducation
2	EVT--2012/10/24	P36-PWR-BATTERY CONN / OTP	@PD6 / Remove ESD diode	company	For part count reducation
3	EVT--2012/10/24	P37-PWR-CHARGER	@PC221 /Remove 10uF capacitor	company	For part count reducation
4	EVT--2012/10/24	P38-PWR-3VALW/5VALW	PC331 /Reserve	PWR	ME limitation
5	EVT--2012/10/24	P38-PWR-3VALW/5VALW	@PC354/mount	PWR	ME limitation
6	EVT--2012/10/24	P38-PWR-3VALW/5VALW	PR337/235K change to 137K	PWR	for RT8243 3V OCP setting
7	EVT--2012/10/24	P38-PWR-3VALW/5VALW	PR357/156K change to 143K	PWR	for RT8243 5V OCP setting
8	EVT--2012/10/24	P39-1.5VP/0.75VSP/1.8VSP	PR158/16.2K change to 27.4K	PWR	for RT8207 OCP setting
9	EVT--2012/10/24	P43-PWR +CPU_CORE DECOUPLING	PC416/ change 560uF	PWR	Based on height and space limitation
10	EVT--2012/10/24	P43-PWR +CPU_CORE DECOUPLING	PC415/ Remove	PWR	Based on height and space limitation
11	EVT--2012/10/25	P37-PWR-CHARGER	PQ203/change to TPCA8507	PWR	for design change
12	DVT--2012/12/06	P37-PWR-CHARGER	PU200/change to BQ24725RGRR	PWR	for design change
13	DVT--2012/12/06	P37-PWR-CHARGER	PQ203/ change to TPCA8507	PWR	AON6504 has burnt out issue
14	DVT--2012/12/06	P38-PWR-3VALW/5VALW	PC534,PC351/Delete	PWR	Based on height and space limitation
15	DVT--2012/12/06	P38-PWR-3VALW/5VALW	PR335/add 100K ohm	PWR	Pull high +3VL
16	DVT--2012/12/06	P38-PWR-3VALW/5VALW	PC344/add 4.7U	PWR	for design request
17	DVT--2012/12/06	P38-PWR-3VALW/5VALW	PC341/change to 4.7U	PWR	for design request
18	DVT--2012/12/06	P38-PWR-3VALW/5VALW	PC352,PC353/add 150U_D2	PWR	Based on height and space limitation
19	DVT--2012/12/06	P39-1.5VP/0.75VSP/1.8VSP	PL152/change to 0.68UH	PWR	for design change
20	DVT--2012/12/06	P40-PWR-1.05VS_VCCP	PL401/change PN	PWR	to integrate PN
21	DVT--2012/12/06	P40-PWR-1.05VS_VCCP	PR403 PC403/Reserve	EMI	EMI Command
22	DVT--2012/12/06	P42-CPU_CORE	CPU_CORE(PR5XX,PC5XX)/change solution	PWR	change solution
23	DVT--2012/12/06	P43-PWR +CPU_CORE DECOUPLING	PC802 PC803/change to 470U	PWR	change solution
24	DVT--2012/12/06	P36-PWR-BATTERY CONN / OTP	PF2/change PN	company	For cost down
25	PVT--2013/01/18	P39-1.5VP/0.75VSP/1.8VSP	PC157/change 390U	PWR	for design change
26	PVT--2013/01/18	P40-PWR-1.05VS_VCCP	PC414 / change 0ohm	PWR	change solution
27	PVT--2013/01/18	P40-PWR-1.05VS_VCCP	PC417,PC418,PC419,PC420,PC421,PC422,PC425/change to 22U	PWR	for 1.05VCCP test
28	PVT--2013/01/18	P40-PWR-1.05VS_VCCP	PC426,PC453/add 22U	PWR	for 1.05VCCP test
29	PVT--2013/01/18	P40-PWR-1.05VS_VCCP	PC407/change 4700P	PWR	for design change
30	PVT--2013/01/18	P40-PWR-1.05VS_VCCP	PC416/Delete	PWR	for 1.05VCCP test
31	PVT--2013/01/18	P40-PWR-1.05VS_VCCP	PL402/change to 0.68U	PWR	for 1.05VCCP test
32	PVT--2013/01/18	P42-CPU_CORE	PQ501,PQ503 /change AON7518	PWR	AON7514 EOL
33	PVT--2013/01/18	P42-CPU_CORE	PR553/Reserve	PWR	change solution
34	PVT--2013/01/18	P42-CPU_CORE	PR541/change to 2.67K	PWR	for CPU setting
35	PVT--2013/01/18	P42-CPU_CORE	PC543/change to 2.2nF	PWR	for CPU setting
36	PVT--2013/01/18	P42-CPU_CORE	PC553/change to 8.2nF	PWR	for CPU setting
37	PVT--2013/01/18	P42-CPU_CORE	PR567/change to 2.05K	PWR	for CPU setting
38	PVT--2013/01/21	P43-PWR +CPU_CORE DECOUPLING	PC802,PC852/change to 560U	PWR	for CPU,GFX Transient
39	PVT--2013/01/21	P39-1.5VP/0.75VSP/1.8VSP	PC152/add 2200p	PWR	EMI Command
40	PVT--2013/01/21	P39-1.5VP/0.75VSP/1.8VSP	PR156/add 4.7ohm	PWR	EMI Command
41	PVT--2013/01/21	P39-1.5VP/0.75VSP/1.8VSP	PC156/add 680p	PWR	EMI Command
42	PVT--2013/01/21	P39-1.5VP/0.75VSP/1.8VSP	PR155/add 2.2ohm	PWR	EMI Command
43	PVT--2013/01/21	P42-CPU_CORE	PQ502,PQ504 /change TPCA8059	PWR	for design change
44	Pre-MP--2013/03/05	P37-PWR-CHARGER	PC214/add 0.1u	PWR	EMI Command
45	Pre-MP--2013/03/05	P38-PWR-3VALW/5VALW	PC339/add 0.1u	PWR	EMI Command
46	Pre-MP--2013/03/05	P39-1.5VP/0.75VSP/1.8VSP	PC157 /change to 330u	PWR	ME limitation
47	Pre-MP--2013/03/05	P39-1.5VP/0.75VSP/1.8VSP	PC152 /change to 330p	PWR	EMI Command
48	Pre-MP--2013/03/05	P40-PWR-1.05VS_VCCP	PR406/add 1 K ohm	PWR	for 1.05 VCCP test(change to location sense)
49	Pre-MP--2013/03/05	P40-PWR-1.05VS_VCCP	PC404/add 0.1u	PWR	EMI Command
50	Pre-MP--2013/03/05	P42-CPU_CORE	PC510/add 0.1u	PWR	EMI Command
51	Pre-MP--2013/03/05	P42-CPU_CORE	PC553/change to 22nF	PWR	for CPUTransient
52	Pre-MP--2013/03/05	P43-PWR +CPU_CORE DECOUPLING	PC802/change to 330U	PWR	for CPUTransient

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Compal Electronics, Inc.			
Title	PWR-PIR		
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HW PIR (Product Improve Record)

VFKTA LA-9862P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	11/28	(P.30)	Mount CA32(SE102104K00)	BOM structure change
2.	11/28	(P.32)	Change RB36 from 2.2k to 0 ohm and CB50 to @	Design change
3.	11/28	(P.24)	Add @ to JHDMI	BOM structure change
4.	11/28	(P.11)	Move RD10, RD11 to page 12.	
5.	11/28	(P.33)	Delete NFC Function	Design change
6.	11/28	(P.28)	Change JCARD.10 to SDWP# and JCARD.11 to SDCD.	Design change
		(P.28)	Add QW1, RW3, RW4 for normal close type connector	
7.	11/28	(P.13)	Add D92 for LID_SW#_D to isolate the +3VL power rail from LID_SW#	Design change
8.	11/28	(P.15)	Update HDMI power circuit	Design change
9.	11/28	(P.20)	Change USB port 10 to NC.	Design change
10.	11/28	(P.16)	Change UH3 from socket to IC	Design change
11.	11/28	(P.09)	Change CC44 to 0805 size (SE00000PL00), Add CC40	For 1206 MLCC Crack issue
		(P.09)	Change CC53 to 47U 0805 (SE00000PL00),Add CC50 (SE00000PL00)	
		(P.12)	Change CD31 to 0805 size (SE00000PL00)	
		(P.29)	Change CR10, CR12 to 0805 size (SE00000PL00)	
12.	11/28	(P.14)	change BOM structure C238,C239,C240,C241,C242,C243 to CRT@EMI@	EMI request
13.	11/28	(P.16)	Change UH3 from socket to IC	Design change
14.	11/28	(P.07)	Change RC73 to 0 ohm (do not use short pad on this location)	For debug
15.	11/28	(P.30)	Change RA50 to 269@	Design change
16.	11/28	(P.31)	Change SPK connector to 6 pin, change SPK_DET0 to SPK_DET, delete SPK_DET1 and RA96	Design change
17.	11/28	(P.21)	Change SPK_DET0 to SPK_DET, delete SPK_DET1	Design change
18.	11/28	(P.13)	Delete D92 and change the netname to BKOFF# for touch Screen	Avoid LCD_INV leak to Touch/B
19.	11/28	(P.13)	SWAP R92,R100 L60 config,SWAP R93.R101,L59 config	BOM structure change
20.	11/28	(P.13)	Reverse LVDS connector pin definition	Design change
21.	11/28	(P.33)	Change H15 from H_3P0 to H_4P0,Add h19 H_3P2N ME follow ME change	ME request
22.	11/29	(P.28)	Modify Jcard @ to update Netlist	BOM structure change
23.	11/29	(P.13)	Delete R87,R88,R89,R90,R92,R93,R100,R101,L59,L60,JCAM,JEDP	Design change
		(P.13)	Change L56 toL55,L58 to L57, JLVDS type and modify net name for LVDS	Design change
24.	11/29	(P.14)	add R62,R63,22-ohm (PN: SD028220A80) on CRT HSYNC/VSYNC trace.	For CRT undershoot issue
25.	11/29	(P.16)	Chane UH4, RH269, RH271 to @,change RH267 from shortpad to 0-ohm	Design change
26.	11/30	(P.8)	Add CC17~CC19 for ESD request	ESD request
27.	11/30	(P.20)	Move PLT_RST# ESD capacitor (CH104) to EC side (CB13) and mount 0.1uF	ESD request
28.	11/30	(P.5)	Change CC63 from @ESD@ to ESD@ for ESD request	ESD request
29.	11/30	(P.30)	Reserve RA31,RA38 for EMI request	EMI request
30.	11/30	(P.32)	Change PM_SLP_S4# from pin127 to pin84.	
		(P.32)	Change USB_EN#0 from pin84 to pin23.	
31.	11/31	(P.33)	Update CPU config&PN	
32.	12/04	(P.29)	Update S&C to 14640/14641 co-layout circuit ,add RR1~RR4, QR1, modify net-name	Design change

REVISION CHANGE: 0.2 TO 0.3

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	01/18	(P.28)	Delete QW2	Design Change
2.	01/18	(P.20)	Change RH166 from ShortPad to 0 ohm resistor.	For ESD Request
3.	01/18	(P.07)	Delete RC3.	Design Change
4.	01/18	(P.32)	Add RB12, RB37, connect EC_MUTE_INT from codec to EC	For boot bobo issue
5.	01/18	(P.05)	Add CC35,CC20	For ESD Request
6.	01/18	(P.21)	reserve CC21	For ESD Request
7.	01/18	(P.32)	reserve CC23,CC24,CC25	For ESD Request
8.	01/18	(P.18)	reserve CC26,CC27	For ESD Request
9.	01/18	(P.32)	Change CB13 to 100P P/NSE071101J80	Design Change
10.	01/18	(P.28)	Add RW2 CW9	For EMI Request

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HW PIR (Product Improve Record)

HW PIR (Product Improve Record)

VFKTA LA-9862P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.3 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	01/28	(P.33)	Modify JTP pin with the same as VFKTA DIS	Design Change
2.	01/28	(P.13)	Reserve R267&R266 0 ohm	For EMI cost down
3.	01/28	(P.32)	Change QB1 to SB00000EN00	For X1 code issue
4.	01/28	(P.07)	Change QC3 to SB00000PF00	For X1 code issue
5.	01/28	(P.15)	Change QY1 QY2 to SB00000PF00	For X1 code issue
6.	01/28	(P.16)	Change UH3 from SA00003K800 to SA00004LI00	For X1 code issue
7.	01/28	(P.27/29)	Change UR1 UR4 from SA00004KB00 to SA00003TV00	For X1 code issue
8.	01/28	(P.13)	Change L2 SM01000CD00E to SM01000JB00	For EOL issue
9.	01/28	(P.9/17/28/34/30/29)	Change QC5,QH3,QH4,QW1,Q6 ,QA1, QR1, Q53 from SB00000EO10 to SB00000DH00	For X1 code issue
10.	01/28	(P.30)	Change RA42 from SM01000CY00 to SM01000A900	For X1 code issue
11.	01/28	(P.29)	Change LR2,LR3,LR4,LR5 from SM070001U00 to SM070001R00	For X1 code issue
12.	02/18	(P.06)	Swap H_EDP_TXN[0\1] to H_EDP_TXP[0\1]	Design mistake
13.	02/18	(P.13)	Change C7 to SE076153K80 (15nF)	for LCD sequence tuning
14.	02/19	(P.05)	Delete CC33, CC36, C4; change R1 to short pad	for part count reduce
15.	02/19	(P.07)	Change RC73 to short pad	for part count reduce
16.	02/19	(P.09)	Delete CC61, CC83; change RC119 to short pad	for part count reduce
17.	02/19	(P.11)	Delete CD2, CD15	for part count reduce
18.	02/19	(P.12)	Delete cD28, CD46	for part count reduce
19.	02/19	(P.13)	Change R106 to shortpad	for part count reduce
20.	02/19	(P.14)	Delete C250	for part count reduce
21.	02/19	(P.16)	Delete CH6, CH100; change RH67, RH68 to short pad	for part count reduce
22.	02/19	(P.19)	Delete RH254	for part count reduce
23.	02/19	(P.26)	Delete CCL2, RCL5, RCL2, net: LAN_X1_R_R, LAN_X1_R	for part count reduce
24.	02/19	(P.27)	Delete net: LAN_X1_R	for part count reduce
25.	02/19	(P.28)	Change RW1 to shortpad	for part count reduce
26.	02/19	(P.29)	Delete CR7, CR8	for part count reduce
27.	02/19	(P.30)	Change RA22, RA18, RA24 to short pad	for part count reduce
28.	02/19	(P.41)	Delete CB4, CB5, CB50	for part count reduce
29.	02/19	(P.42)	Delete SW2, SW3	for part count reduce
30.	02/28	(P.32)	Connect RB14 form CLK_EC_R to POK and reserve RB13,RB22,CB16	for abnormal shut down power request
31.	02/28	(P.20)	change RH167 pin2 netname from CLK_EC_R to CLK_PCI_EC_R	
32.	03/04	(P.20)	change RH167 pin2 netname from CLK_PCI_EC_R to CLK_EC_R	For keep the same as DIS
33.	03/04	(P.32)	Connect RB14 from POK_R to POK and reserve RB13,RB22,CB16	for abnormal shut down power request
34.	03/04	(P.28)	Add RW5~RW8 for EMI request and change netname SD_DATA[0…3] to SD_DATA[0…3]_R on connector side	for EMI request
35.	03/06	(P.28)	Add 10pF CV10~CV13 on SD_DATA[0:3]	for EMI request.

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