

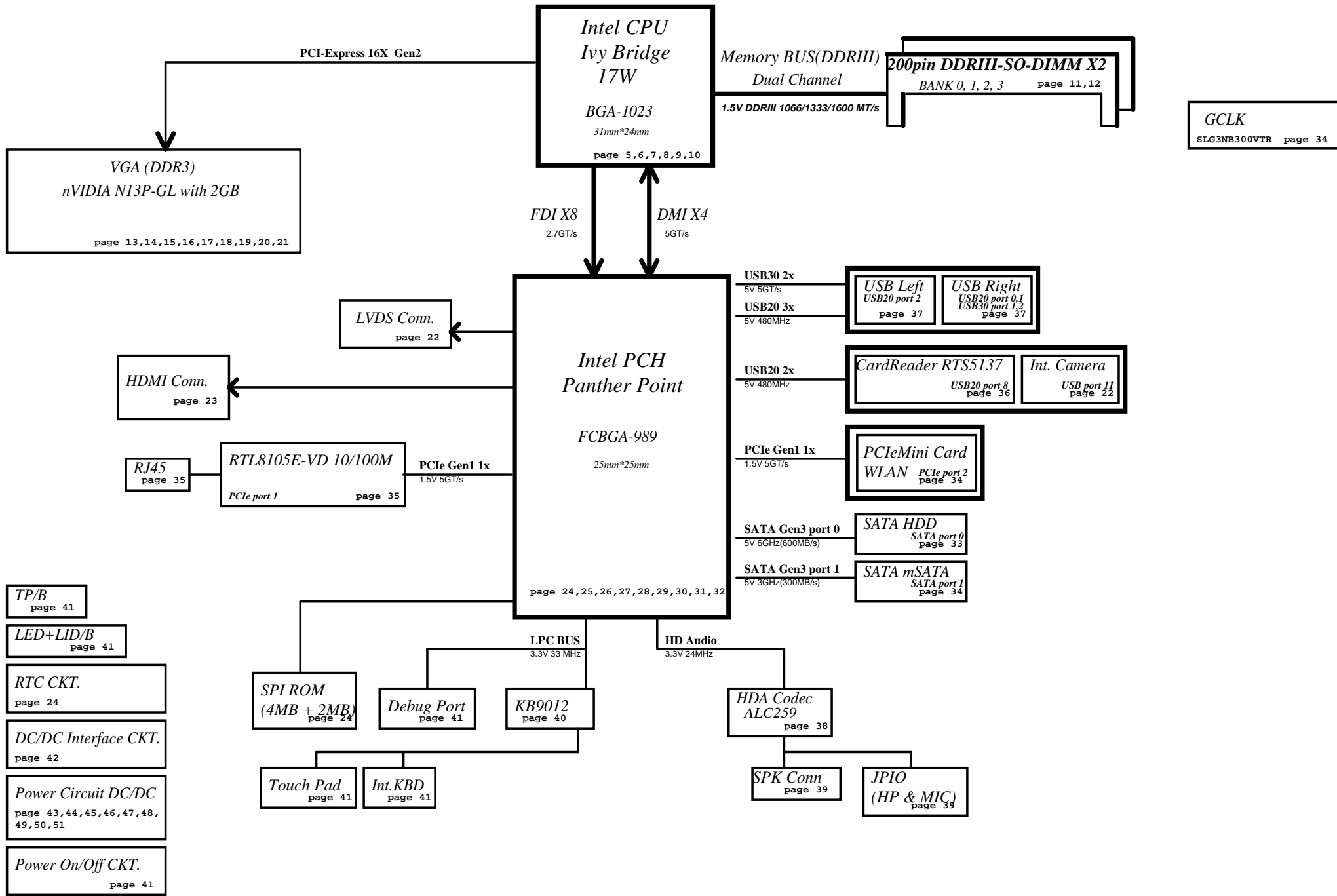
VCUAA

Metis 10F/10FG

LA-9161P REV 1.0 Schematic

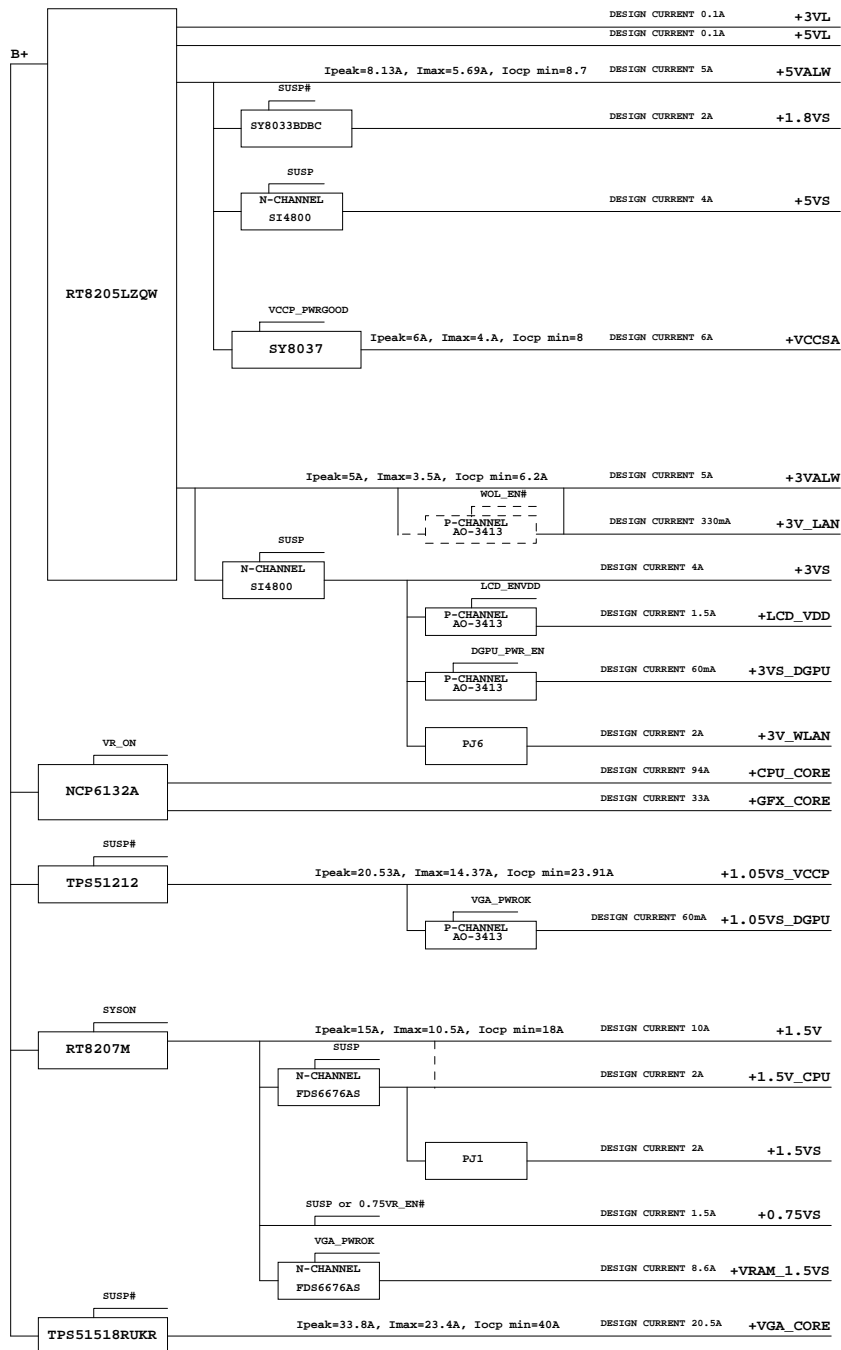
Intel Processor (Ivy Bridge) / PCH(Panther Point)
2012-08-07 Rev 1.0

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Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	Cover Page
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GCLK
SLG3NB300VTR page 34

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Security Classification	Compal Secret Data		Compal Electronics, Inc.	
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				Power Tree
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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane State	+RTCVC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VT +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
	S0	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

Platform	SKU	CPU	PCH	VGA
Chief River		Ivy Bridge i3 (CPUI3@) Ivy Bridge i5 (CPUI5@)	HM77C1 (HM77@) HM77C1_R1 (HM77R1@) HM77C1_R3 (HM77R3@)	nVIDIA N13P-GL (N13PGL@)

BTO Option Table

Function	SKU	MIC	LAN			
description						
explain						
BTO						

Function						
description						
explain						
BTO						

Function						
description						
explain						
BTO						

Function		
description		
explain		
BTO		

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	Smart Charger	12 H	0001 0010 b

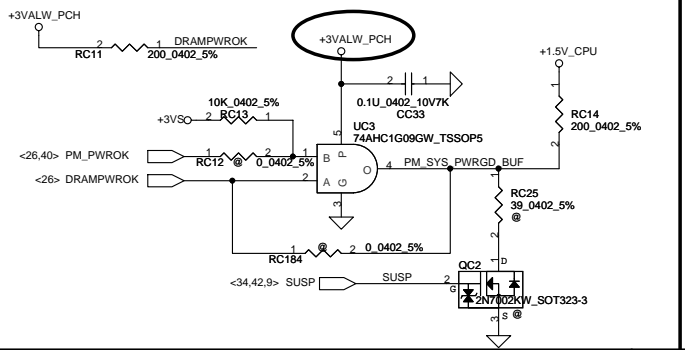
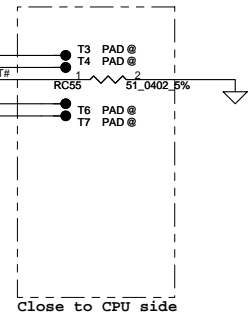
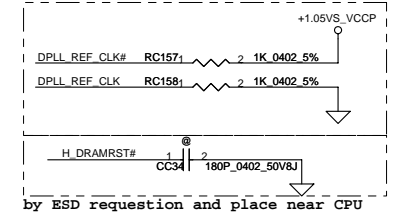
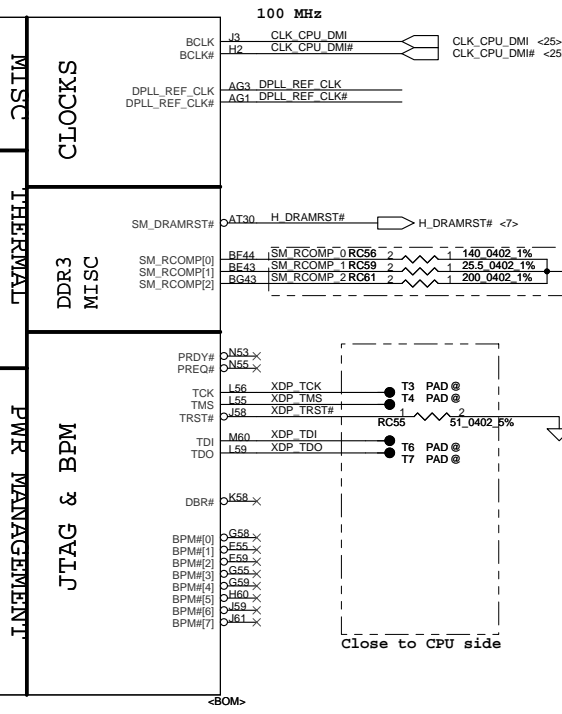
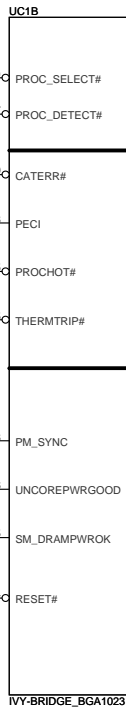
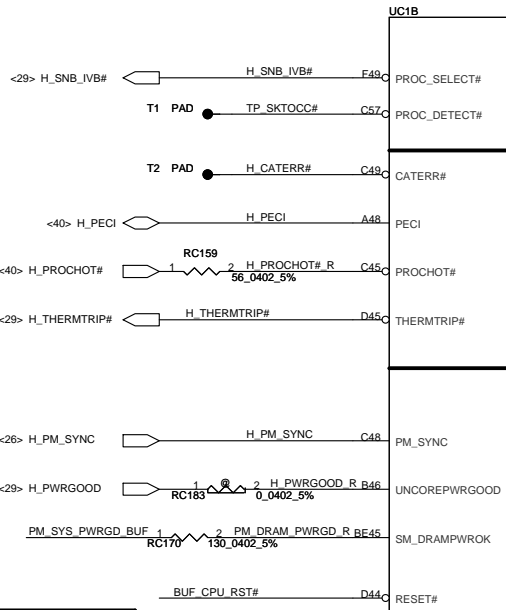
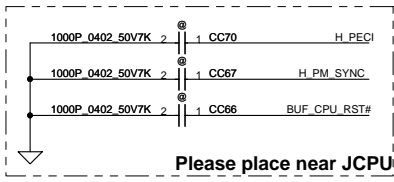
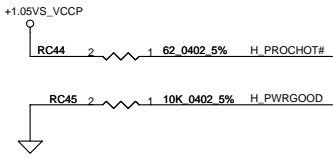
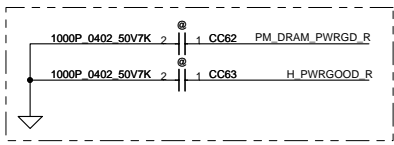
EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9E H	1001 1010 b

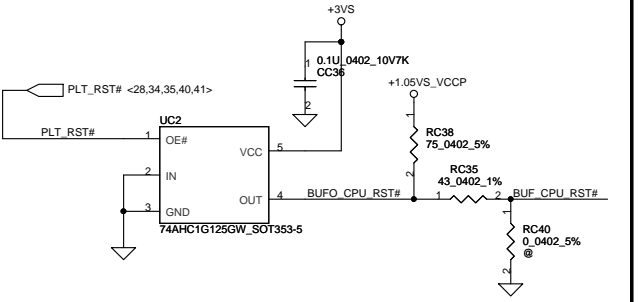
Power	Device	HEX	Address
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Notes List



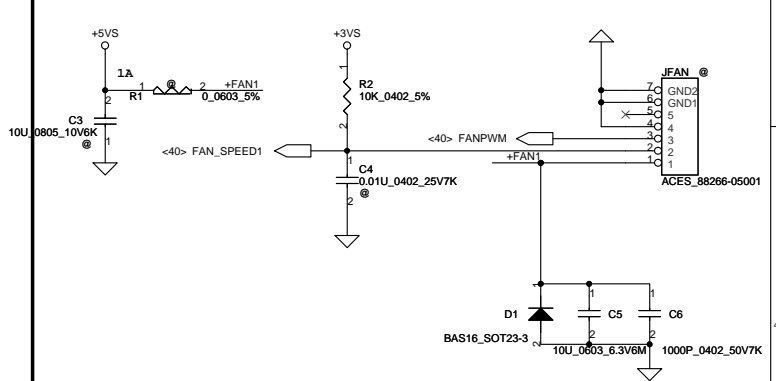
Buffered Rest to CPU



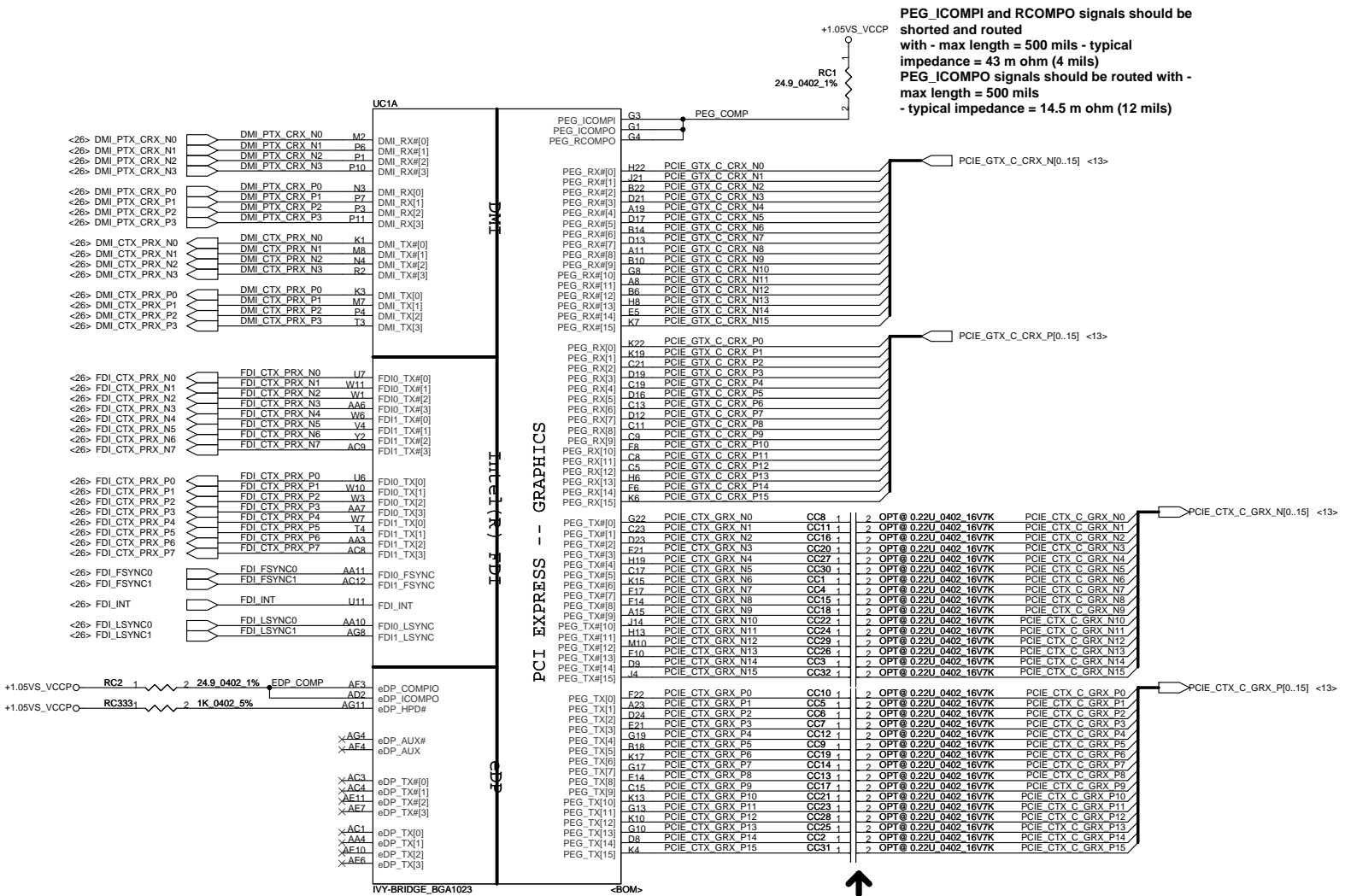
XDP Connector



FAN Control Circuit

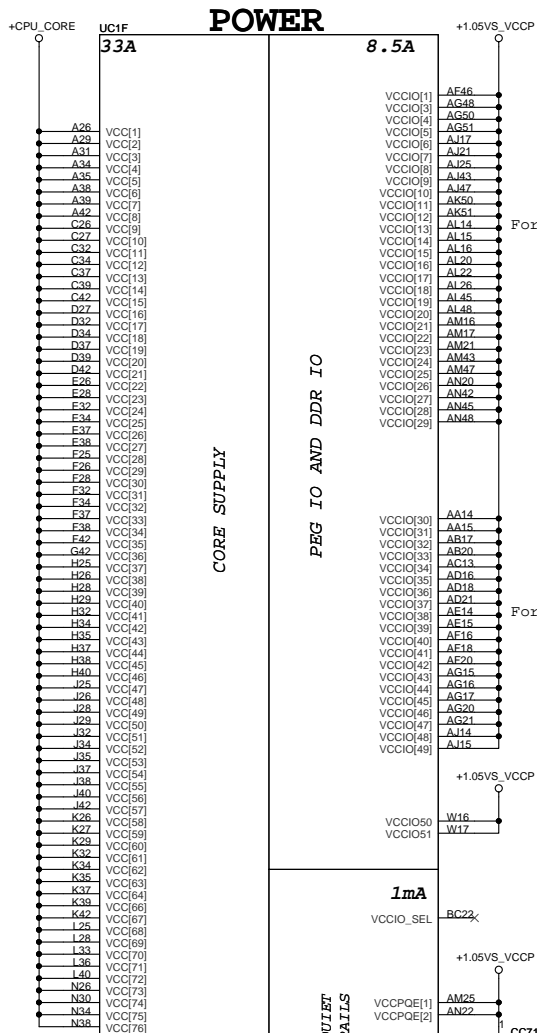


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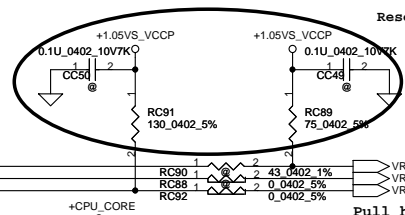
PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils typical impedance = 43 m ohm (4 mils)
 PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 m ohm (12 mils)

	PEG	DG suggest AC cap
IVY Bridge	Gen1/Gen2	75 nF-265 nF
	Gen3	180 nF-265 nF
SANDY Bridge	Gen1/Gen2	180 nF-265 nF
NV N13X	Gen1/2/3	Suggest 220 nF

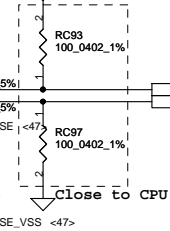


For DDR

For PEG



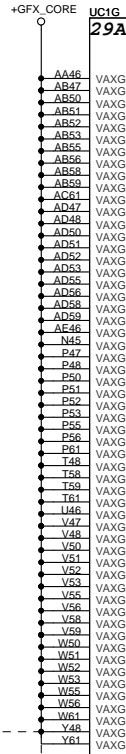
Full high resistor on VR side



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Title		
Ivy Bridge_POWER-1		
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POWER



VREF

5A

DDR3 - 1.5V RAILS

1mA

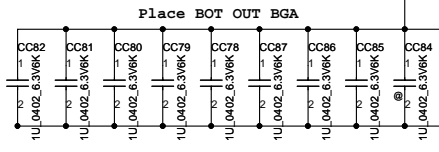
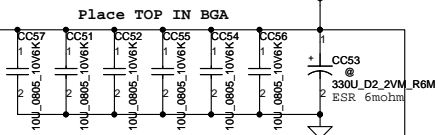
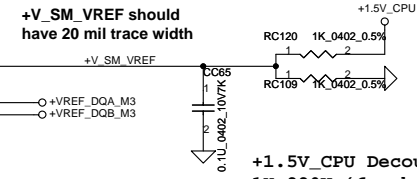
QUIET RAILS

SENSE LINES

1.8V RAIL

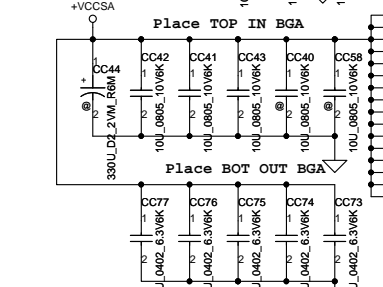
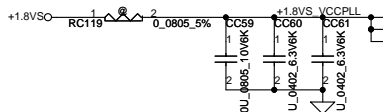
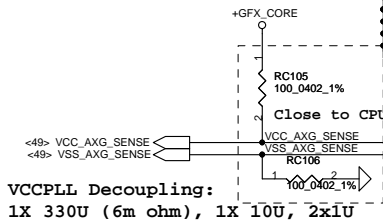
SA RAIL

VCCSA VID Lines



VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.90 V
0	1	0.80 V
1	0	0.725 V
1	1	0.675 V

For Sandy Bridge

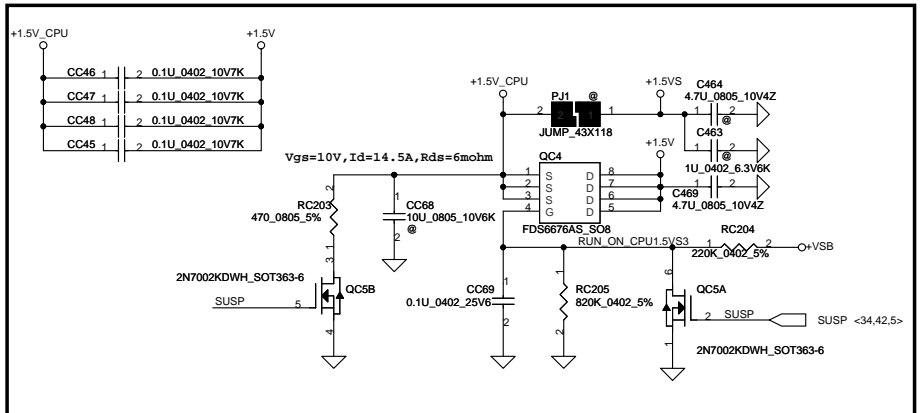
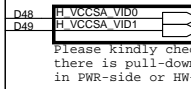
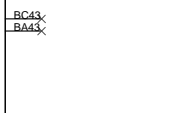
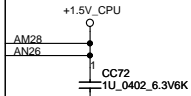


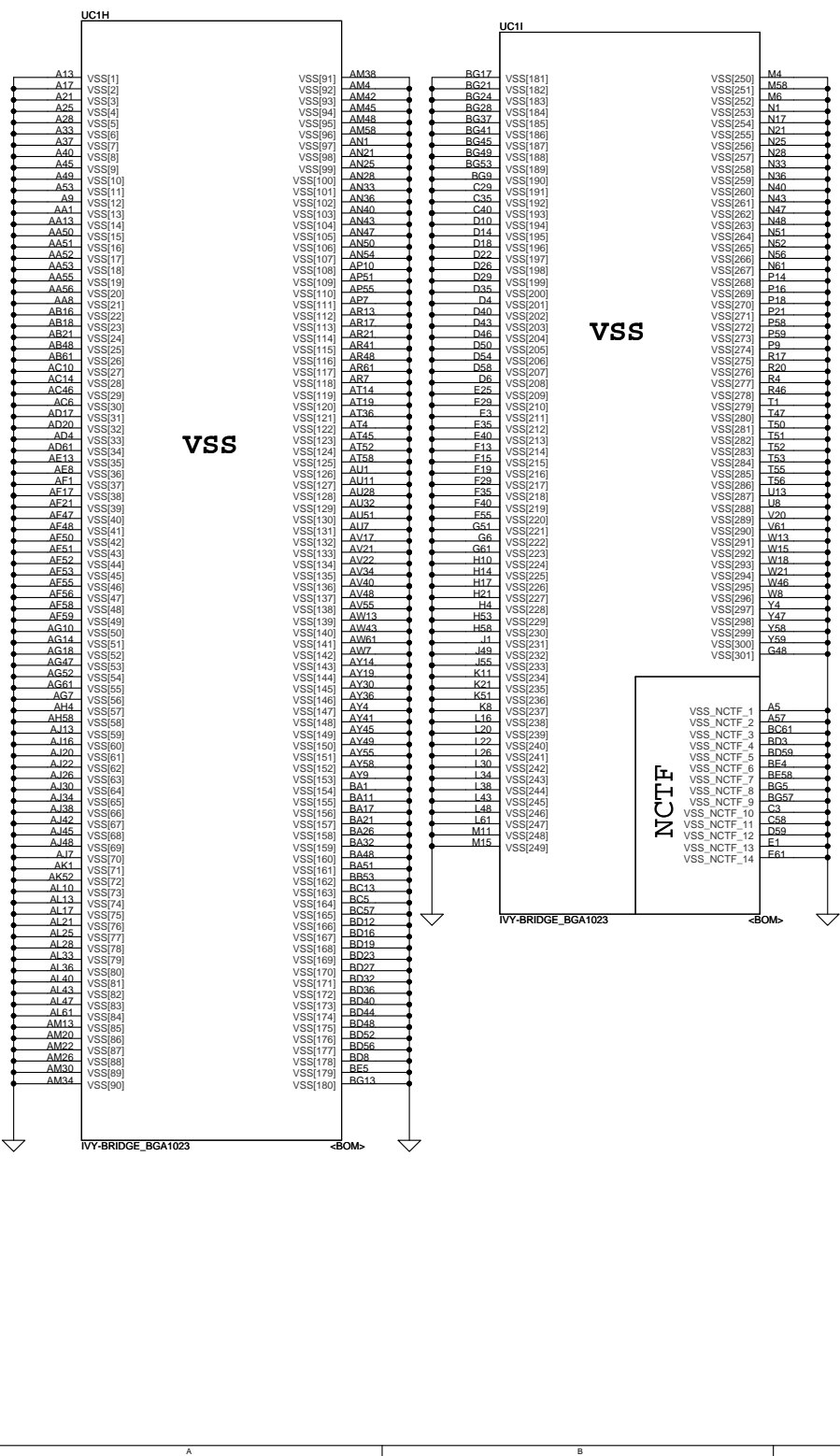
+VCCSA Decoupling:
1X 330U (6m ohm), 3X 10U, 5X 1U

1.2A

6A

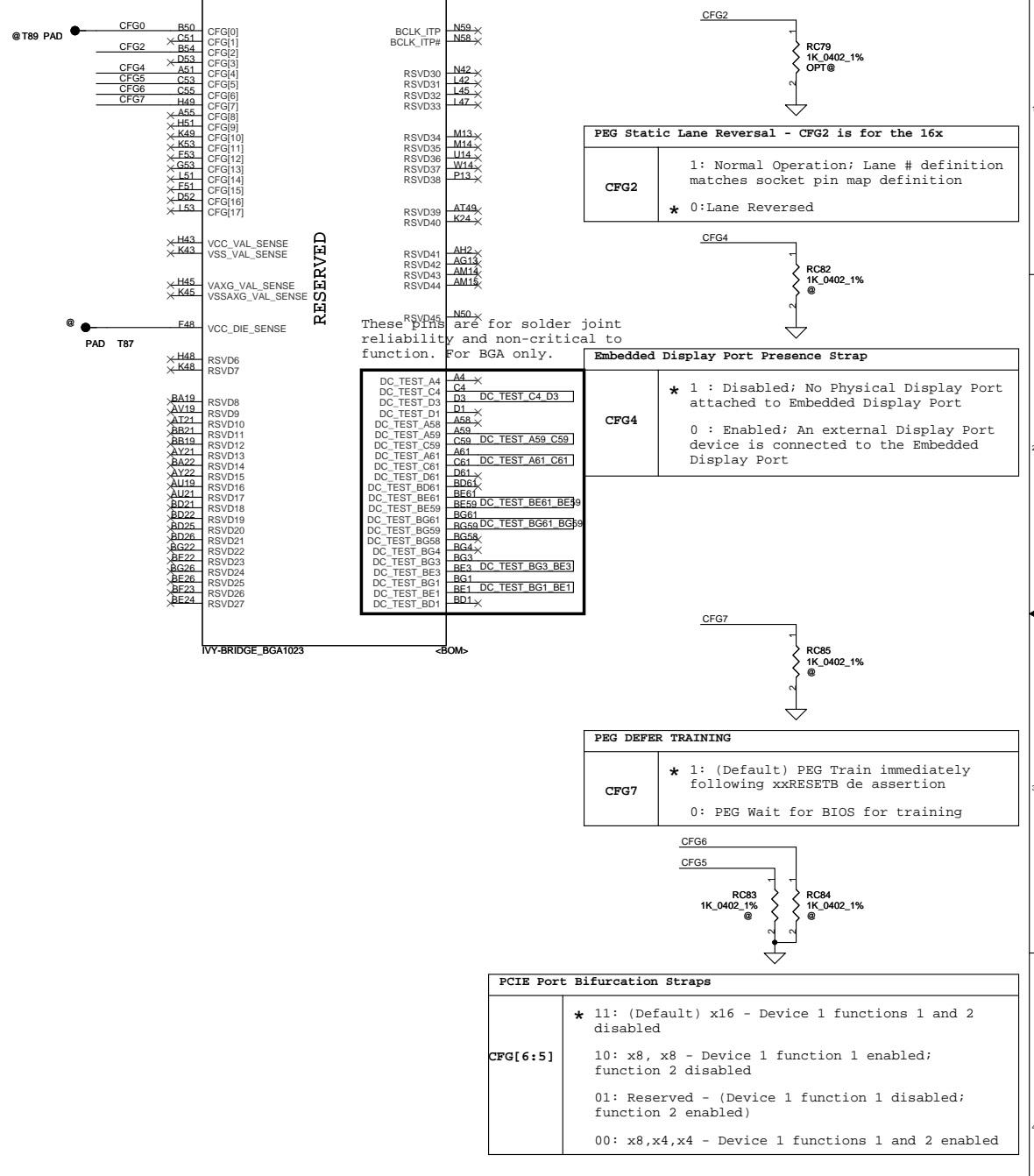
Ivy-Bridge_BGA1023

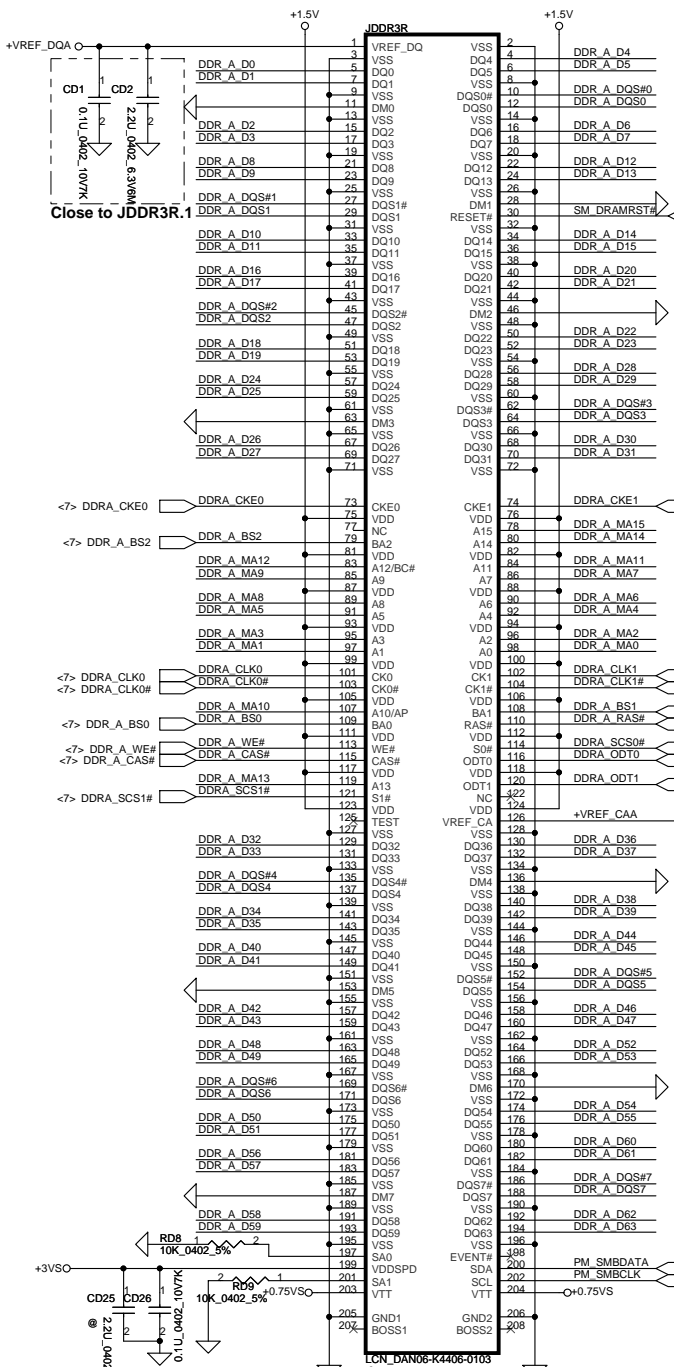




CFG Straps for Processor

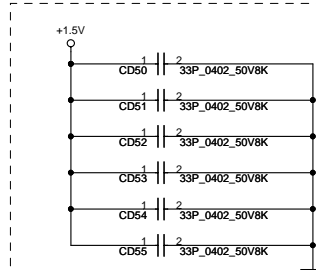
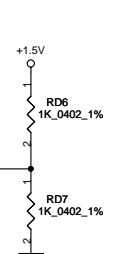
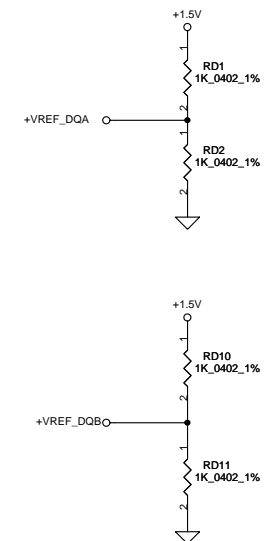
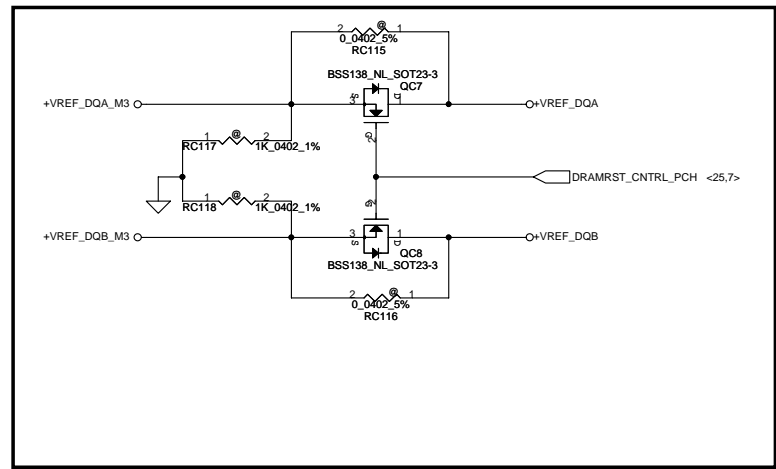
(CFG[17:0] internal pull high 5-15K to VCCIO)



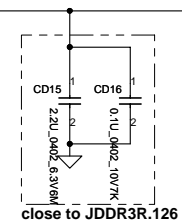


DDR3 SO-DIMM A Reverse Type

Intel DDR Vref M3



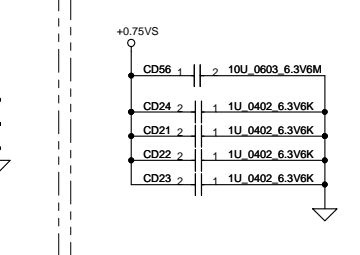
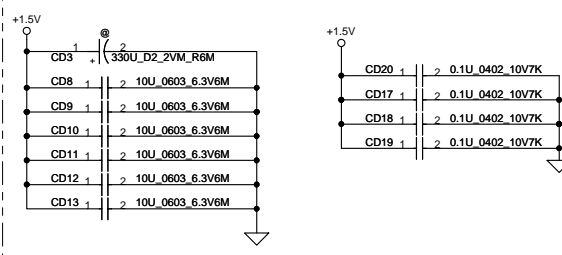
please place these caps near the reference power plane of CMD/AD



Layout Note: Place near JDDRH

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

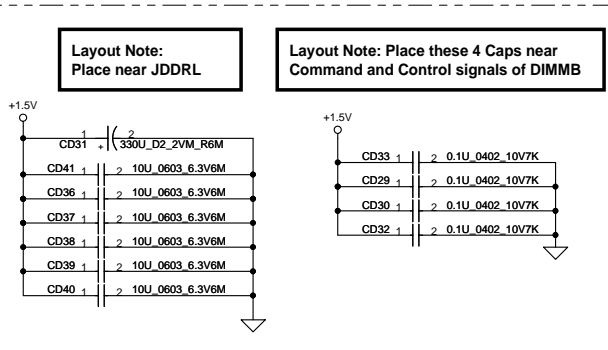
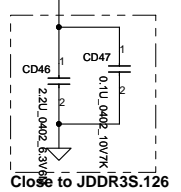
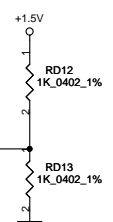
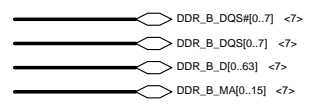
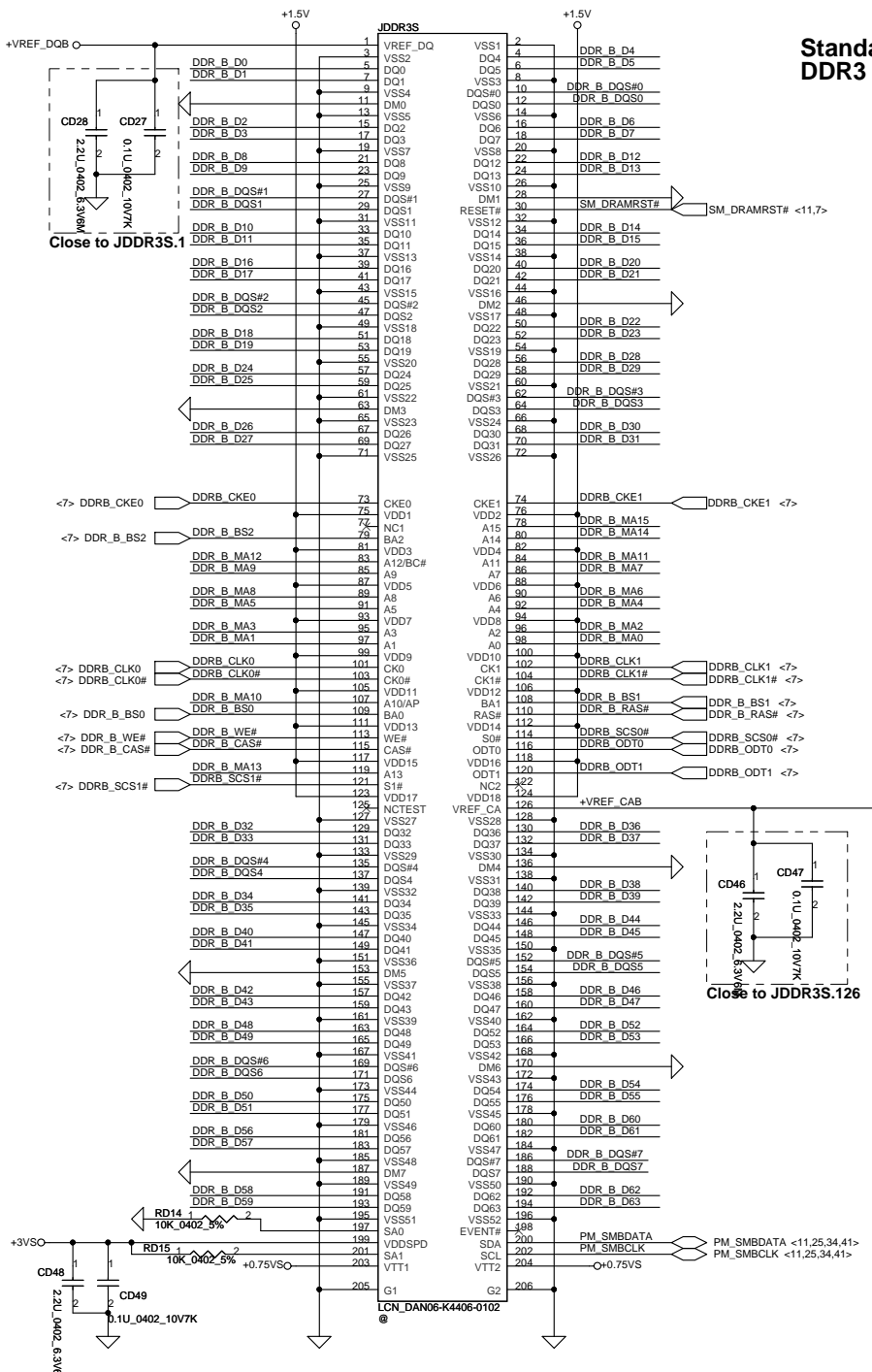
Layout Note: Place near JDDRH.203 and 204



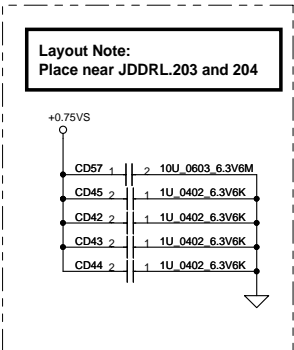
SPD setting (SA0, SA1)
 PU/PD by Channel A/B
 ->Channel A 00
 ->Channel B 01

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Standard Type DDR3 SO-DIMM B

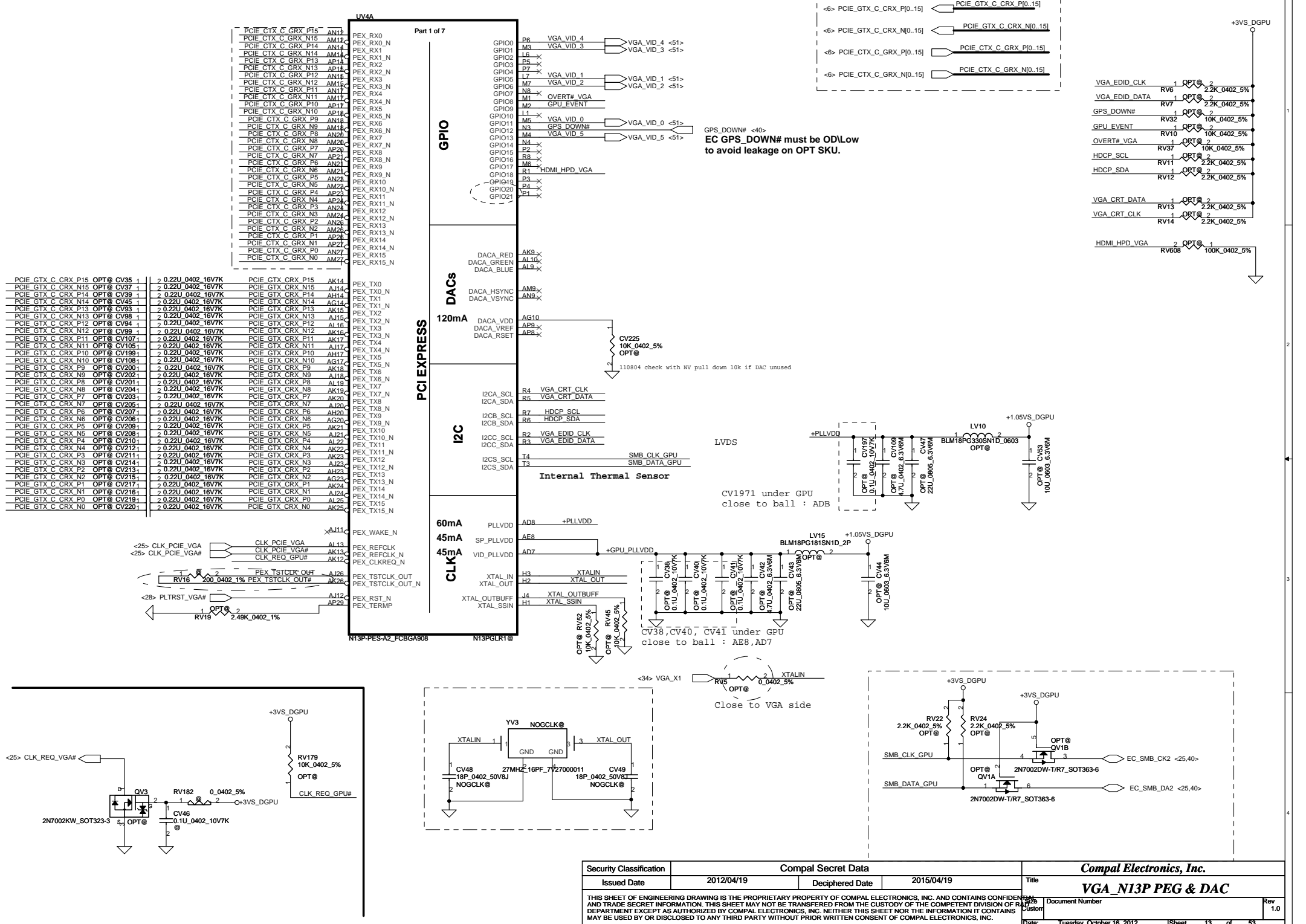


Layout Note: Place these 4 Caps near Command and Control signals of DIMMB

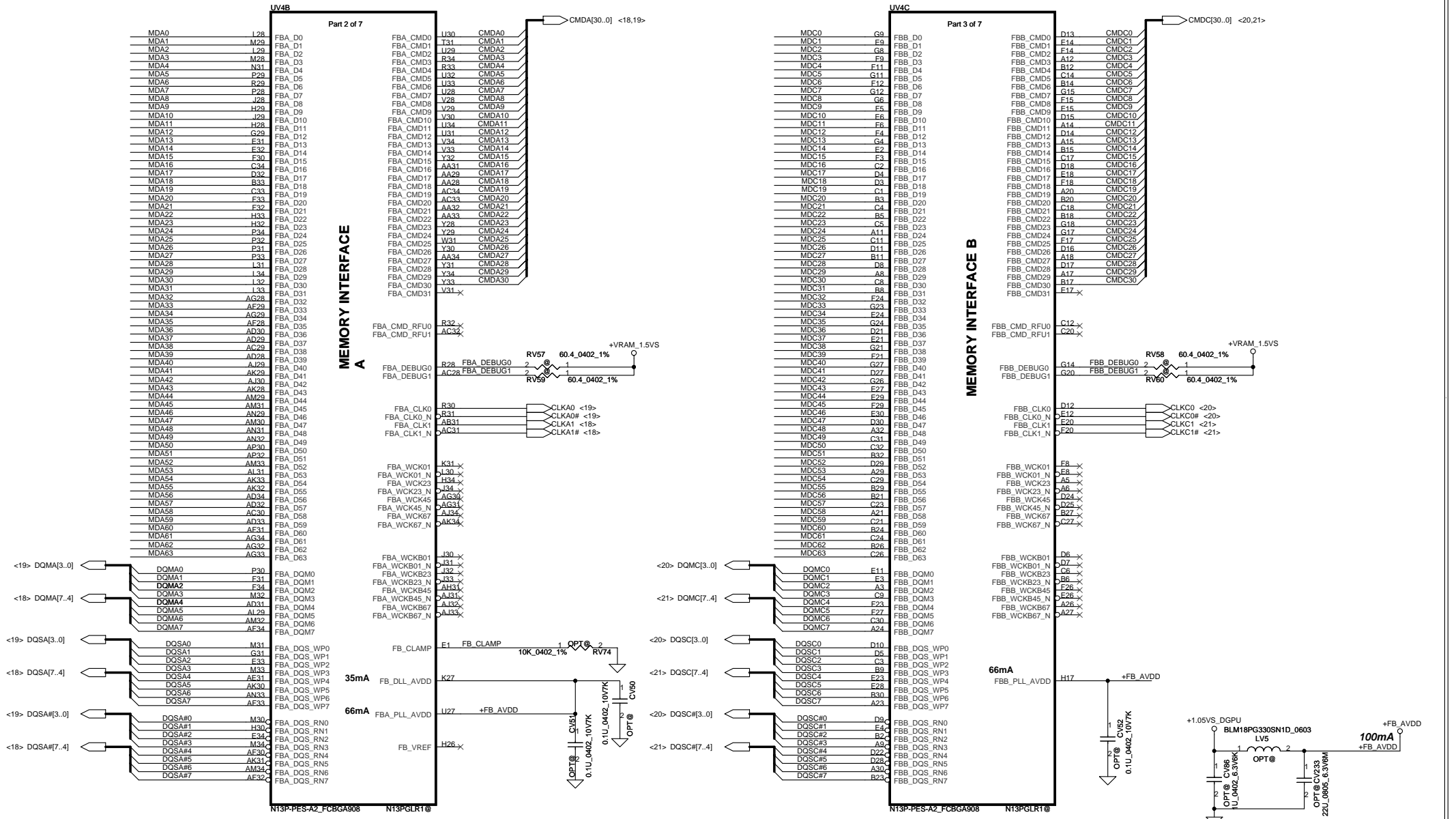
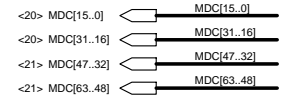
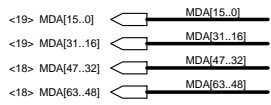


SPD setting (SA0, SA1)
PU/PD by Channel A/B
->Channel A 00
->Channel B 01

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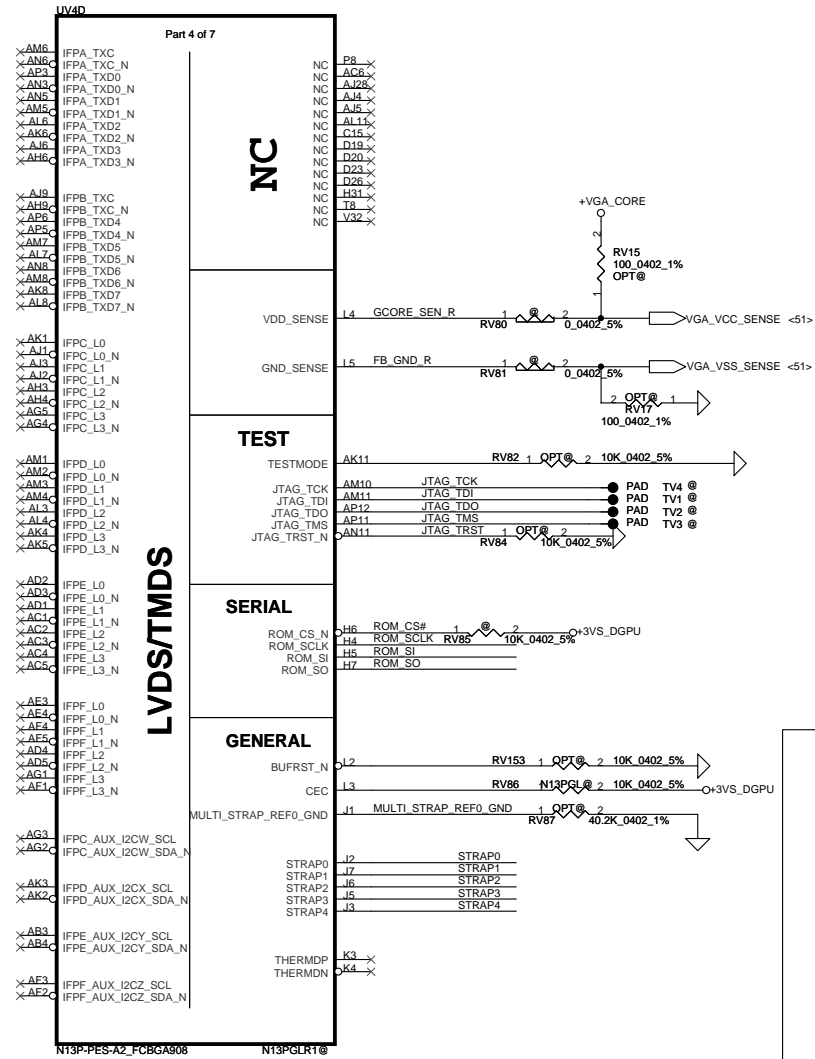


VRAM Interface



12mil

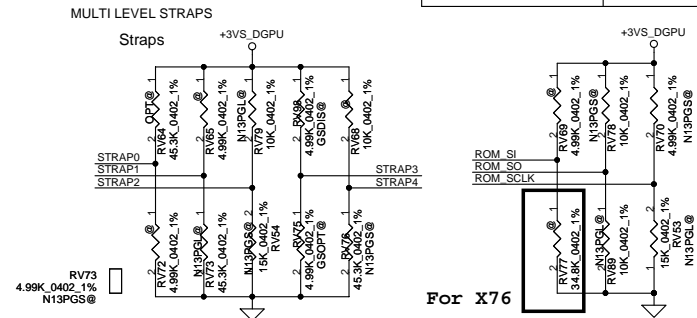
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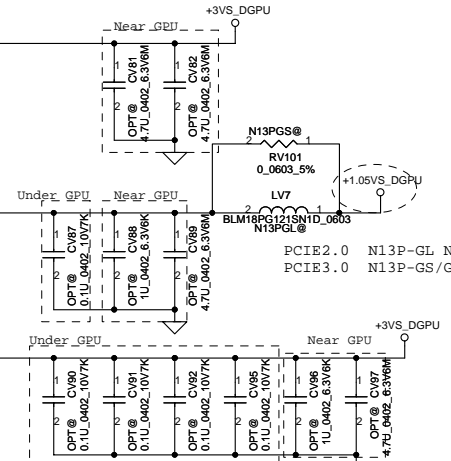
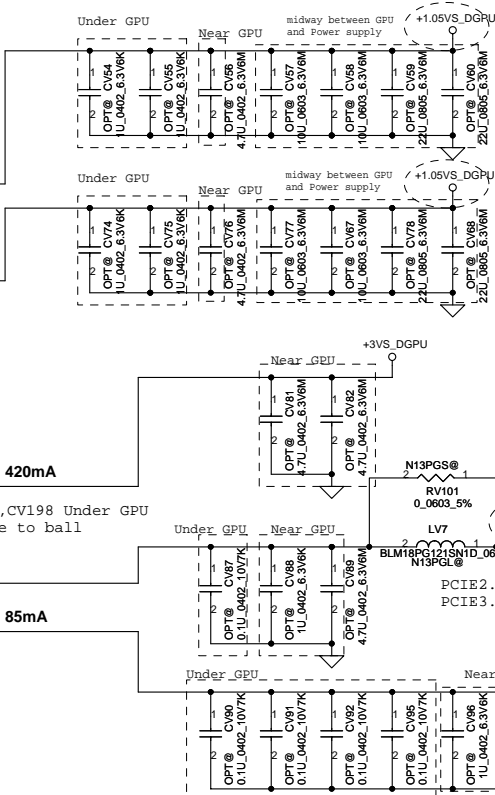
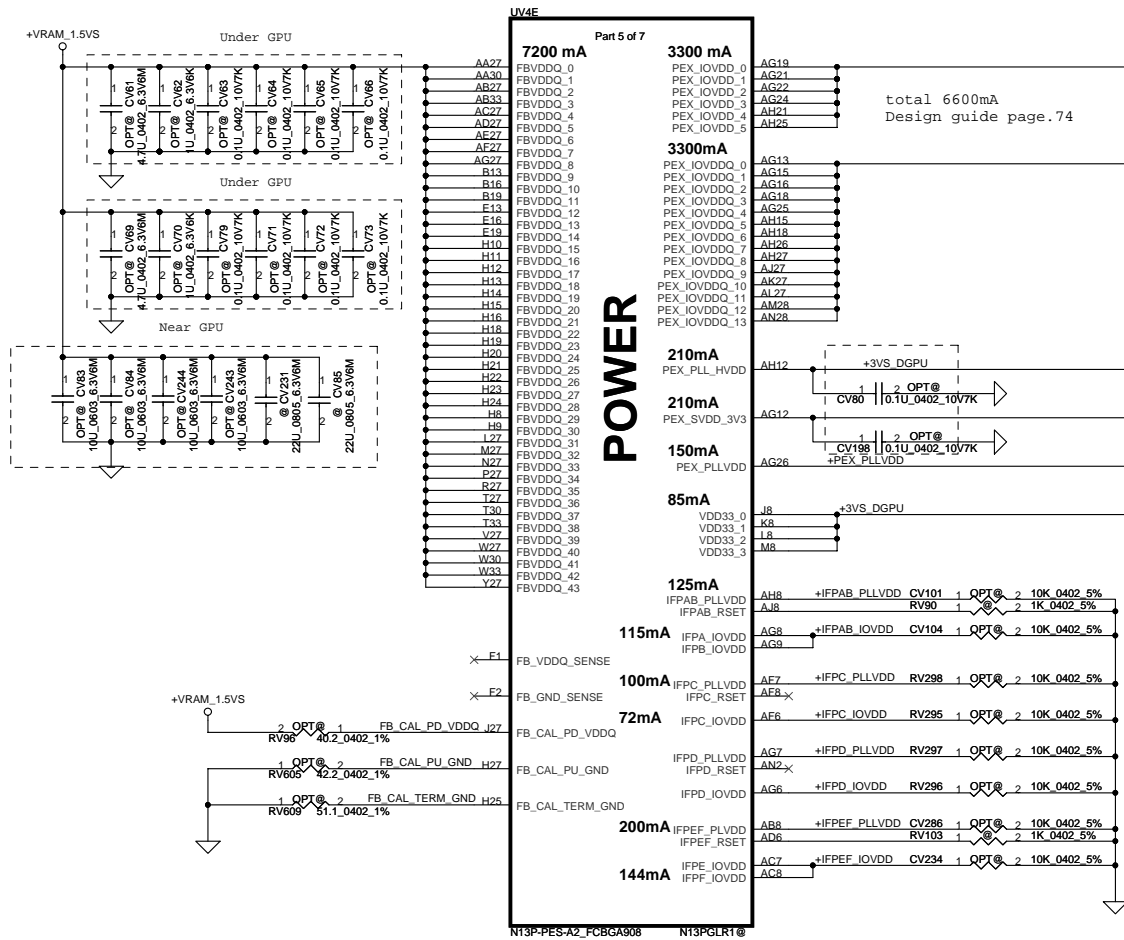
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	XCLK_417 for GL, FB[1]	FB_0_BAR_SIZE for GL, FB[0]	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG for GL, PCI_DEVID[5]	PEX_PLLEN_TERM
ROM_SI	+3VS_DGPU	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VS_DGPU	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_DGPU	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_DGPU	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

SKU	Device ID	bit5 to bit0
N13P-GL ES2	0x0DE9	101001
N13P-GS ES1	0x0FDB	011011
N13P-GS QS	0x0FD2	010010

Resistor Values	Pull-up to +3VS_DGPU	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

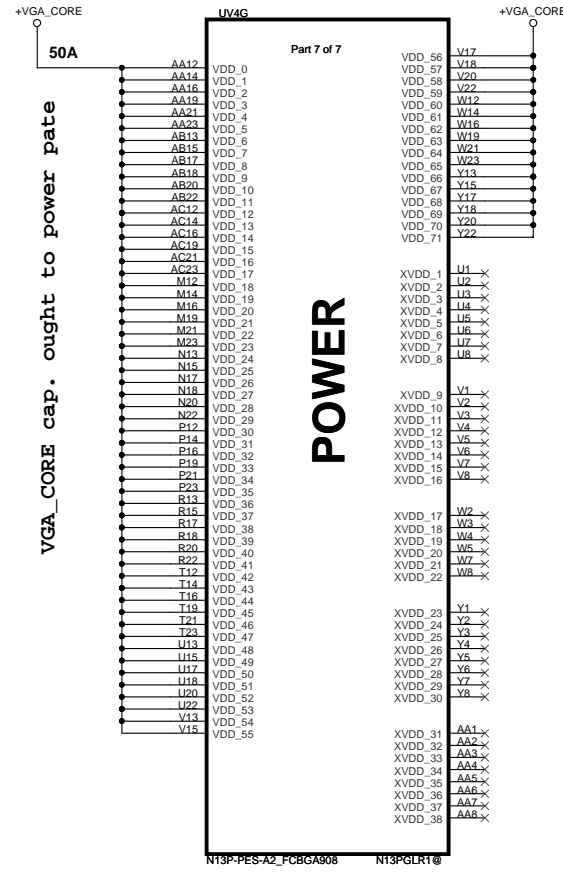
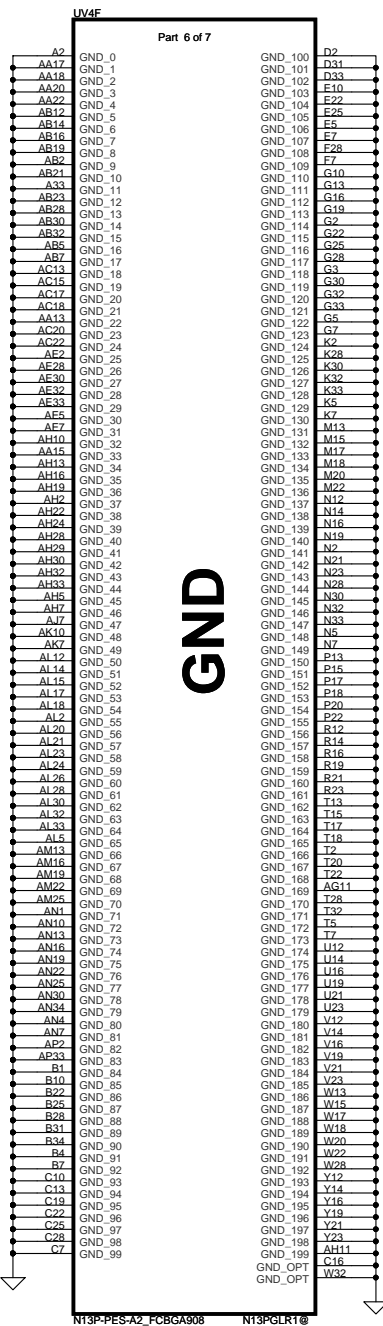


N13P-GL ROM_SI	Hynix (900MHZ)	1GB	0010	RV77 PD 15K (SD034150280)
64MX16 H5TQ1G63DFR-11C SA000041S20				
Hynix (900MHZ)	128MX16 H5TQ2G63BFR-11C SA00003Y000	2GB	0110	RV77 PD 34.8k (SD034348280)
Hynix (900MHZ)	128MX16 H5TQ2G63DFR-11C SA00003Y070	2GB	0101	RV77 PD 30k (SD034300280)
Samsung (900MHZ)	64MX16 K4W1G1646G-BC11 SA00004GS00	1GB	0011	RV77 PD 20K (SD034200280)
Samsung (900MHZ)	128M16 K4W2G1646C-HC11 SA000047Q00	2GB	0111	RV77 PD 45.3K (SD034453280)
Samsung (900MHZ)	128M16 K4W2G1646E-BC11 SA00005SH00	2GB	0001	RV77 PD 10K (SD028100280)



N13P-PES-A2_F0BGA908 N13PGL18

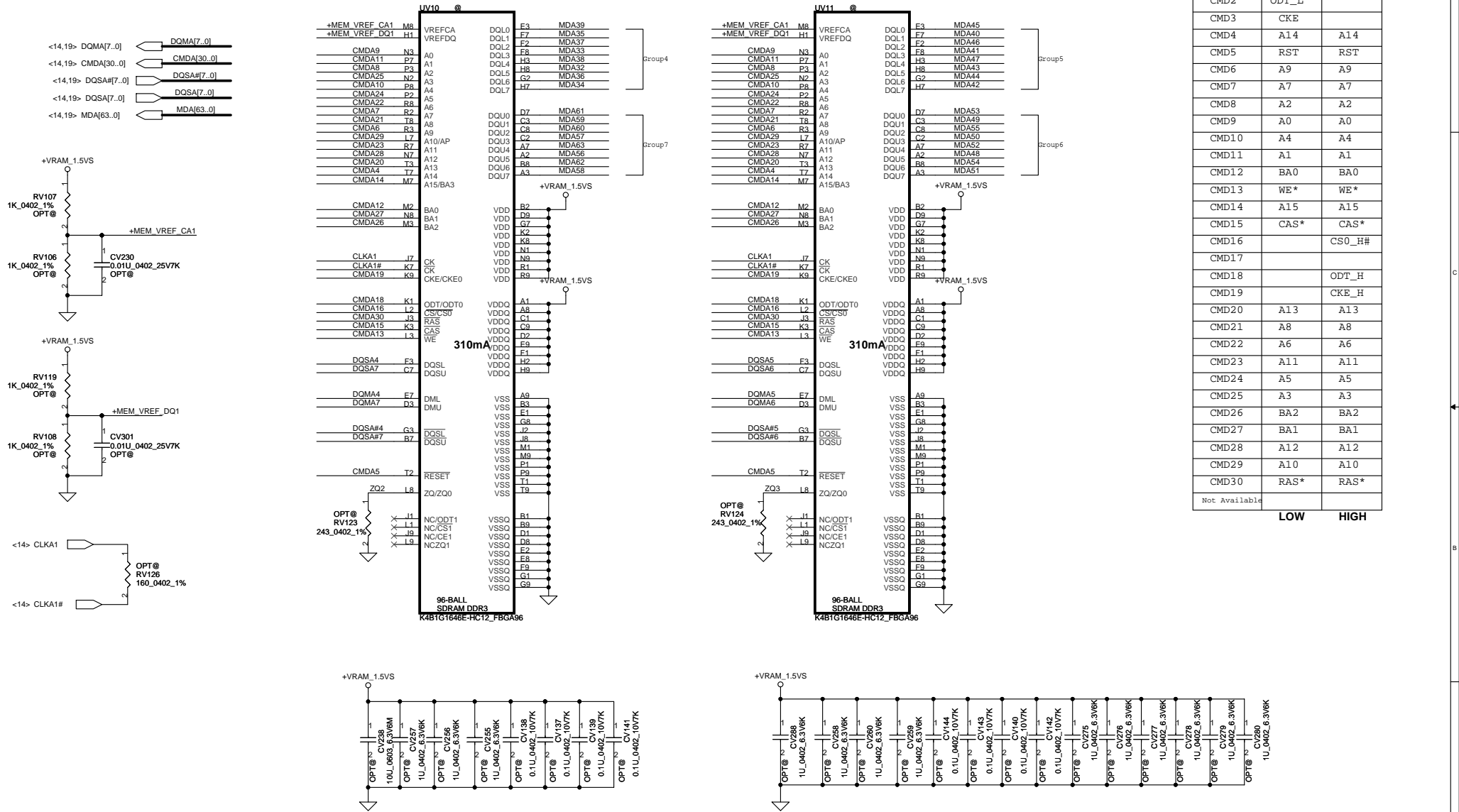
Security Classification		Compal Secret Data		Title	
Issued Date	2012/04/19	Deciphered Date	2015/04/19	VGA N13P POWER	
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Date: Tuesday, October 16, 2012				Sheet	16 of 53



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Date:	Tuesday, October 16, 2012	Sheet	17	of 53	

VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB



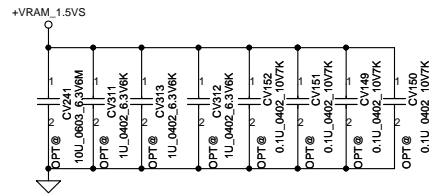
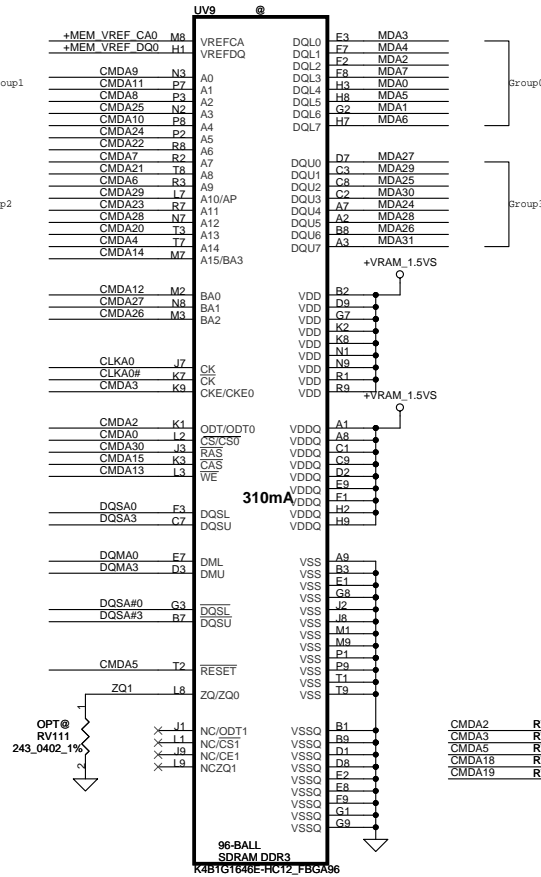
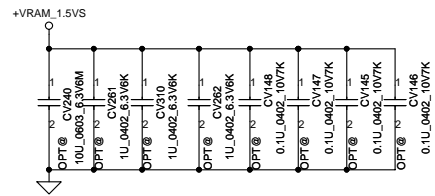
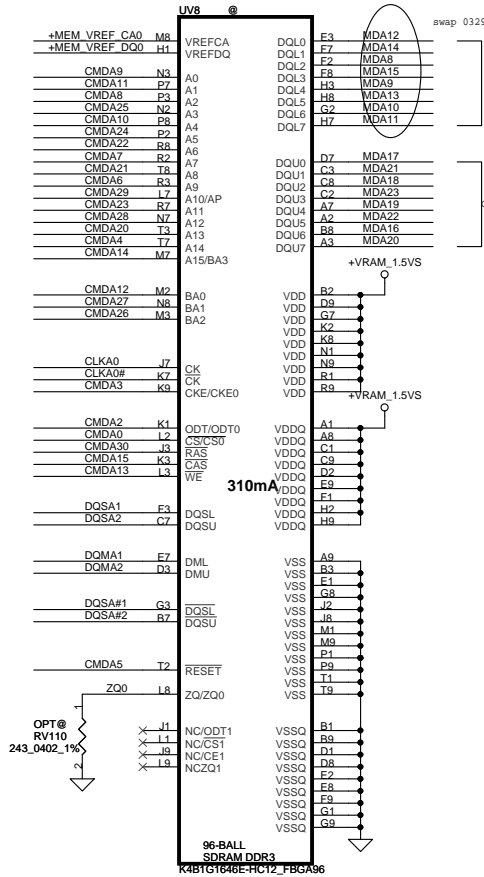
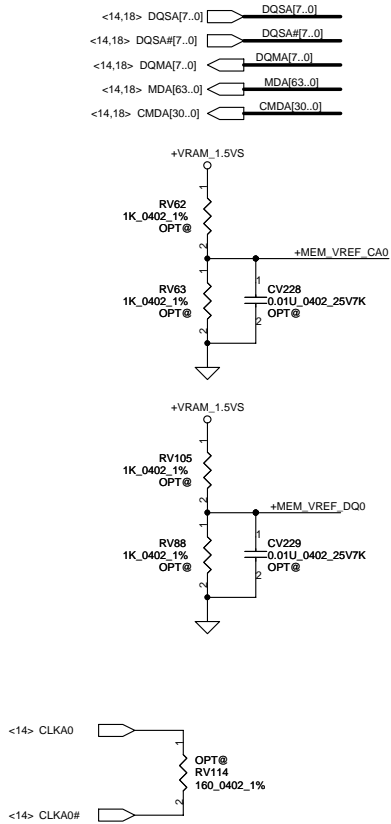
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*

LOW HIGH

Security Classification	Compal Secret Data		Title	VGA N13P VRAM Channel AH	
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Date:	Tuesday, October 16, 2012	Sheet	18	of	53

VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

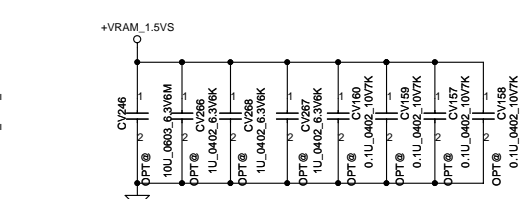
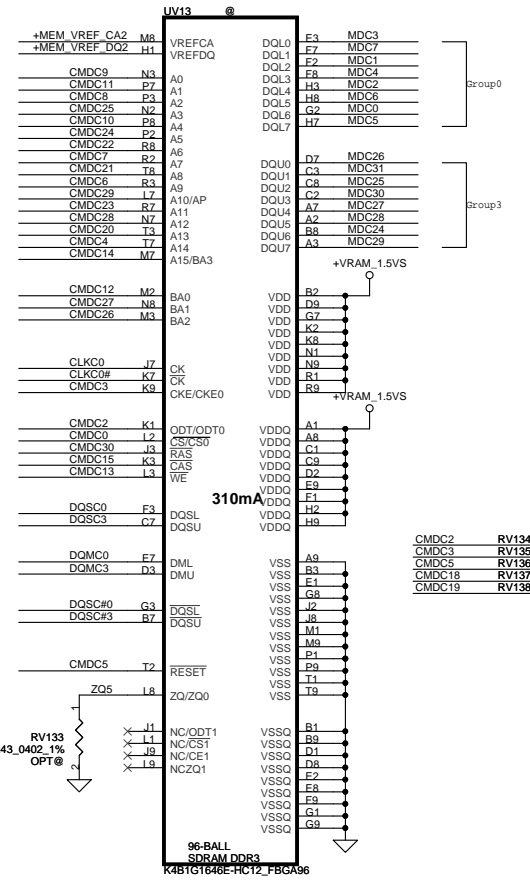
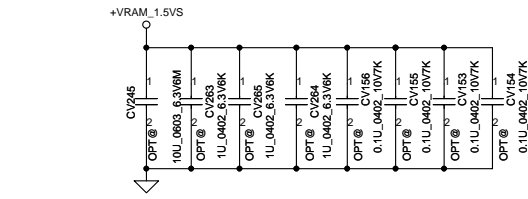
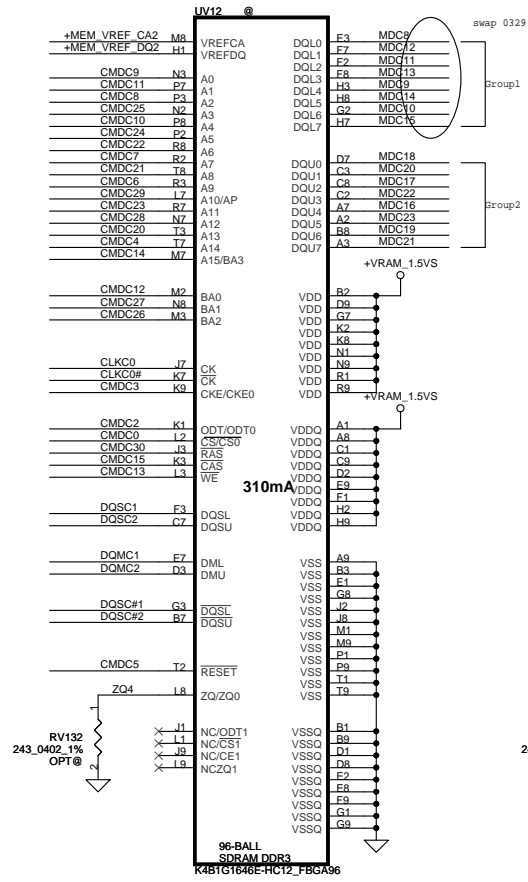
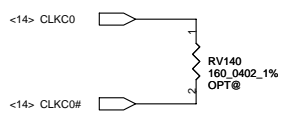
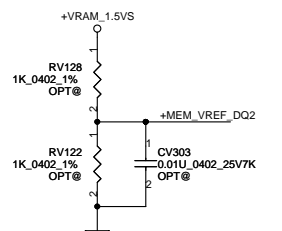
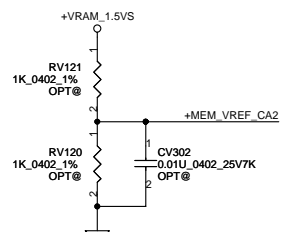
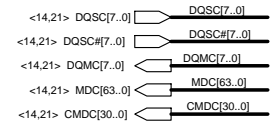


Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available	LOW	HIGH

Command Bit	Default Pull-down
ODTx	10k
CKEx	10k
RST	10k
CS*	No Termination

VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

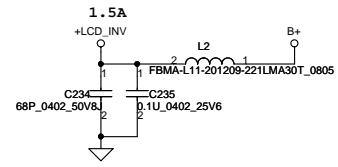
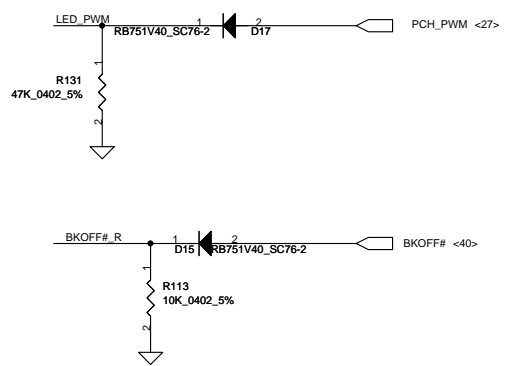
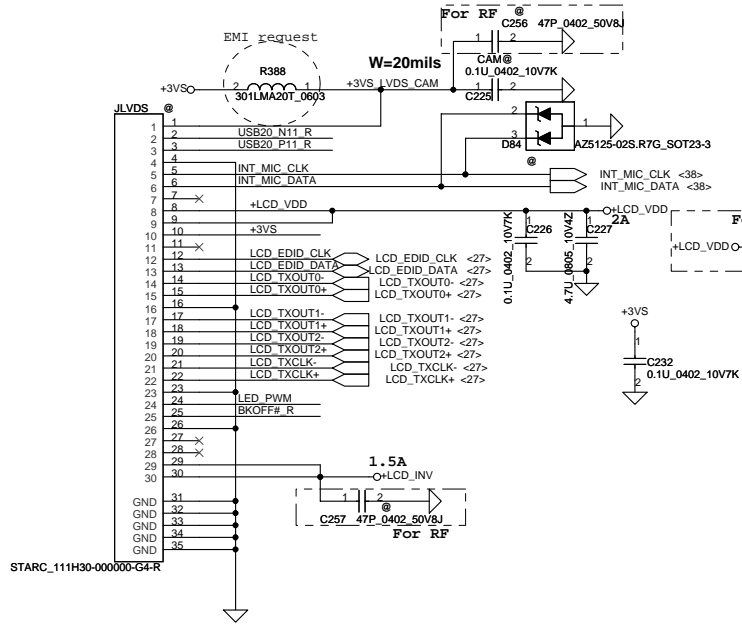
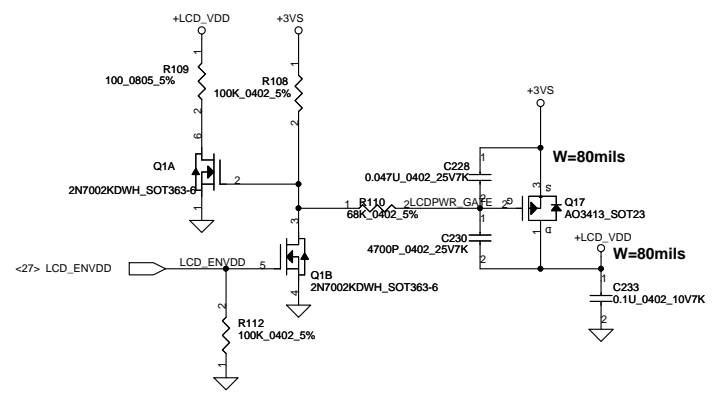
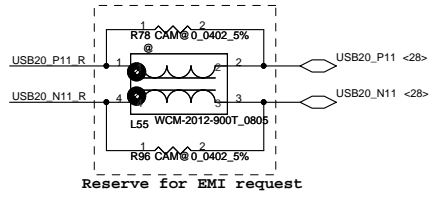


Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

LOW HIGH

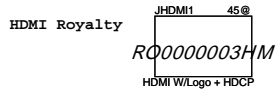
Command Bit	Default Full-down
ODTx	10k
CKEx	10k
RST	10k
CS*	No Termination

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Date:	Tuesday, October 16, 2012	Sheet	20	of 53

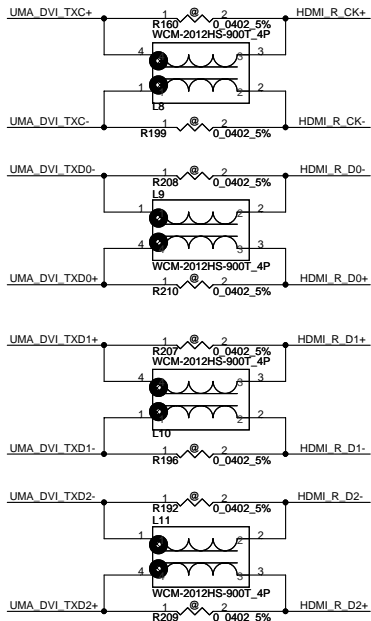
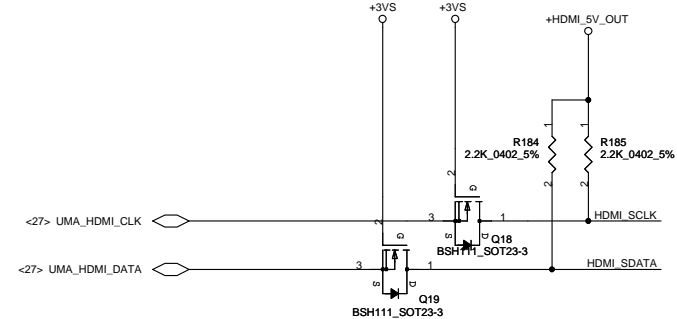


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			Sheet 22 of 53	Rev 1.0

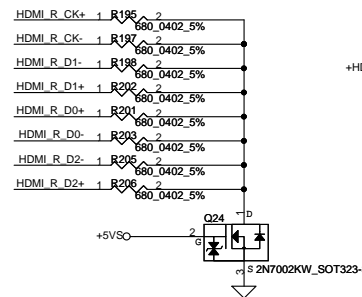
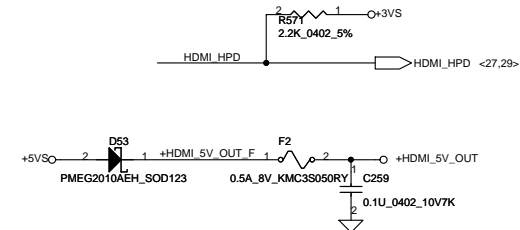
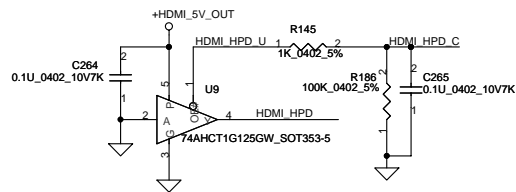
<27> UMA_HDMI_TXC+	CV336	1	2	0.1U_0402_10V7K	UMA DVI_TXC+
<27> UMA_HDMI_TXC-	CV337	1	2	0.1U_0402_10V7K	UMA DVI_TXC-
<27> UMA_HDMI_TX0+	CV338	1	2	0.1U_0402_10V7K	UMA DVI_TXD0+
<27> UMA_HDMI_TX0-	CV339	1	2	0.1U_0402_10V7K	UMA DVI_TXD0-
<27> UMA_HDMI_TX1+	CV340	1	2	0.1U_0402_10V7K	UMA DVI_TXD1+
<27> UMA_HDMI_TX1-	CV341	1	2	0.1U_0402_10V7K	UMA DVI_TXD1-
<27> UMA_HDMI_TX2+	CV342	1	2	0.1U_0402_10V7K	UMA DVI_TXD2+
<27> UMA_HDMI_TX2-	CV343	1	2	0.1U_0402_10V7K	UMA DVI_TXD2-



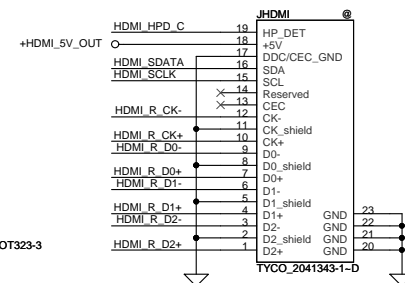
HDMI W/O Logo: RO0000001HM
HDMI W/Logo: RO0000002HM
HDMI W/Logo + HDCP: RO0000003HM



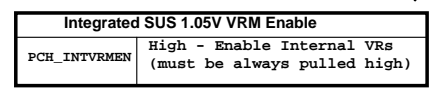
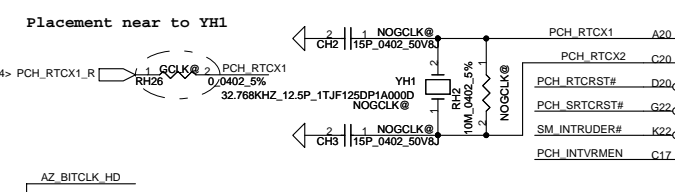
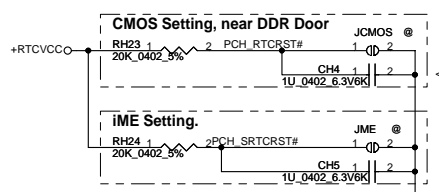
common CHOKE use 67ohm
5/30 change to 90ohm EMI request



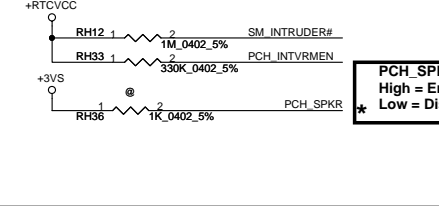
HDMI Connector



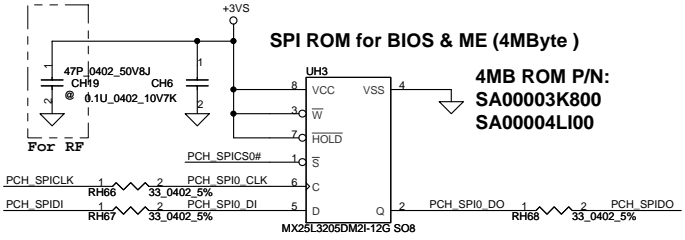
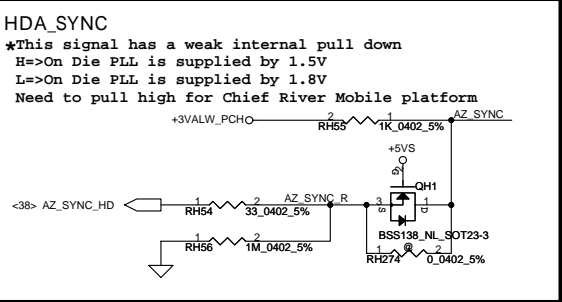
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				VCUAA	1.0
Date: Tuesday, October 16, 2012				Sheet	23 of 53



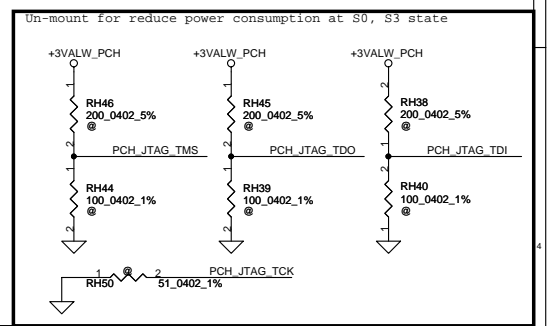
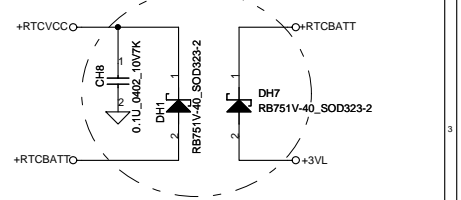
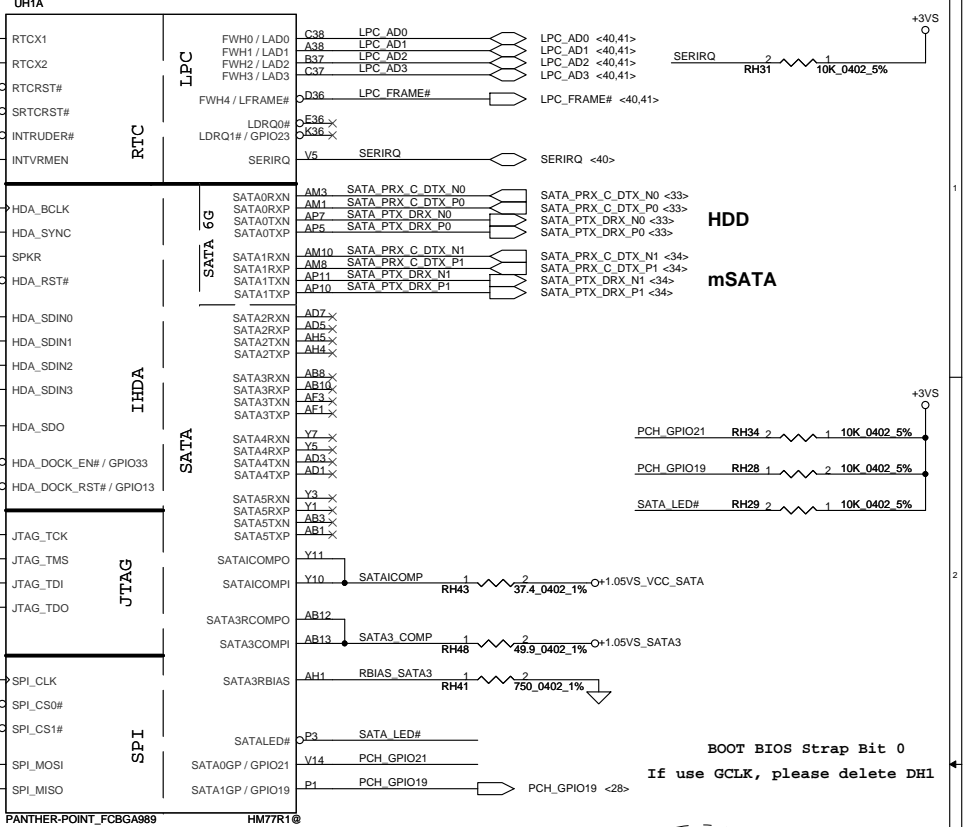
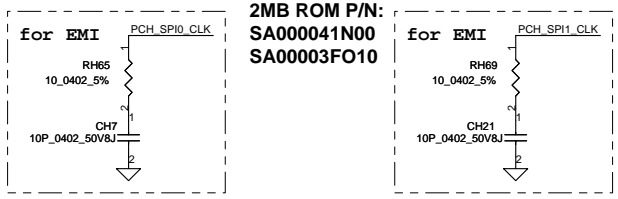
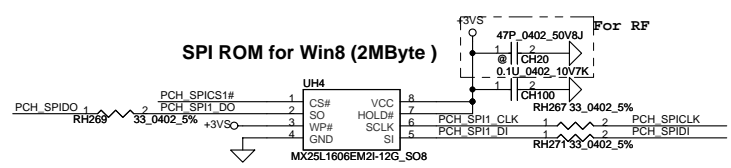
PCH_SPKR
 High = Enabled "No Reboot Mode"
 Low = Disabled (Default)



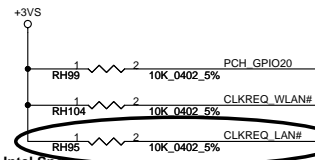
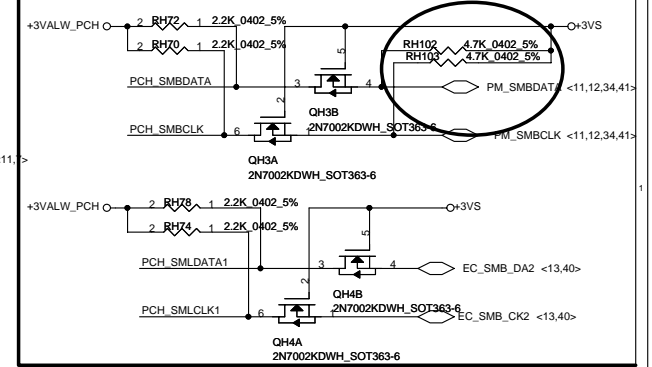
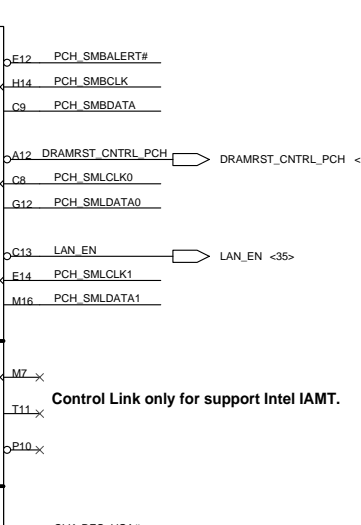
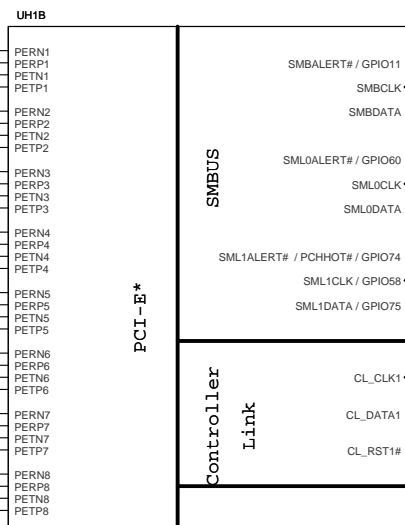
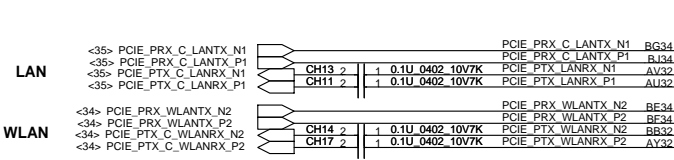
HDA_SDO
 ME debug mode,
 this signal has a weak internal pull down
 *Low = Disable (default)
 High = Enable (flash descriptor security override)



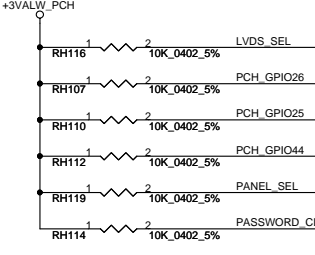
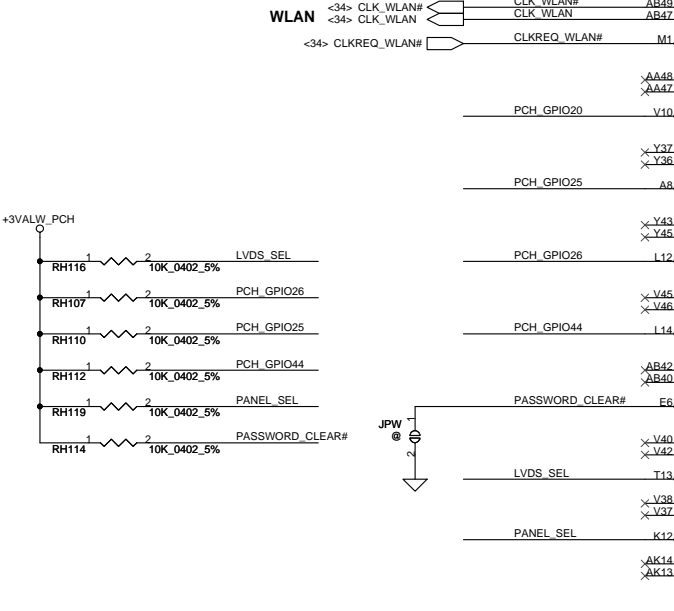
Socket: SP07000F500/SP07000H900
 Please place U13 & U4 close to U2 PCH,
 please place RH66, RH67, RH68 near UH3
 Please place RH267 near RH66, Please place RH271 near RH67,
 Please place RH269 near RH68.



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Intel Spec.
PCIECLK_RQ0# is supend well,
but we pull high to +3VS
for LAN en/disable function



LVDS_SEL

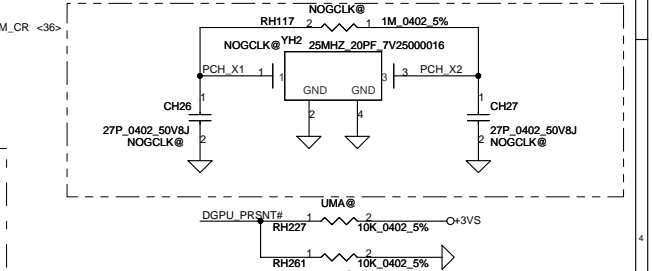
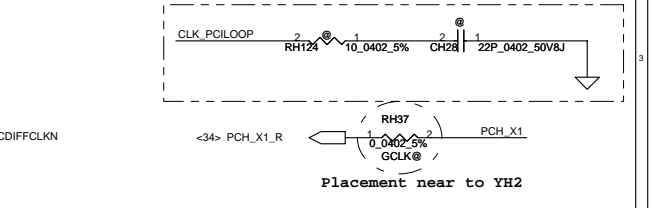
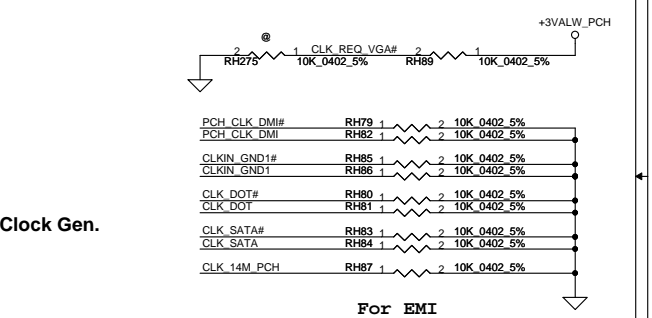
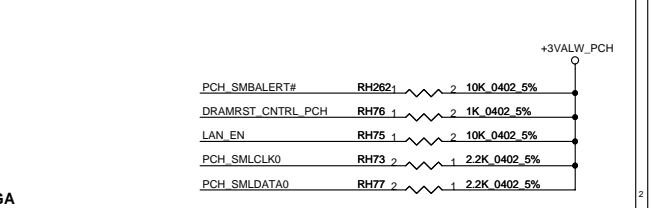
LVDS_SEL	H	L
Channel	Single (Default)	Dual

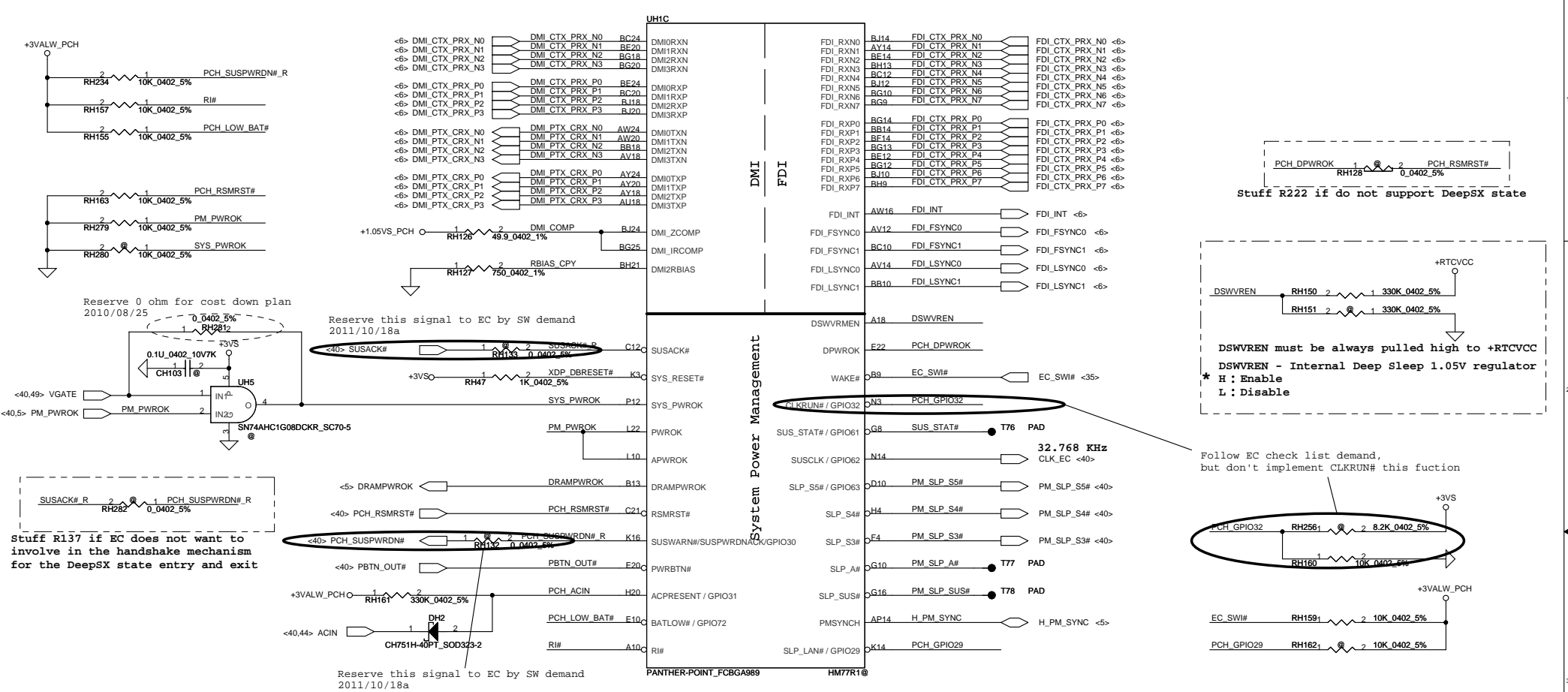
PANEL_SEL

PANEL_SEL	H	L
Channel	LVDS	EDP

DGPU_PRSENT#

DGPU_PRSENT#	H	L
M/B SKU	UMA	DIS/OPT





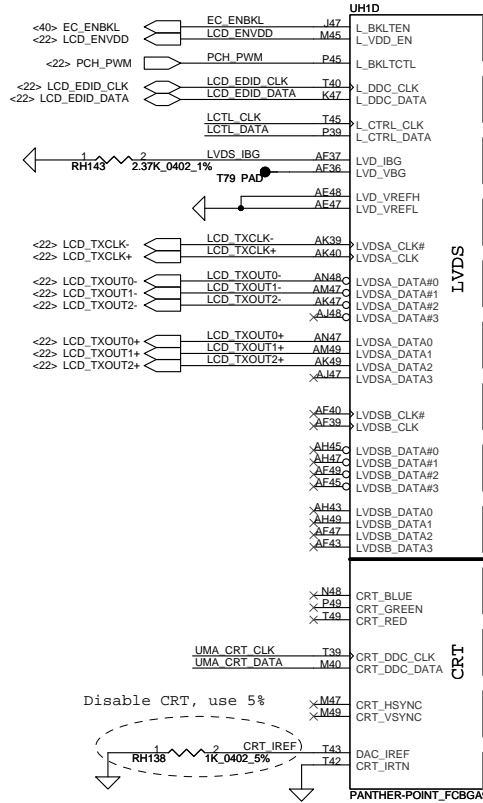
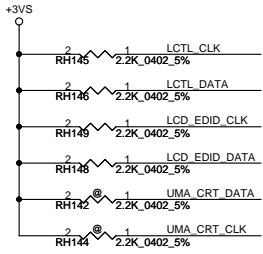
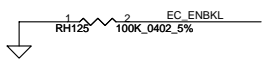
stuff R137 if EC does not want to involve in the handshake mechanism for the DeepSX state entry and exit

stuff R222 if do not support DeepSX state

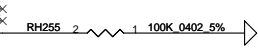
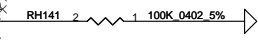
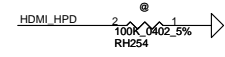
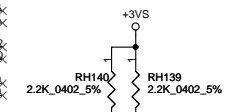
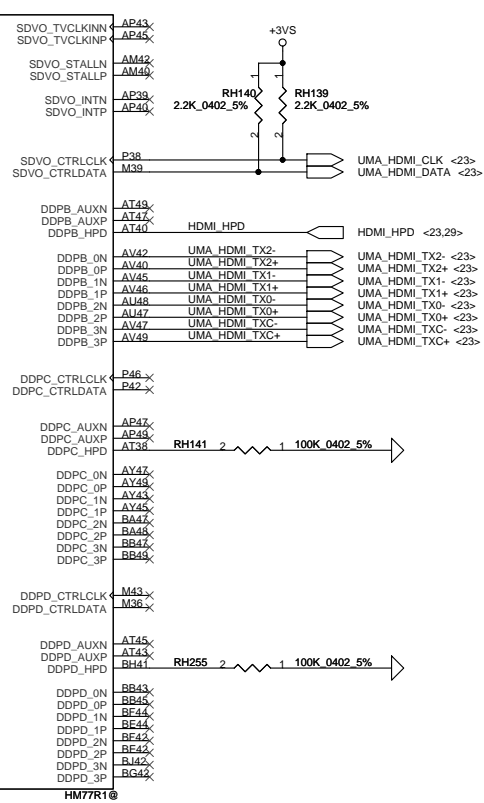
DSWMREN must be always pulled high to +RTCVCC
 * H : Enable
 L : Disable

Follow EC check list demand, but don't implement CLKRUN# this fuction

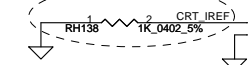
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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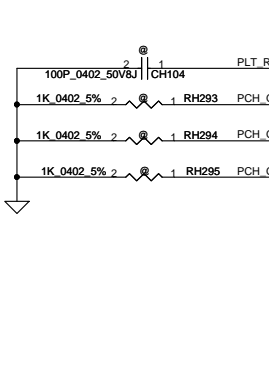
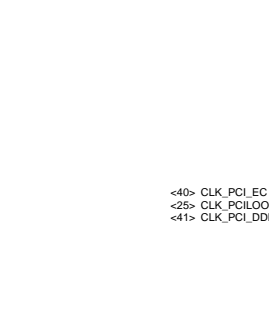
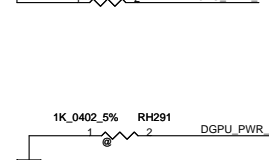
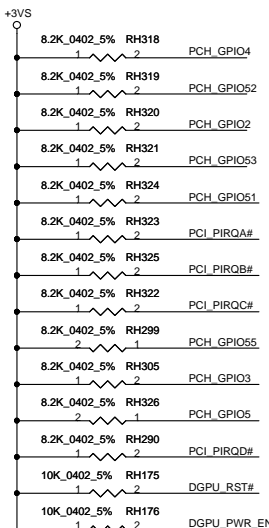
Digital Display Interface



Disable CRT, use 5%

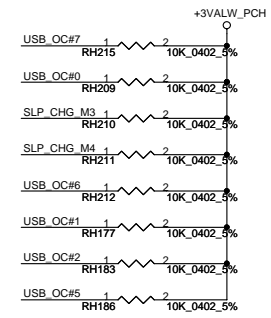
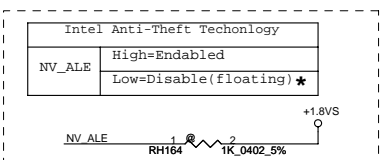
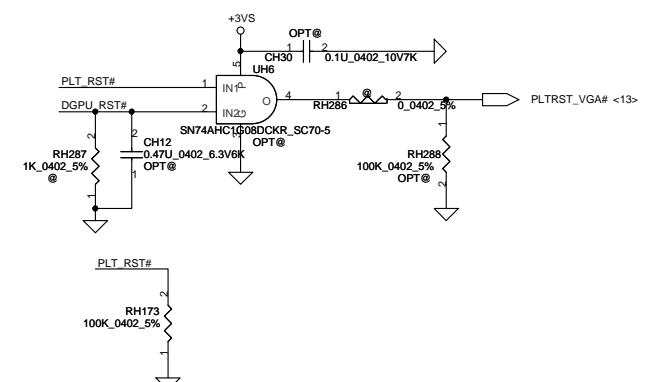
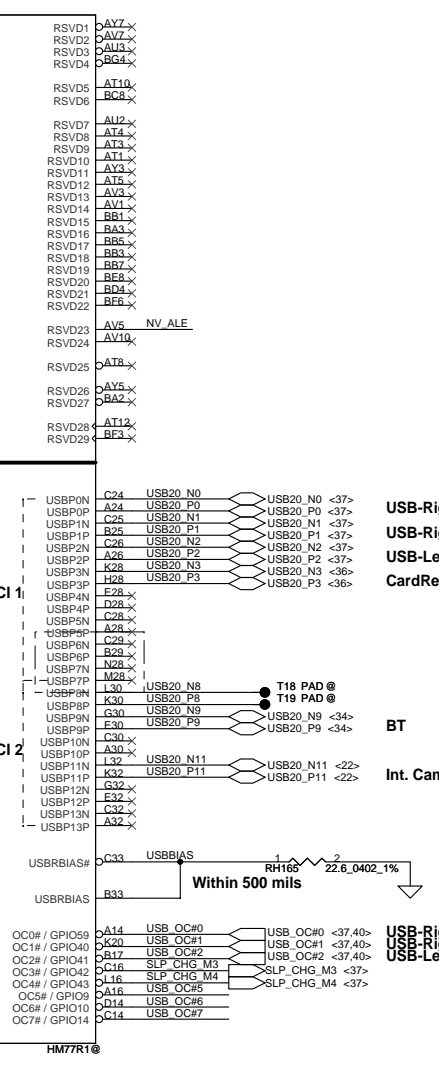
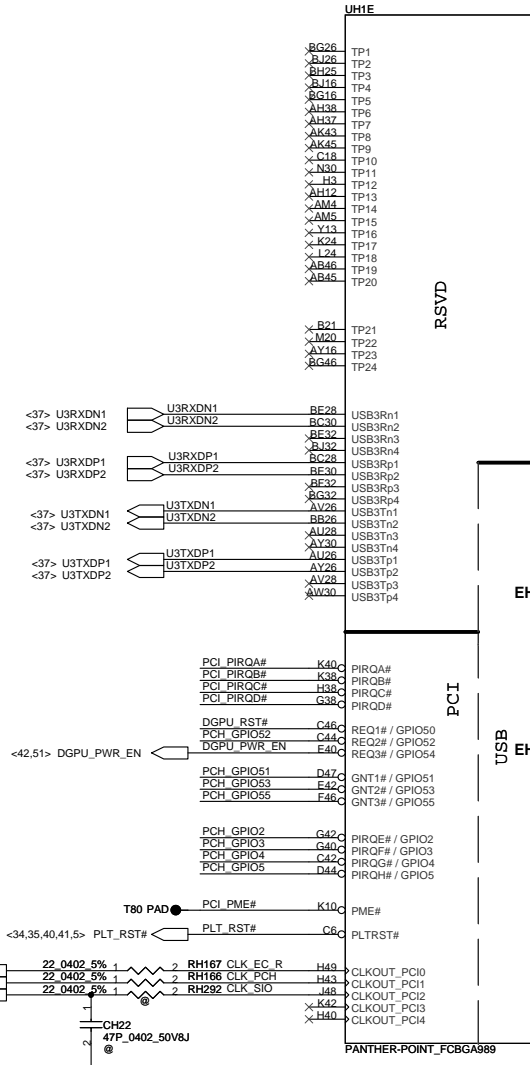


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RE_OFF# PCH_GPIO19	PCH_GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI *

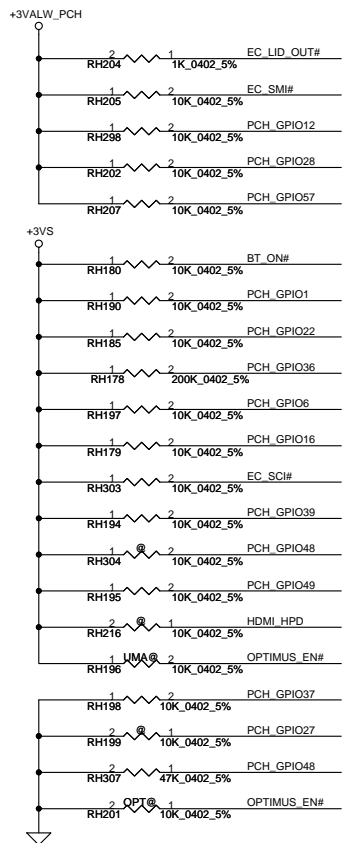
WL_OFF#	Low=A16 swap override Enable High=A16 swap override Disable
*	



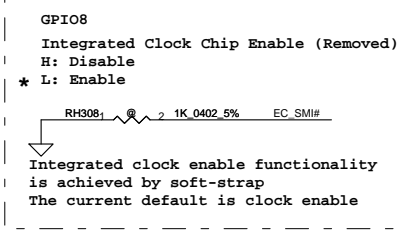
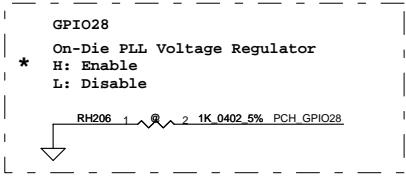
Security Classification	Compal Secret Data	
Issued Date	2012/04/19	Deciphered Date
		2015/04/19

Compal Electronics, Inc.		
PCH_PCI/USB/NAND		
Title	Document Number	Rev
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Follow Compal ORB and Intel Check list 460603 V1.5



OPTIMUS_EN#

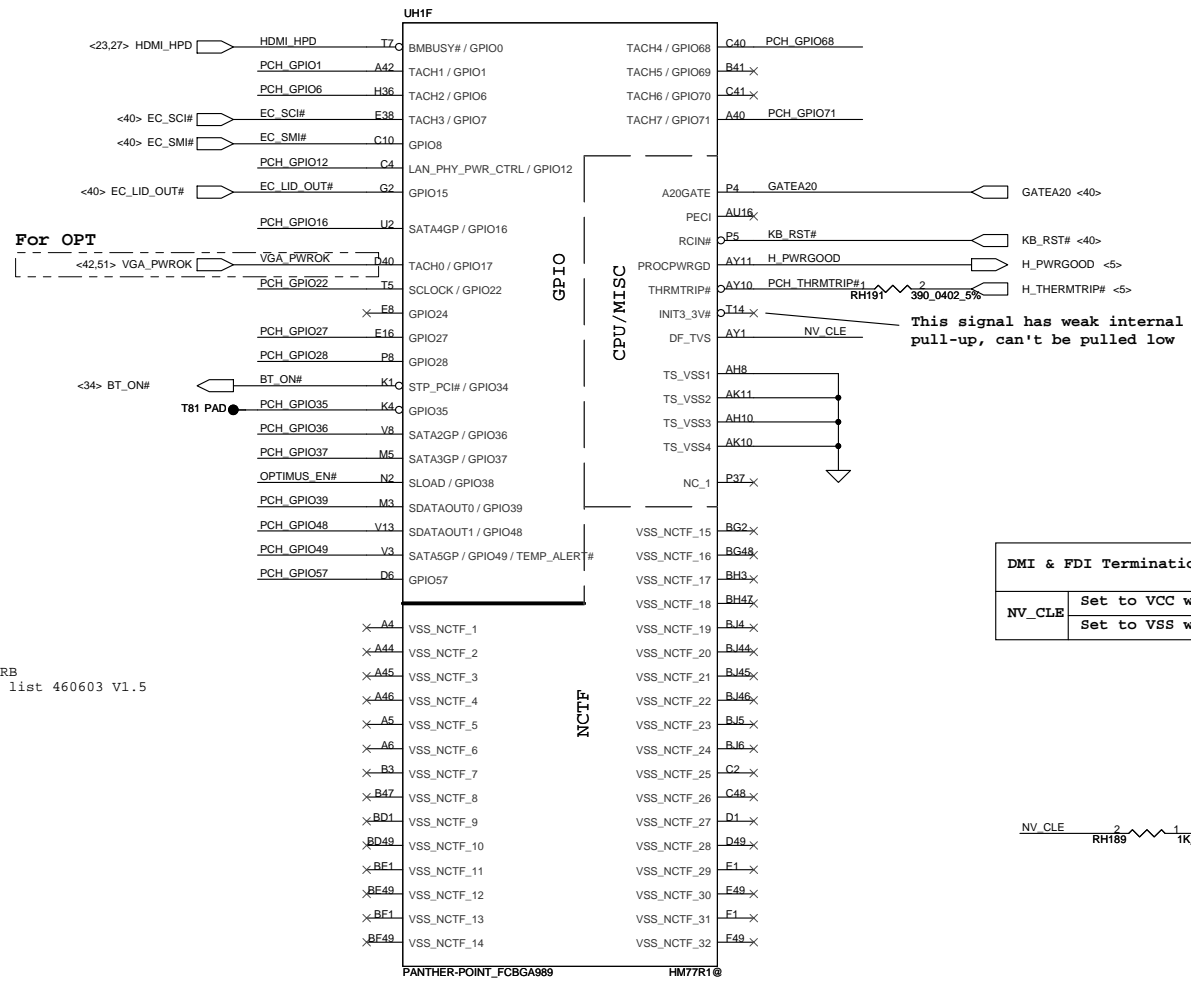
OPTIMUS_EN#	H	L
SKU	NonOPT	Optimus

PCH_GPIO57

HDD2_DET#	H	L
SKU	ONE HDD	TWO HDD

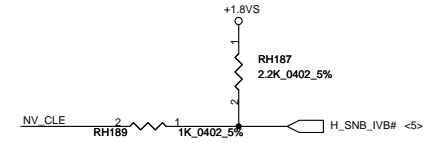
PCH_GPIO71

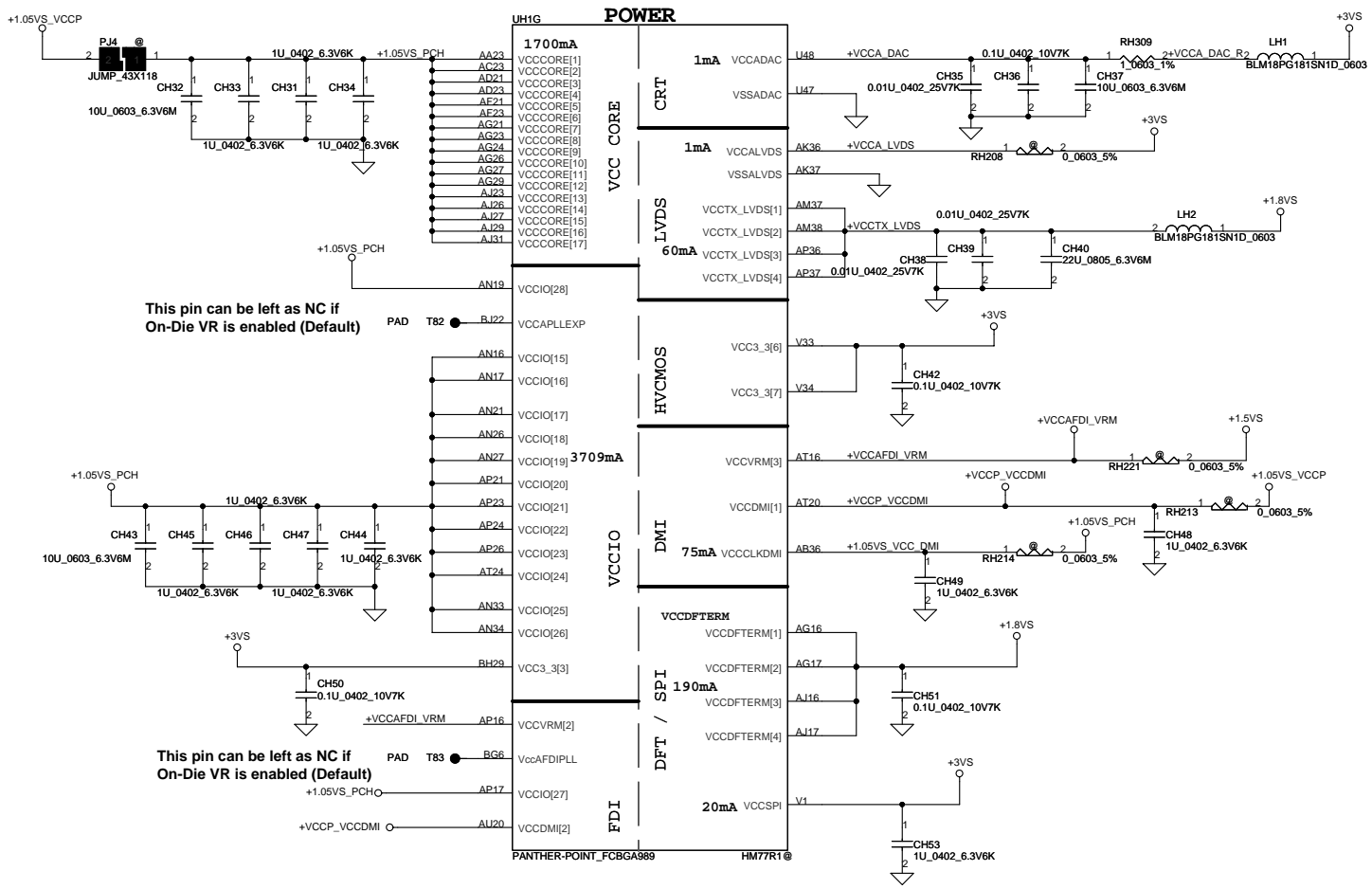
3D_DET#	H	L
SKU	Non3D	3D



DMI & FDI Termination Voltage

NV_CLE	Set to VCC when HIGH
	Set to VSS when LOW

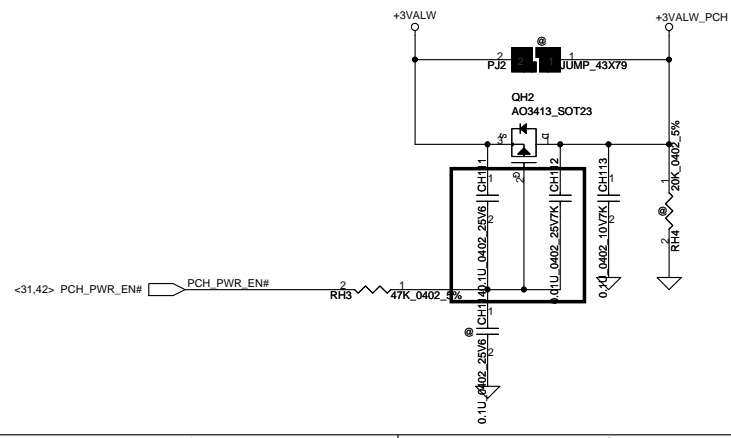




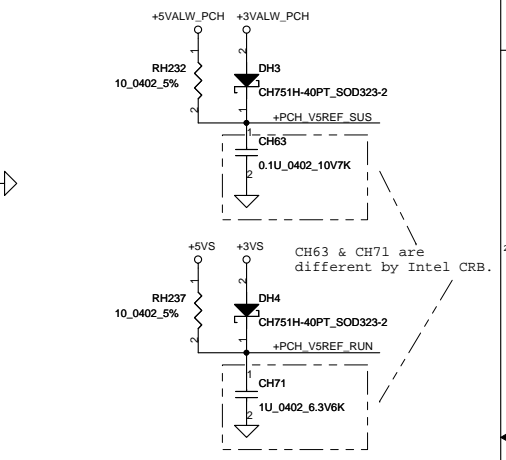
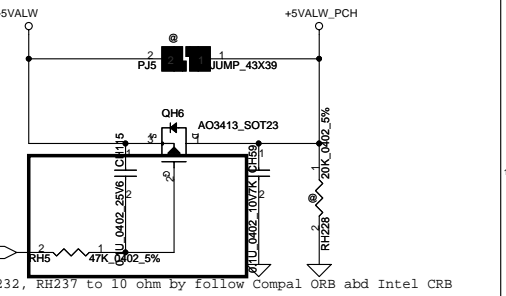
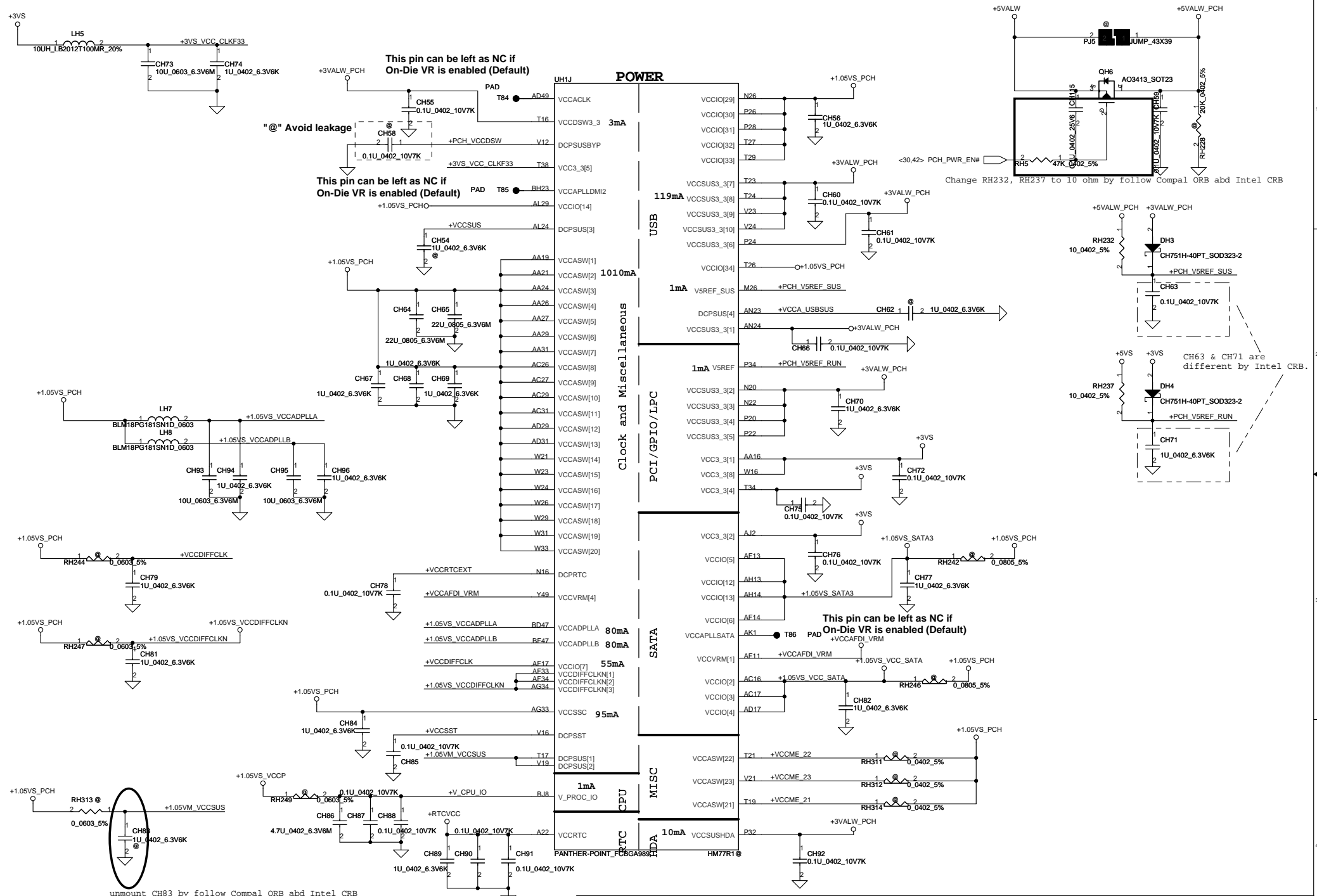
PCH Power Rail Table
Refer to PCH EDS R1.0

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.1	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	N/A
VccSus3_3	3.3	0.095
VccSusHDA	3.3	0.01
VccVRM	1.5	0.167
VccCLKDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

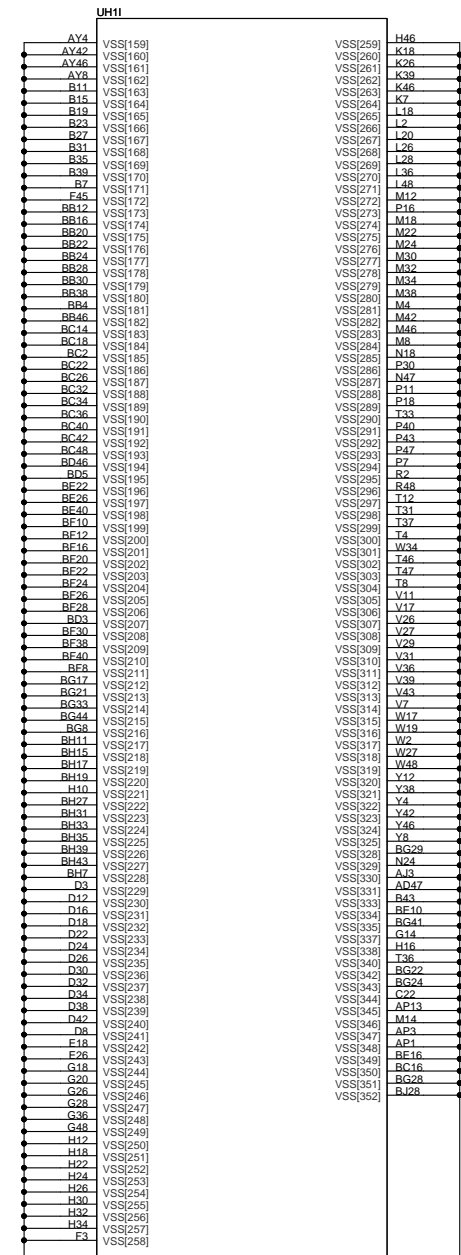
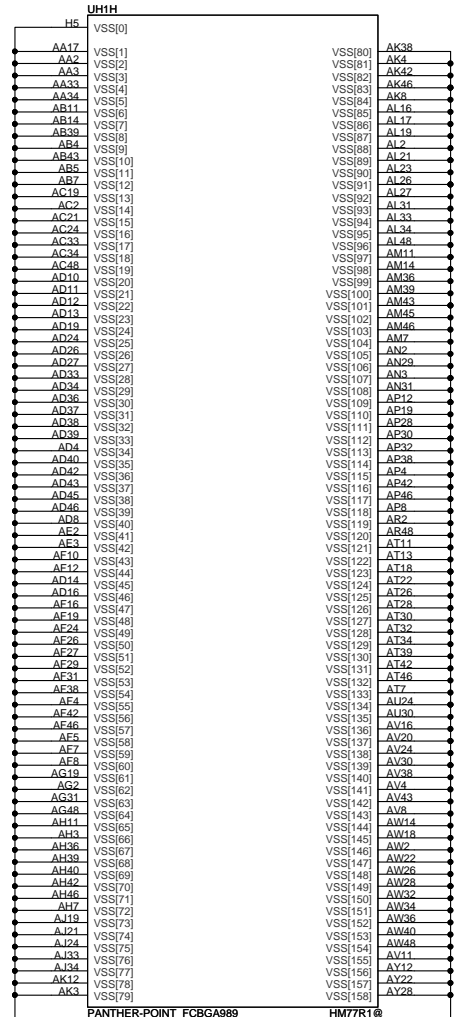
+3VALW to +3V_PCH



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				PCH_POWER-1
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				Date: Tuesday, October 16, 2012
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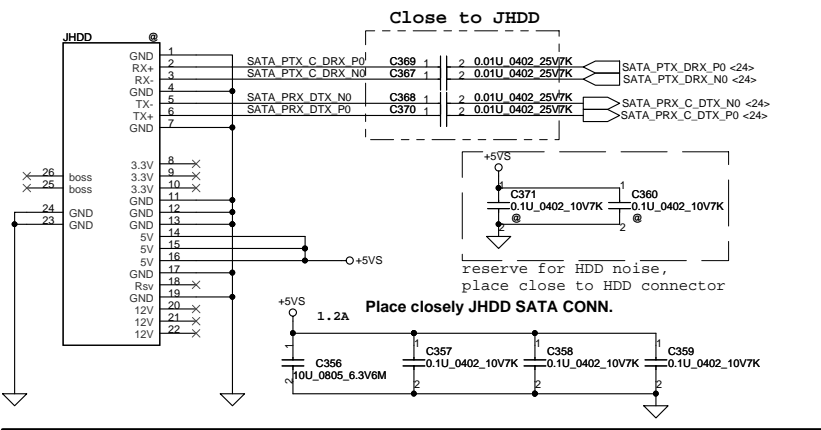


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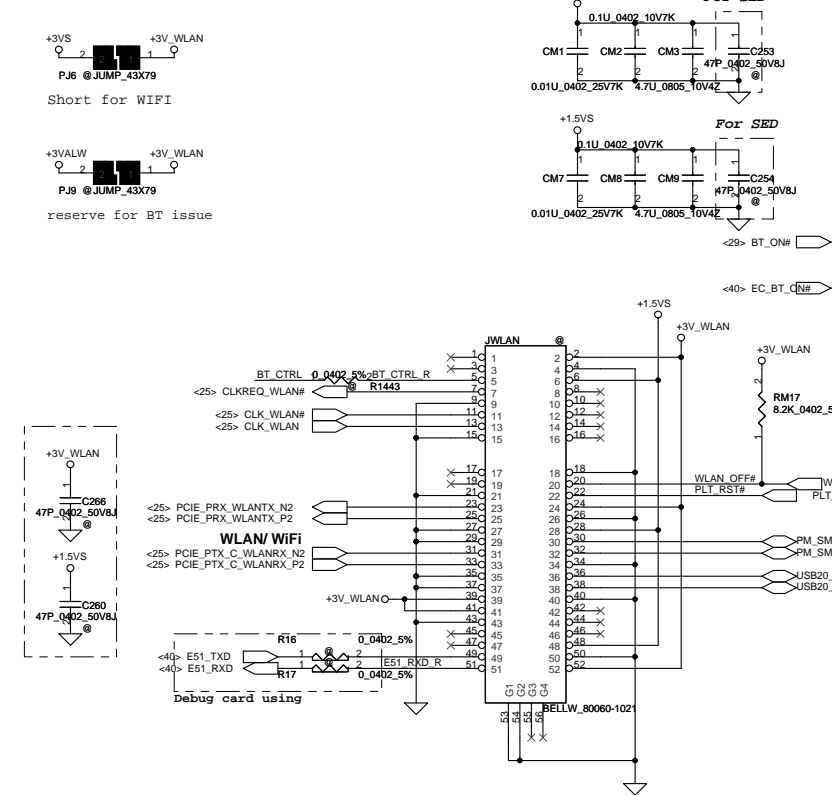
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SATA HDD Conn.

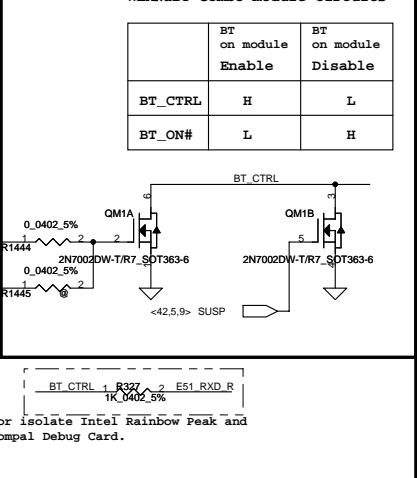


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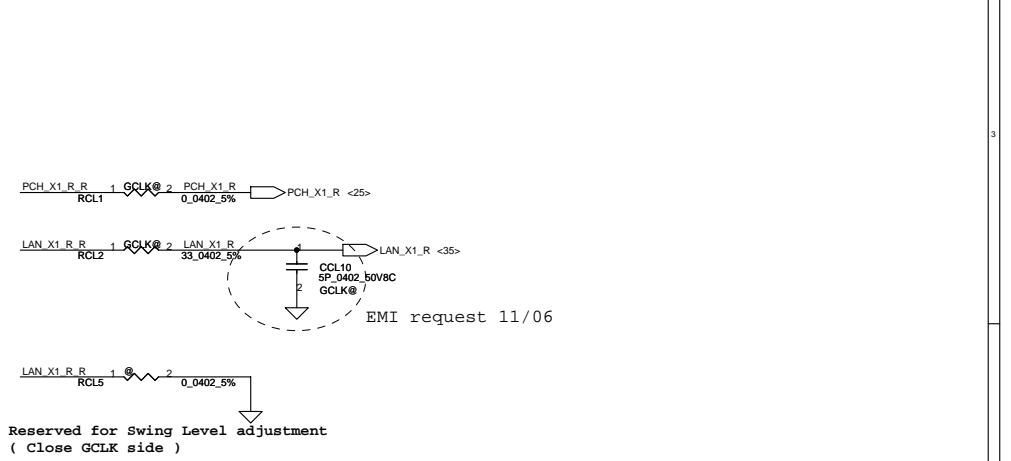
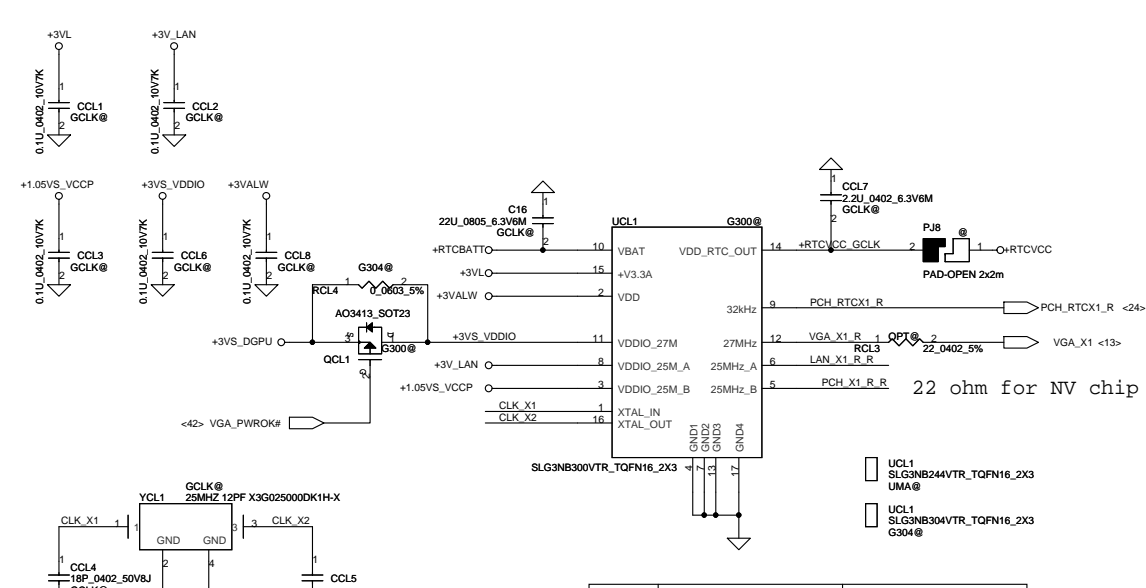
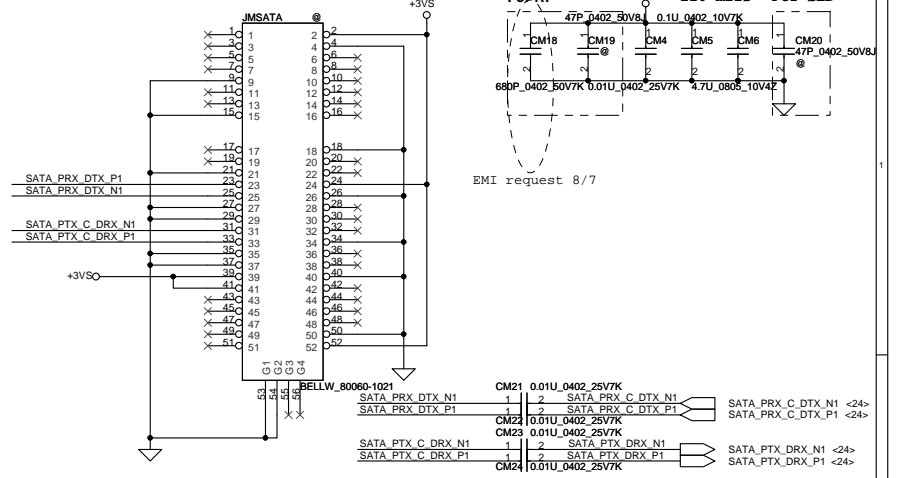
Slot 1 Half PCIe Mini Card-WLAN



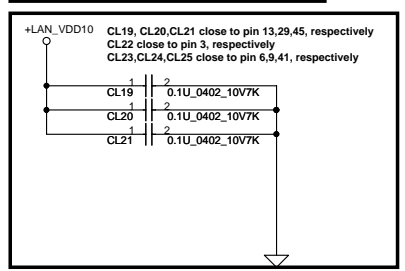
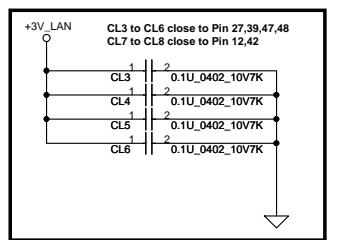
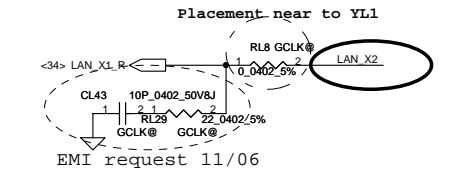
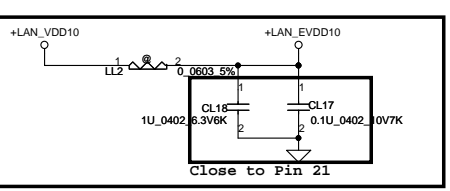
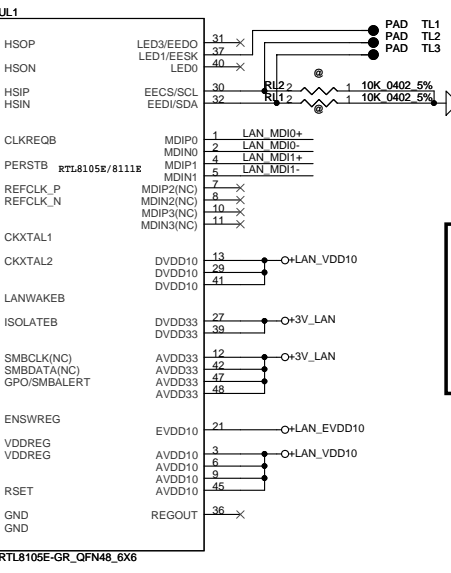
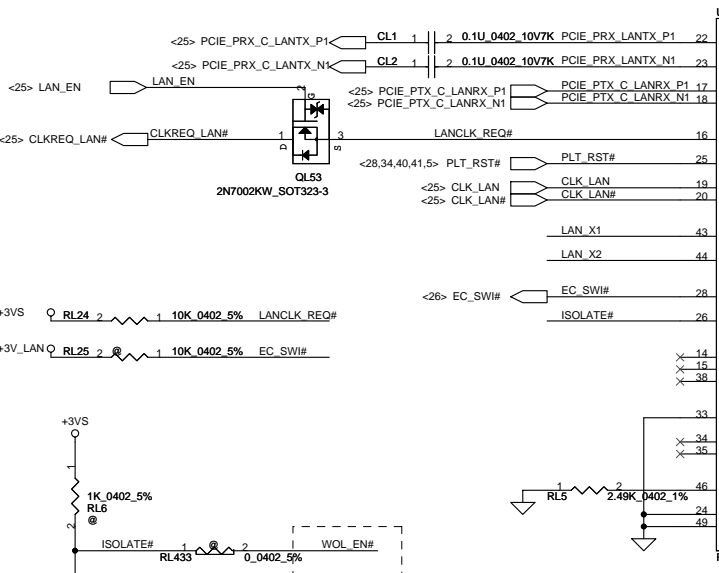
WLAN&BT Combo module circuits



Slot 2 Full PCIe Mini Card- mSATA



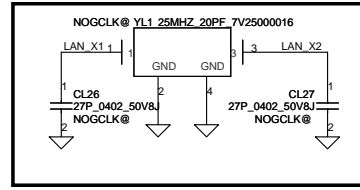
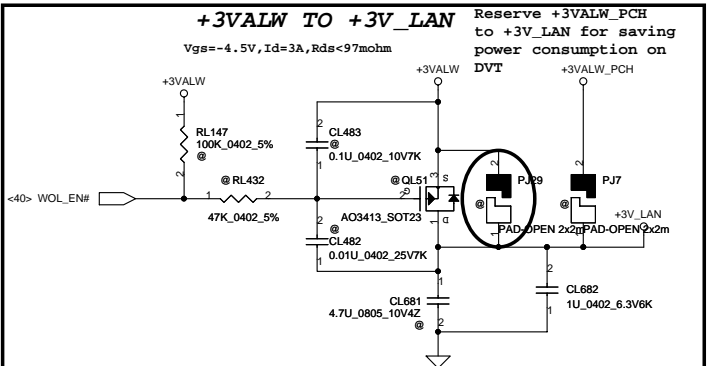
	OPT	UMA
GCLK	300(default) SA00005RS00	244
	304(low power)	SA000057I00



Sx Enable	Sx Disable	S0
Wake up	Wake up	
WOL_EN#	LOW	HIGH

	RTL8105E	RTL8111E/F
Pin14	NC	NC
Pin15	NC	10K ohm PD
Pin38	NC	1K ohm PH

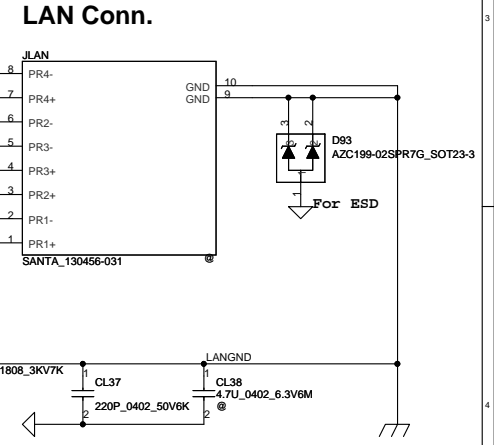
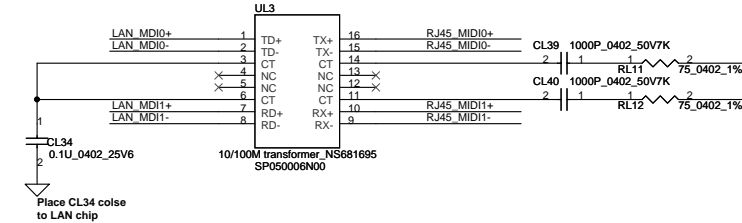
	8105E-VL/VD 8111F/F-VB PWM Mode	8105E-VL/VD LDO Mode
RL4	0 ohm (Pull High)	NC
RL23	NC	0 ohm (Pull Down)

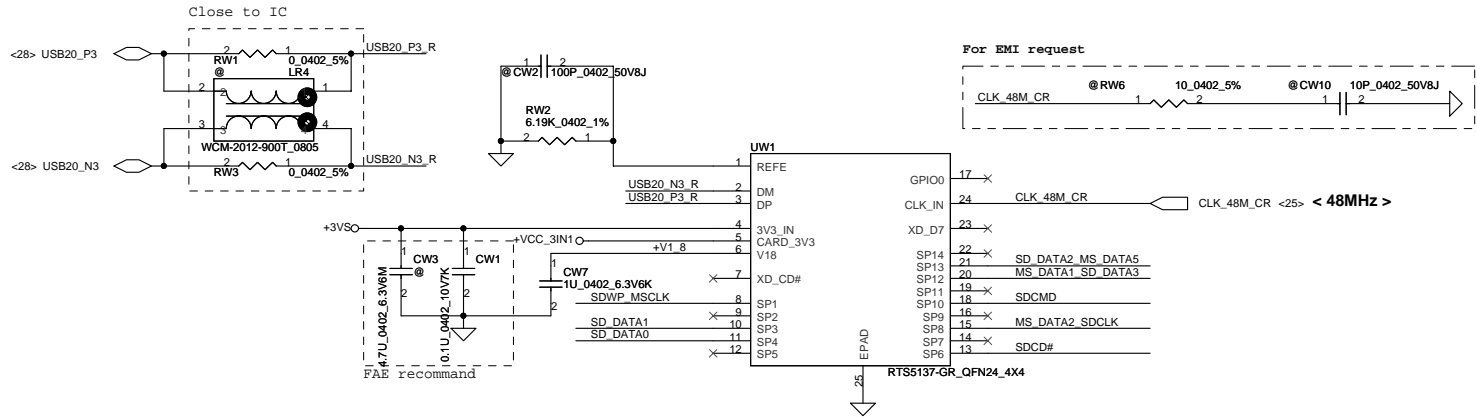


+3V_LAN rising time (10%~90%) need > 1ms and <100ms.

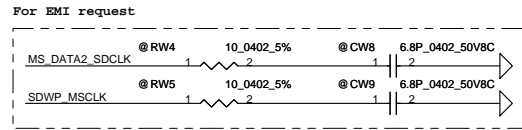
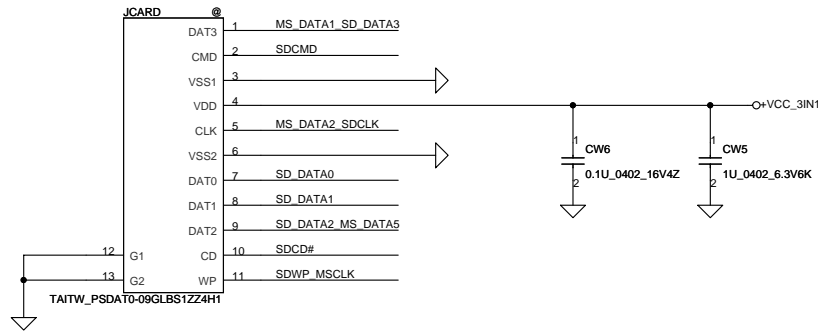
LAN	WOL	LAN_EN		ISOLATEB	
		S0	Sx	S0	Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

*
S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms



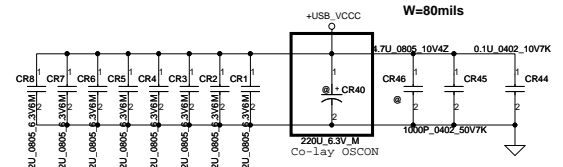
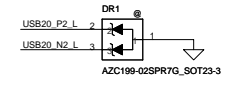
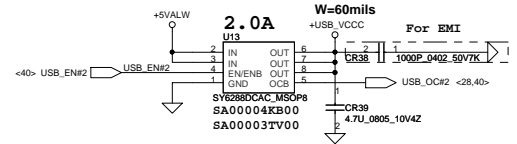
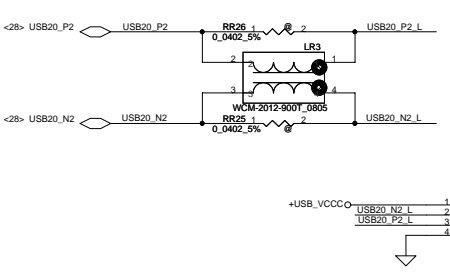


< 2 in 1 Card Reader >



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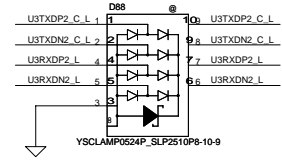
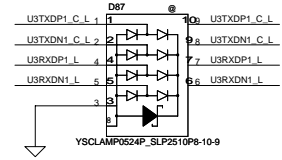
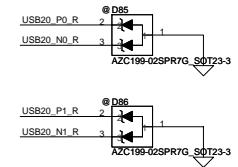
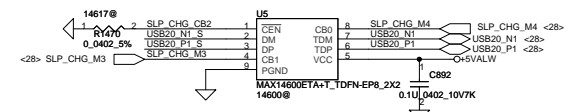
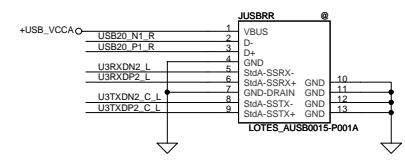
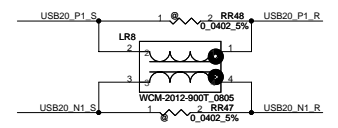
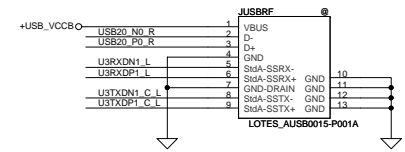
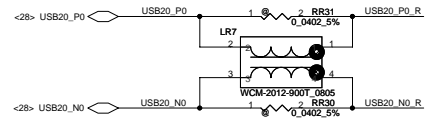
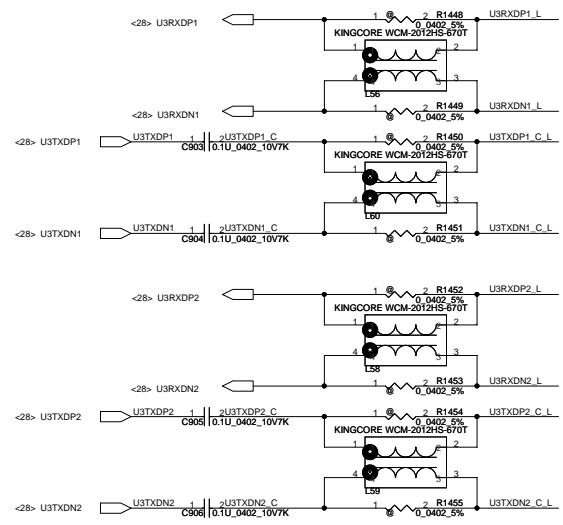
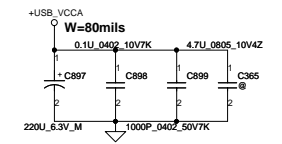
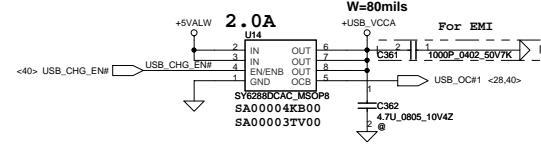
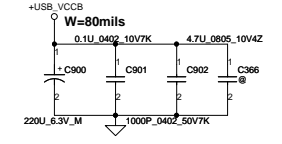
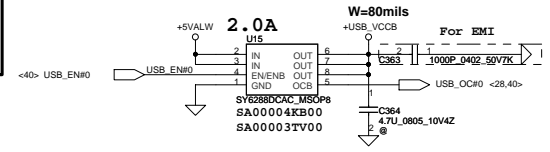
Left USB 2.0 x 1



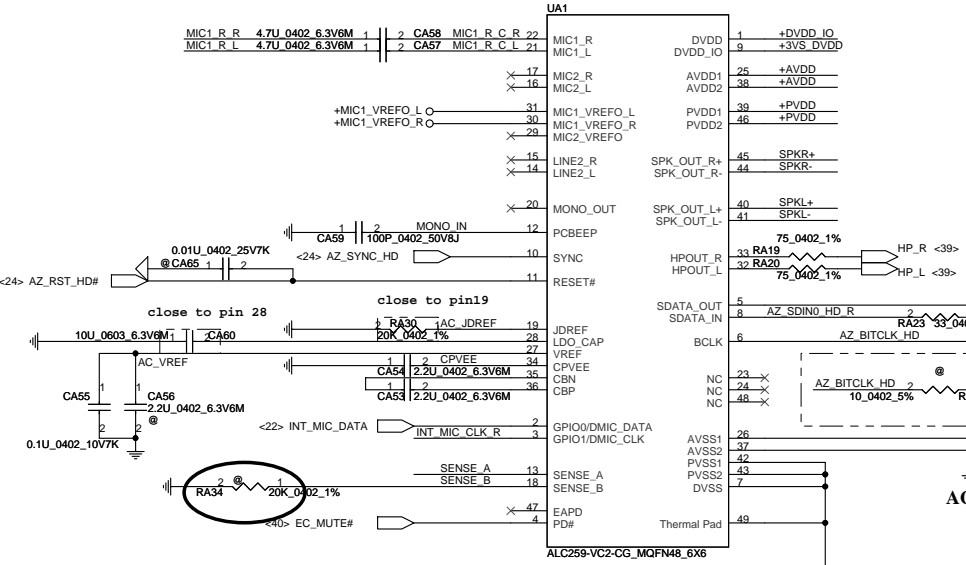
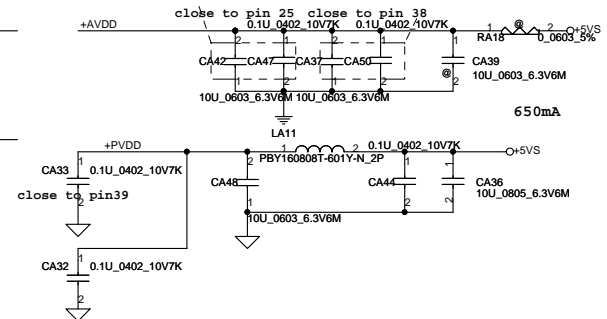
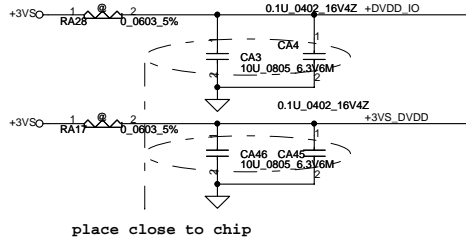
Right side USB 3.0 x 2/ Sleep&Charge

USB Sleep & Charge Auto-Mode/Mode3

MAX14600 & MAX14617			STATUS
CB0 SLP_CHG_M4	CB1 SLP_CHG_M3	CB2 (14617 only)	
0	0	0	AUTO MODE
0	1	0	Force Dedicated charger mode (MODE3)
1	0	0	Pass-Through (USB) Mode: Connect DP/DM to TDRPTDM
1	1	0	Pass-Through (USB) Mode with CDP Emulation: Auto Connect DP/DM to TDRPTDM depending on CDP status
X	X	1	Force Apple 2A Charger Mode: Apple 2A resistor dividers

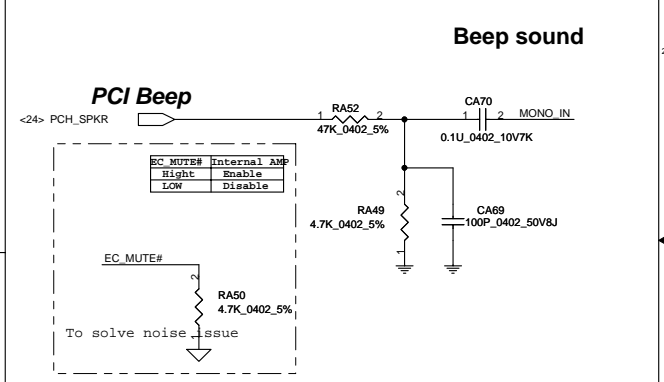
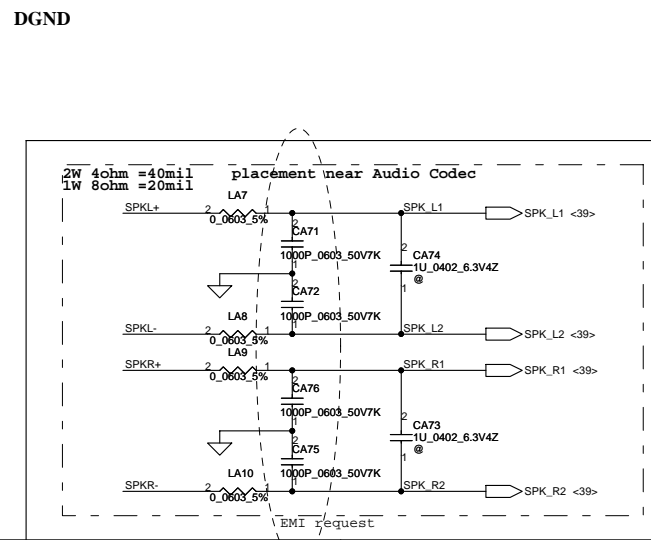


35mA for 3.3V level

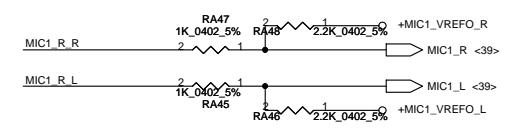


place close to chip

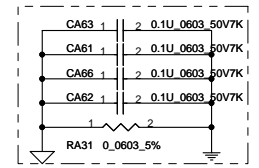
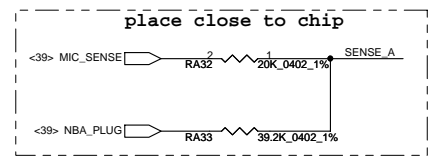
For EMI please place near codec



Ext.MIC/LINE IN JACK

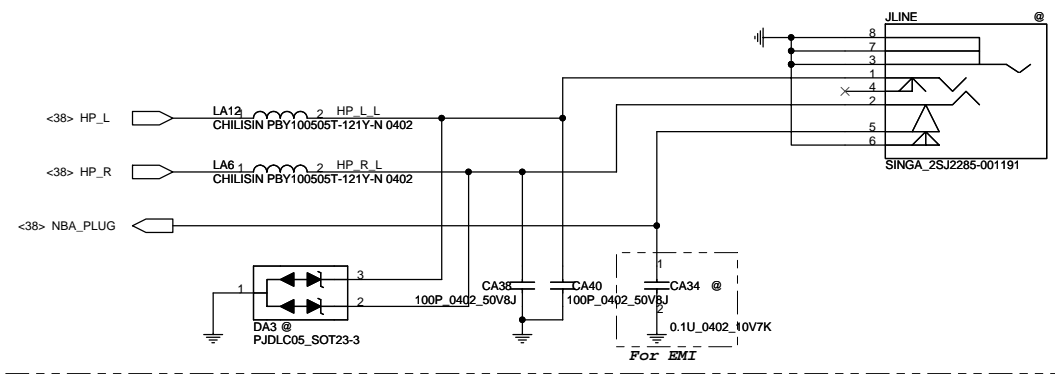


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

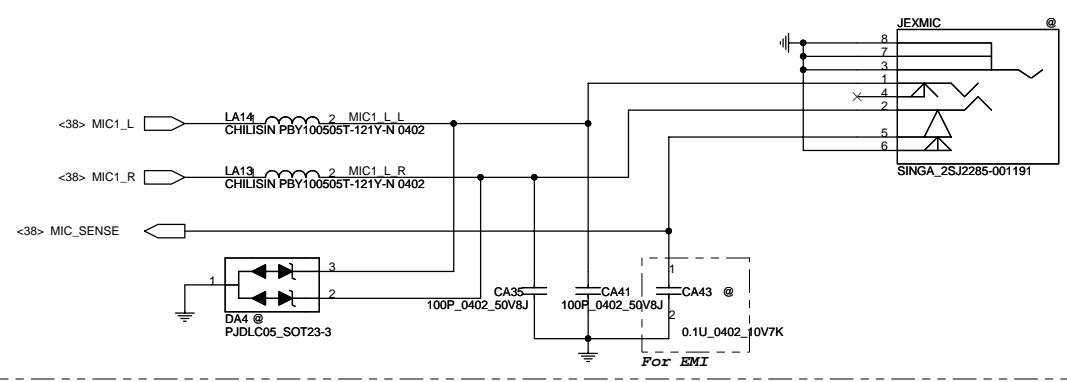


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Date:	Tuesday, October 16, 2012	Sheet	38	of 53

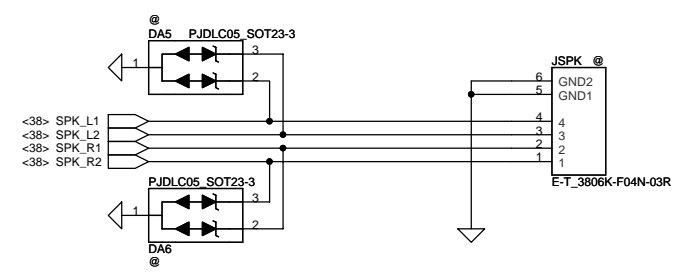
HeadPhone/LINE OUT JACK



EXT.MIC/LINE IN JACK

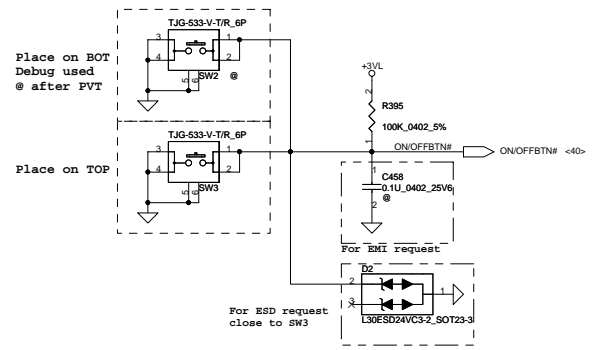


SPK CONN.

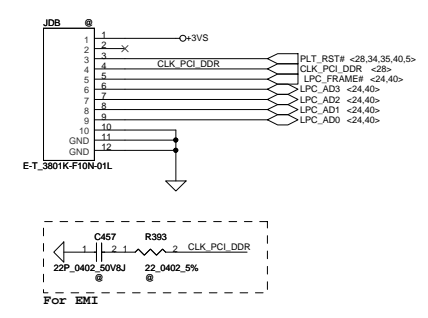


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Issued Date	2012/04/19	Deciphered Date	2015/04/19	AUDIO CONN
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Date:	Tuesday, October 16, 2012	Sheet	39 of 53	

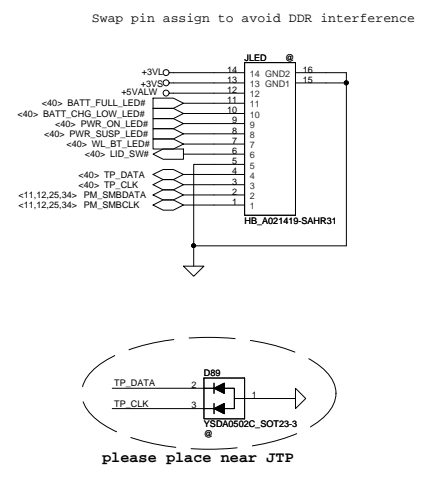
Power Button



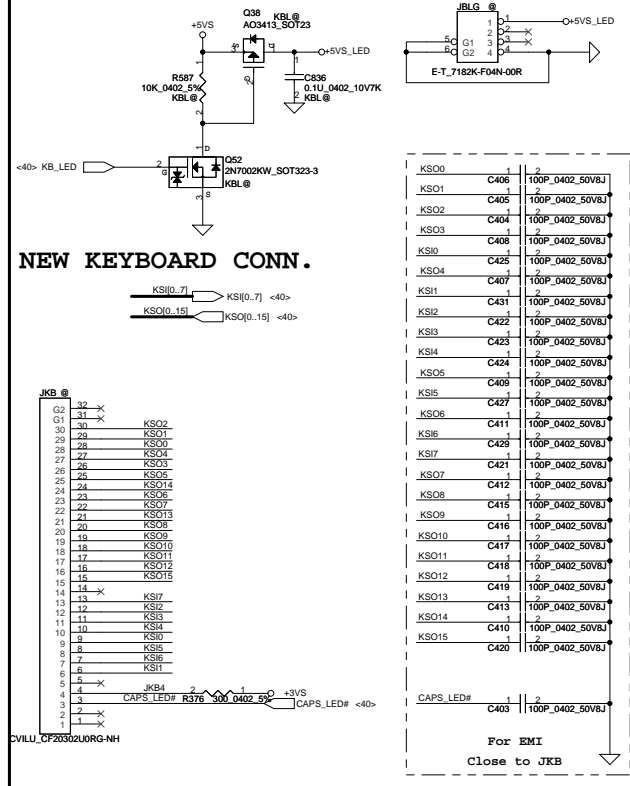
LPC Debug Port



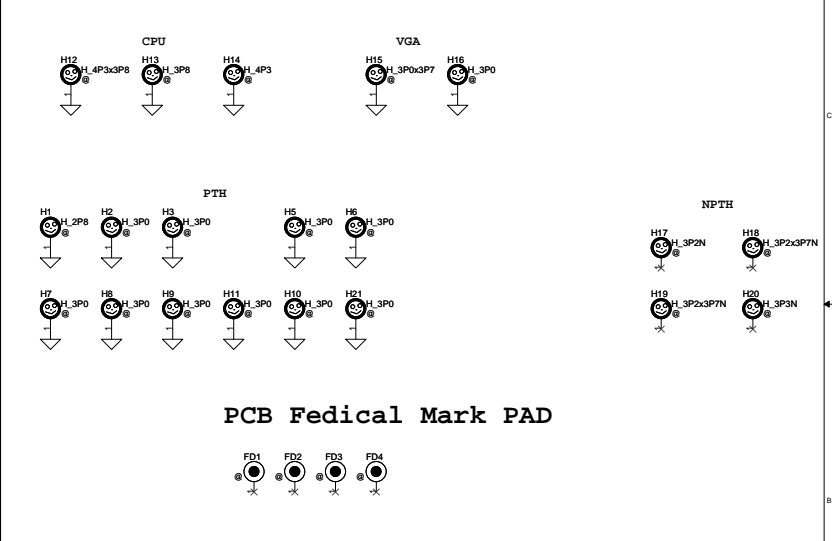
LED/LID/TP SMALL BOARD



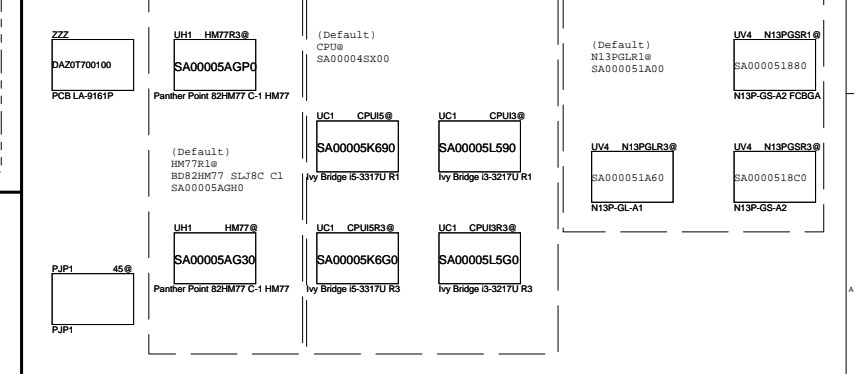
Keyboard LED



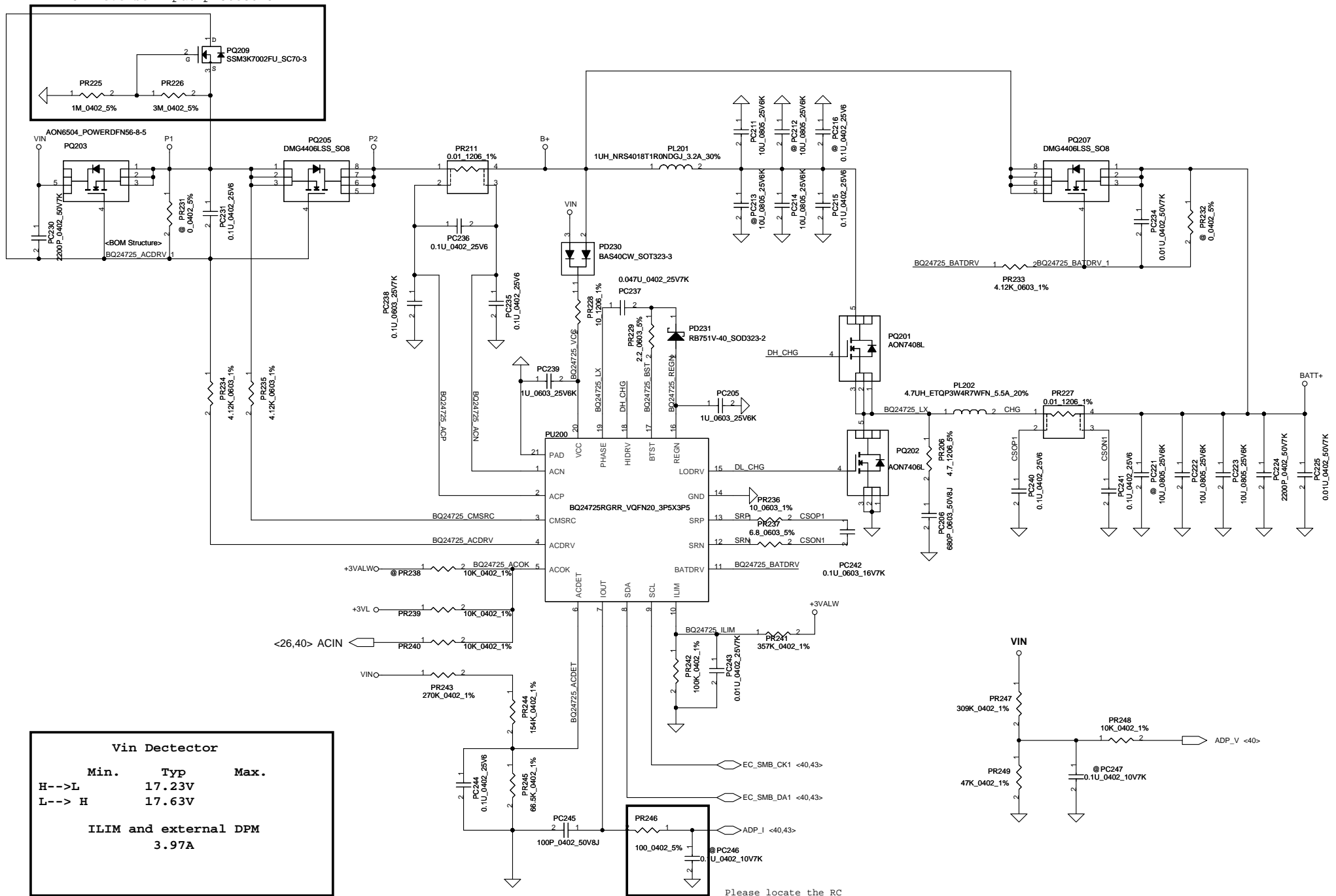
Screw Hole



ISPD



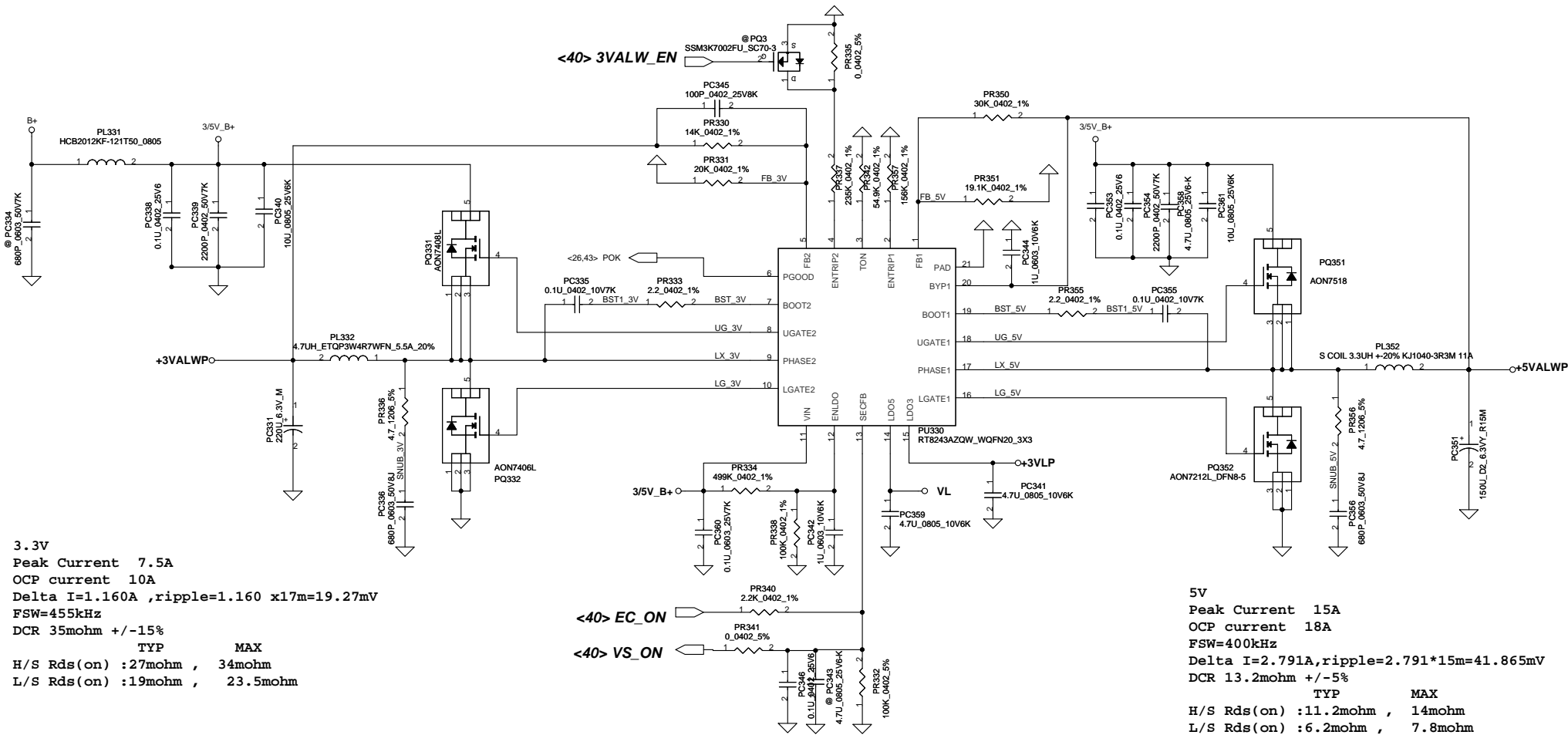
for reverse input protection



Vin Detector			
	Min.	Typ	Max.
H-->L		17.23V	
L--> H		17.63V	
ILIM and external DPM			
3.97A			

Please locate the RC
Near EC chip
2011-02-22

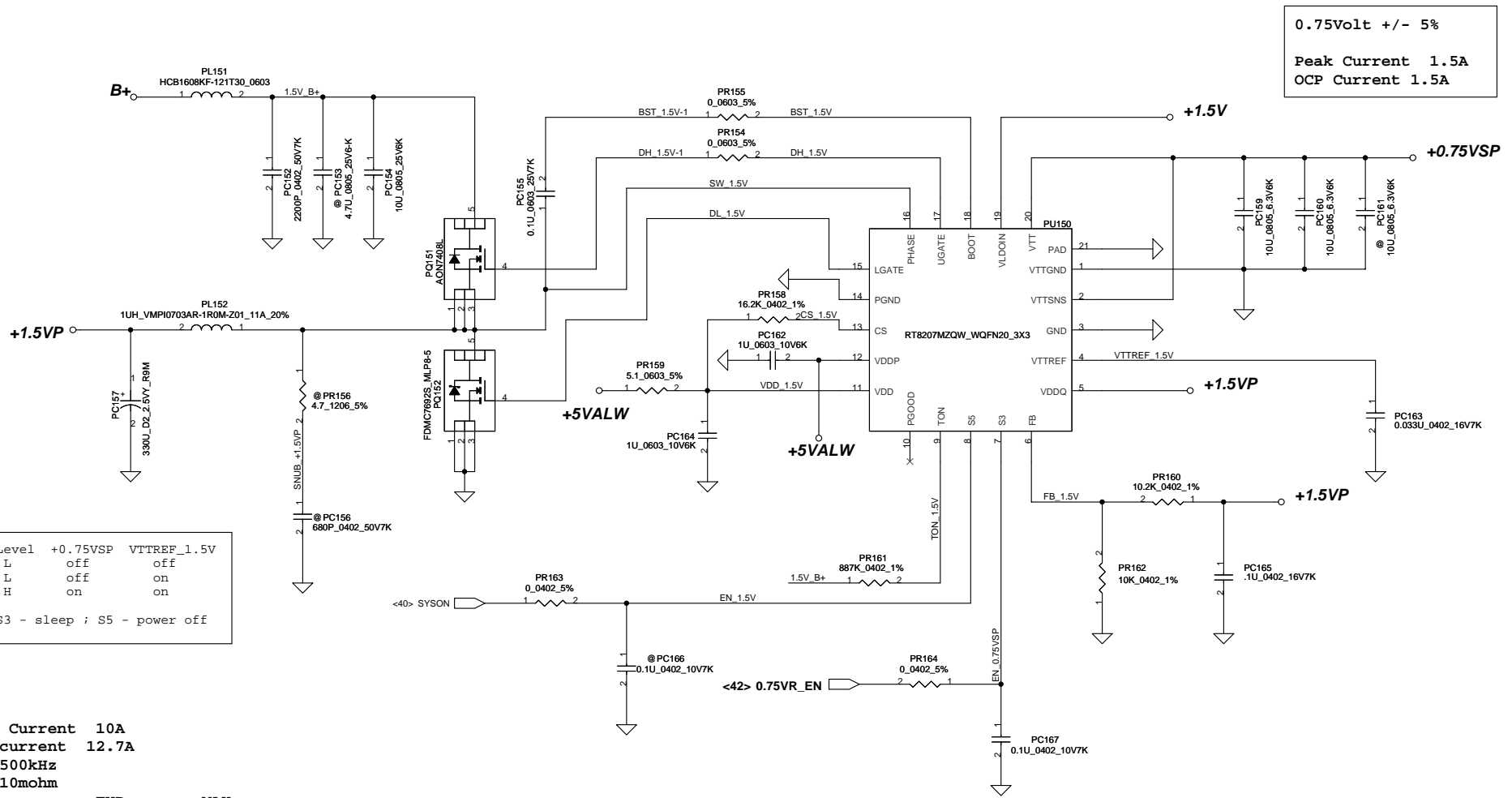
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Document Number	VCUAA			Rev	1.0
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3.3V
 Peak Current 7.5A
 OCP current 10A
 Delta I=1.160A ,ripple=1.160 x17m=19.27mV
 FSW=455kHz
 DCR 35mohm +/-15%
 TYP MAX
 H/S Rds(on) :27mohm , 34mohm
 L/S Rds(on) :19mohm , 23.5mohm

5V
 Peak Current 15A
 OCP current 18A
 FSW=400kHz
 Delta I=2.791A,ripple=2.791*15m=41.865mV
 DCR 13.2mohm +/-5%
 TYP MAX
 H/S Rds(on) :11.2mohm , 14mohm
 L/S Rds(on) :6.2mohm , 7.8mohm

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Issued Date	2012/04/19	Deciphered Date	2015/04/19	Document Number	
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Date:	Tuesday, October 16, 2012	Sheet	45	of	53
Rev					1.0



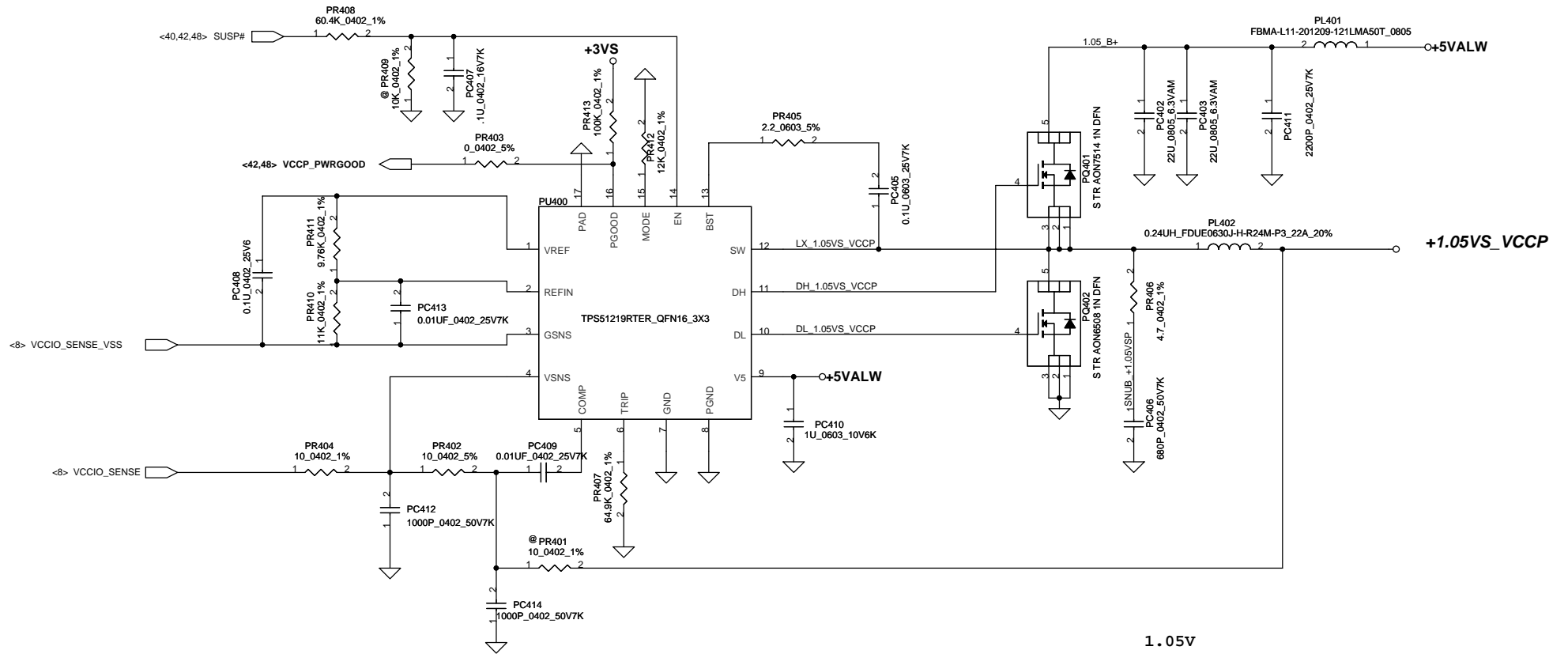
0.75Volt +/- 5%
 Peak Current 1.5A
 OCP Current 1.5A

Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

1.5V
 Peak Current 10A
 OCP current 12.7A
 FSW=500kHz
 DCR 10mohm

	TYP	MAX
H/S Rds(on)	:27mohm	, 34mohm
L/S Rds(on)	:9.6mohm	, 13mohm



1.05V
 Peak Current 14A
 OCP current 15.08A
 FSW=300kHz
 Delta I=5.883A, Rippe=5.883x 4.5m=26.473mV
 DCR 3.7ohm +

	TYP	MAX
H/S Rds(on)	: 5.6mohm	, 6.8mohm
L/S Rds(on)	: 3.7mohm	, 5mohm

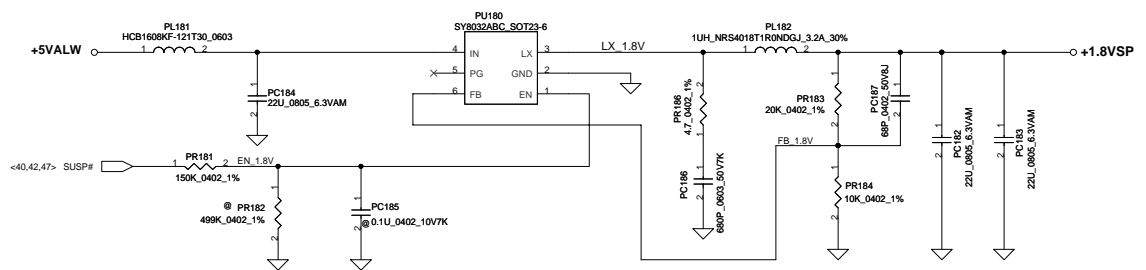
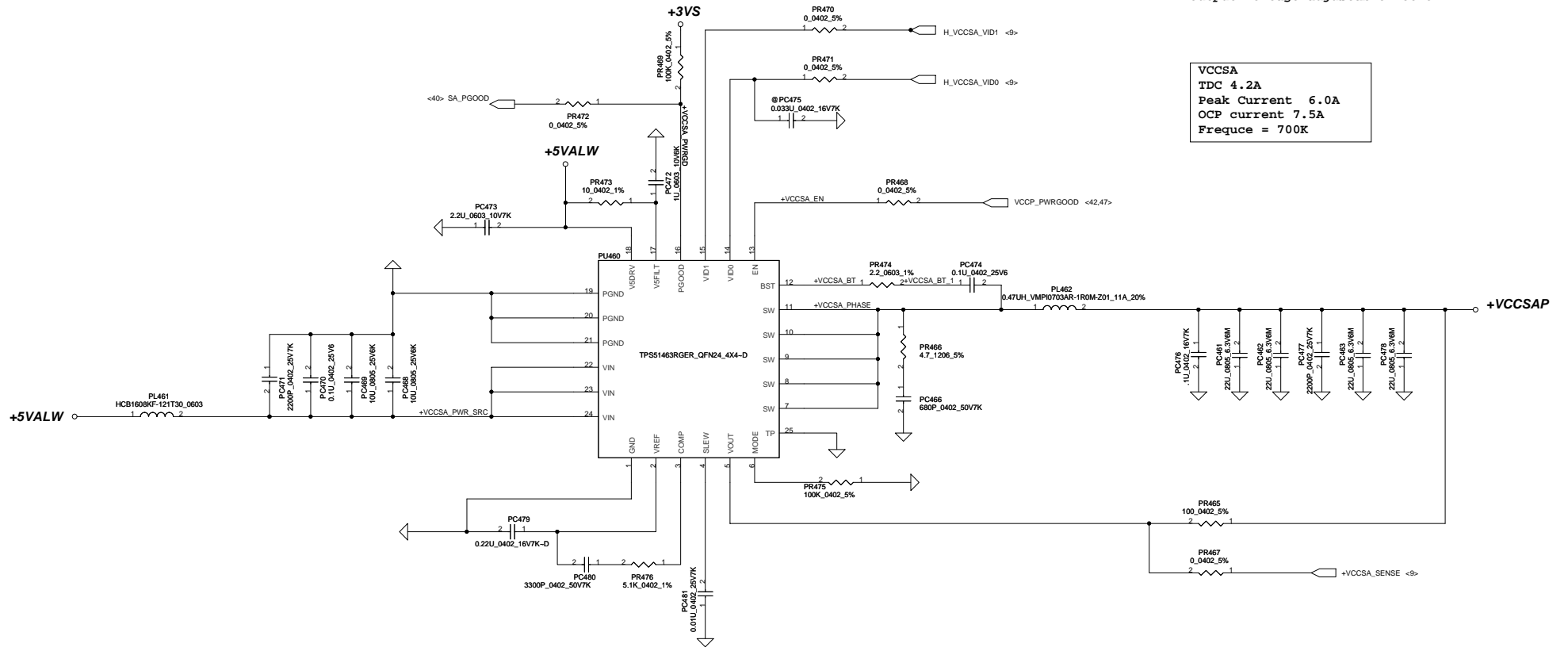
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				Custom	1.0
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Date:				Tuesday, October 16, 2012	Sheet 47 of 53

The 1k PD on the VCCSA VIDs are empty.
These should be stuffed to ensure that
VCCSA VID is 00 prior to VCCIO stability.

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.750V

output voltage adjustable network

VCCSA
TDC 4.2A
Peak Current 6.0A
OCP current 7.5A
Freque = 700K

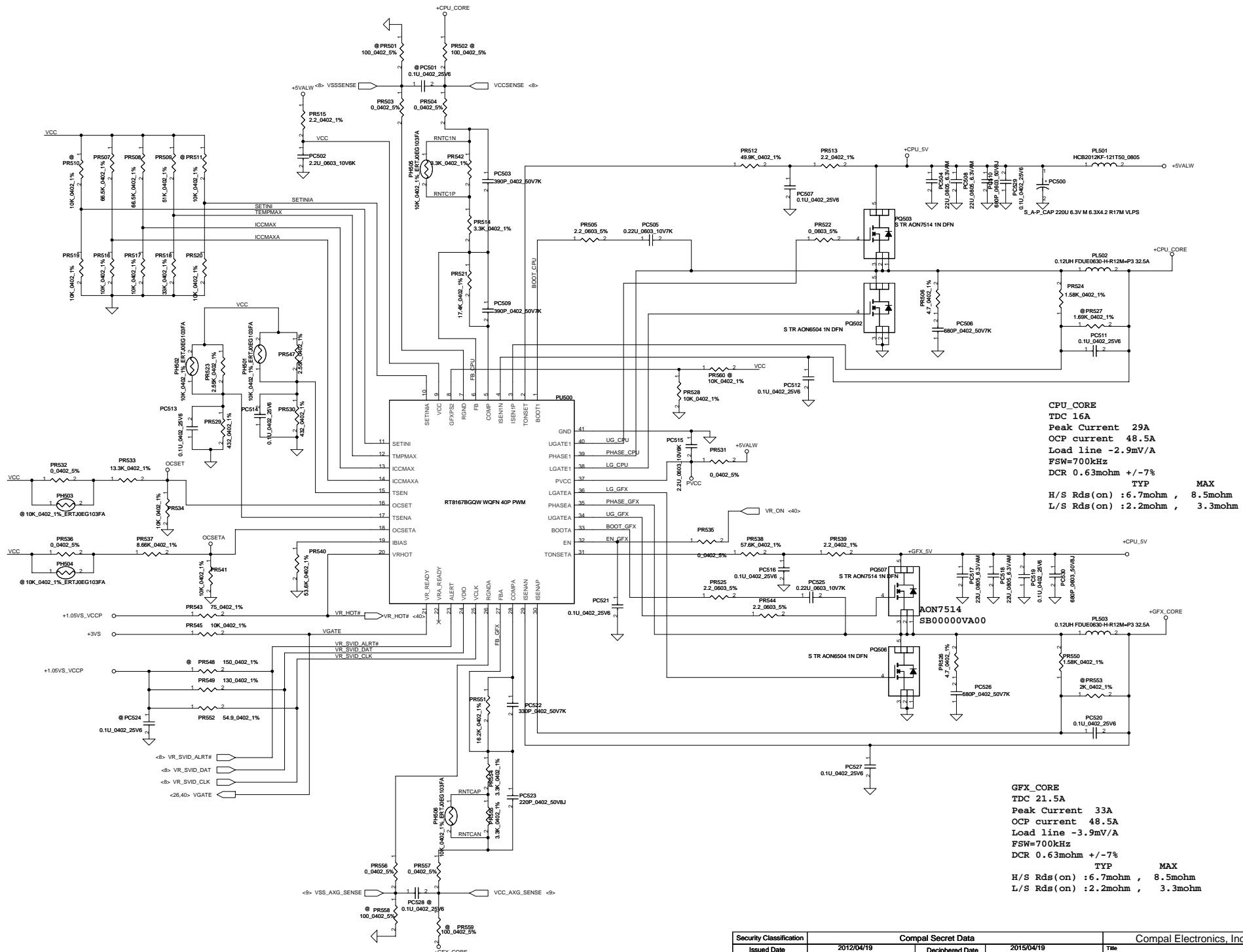


VCCSA
Peak Current 1.54A
OCP current 1.078A

DELL CONFIDENTIAL/PROPRIETARY

123	
File	PWR-VCCSAP/1.8VSP
Size	Document Number
VCUAA	
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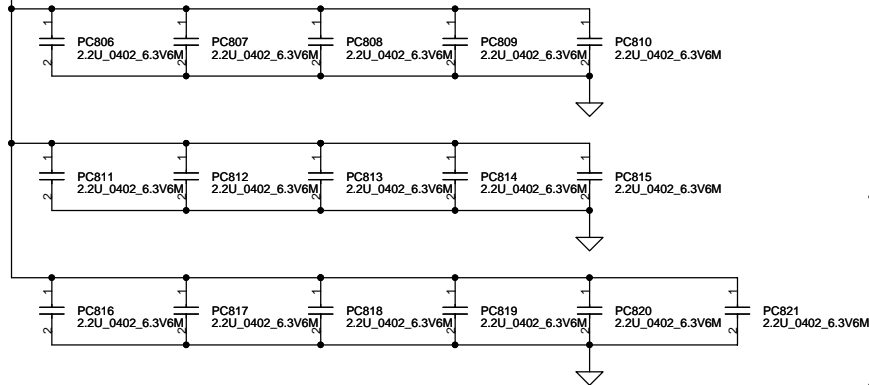


CPU_CORE
 TDC 16A
 Peak Current 29A
 OCP current 48.5A
 Load line -2.9mV/A
 FSW=700kHz
 DCR 0.63mohm +/-7%
 TYP
 H/S Rds(on) : 6.7mohm , 8.5mohm
 L/S Rds(on) : 2.2mohm , 3.3mohm

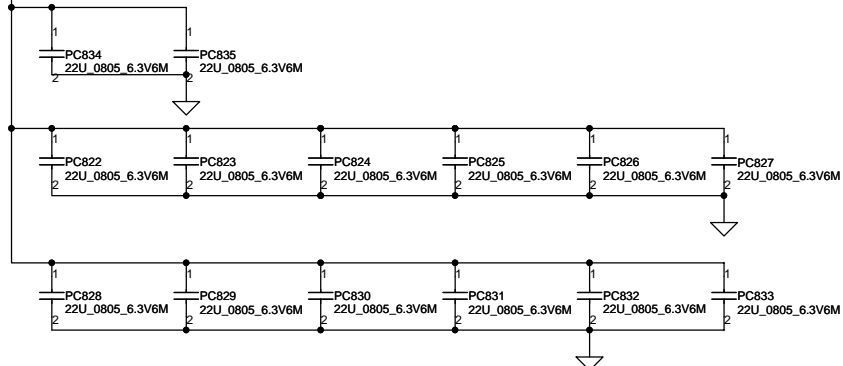
GFX_CORE
 TDC 21.5A
 Peak Current 33A
 OCP current 48.5A
 Load line -3.9mV/A
 FSW=700kHz
 DCR 0.63mohm +/-7%
 TYP
 H/S Rds(on) : 6.7mohm , 8.5mohm
 L/S Rds(on) : 2.2mohm , 3.3mohm

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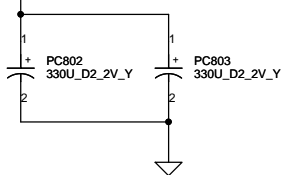
+CPU_CORE



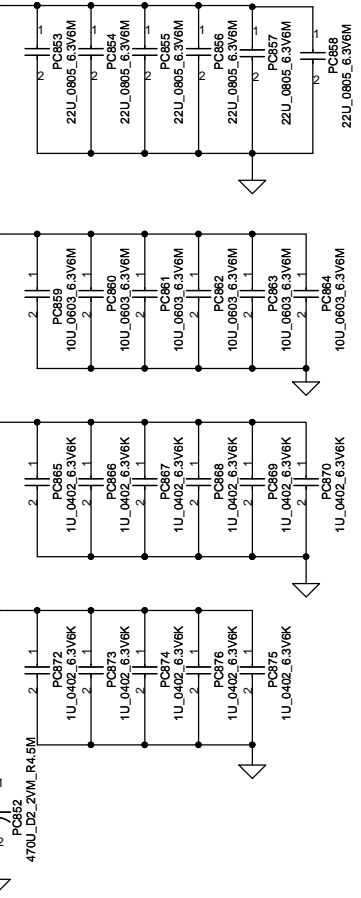
+CPU_CORE



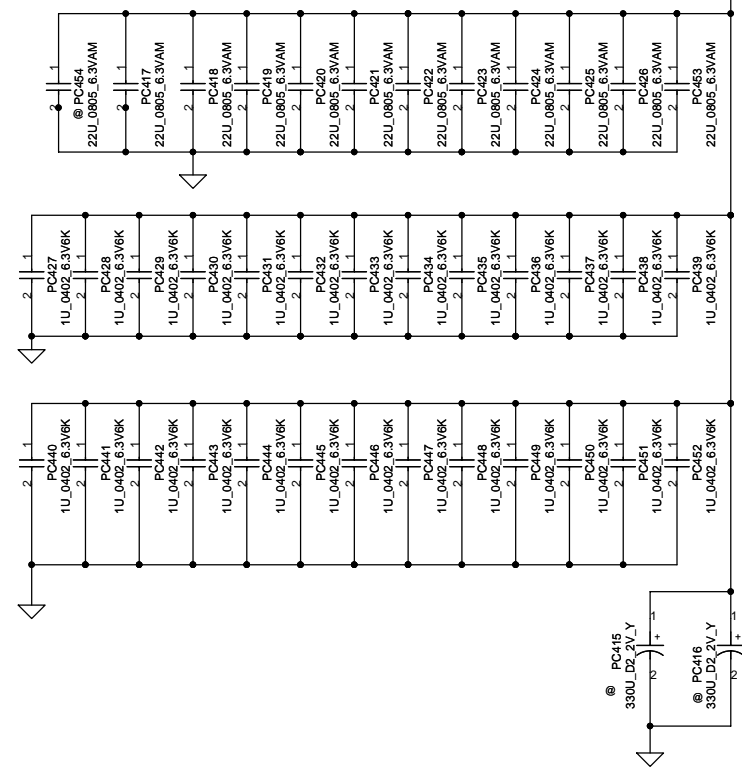
+CPU_CORE



+GFX_CORE



+1.05VS_VCCP

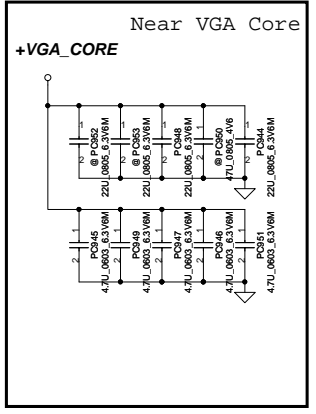
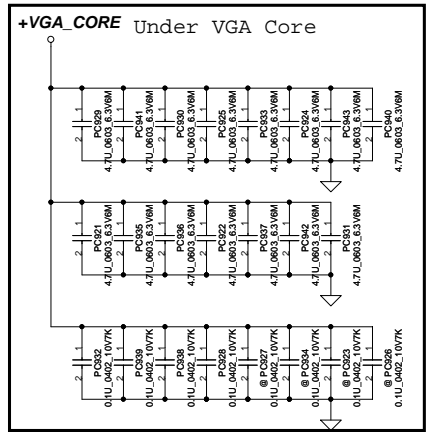
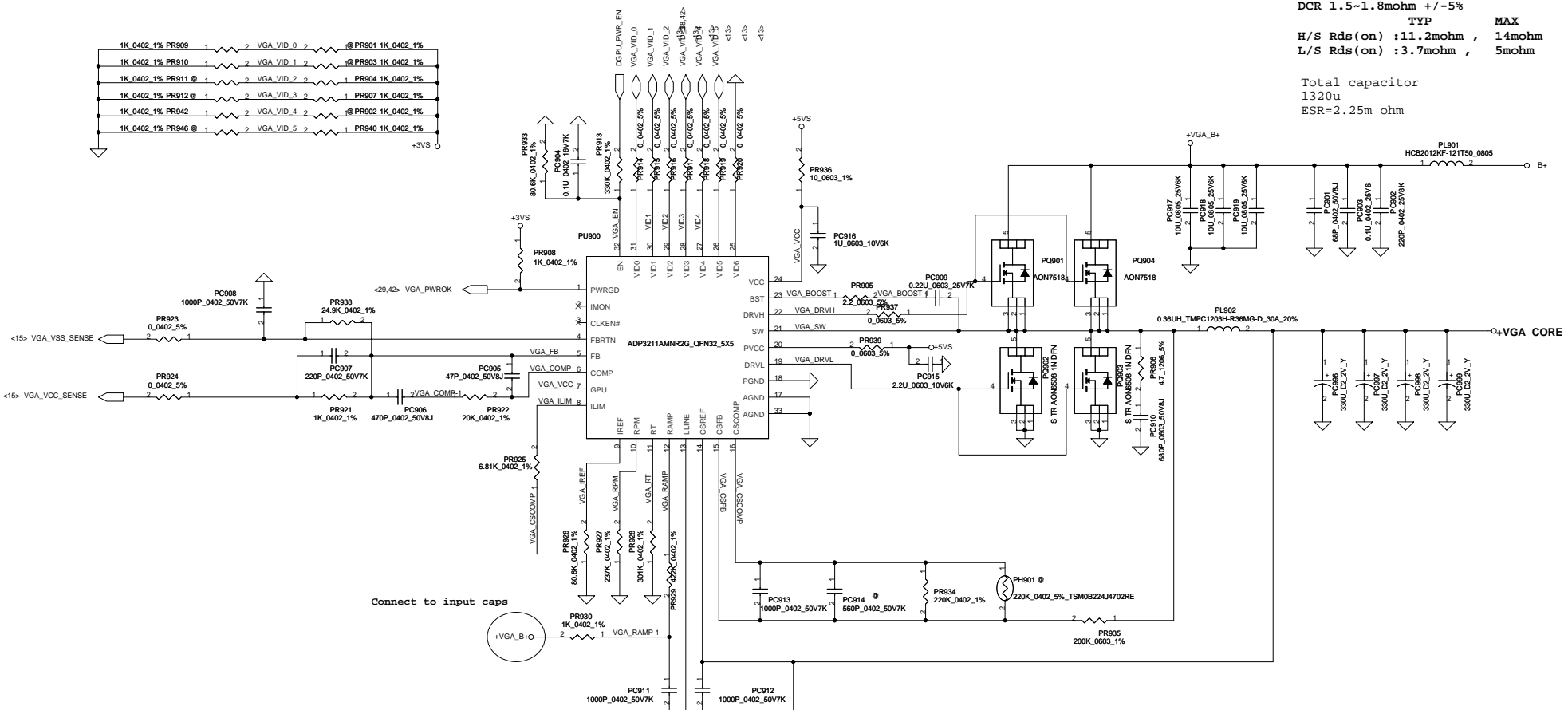


Chief River ULV	330uF*9m	22uF	10uF	2.2uF	1uF
CPU	2	14		16	
GFX_CORE	1	6	6		11
1.05V_VCCP	2		11		26

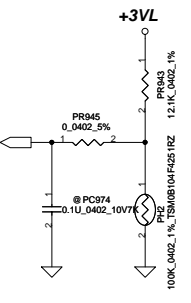
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VGA_Core
 TDC 35A
 Peak Current 42A
 OCP current 65A
 Load line -
 FSW=300kHz
 DCR 1.5-1.8mohm +/-5%
 TYP MAX
 H/S Rds(on) :1.1.2mohm , 14mohm
 L/S Rds(on) :3.7mohm , 5mohm

Total capacitor
 1320u
 ESR=2.25m ohm



PR931	PR932	LL
0	0	X
0	0	V



Item	Reason for change	PG#	Modify List	Date	Phase
1	HW command (Follow QFKAA)	45	change PR330 13K to 14K	2012/5/17	DVT
2	HW command (Follow QFKAA)	45	change PR351 20K to 19.1K	2012/5/17	DVT
4	fine tune 1.5V ocp =12.6A	46	change PR158 13.3K to 16.2K	2012/5/17	DVT
5	fine the 1.05V vout volatge=1.059V	47	change PR411 10.5K to 9.76K	2012/5/17	DVT
6	fine tune the CPU load line =2.7mV	49	change PR521 14.3K to 17.4K	2012/5/17	DVT
7	fine tune the GFX load line =3.7mV	49	change PR551 10.5K to 16.2K	2012/5/21	DVT
8	fine tune the GFX load line =3.7mV	49	change PC522 560P to 330P	2012/5/21	DVT
9	fine tune the GFX OCP setting	49	change PR537 13.3K to 8.66K	2012/5/21	DVT
10	purchaser command for cost down plane	48	change PU460 SY8037D to TPS51463	2012/5/22	DVT
11	for 1.05V high frequence change to remote sense	47	add PR402 reserve PR401	2012/5/24	DVT
12	for 1.05V high frequence	47	change PR412 100k to 12K	2012/5/24	DVT
13	change the same solution for 2nd sourced	44	change PQ203 TPCA8057 to AON6504	2012/5/24	DVT
14	change the same solution for 2nd sourced	44	change PR227 with the same PR211	2012/5/25	DVT
15	change the same solution for 2nd sourced	46	change PC157 with the same PC996	2012/5/25	DVT
16	fine tune 1.05V vout volatge=1.059V	47	change PR410 12K to 11K	2012/5/25	DVT
17	fine tune the CPU DCR sense	49	change PR538 49.9K to 57.6K	2012/5/25	DVT
18	fine tune the CPU DCR sense	49	change PR550 1.13K to 1.58K	2012/5/25	DVT
19	fine tune the 5V OCP=18A	45	change PR357 120K to 133K	2012/5/25	DVT
20	fine tune 3.3V OCP =10A	45	change PR337 120K to 200K	2012/5/25	DVT
21	for 1.05V high frequence	47	change PL402 0.47u to 0.24u	2012/5/25	DVT
22	for 1.05V high frequence	47	Reserve the PC415 and PC416	2012/5/25	DVT
23	change the 3v/5v IC version	45	change the PU330 RT8243B to RT8243A	2012/5/25	DVT
24	change 1.5V chokethe same part number with PL462	46	change the PL152 SH00000GJ00 to SH00000KS00	2012/5/25	DVT
25	change 1.05V high frequence OCP=16.5A	47	change the PR407 75K to 64.9K	2012/5/25	DVT
26	change charger current =3.46A	48	change the PR241 150 Kto 357K		
27	change the PF2 for design change	43	change the PF2 8A to 10A		

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HW PIR (Product Improve Record)

VCUAA LA-9161P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.3 TO 1.0

Item	Page	Date	Request	Solution
1)	24	2012/7/23A	Change RTCBATT power rail from GCLK to original design	DH1 mount always
2)	24	2012/7/23A	remove BIOS socket	UH3 mount always
3)	41	2012/7/23A	remove debug SW	Change SW2 to @
4)	38	2012/7/26A	EMI request	CA71,CA72,CA75,CA76 mount SE025102K80/1000pF
5)	41	2012/8/3A	Update JBLG footprint	Change JBLG footprint to E-T_7182K_F04N-00R_4P
6)	41	2012/8/3A	Update H20	Change H20 from 3P8 to 3P3 size
7)	05	2012/8/6C	remove JTAG for ESD request	remove T5, T8, T9, T10, T11, T12, T13, T14, T15, T16, T17
8)	42	2012/8/6D	ESD request	mount C20,C21,C28,C30,C32,C33,C36,C37,C38,C39,C40; add C44 on SUSP
9)		2012/8/6D	Change footprint of 0ohm to Short_pad	Change location: LL2, R1, R16, R17, R388, RA17, RA18, RA28, RB1,RB32, RB34, RC119, RC183, RC73, RC88, RC92, RC94, RC95, RH128, RH208, RH213, RH214, RH221, RH242, RH244, RH246, RH247, RH249, RH25, RH286, RH311, RH312, RH314, RL433, RV182, RV80, RV81
10)	41	2012/8/6D	Change PCB PN	Change to DAZ0T700100
11)	34	2012/8/6D	EMI request	Change CM18 from 47pF to 680pF
12)	42	2012/8/6D	EMI request	Add C1(680pF) on +GFX_CORE, place close to CPU

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